

# GM6B Studio Intel UMA and Discrete GFX

VER : 1A  
PWA:  
PWB:

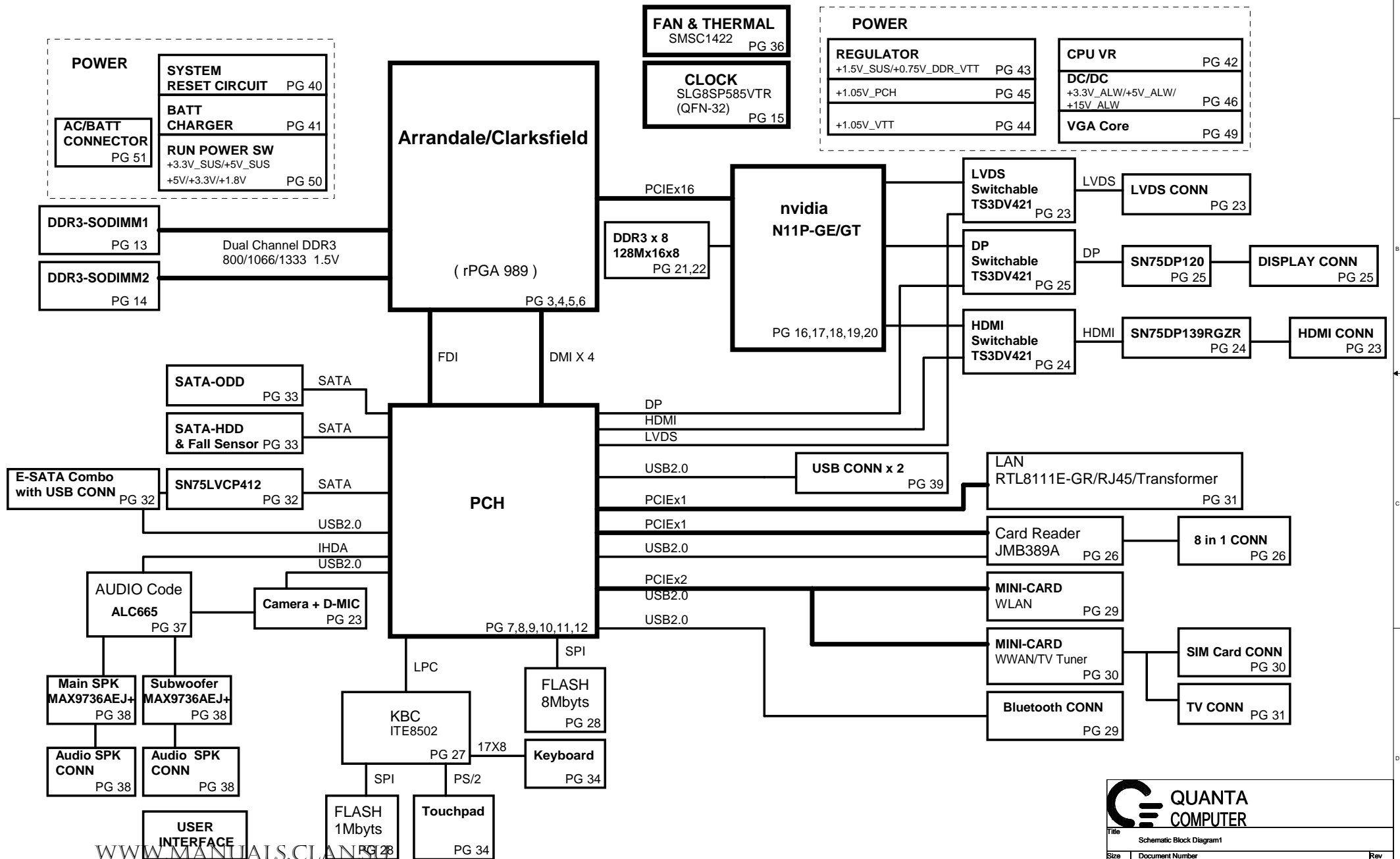




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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0-S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0-S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0-S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0-S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

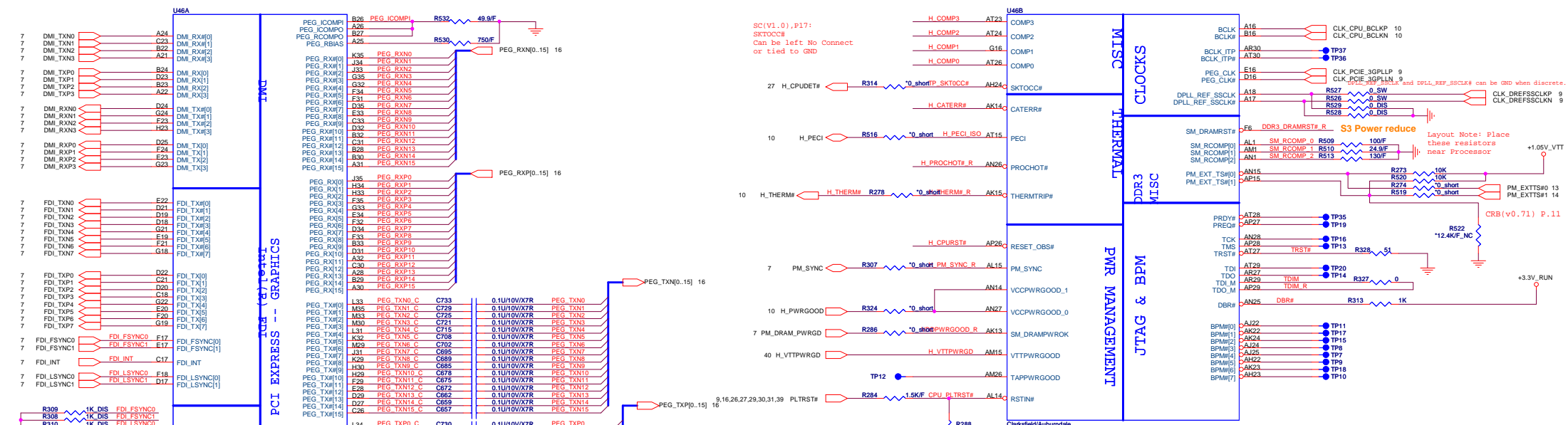
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



**QUANTA  
COMPUTER**

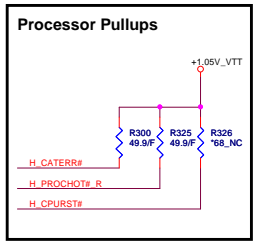
Title: Index & Power Status

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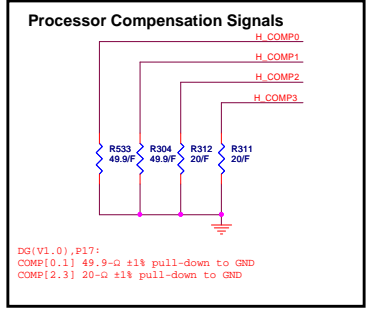
DG(V1.5),P8: FDI\_INT should be tied to GND (through 1K  $\pm 5\%$  resistors), if these signals are left floating, there are nonfunctional impacts but a small amount of power (~15 mW) maybe wasted.  
 DG(V1.5) P8:  
 FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1] can be ganged together with one resistor[1K  $\pm 5\%$  resistors].

RSTIN#:  
 DG(V1.11)(Doc.# 414044),P10:  
 Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

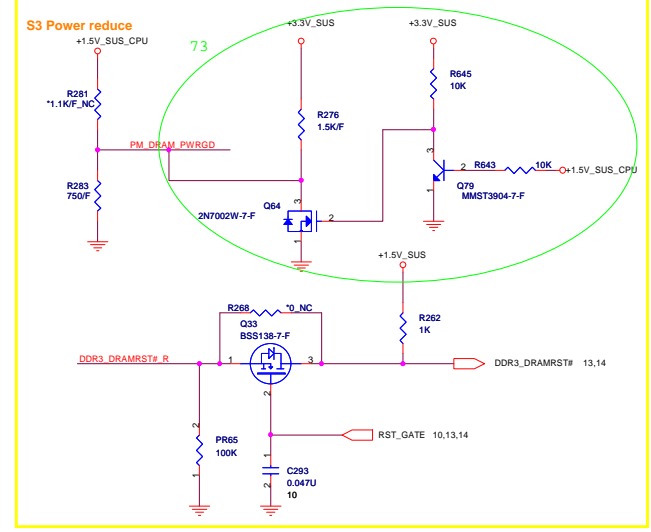
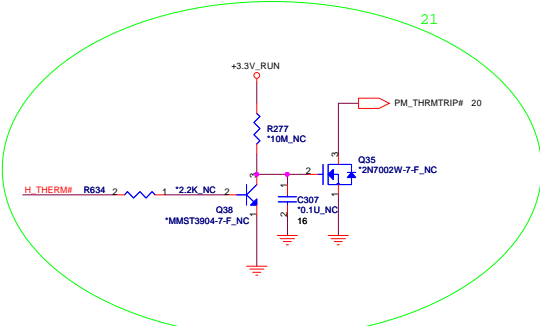


SC(1.0V),P17:  
 H\_PROCHOT#D  
 Use: pull to 68 ohm if it isn't used: pull to 50 ohm

SC(1.0V),P17:  
 H\_CATERR#  
 H\_CATURR#  
 H\_CPURSTW#  
 49.9-D  $\pm 1\%$  Pull-Up to the VTT rail (+V1.15\_VTT)



DG(V1.0),P17:  
 COMP[0.1] 49.9-Q  $\pm 1\%$  pull-down to GND  
 COMP[2.3] 20-Q  $\pm 1\%$  pull-down to GND



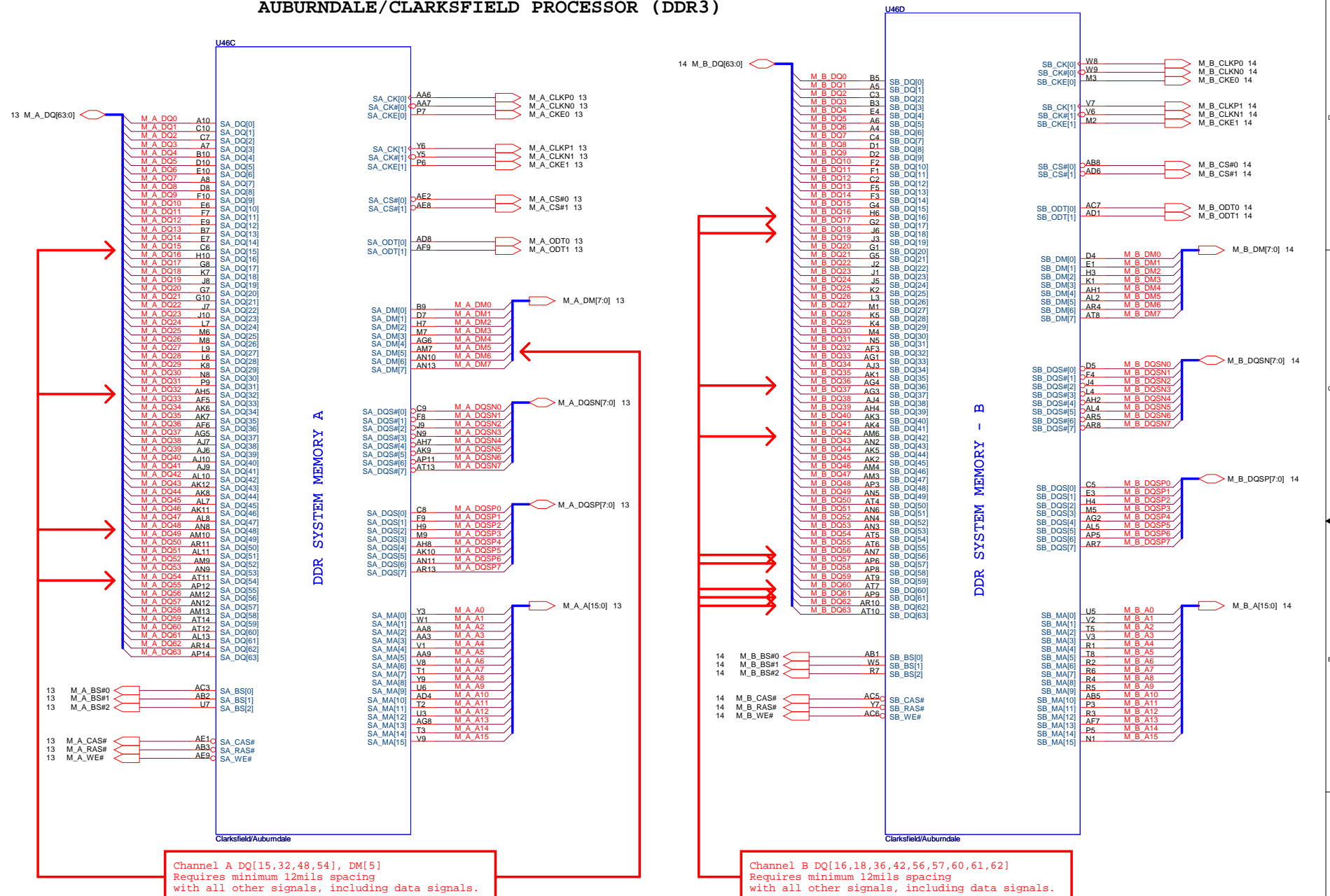
**QUANTA COMPUTER**

File: ARRD/CFD 1/4

Size: Document Number G1M6 Rev 2B

Date: Friday, June 25, 2010 Sheet 3 of 63

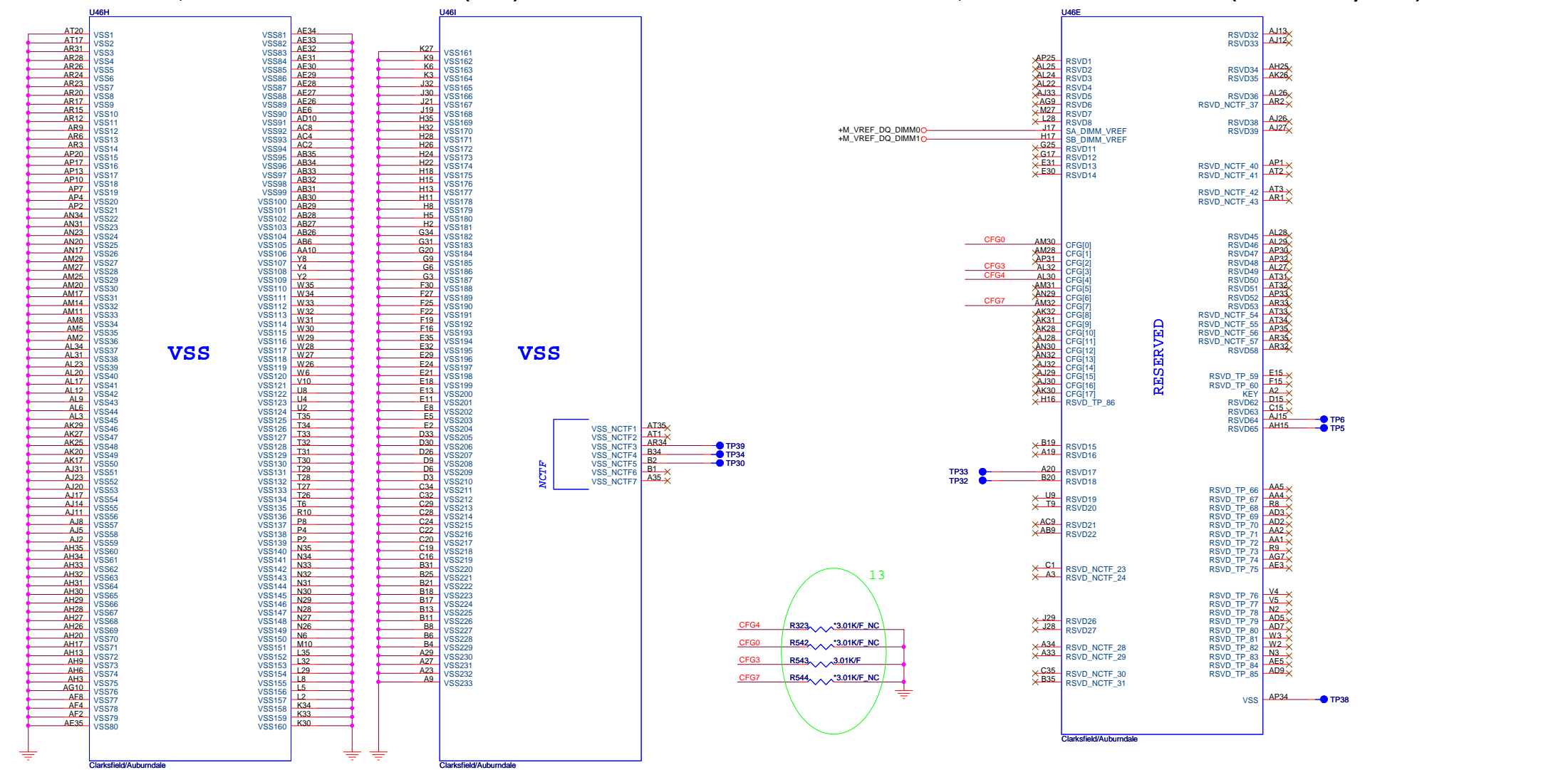
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[ 1:0 ] - PCI\_Epress Configuration Select  
 \* 11= 1 x 16 PEG  
 \* 10= 2 x 8 PEG

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(E51 only)

**QUANTA COMPUTER**

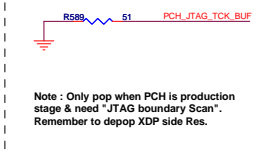
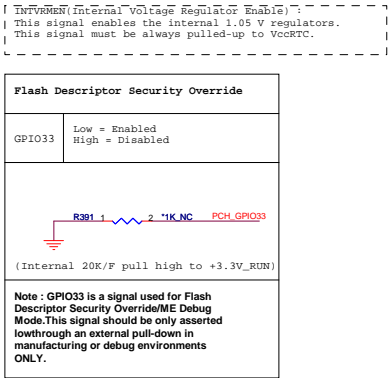
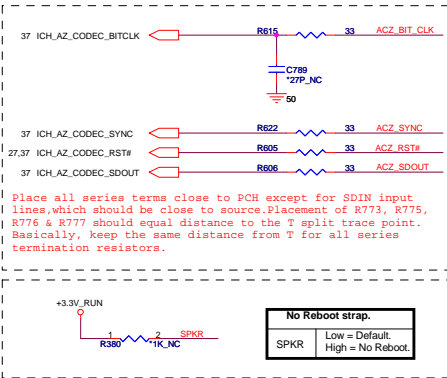
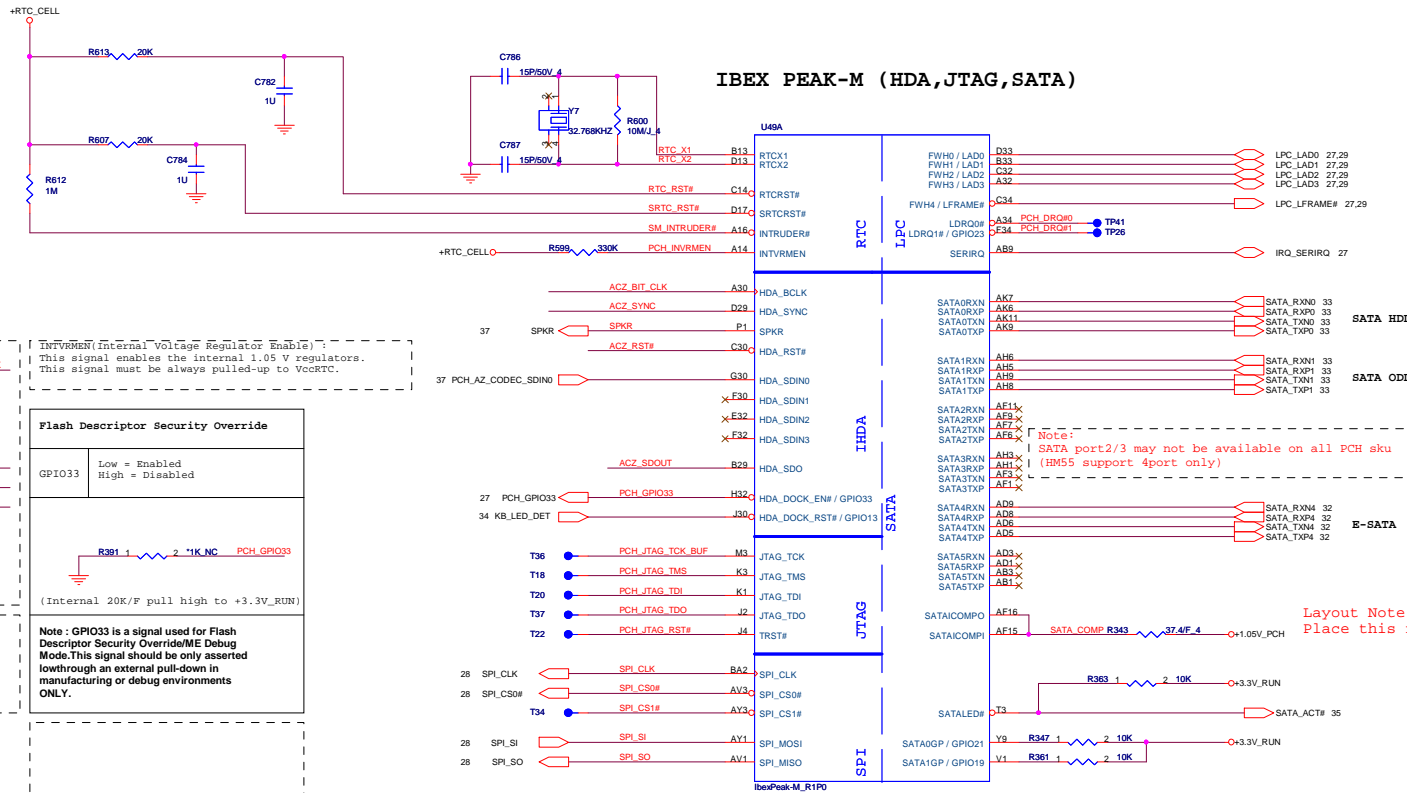
Title: ARR/CFD 4/4

Size: Document Number GM6 Rev 2B

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# IBEX PEAK-M (HDA, JTAG, SATA)

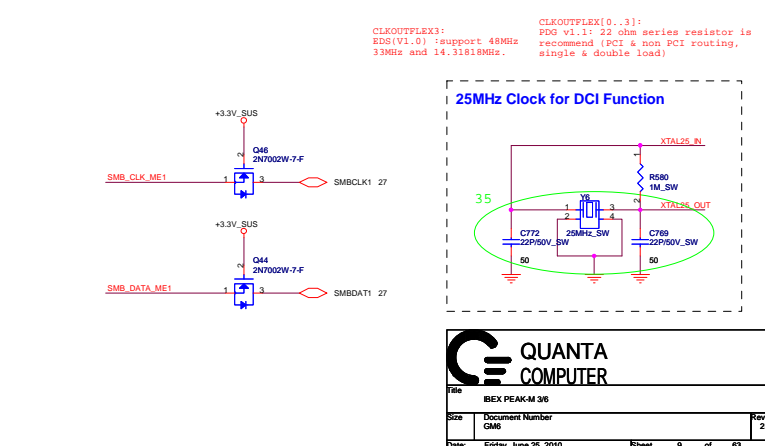
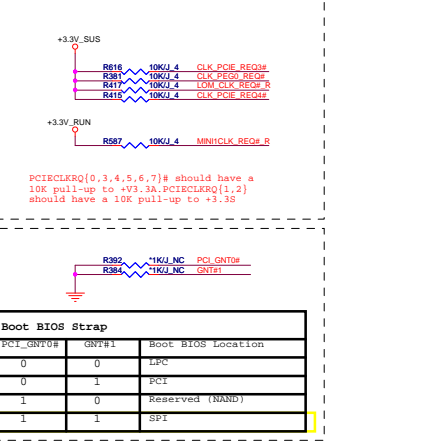
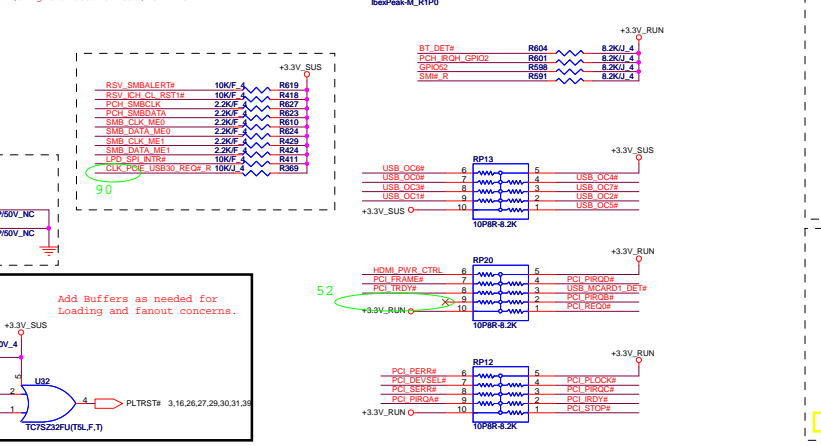
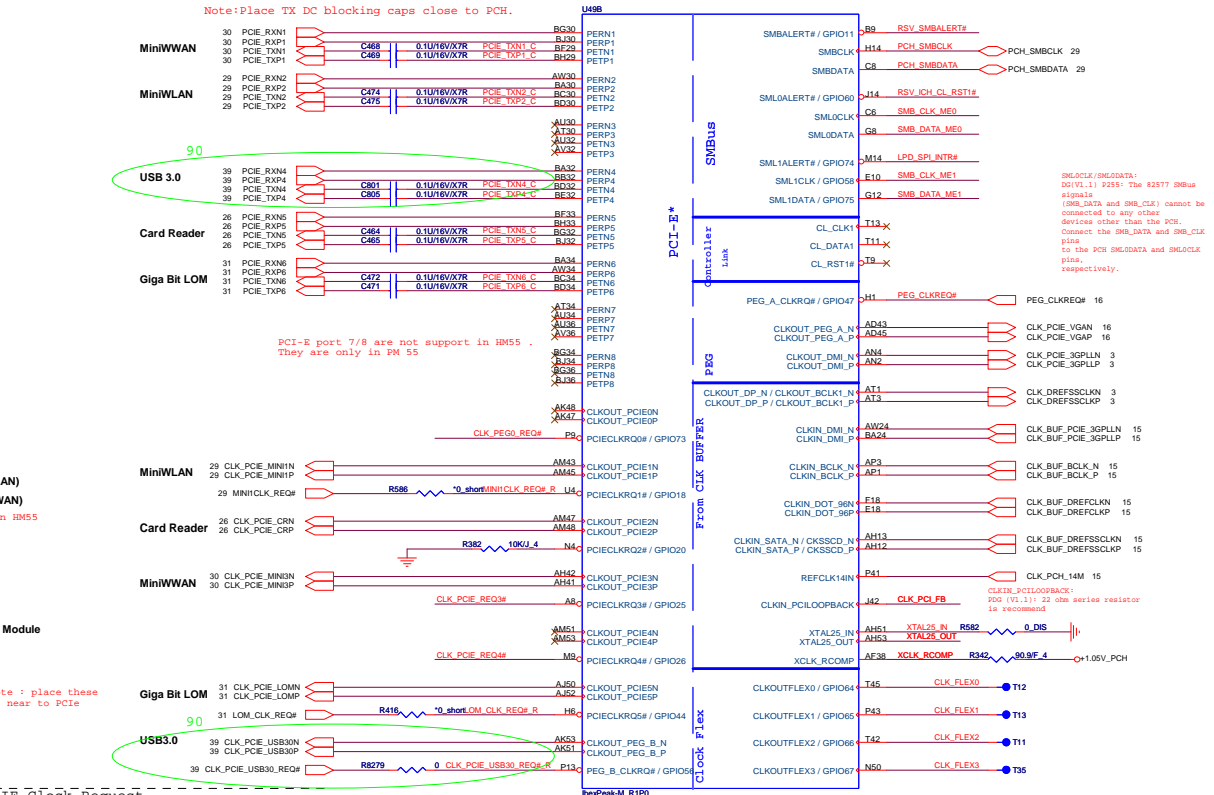
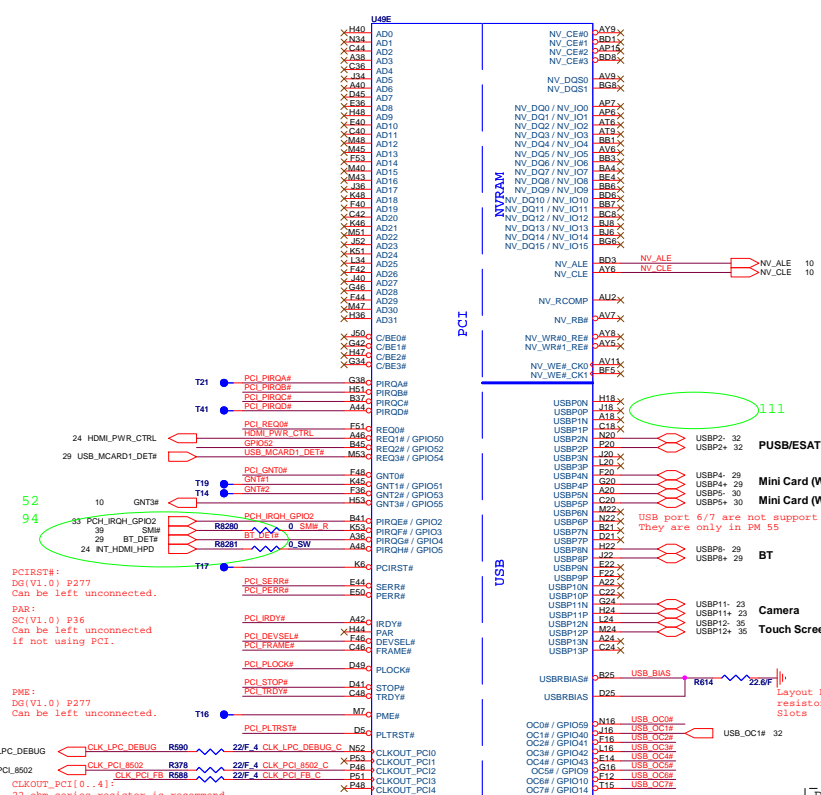


Layout Note: JTAG Test Pads are need to put on the same side of mother board.

Note: SATA port 2/3 may not be available on all PCH sku (HM55 support 4port only)

Layout Note: Place this resistor close to PCH





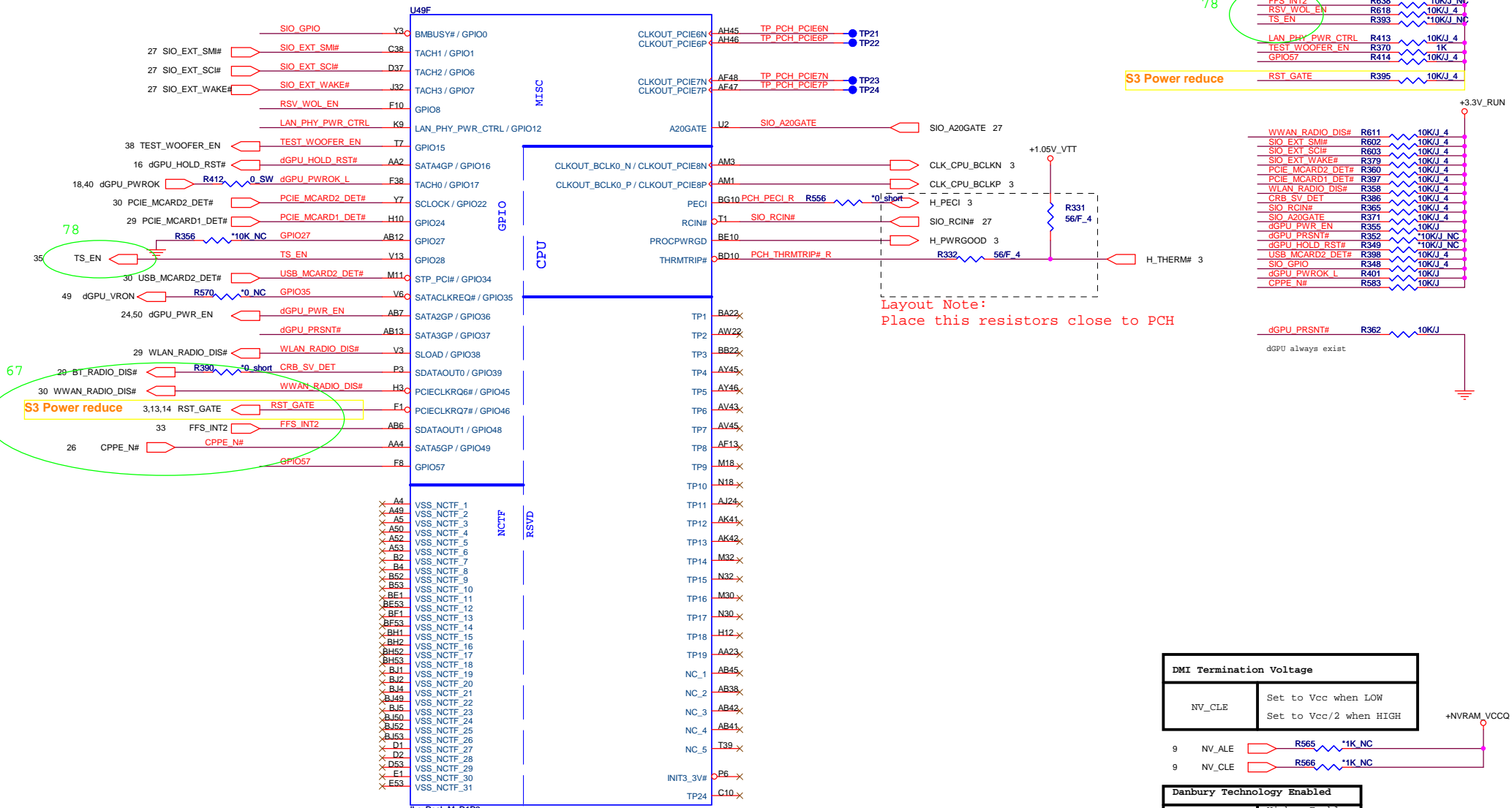
**QUANTA COMPUTER**

File: IBEX PEAK-M 3r0

Size: 28 Document Number: 626

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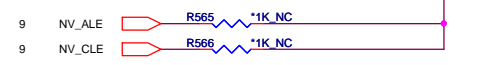
# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



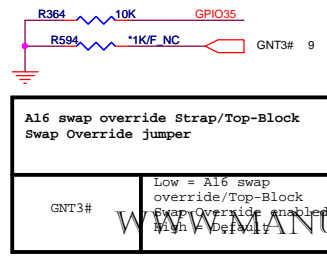
S3 Power reduce

Layout Note:  
Place this resistors close to PCH

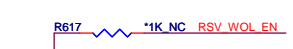
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW
	Set to Vcc/2 when HIGH



Danbury Technology Enabled	
NV_ALE	High = Enable
	Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low
	Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)
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BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is for intel BIOS validation purpose.

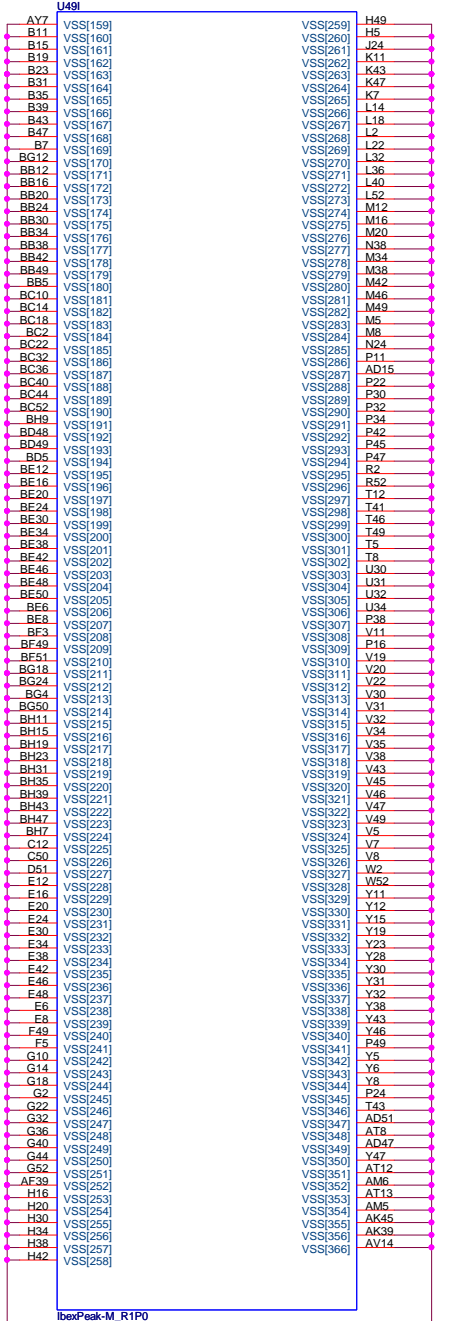
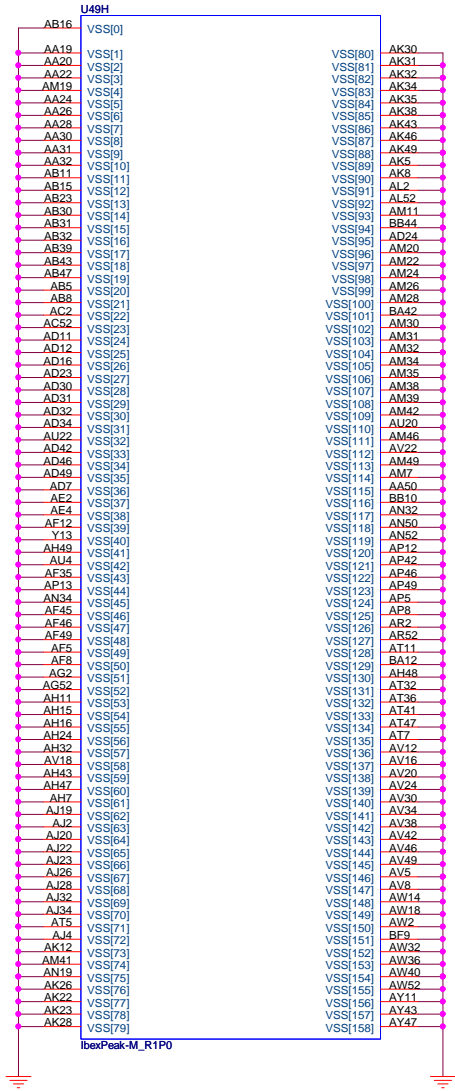
BMBUSY#:  
If not used, require a weak pull-up (8.2-10 to 10 kΩ) to Vcc3.3  
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

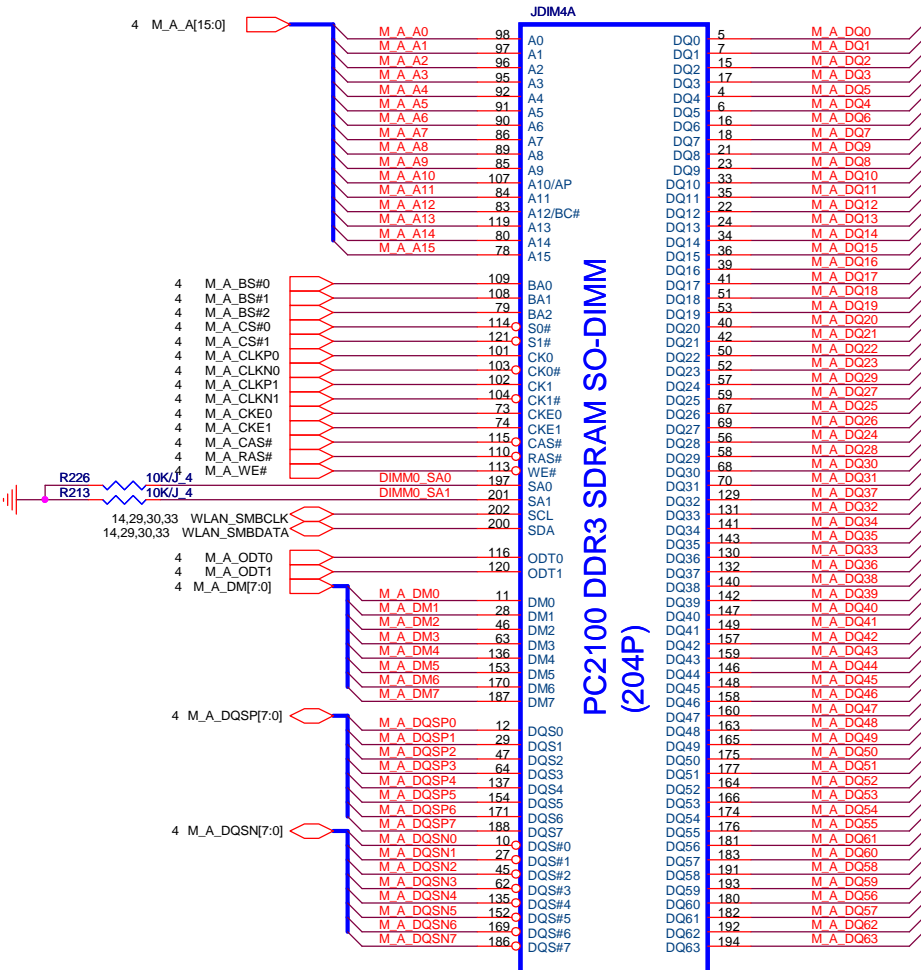


Title	IBEX PEAK-M 4/6	
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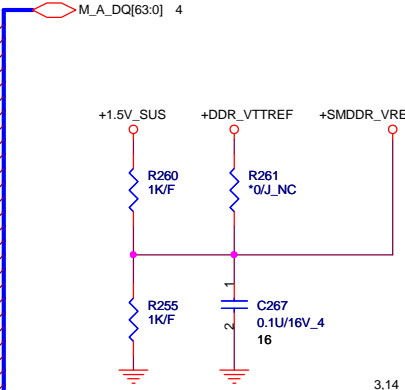
# IBEX PEAK-M (GND)



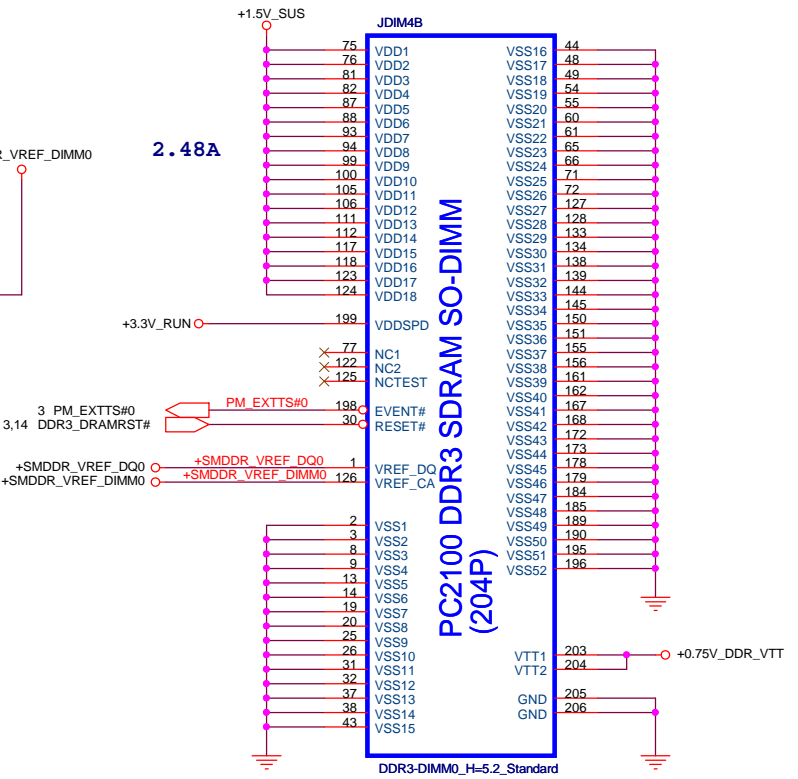


**PC2100 DDR3 SDRAM SO-DIMM (204P)**

DDR3-DIMM0\_H-5.2\_Standard

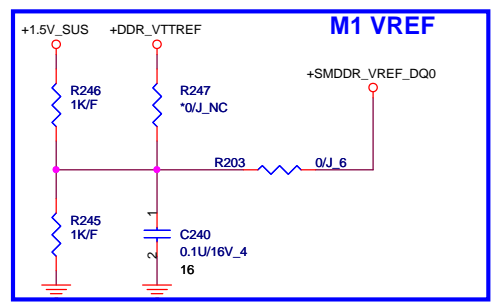


2.48A

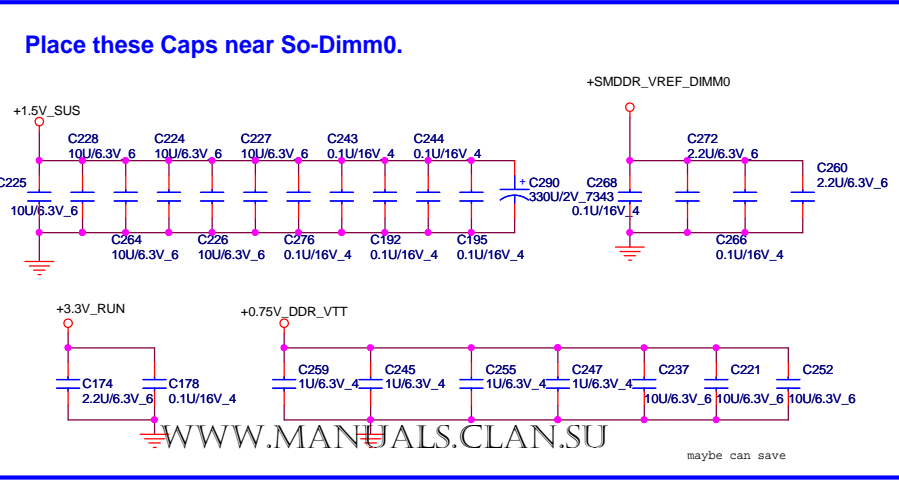


**PC2100 DDR3 SDRAM SO-DIMM (204P)**

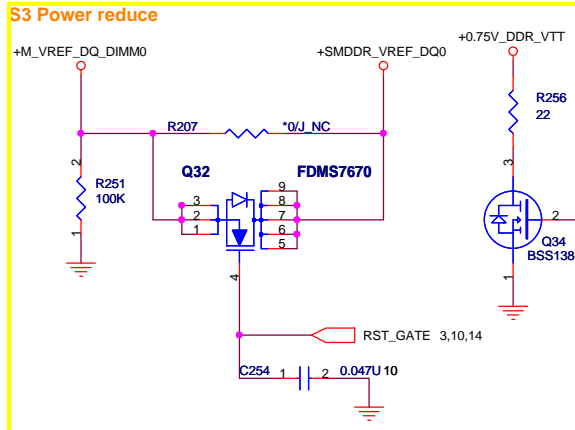
DDR3-DIMM0\_H-5.2\_Standard



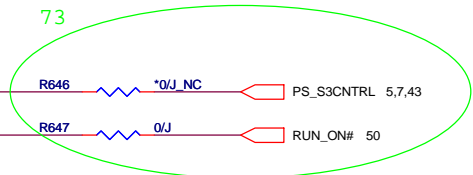
VREF_DQ	R203	R207	R247 (+DDR_VTTREF)
M1	stuff	X	X
M3	X	stuff	X

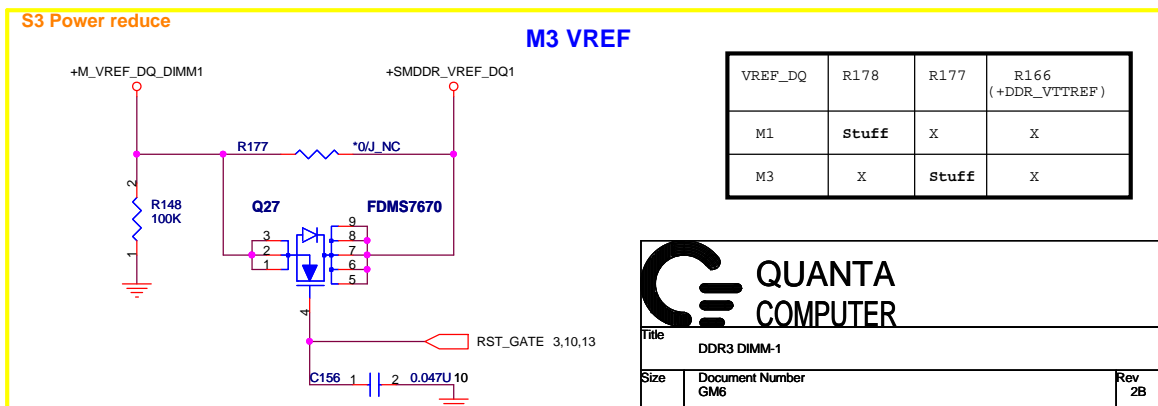
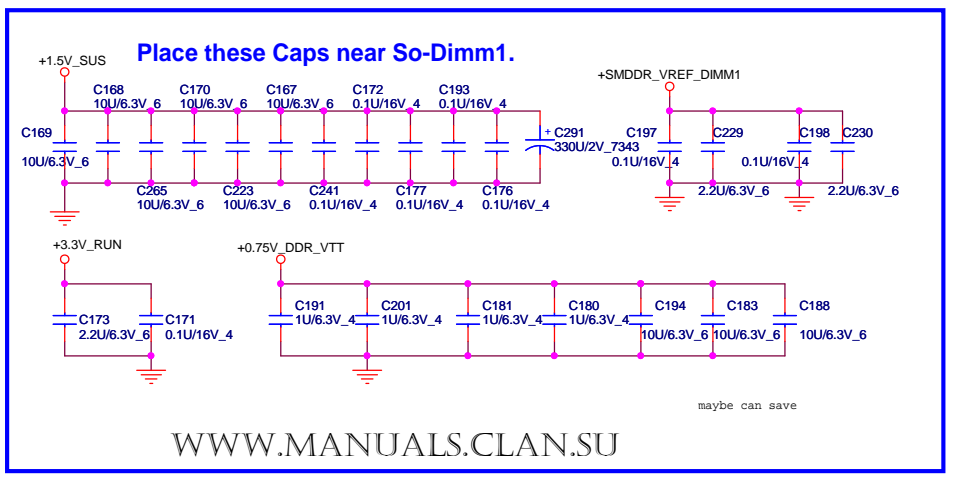
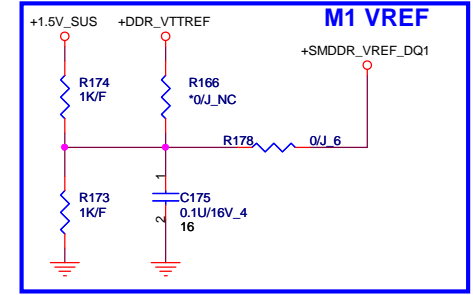
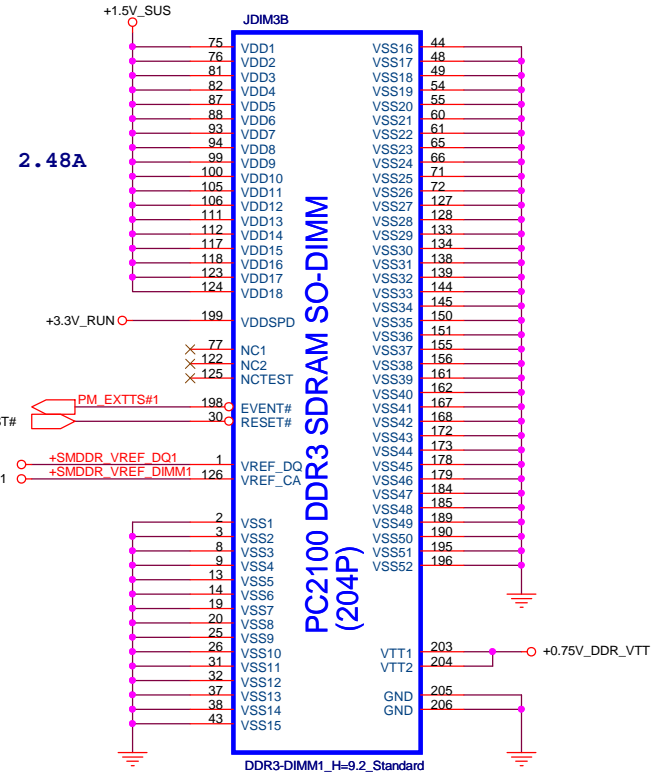
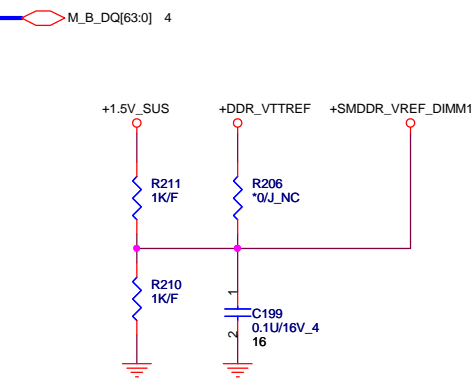
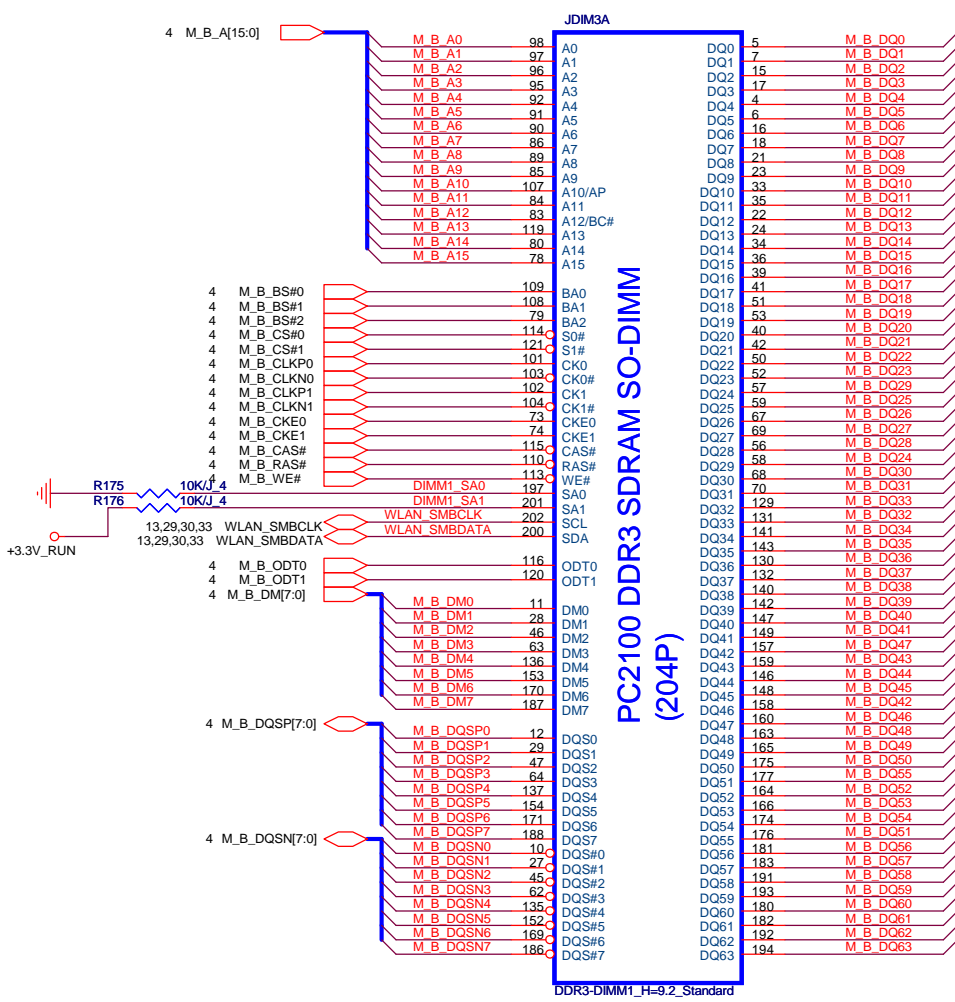


WWW.MANUALS.CLAN.SU

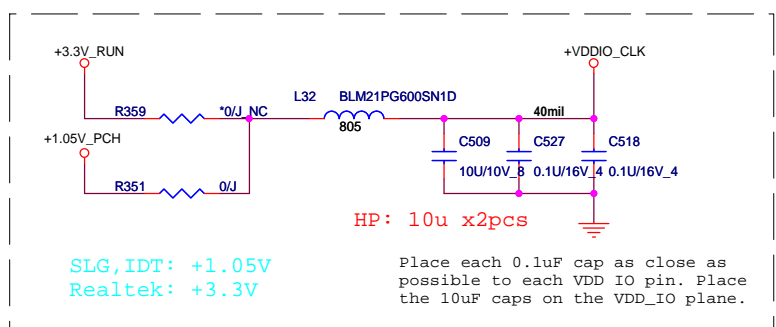
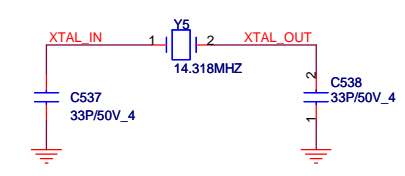
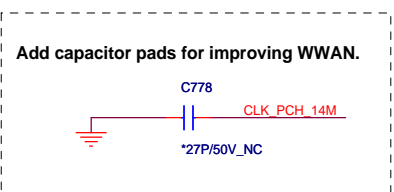
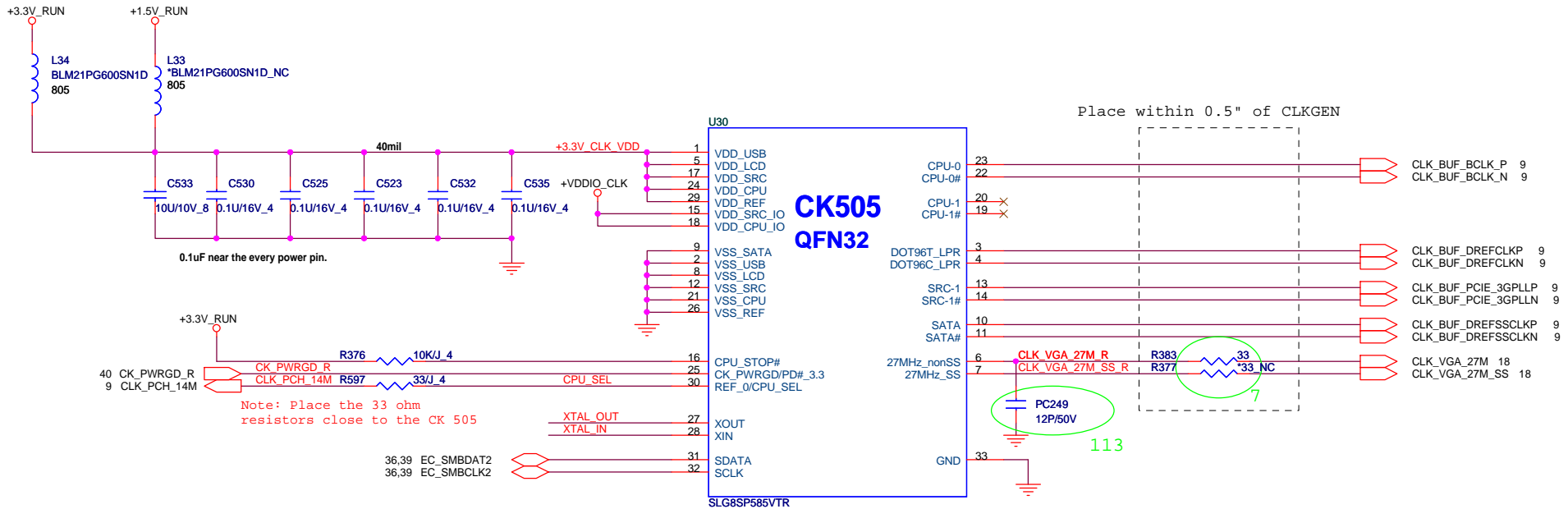


M3 VREF

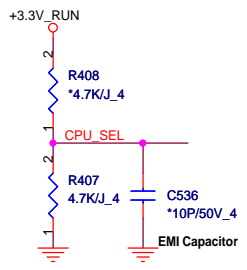




VREF_DQ	R178	R177	R166 (+DDR_VTTREF)
M1	stuff	X	X
M3	X	stuff	X



**+VDDIO\_CLK:**  
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.  
 Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.  
 IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

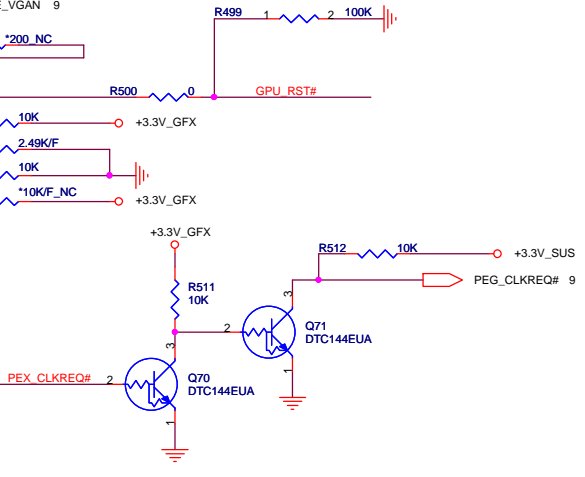
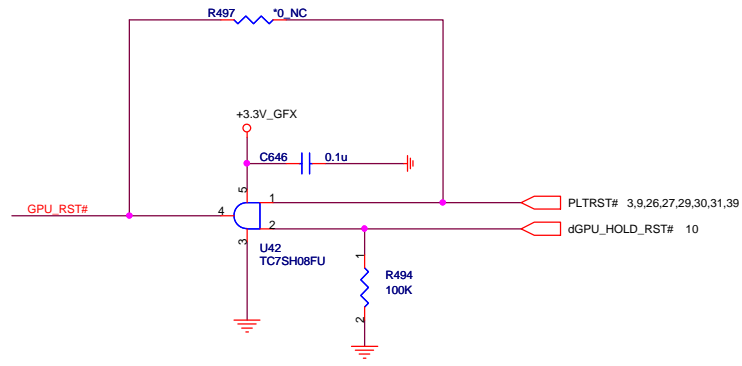
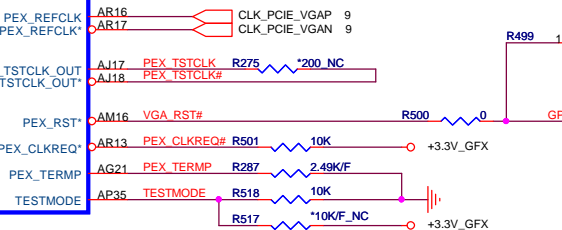
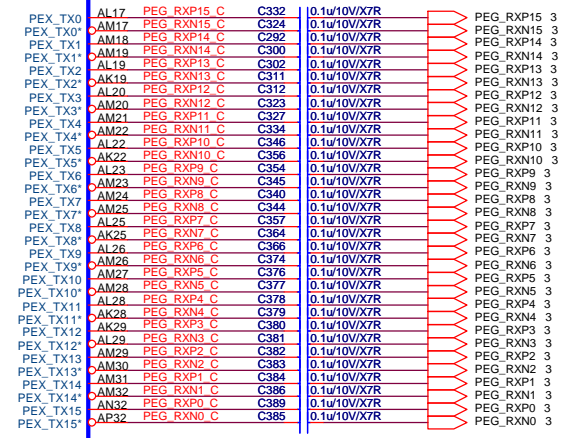
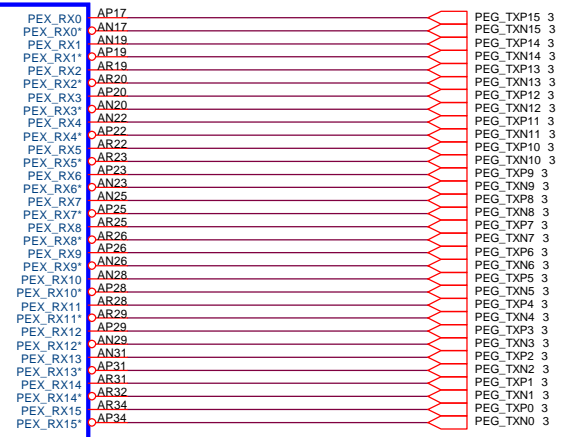
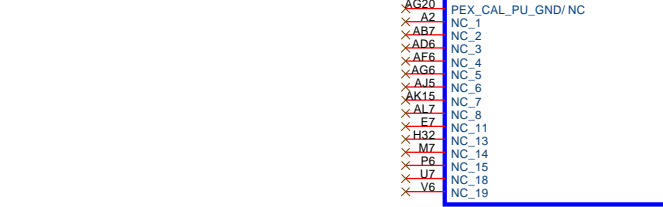
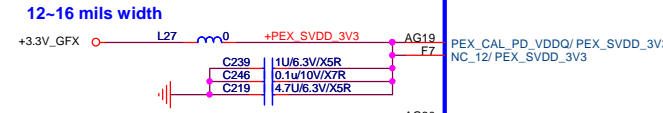
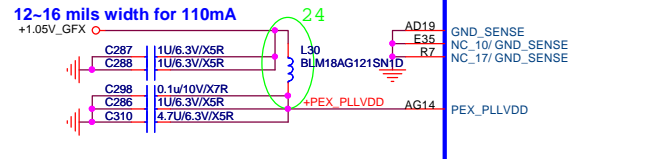
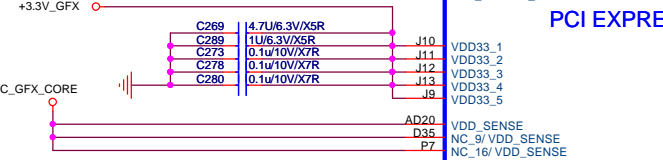
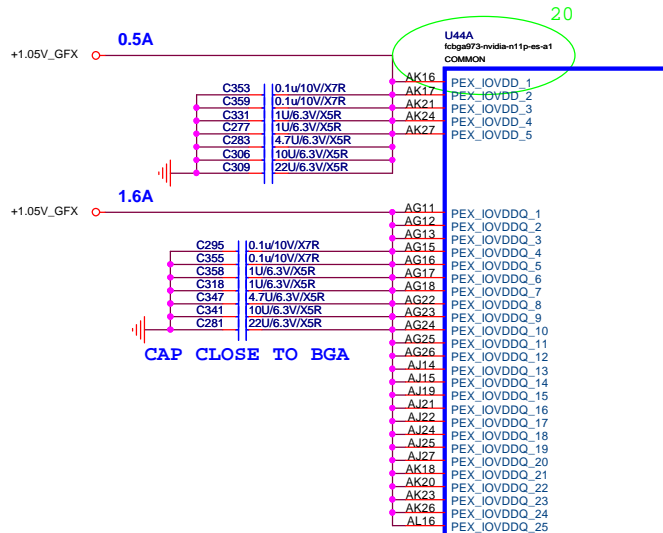
**CPU\_SEL:**  
 SLG date sheet (V0.2) P15:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 Realtek date sheet (V1.2) P11:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 IDT date sheet (V0.7) P10:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.

**QUANTA COMPUTER**

Title: Clock Generator

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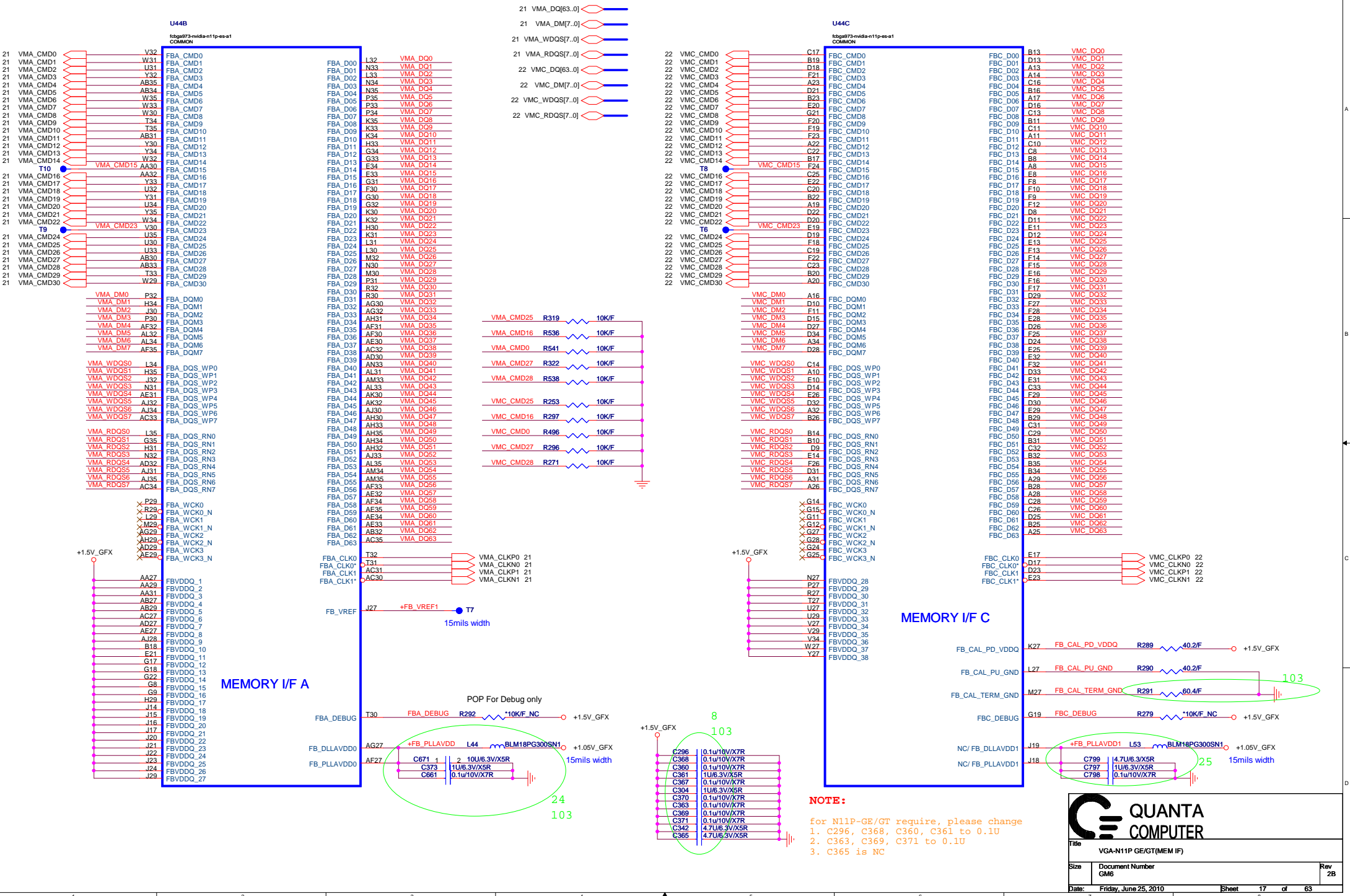
**QUANTA COMPUTER**

Title: VGA-N11P GE/GE(PCie)

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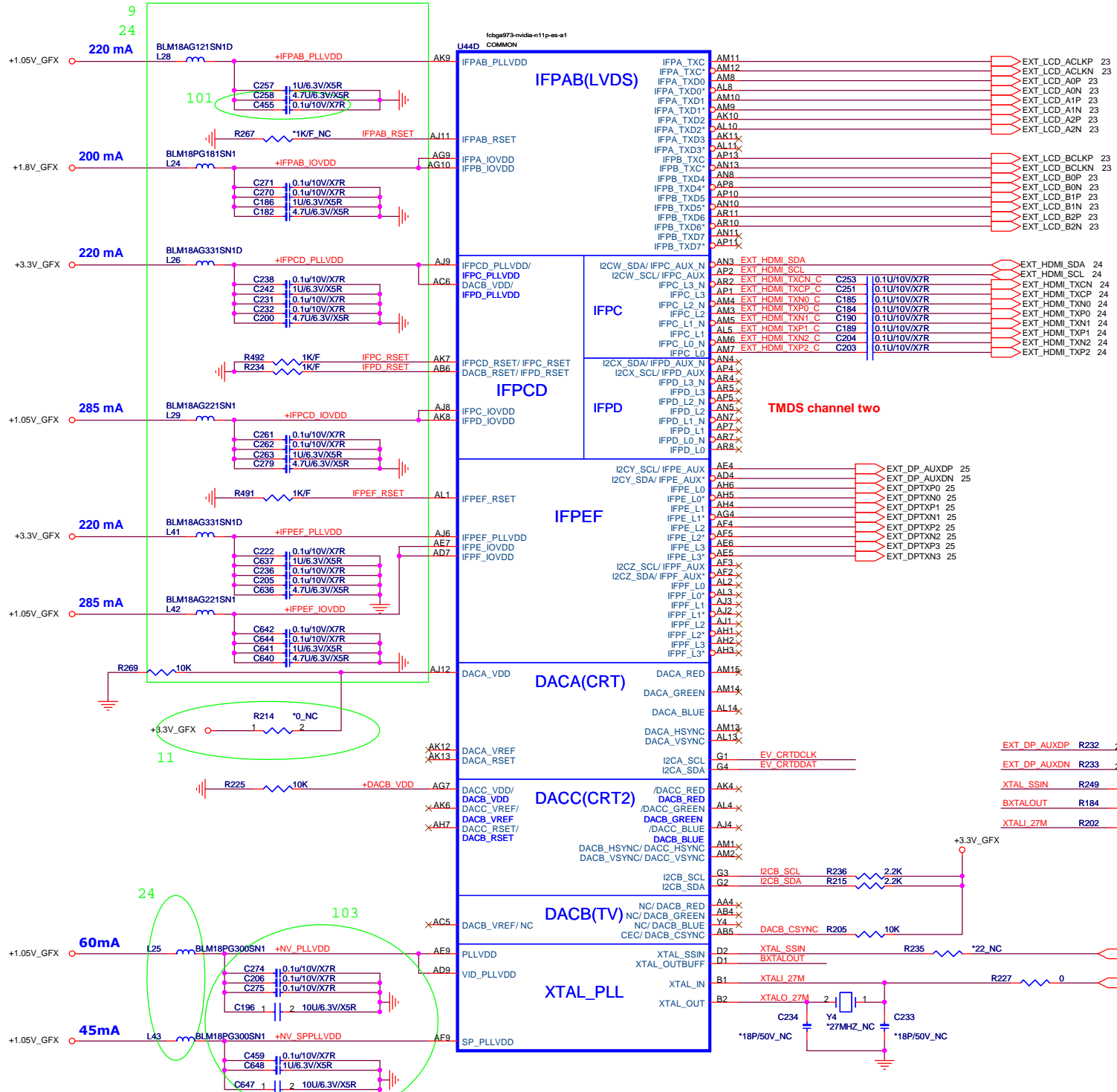


**QUANTA COMPUTER**

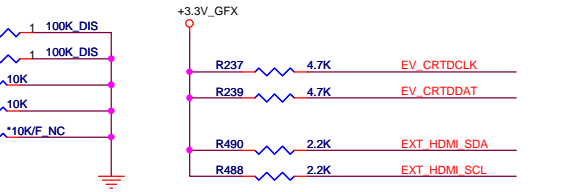
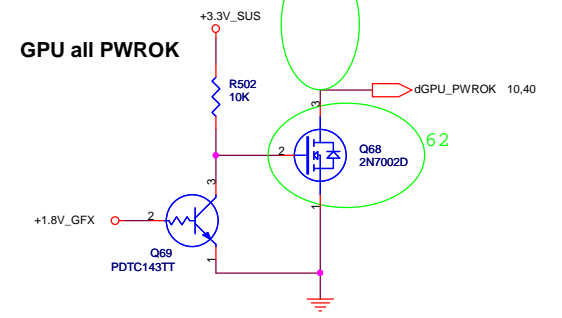
Title: VGA-N11P GE/GT(MEM I/F)

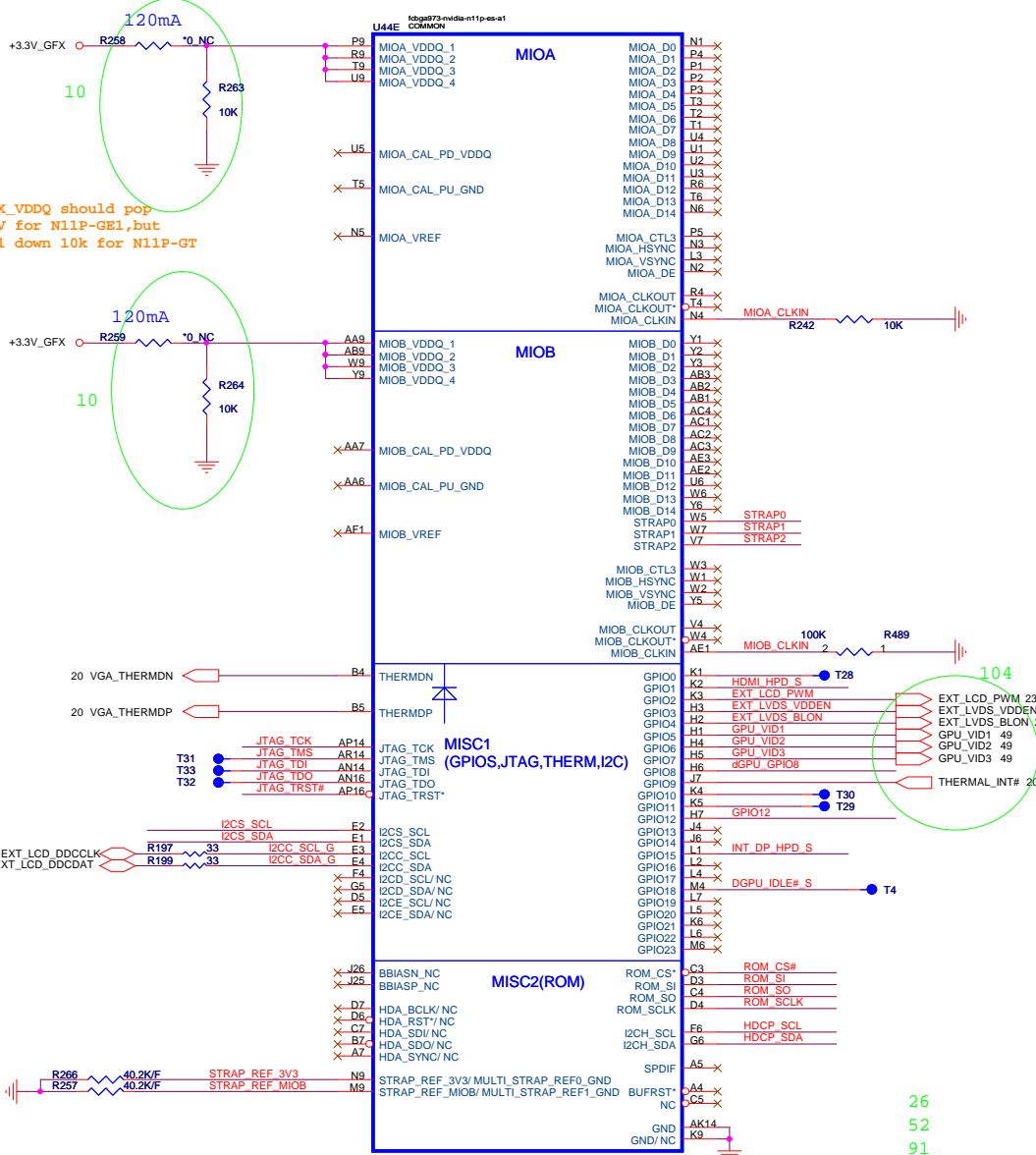
Size: Document Number GM6 Rev 2B

Date: Friday, June 25, 2010 Sheet 17 of 63



**GPU all PWROK**





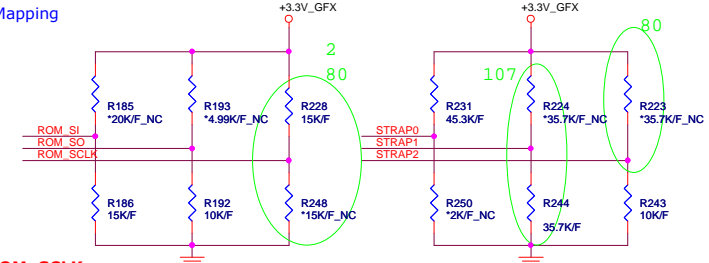
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCL_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCL_DEVID[3]	PCL_DEVID[2]	PCL_DEVID[1]	PCL_DEVID[0]	XXXX
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

39 VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	800MHz 512MB(64M*16)	Samsung AKD5LGGT502	AKD5LGGT502	K4W1G1646E-HC12
0x2(0010)	800MHz 512MB(64M*16)	Hynix AKD5LZGTW00	AKD5LZGTW03	H5TQ1G63BFR-12C
0x6(0110)	800MHz 1GB(128M*16)	Hynix AKD5MGGT00	AKD5MGGT00	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16)	Samsung AKD5MGGT505	AKD5MGGT00	K4W2G1646E-HC12

ROM\_SI Strap Bit for RAM Mapping

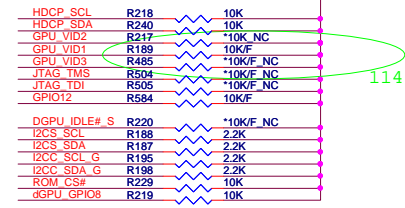
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



STRAP2 ROM\_SCLK

N11P-GE	PD 10K	PU 15K
N11P-GE	PD 15K	PU 15K

SUNSUNG OR HYNIX N11P-ES DevID is 0x0DFE, so pull up ROM\_SCLK with 15Kohm and STRAP2 pull up 35Kohm

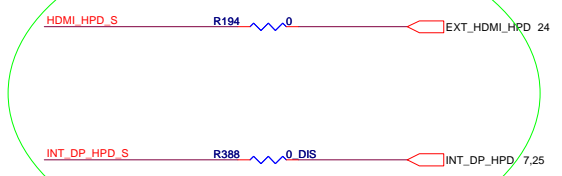


### GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

N11P-GT/GE Table

Quanta PN	DESCRIPTION	Vendor PN
AJ0N11P0T25	IC CTRL(973P) N11P-GT-A1 (BGA)	N11P-GT-A1
AJ0N11P0T26	IC CTRL(973P) N11P-GE-A1 (BGA)	N11P-GE-A1



**QUANTA COMPUTER**

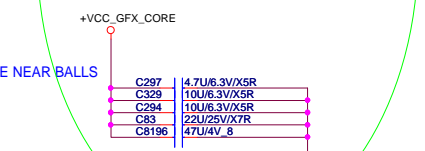
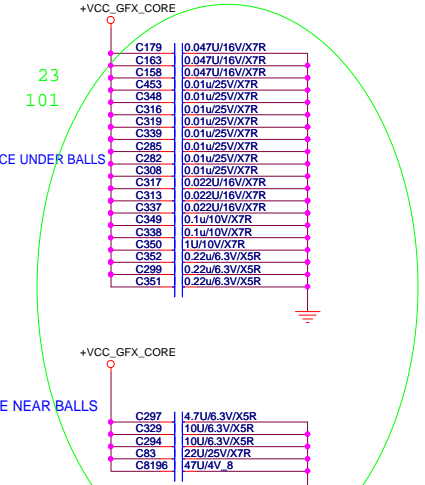
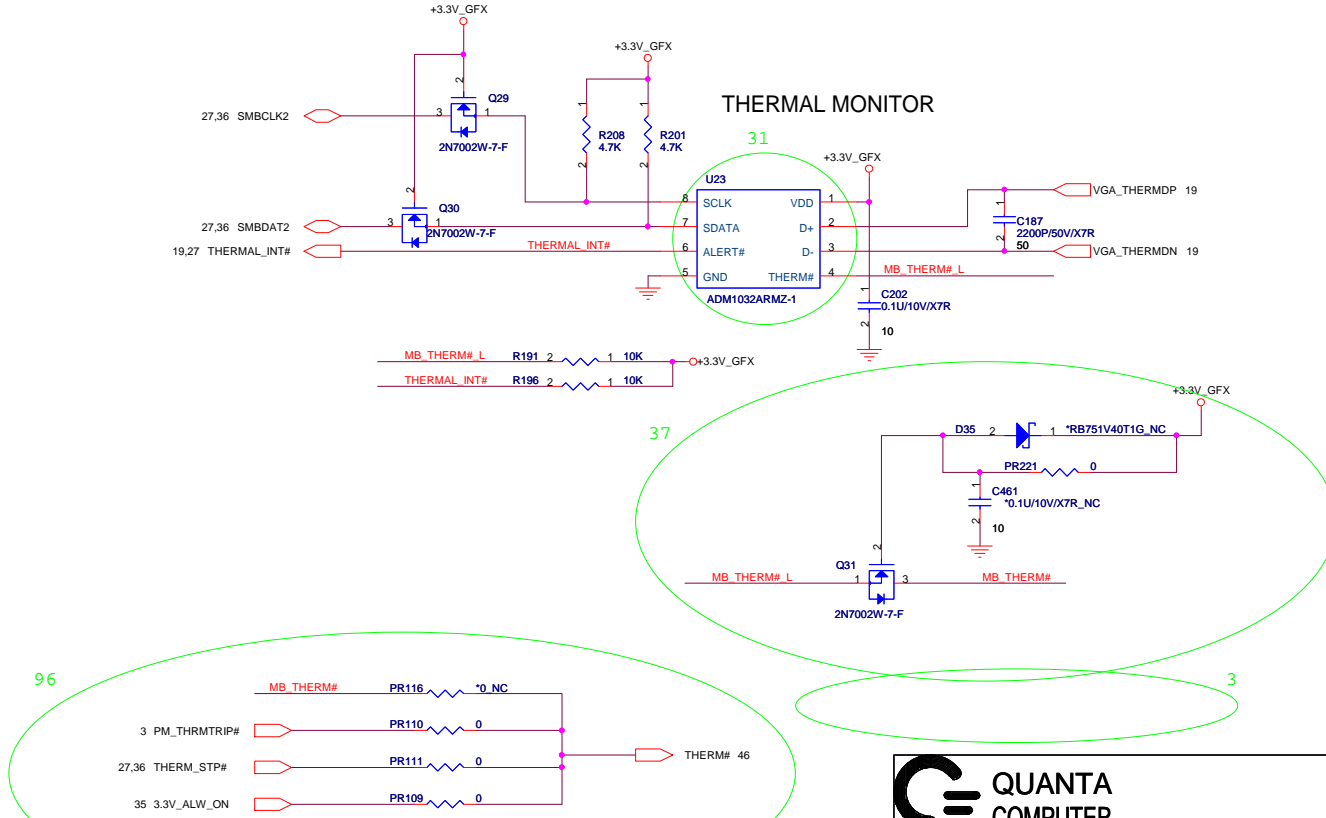
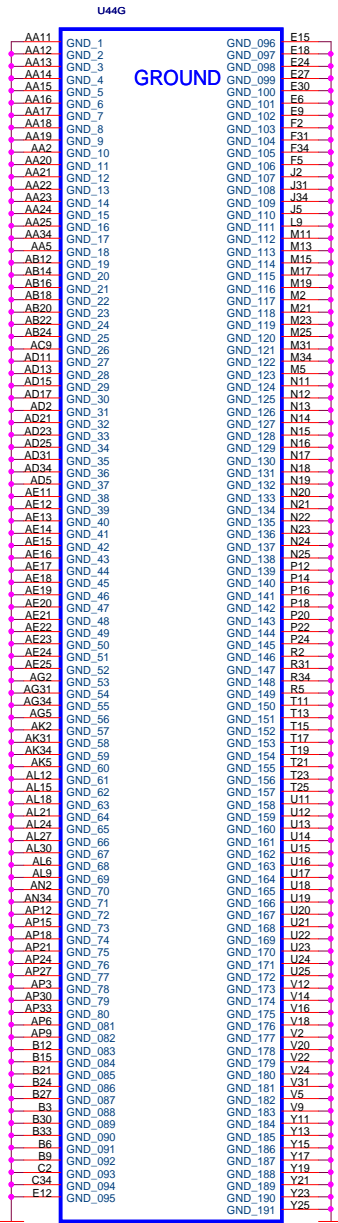
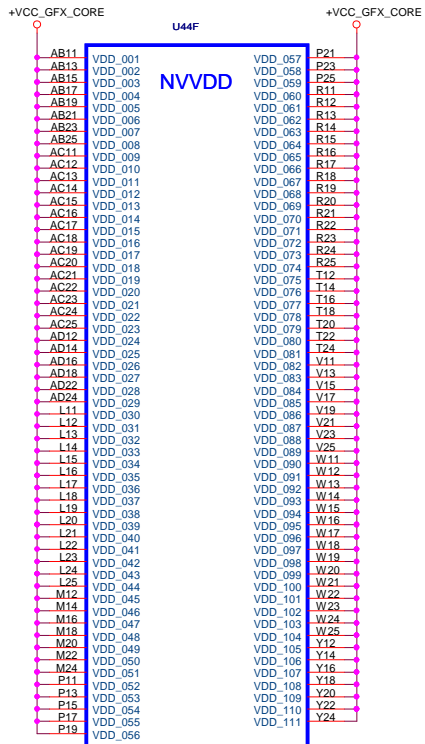
Title: VGA-N11P GE/GT(GPIO/STRAP)

Size: Document Number GM6

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Rev: 2B



**QUANTA COMPUTER**

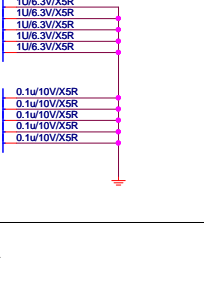
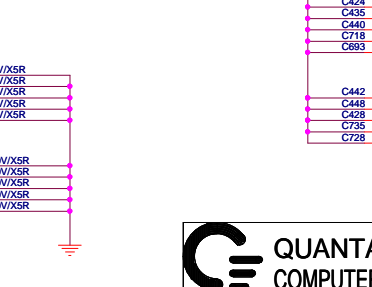
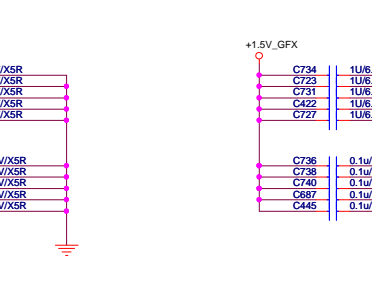
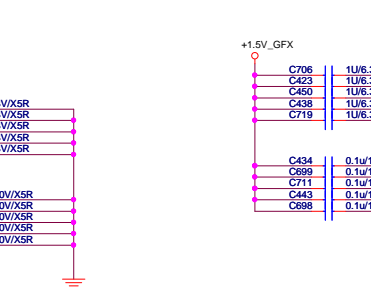
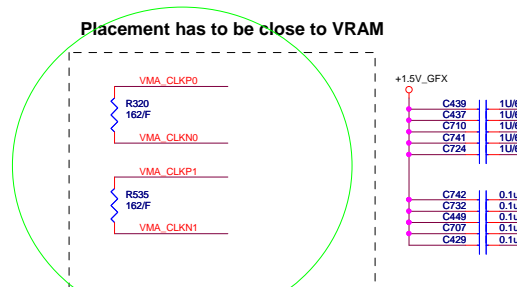
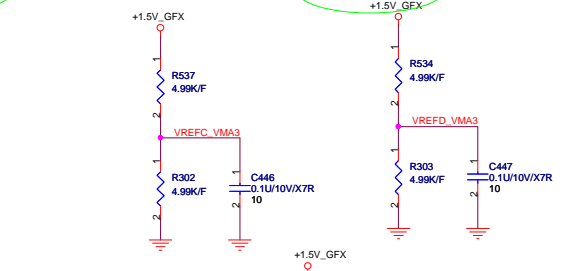
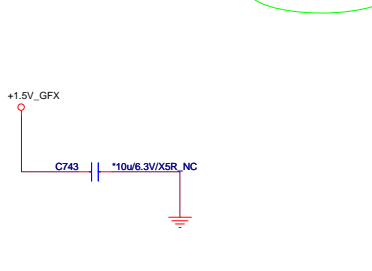
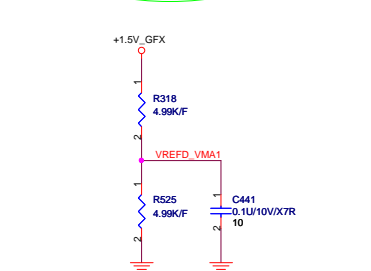
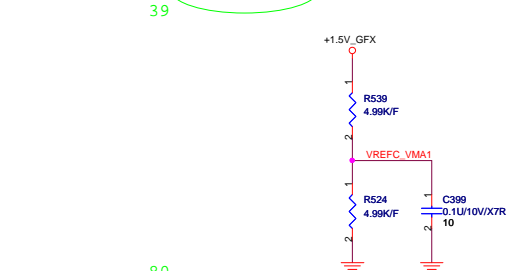
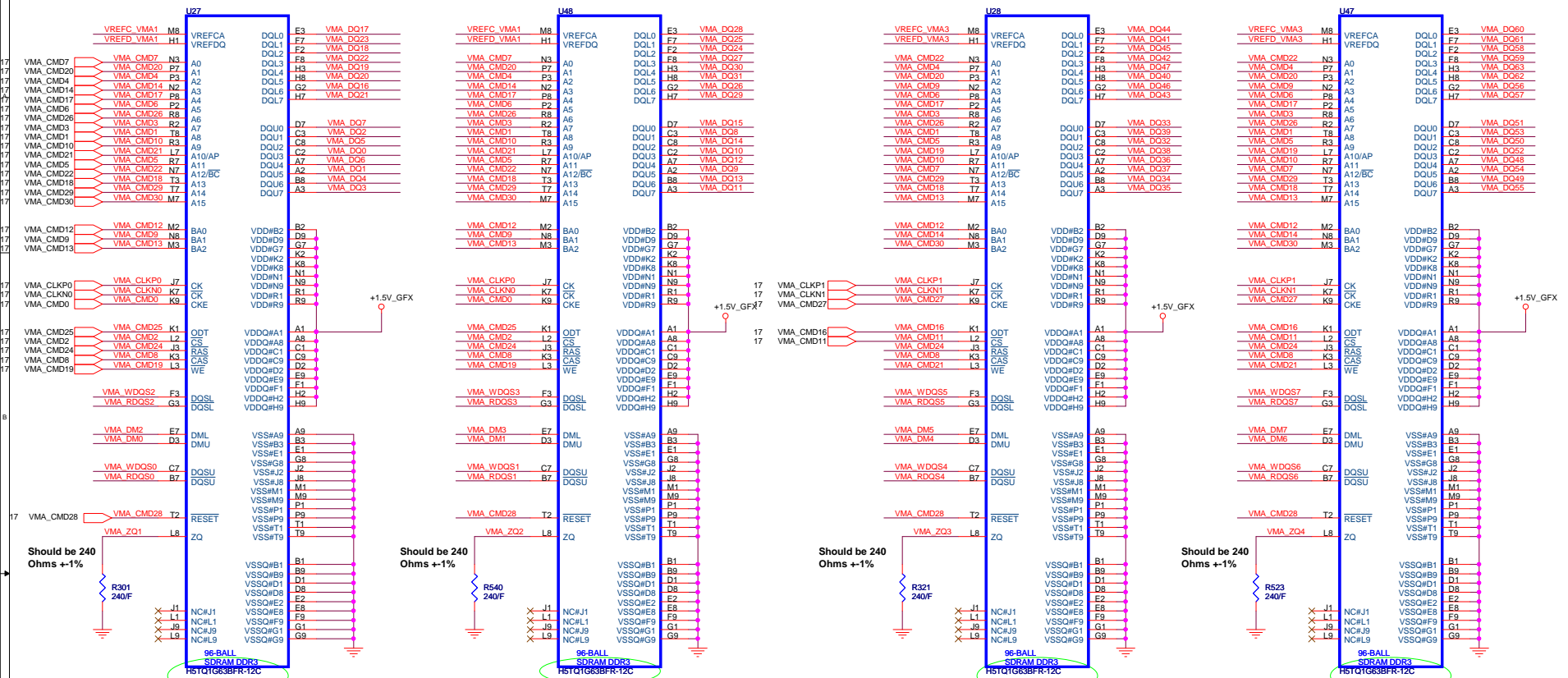
Title: VGA-M11P GE/GT(POWER/THM)

Size: Document Number: Rev 2B

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17 VMA\_DM[6:3]\_0  
 17 VMA\_DM[7]\_0  
 17 VMA\_WD[5:7]\_0  
 17 VMA\_RD[5:7]\_0

# CHANNEL A: 512MB/1024MB DDR3



GE1 FOR 243 BUT GT/8 REQUIRE CHECK FAE

WWW.MANUALS.CLAN.SU

**QUANTA COMPUTER**

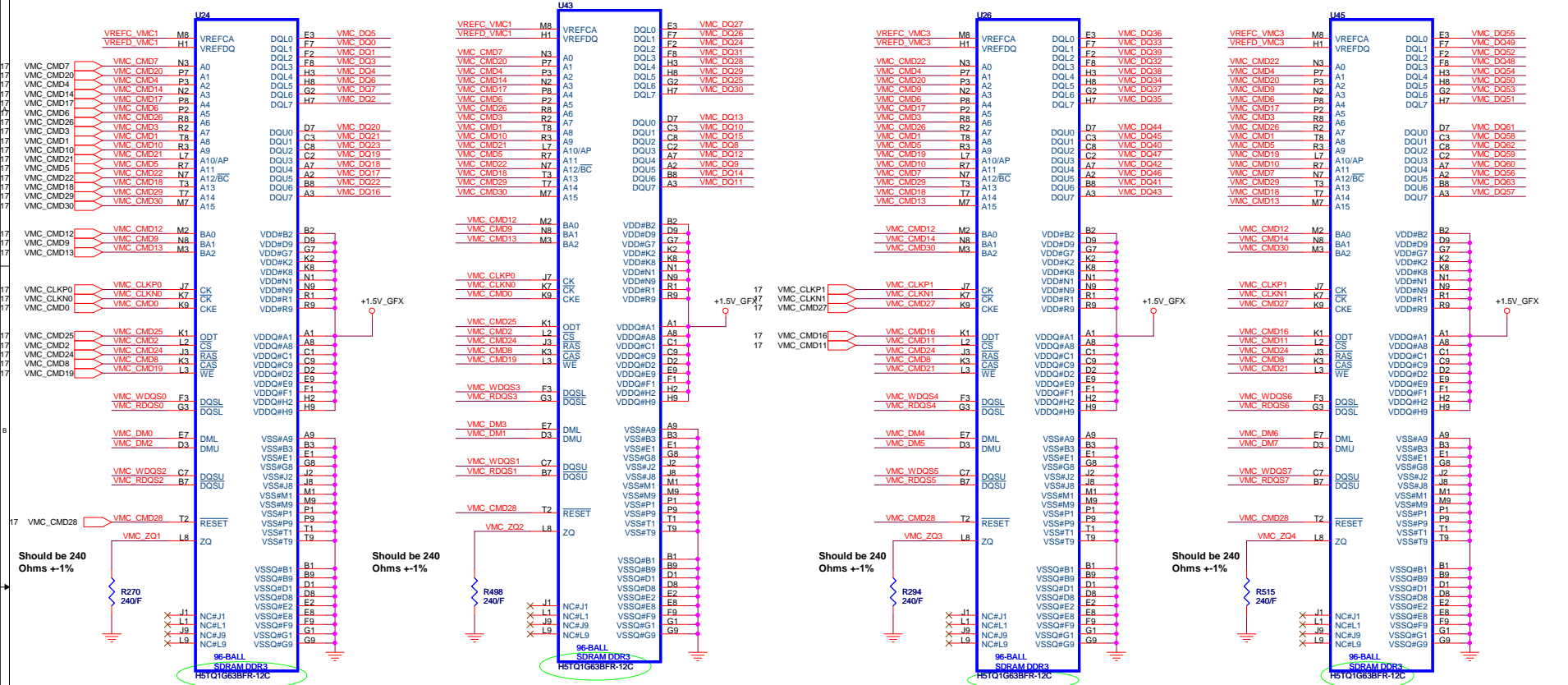
Title: VGA-N11P GE/GT(VRAM-1)

Size: Document Number GMS Rev 2B

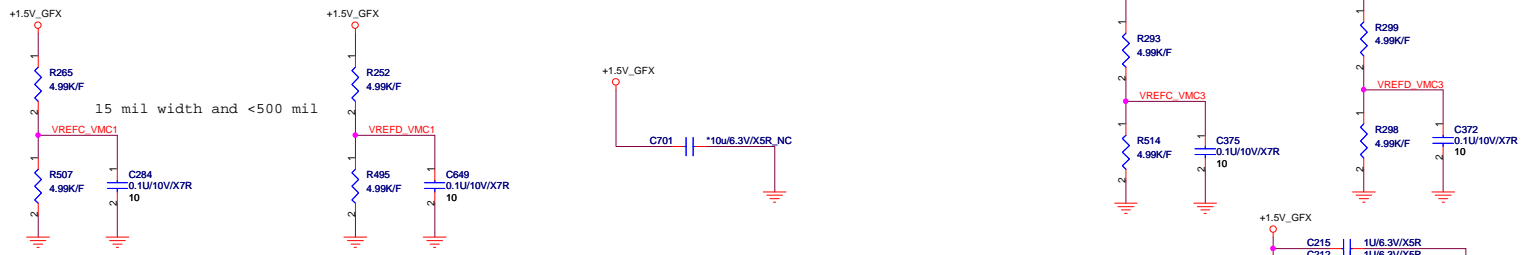
Date: Friday, June 25, 2010 Sheet 21 of 63

17 VMC\_DQ[63..0]  
17 VMC\_DM[7..0]  
17 VMC\_WDQS[7..0]  
17 VMC\_RDQS[7..0]

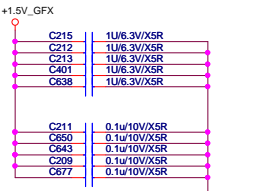
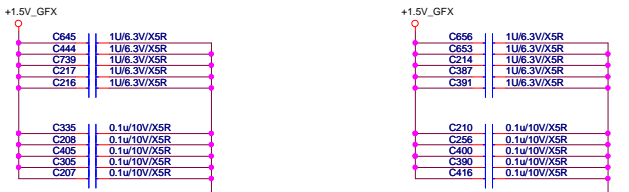
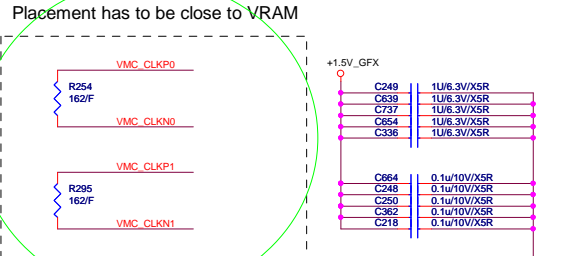
# CHANNEL B: 512MB/1024MB DDR3



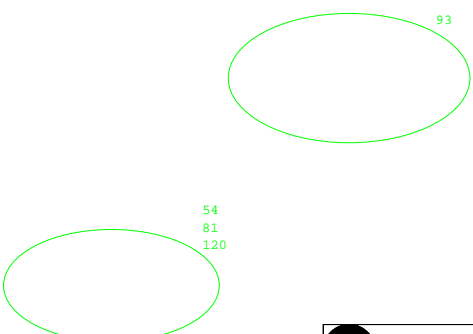
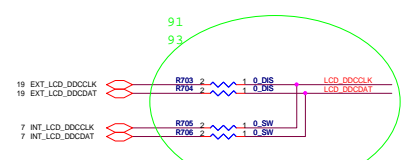
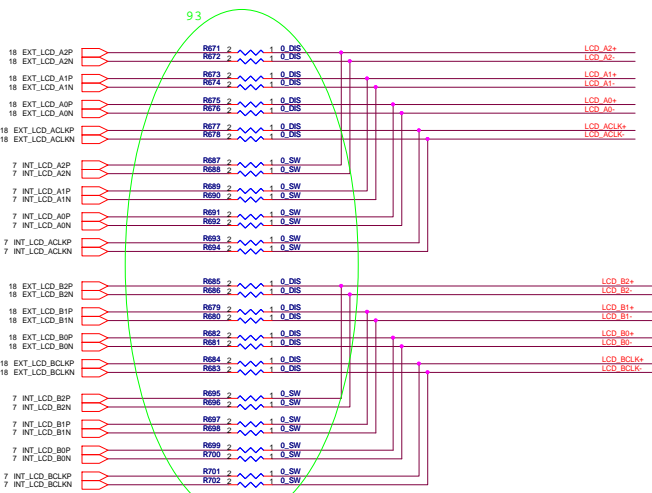
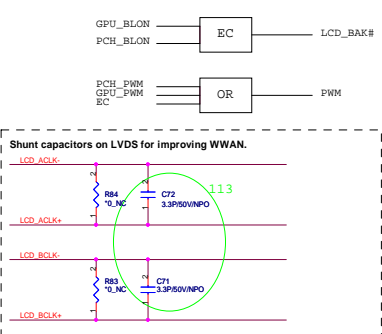
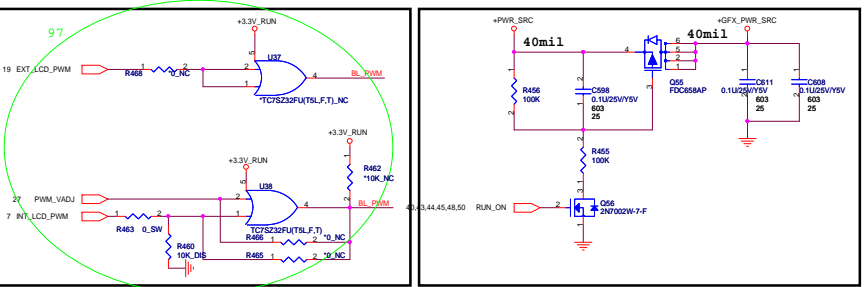
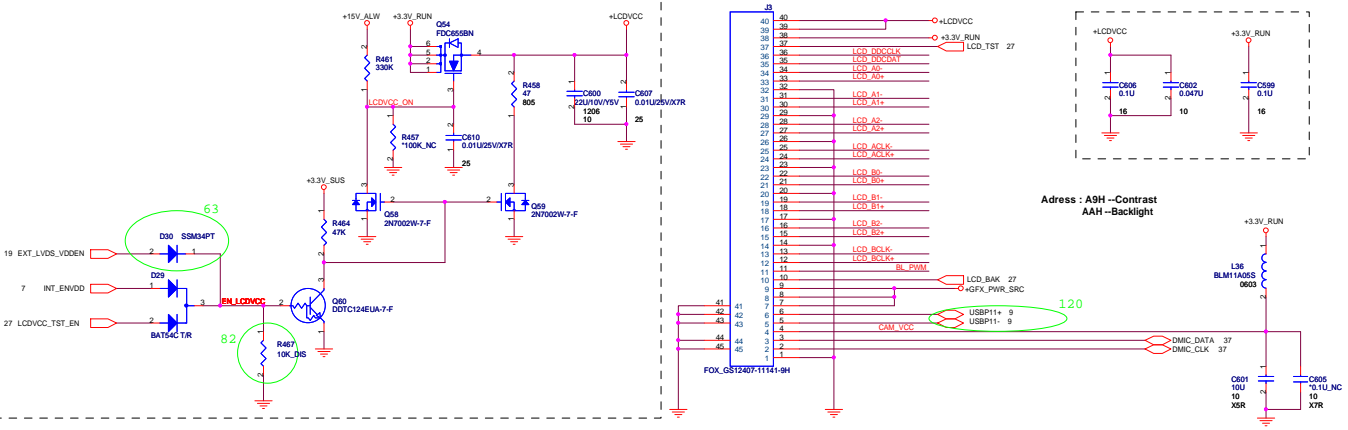
39



80

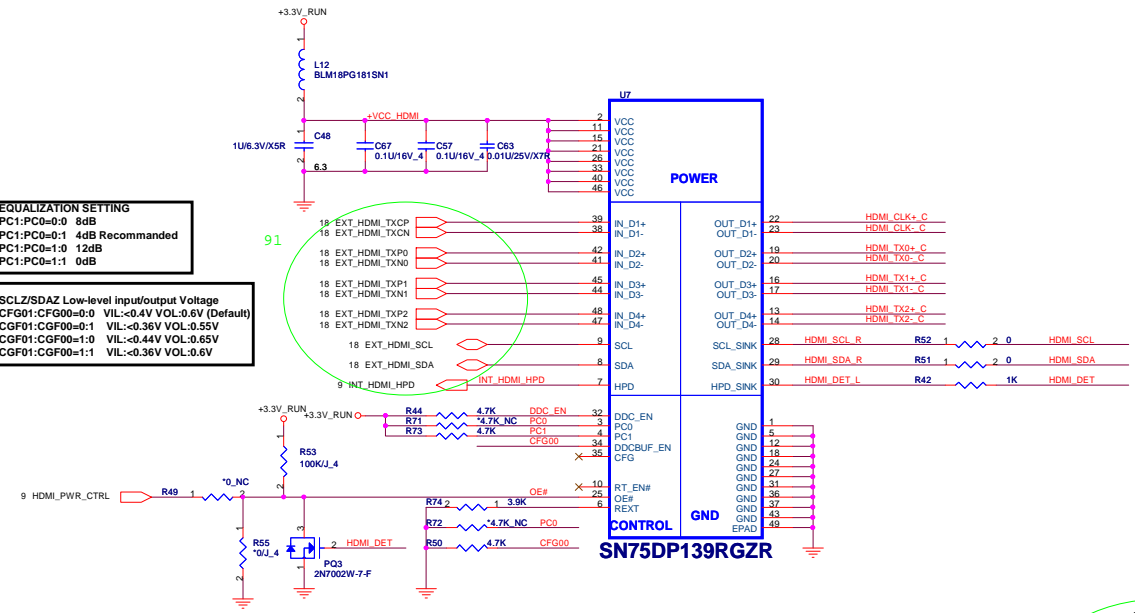


WWW.MANUALS.CLANSU

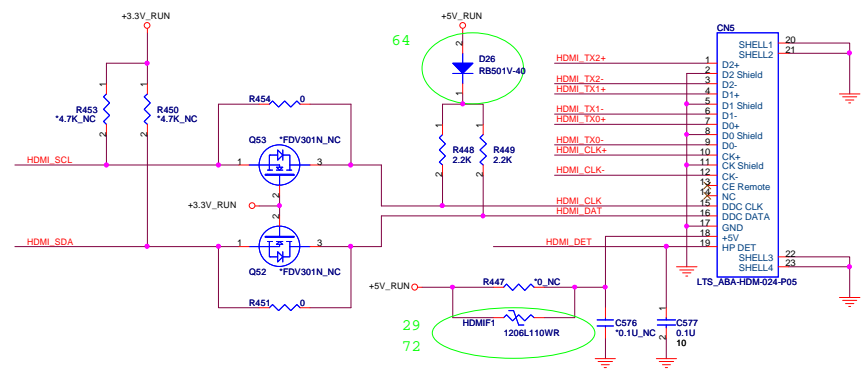
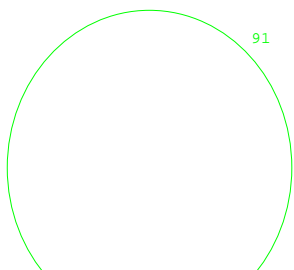


**EQUALIZATION SETTING**  
 PC1:PC0=0:0 8dB  
 PC1:PC0=0:1 4dB Recommended  
 PC1:PC0=1:0 12dB  
 PC1:PC0=1:1 0dB

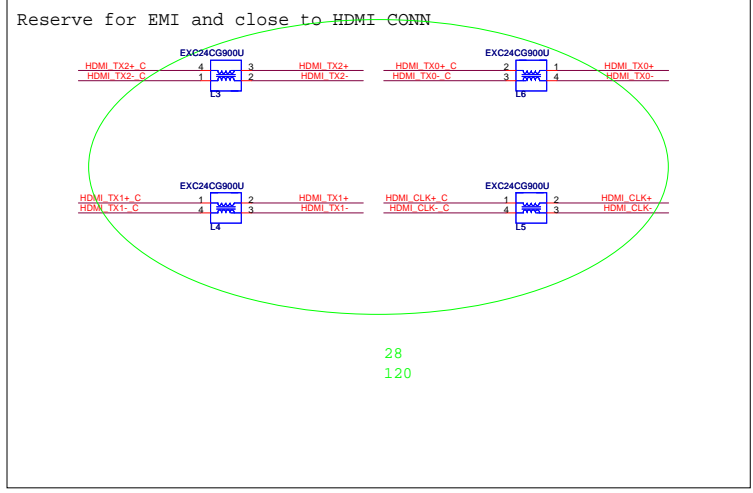
**SCLZ/SDAZ Low-level input/output Voltage**  
 CG501:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)  
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V  
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V  
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V



**HDMI Switch**



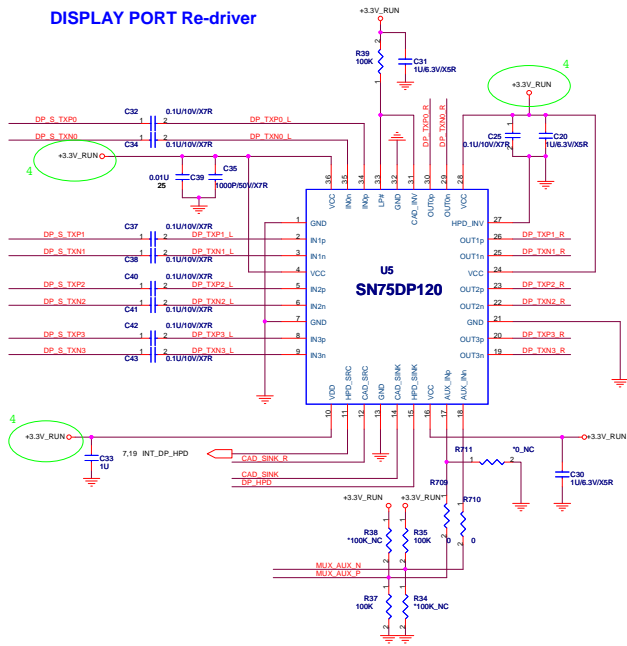
**HDMI**



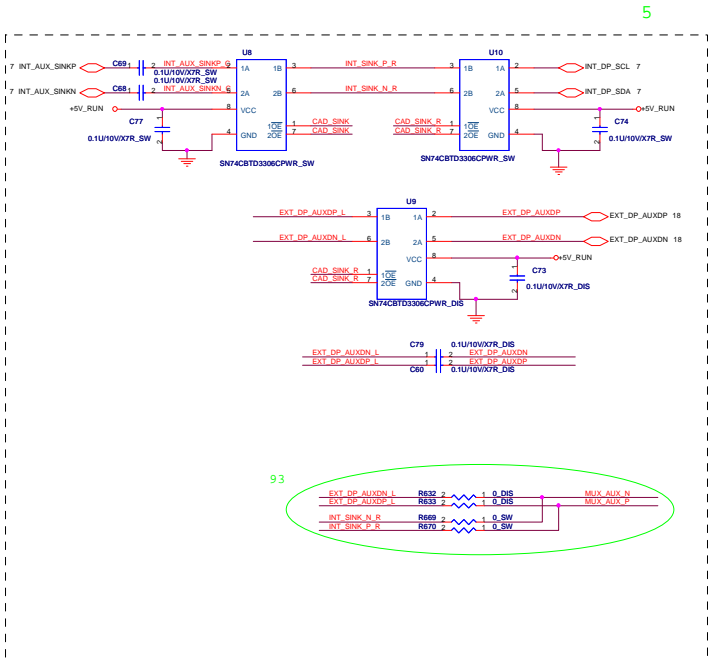
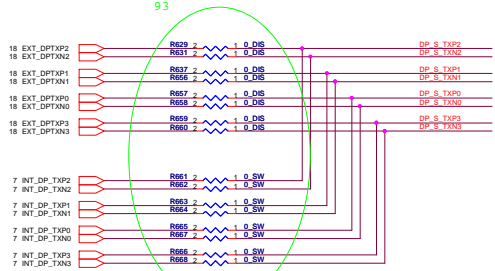
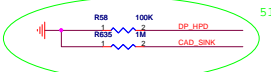
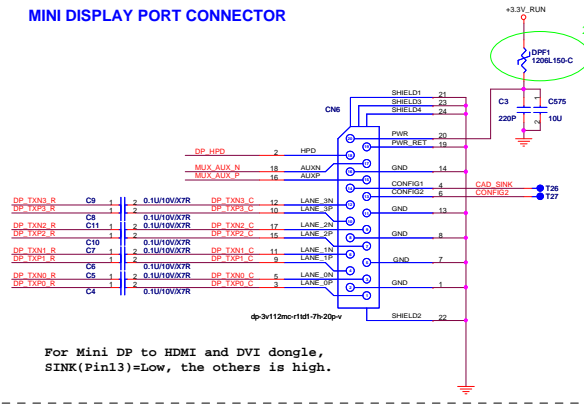
HDMI CONN		
Size	Document Number	Rev
	GM6	2B
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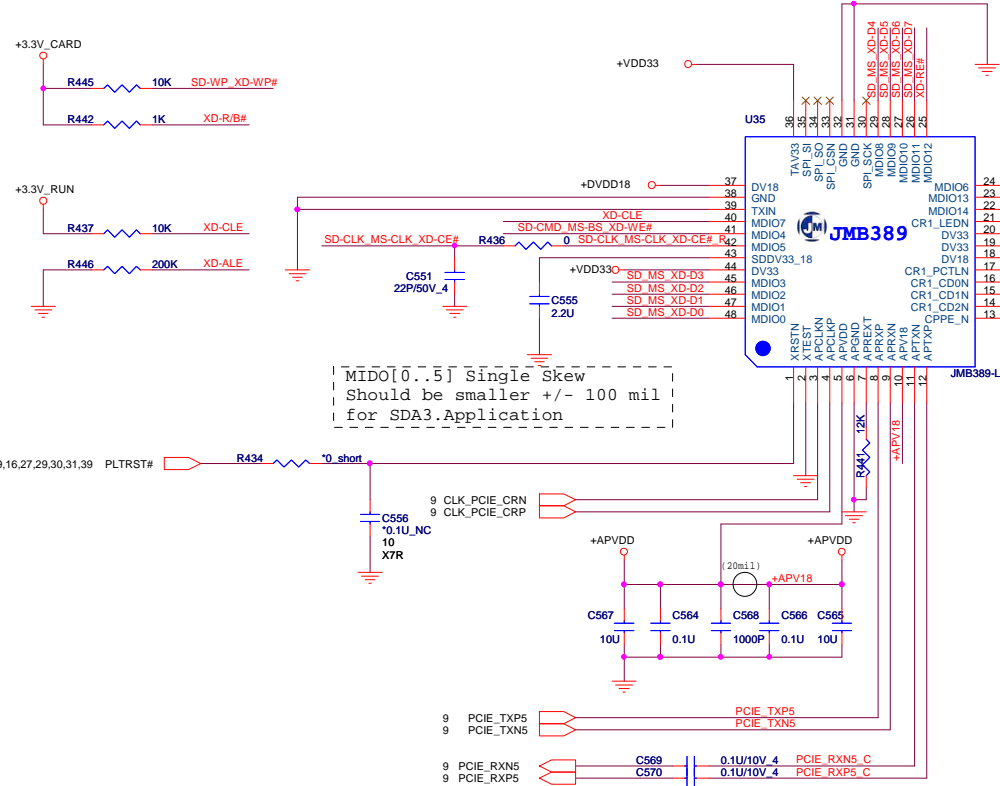
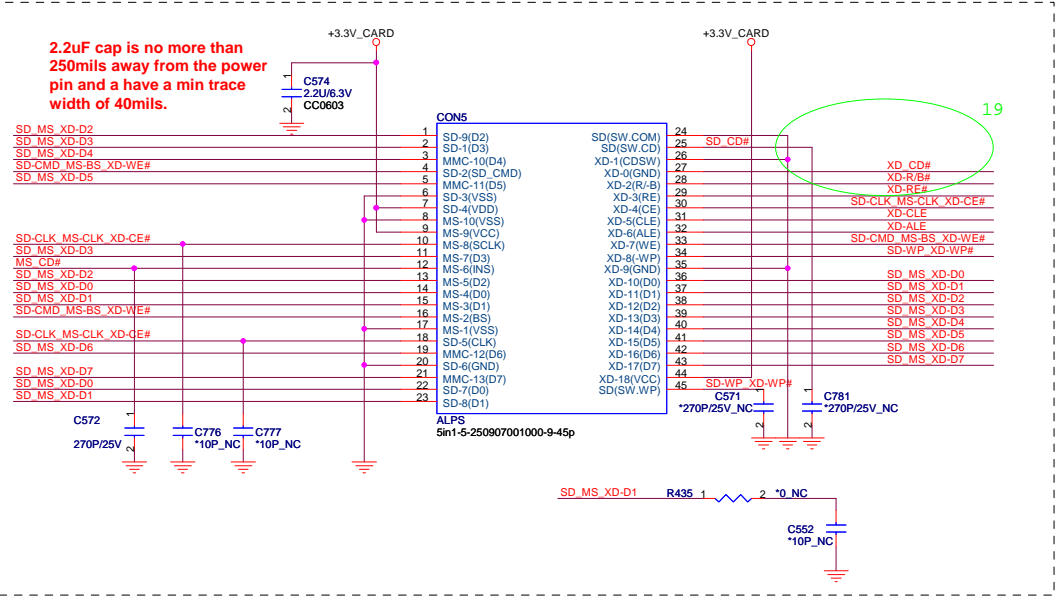
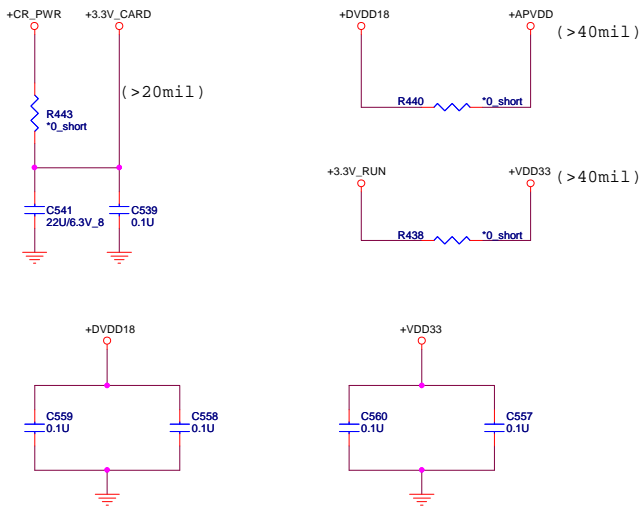
### DISPLAY PORT Re-driver



### MINI DISPLAY PORT CONNECTOR



OE	Output
L	A=B
H	Z



MIDO Single End = 50 ohm

Needs close to Pin17: 12mil/<250mil  
 Layout Note:  
 Place this cap close to pin 18

Card Reader interface signal mapping

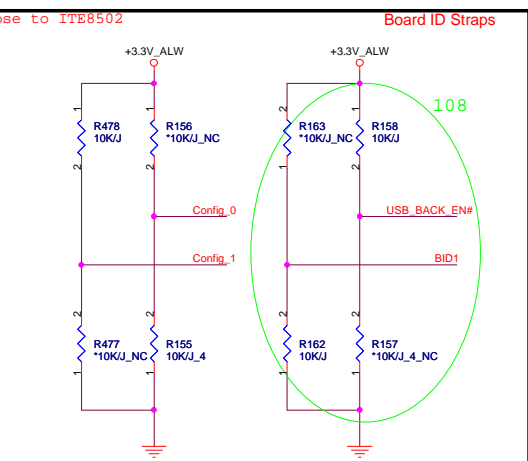
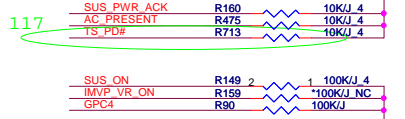
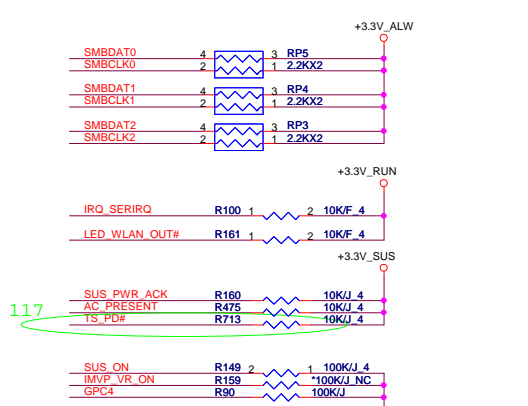
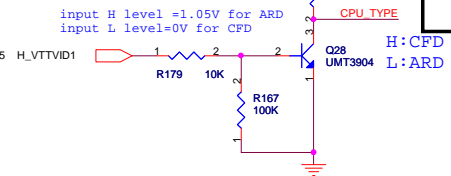
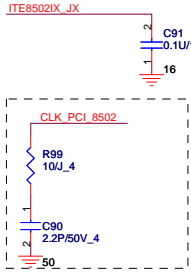
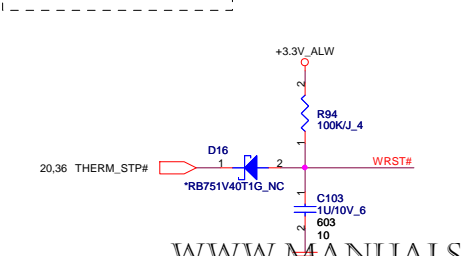
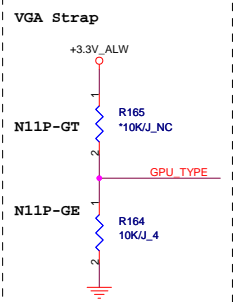
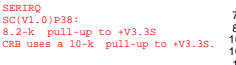
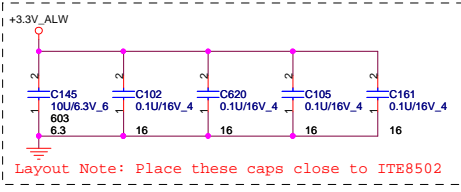
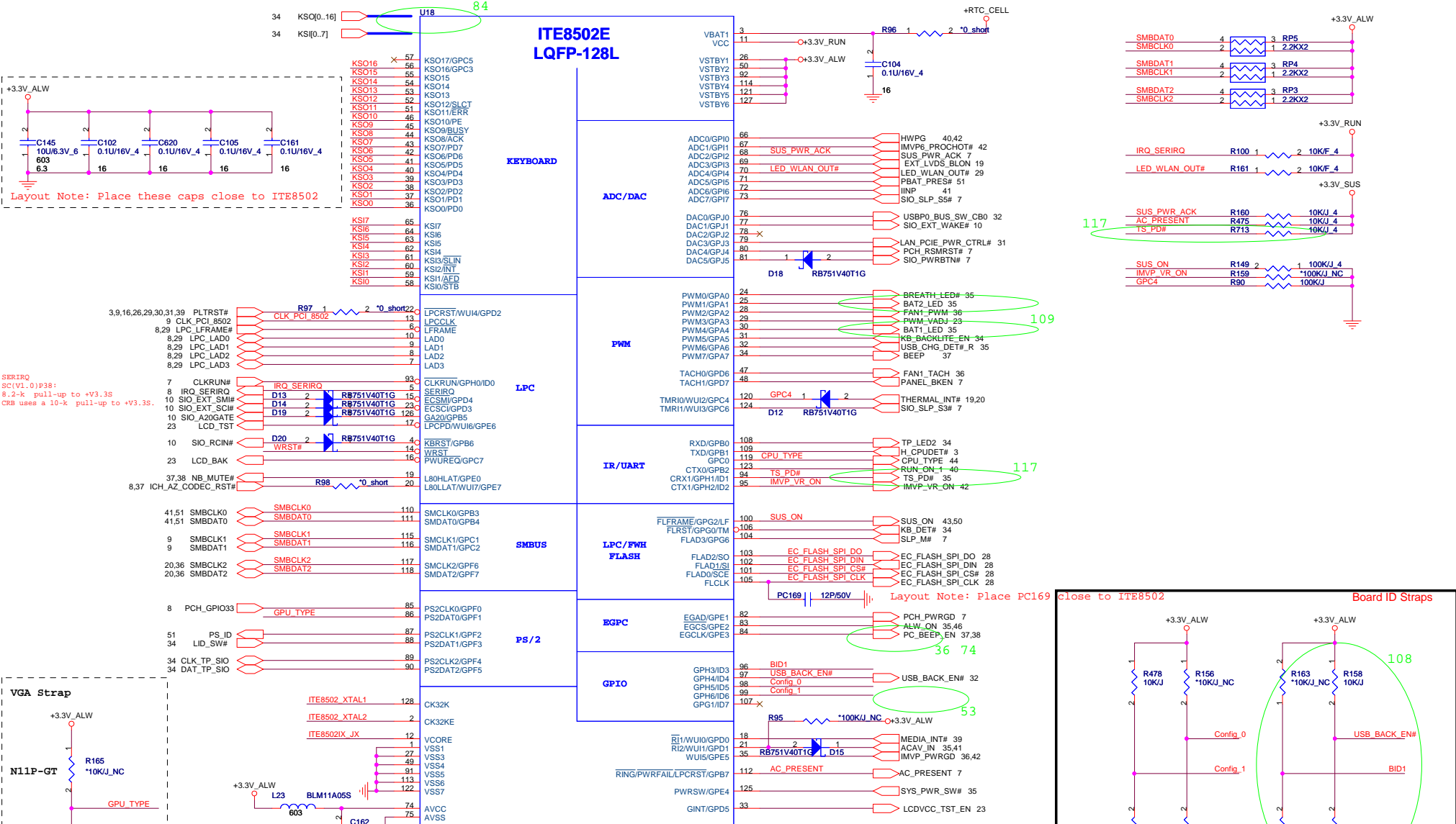
PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MSxD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
E3_LRDW		SD_LRDW	MS_LRDW	XD_LRDW
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		XD_CD#
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

**QUANTA COMPUTER**

Title: Card Reader 8 IN 1

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CHECK MAIL 11/25 1101

Config_0	Config_1	GM6/GM6B	USB_BACK_EN#	BID1	GM6/GM6B
0	0	UMA	0	1	SS1 (X01)
0	0	Studio Switchable	1	0	PT (X01)
0	0	Studio Discrete	1	1	ST (X02)
1	0		0	0	Q1 (A00)
			0	0	(A01)

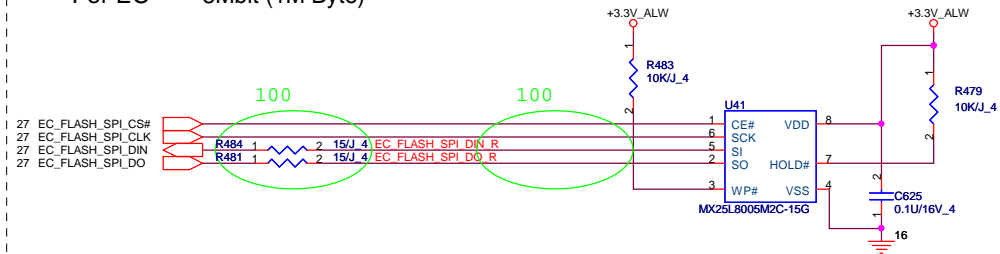


Title: Ultra IO Controller ECE5028

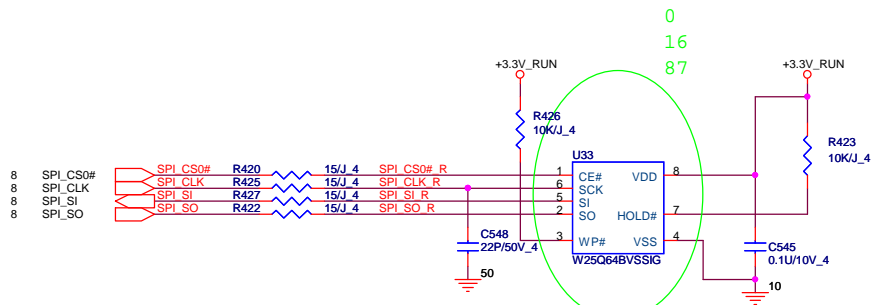
Size: Document Number GM6 Rev 2B

Date: Friday, June 25, 2010 Sheet 27 of 63

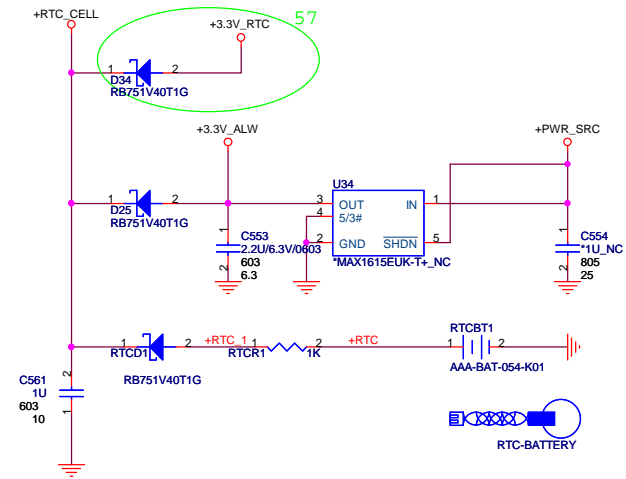
For EC 8Mbit (1M Byte)



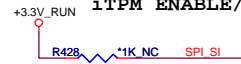
For PCH 32Mbit (4M Byte)



RTC BATTERY



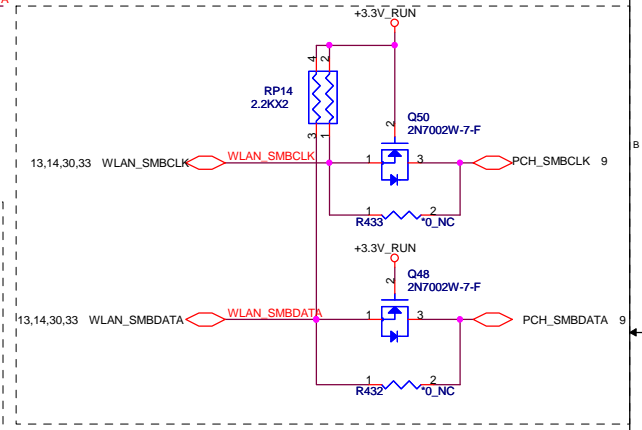
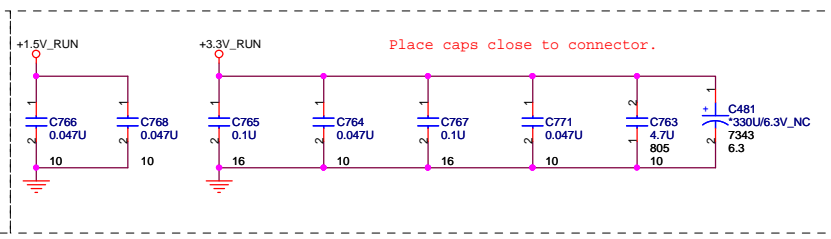
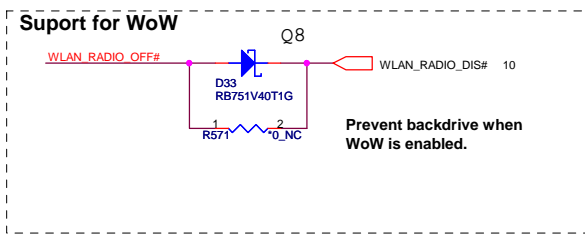
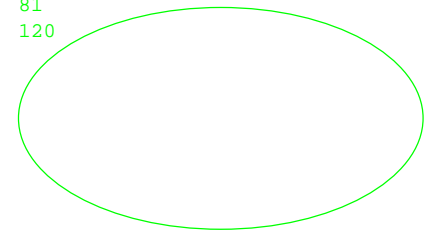
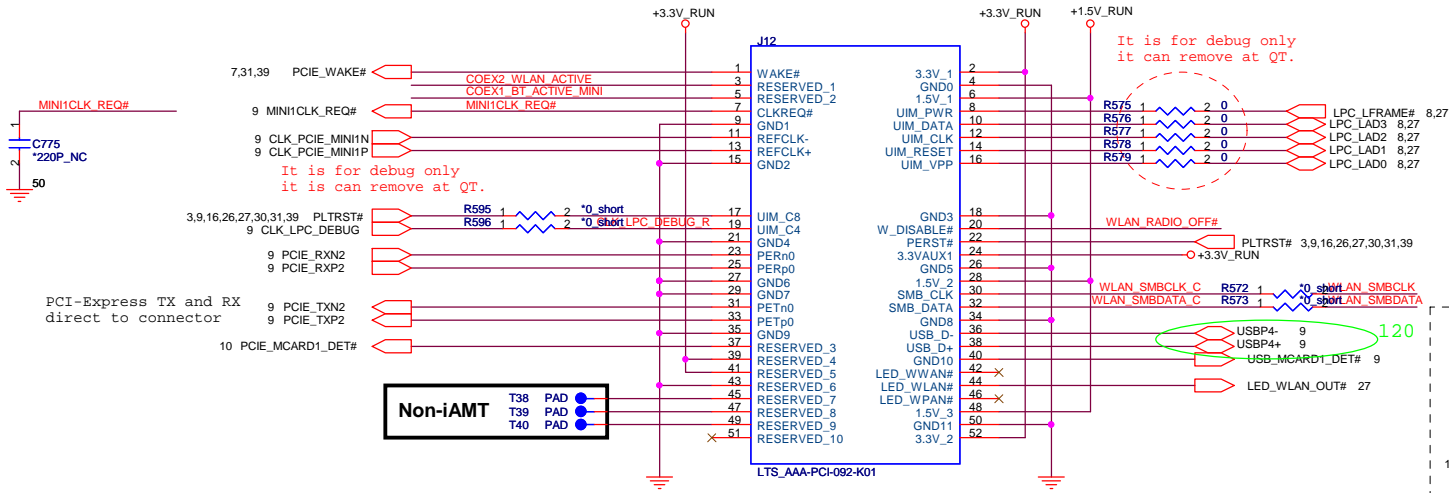
iTPM ENABLE/DISABLE



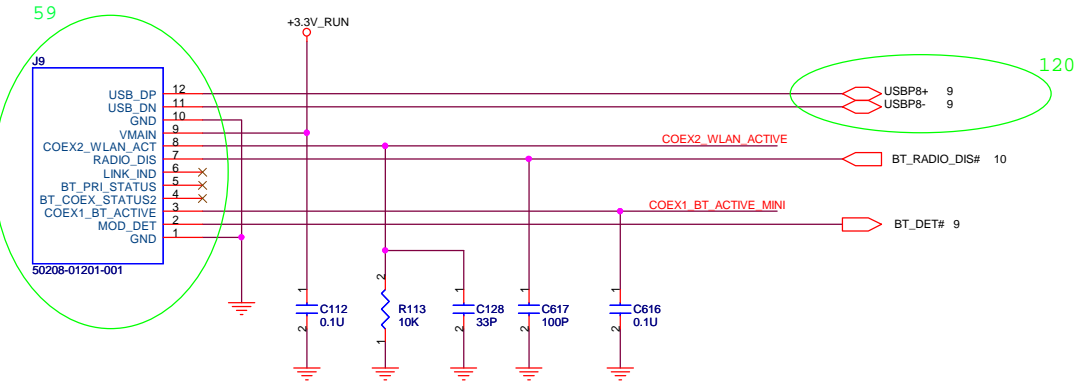
TPM Function	R428
Enable	Mount
Disable	NC (Default)

# MiniCard WLAN connector

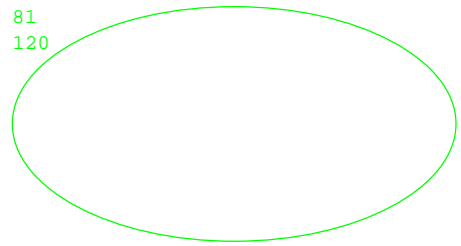
55  
81  
120



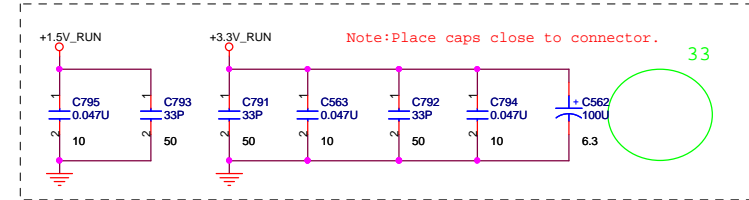
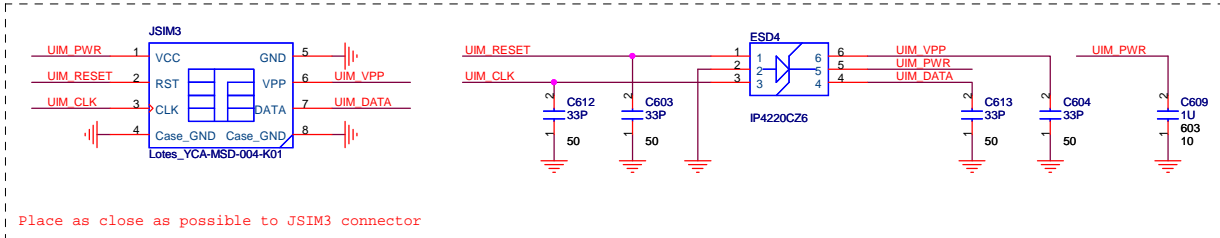
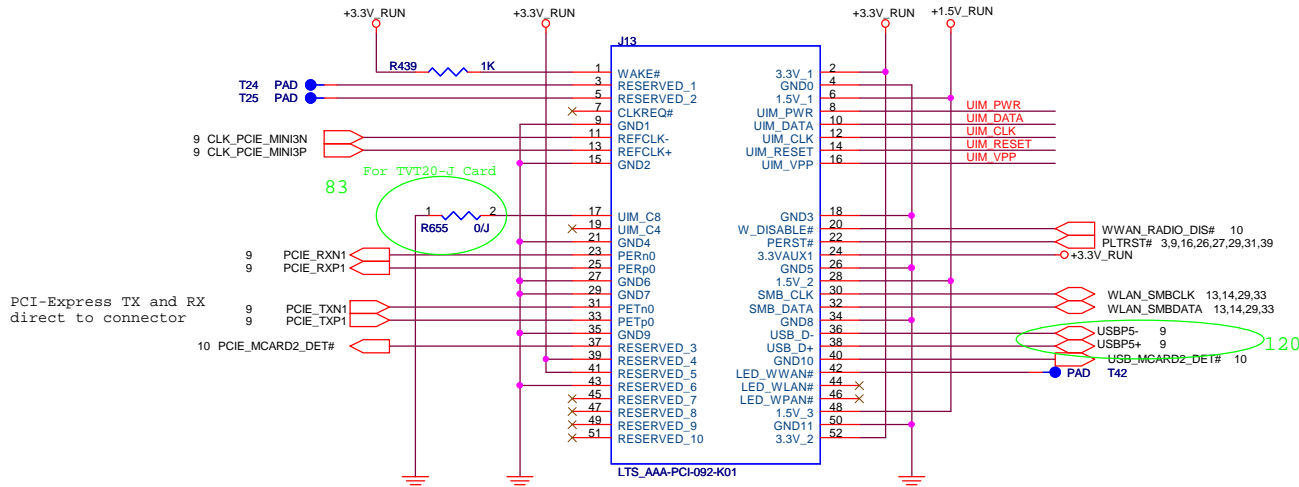
## Support Dell BT375 (Little Stone) module (XPS) W TO B

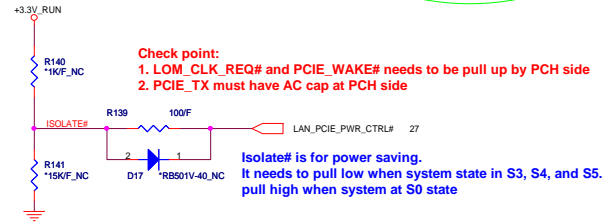
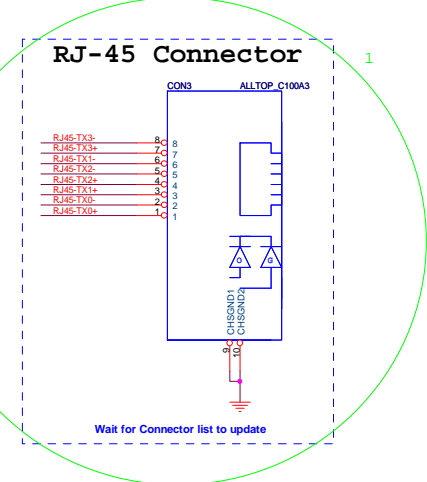
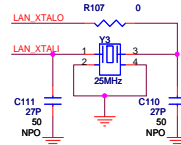
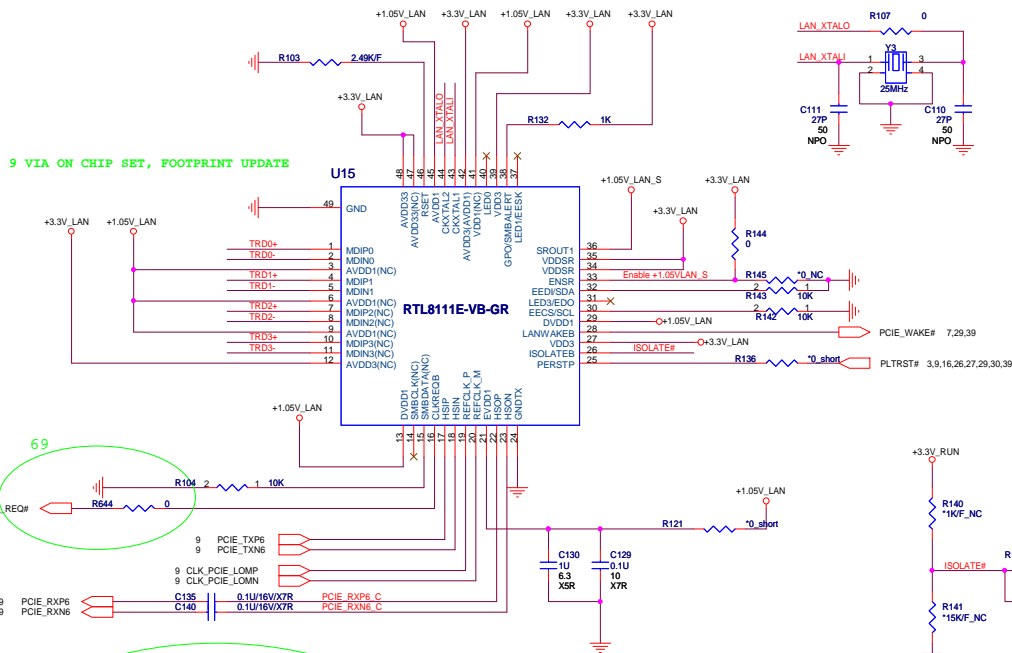
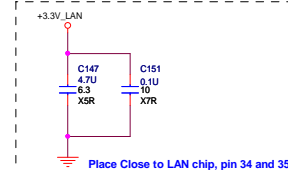
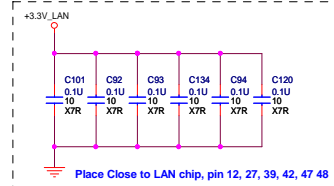
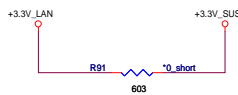
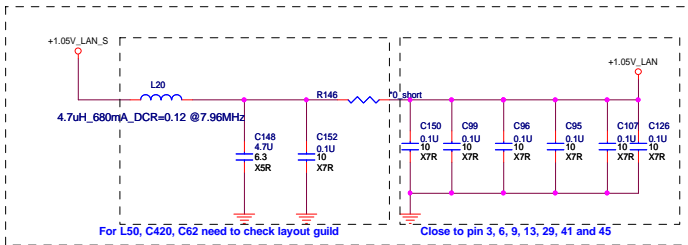


55  
81  
120

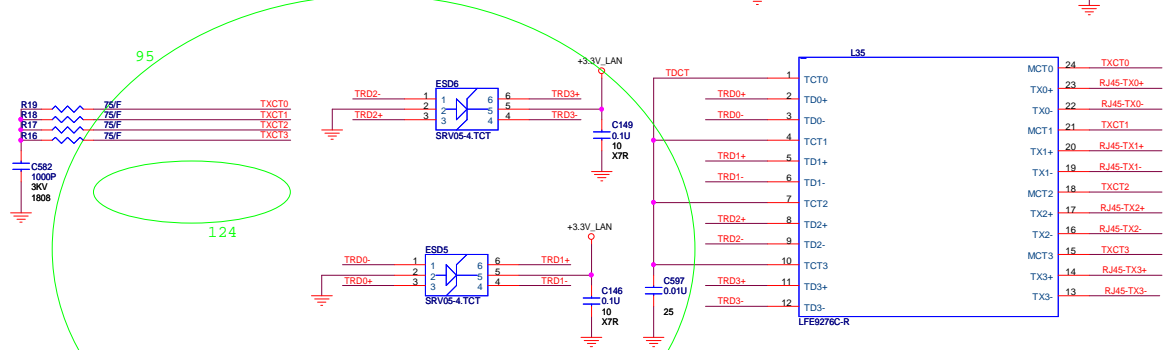


## MiniCard WWAN connector

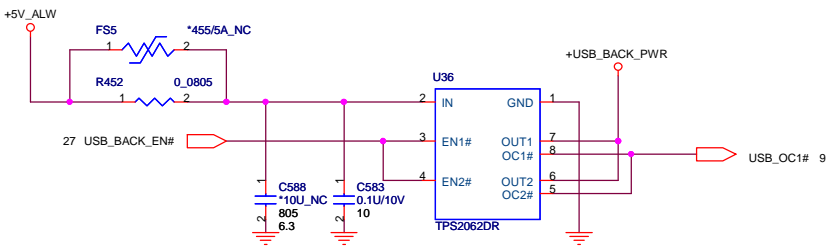




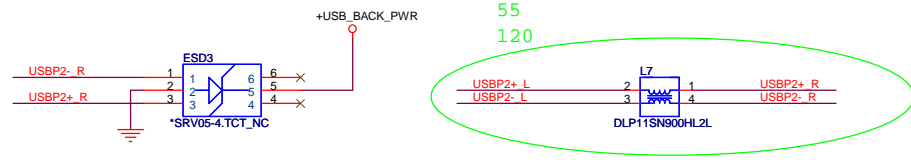
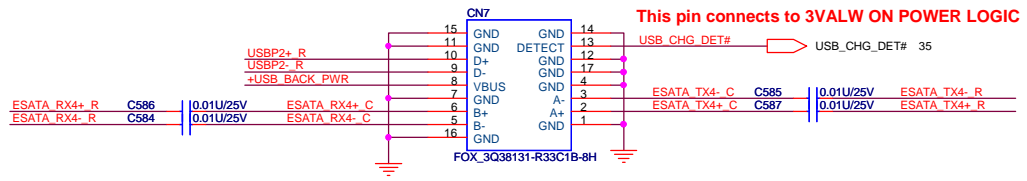
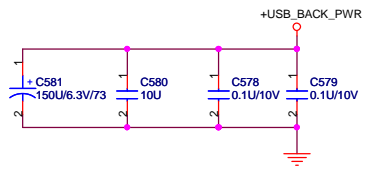
**Check point:**  
 1. LOM\_CLK\_REQ# and PCIE\_WAKE# needs to be pull up by PCH side  
 2. PCIE\_TX must have AC cap at PCH side



# ESATA + USB Conn + Power Share

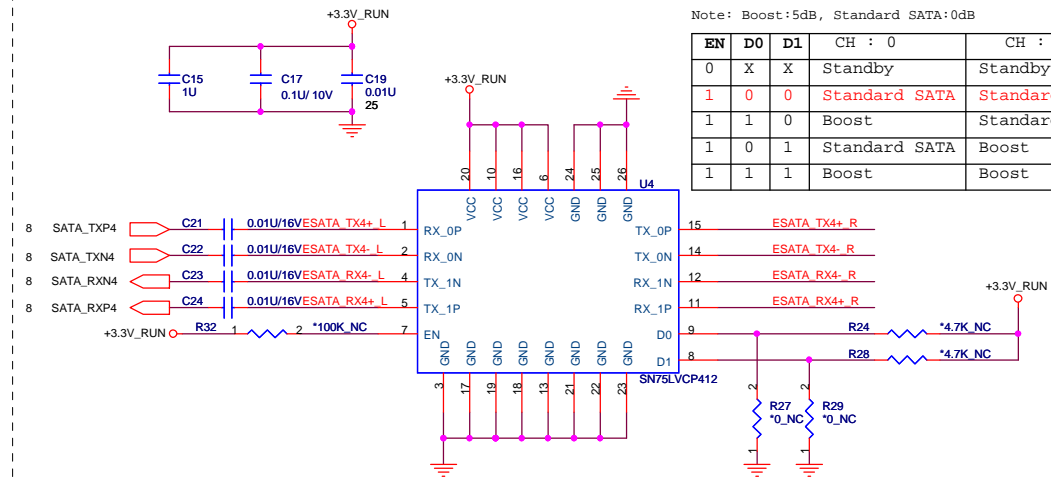


USB\_BACK\_EN# needs to be low when system S3 and S5 for USB charge



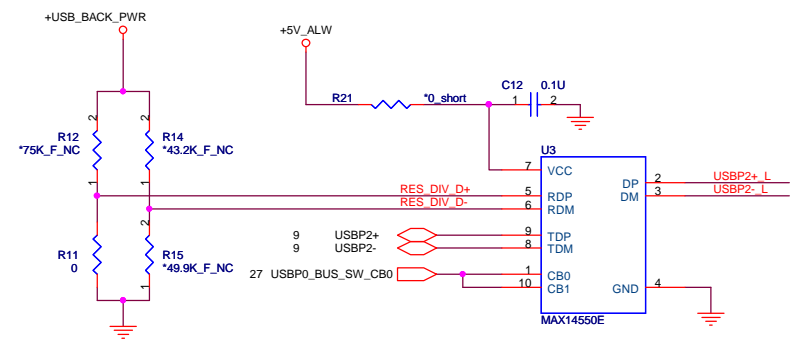
## E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



EC needs to drive CB0/CB1 pins to low when system S3/S5 and drive high when system S0.

U49 PN and Footprint needs to double check

R15 needs to be 49.9K\_F if we use external resistors.

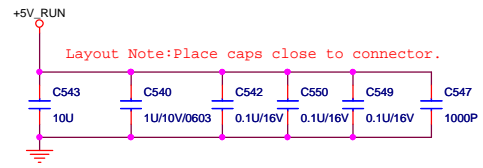
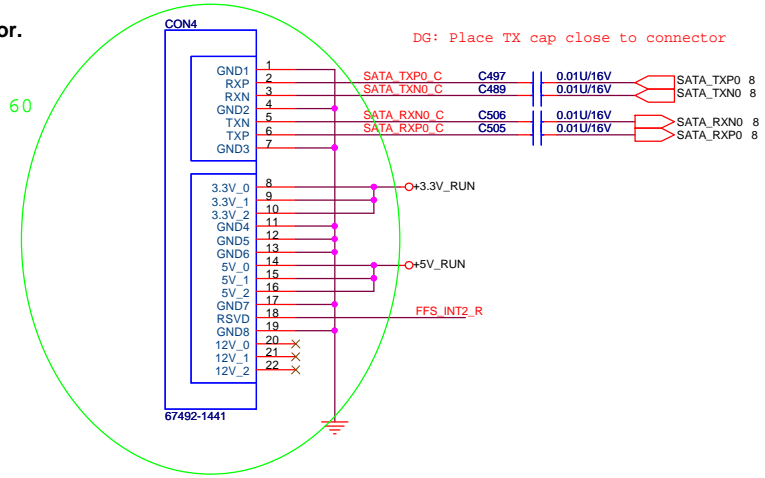
CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)  
 (5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

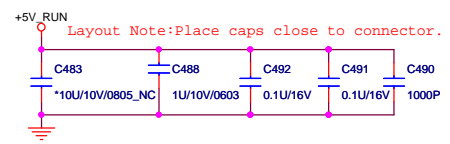
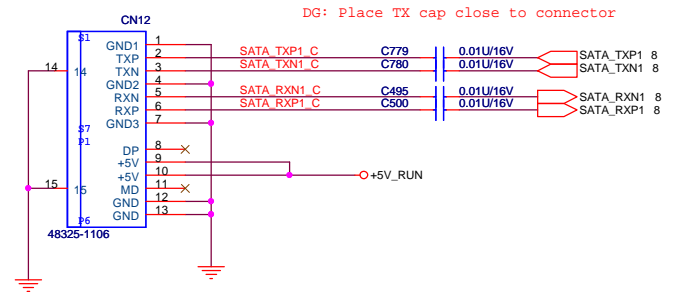




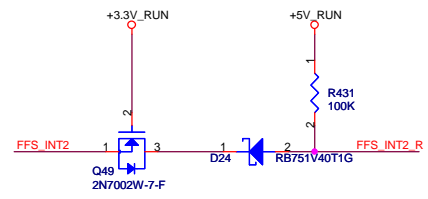
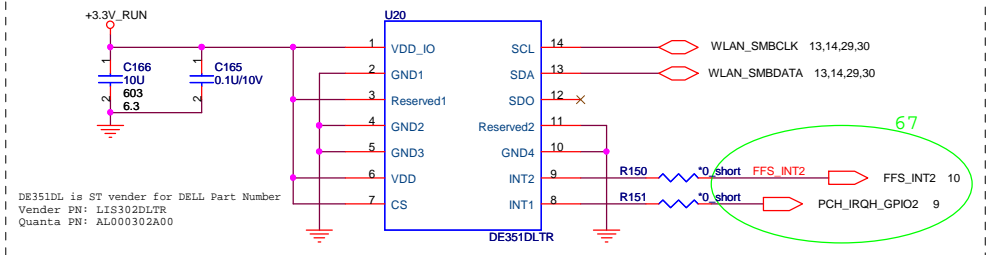
# SATA Connector.



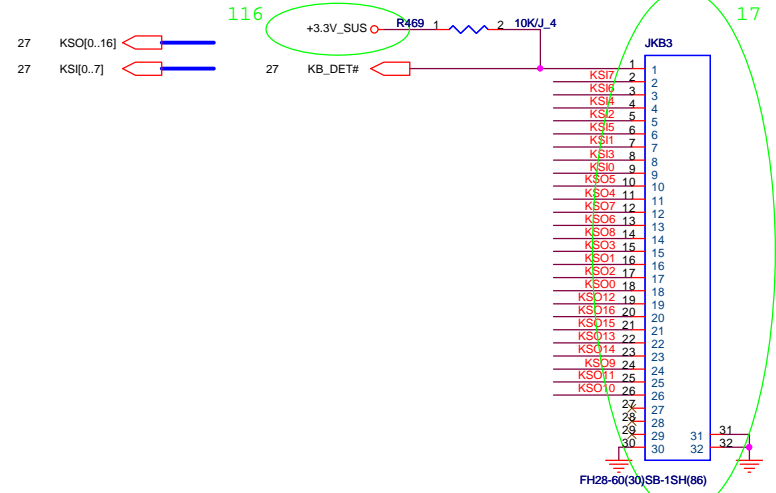
# ODD Connector



# 3-axis Fall Sensor (HDD data protector)

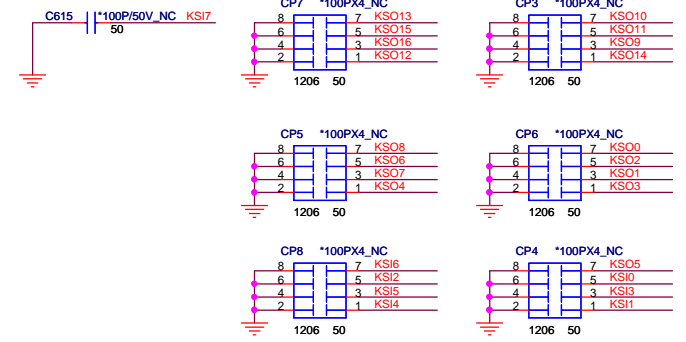
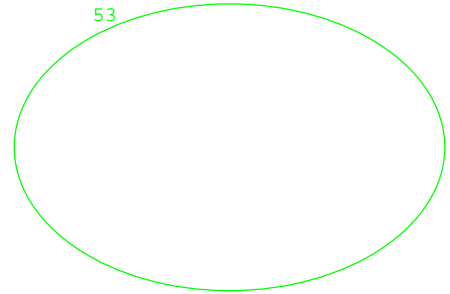
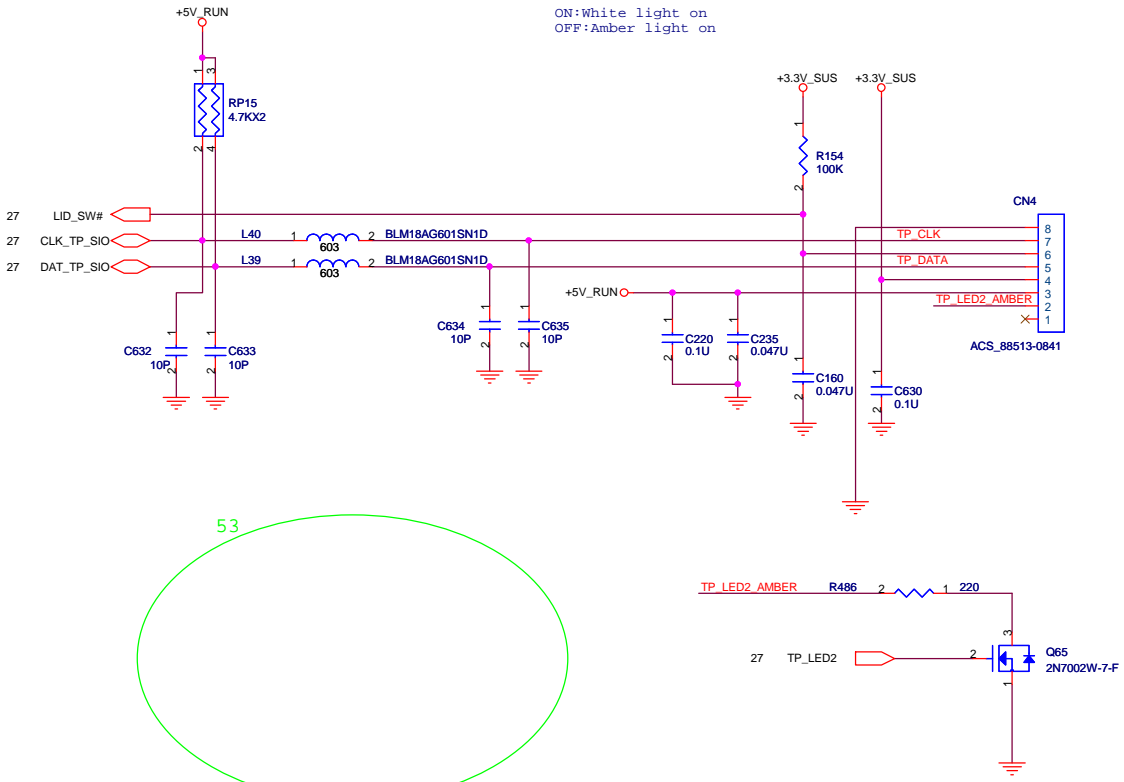


# KEYBOARD CONNECTOR



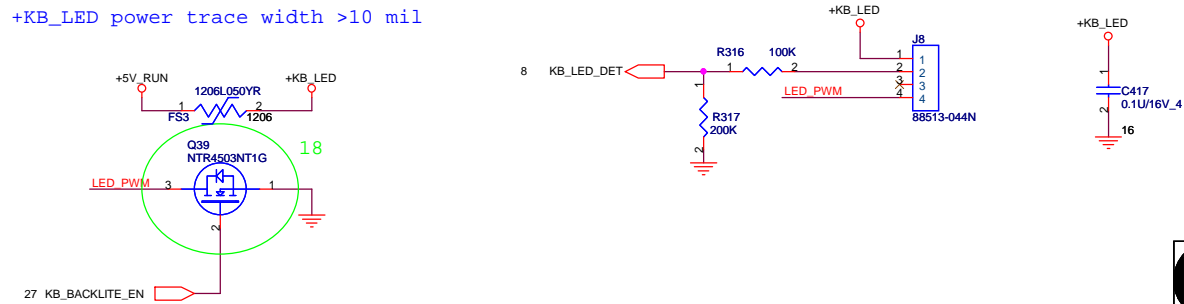
# Touch Pad

ON: White light on  
OFF: Amber light on



# Key board illumination

+KB\_LED power trace width >10 mil

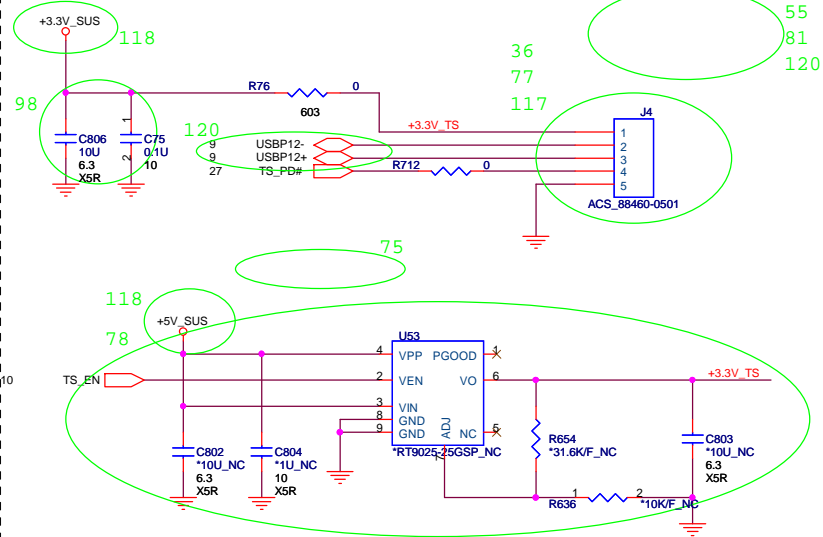


**QUANTA COMPUTER**

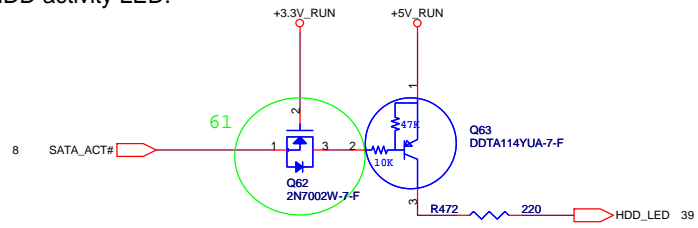
Title: TOUCH PAD, BULE TOOTH & FIR

Size: Document Number GM6	Rev: 2B
Date: Friday, June 25, 2010	
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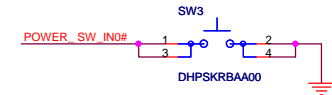
# Touch Screen Module



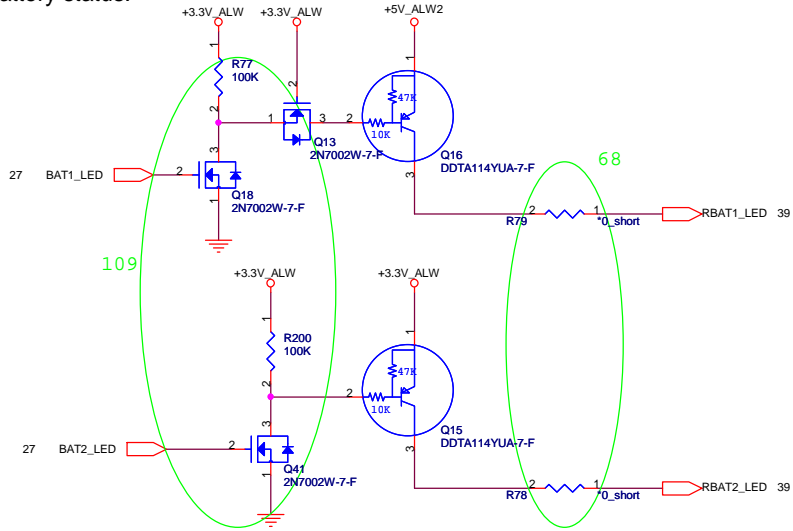
# HDD activity LED.



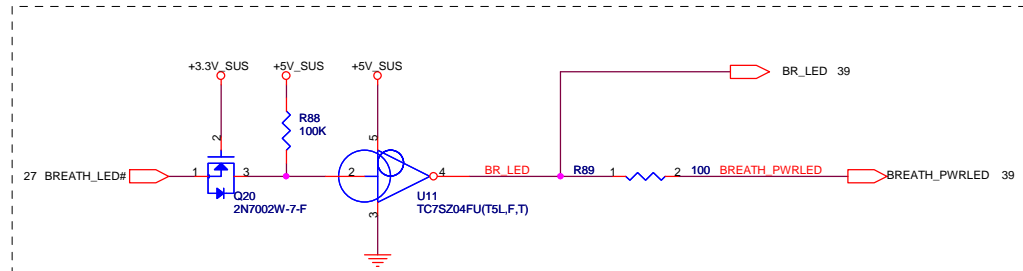
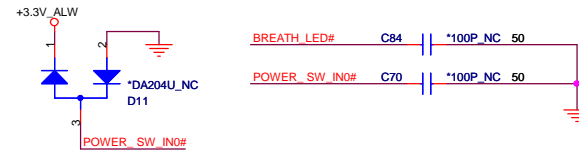
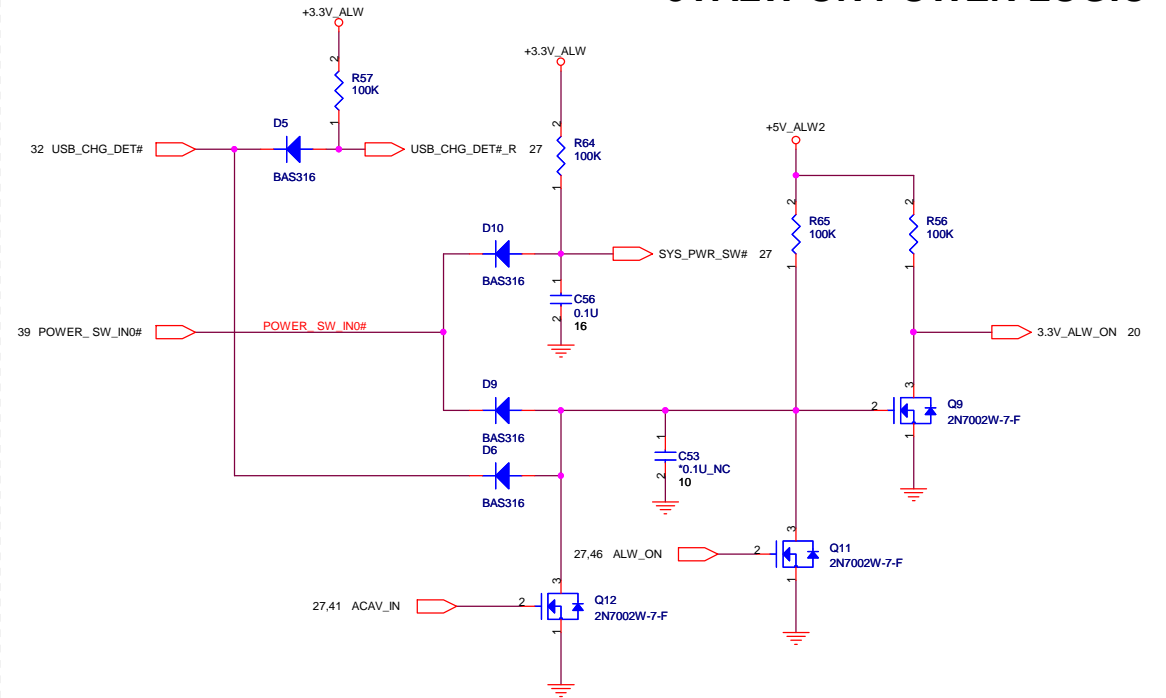
# Power button for Engineer



# Battery status.



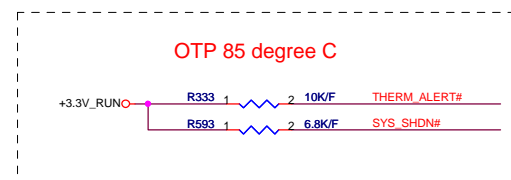
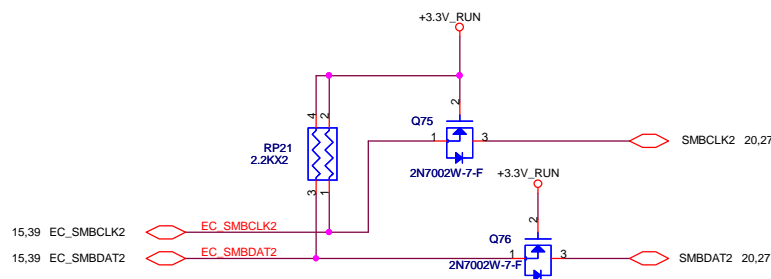
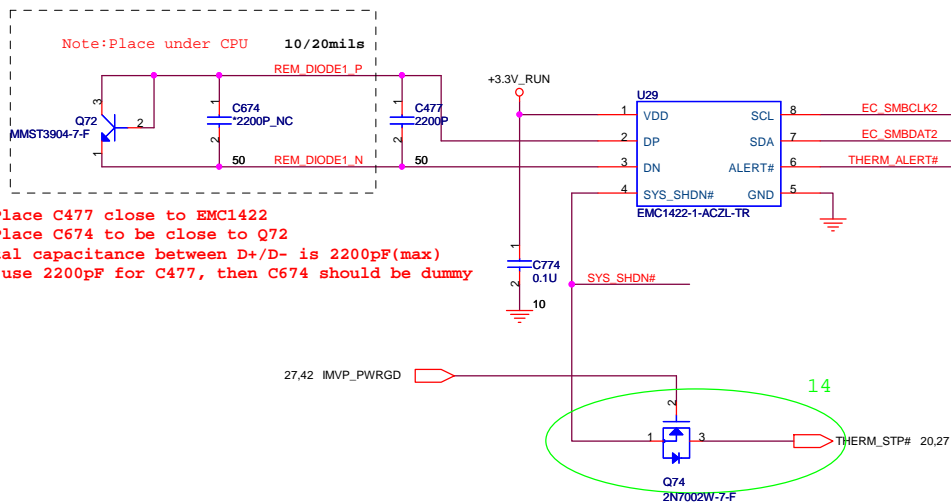
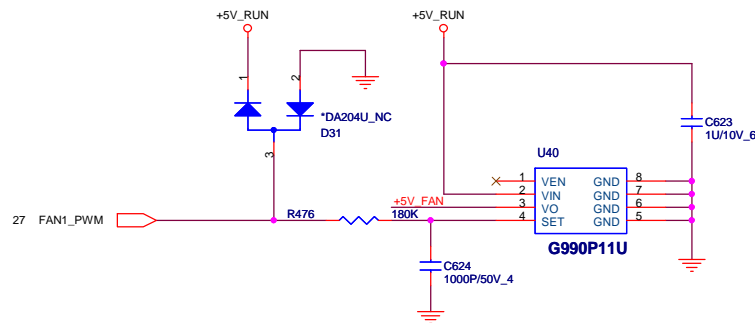
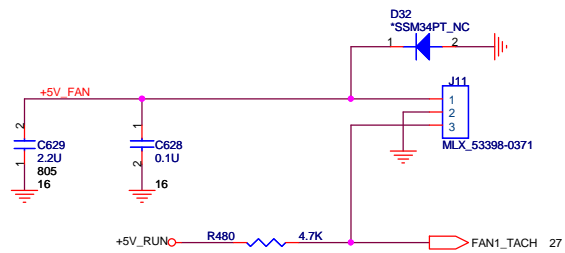
# 3VALW ON POWER LOGIC



WWW.MANUALS-CLAN.SU

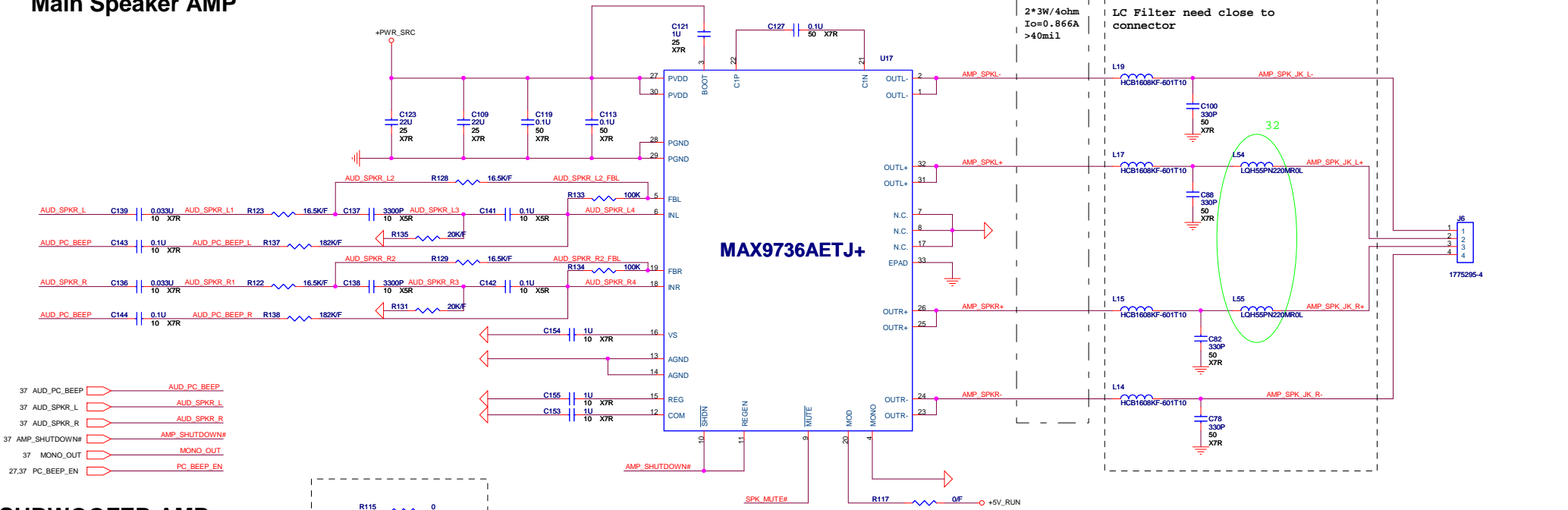


Title SWITCH, KEYBOARD & LED&Touch Screen Module		
Size GM6	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 35	of 63

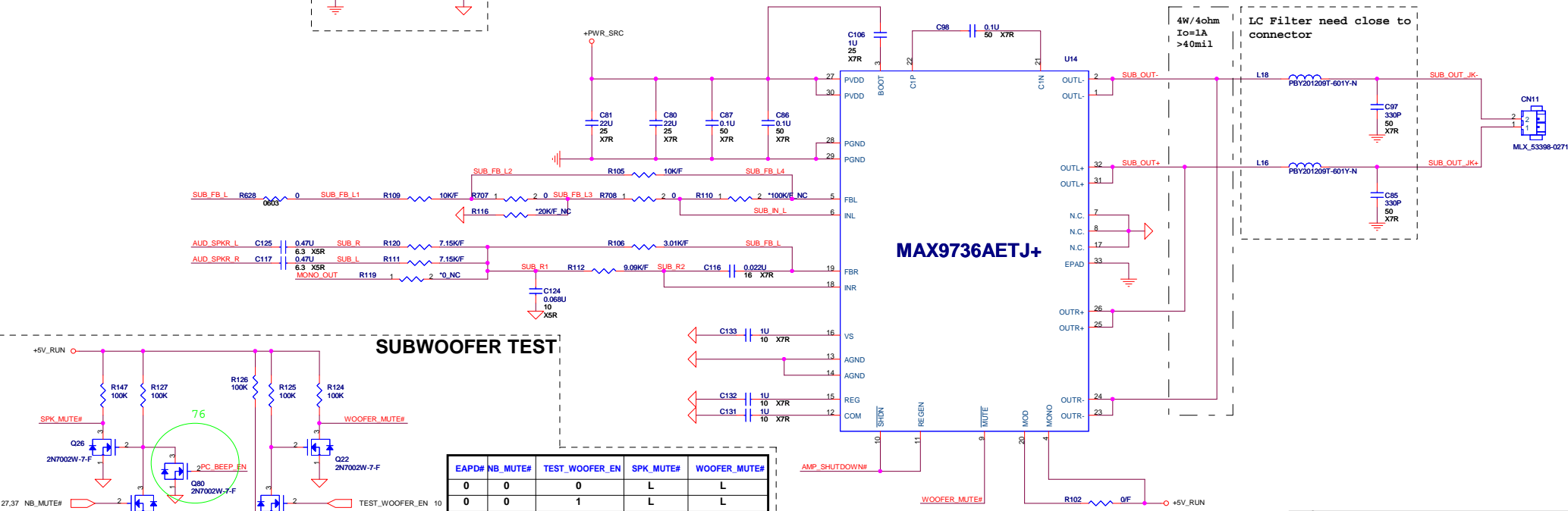




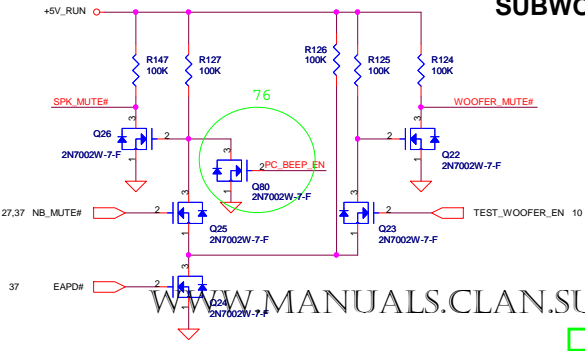
# Main Speaker AMP



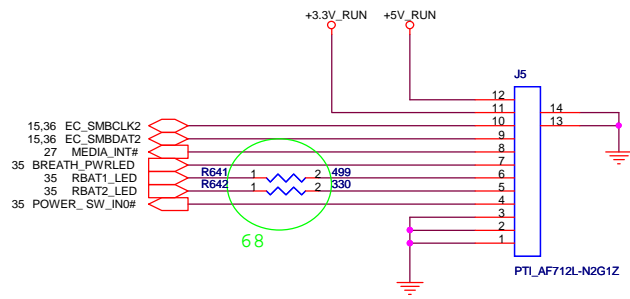
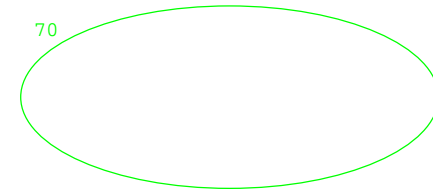
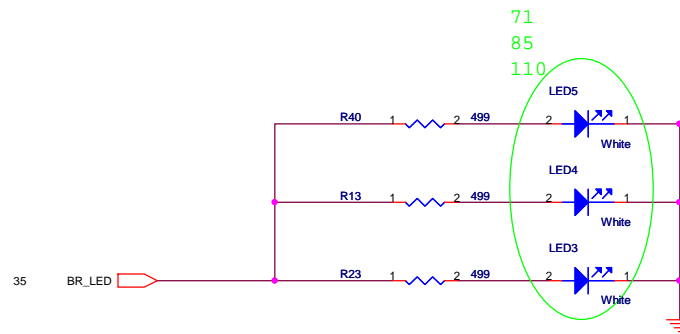
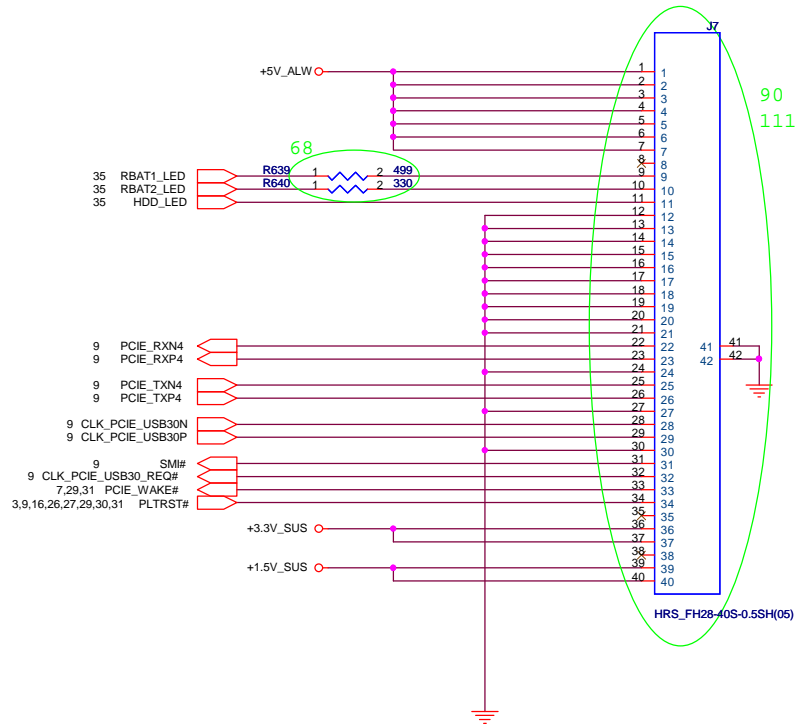
# SUBWOOFER AMP

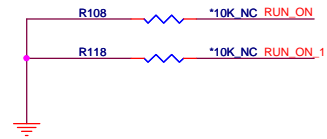
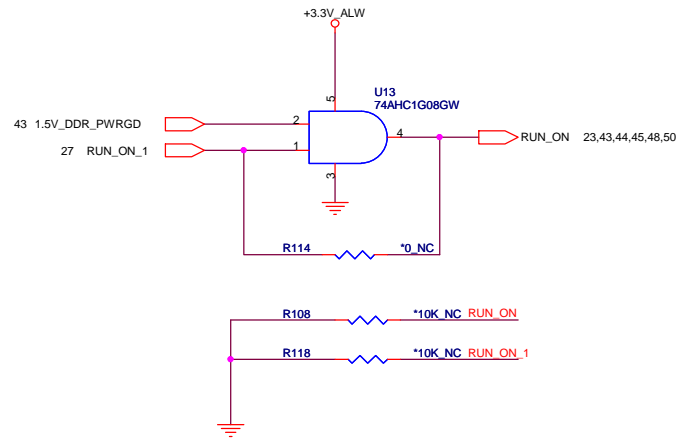
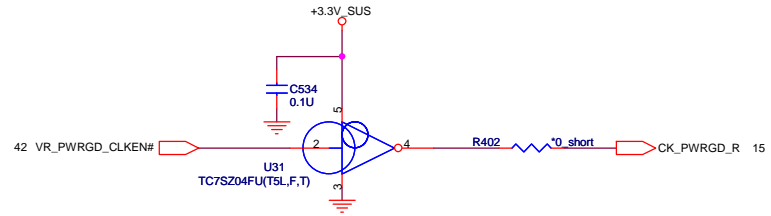
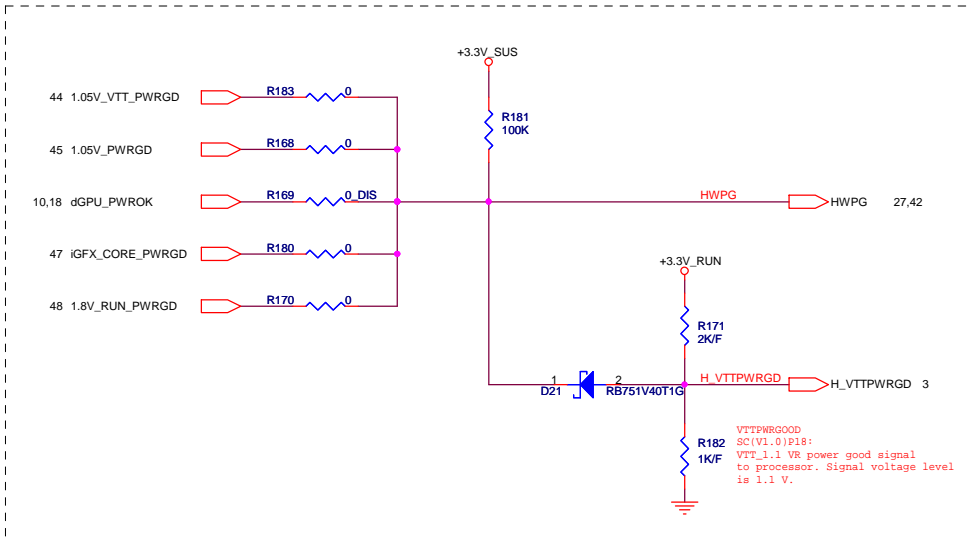


# SUBWOOFER TEST



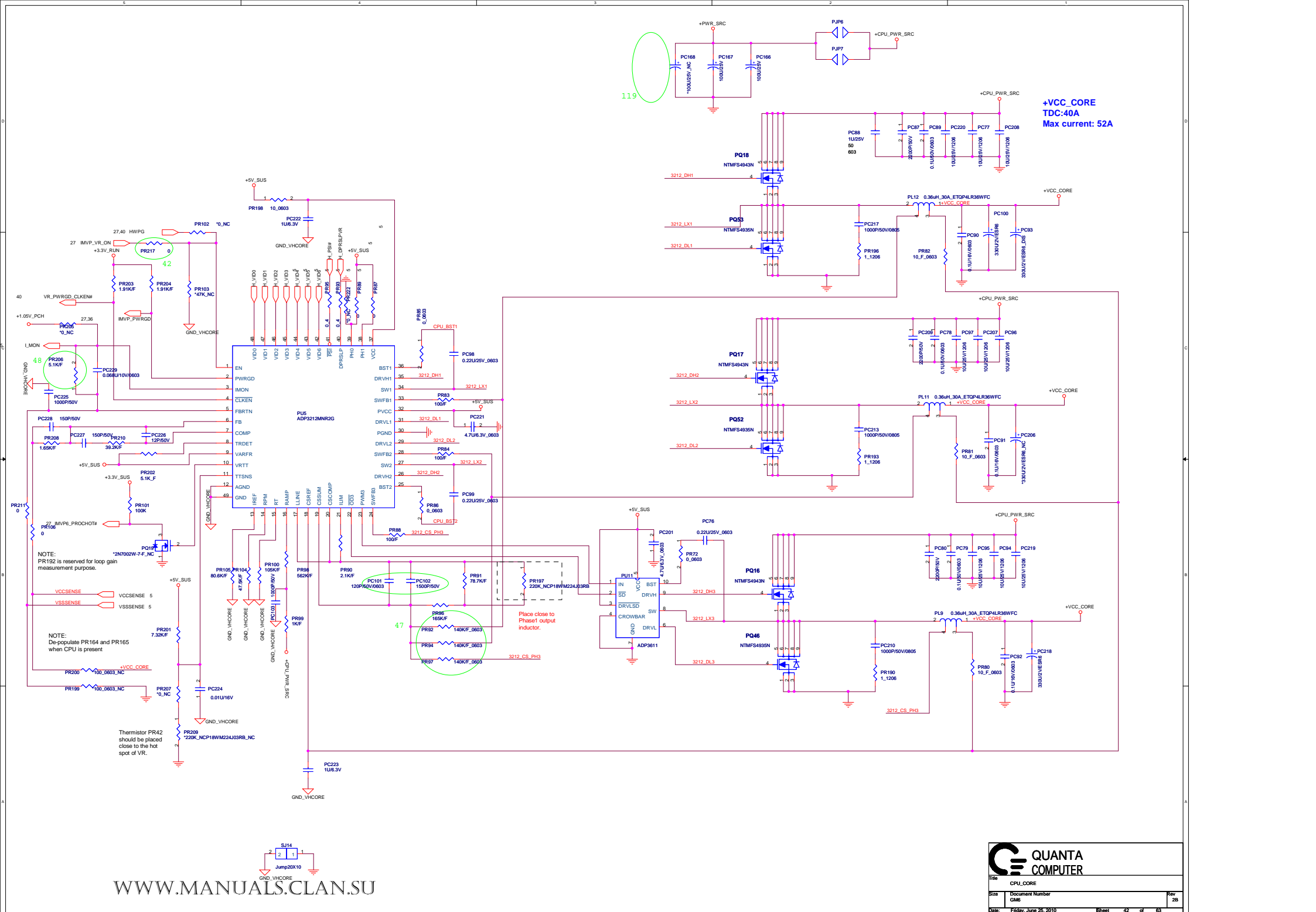
EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H



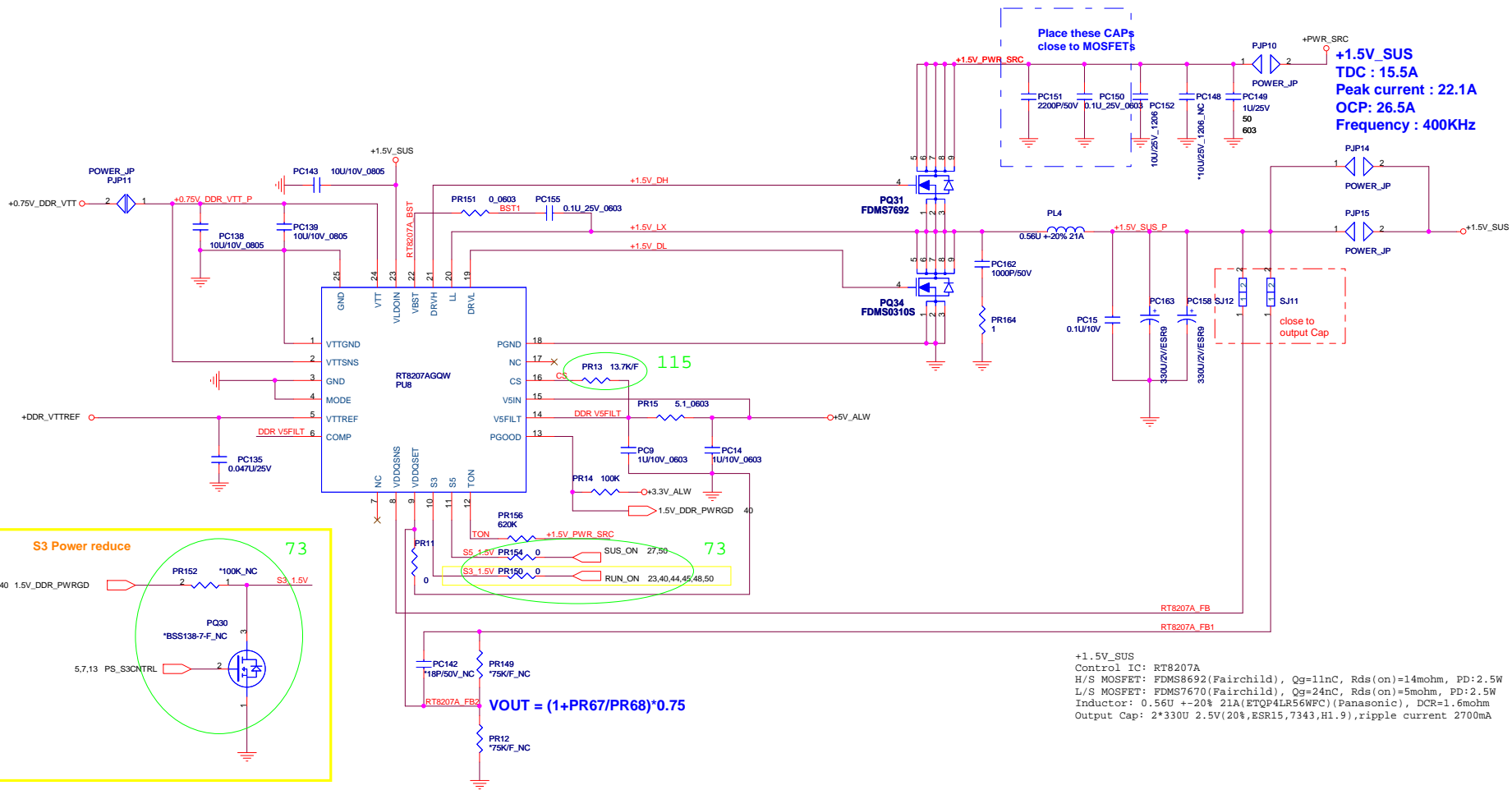




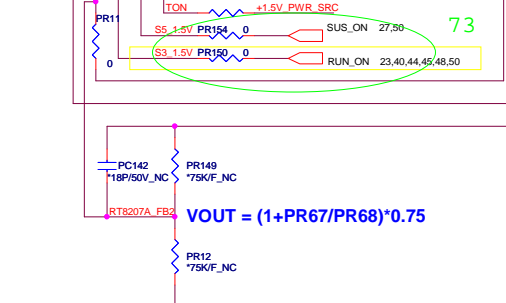
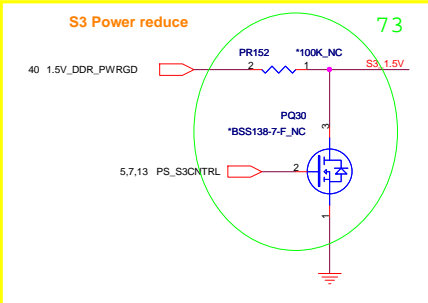




**+VCC\_CORE**  
TDC:40A  
Max current: 52A



**+1.5V\_SUS**  
 TDC : 15.5A  
 Peak current : 22.1A  
 OCP: 26.5A  
 Frequency : 400KHz



+1.5V\_SUS  
 Control IC: RT8207A  
 H/S MOSFET: FDM8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W  
 L/S MOSFET: FDM87670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W  
 Inductor: 0.56U +-20% 21A (ETQP4LR56WFC) (Panasonic), DCR=1.6mohm  
 Output Cap: 2\*330U 2.5V(20%, ESR15, 7343, H1.9), ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

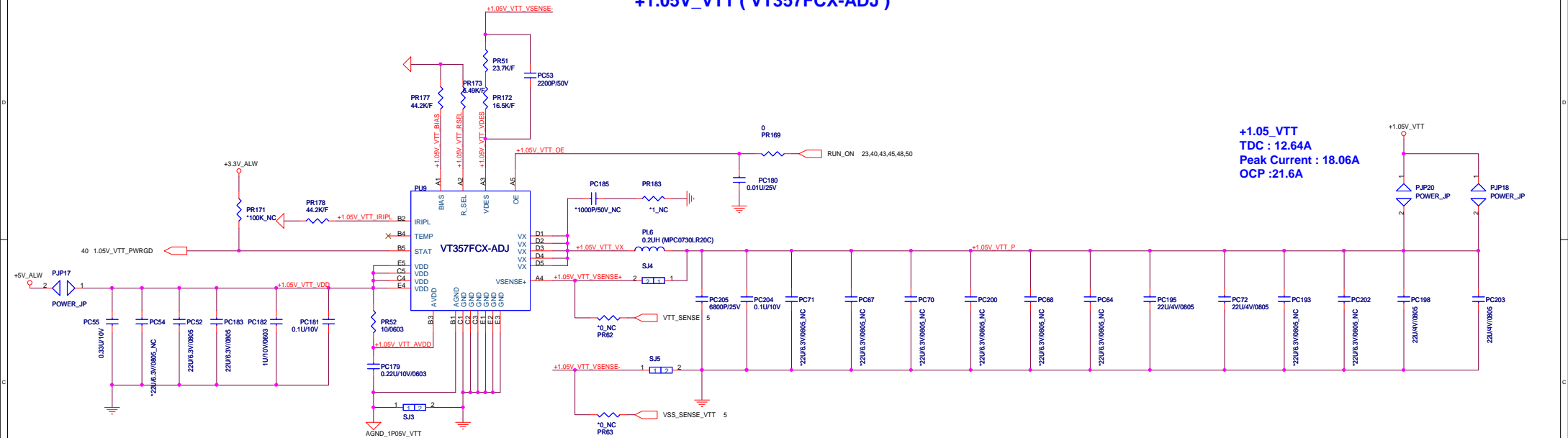
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

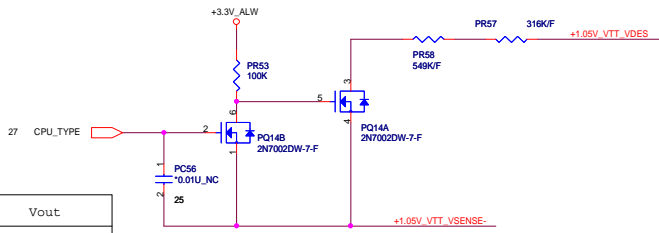
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

# +1.05V\_VTT ( VT357FCX-ADJ )

**+1.05V\_VTT**  
**TDC : 12.64A**  
**Peak Current : 18.06A**  
**OCP : 21.6A**

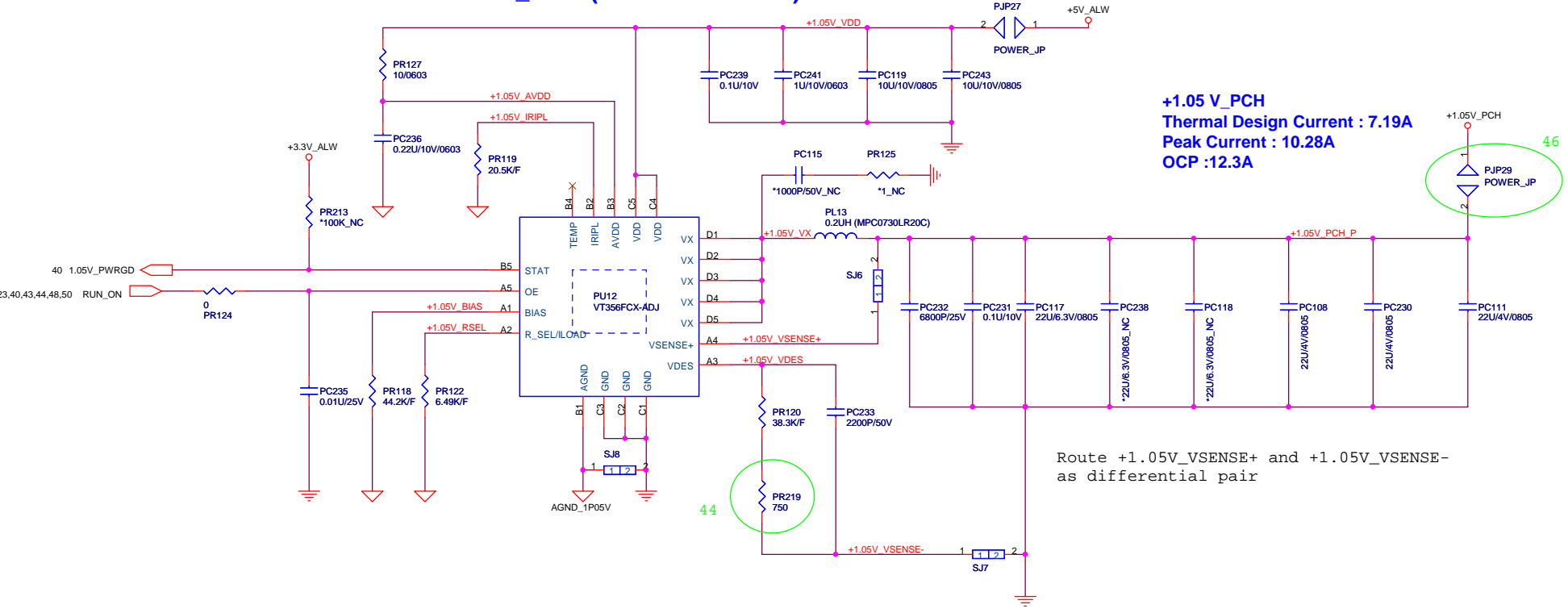


Route +1.05V\_VTT\_VSENSE+ and +1.05V\_VTT\_VSENSE- as differential pair

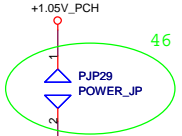


CPU_TYPE	Vout
L	1.05V(ARD)
H	1.1V(CFD)

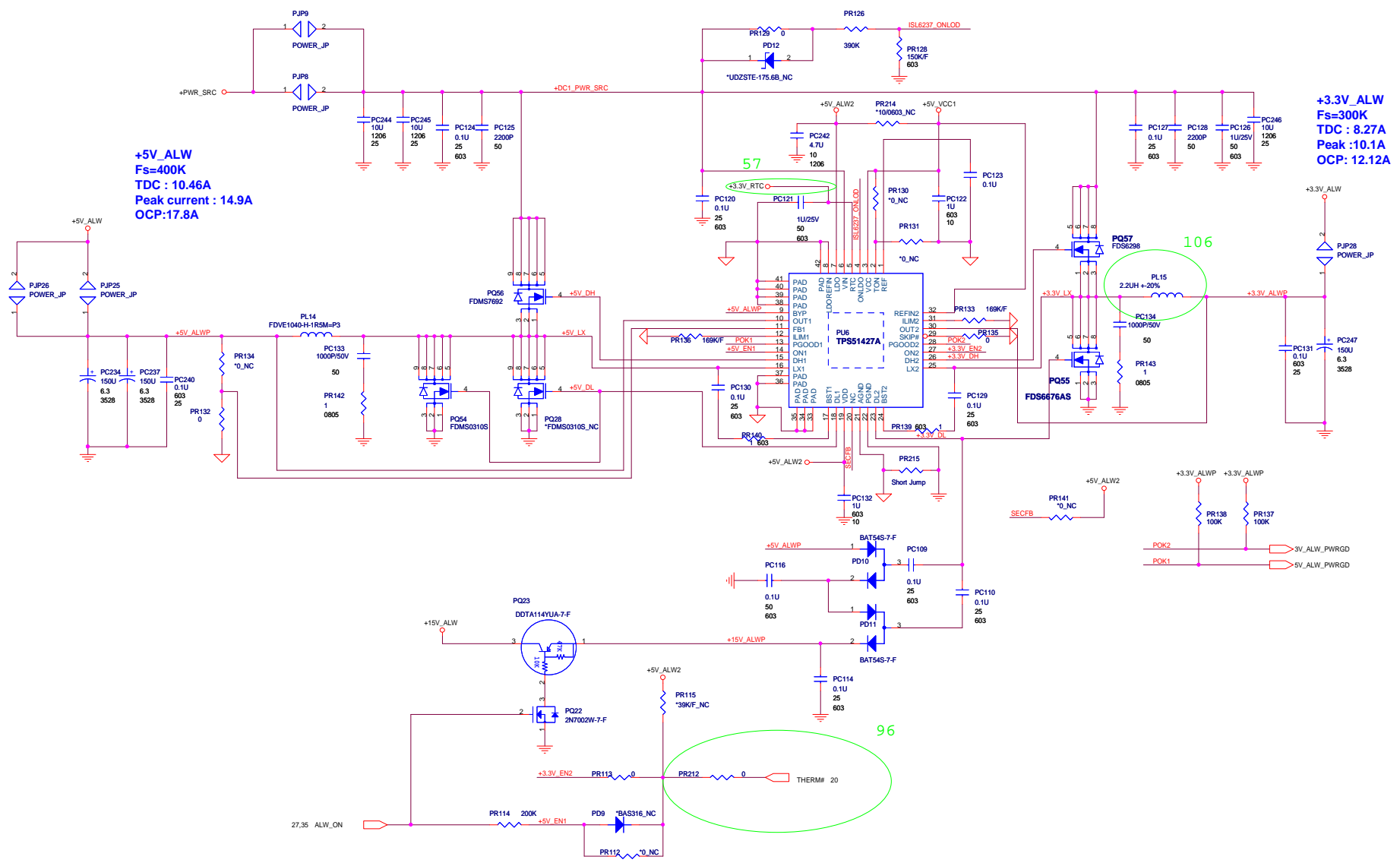
# +1.05V\_PCH ( VT356FCX-ADJ )



**+1.05 V\_PCH**  
**Thermal Design Current : 7.19A**  
**Peak Current : 10.28A**  
**OCP :12.3A**

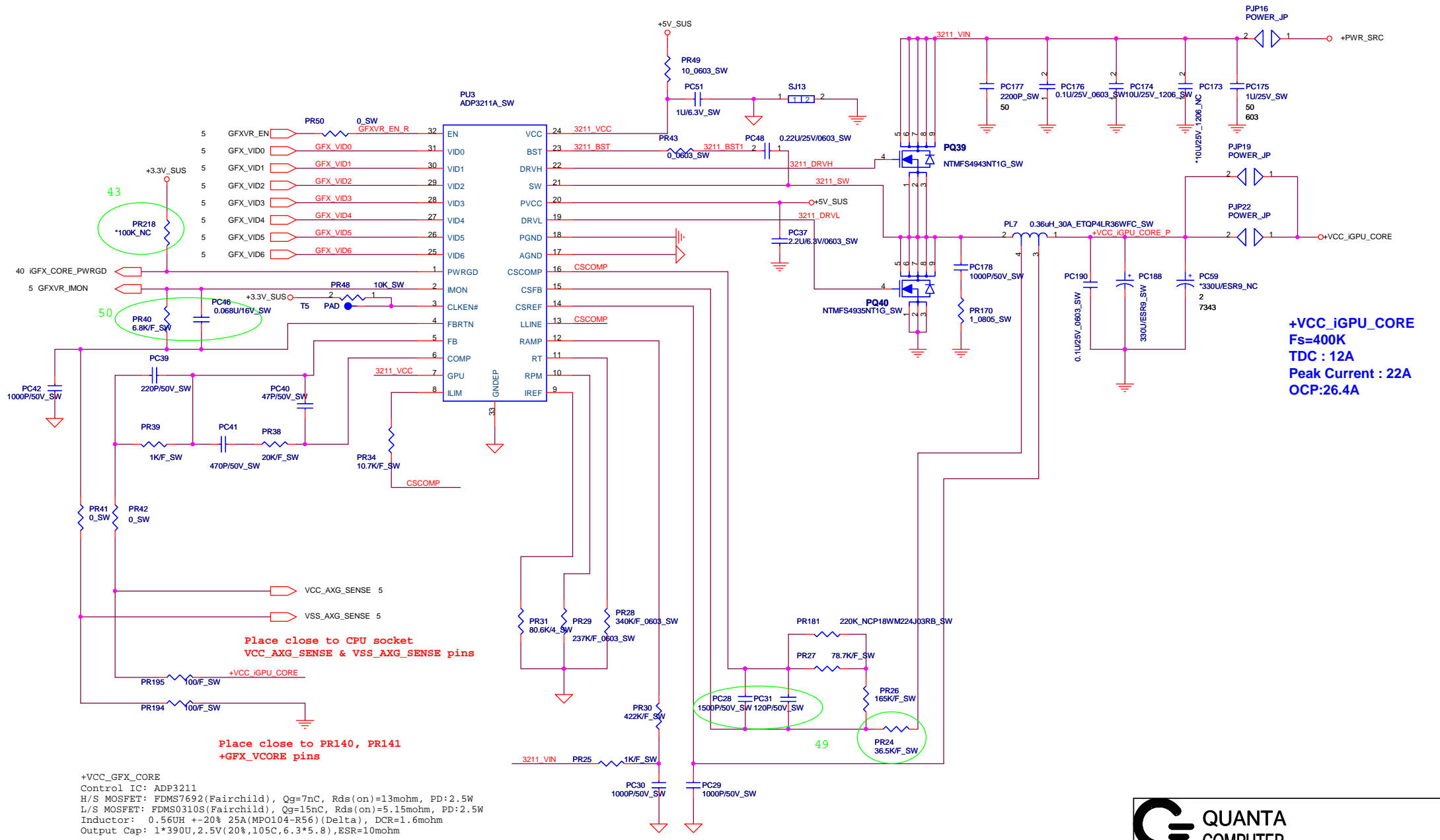


Route +1.05V\_VSENSE+ and +1.05V\_VSENSE- as differential pair



**+5V\_ALW**  
**Fs=400K**  
**TDC : 10.46A**  
**Peak current : 14.9A**  
**OCP:17.8A**

**+3.3V\_ALW**  
**Fs=300K**  
**TDC : 8.27A**  
**Peak :10.1A**  
**OCP: 12.12A**



**+VCC\_iGPU\_CORE**  
**Fs=400K**  
**TDC : 12A**  
**Peak Current : 22A**  
**OCP:26.4A**

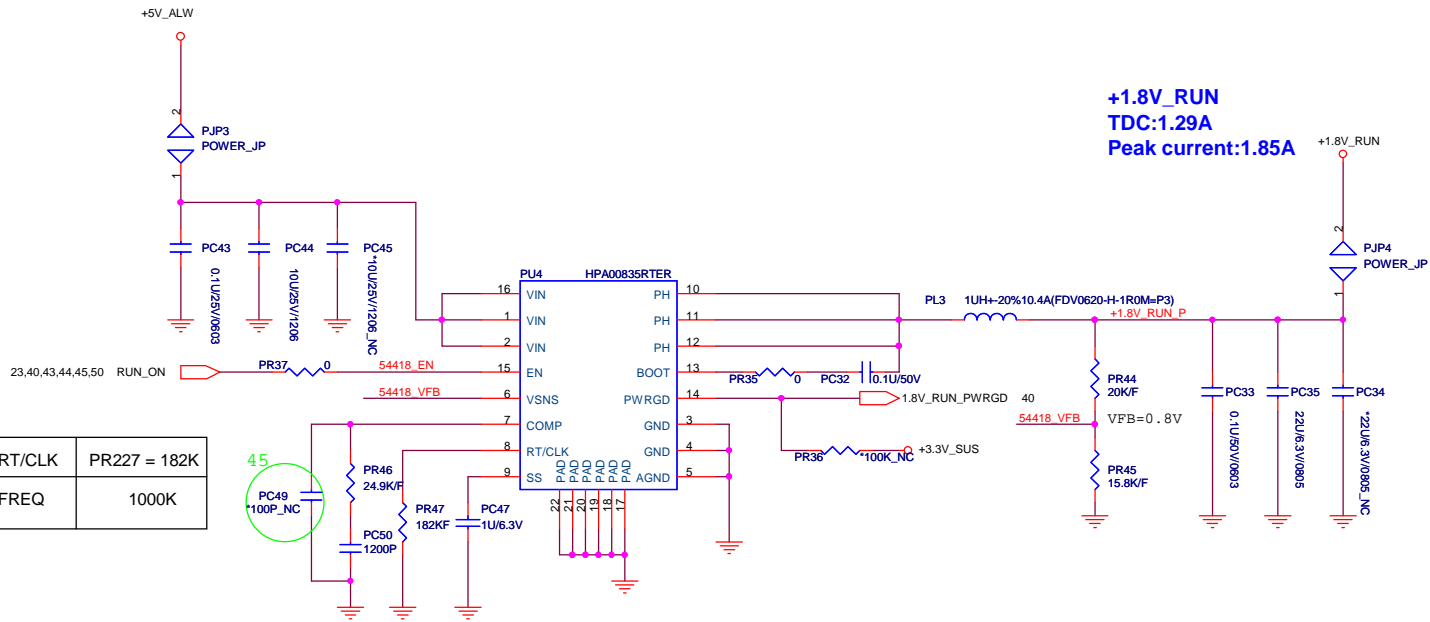
Place close to CPU socket  
**VCC\_AXG\_SENSE & VSS\_AXG\_SENSE pins**

Place close to PR140, PR141  
**+GFX\_VCORE pins**

+VCC\_GFX\_CORE  
 Control IC: ADP3211  
 H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W  
 L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W  
 Inductor: 0.56uH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm  
 Output Cap: 1\*390U, 2.5V(20%, 105C, 6.3\*5.8), ESR=10mohm



Title VCC_iGPU_CORE		
Size	Document Number GM6	Rev 2B
Date:	Friday, June 25, 2010	Sheet 47 of 63

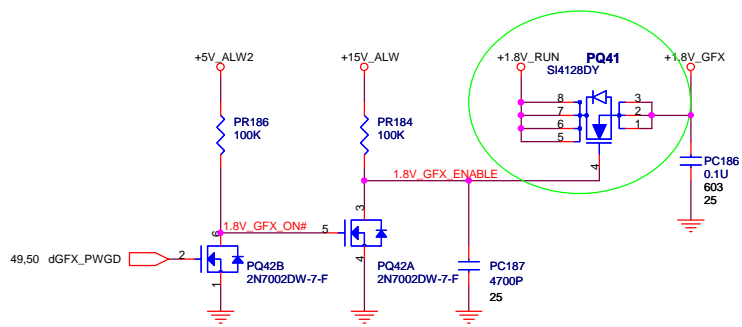


**+1.8V\_RUN**  
**TDC:1.29A**  
**Peak current:1.85A**

RT/CLK	PR227 = 182K
FREQ	1000K

45  
 PC49  
 \*100P\_NC

86

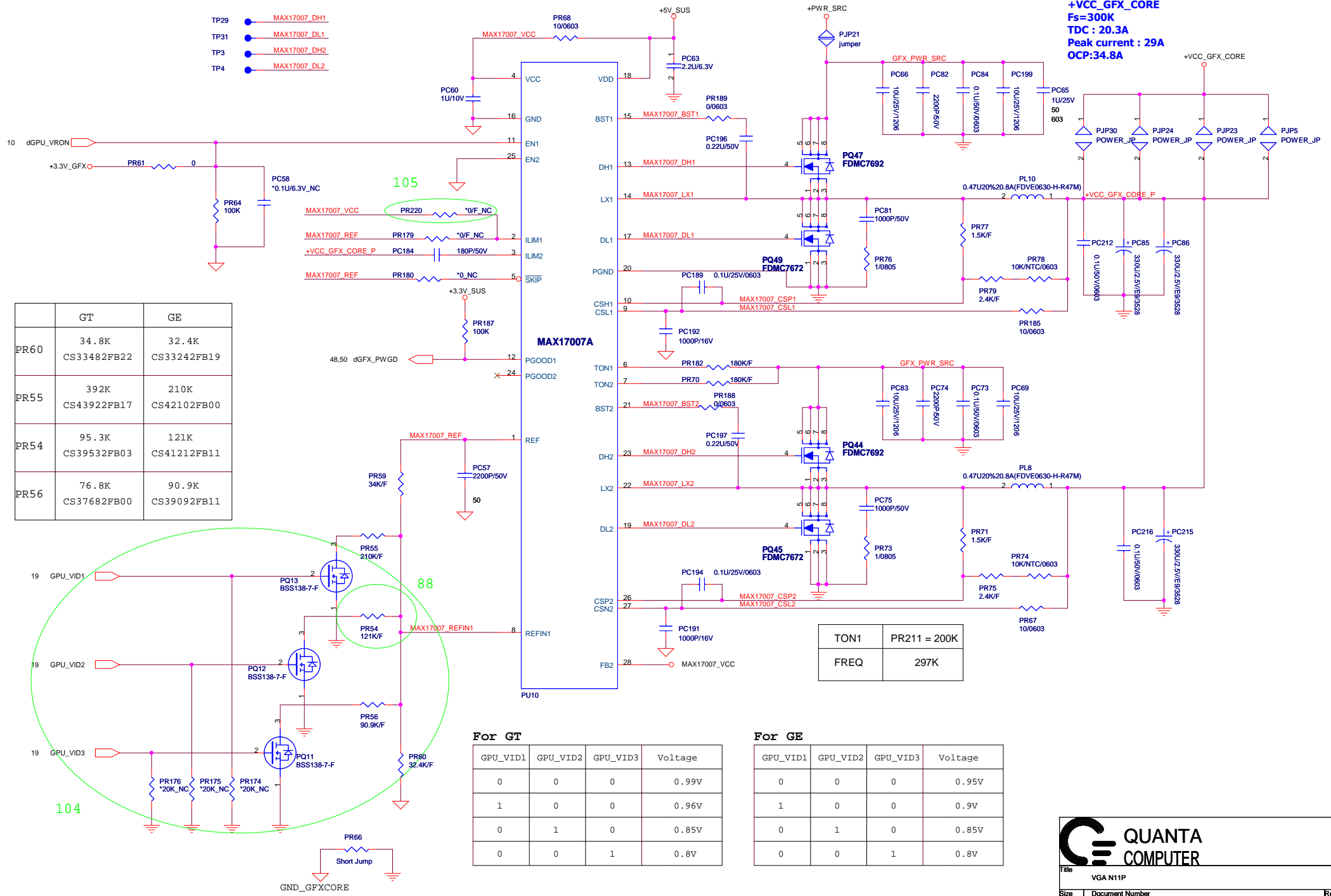


**+1.8V\_GFX**  
**Current : 0.3A**



- TP29 ● MAX17007\_DH1
- TP31 ● MAX17007\_DL1
- TP3 ● MAX17007\_DH2
- TP4 ● MAX17007\_DL2

**+VCC\_GFX\_CORE**  
**Fs=300K**  
**TDC : 20.3A**  
**Peak current : 29A**  
**OCP:34.8A**



	GT	GE
PR60	34.8K CS33482FB22	32.4K CS33242FB19
PR55	392K CS43922FB17	210K CS42102FB00
PR54	95.3K CS39532FB03	121K CS41212FB11
PR56	76.8K CS37682FB00	90.9K CS39092FB11

TON1	PR211 = 200K
FREQ	297K

**For GT**

GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.99v
1	0	0	0.96v
0	1	0	0.85v
0	0	1	0.8v

**For GE**

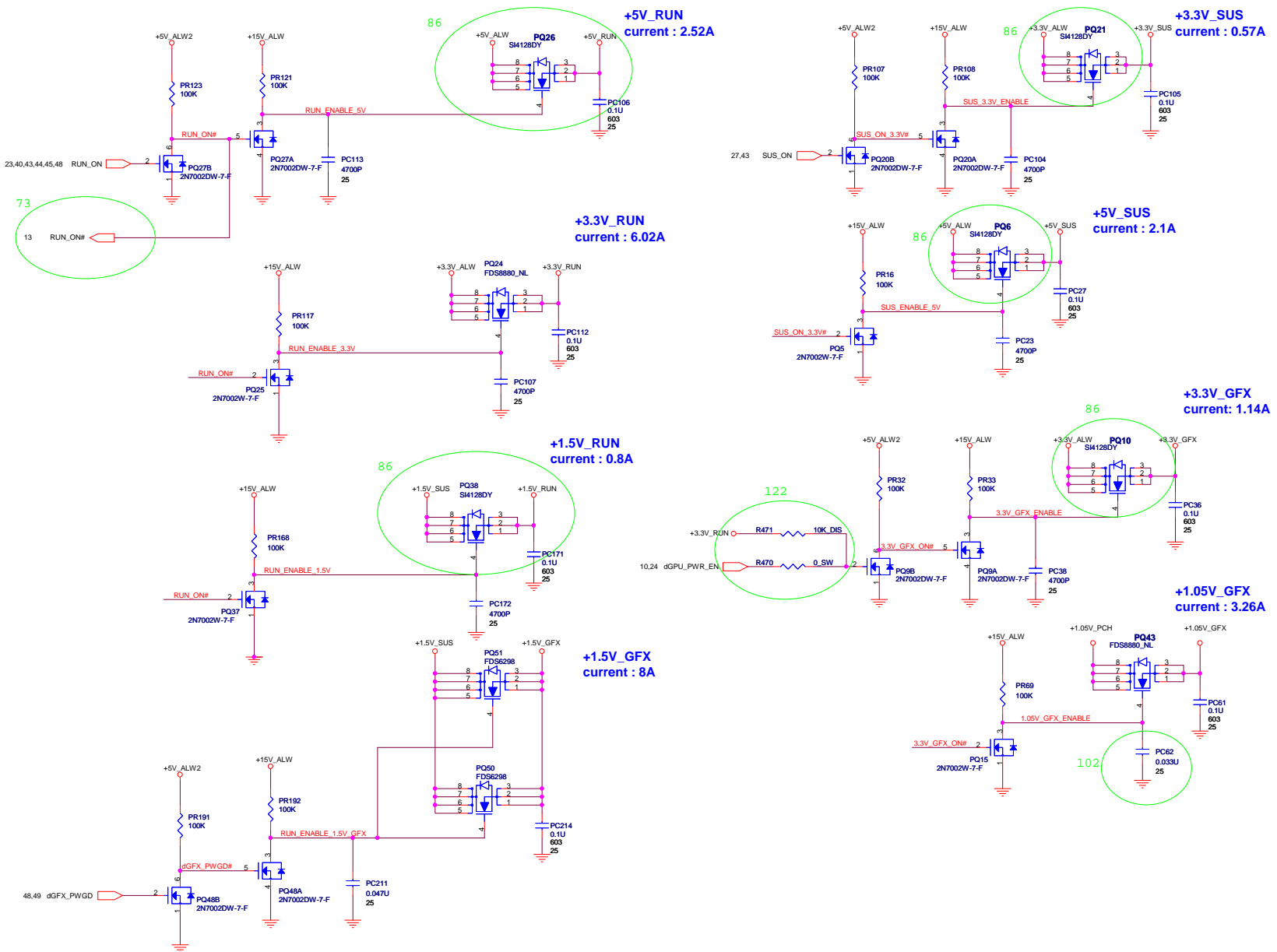
GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.95v
1	0	0	0.9v
0	1	0	0.85v
0	0	1	0.8v

**QUANTA COMPUTER**

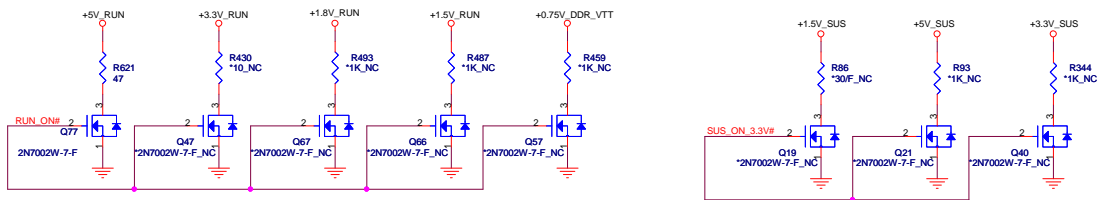
Title: VGA N11P

Size: Document Number GM6 Rev 2B

Date: Friday, June 25, 2010 Sheet 49 of 63



**Reserve discharge path**



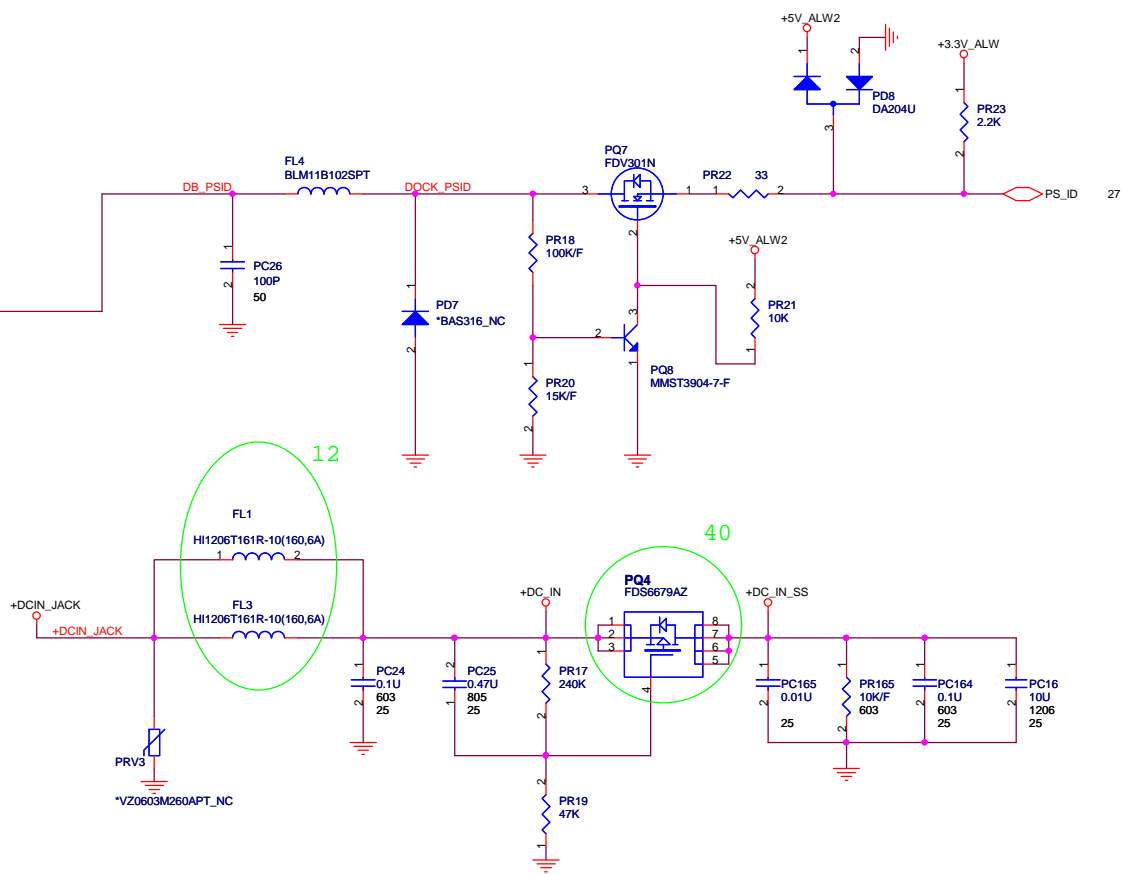
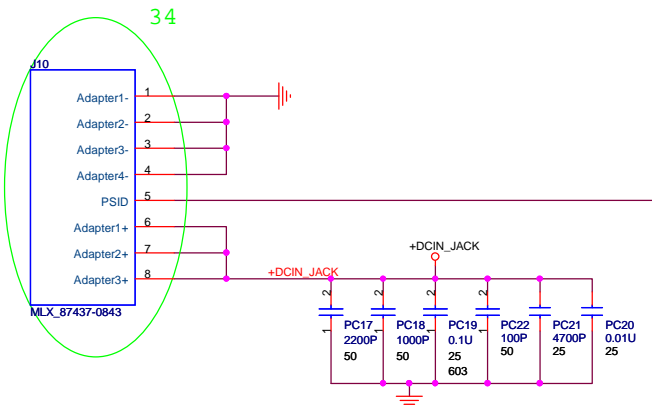
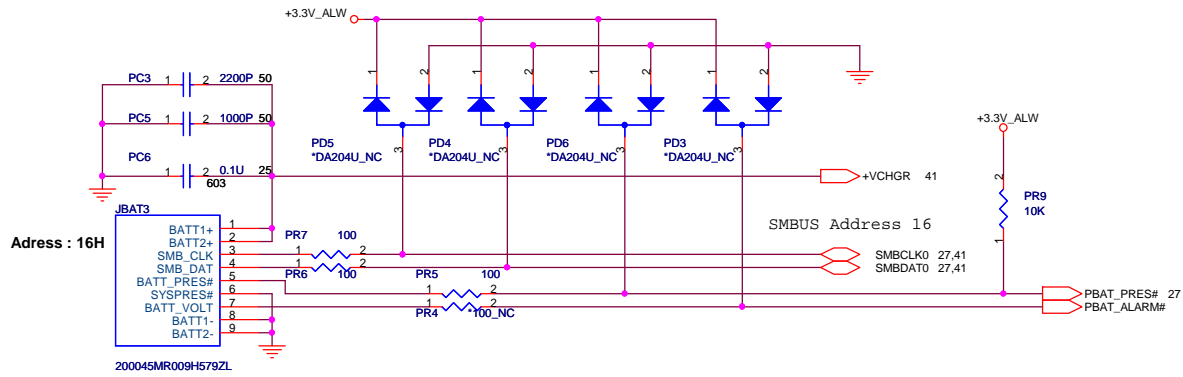
WWW.MANUALS.CLAN.SU

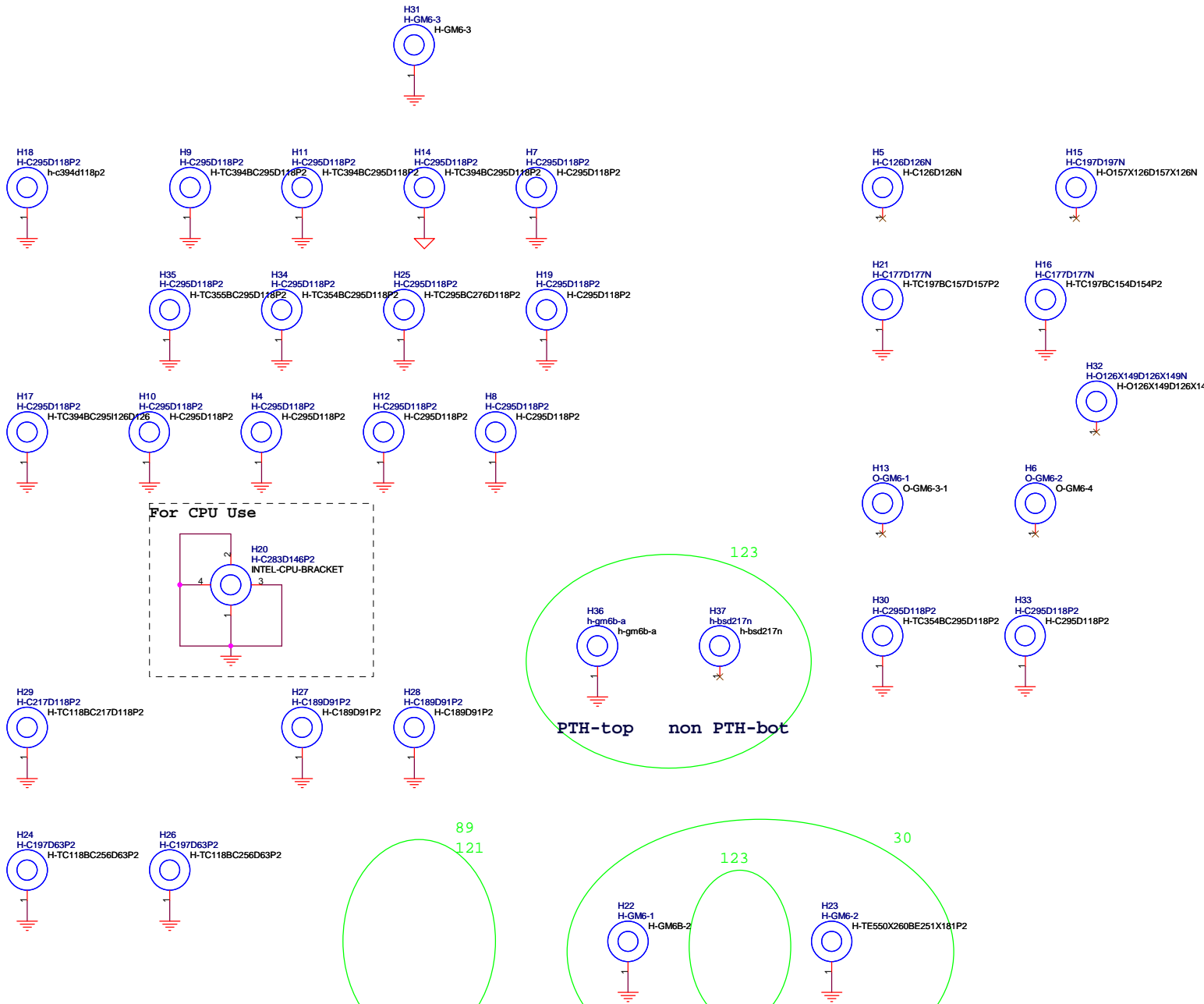
**QUANTA COMPUTER**

Title: RUN / SUS POWER SW

Size: Document Number GM6 Rev 2B

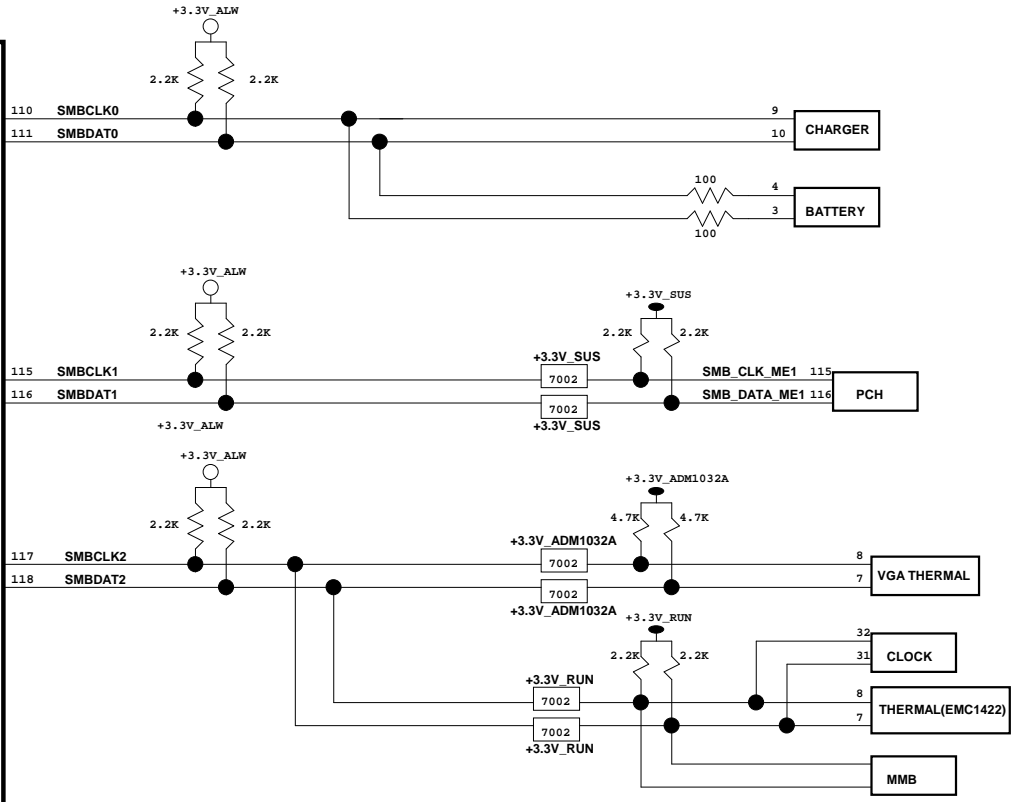
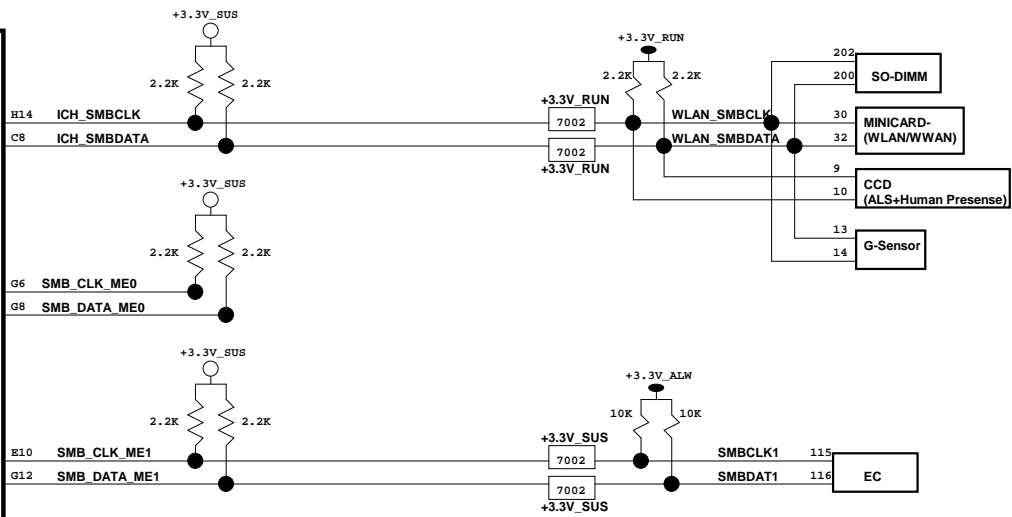
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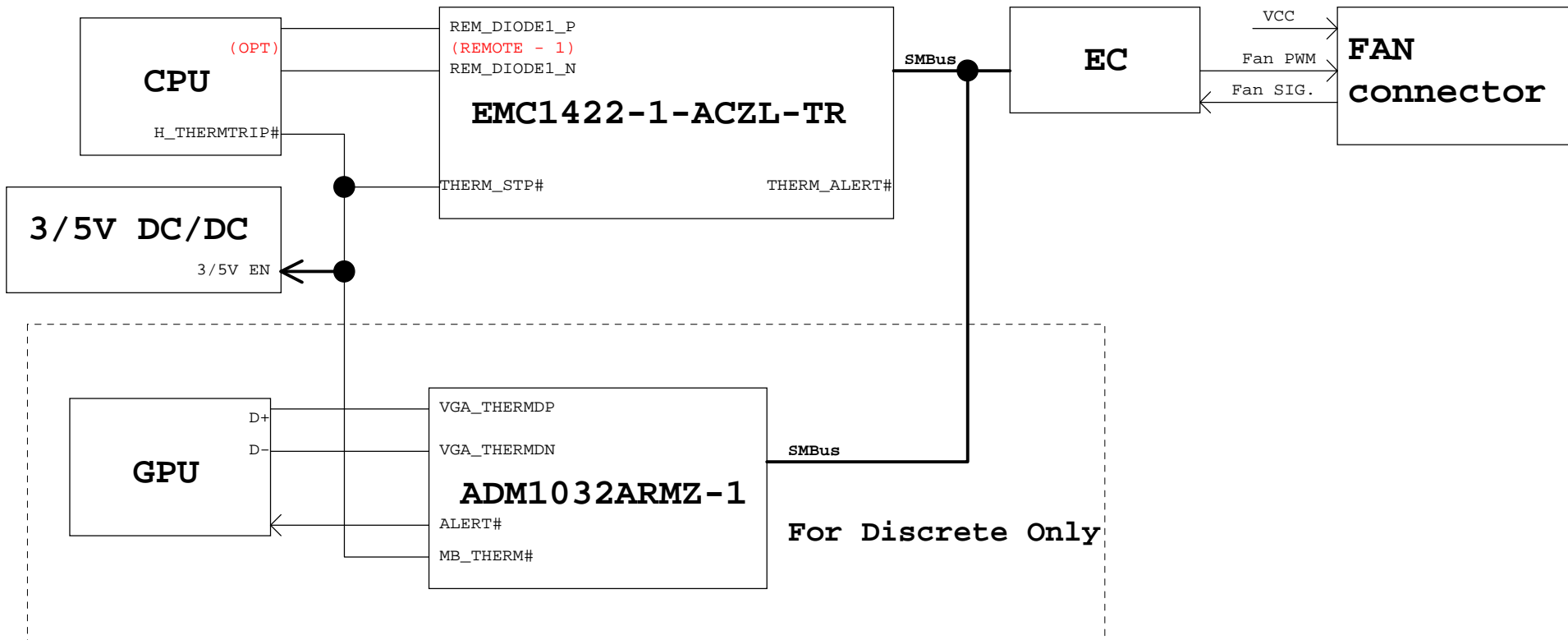


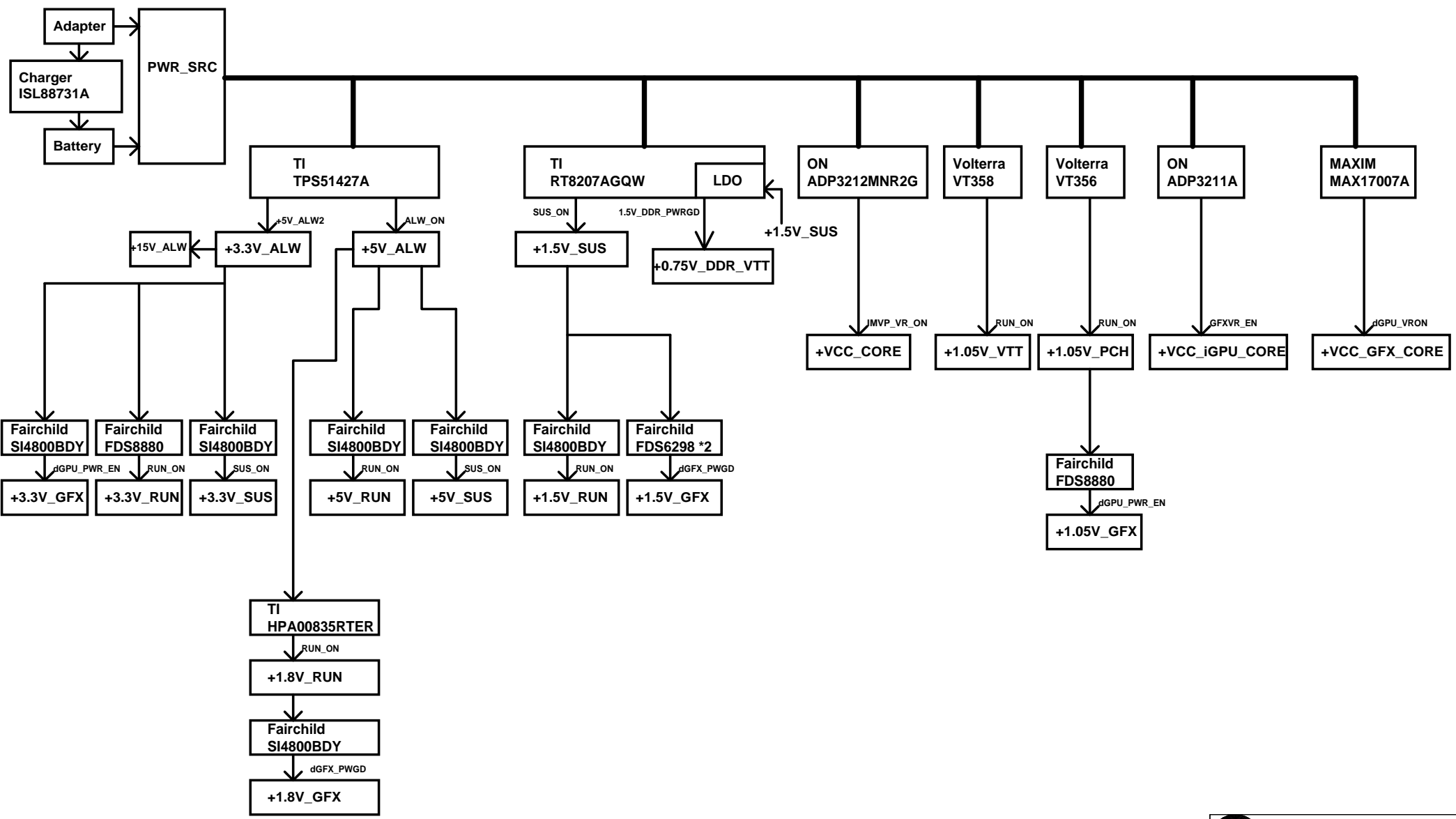


PCH

SIO  
ITE8502



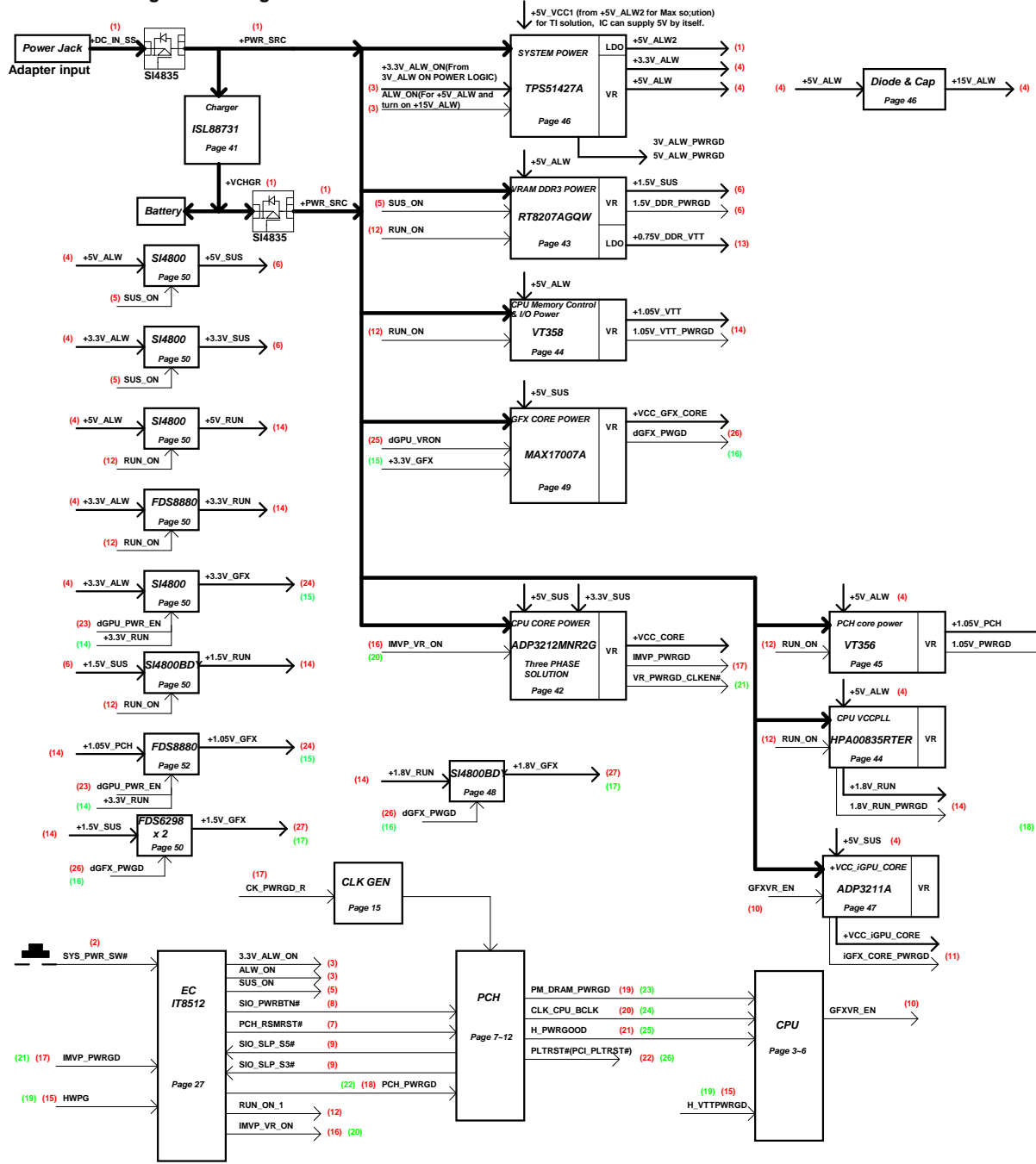




**QUANTA COMPUTER**

Title: Power Block Diagram		
Size: GM6	Document Number: GM6	Rev: 2B
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FM9 Power Design Block Diagram 2009/12/28



Optimus  
DIS only

- (1) (1) AC : DC IN -> DC\_IN\_SS -> +PWR\_SRC
- Bat : +VCHGR -> +PWR\_SRC,+5V\_ALW2
- (2) (2) SYS\_PWR\_SW#
- (3) (3) 3.3V\_ALW\_ON,ALW\_ON
- (4) (4) +3.3V\_ALW,+5V\_ALW,+15V\_ALW
- (5) (5) SUS\_ON
- (6) (6) +5V\_SUS,+3.3V\_SUS,+1.5V\_SUS,1.5V\_DDR\_PWRGD
- (7) (7) PCH\_RSMRST#
- (8) (8) SIO\_PWRBTN#
- (9) (9) SIO\_SLP\_S5#,SIO\_SLP\_S3#
- (10) (10) GFXVR\_EN
- (11) (11) +VCC\_IGPU\_CORE,IGFX\_CORE\_PWRGD
- (12) (12) RUN\_ON\_1(RUN\_ON)
- (13) (13) +0.75V\_DDR\_VTT
- (14) (14) +3.3V\_RUN,+5V\_RUN,
- +1.05V\_VTT,+1.05V\_PCH,+1.8V\_RUN,+1.5V\_RUN,
- (15) (15) HWPG,H\_VTTPWRGD
- (16) (16) IMVP\_VR\_ON
- (17) (17) +VCC\_CORE,IMVP\_PWRGD,VR\_PWRGD\_CLKEN#
- (18) (18) PCH\_PWRGD
- (19) (19) PM\_DRAM\_PWRGD
- (20) (20) CLK\_CPU\_BCLK(PCH to CPU)
- (21) (21) H\_PWRGOOD
- (22) (22) PLTRST#(PCI\_PLTRST#)
- (23) (23) dGPU\_PWR\_EN(PCH GPIO 56)
- (24) (24) +3.3V\_GFX,+1.05V\_GFX
- (25) (25) dGPU\_VRON(PCH GPIO 35)
- (26) (26) +VCC\_GFX\_CORE,dGFX\_PWGD
- (27) (27) +1.5V\_GFX,+1.8V\_GFX
- (28) (28) dGPU\_PWROK

