Enrico/Caruso 15" UMA Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2011-04-22

REV : A00

```
DY : Nopop Component
HDMI : Pop for HDMI function
No_HDMI : Pop for NO HDMI function
10/100 : Pop for 10/100 LAN
GIGA : Pop for GIGA LAN
Surge : Pop for surge option
G709 : Pop G709 thermal solution
INS : Pop for Inspirion series ID
VOS : Pop for Vostro series ID
S3 : Pop for S3 power reduction
Normal : Pop for NO S3 power reduction
```

DV15 CP UMA second

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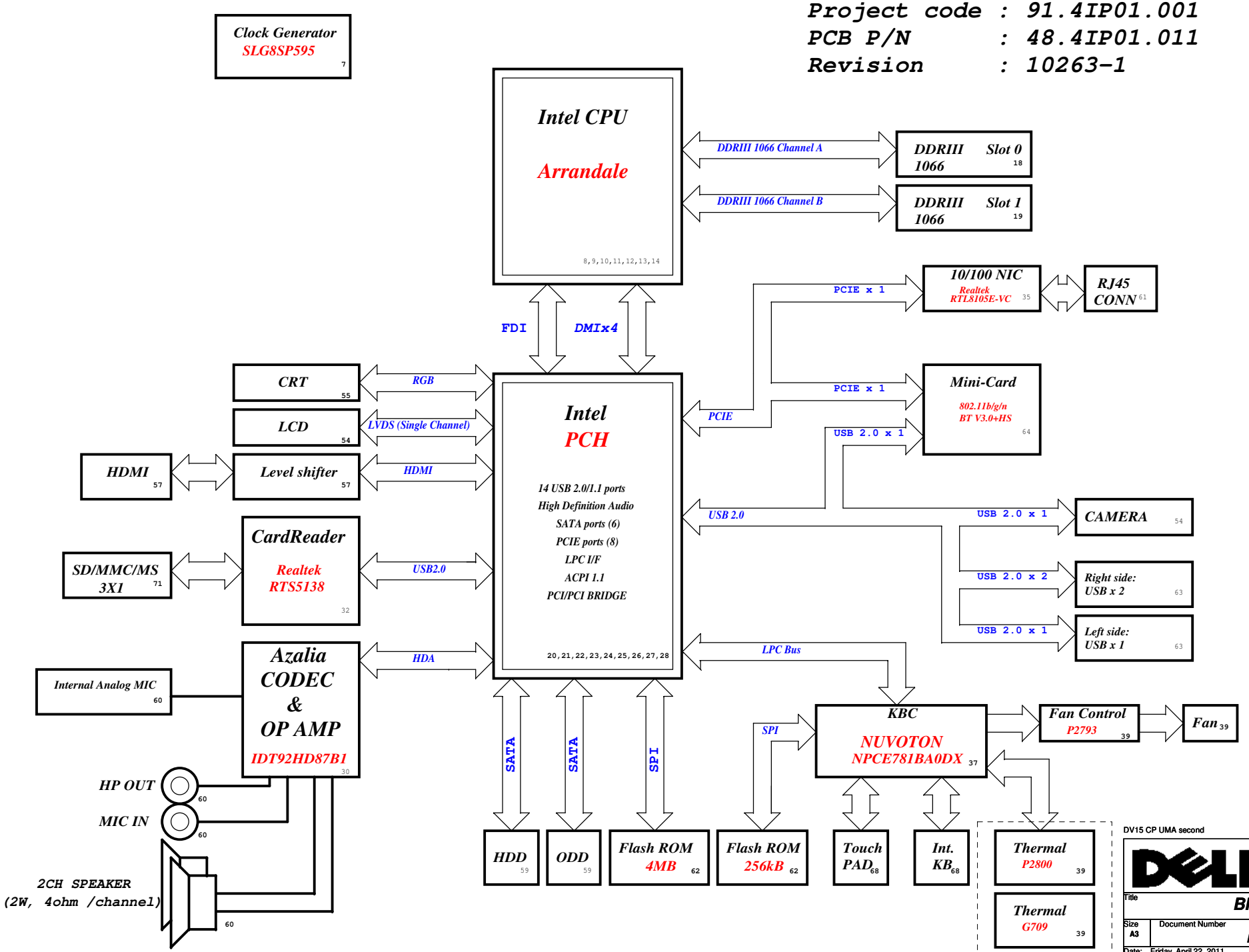
Title	Cover Page	
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Friday, April 22, 2011	Sheet 1 of 99	

DV15 Calpella UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP01.011
Revision : 10263-1



MAXIM CHARGER BQ24707 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51123 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +3.3V_ALW +5V_ALW +15V_ALW

CPU DC/DC ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC RT8237A 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_CPU +1.05V_PCH

SYSTEM DC/DC RT8207 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +V_DDR_REF +0.75V_DDR_VTT

SYSTEM DC/DC APW7153B 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_CPU +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5 VCC
L6: Bottom

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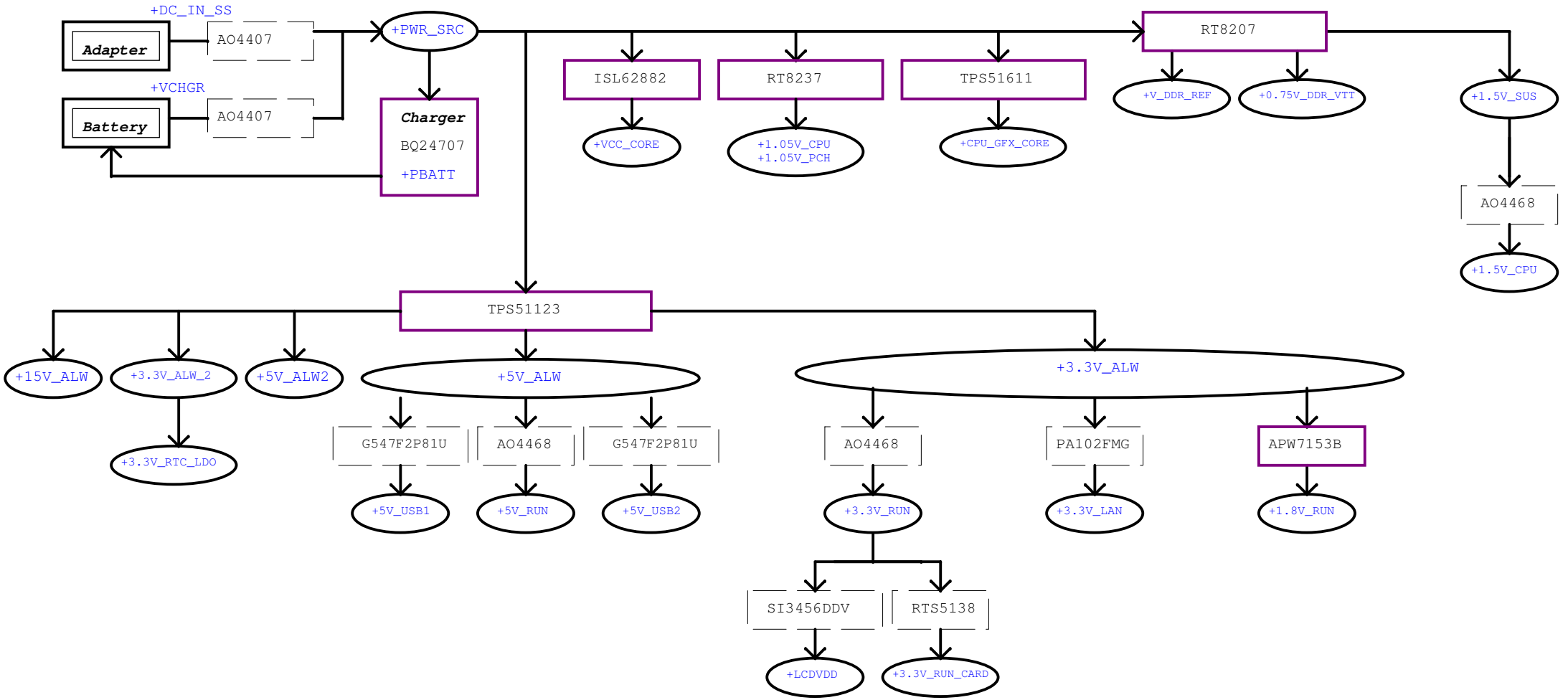
Title: Block Diagram

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 22, 2011 | Sheet 2 of 99



Power Shape

Regulator	LDO	Switch

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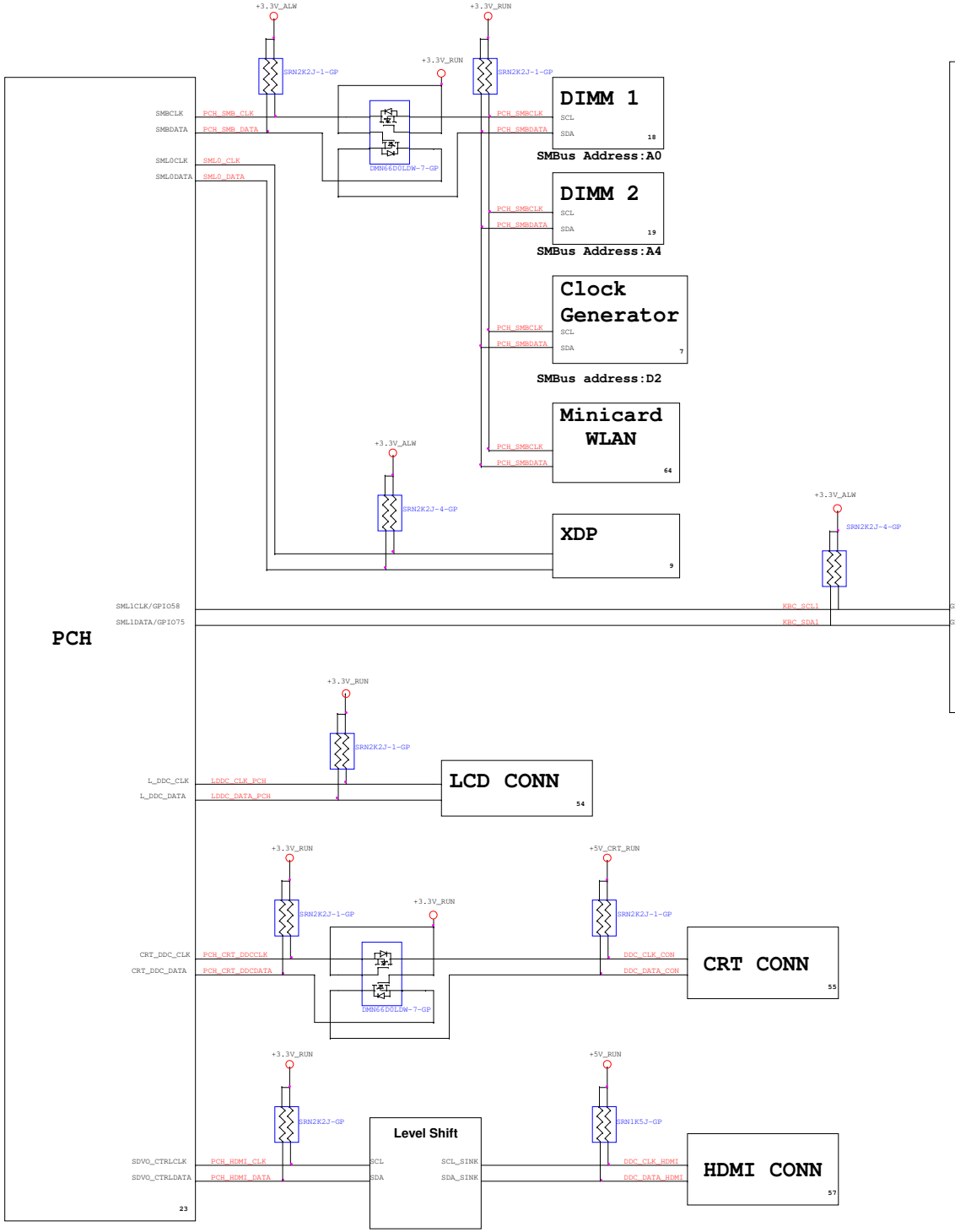
Title: ***Power Block Diagram***

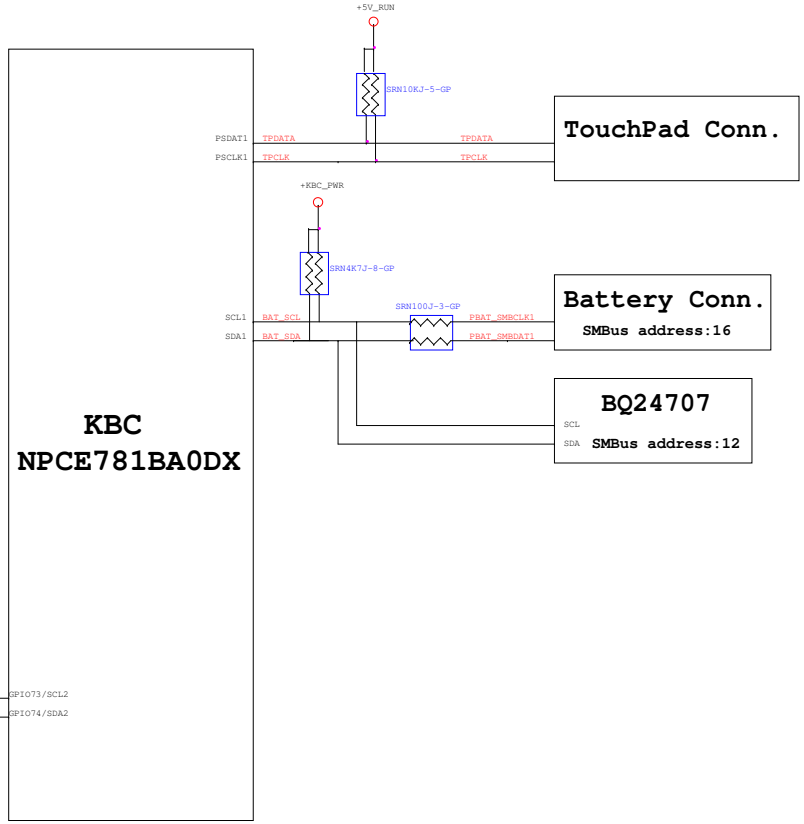
Size	Document Number	Rev
A3	***Enrico/Caruso 15 CP***	***A00***

Date: Friday, April 08, 2011 Sheet 3 of 99

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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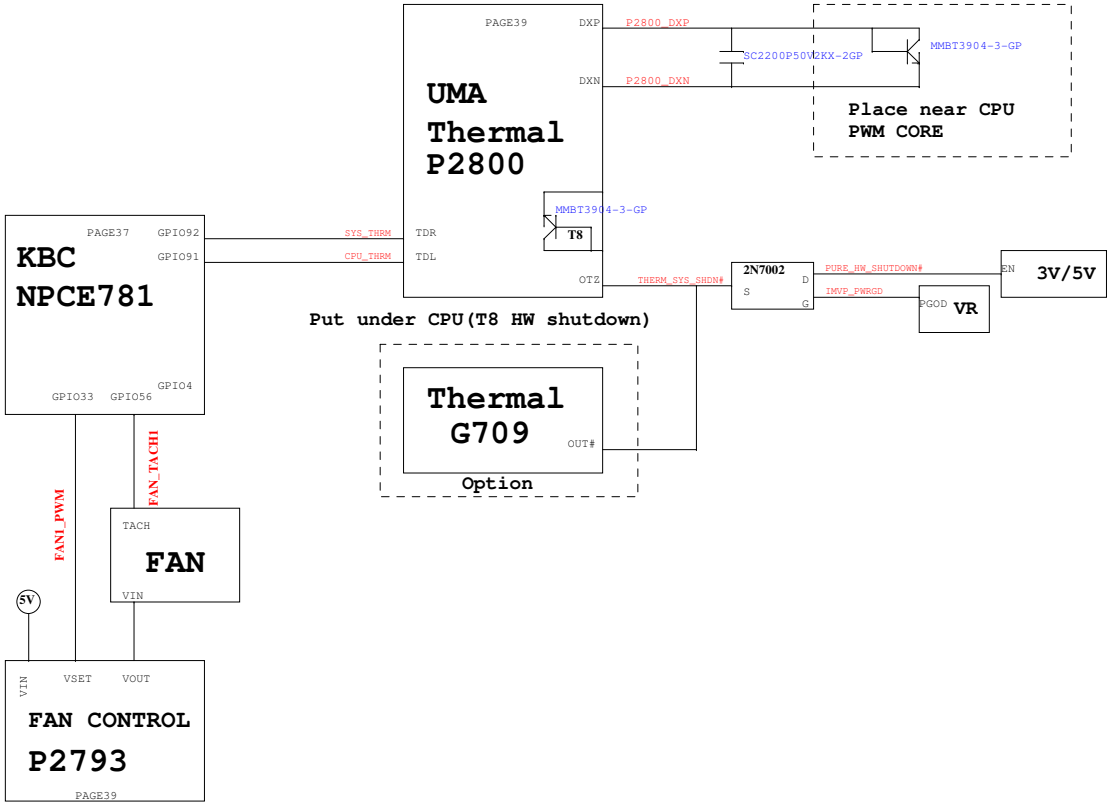
Title: SMBUS Block Diagram

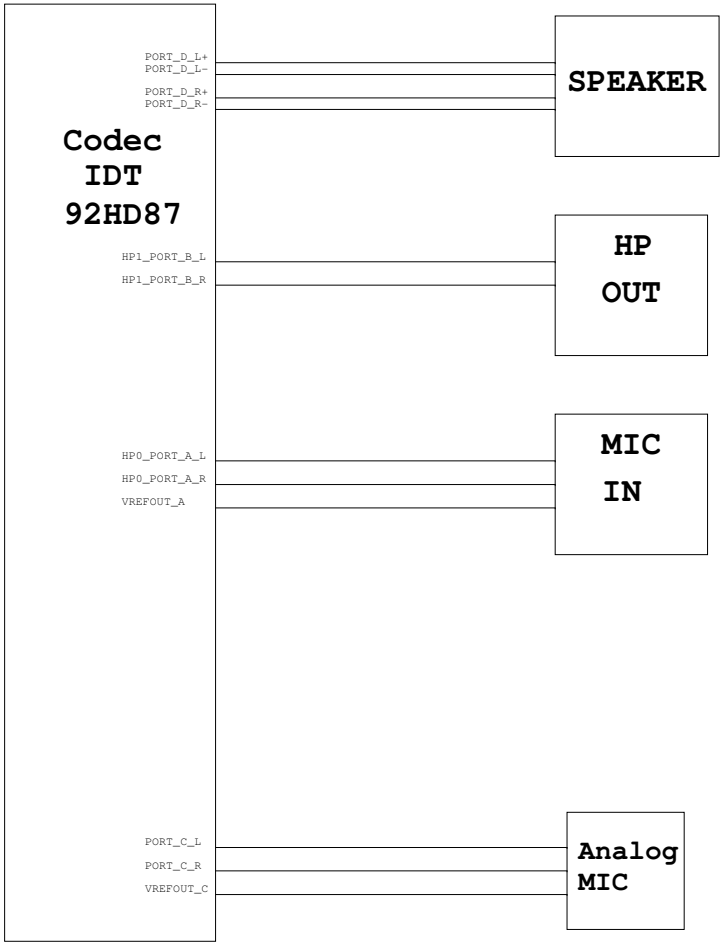
Size	Document Number	Rev
A2	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 4 of 99

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 08, 2011 | Sheet 5 of 99

PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

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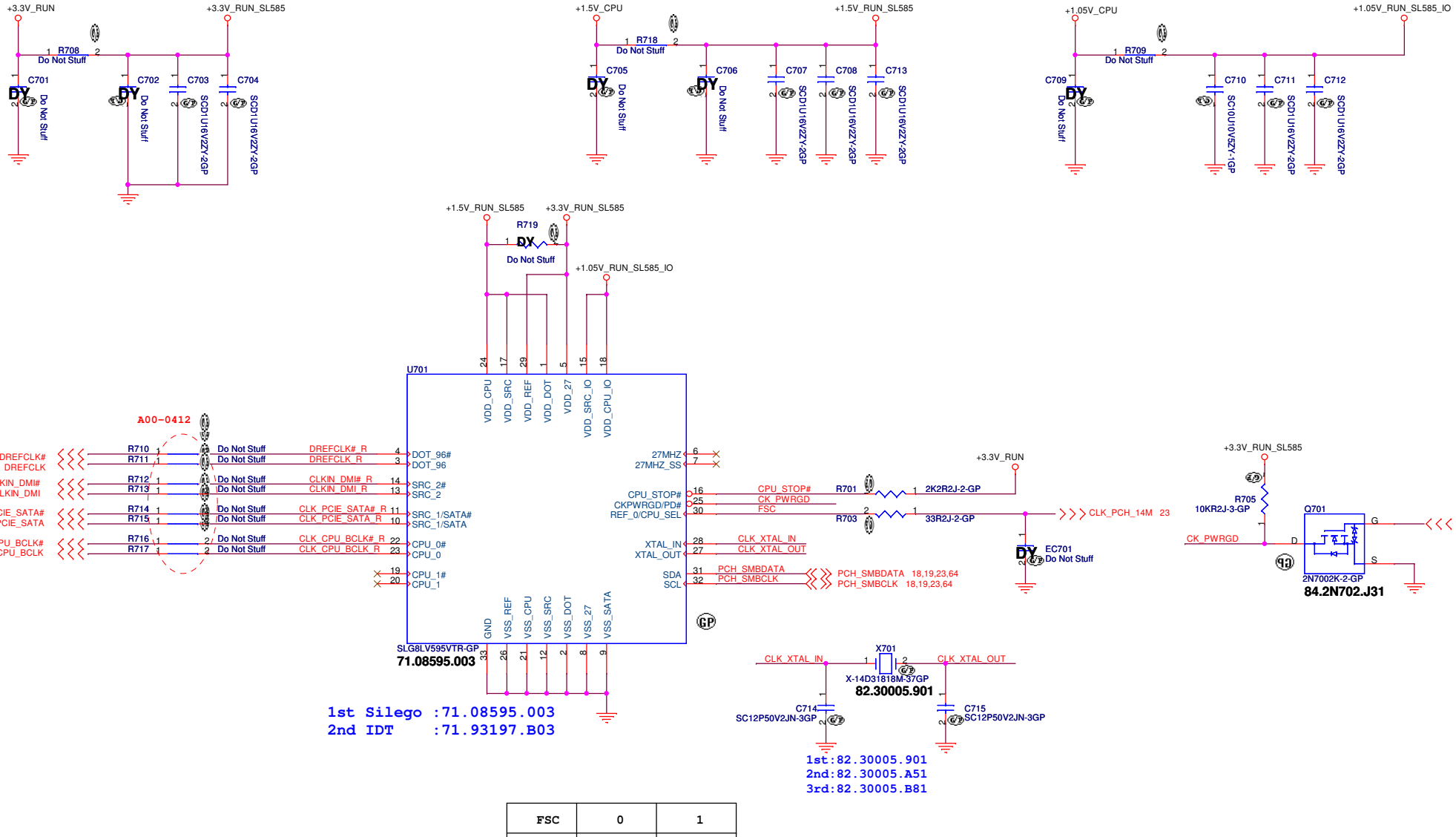
Title: Table of Content

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 08, 2011 | Sheet 6 of 99

SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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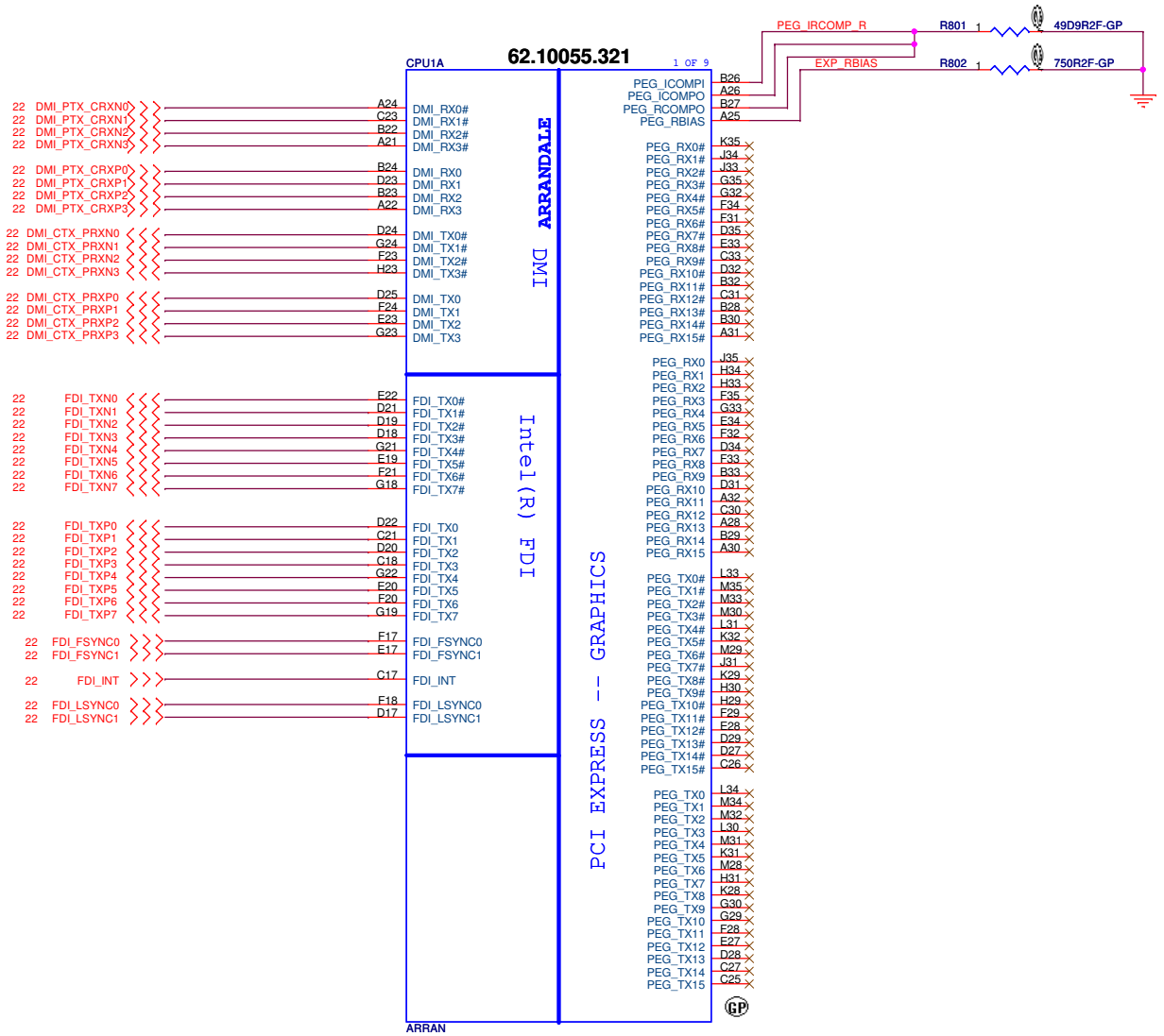
Title: Clock Generator SLG8LV595

Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 7 of 99

SSID = CPU



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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 8 of 99

SSID = CPU

Processor Pullups

+1.05V_CPU

R902 1 — 49D9R2F-GP — H_CATERR#

R933 1 — 49D9R2F-GP — H_PROCHOT#_CPU

R904 1 — DY — Do Not Stuff — H_CPURST#

Processor Compensation Signals

R901 1 — 20R2F-GP — H_COMP3

R903 1 — 20R2F-GP — H_COMP2

R905 1 — 49D9R2F-GP — H_COMP1

R906 1 — 49D9R2F-GP — H_COMP0

Do Not Stuff — TP901 — 1 — SKTOCC#_R

CPU1B 2 OF 9

COMP3	AT23	H_COMP3
COMP2	AT24	H_COMP2
COMP1	G16	H_COMP1
COMP0	AT26	H_COMP0
SKTOCC#	AH24	SKTOCC#_R
CATERR#	AK14	H_CATERR#
PECI	AT15	25 H_PECI
PROCHOT#	AN26	45,47 H_PROCHOT# — R919 DY Do Not Stuff — H_PROCHOT#_CPU
THERMTRIP#	AK15	25 H_THERMTRIP#_CPU
RESET_OBS#	AP26	H_CPURST#
PM_SYNC	AL15	22 H_PM_SYNC
VCCPWRGOOD_1	AN14	
VCCPWRGOOD_0	AN27	25,42 H_PWRGD — R908 Do Not Stuff — VCCPWRGOOD
SM_DRAMPWROK	AK13	VDDPWRGOOD_R
VTTPWRGOOD	AM15	49 H_VTTPWRGD
TAPPWRGOOD	AM26	H_PWRGD_XDP
RSTIN#	AL14	21,35,37,64,70 PLT_RST# — R913 1K6R2F-GP — PLT_RST#_R

ARRANDALE: MISC, THERMAL, PWR MANAGEMENT

R915 750R2F-GP — DY — C904 Do Not Stuff

C904 close to cpu

BCLK	A16	BCLK_CPU_P_R — RN901 — BCLK_CPU_P 25
BCLK#	B16	BCLK_CPU_N_R — RN901 — BCLK_CPU_N 25
BCLK_ITP	AR30	BCLK_ITP_P
BCLK_ITP#	AT30	BCLK_ITP_N
PEG_CLK	E16	PEG_CLK_R — RN903 — CLK_EXP_P 23
PEG_CLK#	D16	PEG_CLK#_R — RN903 — CLK_EXP_N 23
DPLL_REF_SSCLK	A18	
DPLL_REF_SSCLK#	A17	

Do Not Stuff

CLOCKS

SM_DRAMRST#	F6	SM_DRAMRST#
SM_RCOMP0	AL1	SM_RCOMP_0
SM_RCOMP1	AM1	SM_RCOMP_1
SM_RCOMP2	AN1	SM_RCOMP_2
PM_EXT_TS0#	AN15	PM_EXTTS#0_C — RN906 DY Do Not Stuff — PM_EXTTS#0 18
PM_EXT_TS1#	AP15	PM_EXTTS#1_C — RN906 — PM_EXTTS#1 19

RN905 — SRN10KJ-5-GP — +1.05V_CPU

DDR3 MISC

PRDY#	AT28	XDP_PRDY#
PREQ#	AP27	XDP_PREQ#
TCK	AN28	XDP_TCLK
TMS	AP28	XDP_TMS
TRST#	AT27	XDP_TRST#
TDI	AT29	XDP_TDI_R
TDO	AR27	XDP_TDO_R
TDI_M	AP29	XDP_TDI_M
TDO_M	AP29	XDP_TDO_M
DBR#	AN25	H_DBR#_R — R909 Do Not Stuff — XDP_DBRESET#
BPM0#	AJ22	XDP_OBS0
BPM1#	AK22	XDP_OBS1
BPM2#	AK24	XDP_OBS2
BPM3#	AJ24	XDP_OBS3
BPM4#	AJ25	XDP_OBS4
BPM5#	AH22	XDP_OBS5
BPM6#	AK23	XDP_OBS6
BPM7#	AH23	XDP_OBS7

JTAG & BPM

GP

DDR_RST_GATE 25 — C915 SCD047U16V2ZY-1GP — S3 GP

+1.5V_SUS

Q901 2N7002K-2-GP 84.2N702.J31 — S3 GP

R934 1KR2J-1-GP — S3 GP — DDR3_DRAMRST# 18,19

C903 SCD1U10V2KX-5GP — S3 GP

R935 1 Normal — Do Not Stuff

+1.5V_CPU

R936 DY Do Not Stuff — SM_DRAMRST#

R988 S3 100KR2J-1-GP

DDR3 Compensation Signals

SM_RCOMP_0 — R907 — 100R2F-L1-GP-U

SM_RCOMP_1 — R910 — 24D9R2F-L-GP

SM_RCOMP_2 — R911 — 130R2F-1-GP

S3 Power Reduction

+3.3V_RUN +1.5V_CPU

R938 Normal Do Not Stuff

U927 74LVC1G08GW-1-GP — S3 GP

37,49,50 VTT_PWRGD — VTT_PWRGD_R3

R939 1K6R2F-GP — S3 — Normal — R977 Do Not Stuff

VDDPWRGOOD_R

R940 750R2F-GP — S3 — Normal — R937 Do Not Stuff

22 PM_DRAM_PWRGD — R912 Do Not Stuff

S3 circuit	R939	R940	R938
	1.6k	0.75k	DY
Normal	R977	R937	R938
	1.27k	3k	Stuff

XDP1 — NP1 NP2 — Do Not Stuff

XDP_PREQ# XDP_PRDY# XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7 XDP_TCLK

+1.05V_CPU

H_PWRGD — R927 DY Do Not Stuff — H_CPUPWRGD_XDP

22 PM_PWRBTN#_R — R929 DY Do Not Stuff — PM_PWRBTN#_XDP

H_PWRGD_XDP — R930 DY Do Not Stuff — PCIE_CLK_XDP_P

C902 DY Do Not Stuff

23 SML0_DATA 23 SML0_CLK

BCLK_ITP_P BCLK_ITP_N XDP_RST#_R XDP_TDO XDP_TRST# XDP_TDI XDP_TMS

C901 DY Do Not Stuff — +1.05V_CPU

R931 DY Do Not Stuff — H_CPURST#

R932 DY Do Not Stuff — XDP_DBRESET# 22 PLT_RST# 21,35,37,64,70

XDP_TCLK — R918 DY Do Not Stuff

XDP_TRST# — R923 — 51R2J-2-GP

+1.05V_CPU

XDP_TMS — R914 DY Do Not Stuff

XDP_TDI_R — R916 DY Do Not Stuff

XDP_PREQ# — R917 DY Do Not Stuff

XDP_TDO — R920 — 51R2J-2-GP

XDP_TDI_R — R921 Do Not Stuff — XDP_TDI

XDP_TDO_M — R922 DY Do Not Stuff — XDP_TDO

X01-0123 — R924 Do Not Stuff

XDP_TDI_M — R925 DY Do Not Stuff

XDP_TDO_R — R926 Do Not Stuff

JTAG MAPPING

Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

DV15 CP UMA second

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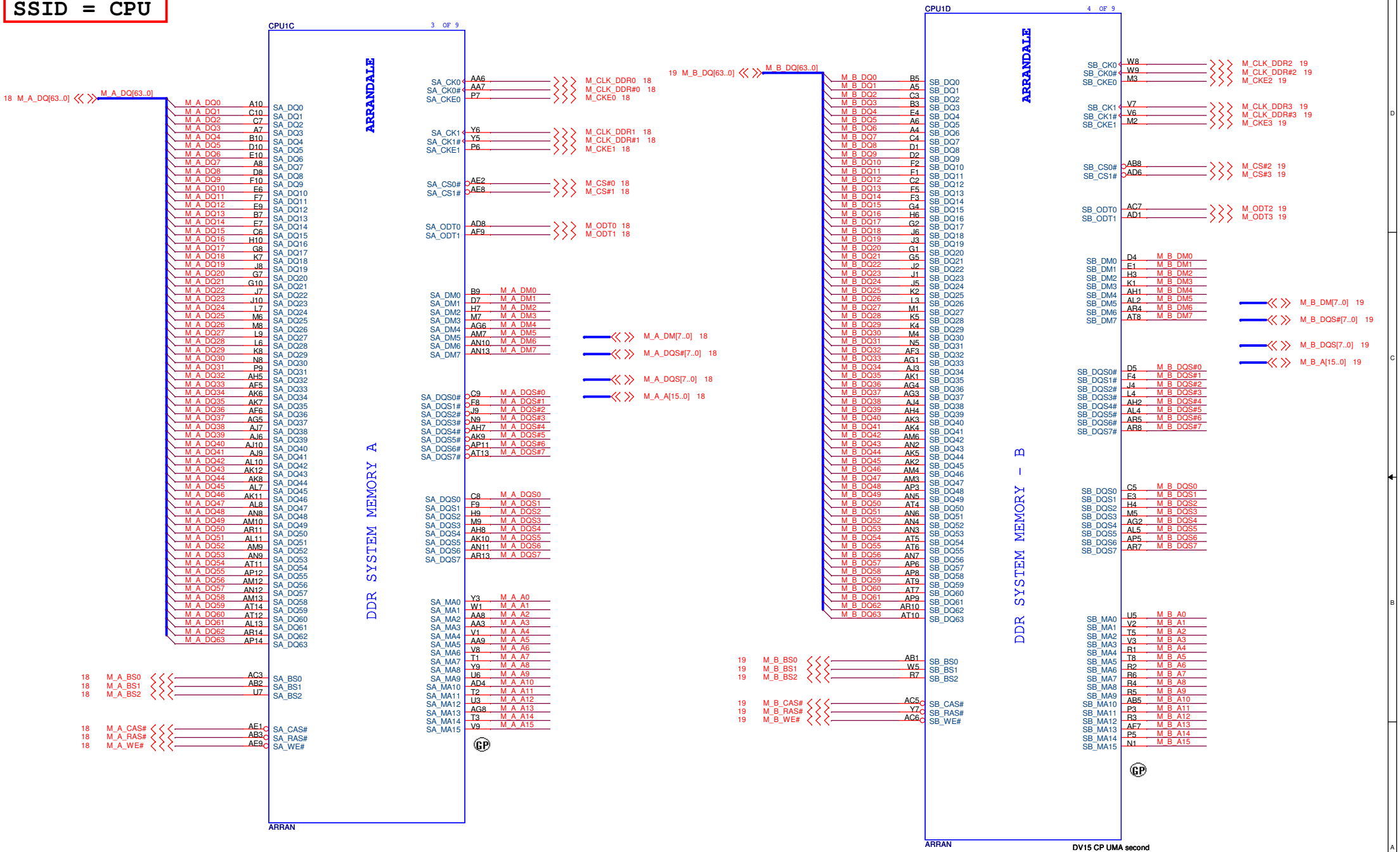
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 9 of 99

SSID = CPU



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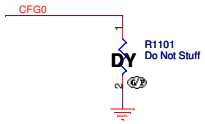
Title: **CPU (DDR)**

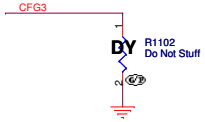
Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 10 of 99

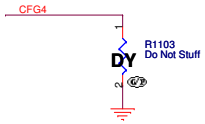
SSID = CPU



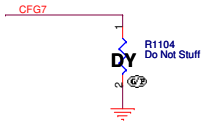
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



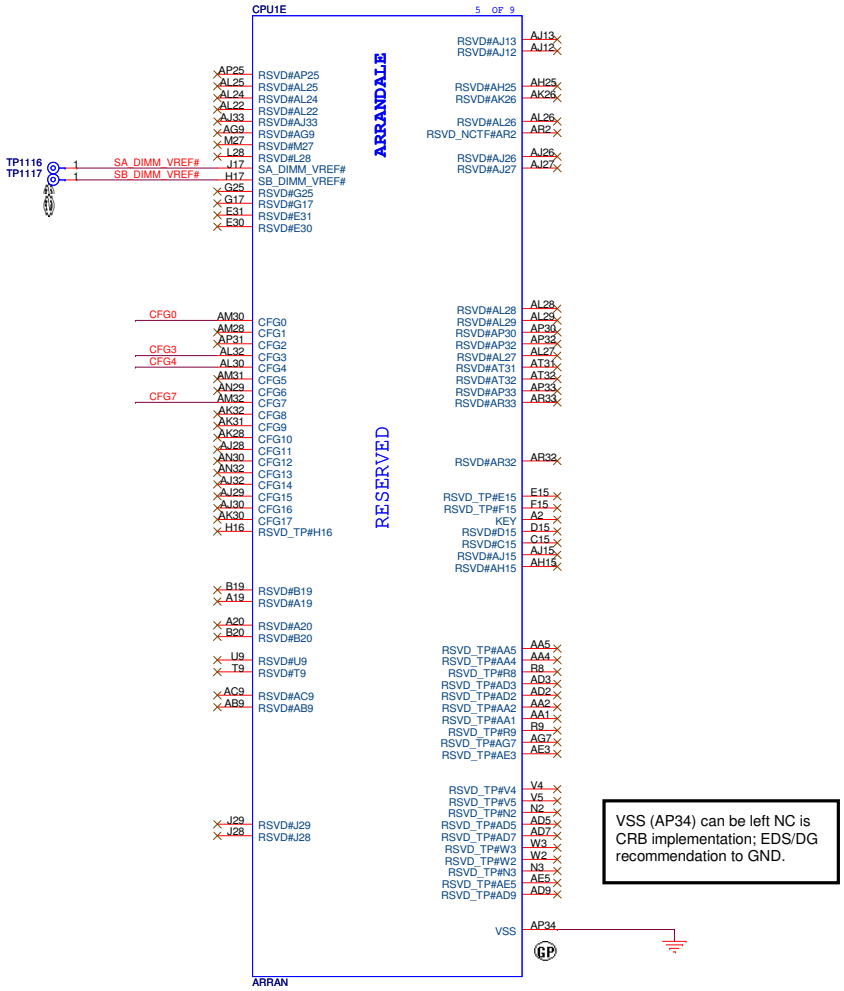
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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Title: ***CPU (RESERVED)***

Size | Document Number: ***Enrico/Caruso 15 CP*** | Rev: ***A00***

Date: Friday, April 08, 2011 | Sheet 11 of 99

SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

For POWER

For POWER

C1206 C1207 C1208 C1209 C1220 C1210

C1212 C1213 C1214 C1215 C1223 C1224

C1225 C1226 C1227 C1228 C1229 C1230 C1231 C1232

C1235 C1236 C1237 C1238 C1239 C1240 C1241 C1242

C1243

CPU1F

6 OF 9

ARRANDALE

CPU CORE SUPPLY

1.1V RAIL POWER

POWER

CPU VIDS

SENSE LINES

ARRAN

+1.05V_CPU

C1216 C1201 C1202 C1217 C1218 C1203 C1219 C1204 C1205

C1211 C1221 C1222

C1233 C1234

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

PSI# AN33 PSI# 47

H_VID[6..0] 47

VID0 AK35 H_VID0

VID1 AK33 H_VID1

VID2 AK34 H_VID2

VID3 AL35 H_VID3

VID4 AL33 H_VID4

VID5 AM33 H_VID5

VID6 AM35 H_VID6

PROC_DPRSLPVR AM34 PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 TP1201Do Not Stuff

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V

ISENSE AN35 IMVP_IMON 47

VCC_SENSE AJ34 VCC_SENSE 47

VSS_SENSE AJ35 VSS_SENSE 47

VTT_SENSE B15 VTT_SENSE 49

VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT TP1202Do Not Stuff

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

DV15 CP UMA second

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Title: CPU (VCC_CORE)

Size | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 12 of 99

SSID = CPU

+1.5V_CPU — DY C1376 Do Not Stuff — +1.5V_SUS
+1.5V_CPU — DY C1377 Do Not Stuff — +1.5V_SUS
+1.5V_CPU — DY C1378 Do Not Stuff — +1.5V_SUS
+1.5V_CPU — DY C1379 Do Not Stuff — +1.5V_SUS

425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7

+CPU_GFX_CORE

22A

C1327 SC10U6D3V5MX-3GP
C1325 SC10U6D3V5MX-3GP
C1328 SC10U6D3V5MX-3GP
C1323 DY Do Not Stuff
C1326 DY Do Not Stuff
C1324 DY Do Not Stuff
C1309 SC10U6D3V5MX-3GP
C1312 DY Do Not Stuff

CPU1G — 7 OF 9

GRAPHICS: AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16 — VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

ARRANDALE

SENSE LINES: VAXG_SENSE VSSAXG_SENSE — AR22 AT22 — VCC_AXG_SENSE 53, VSS_AXG_SENSE 53

GRAPHICS VIDs: GFX_VID0 GFX_VID1 GFX_VID2 GFX_VID3 GFX_VID4 GFX_VID5 GFX_VID6 — AM22 AP22 AN22 AP23 AM23 AP24 AN24 — GFX_VID0 53, GFX_VID1 53, GFX_VID2 53, GFX_VID3 53, GFX_VID4 53, GFX_VID5 53, GFX_VID6 53

GFX_VR_EN GFX_DPRSLPVR GFX_IMON — AR25 AT25 AM24 — R1305 4K7R2J-2-GP; GFX_IMON_C — R1304 DY Do Not Stuff — GFX_VR_EN 53, GFX_DPRSLPVR 53, GFX_IMON 53

POWER

DDR3 - 1.5V RAILS: VDDQ (AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1)

3A — +1.5V_CPU

C1301 SC1U6D3V2KX-GP
C1302 SC1U6D3V2KX-GP
C1303 SCD1U10V2KX-5GP
C1304 SC1U6D3V2KX-GP
C1305 DY Do Not Stuff
C1306 SC10U6D3V5MX-3GP
C1307 SC10U6D3V5MX-3GP
DY TC1301 Do Not Stuff

+1.05V_CPU

C1308 DY Do Not Stuff

FDI: J24 J23 H25 — VTT1 VTT1 VTT1

1.1V: VTT1 (P10 N10 L10 K10)

+1.05V_CPU

C1310 SC10U6D3V5MX-3GP
C1311 SC10U6D3V5MX-3GP

+1.05V_CPU

18A

C1313 DY Do Not Stuff
C1314 DY Do Not Stuff
C1315 DY Do Not Stuff

PEG & DMI: K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25 — VTT1

1.1V: VTT1 (J22 J20 J18 H21 H20 H19)

+1.05V_CPU

C1316 SC4D7U6D3V5KX-3GP
C1317 DY Do Not Stuff

1.8V: VTT1 (L26 L27 M26)

1.35A — +1.8V_RUN

C1318 SC1U6D3V2KX-GP
C1319 SC1U6D3V2KX-GP
C1320 SC10U6D3V5MX-3GP
C1321 SC2D2U6D3V9KX-GP
C1322 DY Do Not Stuff

Please note that the VTT Rail Values are: Auburndale VTT=1.05V Clarksfield VTT=1.1V

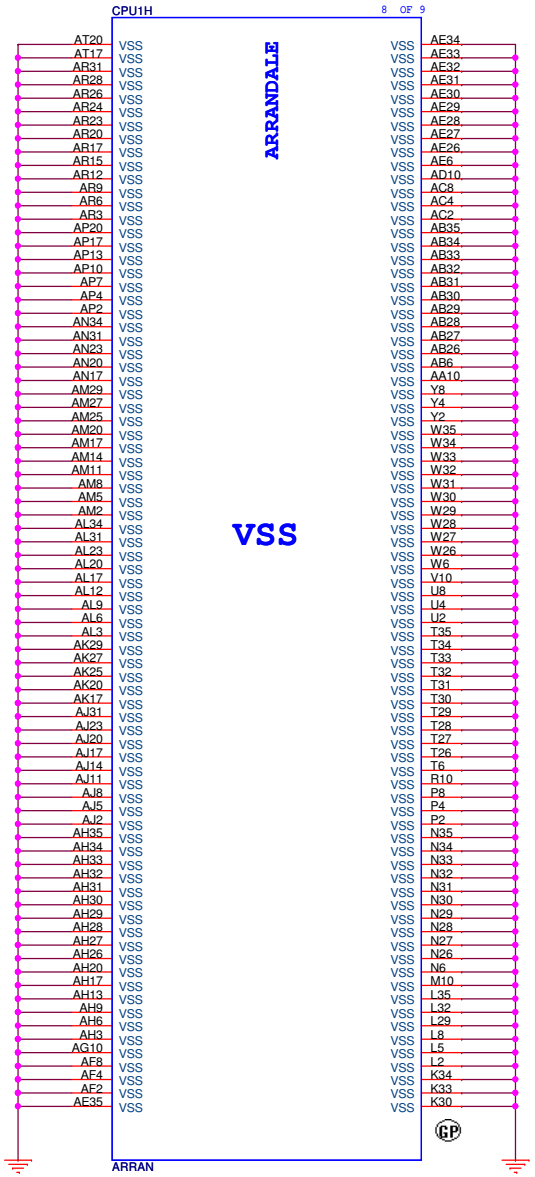
ARRAN

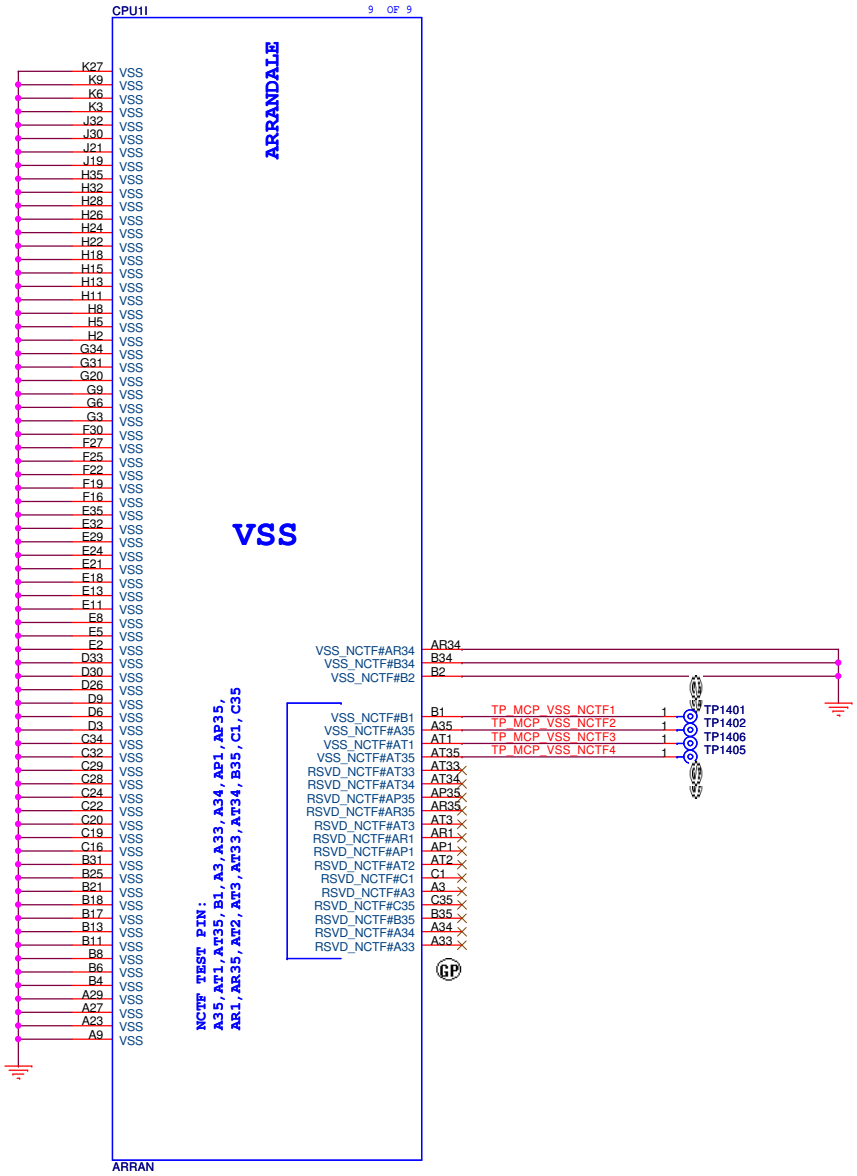
DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: Document Number: Enrico/Caruso 15 CP — Rev: A00
Date: Wednesday, April 13, 2011 — Sheet 13 of 99

SSID = CPU





DV15 CP UMA second

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Friday, April 08, 2011	Sheet 14 of 99	

(Blanking)

DV15 CP UMA second

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 15 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 16 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 17 of 99

SSID = MEMORY

DM1

DDR3-204P-106-GP

62.10017.X31

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

RN1801 SRN10KJ-5-GP

C1801 SCD1U10V2KX-5GP

C1802 Do Not Stuff

+3.3V_RUN

+1.5V_SUS

SODIMM A DECOUPLING

TC1801 150U6.3VM

C1804 SCD1U10V2KX-5GP

C1805 SCD1U10V2KX-5GP

C1806 SCD1U10V2KX-5GP

C1807 SCD1U10V2KX-5GP

C1808 SCD1U10V2KX-5GP

C1809 SCD1U10V2KX-5GP

C1813 SCD1U10V2KX-5GP

C1814 SCD1U10V2KX-5GP

C1815 SCD1U10V2KX-5GP

C1816 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

+V_DDR_REF

C1817 SCD1U10V2KX-5GP

C1818 Do Not Stuff

C1826 SCD1U10V2KX-5GP

+0.75V_DDR_VTT

Place these caps close to VTT1 and VTT2.

C1820 SC1U6D3V2KX-GP

C1821 Do Not Stuff

C1822 SC1U6D3V2KX-GP

C1823 Do Not Stuff

S3 Power Reduction

+0.75V_DDR_VTT

R1806 22R2J-2-GP

Q1801 2N7002K-2-GP

84.2N702.J31

42,50 PS_S3CNTRL

DV15 CP UMA second

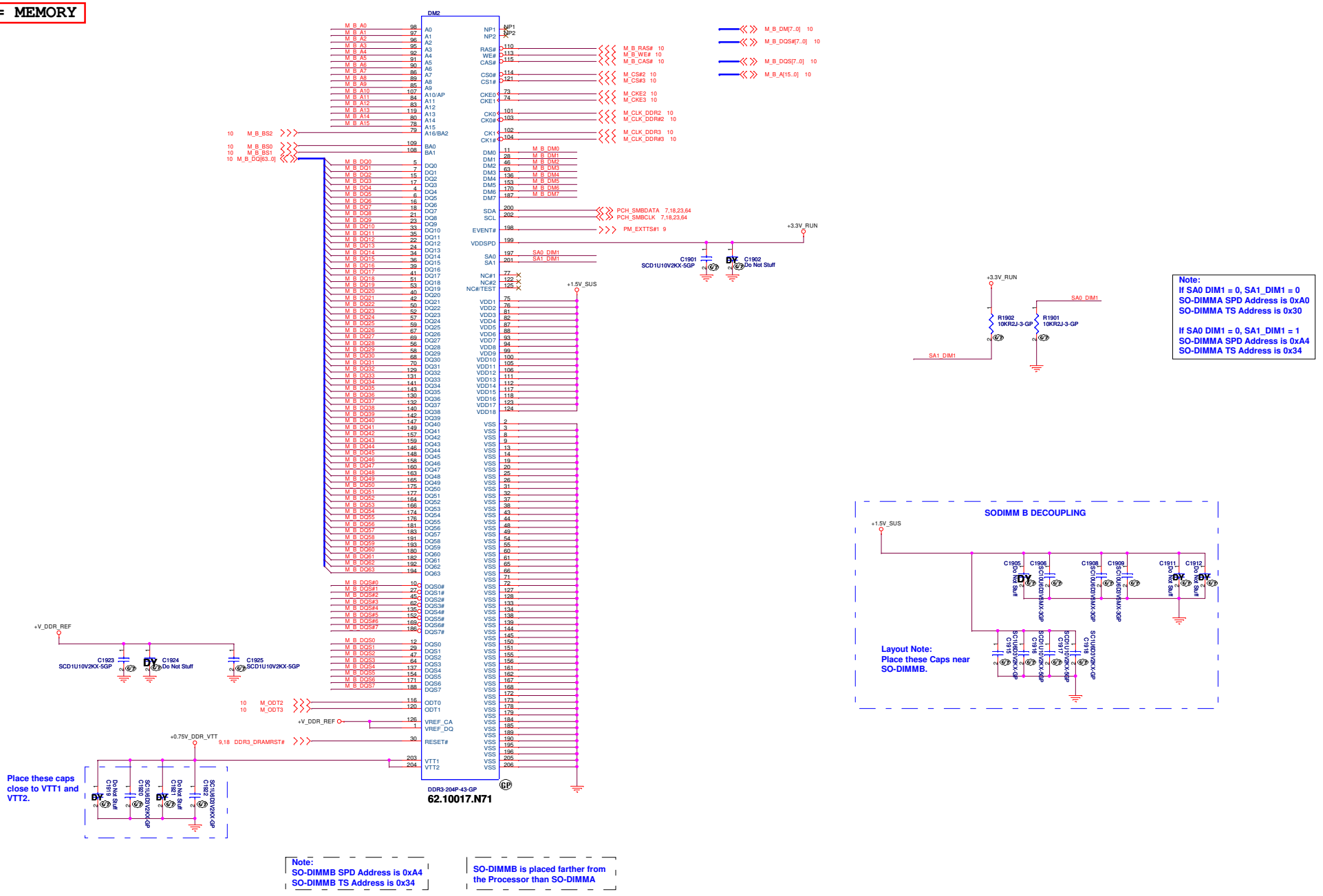
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size | Document Number: ***Enrico/Caruso 15 CP*** | Rev: ***A00***

Date: Wednesday, April 13, 2011 | Sheet 18 of 99

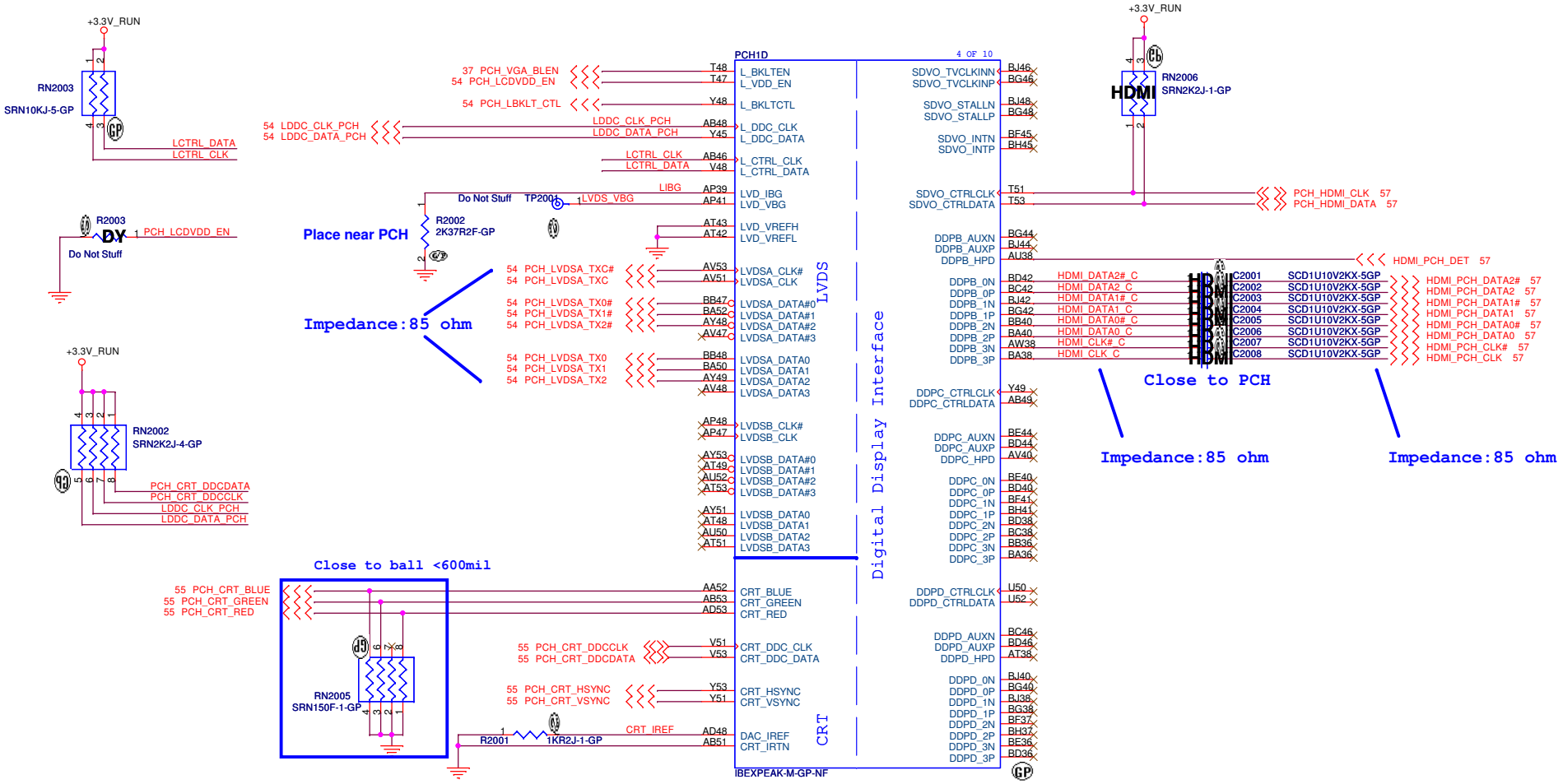
SSID = MEMORY



DV15 CP UMA second

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3-SODIMM2		
Size	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 19 of 99	

SSID = PCH

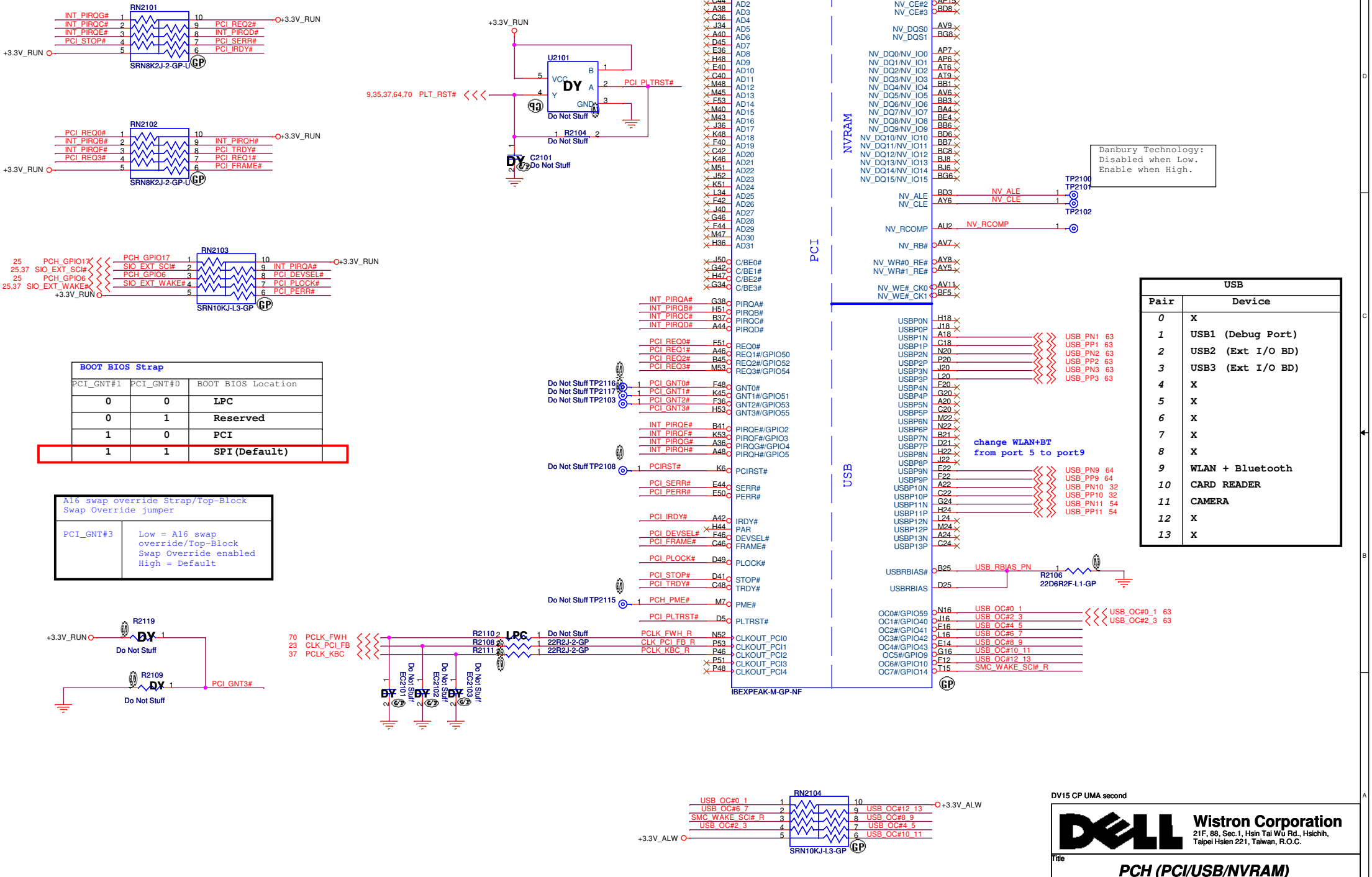


DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (LVDS/CRT/DDI)	
Size	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 20 of 99	

SSID = PCH



BOOT BIOS Strap

PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

USB

Pair	Device
0	X
1	USB1 (Debug Port)
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

DV15 CP UMA second

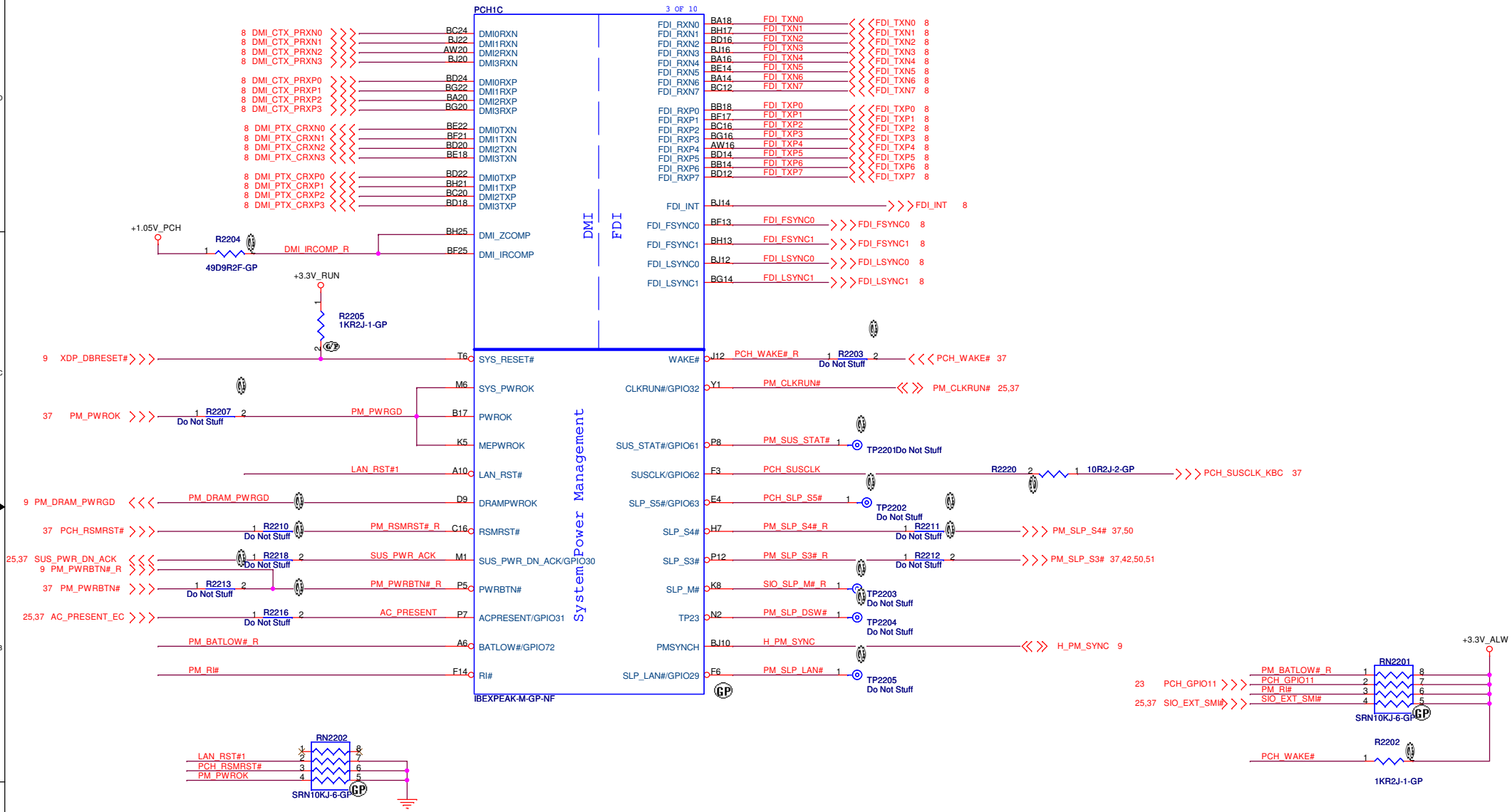
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

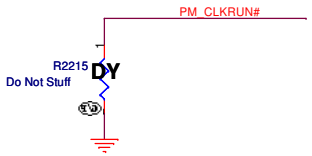
Size | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 21 of 99

SSID = PCH



Option to " Disable " clkrun.
Pulling it down will keep the clks running.



DV15 CP UMA second

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (DM I/FDI/PM)		
Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00
Date: Wednesday, April 13, 2011	Sheet 22 of 99	

SSID = PCH

PCH1B

2 OF 10

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

WLAN

LAN

PCI-E* Controller Link

SMBus

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

RN2301 SRN2K2J-4-GP

RN2302 SRN2K2J-1-GP

RN2303 SRN2K2J-1-GP

Q2301 MN66D0LDW-7-GP

RN2308 SRN10KJ-5-GP

RN2310 SRN10KJ-L3-GP

No_HDMI

HDMI

X2301 XTAL-25MHZ-155-GP 82.30020.D41

1st:82.30020.D41
2nd:82.30020.G71
3rd:82.30020.G61

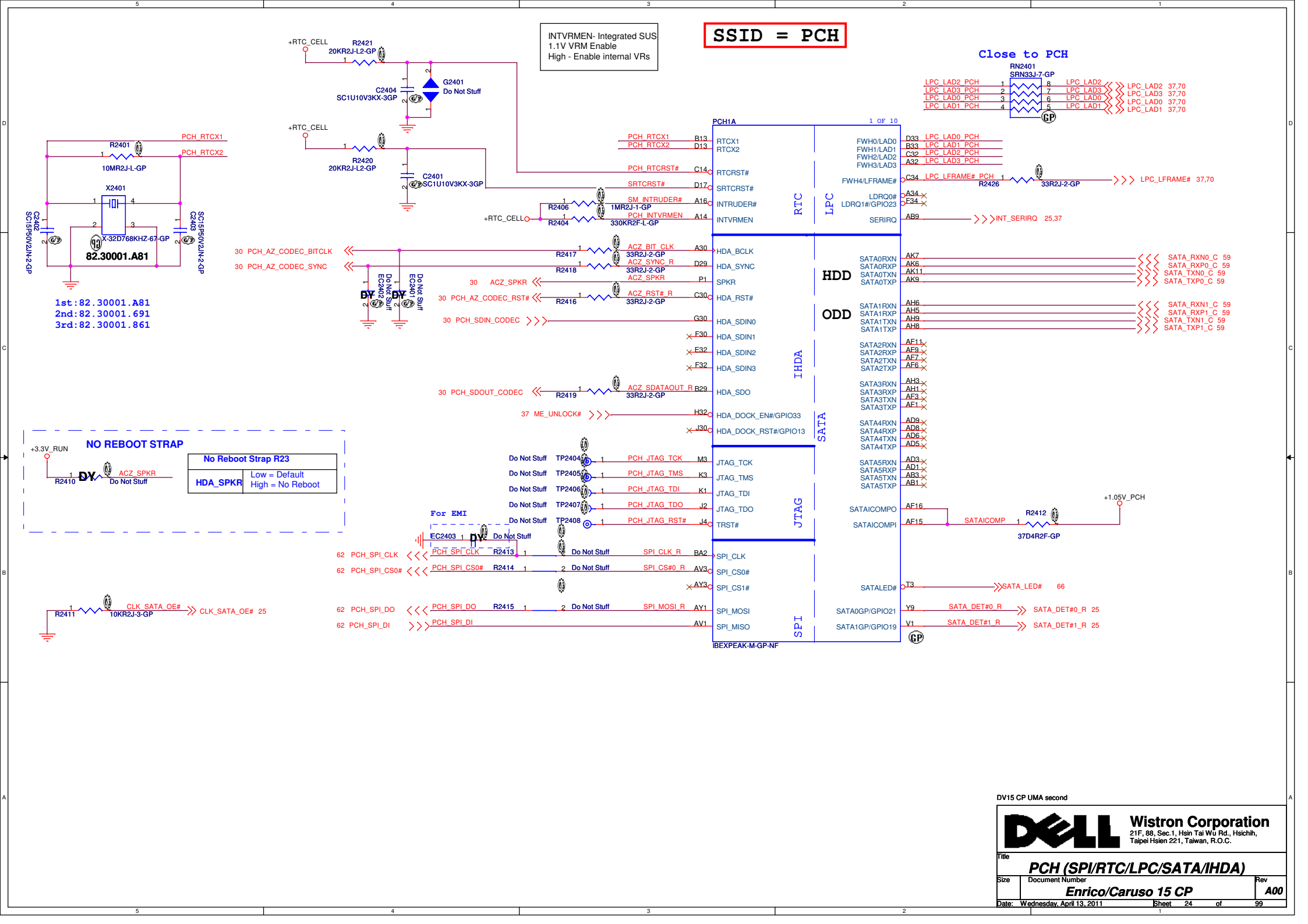
DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

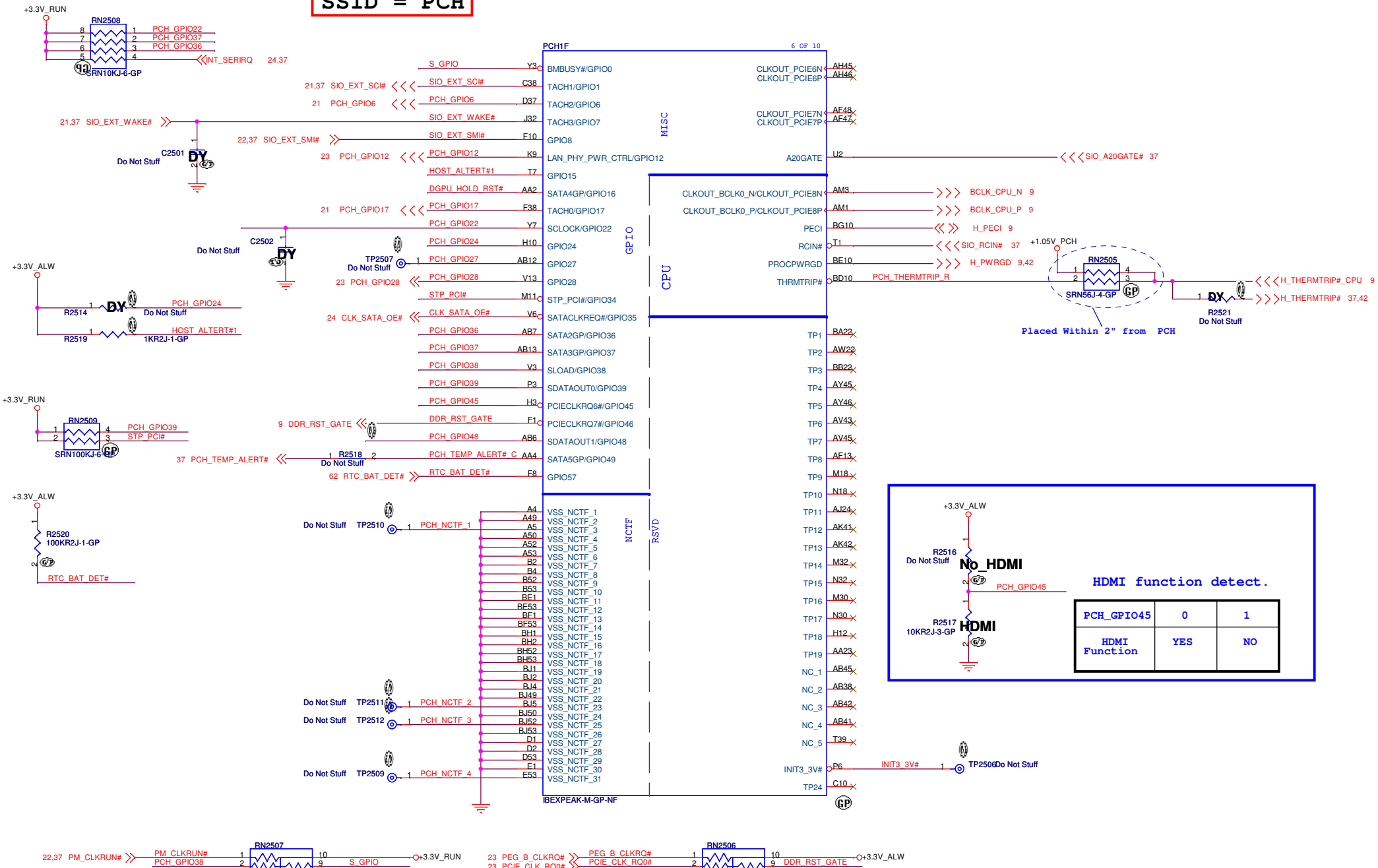
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 23 of 99


SSID = PCH
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
Close to PCH
PCH1A
1 OF 10
IBEXPEAK-M-GP-NF
RTC
LPC
HDA
SATA
JTAG
SPI
HDD
ODD
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
For EMI
82.30001.A81
1st:82.30001.A81
2nd:82.30001.691
3rd:82.30001.861
DV15 CP UMA second
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (SPI/RTC/LPC/SATA/IHDA)
Enrico/Caruso 15 CP
A00
Wednesday, April 13, 2011
24
99

SSID = PCH

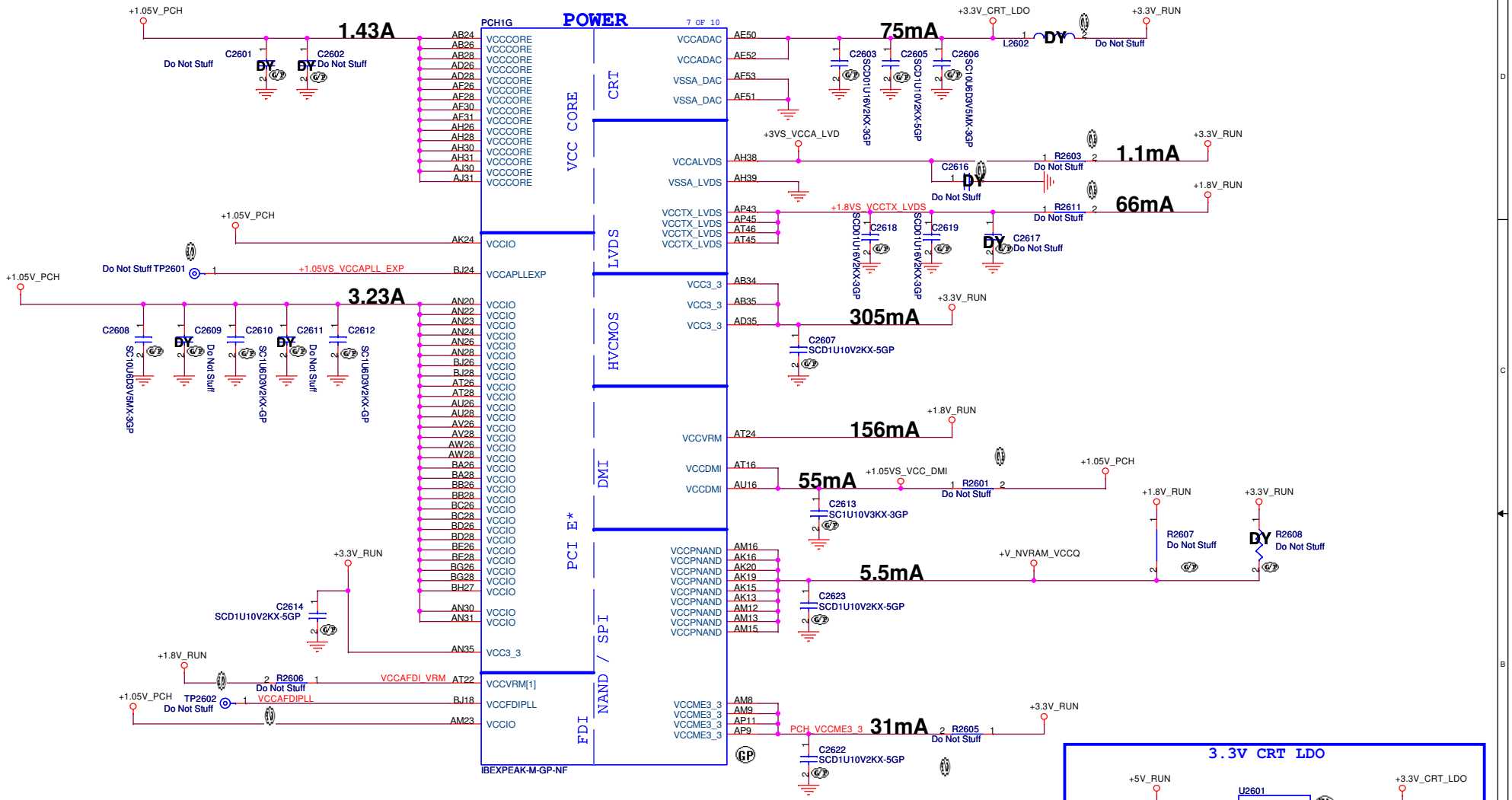


DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (GPIO/CPU)	
Size	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 25 of 99	

SSID = PCH



DV15 CP UMA second

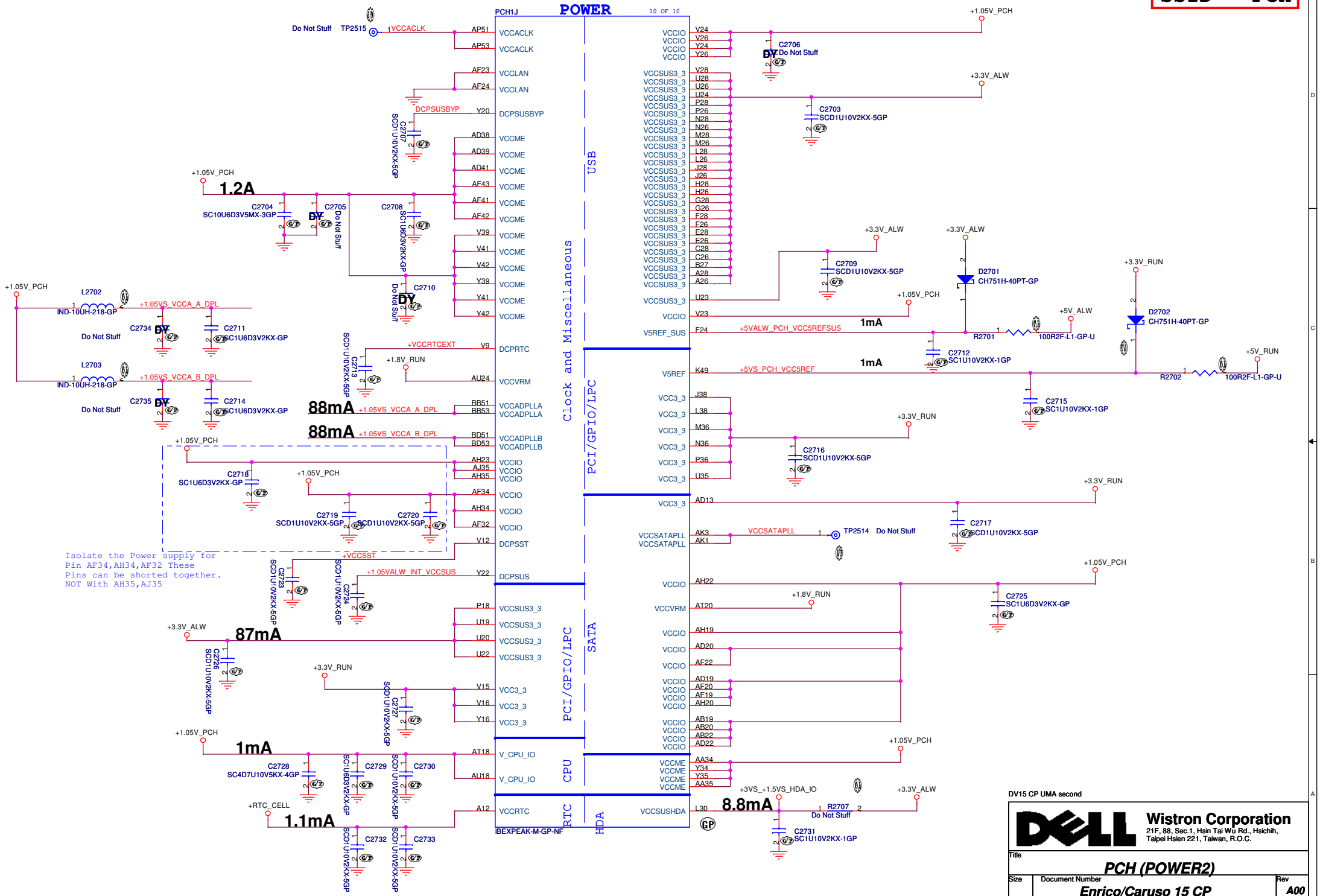
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 26 of 99

SSID = PCH



DV15 CP UMA second

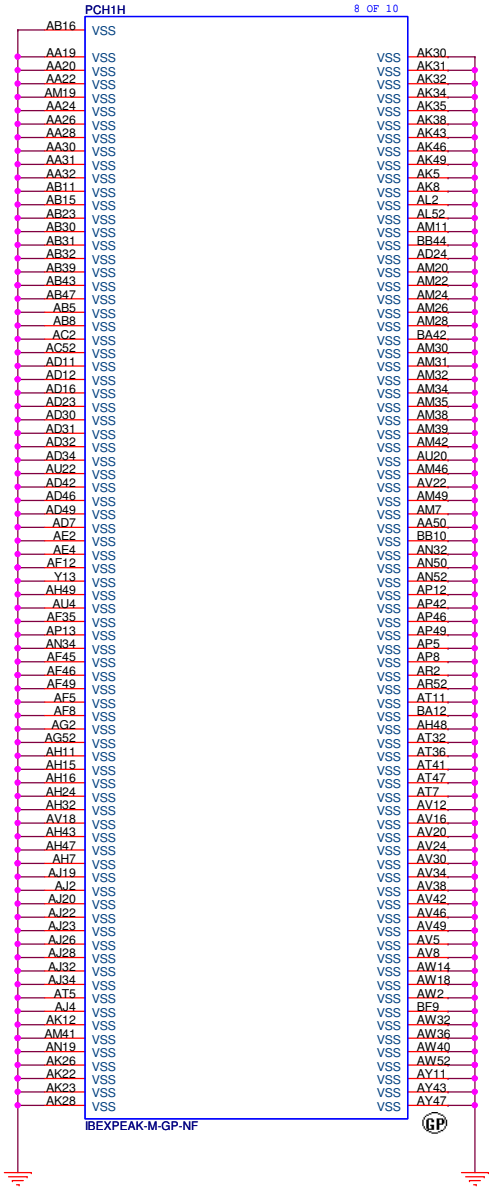
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

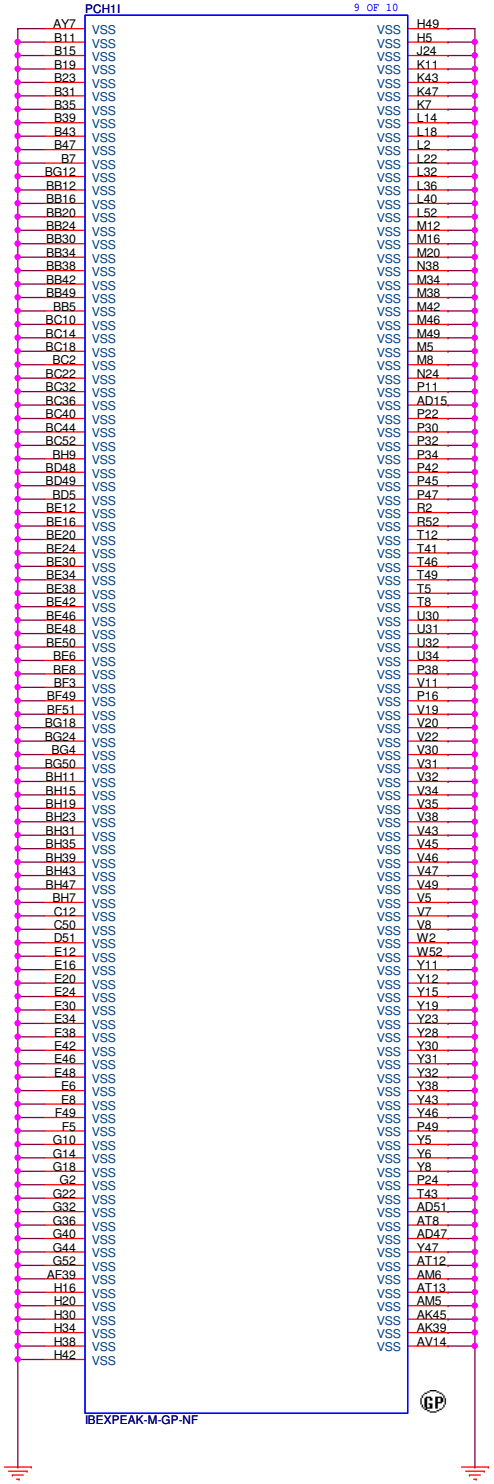
Title: PCH (POWER2)

Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 27 of 99

SSID = PCH





DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
	Enrico/Caruso 15 CP	***A00***

Date: Friday, April 08, 2011 Sheet 28 of 99

(Blanking)

DV15 CP UMA second

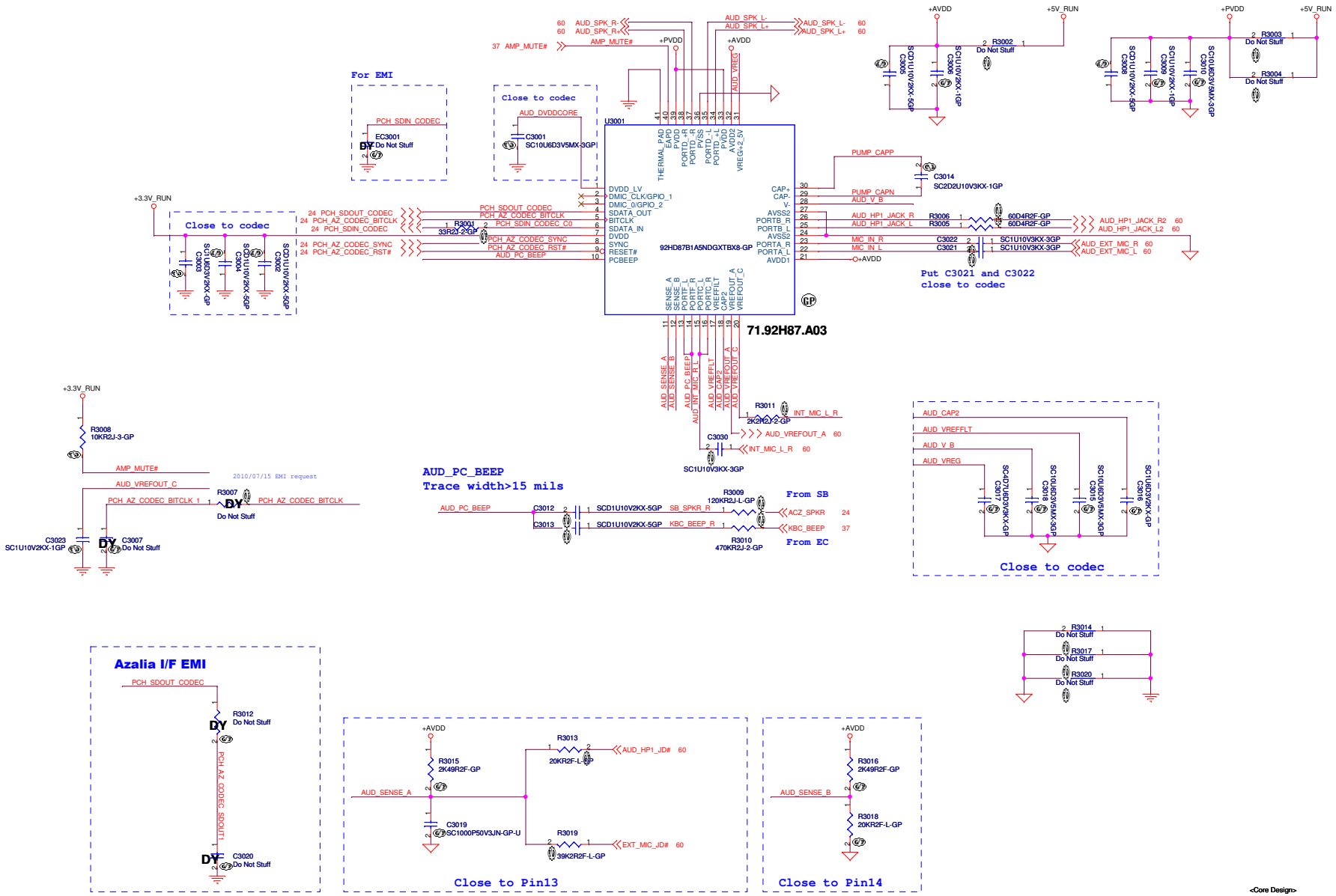
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 29 of 99

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec 92HD87B1**

Size: Custom | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 30 of 99

(Blanking)

DV15 CP UMA second

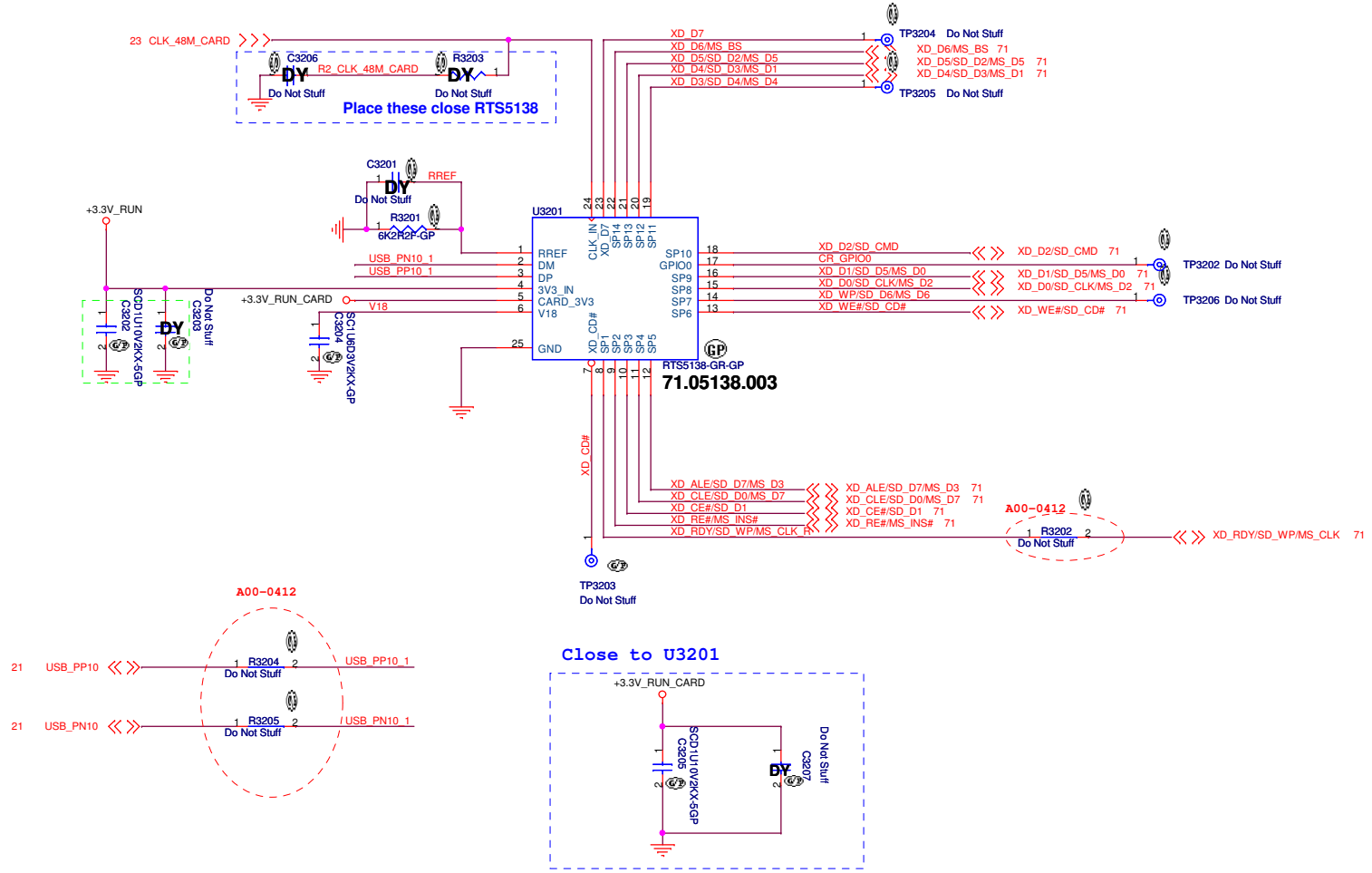
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 31 of 99

SSID = SDIO



DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-RTS5138***

Size	Document Number	Rev
Custom	***Enrico/Caruso 15 CP***	***A00***

Date: Wednesday, April 13, 2011 Sheet 32 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 33 of 99

(Blanking)

DV15 CP UMA second

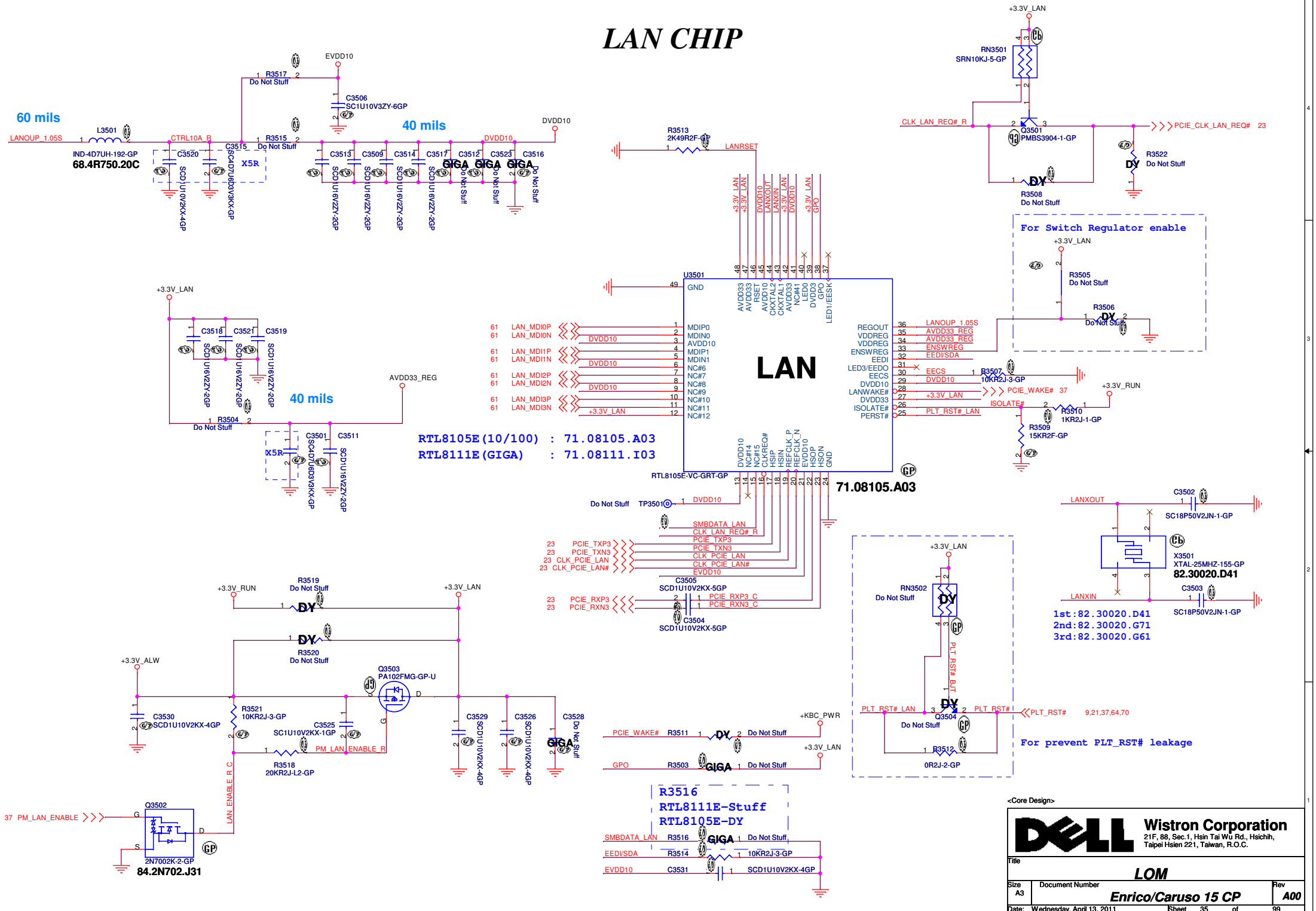
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 34 of 99

LAN CHIP


60 mils
40 mils
40 mils
LANOUP_1.05S
L3501
IND-4D7UH-192-GP
68.4R750.20C
CTRL10A_R
C3520
C3515
SC4D7U6D3V3KX-GP
X5R
EVDD10
R3517
Do Not Stuff
C3506
SC1U10V3ZY-6GP
R3515
Do Not Stuff
DVDD10
C3513
C3509
C3514
C3517
C3512
C3523
C3516
GIGA
GIGA
GIGA
SCD1U16V2ZY-2GP
Do Not Stuff
+3.3V_LAN
C3518
C3521
C3519
SCD1U16V2ZY-2GP
AVDD33_REG
R3504
Do Not Stuff
C3501
C3511
X5R
SCD1U16V2ZY-2GP
R3513
2K49R2F-GP
LANRSET
U3501
GND
LAN
MDIP0
MDIN0
AVDD10
MDIP1
MDIN1
NC#6
NC#7
NC#8
NC#9
NC#10
NC#11
NC#12
REGOUT
VDDREG
VDDREG
ENSWREG
EEDI
LED3/EEDO
EECS
DVDD10
LANWAKE#
DVDD33
ISOLATE#
PERST#
LANOUP_1.05S
AVDD33_REG
AVDD33_REG
ENSWREG
EEDI/SDA
EECS
DVDD10
PCIE_WAKE# 37
+3.3V_LAN
PLT_RST# LAN
RTL8105E-VC-GRT-GP
71.08105.A03
RTL8105E(10/100) : 71.08105.A03
RTL8111E(GIGA) : 71.08111.I03
LAN_MDI0P
LAN_MDI0N
LAN_MDI1P
LAN_MDI1N
LAN_MDI2P
LAN_MDI2N
LAN_MDI3P
LAN_MDI3N
DVDD10
+3.3V_LAN
R3507
10KR2J-3-GP
R3510
1KR2J-1-GP
R3509
15KR2F-GP
+3.3V_RUN
ISOLATE#
For Switch Regulator enable
R3505
Do Not Stuff
R3506
Do Not Stuff
RN3501
SRN10KJ-5-GP
CLK_LAN_REQ# R
Q3501
PMBS3904-1-GP
R3508
Do Not Stuff
R3522
Do Not Stuff
PCIE_CLK_LAN_REQ# 23
TP3501
SMBDATA_LAN
CLK_LAN_REQ# R
PCIE_TXP3
PCIE_TXN3
CLK_PCIE_LAN
CLK_PCIE_LAN#
EVDD10
C3505
SCD1U10V2KX-5GP
C3504
SCD1U10V2KX-5GP
PCIE_RXP3_C
PCIE_RXN3_C
PCIE_RXP3
PCIE_RXN3
LANXOUT
LANXIN
C3502
C3503
SC18P50V2JN-1-GP
X3501
XTAL-25MHZ-155-GP
82.30020.D41
1st:82.30020.D41
2nd:82.30020.G71
3rd:82.30020.G61
RN3502
Do Not Stuff
PLT_RST# BUT
Q3504
Do Not Stuff
R3512
0R2J-2-GP
PLT_RST# LAN
PLT_RST#
PLT_RST# 9,21,37,64,70
For prevent PLT_RST# leakage
+3.3V_RUN
+3.3V_LAN
R3519
Do Not Stuff
R3520
Do Not Stuff
+3.3V_ALW
Q3503
PA102FMG-GP-U
C3530
SCD1U10V2KX-4GP
R3521
10KR2J-3-GP
C3525
SC1U10V2KX-1GP
PM_LAN_ENABLE_R
R3518
20KR2J-L2-GP
C3529
C3526
C3528
SCD1U10V2KX-4GP
Do Not Stuff
LAN_ENABLE_R_C
37 PM_LAN_ENABLE
Q3502
2N7002K-2-GP
84.2N702.J31
+KBC_PWR
PCIE_WAKE#
R3511
Do Not Stuff
GPO
R3503
Do Not Stuff
R3516
RTL8111E-Stuff
RTL8105E-DY
SMBDATA_LAN
R3516
EEDI/SDA
R3514
10KR2J-3-GP
EVDD10
C3531
SCD1U10V2KX-4GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LOM
Size
A3
Document Number
Enrico/Caruso 15 CP
Rev
A00
Date: Wednesday, April 13, 2011
Sheet 35 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 36 of 99

CAP close to VCC-GND pin pair

SSID = KBC

U3701A

NPCE781BA0DX-GP

MB VERSION		
ID	VER1	VER0
X00	0	0
X01	0	1
X02	1	0
A00	1	1

EC HW Strap Pin			
Net Name	Pin	GPIO	Note
BLUETOOTH_EN	83	GPO76	Pull-Low
USB_PWR_EN#	110	GPO82	Dont Pull-Low
E51_TXD	111	GPO83	Dont Pull-Low
AC_PRESENT_EC	112	GPO84	Dont Pull-Low
KCOL0	53	KBSOUT0	Dont Pull-Low
KCOL4	49	KBSOUT4	Dont Pull-Low
KCOL9	41	KBSOUT9	Dont Pull-Low

PCH_SUSCLK_KBC

KBC CLK EMI

SERIES_ID	Inspirion	Vostro
	1	0

U3701B

KBC

PS/2

FIU

Q3705 2N7002K-2-GP 84.2N702.J31

Q3704 PA1203MG-GP-U 84.00102.031 BOM merge

Q3702 PMBS3906-GP

U3702

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 15, 2011 | Sheet 37 of 99

(Blanking)

DV15 CP UMA second

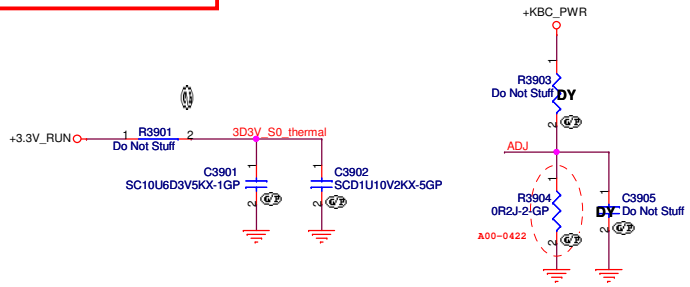
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

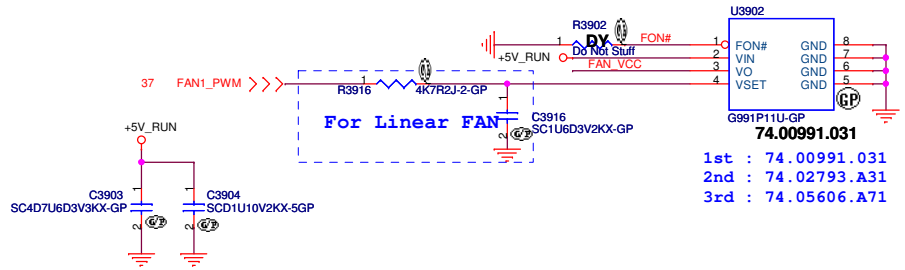
Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 38 of 99

SSID = Thermal



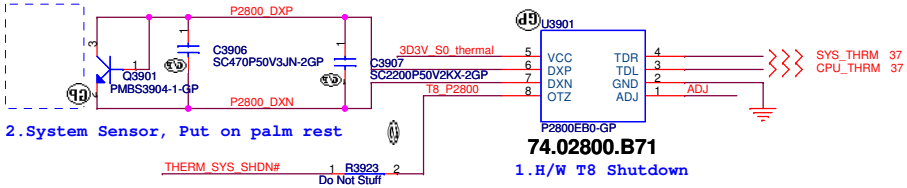
Fan controller



Thermal sensor P2800

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

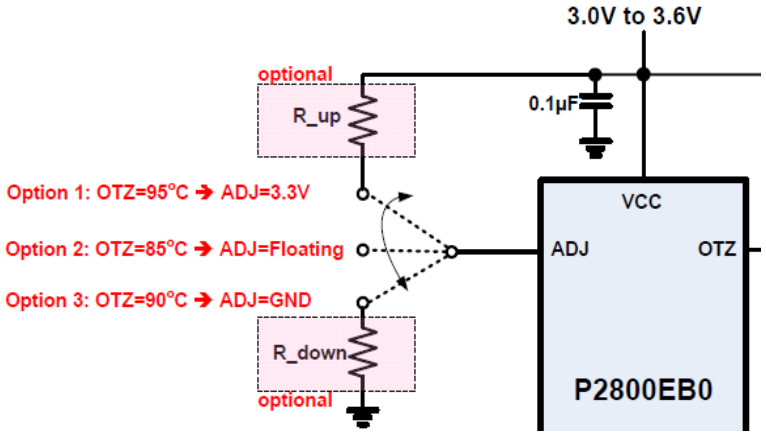
Remove R3908 and
put C3906 close to Q3901



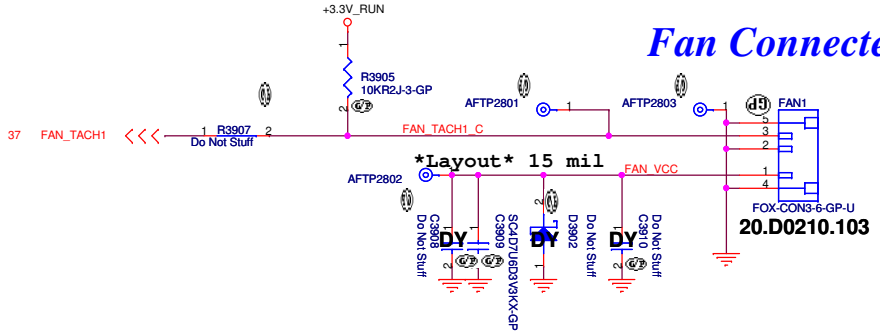
2.System Sensor, Put on palm rest

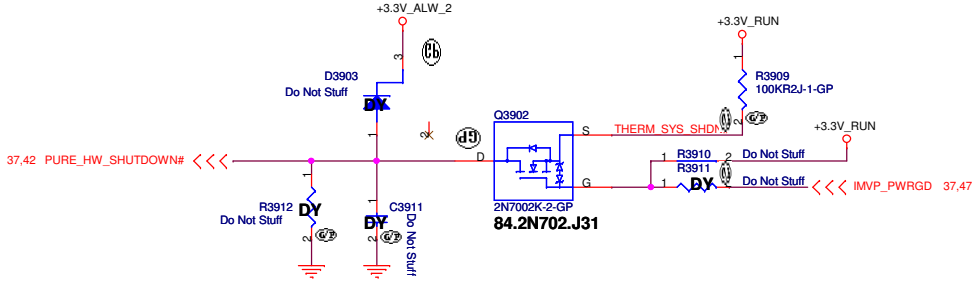
74.02800.B71

1.H/W T8 Shutdown

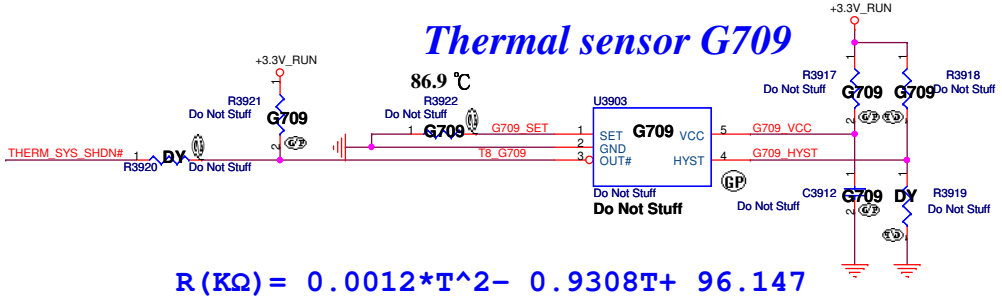


Fan Connecter





Thermal sensor G709



R(KΩ)= 0.0012*T^2- 0.9308T+ 96.147

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal sensor P2800

Size	Document Number	Rev
Custom	Enrico/Caruso 15 CP	A00

Date: Friday, April 22, 2011 Sheet 39 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 40 of 99

(Blanking)

DV15 CP UMA second

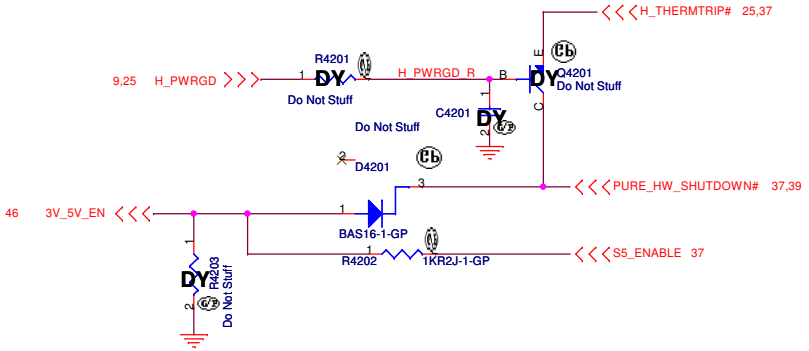
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

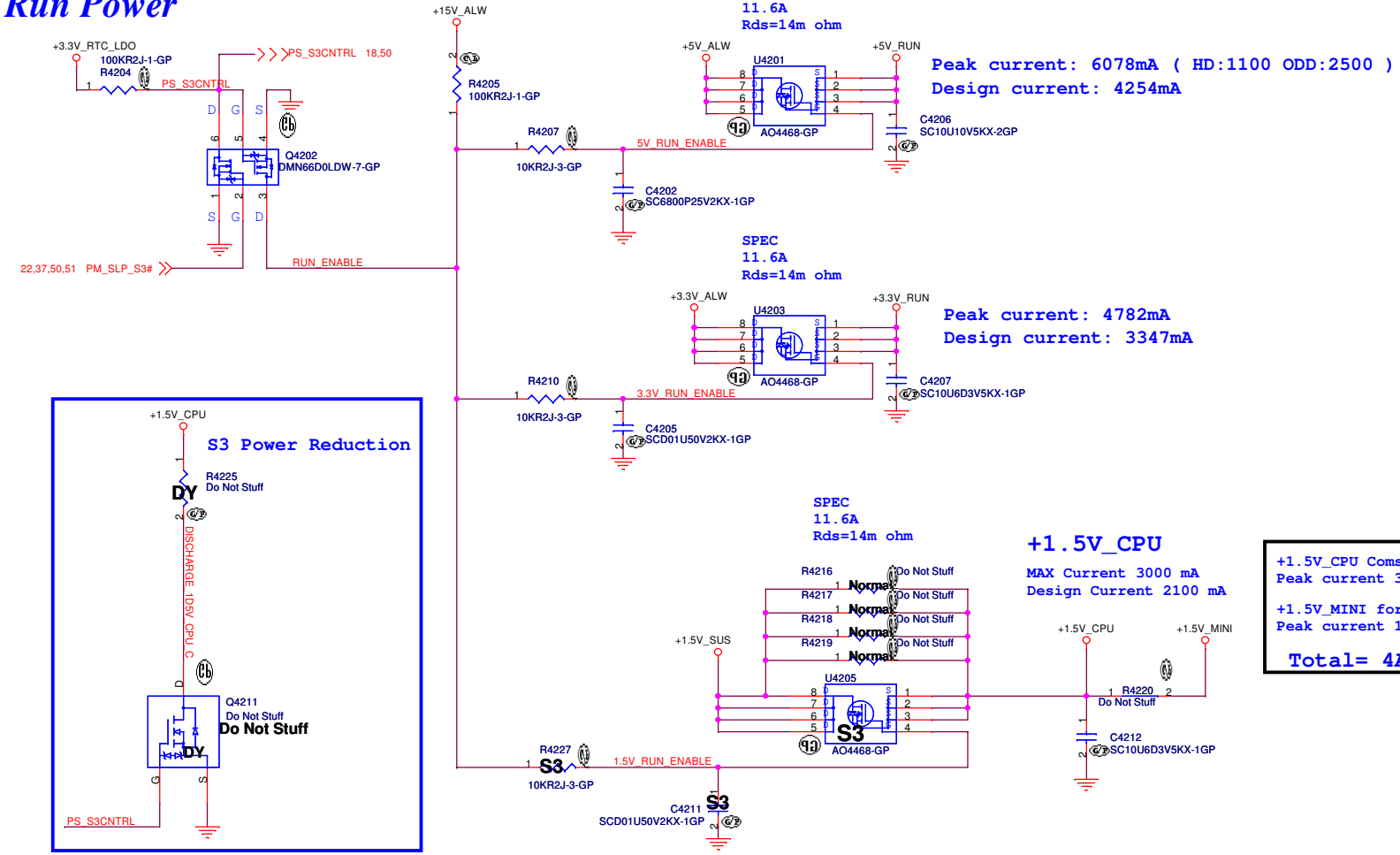
Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 41 of 99

SSID = Reset.Suspend



Run Power



DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

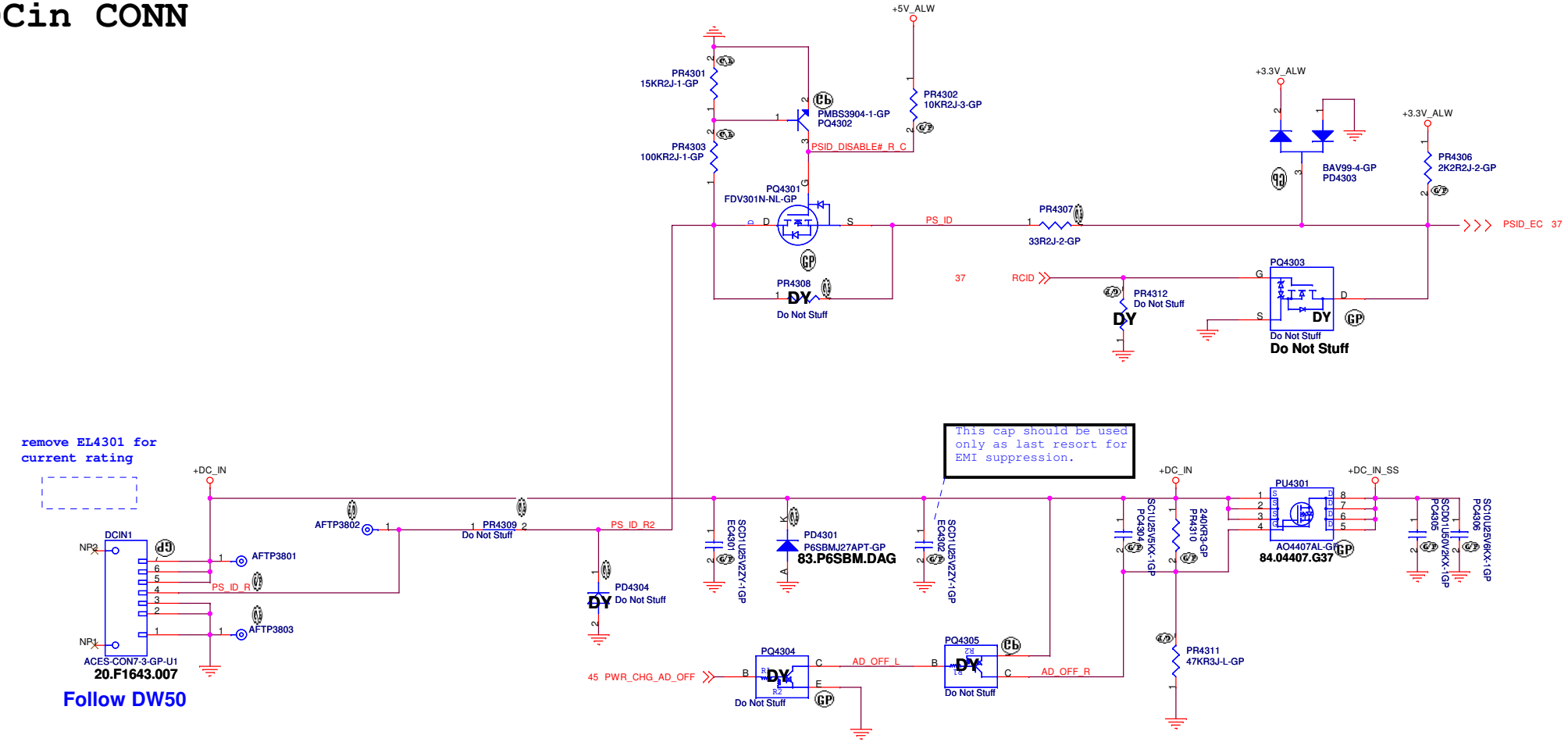
Title: Power Plane Enable

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 42 of 99

SSID = PWR.Support

DCin CONN



DV14 CP

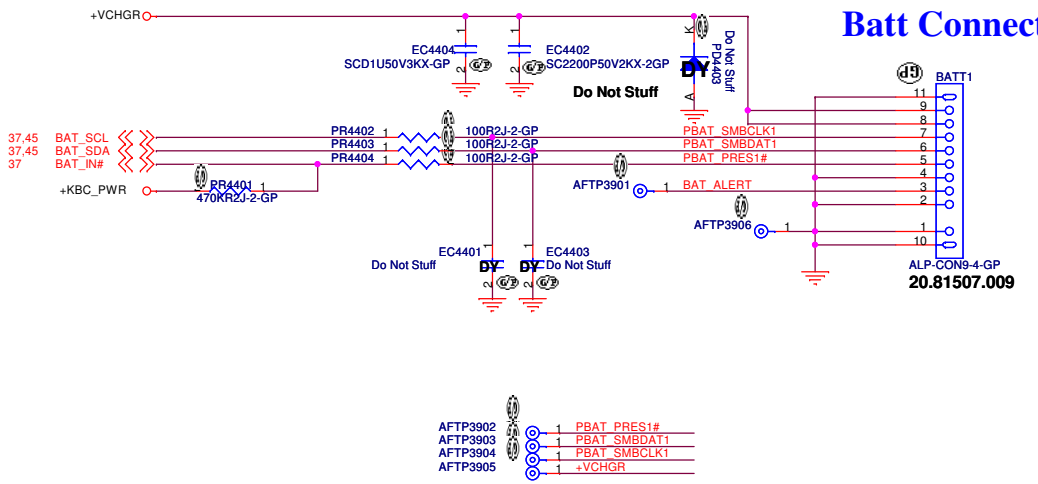
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN Jack

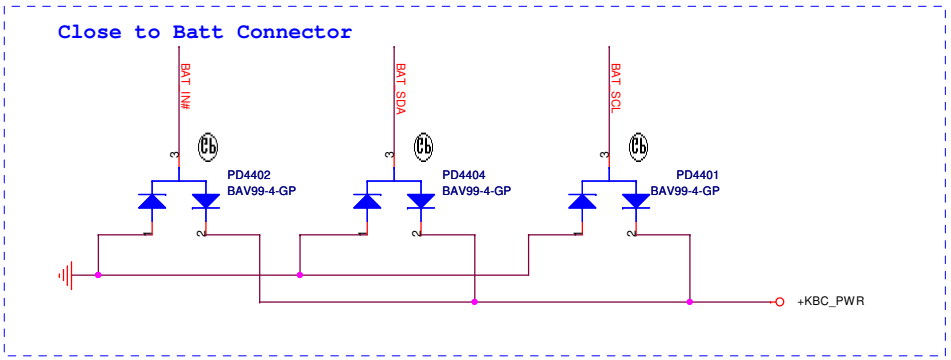
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 43 of 99

SSID = BATT CONN



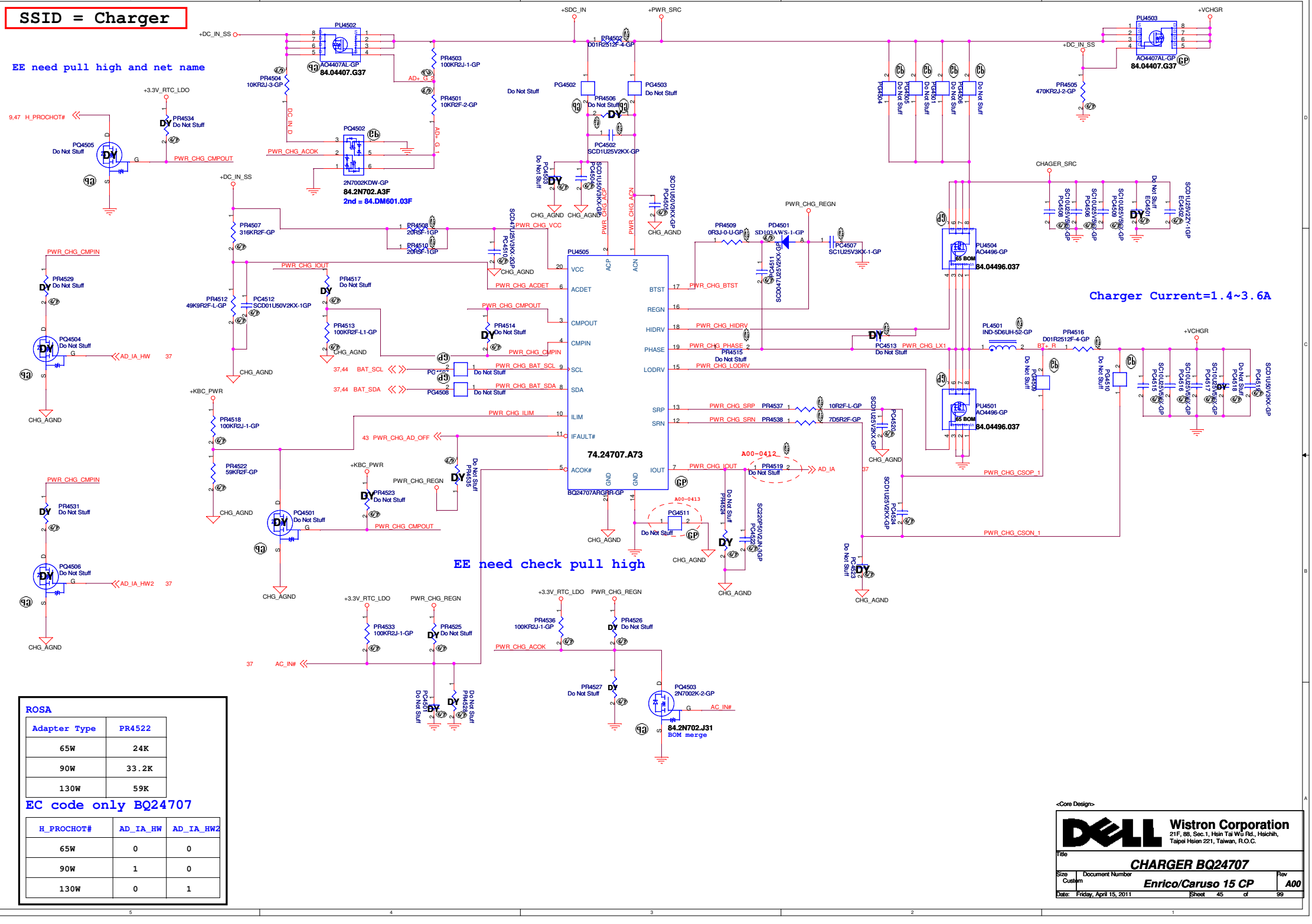
For actual location, need to be swap all pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 44 of 99	



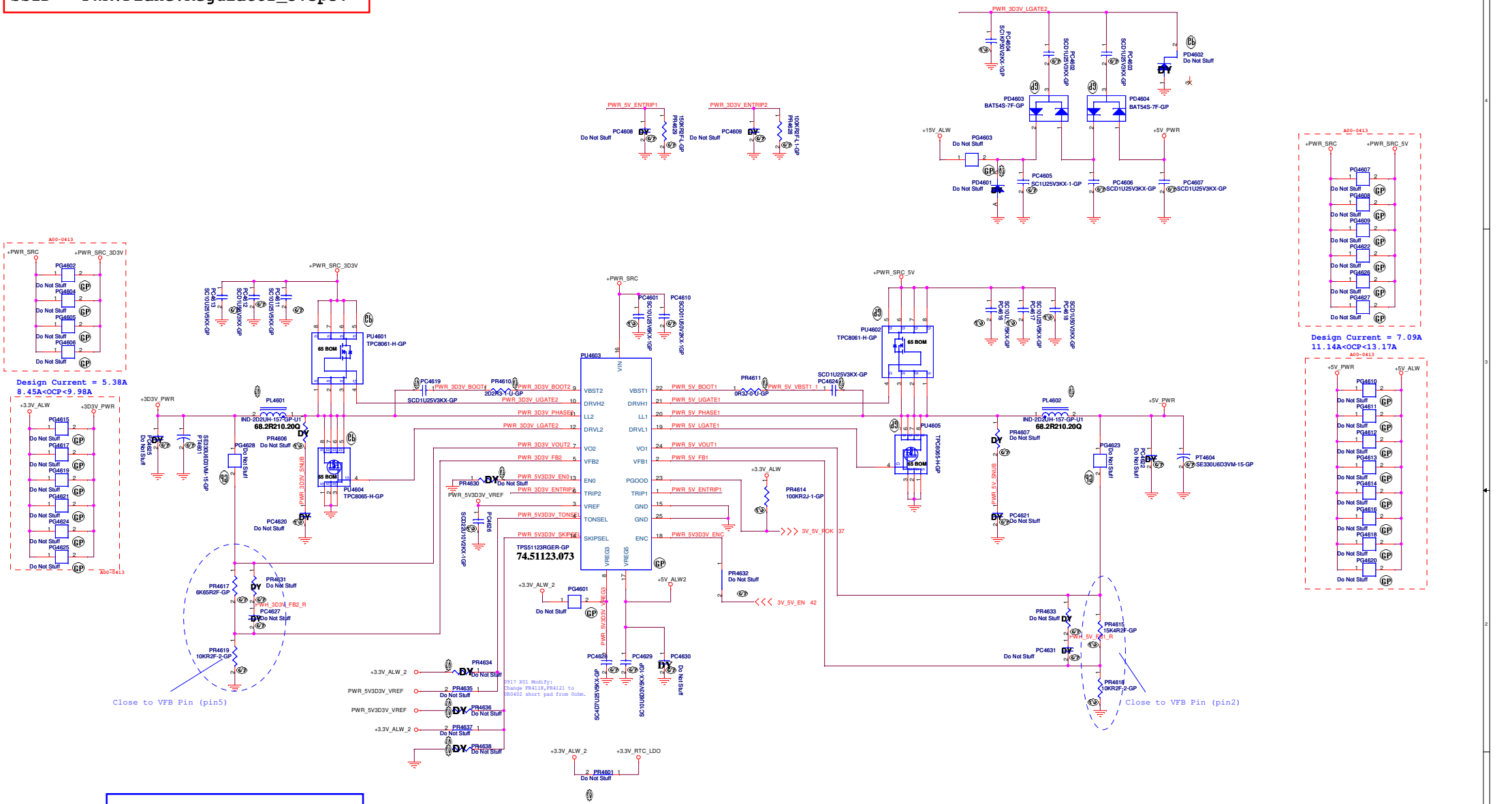
ROSA

Adapter Type	PR4522
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

SSID = PWR.Plane.Regulator_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20Q
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPC8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

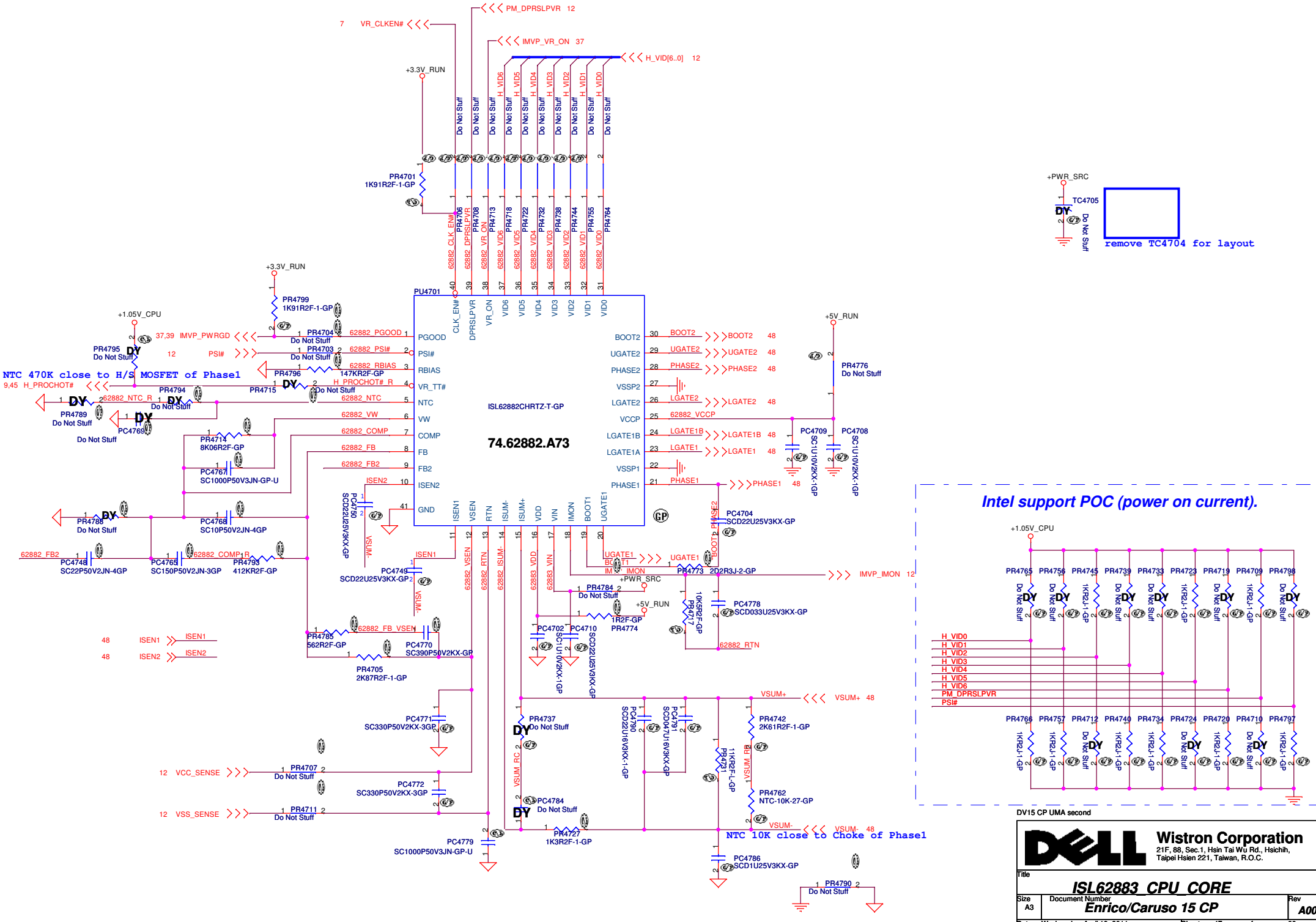
INS 100 NONE SURGE

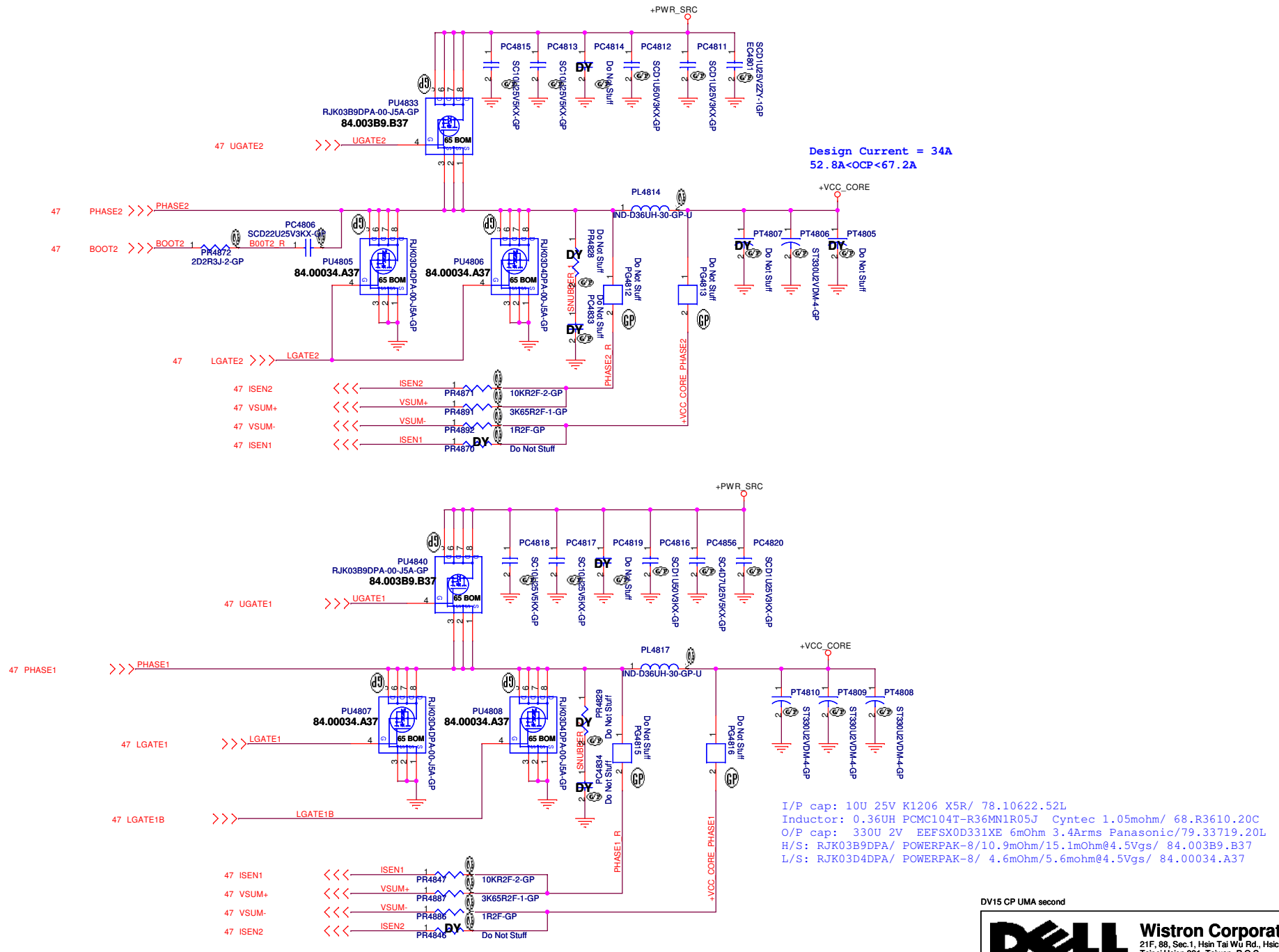
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(TPS51123RGER)

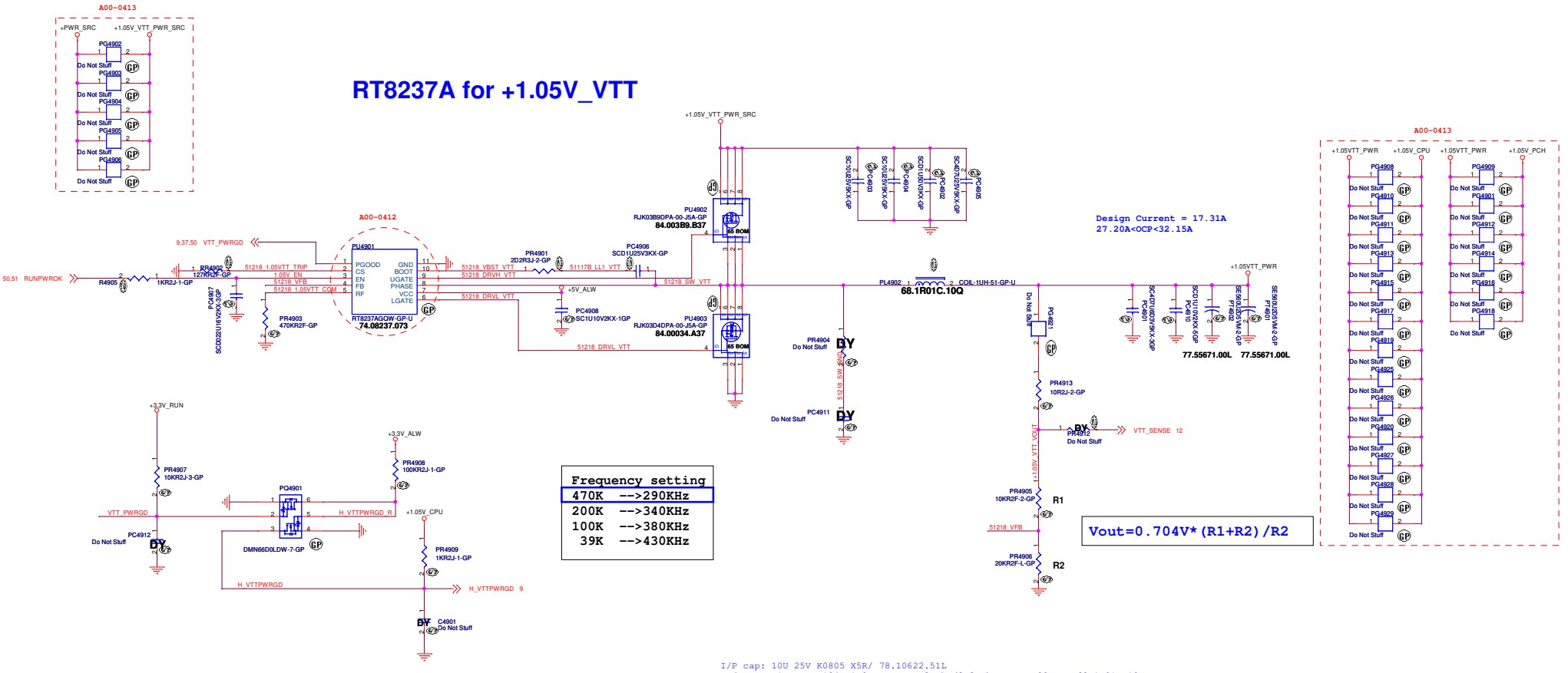
Size: A2 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 46 of 99


PU4701
ISL62882CHRTZ-T-GP
74.62882.A73
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
CLK_EN#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
+3.3V_RUN
+1.05V_CPU
+5V_RUN
+PWR_SRC
NTC 470K close to H/S MOSFET of Phase1
NTC 10K close to Choke of Phase1
remove TC4704 for layout
Intel support POC (power on current).
DV15 CP UMA second
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62883_CPU_CORE
Enrico/Caruso 15 CP
A00
Wednesday, April 13, 2011
47
99


+PWR_SRC
PC4815
PC4813
PC4814
PC4812
PC4811
SCD1U25V2ZY-1GP
EC4801
PU4833
RJK03B9DPA-00-J5A-GP
84.003B9.B37
47 UGATE2
UGATE2
Design Current = 34A
52.8A<OCP<67.2A
PL4814
IND-D36UH-30-GP-U
+VCC_CORE
47 PHASE2
PHASE2
47 BOOT2
BOOT2
PC4806
SCD22U25V3KX-GP
B00T2_R
PR4872
2D2R3J-2-GP
PU4805
84.00034.A37
PU4806
84.00034.A37
RJK03D4DPA-00-J5A-GP
65 BOM
SNUBBER_R
PR4828
PC4833
PG4812
PG4813
PT4807
PT4806
PT4805
ST330U2VDM4-GP
Do Not Stuff
47 LGATE2
LGATE2
47 ISEN2
47 VSUM+
47 VSUM-
47 ISEN1
ISEN2
VSUM+
VSUM-
ISEN1
PR4871
PR4891
PR4892
PR4870
10KR2F-2-GP
3K65R2F-1-GP
1R2F-GP
PHASE2_R
+VCC_CORE_PHASE2
+PWR_SRC
PC4818
PC4817
PC4819
PC4816
PC4856
PC4820
SCD1U25V5KX-GP
SC4D7U25V5KX-GP
PU4840
RJK03B9DPA-00-J5A-GP
84.003B9.B37
47 UGATE1
UGATE1
PL4817
IND-D36UH-30-GP-U
+VCC_CORE
47 PHASE1
PHASE1
PU4807
84.00034.A37
PU4808
84.00034.A37
PR4829
PG4815
PG4816
PT4810
PT4809
PT4808
47 LGATE1
LGATE1
47 LGATE1B
LGATE1B
PHASE1_R
+VCC_CORE_PHASE1
47 ISEN1
47 VSUM+
47 VSUM-
47 ISEN2
PR4847
PR4887
PR4886
PR4846
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37
DV15 CP UMA second
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883_CPU_CORE
Size A3
Document Number
Enrico/Caruso 15 CP
Rev A00
Date: Wednesday, April 13, 2011
Sheet 48 of 99

RT8237A for +1.05V_VTT



Design Current = 17.31A
27.20A<OCP<32.15A

Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1UH PCMC104T-1R0MH Cyntec 3mohm/3.3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L
O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV14 CP

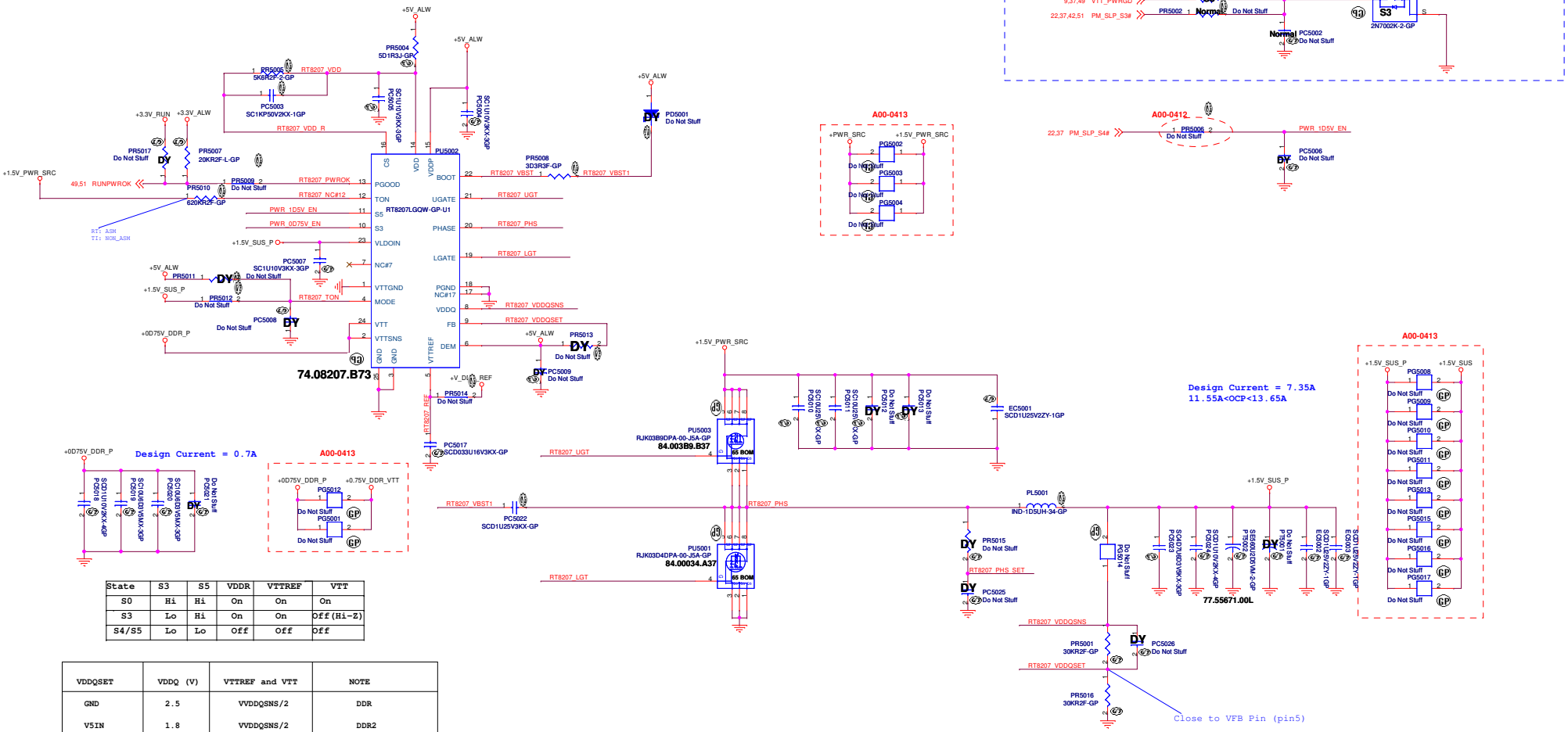
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8237A +1.05V_VTT

Size	Document Number	Rev
A2	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 49 of 99

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5U PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: CHIP CAP POL 560U 2.5V 6.3*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

<Core Design>

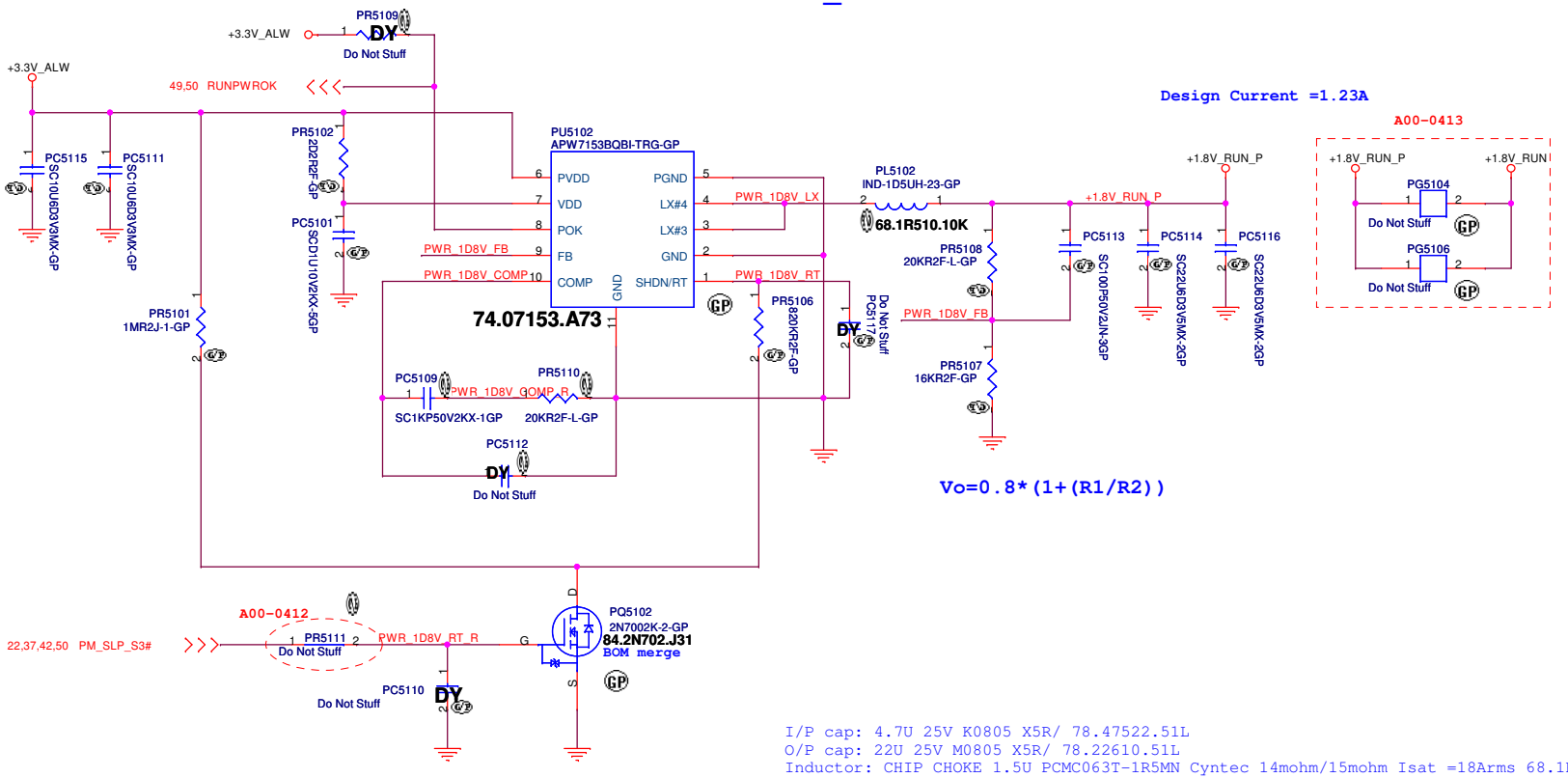
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207_+1.5V_SUS

Size: A2 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 50 of 59

APW7153B for 1D8V_RUN



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

INS 100 NONE SURGE

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APW7153B for 1D8V_RUN	
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Friday, April 15, 2011	Sheet 51 of 99	

(Blanking)

DV15 CP UMA second

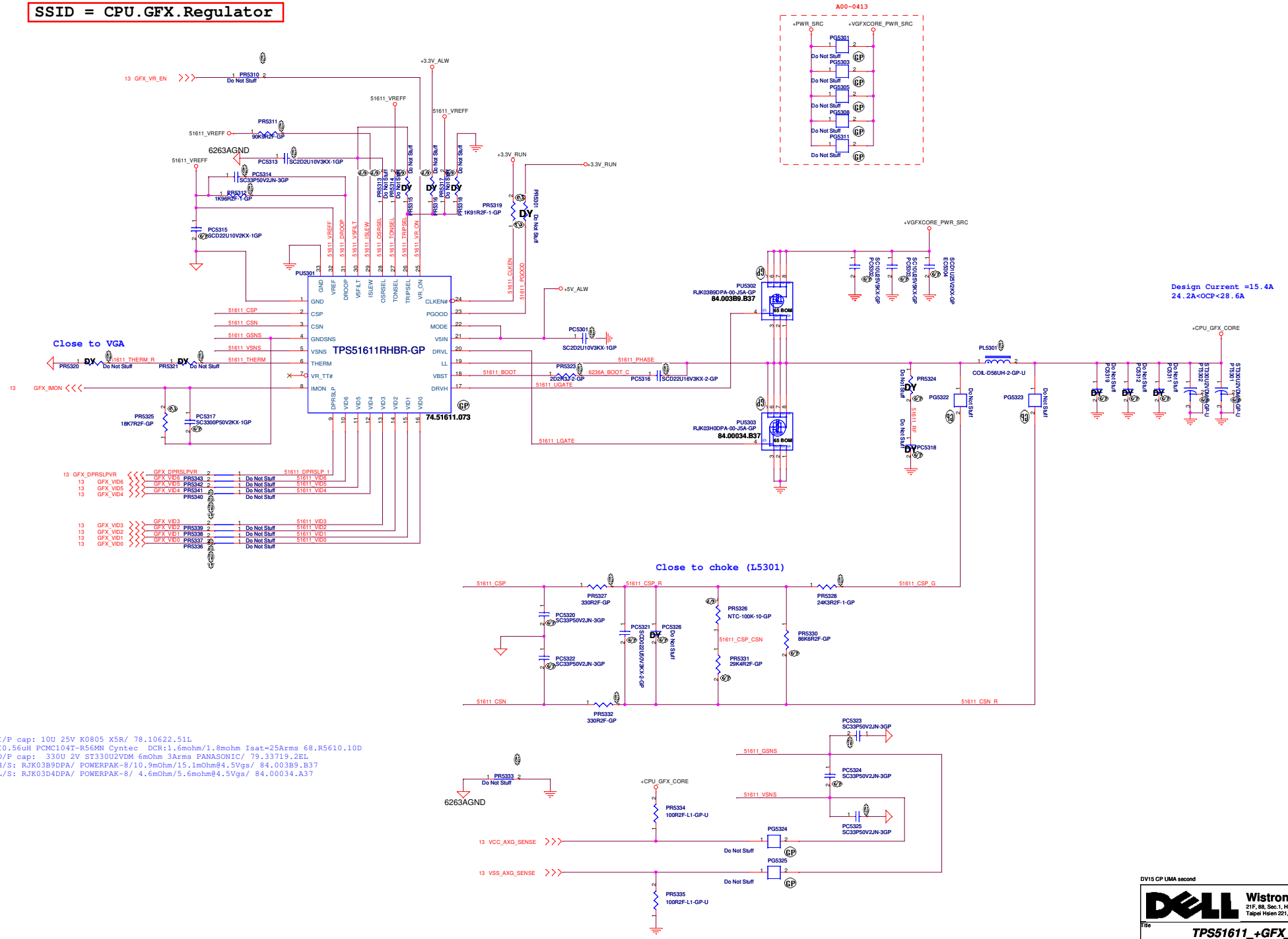
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 52 of 99

SSID = CPU.GFX.Regulator



DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

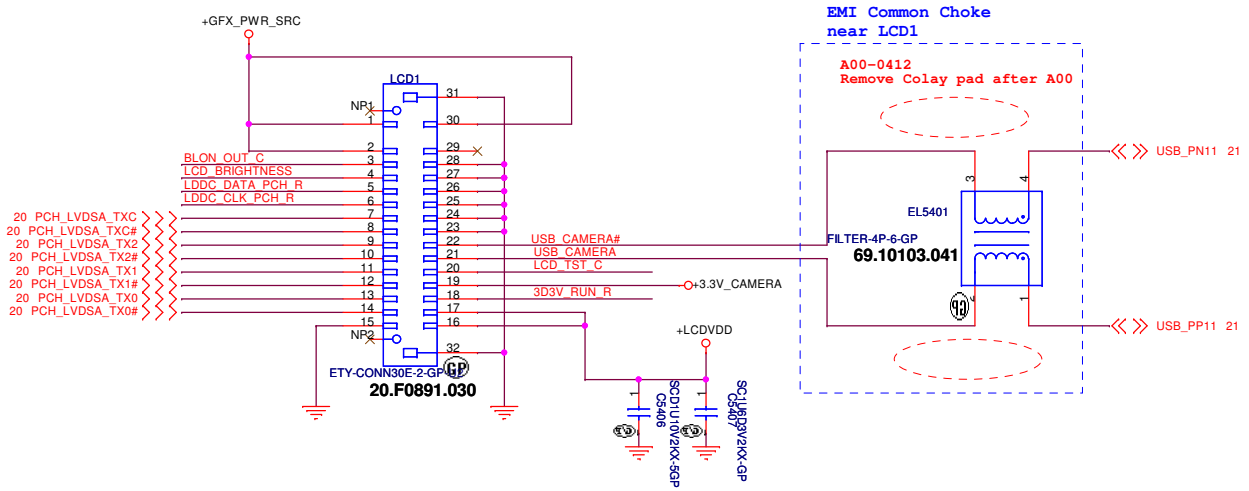
Title: TPS51611_+GFX_CORE

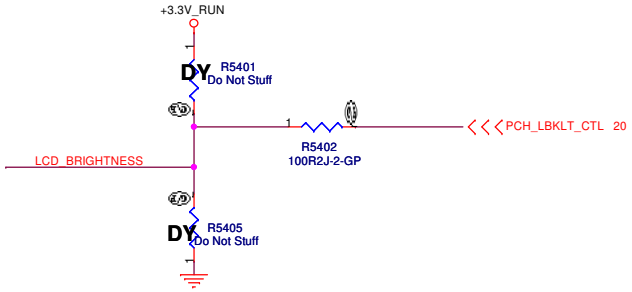
Size: A2 | Document Number: Enrico/Caruso 15 CP | Rev: A00

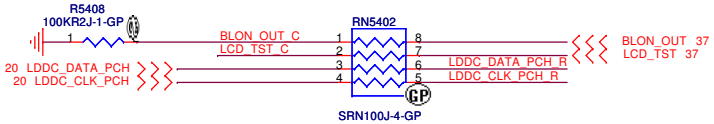
Date: Wednesday, April 13, 2011 | Sheet 53 of 99

SSID = VIDEO

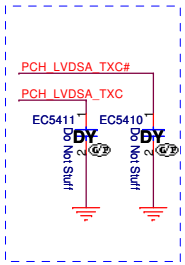
LVDS CONNECTOR

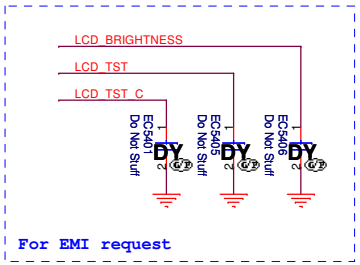


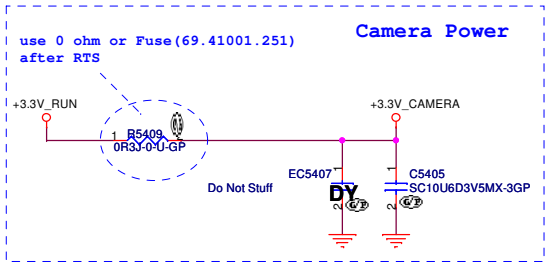




Close to LVDS connector





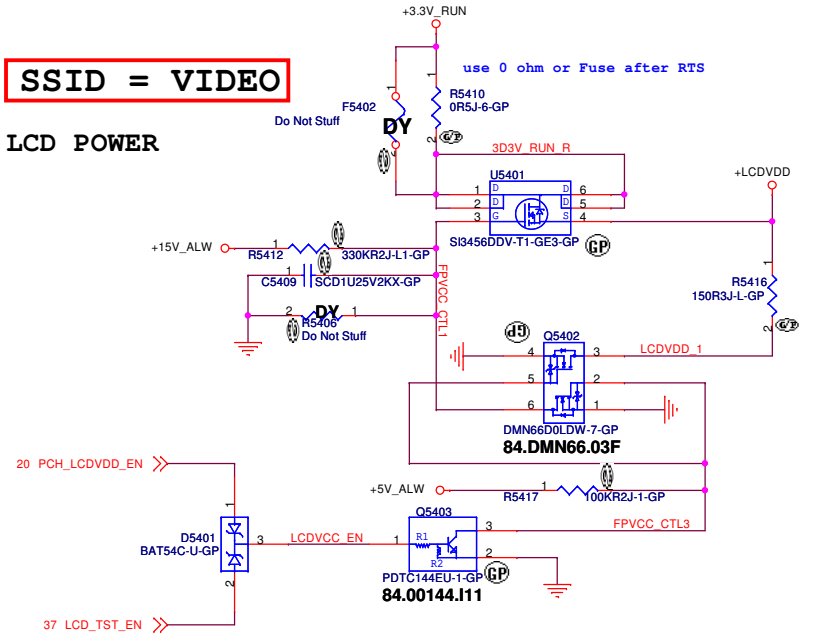


SSID = Inverter

INVERTER POWER

SSID = VIDEO

LCD POWER

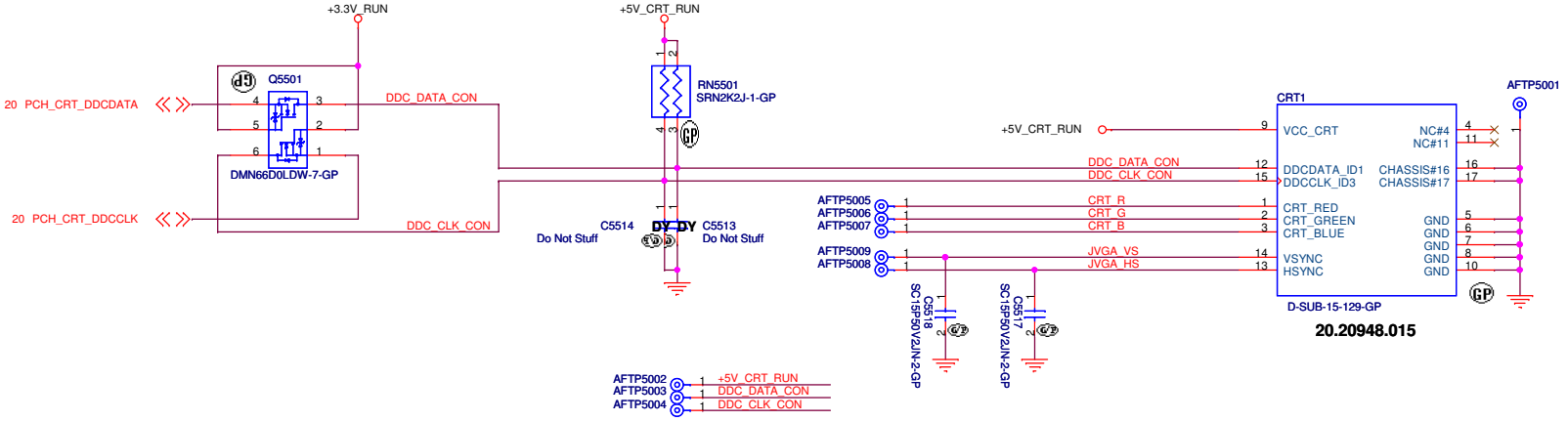


DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
Size A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 54 of 99	

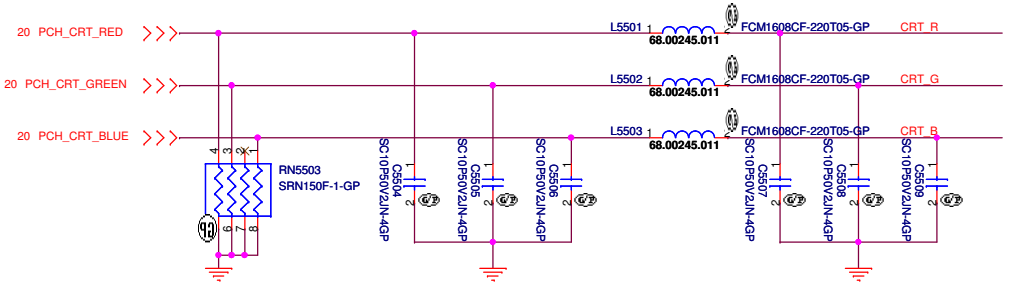
SSID = VIDEO

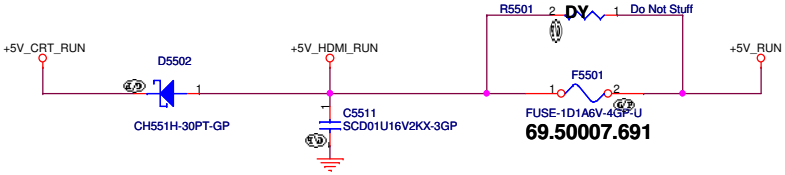


Layout Note:

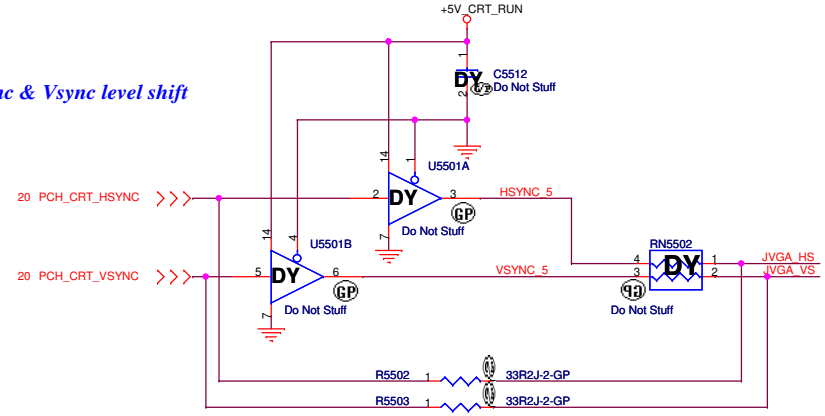
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

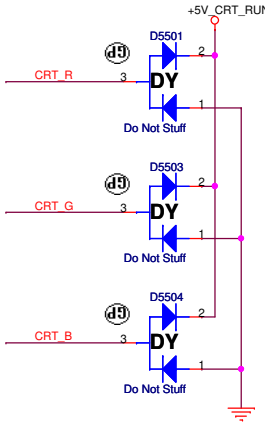
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

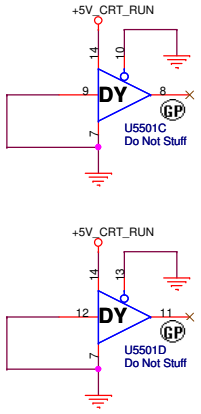




Hsync & Vsync level shift







DV15 CP UMA second

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Title: CRT Connector

Size | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 55 of 99

(Blanking)

DV15 CP UMA second

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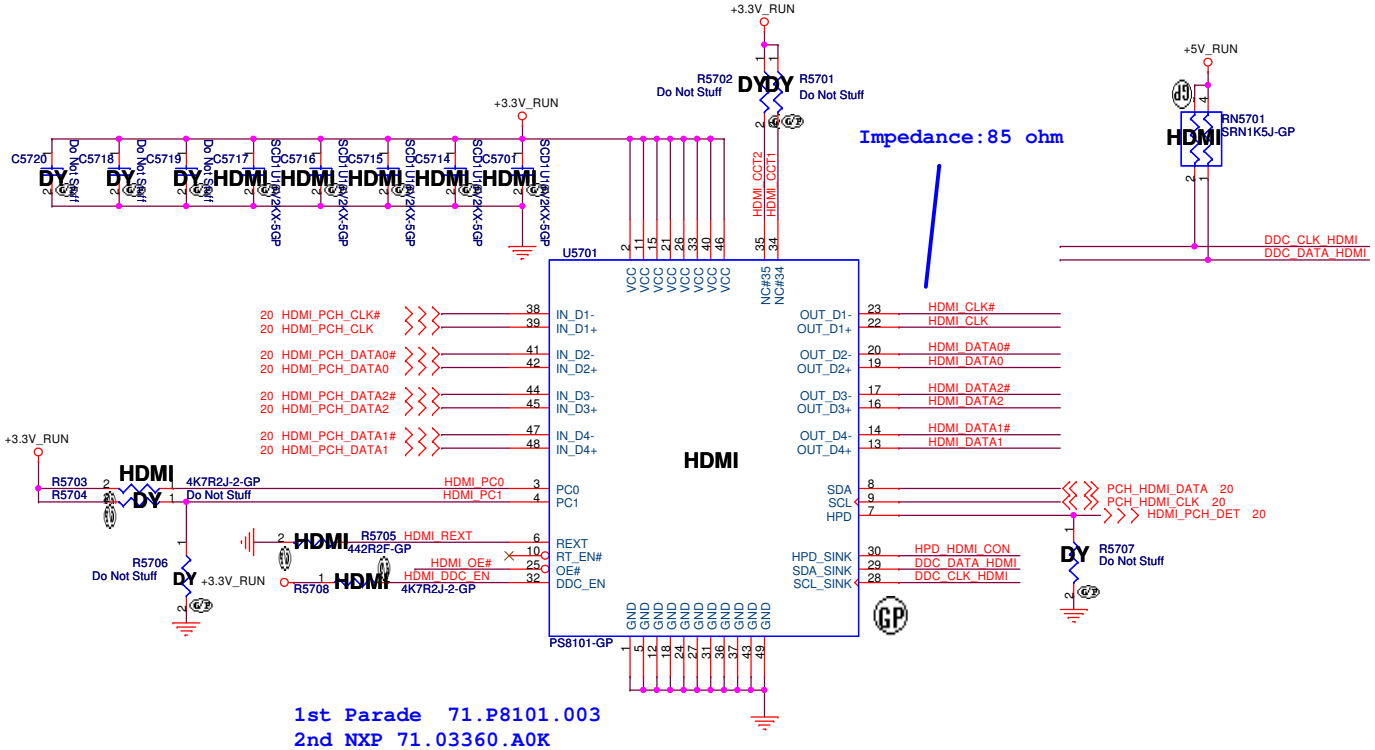
Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 56 of 99

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

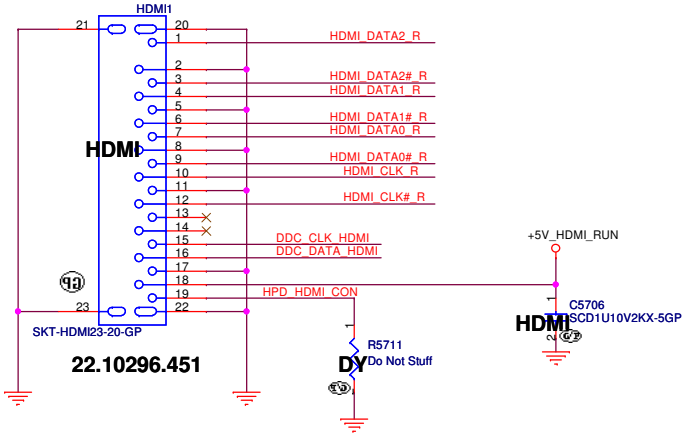


1st Parade 71.P8101.003
2nd NXP 71.03360.A0K
3rd Pericom 71.03411.D03

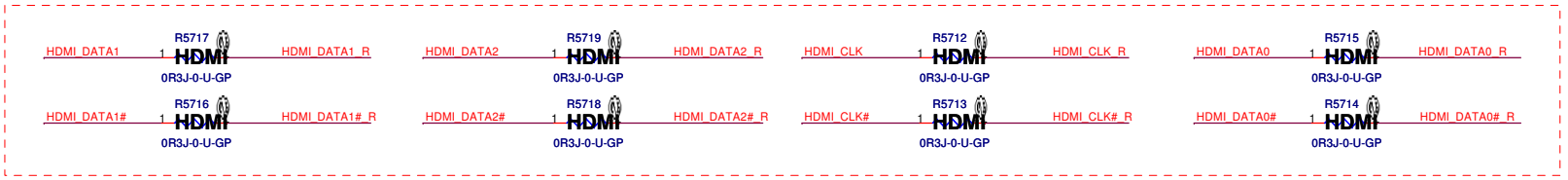
HDMI level shifter BOM controll table

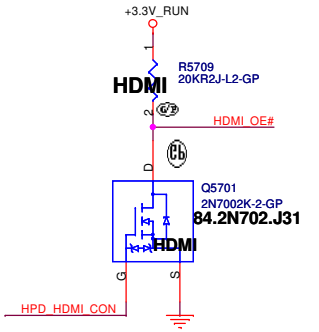
		PS8101	PTN3360B	PI3VDP411LSR
PIN3	R5703	Stuff 4.7K_5%	DY	DY
PIN4	R5704	DY	DY	DY
	R5706	DY	DY	Stuff 200K_5%
PIN6	R5705	Stuff 499_1%	Stuff 10K_1%	DY
PIN10		NC	NC	NC

HDMI CONN



A00-0412





DV15 CP UMA second

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shift/ Connector

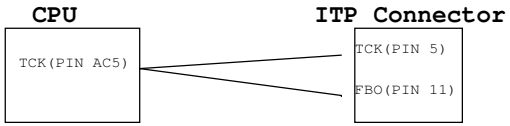
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 57 of 99

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



REMOVE FAN CONNECTOR FOR HR THERMAL SOLUTION 7/12

DV15 CP UMA second

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Taipei Hsien 221, Taiwan, R.O.C.

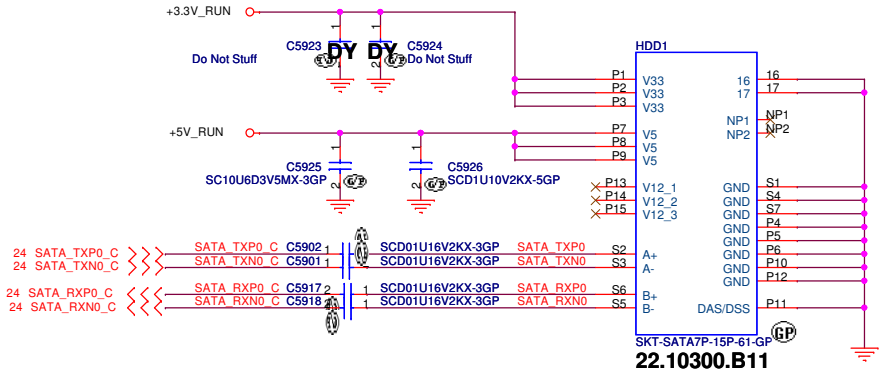
Title: ITP Connector

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 08, 2011 | Sheet 58 of 99

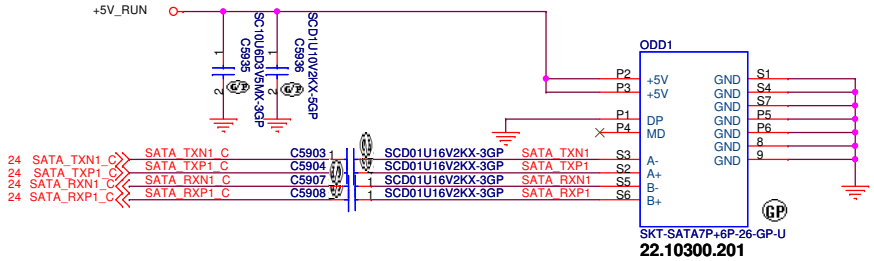
SSID = SATA

SATA HDD Connector



SATA ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

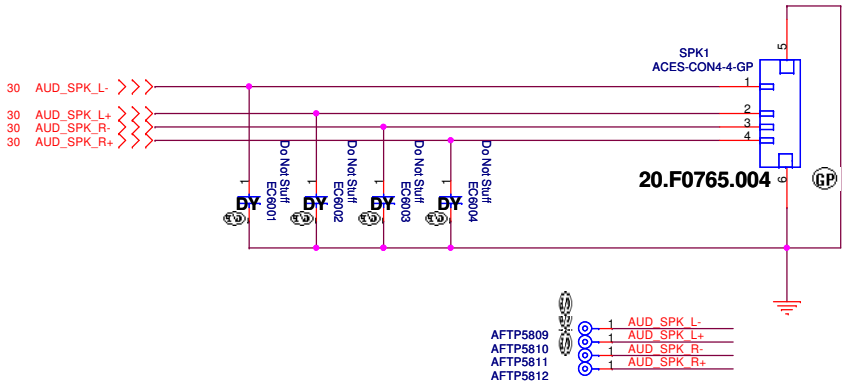
Title: HDD/ODD

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

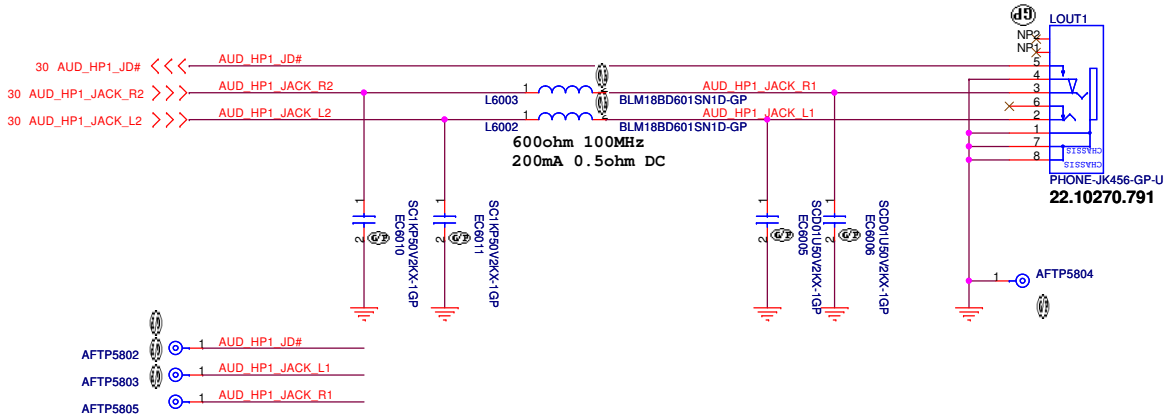
Date: Wednesday, April 13, 2011 Sheet 59 of 99

SSID = AUDIO

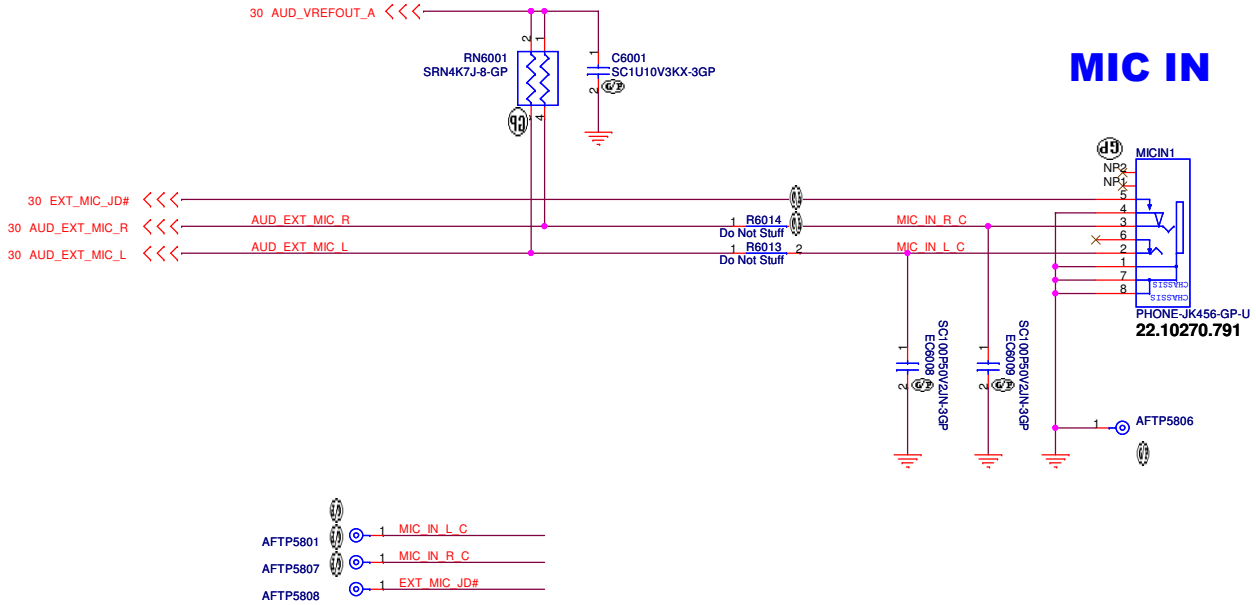
Speaker Connector



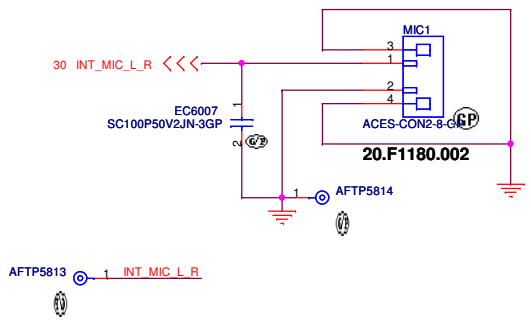
LINE1 OUT



MIC IN



Internal Microphone



DV15 CP UMA second

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

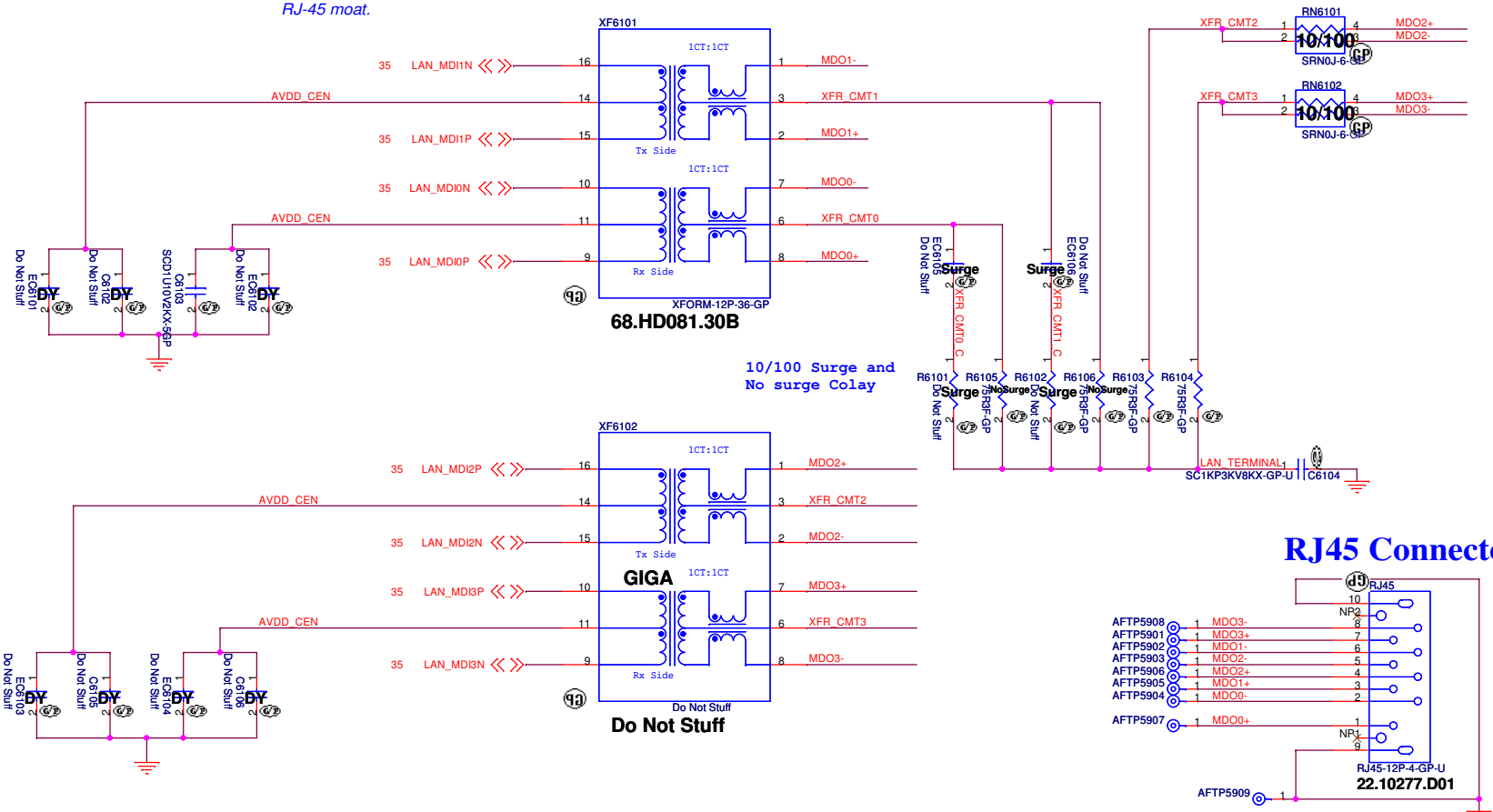
Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 60 of 99

2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
Change MDI1-(XF601.15) to MDI1-(XF601.16)
Change MDI0+(XF601.10) to MDI0+(XF601.9)
Change MDI0-(XF601.9) to MDI0-(XF601.10)
Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
Change RJ45-2(XF601.8) to RJ45-2(XF601.7)

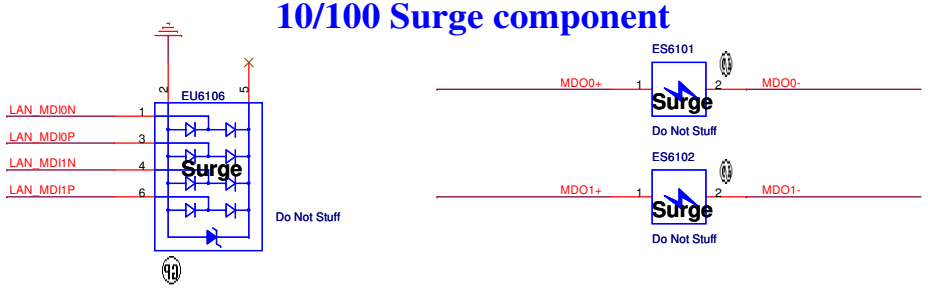
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector

10/100 Surge component



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

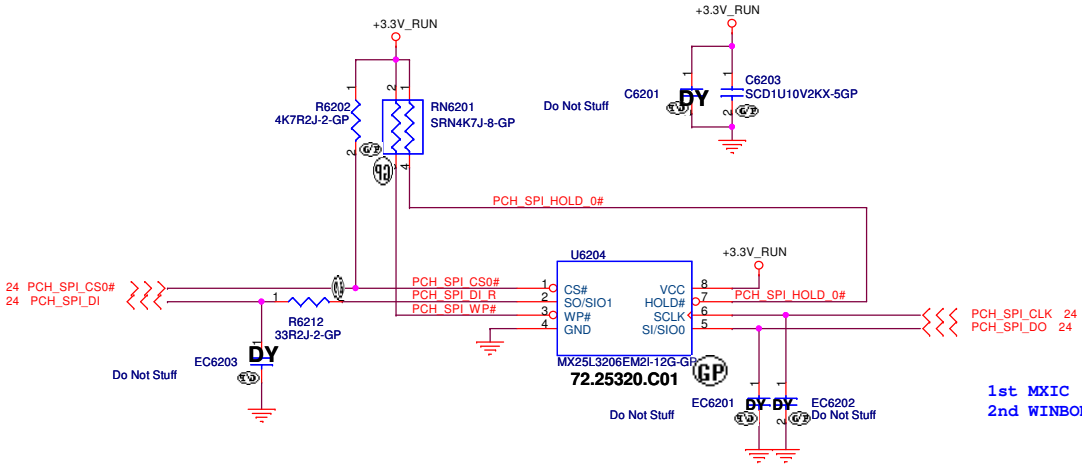
Title: LAN Conn

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 61 of 99

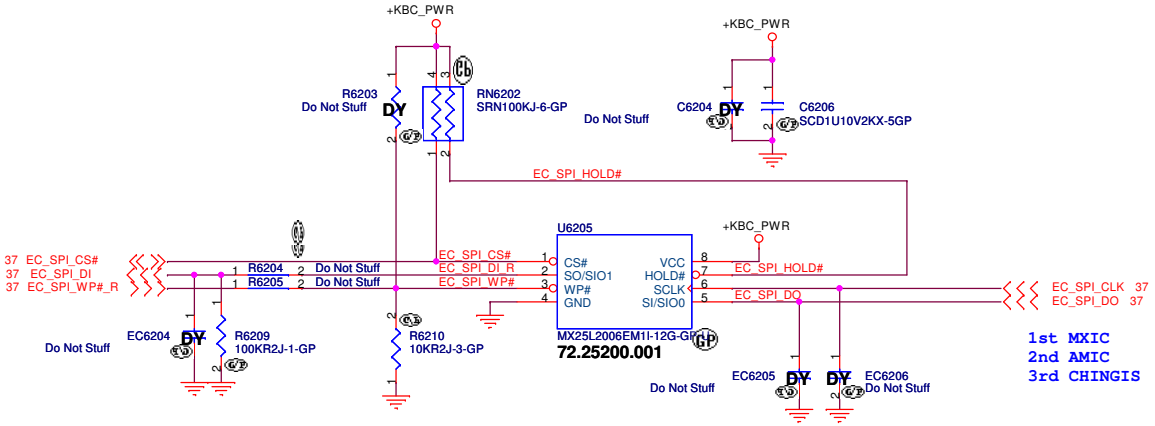
SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH



1st MXIC : 72.25320.C01
2nd WINBOND : 72.25Q32.A01

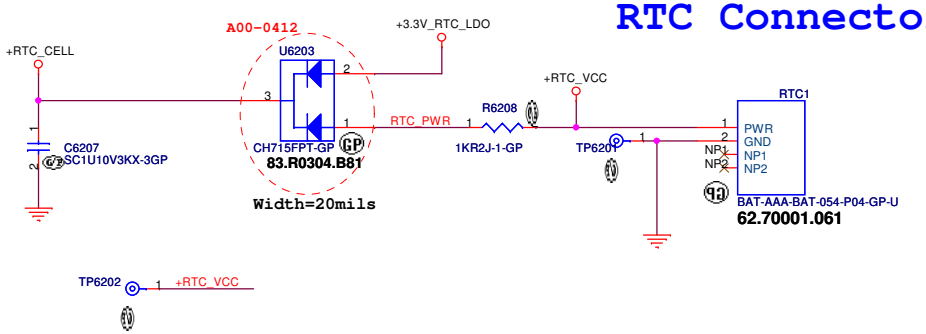
SPI FLASH ROM (2M bits) for KBC

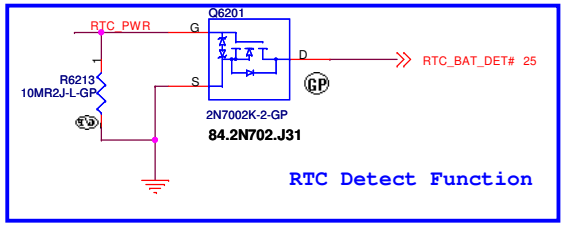


1st MXIC : 72.25200.001
2nd AMIC : 72.25020.00D
3rd CHINGIS : 72.25020.E01

SSID = RBATT

RTC Connector





DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

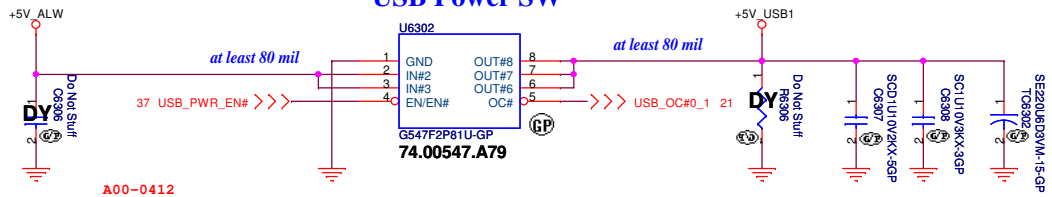
Title: Flash/RTC

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

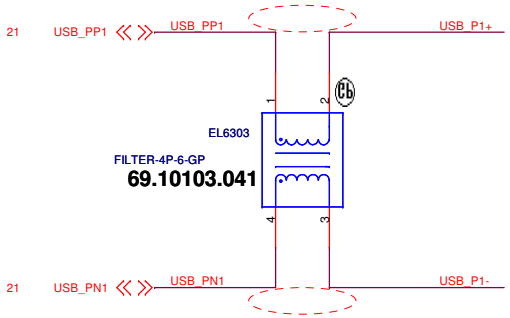
Date: Wednesday, April 13, 2011 Sheet 62 of 99

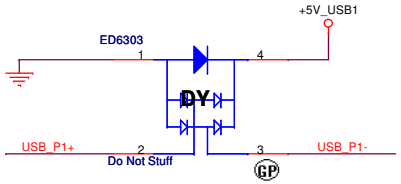
SSID = USB

USB Power SW

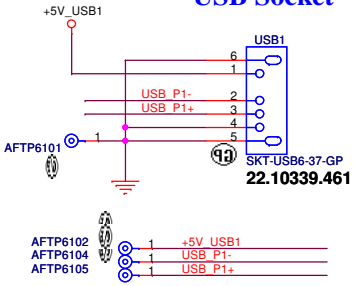


A00-0412
Remove Colay pad after A00

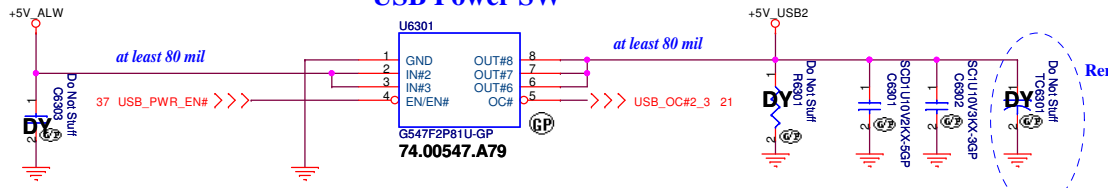




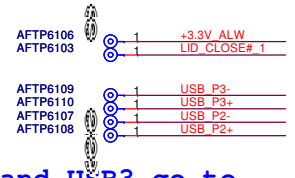
USB Socket



USB Power SW



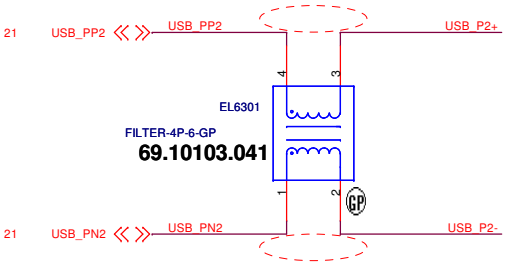
Remove MB cap to DB for droop

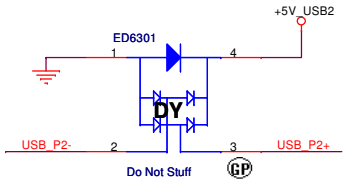


Hall switch, USB2 and USB3 go to daughter board through FFC

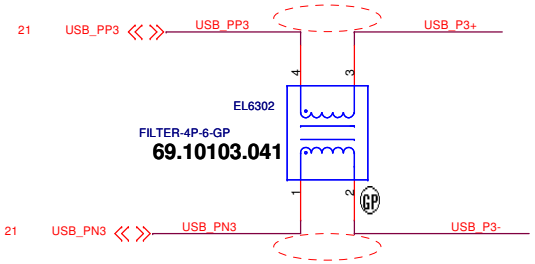
Pitch = 0.5mm

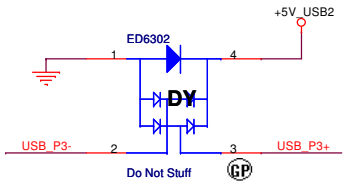
A00-0412
Remove Colay pad after A00

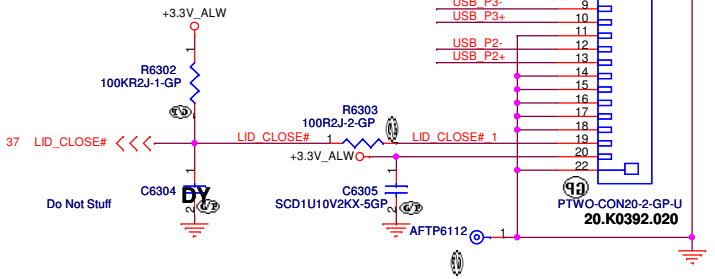




A00-0412
Remove Colay pad after A00





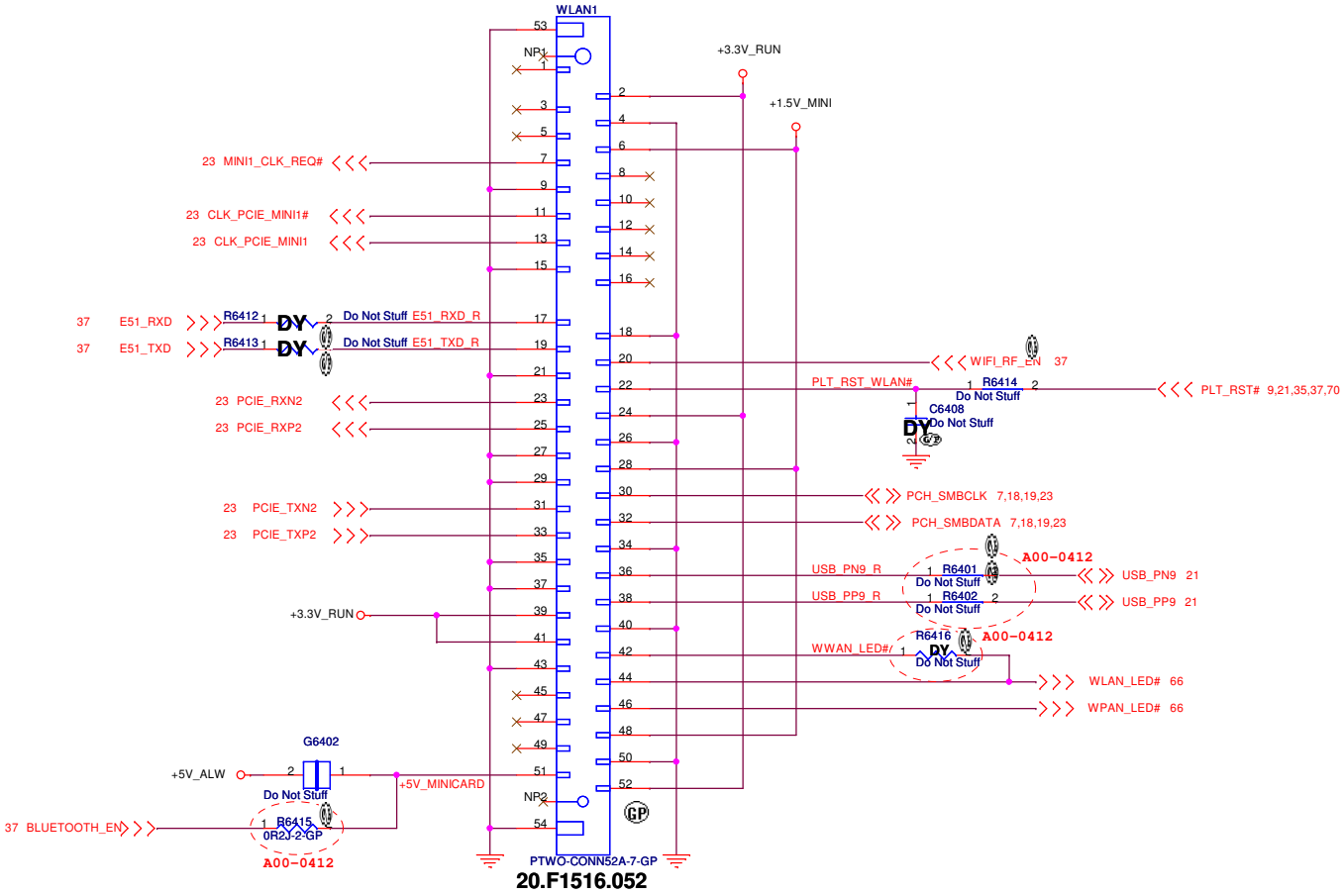


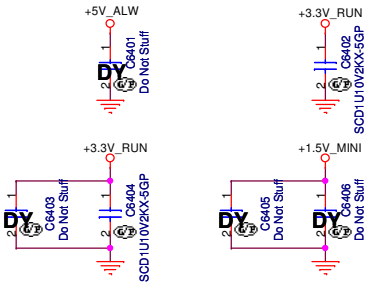
DV15 CP UMA second

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB		
Size	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 63 of 99	

SSID = Wireless

Mini Card Connector(802.11a/b/g)





DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD		
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 64 of 99	

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

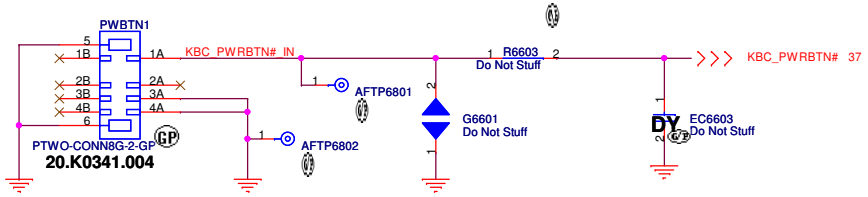
Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 65 of 99

SSID = User.Interface

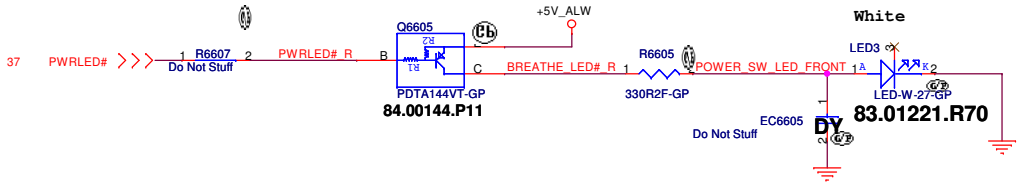
Power BTN Connector



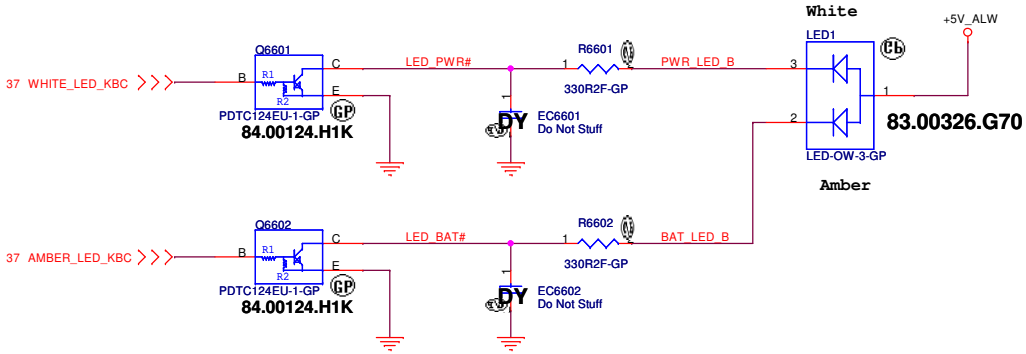
LED Location from left to right
(MB, Top View)

LED3	LED2	LED1	LED4
PWR	HDD	Battery	WLAN

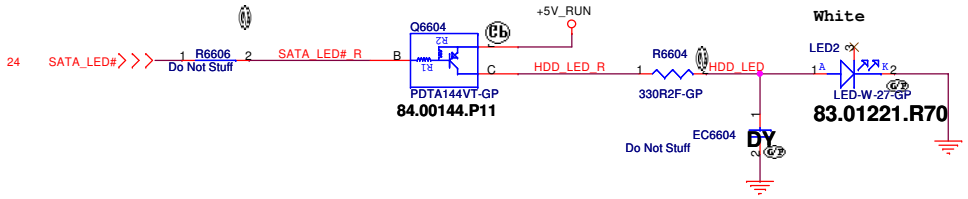
POWER LED



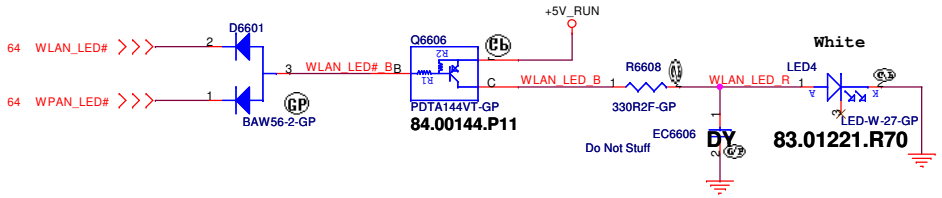
Battery LED



HDD LED



WLAN LED



DV15 CP UMA second

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Title		
LED		
Size: A3	Document Number: Enrico/Caruso 15 CP	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 66 of 99	

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DV15 CP UMA second

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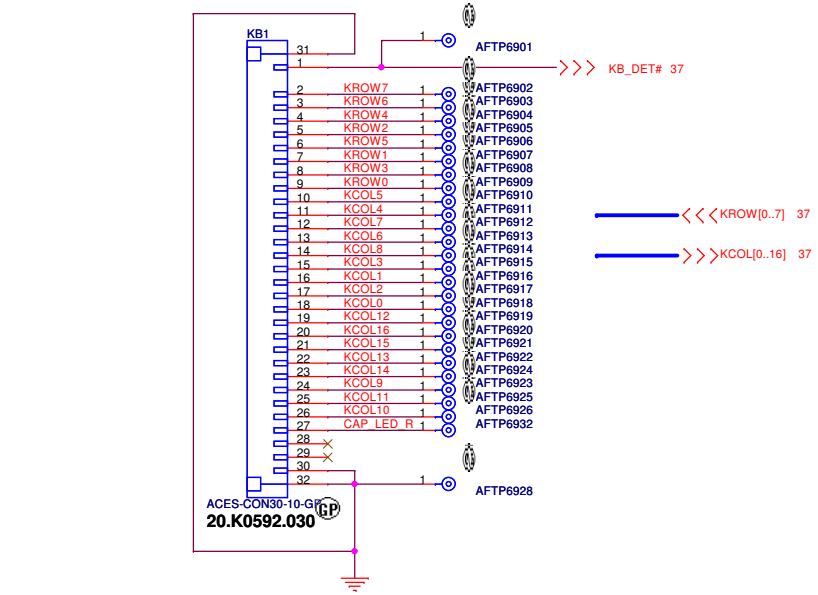
Title: *Reserved*

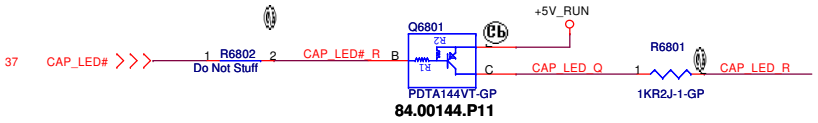
Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 67 of 99

SSID = KBC

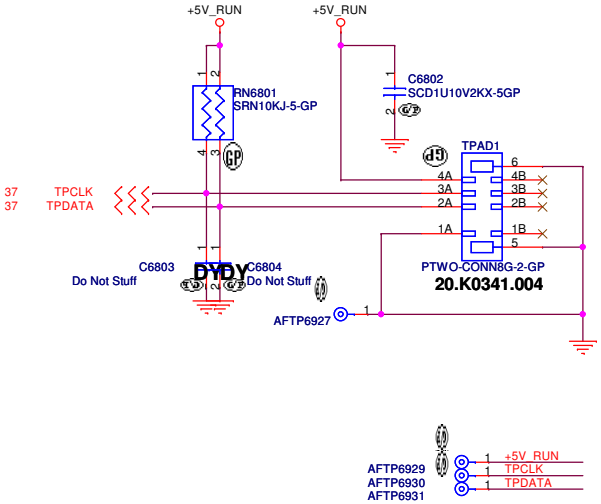
Internal KeyBoard Connector





SSID = Touch.Pad

TouchPad Connector



DV15 CP UMA second

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Title: Key Board/Touch Pad

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 68 of 99

DV15 CP UMA second

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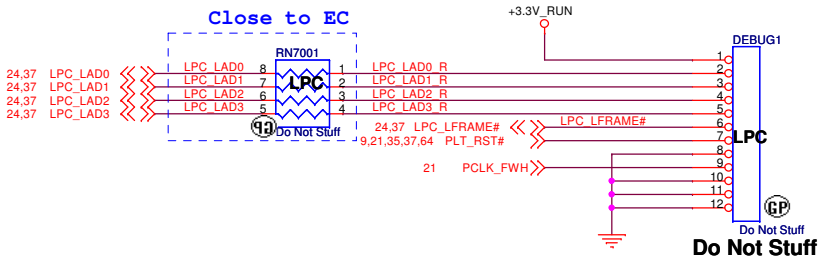
Title

Hall Sensor

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 69 of 99



DV15 CP UMA second

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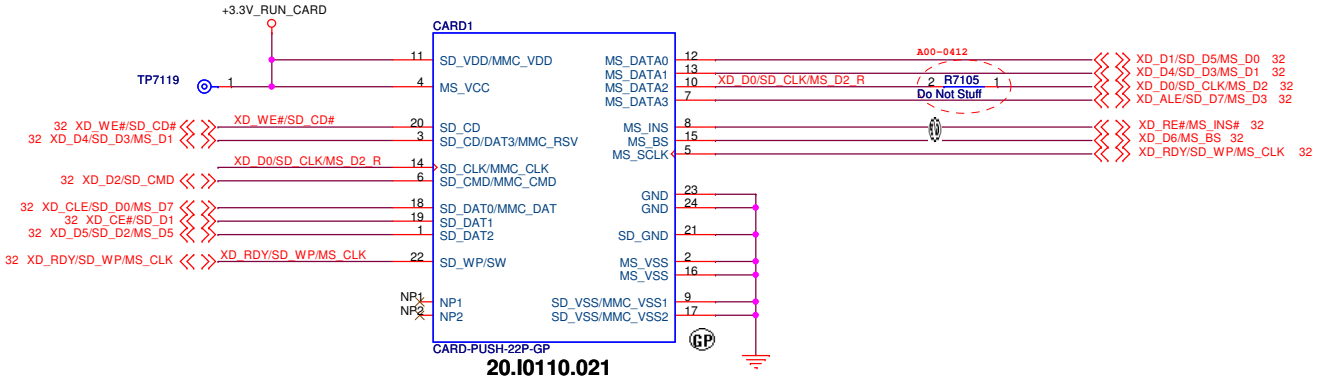
Title: ***Reserved***

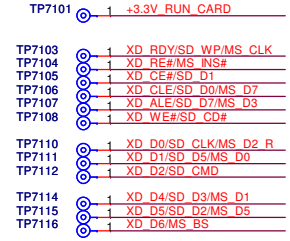
Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

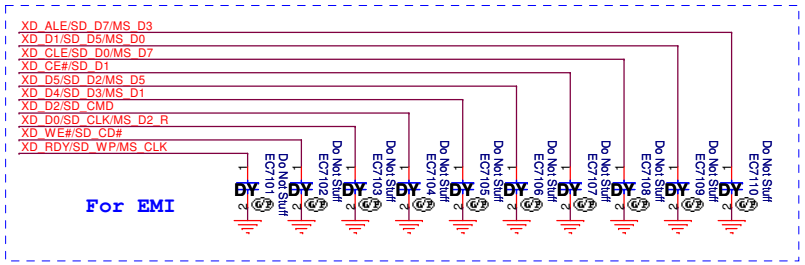
Date: Wednesday, April 13, 2011 Sheet 70 of 99

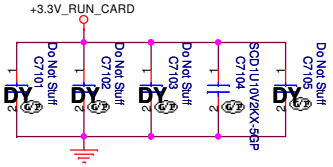
SSID = SDIO

SD/XD/MS Card Reader









DV15 CP UMA second

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Title: CARD Reader Connector

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Wednesday, April 13, 2011 Sheet 71 of 99

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Title: RESERVED

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 08, 2011 | Sheet 72 of 99

DV15 CP UMA second

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Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 73 of 99

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DV15 CP UMA second

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Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 74 of 99

(Blanking)

DV15 CP UMA second

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 75 of 99

DV15 CP UMA second

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Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 76 of 99

(Blanking)

DV15 CP UMA second

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 77 of 99

(Blanking)

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 78 of 99

SSID = Mechanical

H1
Do Not Stuff

H2
Do Not Stuff

H3
Do Not Stuff

H4
Do Not Stuff

H5
Do Not Stuff

H6
Do Not Stuff

H7
Do Not Stuff

H8
Do Not Stuff

H9
Do Not Stuff

HMI1
STF256R117H119-GP
34.4B502.001

HTH1
Do Not Stuff

SPR1
SPRING-58-GP
34.4B312.002

SPR2
SPRING-58-GP
34.4B312.002

H10
Do Not Stuff

H11
Do Not Stuff

H12
Do Not Stuff

H15
Do Not Stuff

+DC_IN_SS
SCD1U25V2ZY-1GP
EC7901

+3.3V_RUN
Do Not Stuff
EC7902

+3.3V_RUN
Do Not Stuff
EC7903

+3.3V_RUN
Do Not Stuff
EC7904

+5V_RUN
SCD1U25V2ZY-1GP
EC7905

+5V_RUN
Do Not Stuff
EC7906

+5V_RUN
Do Not Stuff
EC7907

+5V_RUN
Do Not Stuff
EC7908

+3.3V_ALW
Do Not Stuff
EC7909

+5V_ALW
Do Not Stuff
EC7910

+PWR_SRC
SCD1U25V2ZY-1GP
EC7911

+PWR_SRC
Do Not Stuff
EC7912

+PWR_SRC
SCD1U25V2ZY-1GP
EC7913

+PWR_SRC
SCD1U25V2ZY-1GP
EC7914

+PWR_SRC
Do Not Stuff
EC7915

+PWR_SRC
SCD1U25V2ZY-1GP
EC7916

+PWR_SRC
Do Not Stuff
EC7917

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7918

+1.5V_SUS
SC100P50V2JN-3GP
EC7919

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7920

+1.5V_SUS
SC100P50V2JN-3GP
EC7921

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7922

+1.5V_SUS
SC100P50V2JN-3GP
EC7923

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7924

+1.5V_SUS
SC100P50V2JN-3GP
EC7925

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7926

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7927

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7928

+1.5V_SUS
SC1000P50V3JN-GP-U
EC7929

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 08, 2011 | Sheet 79 of 99

SSID = VIDEO

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 80 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
C	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 81 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A2	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 82 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
C	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 83 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
Custom	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 84 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
Custom	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 85 of 99

DV15 CP UMA second

Wistron Corporation
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Title

Reserved

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 86 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 87 of 99

DV15 CP UMA second

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Title: *Reserved*

Size	Document Number	Rev
C	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 88 of 99

DV15 CP UMA second

Wistron Corporation
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Title

Reserved

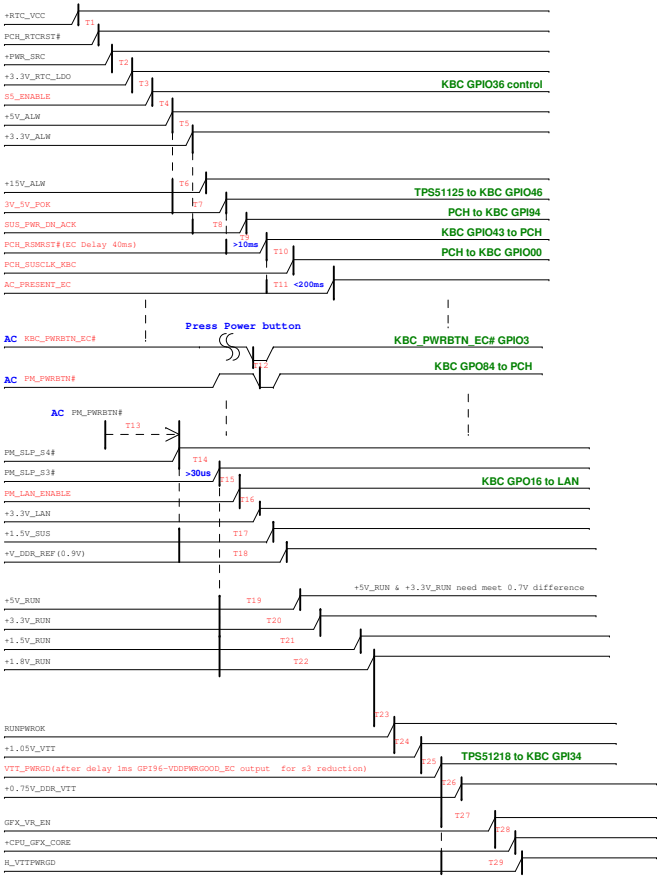
Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

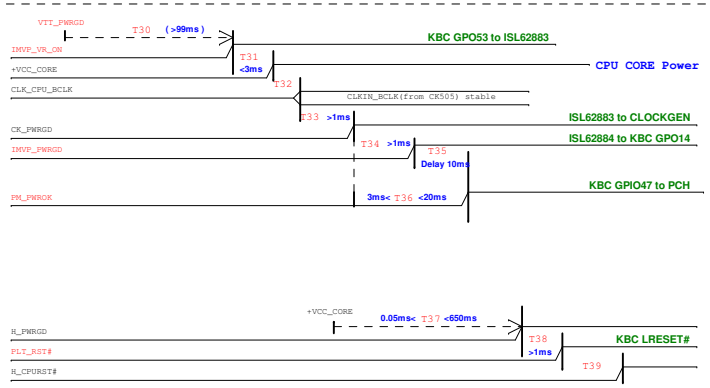
Date: Friday, April 08, 2011 Sheet 89 of 99

DV15 Calpella UMA-Power Up Sequence

(AC mode)

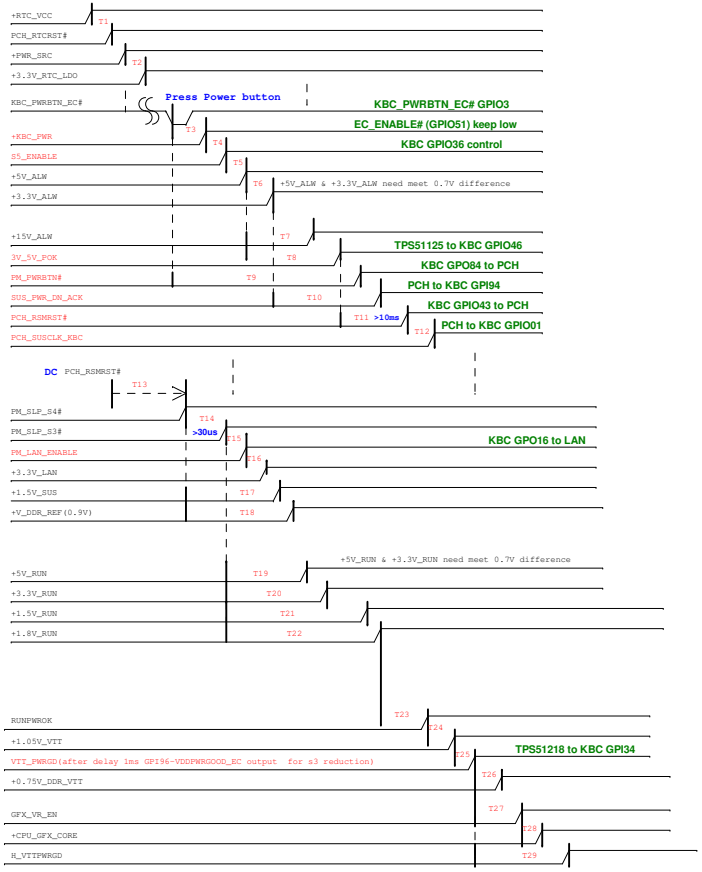
red word: KBC GPIO

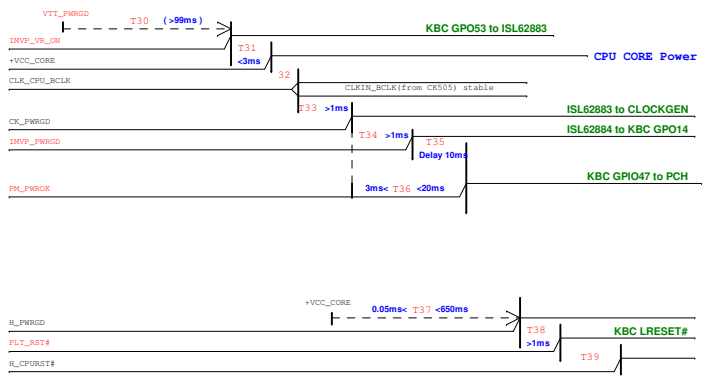




(DC mode)

red word: KBC GPIO





DV15 CP UMA second

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
A1	Enrico/Caruso 15 CP	A00

Date: Friday, April 09, 2010 Sheet 30 of 39

Item	Pg.	Date	Description	Owner
KBC	37	A00-0412	stuff R3722 and DY R3725 for change MB version from X02 to A00	EE
WLAN	64	A00-0412	change R6415 from short pad to 0 ohm for debug	EE
USB	54,63	A00-0412	Remove colay pad(R5403,R5404,R6315,R6316,R6317,R6318,R6319, R6320) after A00	EMI
USB	32,64	A00-0412	Remove colay pad(EL3201,EL6401) and short pad(R3204,R3205, R6401,R6402) after A00	EMI
CLK GEN	7	A00-0412	change R710~R717 from 0 ohm to short pad	EMI
HDMI	57	A00-0412	Remove colay pad(EL5701,EL5702,EL5703,EL5704) after A00	EMI
short pad	ALL	A00-0412	change PR4519,PR5006,PR5111,R3202,R3742,R3743,R3744,R7105 from 0 ohm to short pad	EE
RTC	62	A00-0412	change U6203 P/N to 83.R0304.B81 for RTC detect leakage issue	EE
RT8237A_+1.05V	49	A00-0412	update PU4901 symbol for part manager footprint change	POWER
WLAN	64	A00-0412	add and DY R6416 0 ohm for Wimax future	EE
POWER GAP	ALL	A00-0413	change power GAP(PG4511,PG4602,PG4604,PG4605,PG4606,PG4615, PG4617,PG4619,PG4621,PG4624,PG4625,PG4607,PG4608,PG4609, PG4622,PG4626,PG4627,PG4610,PG4611,PG4612,PG4613,PG4614, PG4616,PG4618,PG4620,PG4902,PG4903,PG4904,PG4905,PG4906, PG4908,PG4910,PG4911,PG4913,PG4915,PG4917,PG4919,PG4925, PG4926,PG4920,PG4927,PG4928,PG4929,PG4909,PG4901,PG4912, PG4914,PG4916,PG4918,PG5001,PG5012,PG5002,PG5003,PG5004, PG5008,PG5009,PG5010,PG5011,PG5013,PG5015,PG5016,PG5017, PG5104,PG5106,PG5301,PG5303,PG5305,PG5308,PG5311) P/N from ZZ.CON2d.XXX to ZZ.CLOSE.001 for PSE requests	POWER
Thermal	39	A00-0422	stuff R3904 to change T8 temperature setting for reliability test	EE

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: Enrico/Caruso 15 CP | Rev: A00

Date: Friday, April 22, 2011 | Sheet 91 of 99

Item	Pg.	Date	Description	Owner

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 92 of 99

Item	Pg.	Date	Description	Owner

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: A3 | Document Number: *Enrico/Caruso 15 CP* | Rev: *A00*

Date: Friday, April 08, 2011 | Sheet 93 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 94 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 95 of 99

DV15 CP UMA second

Wistron Corporation
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Title

Change History

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 96 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 97 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Change History

Size	Document Number	Rev
A3	*Enrico/Caruso 15 CP*	*A00*

Date: Friday, April 08, 2011 Sheet 98 of 99

DV15 CP UMA second

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Change History

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00

Date: Friday, April 08, 2011 Sheet 99 of 99