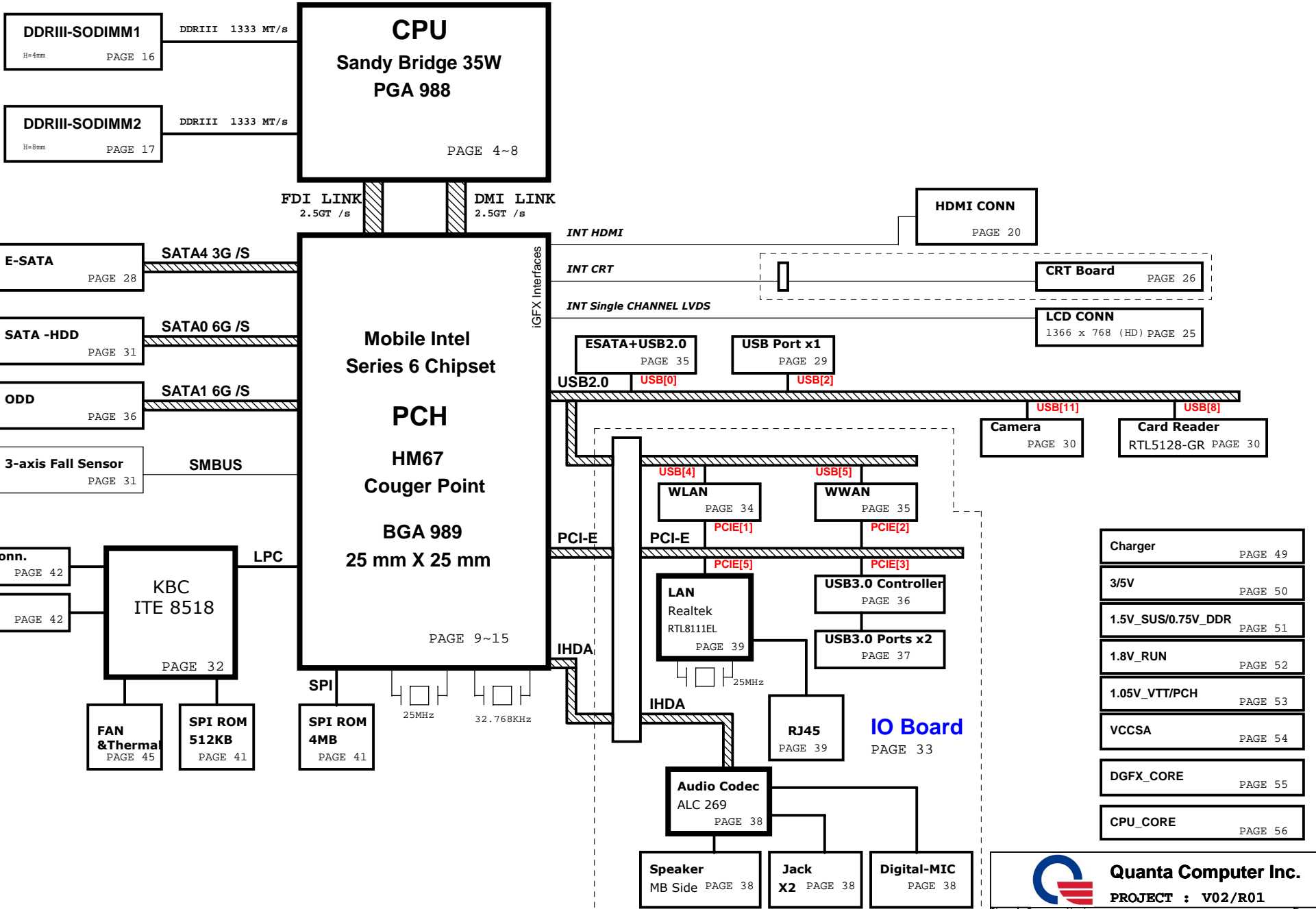


V02/R01 UMA BLOCK DIAGRAM

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



Quanta Computer Inc.
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	BLOCK DIAGRAM	1A
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power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								



Quanta Computer Inc.

PROJECT : V02/R01

5

4

3

2

1

D

D

C


C

B

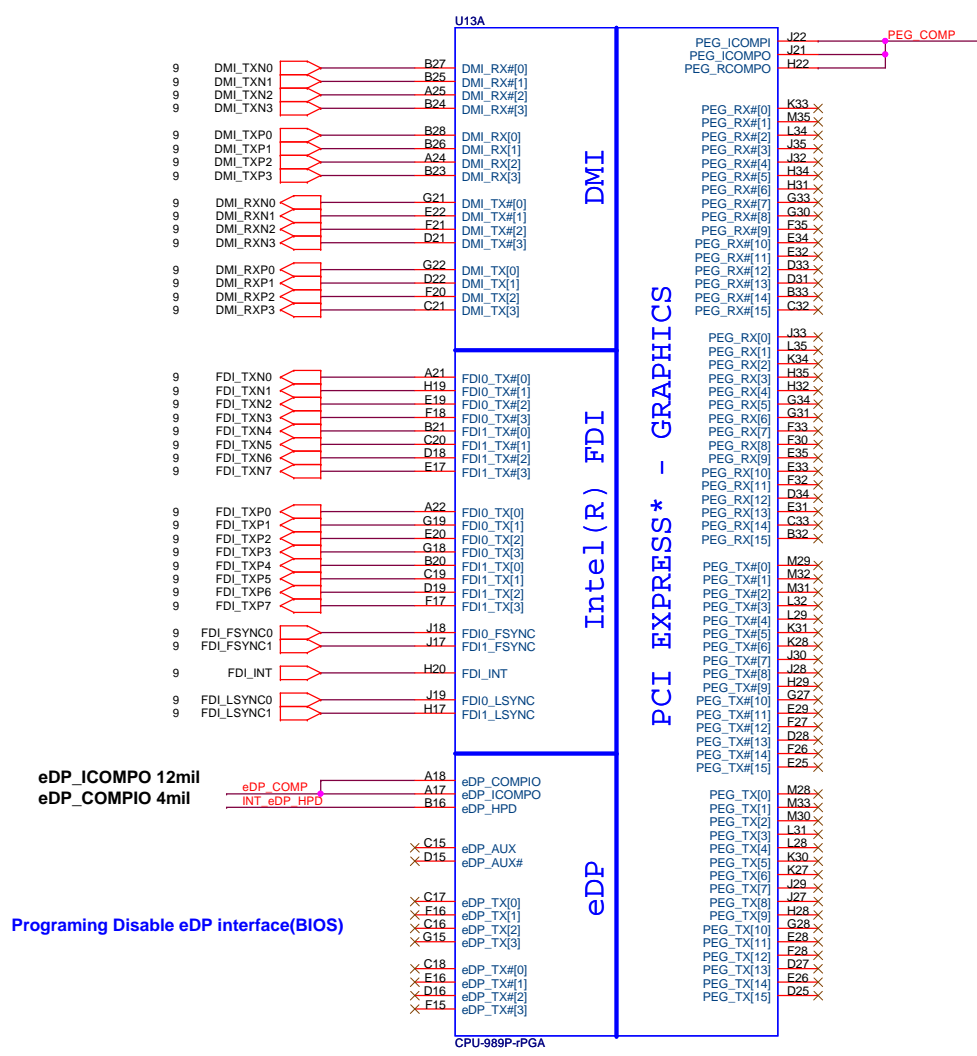
B

A

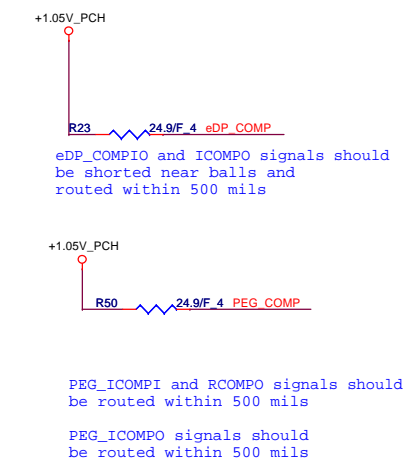
A

		Quanta Computer Inc.
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	BLANK	1A
Date:	Wednesday, January 19, 2011	Sheet 3 of 51

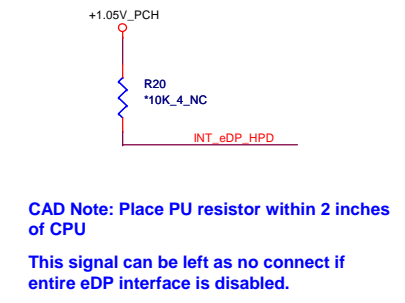
Sandy Bridge Processor (DMI, PEG, FDI)



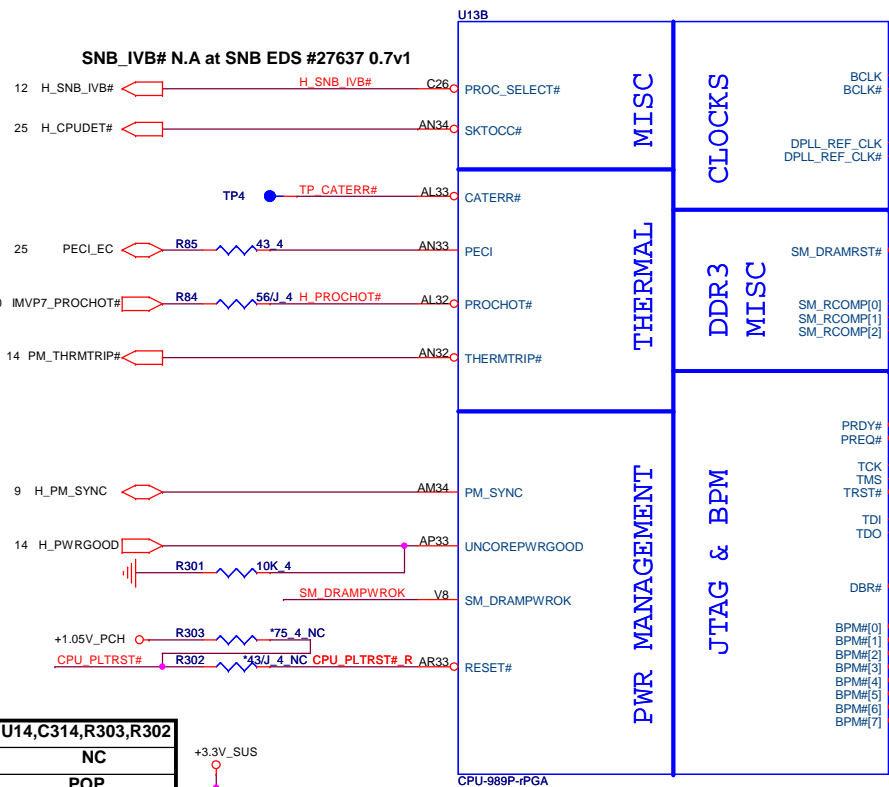
DP & PEG Compensation



eDP Hot-plug (Disable)



Sandy Bridge Processor (CLK,MISC,JTAG)

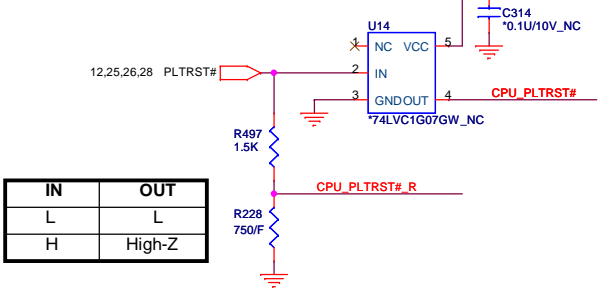


Schematic C/L_v1.0, P56 (PU,PD 1k/J)
 (Intel and PD3)
 Reserve (Intel confirm now)

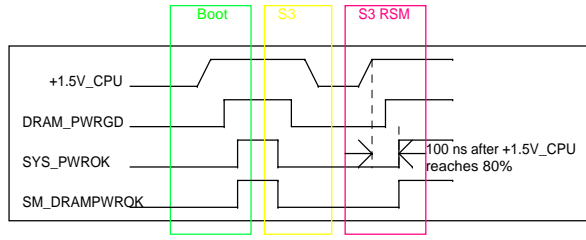
SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

Over 130 degree C will drive low

CPU_PLTRST	R497,R228	U14,C314,R303,R302
Option1	POP	NC
Option2	NC	POP

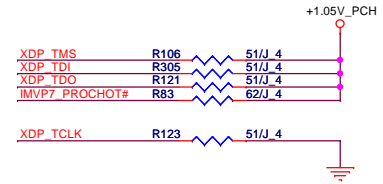


IN	OUT
L	L
H	High-Z



When MP, JTAG PU/PD resistor can be removed?
 Need to confirm with Intel

XDP_DBRST# use a 1k pull-up to 3.3V_S
 TRST# use a 51ohm pull down.

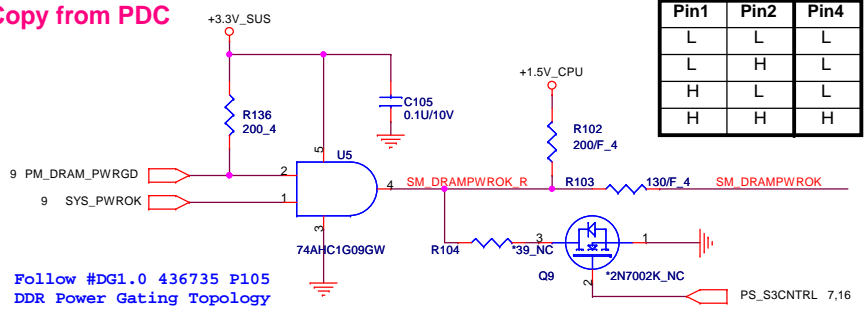


Change OD part same with PDC

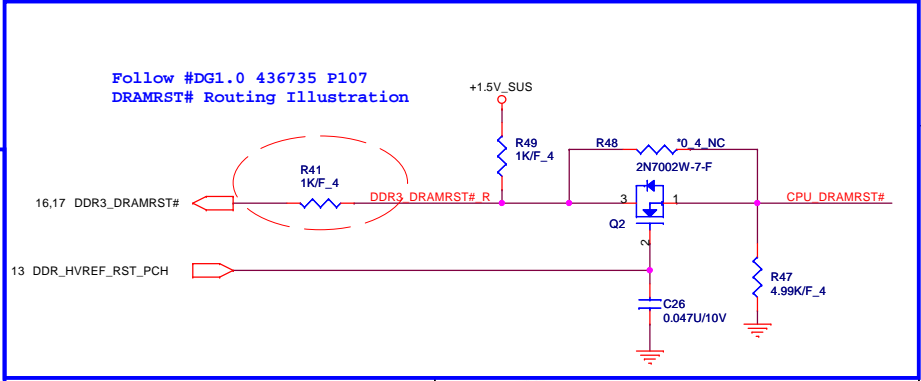
Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H



Follow #DG1.0 436735 P105
 DDR Power Gating Topology

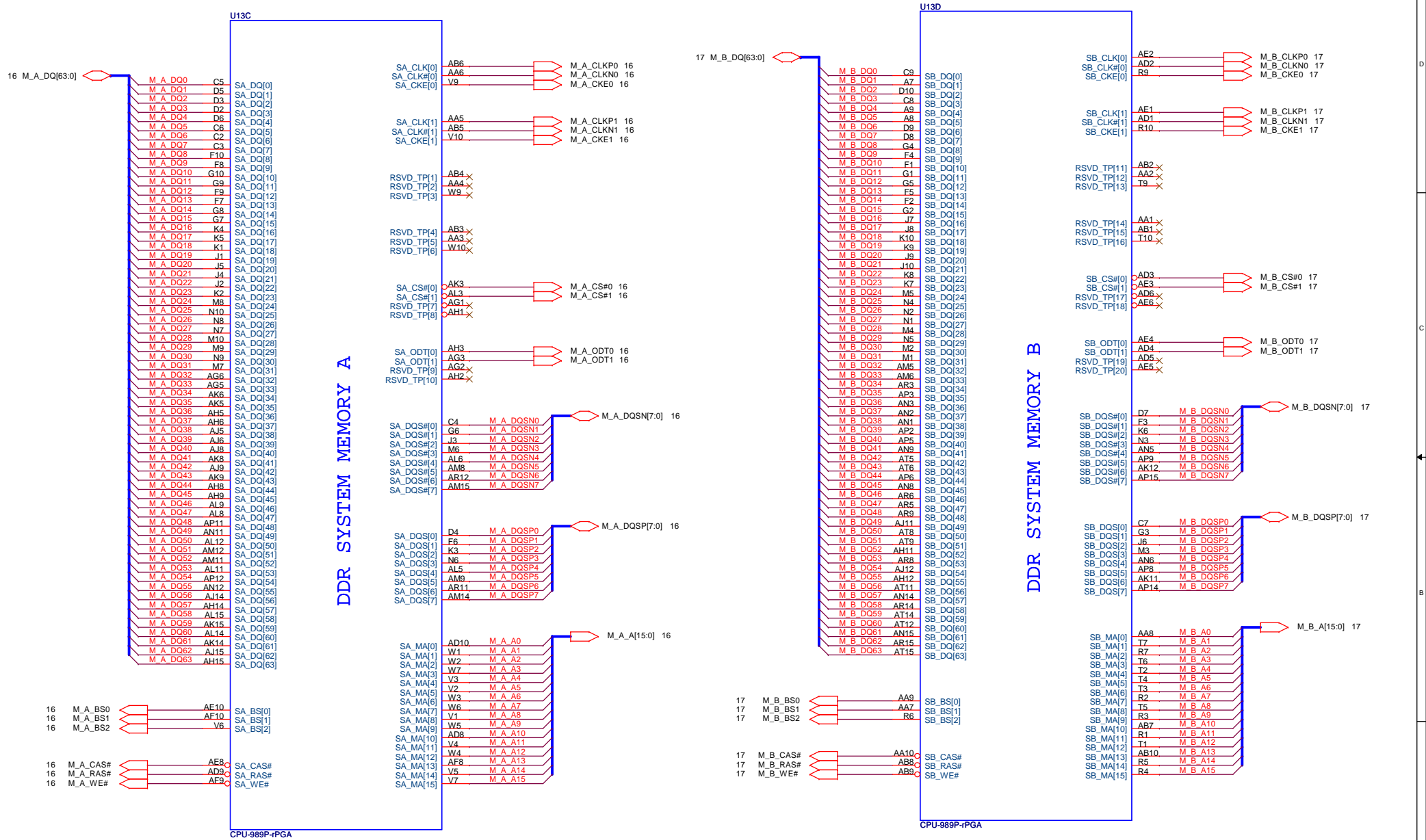


Follow #DG1.0 436735 P107
 DRAMRST# Routing Illustration



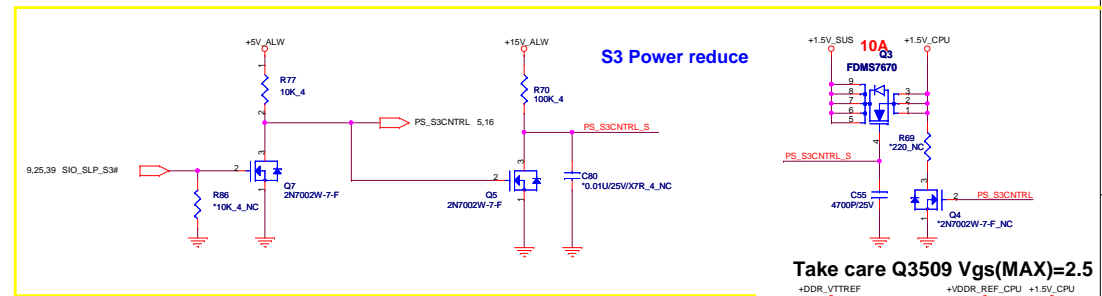
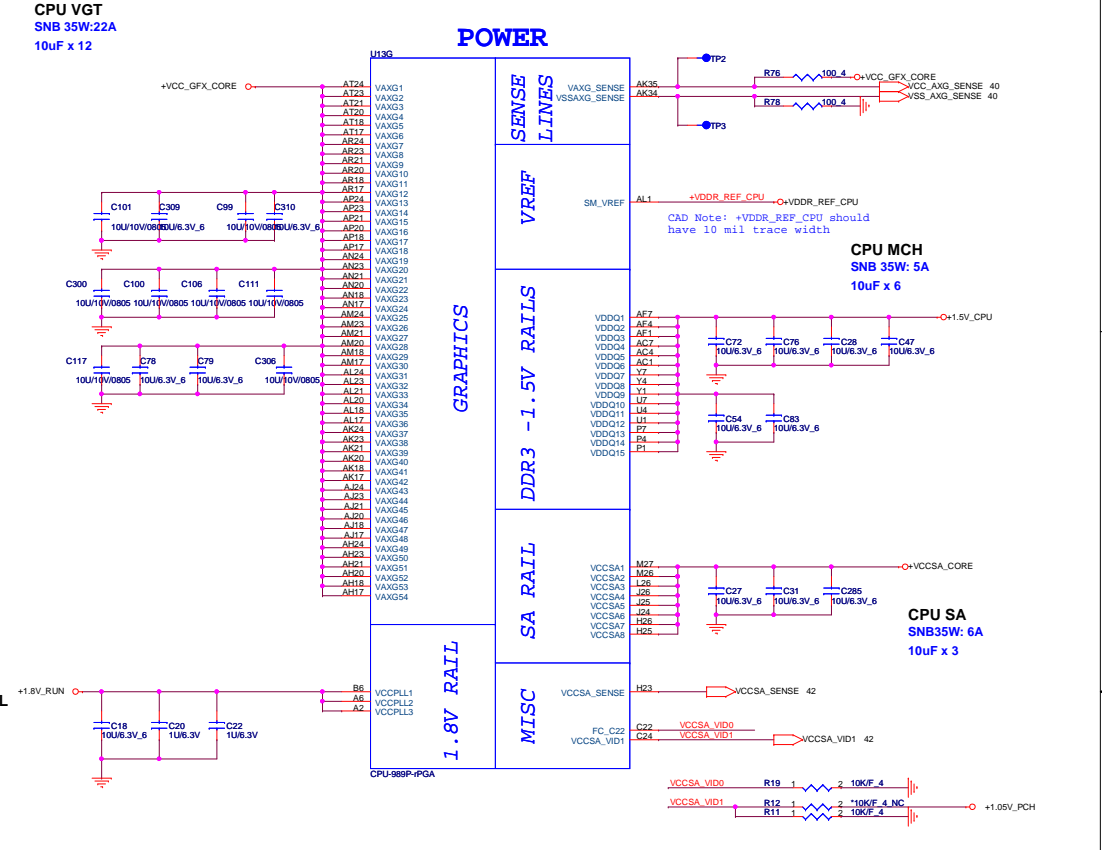
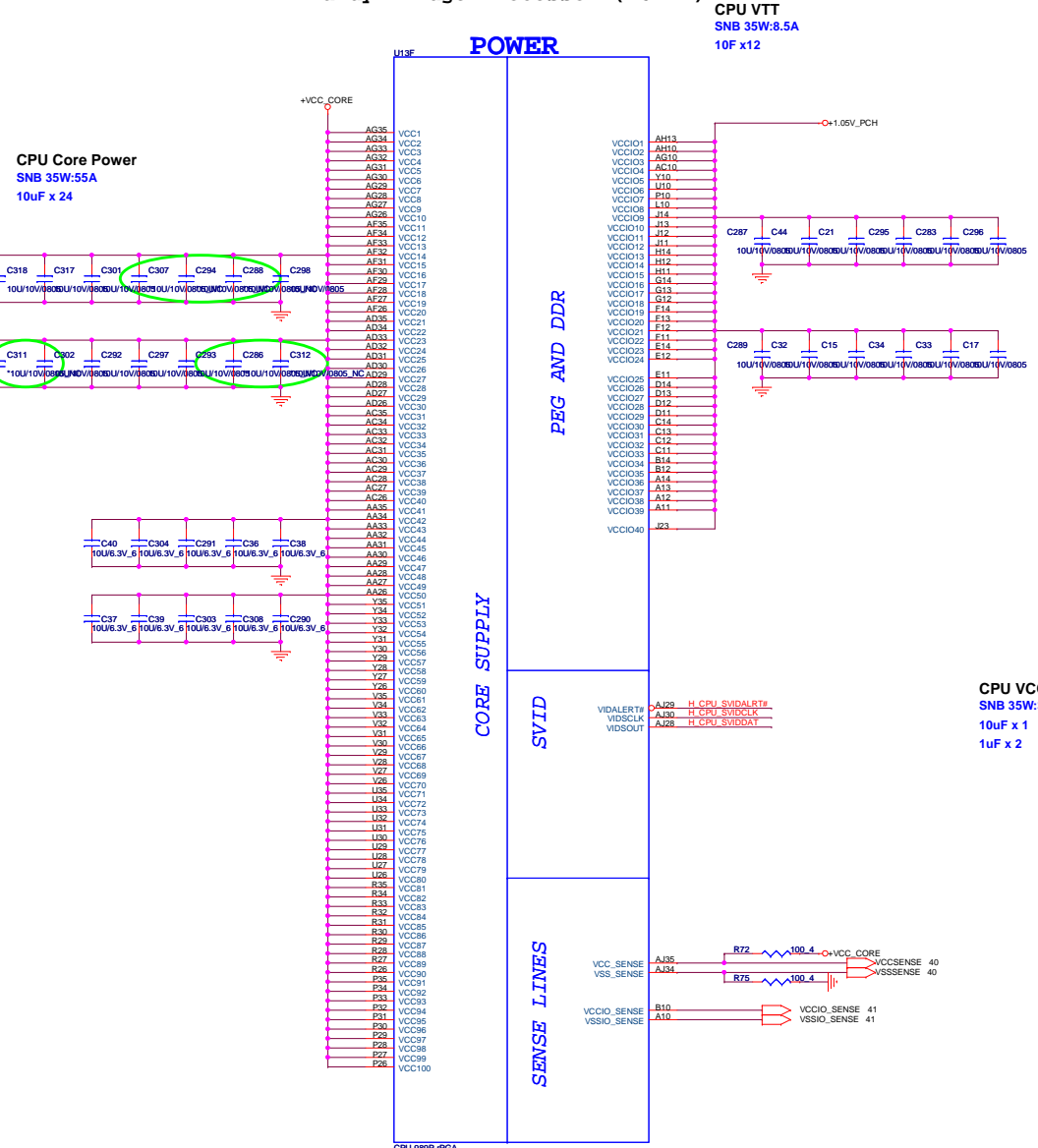
PROJECT : V02/R01

Sandy Bridge Processor (DDR3)

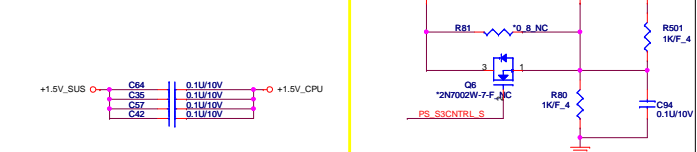
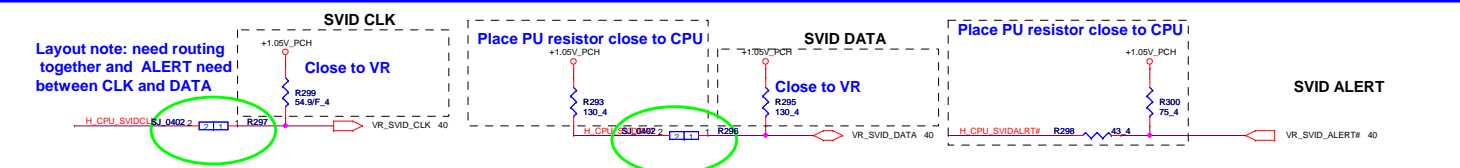


Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

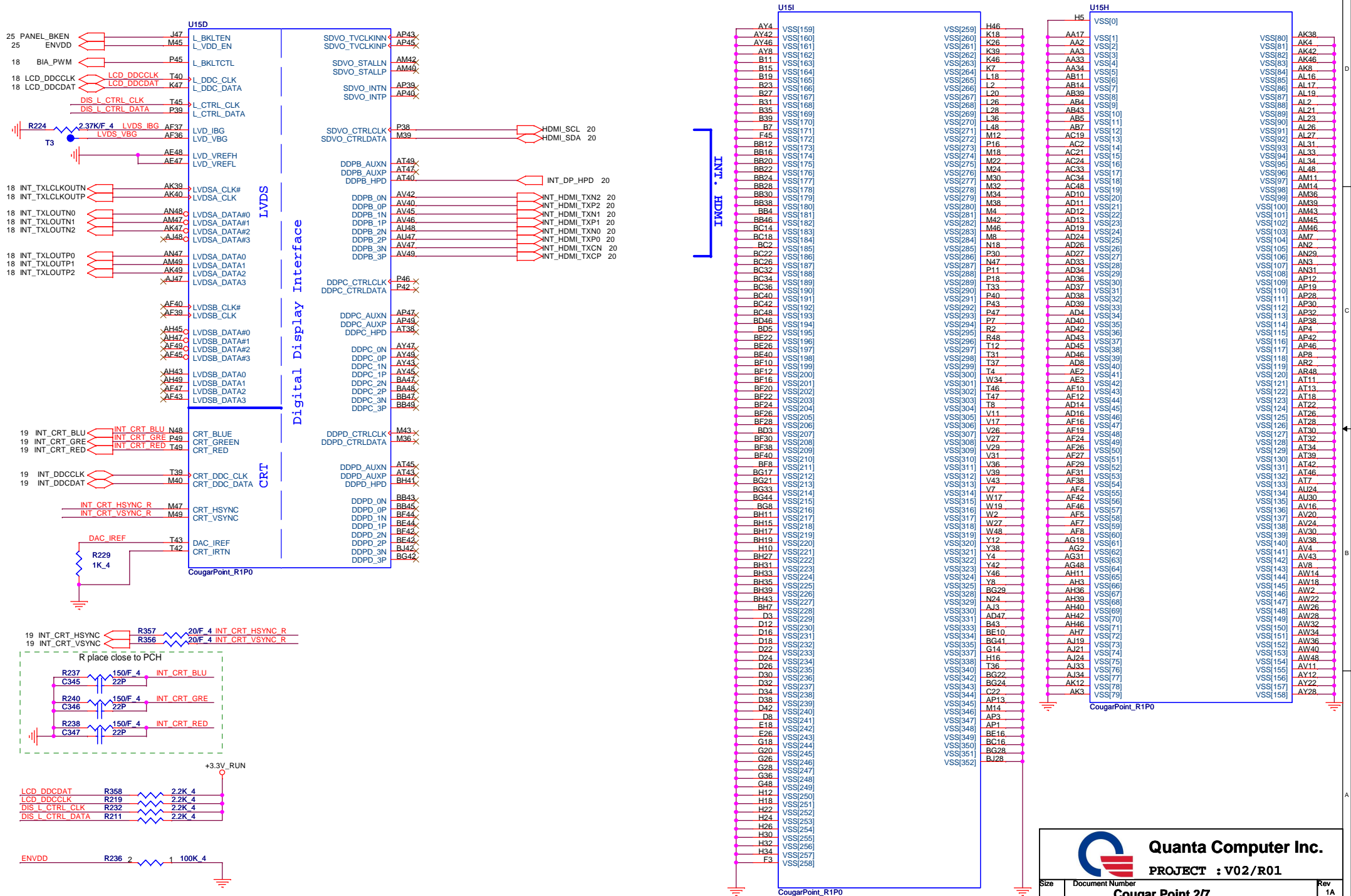


Change R8281, R8285, R8704, R8329 to +/-5%
54.9 ohm has no 5%



Cougar Point (LVDS,DDI)

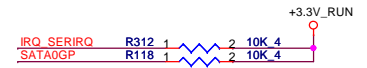
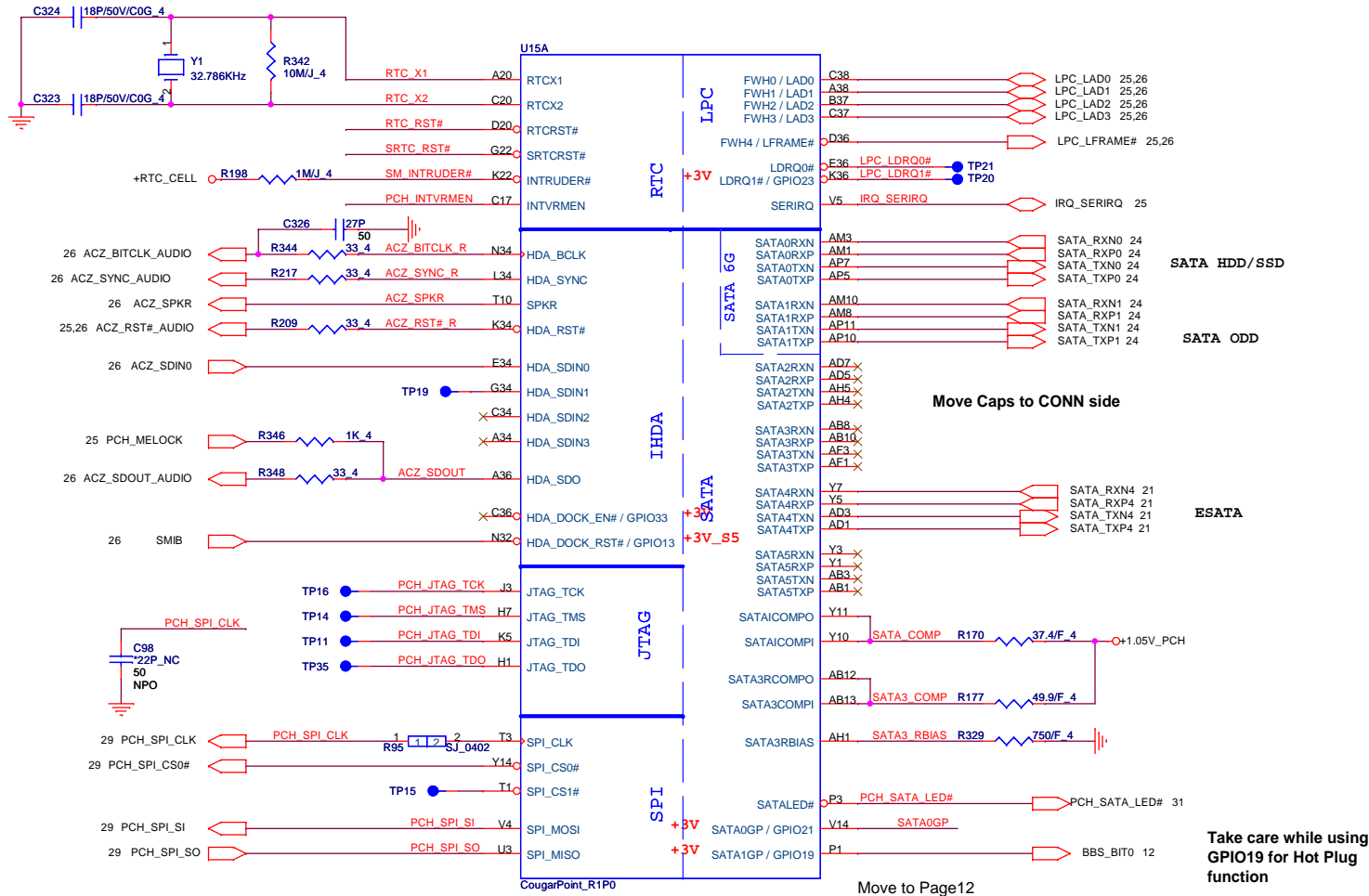
Cougar Point (GND)



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Cougar Point 2/7

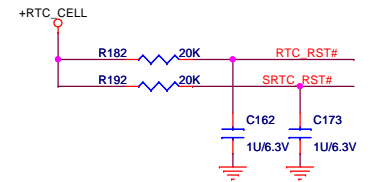
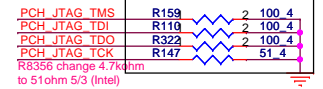
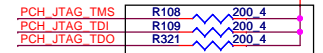
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Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel) +3.3V_SUS



Move Caps to CONN side

Move to Page12

Take care while using GPIO19 for Hot Plug function

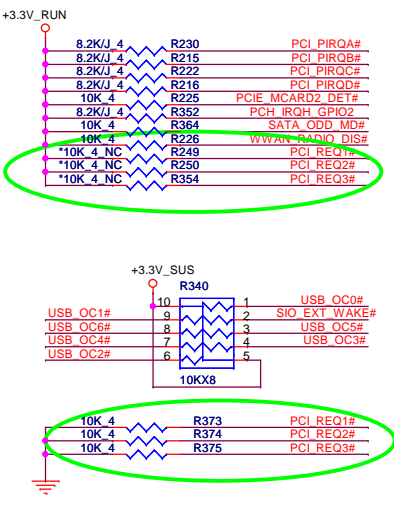
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R146 *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R349 *1K 4 NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R181 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R212 1K 4 ACZ_SYNC_R

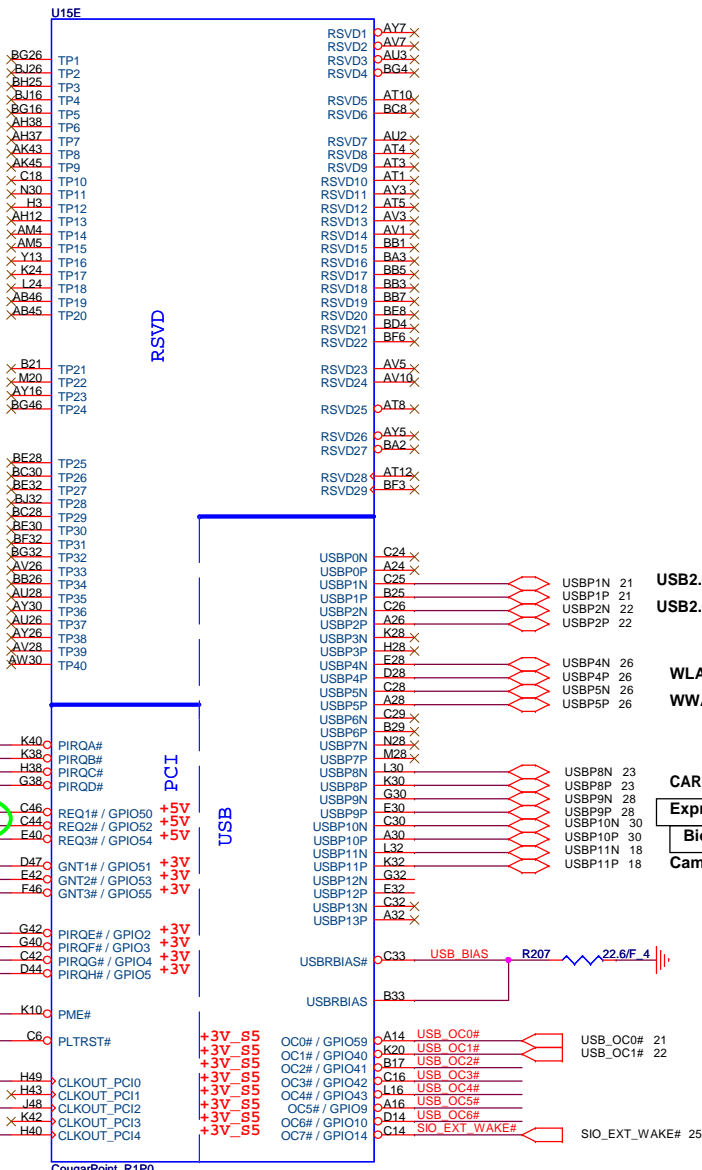
Quanta Computer Inc.
PROJECT : V02/R01

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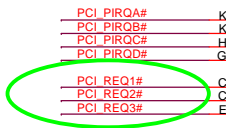
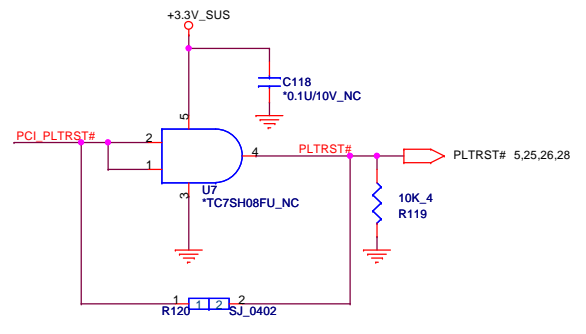
PCI/USB/OC# Pull-up(CLG)



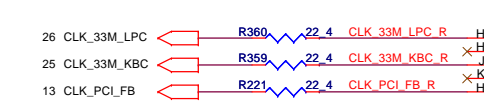
Cougar Point-M (PCI,USB,NVRAM)



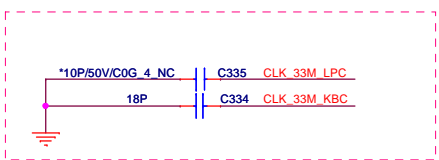
PLTRST#(CLG)



Check with BIOS program or not? (have to be not)



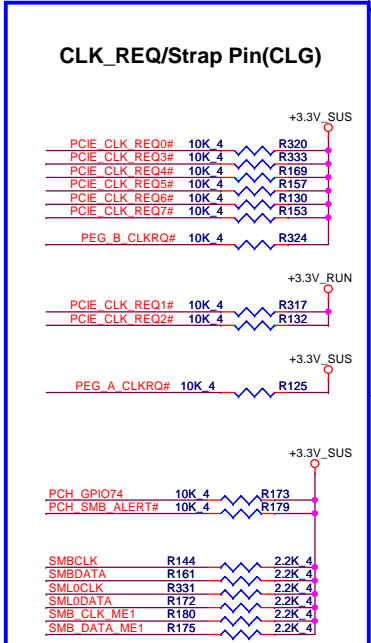
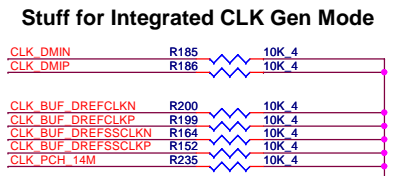
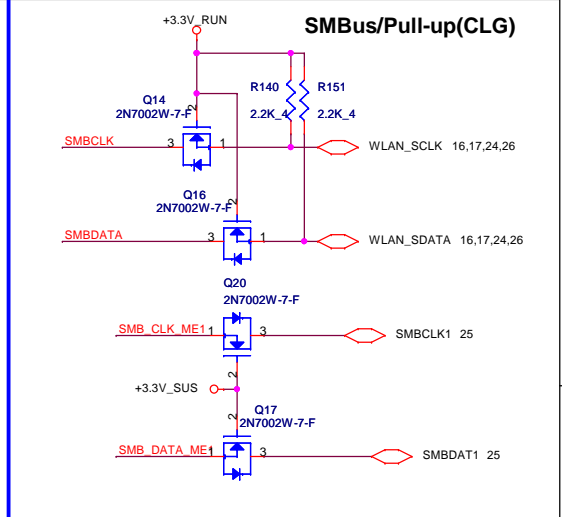
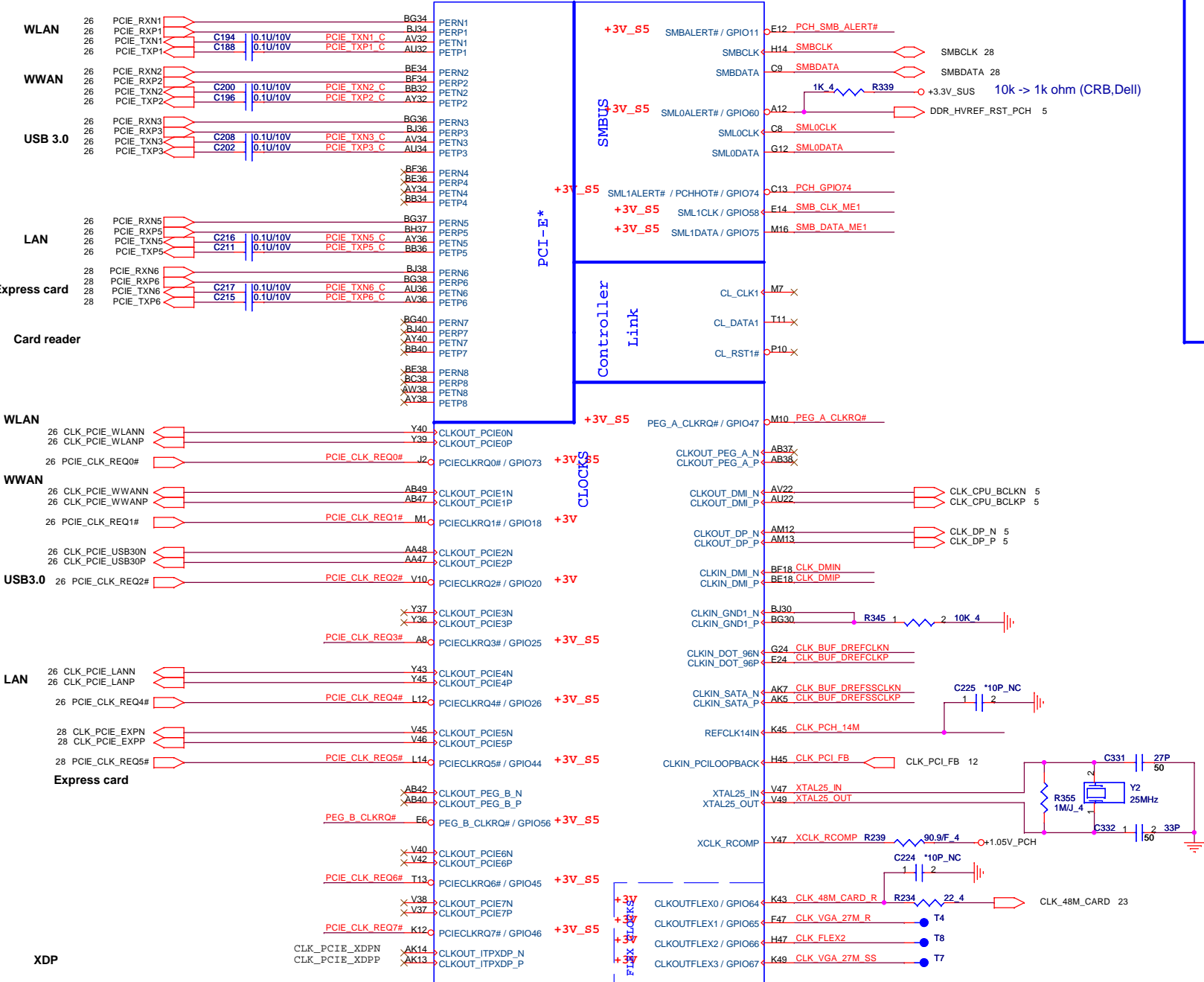
Check CLKOUT if Skew requirement?




Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>Bit 0</th> <th>Bit 1</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
11 BBS_BIT0	R233 *1K_4_NC		Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]									
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
R327	2.2K_4											
R326	1 SJ_0402											

Cougar Point-M (PCI-E, SMBUS, CLK)

U15B



CLKOUTFLEX0 / GPIO64	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: • 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

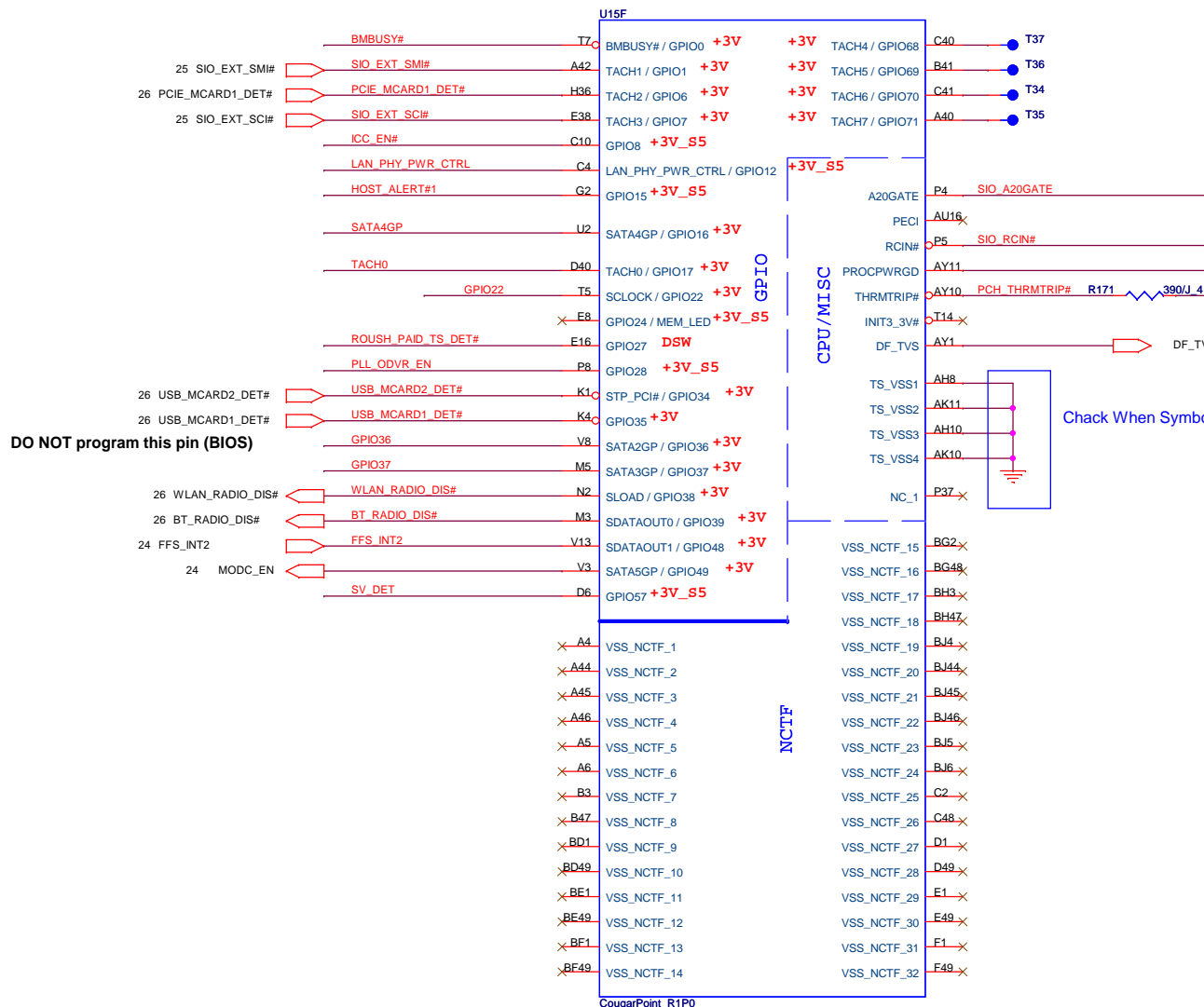


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Cougar Point 5/7

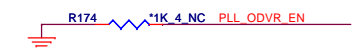
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Cougar Point (GPIO, VSS_NCTF, RSVD)



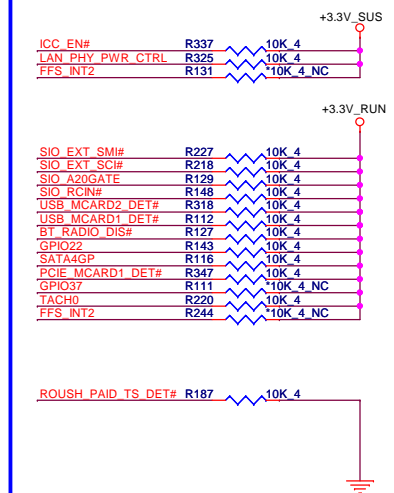
DO NOT program this pin (BIOS)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

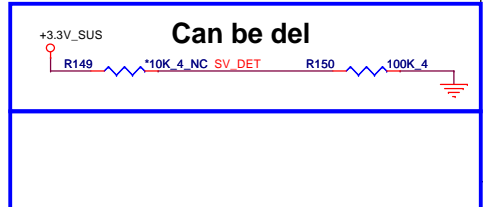


Ask Intel, what's the function?
Add Description in EC GPIO table (keyboard controller reset)

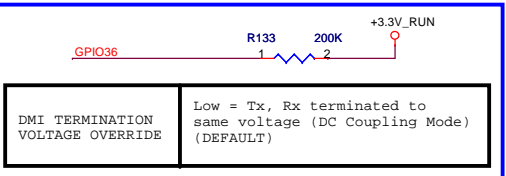
GPIO Pull-up/Pull-down (CLG)



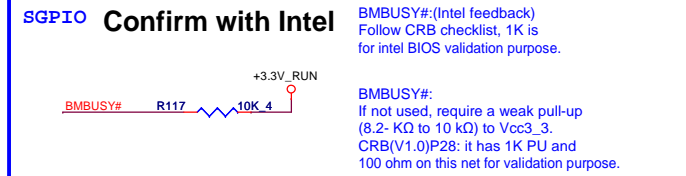
Check When Symbol Update (OK)



Can be del



DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



SGPIO Confirm with Intel
BMBUSY#:(Intel feedback) Follow CRB checklist, 1K is for intel BIOS validation purpose.
BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3. CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

Have to Reserve

HOST_ALERT#1 R323 1K 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

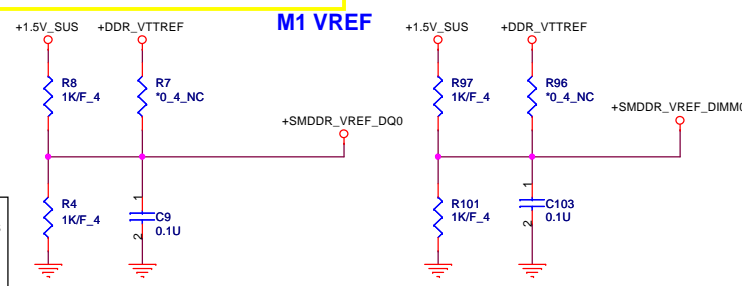
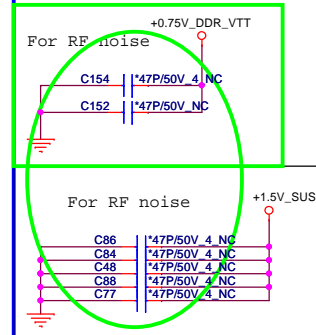
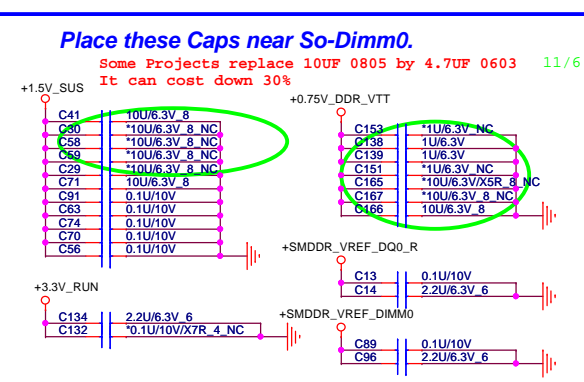
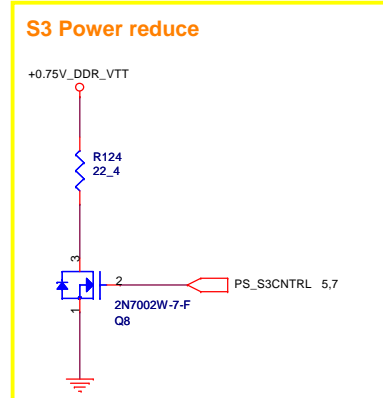
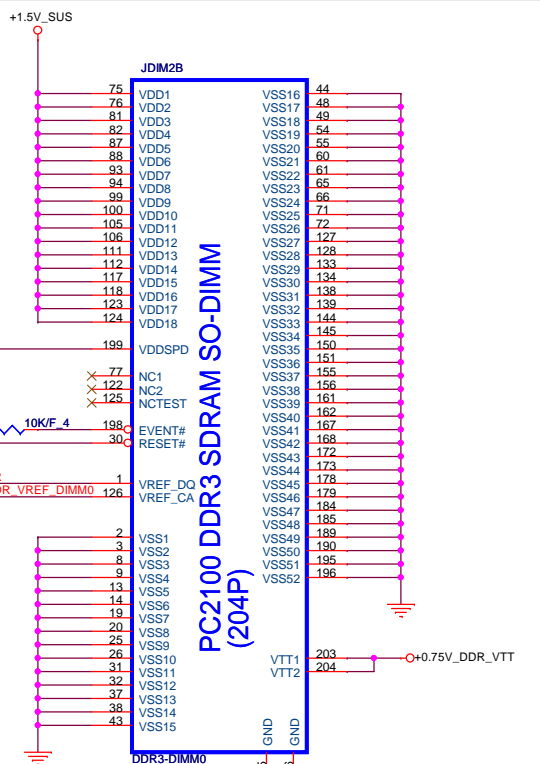
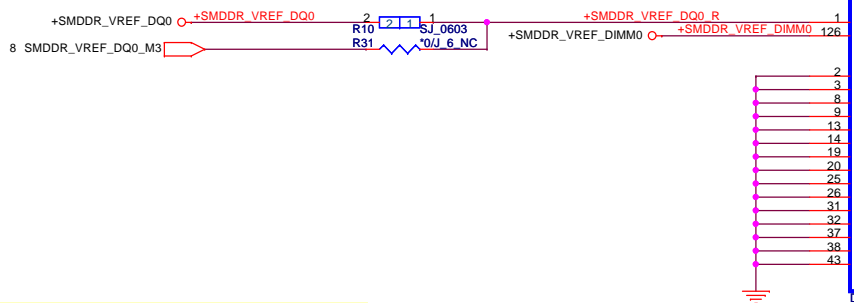
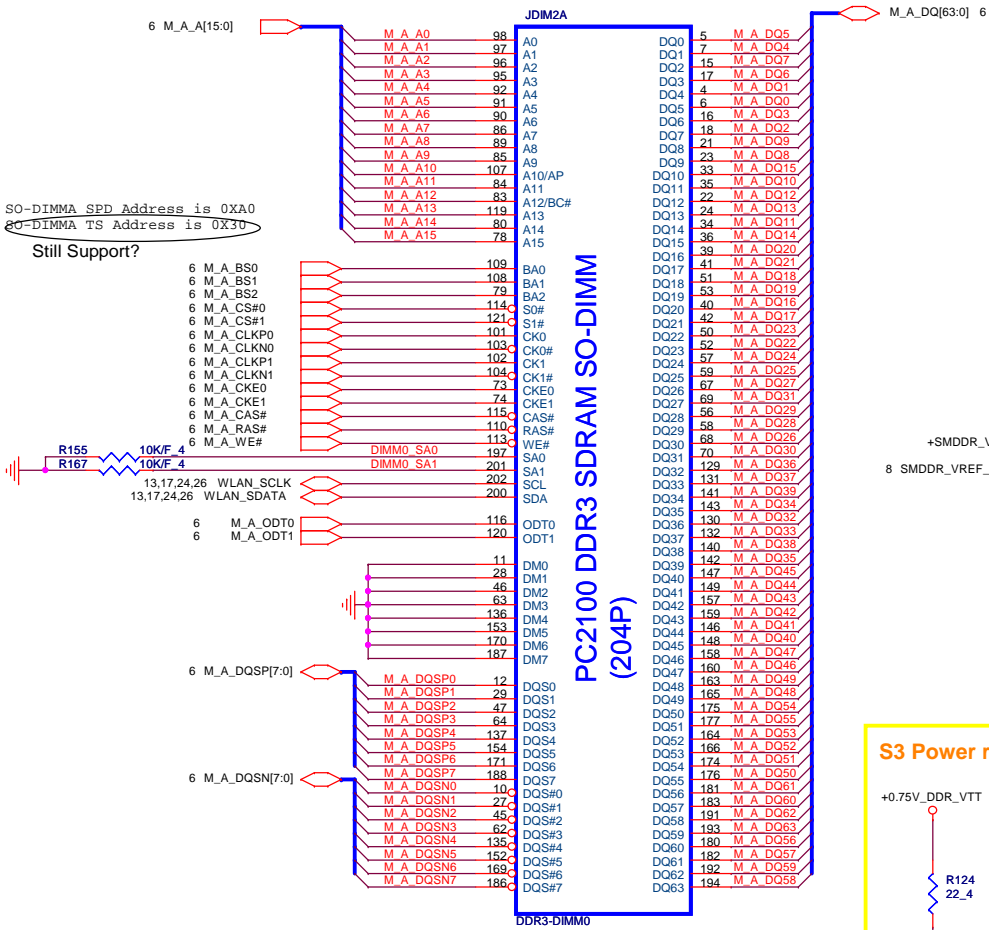
WLAN_RADIO_DIS# R316 10K 4

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Cougar Point 6/7

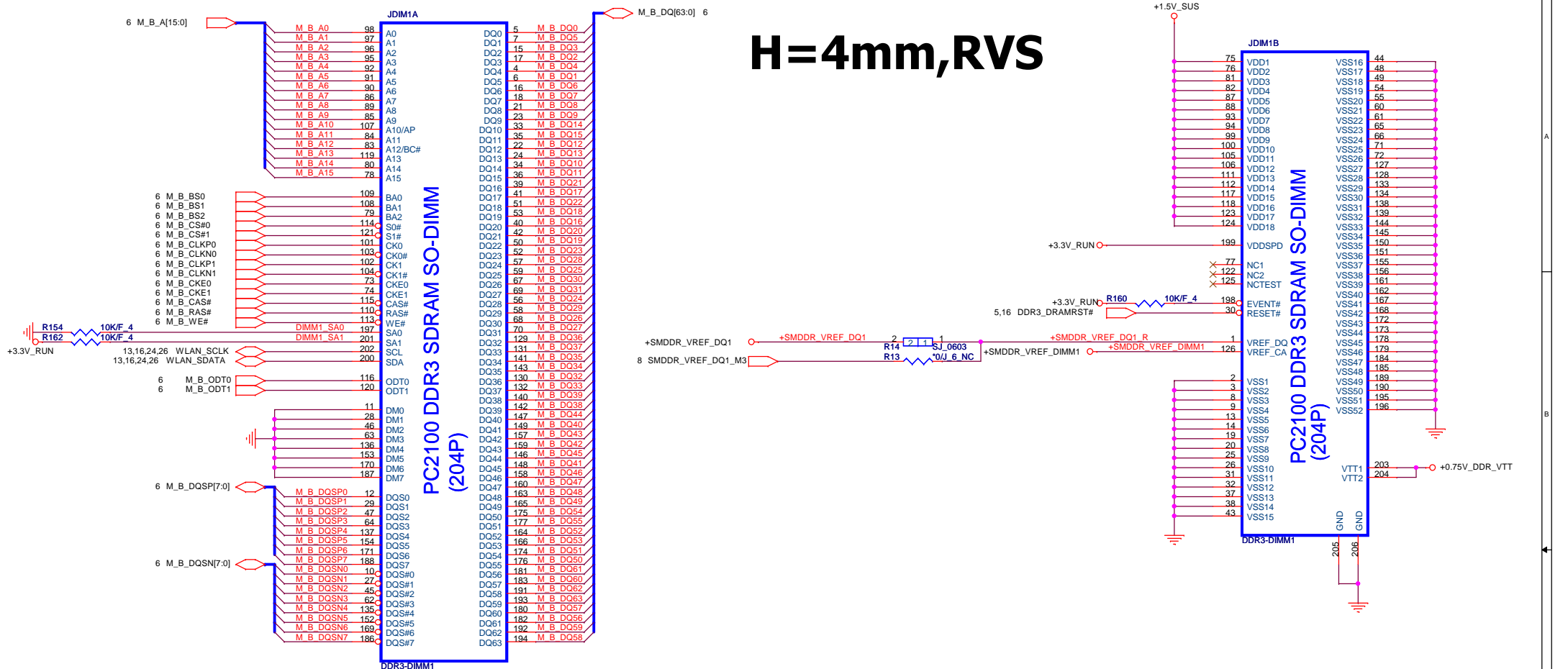
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		1A

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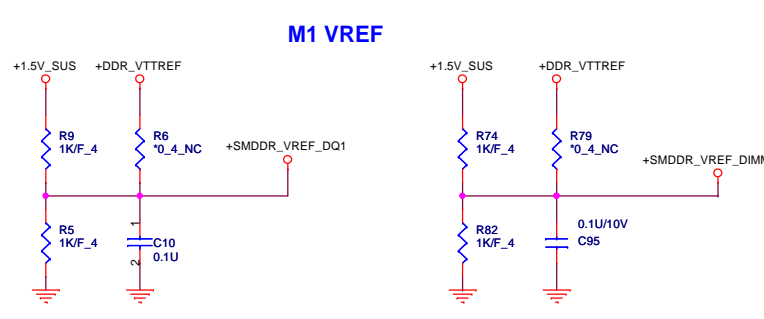
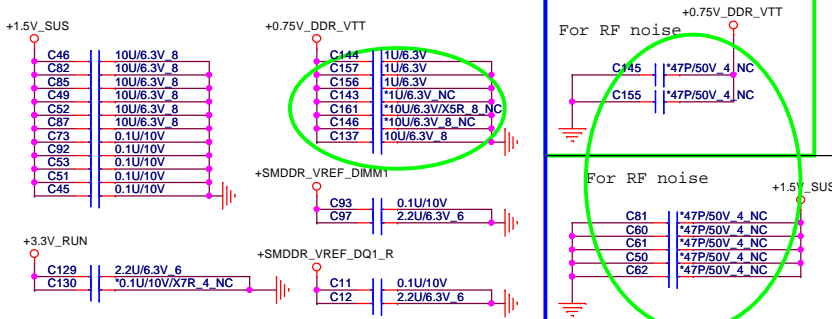
H=8mm,RVS




H=4mm,RVS



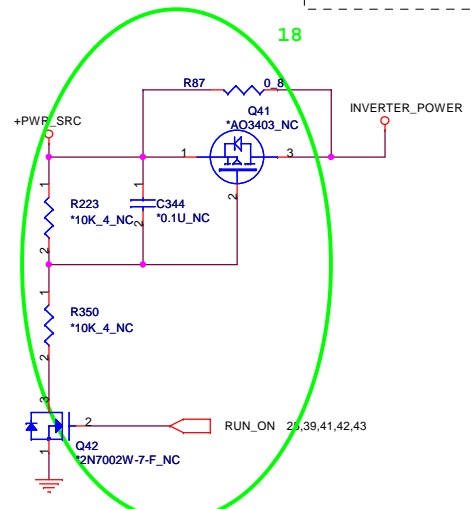
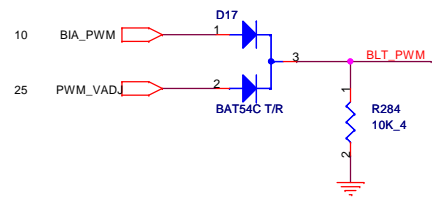
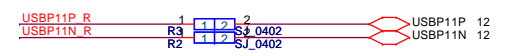
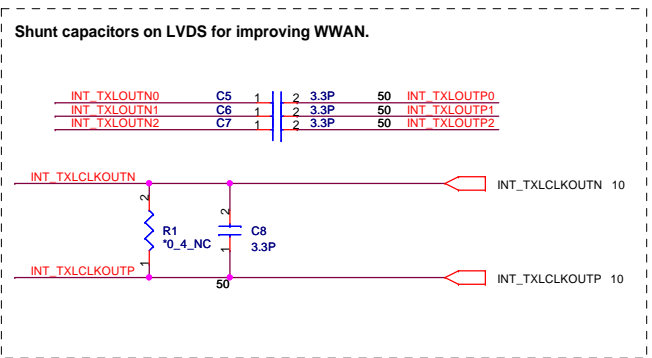
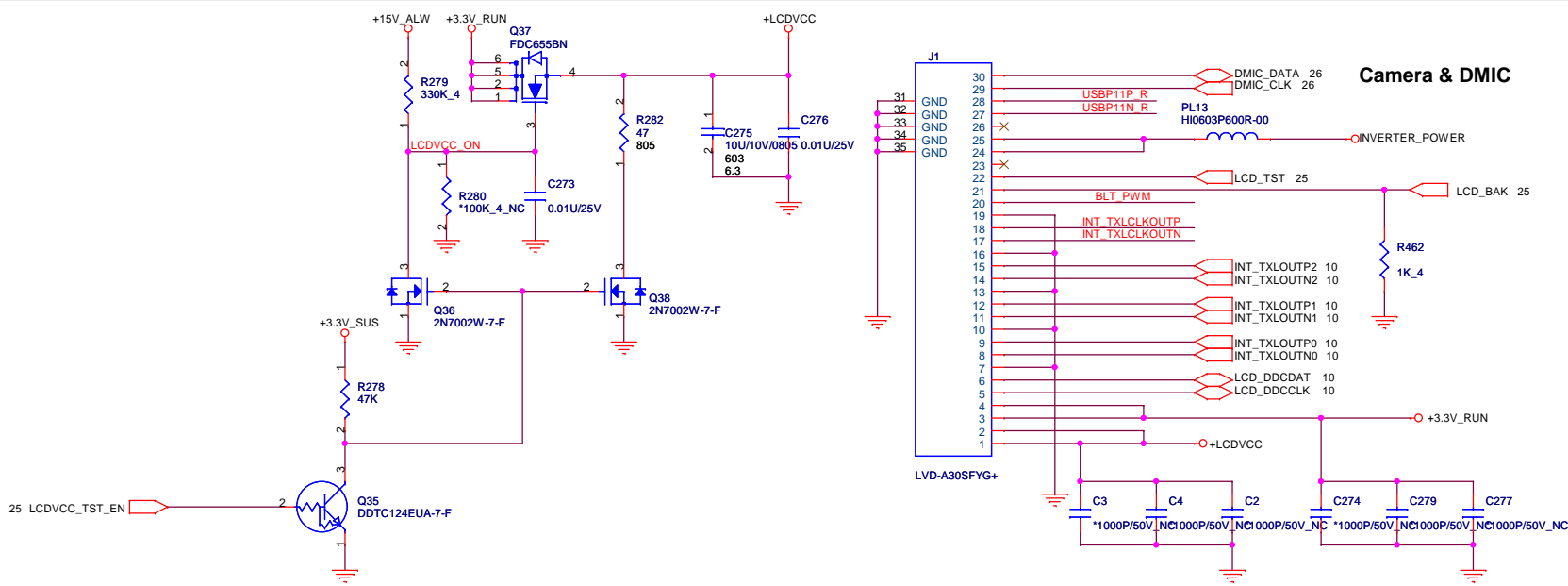
Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%

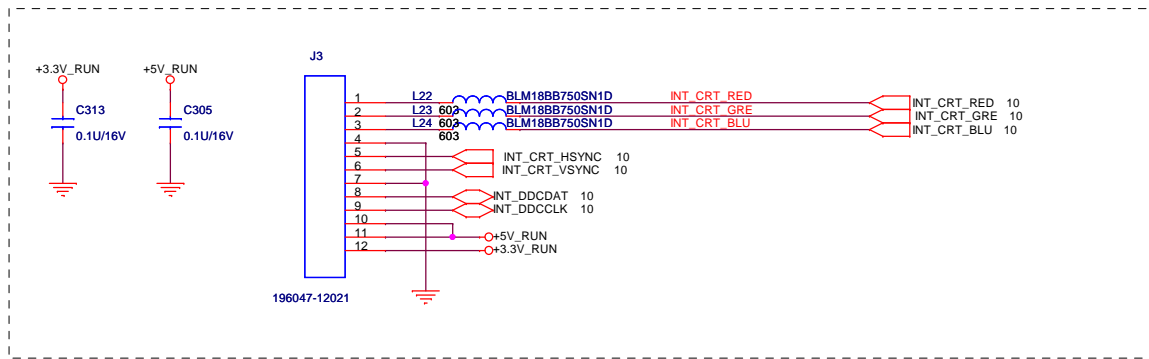




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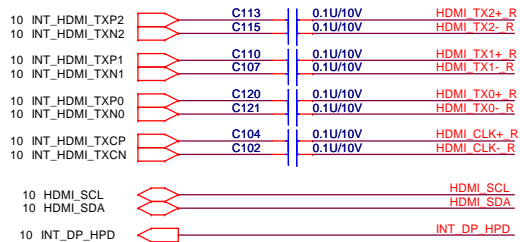


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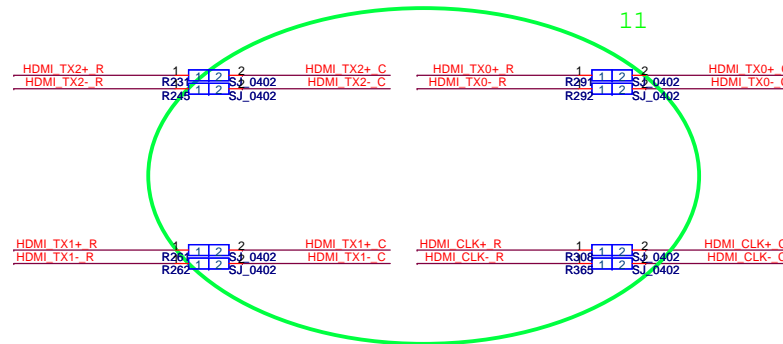
PROJECT : V02/R01

Size	Document Number	Rev
	BLANK	1A

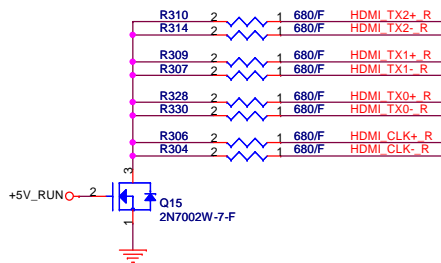
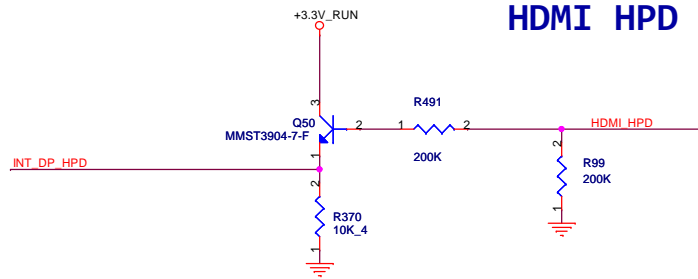
UMA HDMI



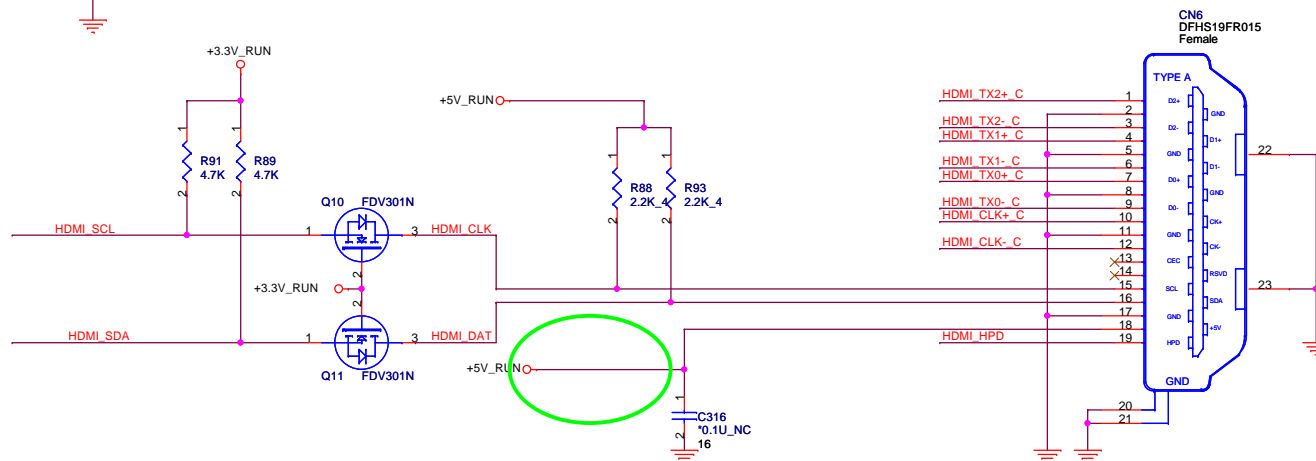
Reserve for EMI and close to HDMI CONN



HDMI HPD

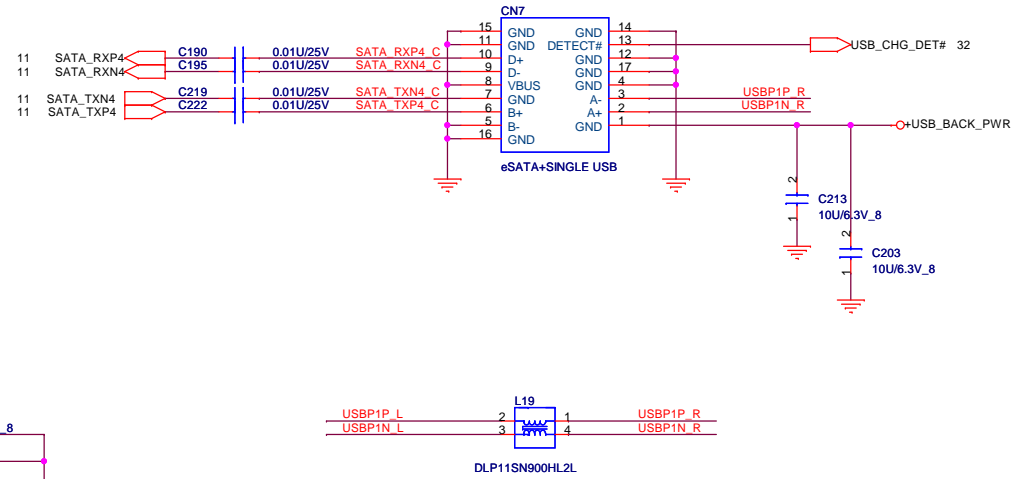
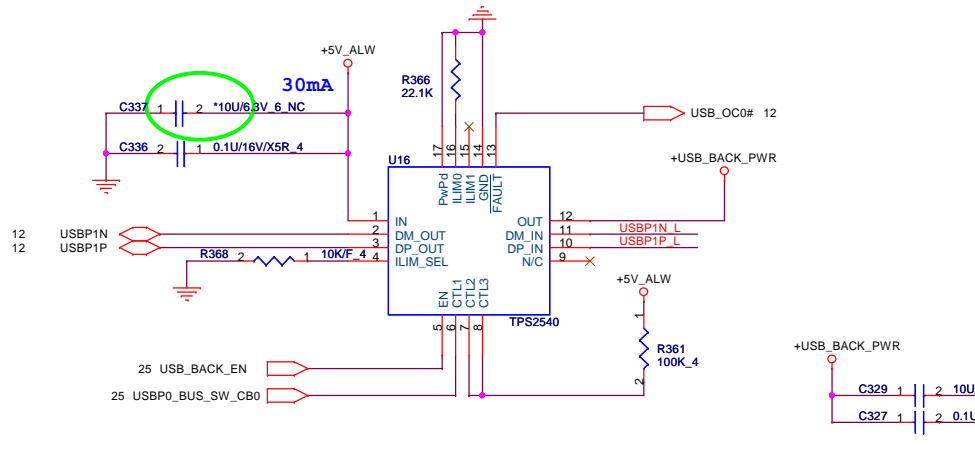


HDMI Conn.



ESATA + USB Conn + Power share

S3/S5 USB charging circuit

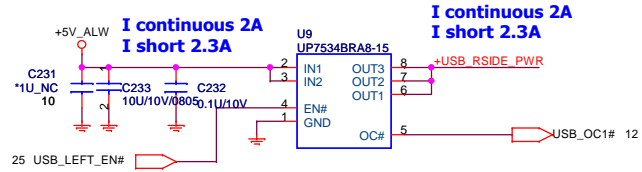


USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

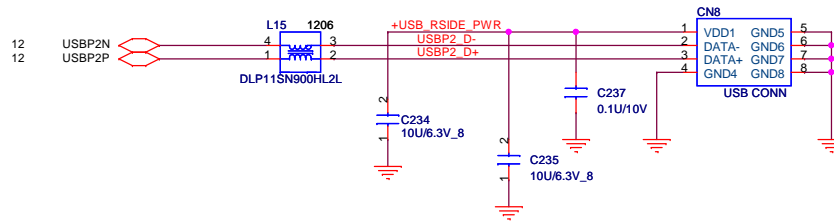
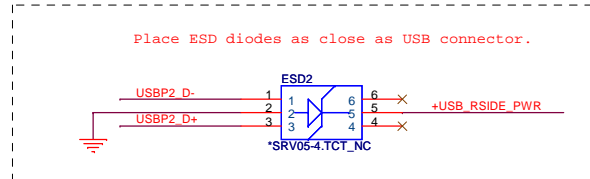
	R8224	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

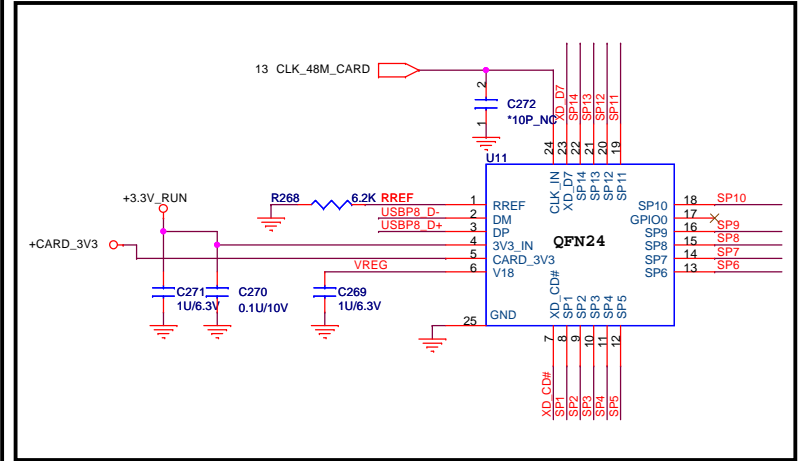
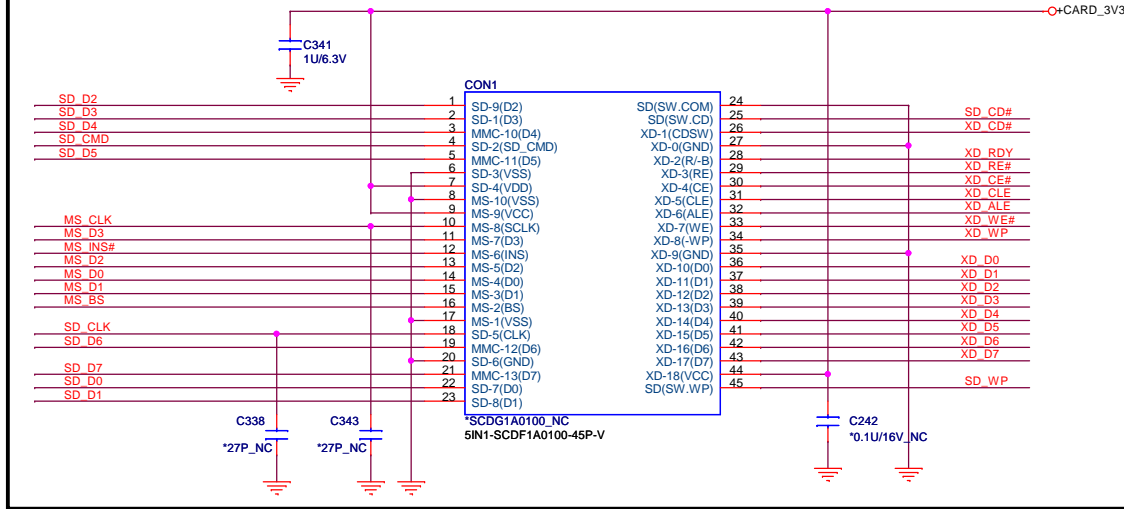


Quanta Computer Inc.

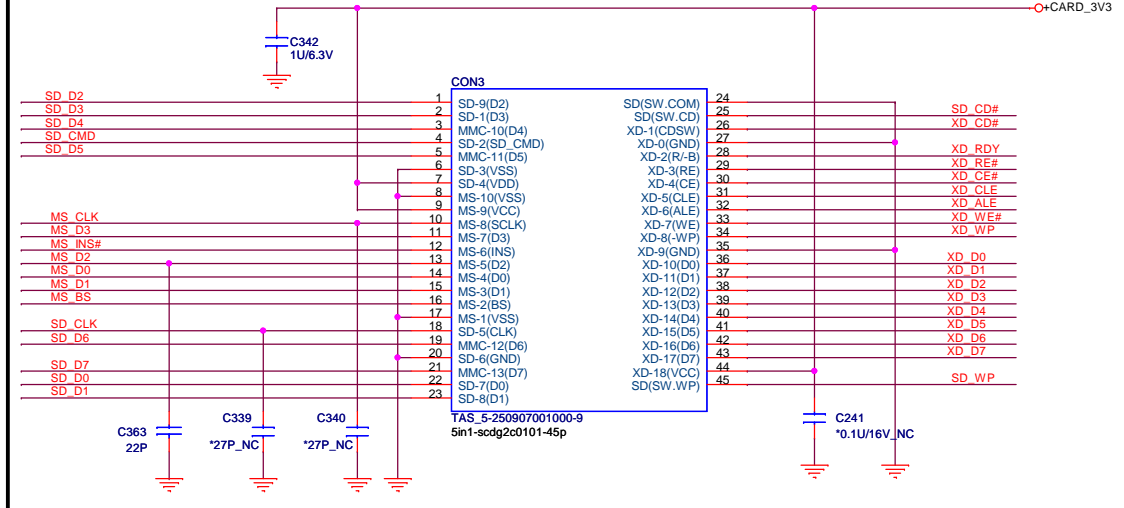
PROJECT : V02/R01

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Inspiron

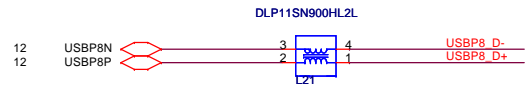


VOSTOR



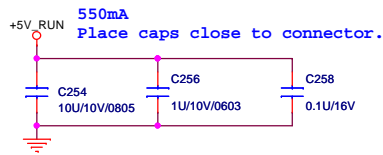
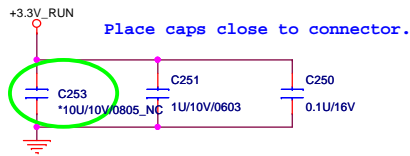
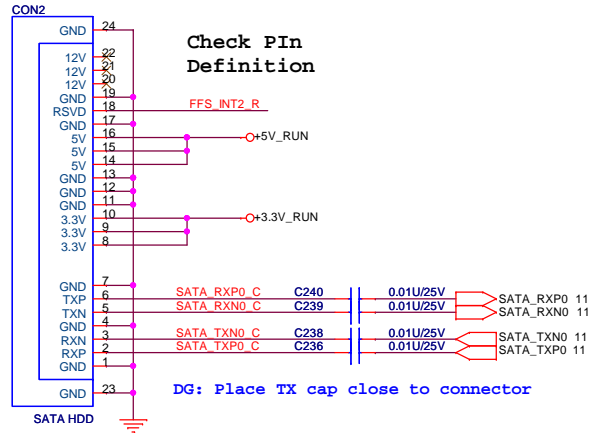
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6		MS BS

Share Pin

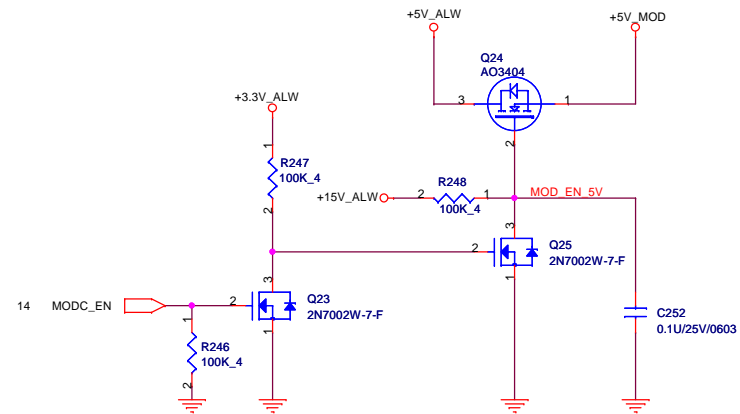
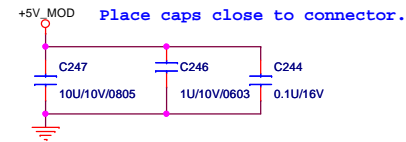
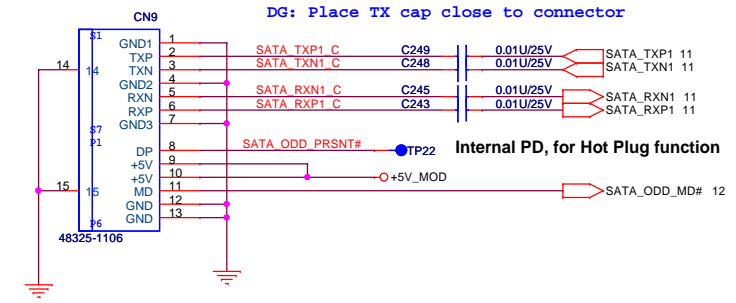


Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

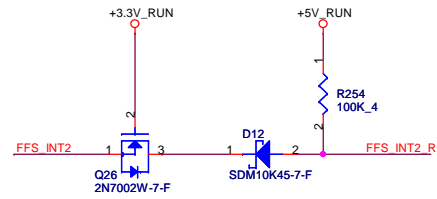
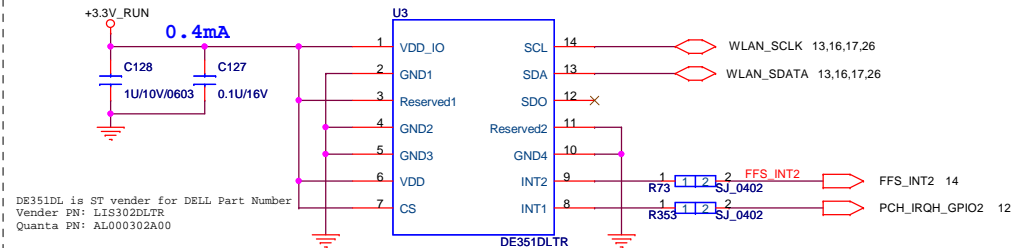
SATA Connector UM8



ODD Connector



3-axis Fall Sensor (HDD data protector)



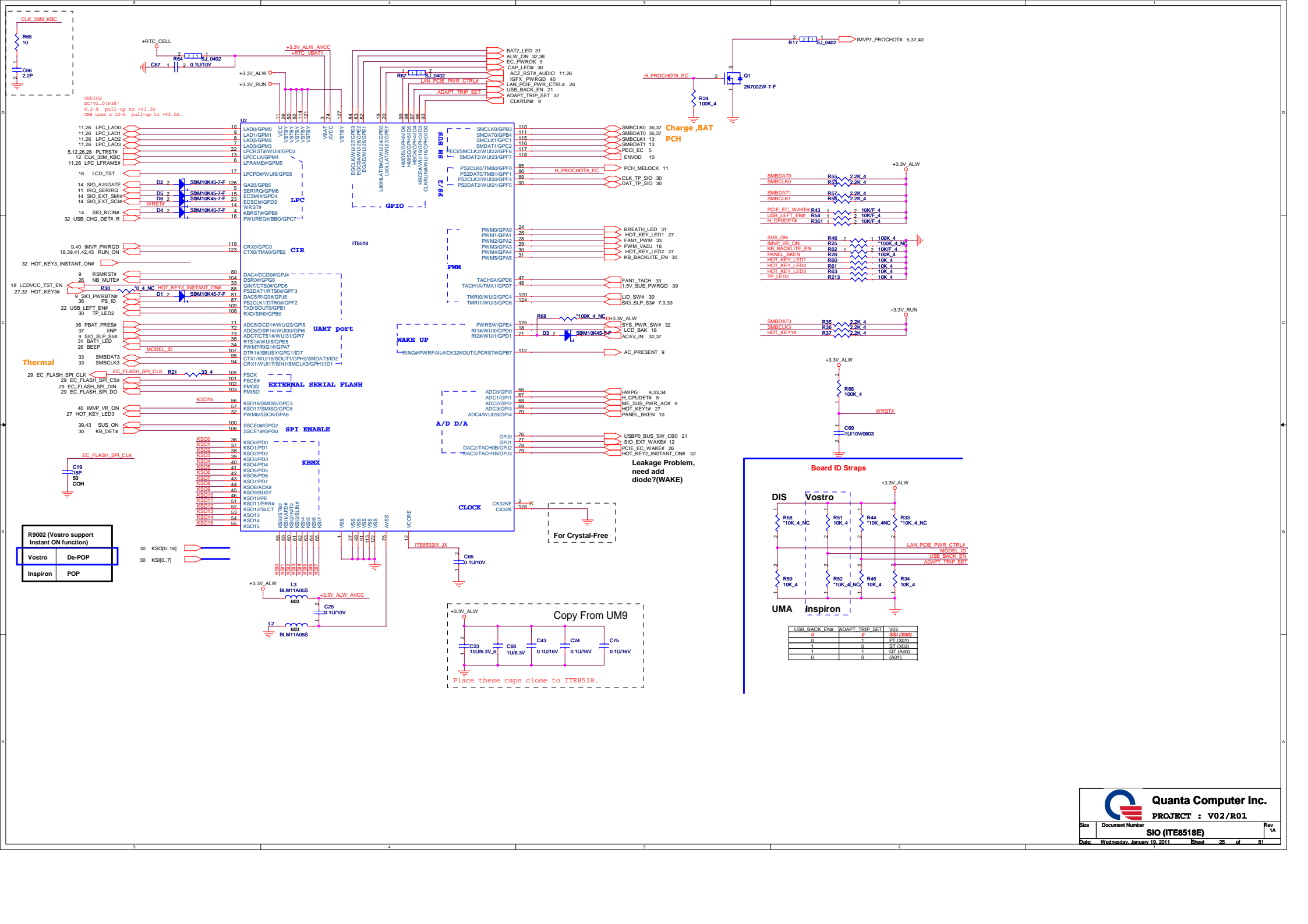
3-axis Fall Sensor	VOSTOR	Inspiron
U3, Q26, D12 R73, R254, R353 C127, C128	POP	NC

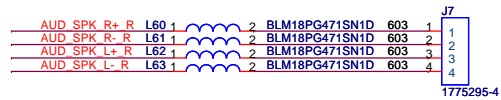
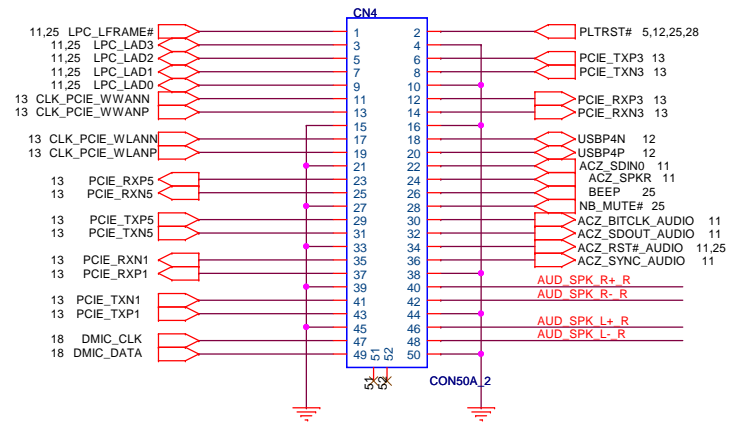
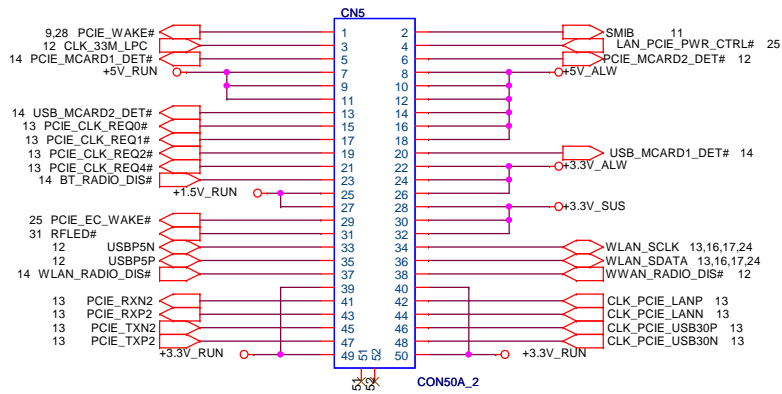
DE351DL is ST vender for DELL Part Number
Vender PN: LIS302DLTR
Quanta PN: AL000302A00



Quanta Computer Inc.

PROJECT : V02/R01





Int. Stereo Speakers
5V / 4 Ohm / 2W

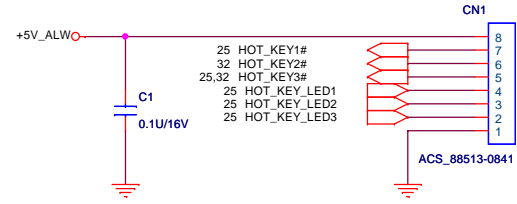
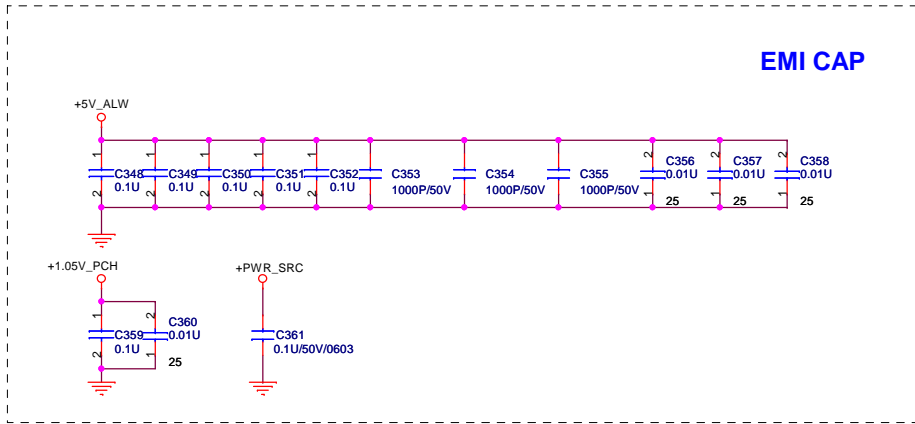


Quanta Computer Inc.

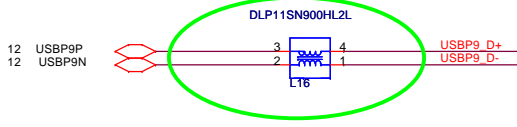
PROJECT : V02/R01

SIO (ITE8518E)

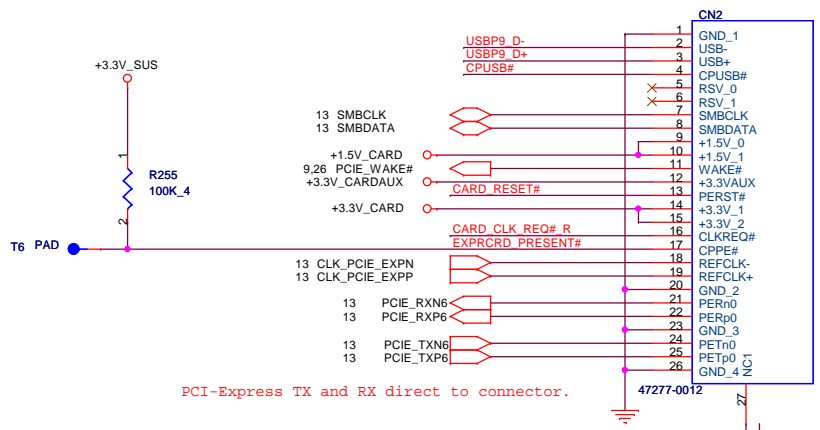
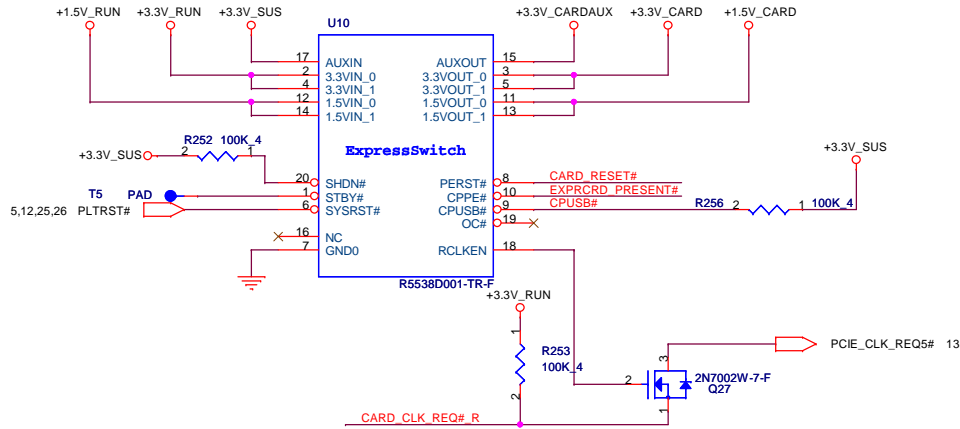
Size	Document Number	Rev
		1A
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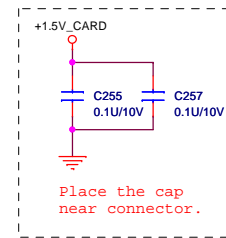
Express Card



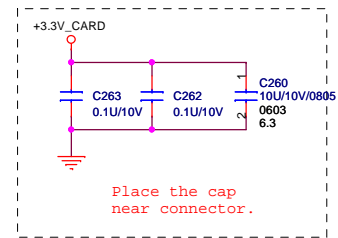
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.

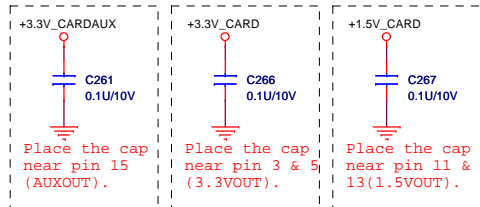


Place the cap near connector.



Place the cap near connector.

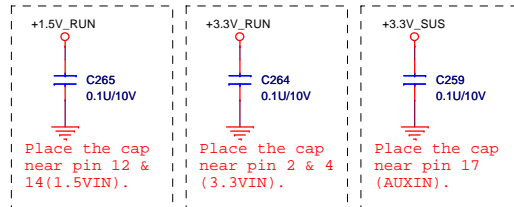
If close enough, could combine



Place the cap near pin 15 (AUXOUT).

Place the cap near pin 3 & 5 (3.3VOUT).

Place the cap near pin 11 & 13 (1.5VOUT).

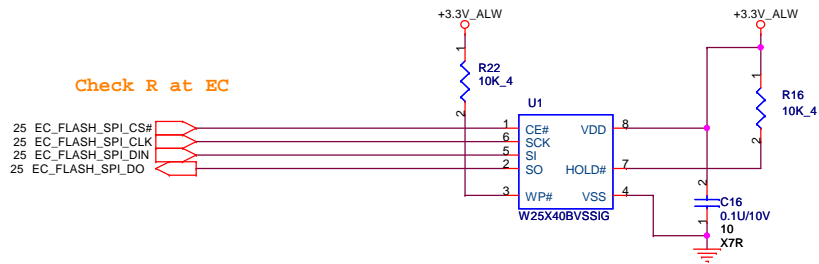


Place the cap near pin 12 & 14 (1.5VIN).

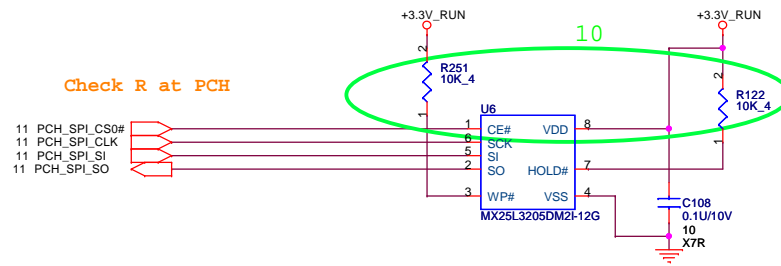
Place the cap near pin 2 & 4 (3.3VIN).

Place the cap near pin 17 (AUXIN).

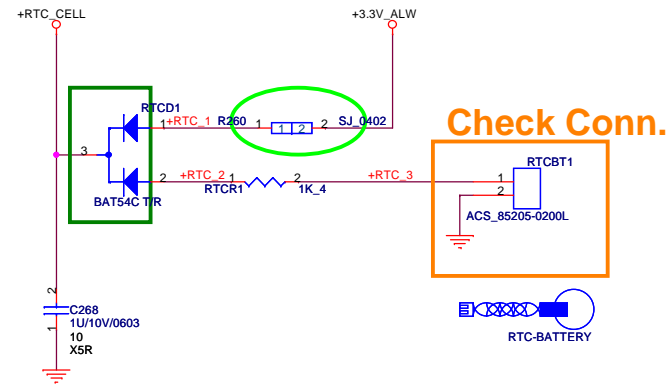
For EC 4Mbit (512K Byte)



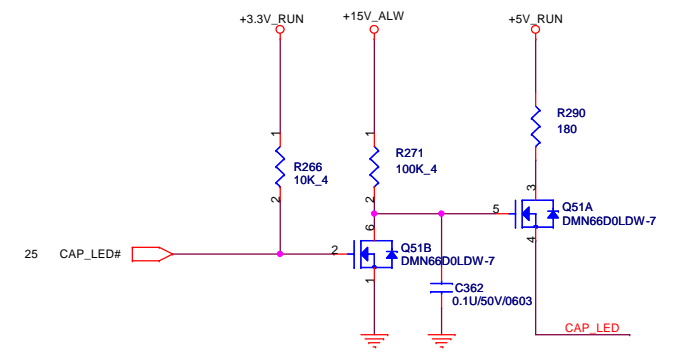
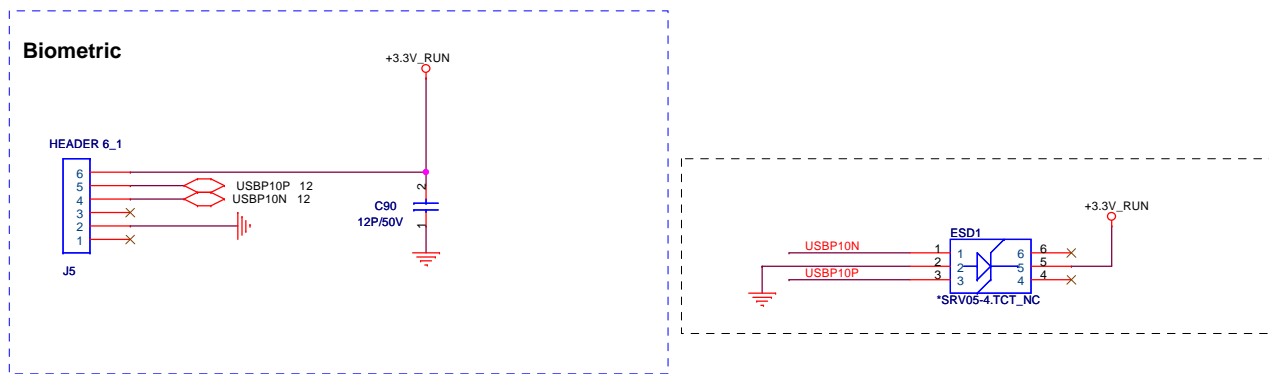
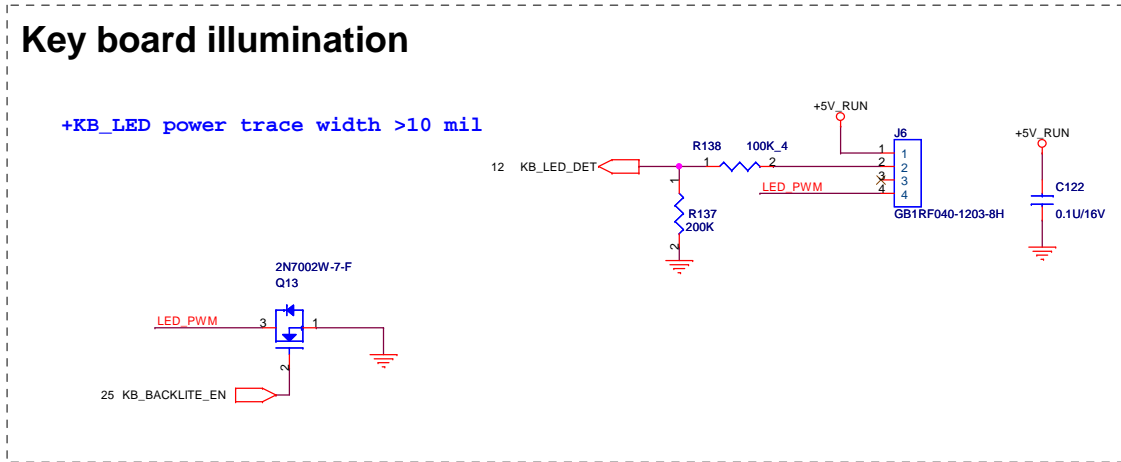
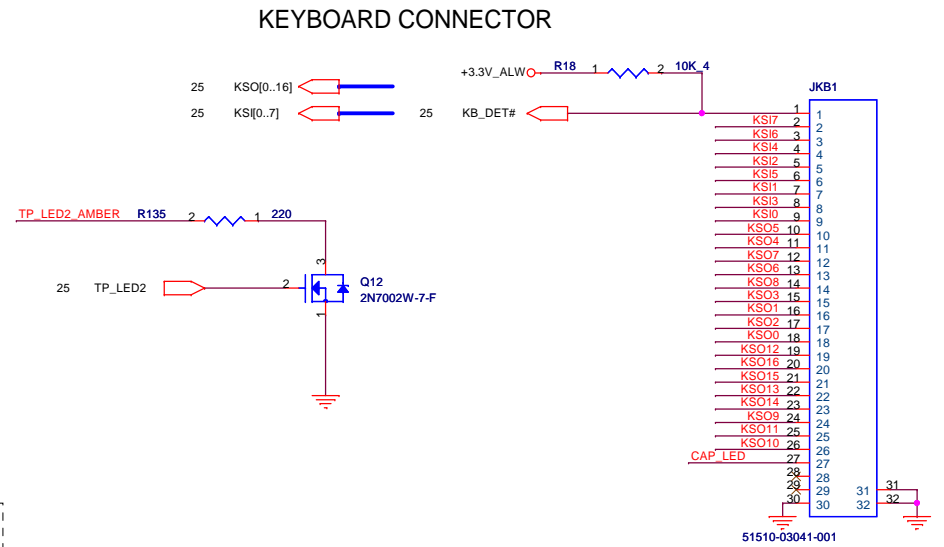
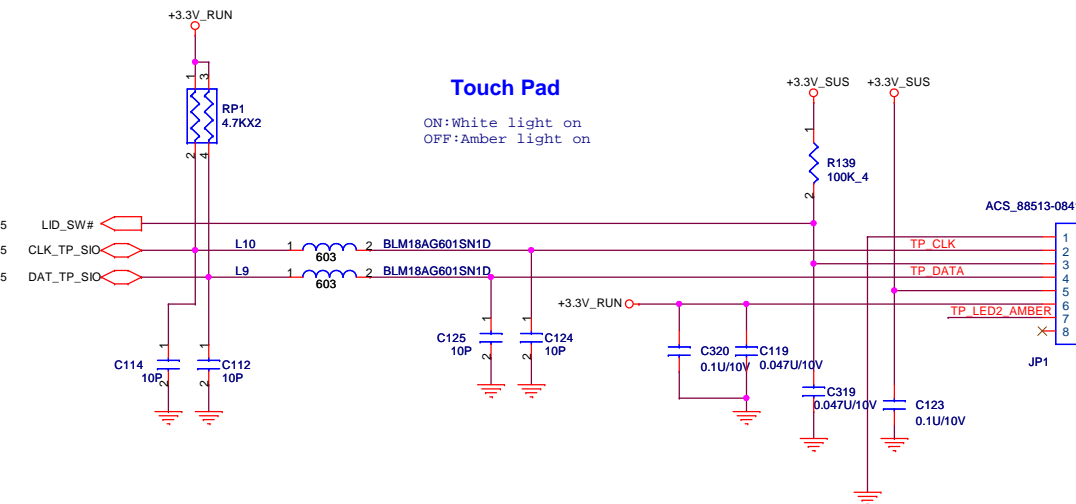
For PCH 32Mbit (4M Byte)

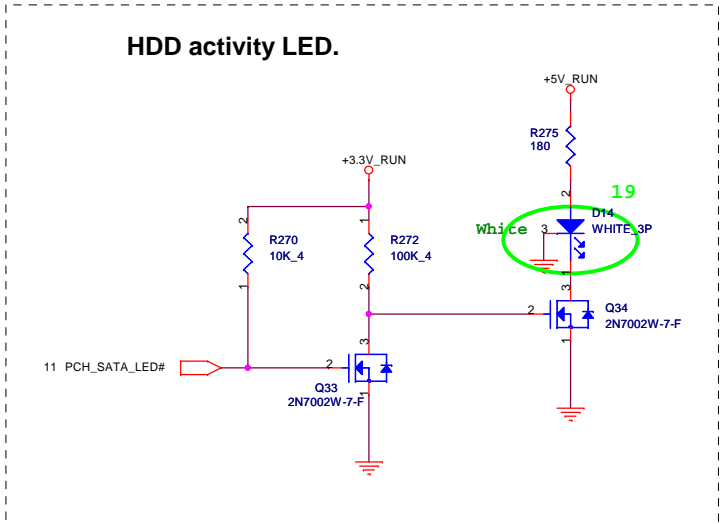
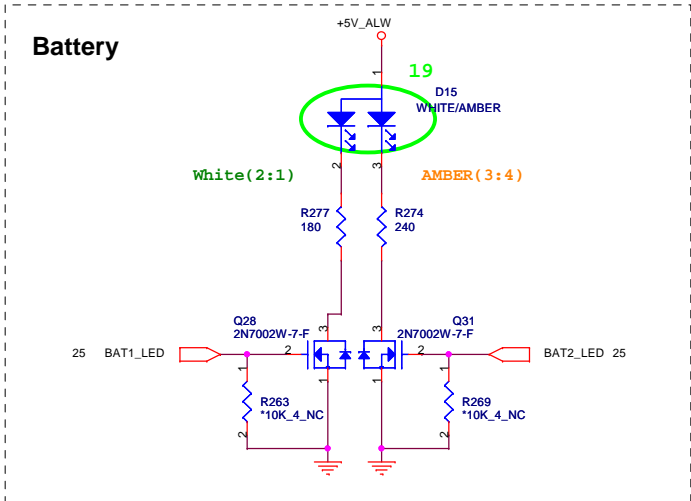
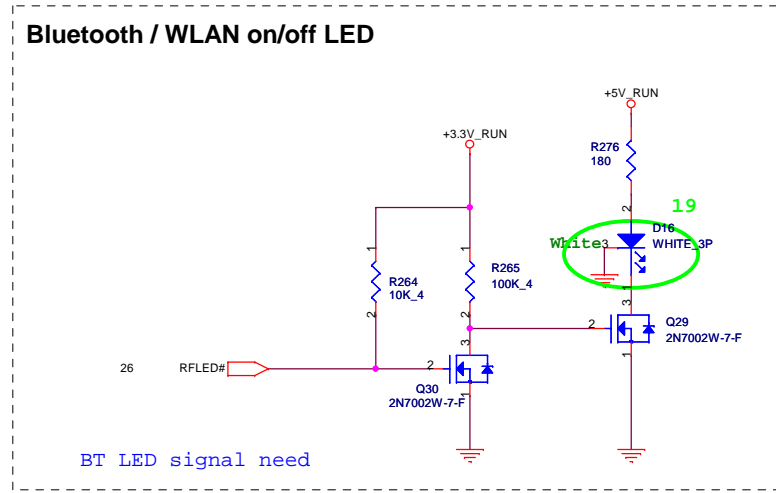
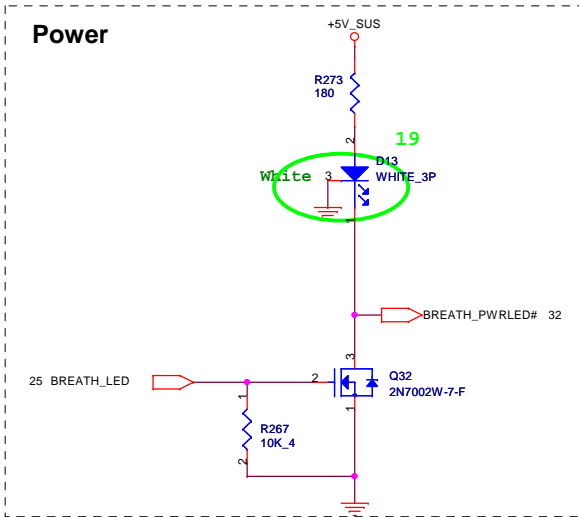


RTC



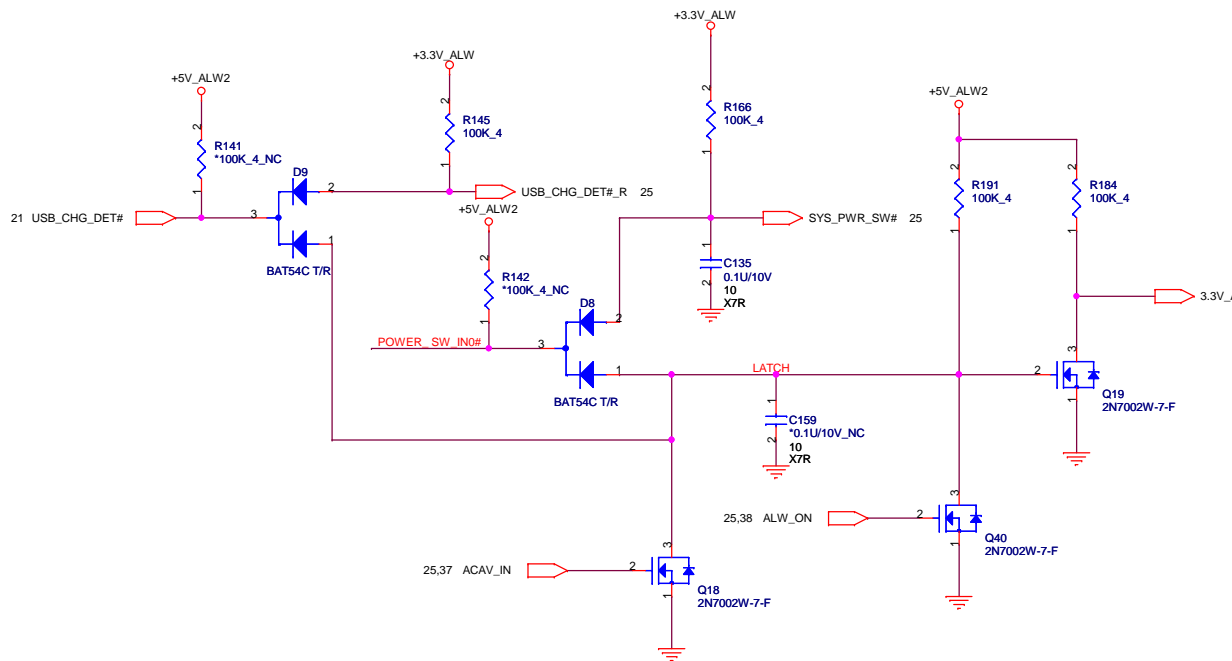
Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA



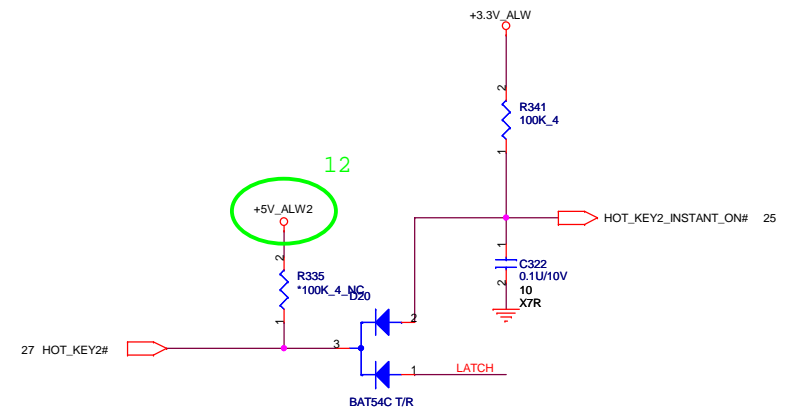


VOSTOR	R273,R276,R277,R275	R274
	180 ohm PN:CS11802JB15	240ohm PN:CS12402JB13
Inspiron	R273,R276,R277,R275	R274
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

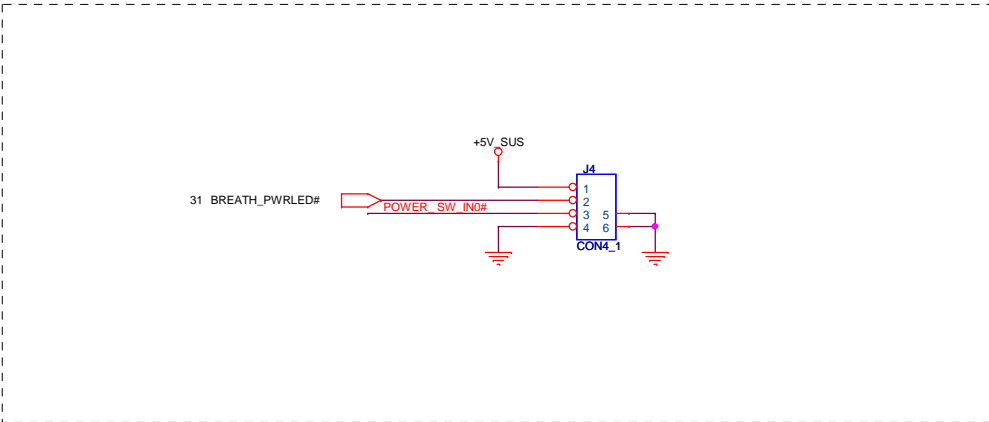
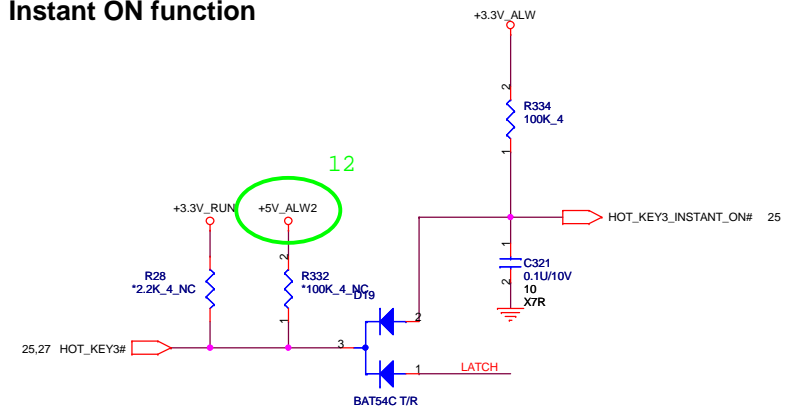
3VALW ON POWER LOGIC



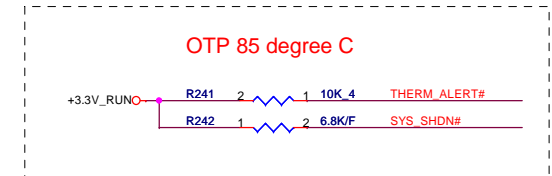
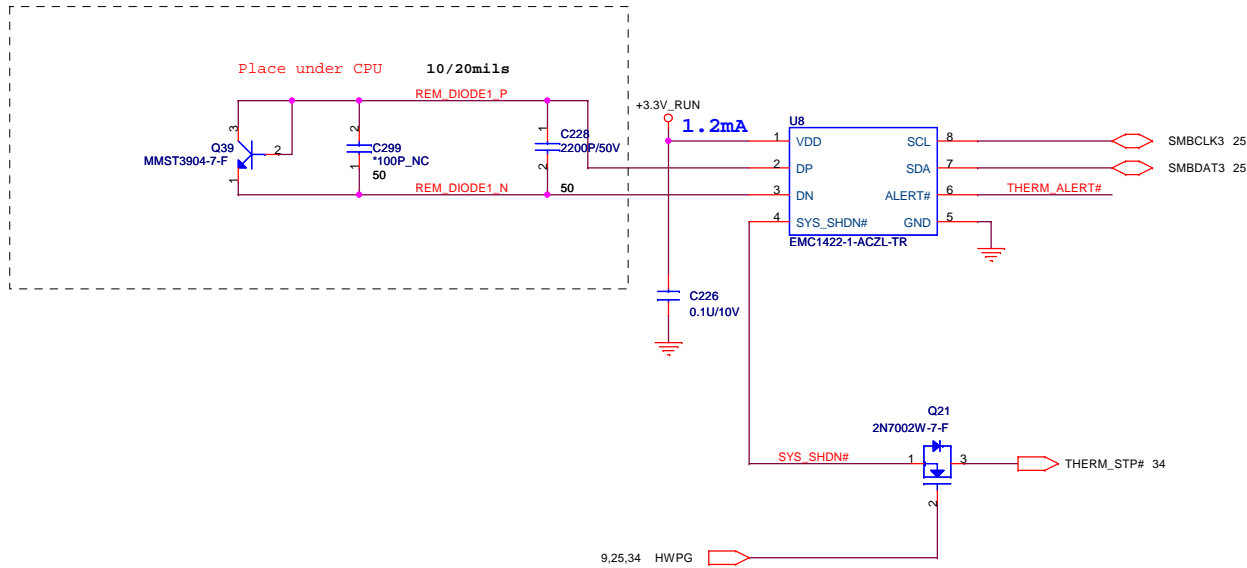
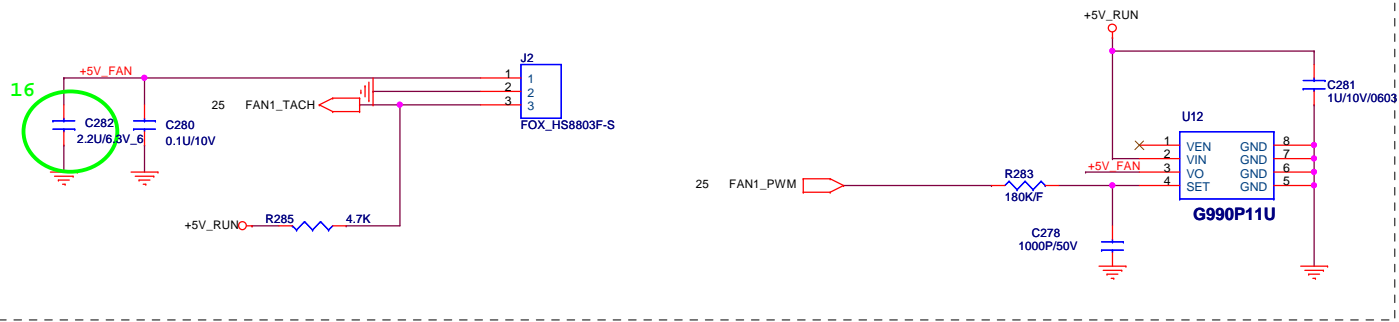
Vostro pop D19,C321,R334 depop R28,R30
 Inspiron depop D19,C321,R334 pop R28,R30



Instant ON function

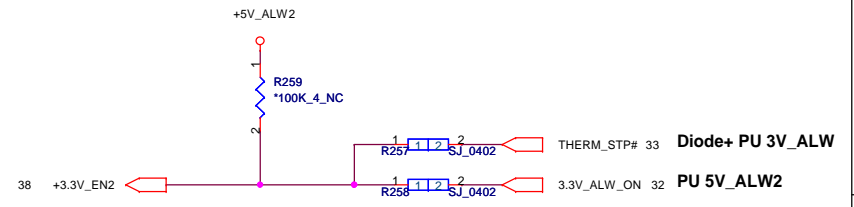
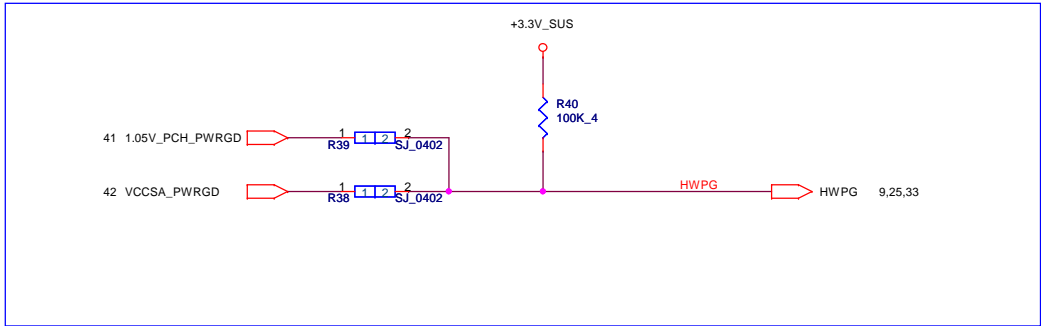


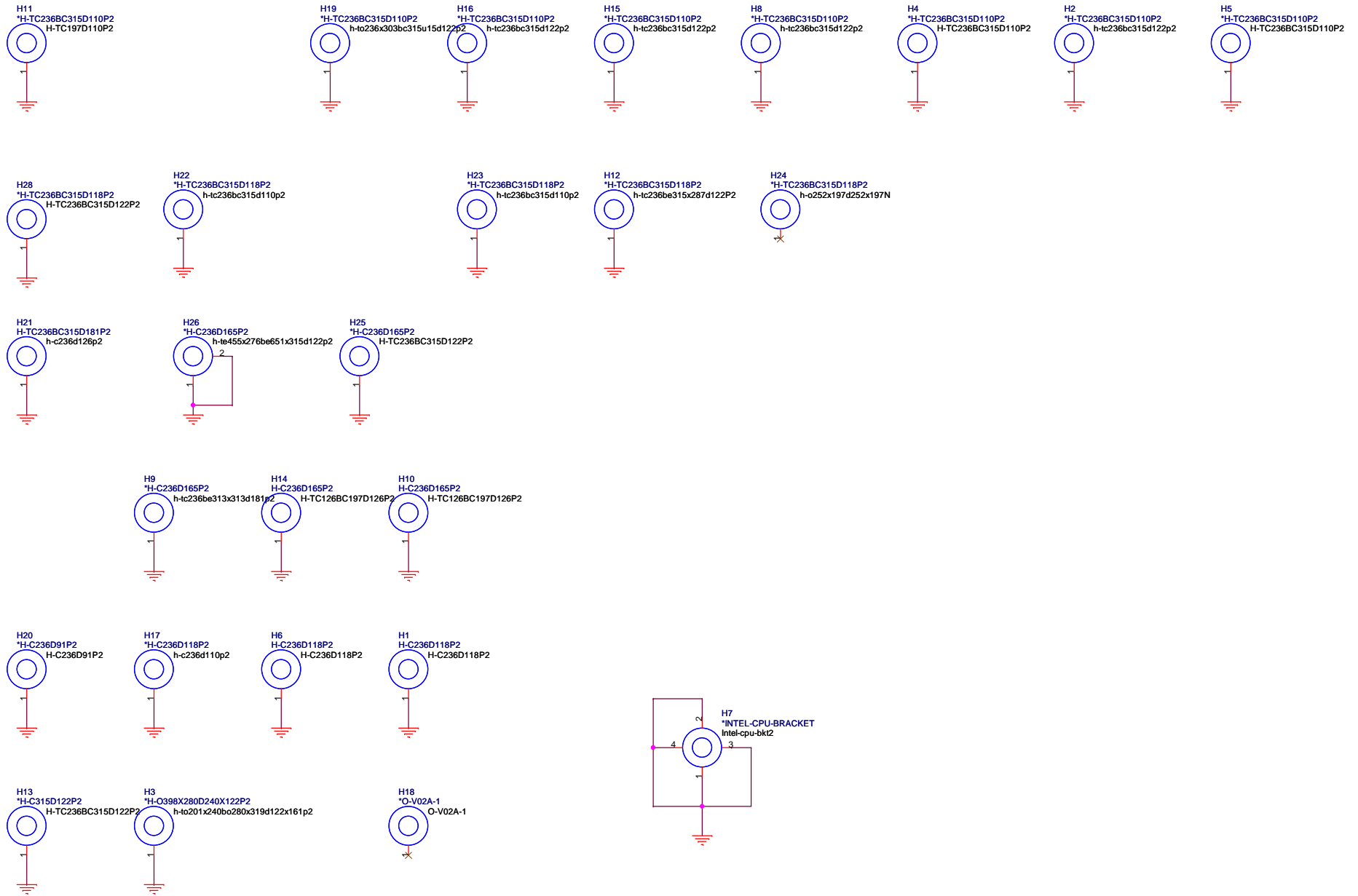
FAN CONTROL

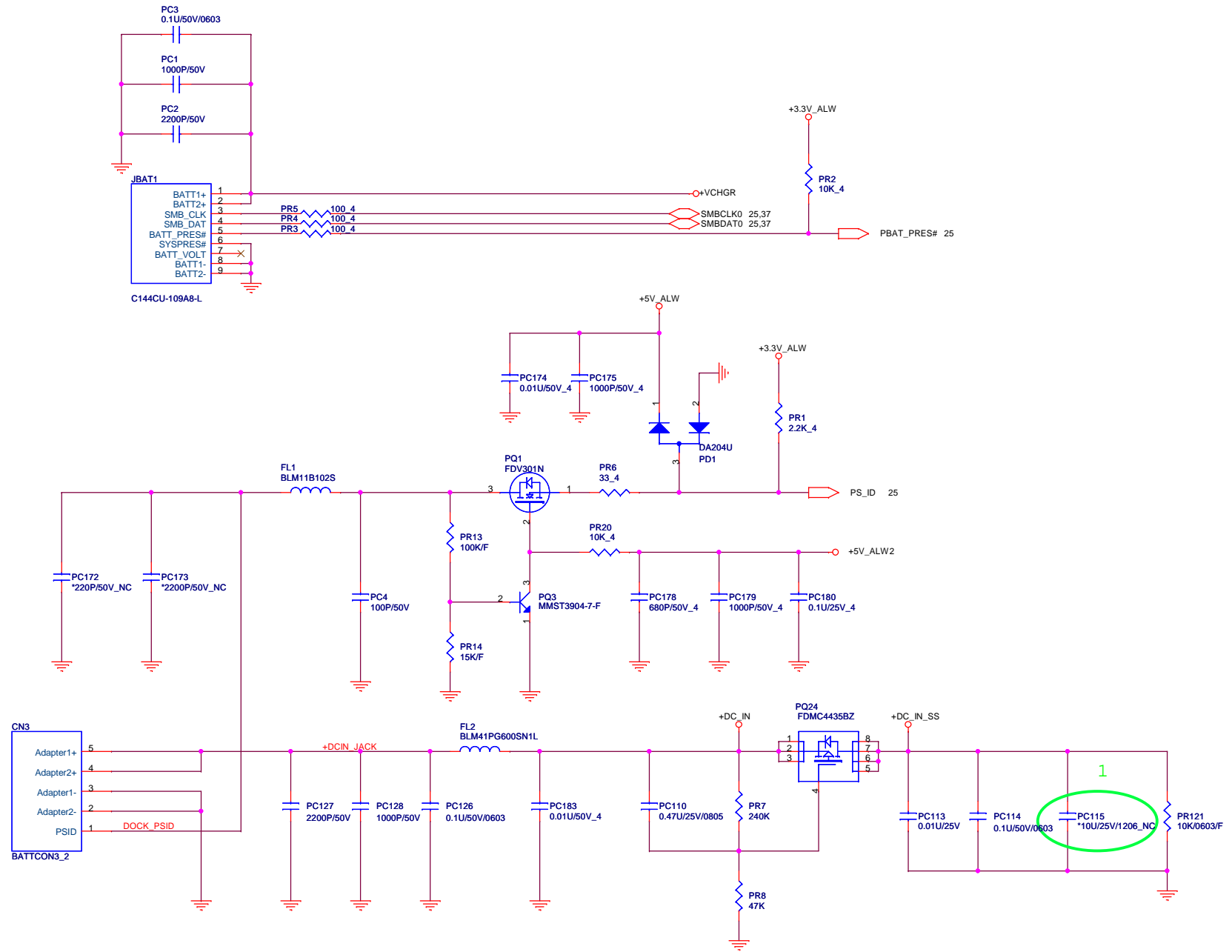


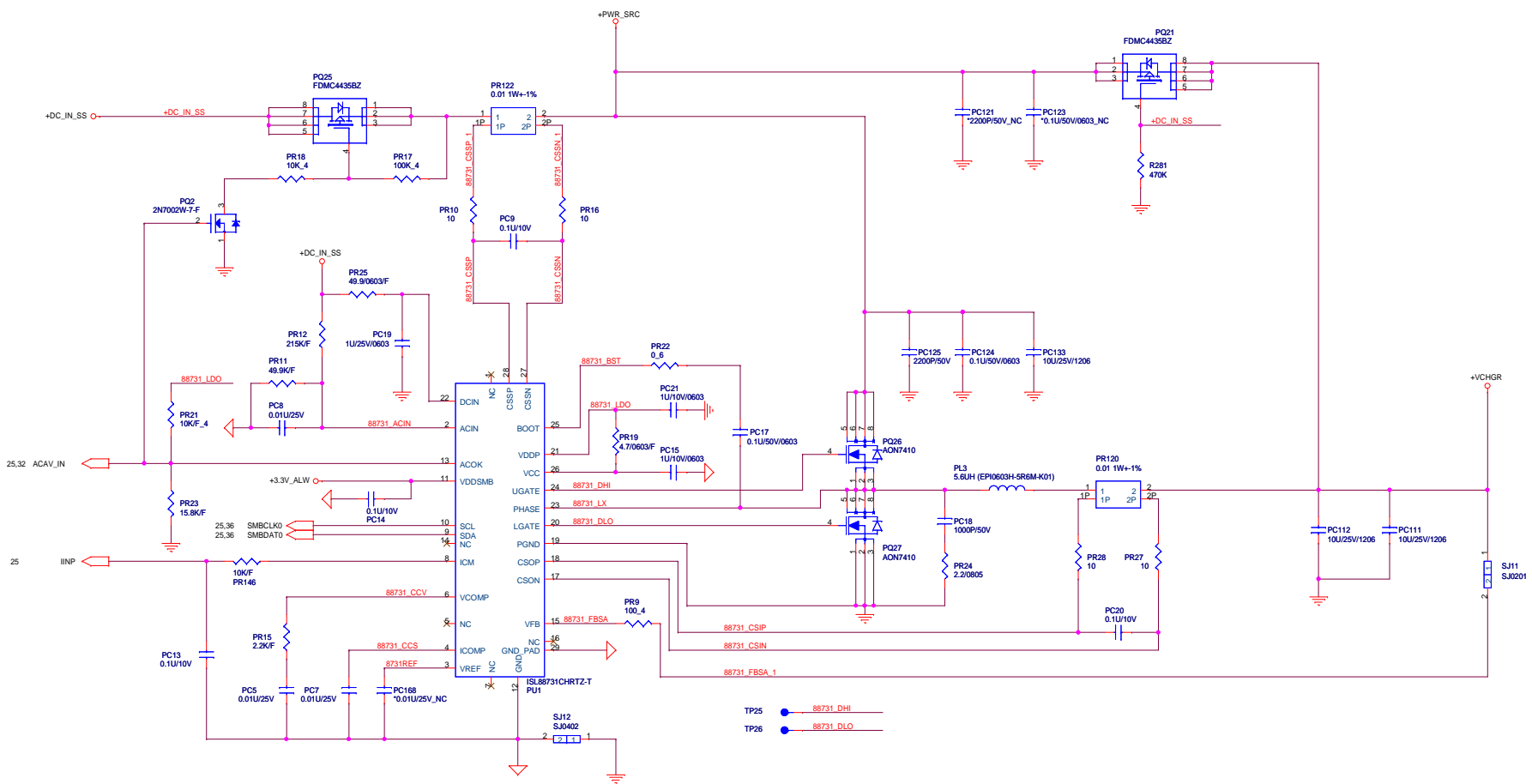
OTP 85 degree C

SYS_SHDN# \ ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77 °C	83 °C	89 °C	95 °C	101 °C	107 °C
6.8K	78 °C	84 °C	90 °C	96 °C	102 °C	108 °C
10K	79 °C	85 °C	91 °C	97 °C	103 °C	109 °C
15K	80 °C	86 °C	92 °C	98 °C	104 °C	110 °C
22K	81 °C	87 °C	93 °C	99 °C	105 °C	111 °C
33K	82 °C	88 °C	94 °C	100 °C	106 °C	112 °C

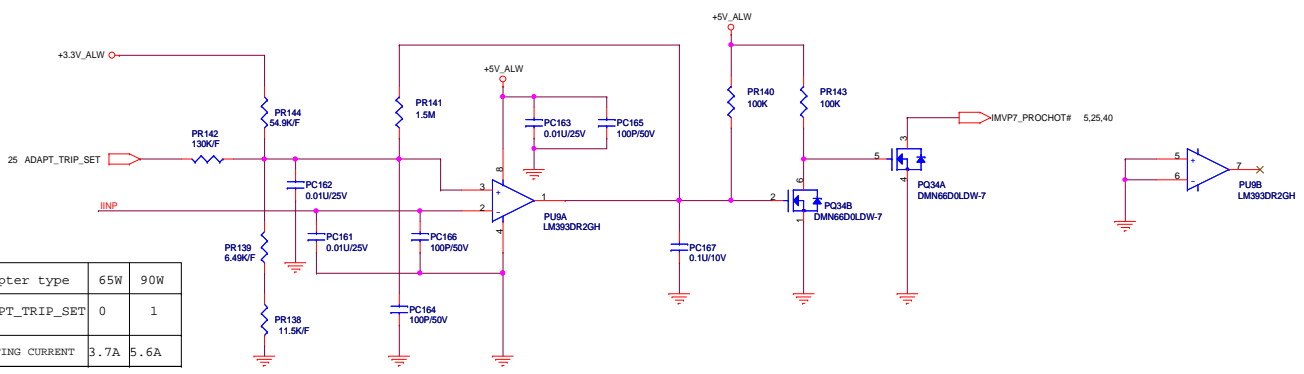


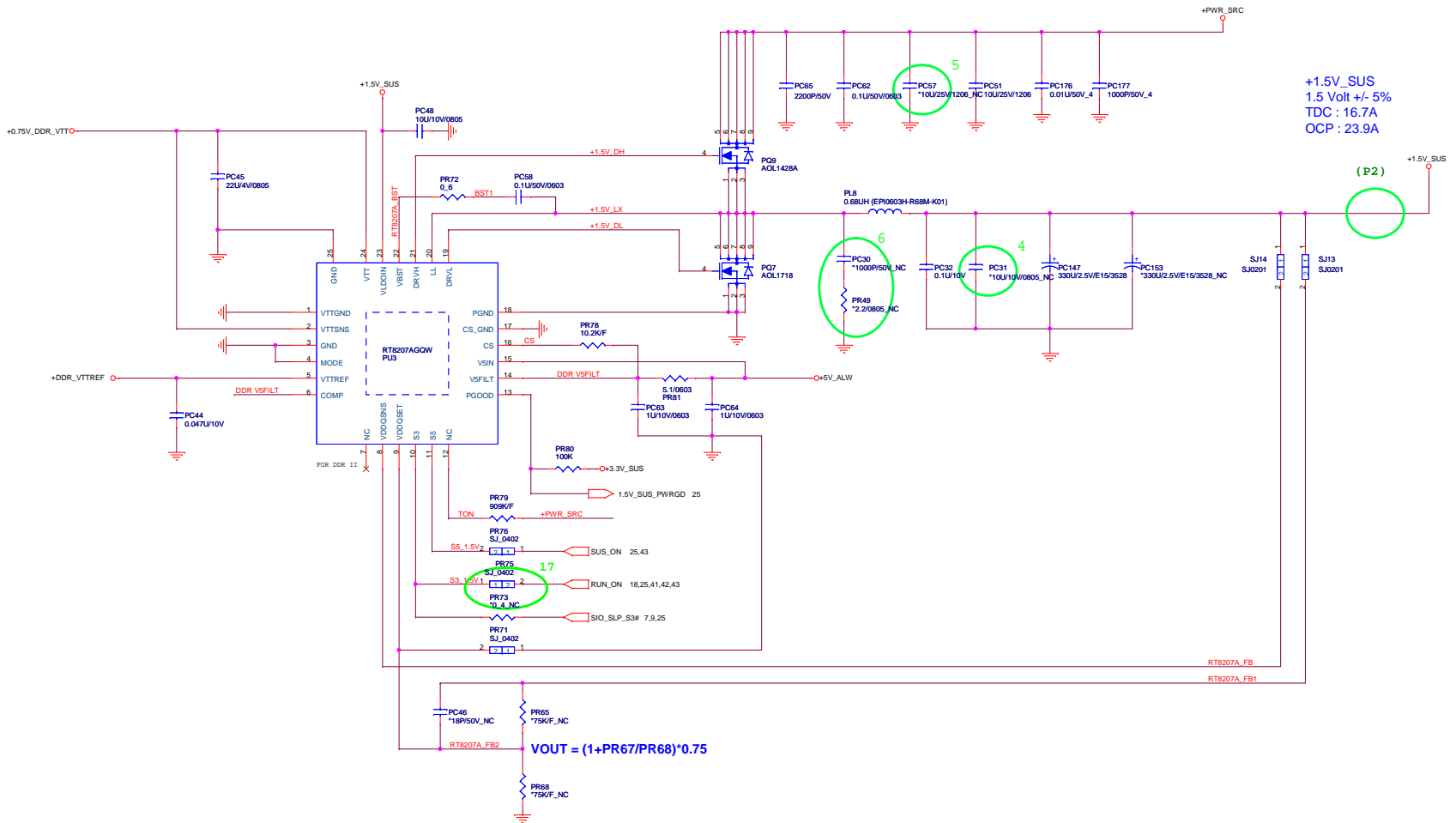






Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A





VDDQ and VTT discharge control

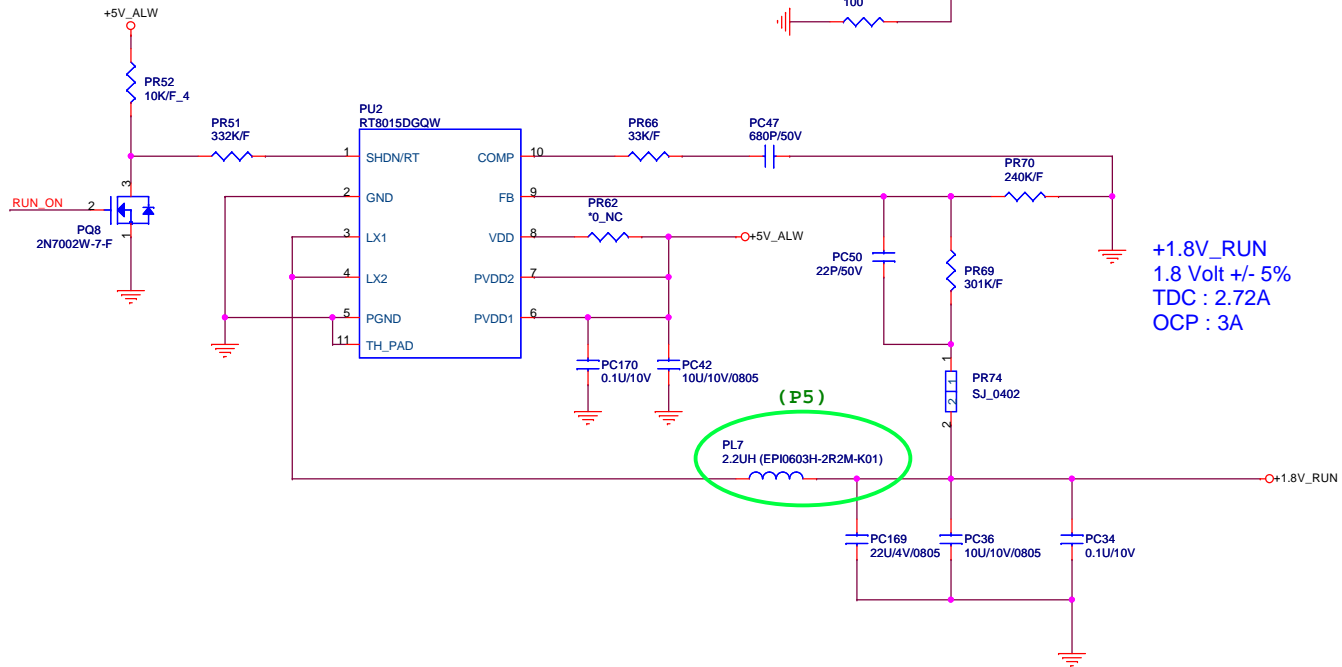
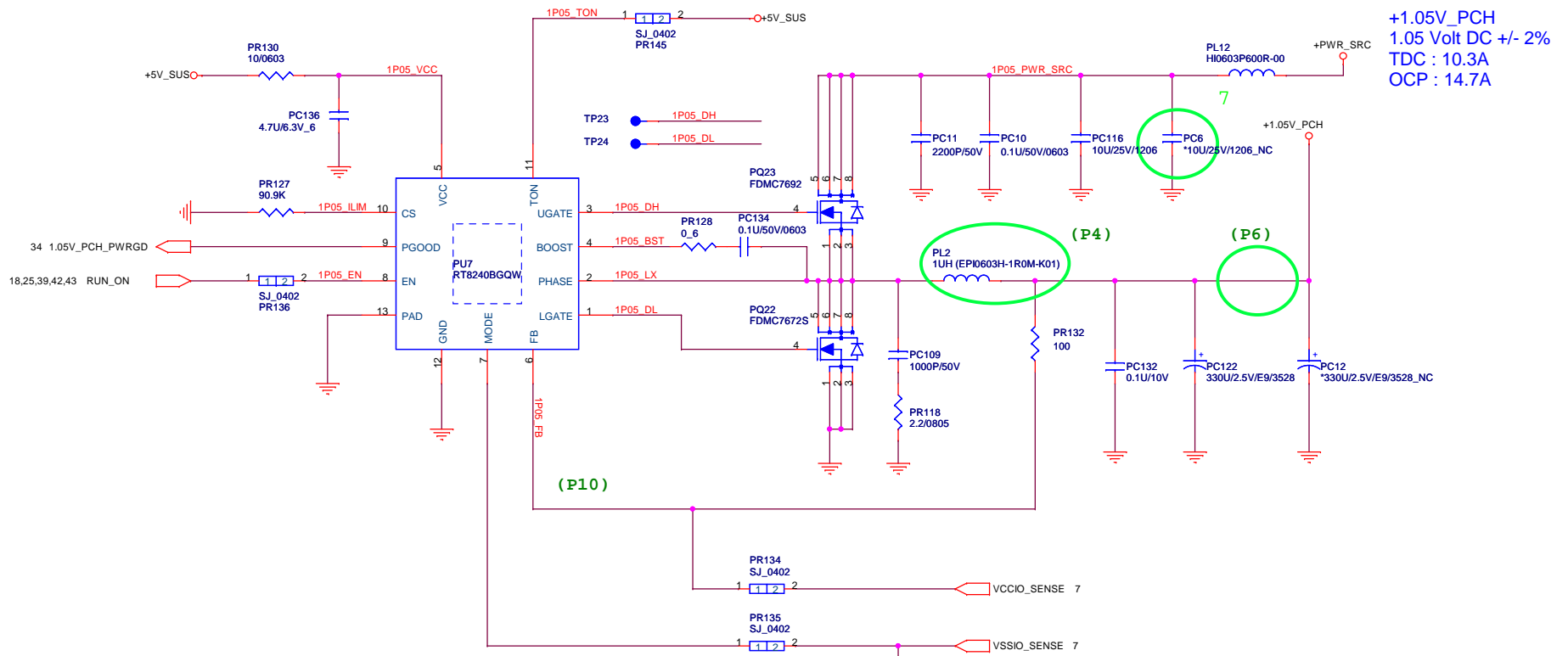
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

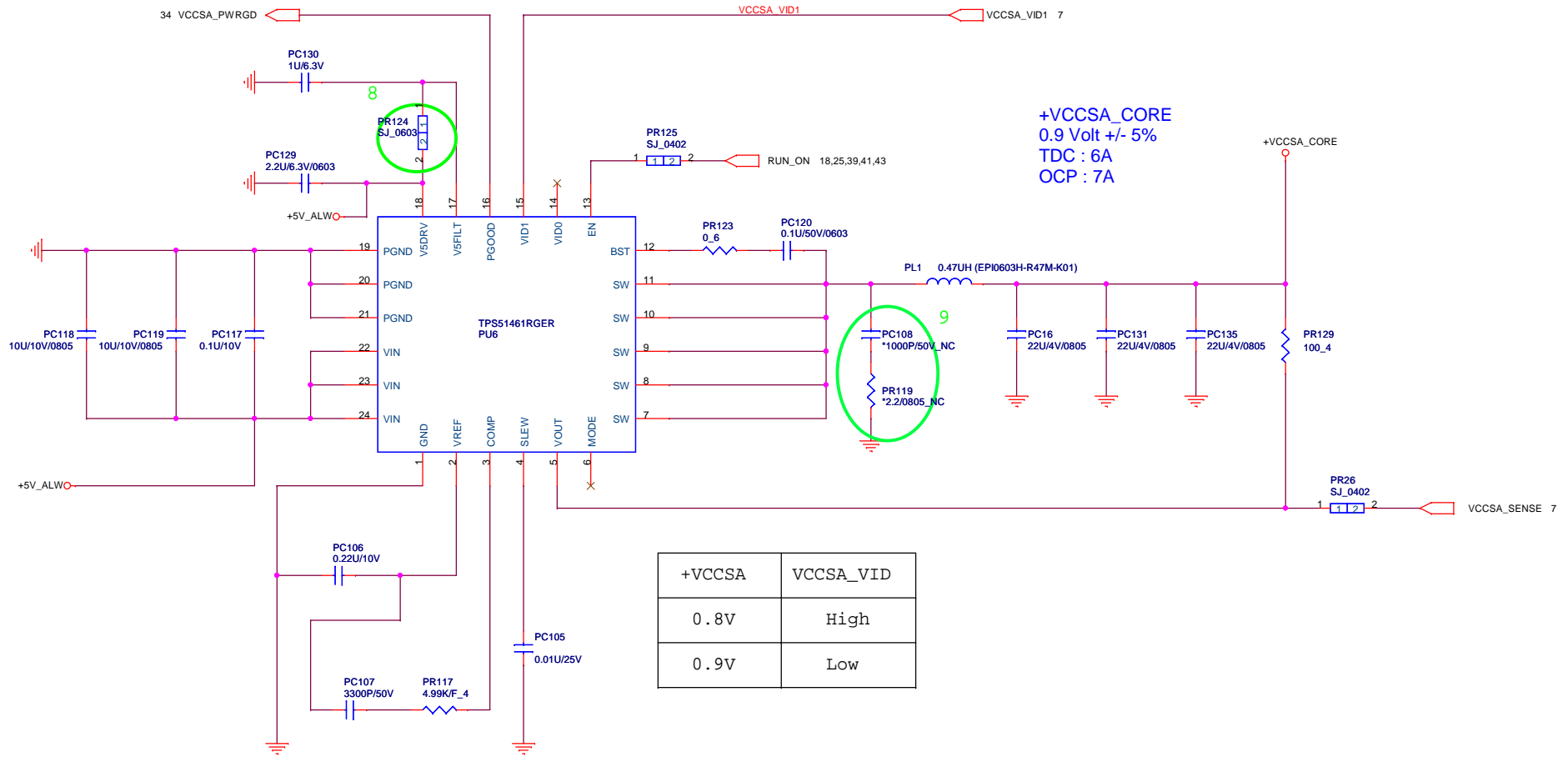
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

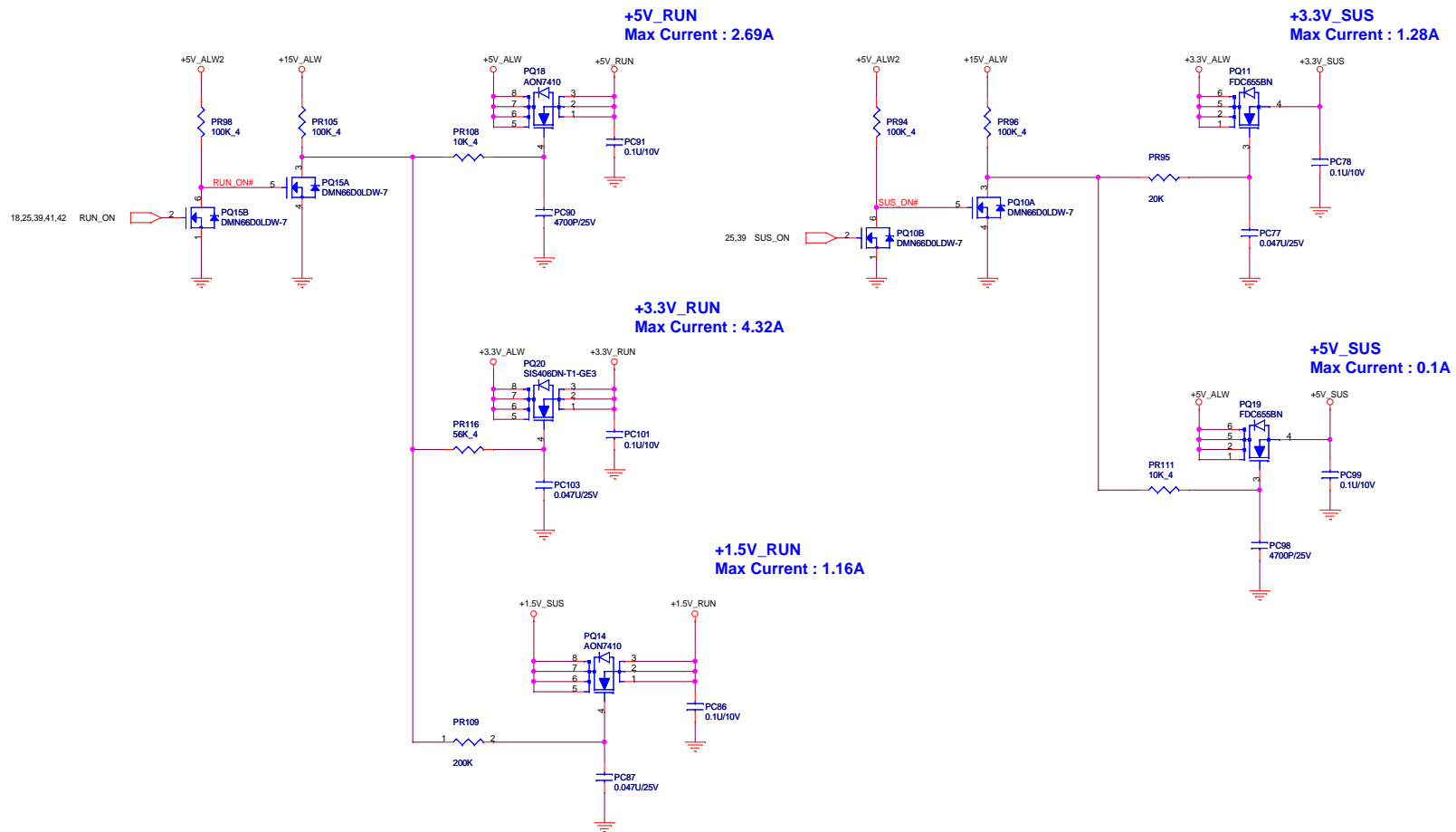
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

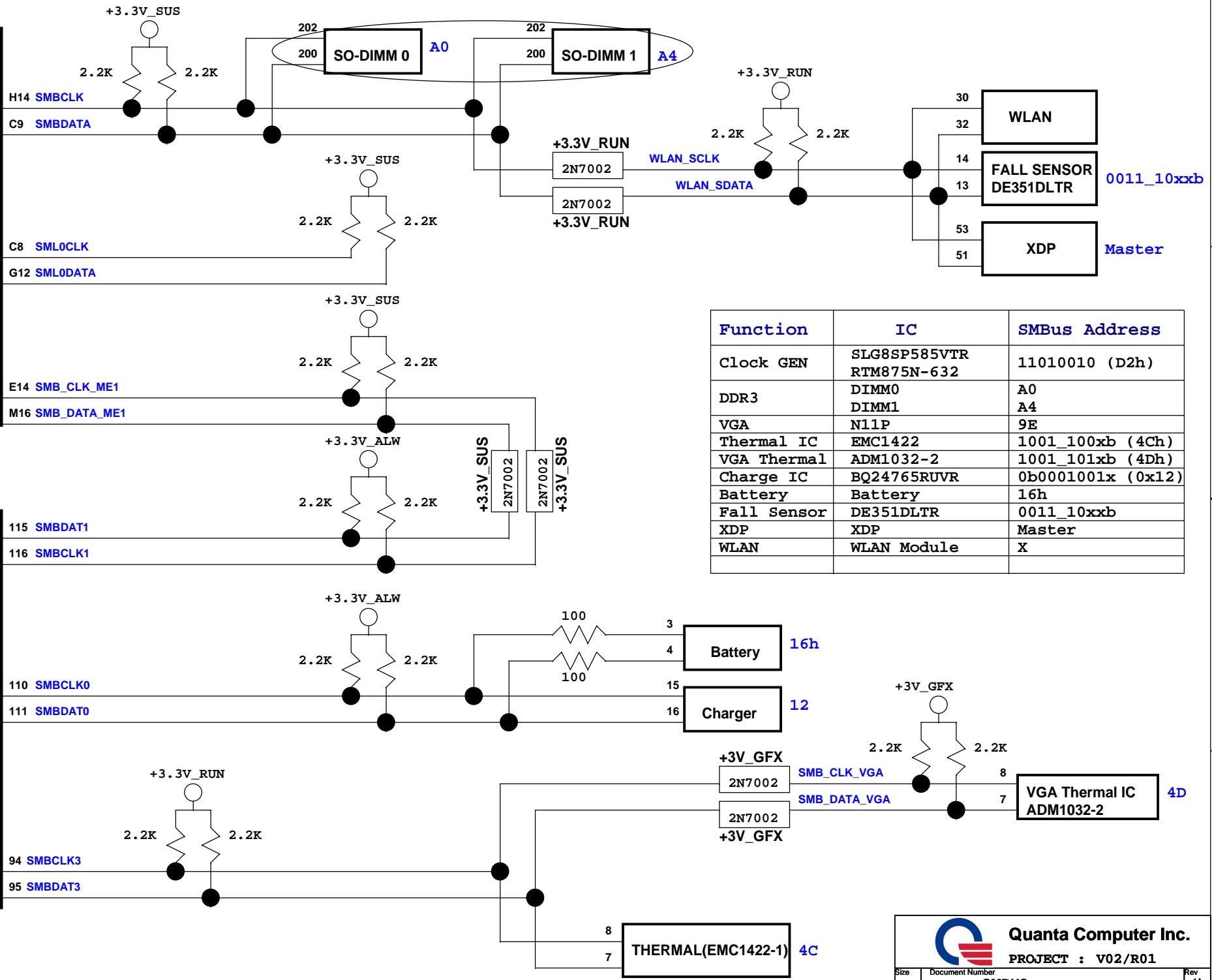
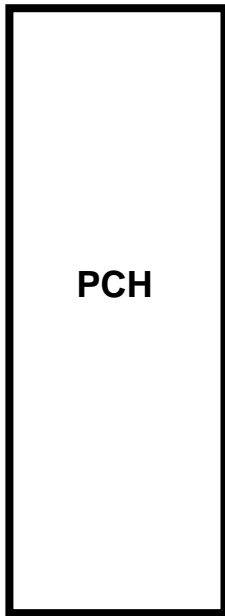




+VCCSA_CORE
 0.9 Volt +/- 5%
 TDC : 6A
 OCP : 7A

+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low





Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001_100xb (4Ch)
VGA Thermal	ADM1032-2	1001_101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X