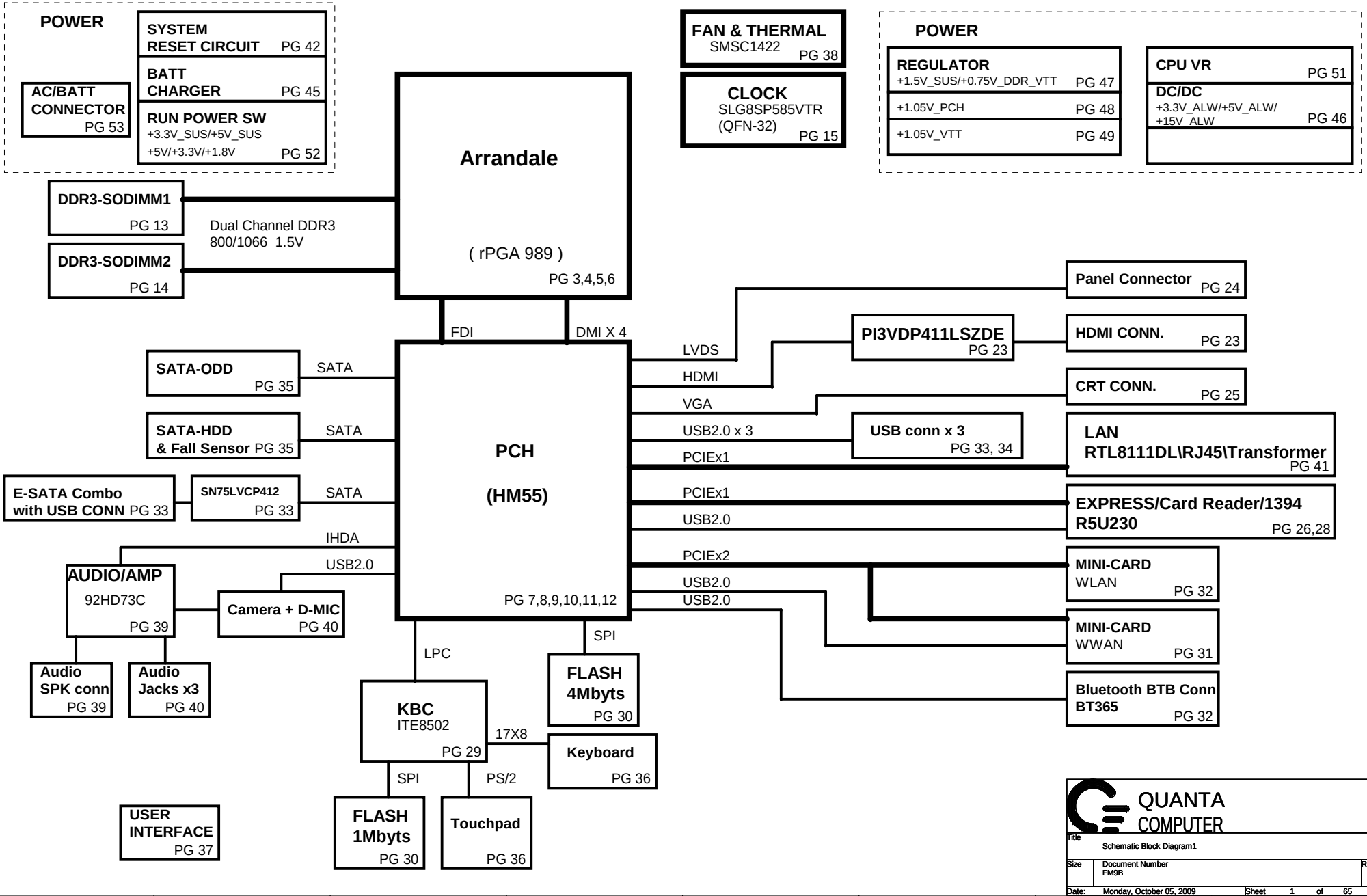
FM9B HANKS Intel UMA

VER : 3A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power State

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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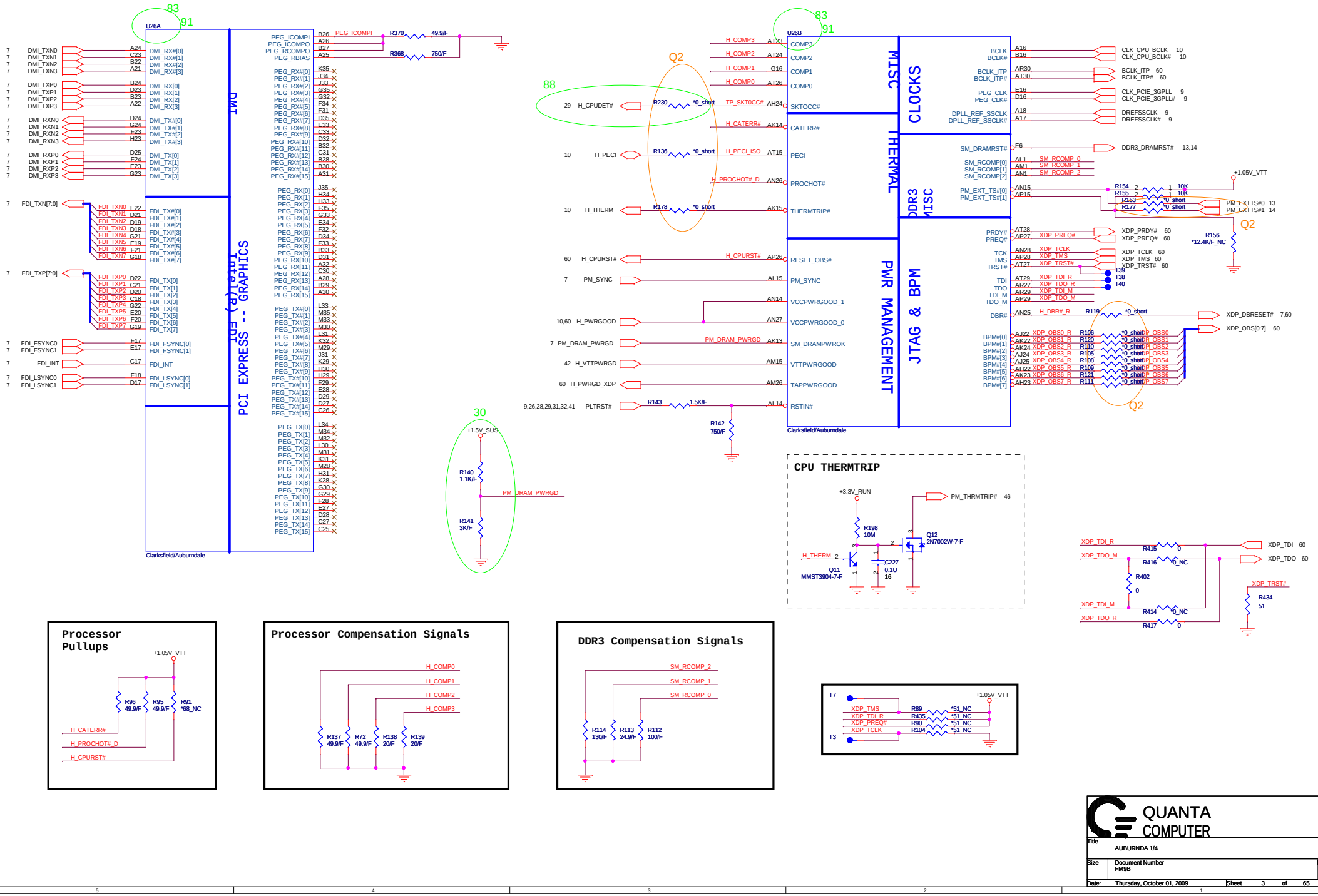
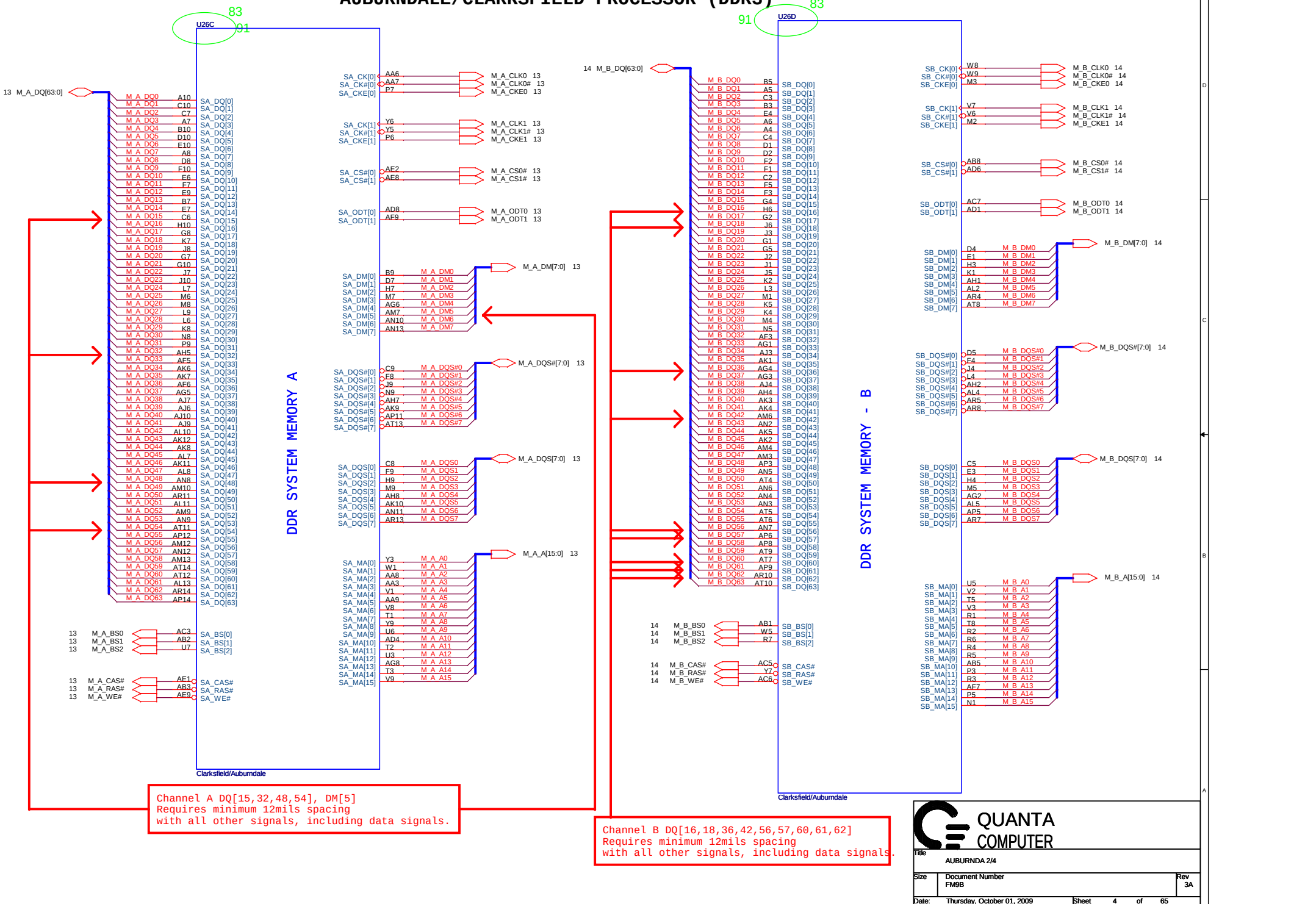


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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CPU Core Power

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

U26F

U26G

Clarksfield/Auburndale

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

1.8V

PEG & DMI

VTT0_43,VTT0_44:
CRB(V1.0)P13
Why add 0ohm?? Is it trace width control??

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality. The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

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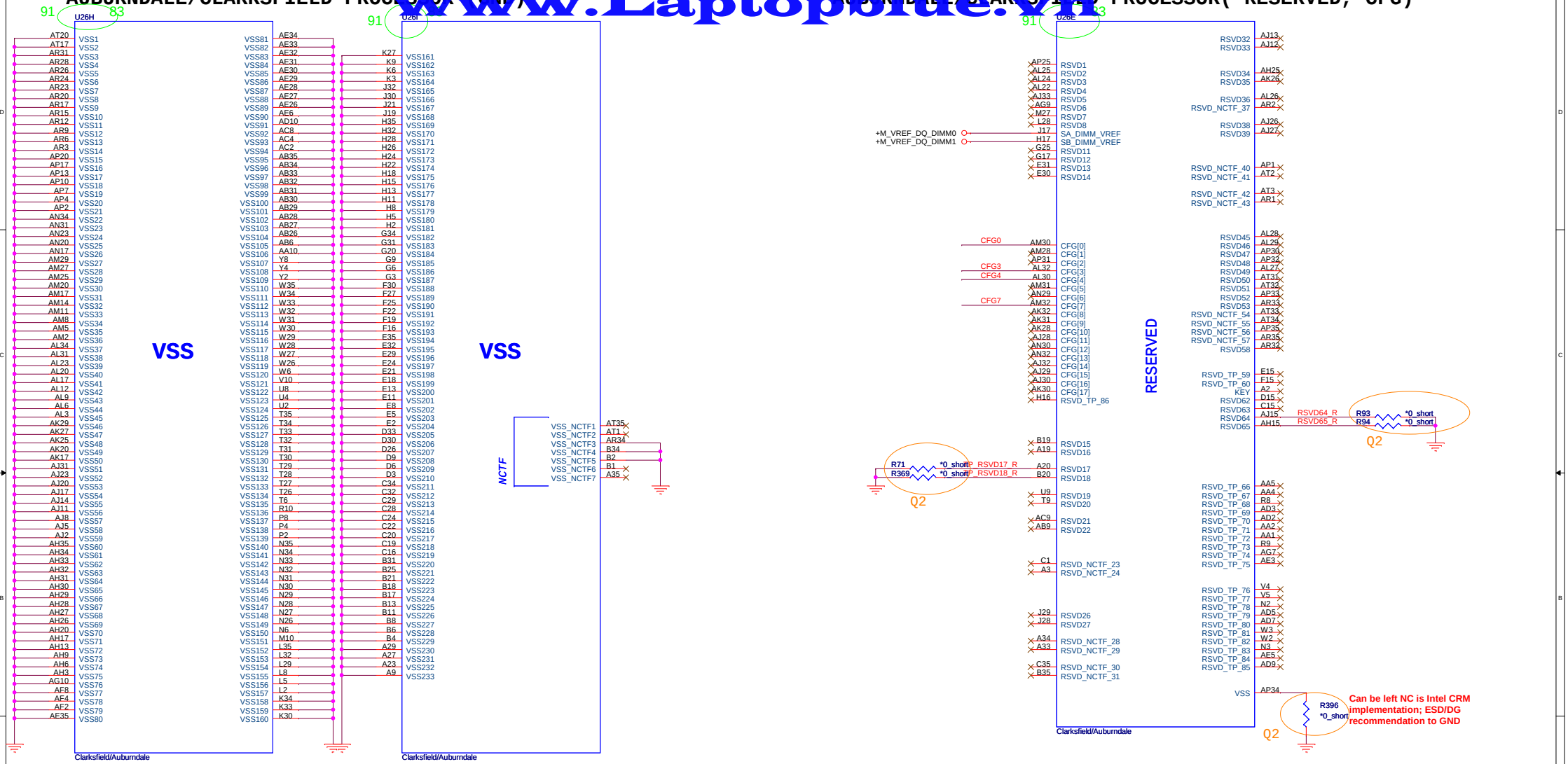
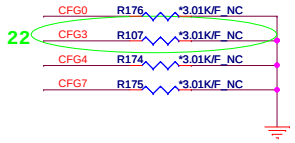
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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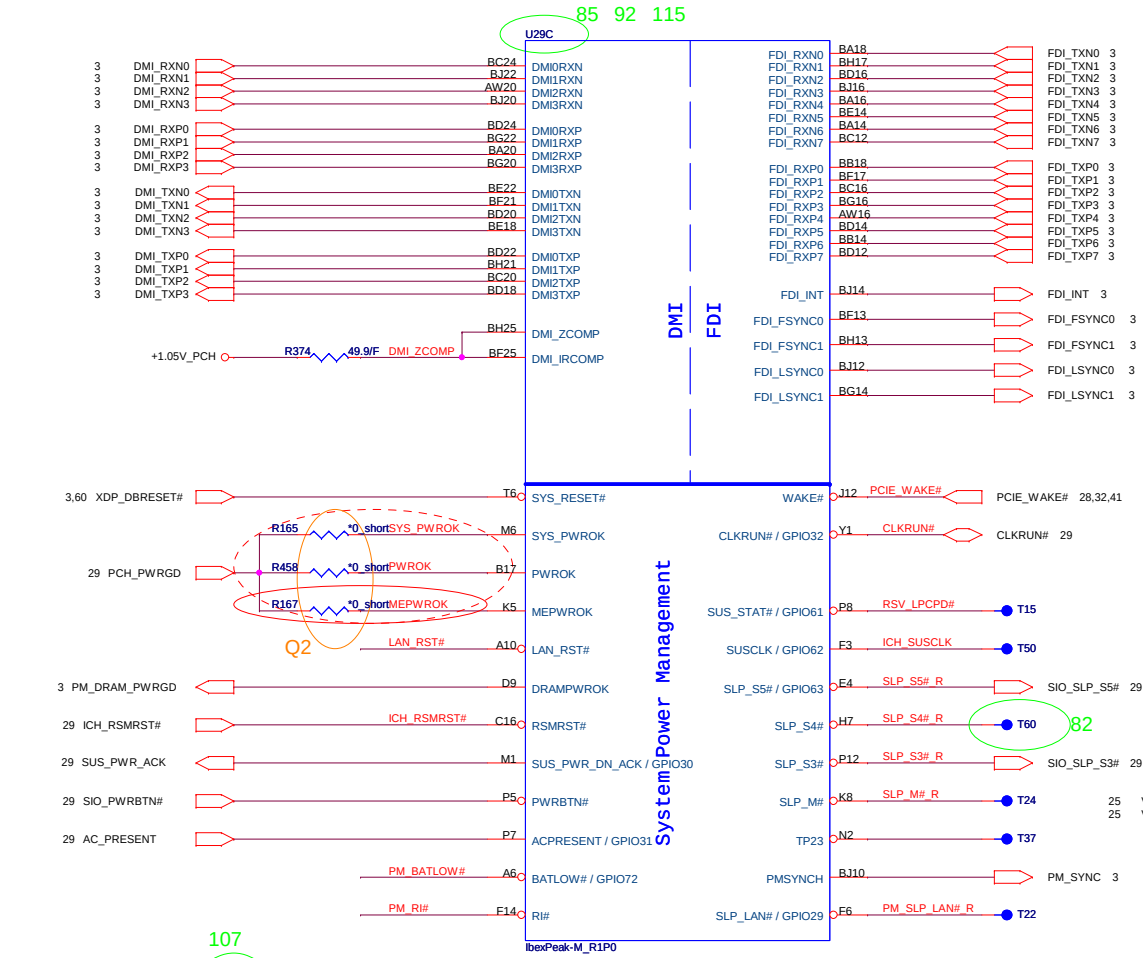
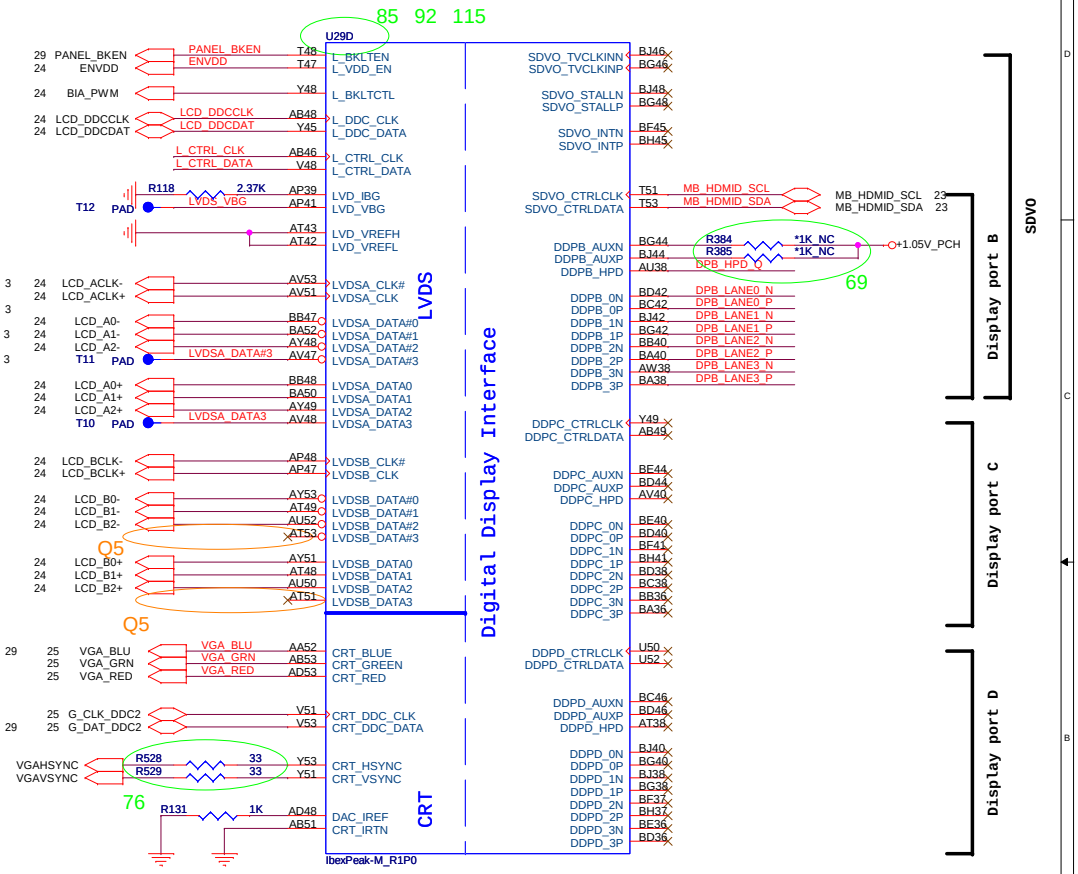
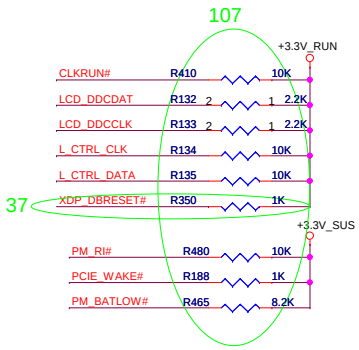
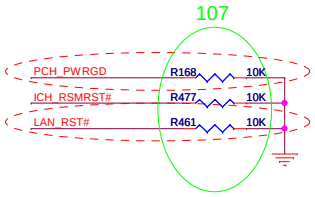
IBEX PEAK-M (DMI,FDI,GPIO)

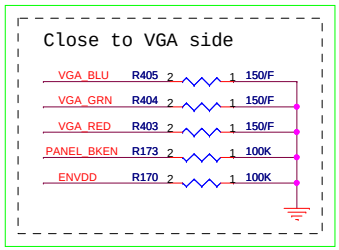


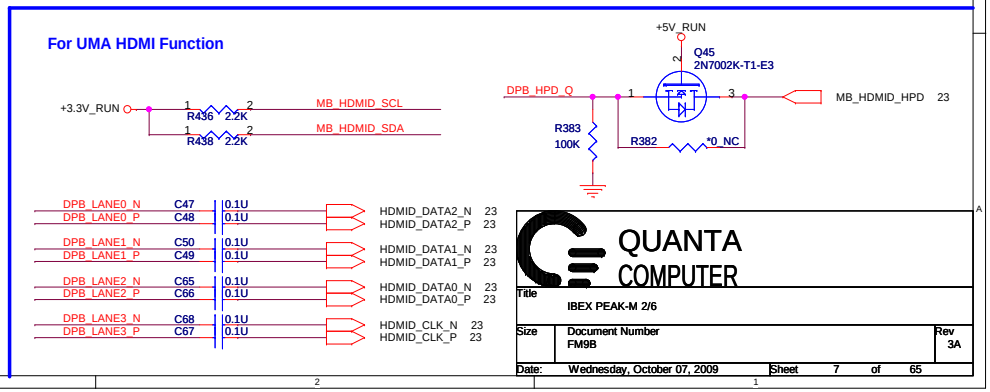
IBEX PEAK-M (LVDS,DDI)











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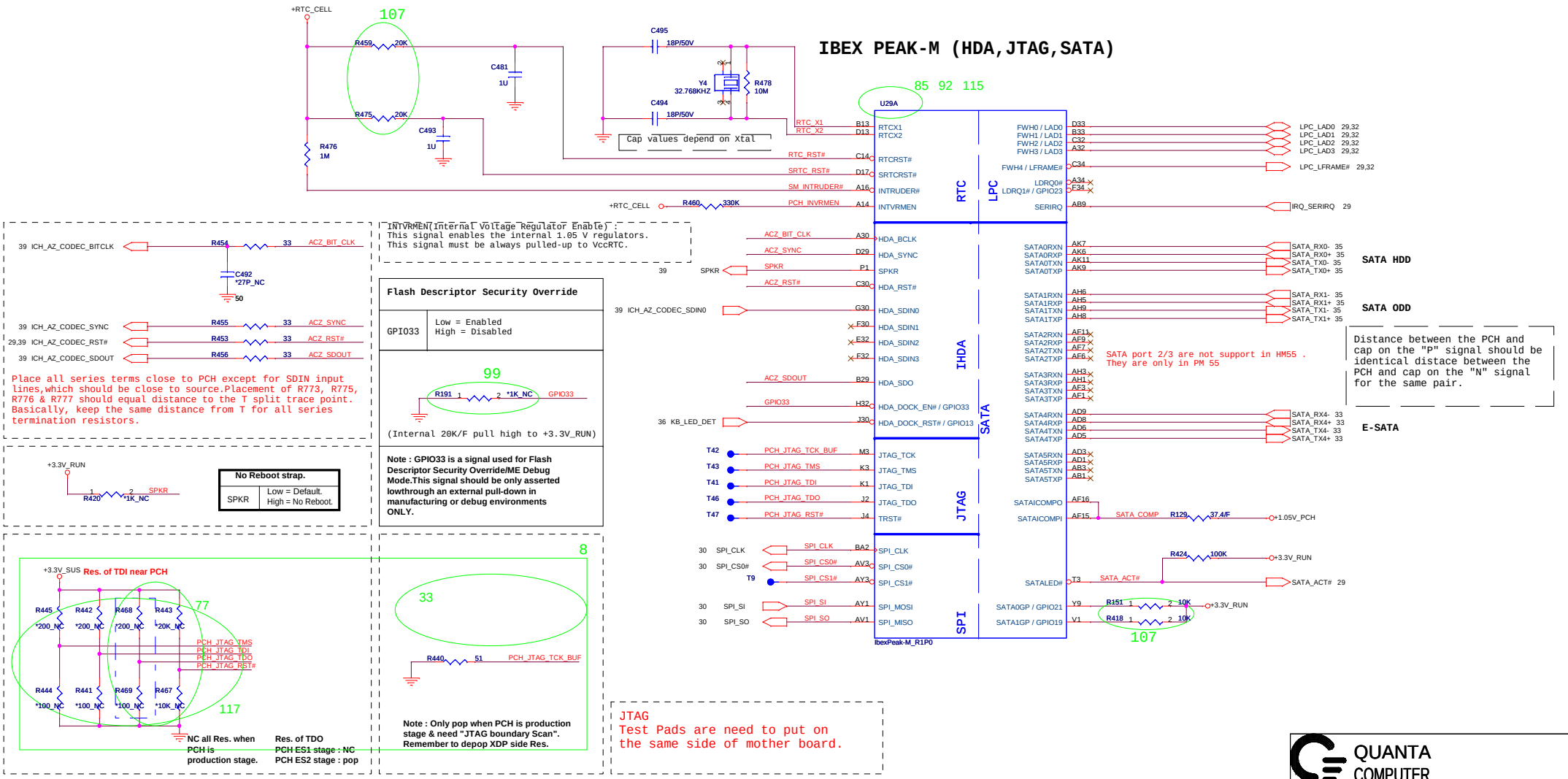
IBEX PEAK-M (HDA,JTAG,SATA)



39 ICH_AZ_CODEC_BITCLK — R454 33 — ACZ_BIT_CLK
C492 *27P_NC
39 ICH_AZ_CODEC_SYNC — R455 33 — ACZ_SYNC
29,39 ICH_AZ_CODEC_RST# — R453 33 — ACZ_RST#
39 ICH_AZ_CODEC_SDOUT — R456 33 — ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled

99
R191 1 2 *1K_NC GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

+3.3V_RUN
R420 1 2 *1K_NC SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

+3.3V_SUS Res. of TDI near PCH
R445 *200_NC
R442 *200_NC
R468 *200_NC
R443 20K_NC
77
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R444 *100_NC
R441 *100_NC
R469 *100_NC
R467 *10K_NC
117

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

8
33
R440 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

JTAG
Test Pads are need to put on the same side of mother board.

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

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Title	IBEX PEAK-M 1/6	
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U29E

PCI

NVRAM

USB

Left Side pair Top

Left Side pair bottom

Right Side pair top (Cable)

Mini Card (WLAN)

Mini Card (WWAN)

Mini Card (WPAN)

Express Card

Camera

Touch Screen Module

Note : place these resistors near to PCIe Slots

USB port 6/7 are not support in HM55
They are only in PM 55

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend (single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214

Pin	Default Port Mapping
OC0#	Port0,Port1
OC1#	Port2,Port3

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

Place TX DC blocking caps close PCH.

MiniWWAN

MiniWLAN

Express Card

Card Reader

Giga Bit LOM

PCI-E port 7/8 are not support in HM55 .
They are only in PM 55

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

DG(V1.1) P256: XTAL_OUT and XTAL_IN are the signal names for the PHY.
Intel feedback:
Fully-Integrated Clocking is a stretch goal for Calpella platforma nd maybe enabled in ES2 Si. Recommend customers to have 25-MHz crystal as a BOM stuff option.

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)

CLKOUTFLEX3 EDS(V1.0) :support 48MHz 33MHz and 14.31818MHz.

25MHz Clock for DCI Function

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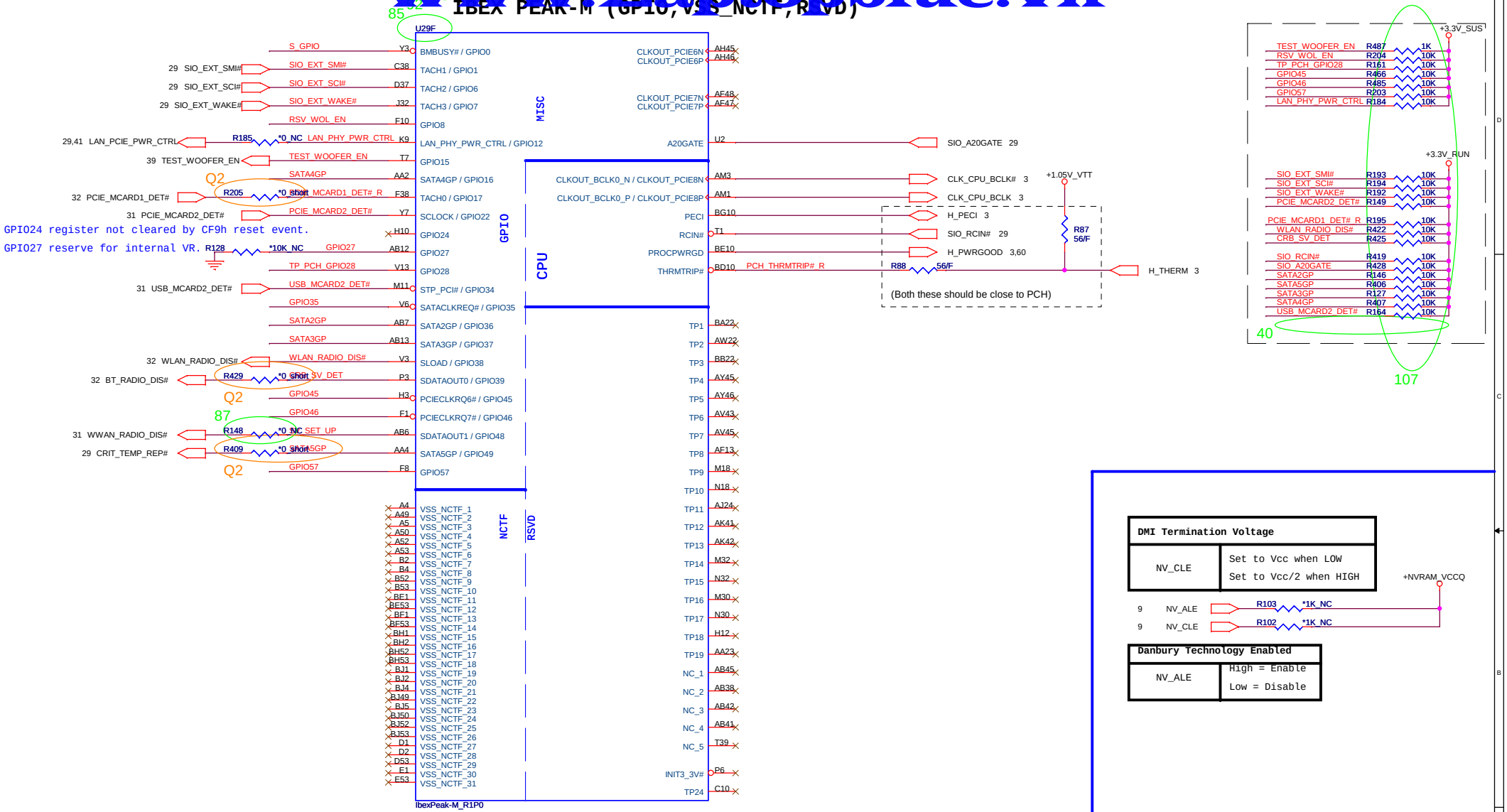
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

9 NV_ALE R103 *1K_NC

9 NV_CLE R102 *1K_NC

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

107 R150 10K GPIO35 R437 *1K_NC GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

34 R186 *1K_NC RSV_WOL_EN

Integrated Clock Chip Enable

(Reserve to validate for future platforms)

RSV_WOL_EN	Enable when sampled low Disable when sampled high

107 +3.3V_RUN S_GPIO R408 10K SV_SET_UP R147 10K

6

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

SV_SET_UP	1-X High = Strong (Default)

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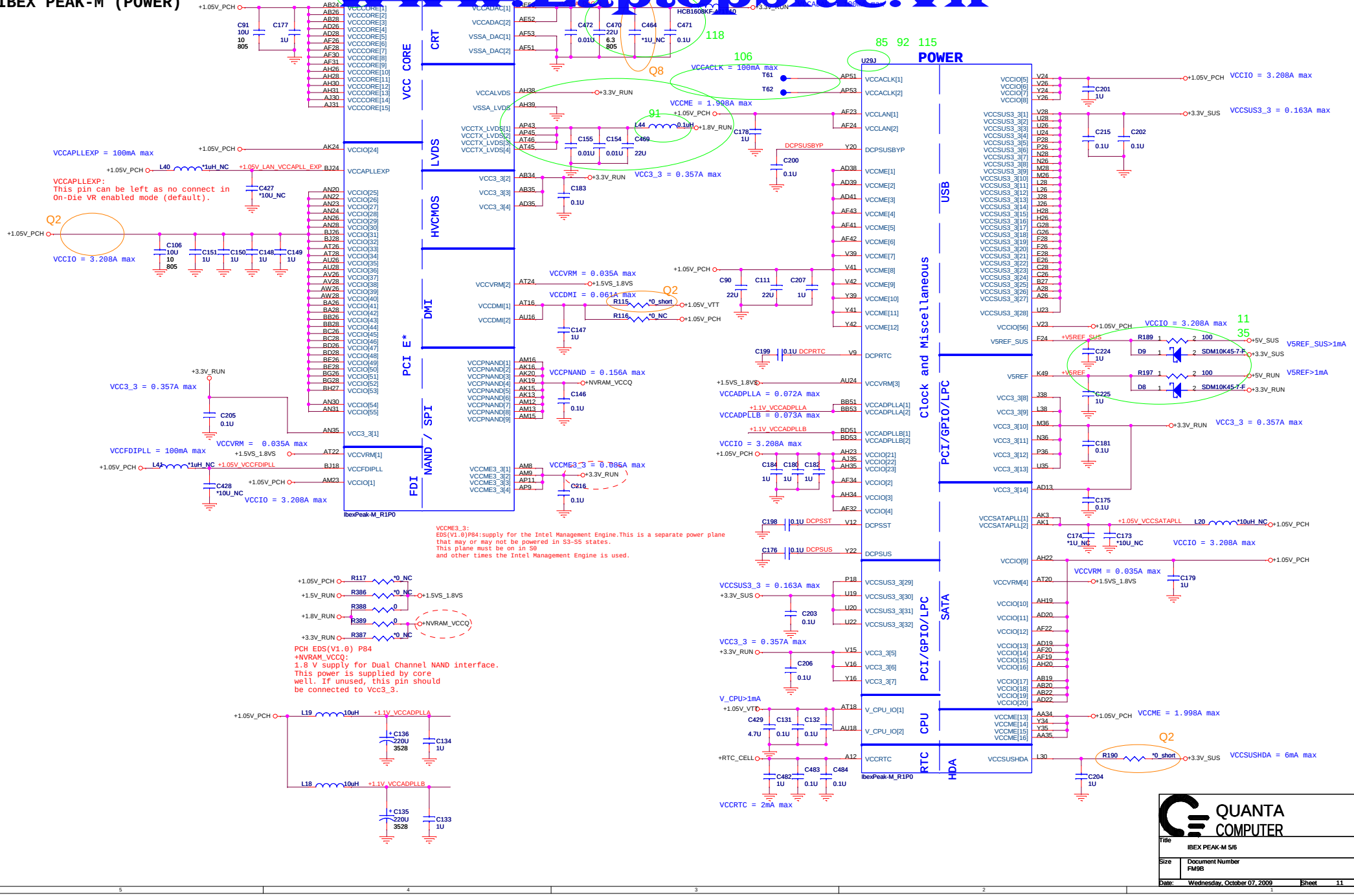
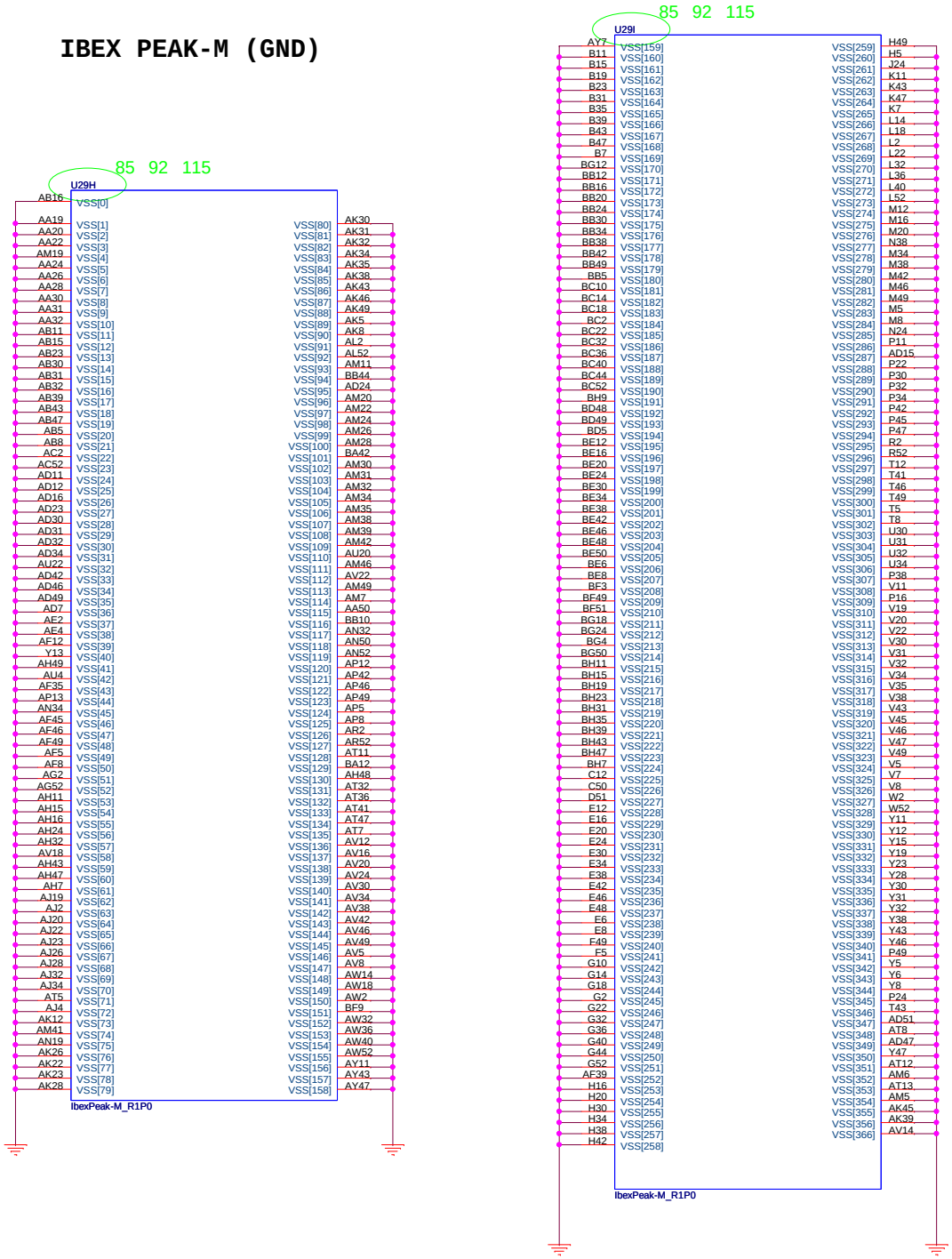
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)



QUANTA COMPUTER

Title	IBEX PEAK-M 6/6	
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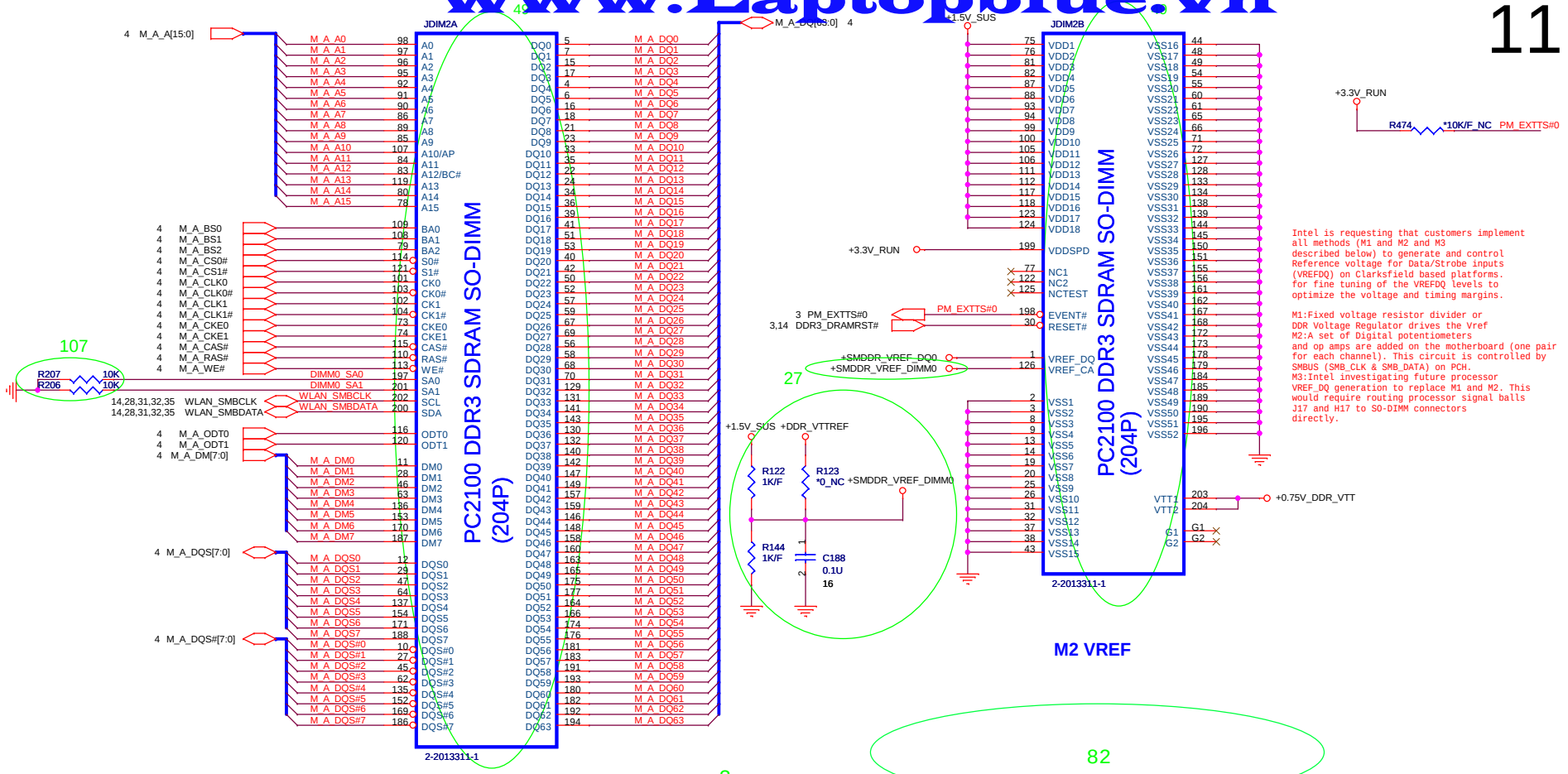
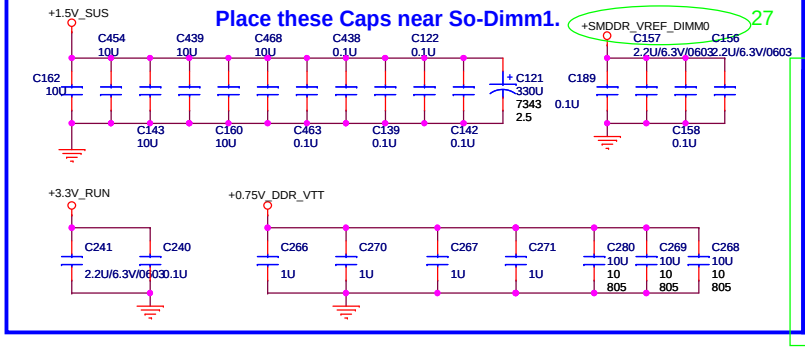
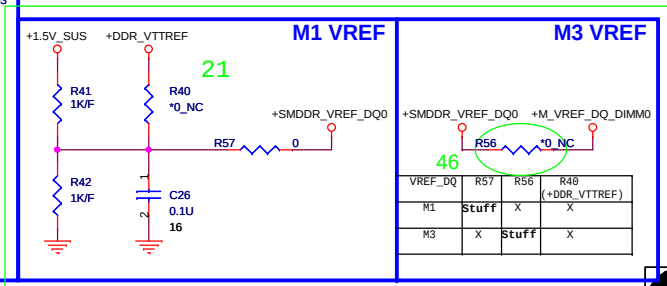


Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.

Place these Caps near So-Dimm1.





VREF_DQ	R57	R56	R40 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

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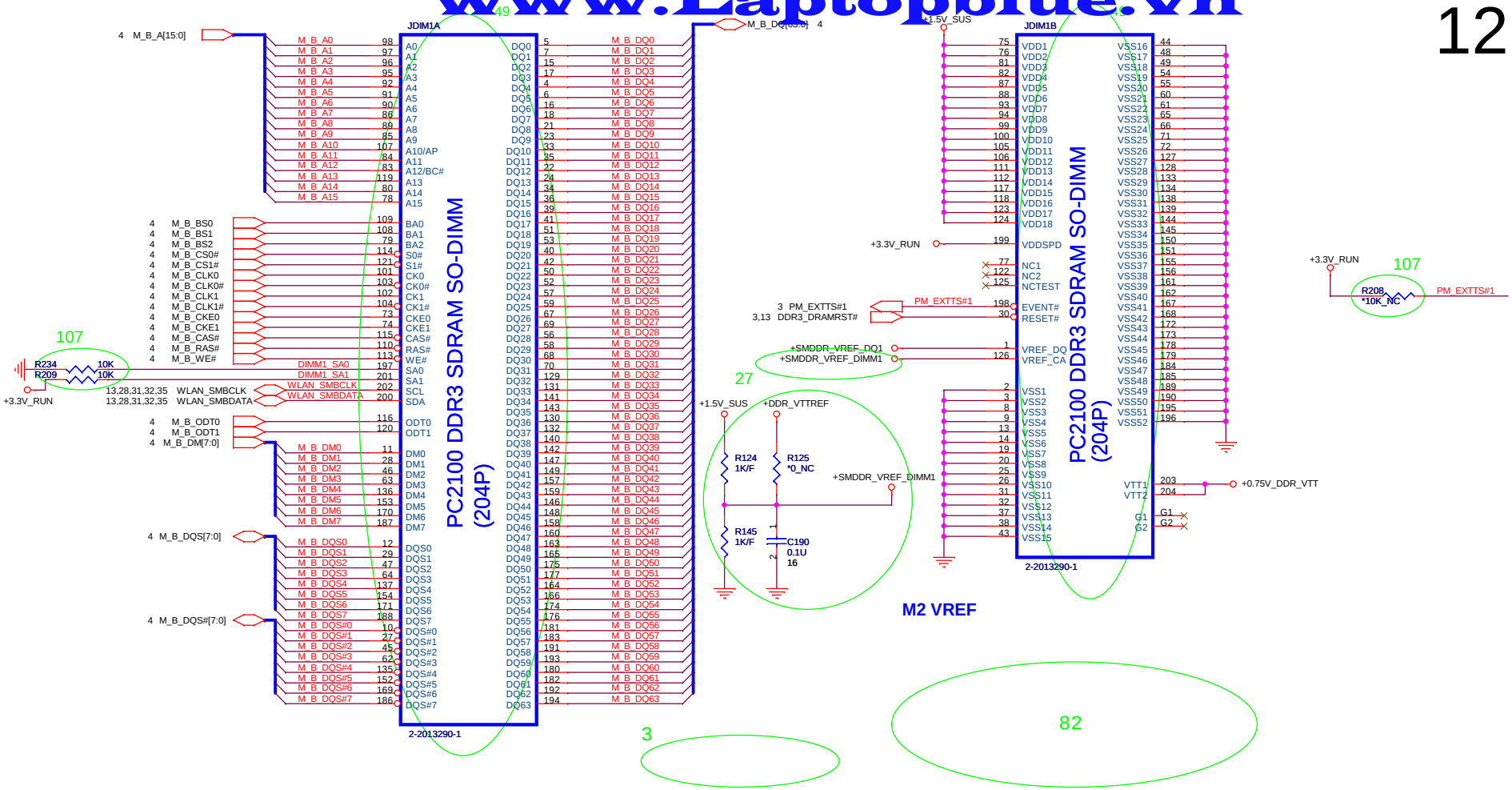

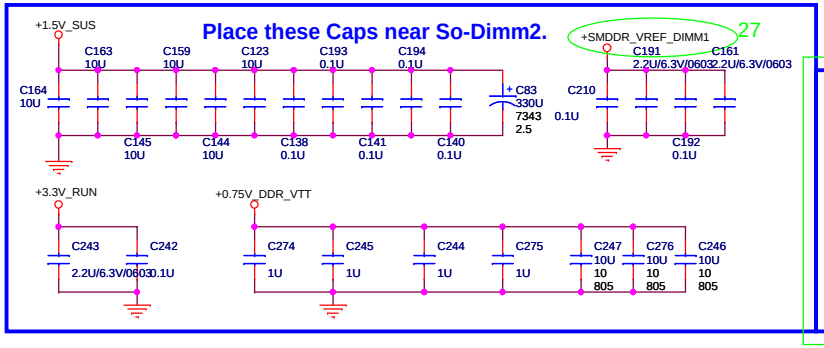

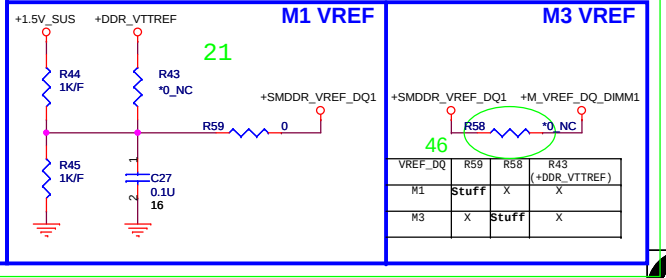

VREF_DQ	R59	R58	R43 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

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Title	DDR3 DIMM-1	
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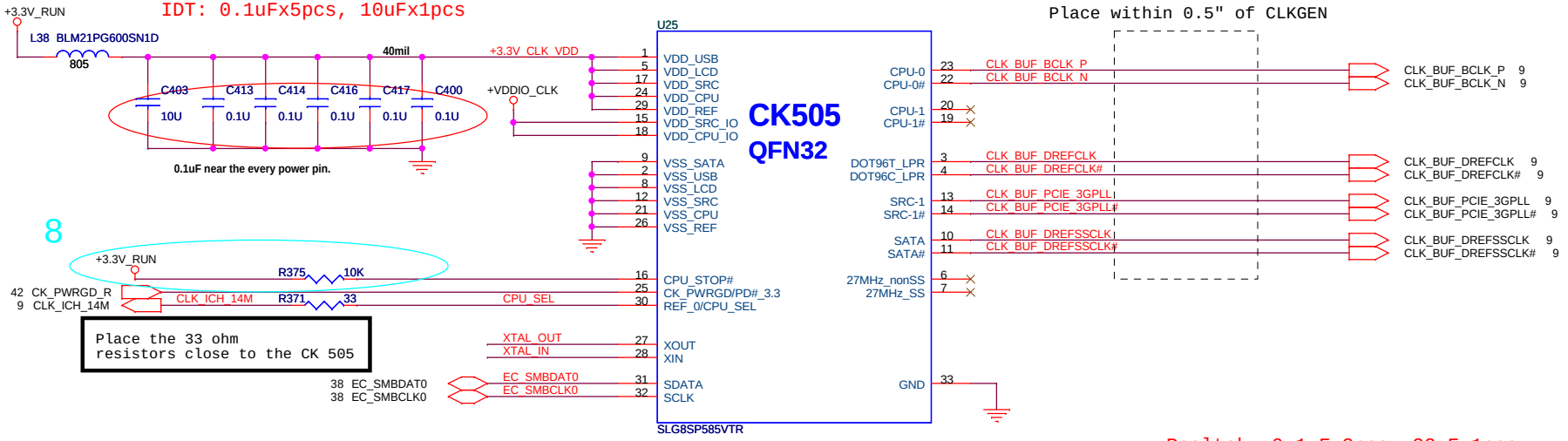
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

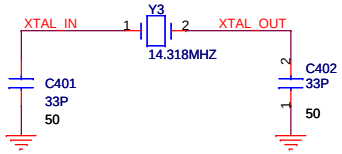
Place within 0.5" of CLKGEN



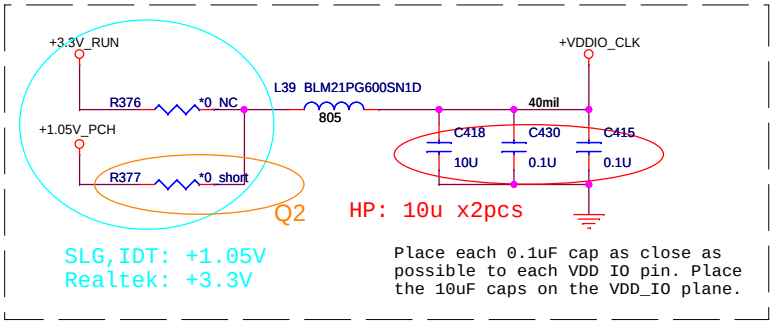
8

Place the 33 ohm resistors close to the CK 505

Add capacitor pads for improving WWAN.



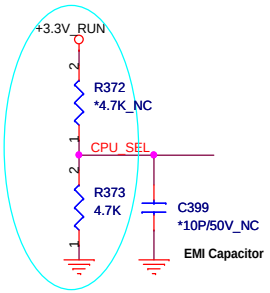
Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

7



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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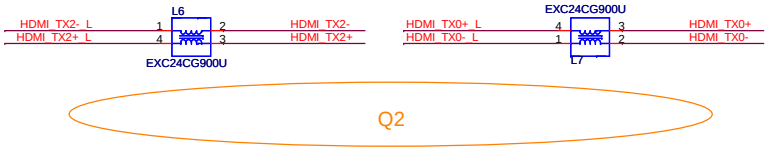
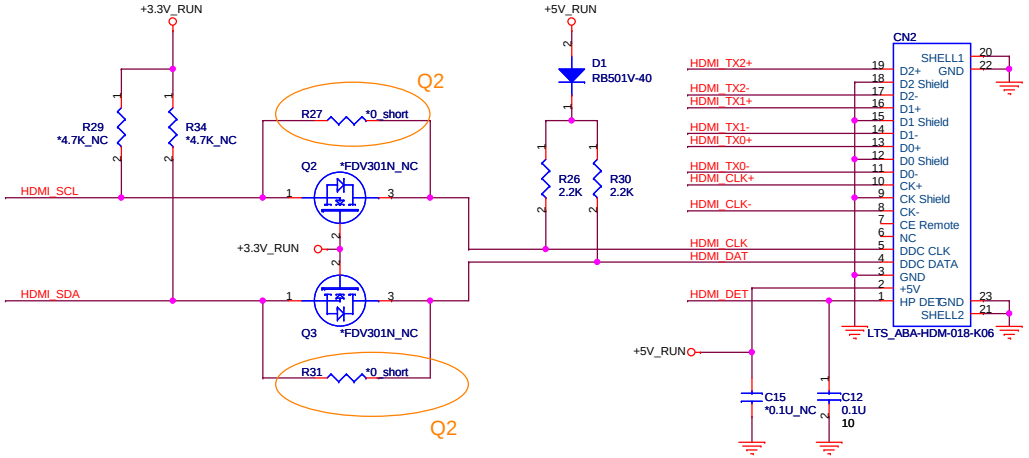
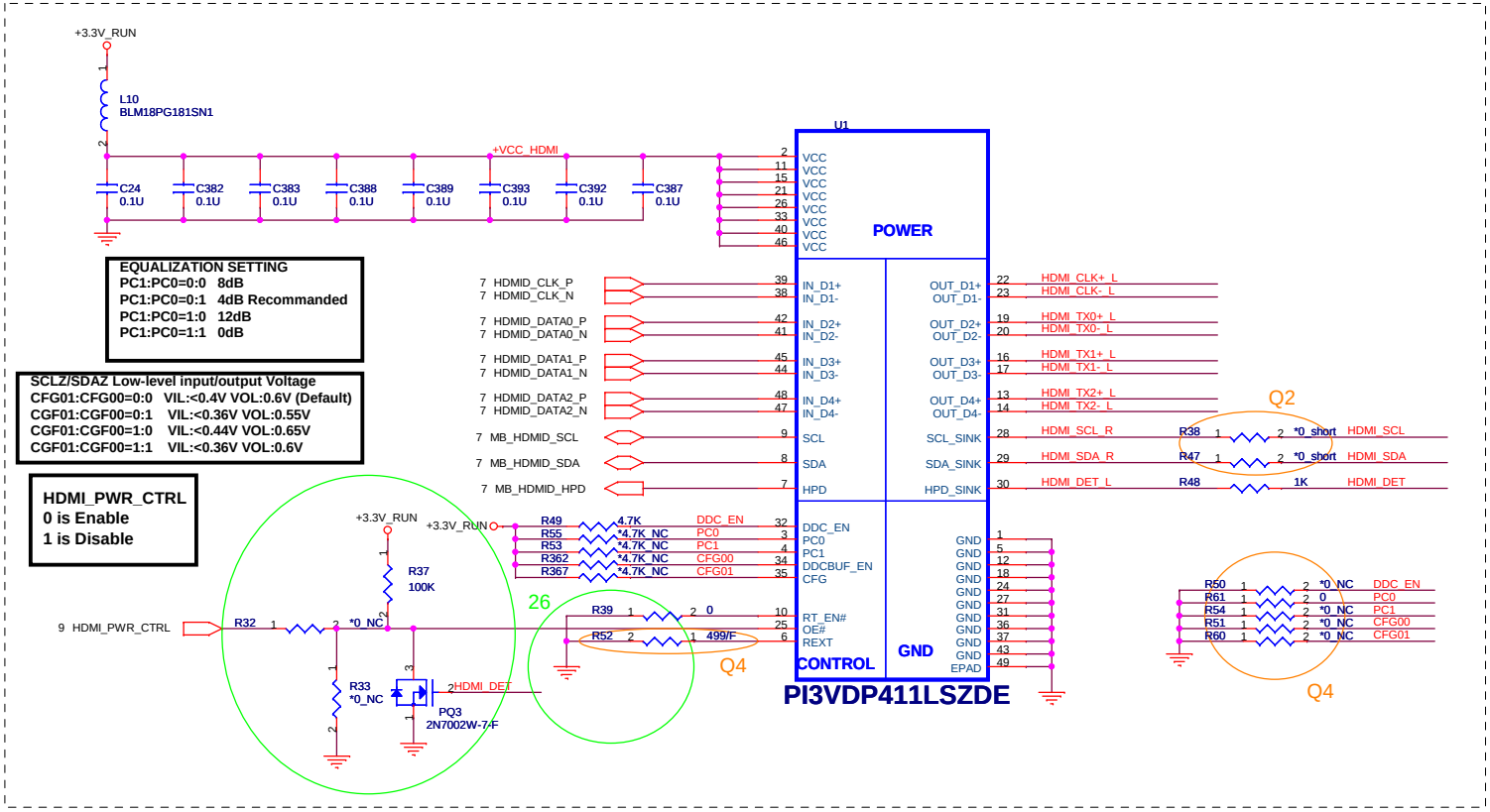
HDMI



Reserve for EMI and close to HDMI CONN





QUANTA COMPUTER			
Title	VGA-M82-S (PCIe)		
Size	Document Number FM9B		Rev 3A
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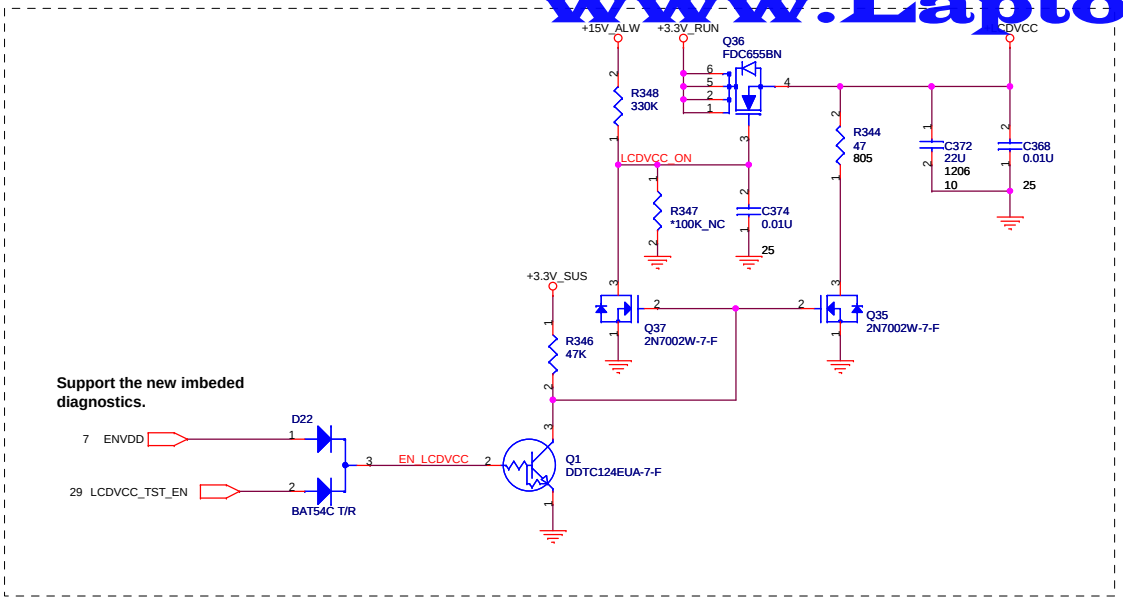
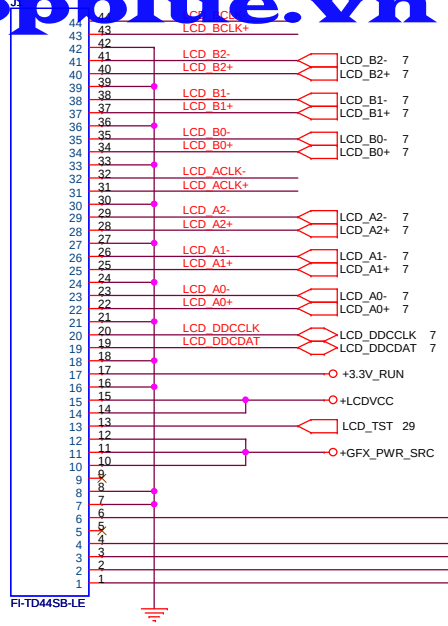
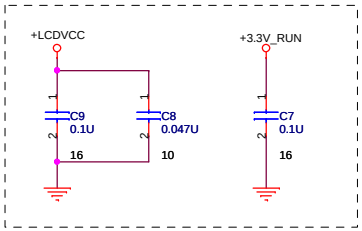
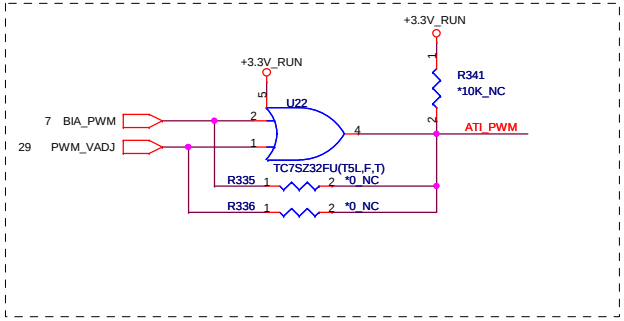


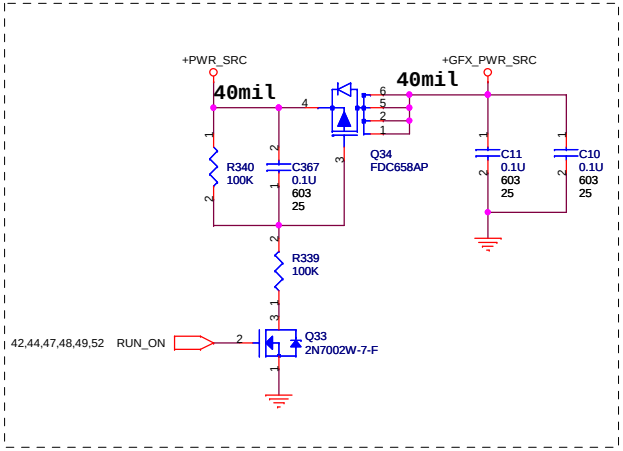




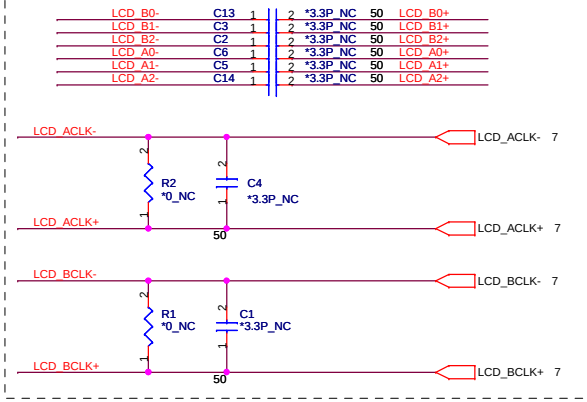
Adress : A9H --Contrast
AAH --Backlight

LCD_CONTRAST 29
INVERTER_CBL_DET# 29
LCD_BAK# 29
ATI_PWM
LCD_CBL_DET# 29





Shunt capacitors on LVDS for improving WWAN.



QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number FM9B	Rev 3A
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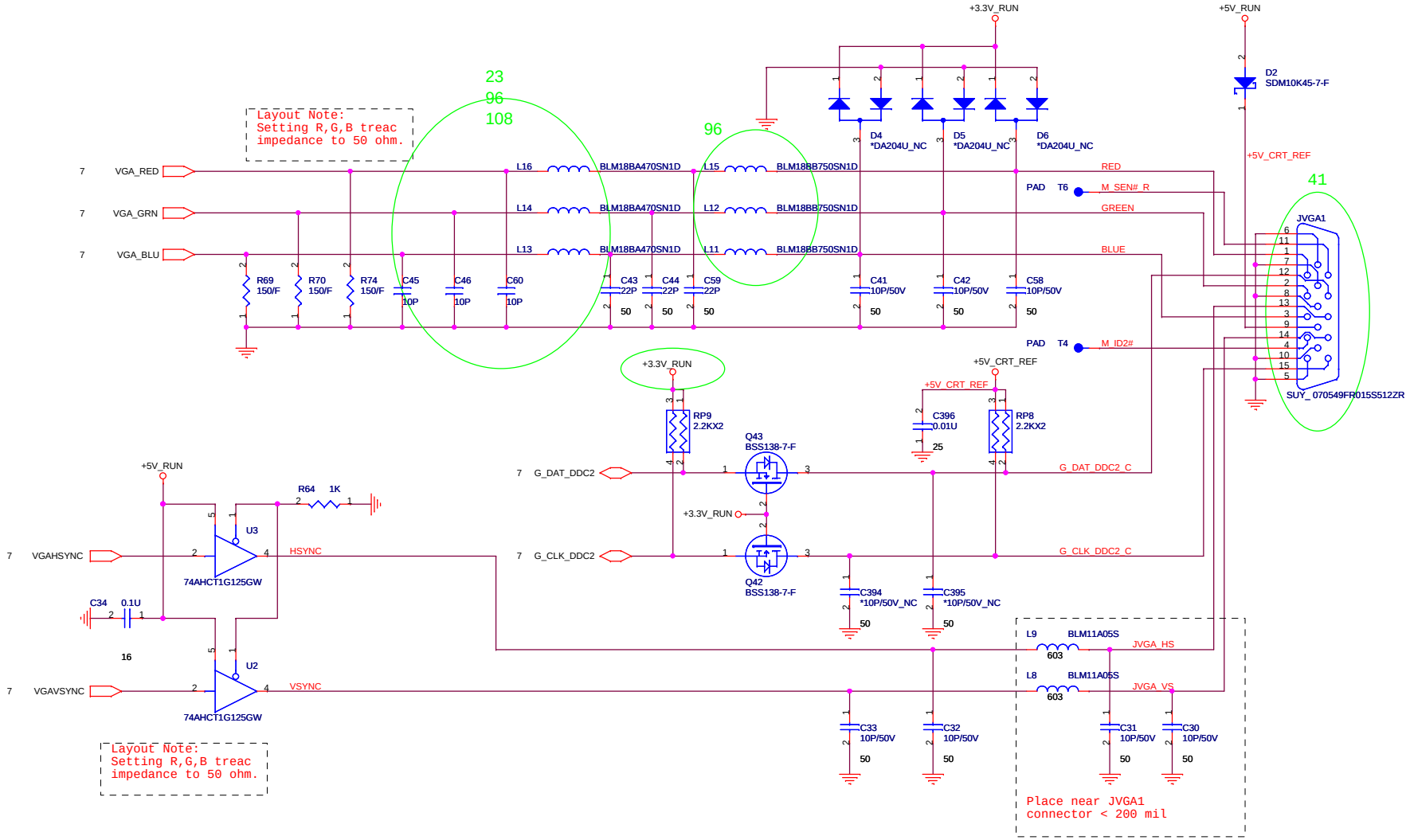

QUANTA COMPUTER

Title	CRT&TV CONN	
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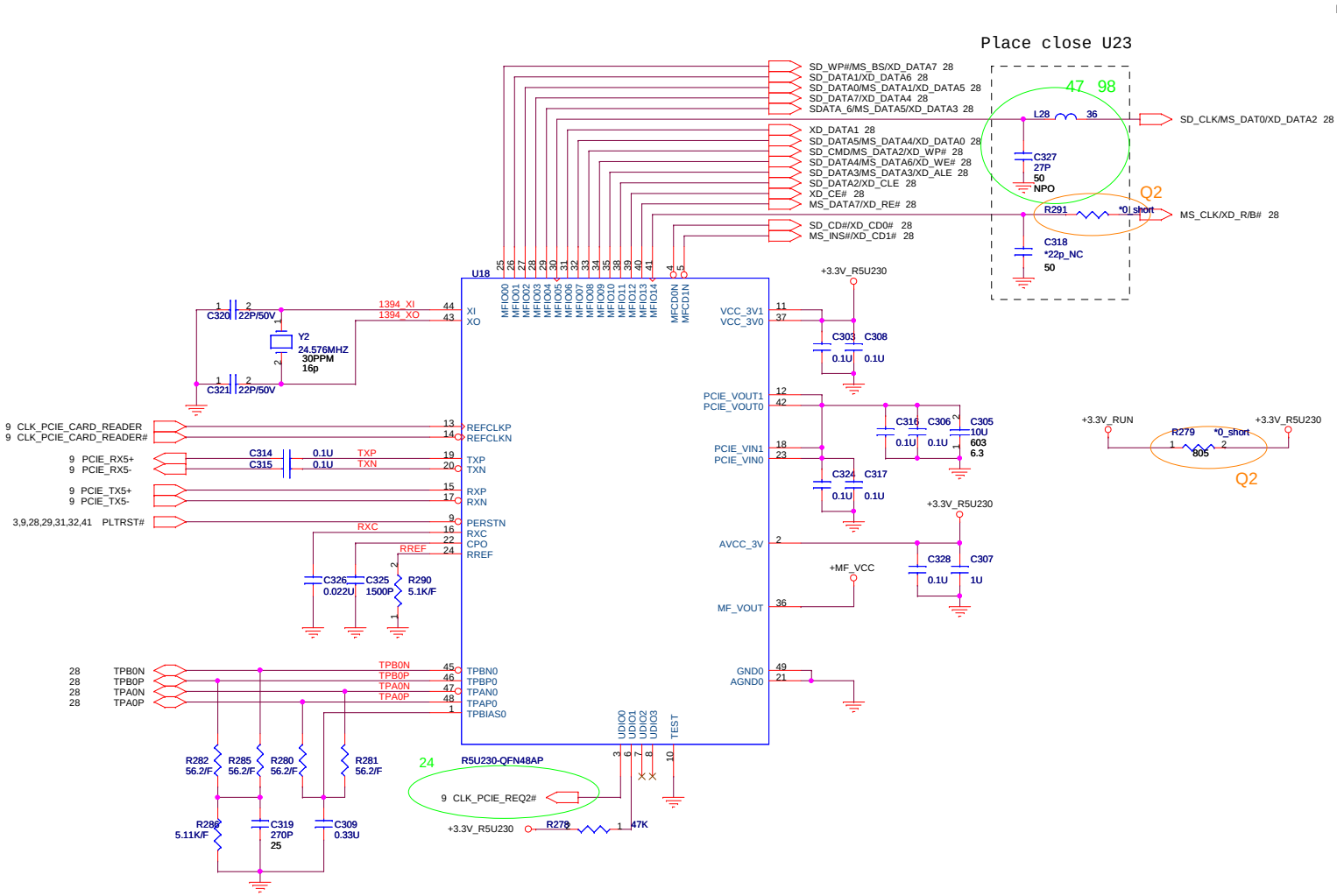

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
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QUANTA COMPUTER

Title	IEEE 1394	
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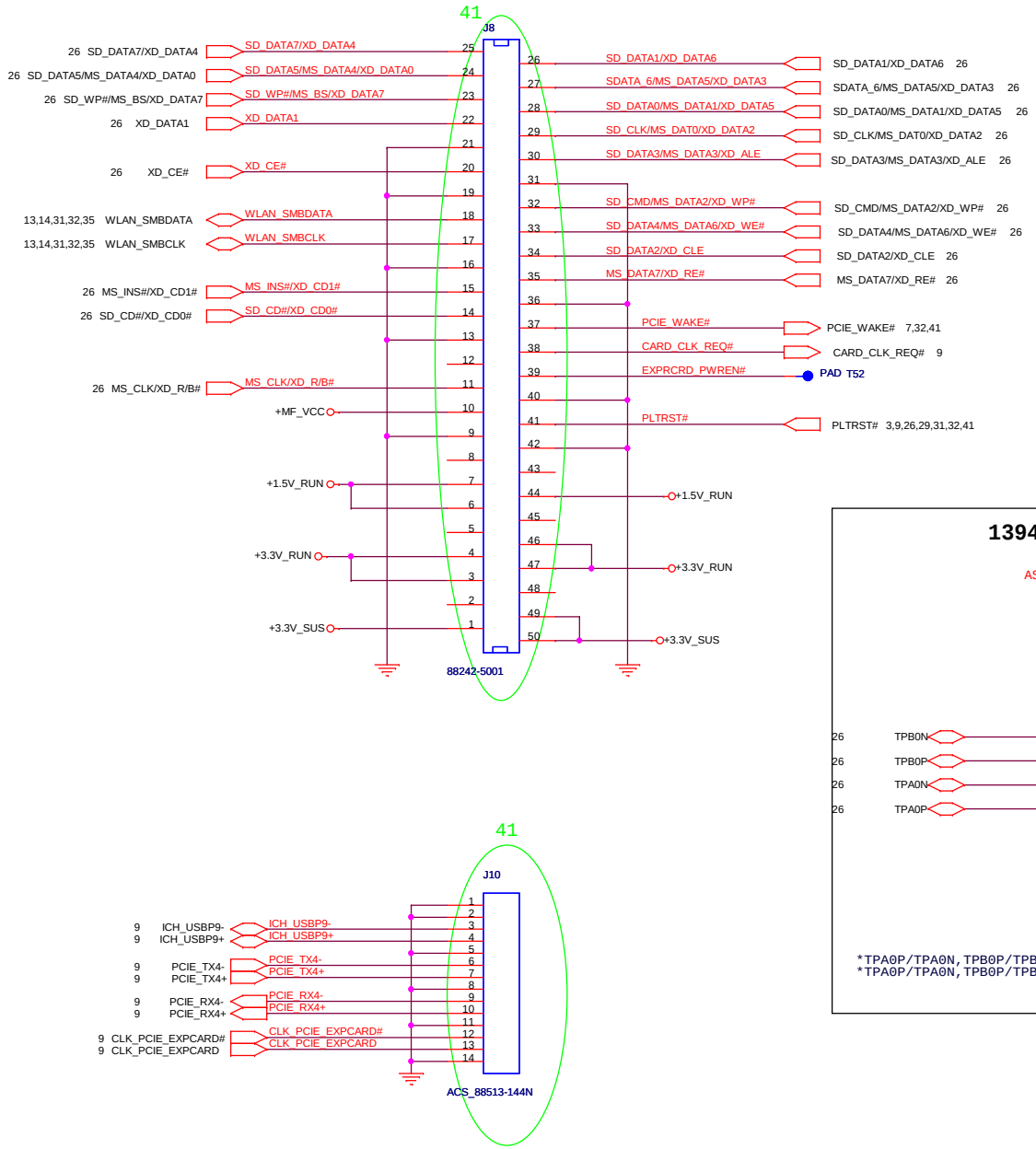
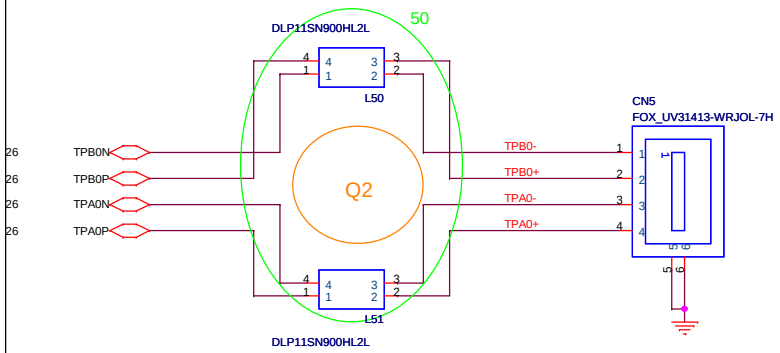
Express Card/CARD READER



1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number FM9B	Rev 3A
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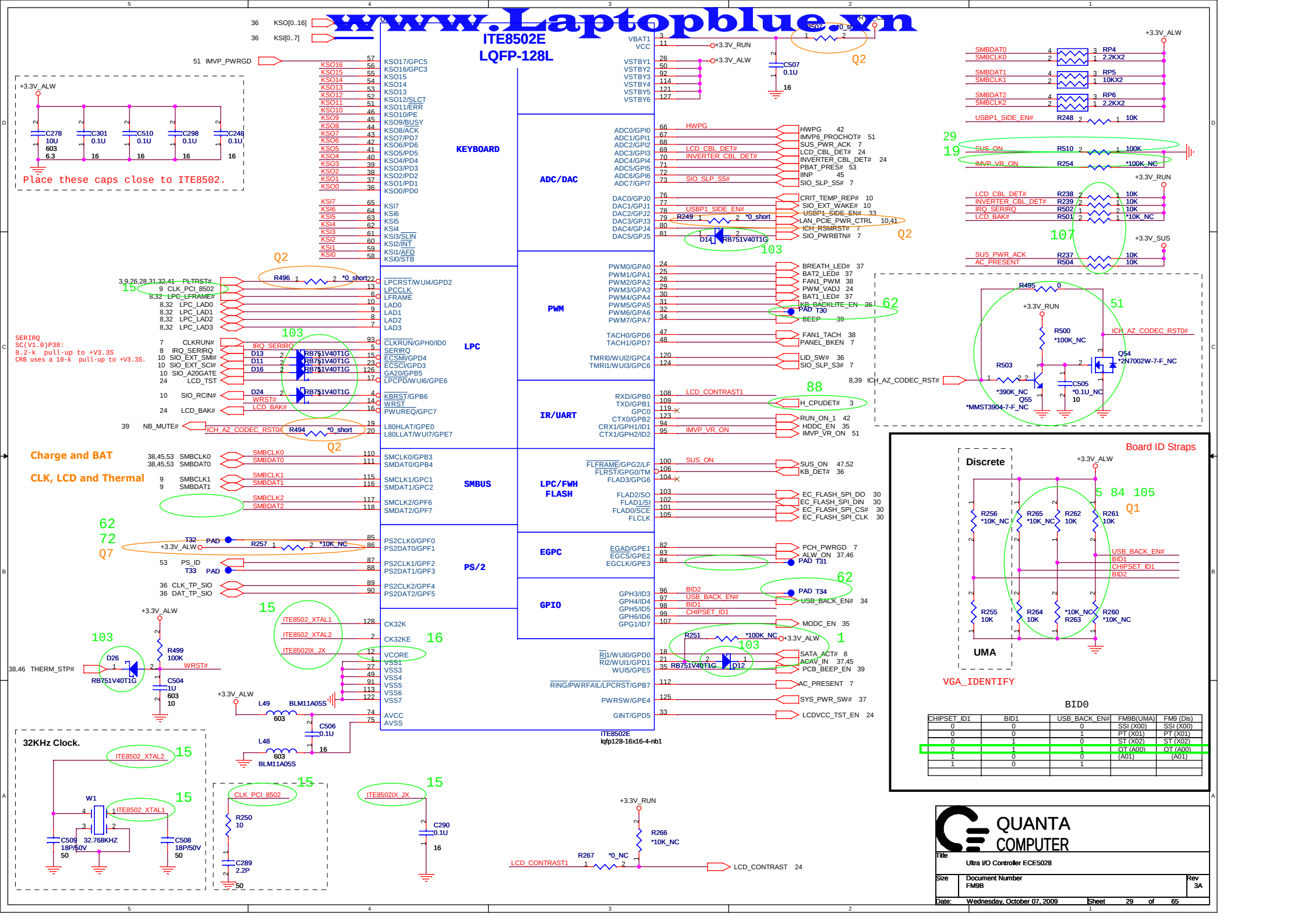
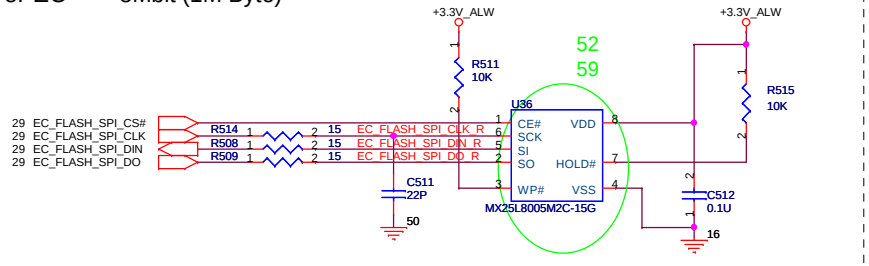
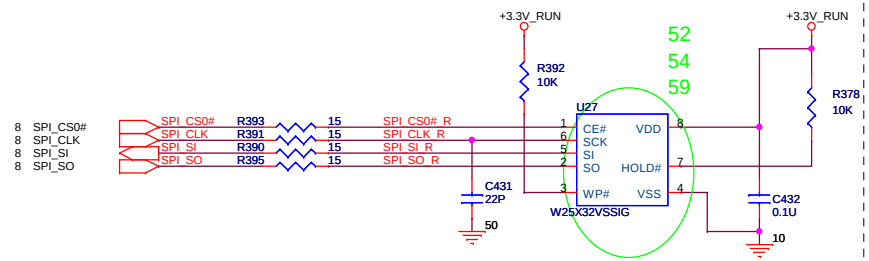


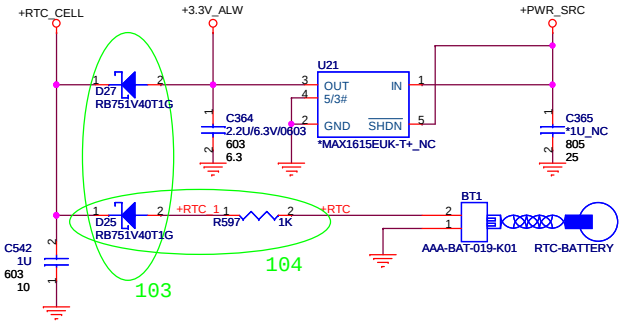
For EC 8Mbit (1M Byte)



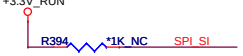
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9B	Rev 3A
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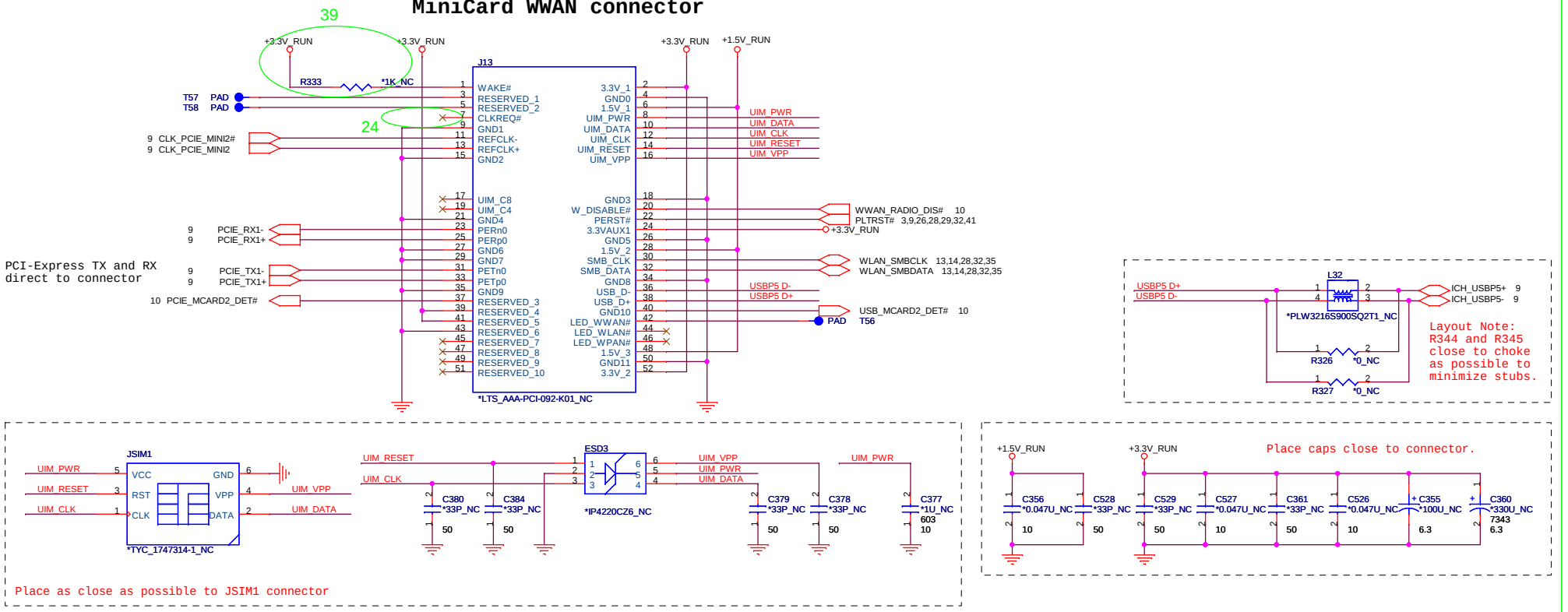
MiniCard WWAN connector



QUANTA COMPUTER

Title	MINI-PCI	
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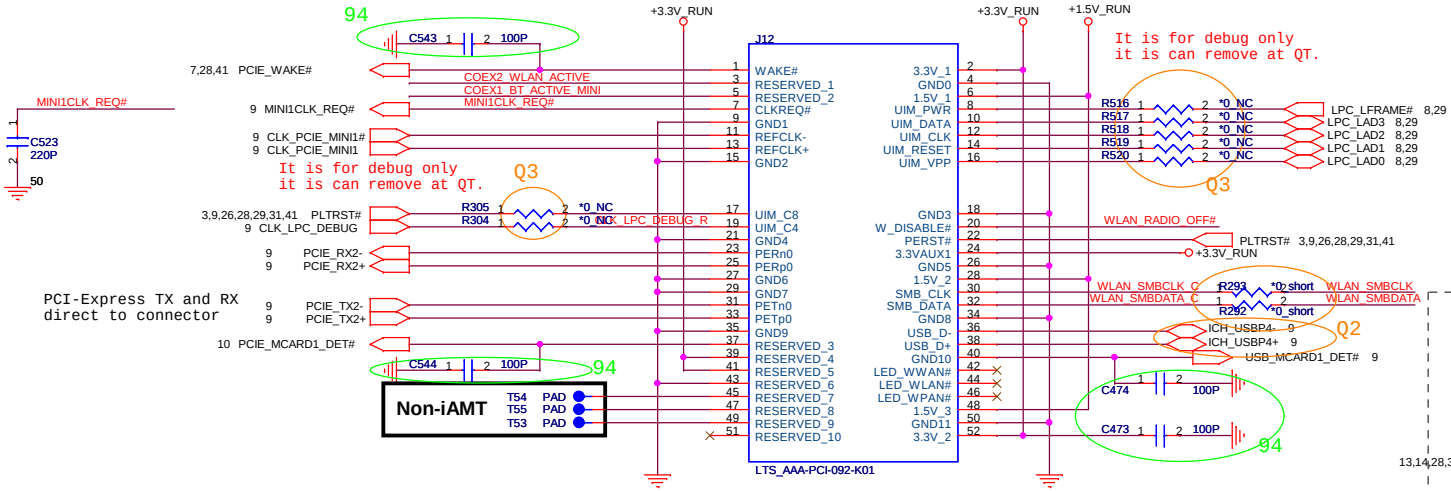
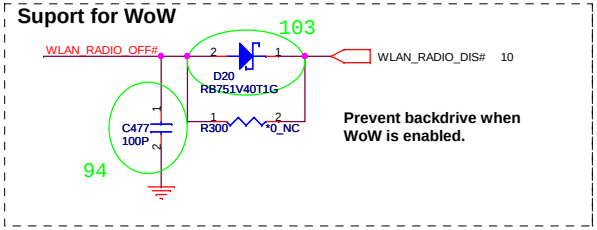
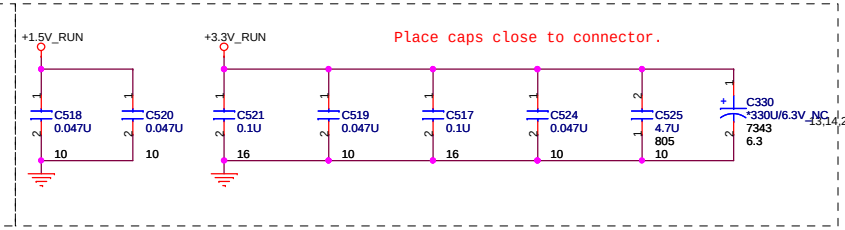
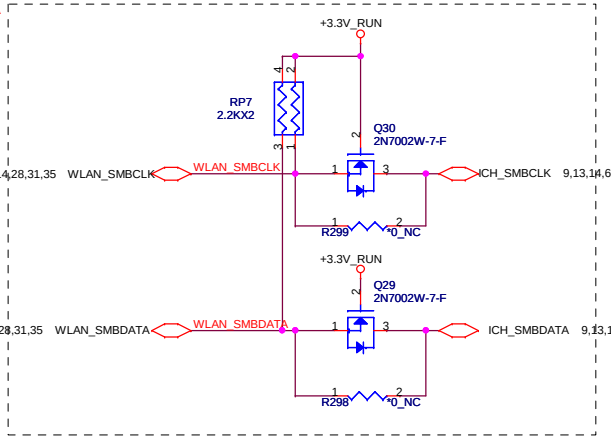
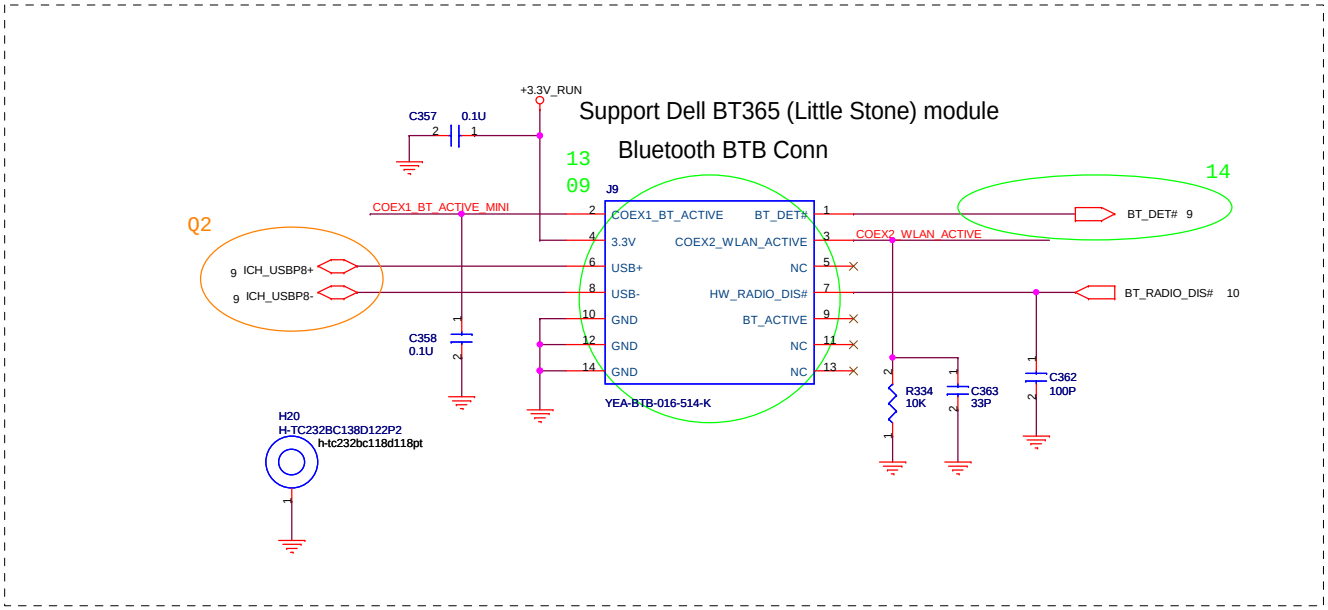
MiniCard WLAN connector











Q2

QUANTA COMPUTER

Title	MDC CONN.	
Size	Document Number FM9B	Rev 3A
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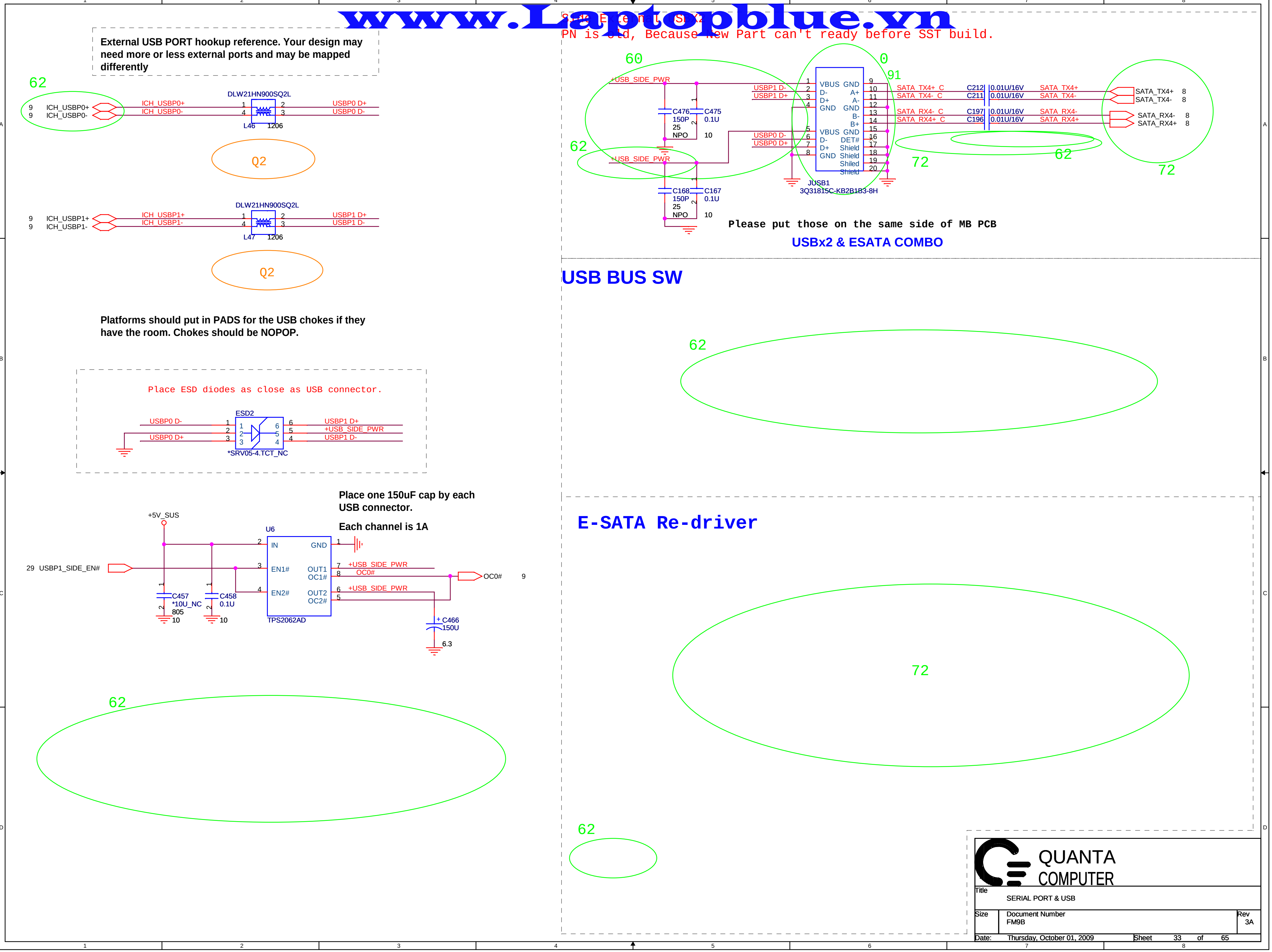
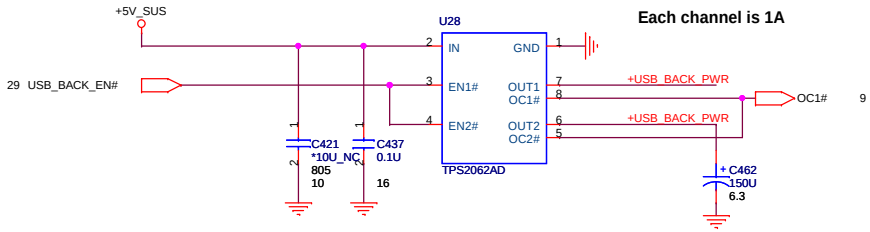
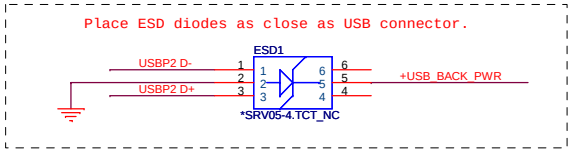


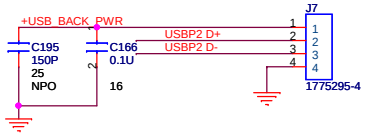
Q2

Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
Size	Document Number FM9B	Rev 3A
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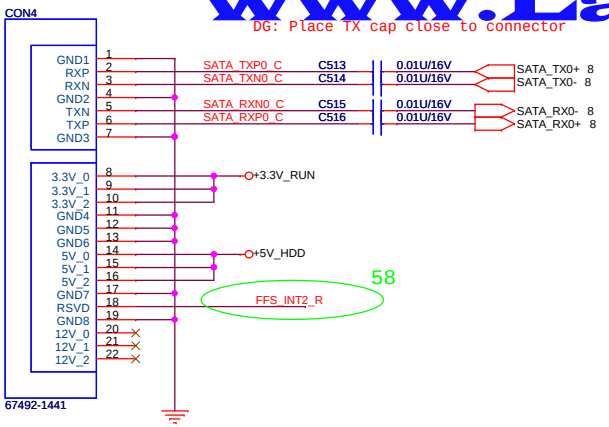
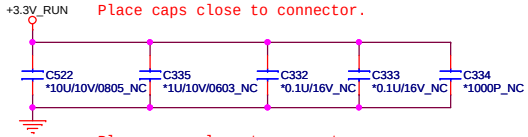
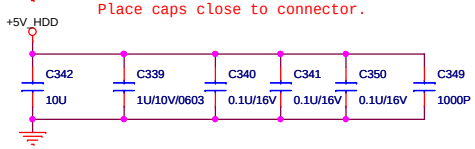
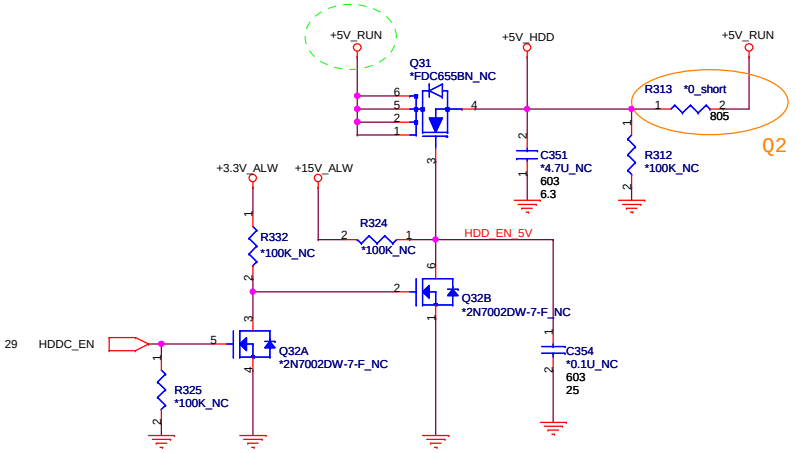
SATA Connector.

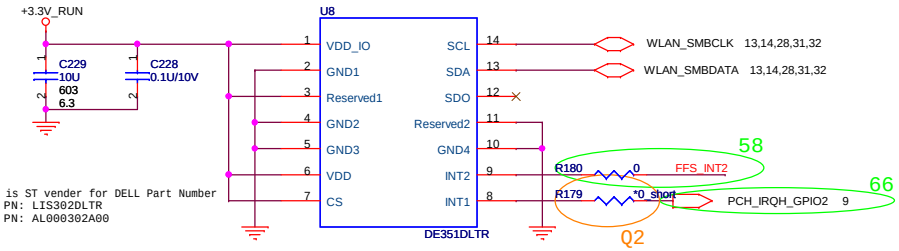




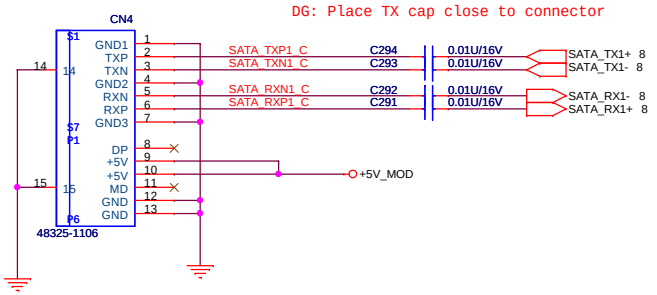


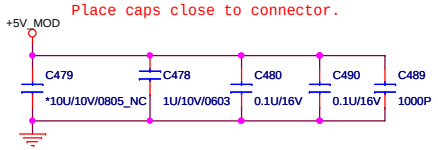


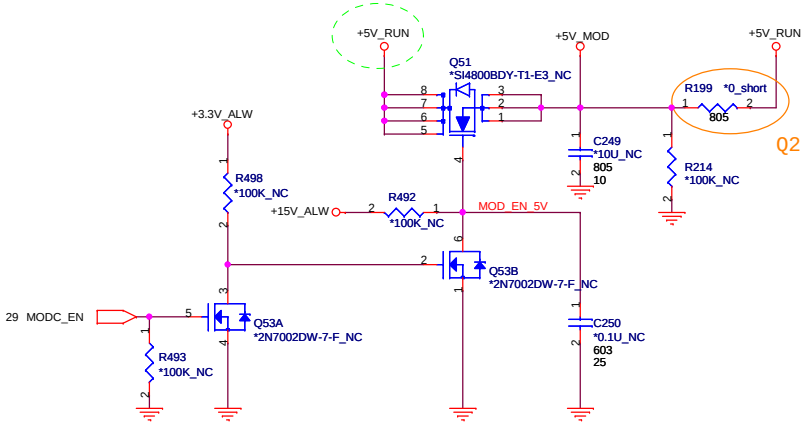
3-axis Fall Sensor (HDD data protector)

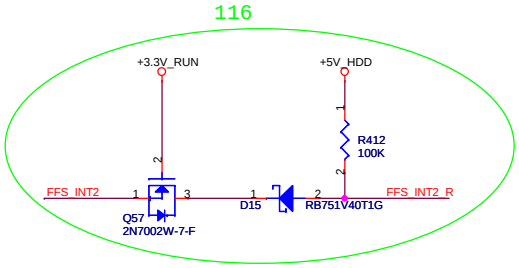


ODD Connector









QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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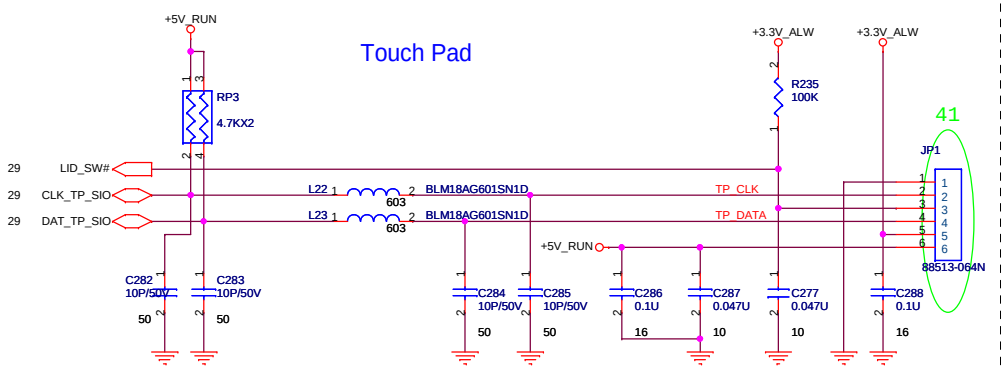
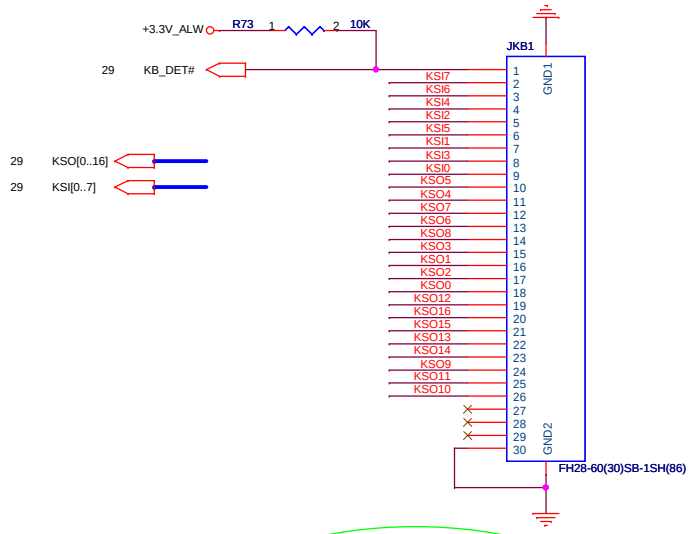
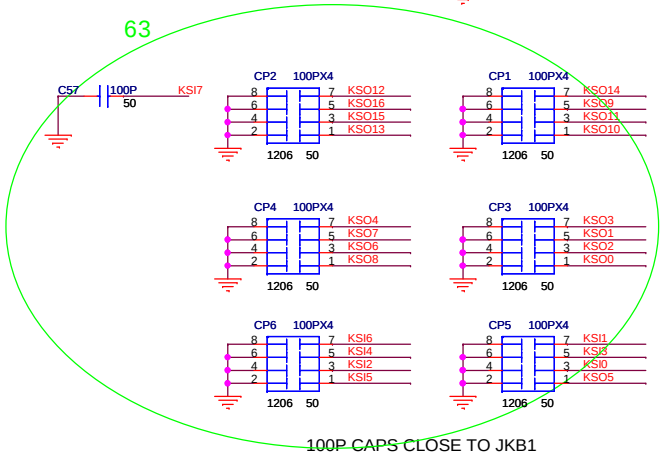
Touch Pad



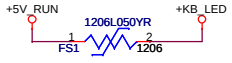


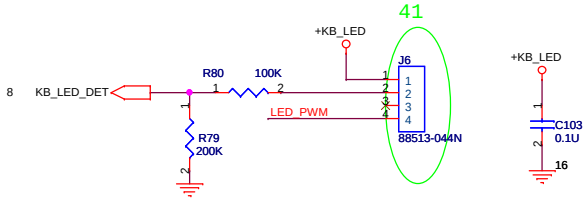


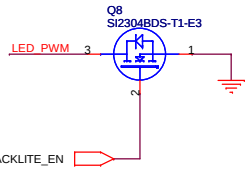
100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil







QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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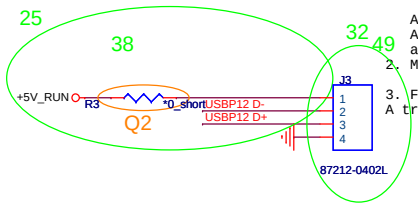
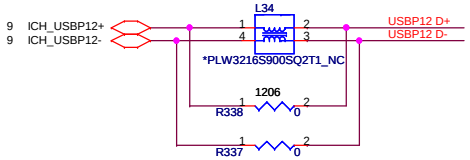
Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

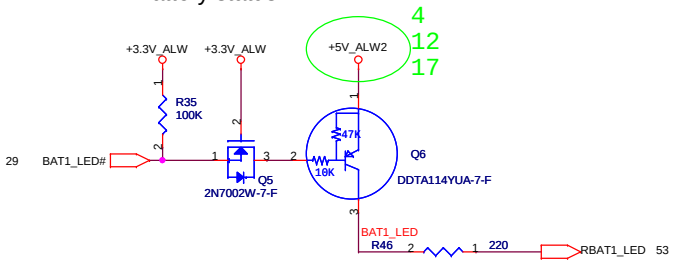


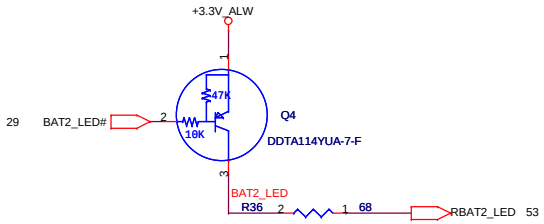
Need check the connector footprint and symble.

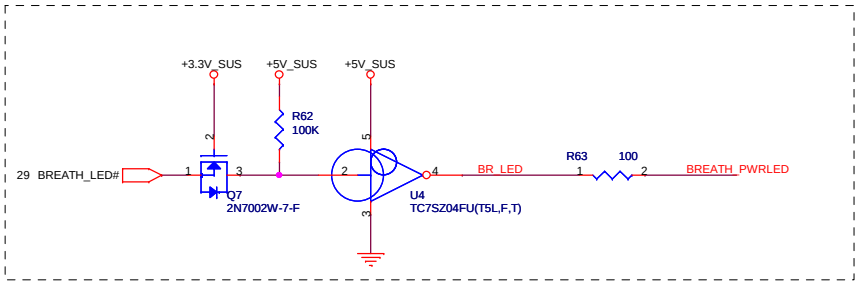


Power button Cable

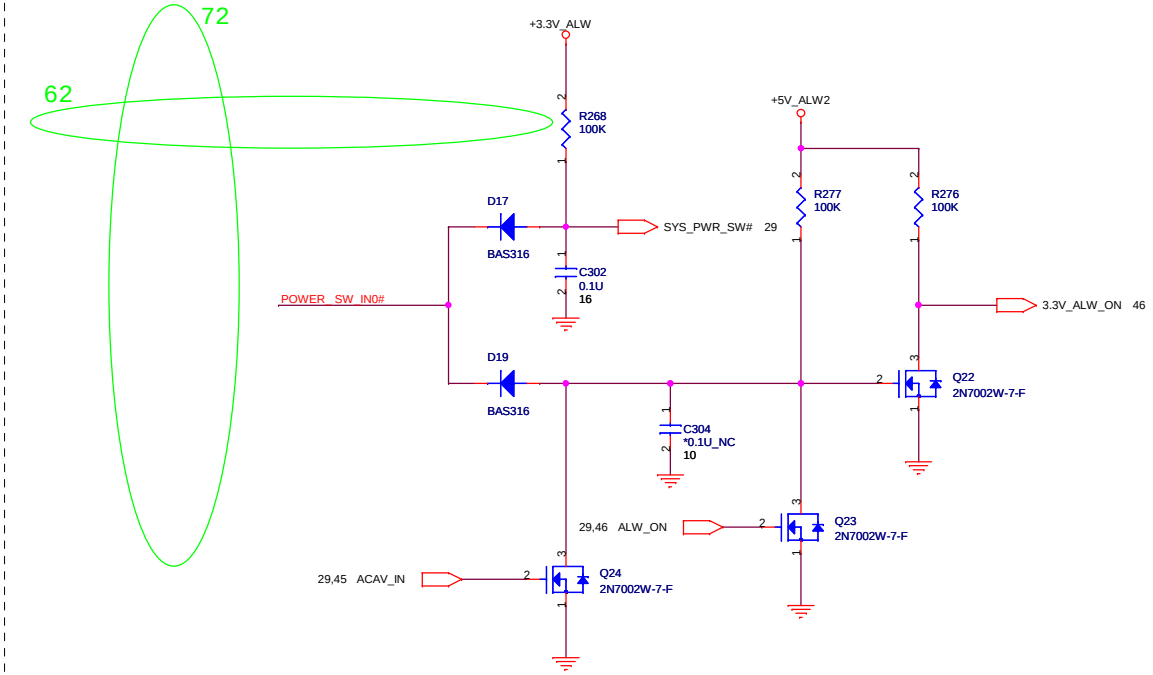
Battery status.

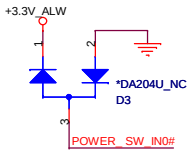


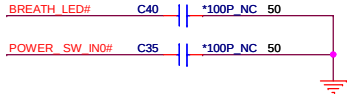




3VALW ON POWER LOGIC

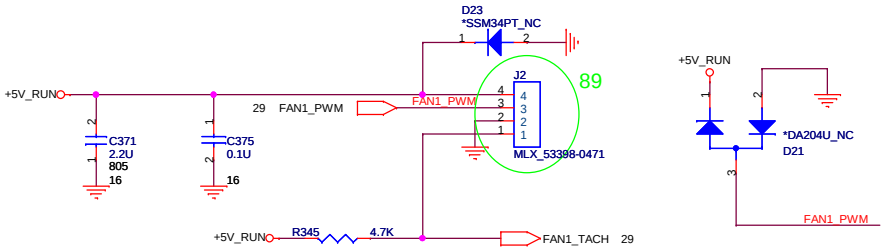


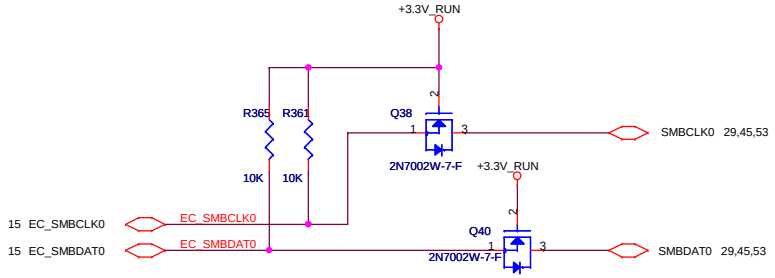


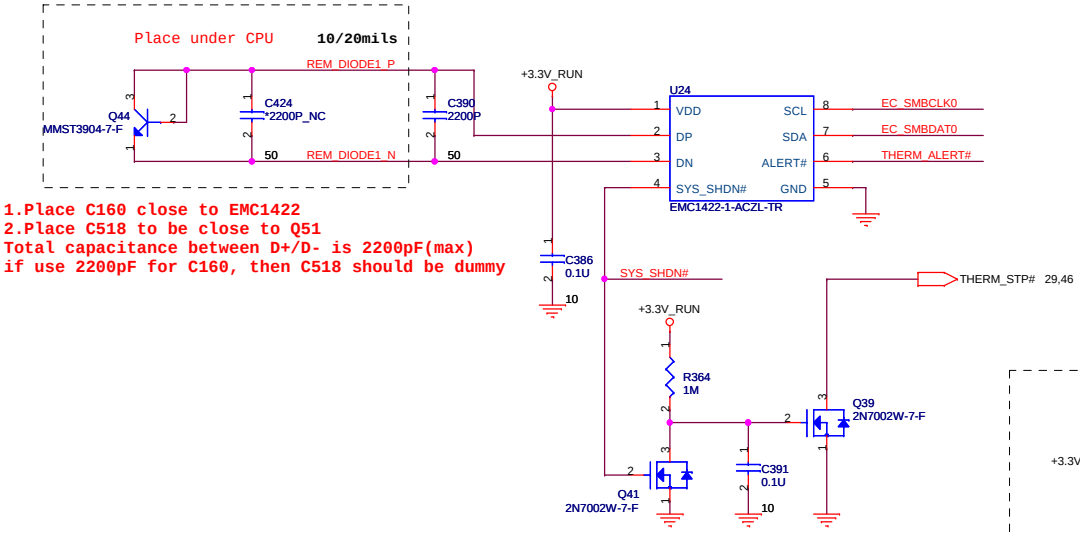


QUANTA COMPUTER

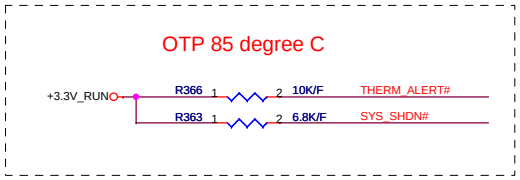
Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9B	Rev 3A
Date: Monday, October 05, 2009	Sheet 37 of 65	







1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 38 of 65	

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H

INTERNAL SPEAKER AMP

TPA6040A4
QFN 32PIN

Layout Note: Place close U18 pin 23.

Layout Note: Close to U18 Pin 34

Layout Note: Place close to pin 18.

Layout Note: Place close U18.

AZALIA (HD) CODEC

U10
92HD73C

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Depop R479,C699 for using 92HD73C

Depop R477,R478,R484,R473
Pop R476,R480,R483,R475
for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils

Close to U19

Layout Note: Close to U19 Pin 13

Check it is ok at ST, if it is ok then remove it.

Title	Azelia CODEC
Size	Document Number: FM9B
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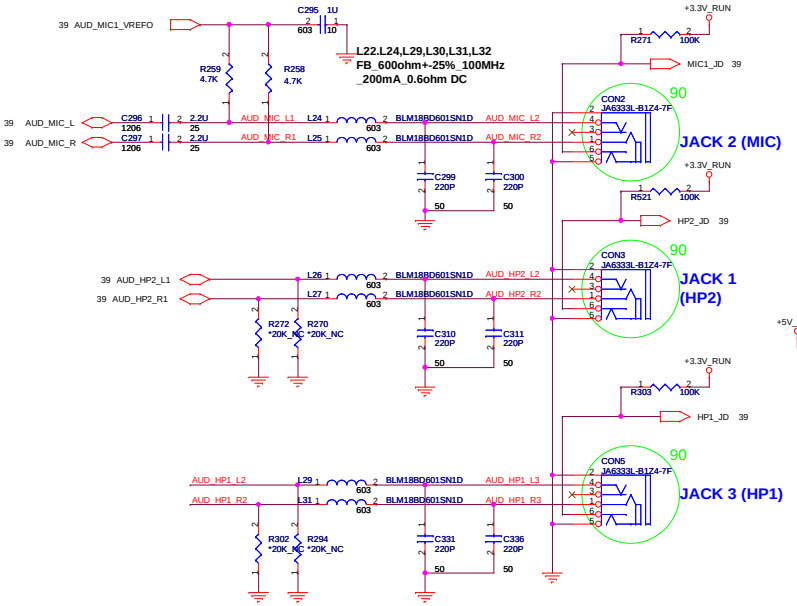
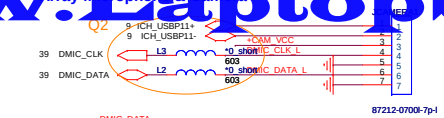
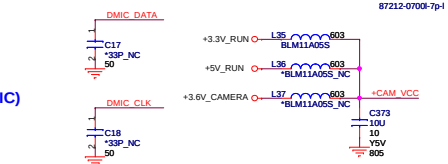
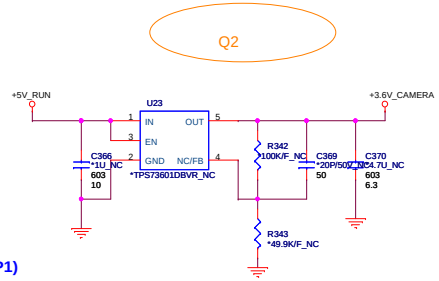
QUANTA COMPUTER

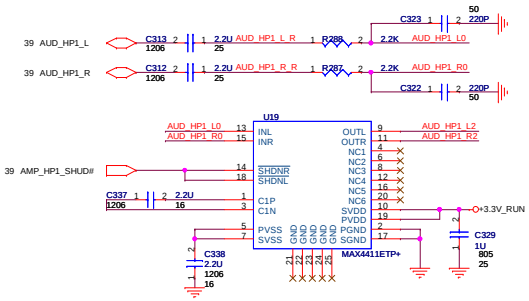
Headphone Jack
Stereo MIC Jack





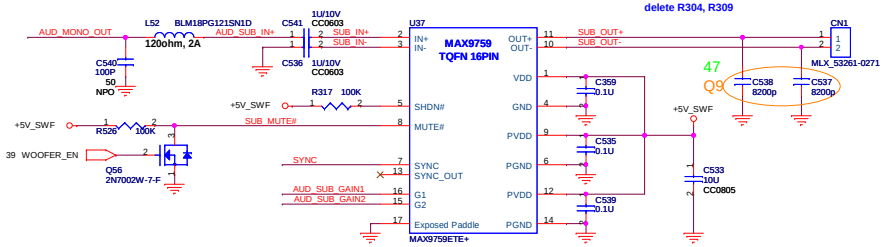




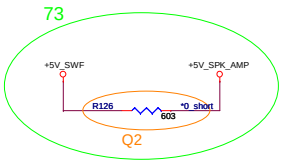


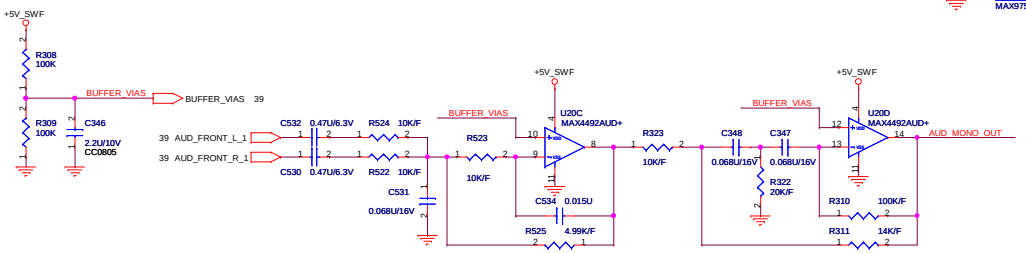
INTERNAL SUBWOOFER AMP

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



Gur_0808: 0 ohm removal,
delete R304, R309

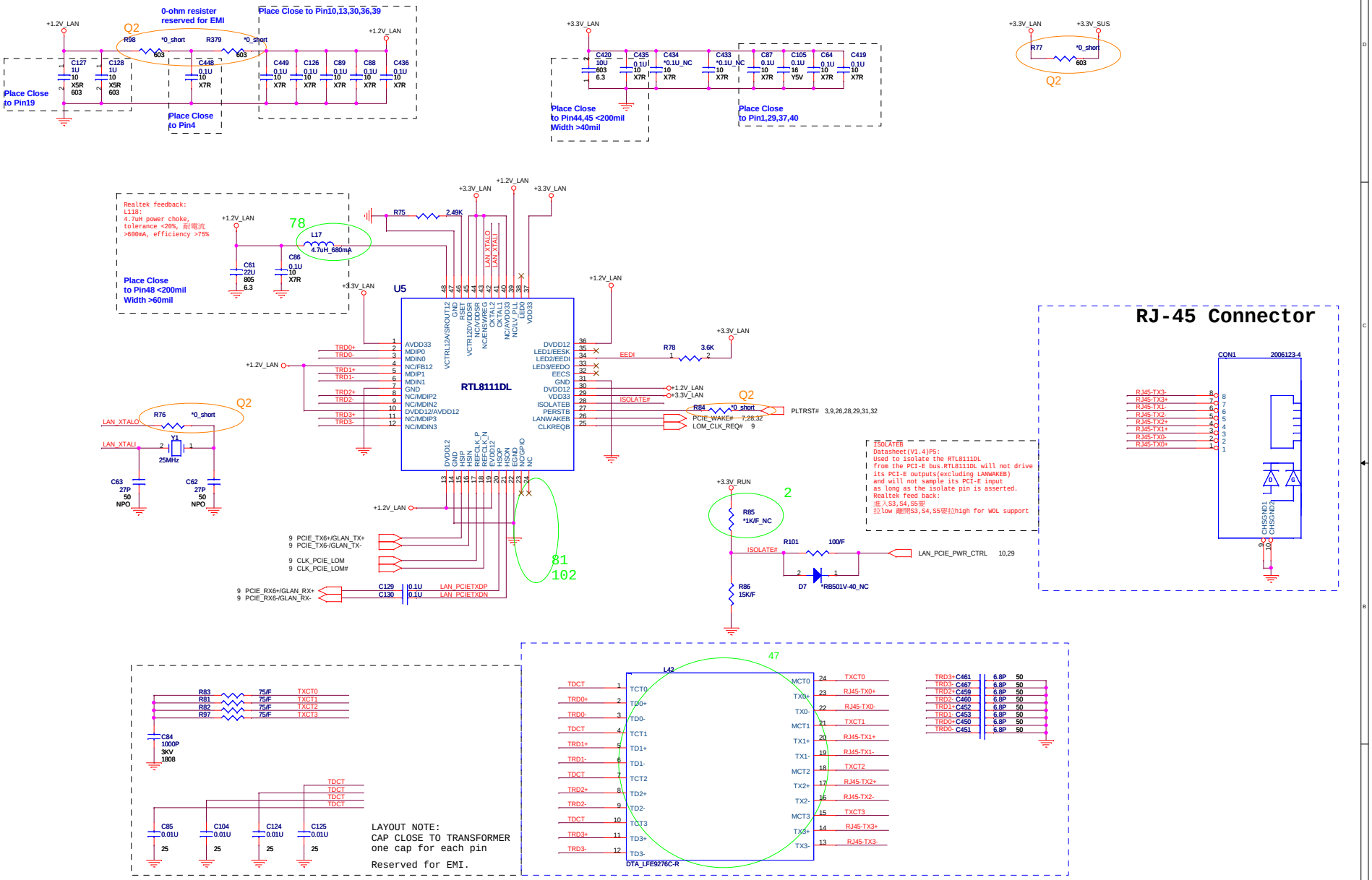




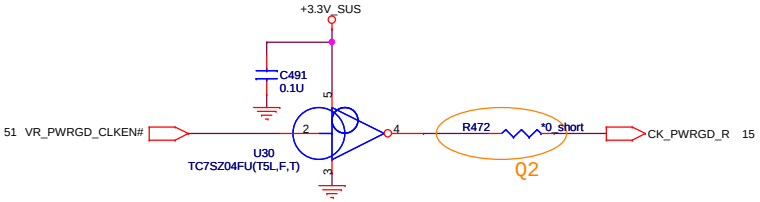
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

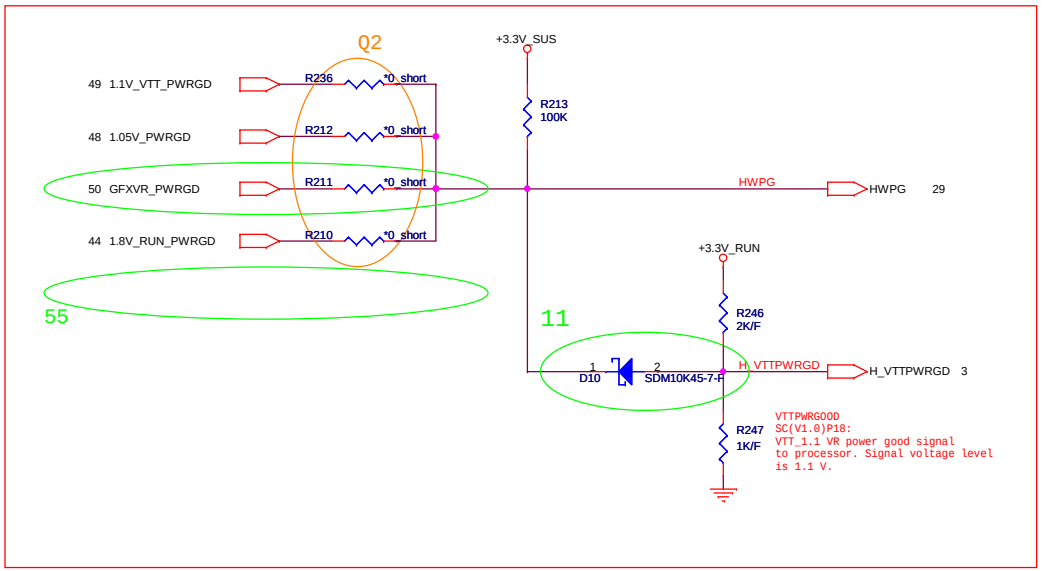
QUANTA COMPUTER

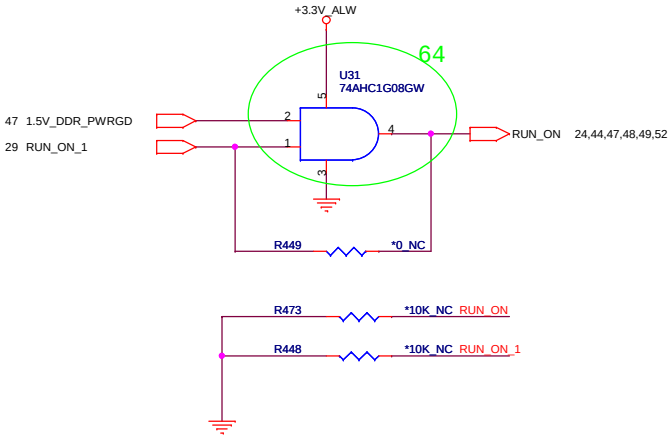
Title	AUDIO CONN	
Size	Document Number FM9B	Rev 3A
Date: Monday, October 12, 2009	Sheet 40 of 65	



Title	LAN		
Size	Document Number FM9B		Rev 3A
Date:	Monday, October 05, 2009	Sheet 41 of 65	





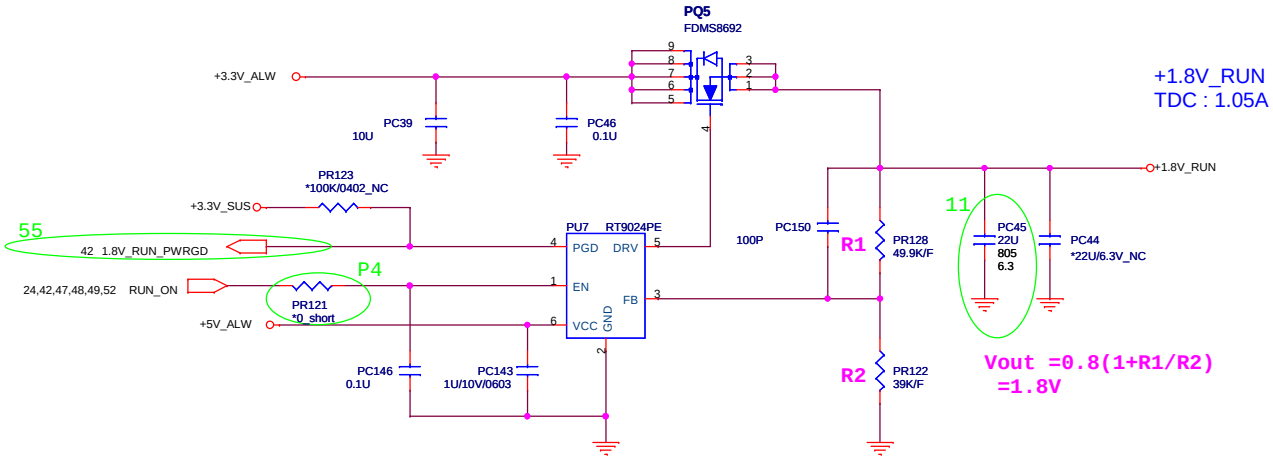


QUANTA COMPUTER

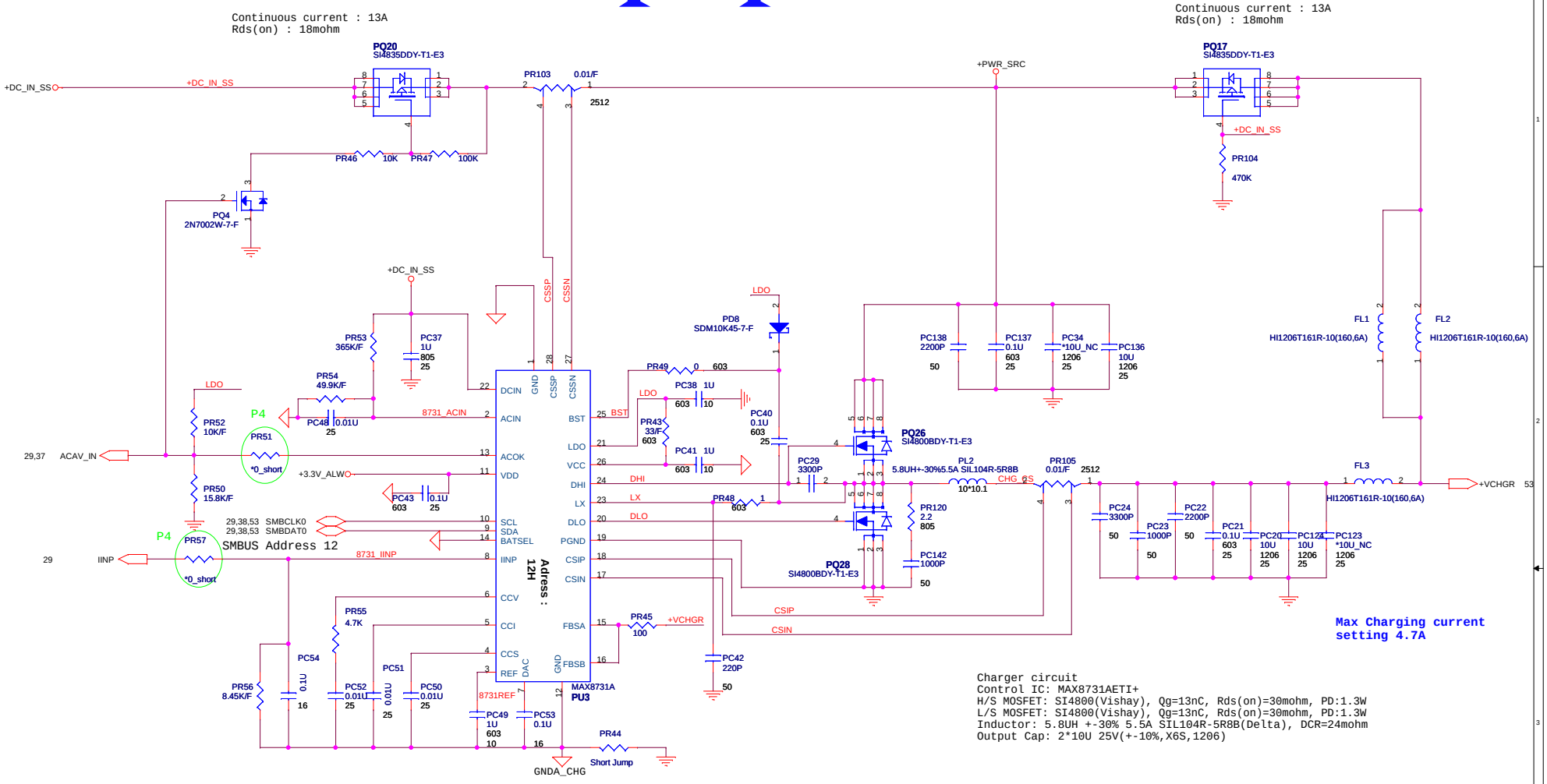
Title	System Reset Circuit	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 42 of 65	

QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 43 of 65	



Title	+1.8V_RUN(RT9024)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 44 of 65	



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 45 of 65	

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 1.5U20%17.1A(FDVE1040-H-1R5M=P3)(TOKO), DCR=4.6mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

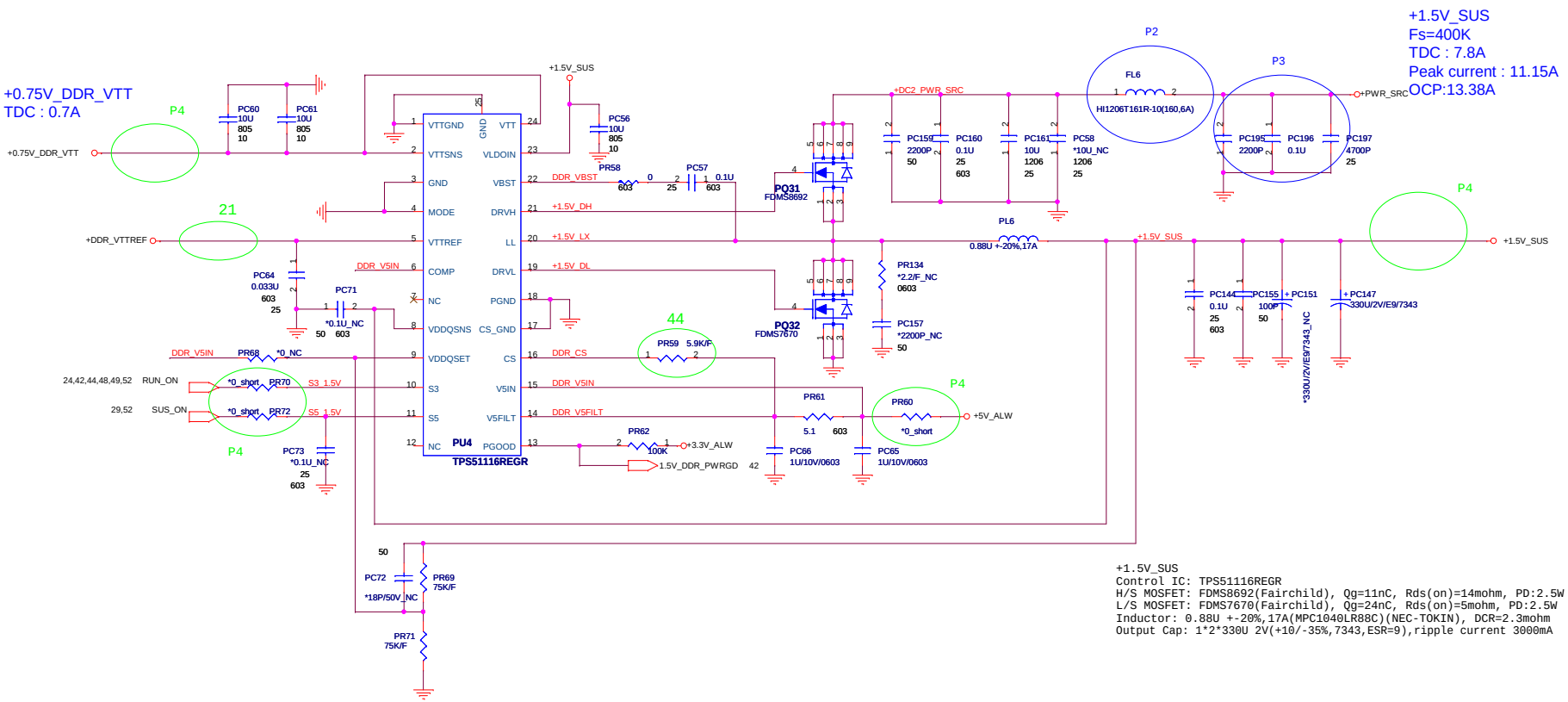
+3.3V_ALW
Fs=300K
TDC : 8.23A
Peak : 11.77A
OCP:14A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number FM9B	Rev 2B
Date: Monday, October 05, 2009	Sheet 46 of 65	



+1.5V_SUS
Control IC: TPS51116REGR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.88U +-20%,17A(MPC1040LR88C)(NEC-TOKIN), DCR=2.3mohm
Output Cap: 1*2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

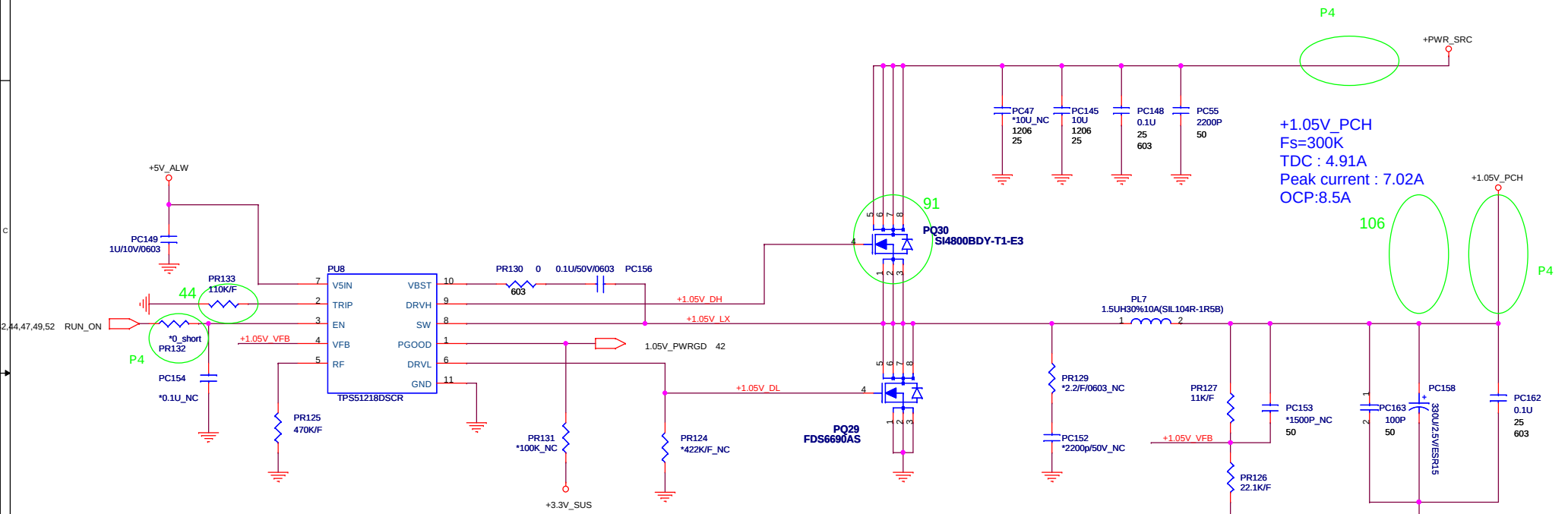
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)		
Size	Document Number FM9B		Rev 2B
Date:	Thursday, October 01, 2009	Sheet 47 of 65	

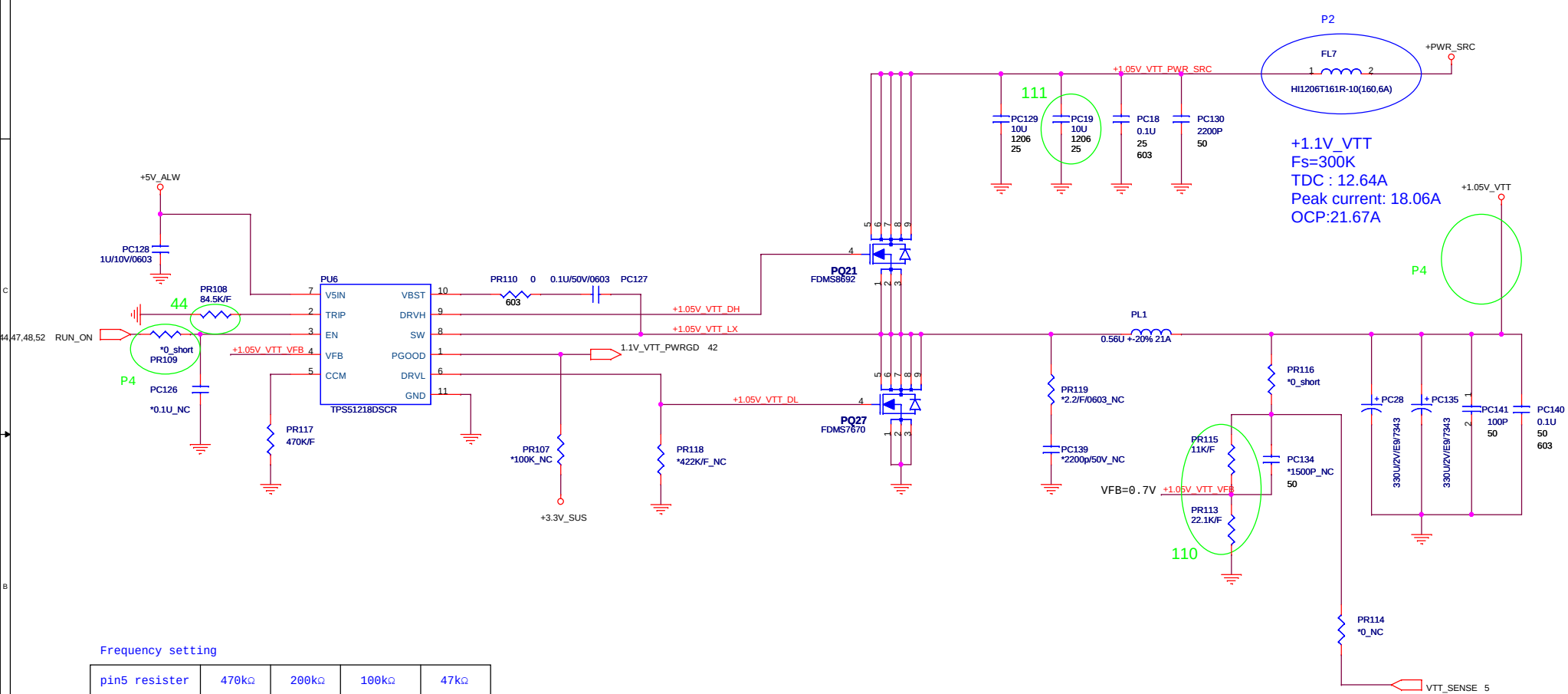


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)		
Size	Document Number FM9B		Rev 2B
Date: Thursday, October 01, 2009		Sheet 48 of 65	

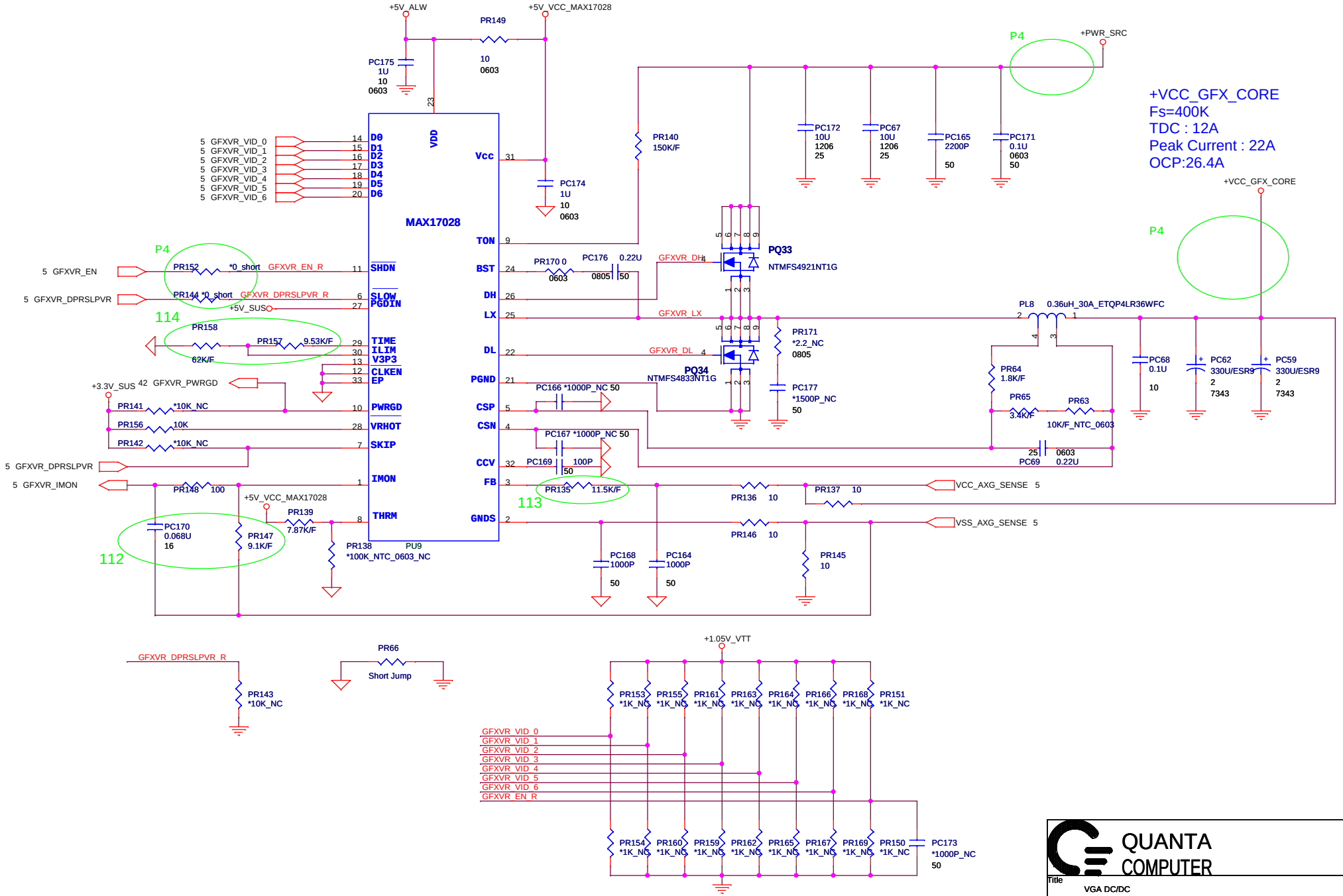


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

Title	+1.05V_VTT(TPS51218)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 49 of 65	



Default Vcc_Core voltage is 1.0500V

QUANTA COMPUTER

Title	VGA DC/DC	
Size	Document Number FM9B	Rev 2B
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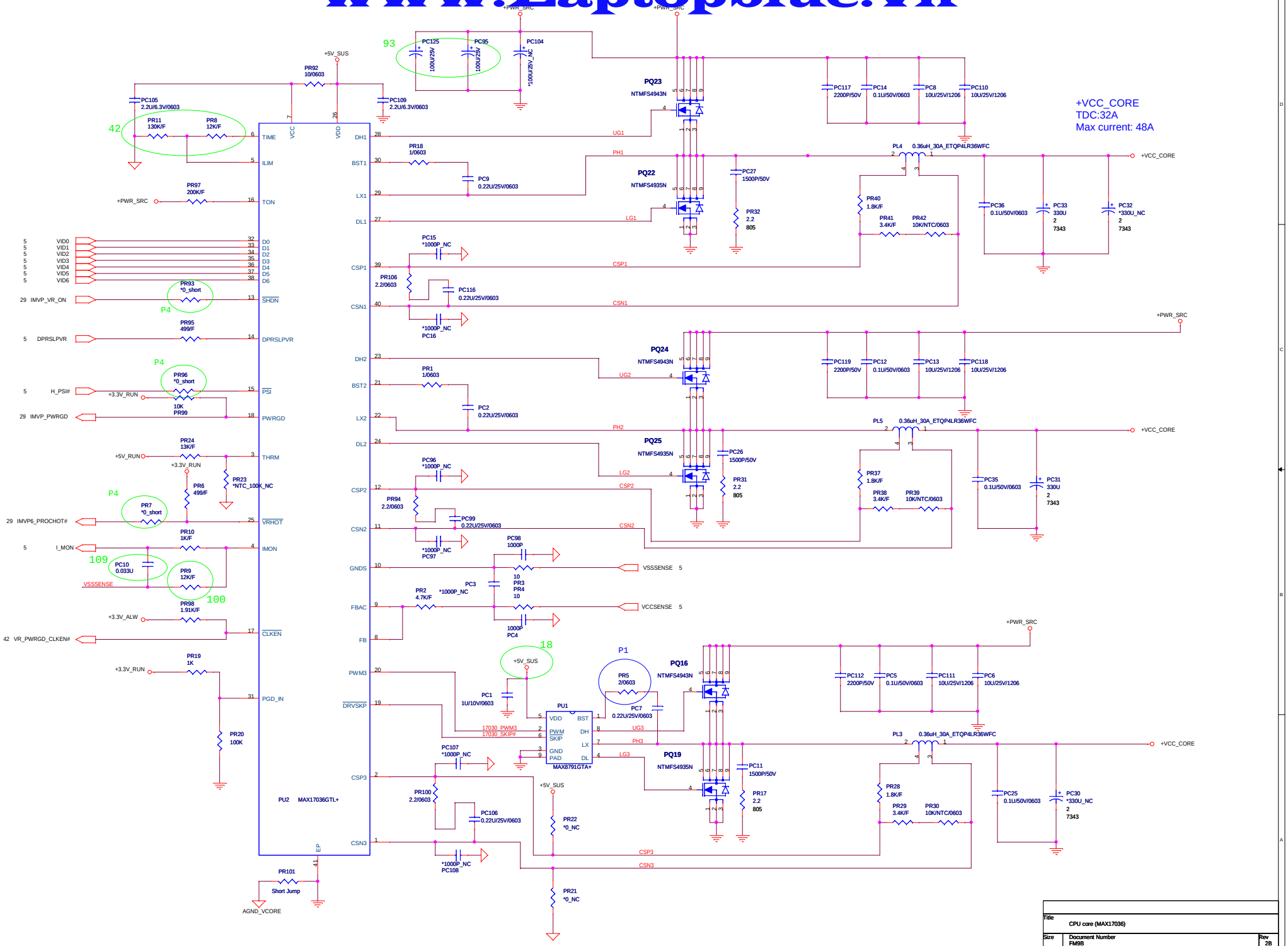
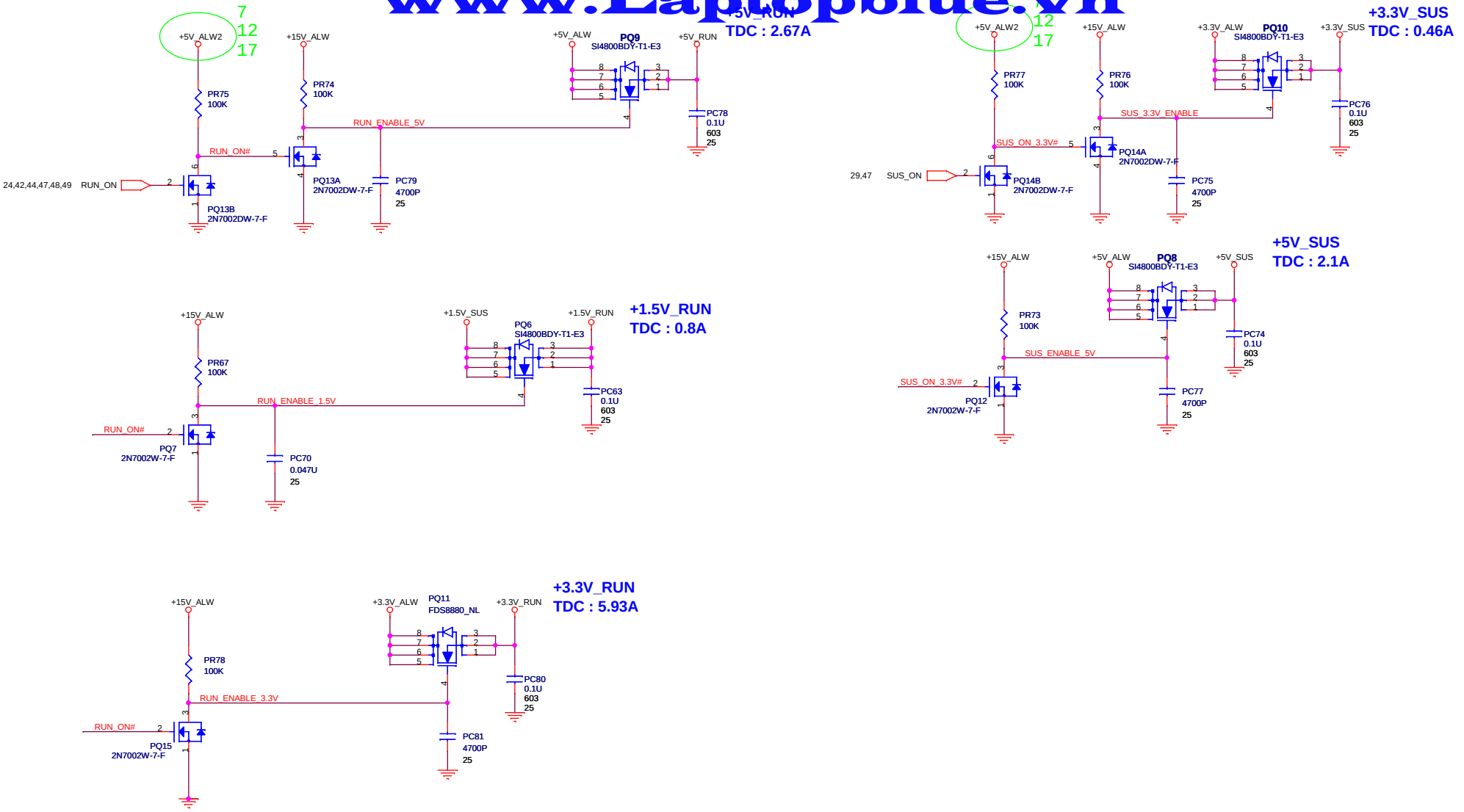
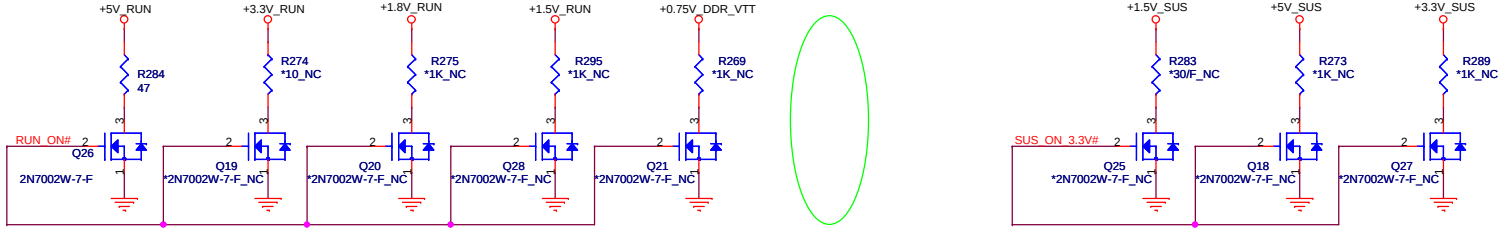


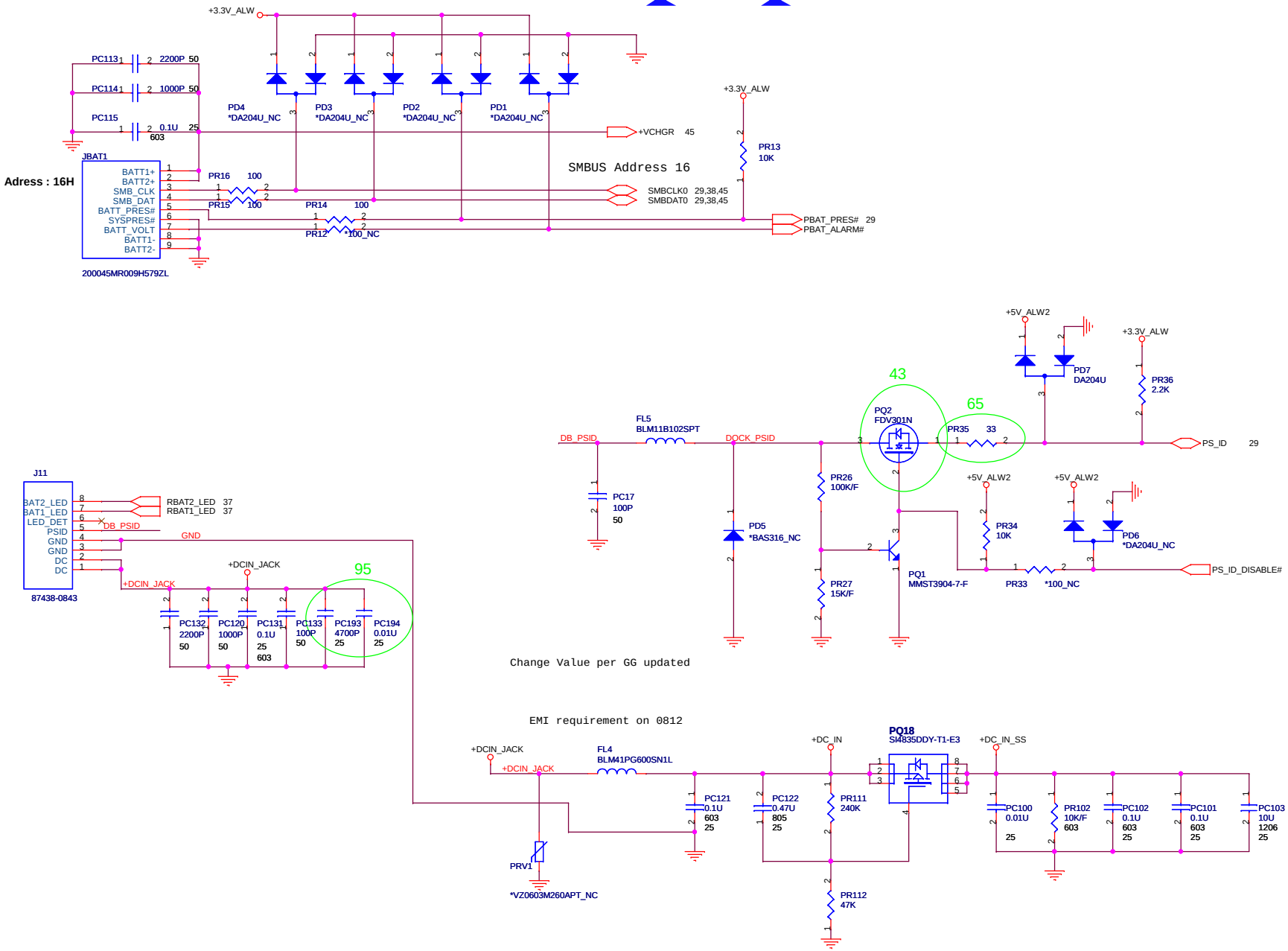


Reserve discharge path



QUANTA COMPUTER

Title	RUN / SUS POWER SW	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 52 of 65	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 53 of 65	

FOR CPU use

H12 *H-C276D177P2_NC H-C276D157P2
H5 *H-C276D177P2_NC H-C276D157P2
H13 *H-C276D177P2_NC TBC276IN197D157P2
H6 *H-C276D177P2_NC TBC276IN197D157P2

87

TH1 *H-TC118BC197D63P2_NC
TH2 H-TC118BC197D63P2

For MiniCard nut use.
on 31' header

H3 *H-TC315BC394D79P2_NC H-TC315BC394D79P2
H1 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H21 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H14 *H-TC315BC335D126P2_NC h-tc315bc295d126p2

H7 *o-o177x472d177x472n_NC o-o177x472d177x472n
H24 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H23 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H18 *h-fm8b-1_NC h-fm8b-1

H15 *H-C256D154P2_NC H-C256D154P2
H11 *H-C256D154P2_NC H-C256D154P2

For PCH nut use.

47
71
97

PV1 *PAD138X98XH_NC
PV2 *PAD138X98XH_NC
PV3 *PAD138X98XH_NC
PV4 PAD138X98XH

GND

H19 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H16 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H9 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H2 *h-TC256BC315D110P2_NC h-TC256BC315D110P2

H4 *h-tc256bc315d126p2_NC h-tc315bc394d126p2

H8 *H-C228D228N_NC H-C228D228N
H10 *H-C197D197N_NC H-C197D197N
H22 *H-C394D394N_NC H-C394D394N
H17 *H-TC256BC315D126P2_NC H-TC256BC315D126P2

QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number FM9B	Rev 3A
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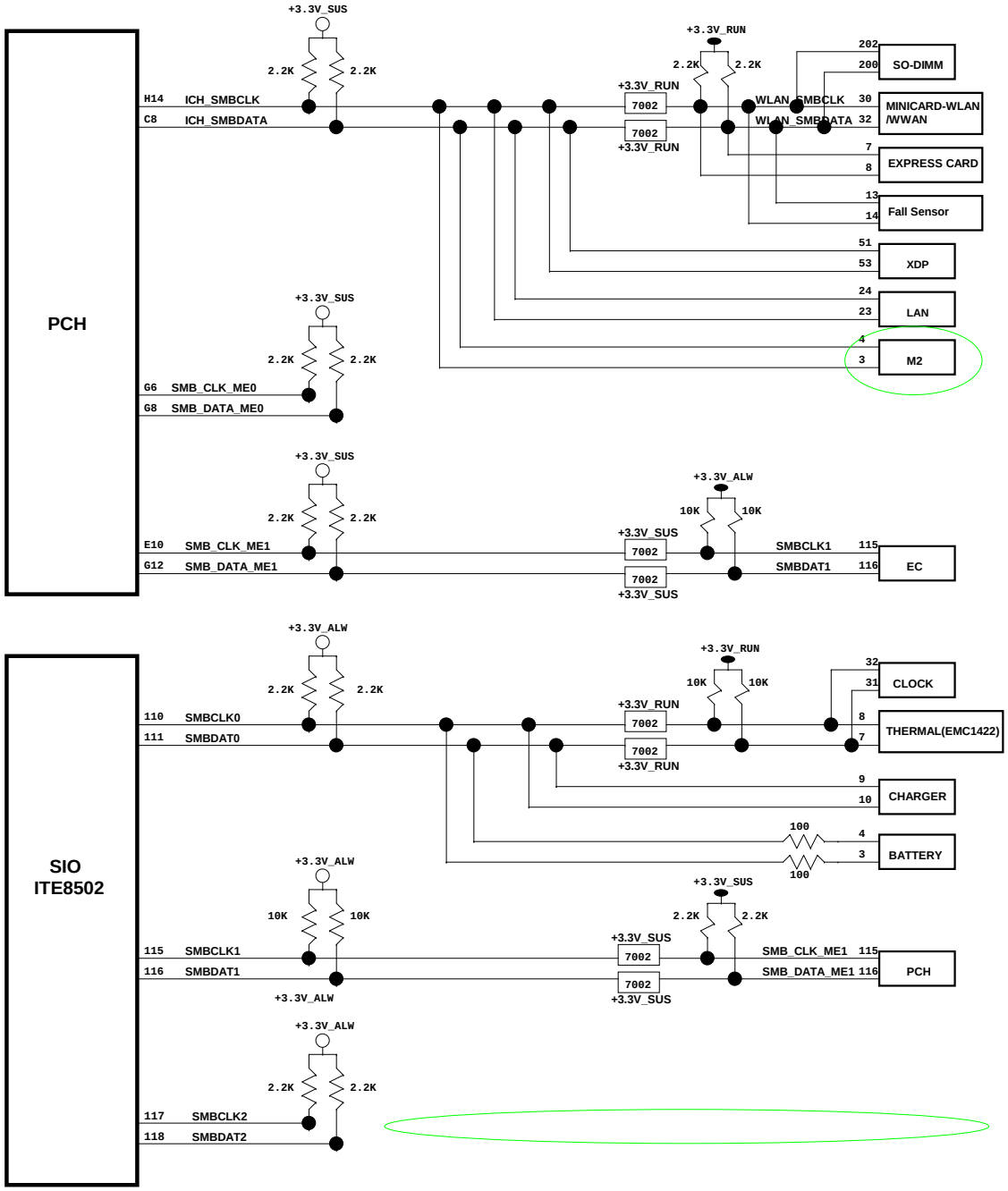
Reserved for EMI.

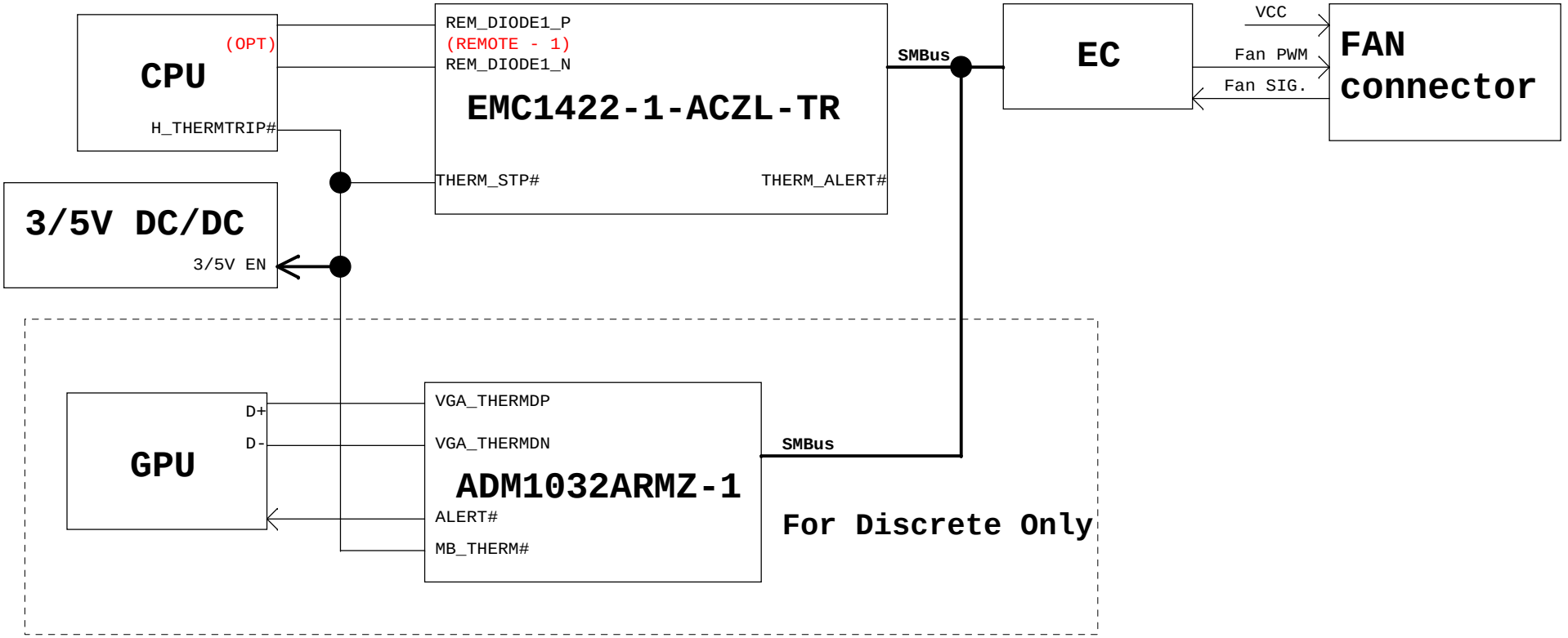
QUANTA COMPUTER

Title	EMI CAP	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 55 of 65	



QUANTA COMPUTER

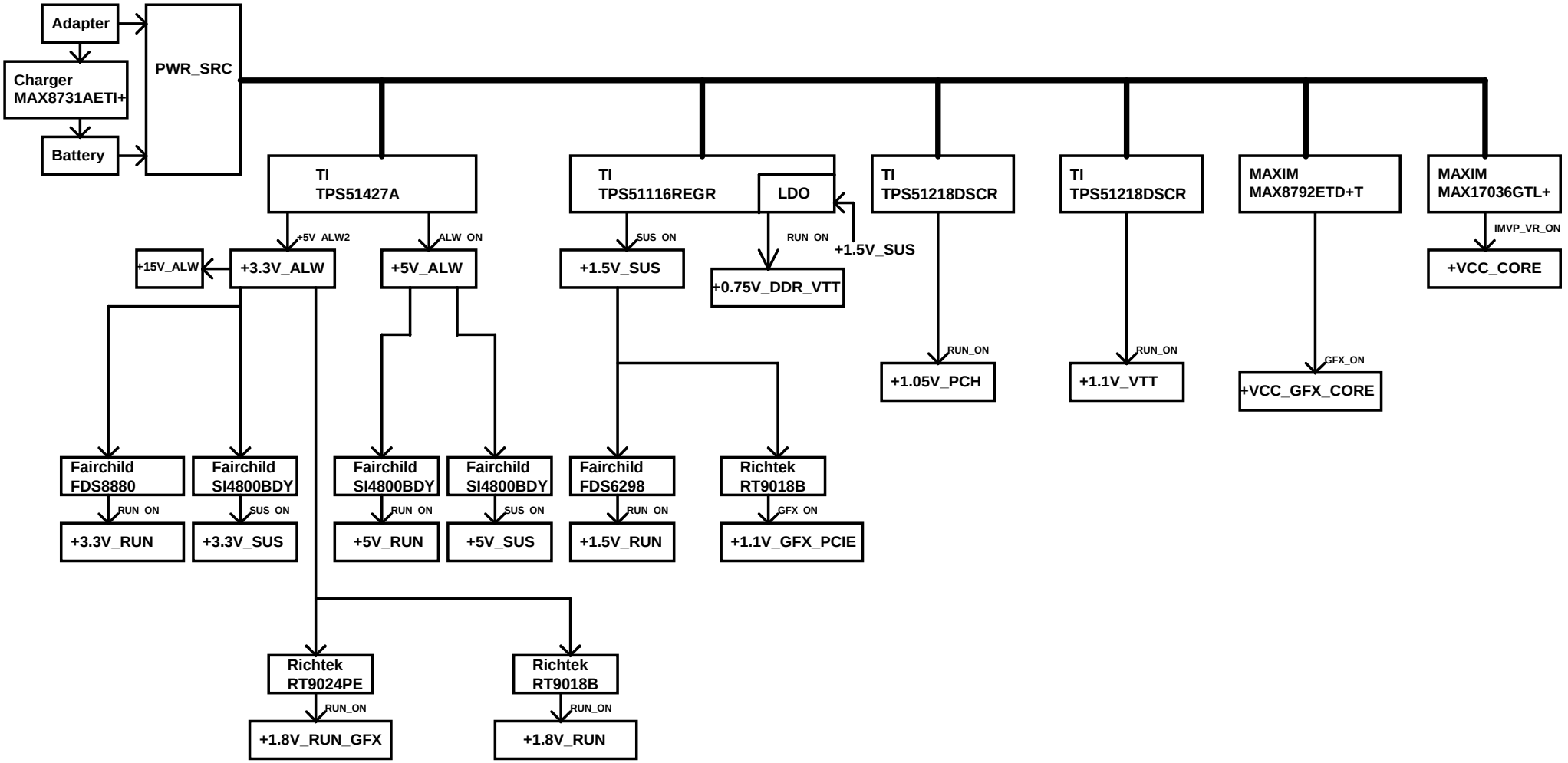
Title	SMBUS BLOCK	
Size	Document Number FM0S	Rev 3A
Date: Thursday, October 01, 2009	Sheet 56 of 65	



QUANTA COMPUTER

Title	Thermal Map	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 57 of 65	

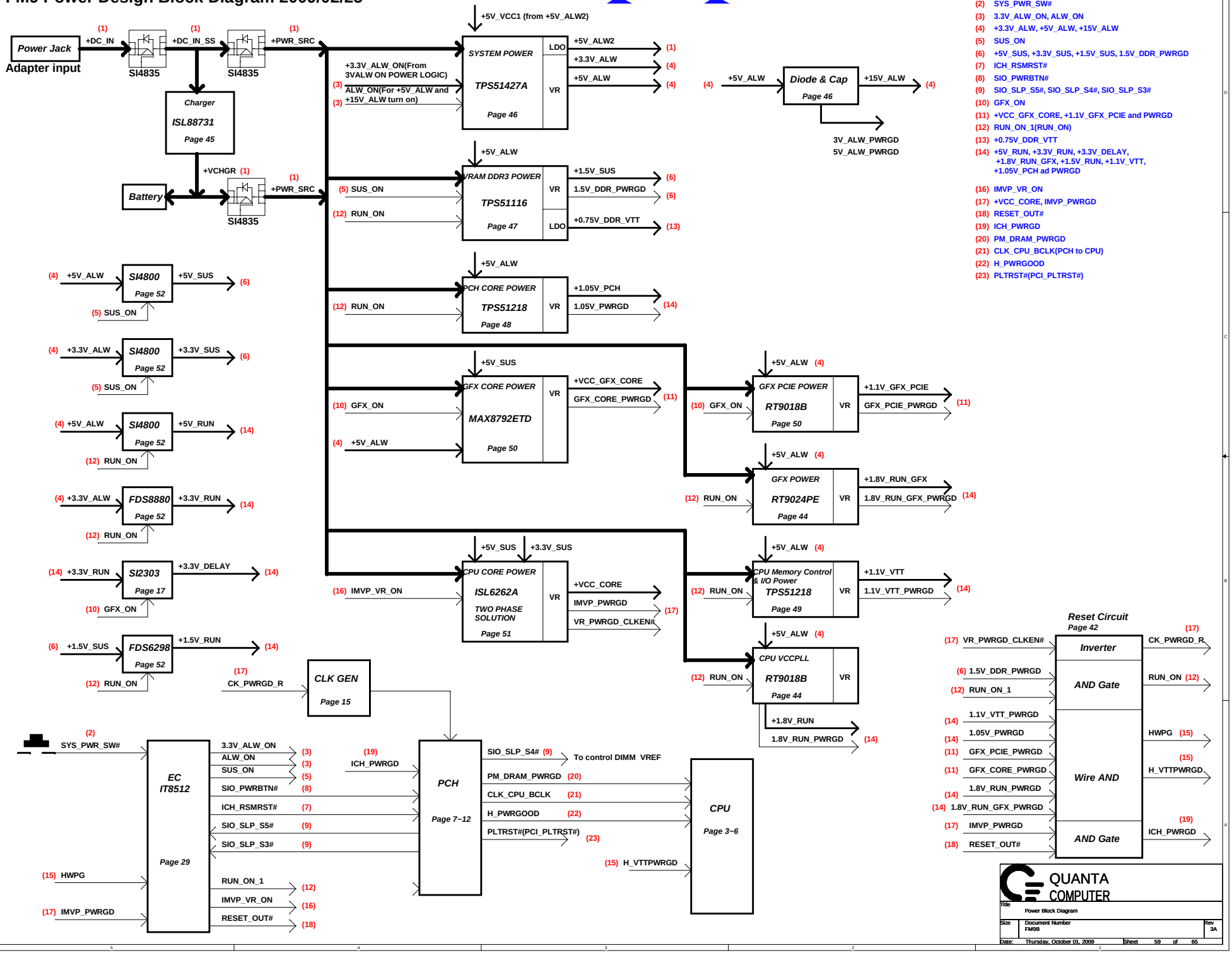
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 58 of 65	

FM9 Power Design Block Diagram 2009/02/25



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

QUANTA COMPUTER

Title	Power Block Diagram	
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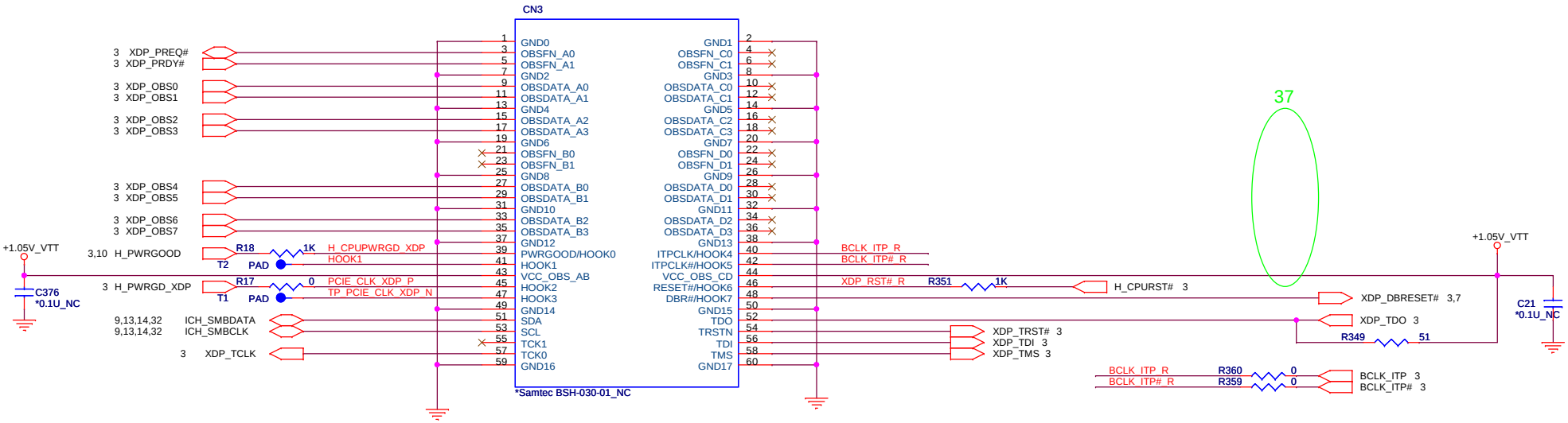

It is for debug. requesst vendeer provide 200 pcs sample.

QUANTA COMPUTER

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