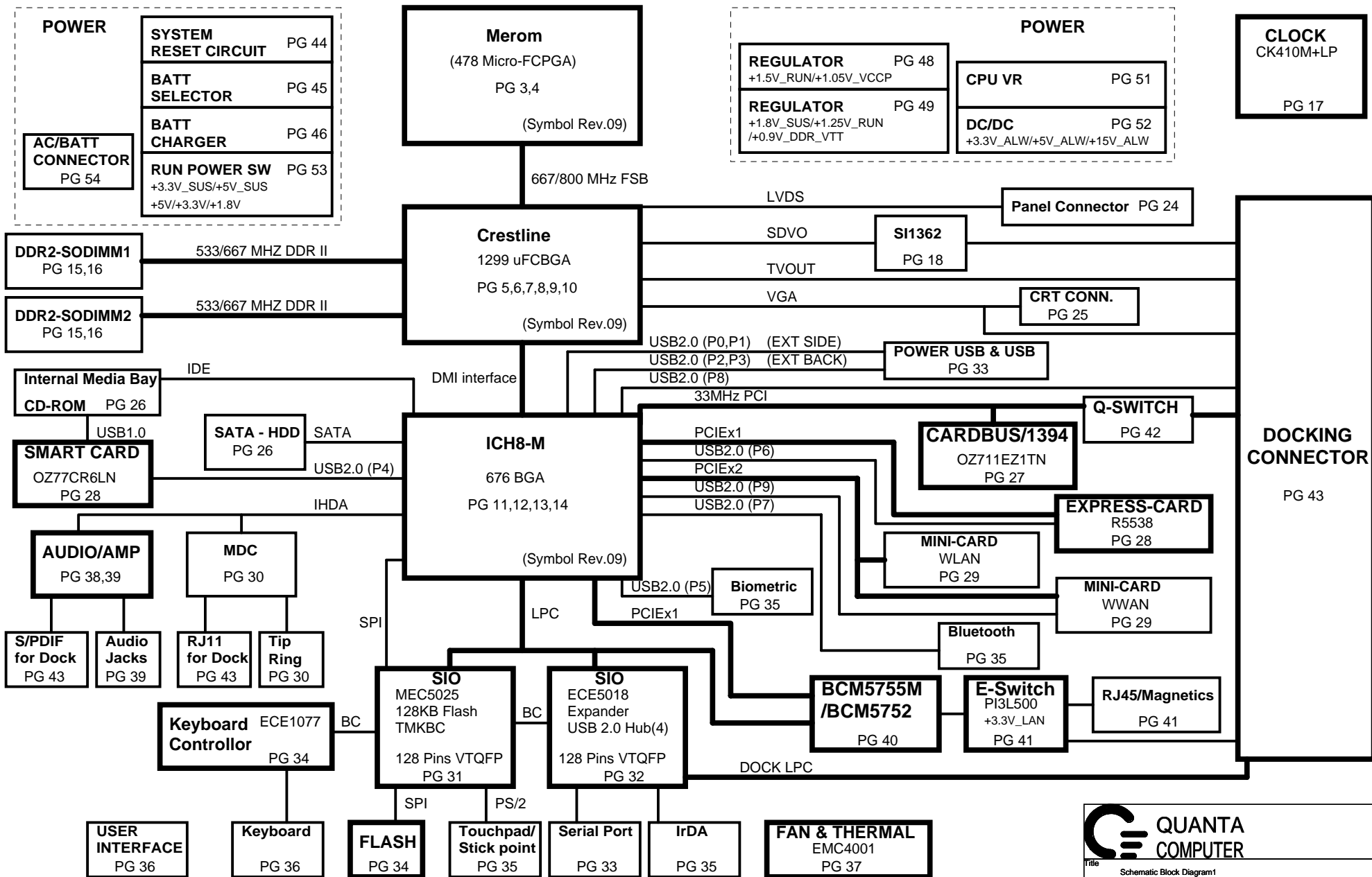
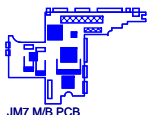


http://laptopblue.vn
JM7-INTEGRATED

PWA FP381, PWB DY483,
 SCHEM UW474.
 VER : 1A

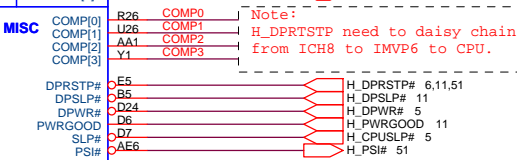
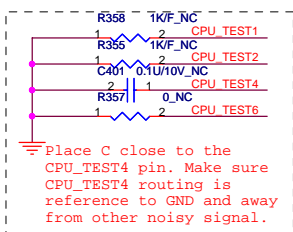
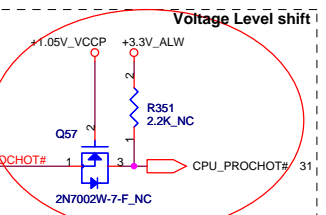
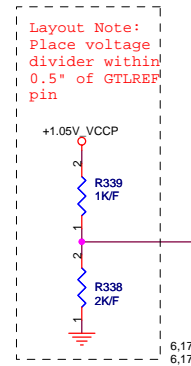
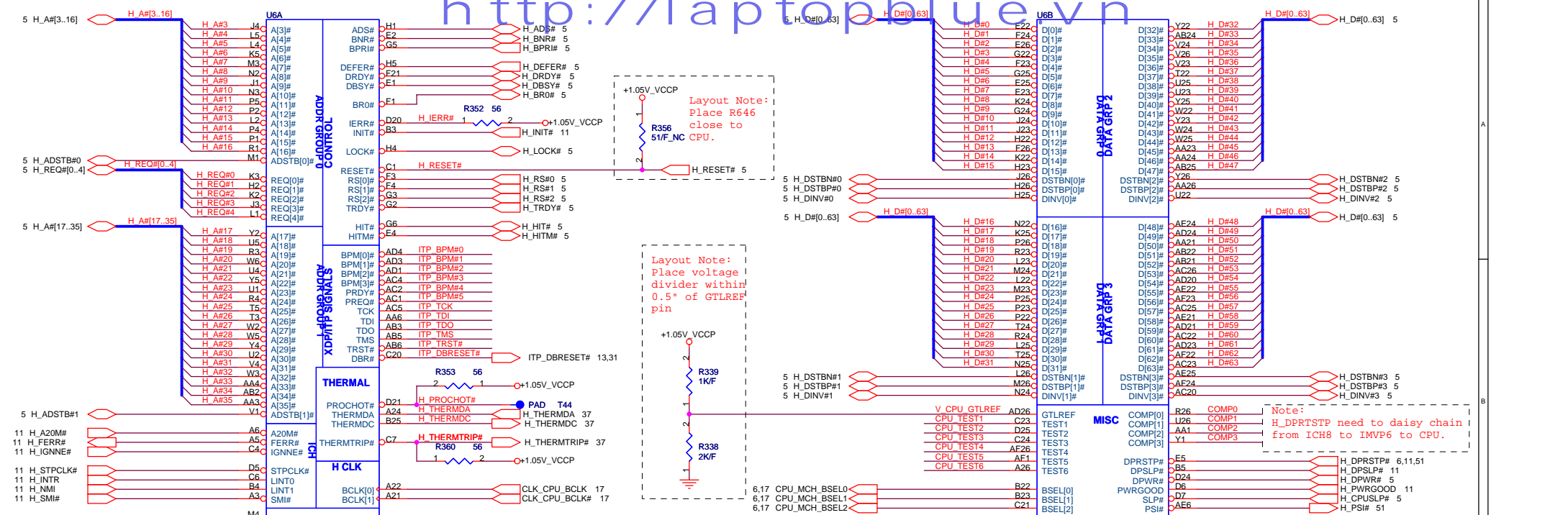


QUANTA COMPUTER

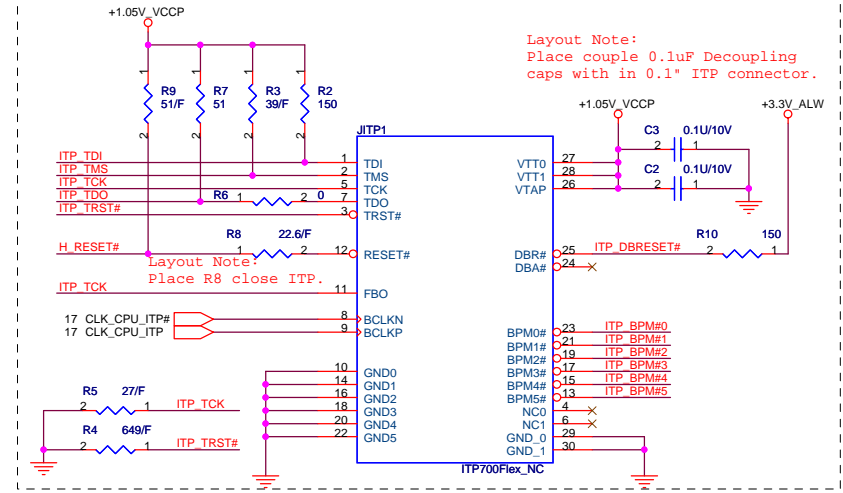
Title: Schematic Block Diagram1

Size: Document Number JM7 Rev 1A

Date: Monday, June 26, 2006 Sheet 1 of 57



Populate ITP700Flex for bringup

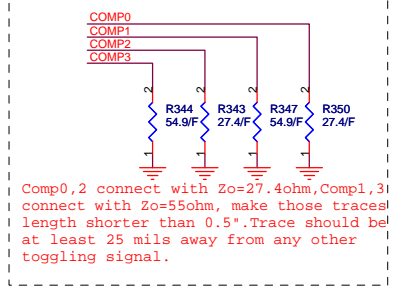


ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPU_RST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



QUANTA COMPUTER

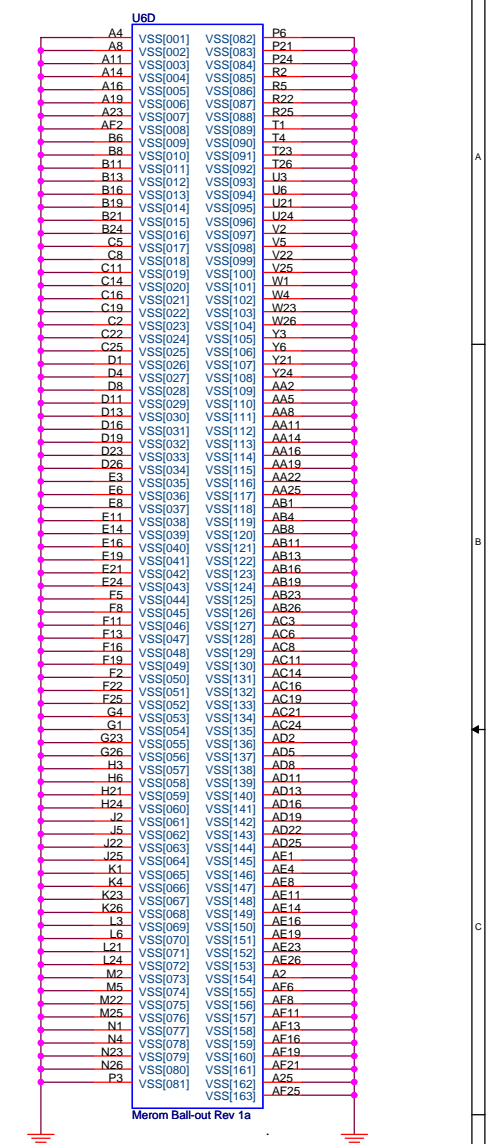
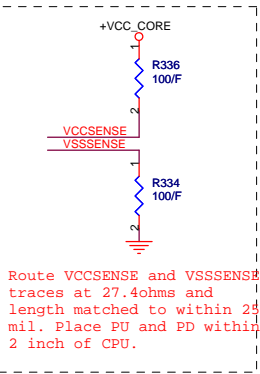
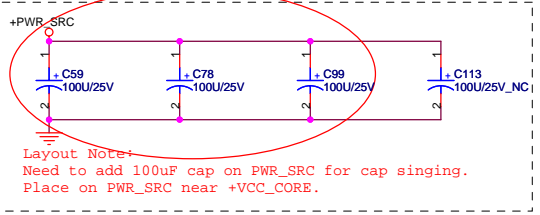
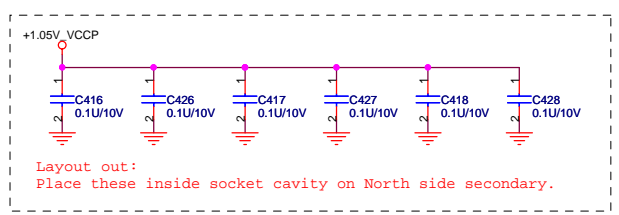
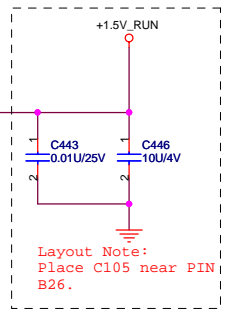
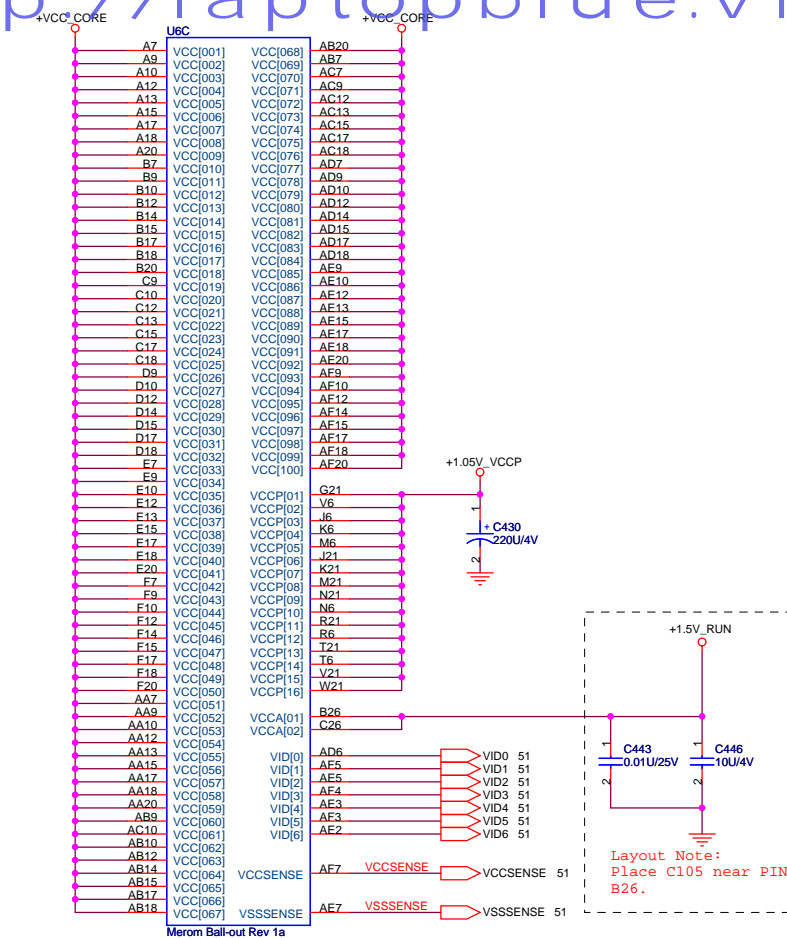
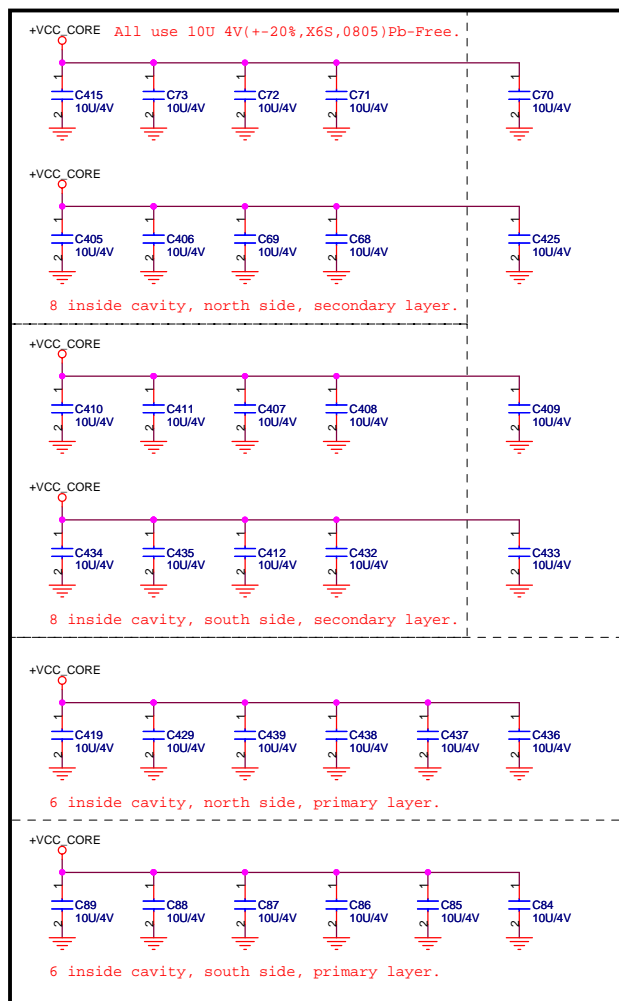
Title: Merom Processor (HOST BUS)

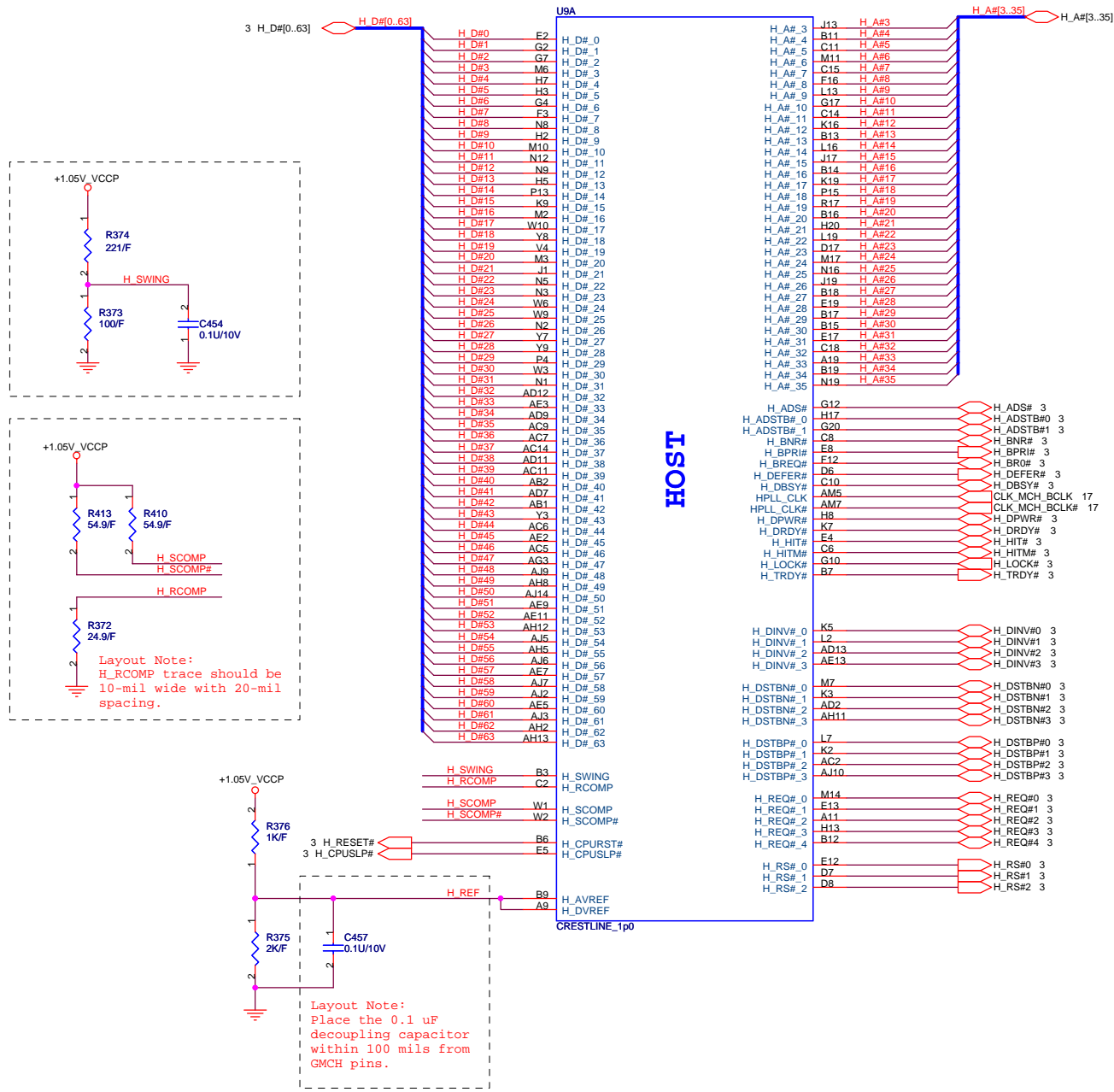
Size: Document Number JM7

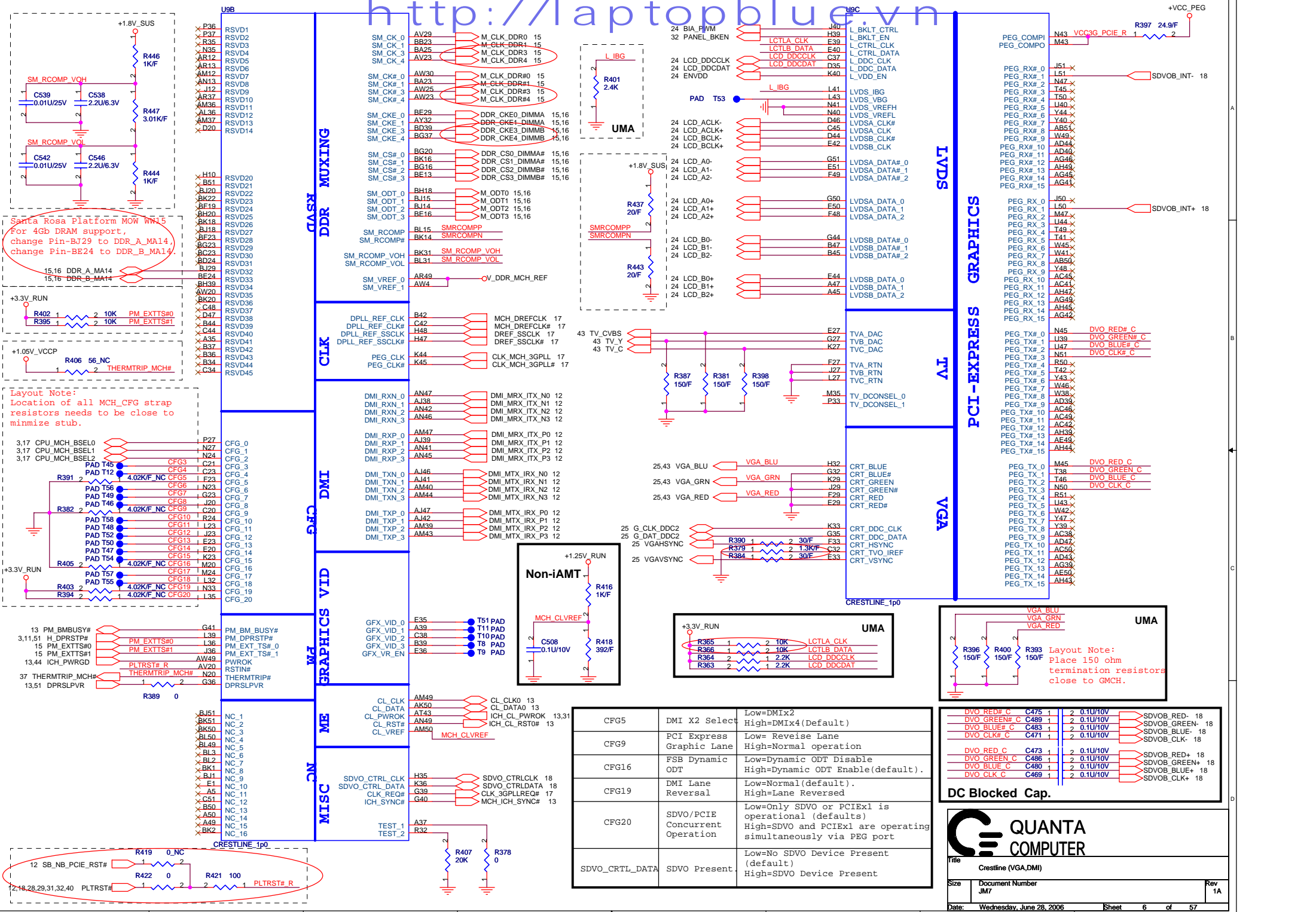
Date: Wednesday, June 28, 2006

Sheet: 3 of 57

Rev: 1A







Santa Rosa Platform MOW W15
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.

UMA
Layout Note:
Place 150 ohm
termination resistors
close to GMCH.

DVO RED# C	A475	1	2	0.1U/10V	SDVOB_RED- 18
DVO GREEN# C	A489	1	2	0.1U/10V	SDVOB_GREEN- 18
DVO BLUE# C	A483	1	2	0.1U/10V	SDVOB_BLUE- 18
DVO CLK# C	A471	1	2	0.1U/10V	SDVOB_CLK- 18
DVO RED C	A473	1	2	0.1U/10V	SDVOB_RED+ 18
DVO GREEN C	A486	1	2	0.1U/10V	SDVOB_GREEN+ 18
DVO BLUE C	A480	1	2	0.1U/10V	SDVOB_BLUE+ 18
DVO CLK C	A489	1	2	0.1U/10V	SDVOB_CLK+ 18

DC Blocked Cap.

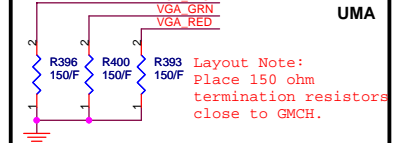
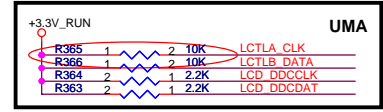
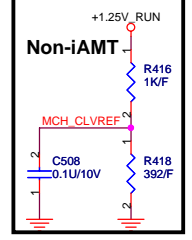
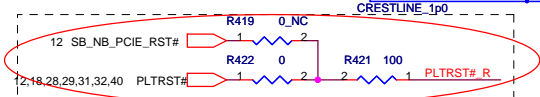
QUANTA COMPUTER

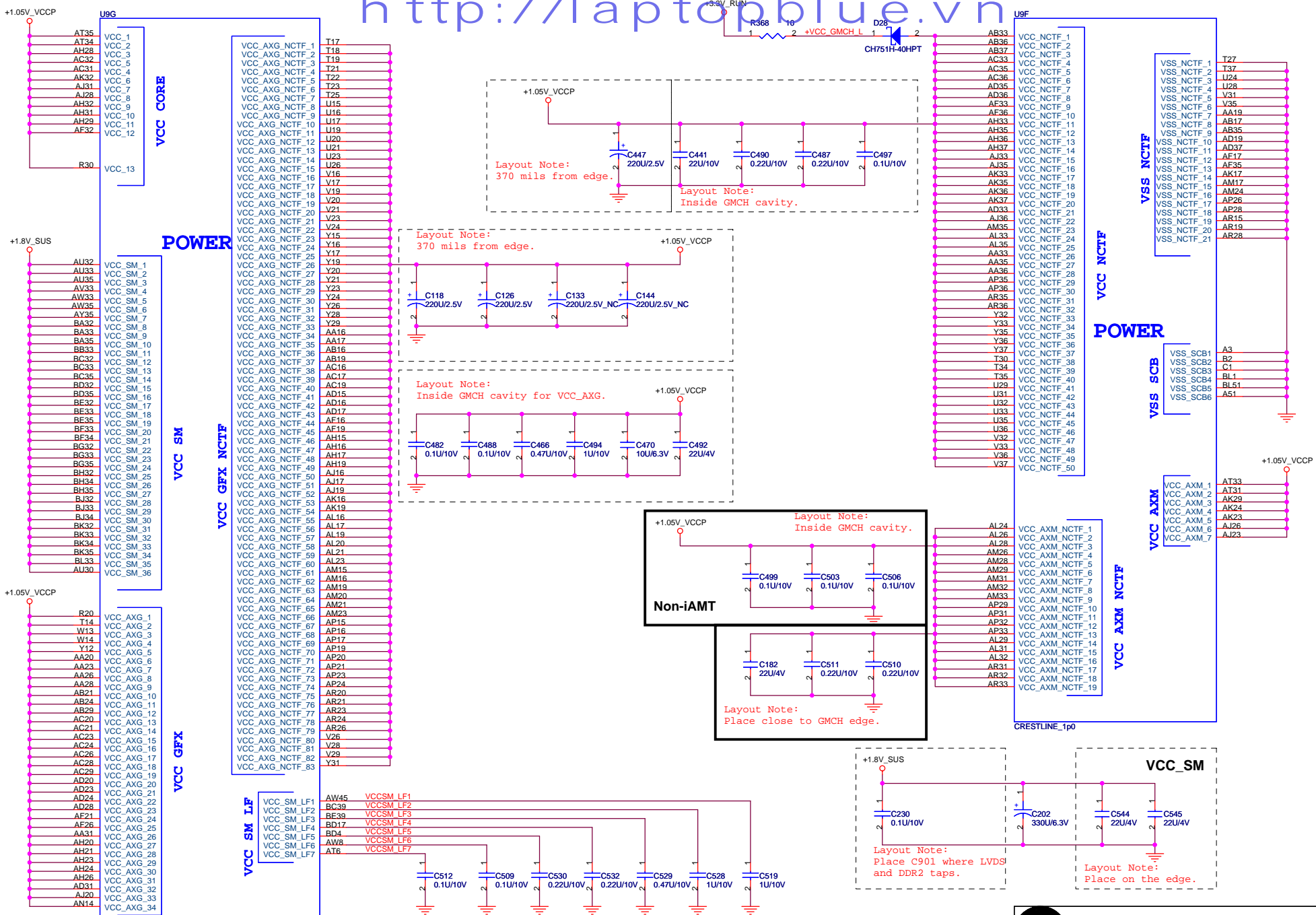
Title: Cresline (VGA,DMI)

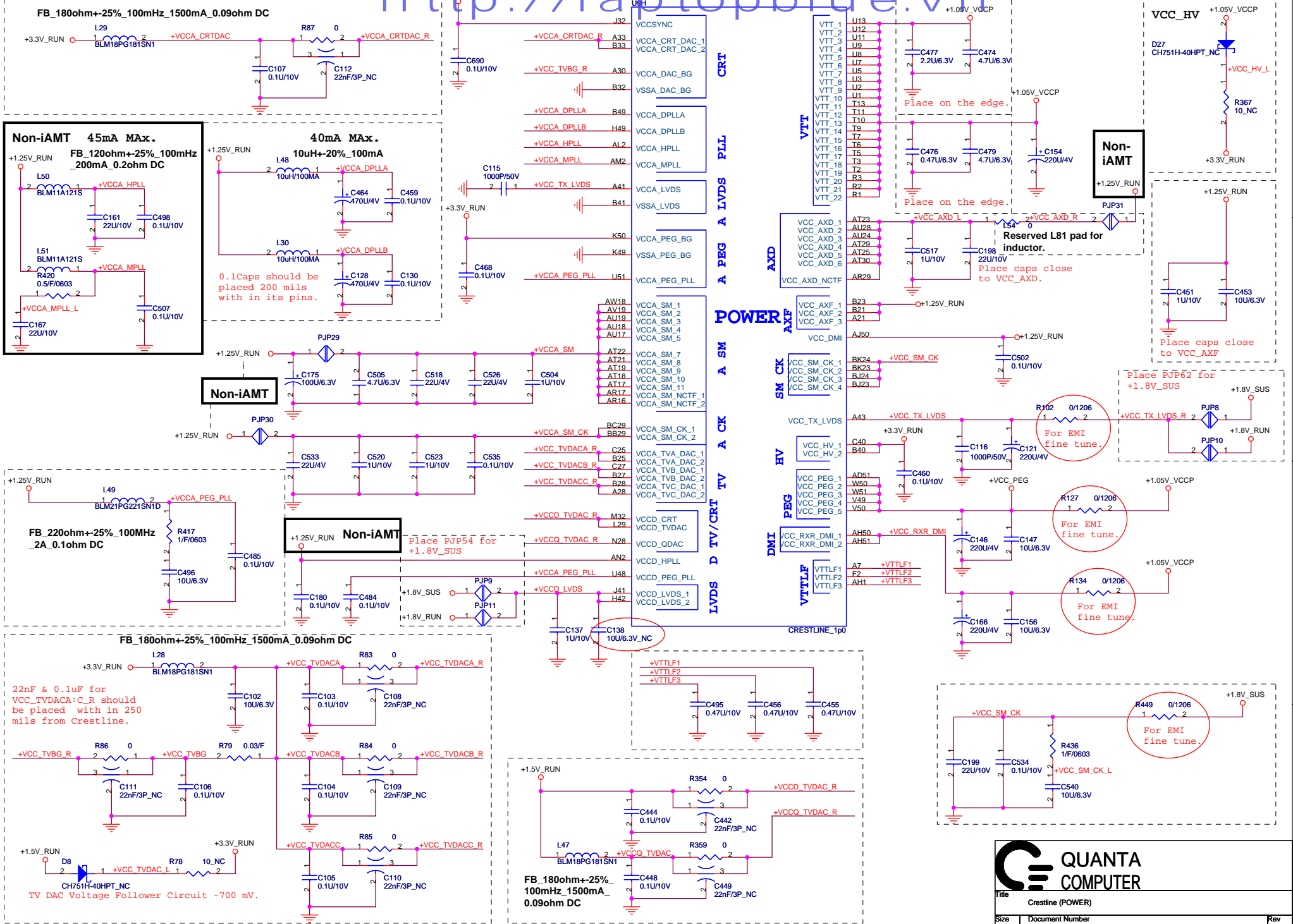
Size	Document Number JM7	Rev	1A
------	---------------------	-----	----

Date: Wednesday, June 28, 2006 Sheet 6 of 57

CFG5	DMI X2 Select	Low=DMiX2 High=DMiX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present





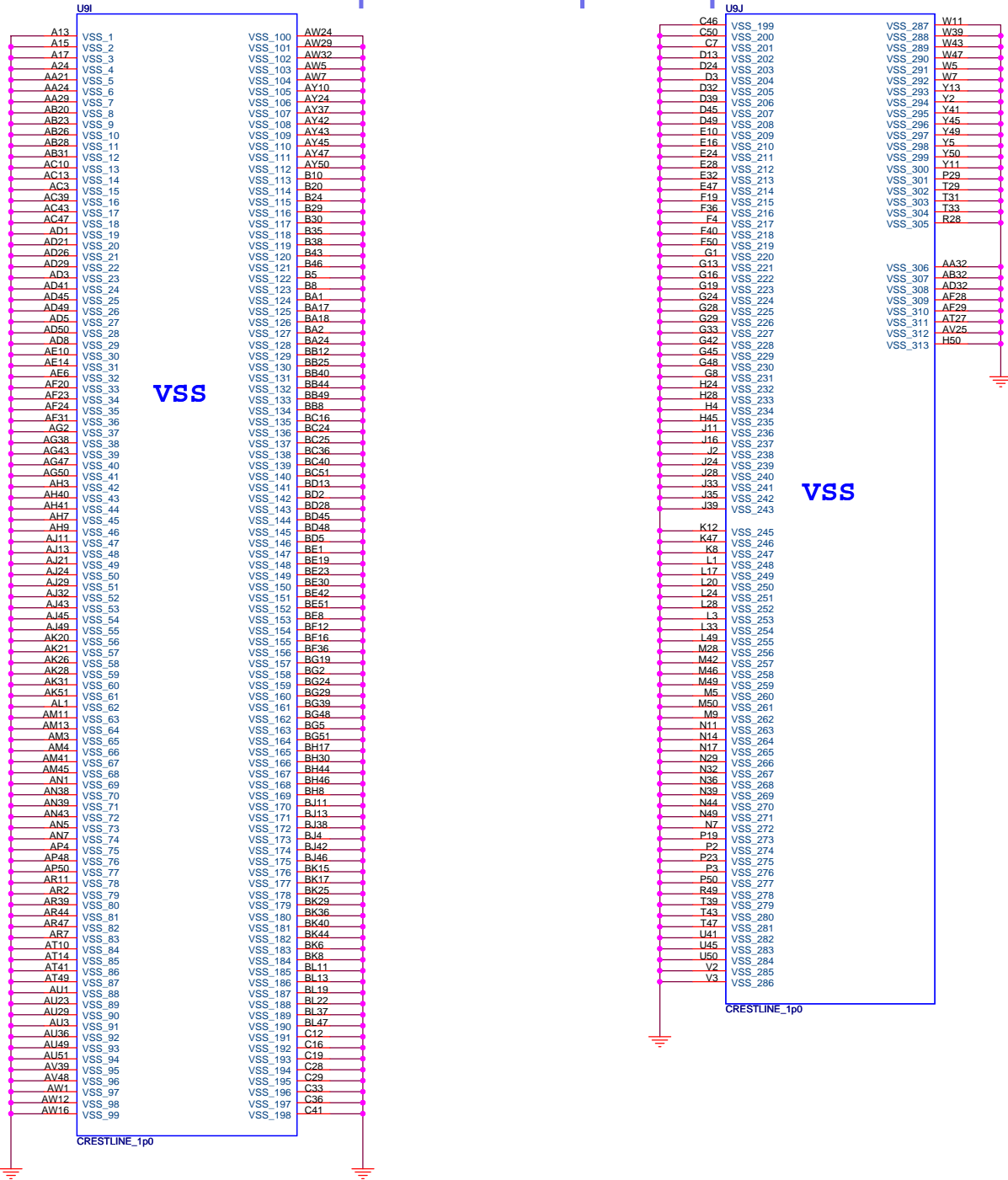


QUANTA COMPUTER

File: Crestline (POWER)

Size: JM7	Document Number: JM7	Rev: 1A
-----------	----------------------	---------

Date: Wednesday, June 28, 2006 Sheet 9 of 57

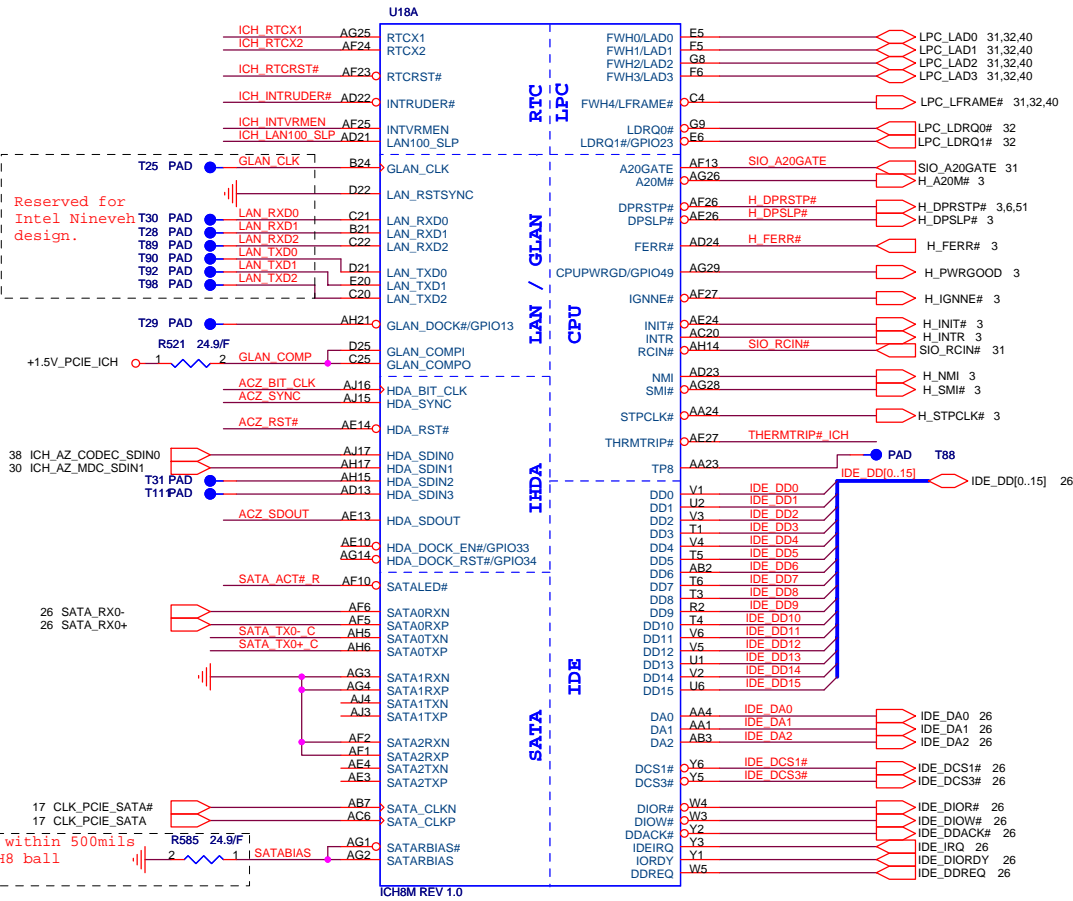
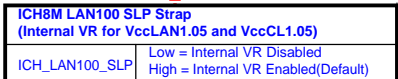
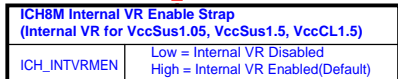
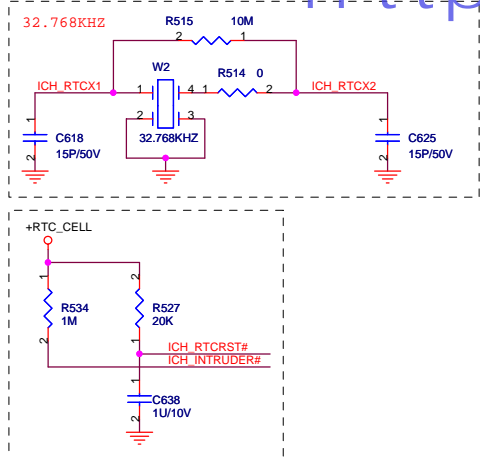


QUANTA COMPUTER

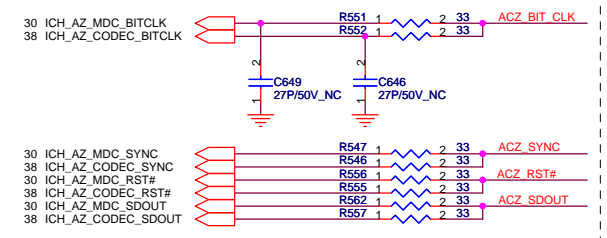
Title: Crestline (VSS)

Size	Document Number	Rev
	JM7	1A

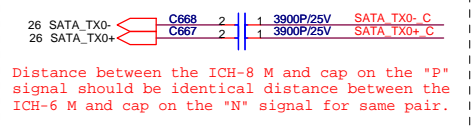
Date: Wednesday, June 28, 2006 Sheet 10 of 57



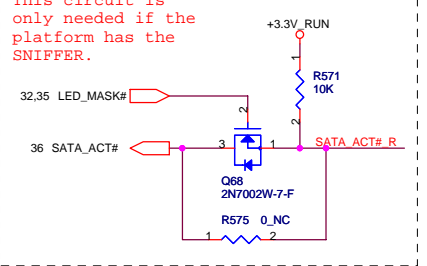
Reserved for Intel Nineveh design.



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

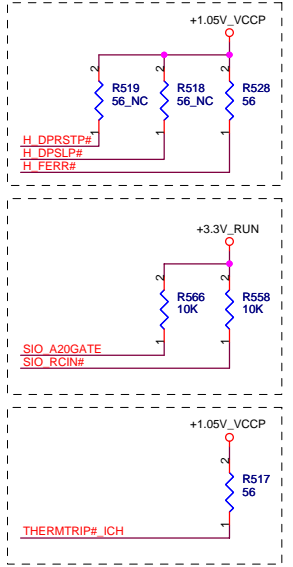
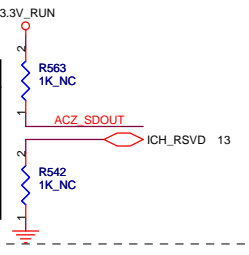


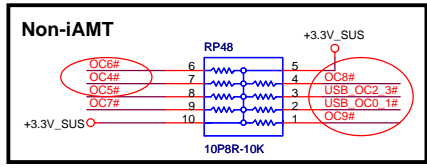
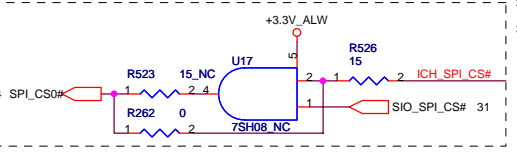
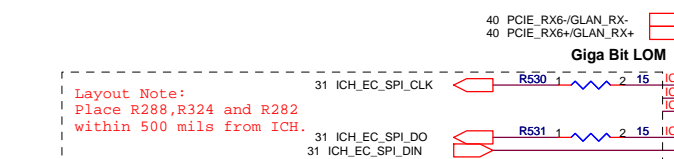
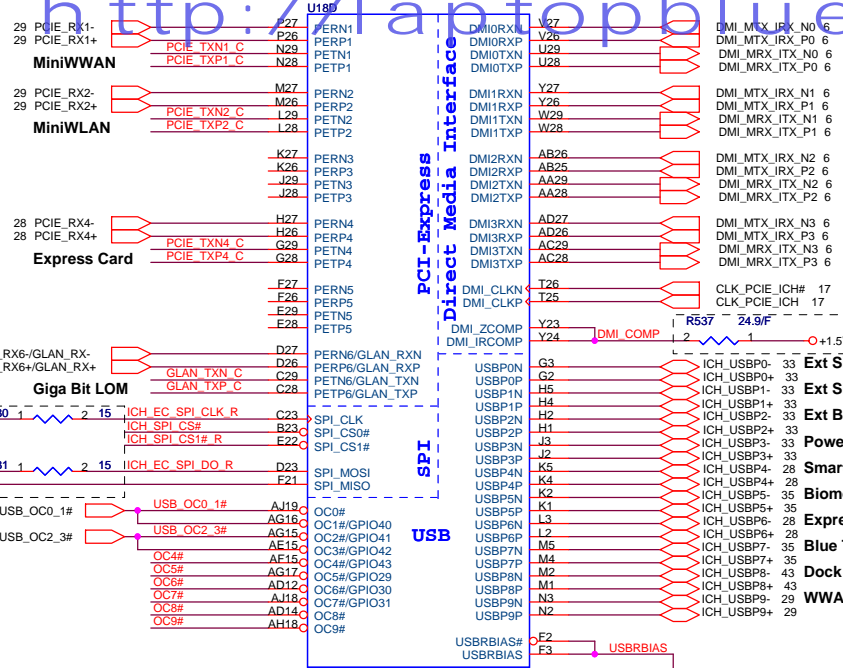
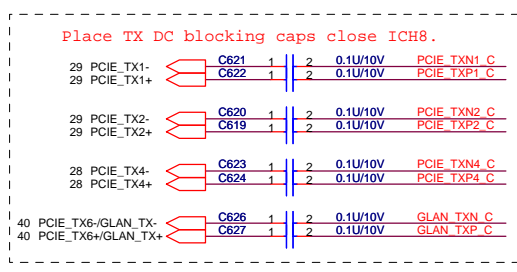
This circuit is only needed if the platform has the SNIFFER.

Place within 500mils of ICH8 ball

XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

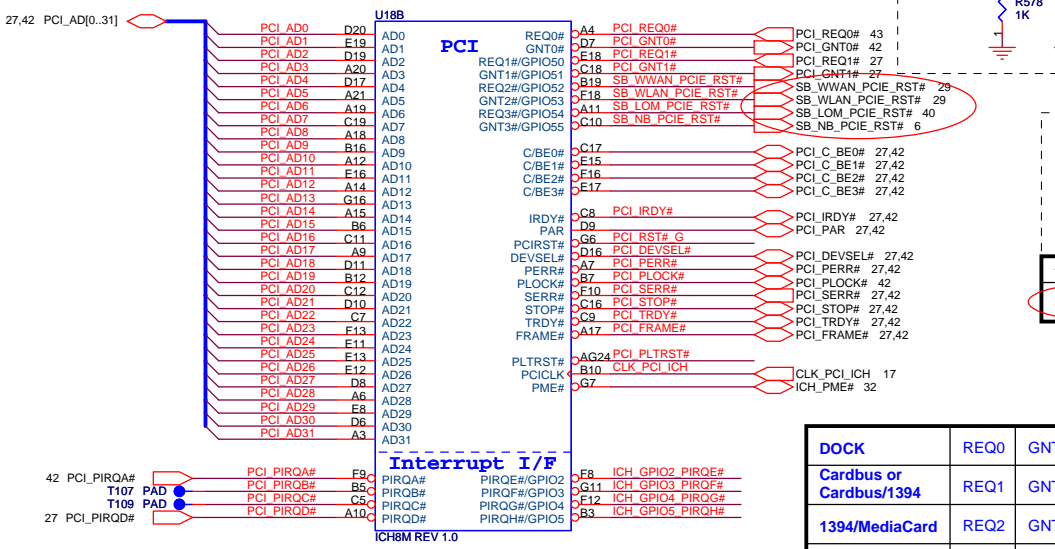




Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

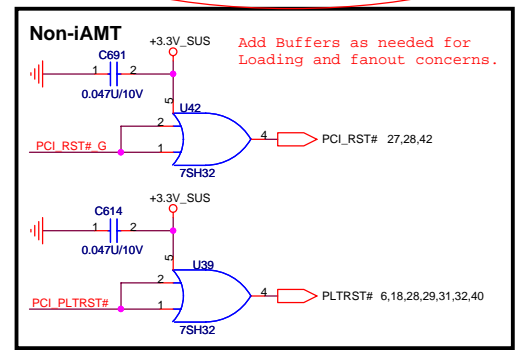
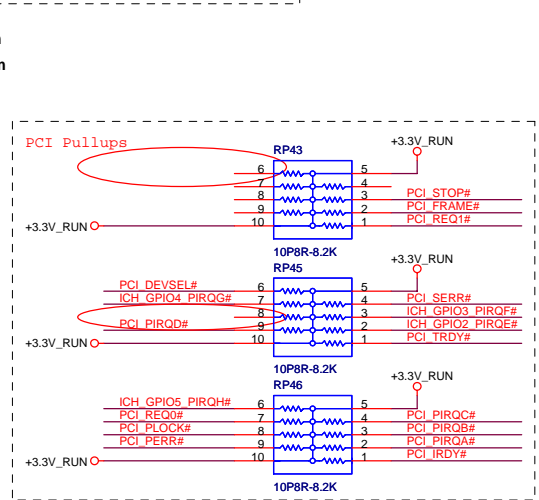
Boot BIOS Strap

	GNT0#	SPI_CS1#
LPC 11	No stuff	No stuff
PCI 10	No stuff	Stuff
SPI 01	Stuff	No stuff



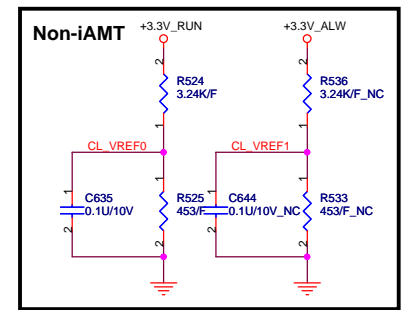
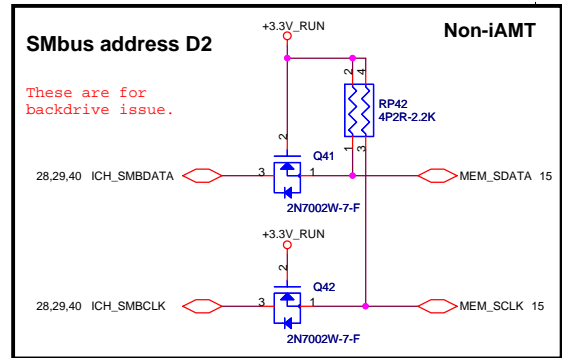
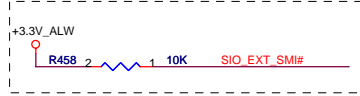
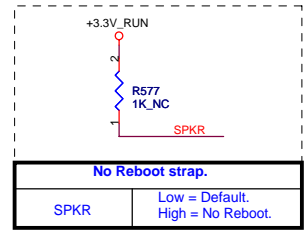
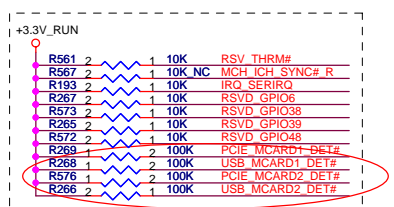
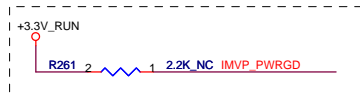
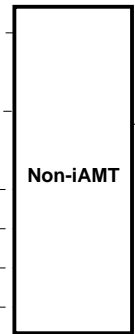
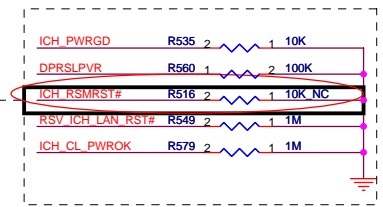
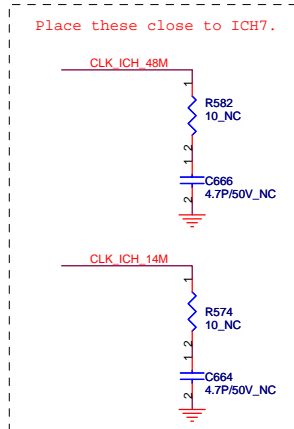
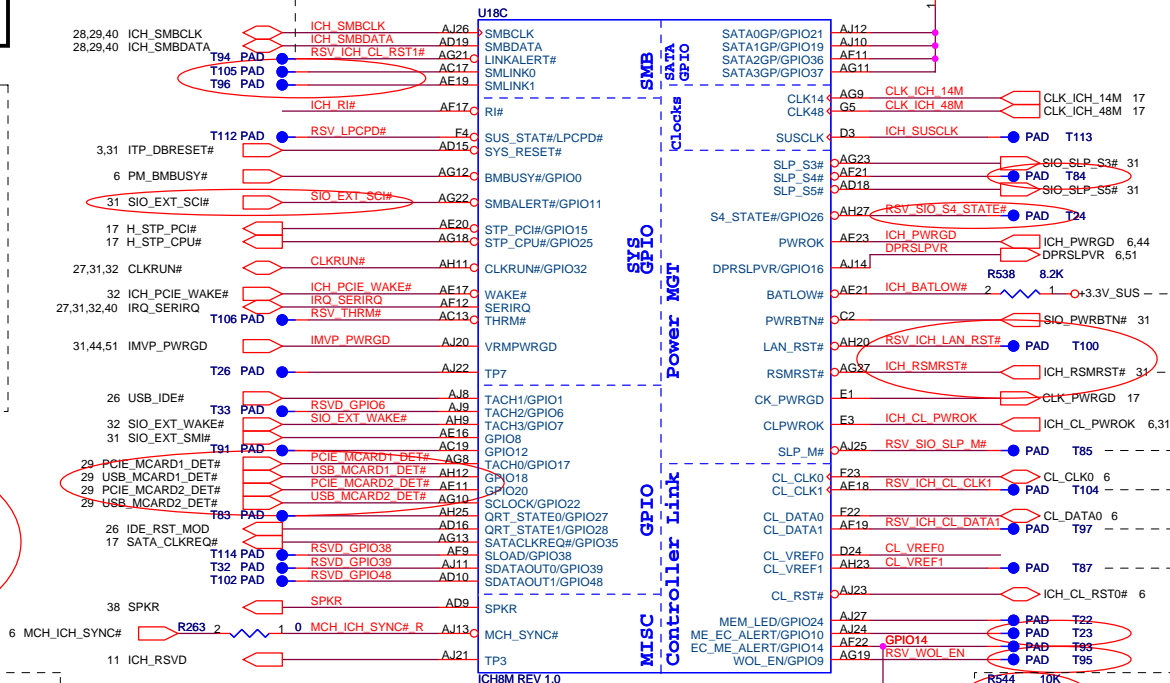
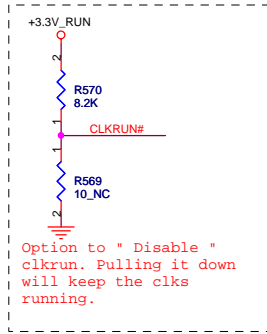
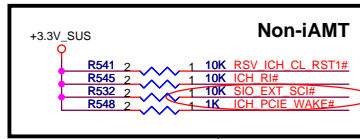
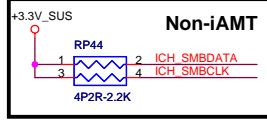
DOCK

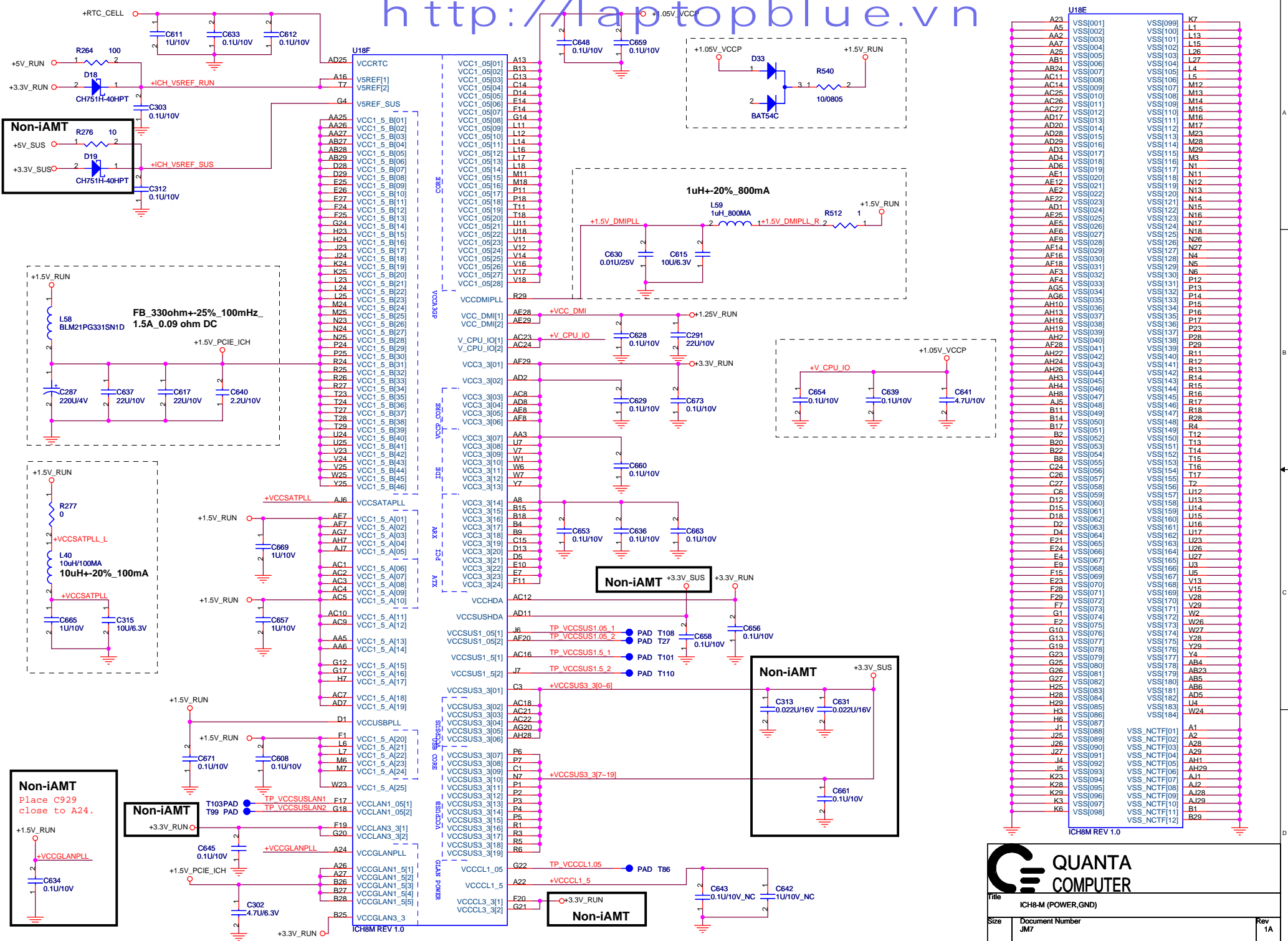
	REQ0	GNT0	PIRQA
Cardbus or Cardbus/1394	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC



A16 away override strap.
 SB_NB_PCIE_RST# Low = A16 swap override enabled. High = Default.

Reserved for EMI. Place resistor and cap close to ICH.





U18E		
A23	VSSJ[001]	VSSJ[099]
A5	VSSJ[002]	VSSJ[100]
AA2	VSSJ[003]	VSSJ[101]
AA7	VSSJ[004]	VSSJ[102]
A25	VSSJ[005]	VSSJ[103]
AB1	VSSJ[006]	VSSJ[104]
AB24	VSSJ[007]	VSSJ[105]
AC11	VSSJ[008]	VSSJ[106]
AC14	VSSJ[009]	VSSJ[107]
AC25	VSSJ[010]	VSSJ[108]
AC26	VSSJ[011]	VSSJ[109]
AC27	VSSJ[012]	VSSJ[110]
AD17	VSSJ[013]	VSSJ[111]
AD20	VSSJ[014]	VSSJ[112]
AD28	VSSJ[015]	VSSJ[113]
AD29	VSSJ[016]	VSSJ[114]
AD3	VSSJ[017]	VSSJ[115]
AD4	VSSJ[018]	VSSJ[116]
AD6	VSSJ[019]	VSSJ[117]
AE1	VSSJ[020]	VSSJ[118]
AE12	VSSJ[021]	VSSJ[119]
AE2	VSSJ[022]	VSSJ[120]
AE22	VSSJ[023]	VSSJ[121]
AD1	VSSJ[024]	VSSJ[122]
AE25	VSSJ[025]	VSSJ[123]
AE5	VSSJ[026]	VSSJ[124]
AE6	VSSJ[027]	VSSJ[125]
AE9	VSSJ[028]	VSSJ[126]
AF14	VSSJ[029]	VSSJ[127]
AF16	VSSJ[030]	VSSJ[128]
AF18	VSSJ[031]	VSSJ[129]
AF3	VSSJ[032]	VSSJ[130]
AF4	VSSJ[033]	VSSJ[131]
AG5	VSSJ[034]	VSSJ[132]
AG6	VSSJ[035]	VSSJ[133]
AH10	VSSJ[036]	VSSJ[134]
AH13	VSSJ[037]	VSSJ[135]
AH16	VSSJ[038]	VSSJ[136]
AH19	VSSJ[039]	VSSJ[137]
AH2	VSSJ[040]	VSSJ[138]
AF28	VSSJ[041]	VSSJ[139]
AH22	VSSJ[042]	VSSJ[140]
AH24	VSSJ[043]	VSSJ[141]
AH26	VSSJ[044]	VSSJ[142]
AH3	VSSJ[045]	VSSJ[143]
AH4	VSSJ[046]	VSSJ[144]
AJ5	VSSJ[047]	VSSJ[145]
B11	VSSJ[048]	VSSJ[146]
B14	VSSJ[049]	VSSJ[147]
B17	VSSJ[050]	VSSJ[148]
B2	VSSJ[051]	VSSJ[149]
B20	VSSJ[052]	VSSJ[150]
VCC3_3[08]	VSSJ[053]	VSSJ[151]
VSSJ[054]	VSSJ[054]	VSSJ[152]
B8	VSSJ[055]	VSSJ[153]
C24	VSSJ[056]	VSSJ[154]
C26	VSSJ[057]	VSSJ[155]
C27	VSSJ[058]	VSSJ[156]
C6	VSSJ[059]	VSSJ[157]
D12	VSSJ[060]	VSSJ[158]
D15	VSSJ[061]	VSSJ[159]
D18	VSSJ[062]	VSSJ[160]
D2	VSSJ[063]	VSSJ[161]
D4	VSSJ[064]	VSSJ[162]
E21	VSSJ[065]	VSSJ[163]
E24	VSSJ[066]	VSSJ[164]
E4	VSSJ[067]	VSSJ[165]
E9	VSSJ[068]	VSSJ[166]
F15	VSSJ[069]	VSSJ[167]
E23	VSSJ[070]	VSSJ[168]
F28	VSSJ[071]	VSSJ[169]
F29	VSSJ[072]	VSSJ[170]
F7	VSSJ[073]	VSSJ[171]
G1	VSSJ[074]	VSSJ[172]
E2	VSSJ[075]	VSSJ[173]
G10	VSSJ[076]	VSSJ[174]
G13	VSSJ[077]	VSSJ[175]
G19	VSSJ[078]	VSSJ[176]
G23	VSSJ[079]	VSSJ[177]
G25	VSSJ[080]	VSSJ[178]
G26	VSSJ[081]	VSSJ[179]
G27	VSSJ[082]	VSSJ[180]
H25	VSSJ[083]	VSSJ[181]
H28	VSSJ[084]	VSSJ[182]
H29	VSSJ[085]	VSSJ[183]
H3	VSSJ[086]	VSSJ[184]
H6	VSSJ[087]	VSSJ[184]
J1	VSSJ[088]	VSS_NCTFF[01]
J25	VSSJ[089]	VSS_NCTFF[02]
J26	VSSJ[090]	VSS_NCTFF[03]
J27	VSSJ[091]	VSS_NCTFF[04]
J4	VSSJ[092]	VSS_NCTFF[05]
J5	VSSJ[093]	VSS_NCTFF[06]
K23	VSSJ[094]	VSS_NCTFF[07]
K28	VSSJ[095]	VSS_NCTFF[08]
P2	VSSJ[096]	VSS_NCTFF[09]
K29	VSSJ[097]	VSS_NCTFF[10]
K3	VSSJ[098]	VSS_NCTFF[11]
K6	VSSJ[099]	VSS_NCTFF[12]

QUANTA COMPUTER

File: ICH8-M (POWER.GND)

Size: Document Number JM7

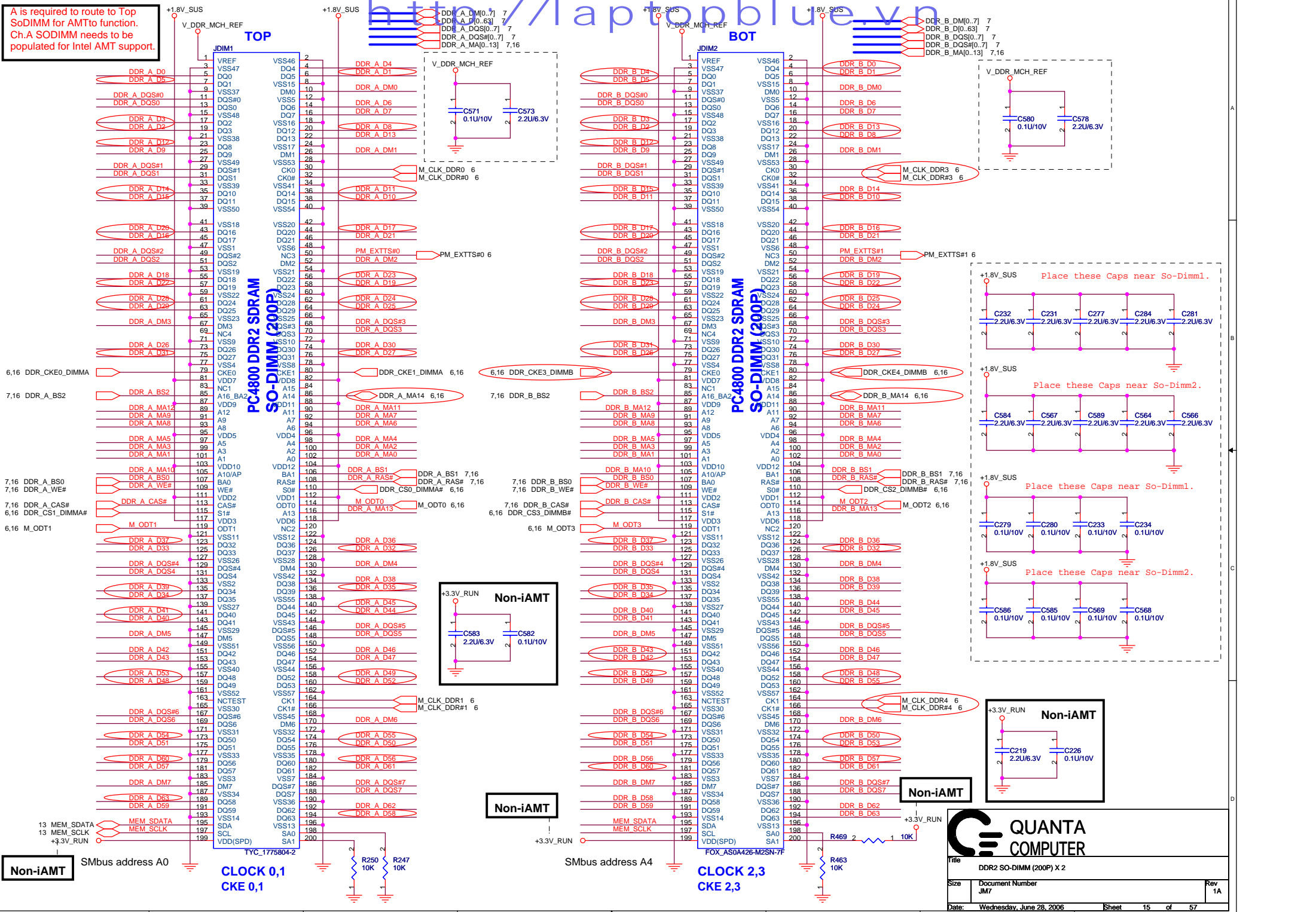
Date: Wednesday, June 28, 2006

Sheet: 14 of 57

Rev: 1A

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

http://laptopblue.vn



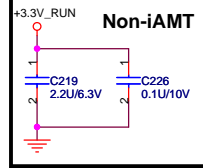
Non-iAMT

CLOCK 0,1
CKE 0,1

Non-iAMT

CLOCK 2,3
CKE 2,3

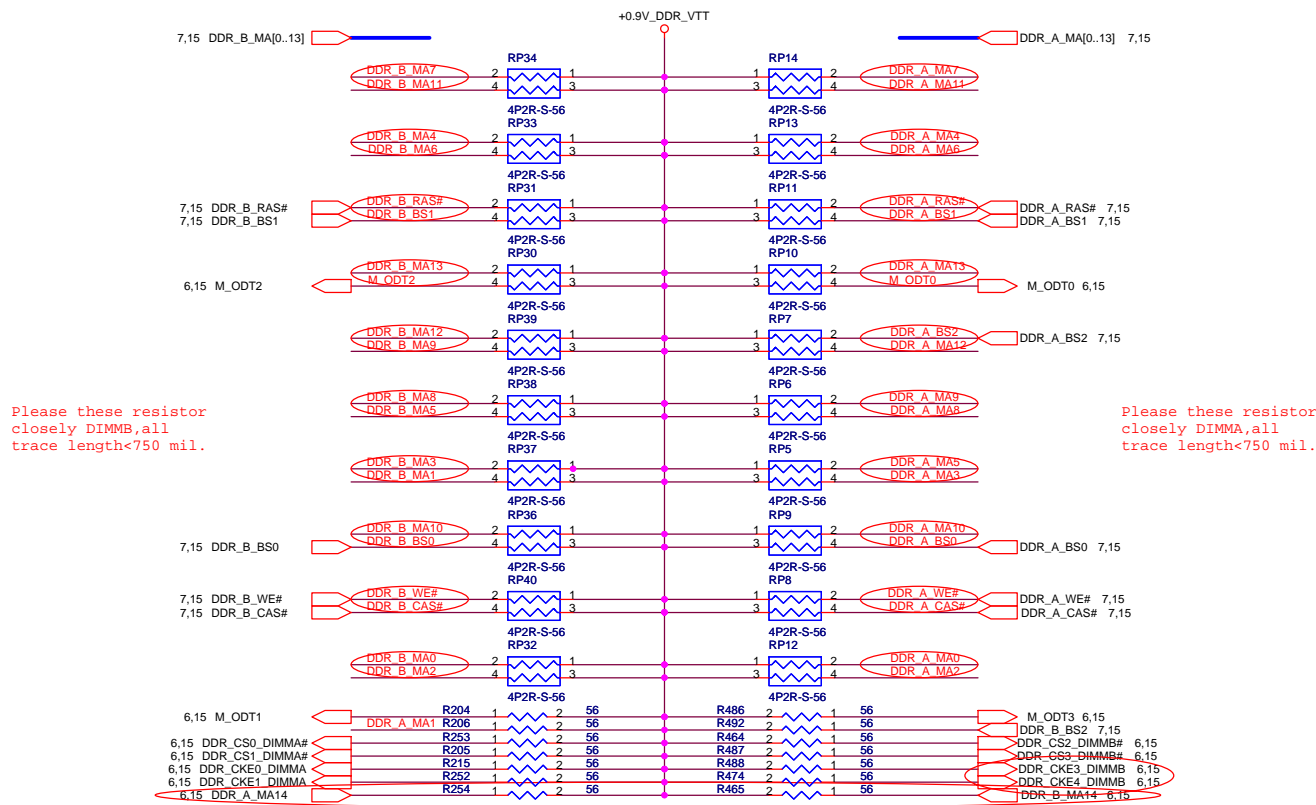
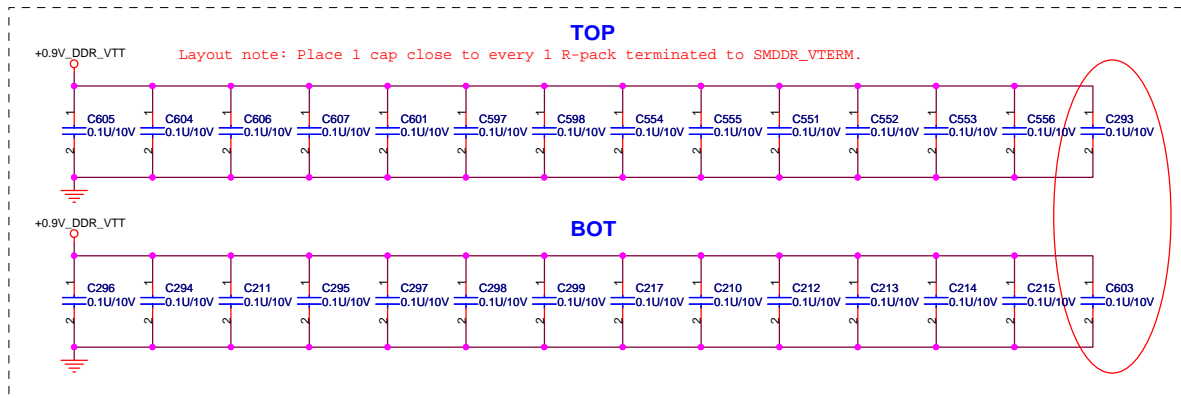
Non-iAMT

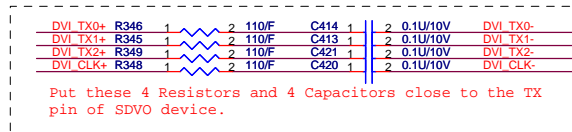
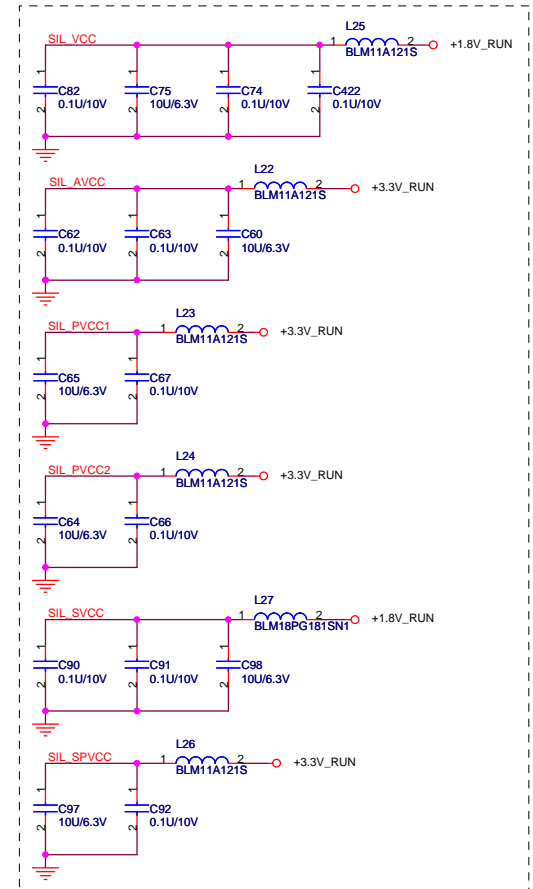
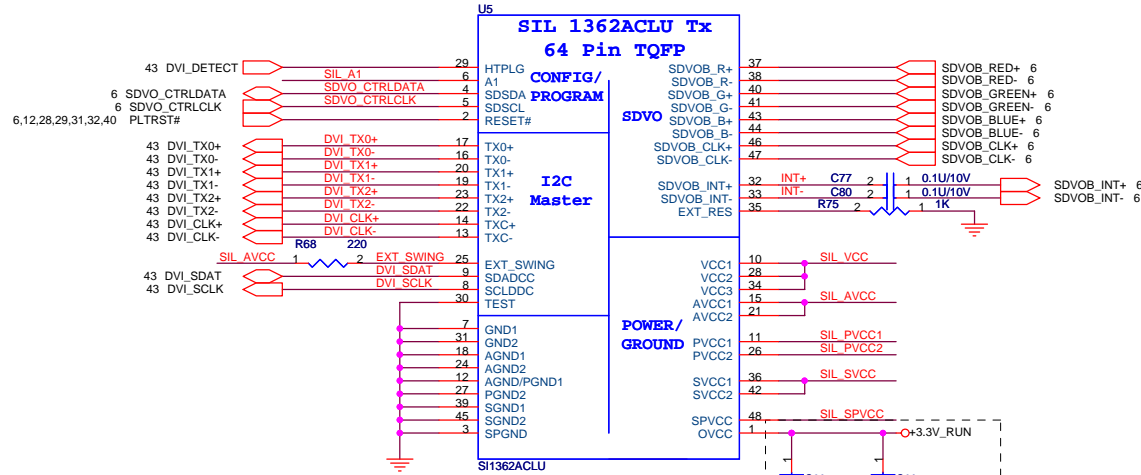
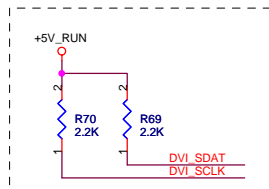
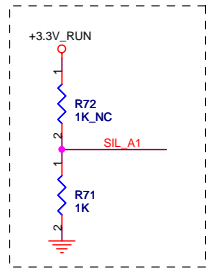
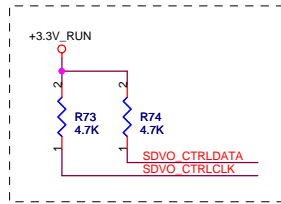


QUANTA COMPUTER


Title: DDR2 SO-DIMM (200P) X 2

Size	Document Number JM7	Rev 1A
Date:	Wednesday, June 28, 2006	Sheet 15 of 57






**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**


 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	JM7	1A
Date: Monday, June 26, 2006		
Sheet 19 of 57		

<http://laptopblue.vn>

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**


 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	JM7	1A
Date:	Monday, June 26, 2006	Sheet 20 of 57

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	JM7	1A
Date:	Monday, June 26, 2006	Sheet 21 of 57


<http://laptopblue.vn>

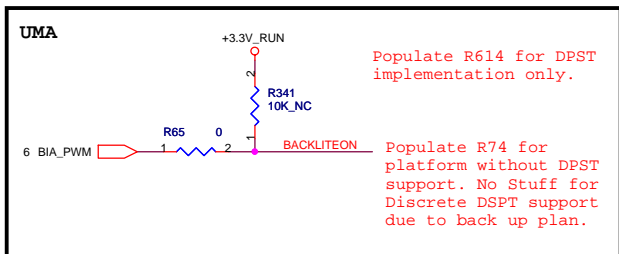
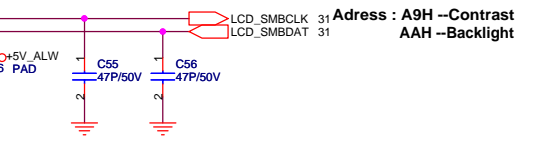
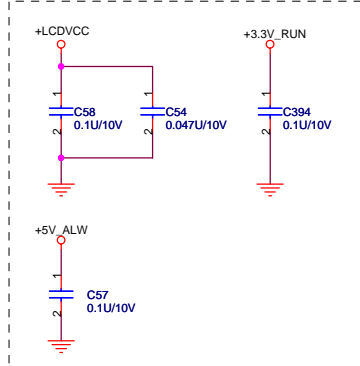
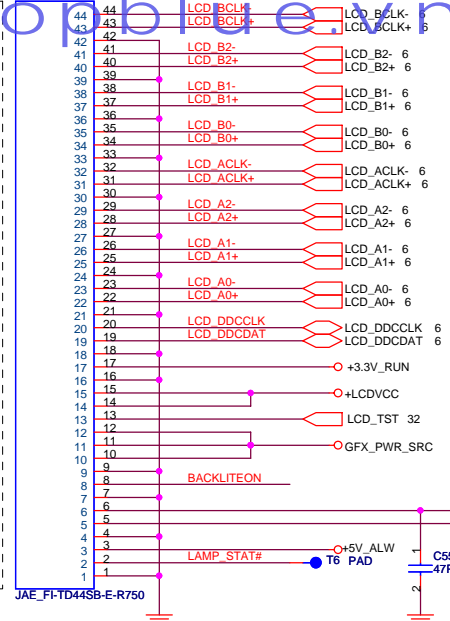
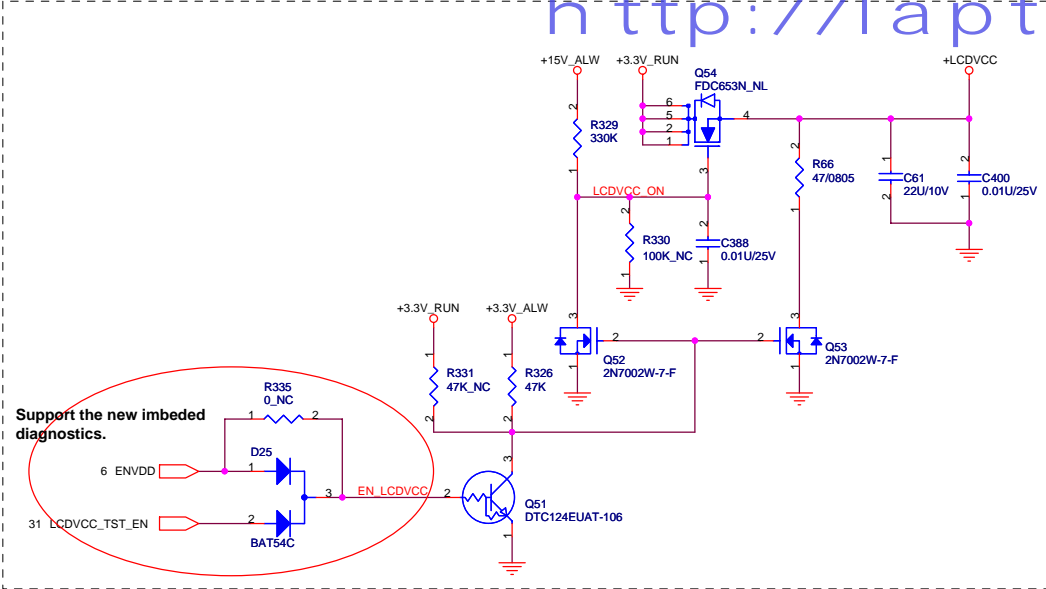
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	JM7	1A
Date:	Monday, June 26, 2006	Sheet 22 of 57

<http://laptopblue.vn>

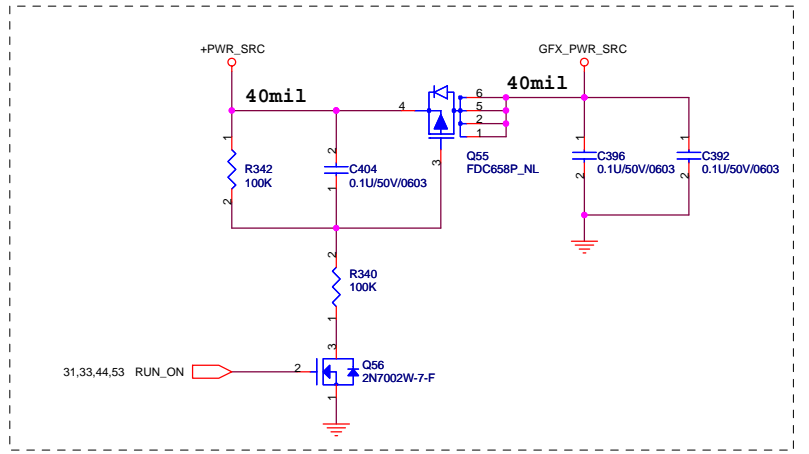
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

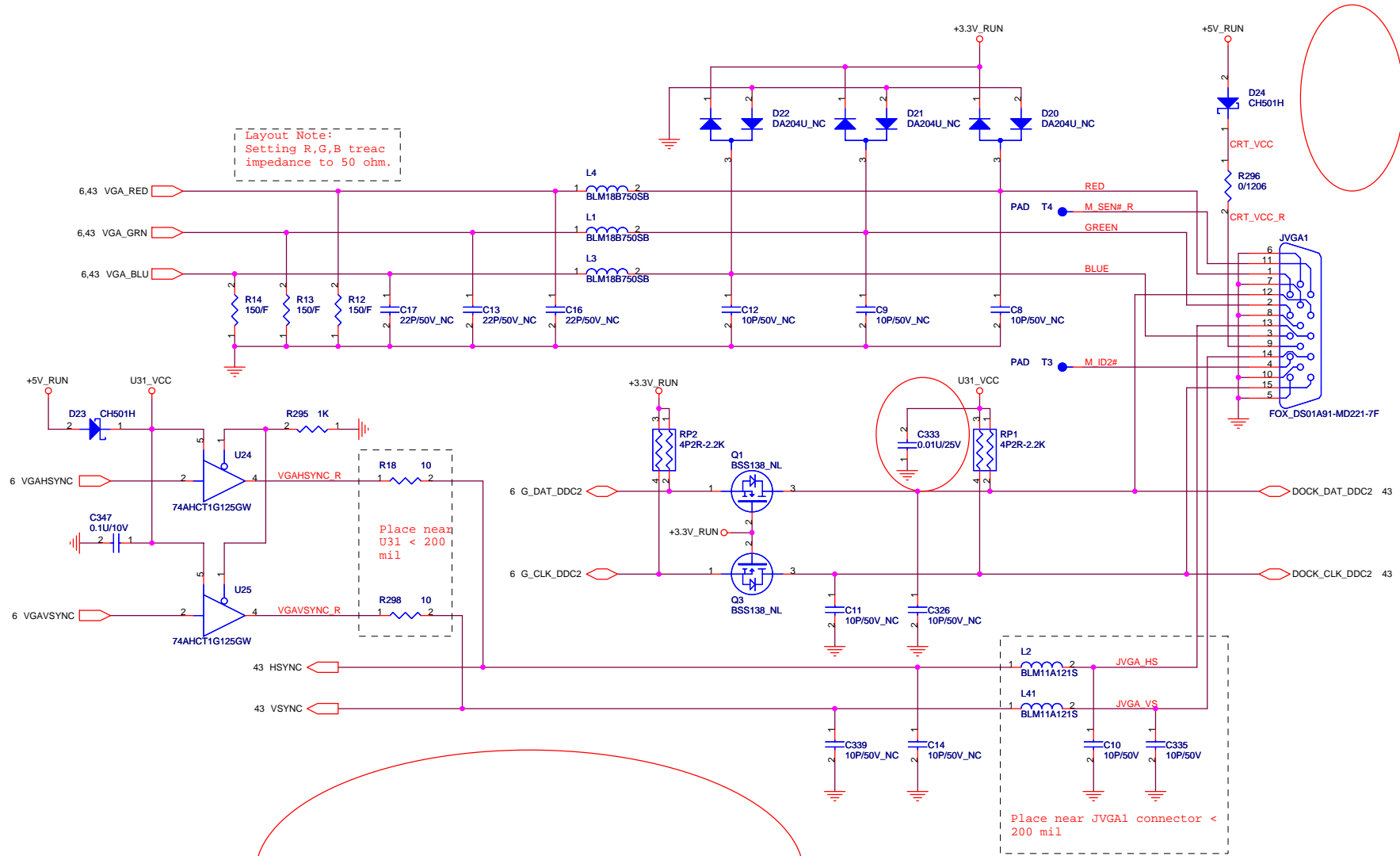
 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	JM7	1A
Date:	Monday, June 26, 2006	Sheet 23 of 57



Shunt capacitors on LVDS for improving WWAN.

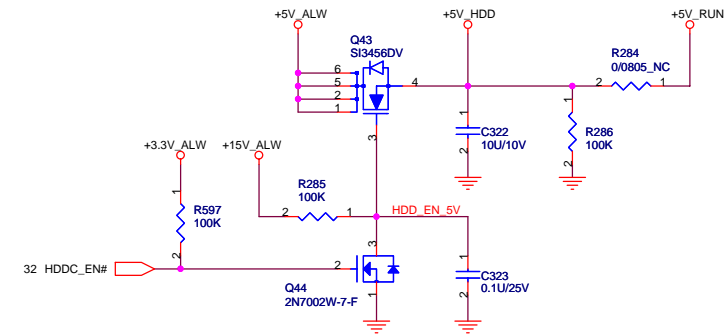
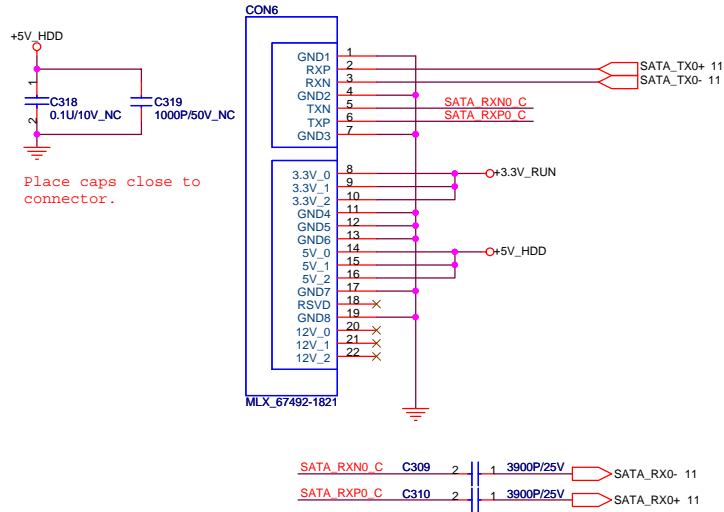
LCD B0-	C399	1	2	3.3P/50V NC	LCD B0+
LCD B1-	C398	1	2	3.3P/50V NC	LCD B1+
LCD B2-	C384	1	2	3.3P/50V NC	LCD B2+
LCD BCLK-	C386	1	2	3.3P/50V NC	LCD BCLK+
LCD A0-	C403	1	2	3.3P/50V NC	LCD A0+
LCD A1-	C402	1	2	3.3P/50V NC	LCD A1+
LCD A2-	C397	1	2	3.3P/50V NC	LCD A2+
LCD ACLK-	C393	1	2	3.3P/50V NC	LCD ACLK+



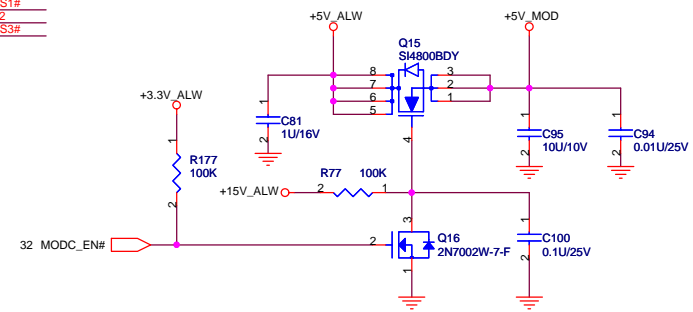
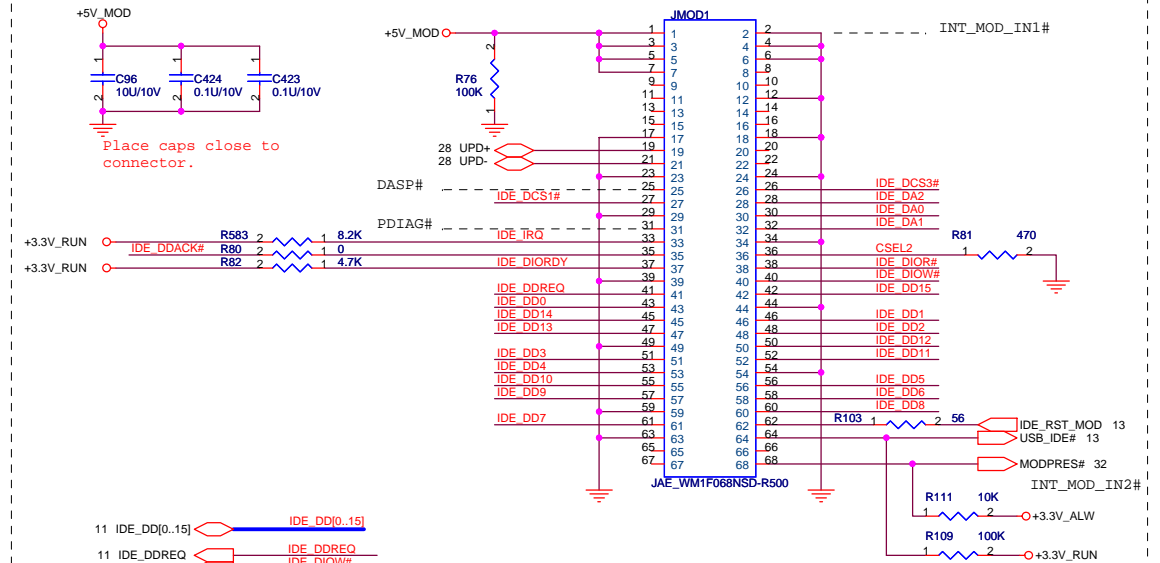


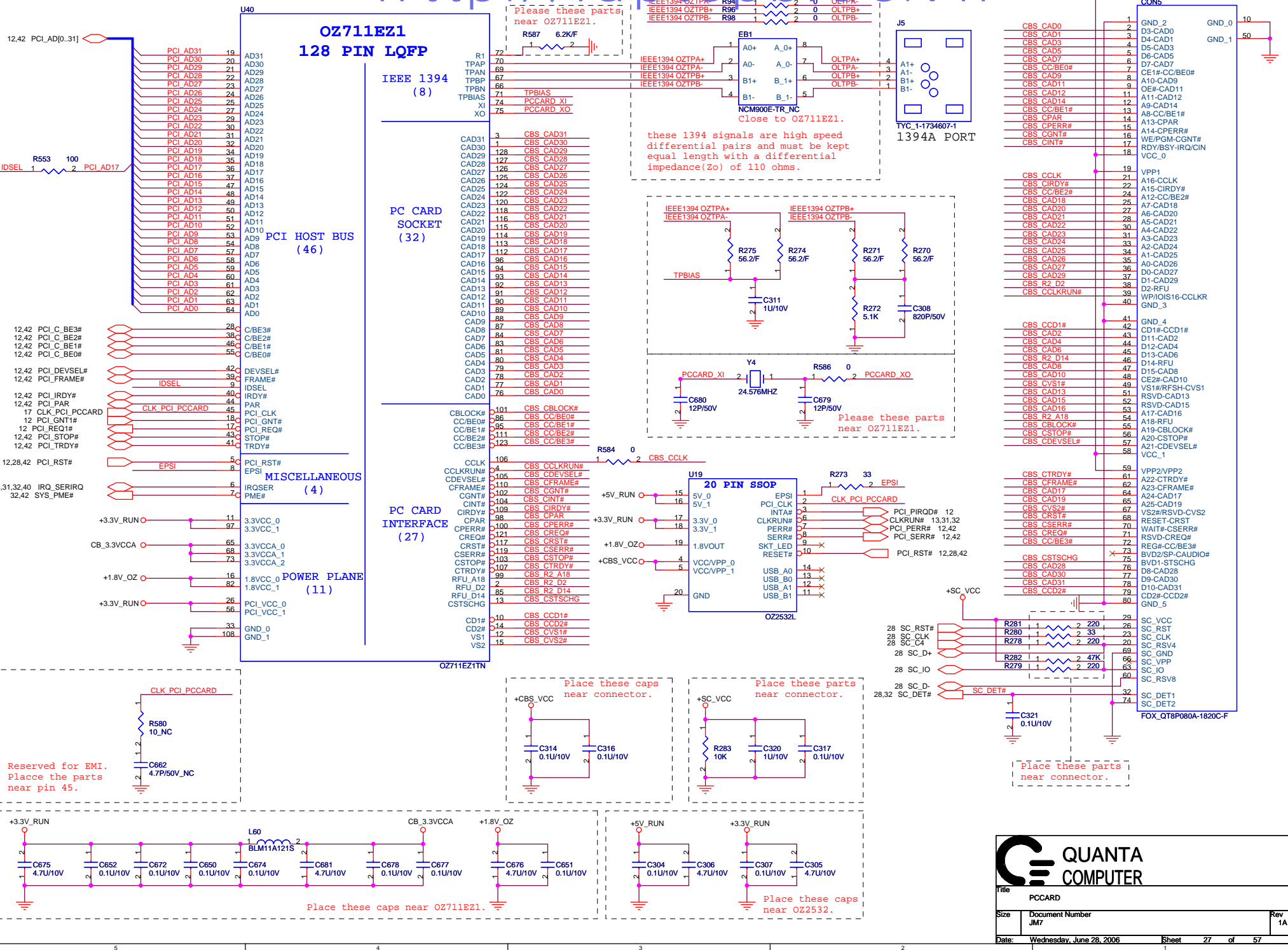
Title		CRT&TV CONN
Size	Document Number	Rev
	JM7	1A
Date:	Wednesday, June 28, 2006	Sheet 25 of 57

SATA Connector.



ODD Connector.

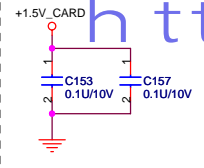
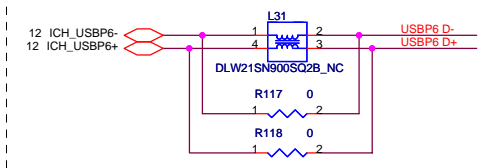




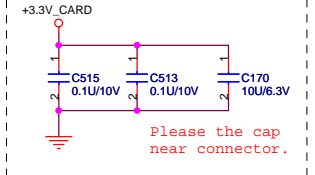
QUANTA COMPUTER

Title: PCCARD
Size: Document Number JM7
Date: Wednesday, June 28, 2006
Sheet: 27 of 57
Rev: 1A

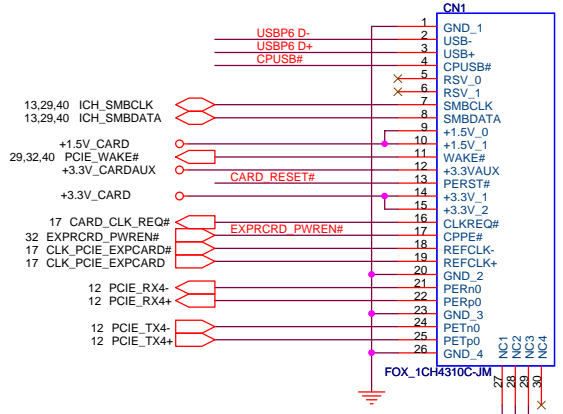
+1.5V_CARD Max. 650mA, Average 500mA.
 +3V_CARD Max. 1300mA, Average 1000mA.



Please the cap near connector.

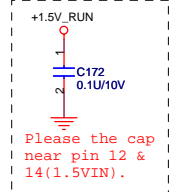
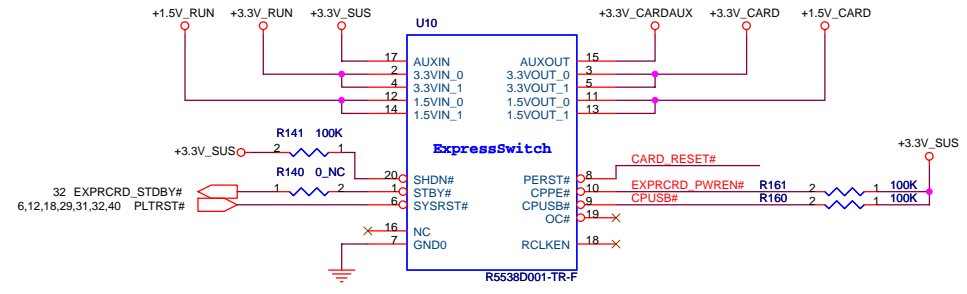


Please the cap near connector.

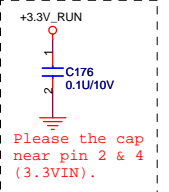


JAE PX10FS16PH-26P

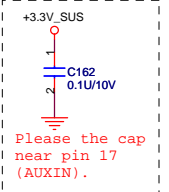
PCI-Express TX and RX direct to connector.



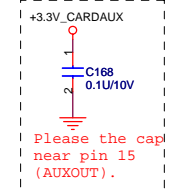
Please the cap near pin 12 & 14 (1.5VIN).



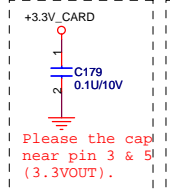
Please the cap near pin 2 & 4 (3.3VIN).



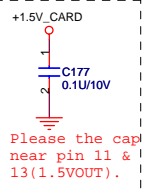
Please the cap near pin 17 (AUXIN).



Please the cap near pin 15 (AUXOUT).



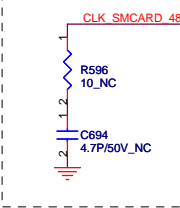
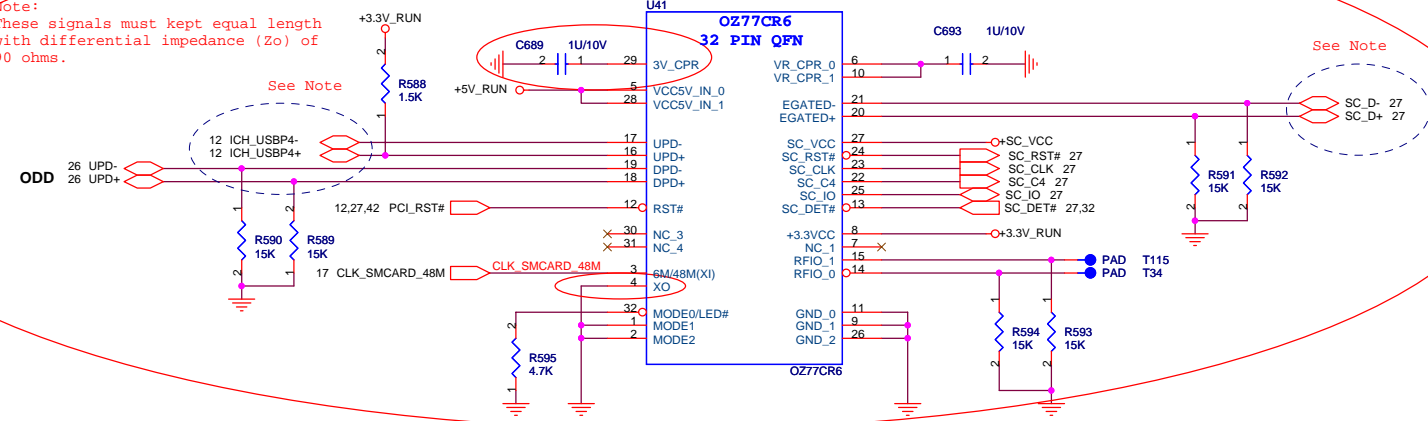
Please the cap near pin 3 & 5 (3.3VOUT).



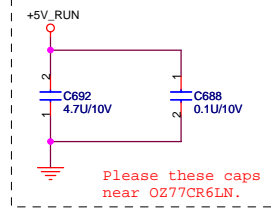
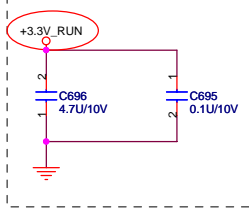
Please the cap near pin 11 & 13 (1.5VOUT).

Smart Card

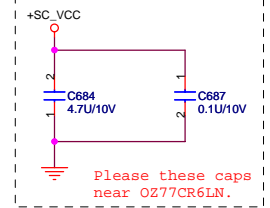
Note:
 These signals must kept equal length with differential impedance (Z_0) of 90 ohms.



Reserved for EMI. Place the parts near pin 45.

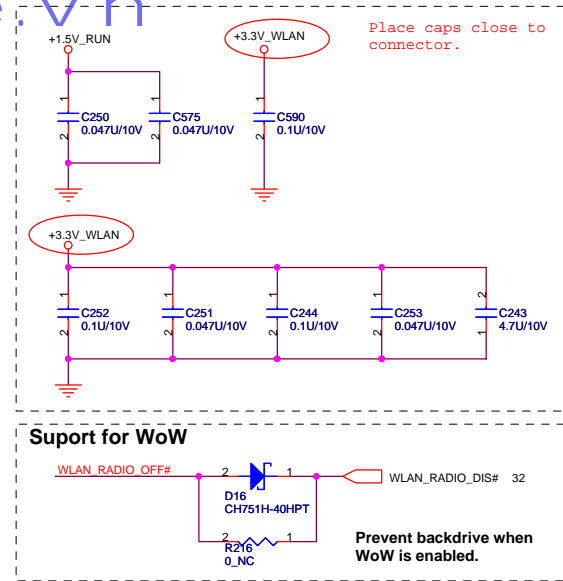
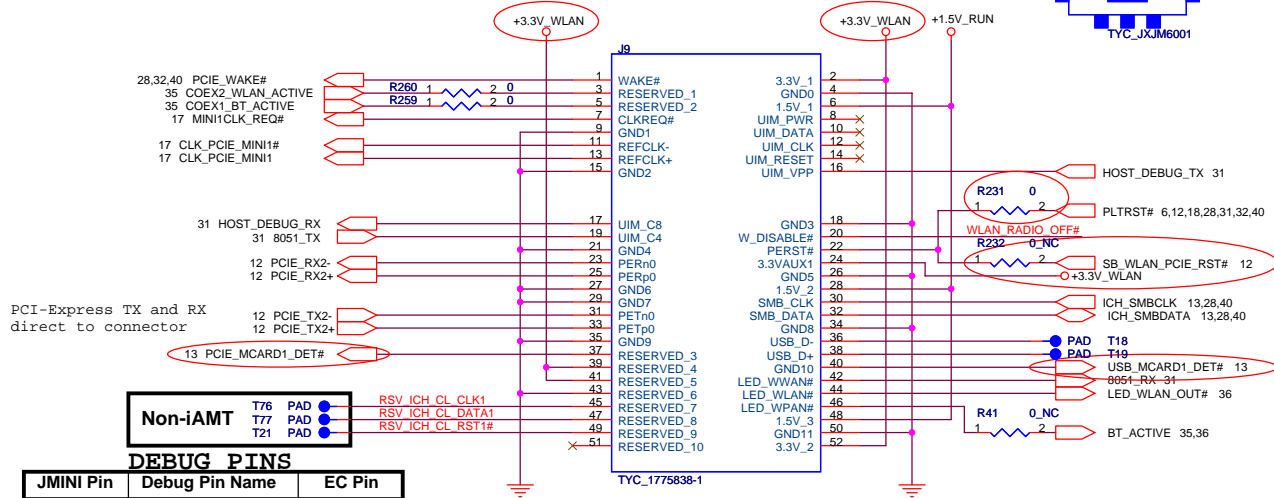


Please these caps near OZ77CR6LN.

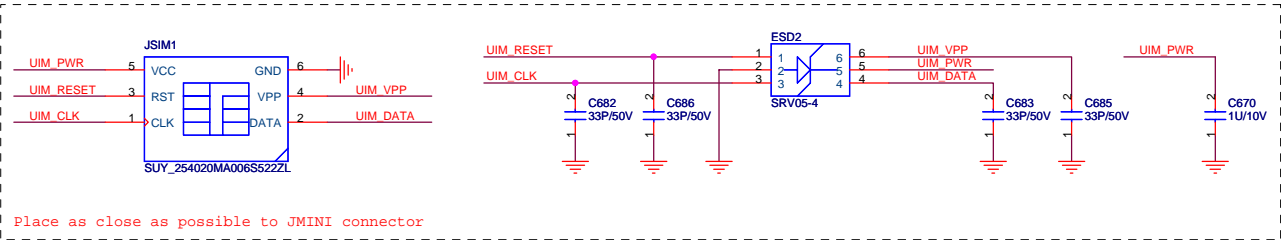
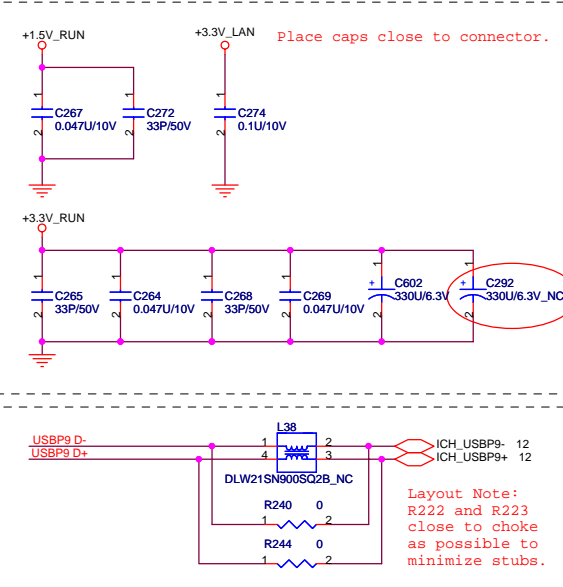
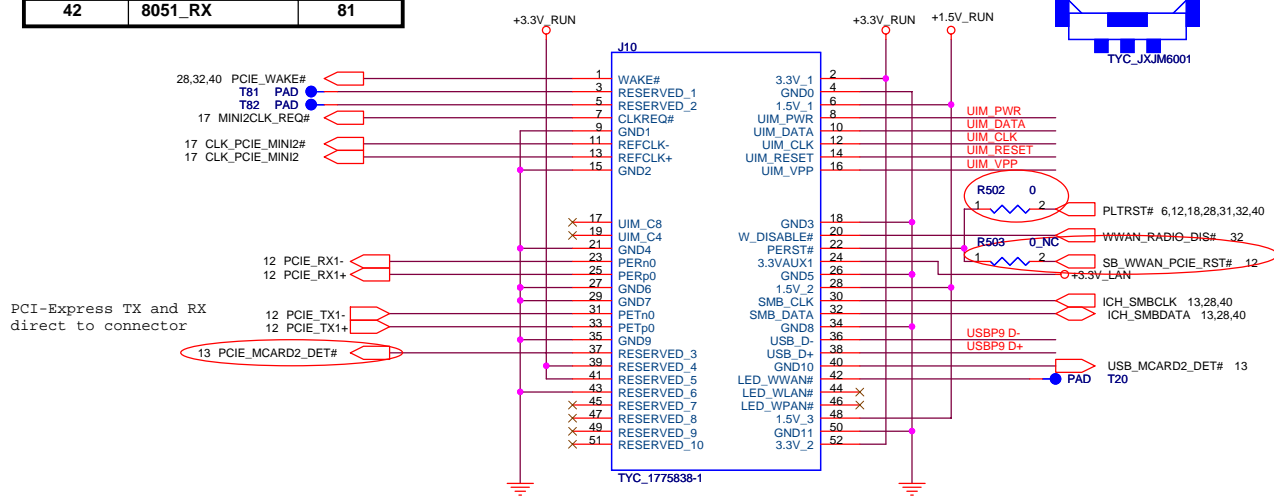


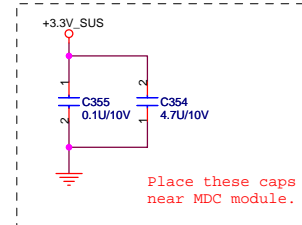
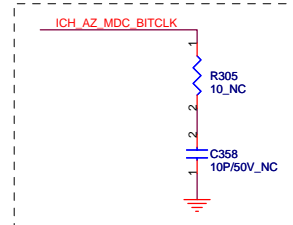
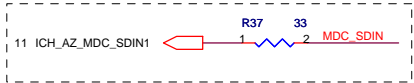
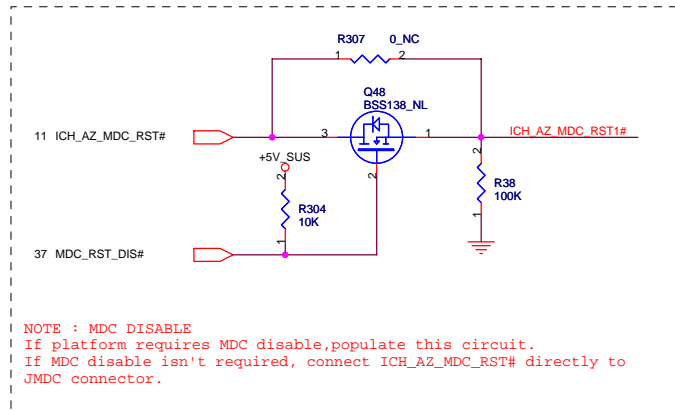
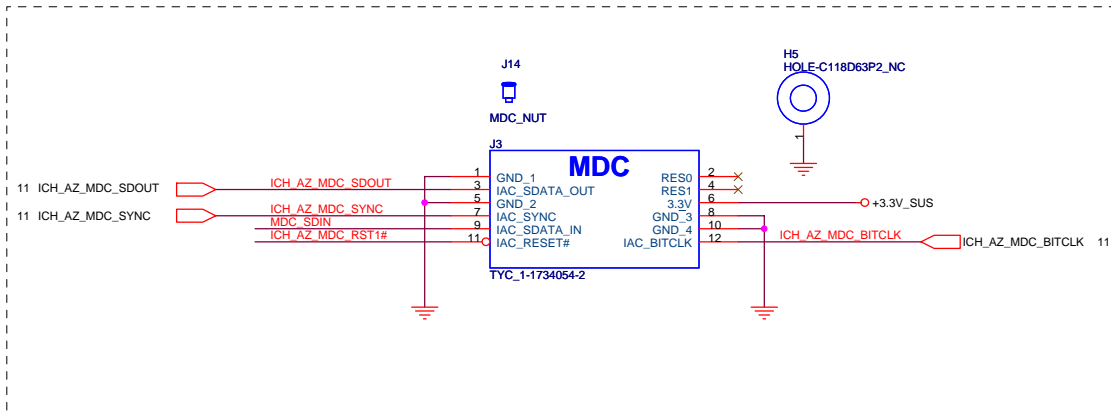
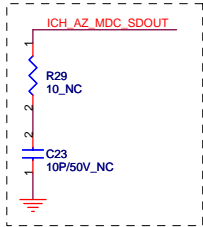
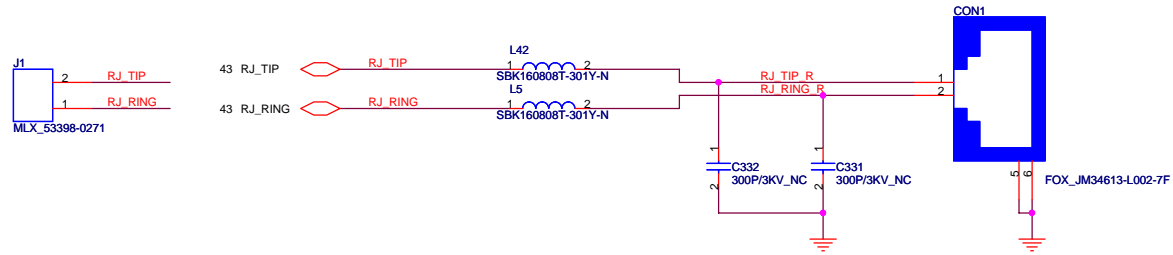
Please these caps near OZ77CR6LN.

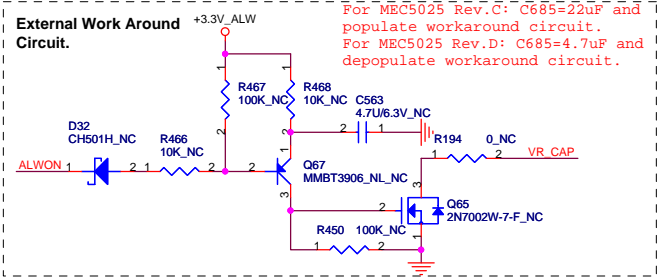
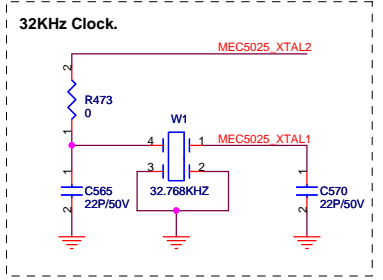
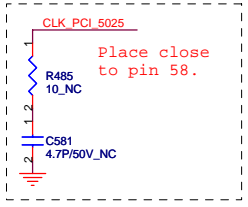
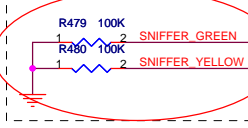
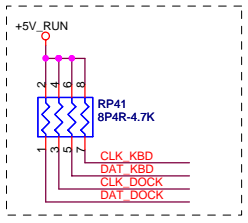
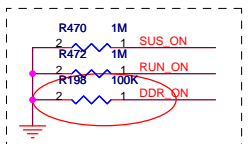




MiniCard WWAN connector

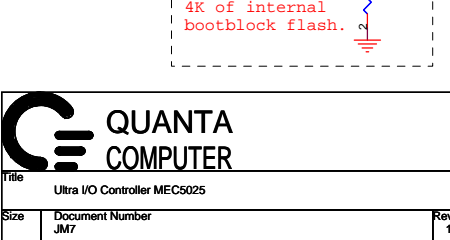
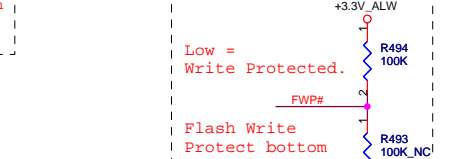
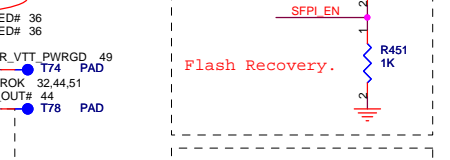
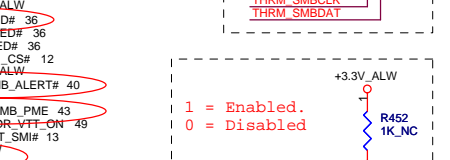
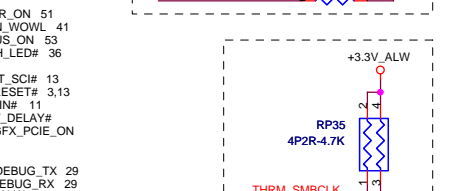
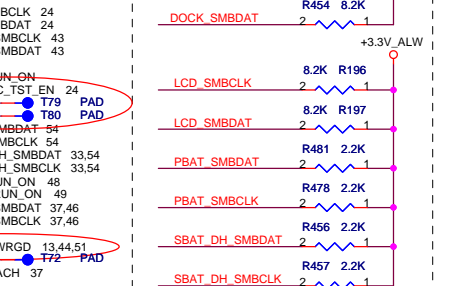
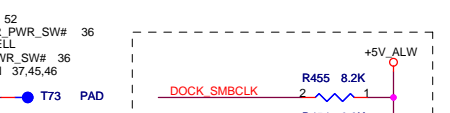
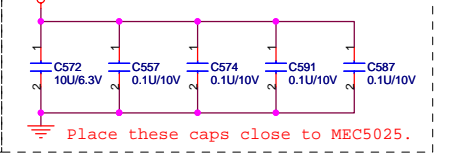
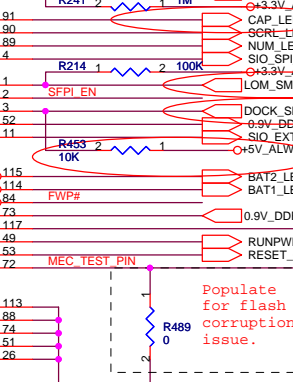
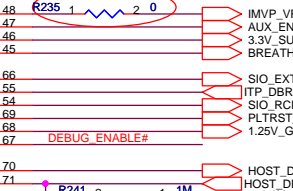
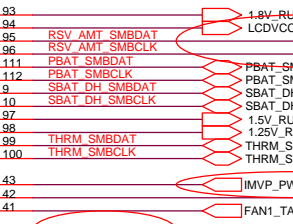
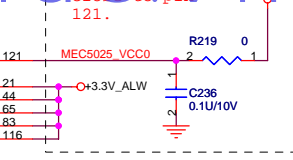




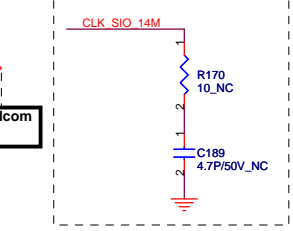
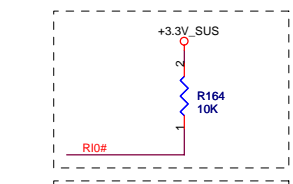
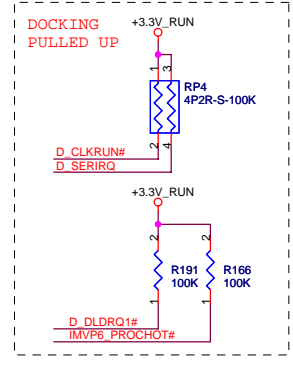
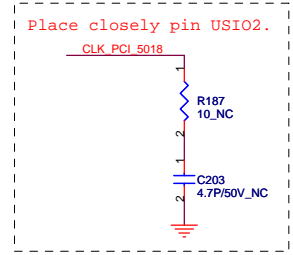
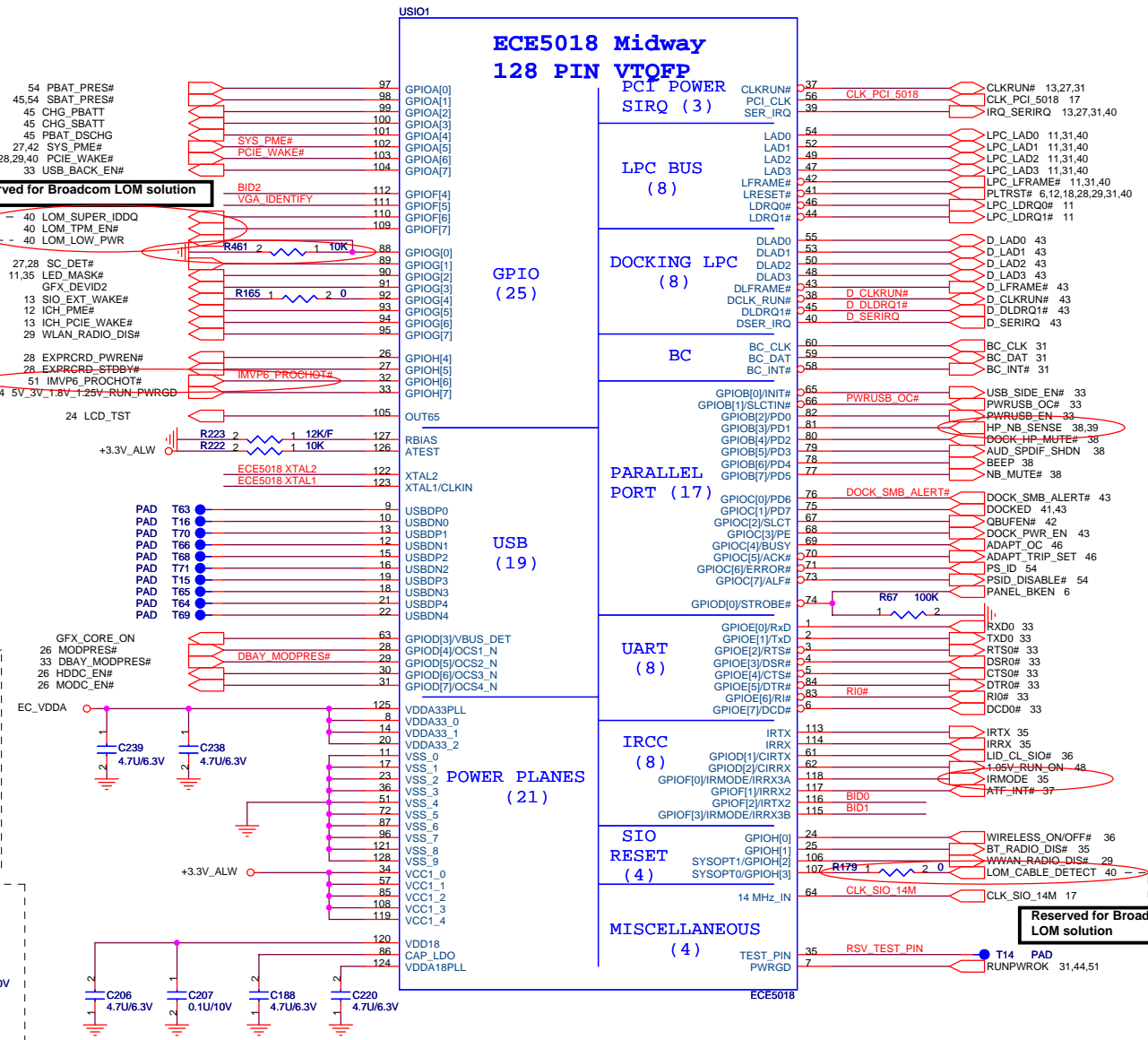
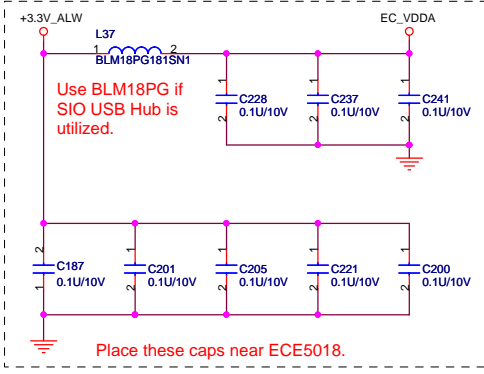
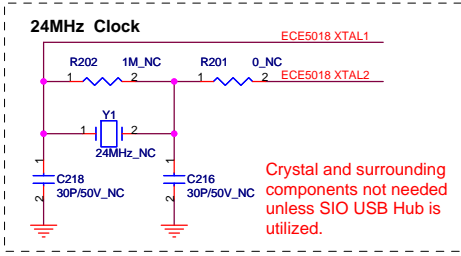
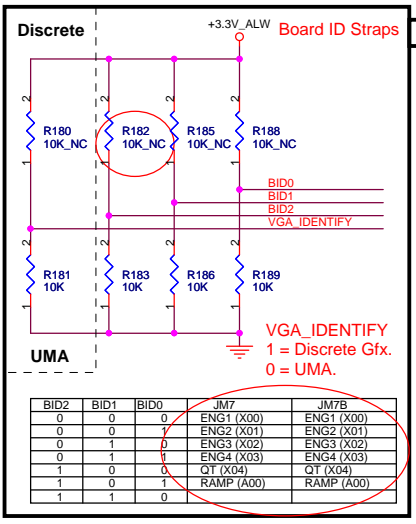
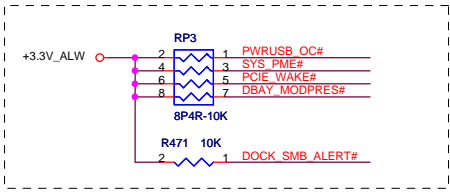


For MEC5025 Rev.C: C685=22uF and populate workaround circuit. For MEC5025 Rev.D: C685=4.7uF and depopulate workaround circuit.

MEC5025 EC-08 128 PIN VTQFP pinout table with columns for pin number, signal name, and connector/pin reference.



QUANTA COMPUTER logo and title block containing document number (JM7), date (Wednesday, June 28, 2006), and sheet information (31 of 57).

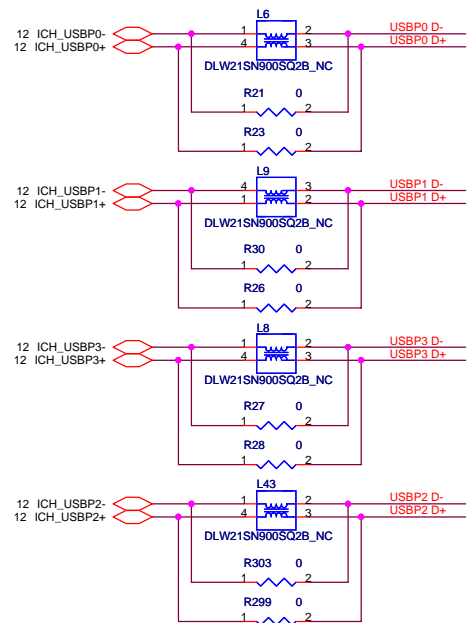


QUANTA COMPUTER

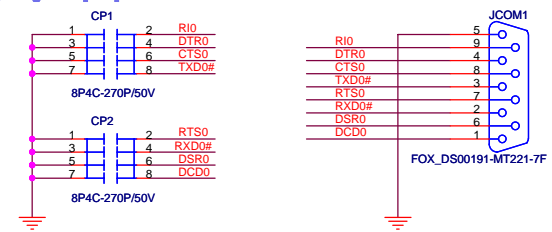
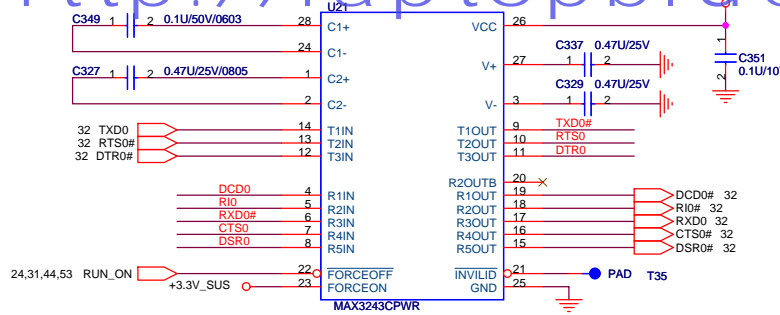
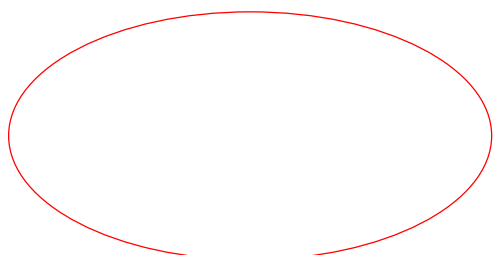
Ultra I/O Controller EECS018

Title	EECS018	Rev	1A
Size	Document Number JM7		
Date:	Wednesday, June 28, 2006	Sheet	32 of 57

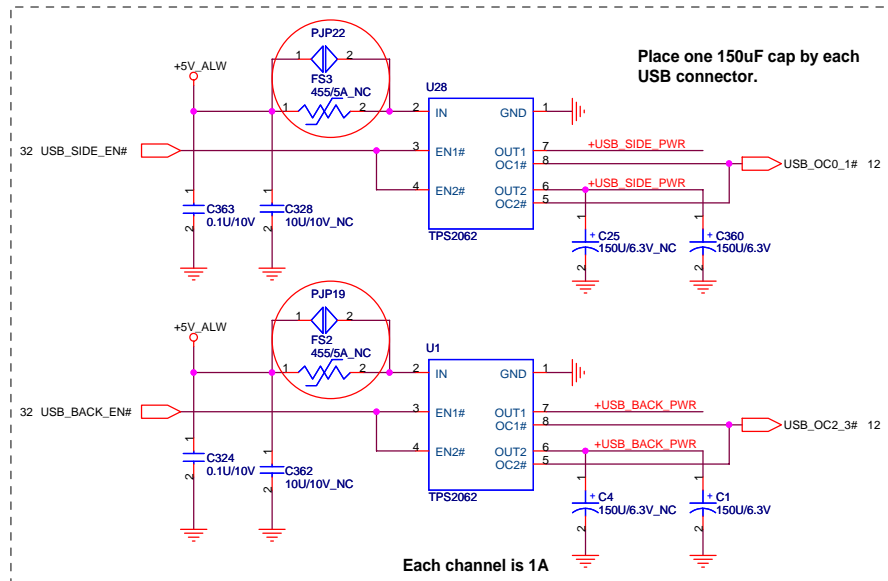
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



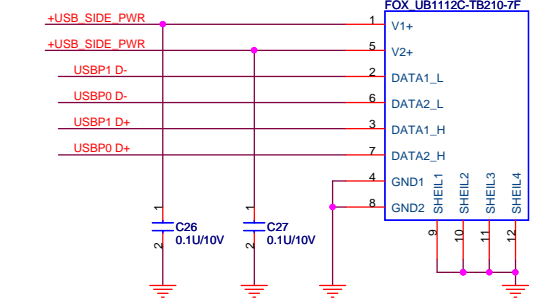
Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



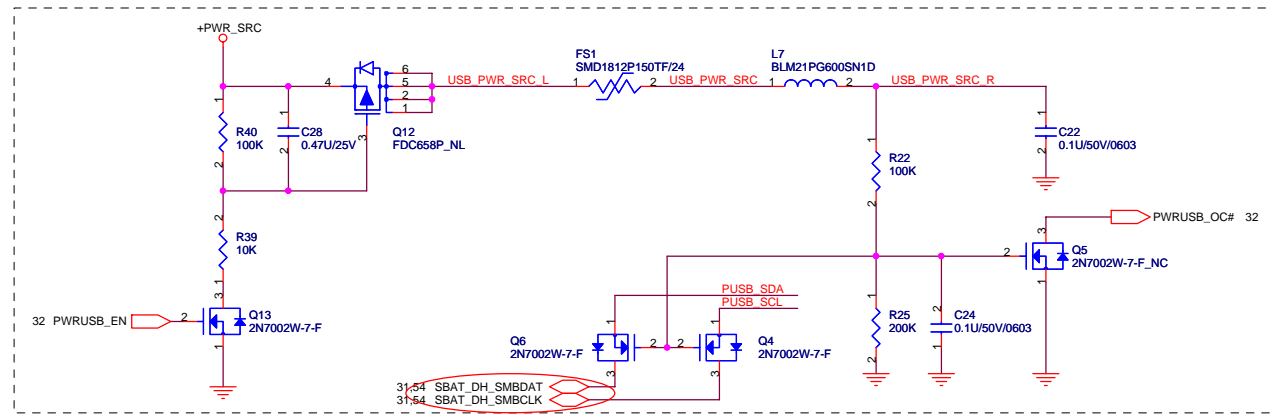
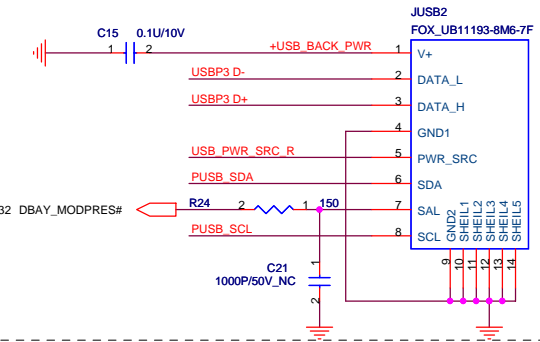
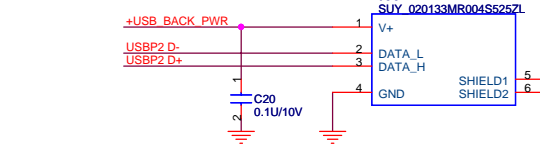
Place one 150uF cap by each USB connector.

Each channel is 1A

Ext Side

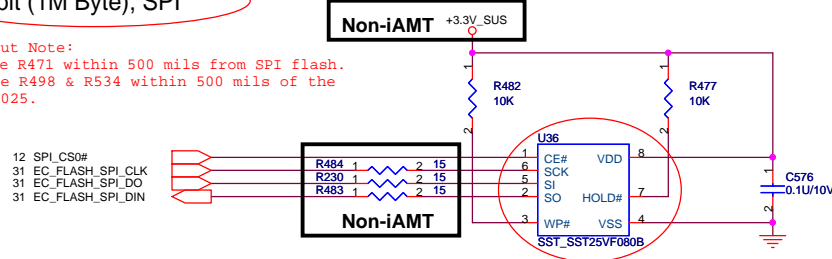


Ext Back

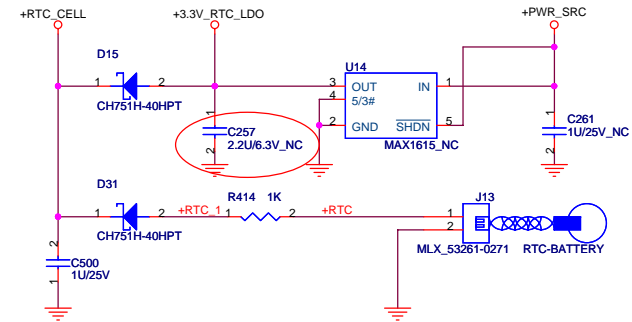


8Mbit (1M Byte), SPI

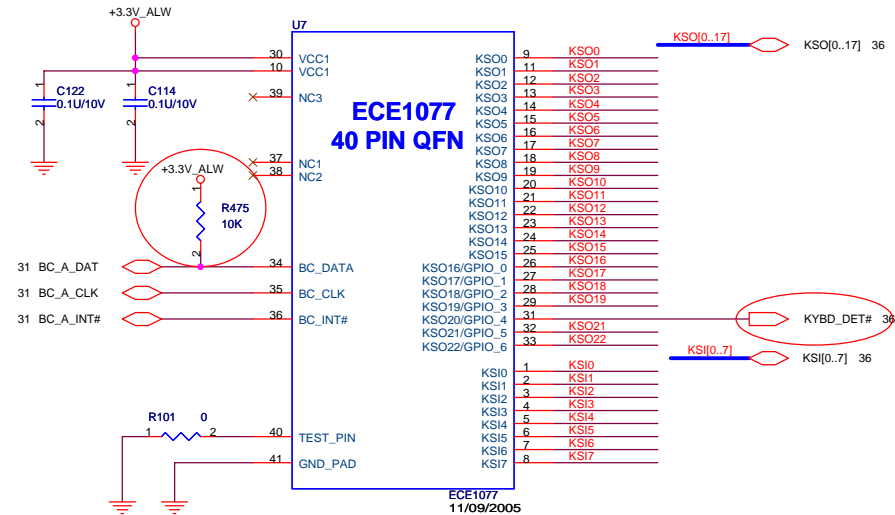
Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.



RTC BATTERY



Keyboard Scan Extension



Title FLASH, RTC & KC

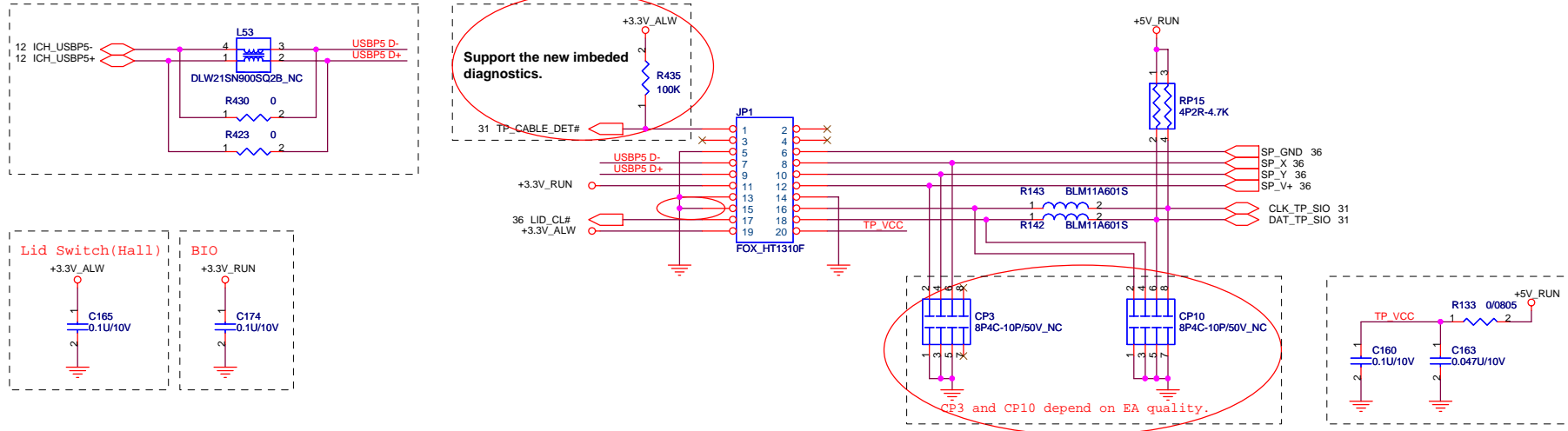
Size Document Number JM7

Rev 1A

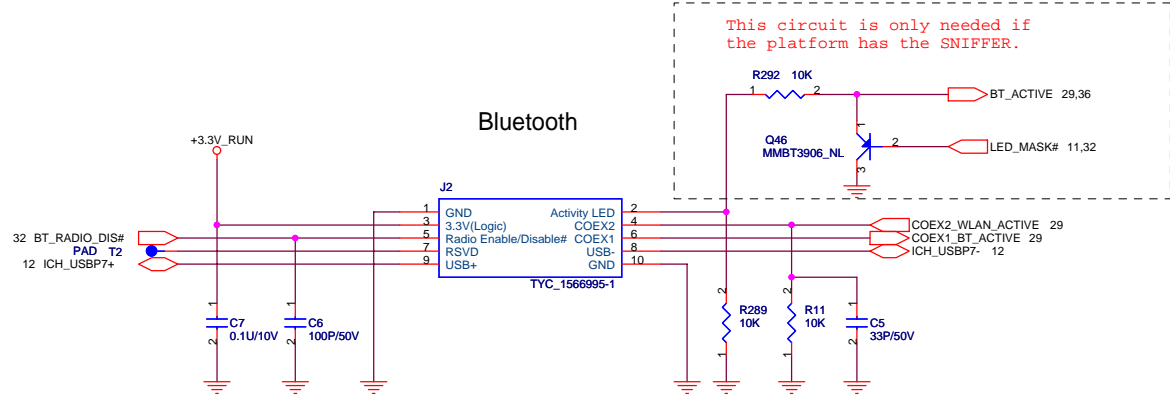
Date: Wednesday, June 28, 2006

Sheet 34 of 57

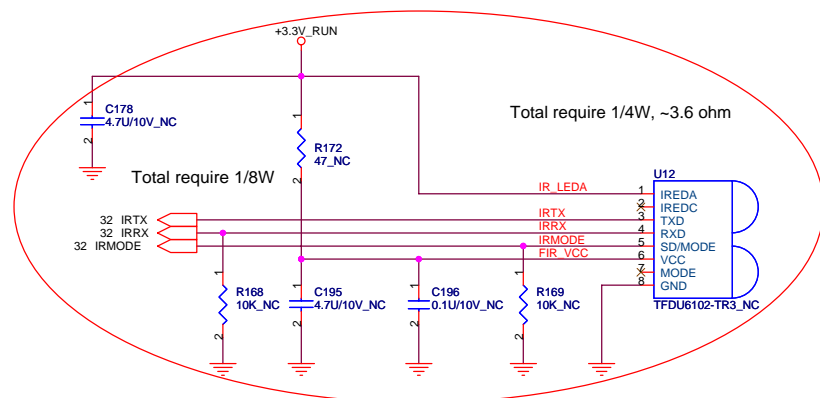
Touch Pad



Bluetooth



FIR



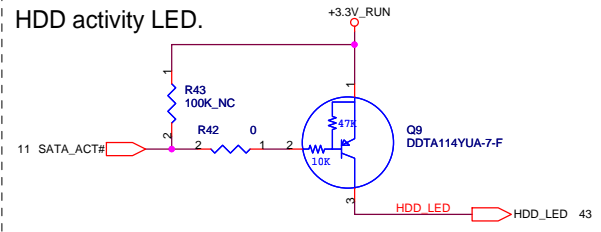
QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

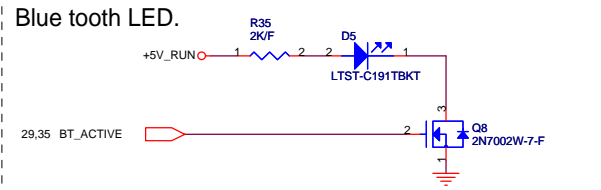
Size: Document Number JM7 Rev 1A

Date: Wednesday, June 28, 2006 Sheet 35 of 57

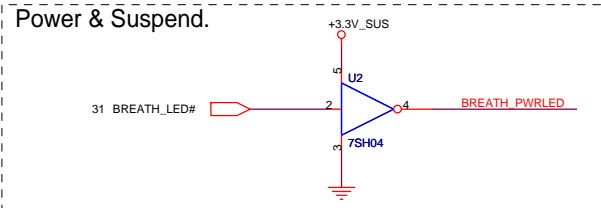
HDD activity LED.



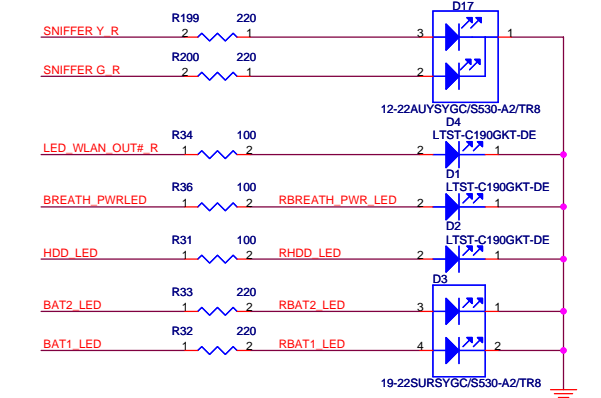
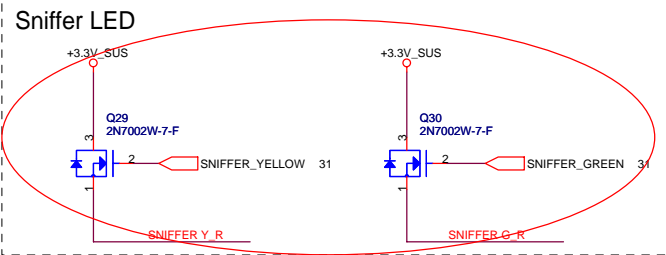
Blue tooth LED.



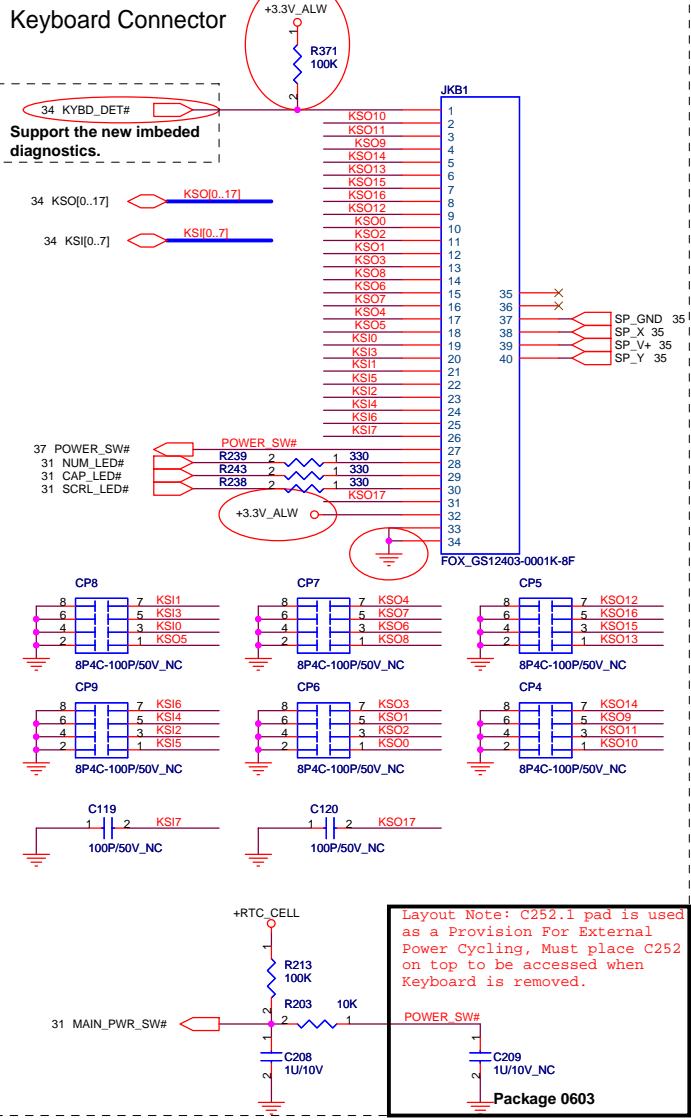
Power & Suspend.



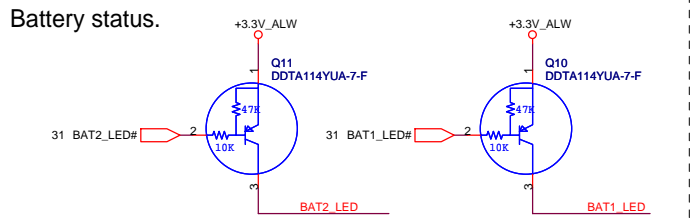
Sniffer LED



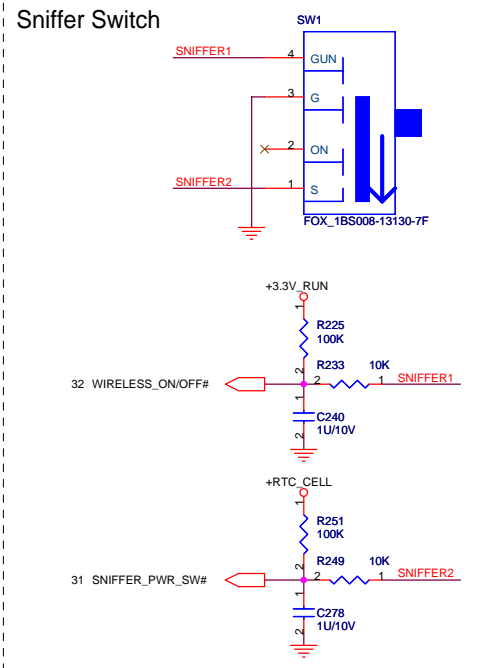
Keyboard Connector



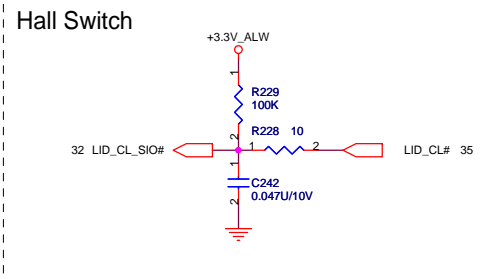
Battery status.



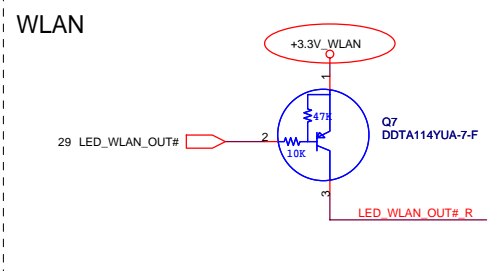
Sniffer Switch

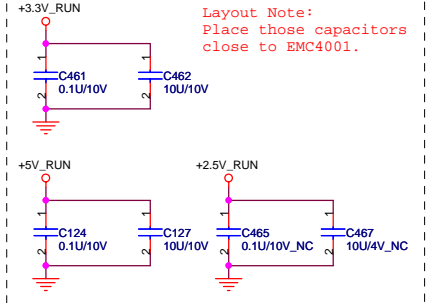
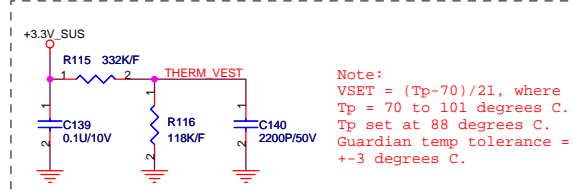
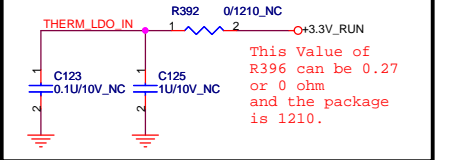
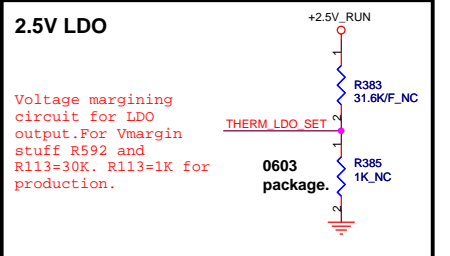
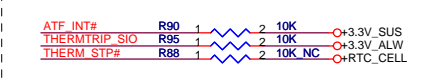
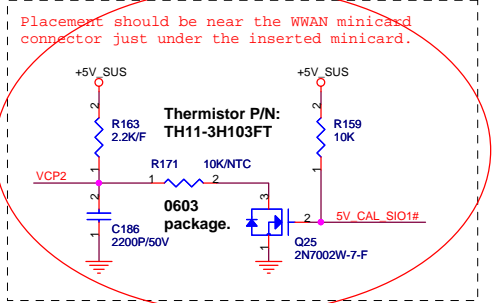
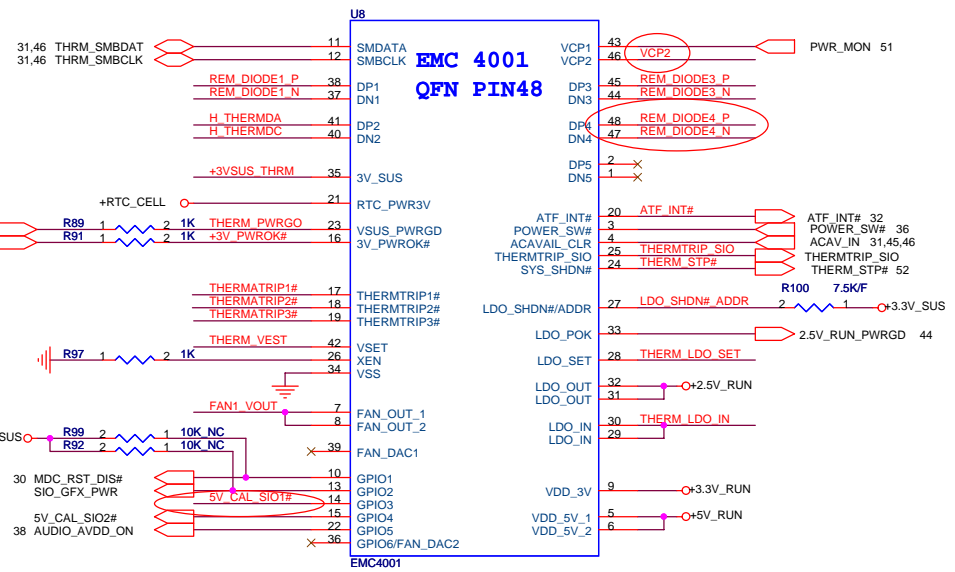
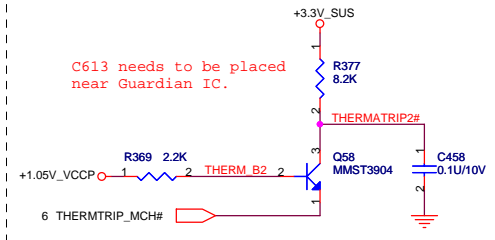
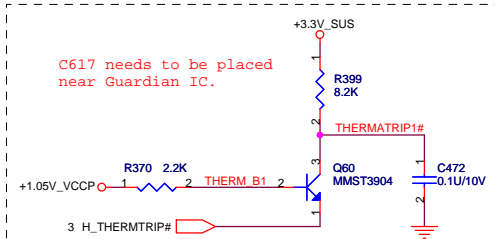
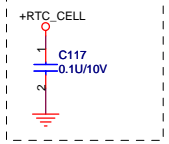
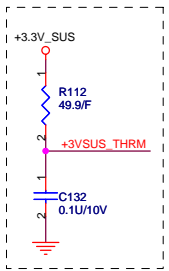
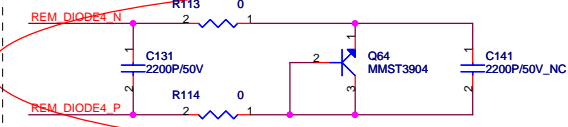
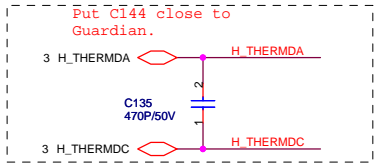
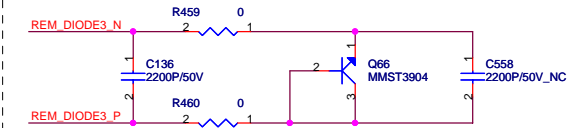
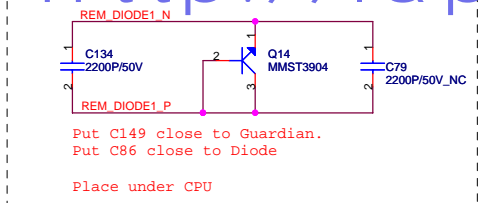
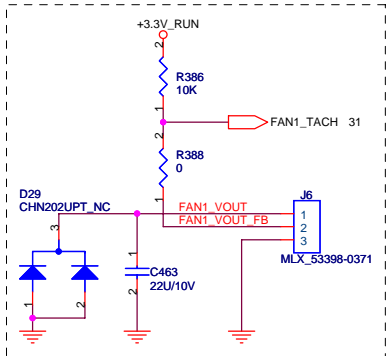


Hall Switch



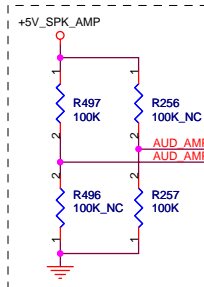
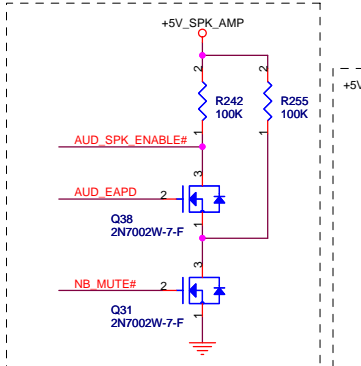
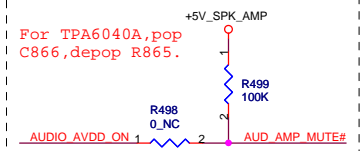
WLAN



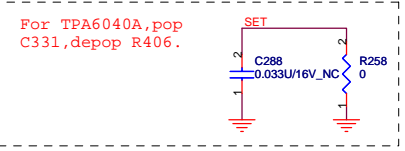
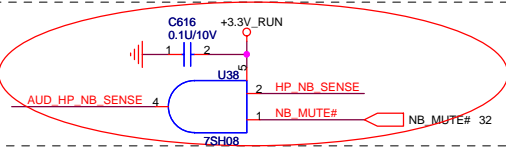
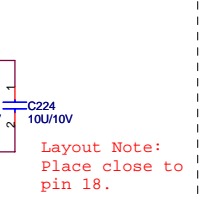
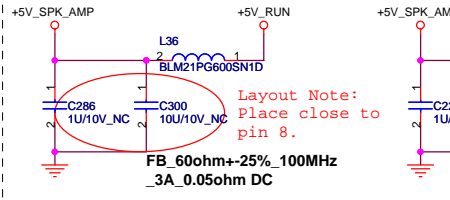
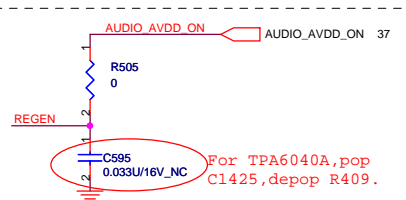
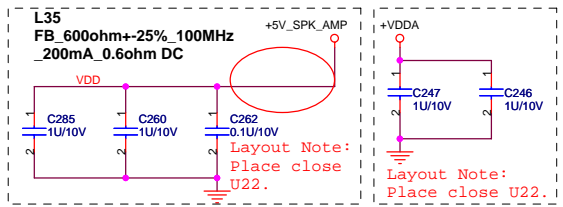
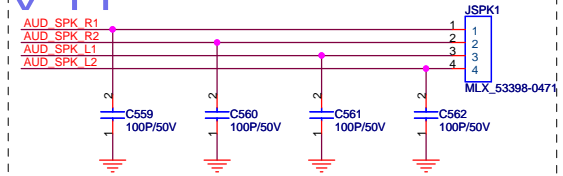
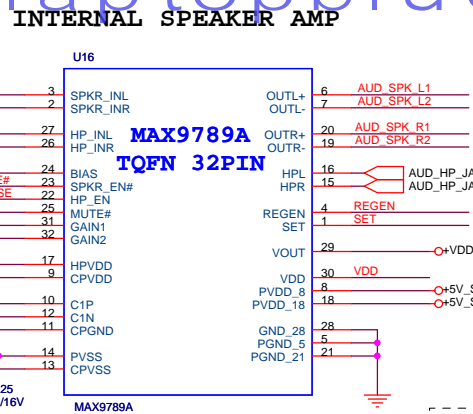


Package 1206 For THD+N performance and Vista Logo requirements.

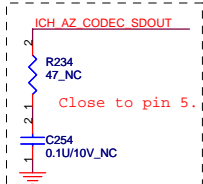
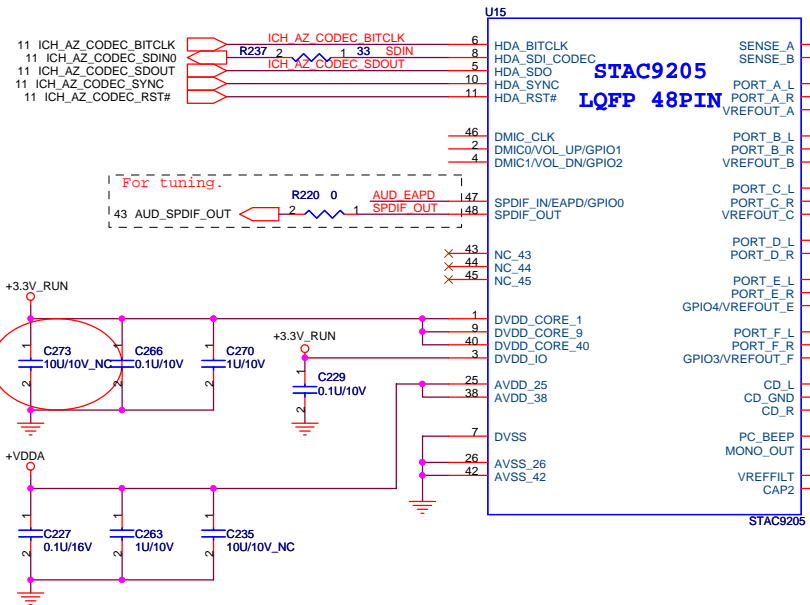
AUD_LINE_OUT_L C301 1 2 0.033U/200V
AUD_LINE_OUT_R C259 1 2 0.033U/200V
AUD_HP_OUT_L C613 2 2 1U/100V
AUD_HP_OUT_R C594 2 2 1U/100V



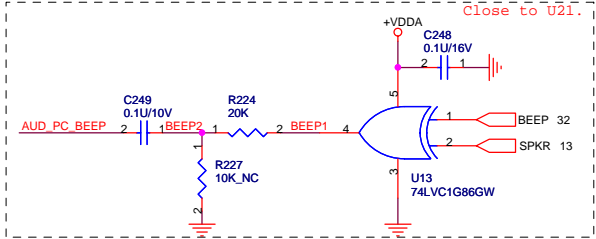
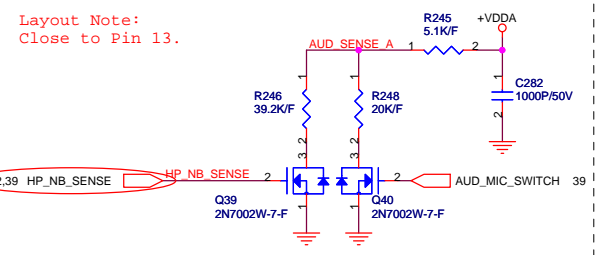
GAIN2	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

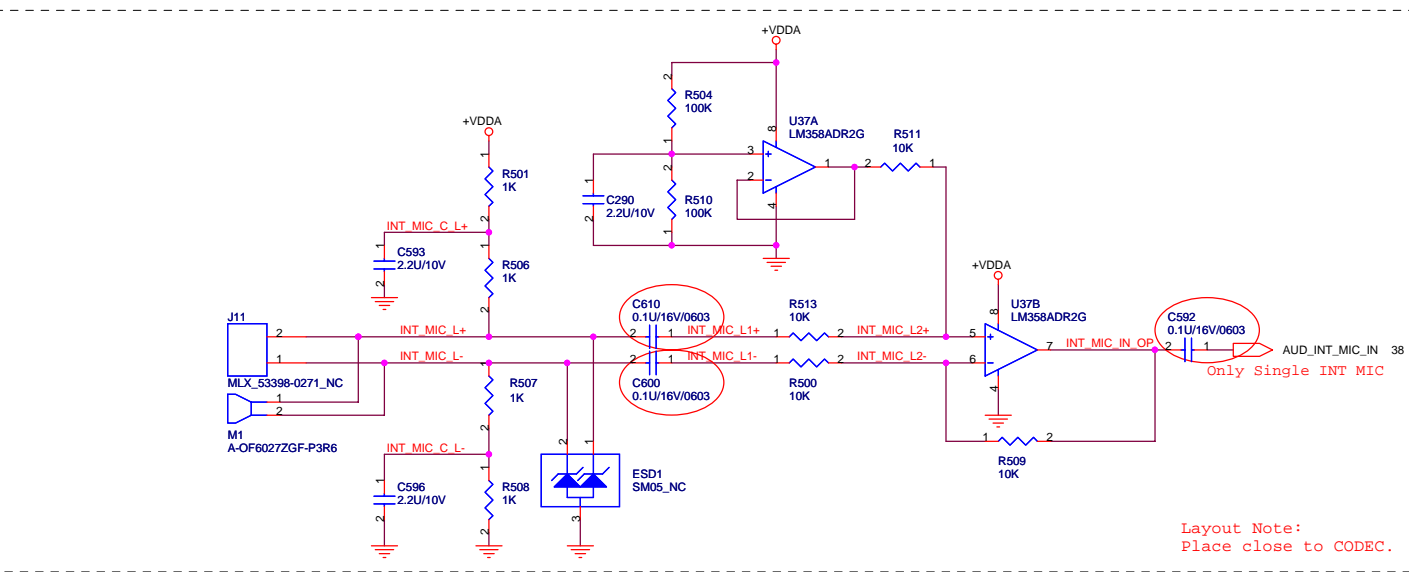
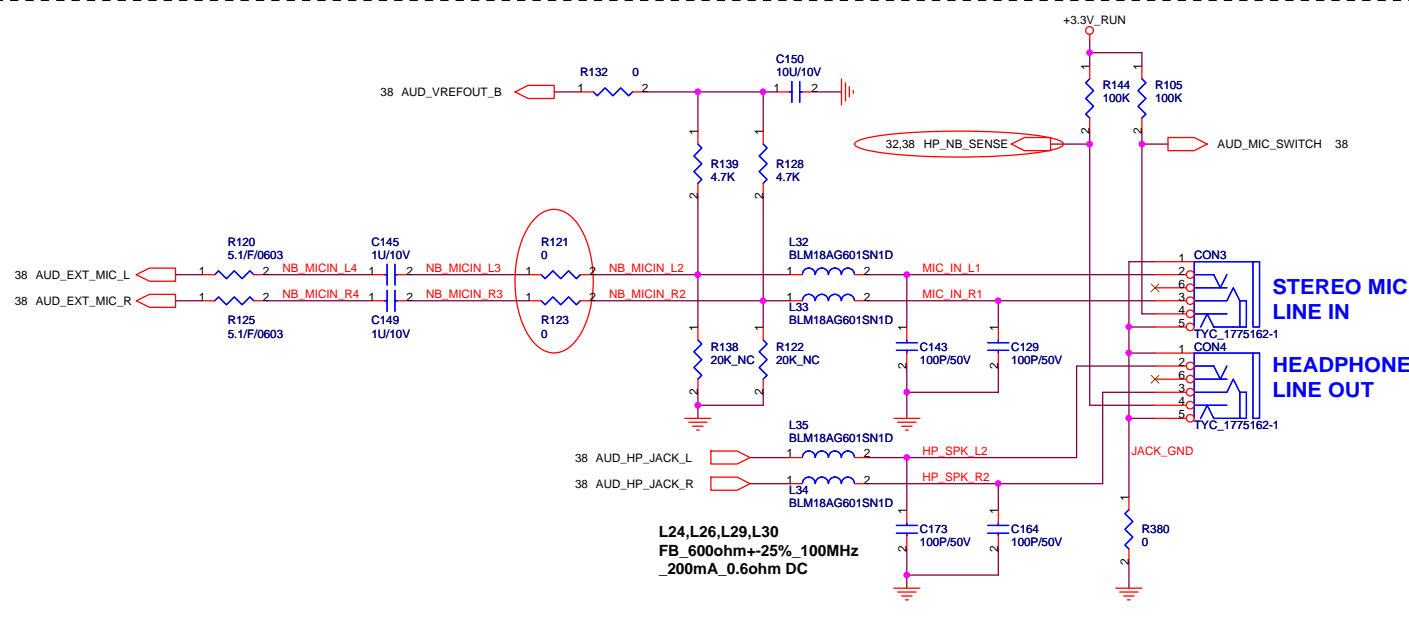


AZALIA (HD) CODEC



For tuning, R220 0 AUD_EAPD SPDIF_OUT





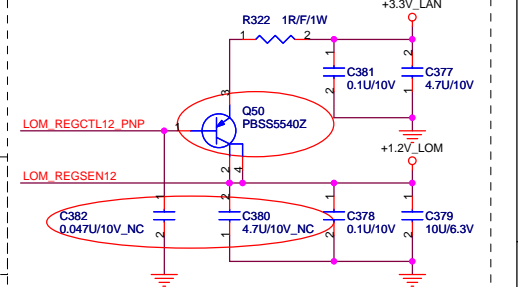
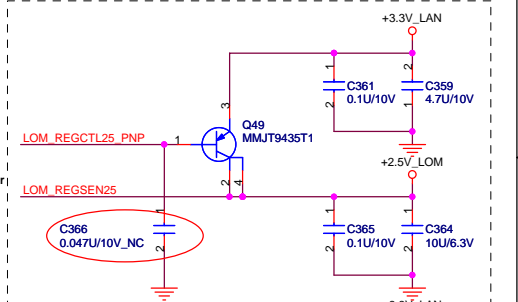
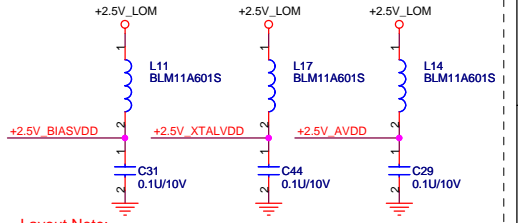
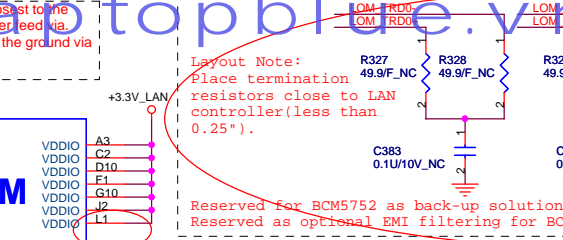
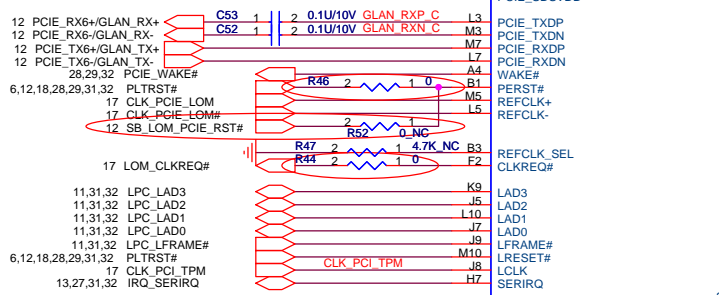
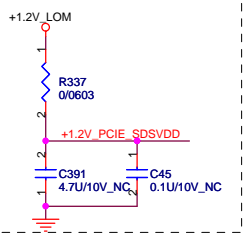
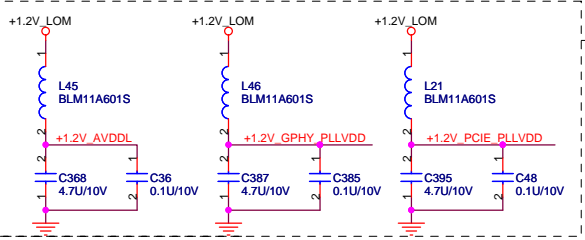
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Layout Note:
Place termination resistors close to LAN controller (less than 0.25").

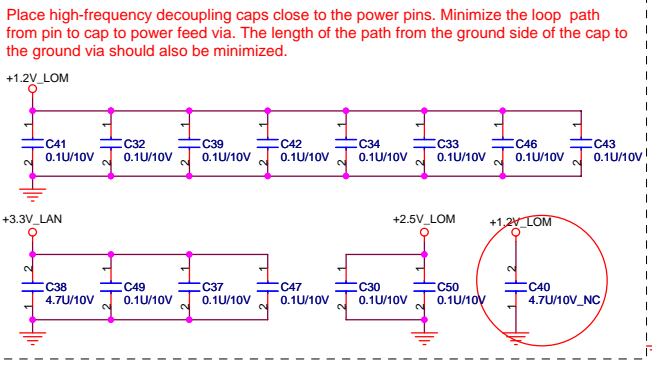
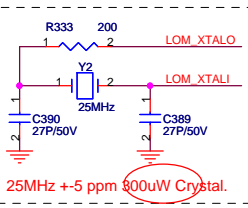
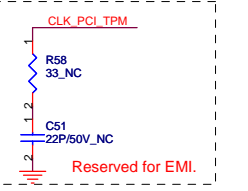
Reserved for BCM5752 as back-up solution.
Reserved as optional EMI filtering for BCM5755M.

Place R676 as close as possible to the ASIC. Pad is needed to measure 125Mhz clock for debugging.

Layout Note:
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.



LOM_REGSEN12 and LOM_REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane. Use 8 mils trace width for these signals.



RDAC resistor R674 - 1%
- 1.15K for Docking solutions with analog s/w
- 1.24K for Non-Docking solutions
Place as close to the ASIC as possible

Reserved for BCM5752 as back-up solution.

Reserved for BCM5752 as back-up solution.

Reserved for BCM5752 as back-up solution.

Reserved for BCM5752 as back-up solution.

Logic High Voltage must be 0.7V to 2.75V

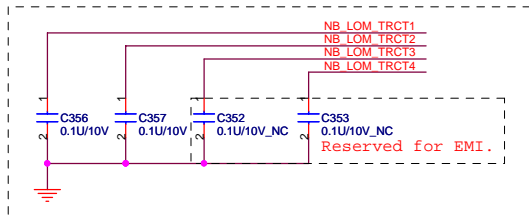
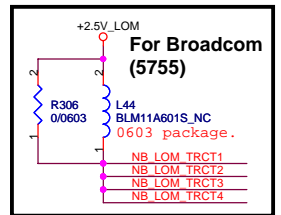
BCM5755M

10mm x 10mm
BGA144

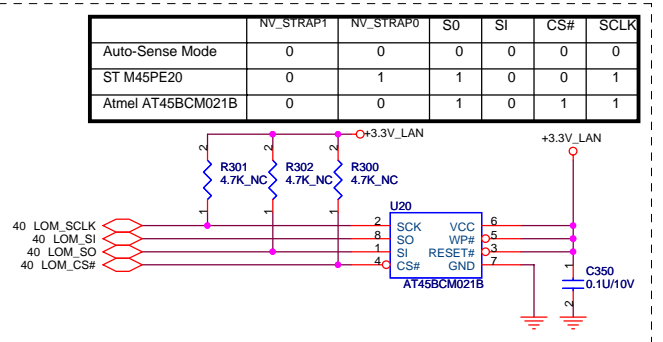
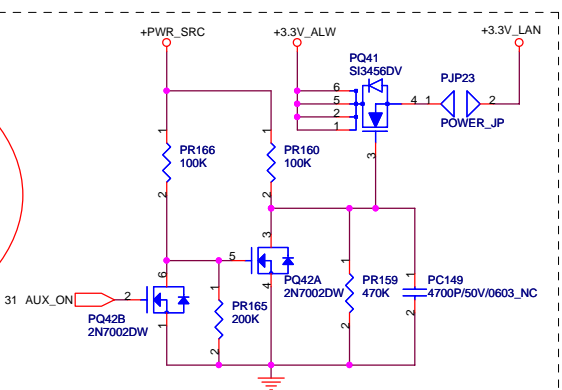
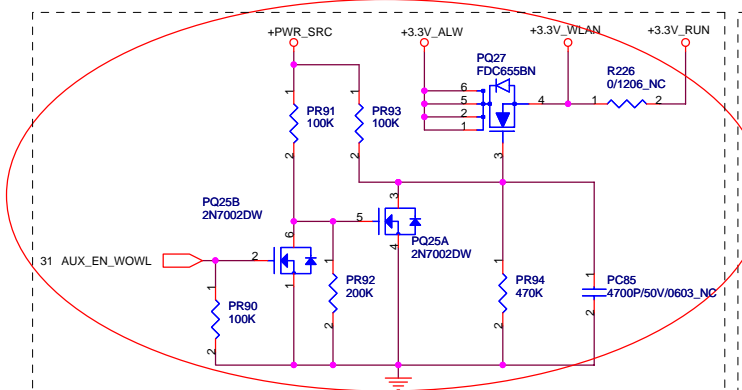
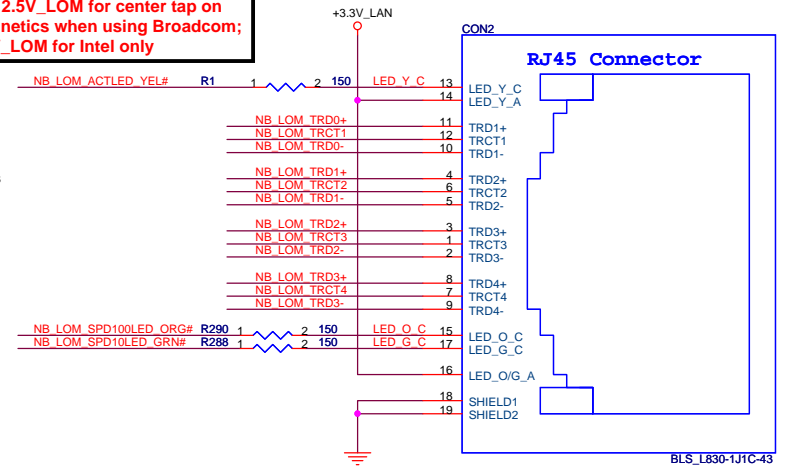
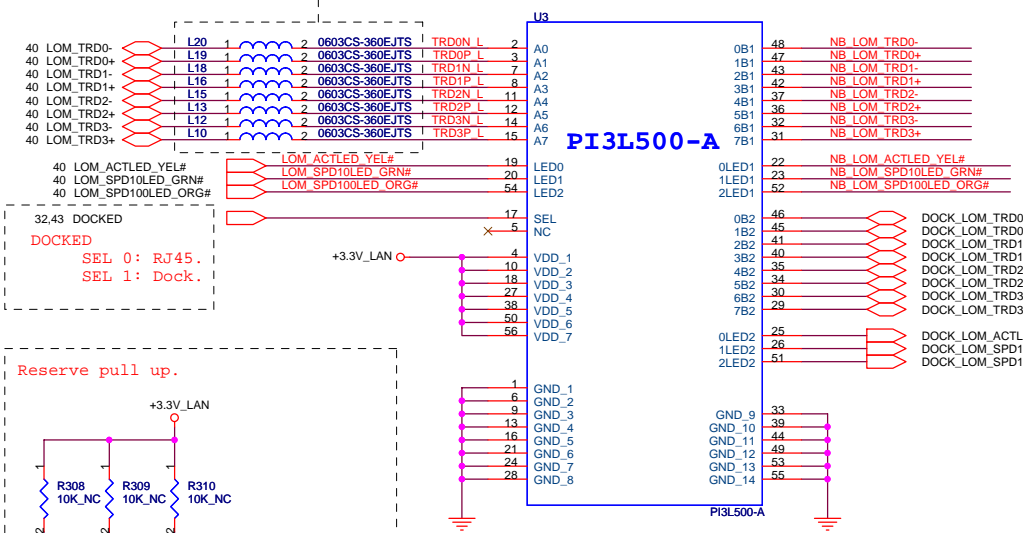


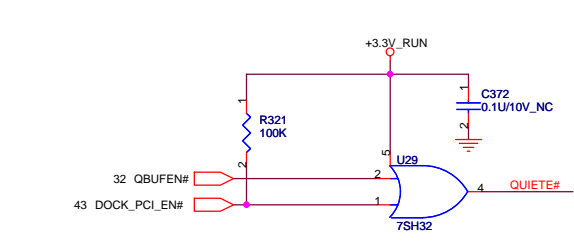
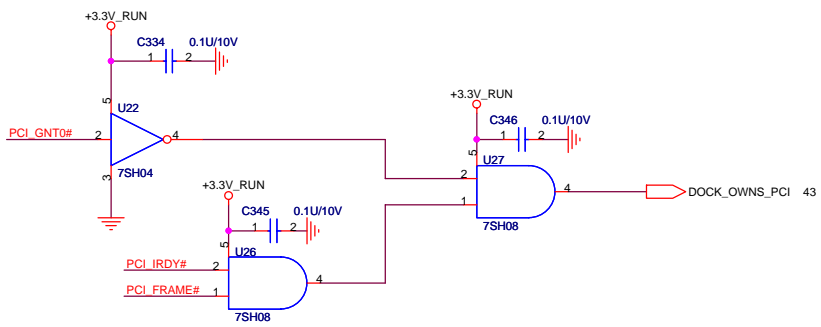
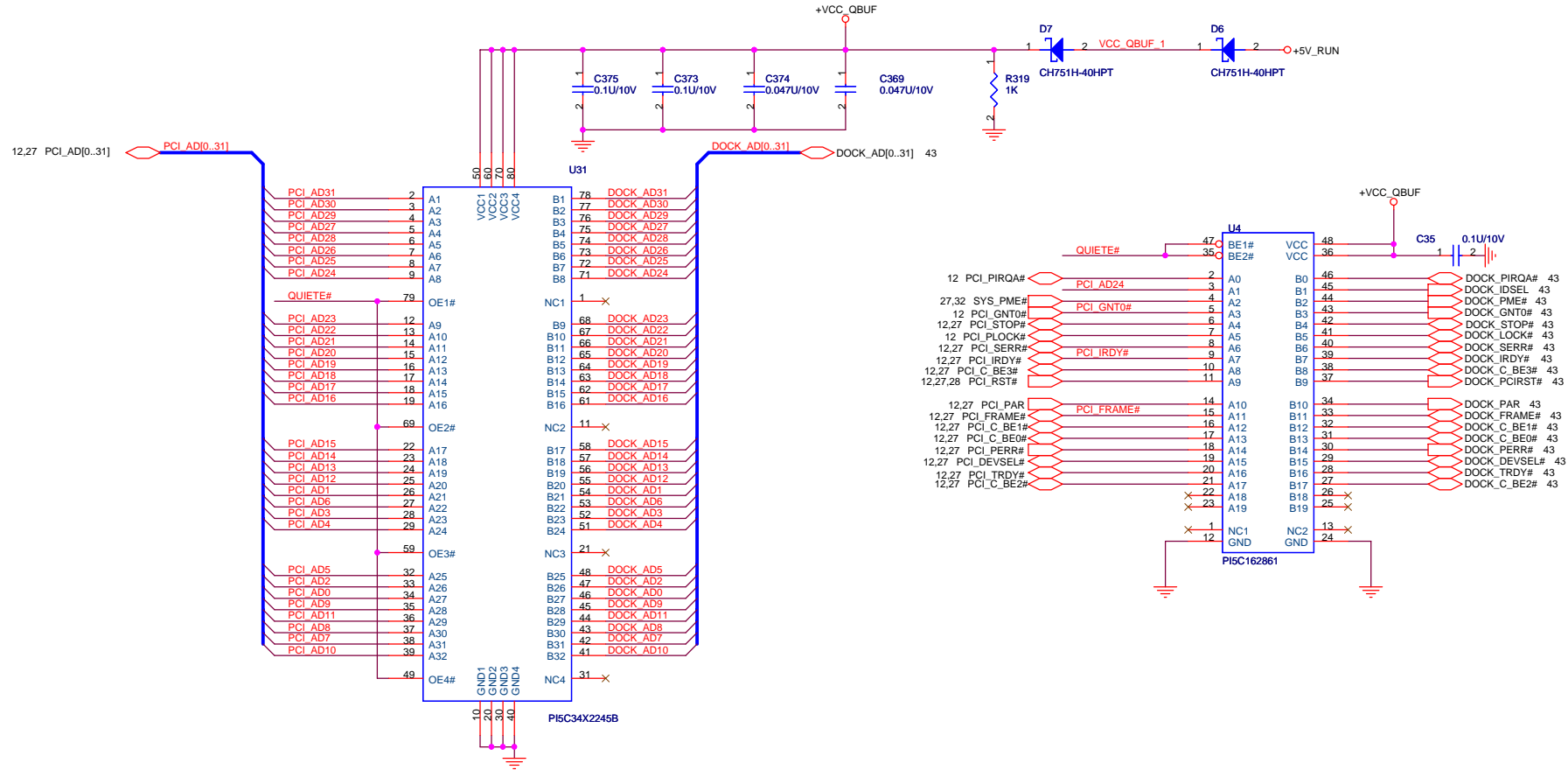
Title LAN Broadcom 5755		
Size JM7	Document Number	Rev 1A
Date: Wednesday, June 28, 2006	Sheet 40	of 57

36nH is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.



Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only



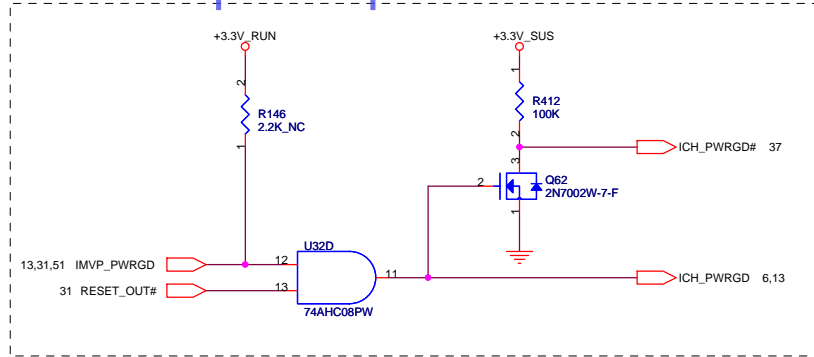
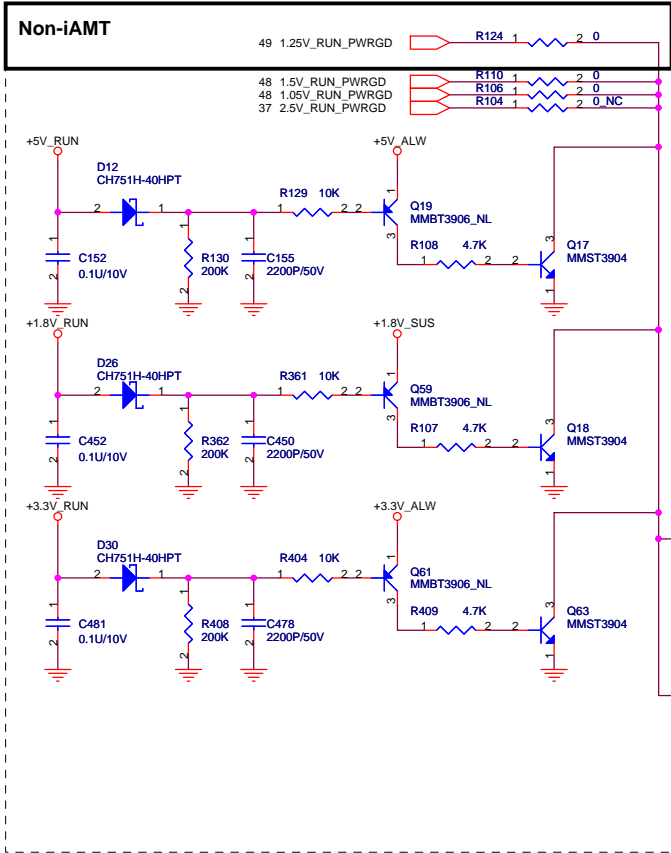


QUANTA COMPUTER

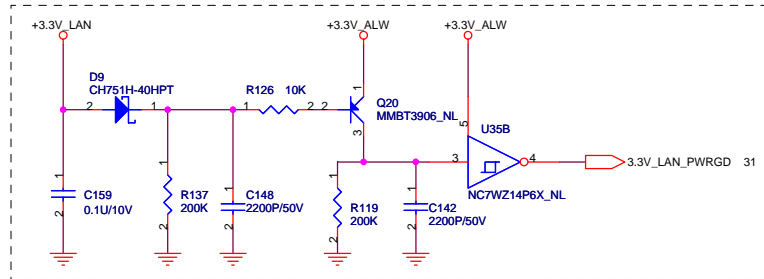
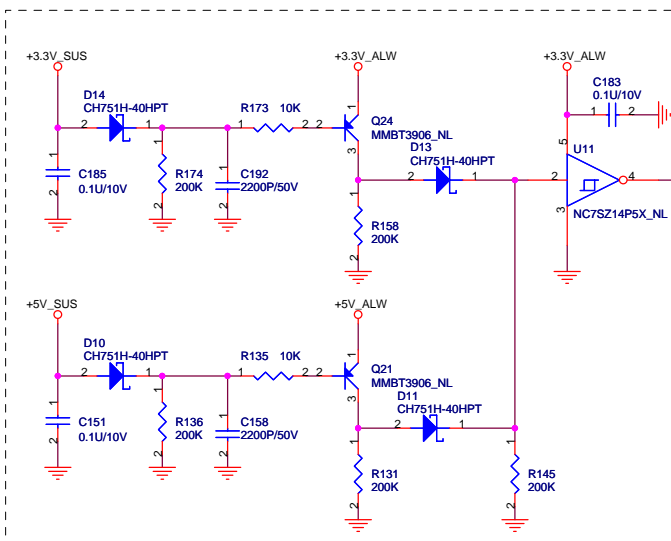
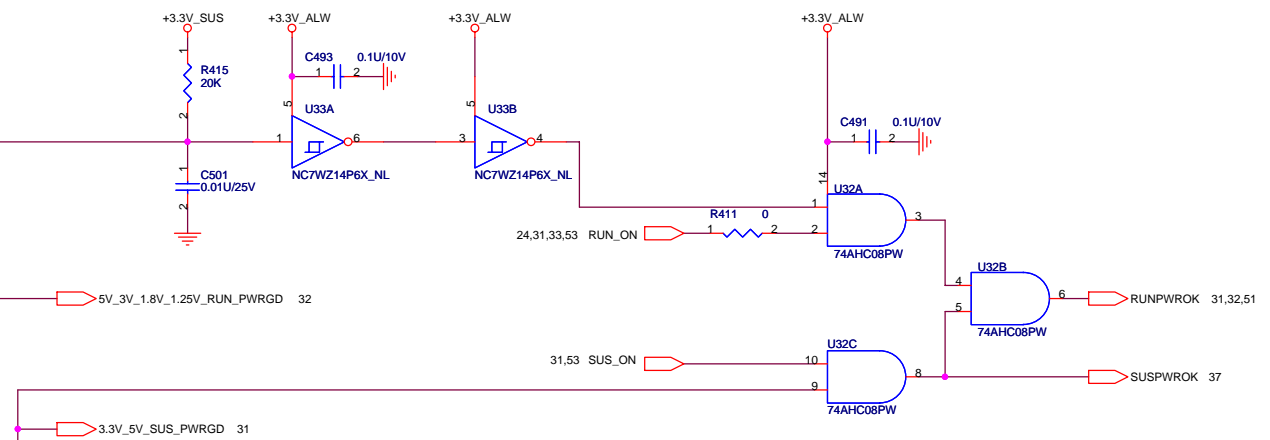
Title: Docking Q-SWITCH

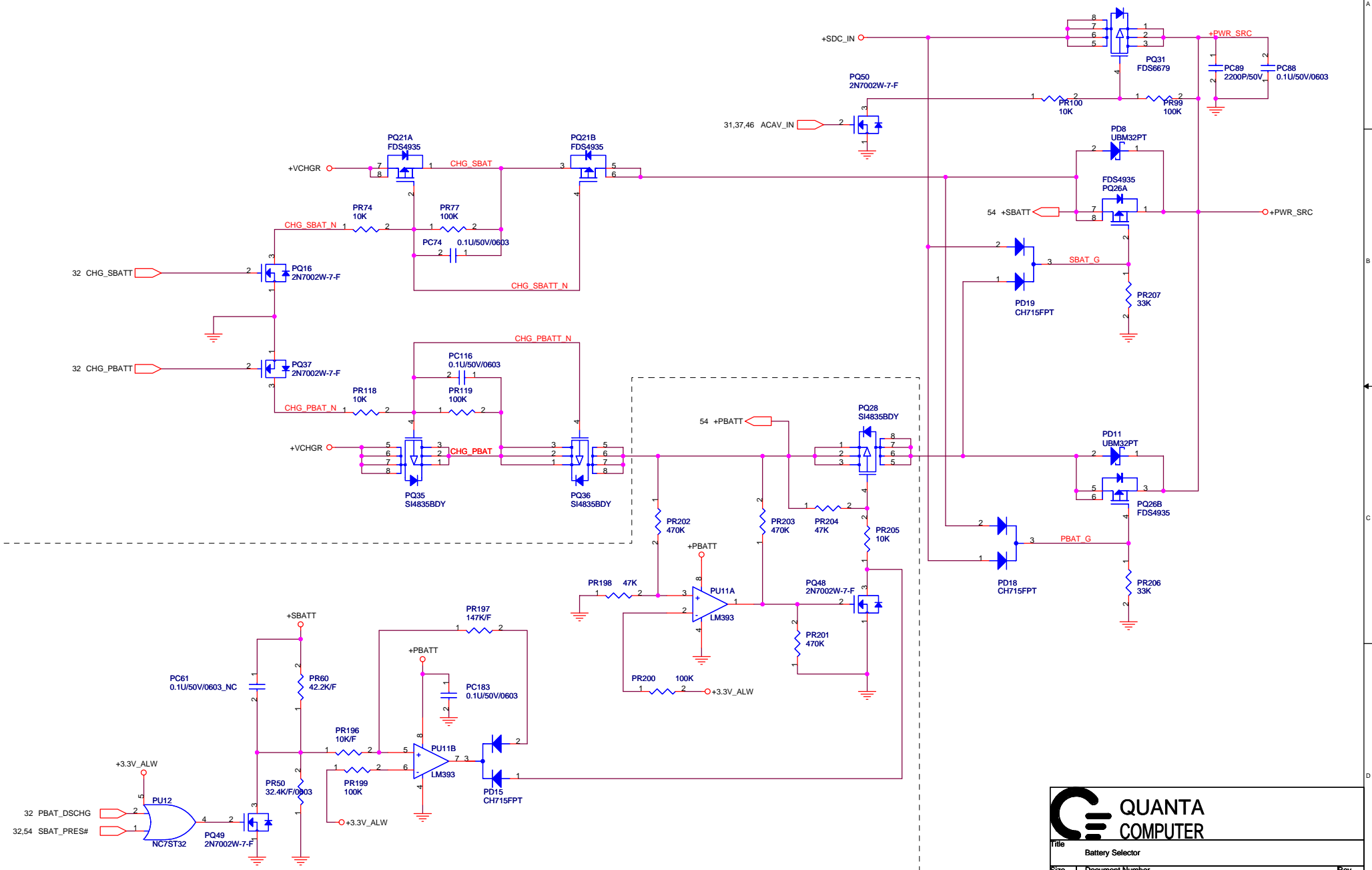
Size	Document Number JM7	Rev 1A
------	---------------------	--------

Date: Wednesday, June 28, 2006 Sheet 42 of 57



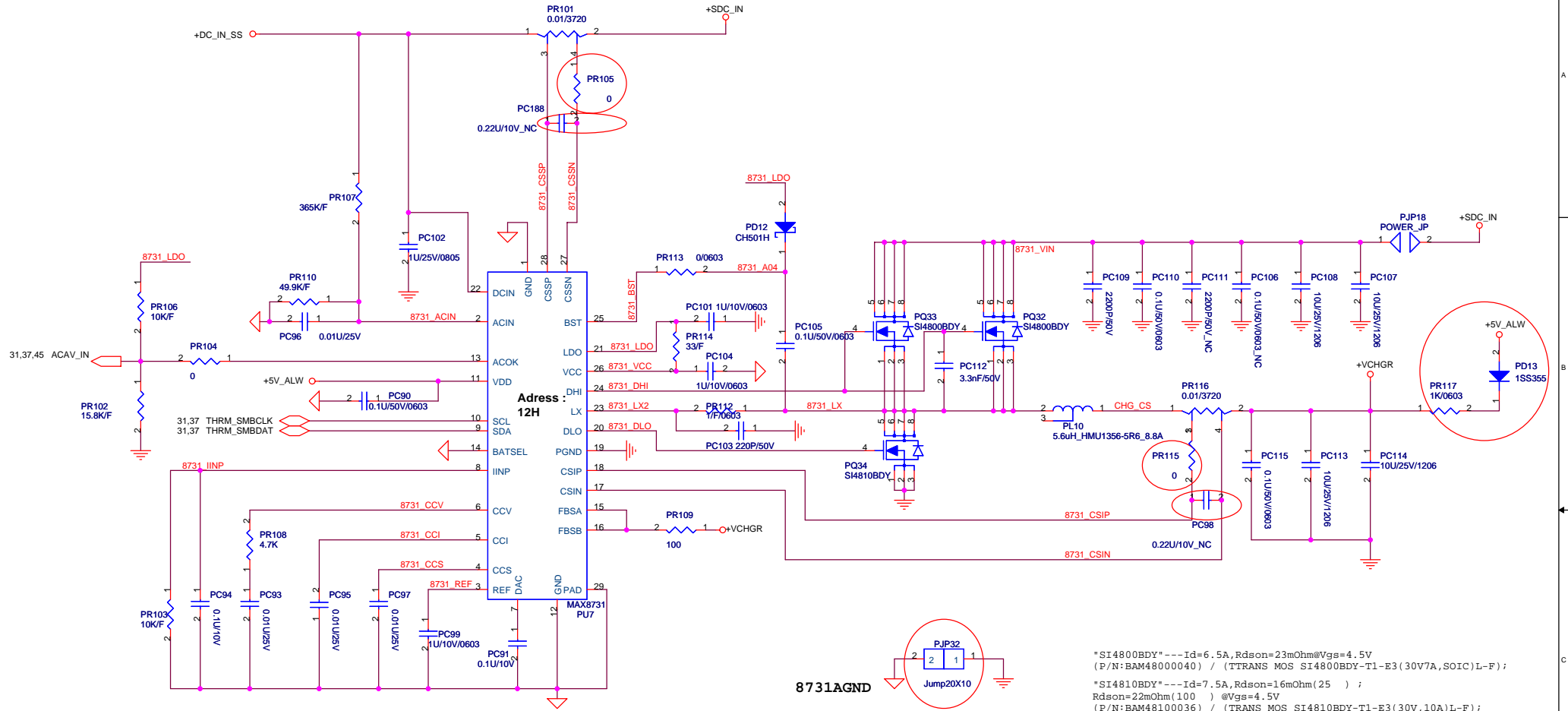
Keep Away from high speed buses



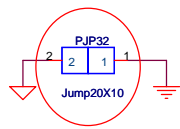


QUANTA COMPUTER

Title		Battery Selector
Size	Document Number	Rev
JM7		1A
Date:	Wednesday, June 28, 2006	Sheet 45 of 57

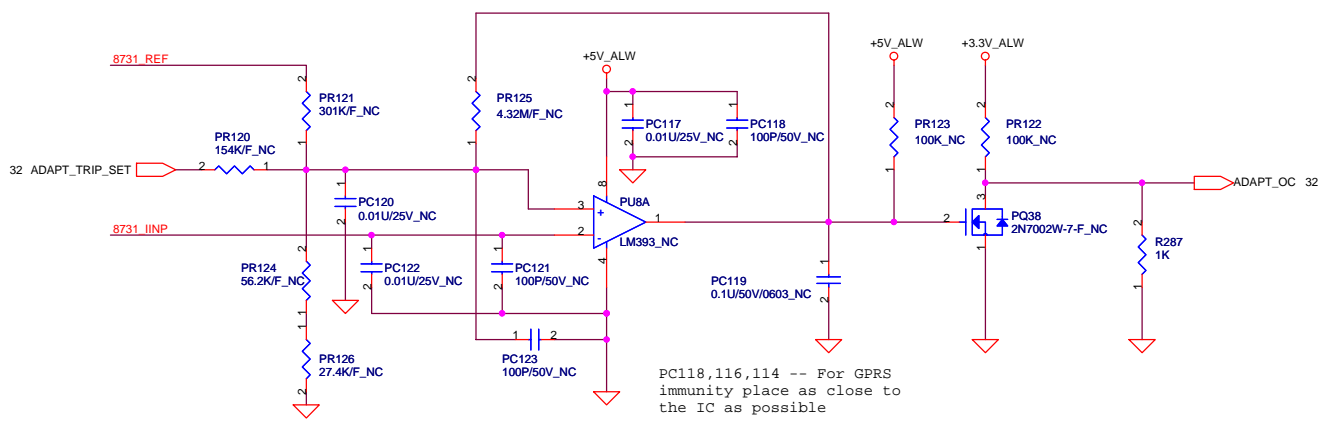


8731AGND



"SI4800BDY"---Id=6.5A,Rdson=23mOhm@Vgs=4.5V
(P/N:BAM48000040) / (TTRANS MOS SI4800BDY-T1-E3(30V7A,SOIC)L-F) ;
"SI4810BDY"---Id=7.5A,Rdson=16mOhm(25) ;
Rdson=22mOhm(100) @Vgs=4.5V
(P/N:BAM48100036) / (TRANS MOS SI4810BDY-T1-E3(30V,10A)L-F) ;

8731_VREF=4.096V
8731_VLDO=5.4V
ACIN switch
threshold=2.048V
400KHz PWM
nominal

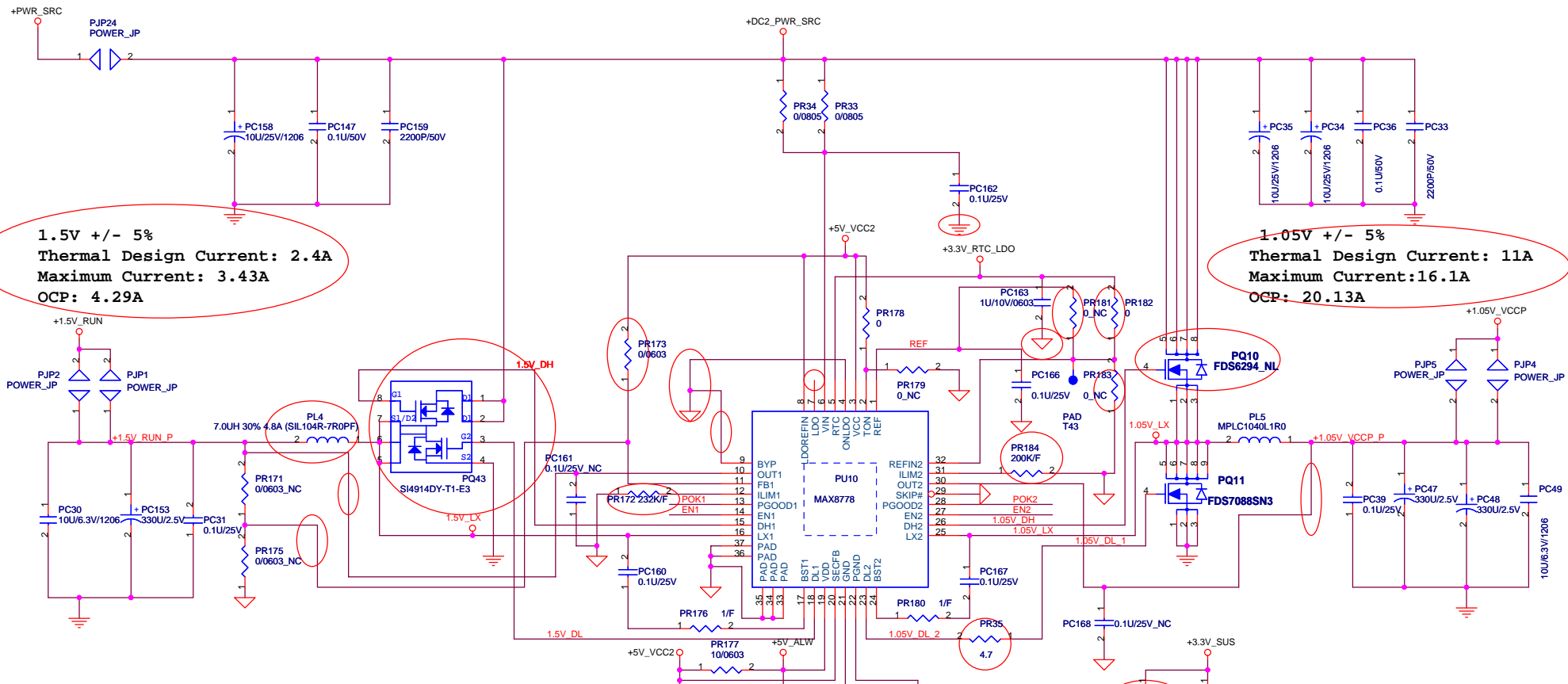


PC118,116,114 -- For GPRS immunity place as close to the IC as possible



Title Battery Charger		
Size JM7	Document Number JM7	Rev 1A
Date: Wednesday, June 28, 2006	Sheet 46	of 57

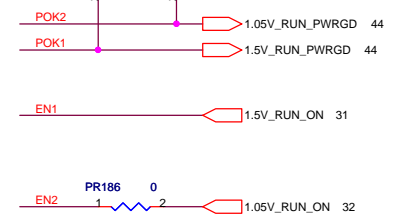
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**



1.5V +/- 5%
Thermal Design Current: 2.4A
Maximum Current: 3.43A
OCP: 4.29A

1.05V +/- 5%
Thermal Design Current: 11A
Maximum Current: 16.1A
OCP: 20.13A

Layout Notes:
 Place C7 very near U1-pin19 and PU1-pin20.
 Place C8 very near U1-pin3.
 Place R19 very near U1-pin21.
 Minimize loop including Q4, L2, C11, C12 and R19.
 Minimize loop including Q2, L3, C17, C18, C19 and R19.
 Route GNDA_DC2 using at least 25 mil trace width.
 Minimize GNDA_DC2 trace length.
 Place C15 near U1-pin7.
 Place C20 near U1-pin5.
 Place R7 near U1-pin11.
 Place R12 near U1-pin31.
 Place R3, C10 near U1-pins 24 and 25.
 Place R2, C9 near U1-pins 16 and 17.
 Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
 Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
 Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
 Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
 Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
 Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
 Route OUT1 and OUT2 away from inductor and switch-node.
 Sense Vout directly at output bulk cap.

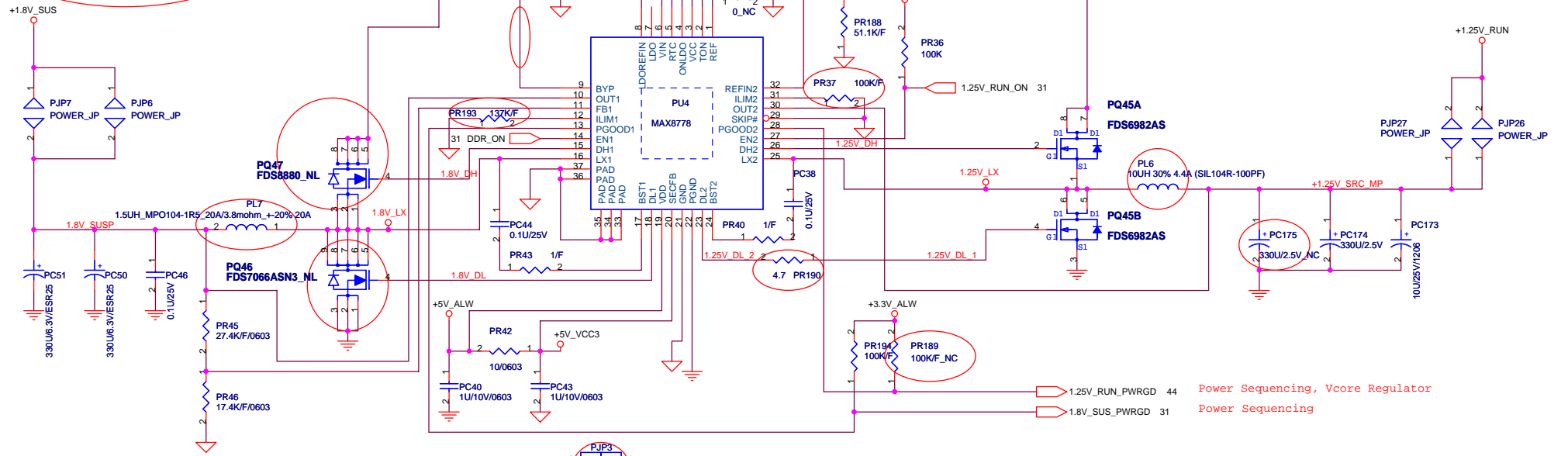


QUANTA COMPUTER

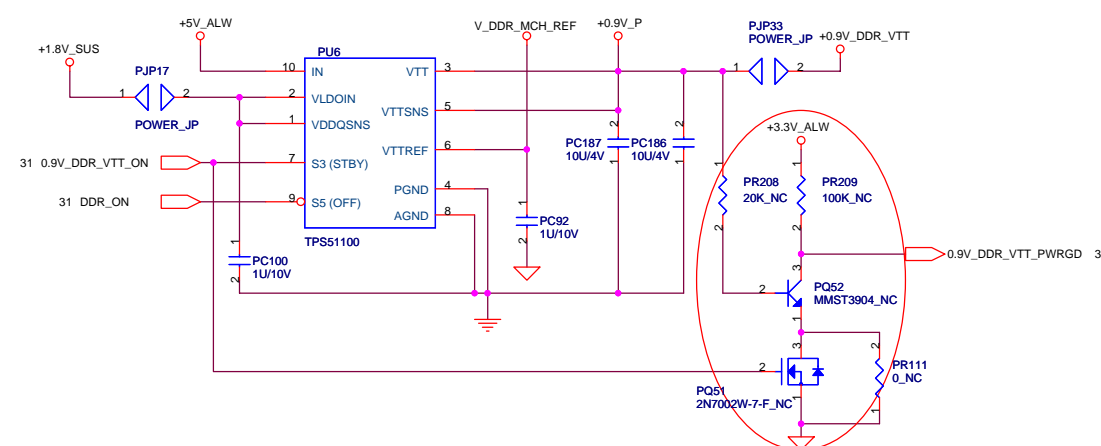
Title		1.5V,1.05V
Size	Document Number	Rev
JM7		1A
Date:	Wednesday, June 28, 2006	Sheet 48 of 57

1.8 Volt +/- 5%
 Design current 6.5A
 Maximum current 9.2A
 OCP: 11.5A

1.25V +/- 5%
 Thermal Design Current: 0.92A
 Maximum Current: 1.32A
 OCP: 1.65A



0.9V +/- 5%
 Design current 1.05 A
 Peak Current 1.5 A

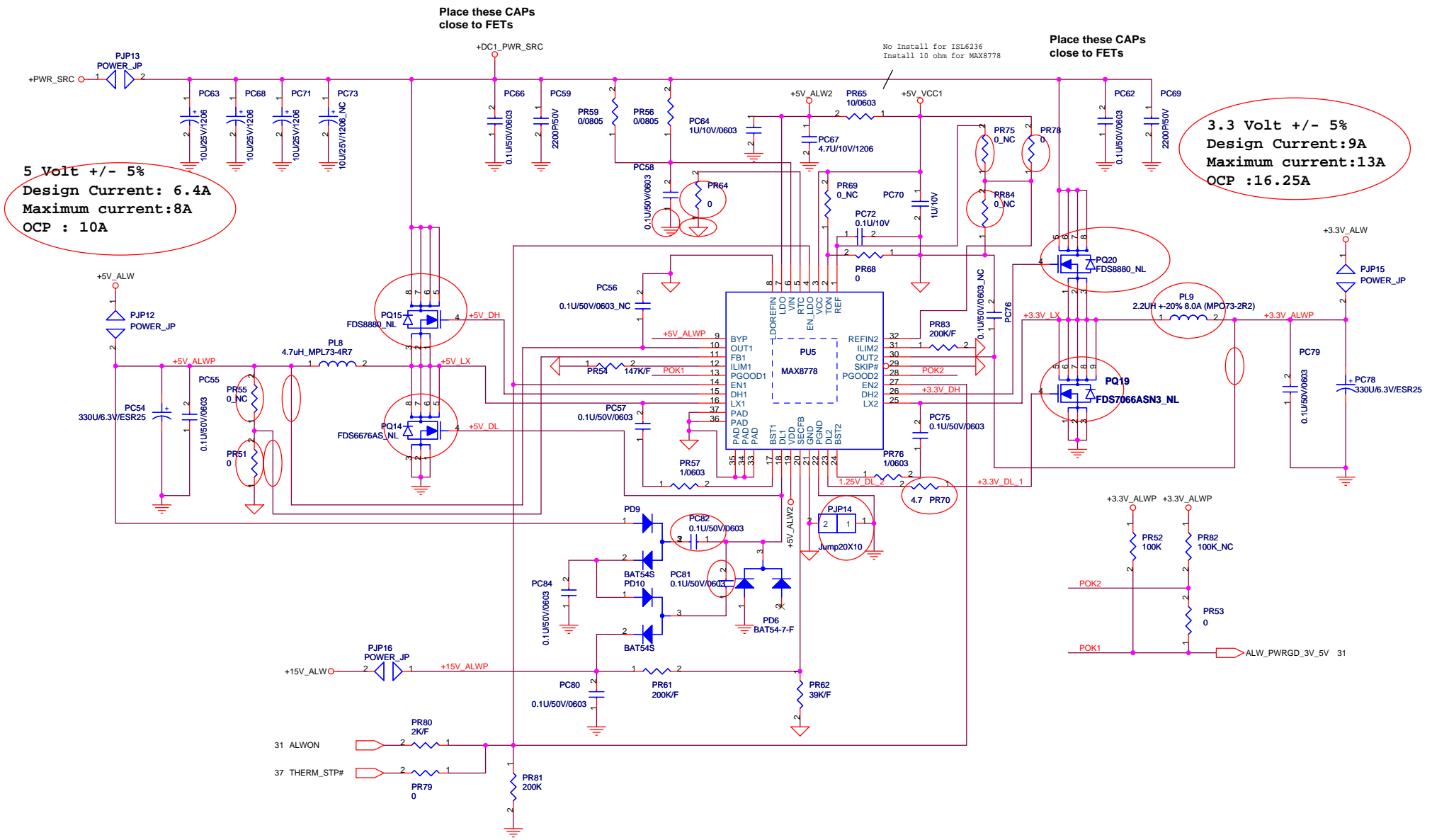


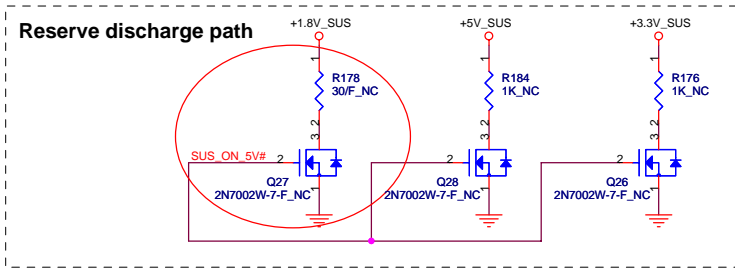
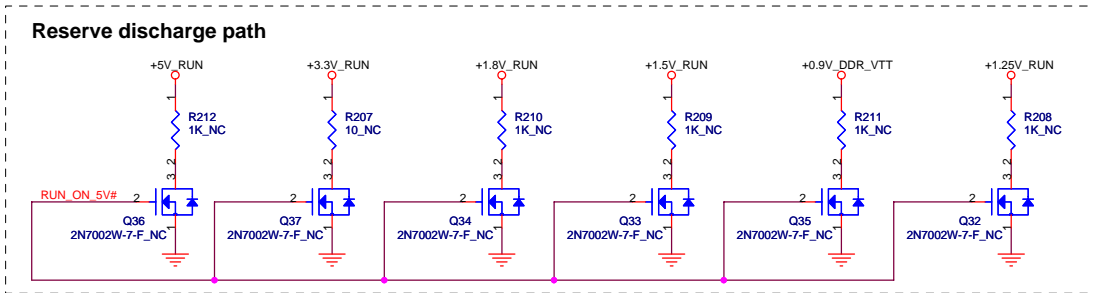
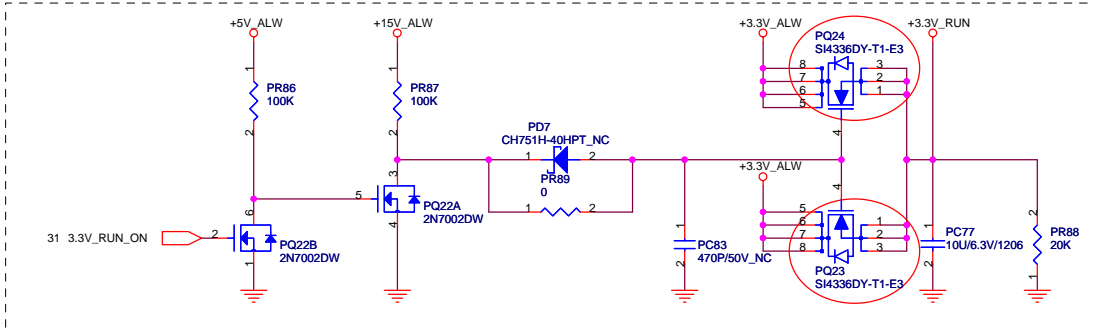
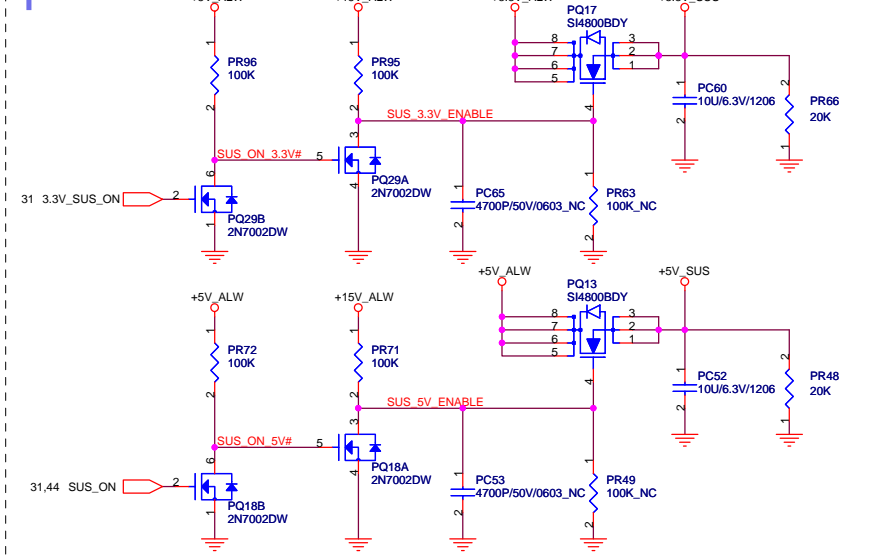
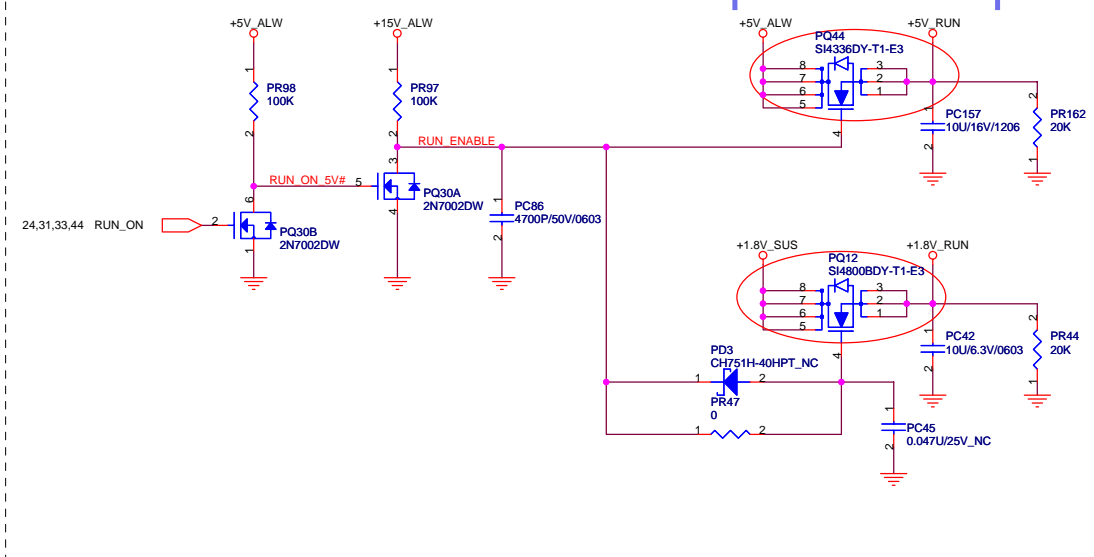
Power Sequencing, Voore Regulator
 Power Sequencing



Title		1.25V, 1.8V, 0.9V
Size	Document Number	Rev
	JM7	1A
Date:	Wednesday, June 28, 2006	Sheet 49 of 57

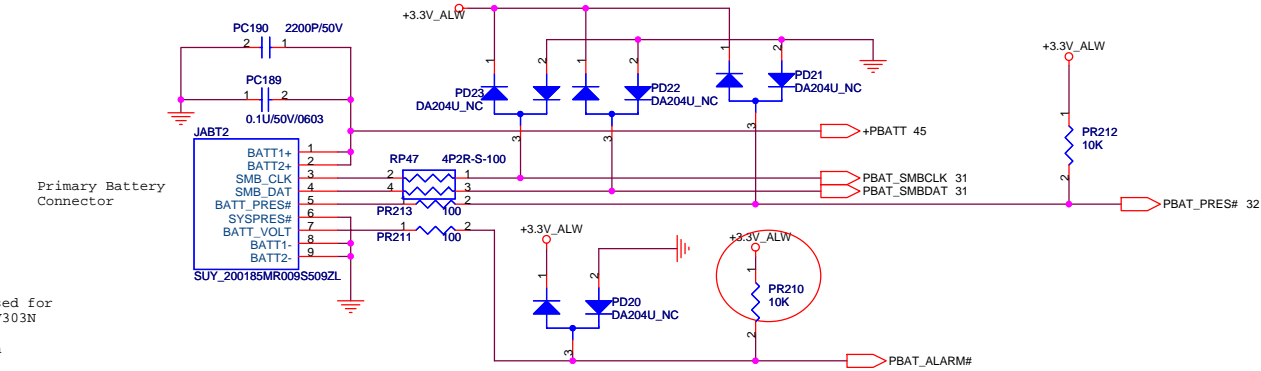
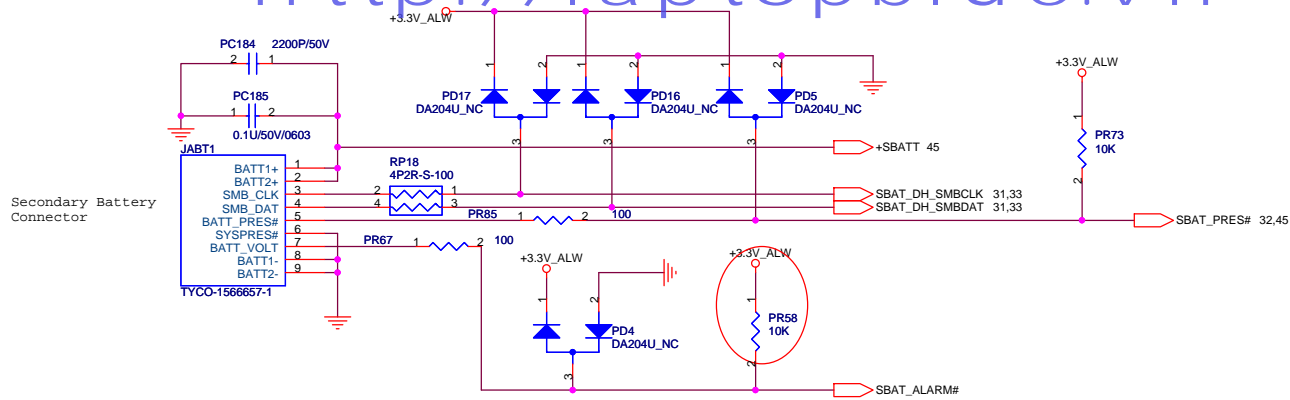
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**





QUANTA COMPUTER

Title		RUN POWER SW
Size	Document Number	Rev
JM7		1A
Date:	Wednesday, June 28, 2006	Sheet 53 of 57



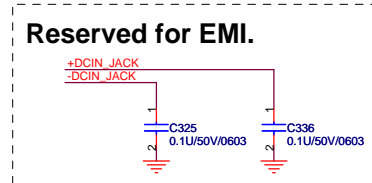
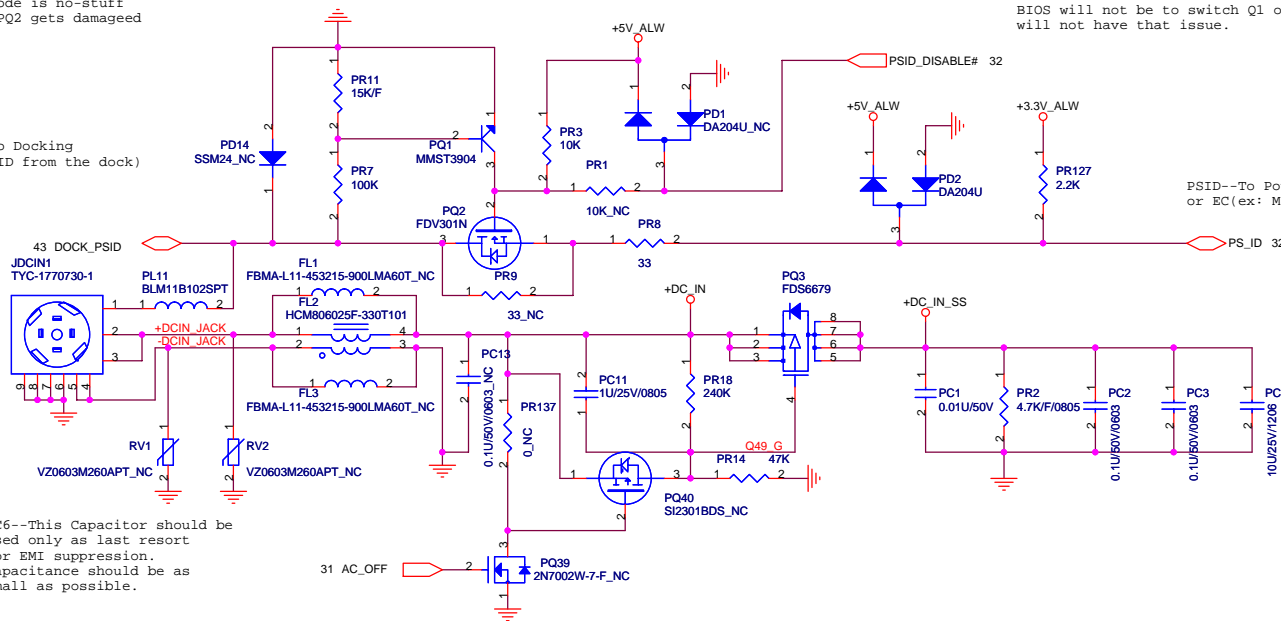
PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/buit-in ESD protection.MMBT100 BJT works in reverse conduction mode.

D12--This diode is no-stderr populate if PQ2 gets damaged by ESD.

PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.

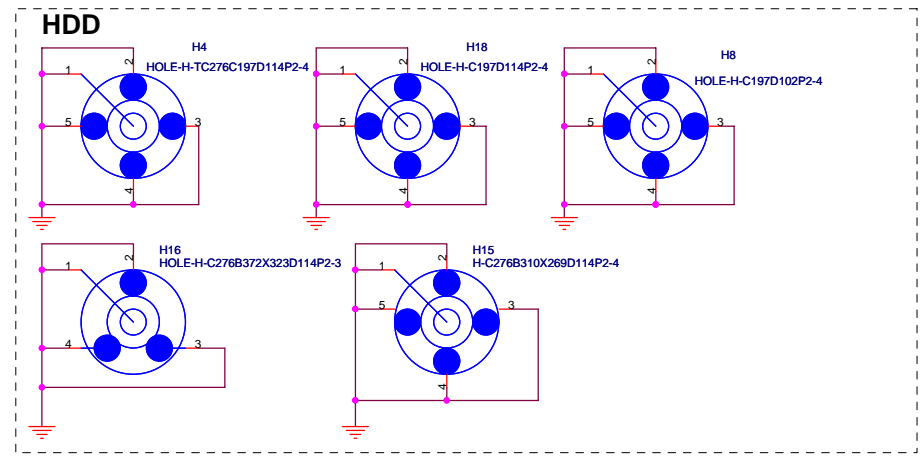
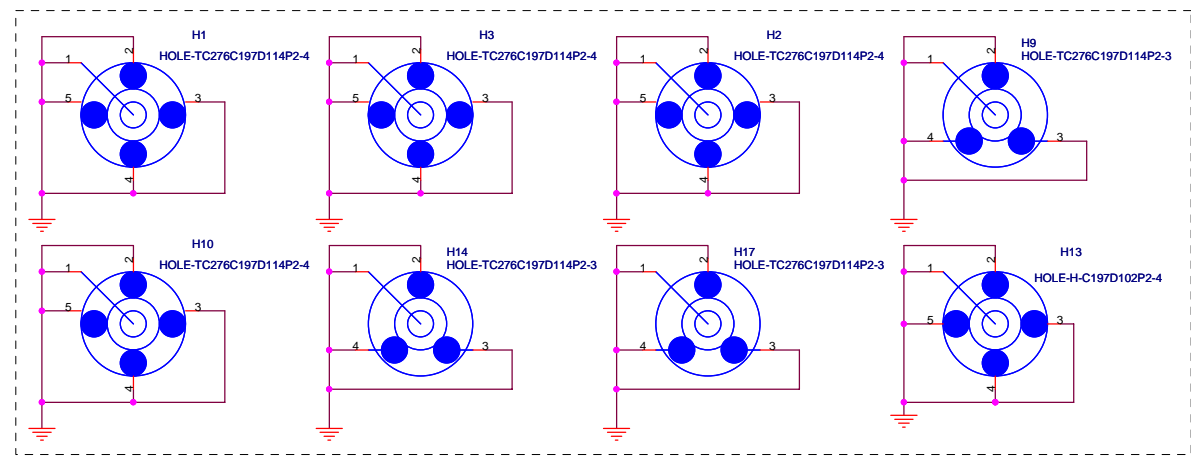
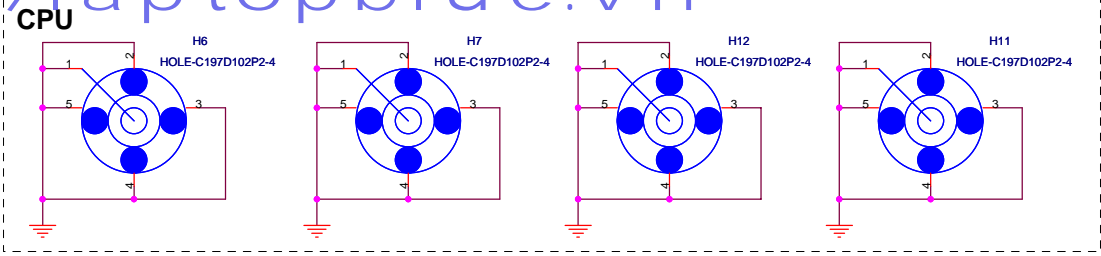
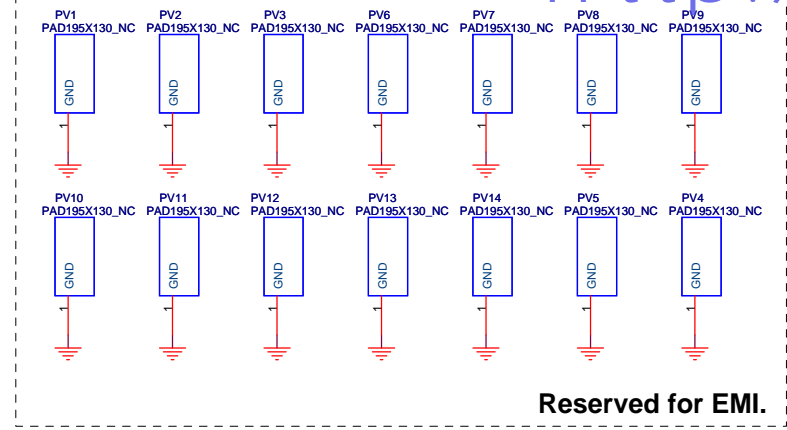
DOCK_PSID--To Docking connector(PSID from the dock)

PSID--To Power Management Controller or EC(ex: Macallan3)

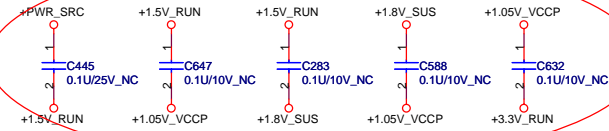


PC5--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.





Stitching caps



Page 26
SATA (HDD&CD_ROM)

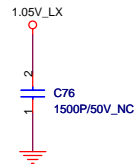
Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

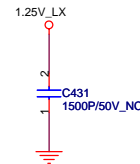
Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)



Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V



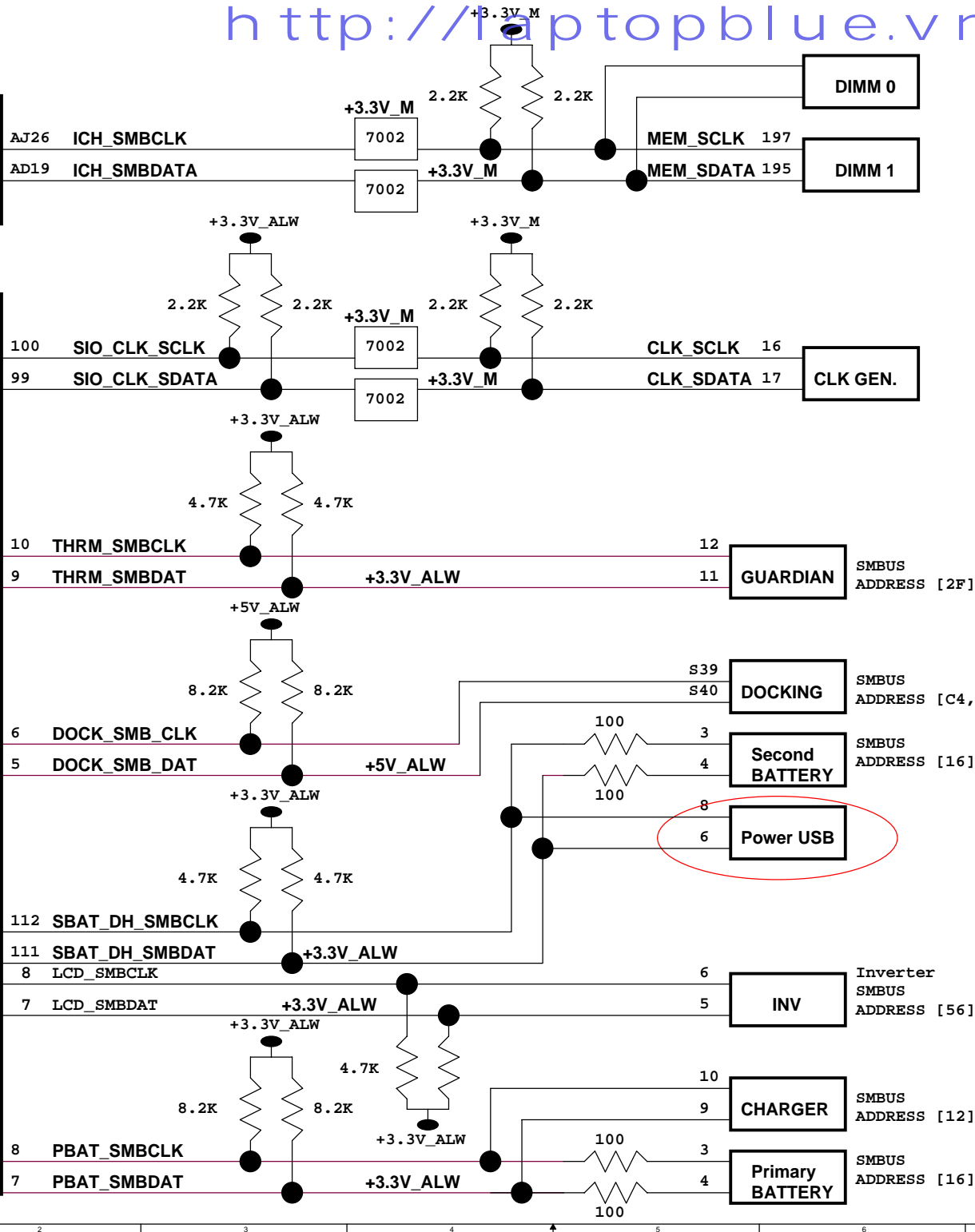
Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.

Page 51
CPU_MAX8786(3phase)

Page 52
D/D Power

ICH8-M

SIO MEC5025



QUANTA COMPUTER

Title: SMBUS BLOCK

Size	Document Number JM7	Rev 1A
------	------------------------	-----------

Date: Monday, June 26, 2006 Sheet 57 of 57