

Essentials Oak 14 Schematic

Chief River

2012-09-05

REV : A00


DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

h0005/15128/01/11h

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Cover Page		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012		Sheet 1 of 105

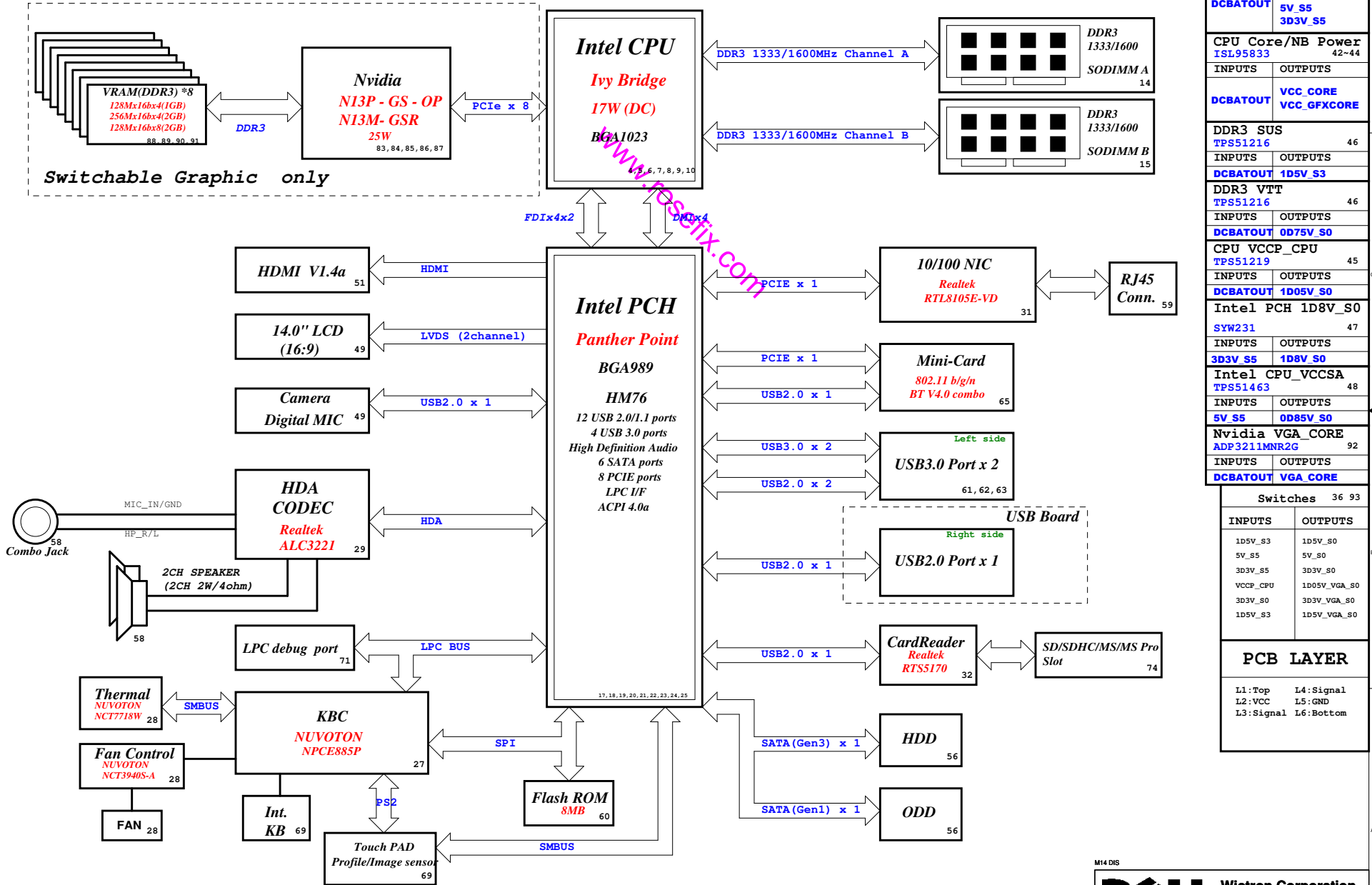
Project code: 91.4WT01.001

91.4XP01.001

PCB P/N : 12204

Revision: A00

Oak14 Block Diagram



CHARGER		40
BQ24727		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		41
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core/NB Power		42-44
ISL95833		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE VCC_GFXCORE	
DDR3 SUS		46
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3	
DDR3 VTT		46
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	0D75V_S0	
CPU VCCP_CPU		45
TPS51219		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
Intel PCH 1D8V_S0		47
SYW231		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S0	
Intel CPU VCCSA		48
TPS51463		
INPUTS	OUTPUTS	
5V_S5	0D85V_S0	
Nvidia VGA_CORE		92
ADP3211MNR2G		
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
Switches		36 93
INPUTS	OUTPUTS	
1D5V_S3	1D5V_S0	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
VCCP_CPU	1D05V_VGA_S0	
3D3V_S0	3D3V_VGA_S0	
1D5V_S3	1D5V_VGA_S0	
PCB LAYER		
L1:Top	L4:Signal	
L2:VCC	L5:GND	
L3:Signal	L6:Bottom	

Copyright © 2012 Dell

M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: C Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet: 2 of 105

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kohms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kohms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kohms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kohms ±5% pull-up resistor to PCH_VccDFTERM.
SATA1GP/ GPIO19	Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Panther Point require SPI flash connected directly to the Panther Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug. This signal has a 20k internal pull down resistor.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform. Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.
GPIO15	Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected. When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
BDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
BDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7k resistor to ensure proper strap setting when used as the chipset test interface. Refer to the latest platform debug design guide and platform design guide for more details. NOTE: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft strap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping Chief River Schematic Checklist Revision 1.5

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kohms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort 0: Enabled - An external Display Port device is connected to the Embedded Display Port pull-down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	PCIe Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

Sandy Bridge + Ivy Bridge Compatibility Requirements Chief River Schematic Checklist Revision 1.5

Pin Name	Configuration	Schematic Notes
DDR3_VREF	Sandy Bridge + Ivy Bridge Ivy Bridge	DDR3 VREF M1 and M3 Guidelines are required. Note: The M3 traces are routed to the Sandy Bridge Processor reserved pins. No change.
PROC_SELECT# & DF_TVS	Sandy Bridge + Ivy Bridge Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1k±5% series resistor. PROC_SELECT# also needs a 2.2k±5% pull up resistor to PCH_VccDFTERM rail. No change.
VCCIO VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a requirement for a separate VCCIO VR for Sandy Bridge + Ivy Bridge compatibility. No change.
VCCSA_SEL connection to VCCSA_VID[1:0] lines	Sandy Bridge + Ivy Bridge Ivy Bridge	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller. No change.
Layout Requirement on PCI Express Gen3	Sandy Bridge + Ivy Bridge Ivy Bridge	The total motherboard length for a pair of consecutive PCI Express Tx lanes be length matched within 100 mils (2.54 mm). No change.
GT Core VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	Depending on the PDBG specifications, some IVB GT2 SKUs may require a new VR controller and 2 phase VCC GT core VR. No change.
Processor PCI Express Graphics Guidelines	Sandy Bridge + Ivy Bridge (PCIe Gen3): Ivy Bridge	To support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 180 - 265 nF. No change.

Power Plane

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
IV_S0 IVS_V0 IVS_V1 IVS_V2 IVS_V3 IVS_V4 IVS_V5 IVS_V6 IVS_V7 IVS_V8 IVS_V9 IVS_V10 IVS_V11 IVS_V12 IVS_V13 IVS_V14 IVS_V15 IVS_V16 IVS_V17 IVS_V18 IVS_V19 IVS_V20 IVS_V21 IVS_V22 IVS_V23 IVS_V24 IVS_V25 IVS_V26 IVS_V27 IVS_V28 IVS_V29 IVS_V30 IVS_V31 IVS_V32 IVS_V33 IVS_V34 IVS_V35 IVS_V36 IVS_V37 IVS_V38 IVS_V39 IVS_V40 IVS_V41 IVS_V42 IVS_V43 IVS_V44 IVS_V45 IVS_V46 IVS_V47 IVS_V48 IVS_V49 IVS_V50 IVS_V51 IVS_V52 IVS_V53 IVS_V54 IVS_V55 IVS_V56 IVS_V57 IVS_V58 IVS_V59 IVS_V60 IVS_V61 IVS_V62 IVS_V63 IVS_V64 IVS_V65 IVS_V66 IVS_V67 IVS_V68 IVS_V69 IVS_V70 IVS_V71 IVS_V72 IVS_V73 IVS_V74 IVS_V75 IVS_V76 IVS_V77 IVS_V78 IVS_V79 IVS_V80 IVS_V81 IVS_V82 IVS_V83 IVS_V84 IVS_V85 IVS_V86 IVS_V87 IVS_V88 IVS_V89 IVS_V90 IVS_V91 IVS_V92 IVS_V93 IVS_V94 IVS_V95 IVS_V96 IVS_V97 IVS_V98 IVS_V99	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.75V 0.33V to 1.25V 1.8V 3.3V 1V	S0 S3	CPU Core Rail Graphics Core Rail
IV_USBK_S3 IVS_S3 IVR_PREF_S3	5V 1.5V 0.75V	S3	
IV_CSBADOUT IV_S5 IV_AUX_S5 IVS_S5 IVS_AUX_S5	6V-14.1V 6V-14.1V 5V 3.3V 3.3V	All S states	AC Brick Mode only
IVS_LAN_S5	3.3V	NOL_EN	Legacy WOL
IVS_AUX_S0C	3.3V	DSW_Sx	ON for supporting Deep Sleep states
IVS_AUX_S5	3.3V	GI_Sx	Powered by Li Coin Cell in G3 and +V3ALM in Sx

PCIe Routing

LANE	X
LANE1	X
LANE2	X
LANE3	Mini Card1 (WLAN)
LANE4	x
LANE5	X
LANE6	Onboard LAN
LANE7	X
LANE8	X

USB Table

Pair	Device
0	USB3.0 port1
1	USB3.0 port2, with Debug Port
2	USB2.0 port3
3	X
4	X
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	X
9	X
10	CARD READER
11	Mini Card (WLAN)
12	X
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

M14 DS
 **Wistron Corporation**
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
 Title: **Table of Content**
 Doc No: **OAK14 Chief River DIS**
 Date: **Wednesday, September 05, 2012** Sheet **3** of **106**



SSID = CPU

D

C

B

A

D

C

B

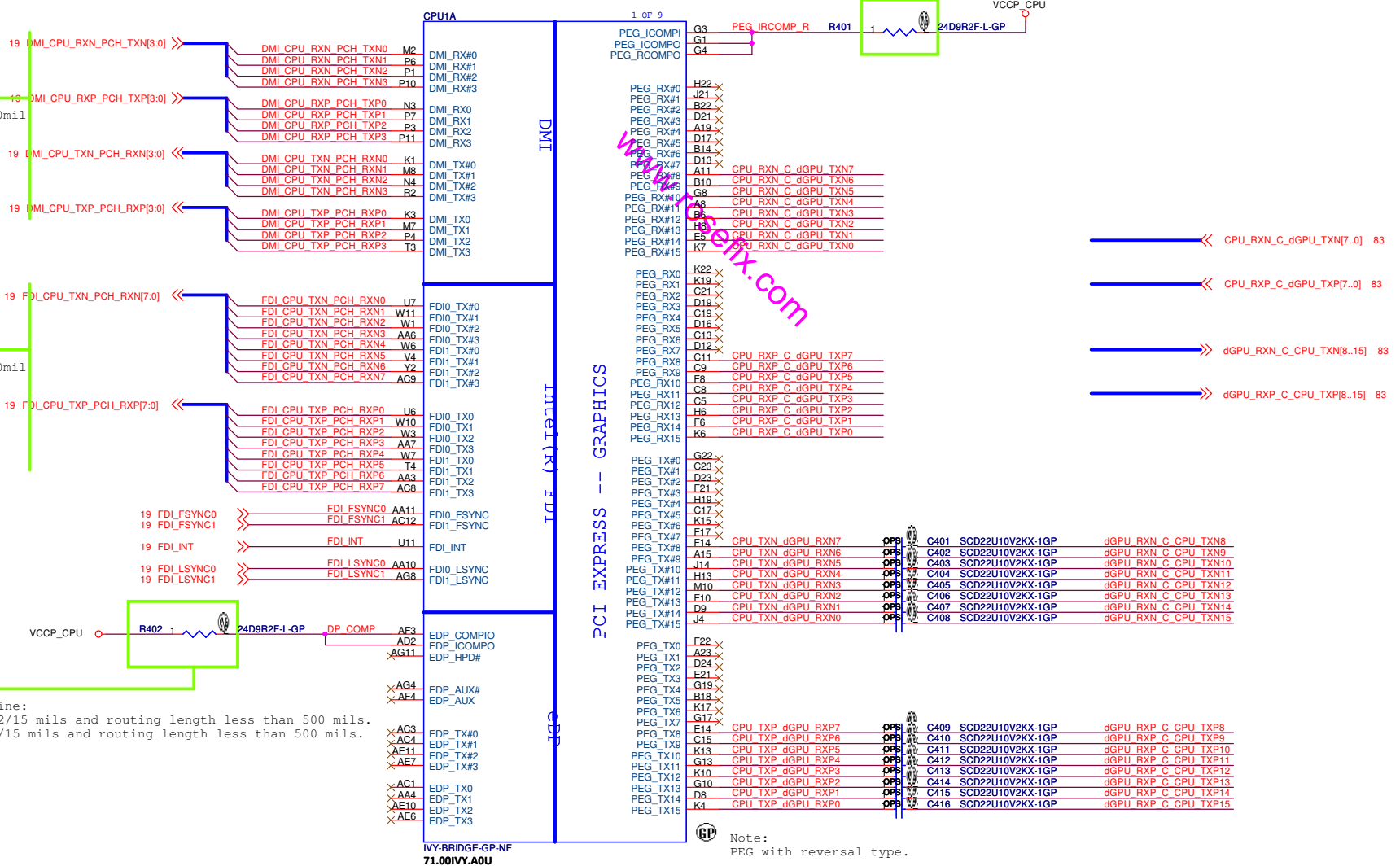
A

Layout Note:
DMI trace length 2000-8000mil

Layout Note:
FDI trace length 2000-6500mil

Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
PEG with reversal type.

Copyright © 2012 Dell Inc. All rights reserved. This document is the property of Dell Inc. and is intended for use only by the individual named.

M14 DIS

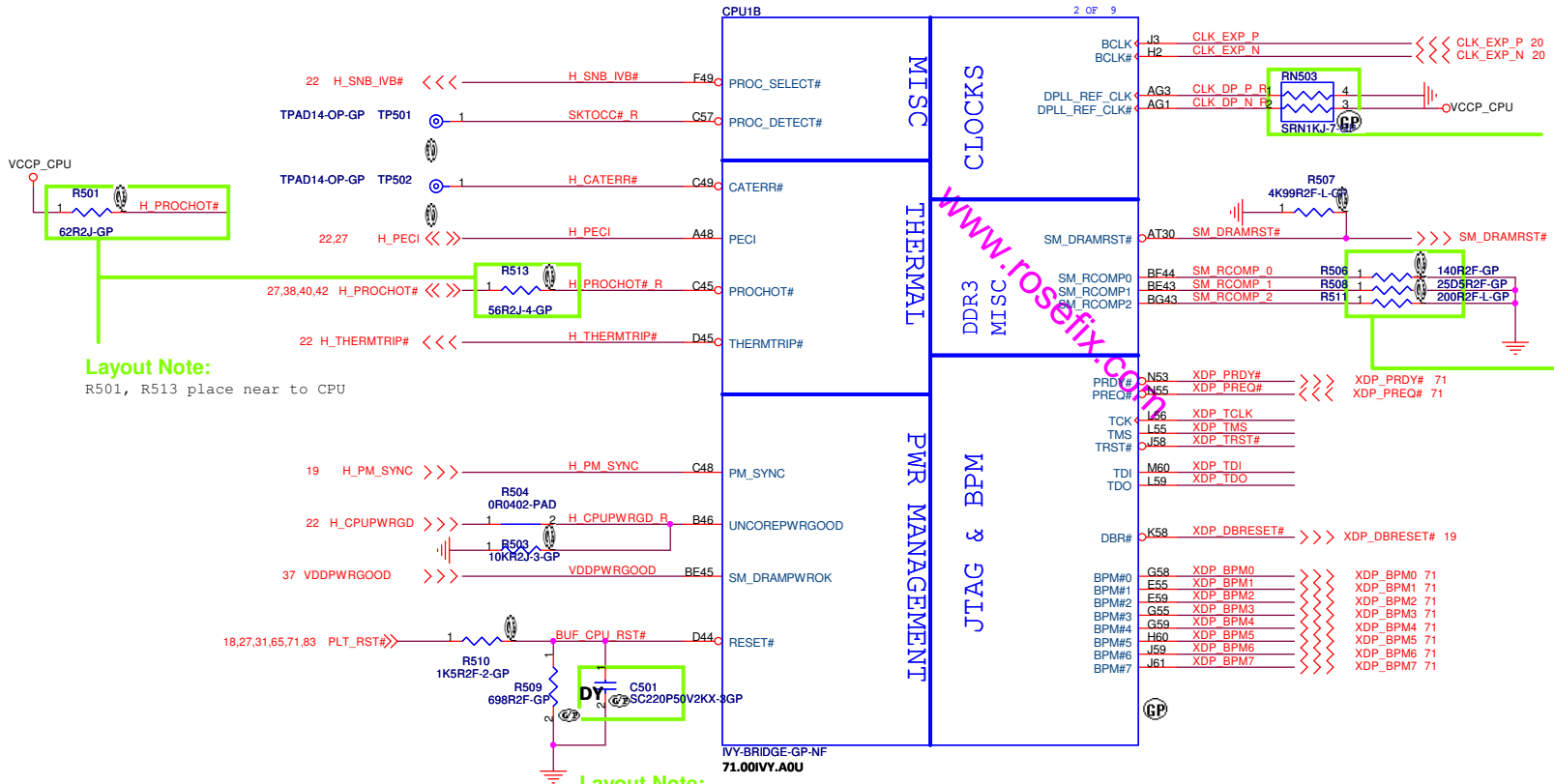
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(PCIE/DMI/FDI)**

Size: AS Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 4 of 105

SSID = CPU

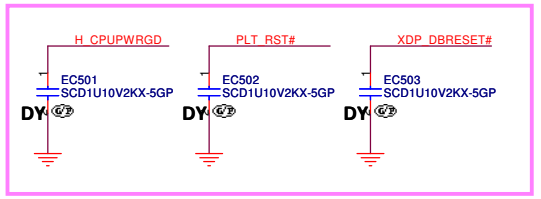


Layout Note: Checking the connector pin's LAYOUT

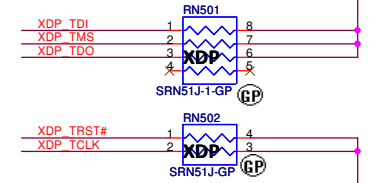
Layout Note: R501, R513 place near to CPU

Layout Note: Signal Routing Guideline: SM_RCOMP keep routing length less than 500 mils. Trace width = 15mil

Layout Note: C501 place near to CPU



reserve for EMI Request



h0p0y0t02000P.Mh

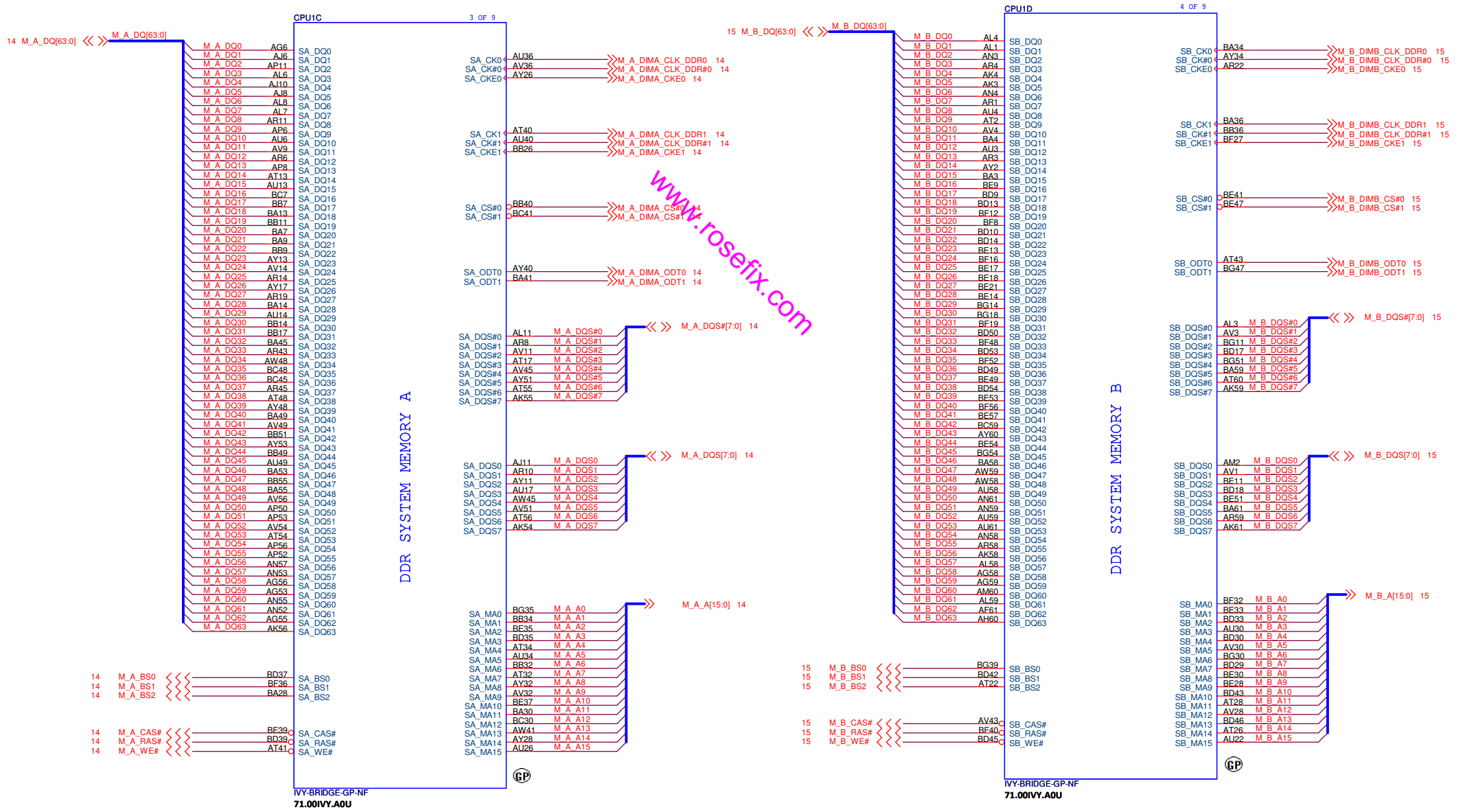
M14 DIS

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(THERMAL/CLOCK/PM)**

Size A3	Document Number	Rev A00
OAK14 Chief River DIS		
Date: Wednesday, September 05, 2012	Sheet 5	of 105

SSID = CPU



www.rosefix.com

M14 DIS

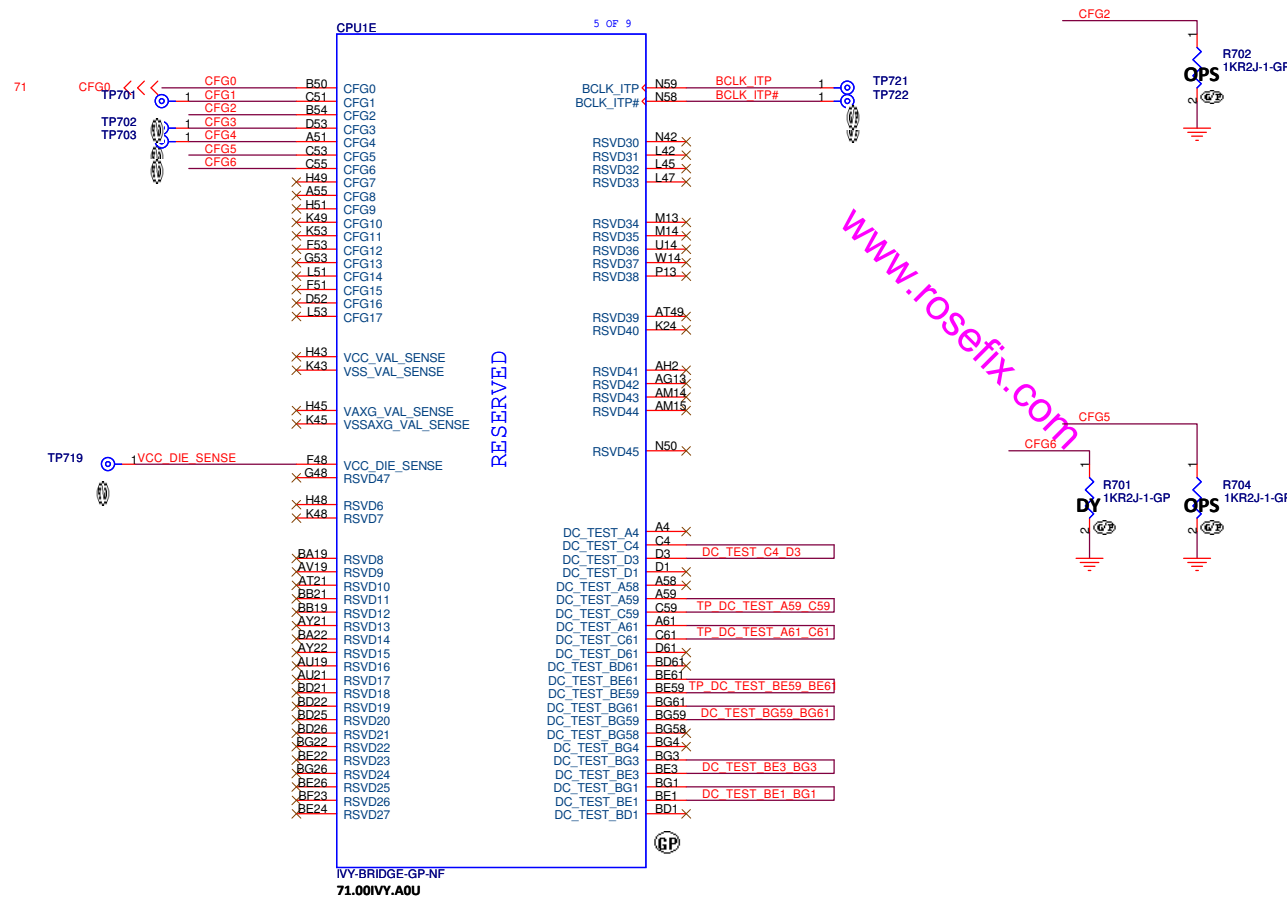
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

Size A3 Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 6 of 105

h0p0jy1512866P.M



PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express

www.rosefix.com

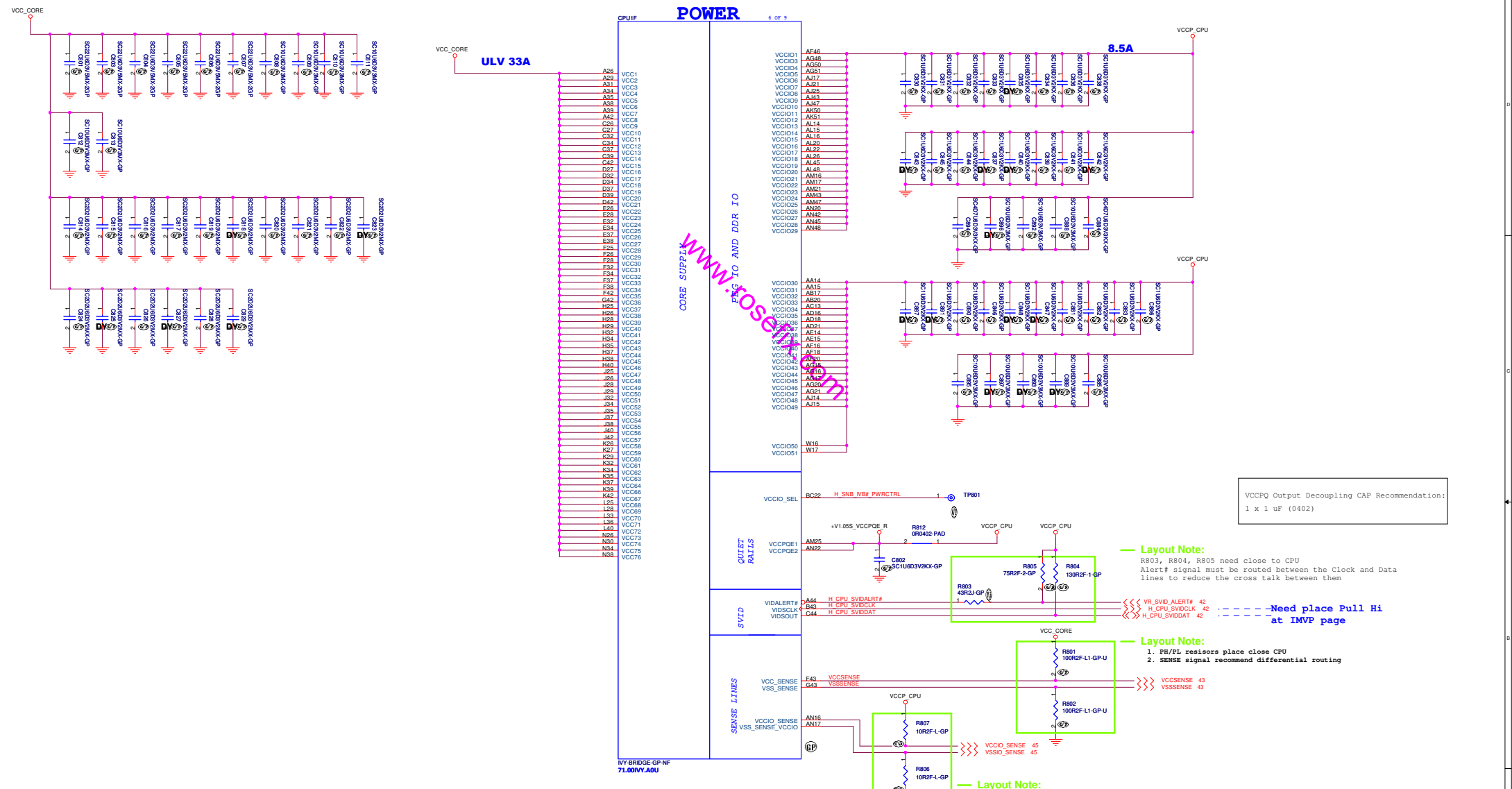
RESERVED

IVY-BRIDGE-GP-NF
71.00IVY.A0U

M14 DIS

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (RESERVED)			
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00	
Date: Wednesday, September 05, 2012	Sheet: 7	of: 105	

h 06 05 / 15 12 28 26 PM



Voltage Rail	Voltage (V)	Iccmax (A)
VCC_CORE	0.9-1.52	33
VAXG	0-1.52	29 (gr2)
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.675-0.9	4
VCCPLL	1.8	1.2

Refer to CPU EDS V.1.7.5

VCCPO Output Decoupling CAP Recommendation:
1 x 1 uF (0402)

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Need place Pull Hi at IMVP page

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Copyright © 2012 Dell Inc. All rights reserved. Dell, the Dell logo, and Wistron are trademarks of Dell Inc. in the United States and other countries.

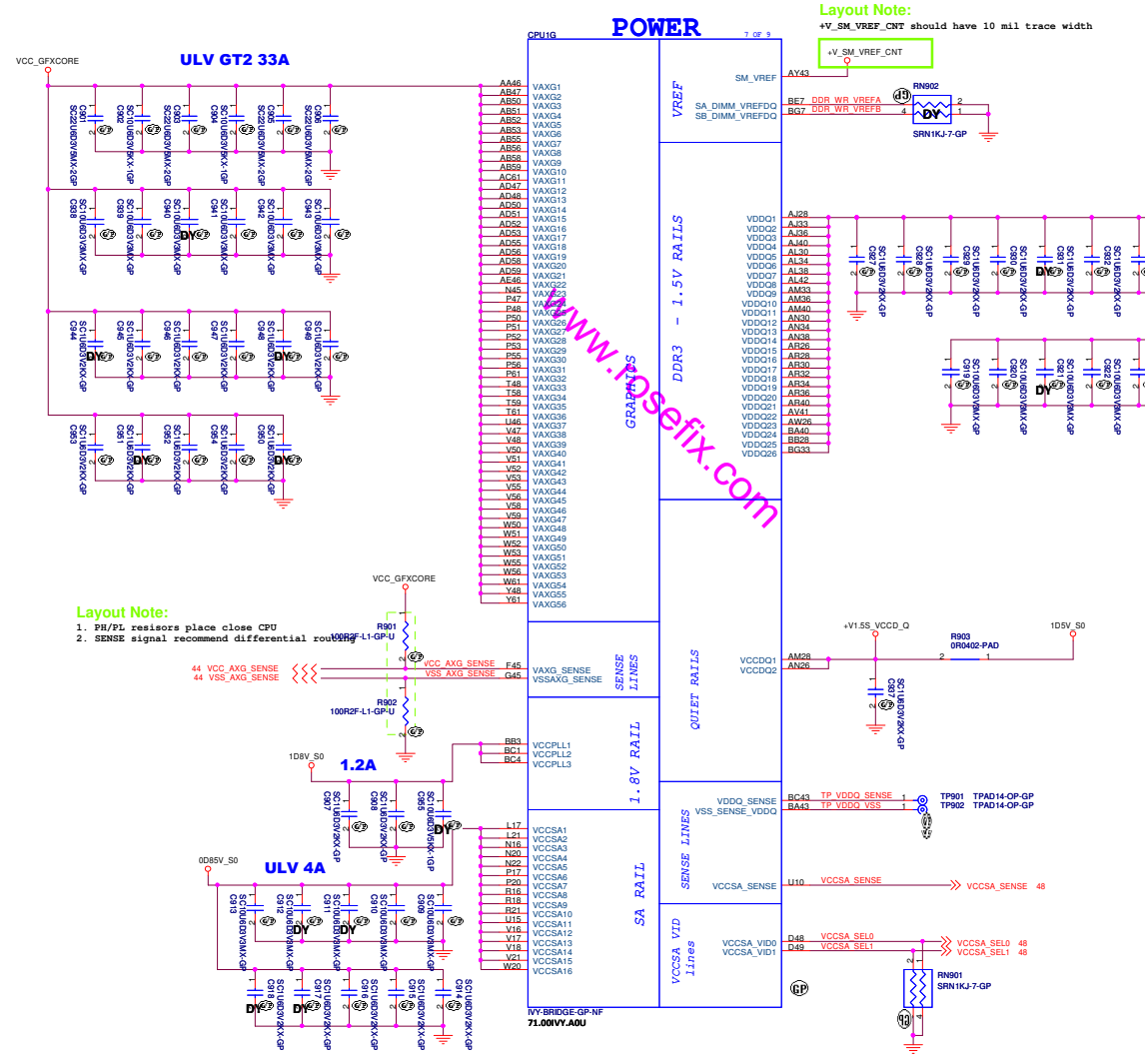
M14 DIS

DELL Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VCC CORE)**

Size A2 Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 8 of 106



Voltage Rail	Voltage (V)	Iccmax (A)
VCC_CORE	0.3-1.52	33
VAXG	0-1.52	29 (GT2)
VCCIO	1.05	8.5
VDDO	1.5	5
VCCSA	0.675-0.9	3
VCCPLL	1.8	1.2

Refer to CPU EDS V2.0

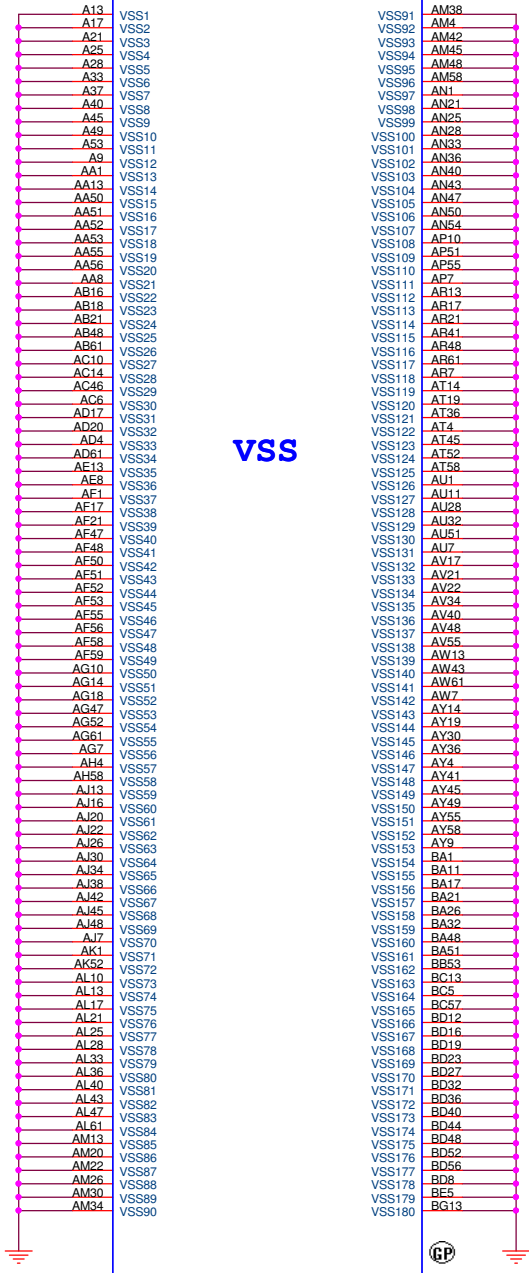
- Layout Note:**
1. P8/P1 resistors place close CPU
 2. SENSE signal recommend differential routing

VCCSA Power Select		
Voltage (ULV)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

hOp9y5h286Pm

SSID = CPU

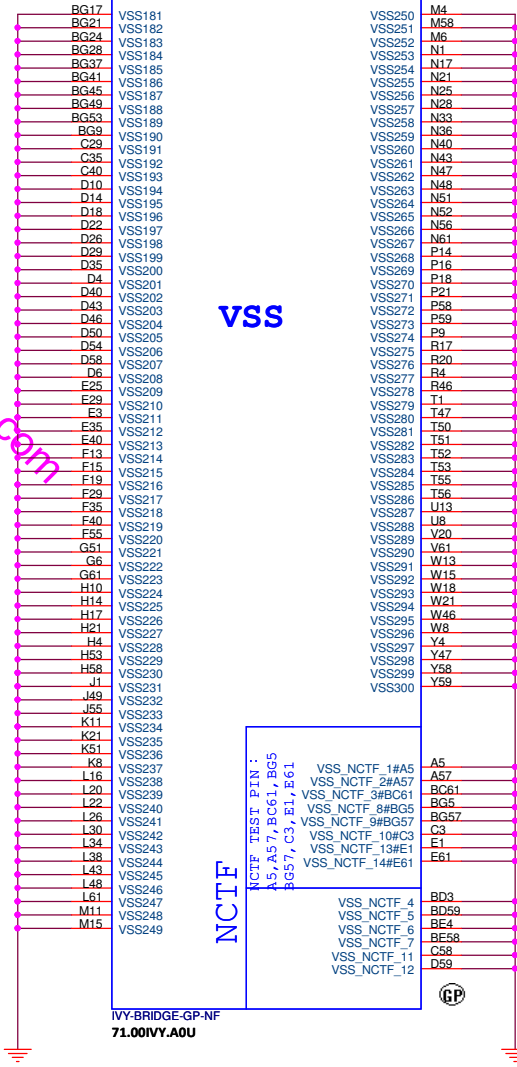
CPU1H 8 OF 9



VSS

IVY-BRIDGE-GP-NF
71.00IVY.A0U

CPU1I 9 OF 9



VSS

NCTF

NCTF TEST PIN :
 A5, A57, BC61, BG5
 BG57, C3, E1, E61
 VSS_NCTF_1#A5
 VSS_NCTF_2#A57
 VSS_NCTF_3#BC61
 VSS_NCTF_9#BG5
 VSS_NCTF_9#BG57
 VSS_NCTF_10#C3
 VSS_NCTF_13#E1
 VSS_NCTF_14#E61
 VSS_NCTF_4
 VSS_NCTF_5
 VSS_NCTF_6
 VSS_NCTF_7
 VSS_NCTF_11
 VSS_NCTF_12

IVY-BRIDGE-GP-NF
71.00IVY.A0U

M14 DIS




Title CPU (VSS)		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 10	of 105

Copyright © 2012 Intel Corporation

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		XDP
Size A3	Document Number	Rev A00
Date: Wednesday, September 05, 2012		Sheet 11 of 105

h0605/151280617.Mn

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 12 of 105

h0605/151280617.Mn

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
(Reserved)		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 13 of 105	

h0605/15128067.Mn

www.rosefix.com

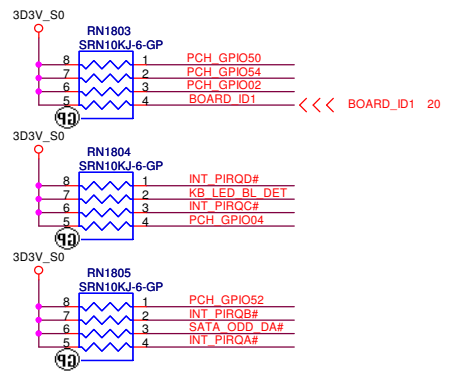
(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 16 of 105

h0605/151280617.Mn

SSID = PCH



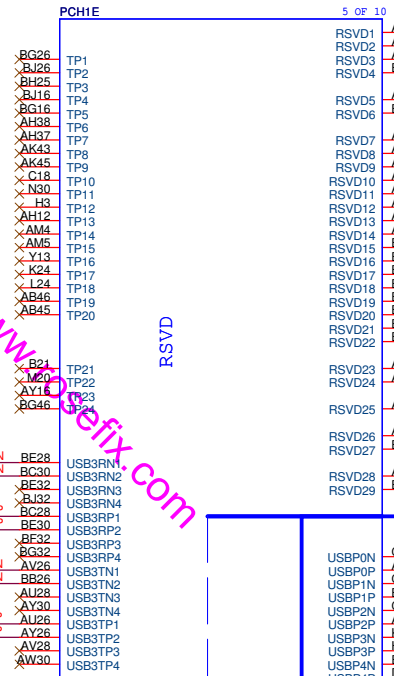
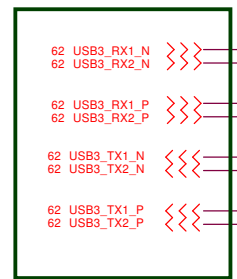
USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Layout Note:
Trace Length :
PCH ~9000mil~~Cap~~1000mil~~CONN

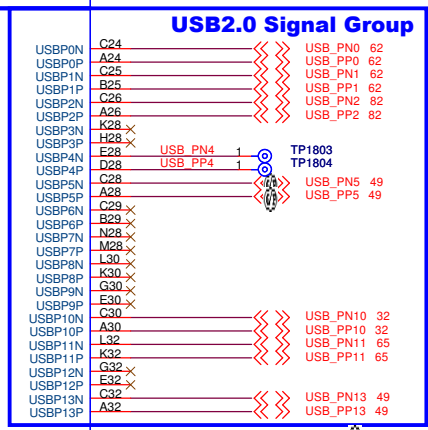


www.digifox.com

USB Table

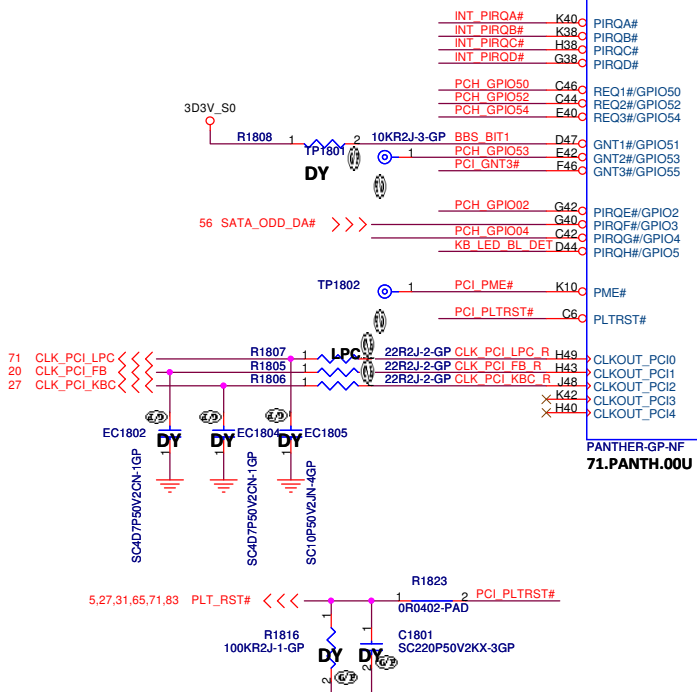
Pair	Device
0	USB3.0 port2
1	USB3.0 port1, with Debug Port
2	USB2.0 port3
3	NC
4	NC
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	NC
9	NC
10	Card reader
11	WLAN
12	NC
13	CAMERA

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.



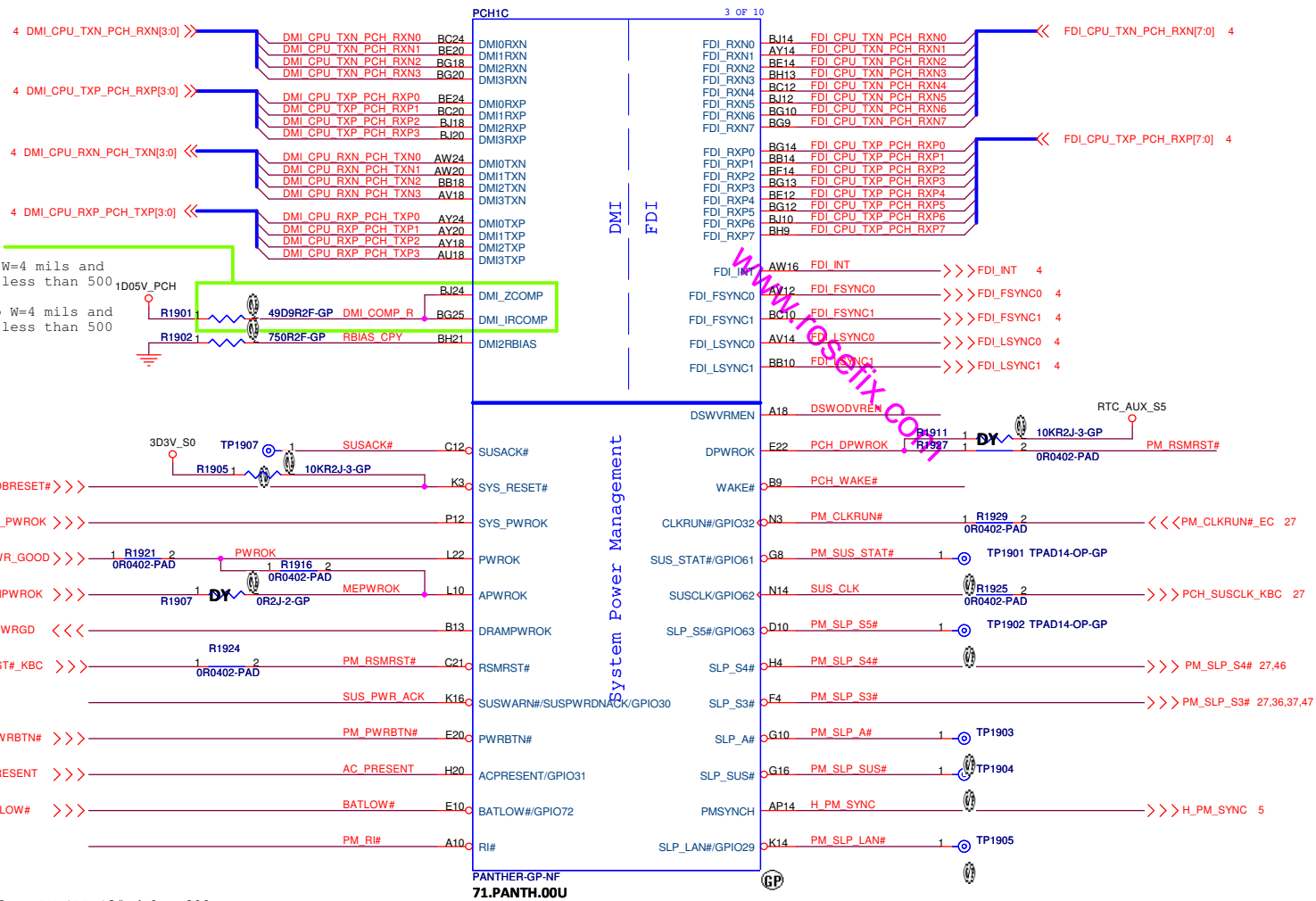
Layout Note:

1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil



SSID = PCH

Layout Note:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

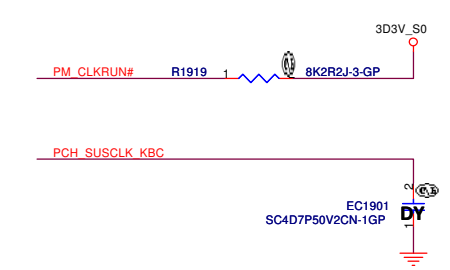


DSWODVREN - On Die DSW VR Enable

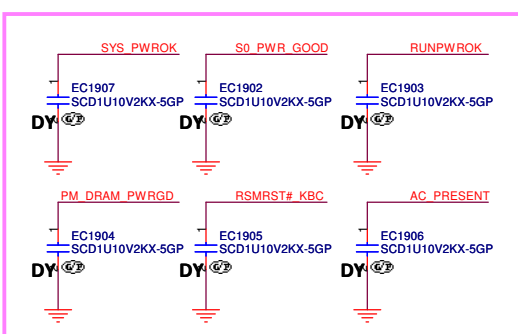
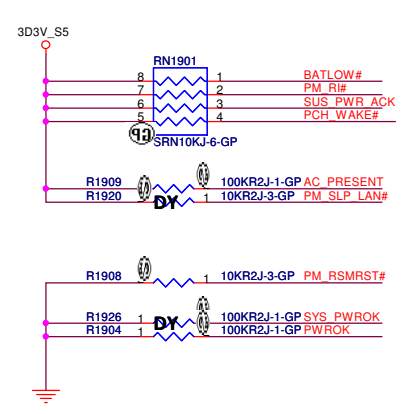
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5

DSWODVREN R1917 10K R2J-3-GP



Sequence:
 S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



reserve for EMI Request

h0p05/15128061M

M14 DIS

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

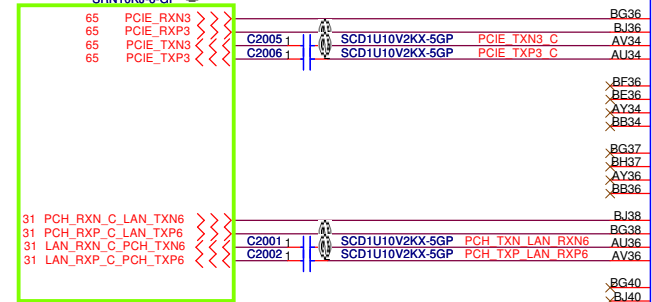
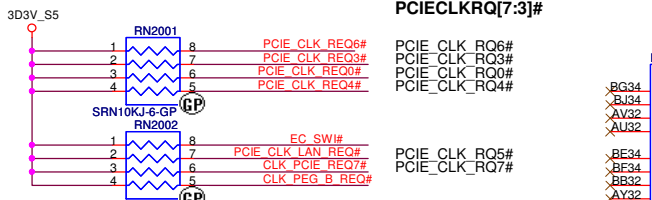
Title: **PCH (DM I/FDI/PM)**

Size A3 Document Number: **DNE40 14 CR DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 19 of 105

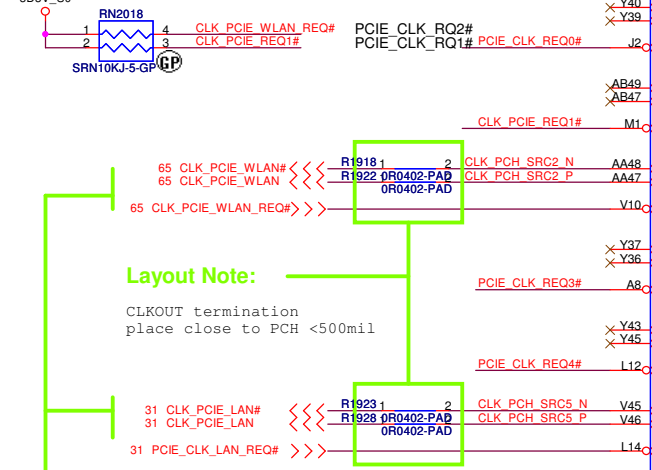
SSID = PCH

S5 power rail CLKREQ#:
 PCIECLKRQ[0]#
 PCIECLKRQ[7:3]#



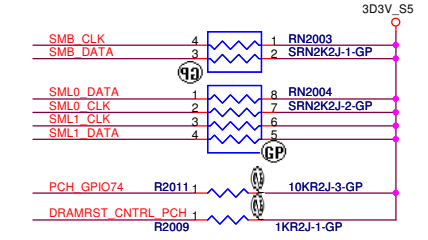
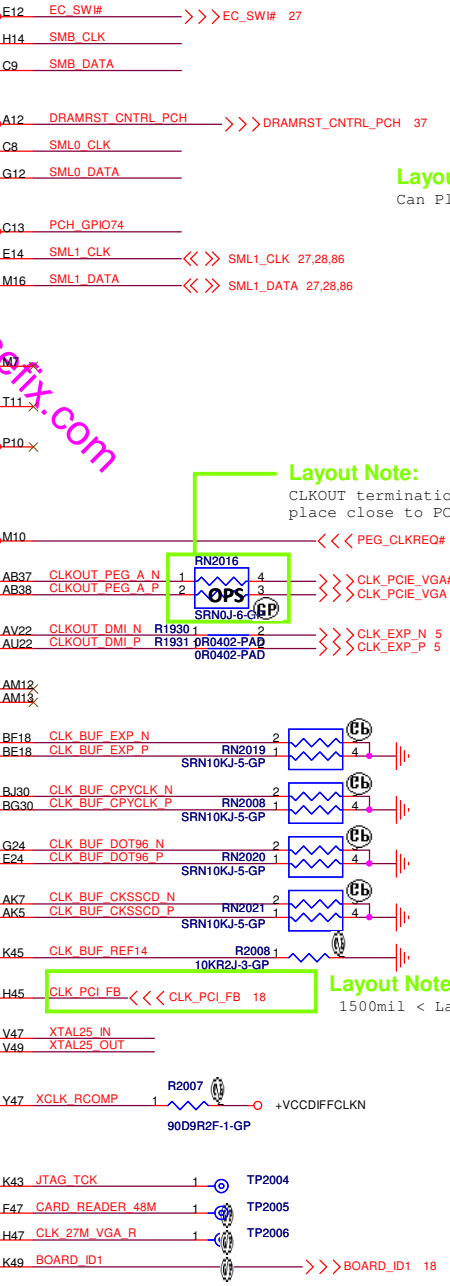
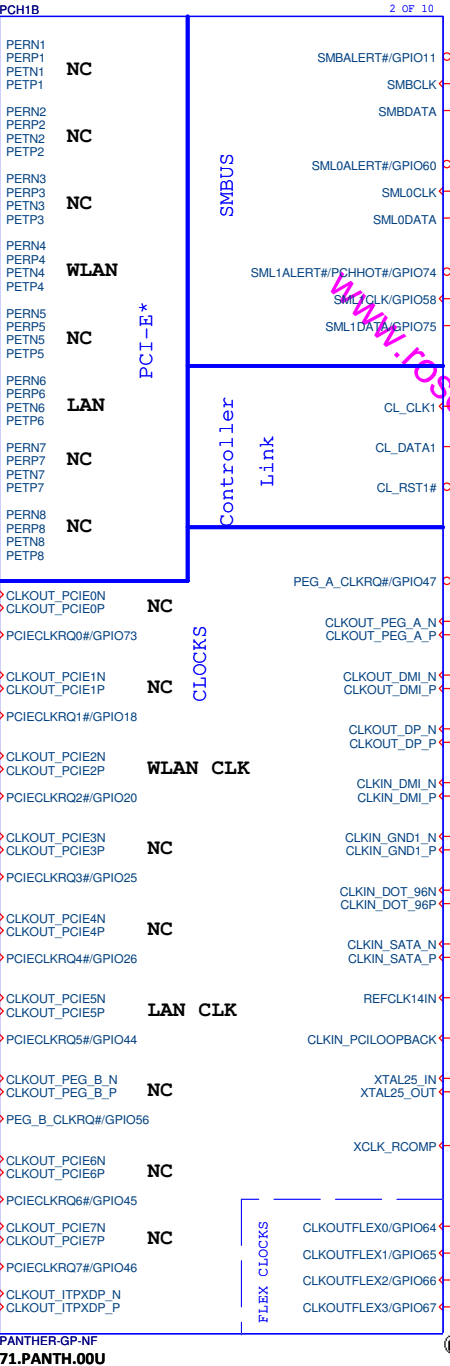
Layout Note:
 Layout trace < 14000mil

S0 power rail CLKREQ#:
 PCIECLKRQ[2:1]#

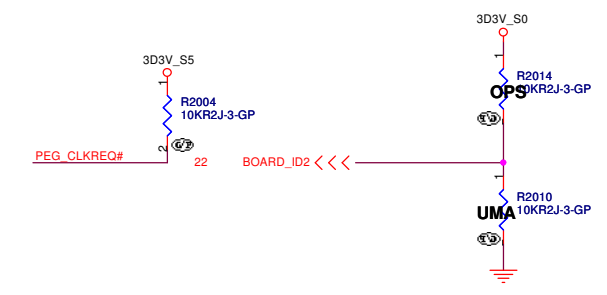
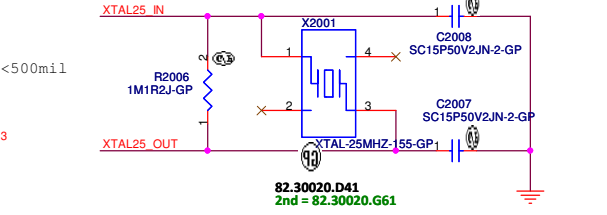
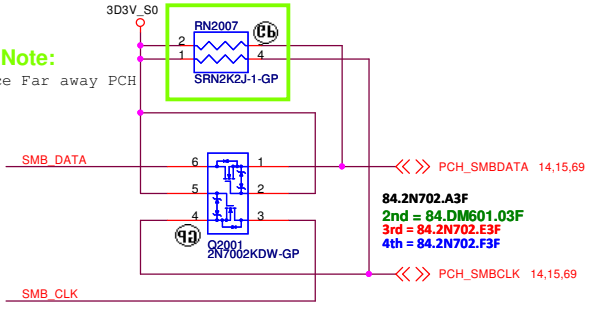


Layout Note:
 CLKOUT termination place close to PCH < 500mil

Layout Note:
 Layout trace < 14000mil



Layout Note:
 Can Place Far away PCH



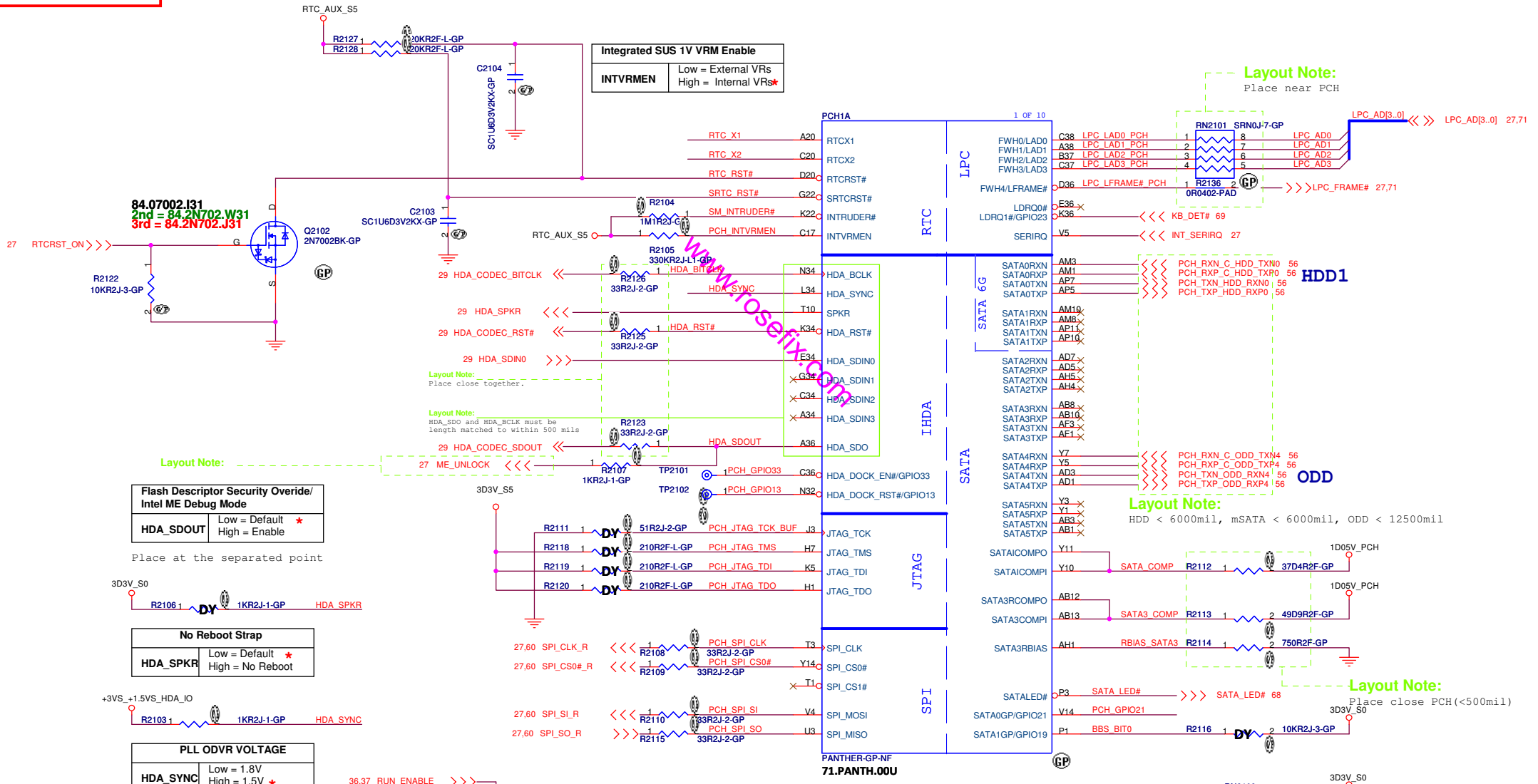
BIOS UMA/DIS Strap pin

	BOARD_ID1	BOARD_ID2
UMA (NV)	0	0
UMA	1	0
Optimus (NV)	1	1

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Copyright © 2012 Dell Inc. All rights reserved. This document is the property of Dell Inc. and is intended for use only by the individual named.

SSID = PCH



Integrated SUS 1V VRM Enable

INTVRMEN	Low = External VRs
	High = Internal VRs*

Layout Note:
Place near PCH

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

Flash Descriptor Security Override/ Intel ME Debug Mode

HDA_SDOOUT	Low = Default *
	High = Enable

Place at the separated point

No Reboot Strap

HDA_SPKR	Low = Default *
	High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V
	High = 1.5V *

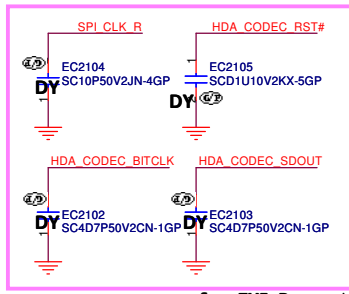
Layout Note:
Place close together.

Layout Note:
HDA_SDO and HDA_BCLK must be length matched to within 500 mils

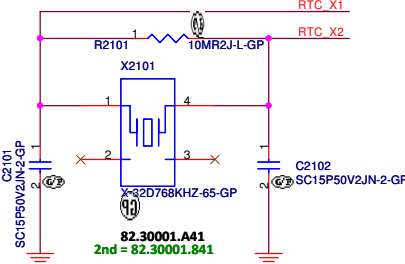
Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil

Layout Note:
Place close PCH(<500mil)

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



reserve for EMI Request



M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

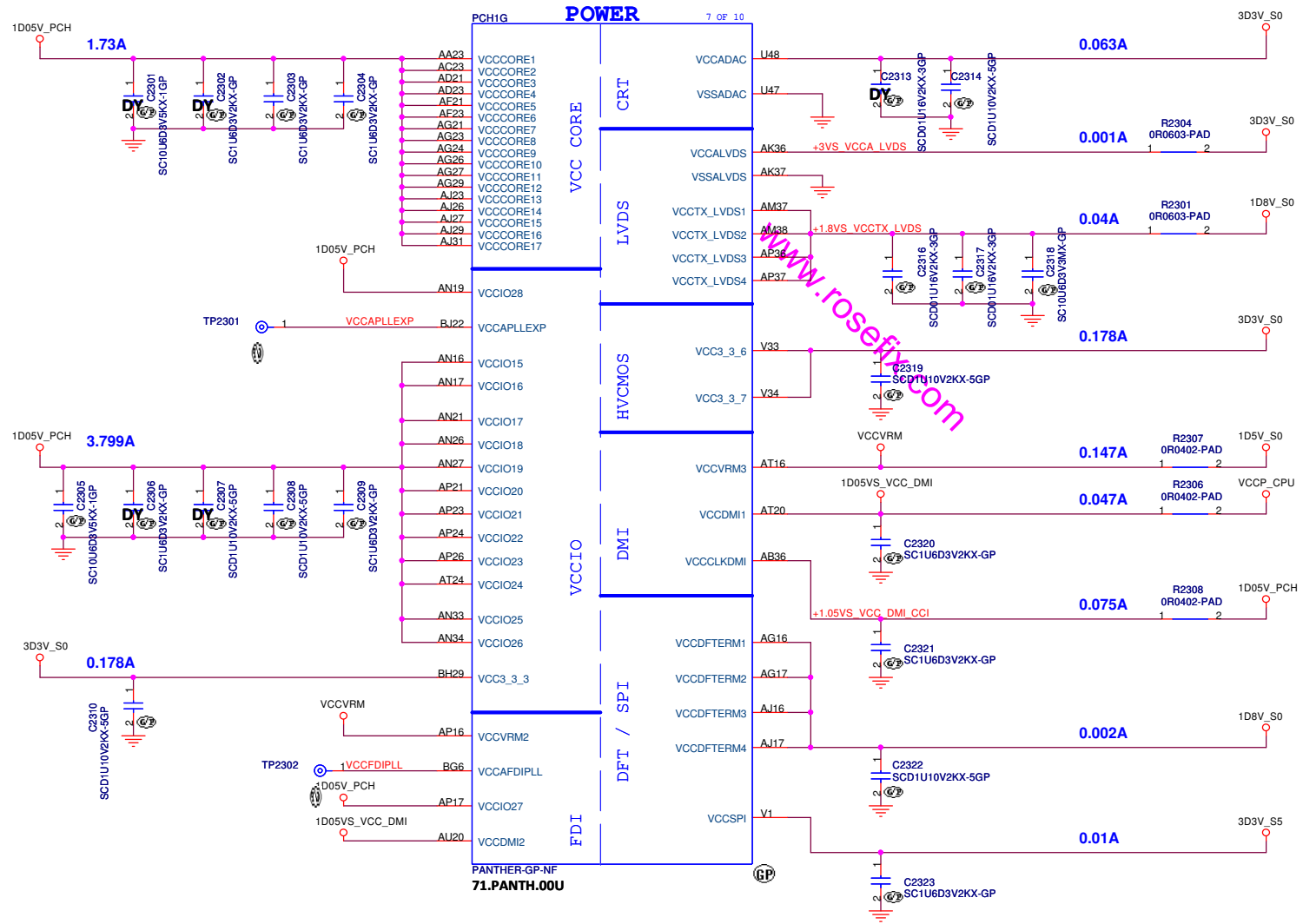
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size A3	Document Number	Rev A00
OAK14 Chief River DIS		

Date: Wednesday, September 05, 2012 Sheet 21 of 105

h 0 0 0 5 y 1 5 1 2 8 2 8 2 8 2 8 P M h

SSID = PCH



Voltage Rail	Voltage (V)	Iccmax (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8

check

h 0 0 0 5 / 1 5 1 2 8 2 8 2 6 P M m

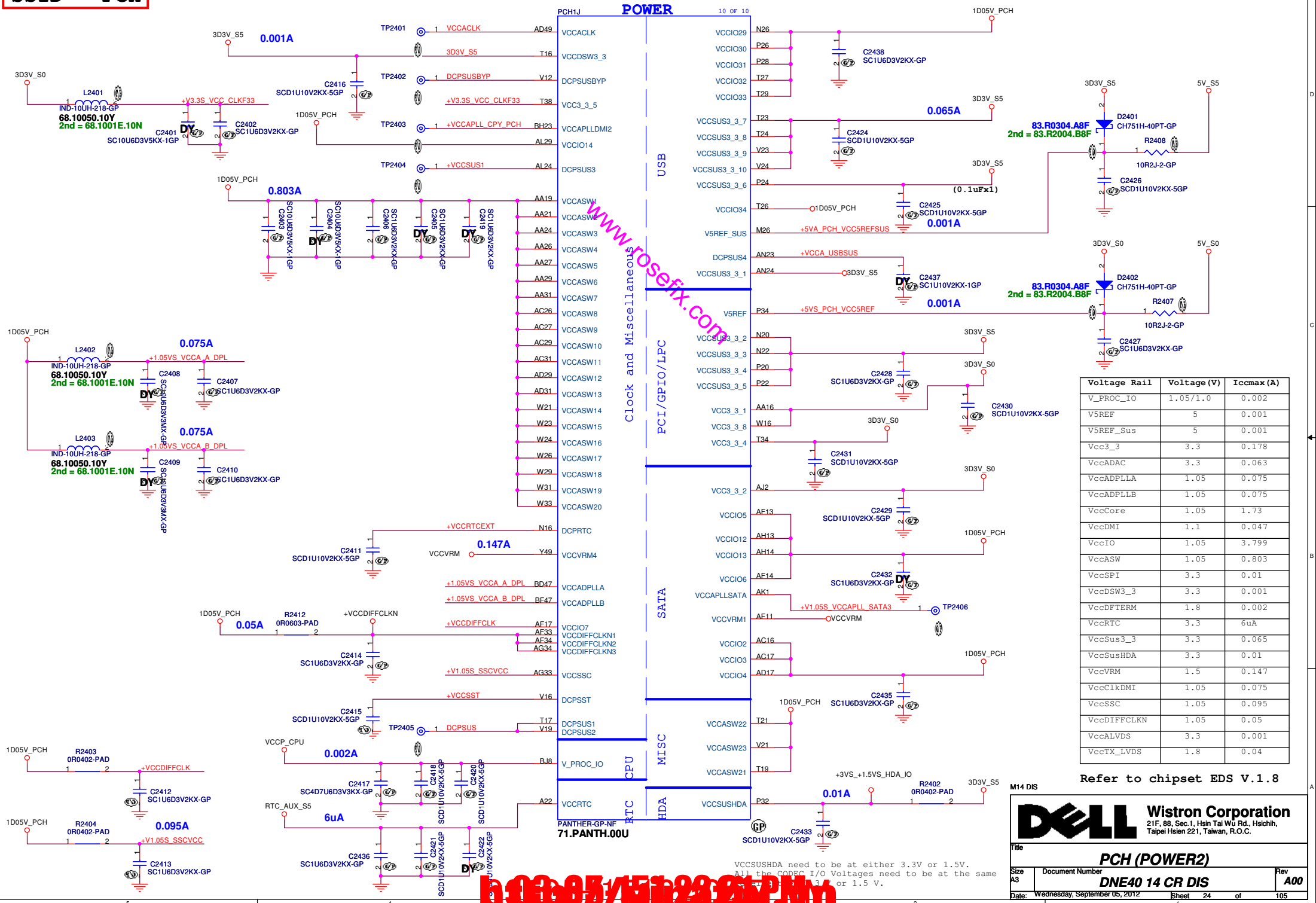
M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet 23	of 105

SSID = PCH



Voltage Rail	Voltage (V)	Iccmax (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8

M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER2)**

Size A3 Document Number: **DNE40 14 CR DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 24 of 105

VCCSUS_HDA need to be at either 3.3V or 1.5V.
All the CODEP I/O Voltages need to be at the same level as either 3.3V or 1.5V.

NO. 03/15/2012

SSID = PCH

PCH1H 8 OF 10

H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK9
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB43	VSS10	VSS89	AL21
AB5	VSS11	VSS90	AL23
AB7	VSS12	VSS91	AL26
AC19	VSS13	VSS92	AL27
AC2	VSS14	VSS93	AL31
AC21	VSS15	VSS94	AL33
AC24	VSS16	VSS95	AL34
AC33	VSS17	VSS96	AL48
AC34	VSS18	VSS97	AM11
AC48	VSS19	VSS98	AM14
AD10	VSS20	VSS99	AM36
AD11	VSS21	VSS100	AM39
AD12	VSS22	VSS101	AM43
AD13	VSS23	VSS102	AM45
AD19	VSS24	VSS103	AM46
AD24	VSS25	VSS104	AM7
AD26	VSS26	VSS105	AN2
AD27	VSS27	VSS106	AN29
AD33	VSS28	VSS107	AN3
AD34	VSS29	VSS108	AN31
AD36	VSS30	VSS109	AP12
AD37	VSS31	VSS110	AP19
AD38	VSS32	VSS111	AP28
AD39	VSS33	VSS112	AP30
AD4	VSS34	VSS113	AP32
AD40	VSS35	VSS114	AP38
AD42	VSS36	VSS115	AP4
AD43	VSS37	VSS116	AP42
AD45	VSS38	VSS117	AP46
AD46	VSS39	VSS118	AP8
AD8	VSS40	VSS119	AR2
AE2	VSS41	VSS120	AR48
AE3	VSS42	VSS121	AT11
AE10	VSS43	VSS122	AT13
AE12	VSS44	VSS123	AT18
AD14	VSS45	VSS124	AT22
AD16	VSS46	VSS125	AT26
AE16	VSS47	VSS126	AT28
AE19	VSS48	VSS127	AT30
AF24	VSS49	VSS128	AT32
AF26	VSS50	VSS129	AT34
AF27	VSS51	VSS130	AT39
AF29	VSS52	VSS131	AT42
AF31	VSS53	VSS132	AT46
AF38	VSS54	VSS133	AT7
AF4	VSS55	VSS134	AU24
AF42	VSS56	VSS135	AU30
AF46	VSS57	VSS136	AV16
AF5	VSS58	VSS137	AV20
AF7	VSS59	VSS138	AV24
AF8	VSS60	VSS139	AV30
AG19	VSS61	VSS140	AV38
AG2	VSS62	VSS141	AV4
AG31	VSS63	VSS142	AV43
AG48	VSS64	VSS143	AV8
AH11	VSS65	VSS144	AW14
AH3	VSS66	VSS145	AW18
AH36	VSS67	VSS146	AW2
AH39	VSS68	VSS147	AW22
AH40	VSS69	VSS148	AW26
AH42	VSS70	VSS149	AW28
AH46	VSS71	VSS150	AW32
AH7	VSS72	VSS151	AW34
AJ19	VSS73	VSS152	AW36
AJ21	VSS74	VSS153	AW40
AJ24	VSS75	VSS154	AW48
AJ33	VSS76	VSS155	AV11
AJ34	VSS77	VSS156	AY12
AK12	VSS78	VSS157	AY22
AK3	VSS79	VSS158	AY28

PANTHER-GP-NF
71.PANTH.00U



PCH1I 9 OF 10

AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K32
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L26
B35	VSS169	VSS269	L28
B39	VSS170	VSS270	L36
B7	VSS171	VSS271	L48
F45	VSS172	VSS272	M12
BB12	VSS173	VSS273	P16
BB16	VSS174	VSS274	M18
BB20	VSS175	VSS275	M22
BB22	VSS176	VSS276	M24
BB24	VSS177	VSS277	M30
BB28	VSS178	VSS278	M32
BB30	VSS179	VSS279	M34
BB38	VSS180	VSS280	M38
BB4	VSS181	VSS281	M4
BB46	VSS182	VSS282	M42
BC14	VSS183	VSS283	M46
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	P30
BC26	VSS187	VSS287	P32
BC32	VSS188	VSS288	N47
BC34	VSS189	VSS289	P11
BC36	VSS190	VSS290	P18
BC40	VSS191	VSS291	T33
BC42	VSS192	VSS292	P40
BC48	VSS193	VSS293	P43
BD46	VSS194	VSS294	P47
BE5	VSS195	VSS295	P7
BE22	VSS196	VSS296	R2
BE26	VSS197	VSS297	R48
BE40	VSS198	VSS298	T12
BF10	VSS199	VSS299	T31
BF12	VSS200	VSS300	T37
BF16	VSS201	VSS301	T4
BF20	VSS202	VSS302	W34
BF22	VSS203	VSS303	T46
BF24	VSS204	VSS304	T47
BF26	VSS205	VSS305	T8
BF28	VSS206	VSS306	V11
BF3	VSS207	VSS307	V17
BF38	VSS208	VSS308	V26
BF40	VSS209	VSS309	V27
BF8	VSS210	VSS310	V29
BG17	VSS211	VSS311	V31
BG21	VSS212	VSS312	V36
BG33	VSS213	VSS313	V39
BG44	VSS214	VSS314	V43
BG8	VSS215	VSS315	V7
BH11	VSS216	VSS316	W17
BH15	VSS217	VSS317	W19
BH17	VSS218	VSS318	W2
BH19	VSS219	VSS319	W27
H10	VSS220	VSS320	W48
BH27	VSS221	VSS321	Y12
BH31	VSS222	VSS322	Y38
BH33	VSS223	VSS323	Y4
BH35	VSS224	VSS324	Y42
BH39	VSS225	VSS325	Y46
BH43	VSS226	VSS326	Y8
D3	VSS227	VSS327	BG29
D12	VSS228	VSS328	N24
D16	VSS229	VSS329	A13
D18	VSS230	VSS330	AD47
D22	VSS231	VSS331	B43
D24	VSS232	VSS332	BE10
D26	VSS233	VSS333	BG41
D30	VSS234	VSS334	G14
D32	VSS235	VSS335	H16
D34	VSS236	VSS336	T36
D38	VSS237	VSS337	BG22
D42	VSS238	VSS338	BG24
D48	VSS239	VSS339	C22
D8	VSS240	VSS340	AP13
E18	VSS241	VSS341	M14
E26	VSS242	VSS342	AF3
G18	VSS243	VSS343	AP1
G20	VSS244	VSS344	BE16
G26	VSS245	VSS345	BC16
G28	VSS246	VSS346	BG28
G36	VSS247	VSS347	VSS351
G48	VSS248	VSS348	VSS352
H12	VSS249	VSS349	BJ28
H18	VSS250		
H22	VSS251		
H24	VSS252		
H26	VSS253		
H30	VSS254		
H32	VSS255		
H34	VSS256		
F3	VSS257		
F3	VSS258		

PANTHER-GP-NF
71.PANTH.00U



M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size A3 Document Number: **OAK14 Chief River DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 25 of 105

Copyright © 2012 Dell Inc. All rights reserved. Dell, the Dell logo, and Wistron are trademarks of Dell Inc. in the United States and other countries. OAK14 is a trademark of Dell Inc. in the United States and other countries. PCH is a trademark of Dell Inc. in the United States and other countries. VSS is a trademark of Dell Inc. in the United States and other countries.

www.rosefix.com

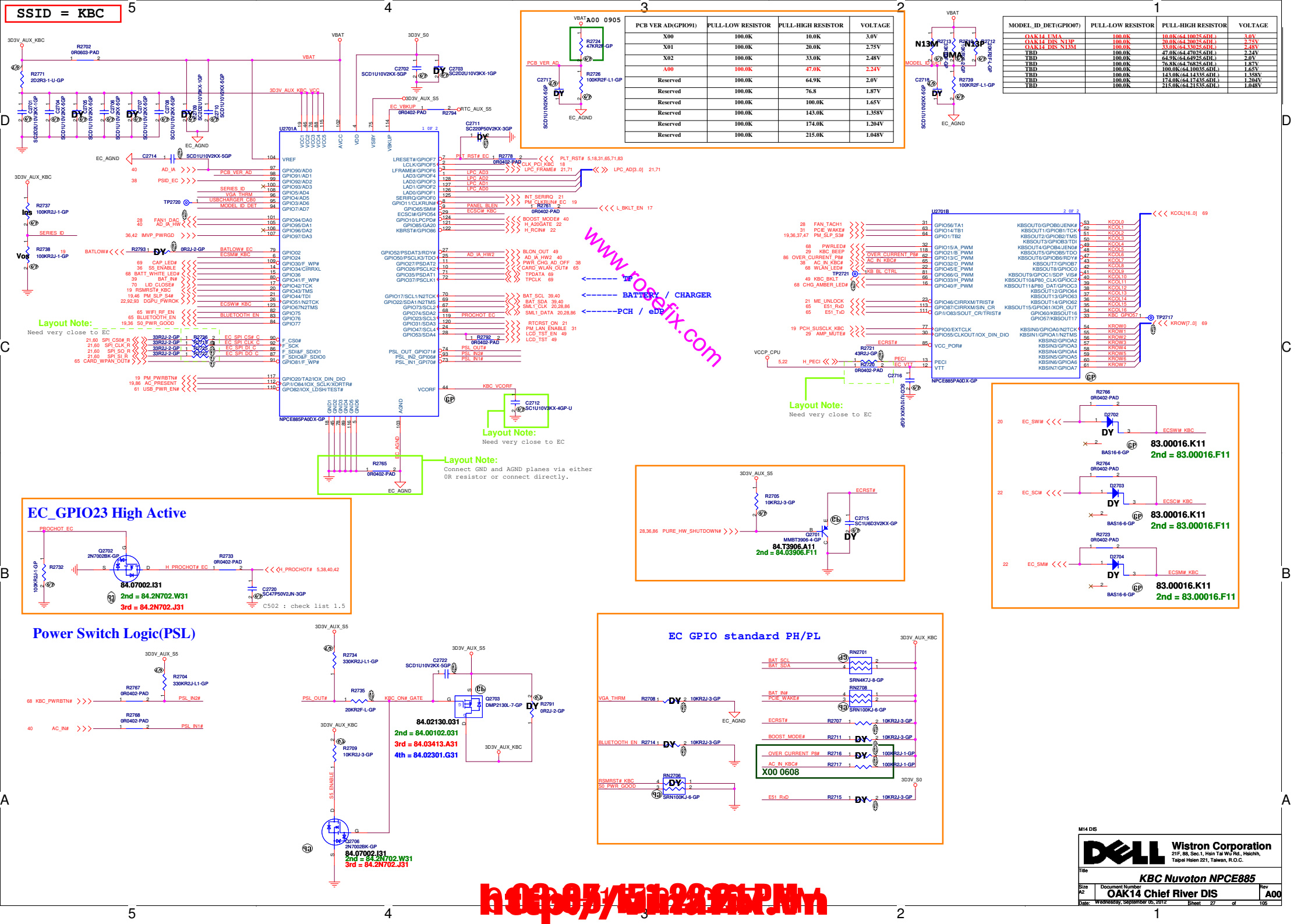
(Blanking)

M14 DIS



Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date:	Wednesday, September 05, 2012	Sheet 26 of 105

h0005/15128067.Mn



PCB VER AD(GPIO#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	100.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO#07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
0AK14_LINA	100.0K	100.0K(64.10035.GDI)	3.0V
0AK14_DIS_N13M	100.0K	20.0K(64.20035.GDI)	2.75V
0AK14_DIS_N13M	100.0K	33.0K(64.33035.GDI)	2.48V
TBD	100.0K	47.0K(64.47035.GDI)	2.24V
TBD	100.0K	64.9K(64.64925.GDI)	2.0V
TBD	100.0K	76.8K(64.76825.GDI)	1.87V
TBD	100.0K	100.0K(64.10035.GDI)	1.65V
TBD	100.0K	143.0K(64.14335.GDI)	1.358V
TBD	100.0K	174.0K(64.17435.GDI)	1.204V
TBD	100.0K	215.0K(64.21535.GDI)	1.048V

www.forefix.com

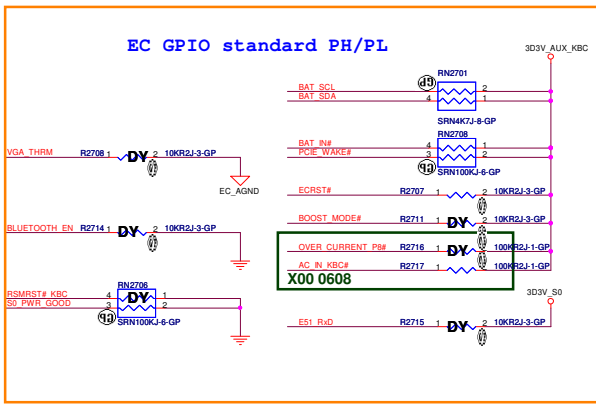
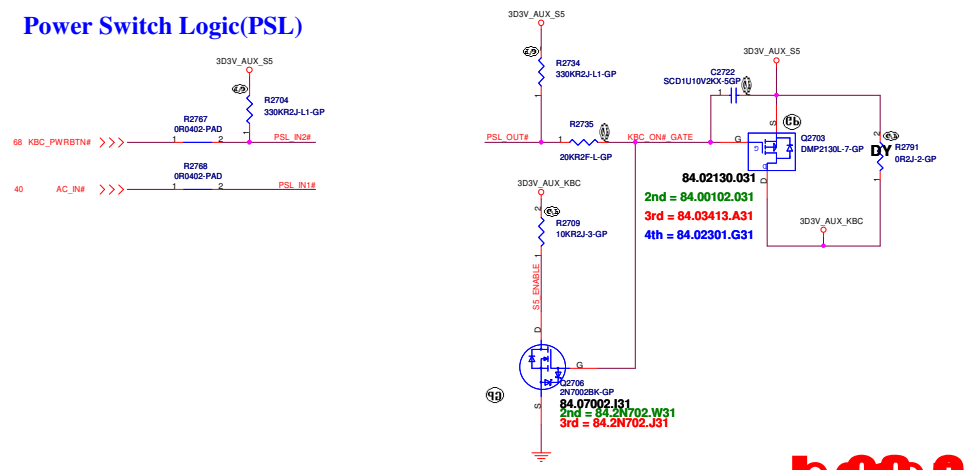
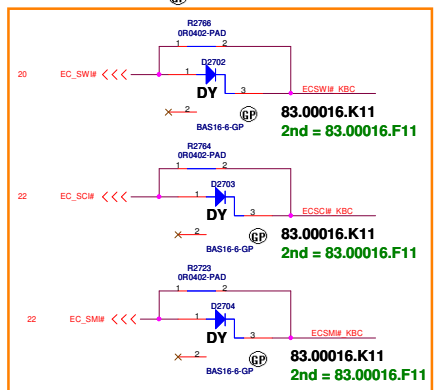
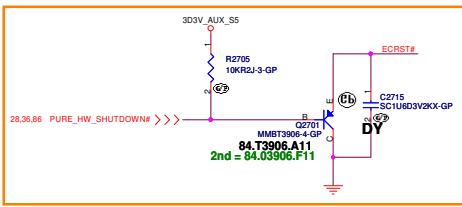
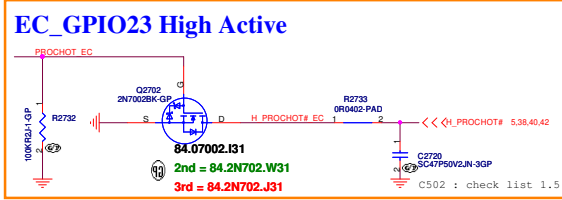
←←←←← BATTERY / CHARGER

←←←←← PCH / eDP

Layout Note:
Need very close to EC

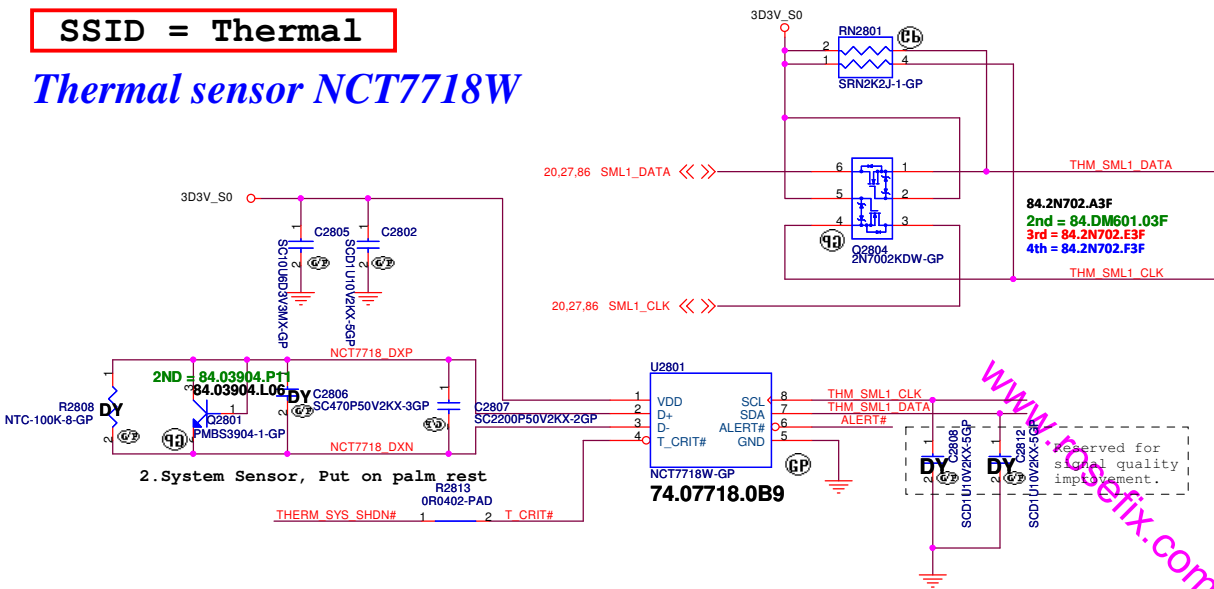
Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes with either OR resistor or connect directly.



SSID = Thermal

Thermal sensor NCT7718W

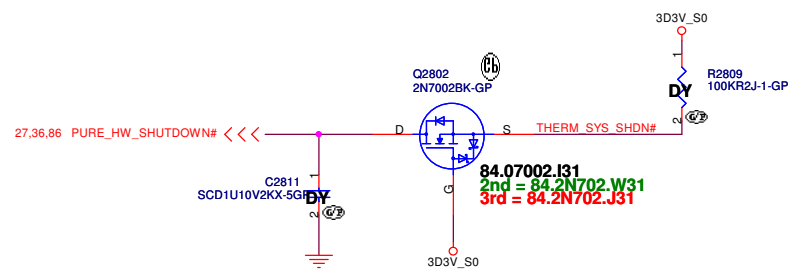


ALERT# /T CRIT# Pull-up Resistor

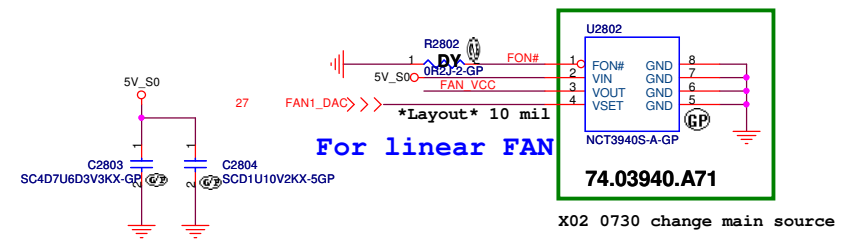
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	82°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing, and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W



Fan controller NCT3940S-A



Layout 10 mil

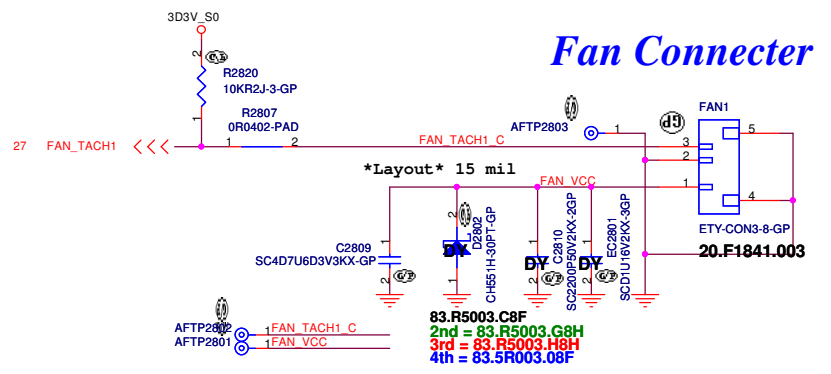
For linear FAN

74.03940.A71

X02 0730 change main source

h0p05y1512806PM

Fan Connector



Layout 15 mil

83.R5003.C8F
2nd = 83.R5003.G8H
3rd = 83.R5003.H8H
4th = 83.R5003.O8F

M14 DIS

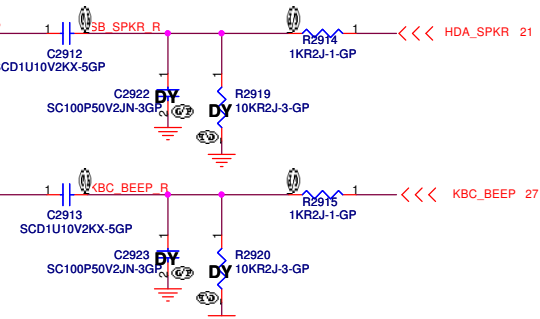
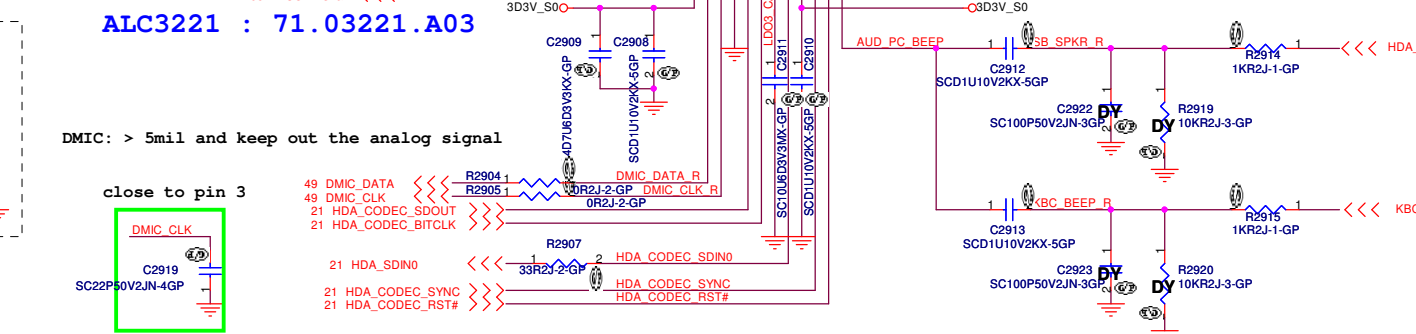
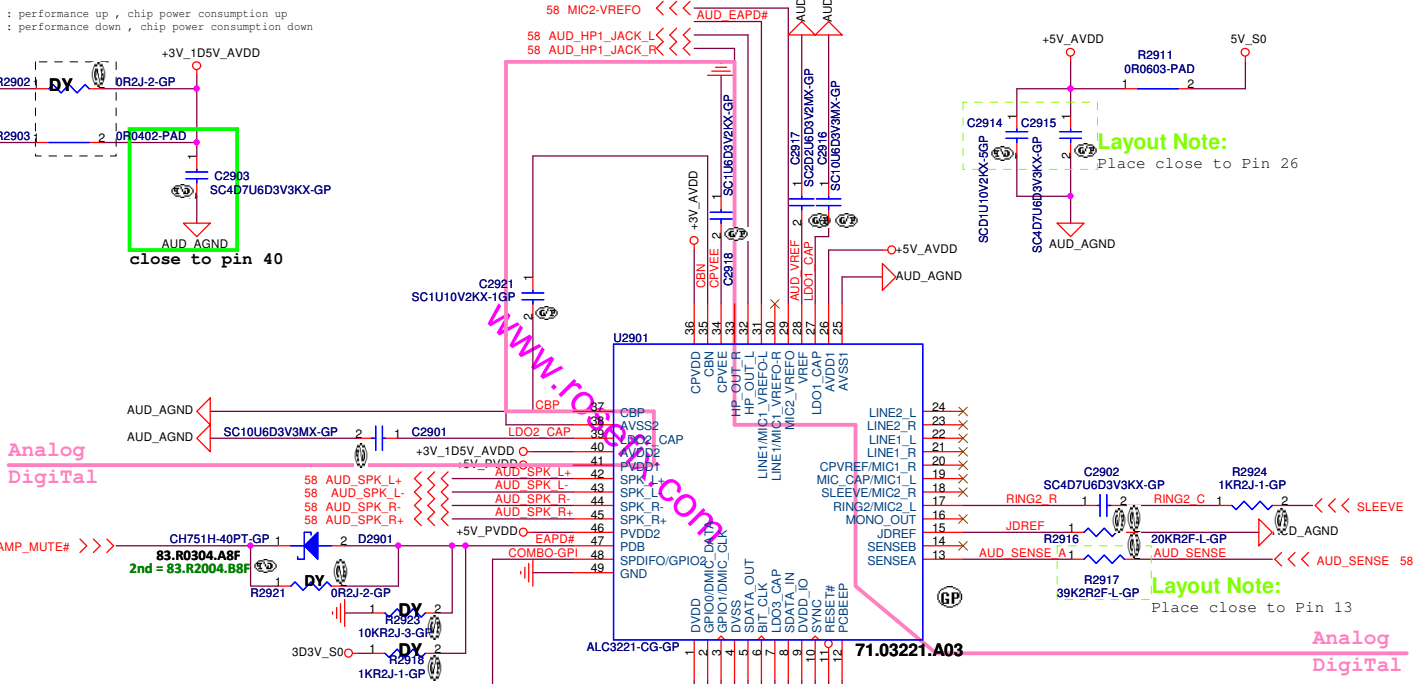
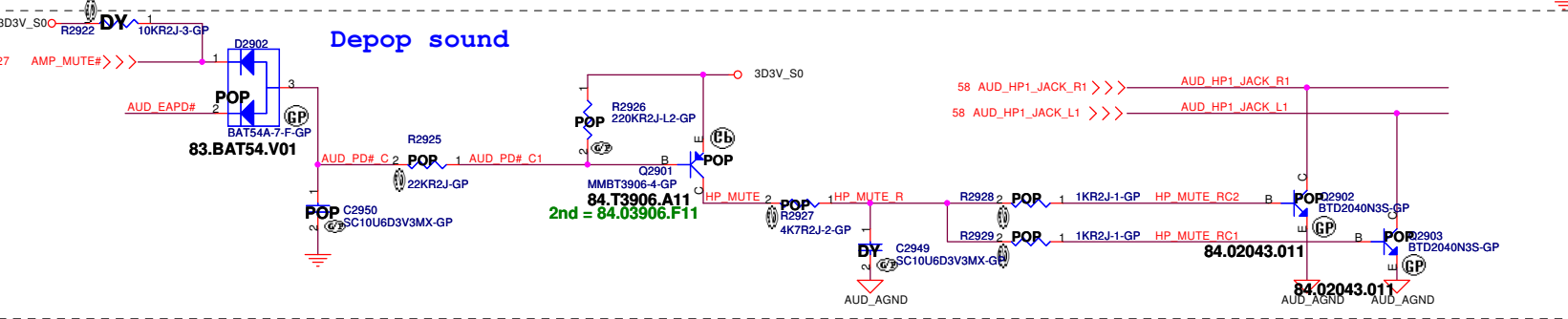
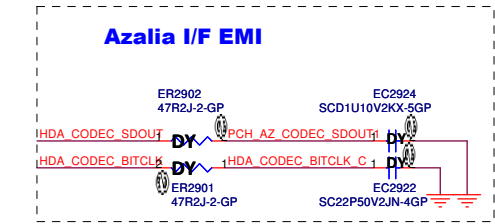
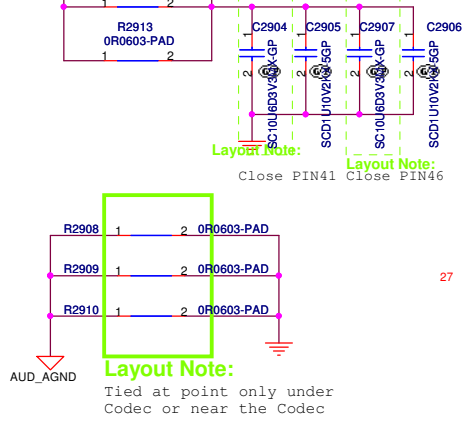
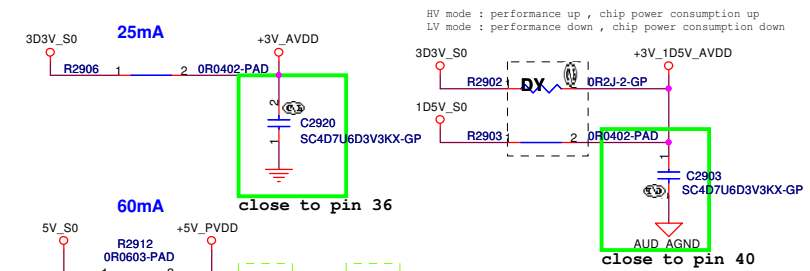
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal NCT7718W/Fan Controller P2793**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 28 of 105

SSID = AUDIO



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3221**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 29	of 105

www.foc.com

(Blanking)

www.usefix.com

M14 DIS

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number

OAK14 Chief River DIS

Rev

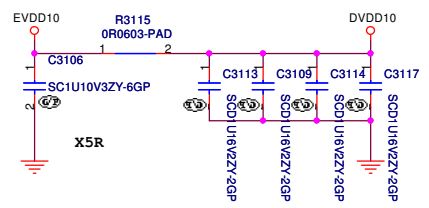
A00

Date: Wednesday, September 05, 2012

Sheet 30 of 105

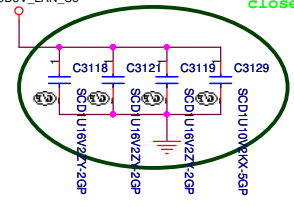
h0005/151280617.Mh

LAN CHIP

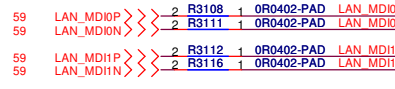


1ms < +3D3V_LAN_S5 Rising time (10%~90%) <100ms

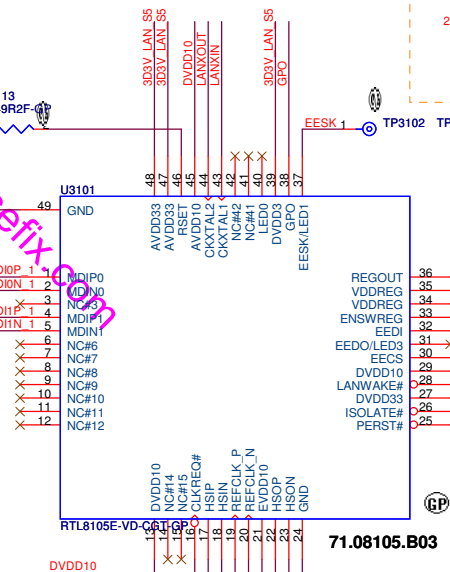
40 mils



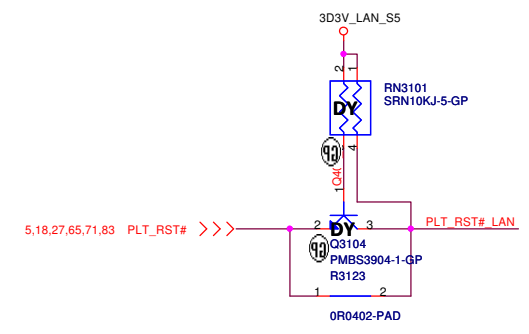
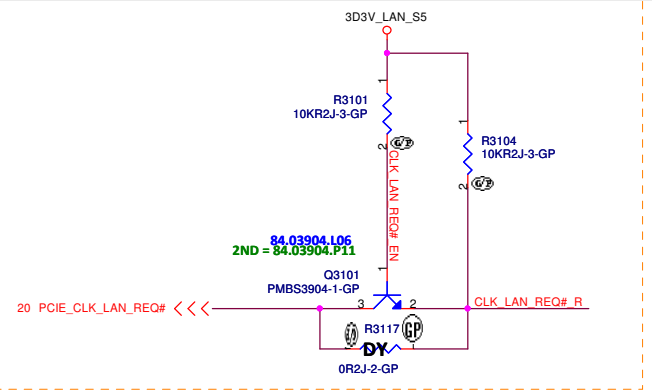
close to pin 27 39 47 48



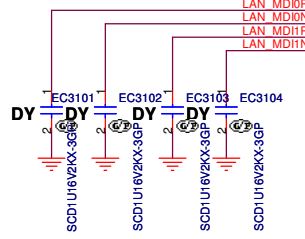
www.rosefix.com



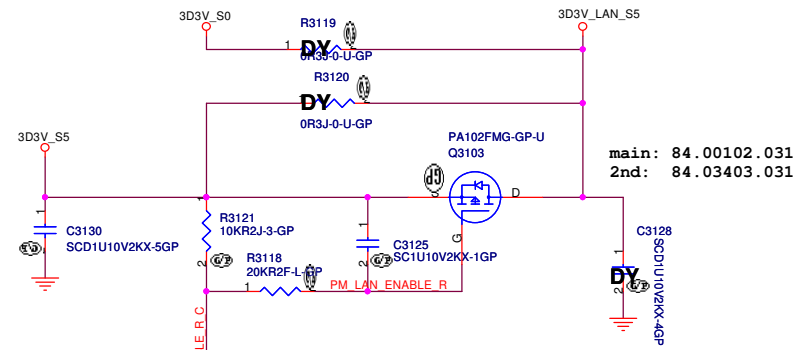
71.08105.B03



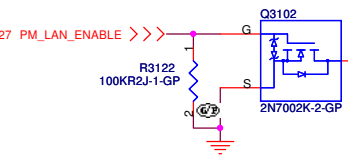
5,18,27,65,71,83 PLT_RST# >>>



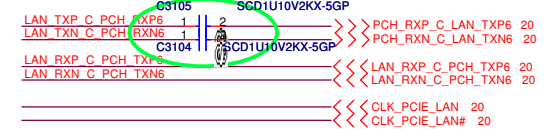
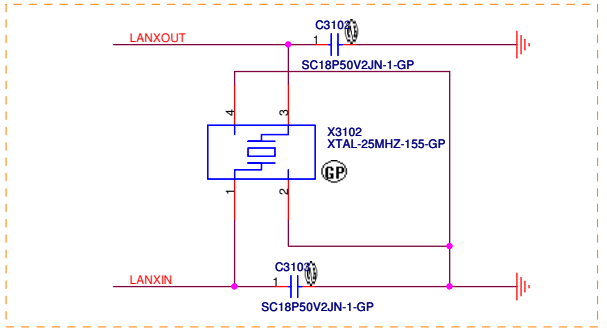
251mA



main: 84.00102.031
2nd: 84.03403.031



27 PM_LAN_ENABLE >>>



LAN TXP C PCH TXP6 >>> PCH_RXP_C_LAN_TXP6 20
LAN TXN C PCH RXN6 >>> PCH_RXN_C_LAN_TXN6 20
LAN RXP C PCH TXP6 >>> LAN_RXP_C_PCH_TXP6 20
LAN RXN C PCH TXN6 >>> LAN_RXN_C_PCH_TXN6 20
CLK_PCIE_LAN 20
CLK_PCIE_LAN# 20

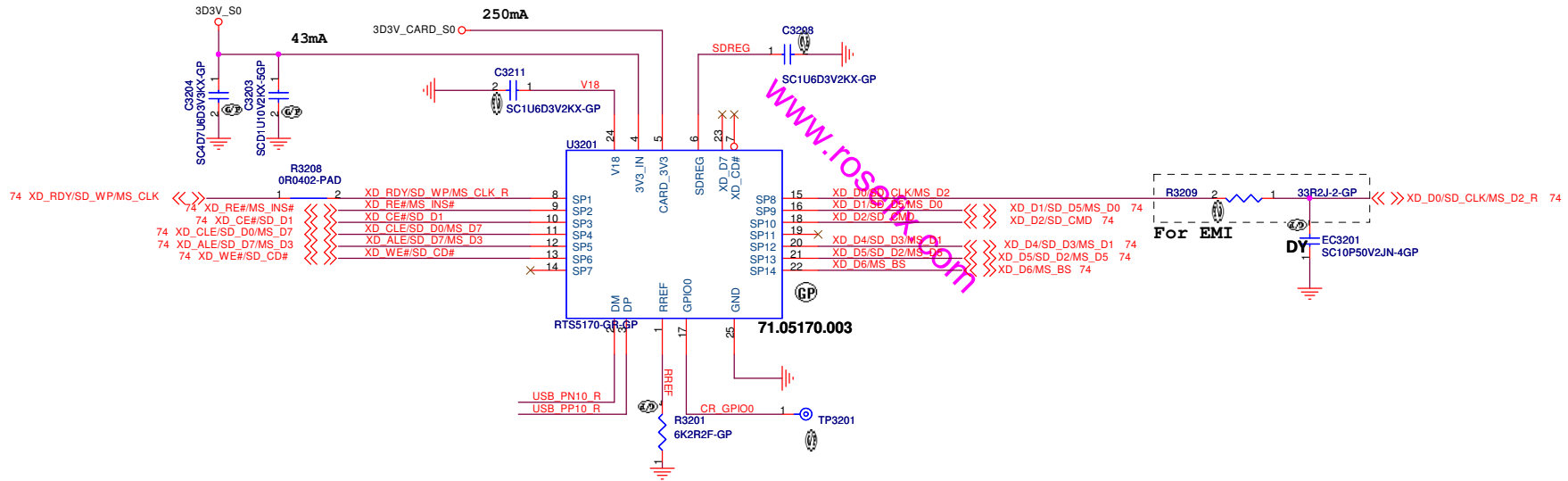
M14 DIS



Title LOM		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012 Sheet 31 of 105		

80085151286PM

SSID = SDIO



Close U3201



M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card Reader-RTS5170			
Size A3	Document Number OAK14 Chief River DIS		Rev A00
Date: Wednesday, September 05, 2012		Sheet 32	of 105

h0905/15128061M

www.rosefix.com

(Blanking)

h0005/15128067.Mn

M14 DIS

	Wistron Corporation	
	21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

Title **Reserved**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
------------	---	-------------------

Date: Wednesday, September 05, 2012 Sheet 33 of 105

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 34 of 105

h0605/15128067.Mn

www.rosefix.com

(Blanking)

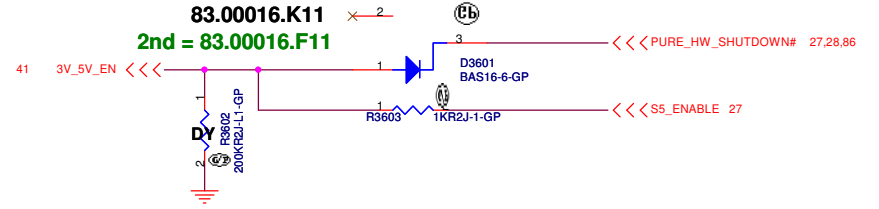
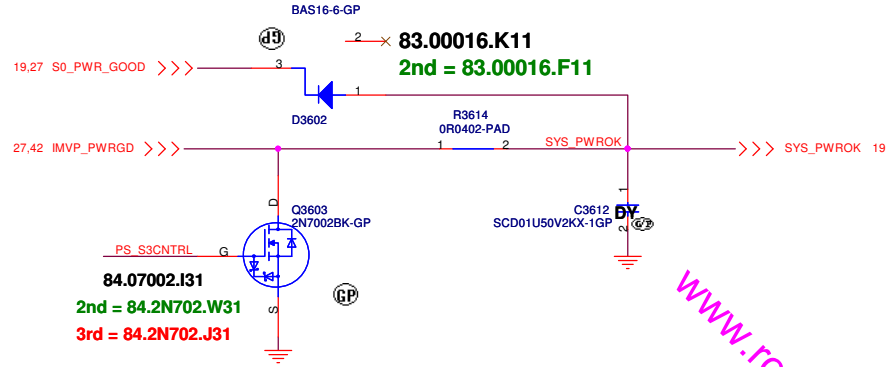
M14 DIS

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

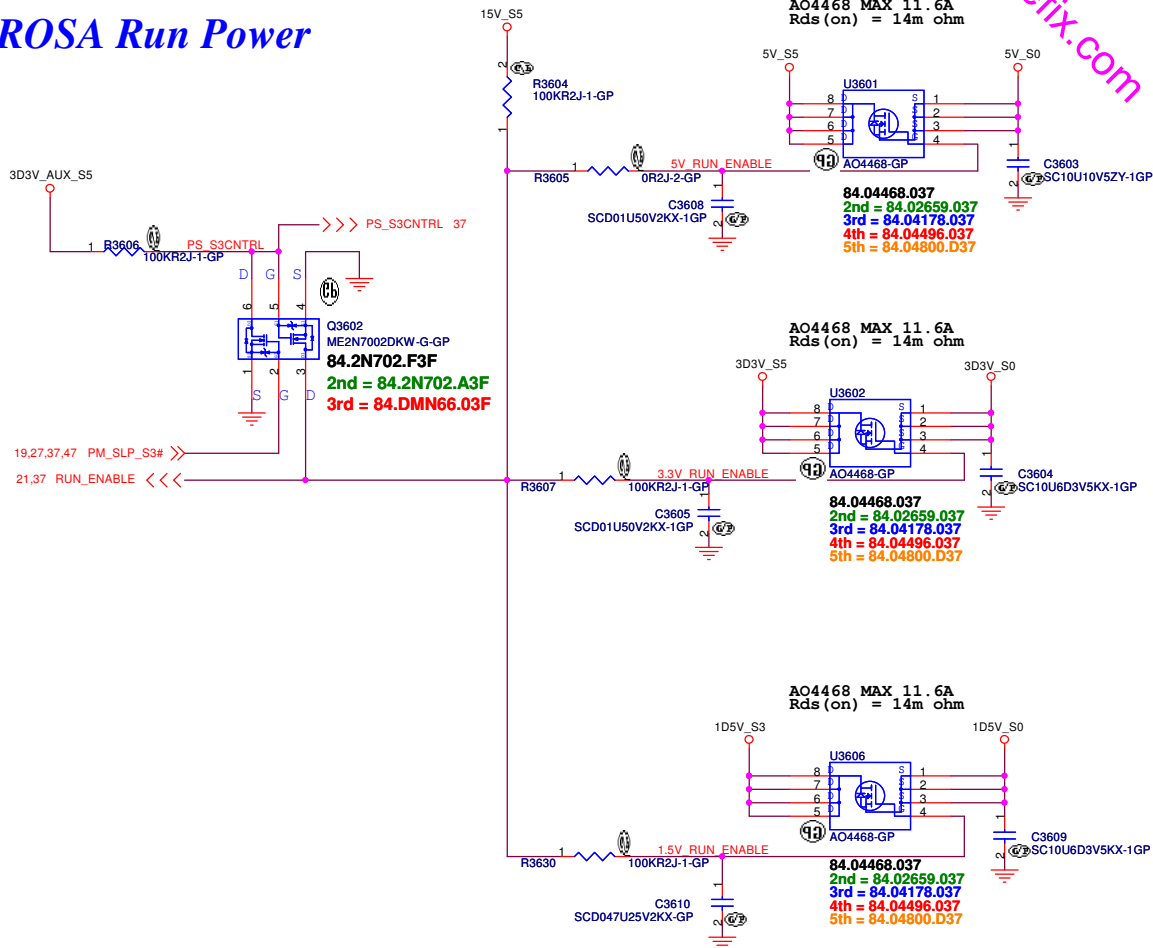
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 35 of 105

h0005/151280617.Mn

SSID = Reset.Suspend



ROSA Run Power



5V_S0

+5V_RUN Consumption
Peak current ?A
Design current ?A

3D3V_S0

+3.3V_RUN Consumption
Peak current ?A
Design current ?A

1D5V_S0

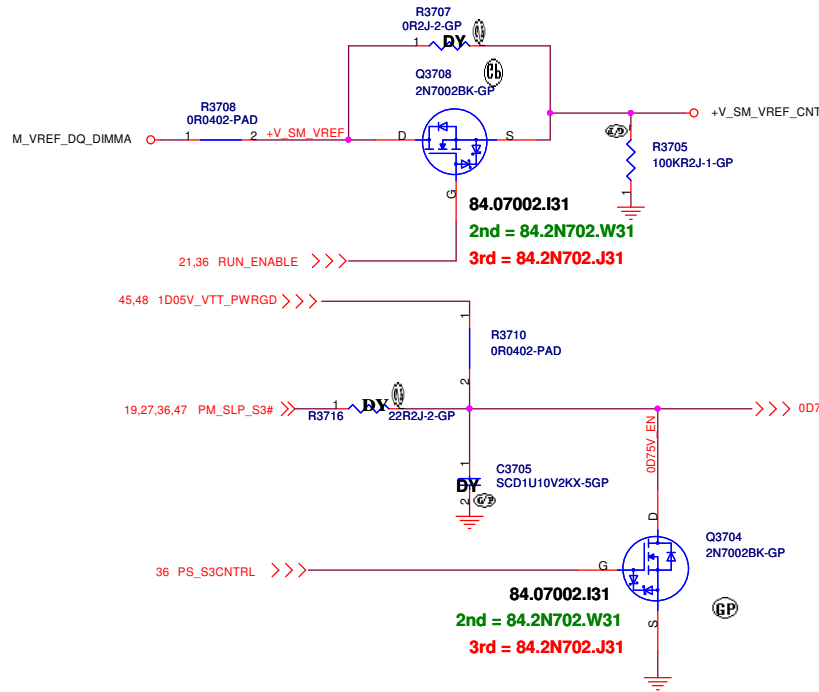
+1.5V_RUN Consumption
Peak current ?A
Design current ?A

M14 DIS

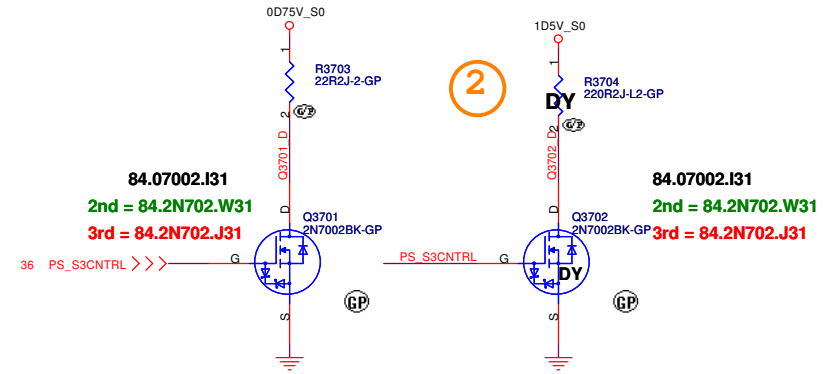
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power Plane Enable			
Size A3	Document Number	Rev	
OAK14 Chief River DIS		A00	
Date: Wednesday, September 05, 2012	Sheet 36	of 105	

h 0 3 3 y 1 5 1 2 8 2 6 P M h

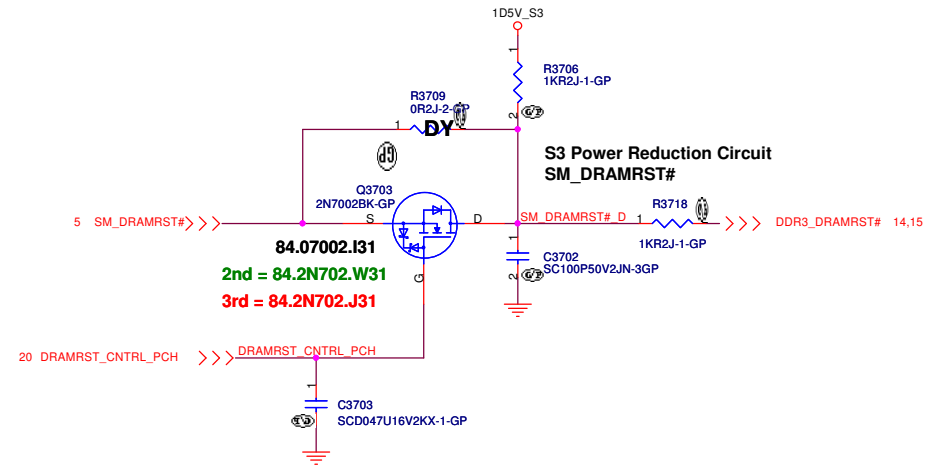
**Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation**



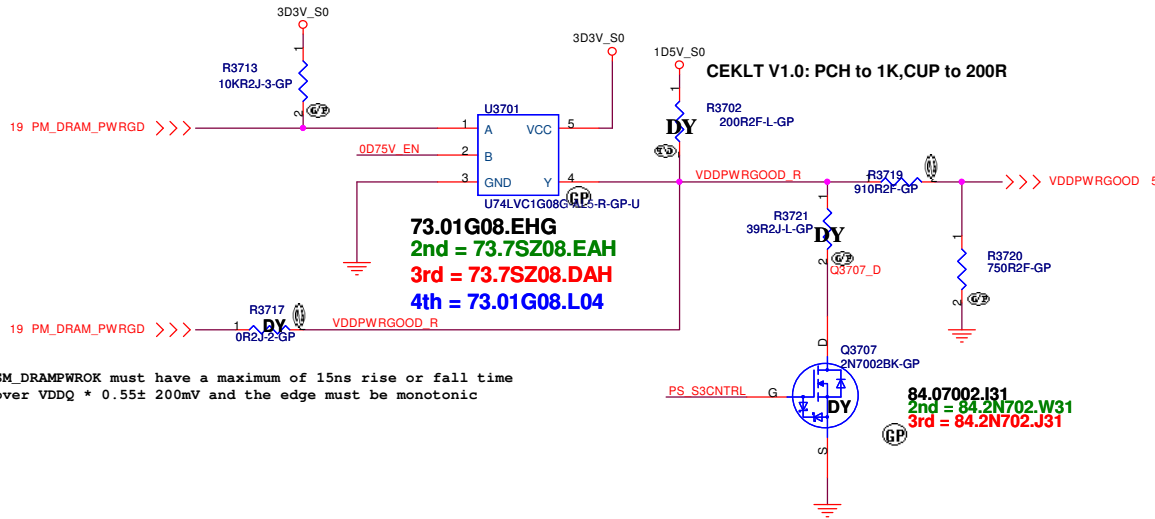
**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

www.rosefix.com

M14 DIS

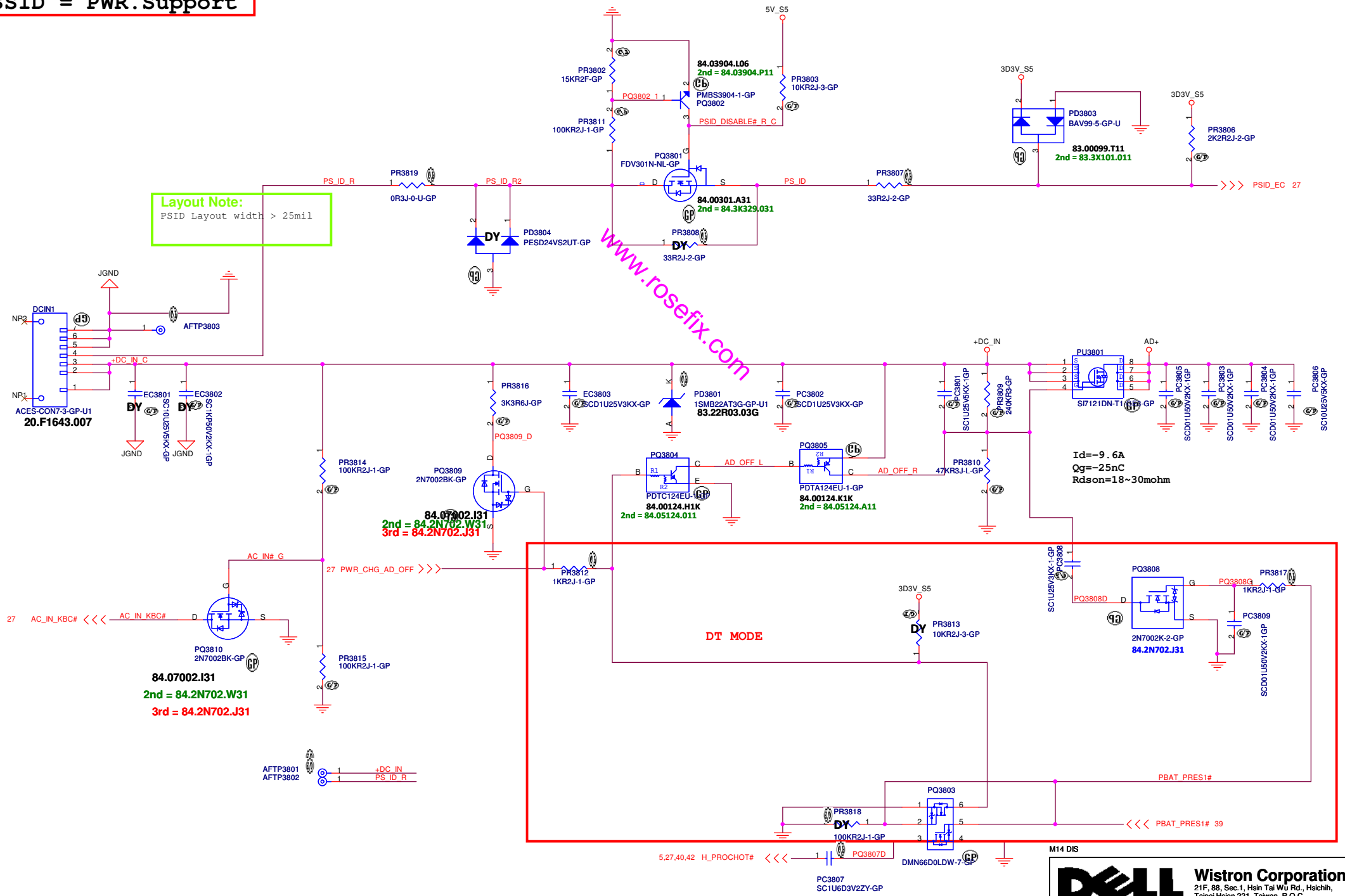


Title S3 Reduction Circuit		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 37	of 105

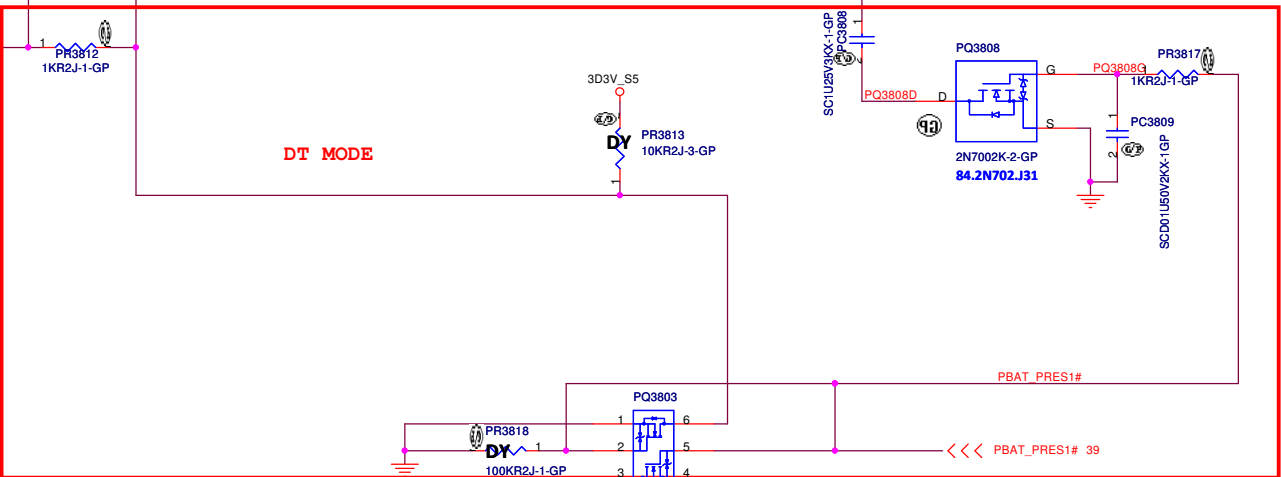
h0p05y1512806PM

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil



www.rosefix.com



M14 DIS

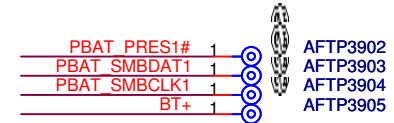
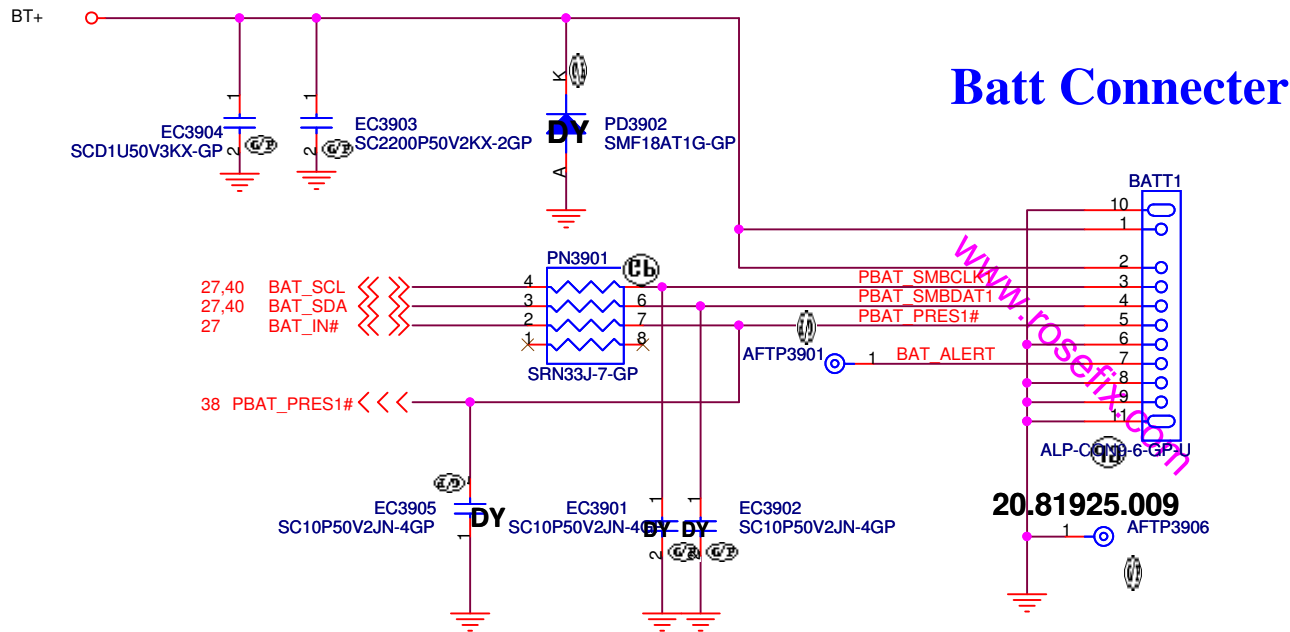
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN**

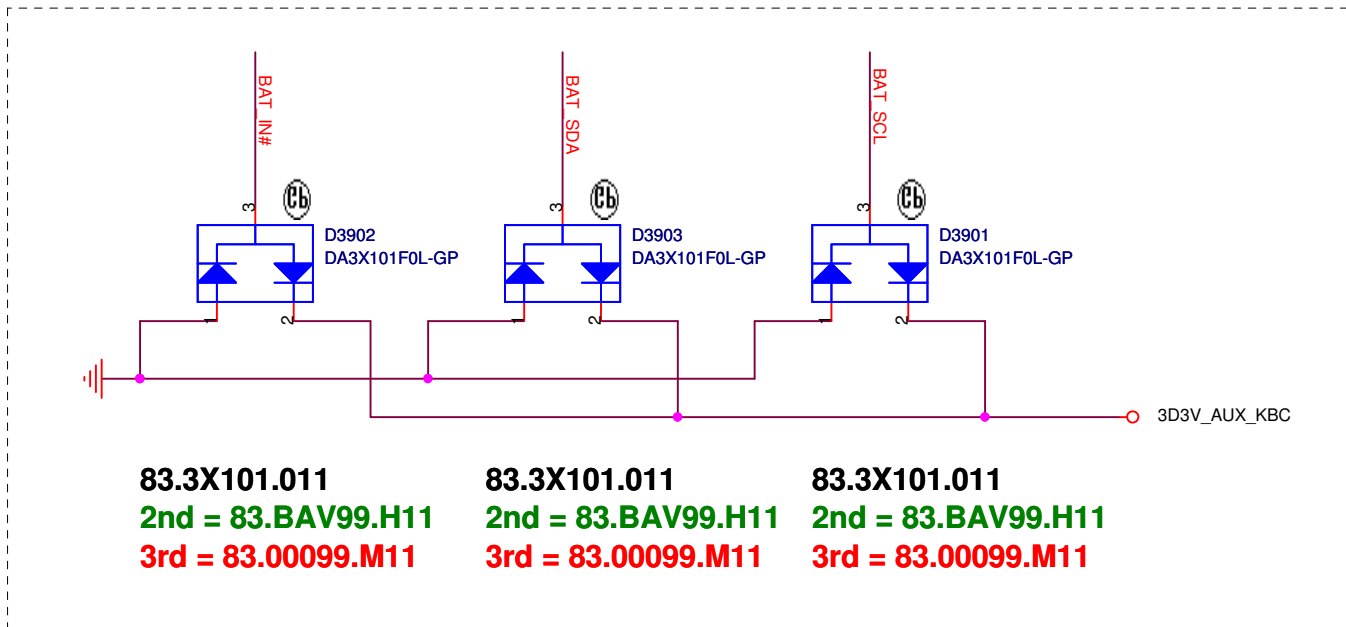
Size A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet 38	of 105

h0p05y5t286kPm

SSID = PWR. Support



Placement: Close to Batt Connector

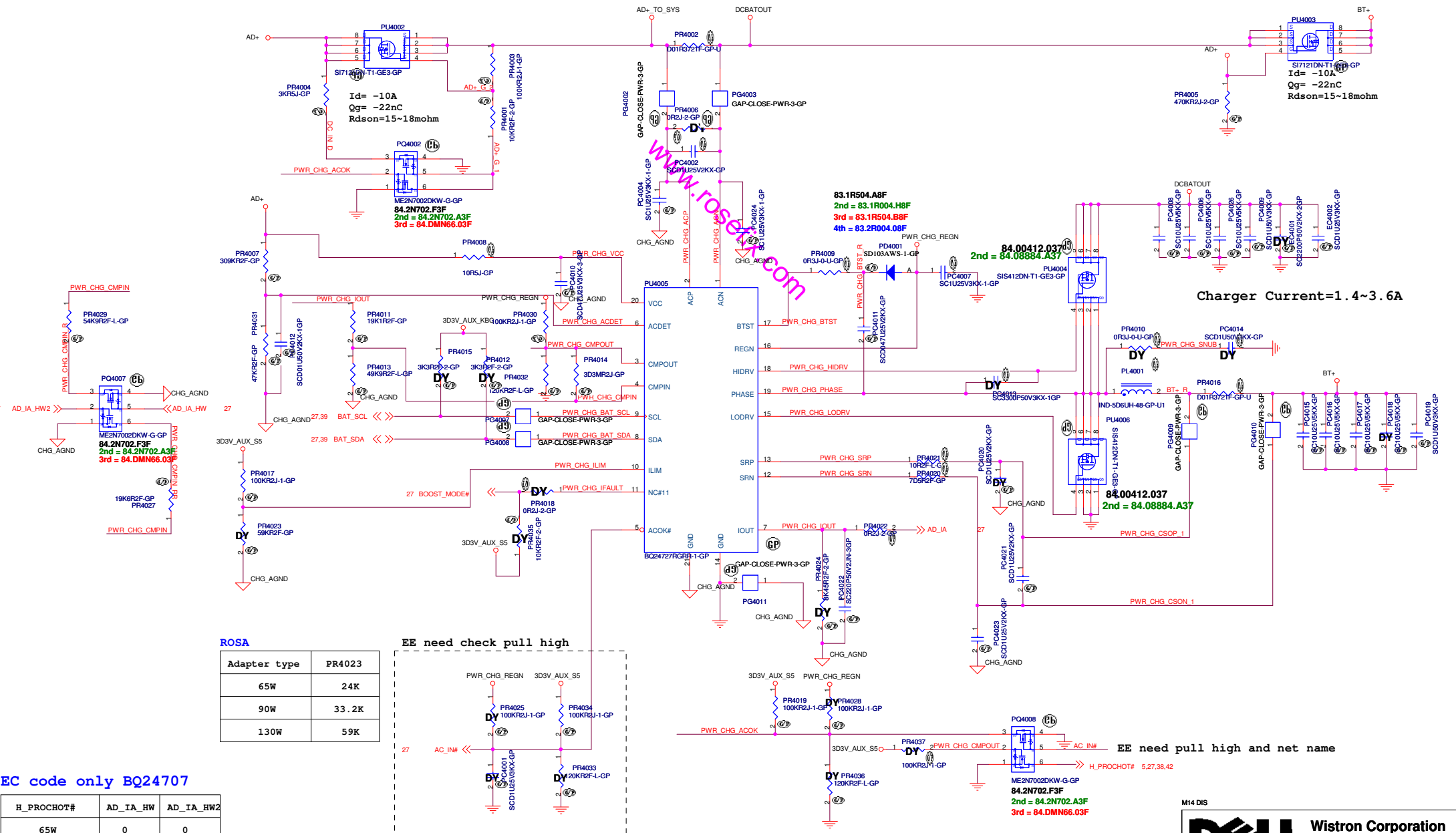


80305/15128/05P.Mm

M14 DIS

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: BATT CONN			
Size: A4	Document Number: OAK14 Chief River DIS	Rev: A00	
Date: Wednesday, September 05, 2012	Sheet: 39	of	105

SSID = Charger

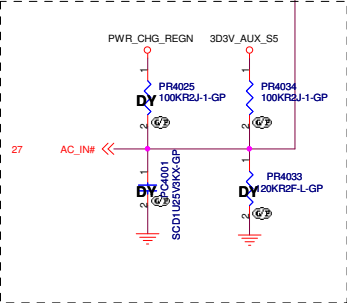


Charger Current=1.4~3.6A

ROSA

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

EE need check pull high



EC code only BQ24707

H_PROCHOT#	AD_IA_HW2	AD_IA_HW1
65W	0	0
90W	1	0
130W	0	1

M14 DIS

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wd Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

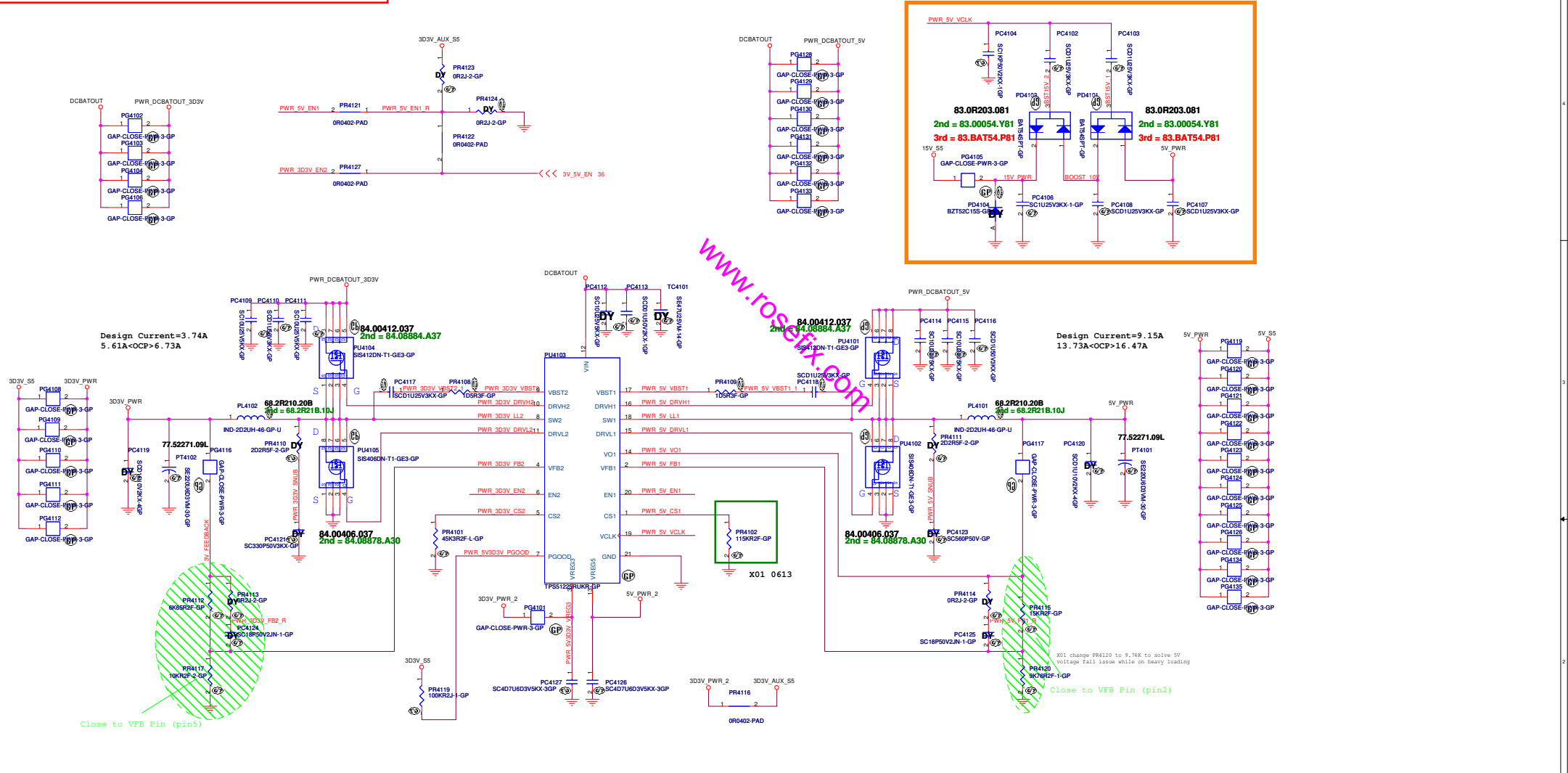
File: **CHARGER BQ24727**

Size: Document Number: **DNE40 14 CR DIS** Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 40 of 105

h0p05/512866Pm

SSID = PWR.Plane.Regulator_5v3p3v



www.rosechip.com

Design Current=3.74A
5.61A<OCP>6.73A

Design Current=9.15A
13.73A<OCP>16.47A

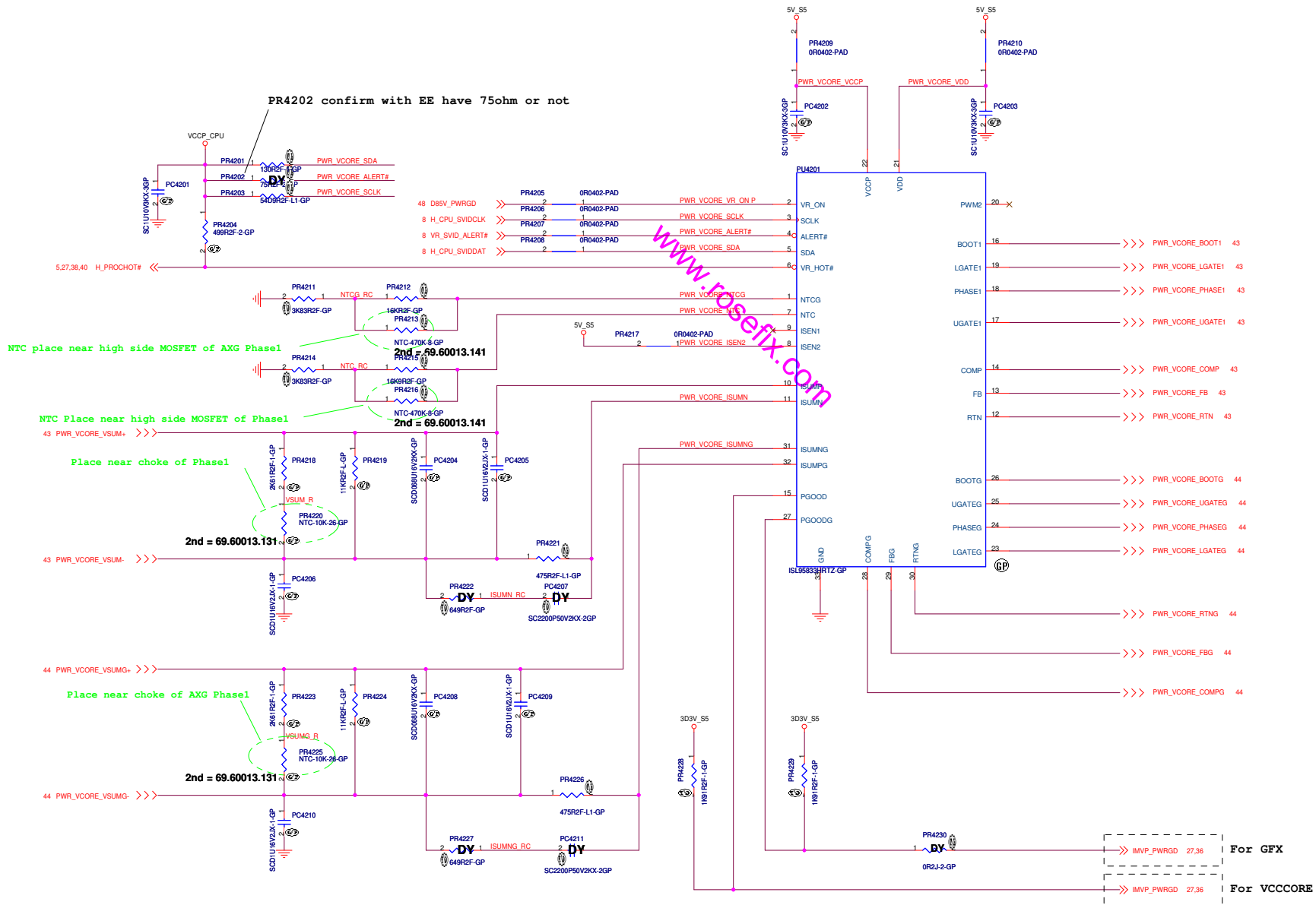
Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mohm / 77.52271.09L
R/S: S1S412DN-T1-GE3 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: S1S406DN-T1-GE3 / 11.5mohm/14.5mohm@4.5Vgs / 84.00406.037

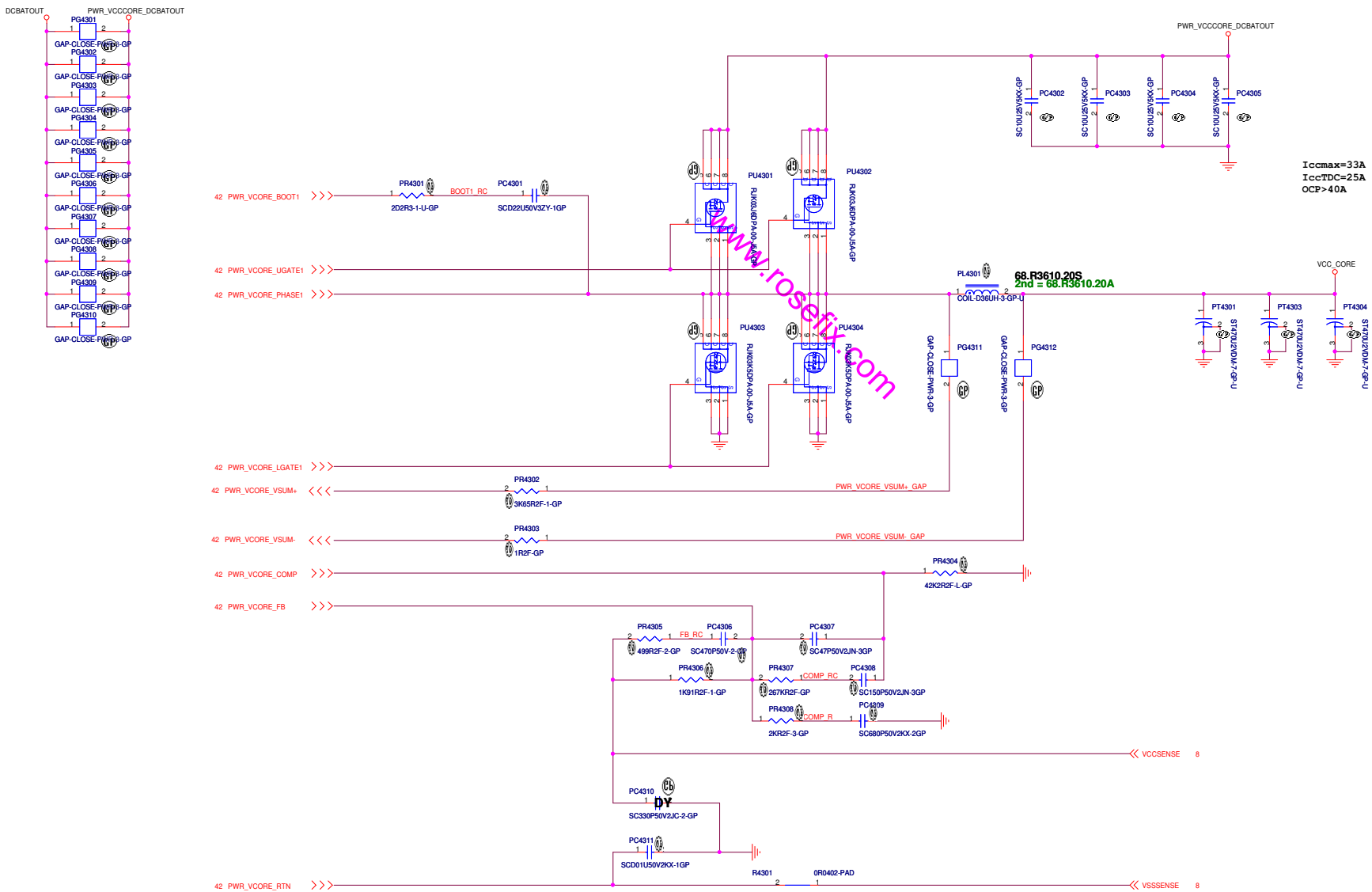
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mohm / 77.52271.09L
R/S: S1S412DN-T1-GE3 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: S1S406DN-T1-GE3 / 11.5mohm/14.5mohm@4.5Vgs / 84.00406.037





www.esefix.com

h0p0y0h0z0h0p0h0



Iccmax=33A
IccTDC=25A
OCP>40A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
 O/P cap: CHIP CAP EL 470U 2V 7.3*4.3 ESR=0.0045 3.8Arms Panasonic/79.47719.9BL
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K5DPA-00#J5A / 3mohm/3.9mOhm@4.5Vgs/ 84.00035.037

M14 DIS

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

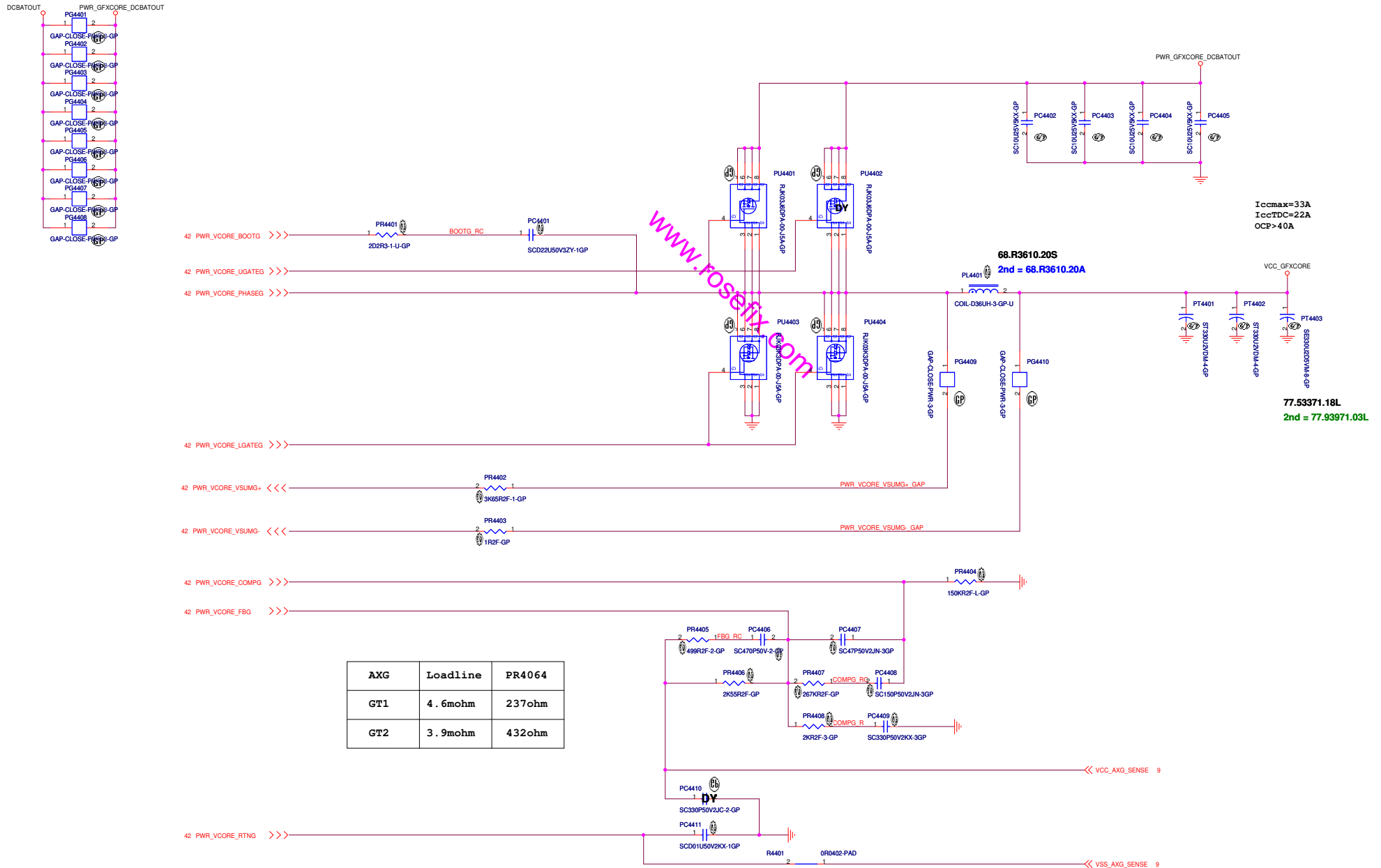
Title: **ISL95833 CPU CORE(2/3)**

Size: C Document Number: OAK14 Chief River DIS Rev: A00

Date: Wednesday, September 05, 2012 Sheet: 43 of 105

h0p0y0h0z0h0p0h0

SSID = CPU.Regulator



Iccmax=33A
IccTDC=22A
OCP>40A

77.53371.18L
2nd = 77.93971.03L

AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
 O/P cap: CHIP CAP 330U 2V EEP5X0D331XE 3.5Arms Panasonic/79.33719.20L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.00333.037

100p03/10022000P.Mh

M14 DIS

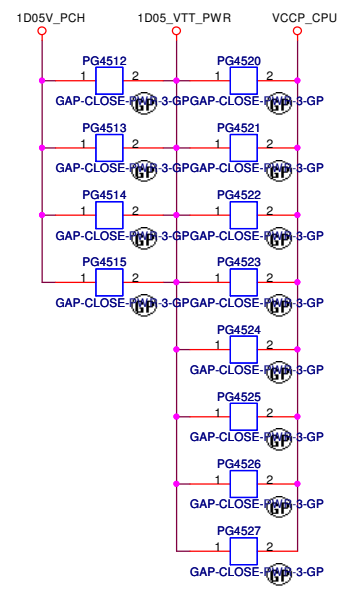
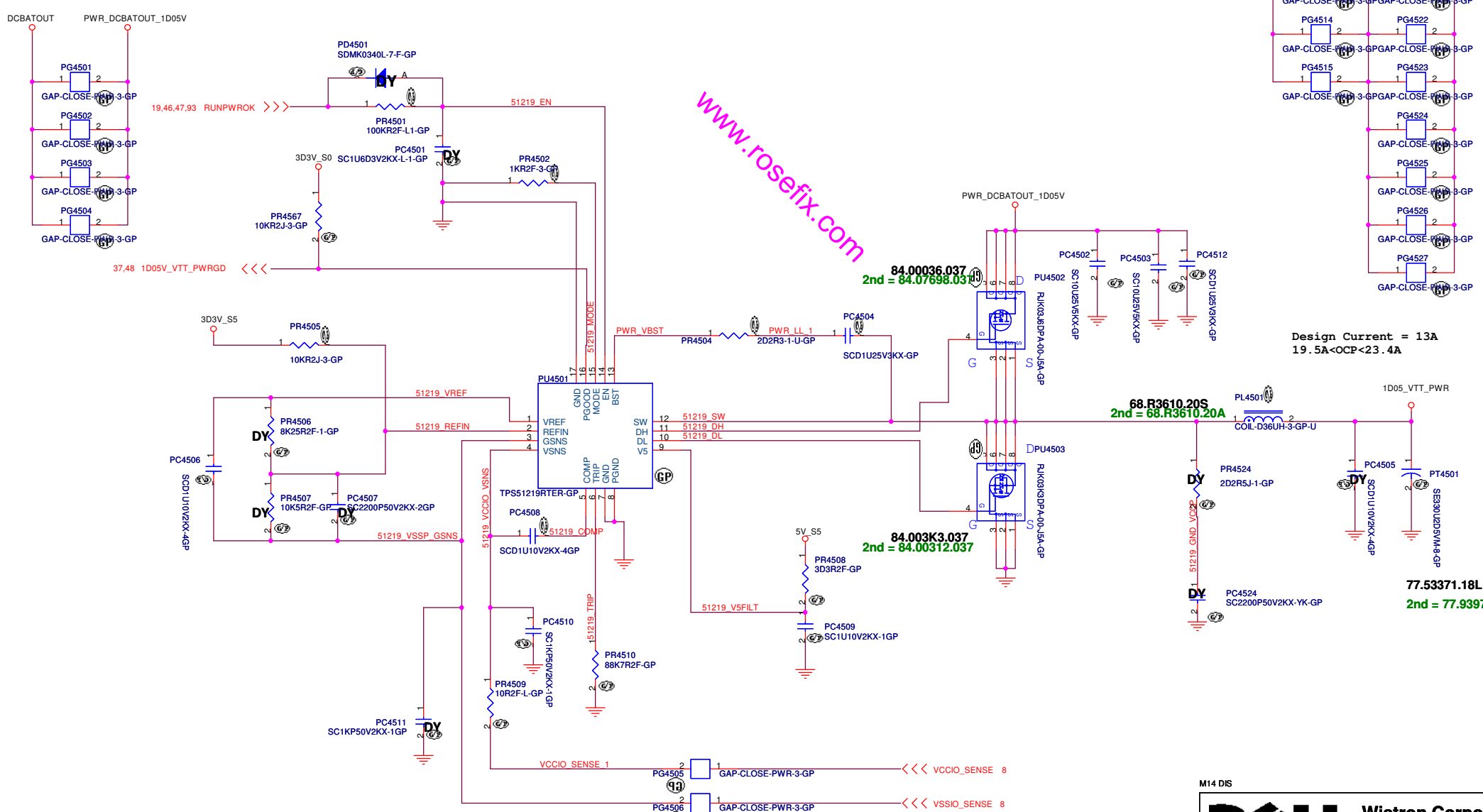
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **ISL95833 CPU CORE(3/3)**

Size: C Document Number OAK14 Chief River DIS Rev: A00

Date: Wednesday, September 05, 2012 Sheet: 44 of 105

TPS51219 for 1D05V_VTT



Design Current = 13A
19.5A < OCP < 23.4A

84.00036.037
2nd = 84.07698.037

84.003K3.037
2nd = 84.00312.037

68.R3610.20S
2nd = 68.R3610.20A

77.53371.18L
2nd = 77.93971.03L

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

h0p05y5t286kPm

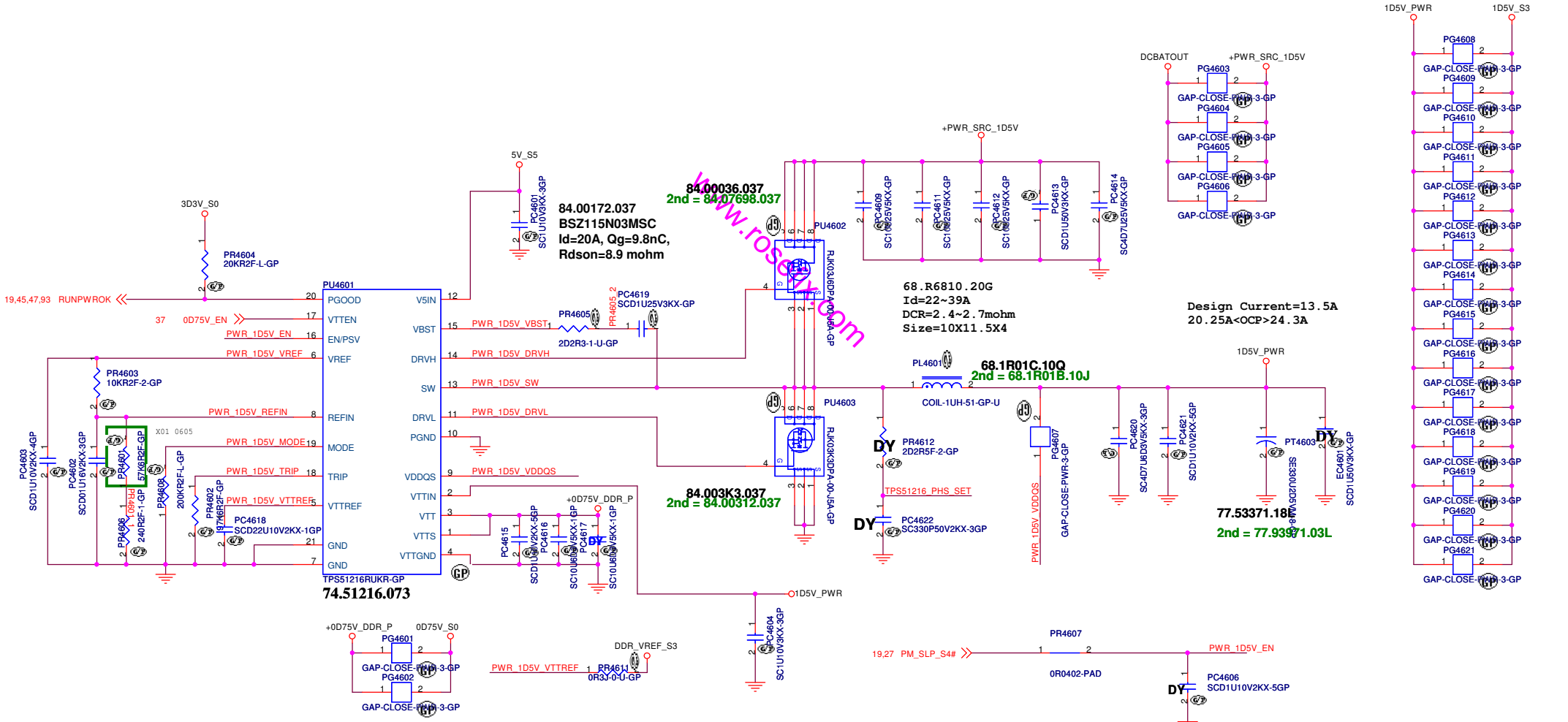
M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51219 1D05V_VTT**

Size A3	Document Number DNE40 14 CR DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 45	of 105

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

h0p0y1512286P.M

M14 DIS

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

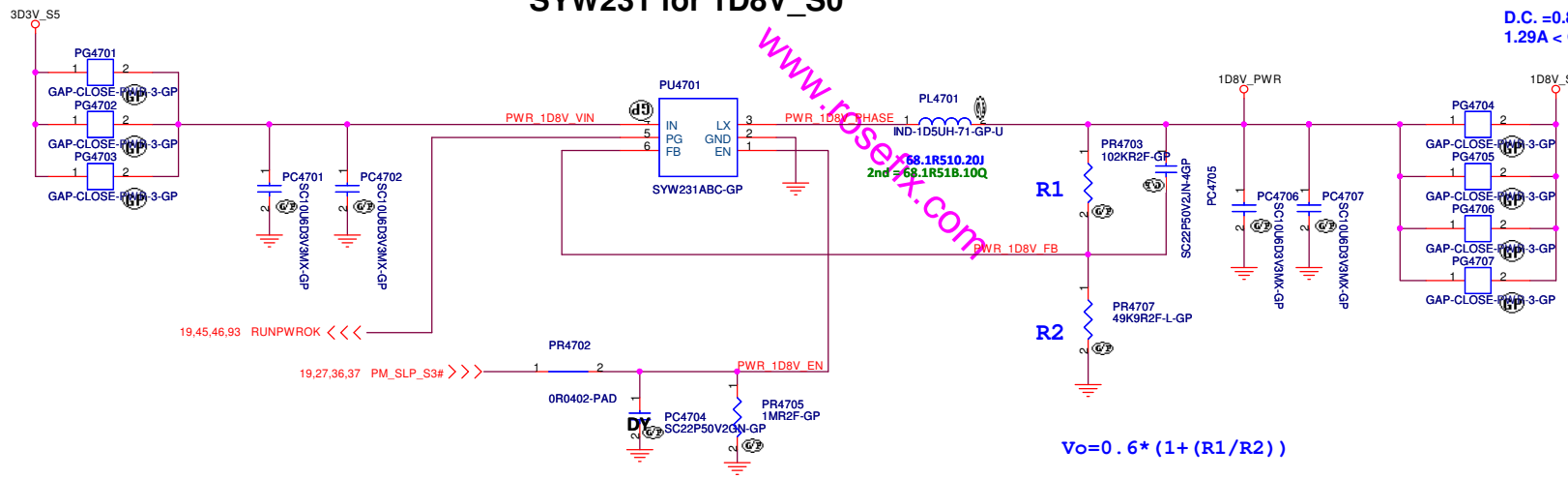
Title: **TPS51216 +1.5V SUS**

Size A3	Document Number	Rev
Date: Wednesday, September 05, 2012	OAK14 Chief River DIS	A00

Sheet 46 of 105

SYW231 for 1D8V_S0

D.C. = 0.87A
1.29A < OCP < 1.52A

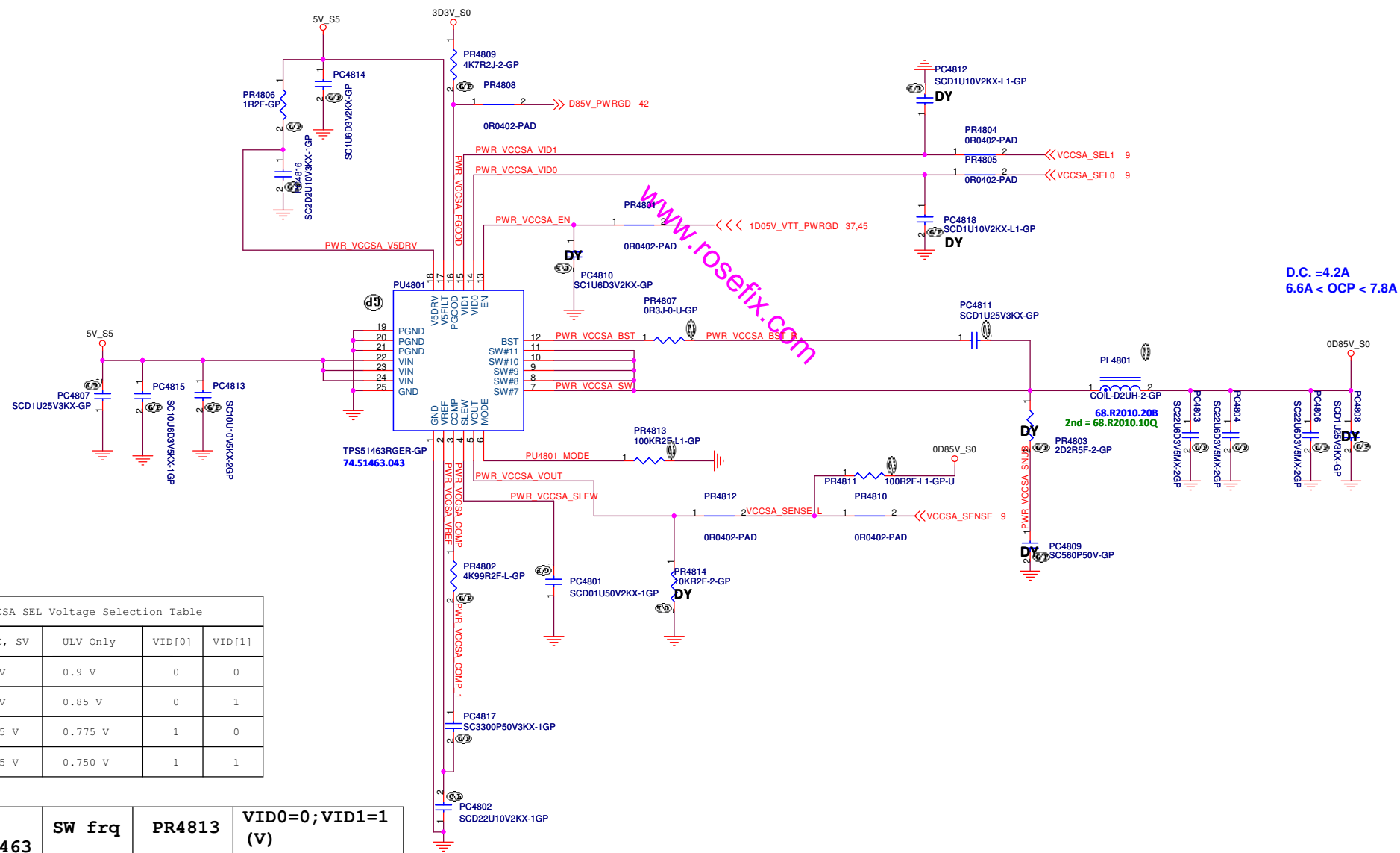


www.fosex.com

h0p05/y5h2806P.Mh

M14 DIS

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SYW231 1D8V S0			
Size	Document Number	Rev	
A3	OAK14 Chief River DIS	A00	
Date: Wednesday, September 05, 2012	Sheet 47	of	105



D.C. =4.2A
6.6A < OCP < 7.8A

XE, QC, SV	ULV Only	VID[0]	VID[1]
0.9 V	0.9 V	0	0
0.8 V	0.85 V	0	1
0.725 V	0.775 V	1	0
0.675 V	0.750 V	1	1

TPS51463 for ULV	SW frq	PR4813	VID0=0; VID1=1 (V)
	700KHz	100K	0.85
	1MHz	Open	0.85

h0p05/y5t286kPm

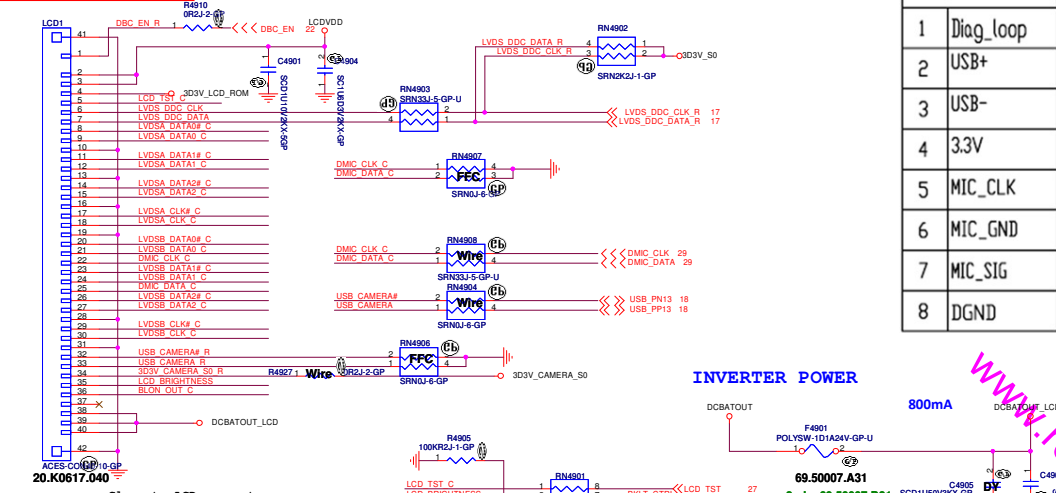
M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51463 VCCSA**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 48	of 105

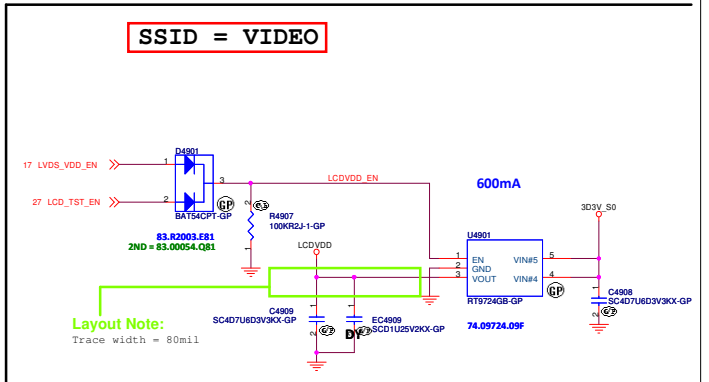
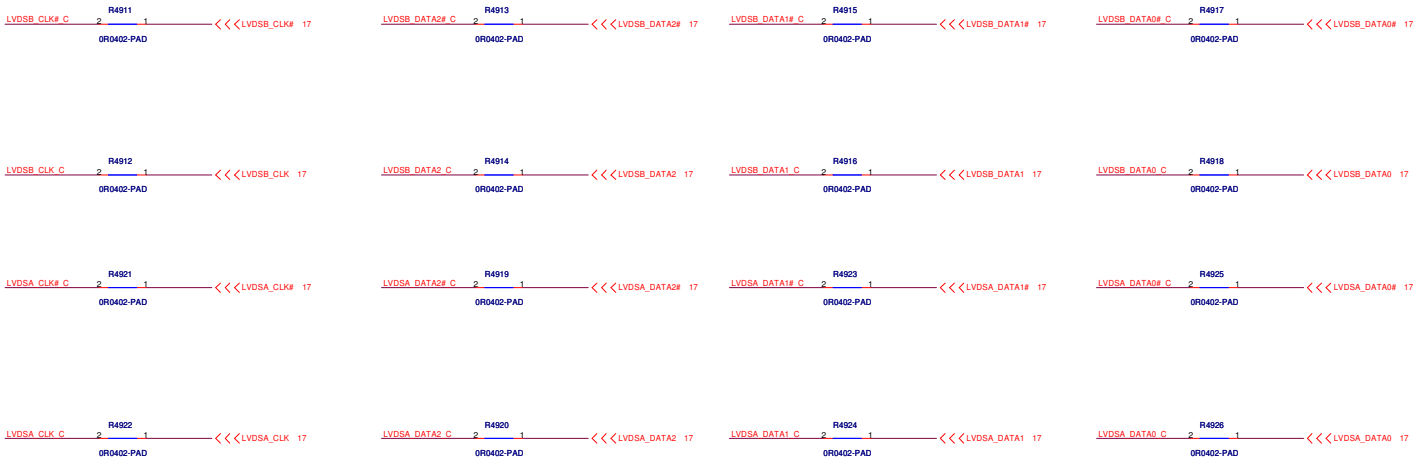
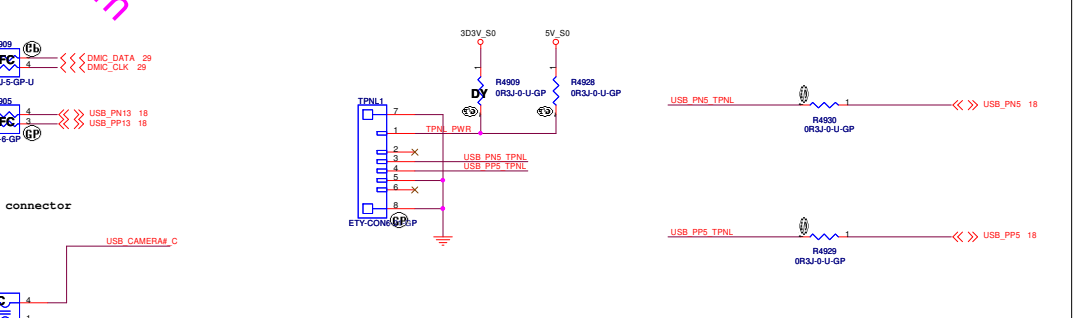
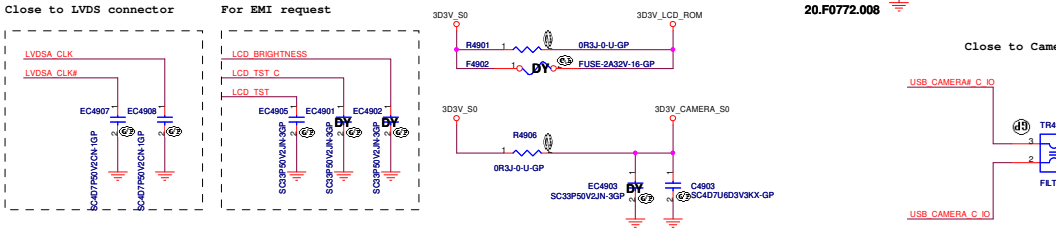
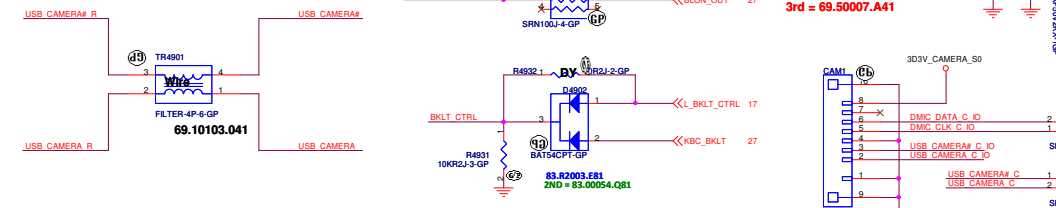
SSID = VIDEO



CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

Pin	MB Connector	是否接線	Wire (40 PIN)	Wire (40 PIN)
Pin 10	GND	Y	Pin 10(GND 實體線)	Pin 10 GND
Pin 13	GND	Y	Pin 13(GND 實體線)	Pin 13 GND
Pin 16	GND	Y	Pin 16 (GND實體線)	Pin 16 GND
Pin 19	GND	Y	Camera Module Pin 6 DMIC_GND(實體線)	Pin 19 GND
Pin 22	GND	Y	Camera Module Pin 5 AUD_DMIC_CLK	Pin 22 GND
Pin 25	GND	Y	Camera Module Pin 7 AUD_DMIC_IN0	o
Pin 28	GND	Y	Camera Module Pin 8 CCD_GND(實體線)	Pin 28 GND
Pin 31	GND	Y	Pin 31 (實體線)	Pin 31 GND
Pin 32	GND	Y	Camera Module Pin 3 USB_CAMERA#	Pin 32 GND
Pin 33	GND	Y	Camera Module Pin 2 USB_CAMERA	Pin 33 GND
Pin 34	3D3V_CAMERA_S0	Y	Camera Module Pin 4 3D3V_CAMERA_S0	NC(0 ohm DY)

PIN	MB Connector	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0



h0p0p0p0p0p0p0p0p0p0

M14 DIS

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Document Number: **LCD Connector**

Rev: **A00**

Date: Wednesday, September 05, 2012 Sheet 49 of 105

www.rosefix.com

(Blanking)

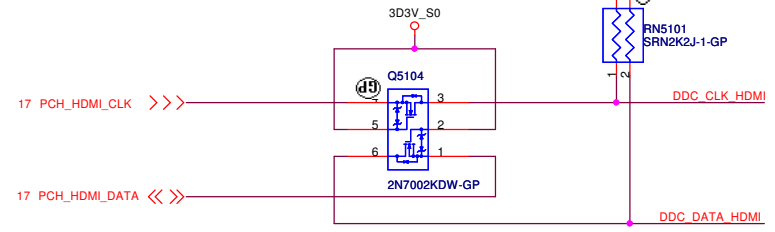
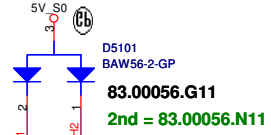
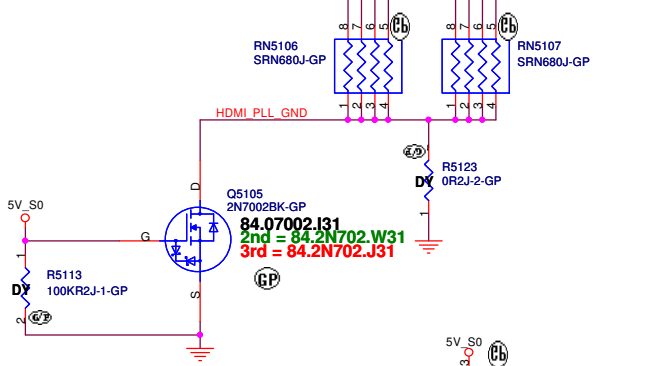
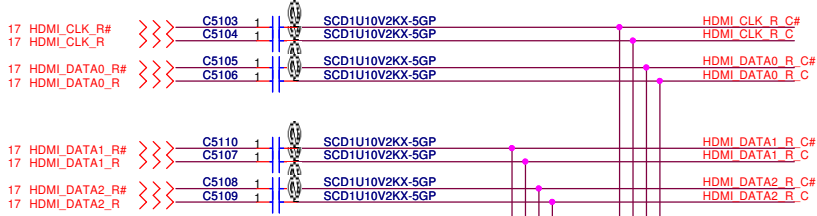
M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		CRT Connector
Size A3	Document Number	Rev A00
Date: Wednesday, September 05, 2012	Sheet 50	of 105

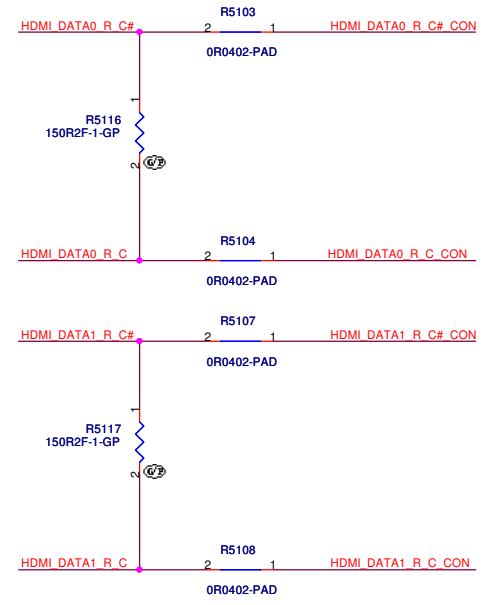
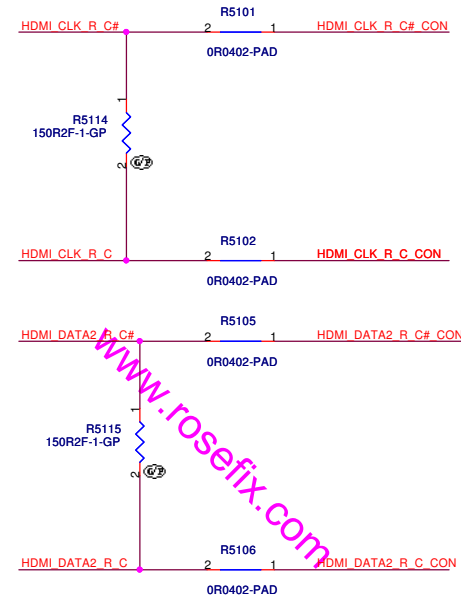
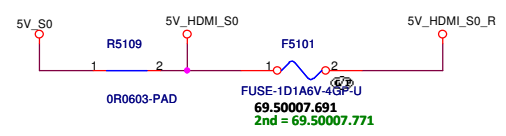
h0605/15128061.Mh

SSID = VIDEO

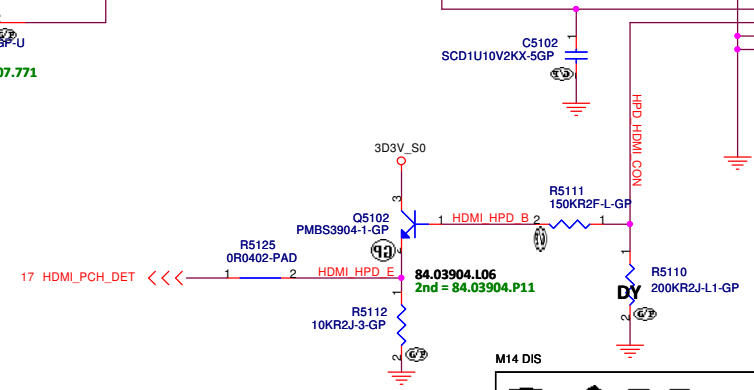
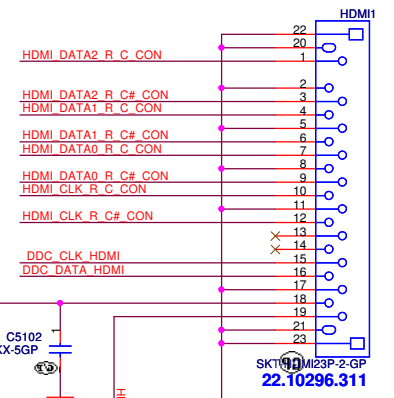
HDMI Level Shifter



84.2N702.A3F
 2nd = 84.DM601.03F
 3rd = 84.2N702.E3F
 4th = 84.2N702.F3F



HDMI CONN



DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Connector**
 Size A3 Document Number: **OAK14 Chief River DIS** Rev: **A00**
 Date: Wednesday, September 05, 2012 Sheet 51 of 105

h0p05y1512806PMh

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 52 of 105

h0605/151280617.Mn

www.rosefix.com
(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 53 of 105

h0605/151280617.Mn

www.rosefix.com

(Blanking)

M14 DIS


		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 54 of 105

h0605/151280617.Mn

SSID = User.Interface

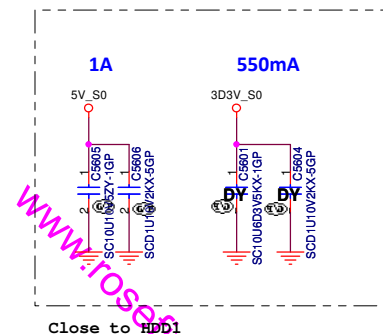
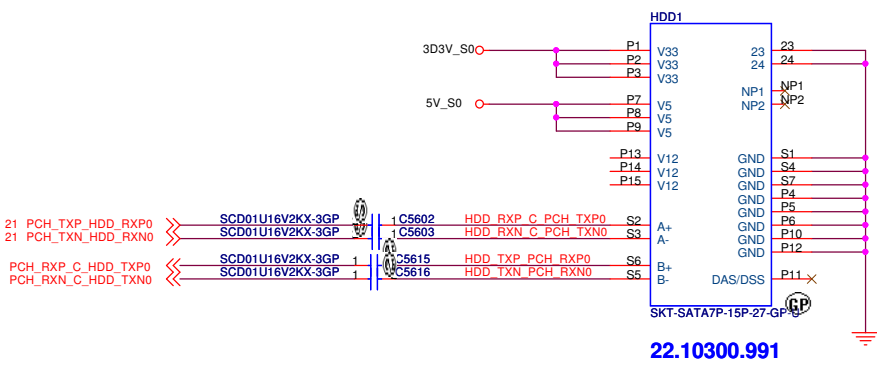
www.rosefix.com
(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
ITP/Fan Connector		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 55	of 105

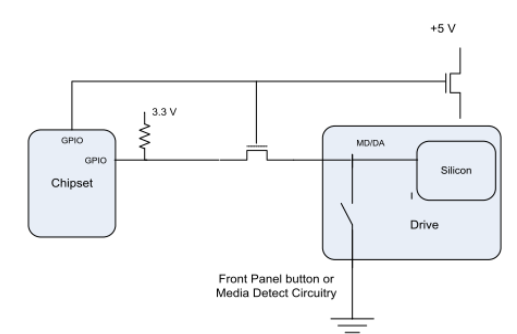
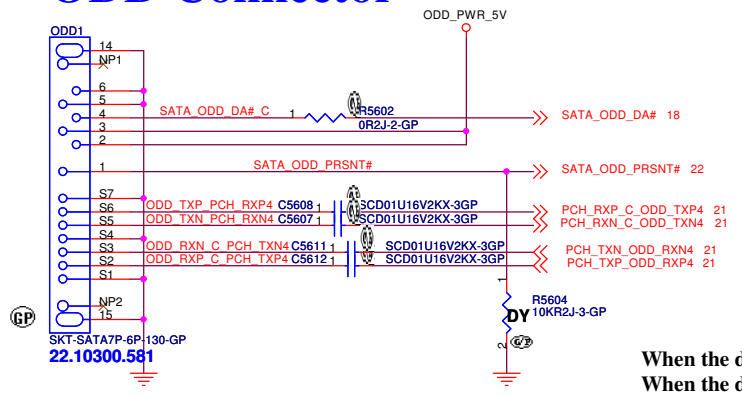
h0005/15128061.Mn

SATA HDD Connector

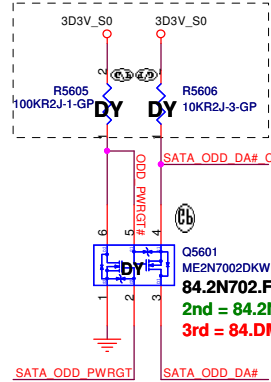


www.rosefix.com

ODD Connector



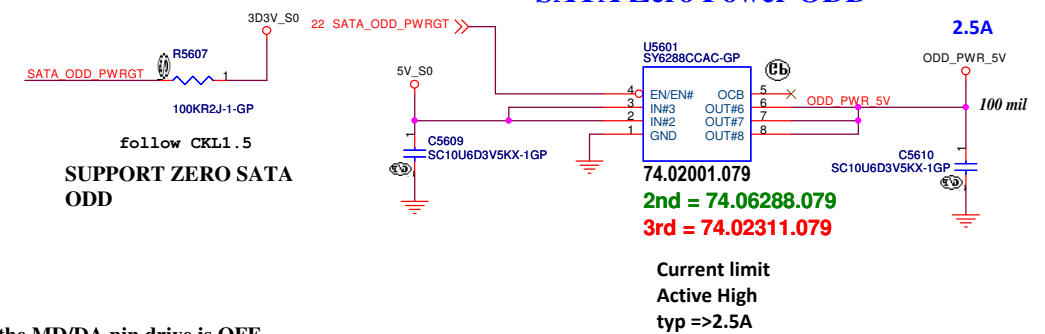
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
 When the drive is powered off, the FET to the MD/DA pin is ON



A00-0408 Add R5606 to pull high 3.3V_S0
 Change pull high to 3.3V_S0
 A00-0415 Dummy R5606

Q5601
 ME2N7002DKW-G-GP
84.2N702.F3F
 2nd = 84.2N702.A3F
 3rd = 84.DMN66.03F

SATA Zero Power ODD



www.rosefix.com

SSID = ESATA

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		ESATA
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 57 of 105

h0005/151280617.Mn

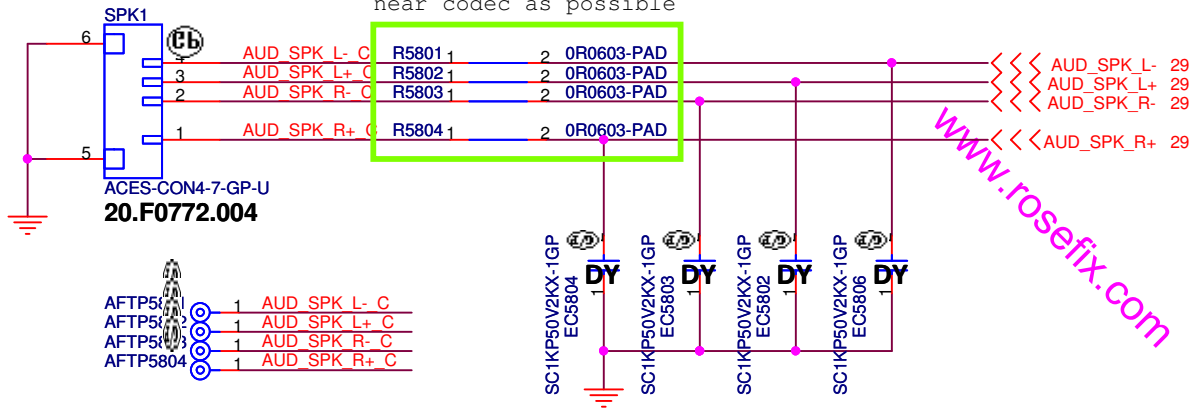
SSID = AUDIO

Speaker

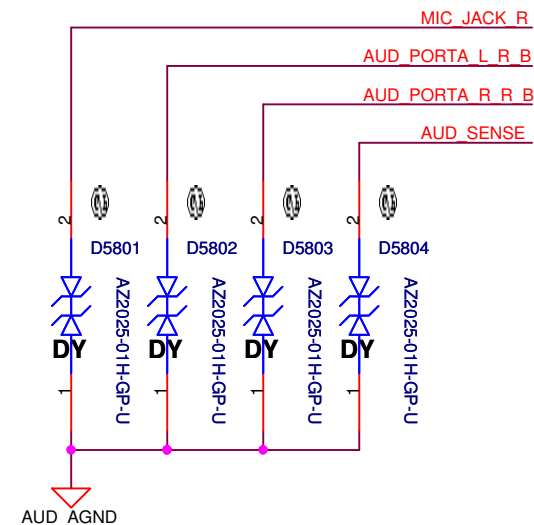
Layout Note:

trace width=30mil

R5801~R5804 and EC5804~EC5806
near codec as possible

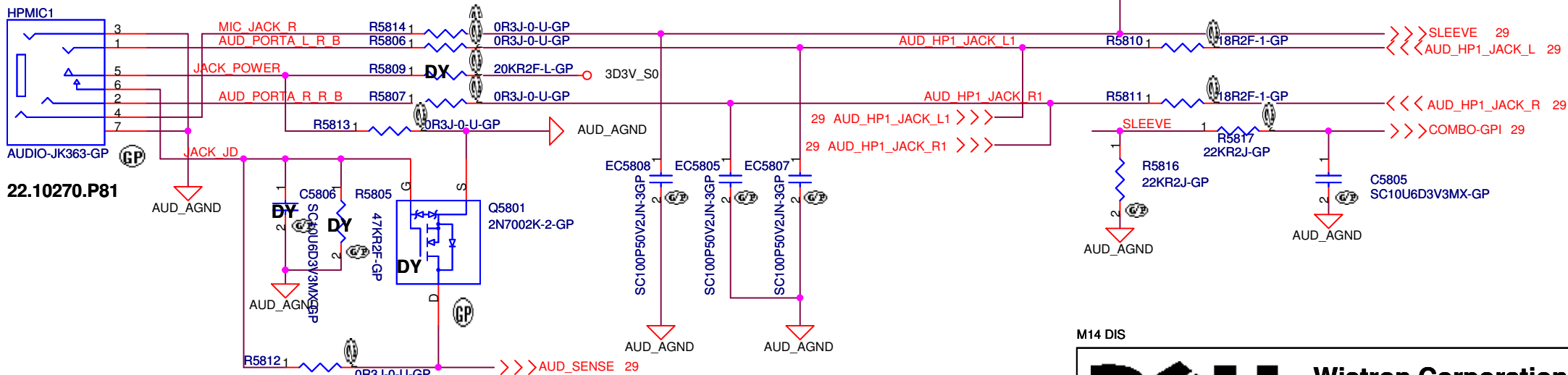


X01 0605



Combo Jack

change to 22.10270.P81, but symble not change



M14 DIS



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Speaker/HPMIC CONN

Size

Document Number

Rev

OAK14 Chief River DIS

A00

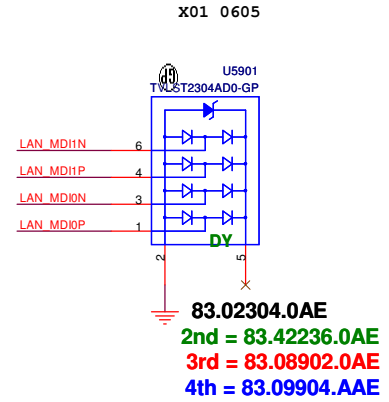
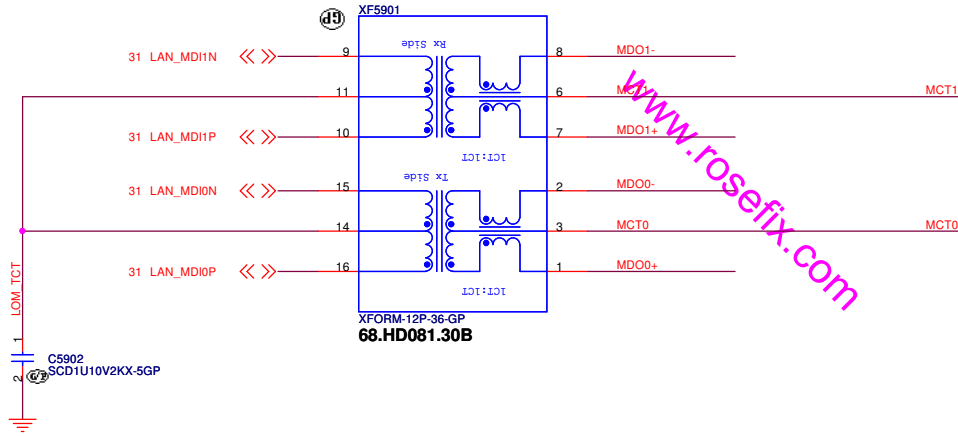
Date: Wednesday, September 05, 2012

Sheet 58 of 105

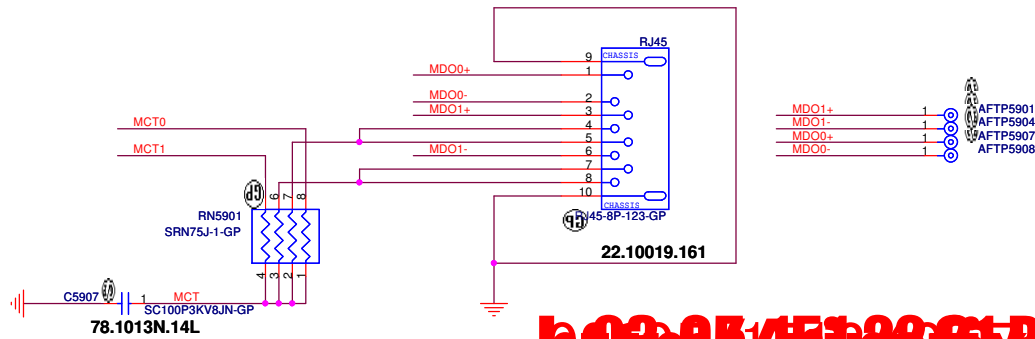
h0p05y0h02000P.Mh

SSID = LOM

LAN TransFormer



RJ45



<Core Design>

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

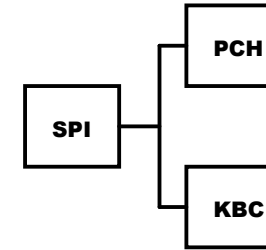
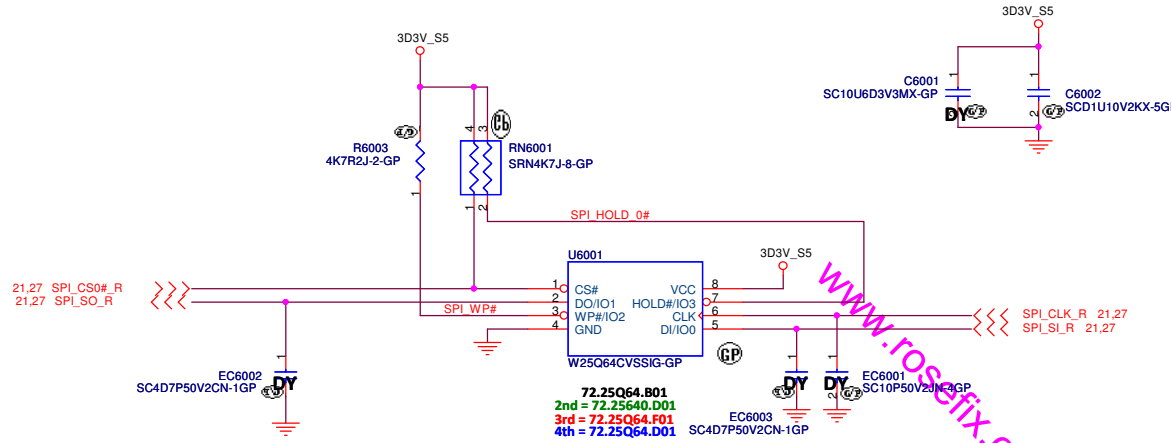
Title: **XFOM&RJ45**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012 Sheet 59 of 105		

h0p05y4512806P.M

SSID = Flash.ROM

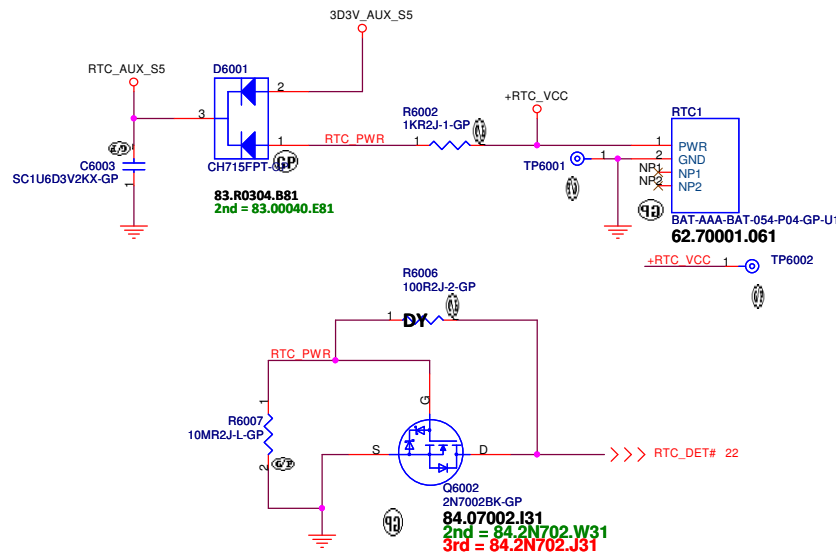
SPI Flash ROM(8M) for PCH



Layout Note:

KBC---1.0"---PCH
KBC---1.5"~6.5"---SPI
PCH---0.5"~6.5"---SPI

SSID = RBATT

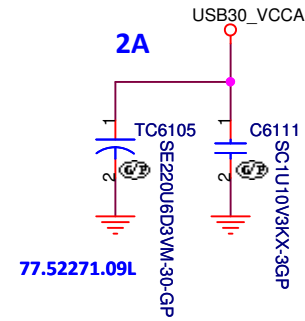
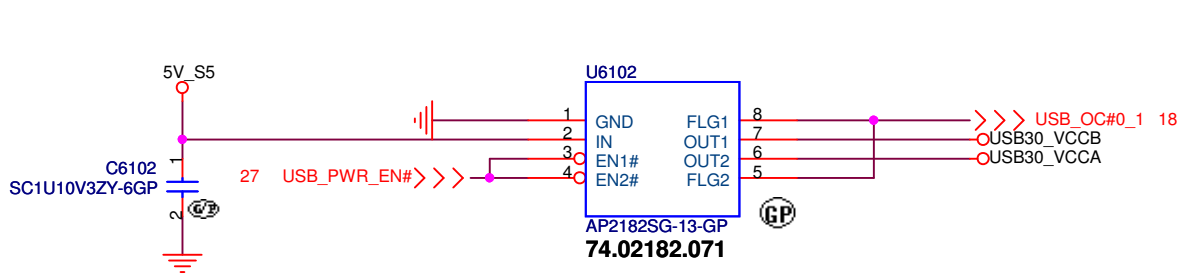


M14 DIS

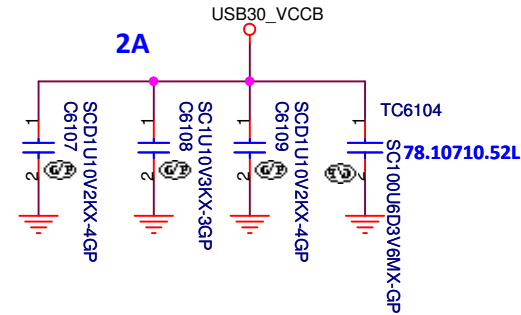


Title Flash/RTC		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date Wednesday, September 05, 2012	Sheet 60	of 105

h0p05y1512806PM



USB3.0 Port1

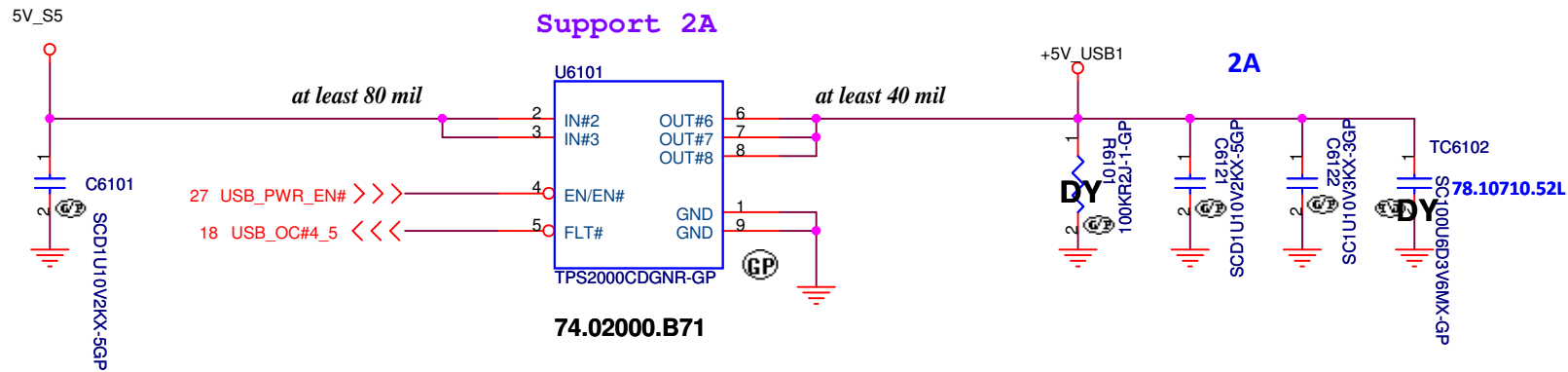


USB3.0 Port2

www.rosefix.com

Right USB Power x1

Support 2A



M14 DIS

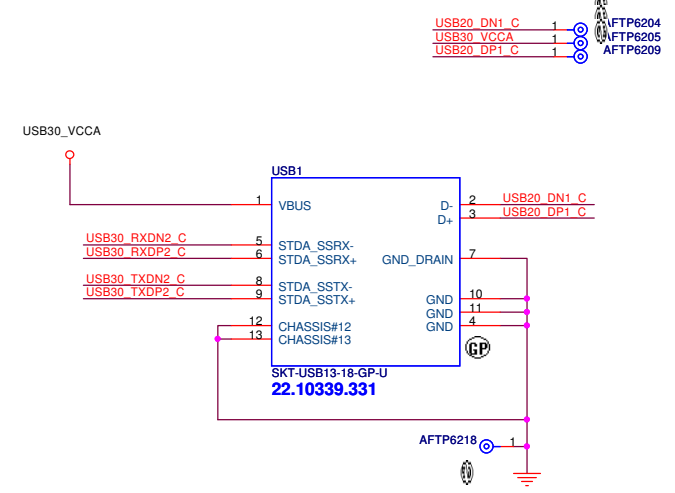
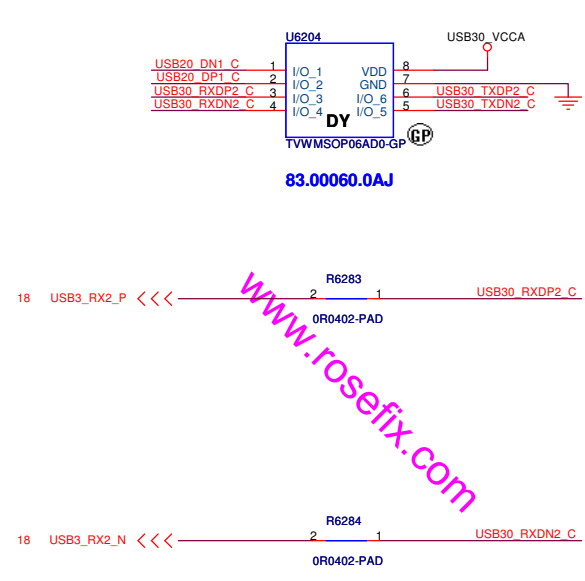
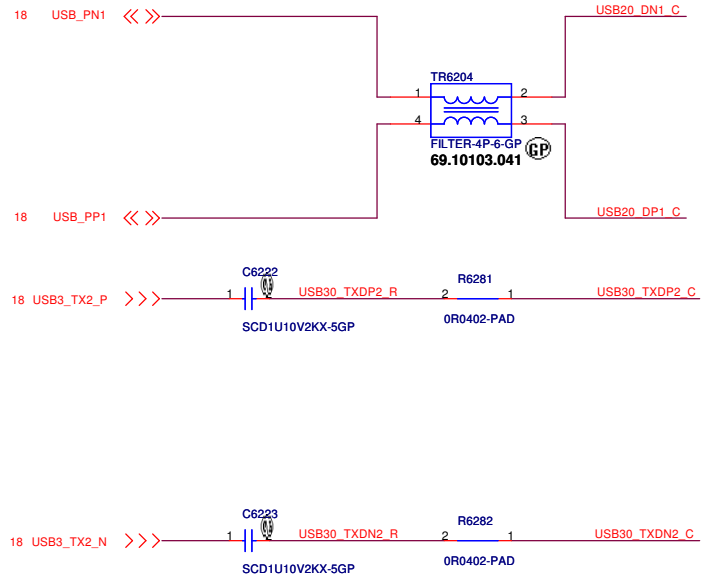
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB Power SW		
Size	Document Number	Rev
	OAK14 Chief River DIS	A00
Date:	Wednesday, September 05, 2012	Sheet 61 of 105

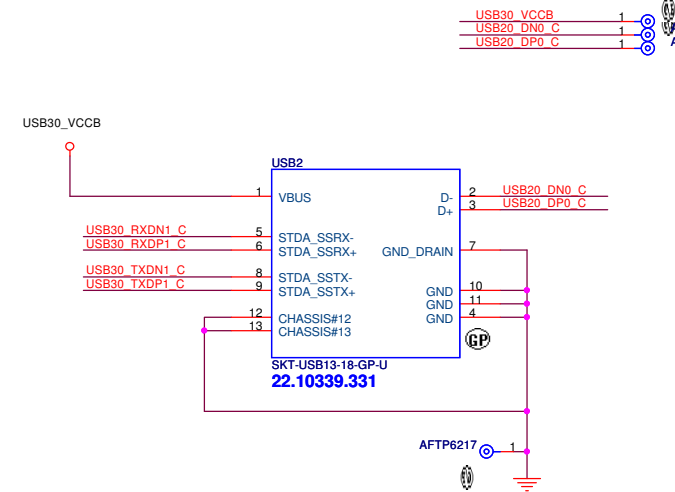
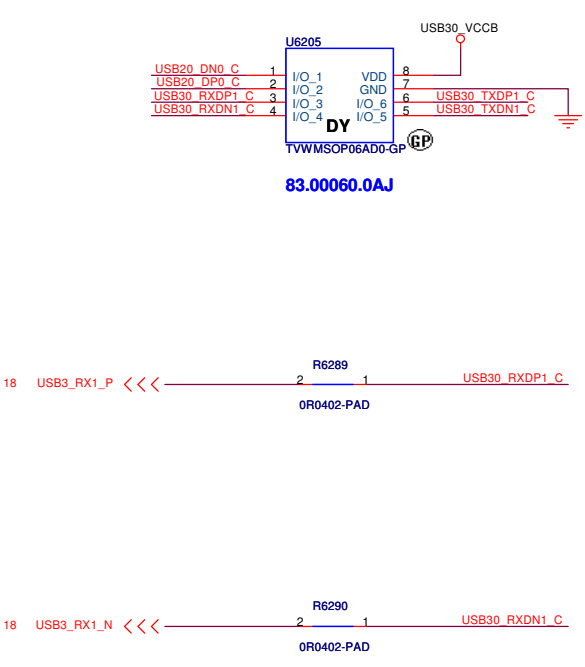
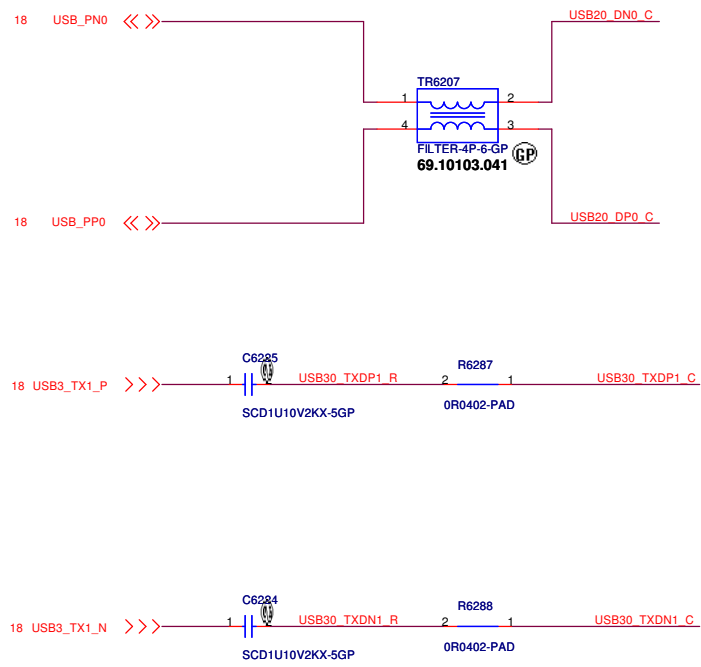
h0p05y15128061P.Mh

SSID = USB

USB3.0 Port1



USB3.0 Port2



M14 DIS

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 62	of 105

h0p05y15128062PNh

SSID = USB

www.rosefix.com

(Blanking)

h0005/151280617.Mn

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
USB3.0 PORT		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 63 of 105

www.rosefix.com

(Blanking)

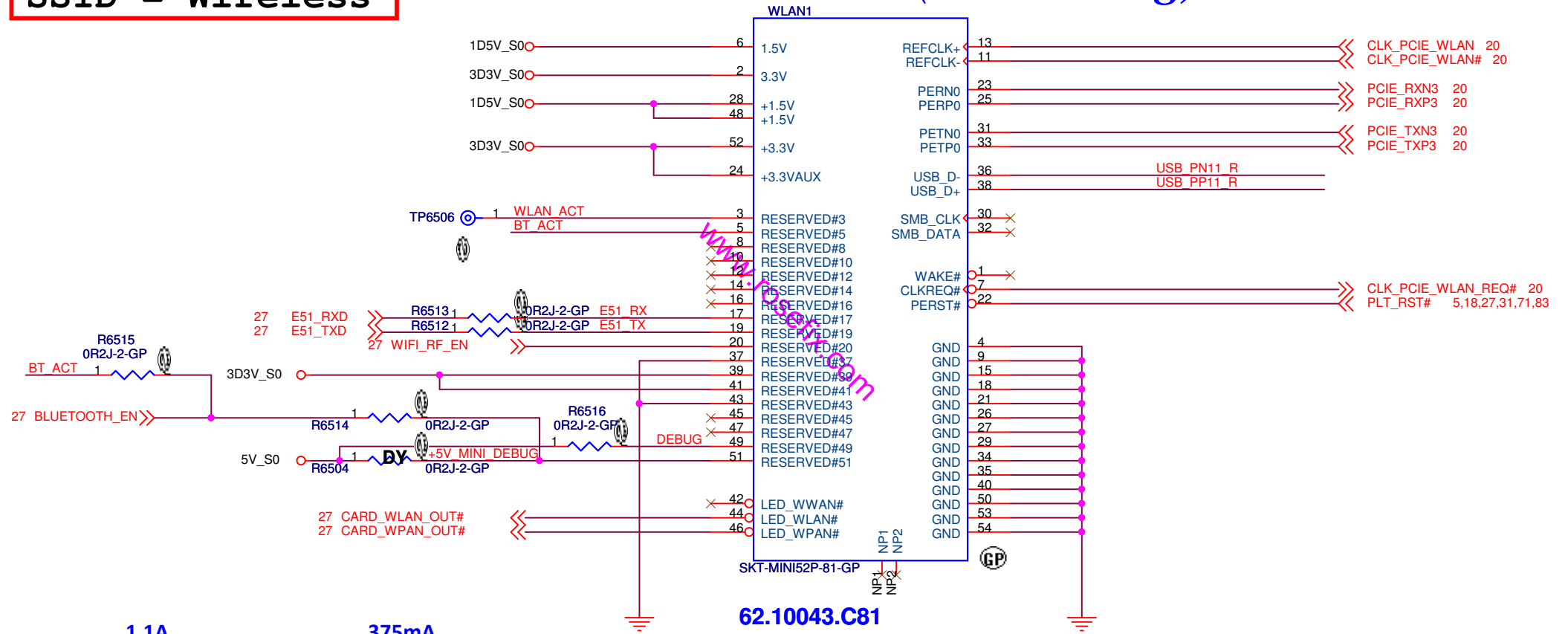
M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RESERVED		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 64	of 105

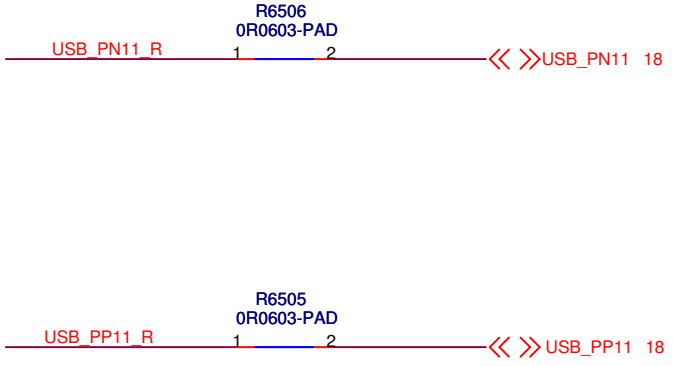
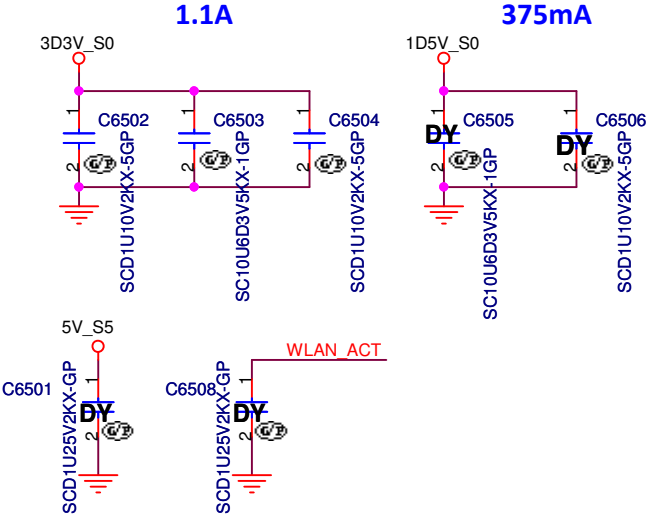
h0605/15128061.Mh

SSID = Wireless

Mini Card Connector(802.11a/b/g)



62.10043.C81



h0605/1512861P.M

M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title MINICARD(WLAN)/ITP CONN			
Size A4	Document Number OAK14 Chief River DIS		Rev A00
Date: Wednesday, September 05, 2012		Sheet 65	of 105

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	OAK14 Chief River DIS	A00	
Date: Wednesday, September 05, 2012		Sheet 66	of 105

h0005/151280617.Mn

www.rosefix.com

(Blanking)

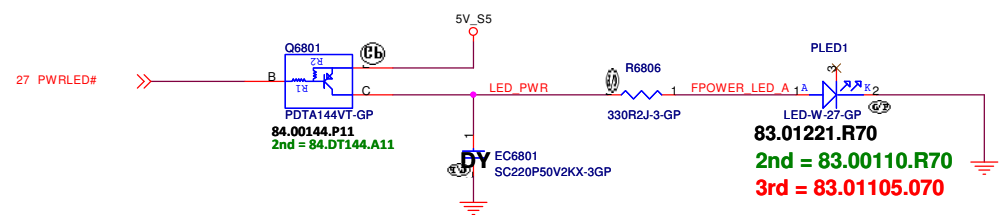
M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 67 of 105

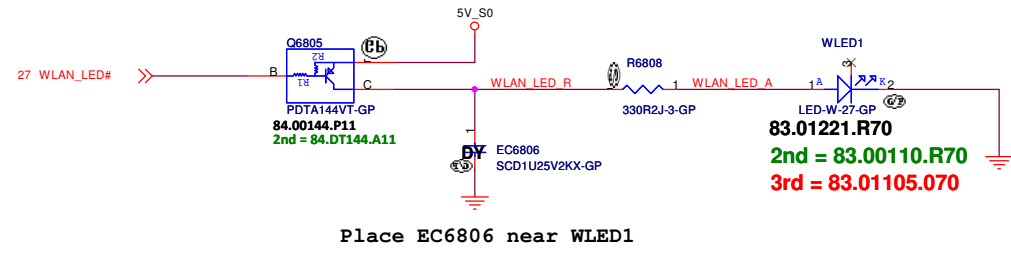
h0605/15128067.Mn

SSID = User.Interface

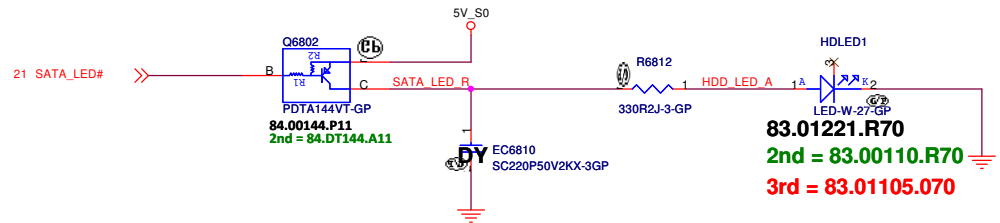
FRONT POWER LED
Low actived from KBC GPIO



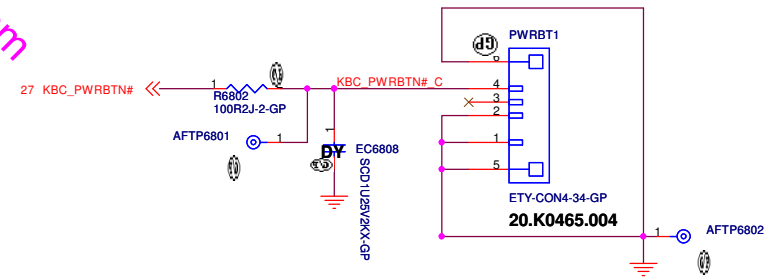
Wireless LED
Low actived from KBC GPIO



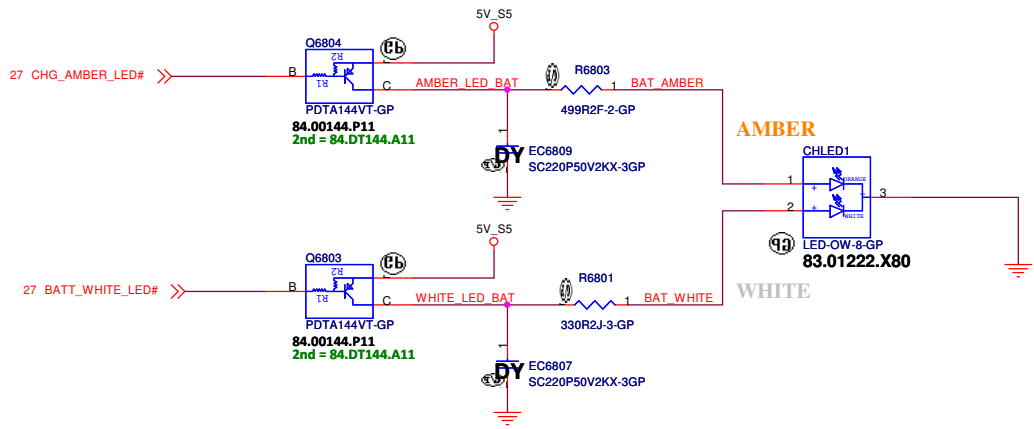
SATA HDD LED (White)
Low actived from PCH GPIO



Power button



Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

h0p05/y5t286P.Mh

M14 DIS

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

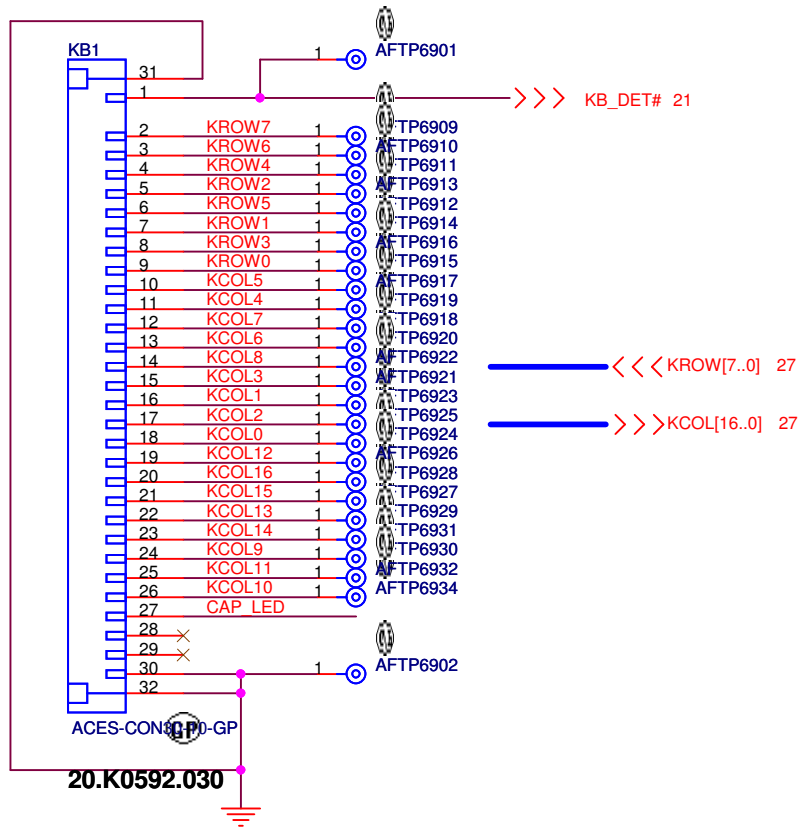
Title: **LED Bard/Power Button**

Size A3 Document Number **OAK14 Chief River DIS** Rev **A00**

Date: Wednesday, September 05, 2012 Sheet 68 of 105

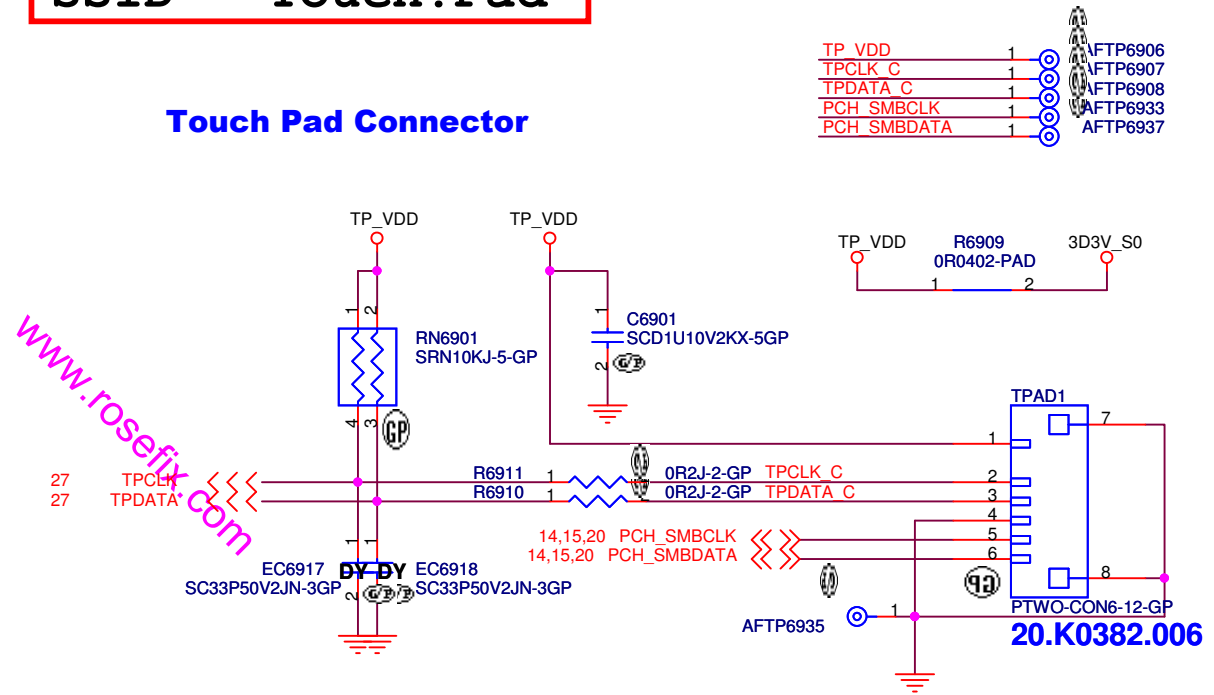
SSID = KBC

Internal Keyboard Connector



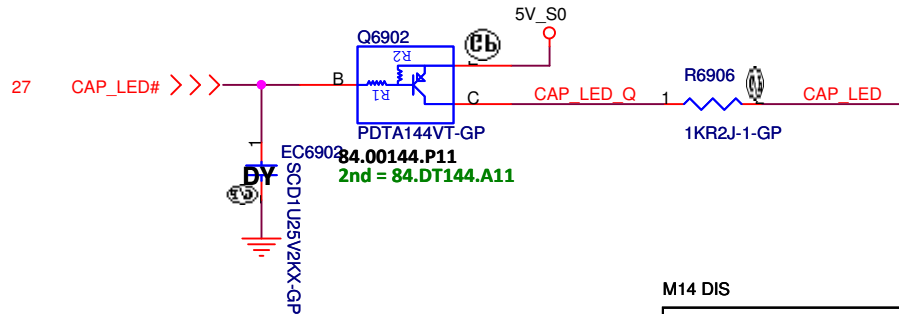
SSID = Touch.Pad

Touch Pad Connector



CAP LED Control

LOW acted from KBC GPIO



M14 DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size
A4

Document Number

OAK14 Chief River DIS

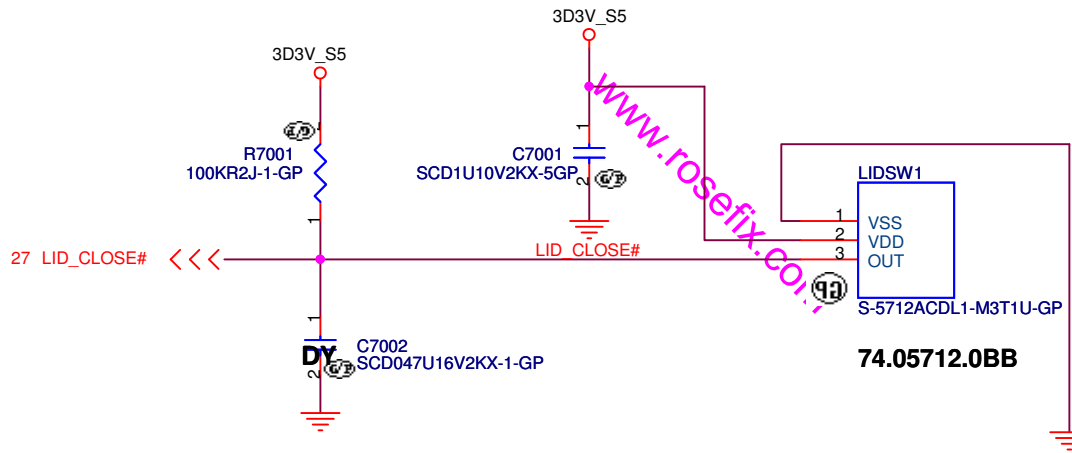
Rev
A00

Date: Wednesday, September 05, 2012

Sheet 69 of 105

h0p05/1512861P.Mh

SSID = User.Interface



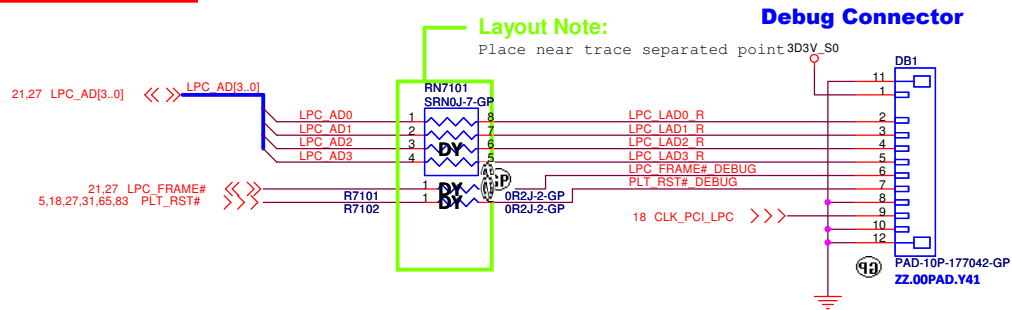
M14 DIS



Title		
Hall Sensor		
Size A4	Document Number OAK14 Chief River DIS	Rev A00
Date	Wednesday, September 05, 2012	Sheet 70 of 105

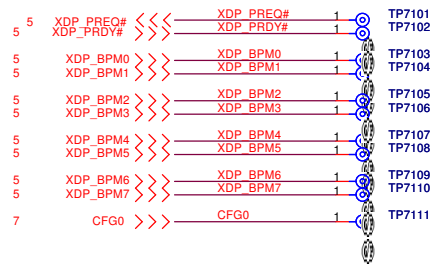
h0p05y1512806P.Mm

SSID = DEBUG PORT



SSID = CPU

CPU XDP



www.rosefix.com

M14 DIS

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Dubug connector			
Size: A3	Document Number: OAK14 Chief River DIS		Rev: A00
Date: Wednesday, September 05, 2012		Sheet: 71	of: 105

h0005/15128061.M

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 72 of 105

h0005/151280617.Mn

www.rosefix.com

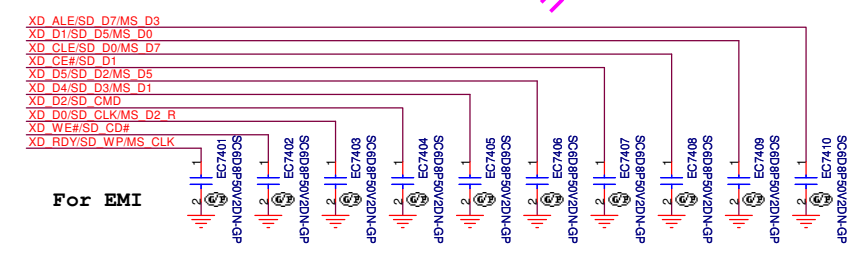
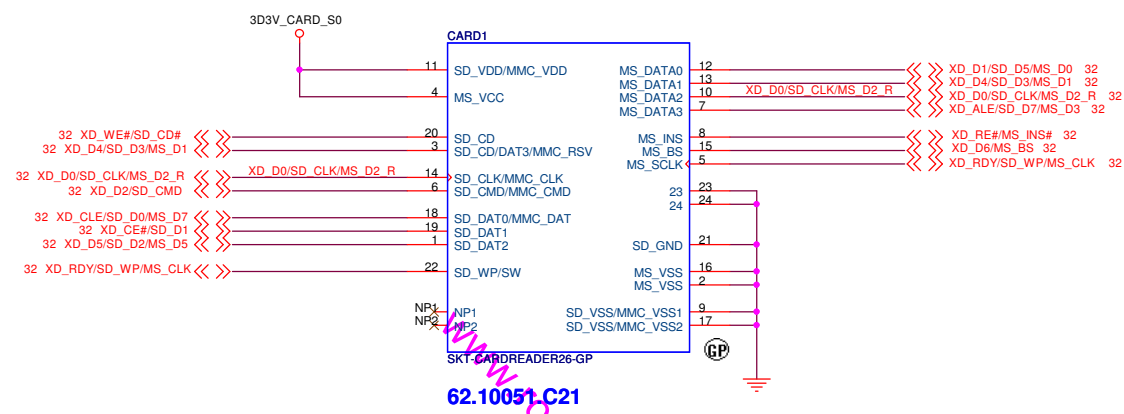
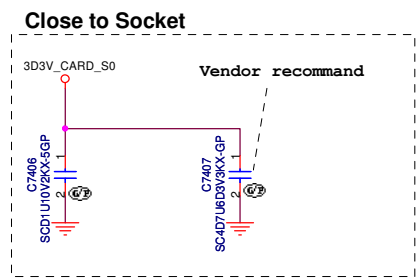
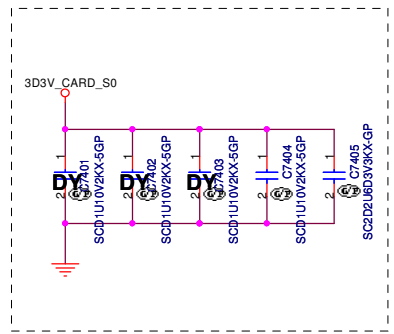
(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	OAK14 Chief River DIS	A00	
Date: Wednesday, September 05, 2012		Sheet 73	of 105

h0605/15128067.Mn

SSID = SDIO



h 0 6 0 5 / 1 5 1 2 8 2 6 P M h

M14 DIS

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SD/XD/MS/MMC Card CONN**

Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012		Sheet 74 of 105

www.rosefix.com
(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Express Card		
Size A3	Document Number OAK14 Chief River DIS	Rev A00
Date: Wednesday, September 05, 2012		Sheet 75 of 105

h0605/15128067.Mn

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 76 of 105

h0605/15128067.Mn

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 77 of 105

h0605/151280617.Mn

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 78 of 105

h0005/15128067.Mn

www.rosefix.com

(Blanking)

h0605/151280617M

M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Free Fall Sensor		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 79 of 105

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 80 of 105

h0005/15128061.m

www.rosefix.com

(Blanking)

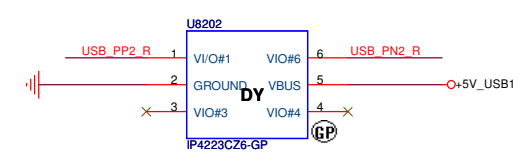
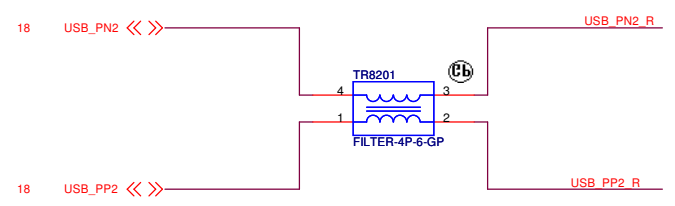
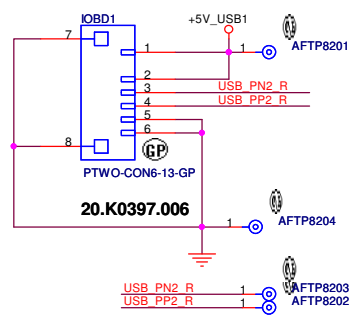
M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012		Sheet 81 of 105

h0605/151280617.Mn

SSID = User.Interface

www.rosefix.com



M14 DIS

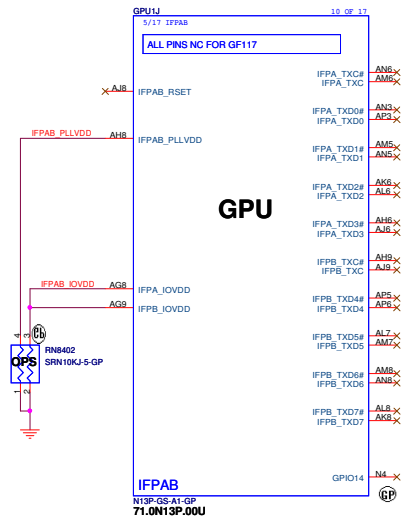
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

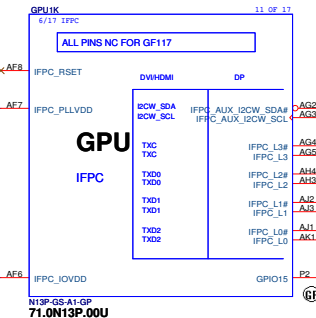
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet: 82 of 105	

h0005/15128061.M

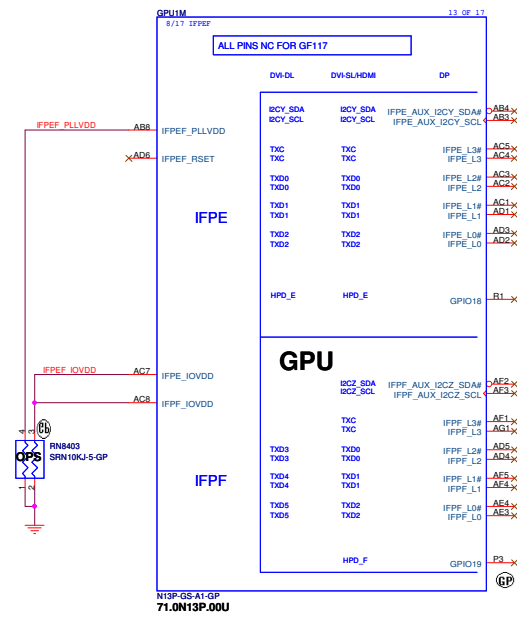
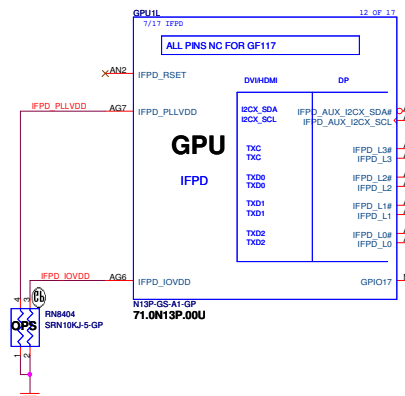
LVDS Interface



www.rosefix.com



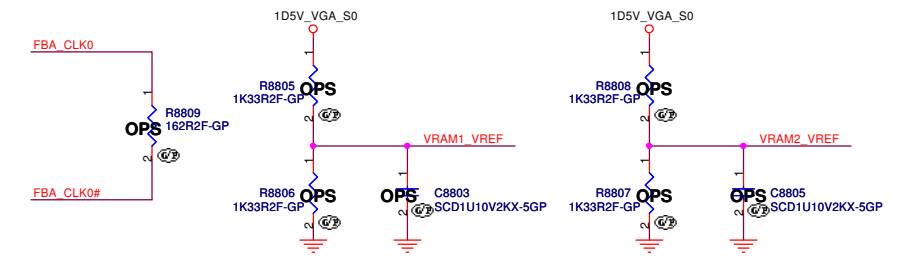
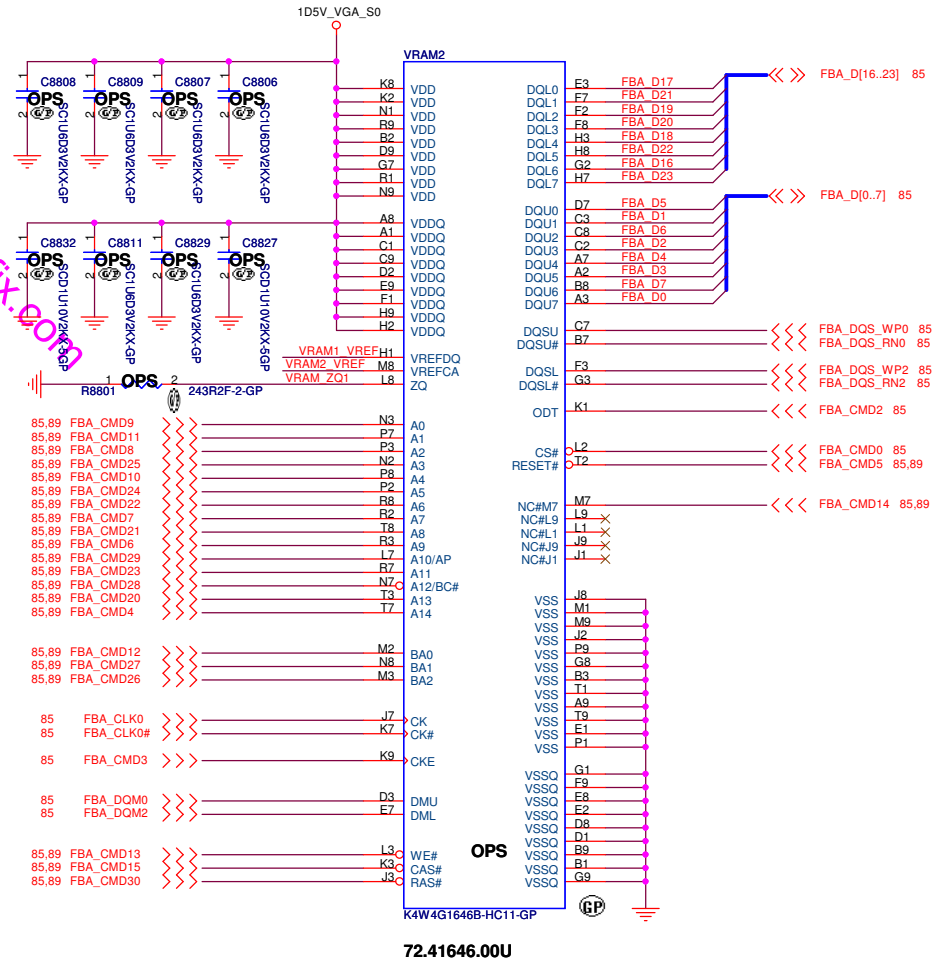
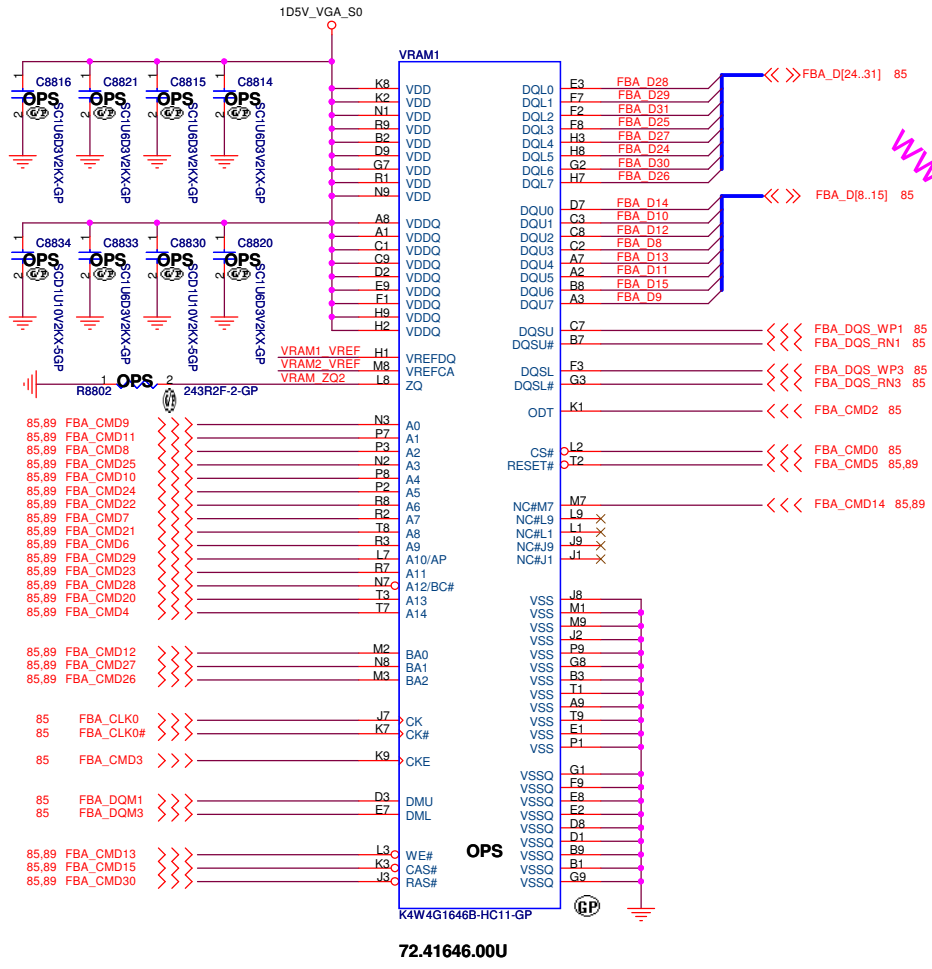
HDMI Interface



h0p0j/512861M

Frame Buffer Partition A-Lower Half

www.rosefix.com



M14 DIS

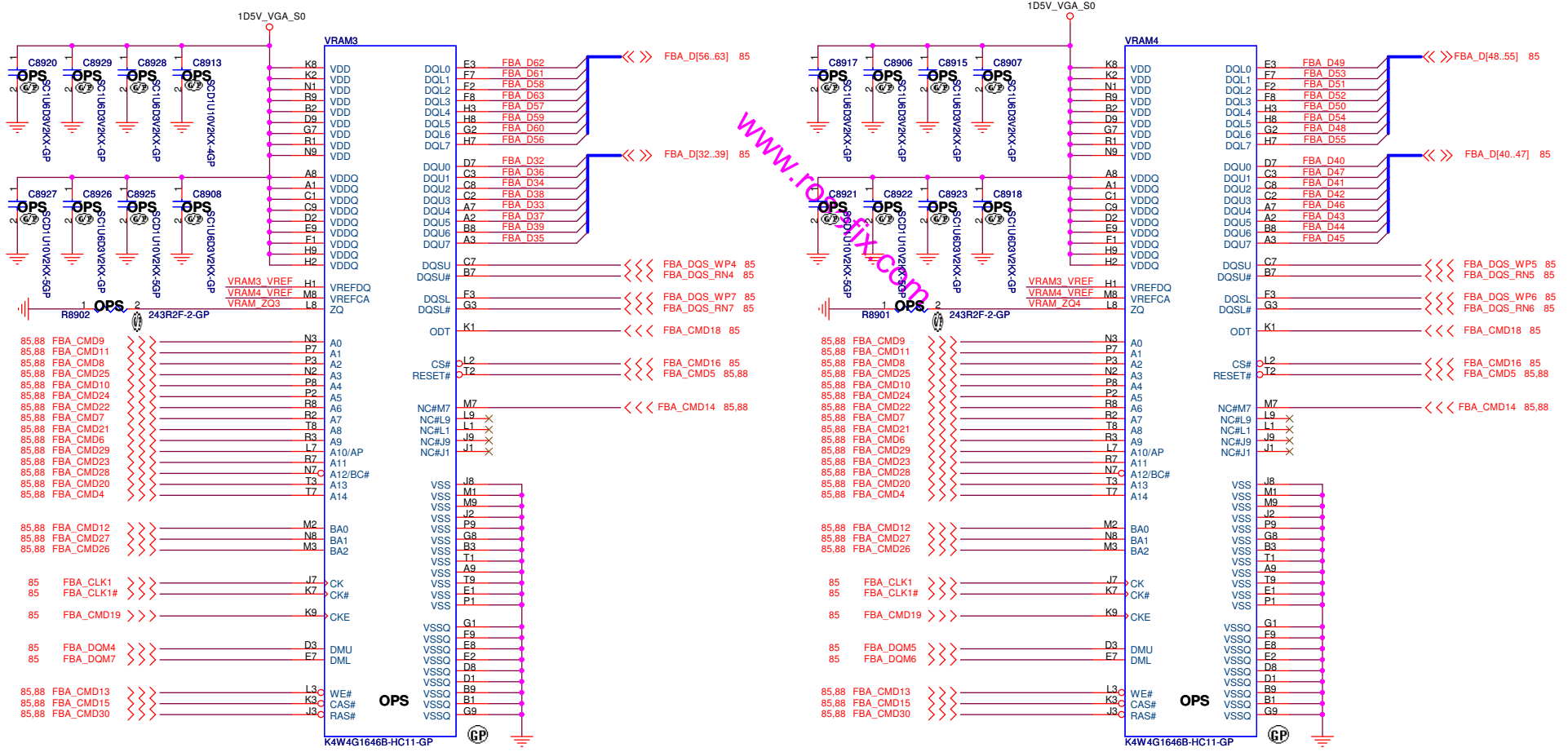
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

Size A3	Document Number	Rev
	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 88	of 105

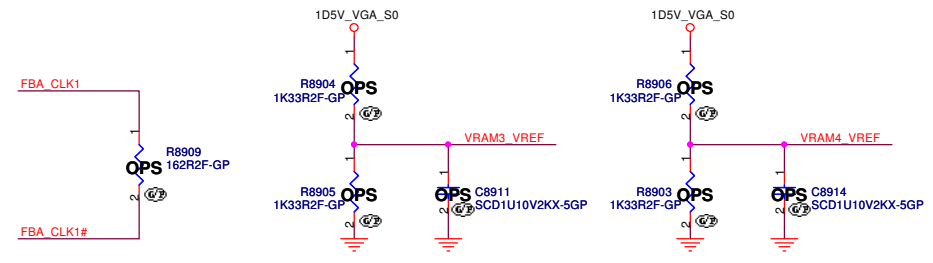
h0p05/1512826P.M

Frame Buffer Partition A-Upper Half



72.41646.00U

72.41646.00U



M14 DIS

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

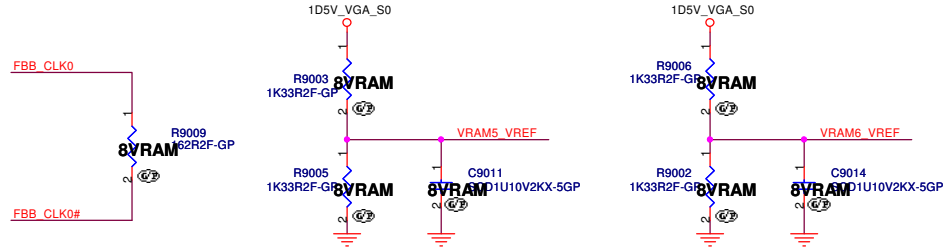
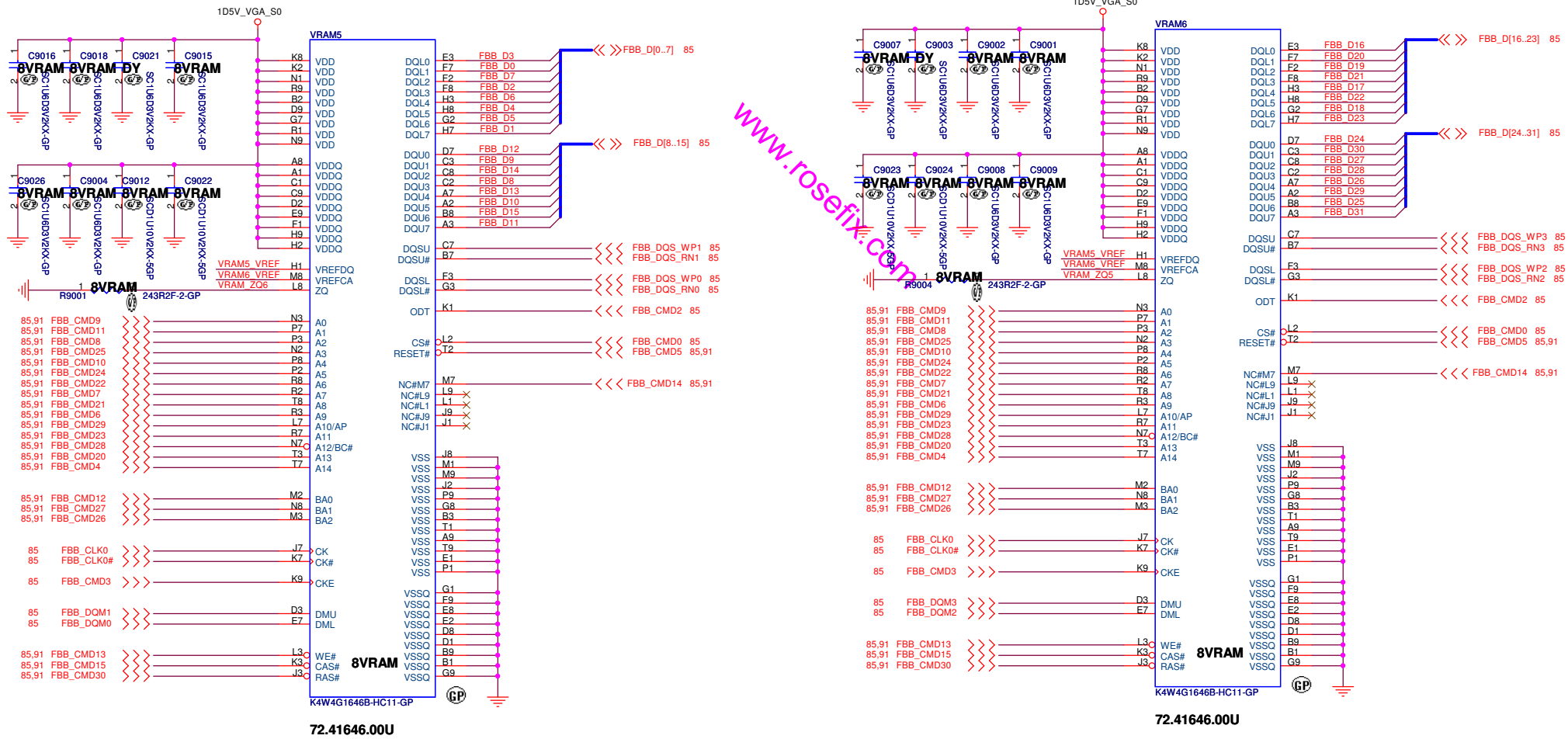
Title: GPU-VRAM3,4 (2/4)

Size A3 Document Number OAK14 Chief River DIS Rev A00

Date: Wednesday, September 05, 2012 Sheet 89 of 105

Copyright © 2012 Dell Inc. All rights reserved. This document is the property of Dell Inc. and is intended for use only by the individual named.

Frame Buffer Partition B-Lower Half



M14 DIS

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

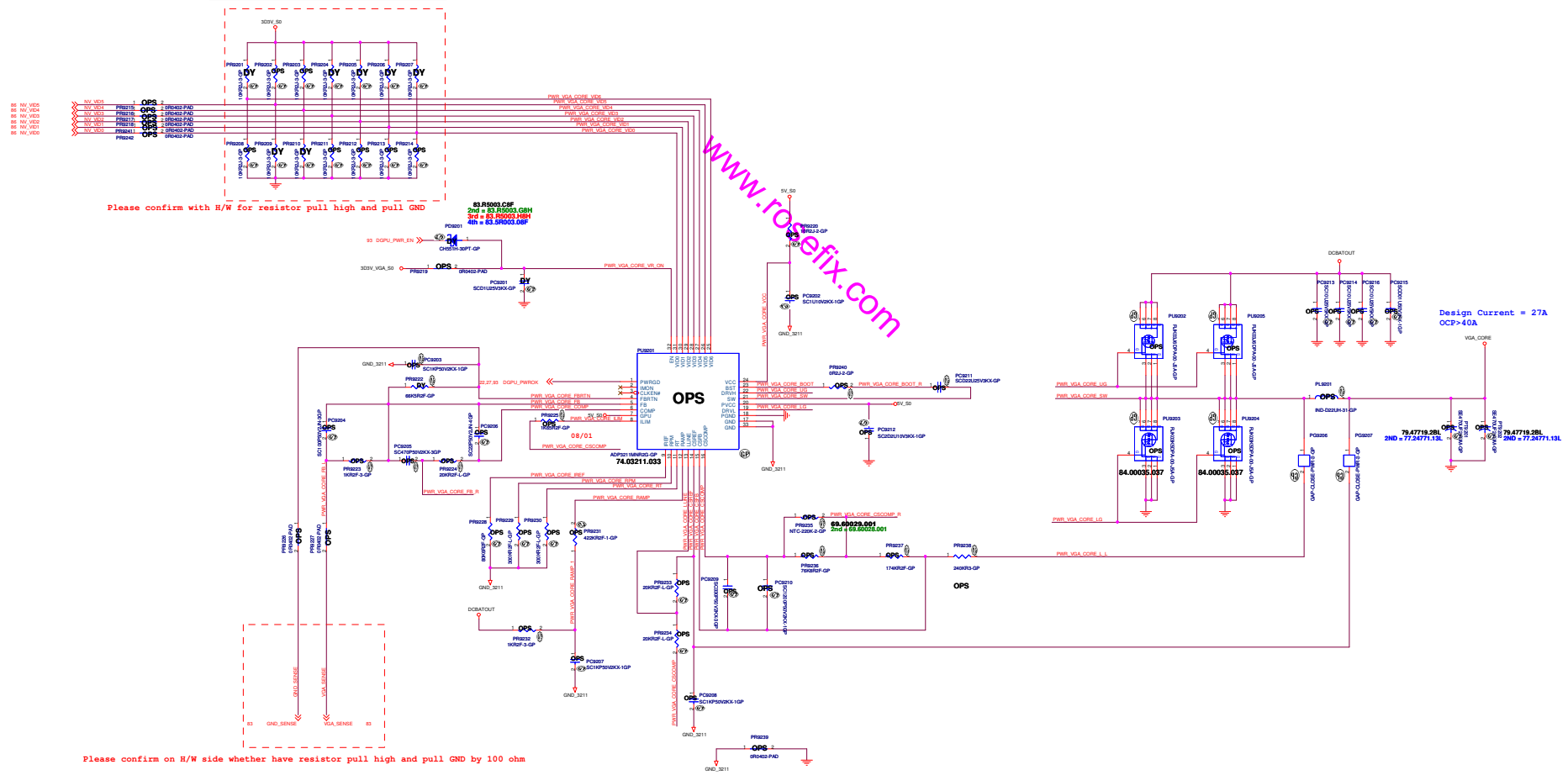
Title: **GPU-VRAM5,6 (3/4)**

Size A3 Document Number **OAK14 Chief River DIS** Rev **A00**

Date: Wednesday, September 05, 2012 Sheet 90 of 105

In Order by 15th 28th 26th PM

V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0



Please confirm with H/W for resistor pull high and pull GND

Please confirm on H/W side whether have resistor pull high and pull GND by 100 ohm

I/P cap: 100 25V K0805 XSR/ 78.10622.511
 Inductor: CHIP COIL 0.303H POWR1047-8340H 1.05mohm/ Isat -60A rms68.R3610.208
 O/P cap: CHIP CAP 470UF 2V EEP3X0D41X/ 3.5Ams Panasonic/79.47719.28L
 R/S: R3M033K0PA-008J5A / 10mohm/13mOhm±4.5Vpp/ 84.00036.037
 L/S: R3M033K5DPA-008J5A / 3mohm/3.5mOhm±4.5Vpp/ 84.00031.037

M14 018

DELL Wistron Corporation
 P.O. Box 1, Main Floor, Taipei, Taiwan, R.O.C.

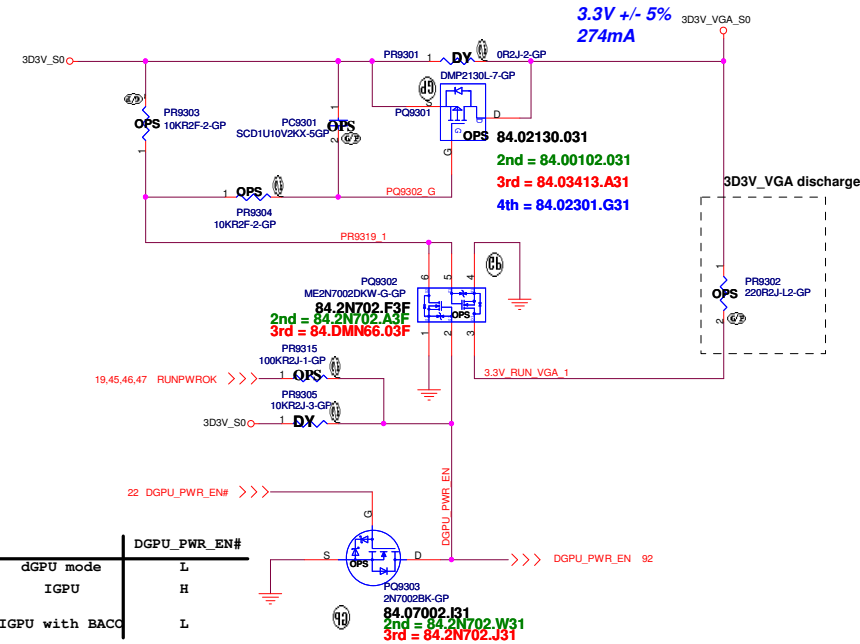
Part: **ADP3211 +VGA CORE**

Rev: **DNE40 14 CR DIS**

Date: Wednesday, September 05, 2012 Sheet: 01 of 100

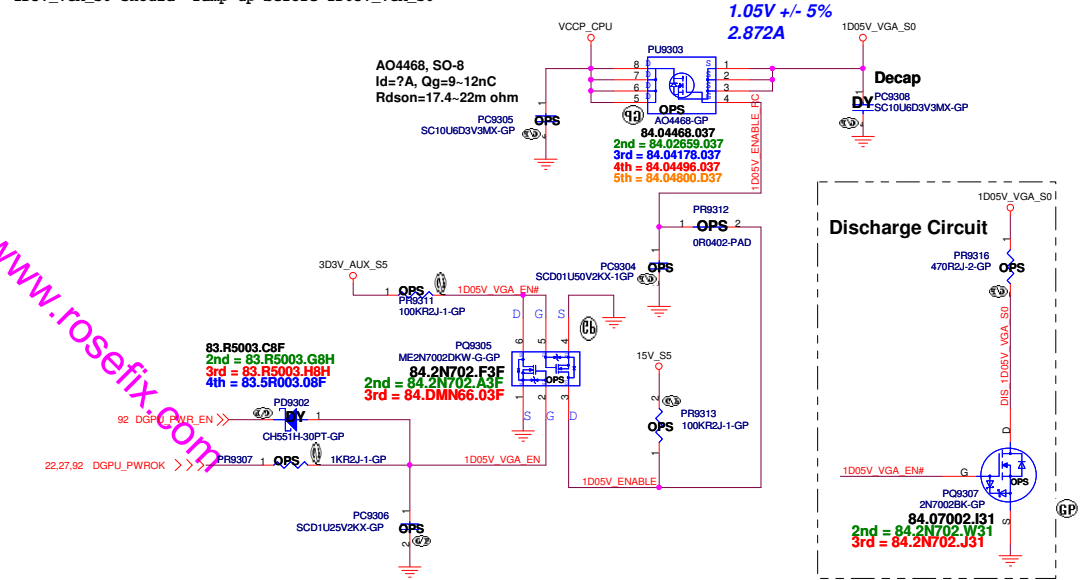
h0p0y4h286P.Mh

3D3V_VGA_S0

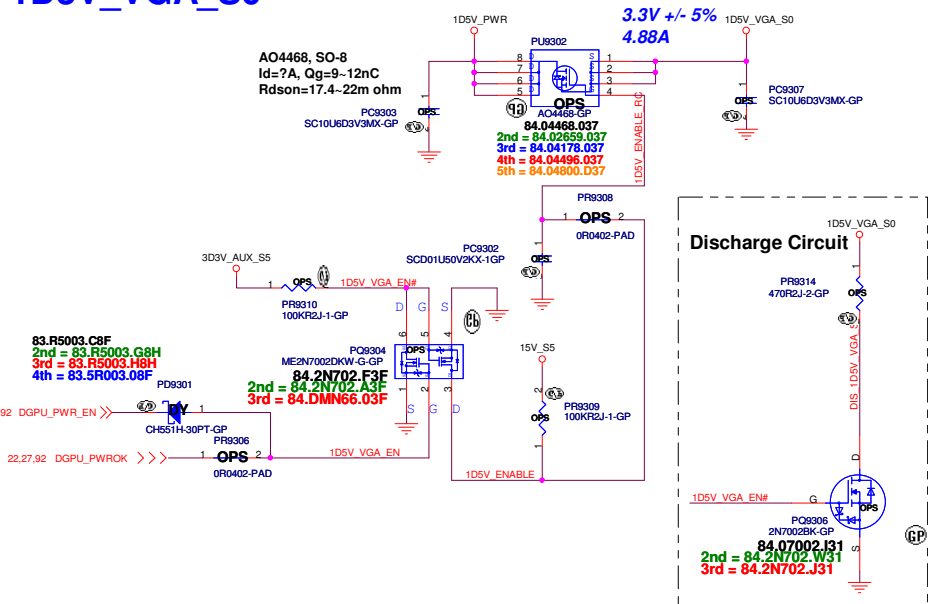


1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0



1D5V_VGA_S0



NV do not need 1.8V

h0p05/y5t286P/Nh

www.rosefix.com

(Blanking)

M14 DIS

			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
LVDS Switch					
Size	Document Number				Rev
A3	OAK14 Chief River DIS				A00
Date:	Wednesday, September 05, 2012	Sheet	94	of	105

10000515129017.Mh

www.rosefix.com

(Blanking)

M14 DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CRT Switch		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date: Wednesday, September 05, 2012	Sheet 95 of	105

100005/15128017.Mn

SSID = SDIO

www.rosefix.com

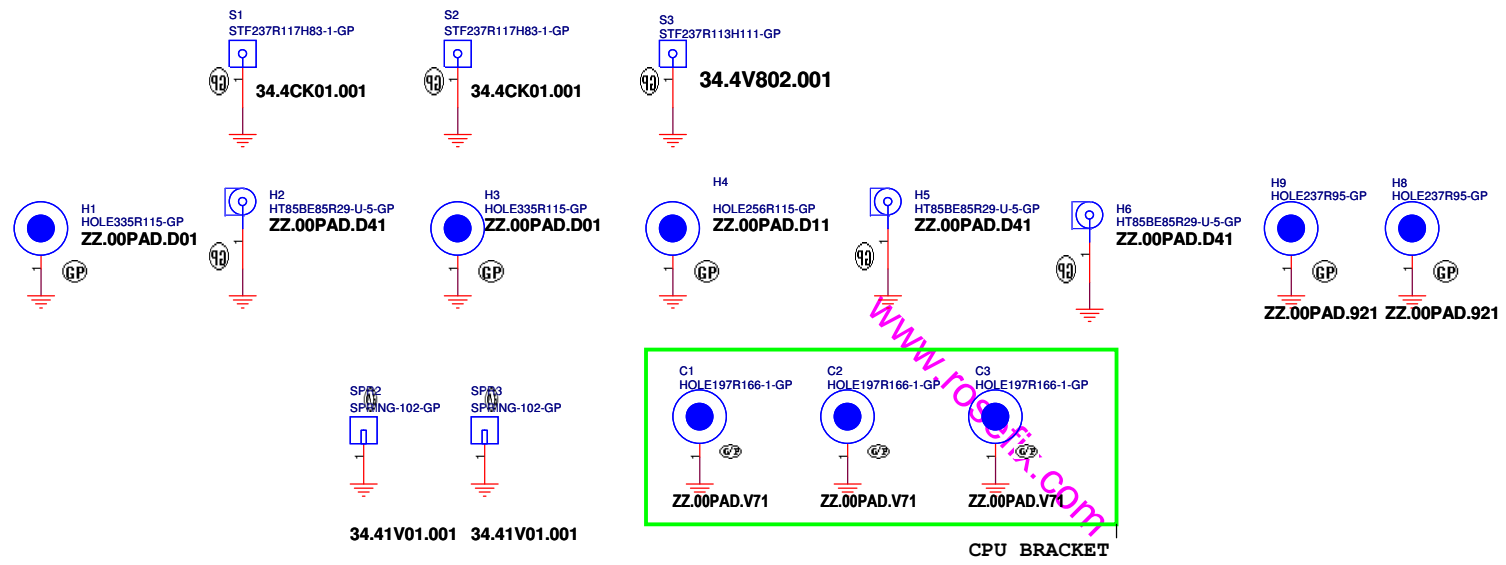
(Blanking)

M14 DIS

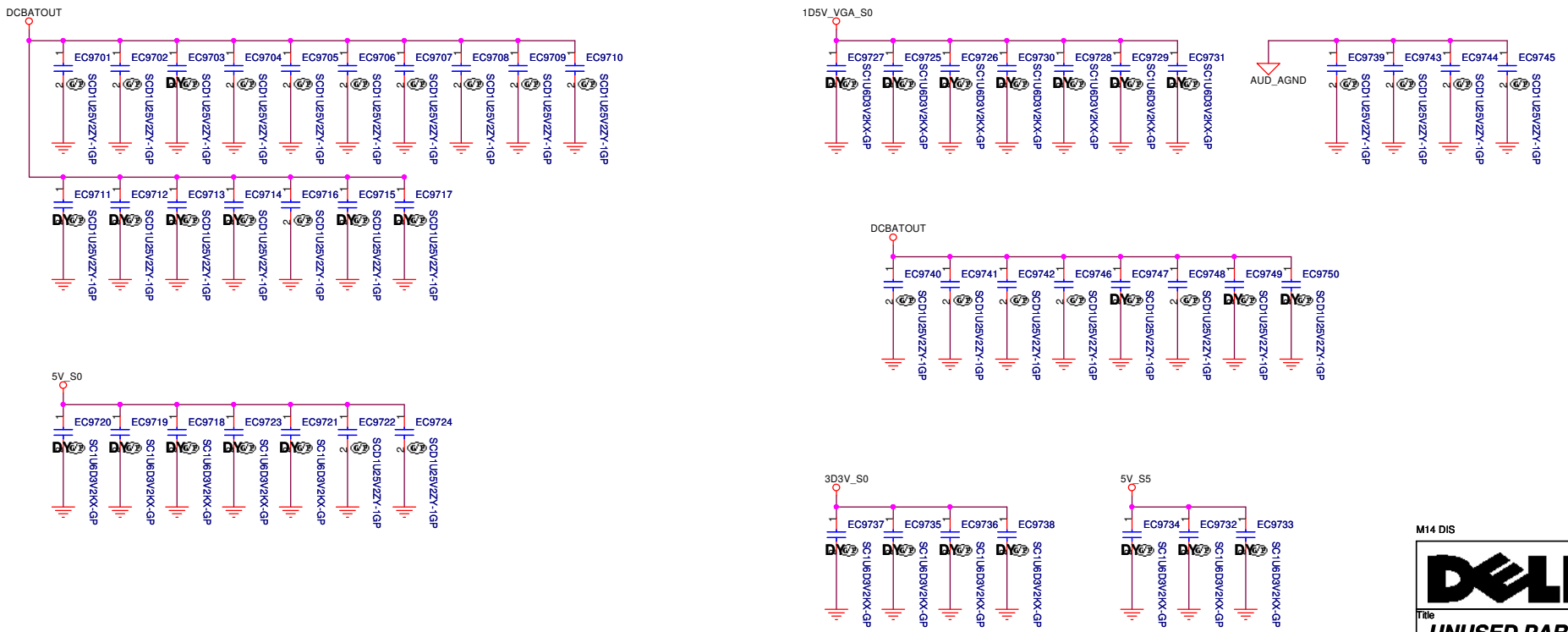
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
TOUCH PANEL		
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00
Date:	Wednesday, September 05, 2012	Sheet 96 of 105

h0005/151280617.Mh

SSID = Mechanical



SSID = EMI



h0p05/1512866PM

M14 DIS

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **UNUSED PARTS/EMI Capacitors**

Size A3	Document Number	Rev
Date: Wednesday, September 05, 2012	OAK14 Chief River DIS	A00
	Sheet 97 of 105	

Chief River Platform Power Sequence

(AC mode)

Red Words: Controlled by EC GPIO

Discrete logic high level, and disable it if it is case than the signal low level.

Td
VDDP_0A must be powered up before VDDA_1, or after VDDA_2 within 0.7V. Also, VDDP_0A must power down after VDDA_2, or before VDDA_1 within 0.7V.

Not floating.

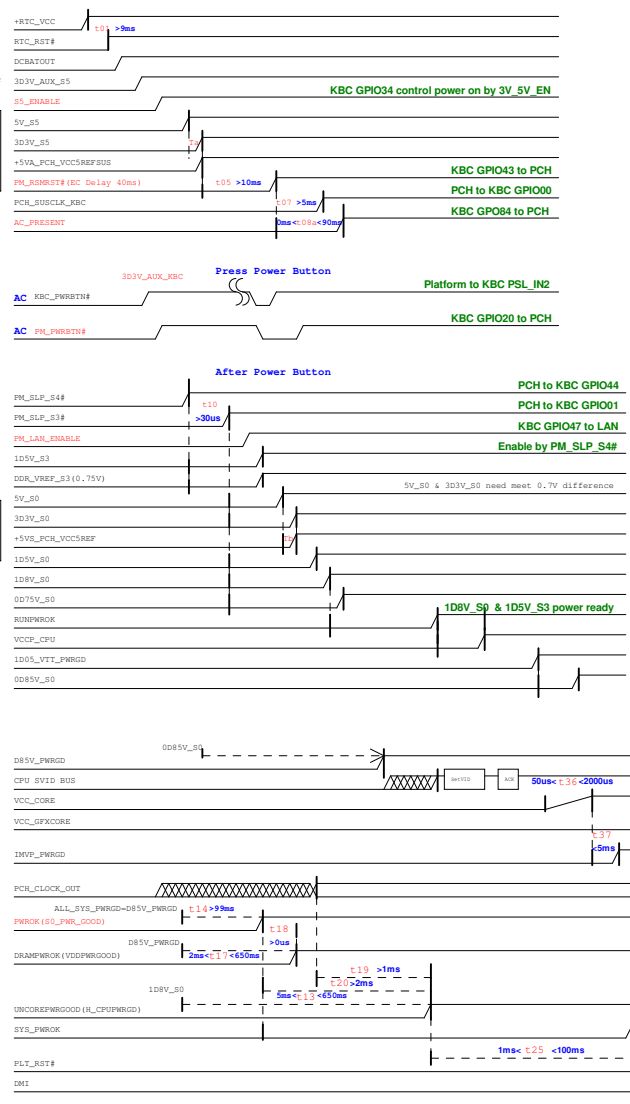
Press the power button status

This signal has an internal pull-up resistor and has no external 1k ohm resistor on the input.

Td

VDDP_0A must be powered up before VDDA_1, or after VDDA_2 within 0.7V. Also, VDDP_0A must power down after VDDA_2, or before VDDA_1 within 0.7V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



(DC mode)

Red Words: Controlled by EC GPIO

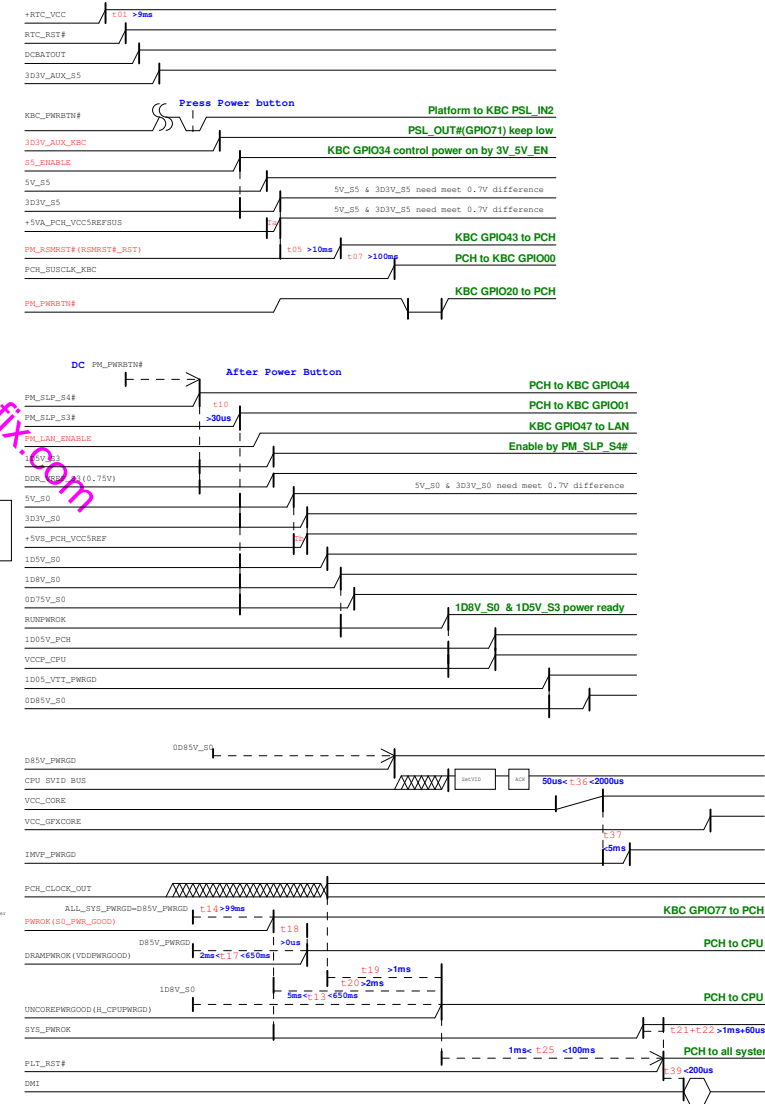
Press the power button status

VDDP_0A must be powered up before VDDA_1, or after VDDA_2 within 0.7V. Also, VDDP_0A must power down after VDDA_2, or before VDDA_1 within 0.7V.

In case of a non-Deep Sleep Platform, please add a 10k pull-up resistor to the PSL_IN2 signal.

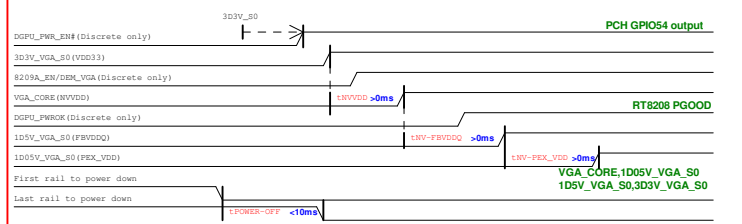
VDDP_0A must be powered up before VDDA_1, or after VDDA_2 within 0.7V. Also, VDDP_0A must power down after VDDA_2, or before VDDA_1 within 0.7V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



www.rosefix.com

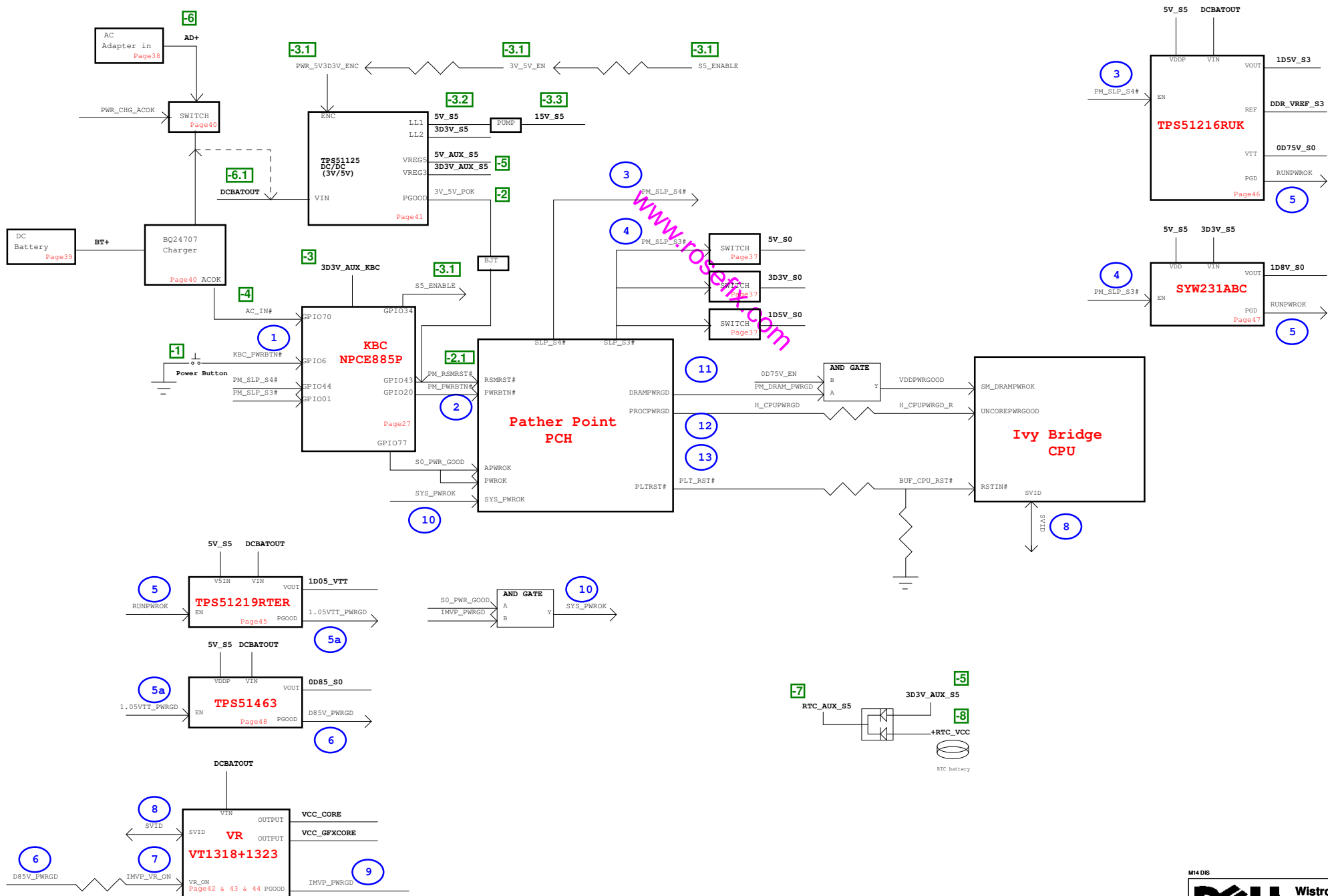
N13M-GS Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

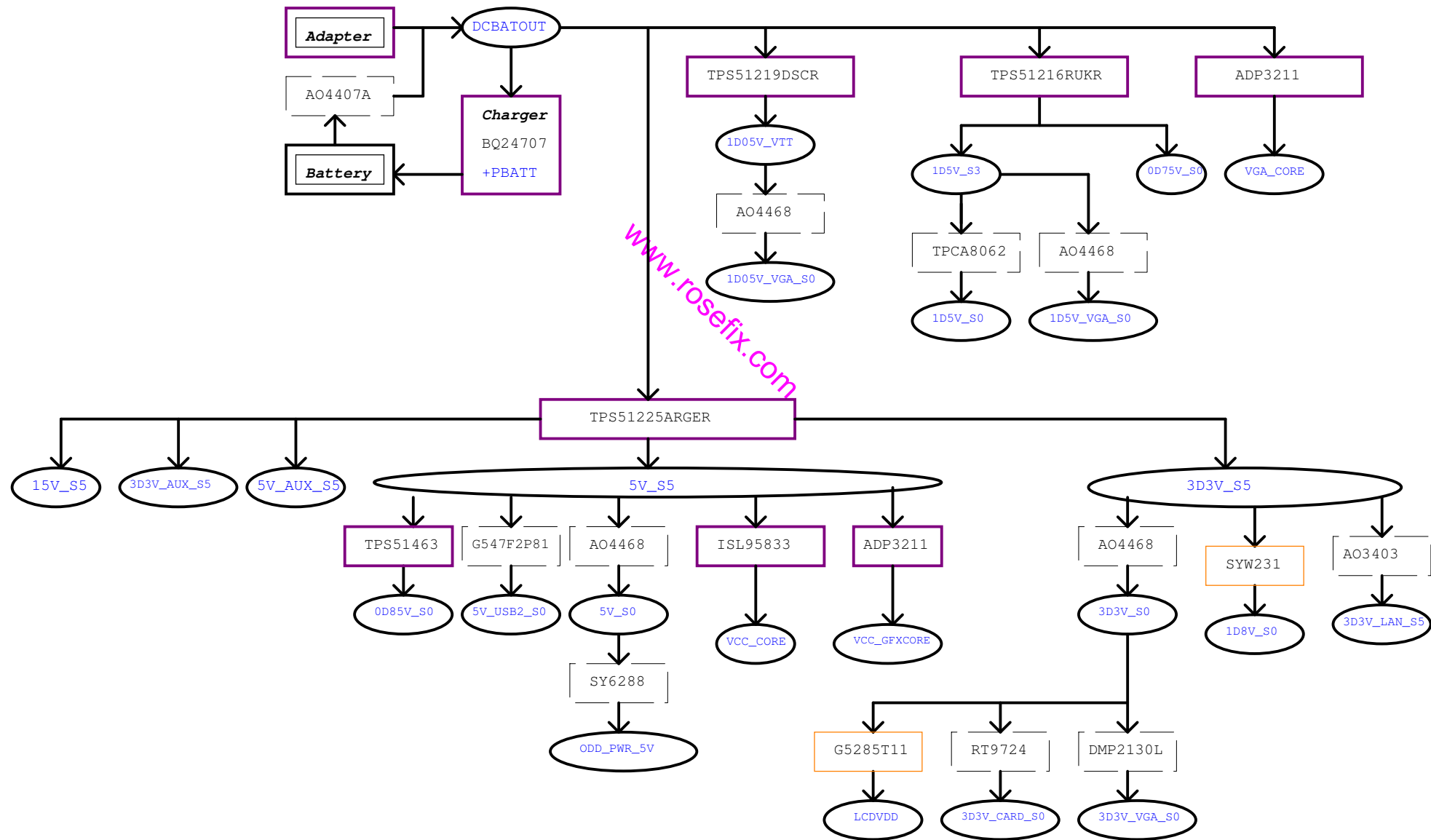
www.rosefix.com

OAK14 Chief River POWER UP SEQUENCE DIAGRAM

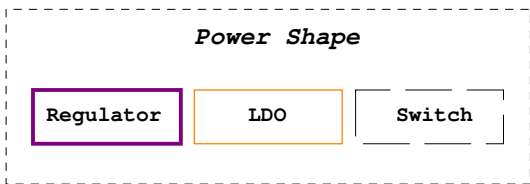


Power Up Sequence: [-8] ~ [13]

h0p05/512806PM



www.rosefix.com



M14 DIS

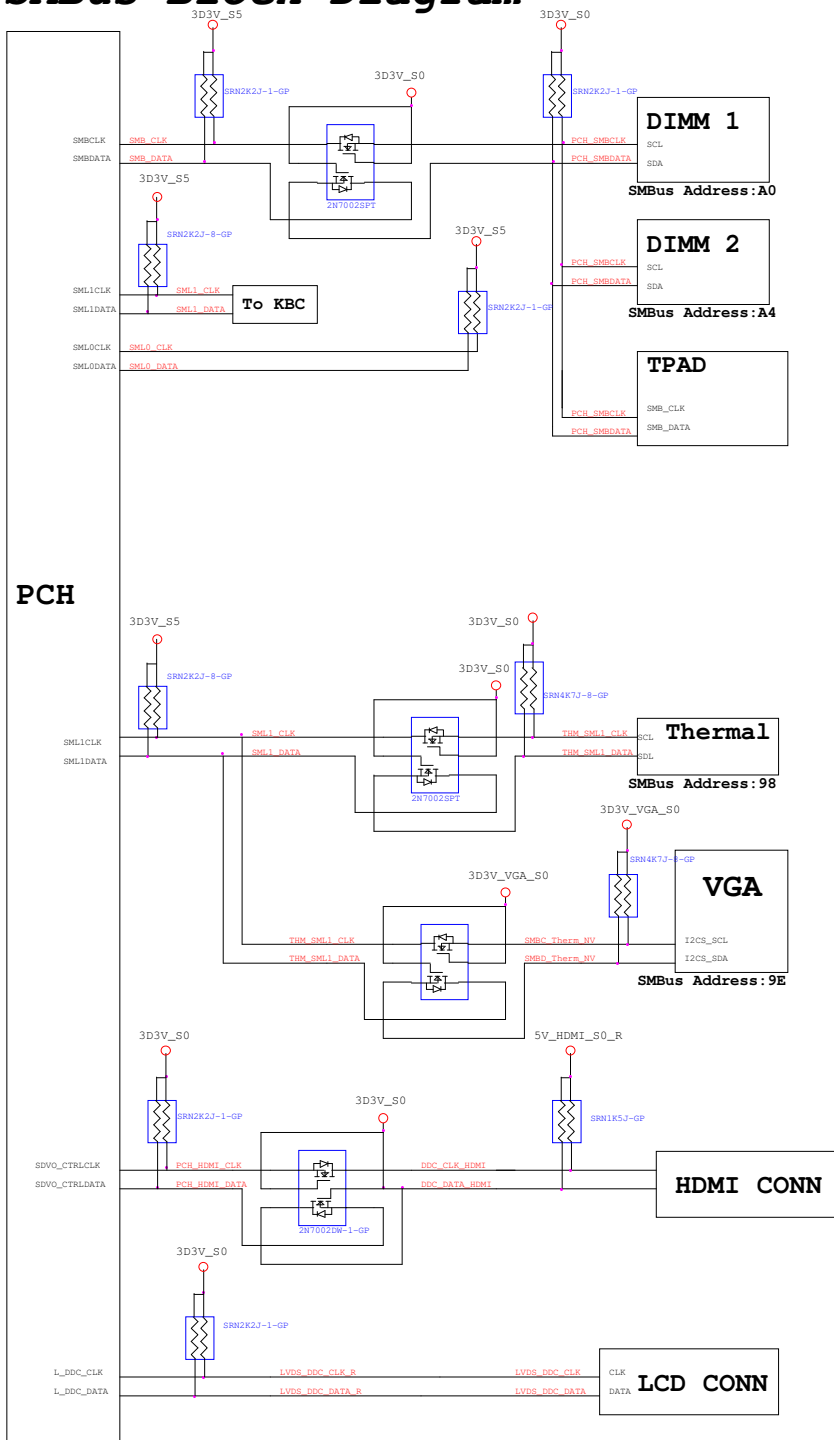
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

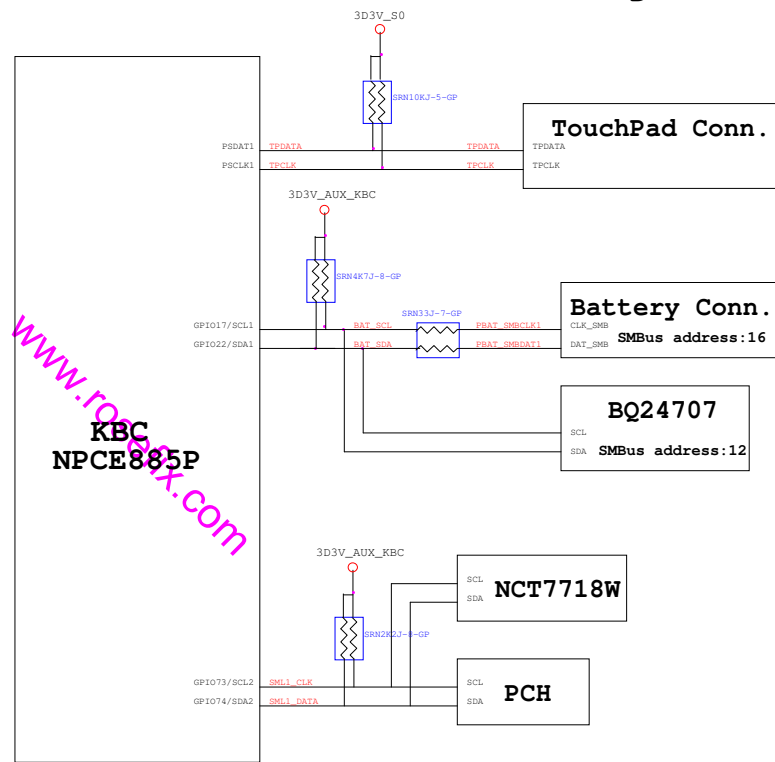
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet: 100 of 105	

h0005/15128/01/11

PCH SMBus Block Diagram



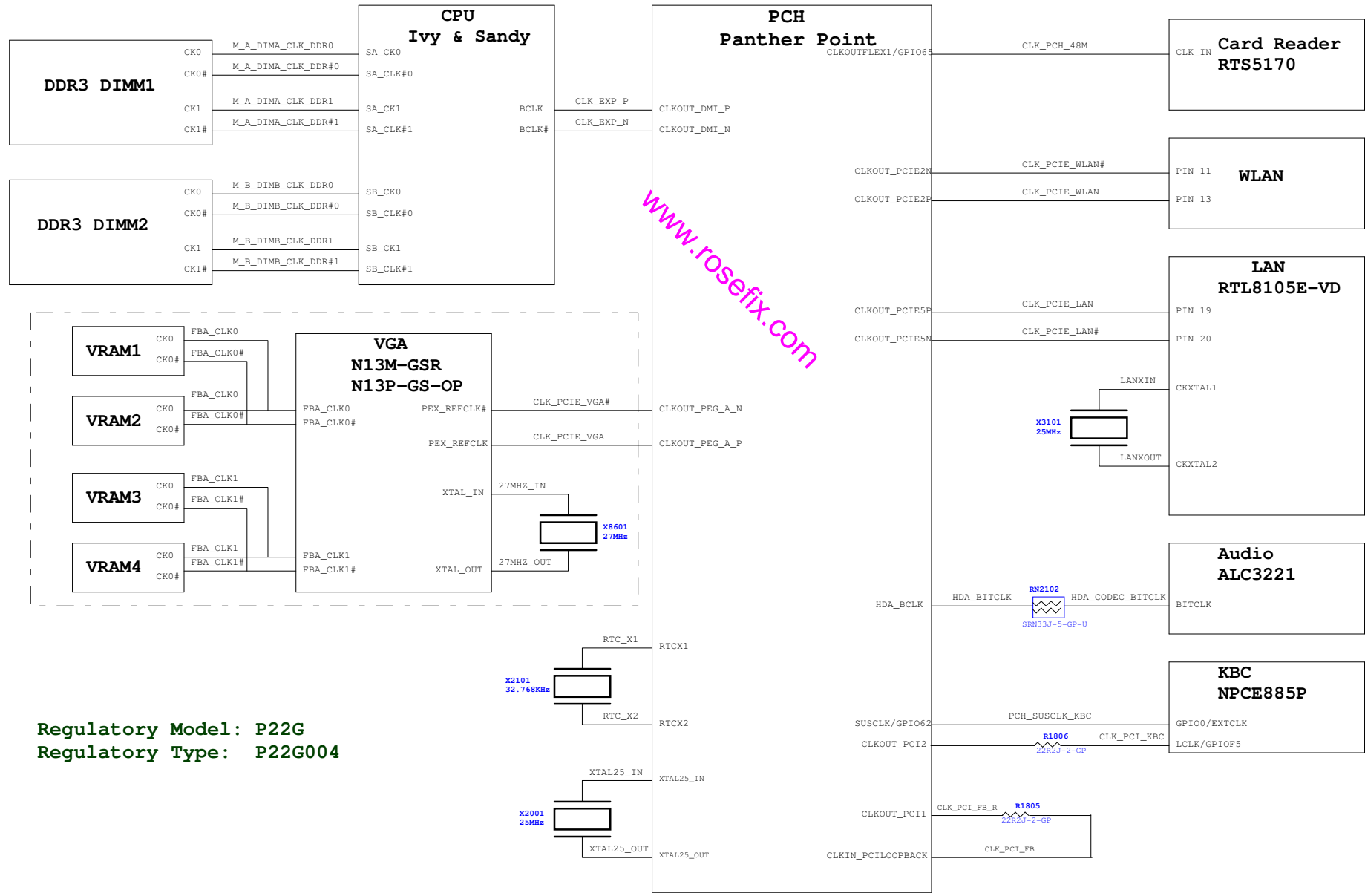
KBC SMBus Block Diagram



www.focustek.com
KBC
NPCE885P

h0p05y5h286bPm

OAK14 DIS CLK Block Diagram

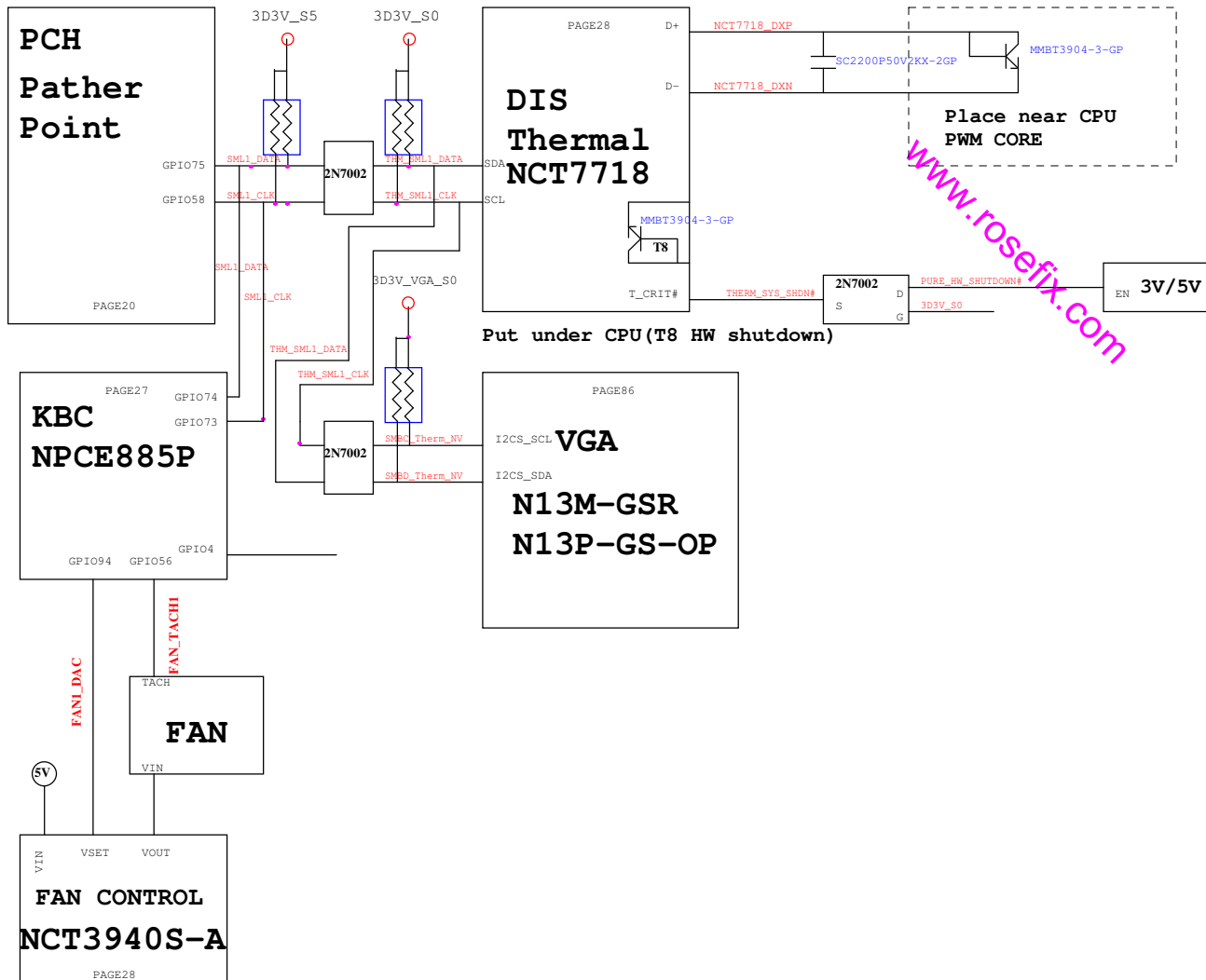


Regulatory Model: P22G
 Regulatory Type: P22G004

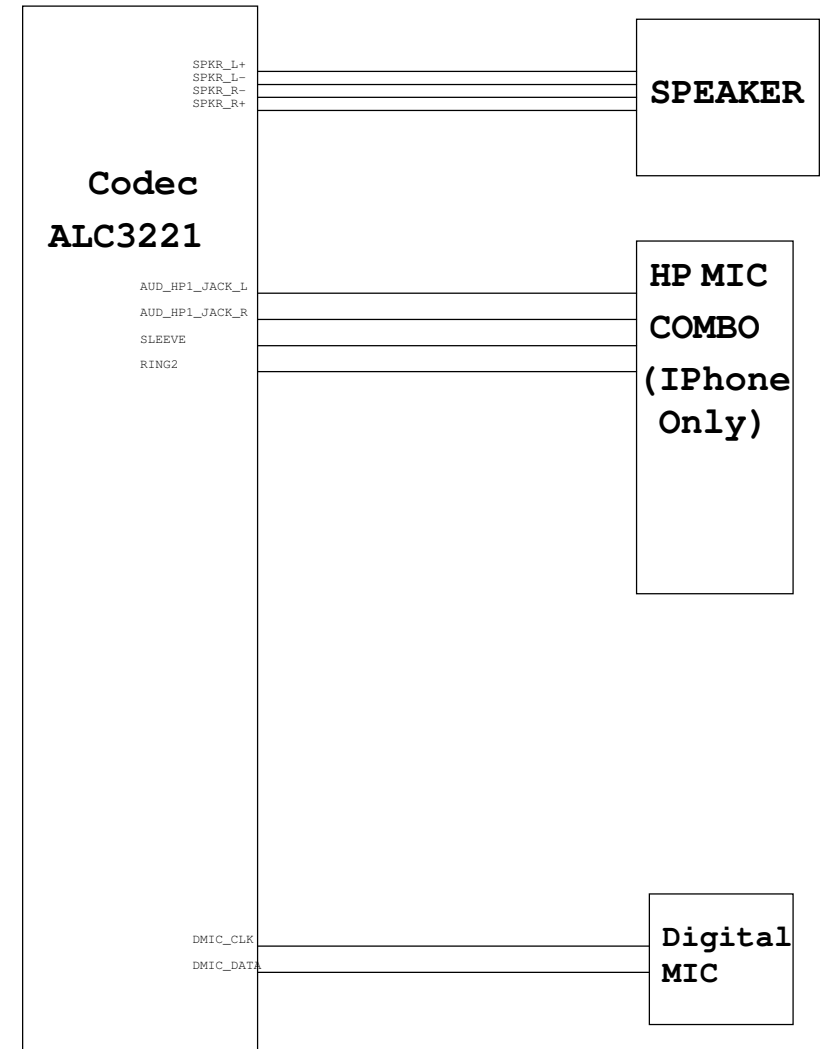
www.rosefix.com

h0p05/15128626PM

Thermal Block Diagram



Audio Block Diagram



http://www.rosefix.com

M14 DIS

Version	Date	PAGE	Description of Required Change
X01	5/10	P38	Dummy R3818 R3813 for DT Mode
X01	5/10	P20	Change CLK_PCIE_WLAN_REQ# PU from 3D3V_S5 to 3D3V_S0 & change port 3 to port 2(non AOAC)
X01	5/10	P86	Dummy R8613 (for N13M-GS1 strappin)
X01	5/28		Update connector list(5/28) for X01
X01	5/30	P49	Add TPNL1 (USB20 port#3)
X01	5/30	P29	Add delay circuit for Audio Jack JD pin
X01	5/30	P59	Change RJ45 Conn
X01	6/1	P38	Stuff PQ3801 PR3814 PR3815 for DT mode
X01	6/1	P37	Change R3713 to 10k for sequence timing
X01	6/1	P31	Change R3118 to 20k for sequence timing
X01	6/1	P69	Add KBL1 and keyboard backlight function
X01	6/1	P27	Change PCB version from X00 to X01
X01	6/5	P46	Fine tune the level of 1d5v_vga_s0: PR4601 (47K -> 57.6K)
X01	6/5	P58	Add TVS at combo JACK & RJ45 for EMI request
X01	6/5	P18	Move the KB_LED_BL_DET from GPIO5 to GPIO4
X01	6/11		Implement EMI change request 6/11
X01	6/11	P27	Delete RN2702 , DY R2716, Stuff R2717 For DT Mode
X01	6/11	P21	Add VRAM detect circuit at PCH_GPIO57
X01	6/11	P51	Change D5101 to 83.00056.G11 for lower internal cap
X01	6/12	P18	Move USB2.0 from port4# to port2#
X01	6/12	P49	Modify CAMERA1 to CAM1
X01	6/13	P61	Separate the USB3.0 PWR to USB30_VCCA & USB30_VCCB
X01	6/14	P49	Add LCD Back Light control circuit from KBC GPIO33
X01	6/14	P40	implement Power team request item
X01	6/15	P31	Change C3102=C3103=18pf for Xtal vendor request
X01	6/15	P62	Modify cap value for USB30_VCCA & USB30_VCCB
X01	6/18	P69	DY the Keyboard back light parts, add R6916 for PU
X01	6/18	P61	Change TC6102 & TC6104 to 78.10710.52L; TC6103 to 79.10710.60L
X01	6/18	P20	Move WLAN from PCIE 4# to PCIE 3#
X01	6/18	P51	implement EMI team request item (6/15)
X01	6/18	P69	Remove R6916 Stuff R6912
X01	6/18	P69	Change Q6801~Q6805 & Q6902 to 84.00144.P11

www.rosefix.com

M14 DIS



Title			Change History		
Size	Document Number	Rev			
A3	OAK14 Chief River DIS	A00			
Date:	Wednesday, September 05, 2012	Sheet	104	of	105

h0005y1512806P.M

