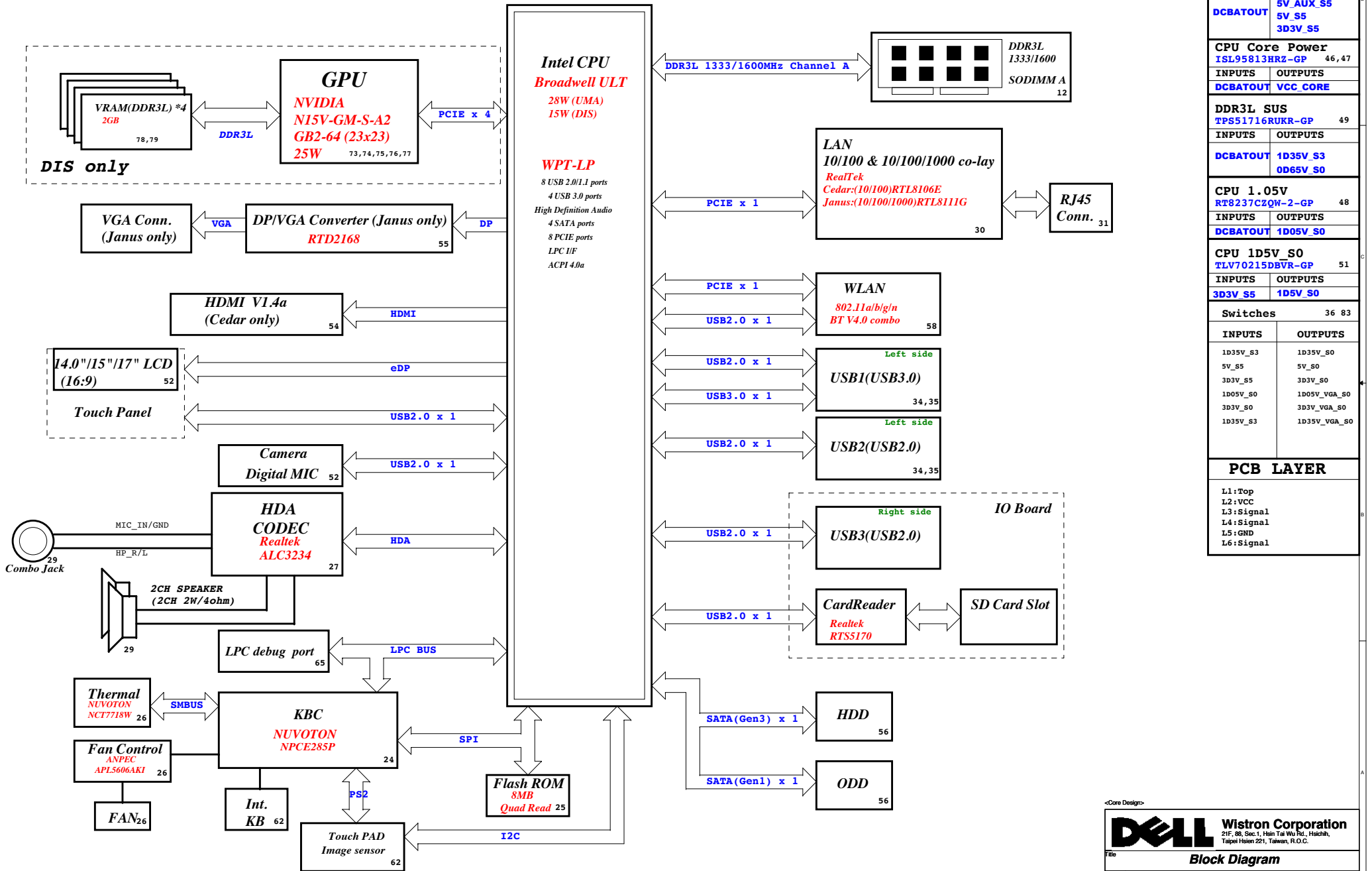


Project code:4PD00I010001
 PCB P/N: 13302-1
 Revision: A00

Cedar/Janus Block Diagram



CHARGER	
HPA02224RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HR2-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
RT8237CZQW-2-GP 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1D5V_S0	
TLV70215DBVR-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Signal	

(Blanking)

<Core Design>



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Title

(Reserved)

Size
A4

Document Number

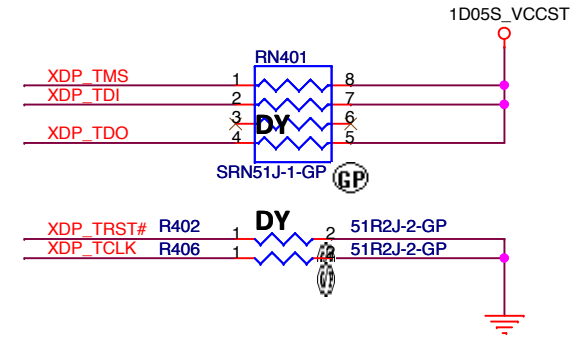
Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

Sheet 3 of 104

SSID = CPU



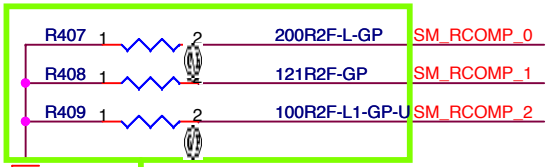
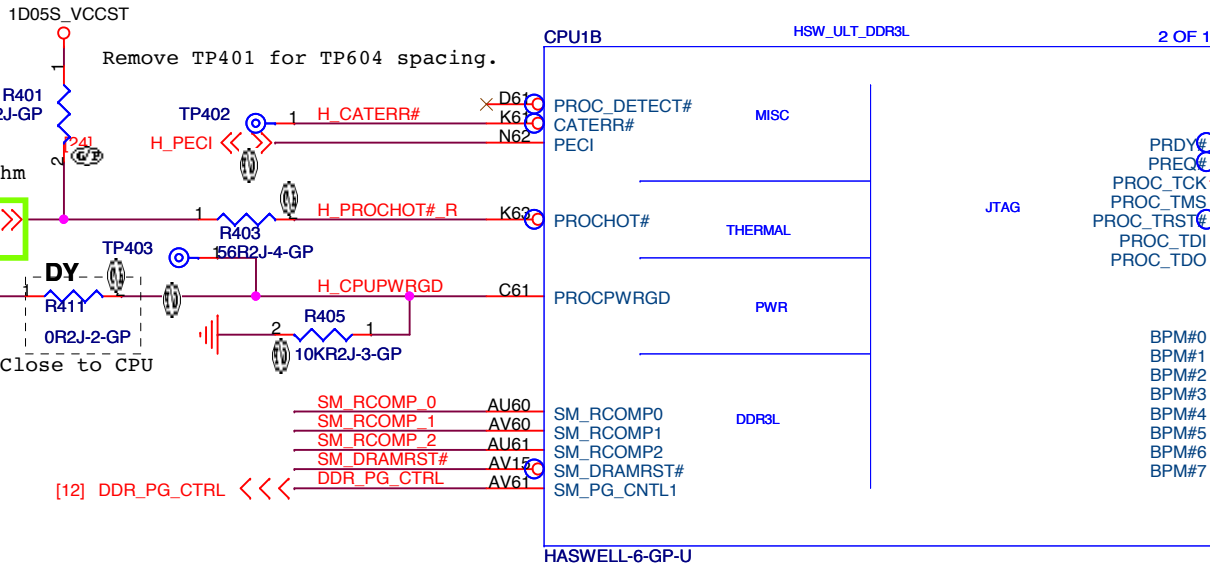
Layout Note:

Impedance control: 50 ohm

[24,42,44,46] H_PROCHOT# <<<>>

[36] H_THERMTRIP_EN <<<<

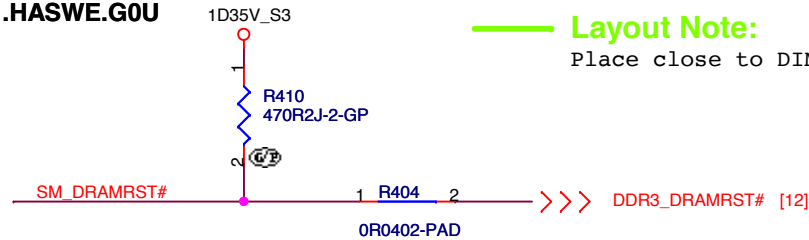
Layout Note: Close to CPU



Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

71.HASWE.G0U



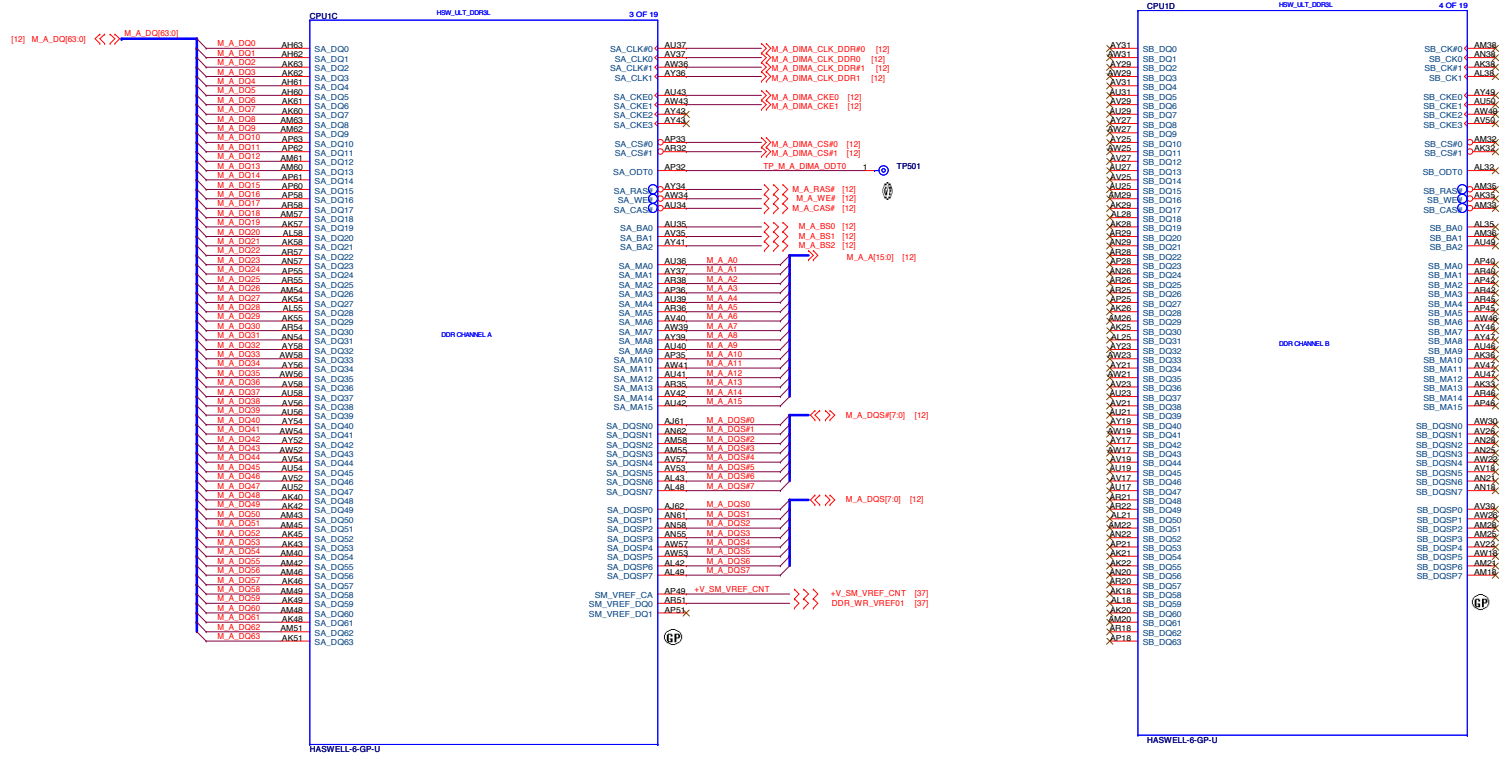
Layout Note:

Place close to DIMM

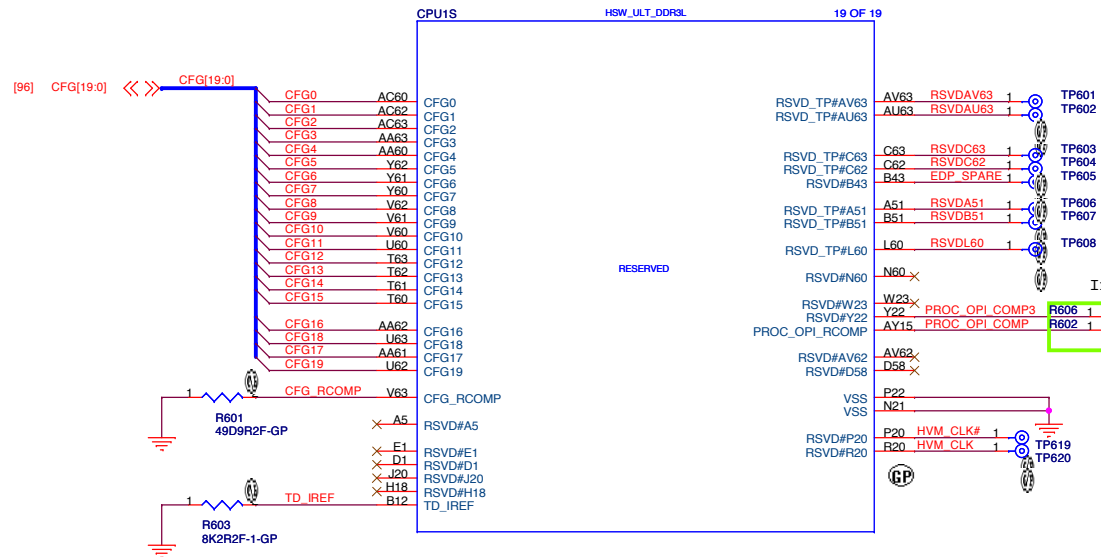
<Core Design>

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Title			
CPU (THERMAL/MISC/PM)			
Size	Document Number	Rev	
A4		Janus HSW 40/50/70	
Date: Friday, February 07, 2014		Sheet 4	of 104

DDR3L ball type: Non-Interleaved Type



SSID = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

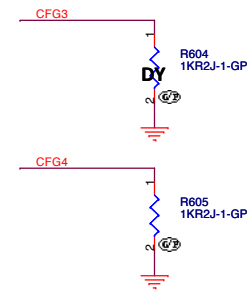
- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • CFG[3]: MSR Privacy Bit Feature <ul style="list-style-type: none"> - 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting - 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • CFG[4]: eDP enable <ul style="list-style-type: none"> - 1 = Disabled - 0 = Enabled • CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lanes. 	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>

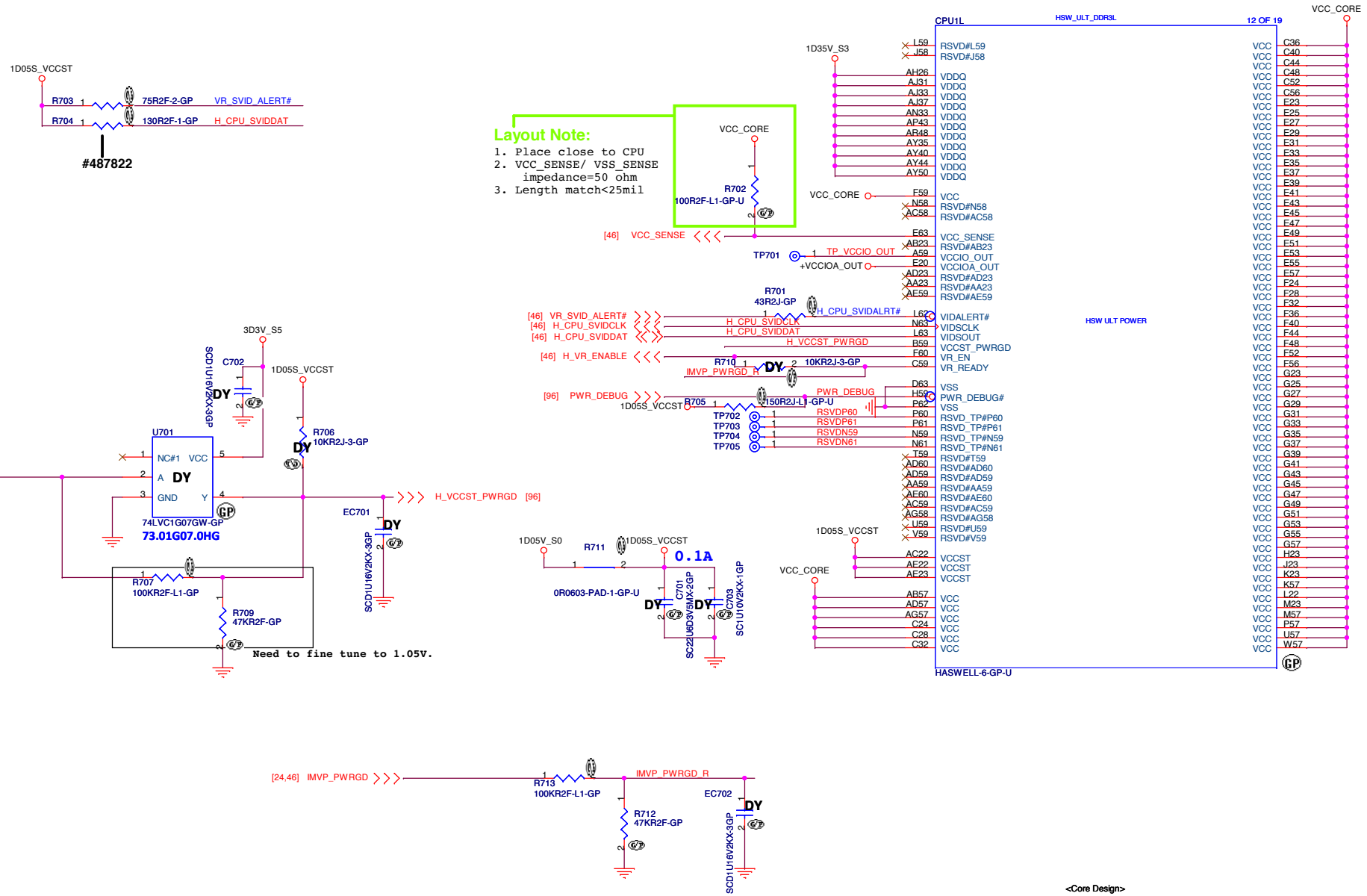
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CFG)**

Size A3 Document Number: **Janus HSW 40/50/70** Rev **A00**

Date: Friday, February 07, 2014 Sheet 6 of 104

SSID = CPU



<Core Design>

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Title: **CPU (VCC CORE)**

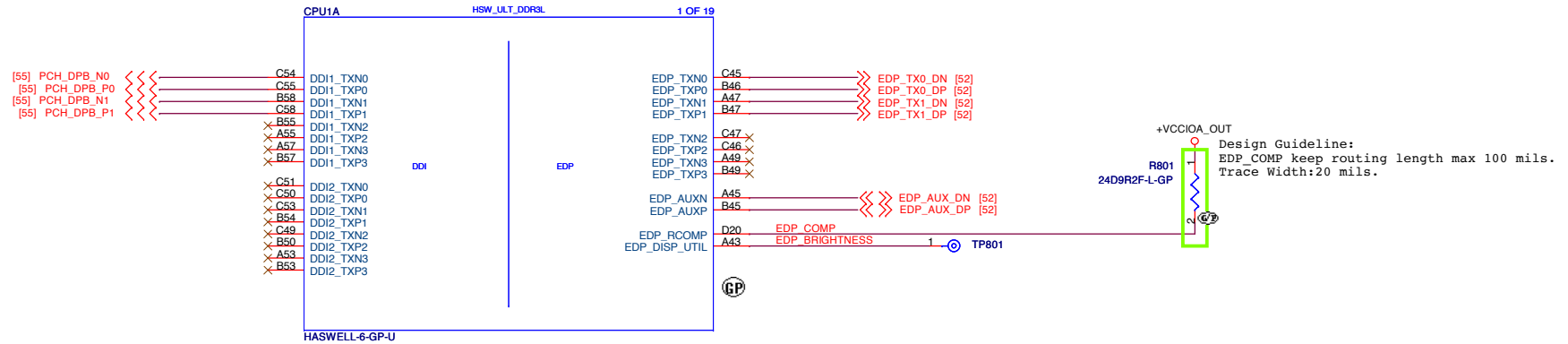
Size A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

Date: Friday, February 07, 2014 Sheet 7 of 104

SSID = CPU

www.vinafix.vn

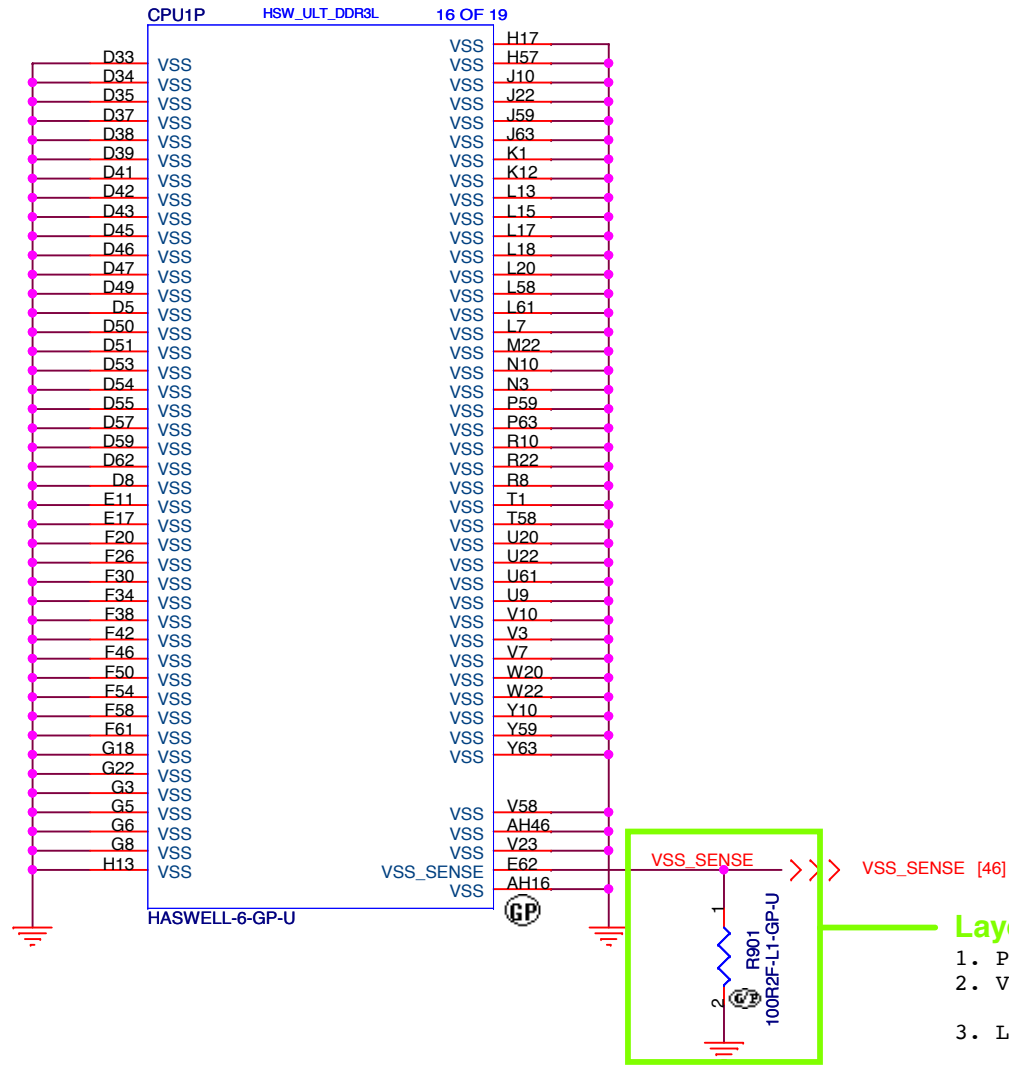
DP to VGA Converter



<Core Design>

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Title			
CPU (DDI/EDP)			
Size	Document Number	Rev	
A3	Janus HSW 40/50/70	X02	
Date:	Friday, February 07, 2014	Sheet	8 of 104

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title

CPU (VSS)

Size
A4

Document Number

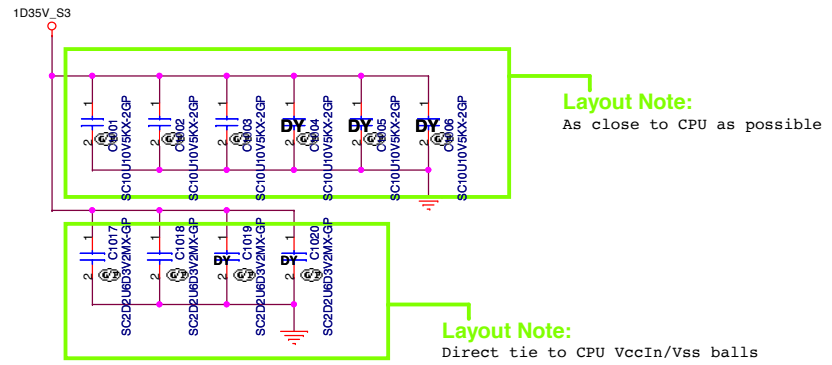
Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

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SSID = CPU



<Core Design>

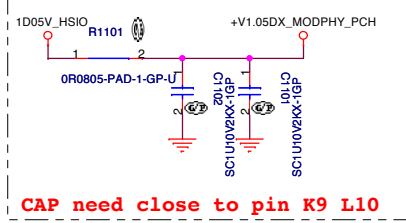
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (Power CAP1)**

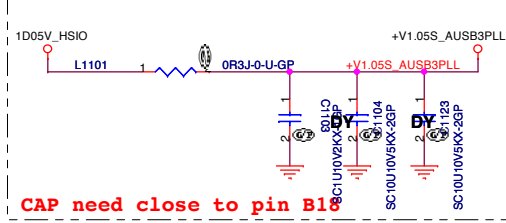
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet: 10	of 104

MAX: 1.92A

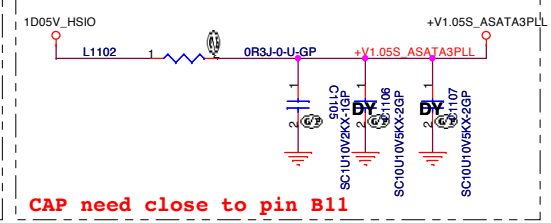
1.838A



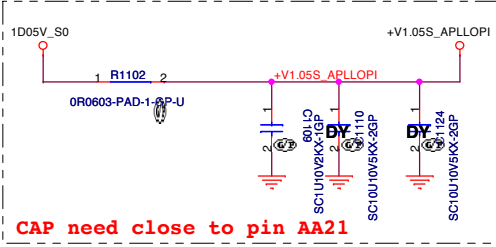
41mA



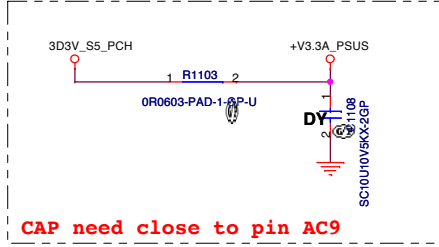
42mA



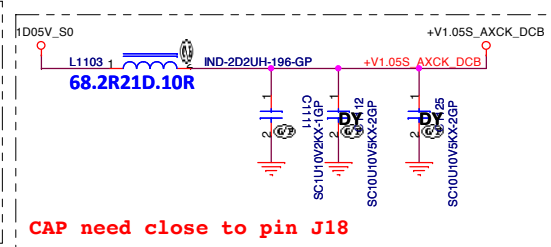
57mA



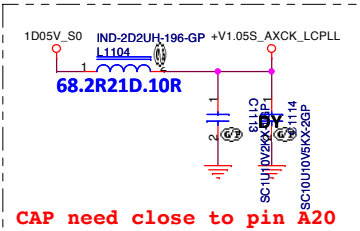
62mA



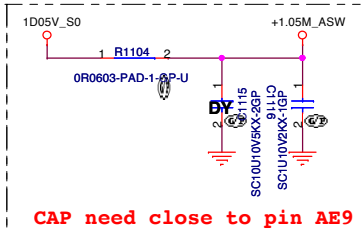
185mA



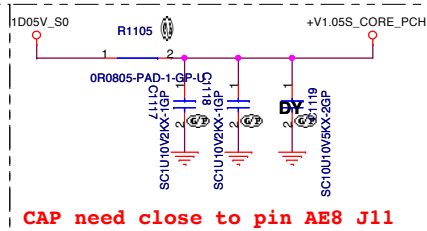
31mA



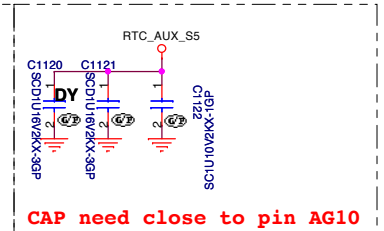
658mA




1.632A



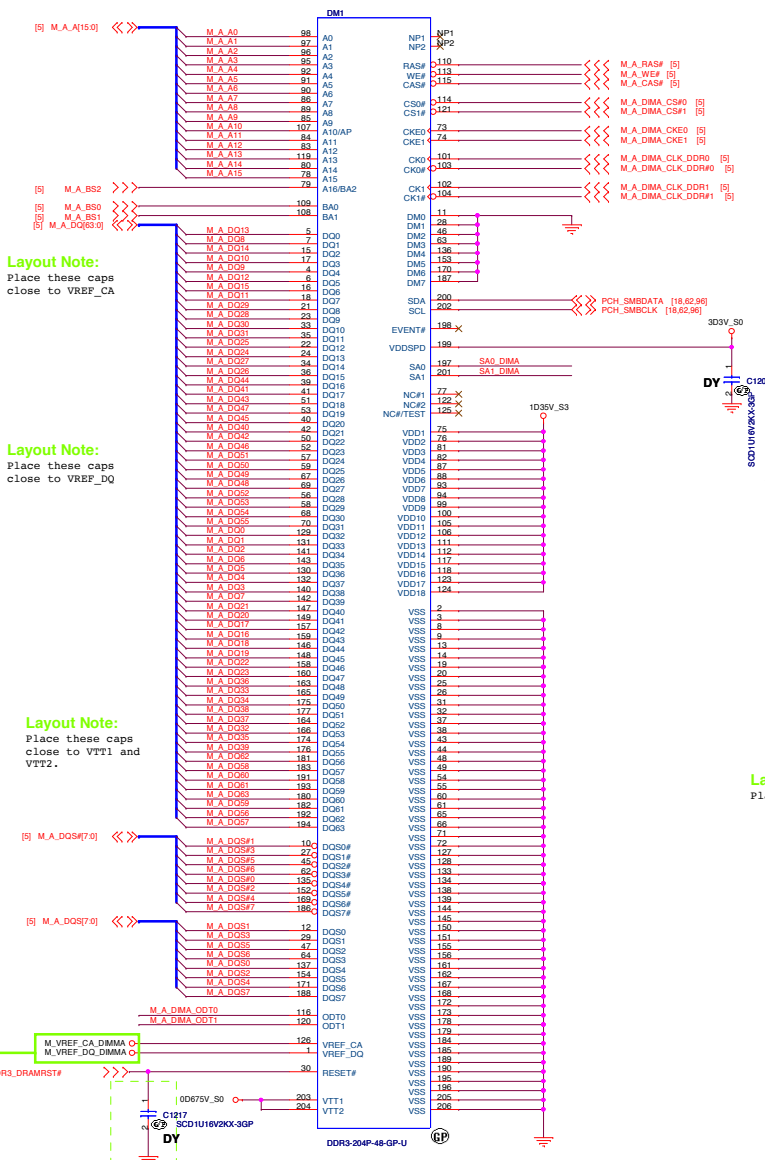
1mA



<Core Design>

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Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet: 11	of: 104

SSID = MEMORY



Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

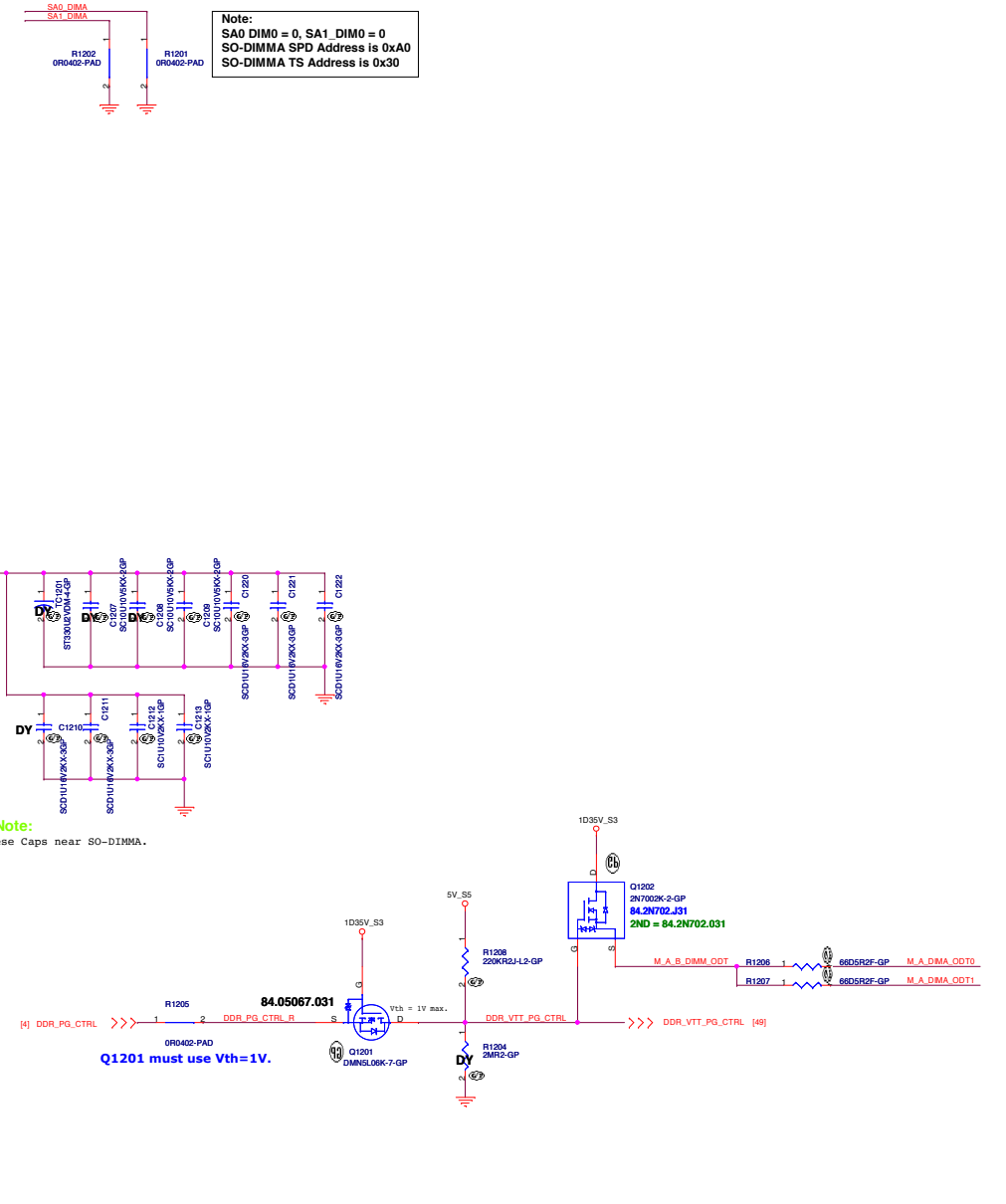
Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Note:
SA0 DIM0 = 0, SA1 DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30


Layout Note:
Place these Caps near SO-DIMMA.

Q1201 must use Vth=1V.



(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)DDR3-SODIMM2		
Size A3	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 13	of 104

5

4

3

2

1

D

D

C

C

B

B

A

A

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title **(Reserved)_SODIMM_SODIMM4**

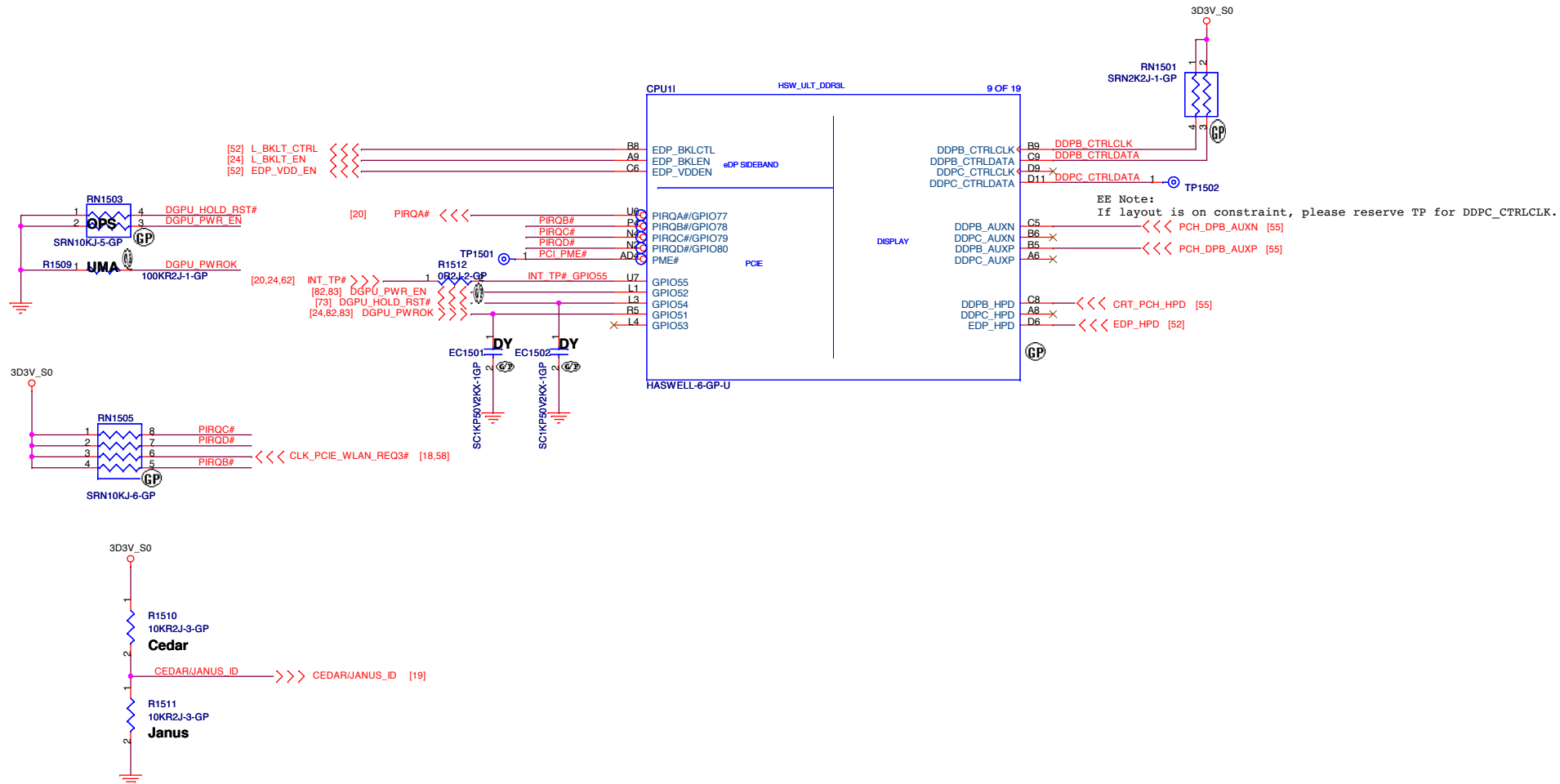
Size A4	Document Number Janus HSW 40/50/70	Rev A00
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SSID = CPU

PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	Low = Disable Port B (default) * High = Enable Port B
DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts

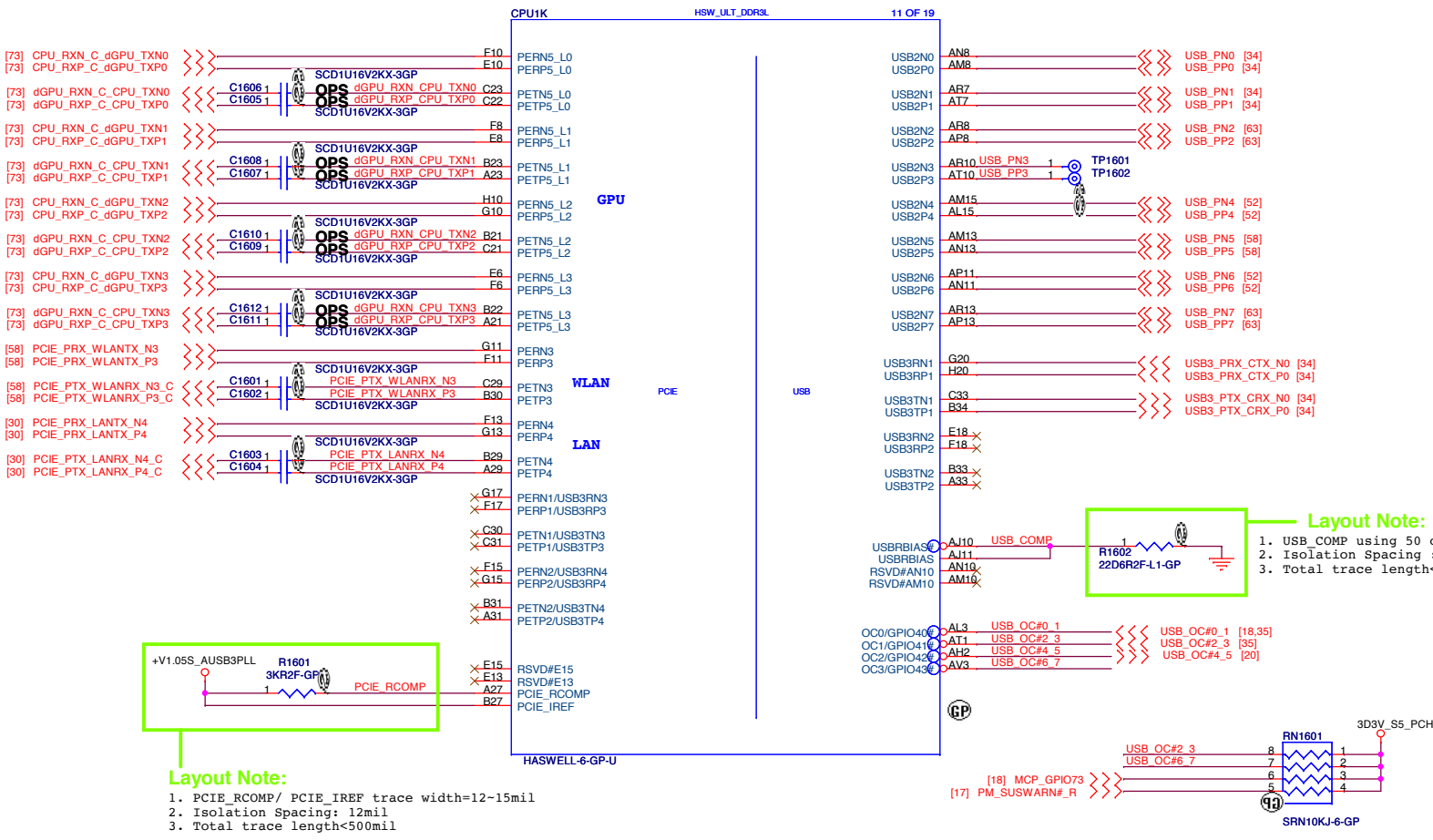


EE Note:
If layout is on constraint, please reserve TP for DDPC_CTRLCLK.

<Core Design>

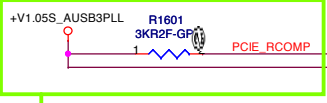
			Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title PCH (EDP/GPIO/DDI)			
Size A3	Document Number Janus HSW 40/50/70	Rev X02	
Date: Friday, February 07, 2014	Sheet 15	of 104	

SSID = PCH



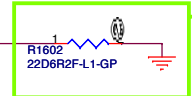
USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12-15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0-L1)	N/A	

#515621
Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD		

<Core Design>

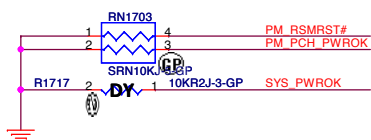
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Title: **PCH (PCIE/USB)**

Size: A3 | Document Number: **Janus HSW 40/50/70** | Rev: **A00**

Date: Friday, February 07, 2014 | Sheet: 16 of 104

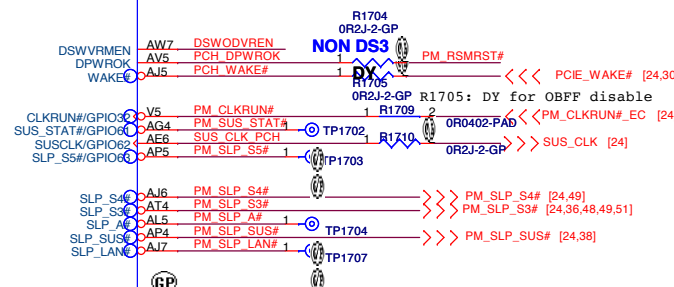
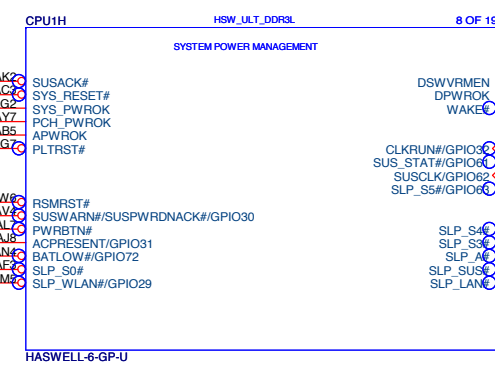
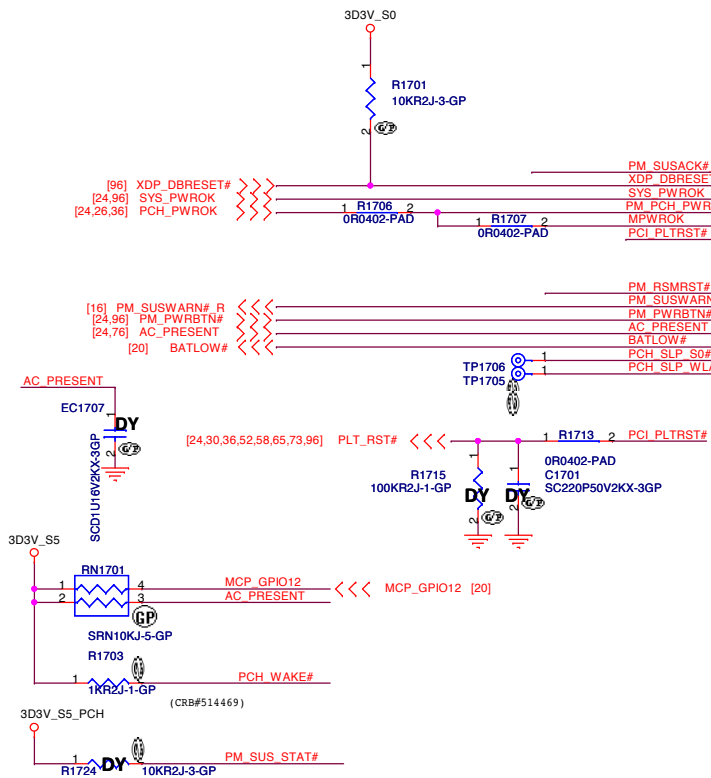
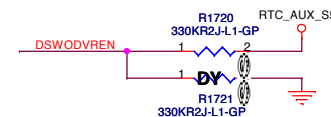
SSID = PCH



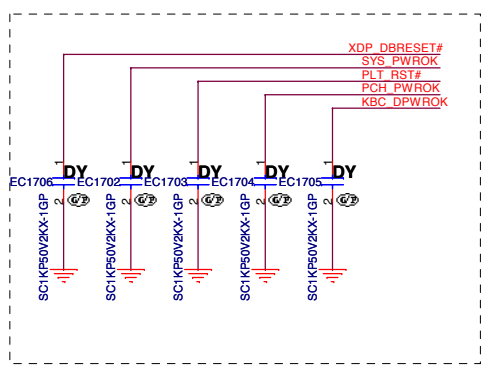
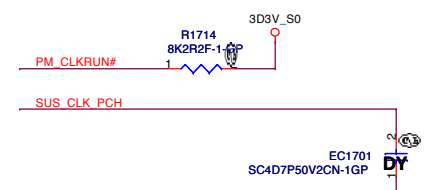
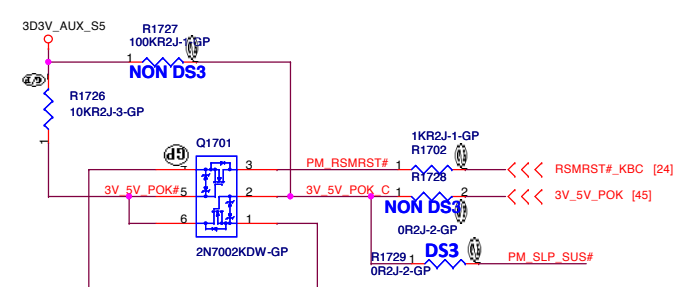
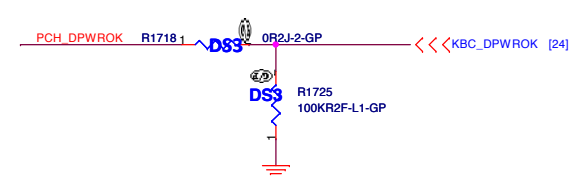
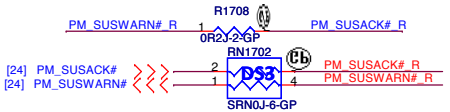
PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default) *

This signal has no integrated pull-up/pull-down.



NON DS3



84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

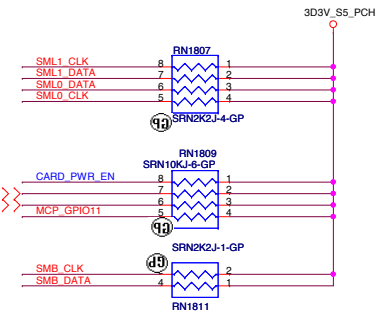
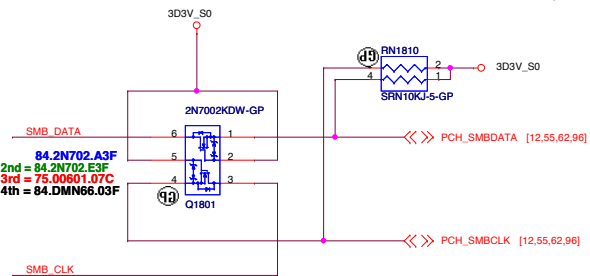
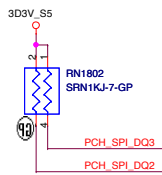
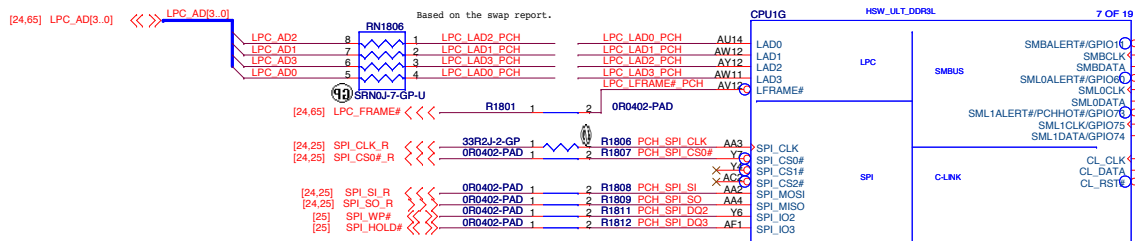
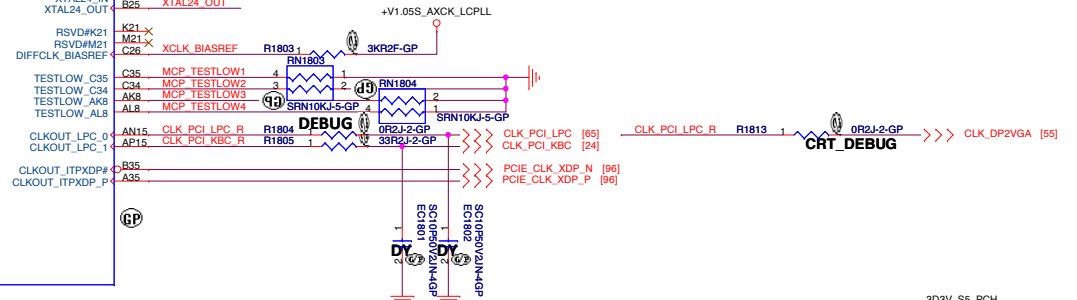
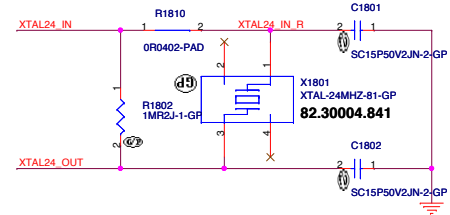
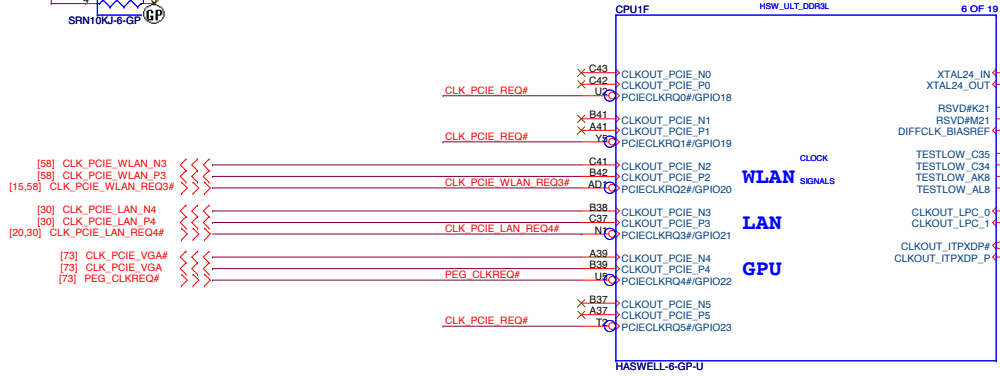
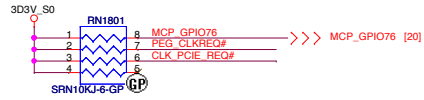
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Title: **PCH (PM)**

Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet: 17	of: 104

SSID = PCH



<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

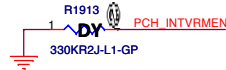
Title: **PCH (CLOCK/SMBUS/CL/LPC/SPI)**
 Size: Custom Document Number
 Date: Friday, February 07, 2014

Rev: **X02**
 Janus HSW 40/50/70
 Sheet 18 of 104

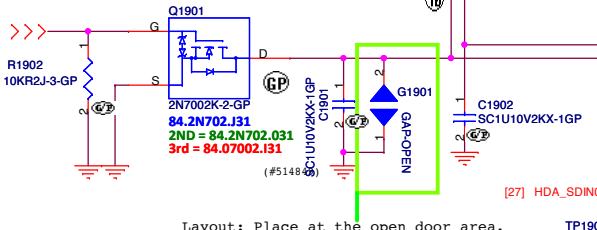
SSID = CPU

PCH strap pin:

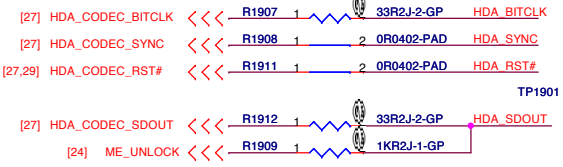
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*



[24] RTCRST_ON >>>



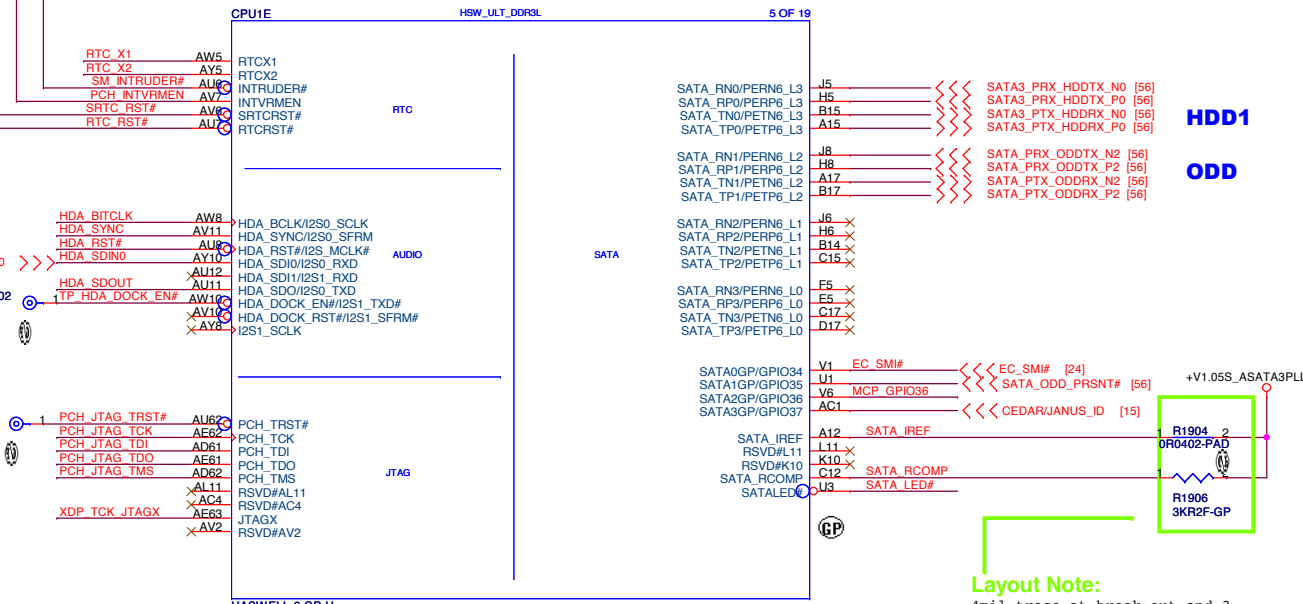
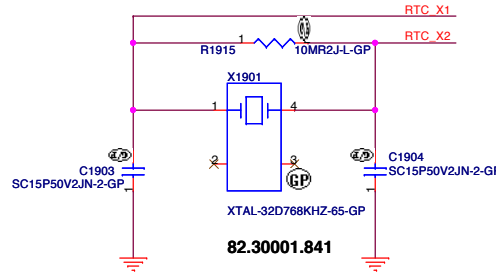
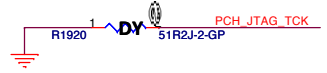
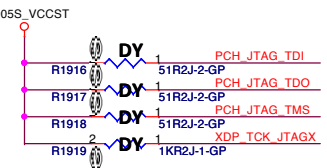
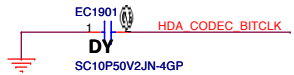
Layout: Place at the open door area.



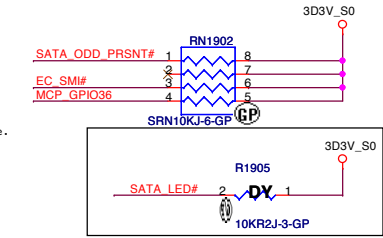
PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.



Unused SATA[13:0] pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

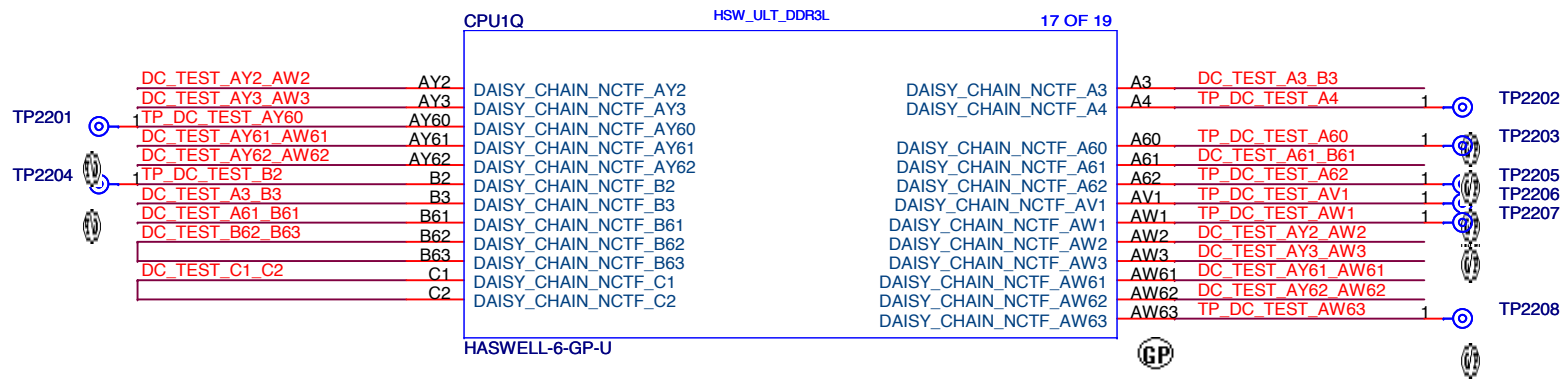
<Core Design>

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Title: **PCH (RTC/SATA/HDA/JTAG)**

Size A3	Document Number	Rev A00
Date: Friday, February 07, 2014	Sheet 19 of 104	

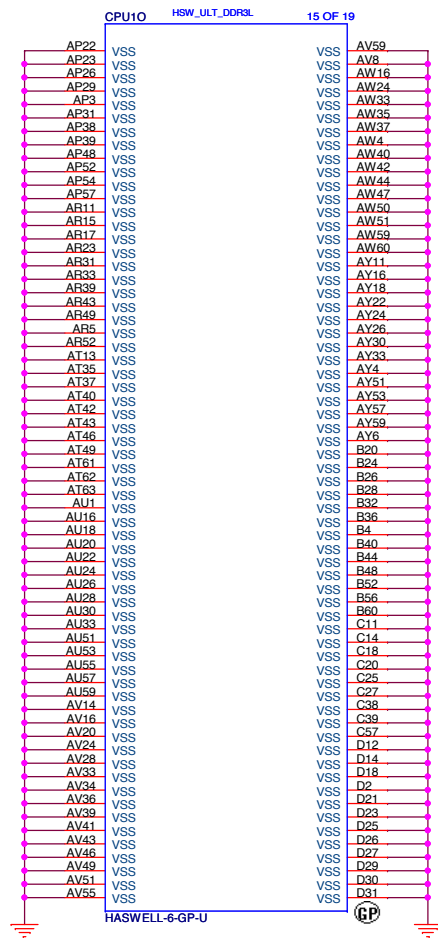
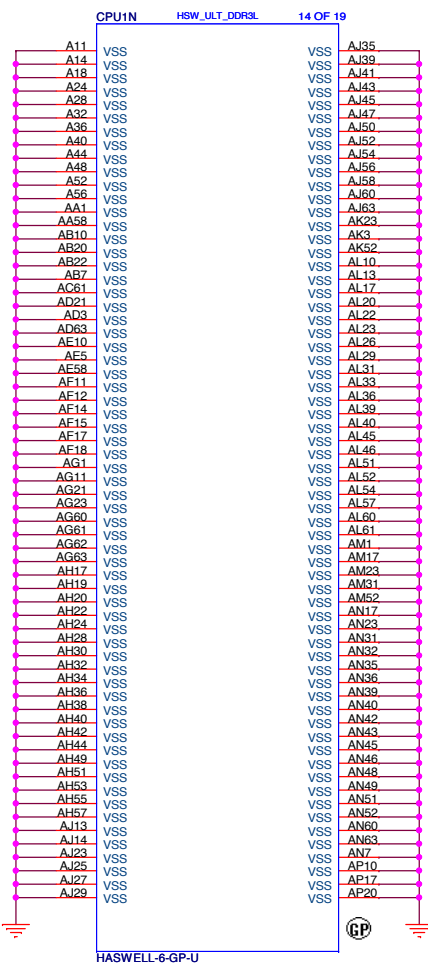
SSID = PCH



<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number	Rev	
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SSID = PCH



<Core Design>

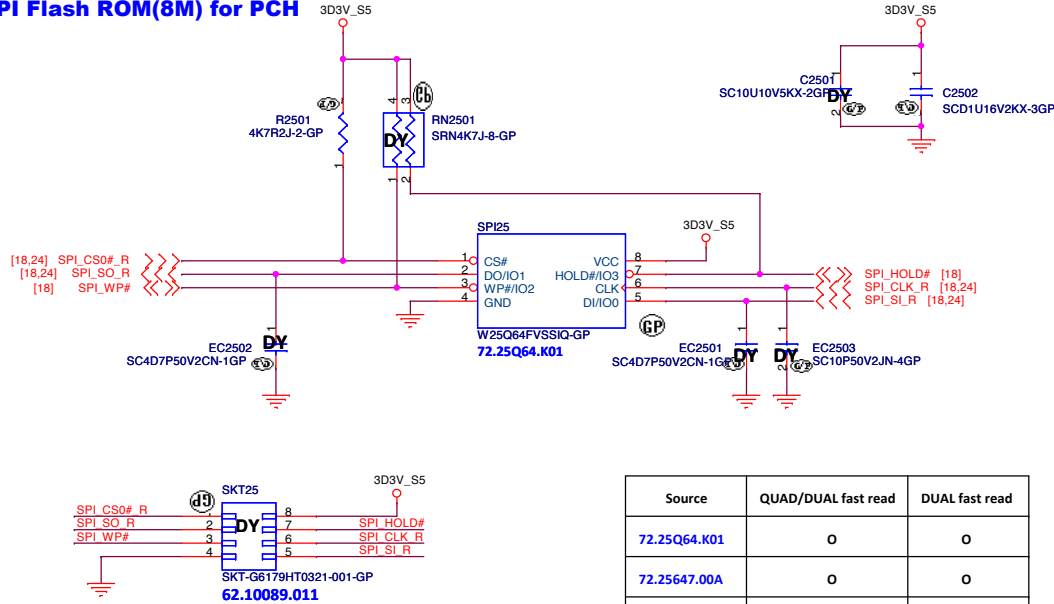
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU(VSS)

Size A3	Document Number Janus HSW 40/50/70	Rev A00
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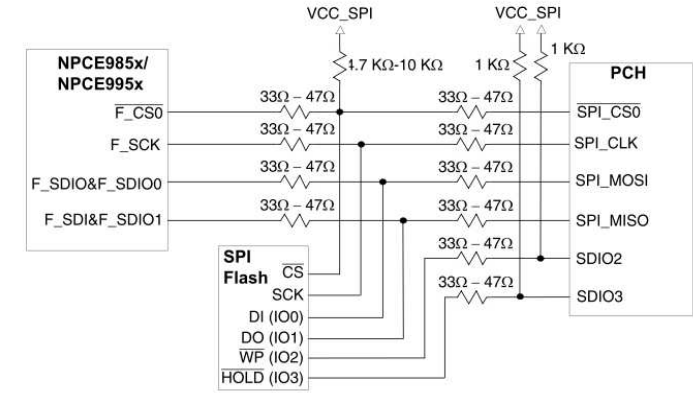
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



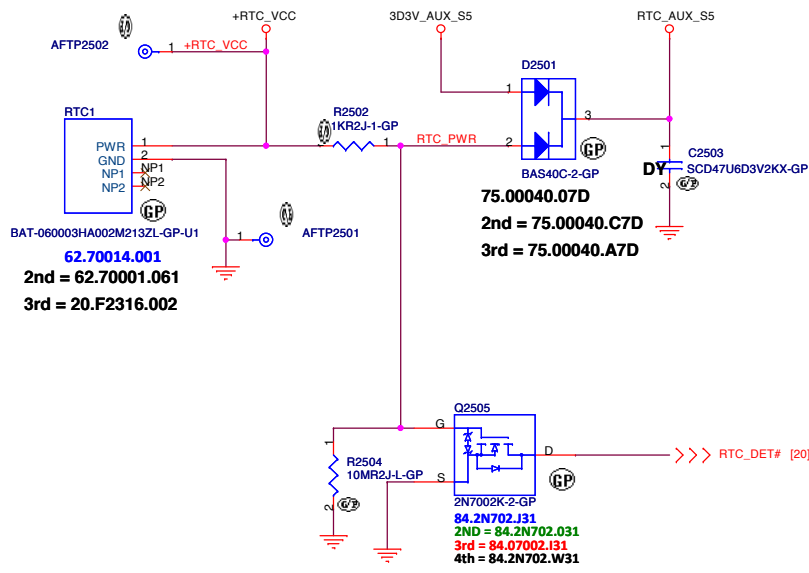
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



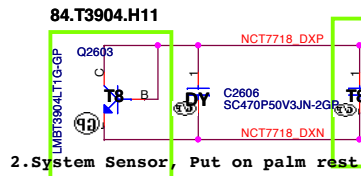
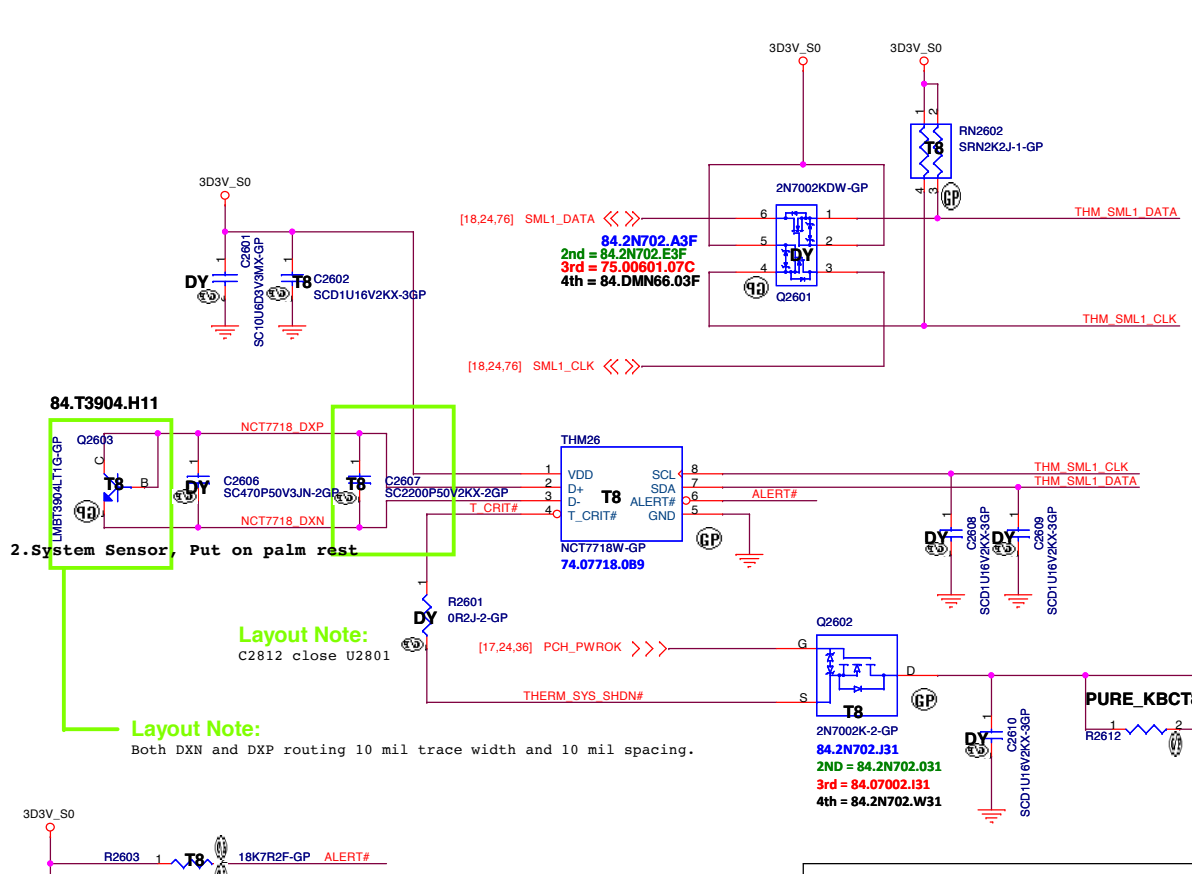
<Core Design>

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Title: **Flash/RTC**

Size A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

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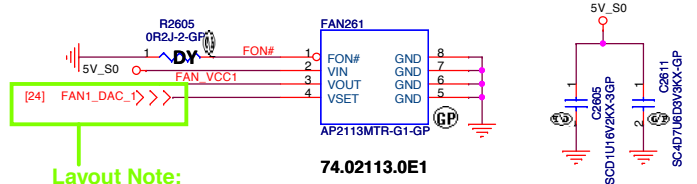


Layout Note:
C2812 close U2801

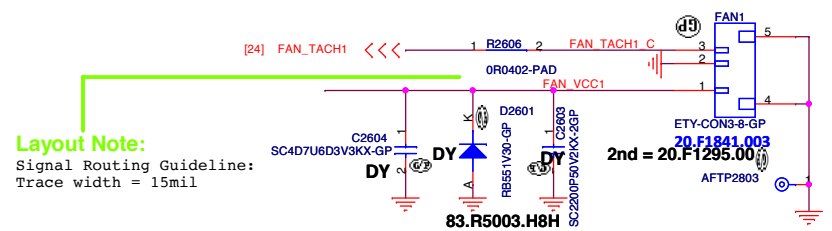
Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

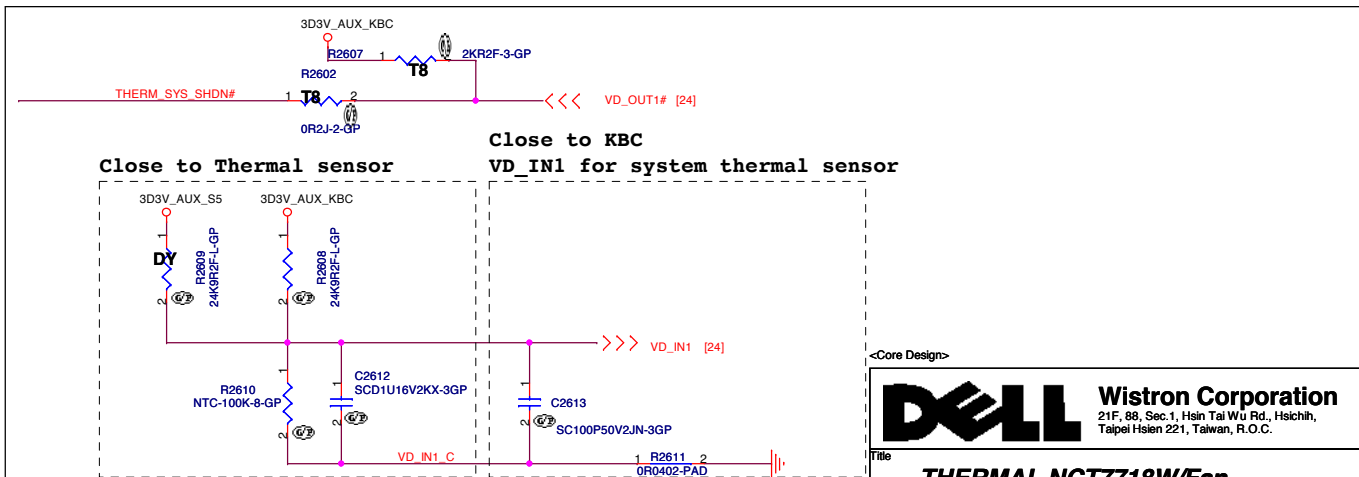
Fan controller1



Layout Note:
Need 10 mil trace width.



Layout Note:
Signal Routing Guideline:
Trace width = 15mil



Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor

<Core Design>

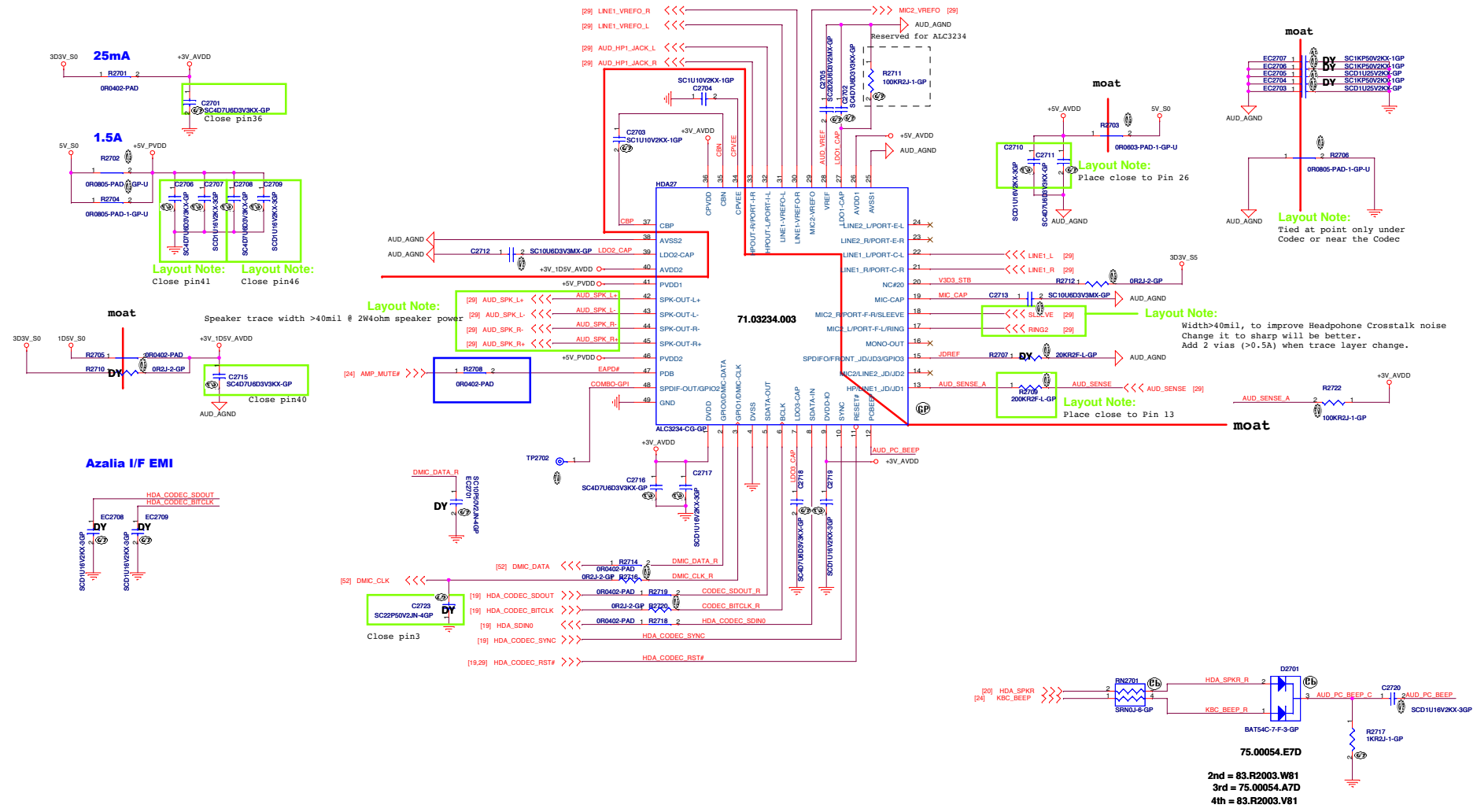
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Title: **THERMAL NCT7718W/Fan**

Size: A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

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SSID = AUDIO



75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
4th = 83.R2003.V81

(Blanking)

<Core Design>



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Title

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Size
A4

Document Number

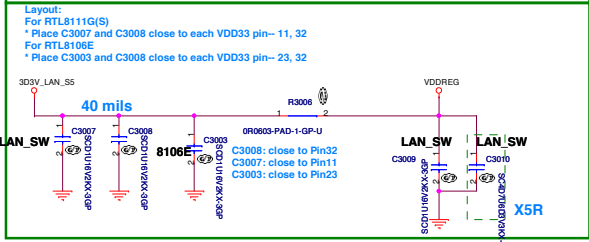
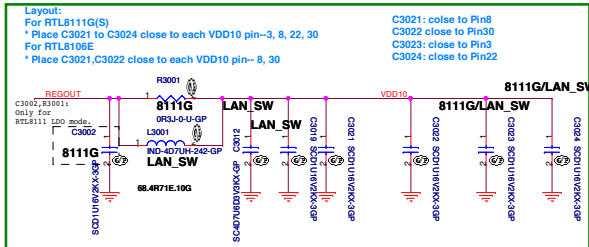
Janus HSW 40/50/70

Rev
A00

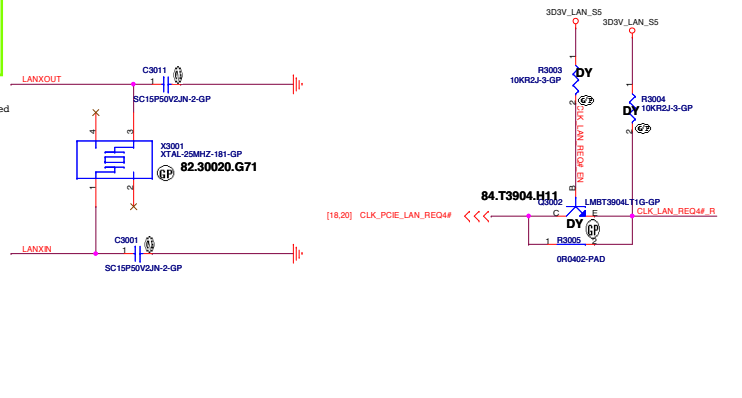
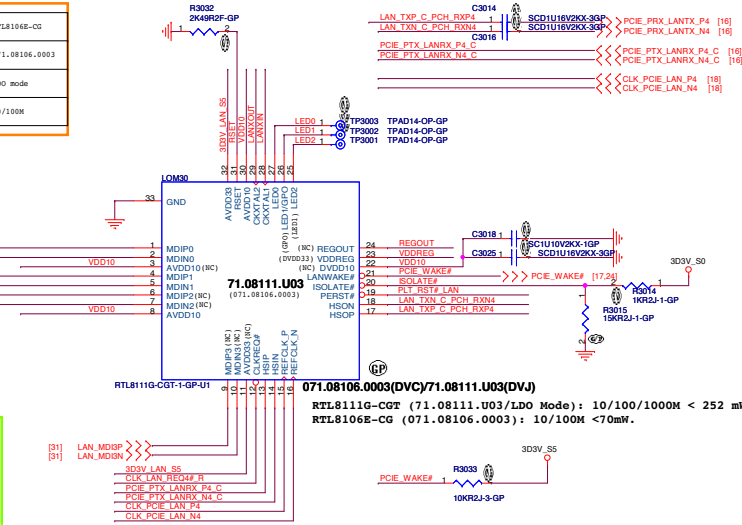
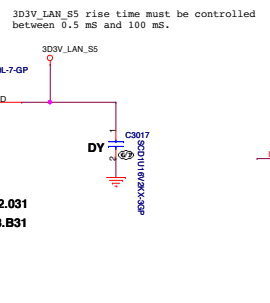
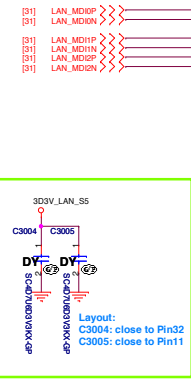
Date: Friday, February 07, 2014

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LAN CHIP (10/100/1000M & 10/100M co-lay)



RTL811100B-CG	RTL8111G-CGT	RTL8106E0B-CG	RTL8106E-CG
71.08111.W03	71.08111.003	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

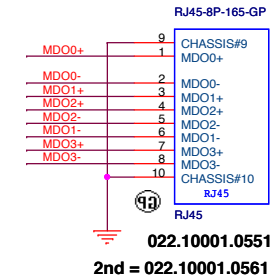
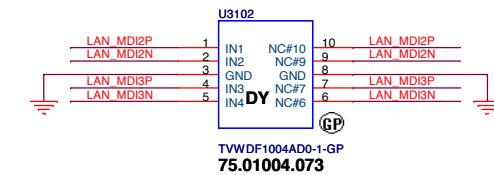
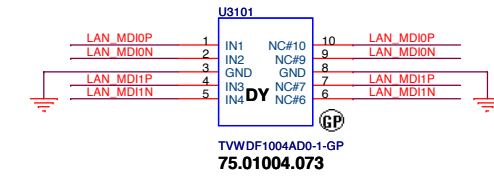
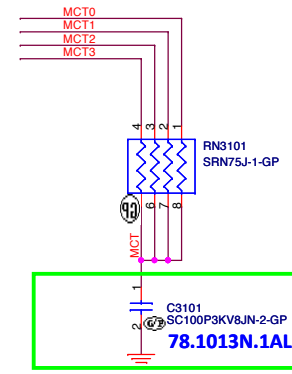
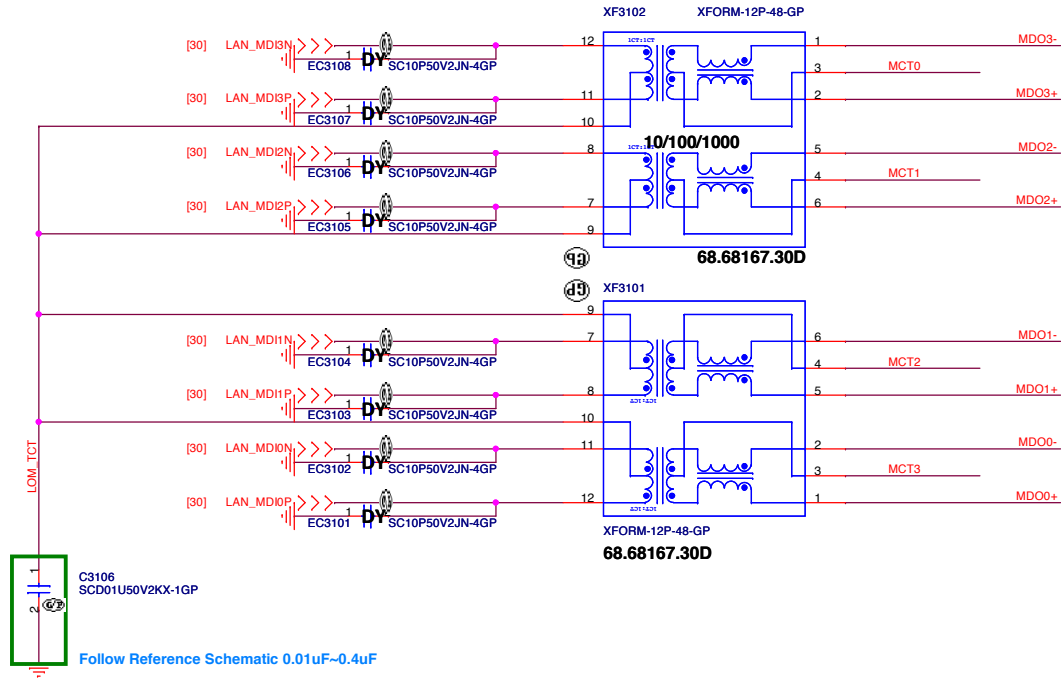


	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03) / RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

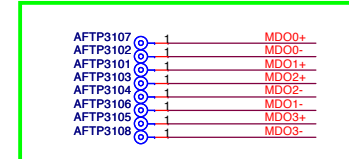
SSID = LOM

LAN Transformer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



(Blanking)

<Core Design>



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Title

(Reserved)Card Reader

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<Core Design>



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Title

(Reserved)

Size
A4

Document Number

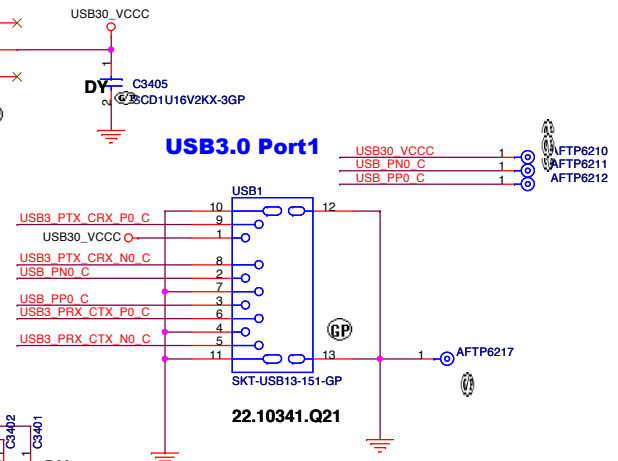
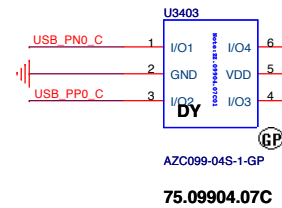
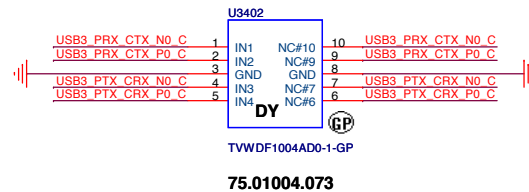
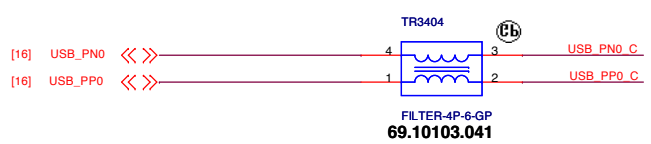
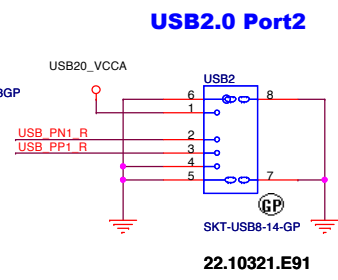
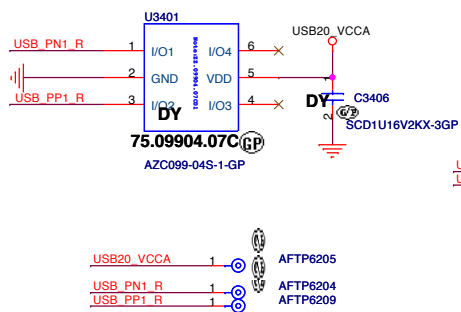
Janus HSW 40/50/70

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SSID = USB



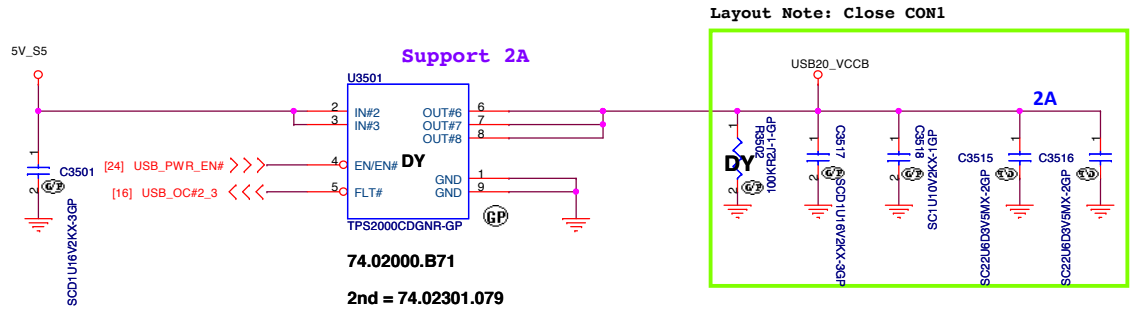
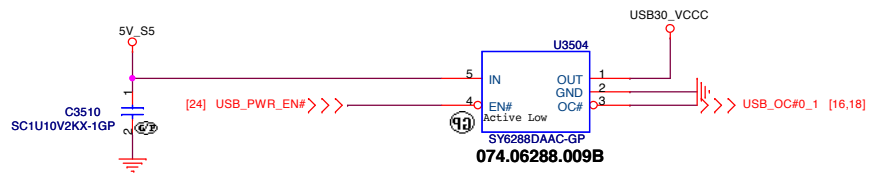
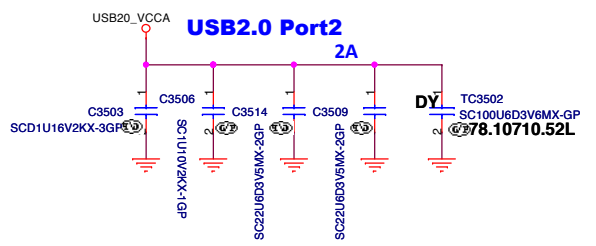
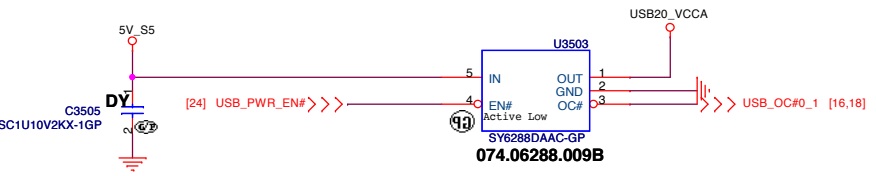
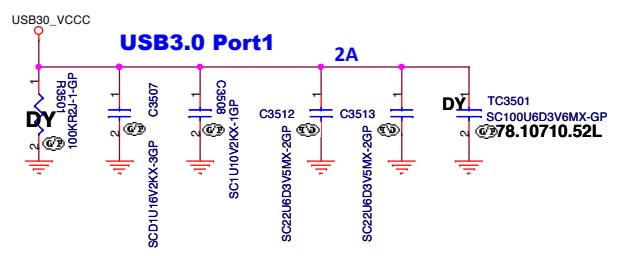
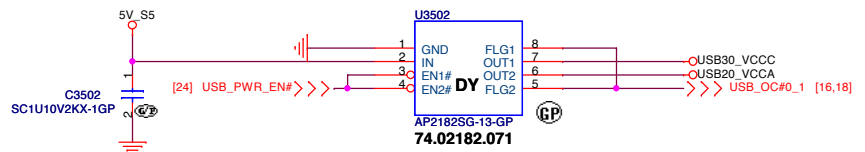
<Core Design>

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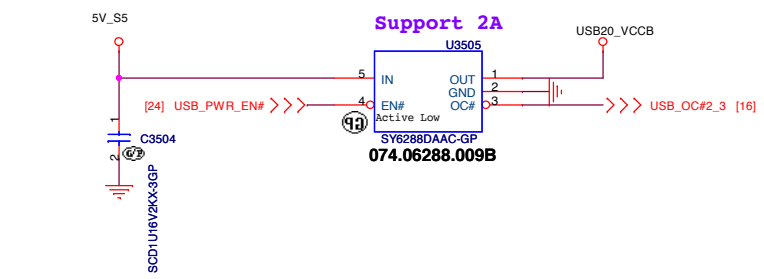
Title: **USB 3.0**

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Custom	Janus HSW 40/50/70	A00

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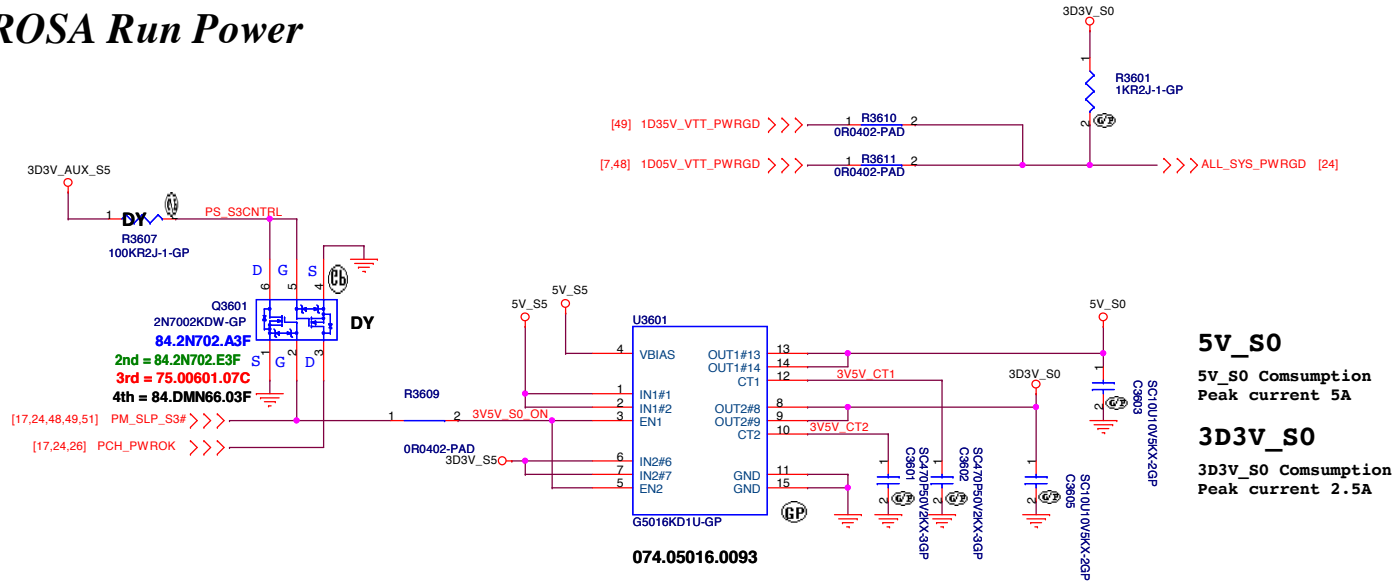
USB2.0 Port3 (IO Board)



SSID = Reset.Suspend

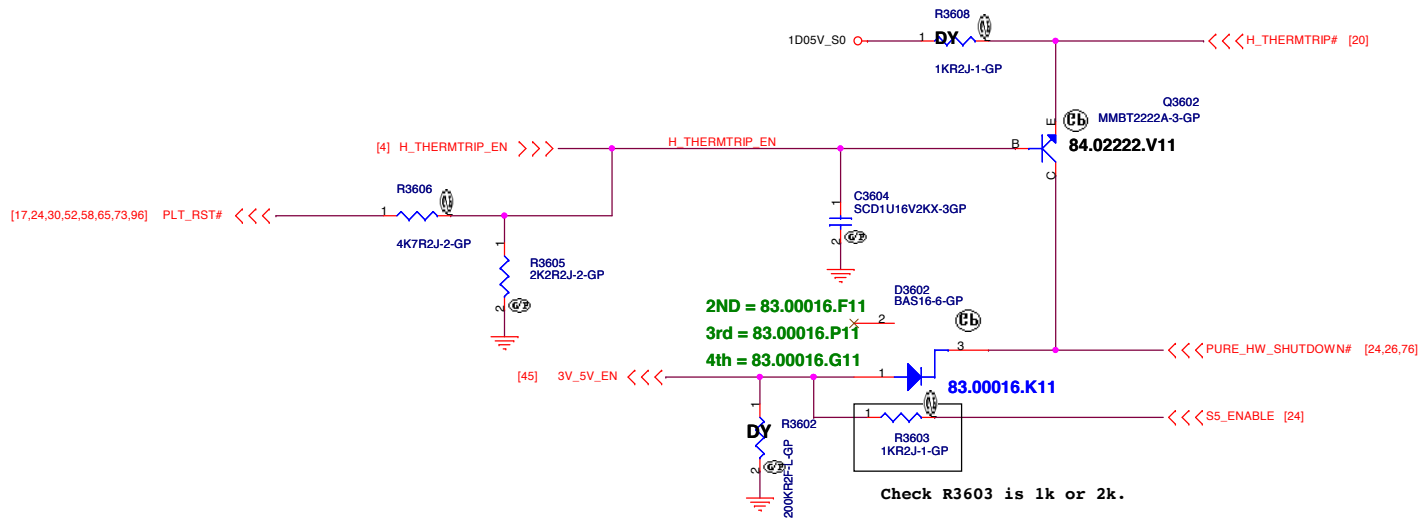
Power Good

ROSA Run Power



5V_S0
5V_S0 Consumption
Peak current 5A

3D3V_S0
3D3V_S0 Consumption
Peak current 2.5A



<Core Design>

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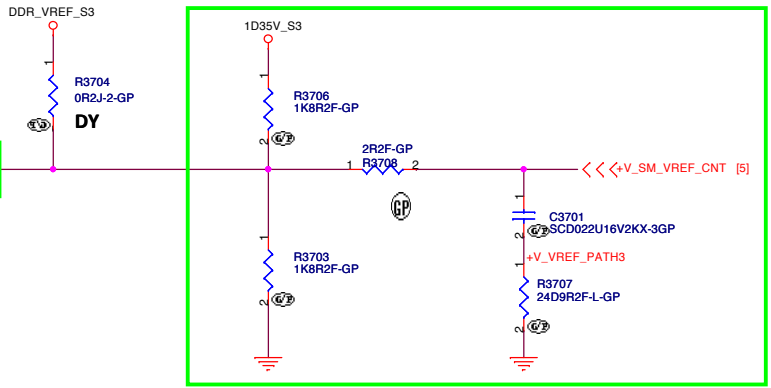
Title: **Power Plane Enable**

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SSID = Reset.Suspend

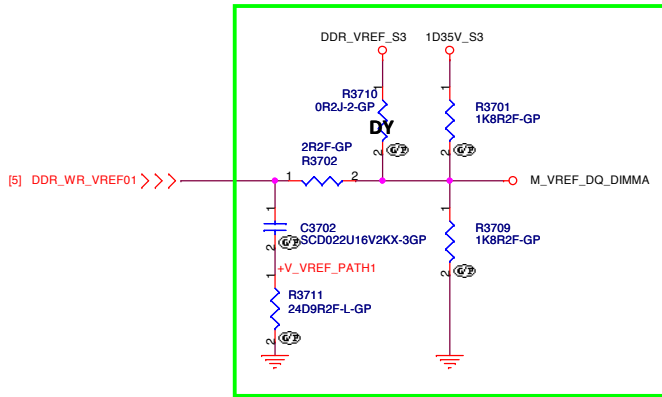
SA_DIMM_VREFDQ

SODIMM1 M_VREF_CA_DIMMA



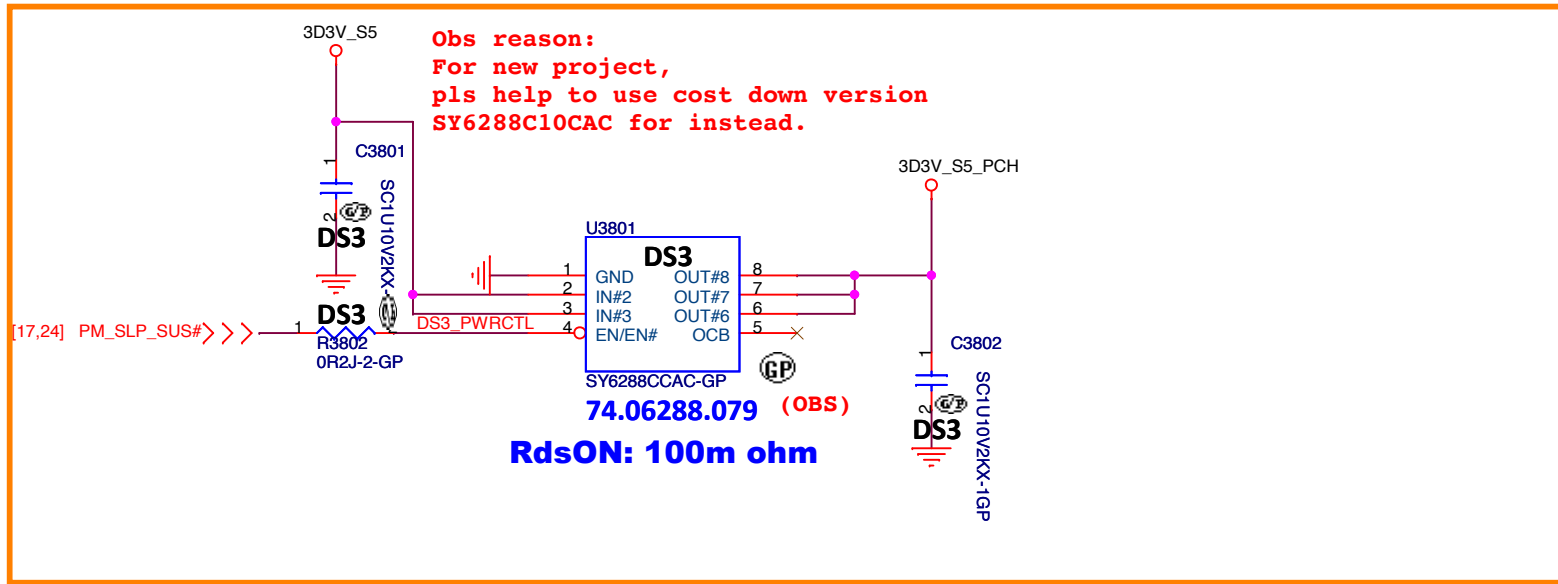
Layout Note:

Place Close SO-DIMM1



<Core Design>

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Title <p align="center">S3 Reduction Circuit</p>		
Size A3	Document Number Janus HSW 40/50/70	Rev A00
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**Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.**

<Core Design>

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Title		DSW	
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Title
(Reserved) 1D05_M

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<i>Reserved</i>		
Size A4	Document Number <i>Janus HSW 40/50/70</i>	Rev <i>A00</i>
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<Core Design>



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Title

Reserved

Size
A4

Document Number

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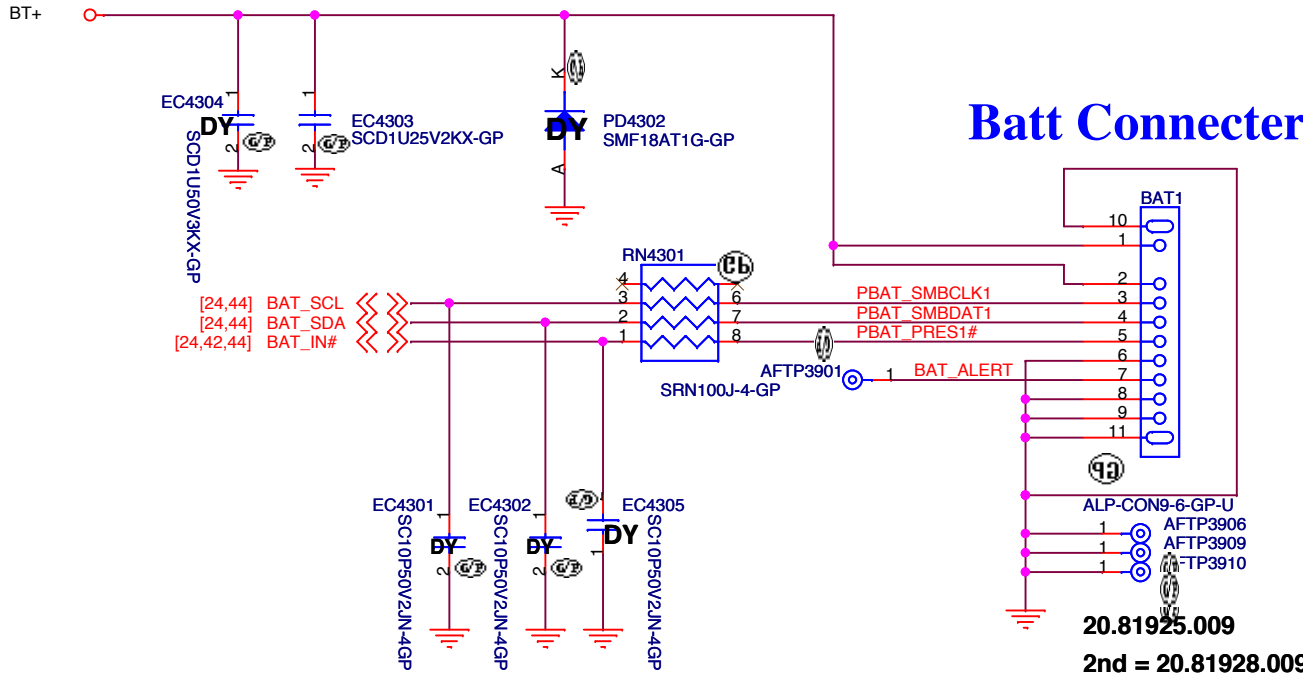
Rev

A00

Date: Friday, February 07, 2014

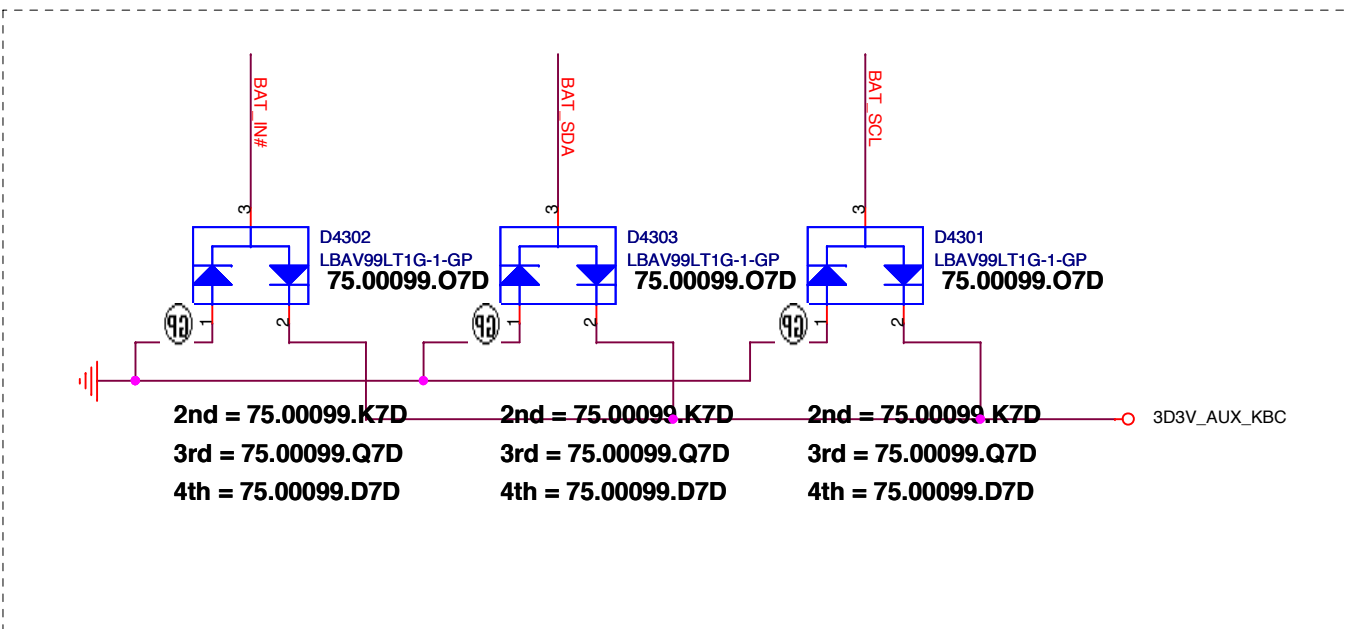
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SSID = PWR.Support




PBAT_PRES1#	1	AFTP3902
PBAT_SMBDAT1	1	AFTP3903
PBAT_SMBCLK1	1	AFTP3904
BT+	1	AFTP3905
BT+	1	AFTP3907
BT+	1	AFTP3908

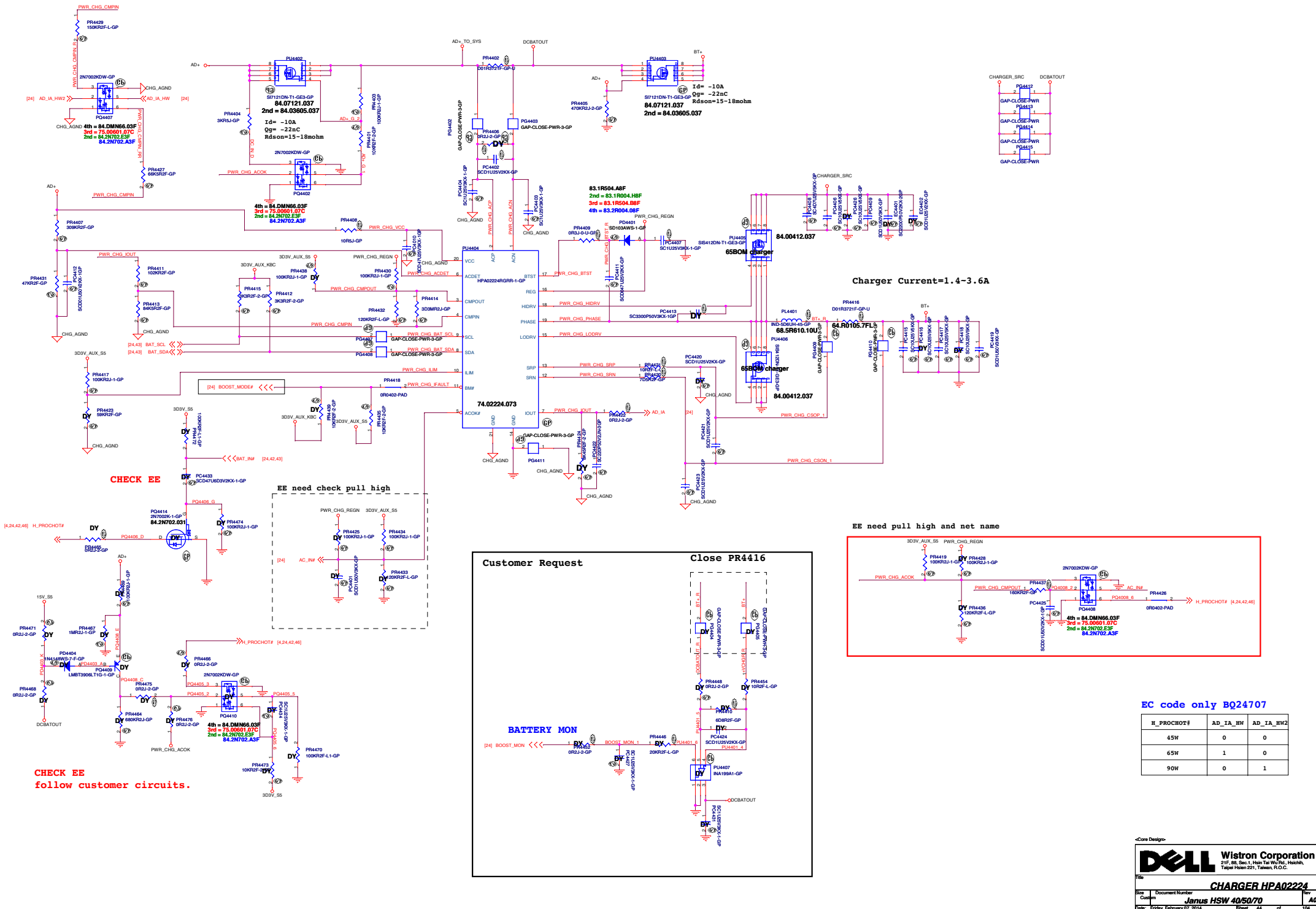
Placement: Close to Batt Connector



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		BATT CONN	
Title	Document Number		Rev
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SSID = Charger



CHECK EE

EE need check pull high

Customer Request

Close PR4416

BATTERY MON

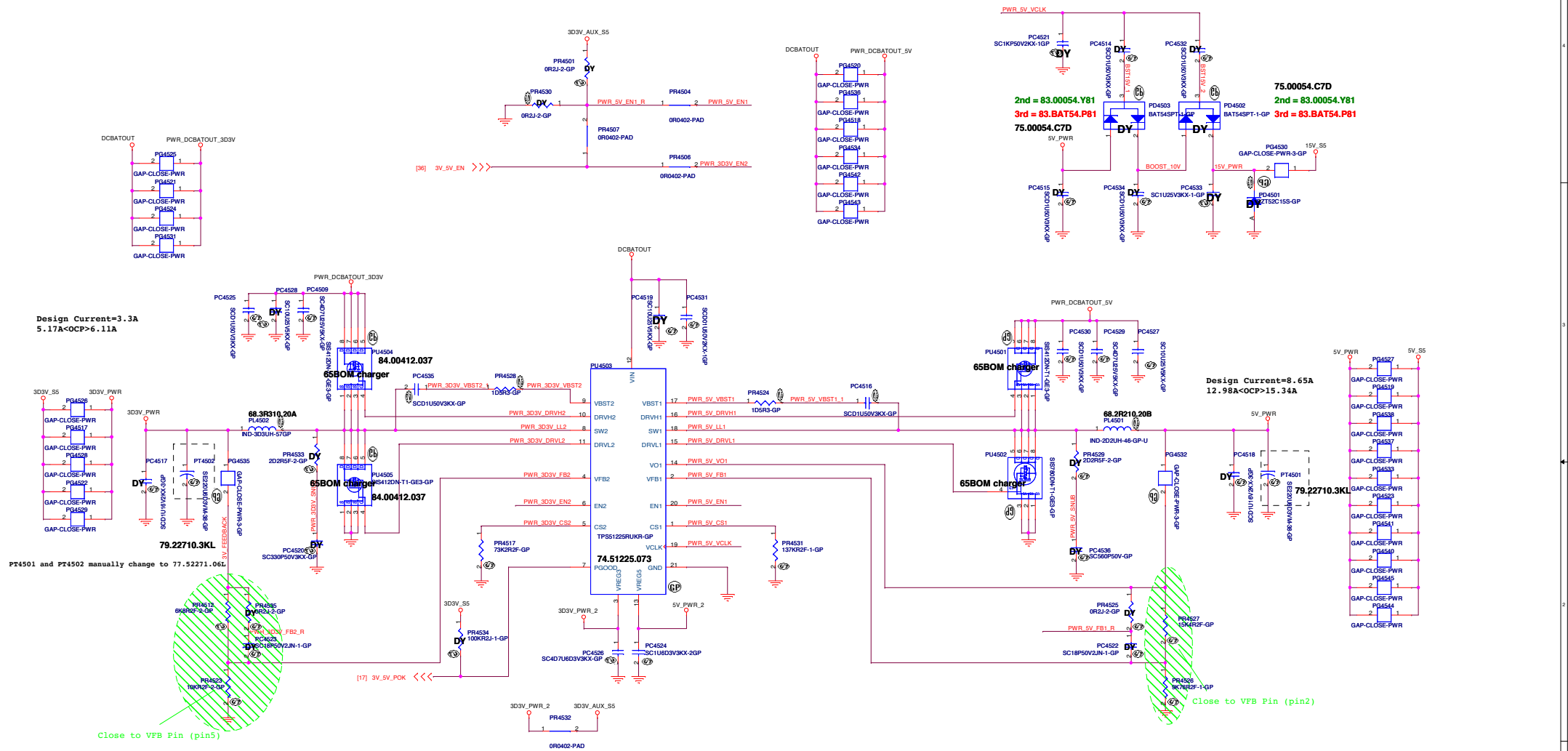
EE need pull high and net name

EC code only BQ24707

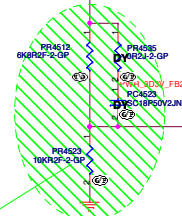
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

SSID = PWR.Plane.Regulator_5v3p3v

Design Current=3.3A
5.17A<OCP>6.11A



PT4501 and PT4502 manually change to 77.52271.06L



Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

TPS51225 & TPS51285 Co-Lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 3.3UH PCMC063T-3R3M Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
 O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
 H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOK 2.2UH PCMC063T-2R2M 18mohm/20mohm Isat =14Arms 68.2R210.20B
 O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
 H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

<Core Design>

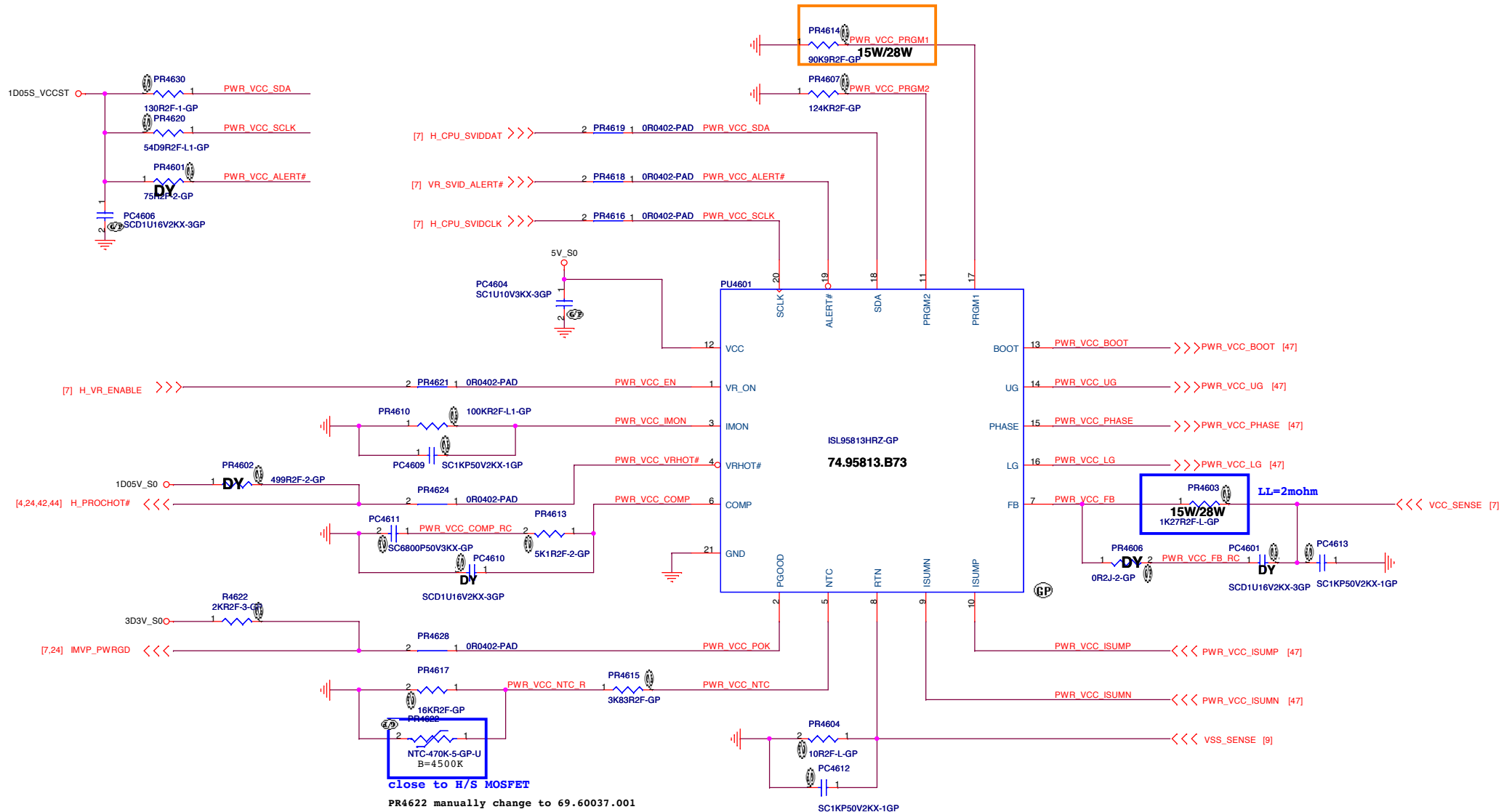
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: **3V/5V TPS51225**

Size: 42 Document Number: **Janus HSW 40/50/70** Rev: **ADD**

Date: Friday, February 07, 2014 Sheet: 35 of 103

SSID = CPU.Regulator

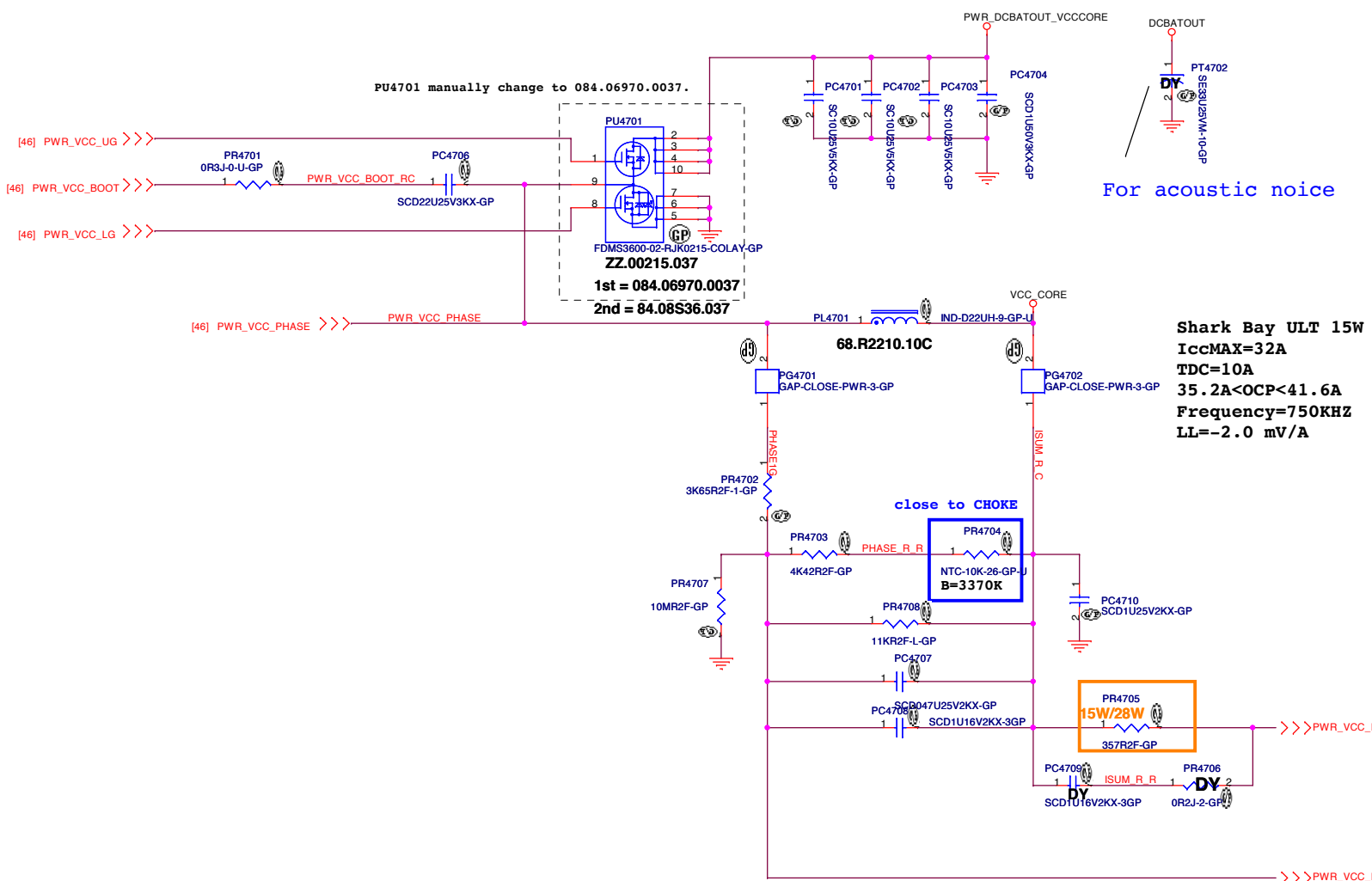


	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

<Core Design>

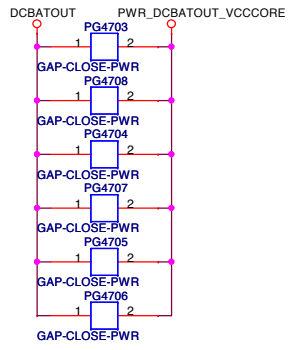


Title ISL95813_CPUCORE(1/2)		
Size A3	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 46	of 104



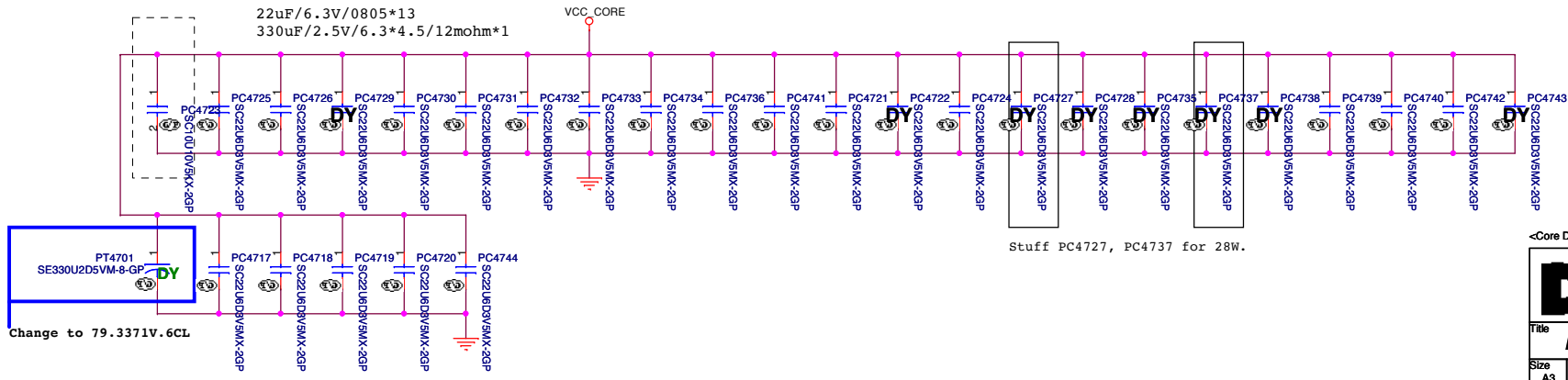
For acoustic noise

Shark Bay ULT 15W CPU
 IccMAX=32A
 TDC=10A
 35.2A<OCP<41.6A
 Frequency=750KHZ
 LL=-2.0 mV/A



	PR4705 (Cyntec)	OCP
15W	357 ohm (64.35705.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A

Change PC4723 to 10U from 22U based on PI Simulation.



<Core Design>

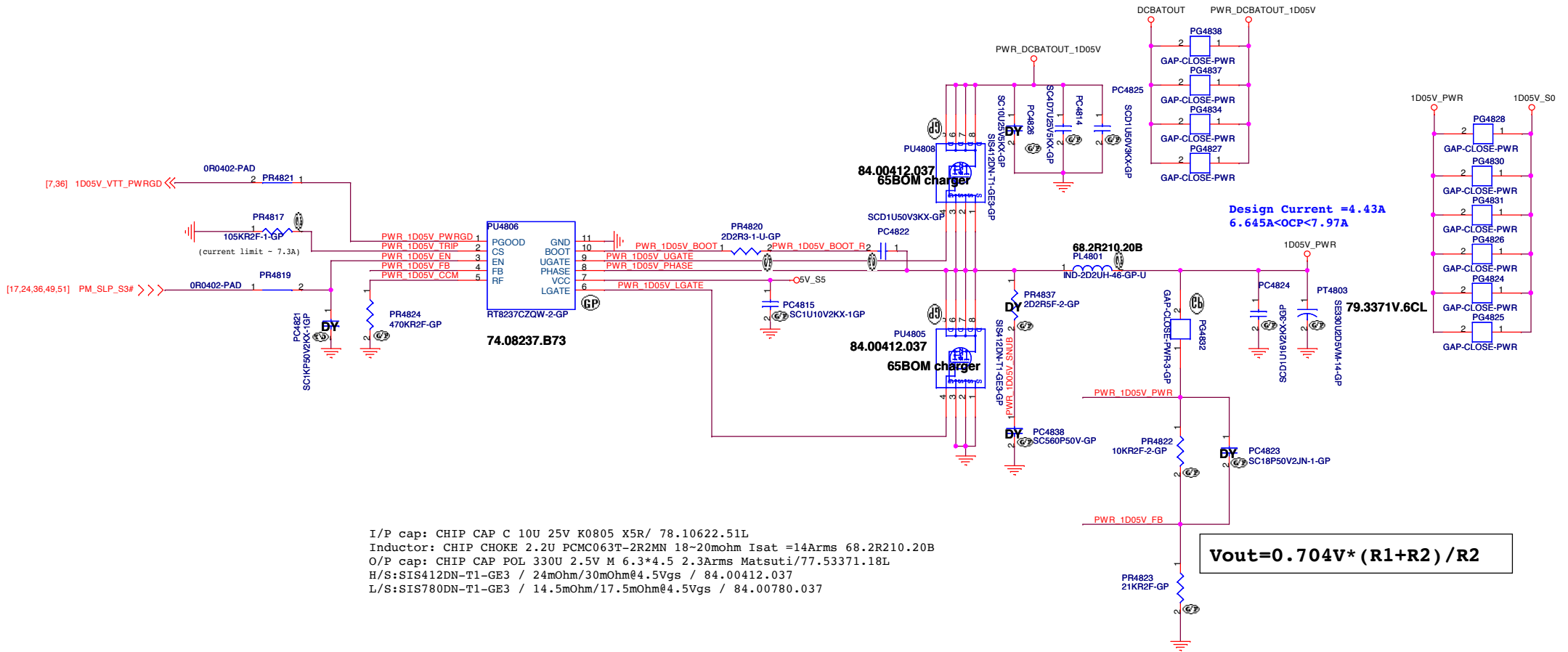
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95813_CPUCORE(2/2)**

Size: A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

Date: Friday, February 07, 2014 Sheet 47 of 104

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
 L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

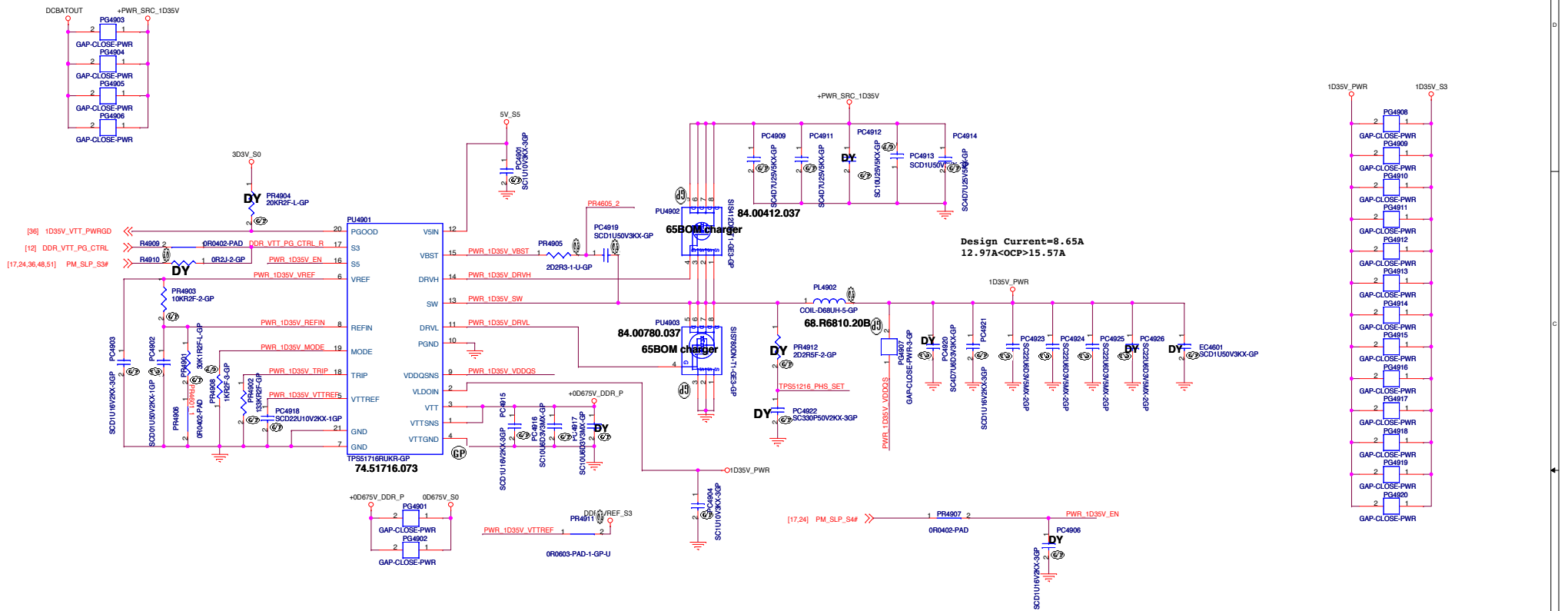
<Core Design>

Wistron Corporation
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Title: **RT8237_1D05V**

Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 48 of 104	

SSID = PWR.Plane.Regulator lp35v0p675v




State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCM063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 MOS: FET MOS FDM53664S NC POWER56 / 84.03664.037 / Q1: 8.5-11mohm @Vgs=4.5V Q2: 2.6-3.2mohm @Vgs=4.5V

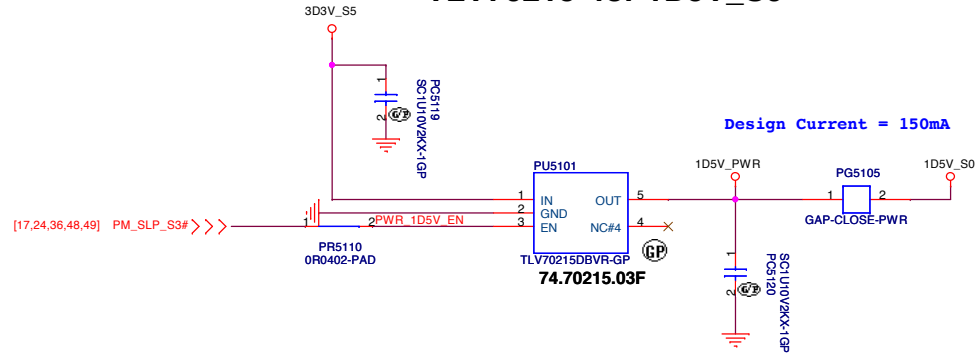
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<Core Design>

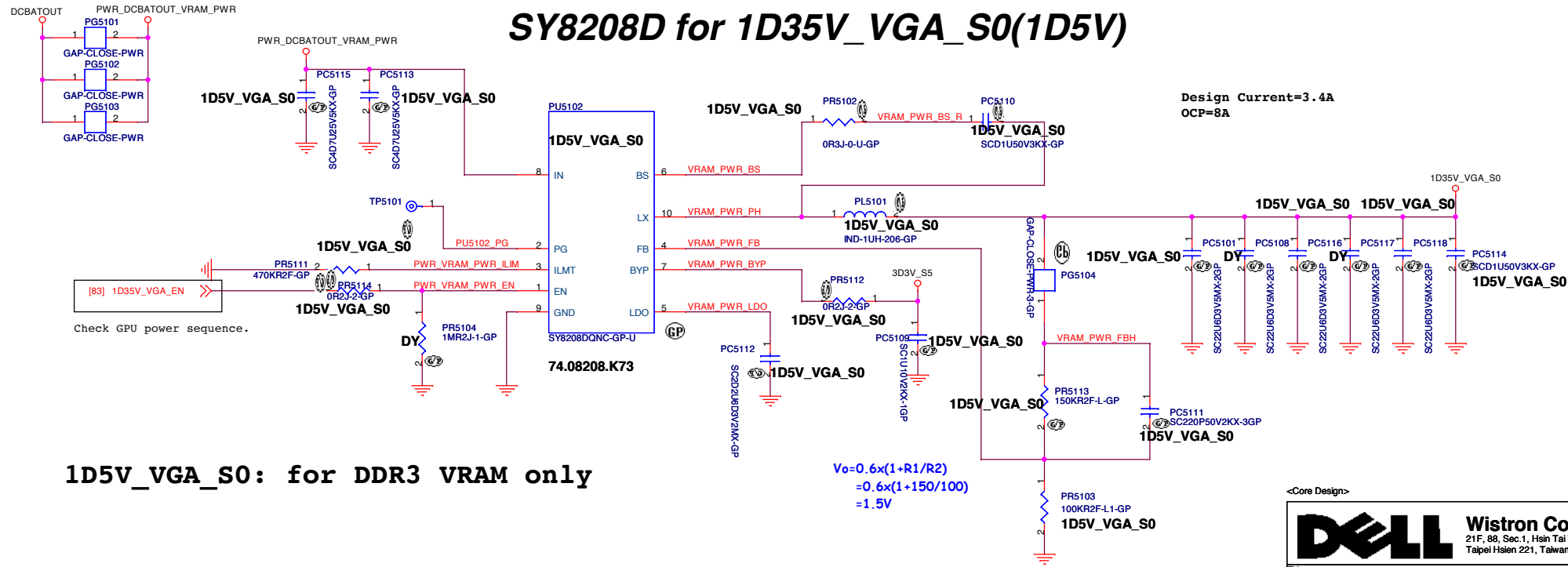
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00
Date: Friday, February 07, 2014	Sheet 50 of	104

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

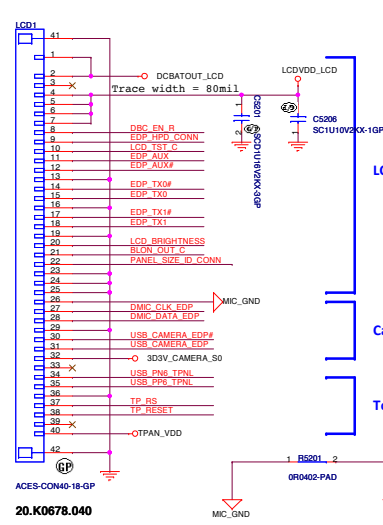
$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5V$$

<Core Design>

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Title: **TLV70215_1D5V / SY8208D_1D5V(VGA)**

Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet: 51	of 104



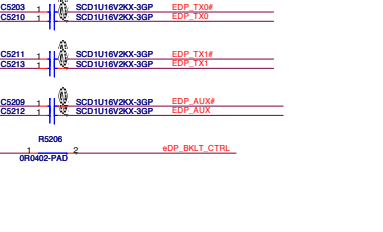
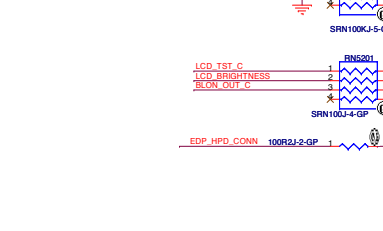
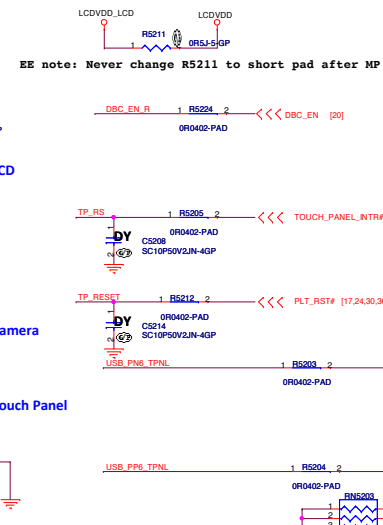
ACES-CON40-18-GP
20.K0678.040

LCD_BRIGHTNESS	1	AFTPS203
BLON_OUT_C	1	AFTPS205
LCD_TST_C	1	AFTPS207
EDP_AUX	1	AFTPS206
EDP_AUX#	1	AFTPS208
EDP_TX0#	1	AFTPS210
EDP_TX0	1	AFTPS212
EDP_TX1#	1	AFTPS211
EDP_TX1	1	AFTPS213
DMIC_CLK_C	1	AFTPS222
DMIC_DATA_C	1	AFTPS228
USB_CAMERA#	1	AFTPS225
USB_CAMERA	1	AFTPS226
3D3V_CAMERA_S0	1	AFTPS227
EDP_HPDI_CONN	1	AFTPS201
LCDVDD_LCD	1	AFTPS202
DCBATOUT_LCD	1	AFTPS204
TP_RS	1	AFTPS209
TP_RESET	1	AFTPS214

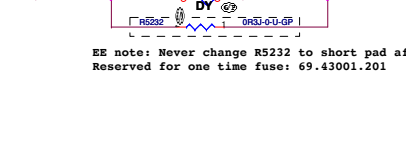
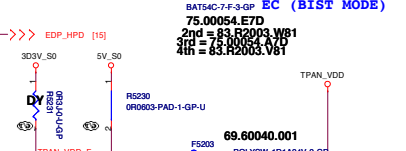
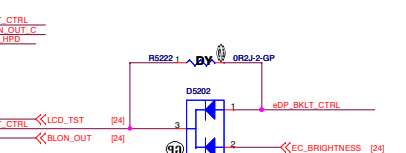
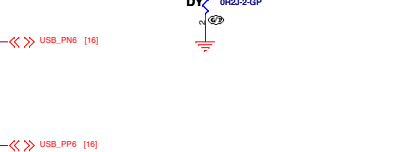
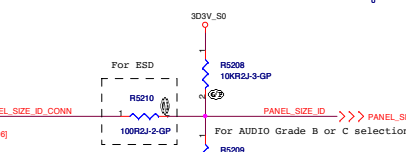
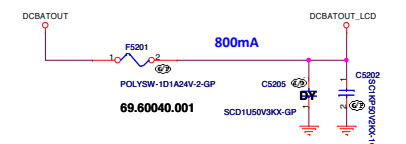
[8] EDP_TX0_DN	>>>	C5203	SCD1U18V2KX-3GP	EDP_TX0#
[8] EDP_TX0_DP	>>>	C5210	SCD1U18V2KX-3GP	EDP_TX0
[8] EDP_TX1_DN	>>>	C5211	SCD1U18V2KX-3GP	EDP_TX1#
[8] EDP_TX1_DP	>>>	C5213	SCD1U18V2KX-3GP	EDP_TX1
[8] EDP_AUX_DN	>>>	C5209	SCD1U18V2KX-3GP	EDP_AUX#
[8] EDP_AUX_DP	>>>	C5212	SCD1U18V2KX-3GP	EDP_AUX
[15] L_BKLT_CTRL	>>>	R5206	OR0402-PAD	eDP_BKLT_CTRL

Brightness

[15] L_BKLT_CTRL >>> R5206 OR0402-PAD eDP_BKLT_CTRL

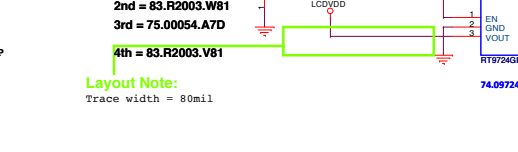
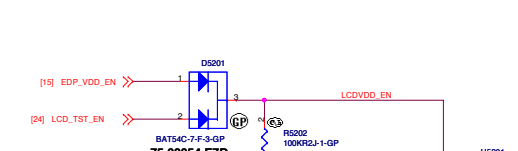
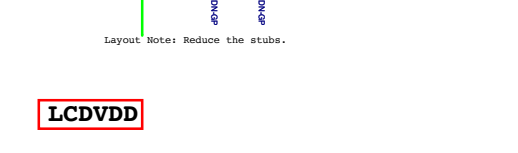
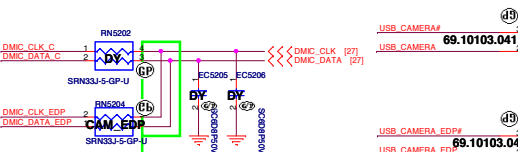
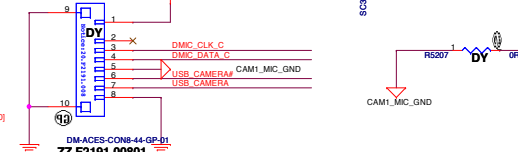
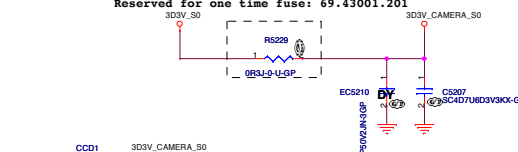


INVERTER POWER



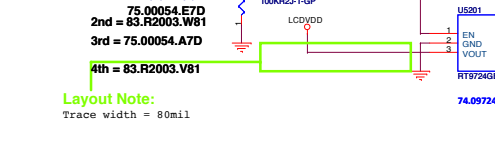
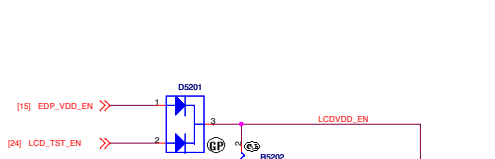
EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

CAM1



Layout Note: Reduce the stubs.


LCDVDD



Layout Note: Trace width = 80mil

(Blanking)

<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
Size	Document Number				Rev
A3	Janus HSW 40/50/70				A00
Date: Friday, February 07, 2014			Sheet	53	of 104

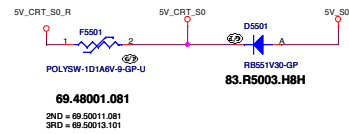
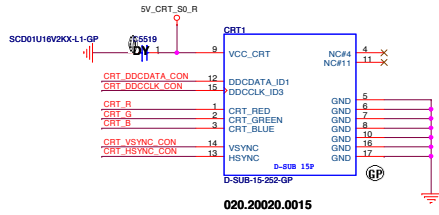
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<Core Design>

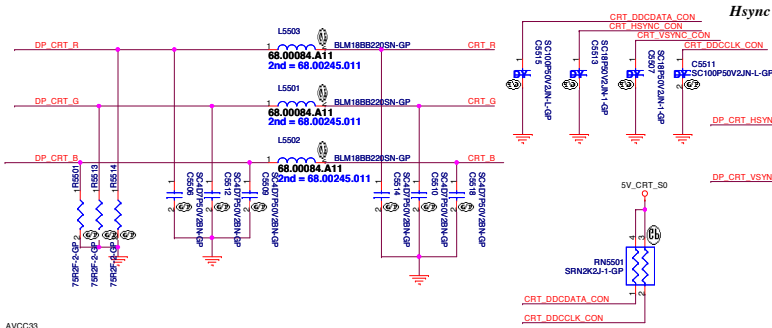
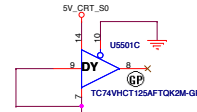
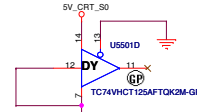


Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	Janus HSW 40/50/70	X02
Date:	Friday, February 07, 2014	Sheet 54 of 104

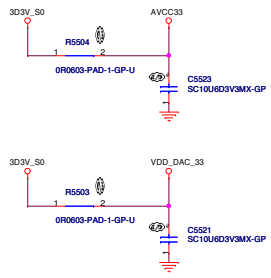
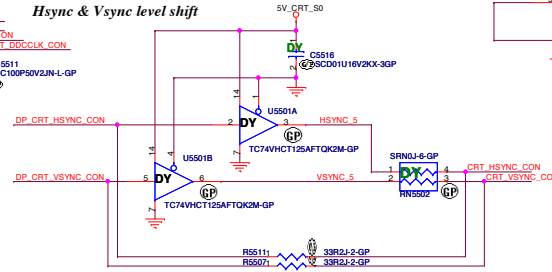
CRT Board Connector



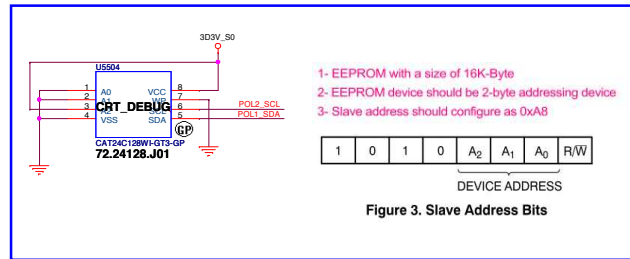
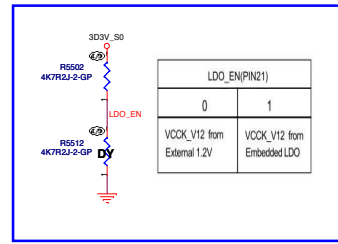
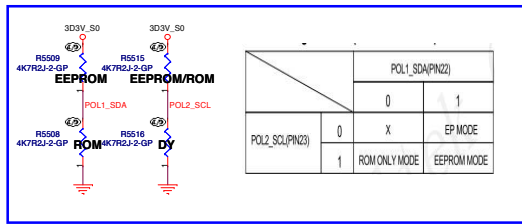
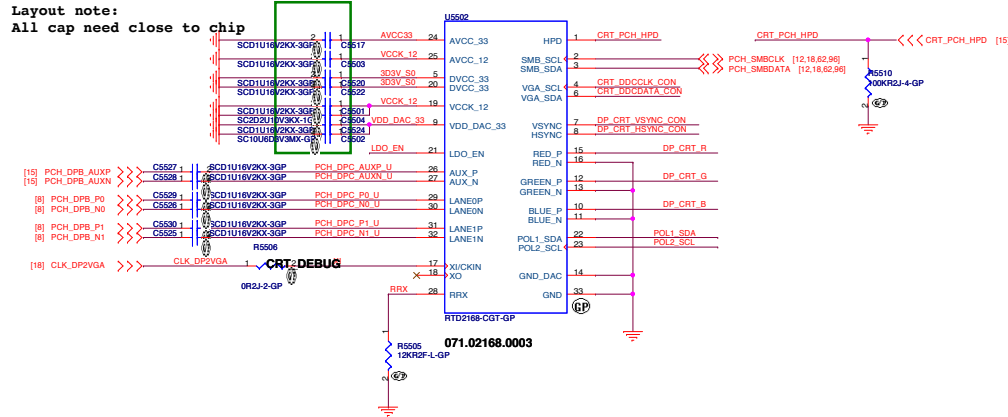
CRT RGB CRT H/VSNC CRT SMBUS



Hsync & Vsync level shift

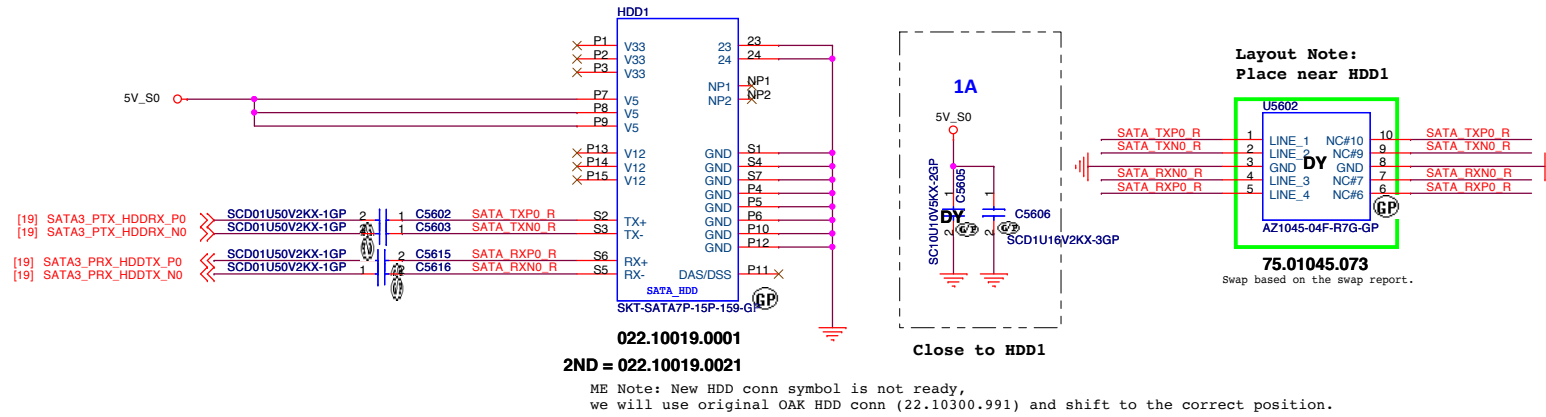


Layout note:
 All cap need close to chip

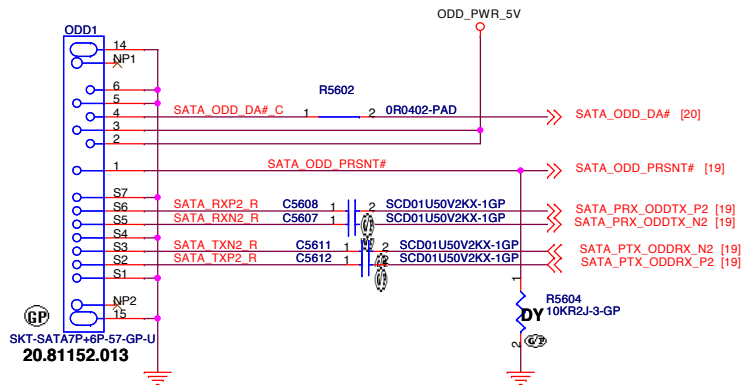


<Core Design>

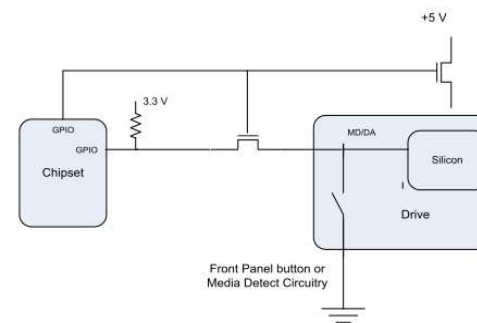
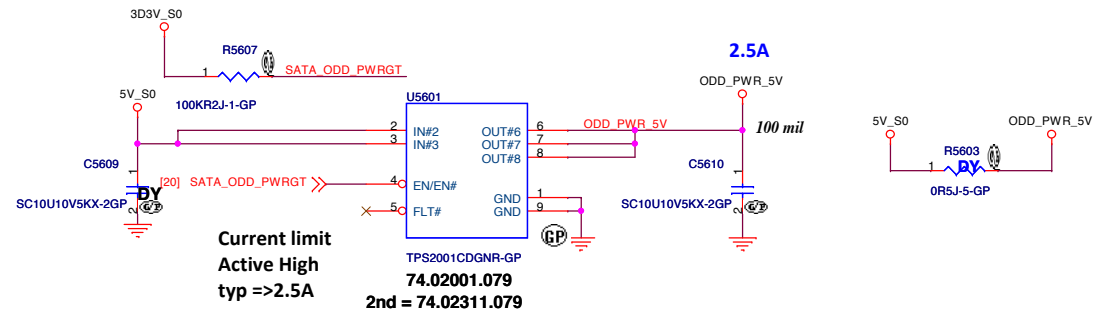
SATA HDD Connector



ODD Connector



SATA Zero Power ODD




<Core Design>



SSID = ESATA

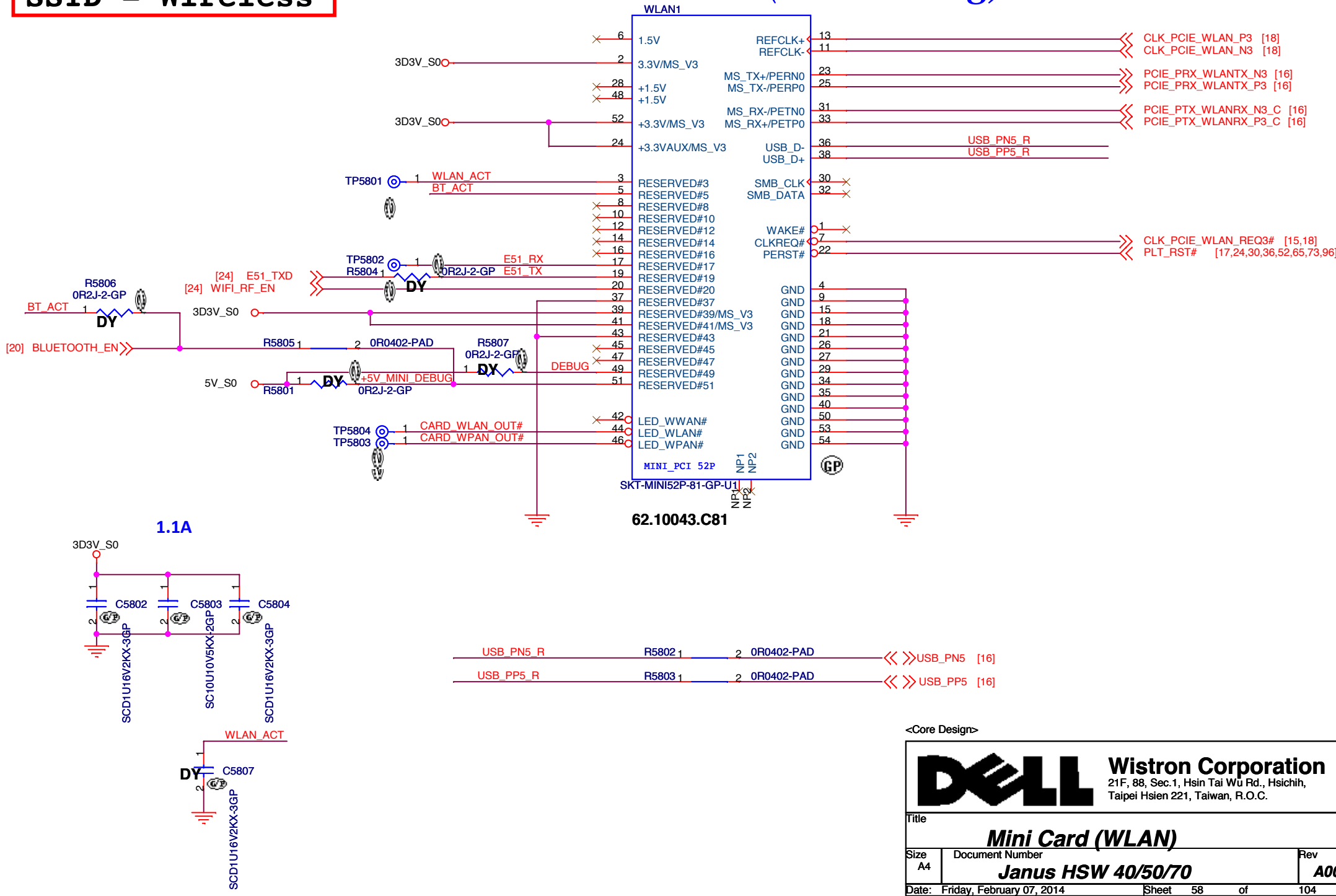
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<Core Design>


		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		ESATA
Size A3	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 57	of 104

SSID = Wireless

Mini Card Connector(802.11a/b/g)




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h3>Mini Card (WLAN)</h3>	
Size A4	Document Number <h3>Janus HSW 40/50/70</h3>	Rev A00	
Date: Friday, February 07, 2014		Sheet 58	of 104


(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Reserved		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 59 of	104

(Blanking)

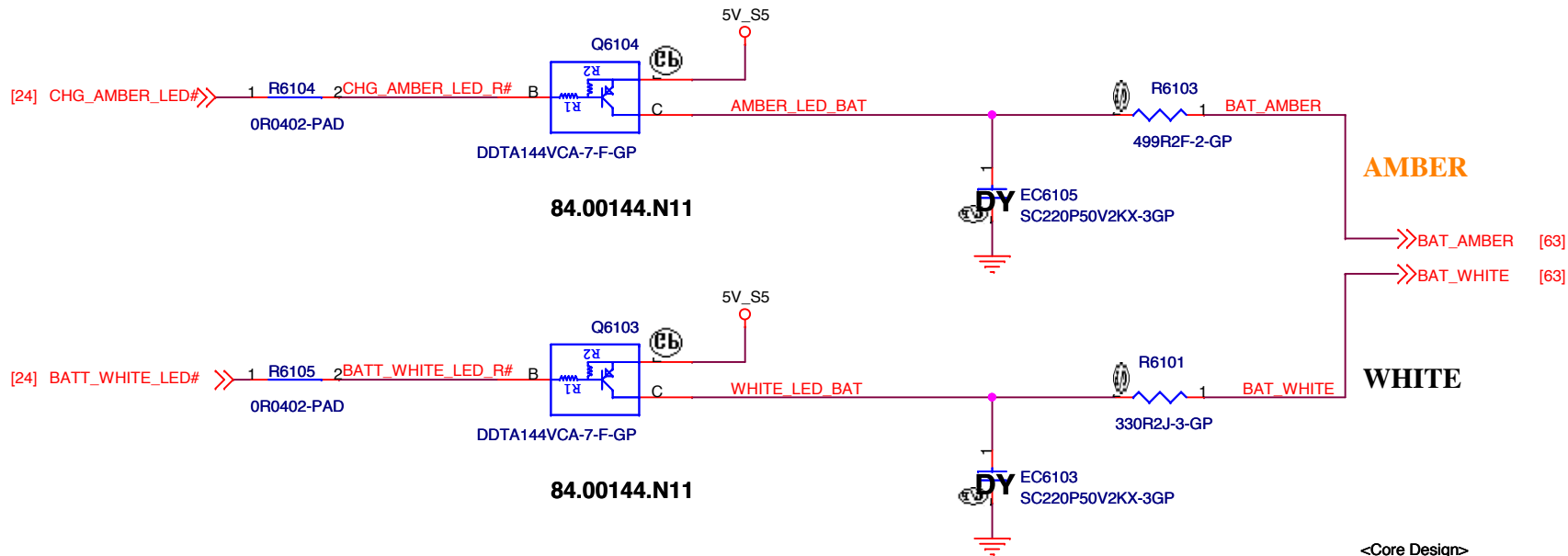
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
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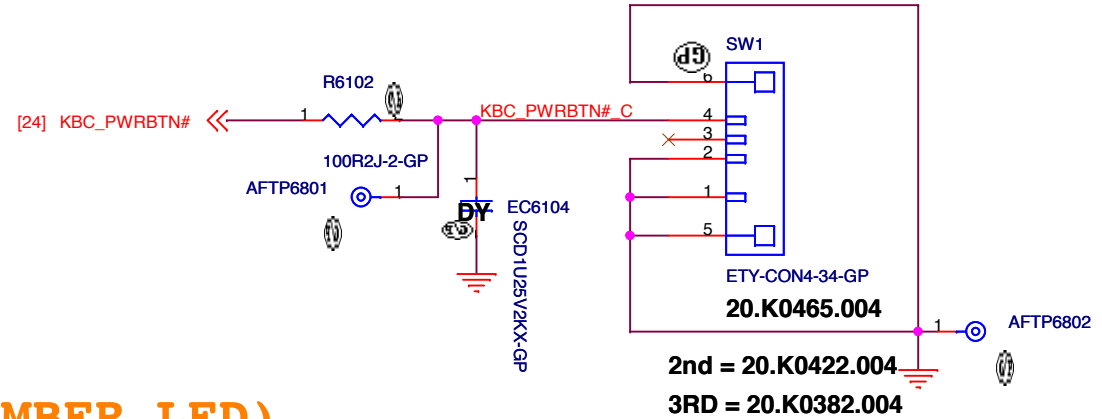
SSID = User.Interface

Power button

Battery LED1 (AMBER_LED) Low actived from KBC GPIO



Battery LED2 (WHITE_LED) Low actived from KBC GPIO



<Core Design>

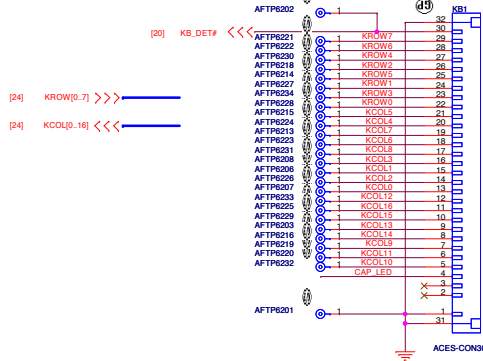


Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

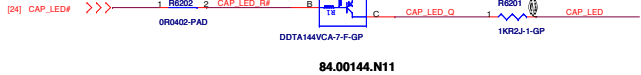
Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00
Date:	Friday, February 07, 2014	Sheet 61 of 104

SSID = KBC

Internal Keyboard Connector (DVC40)

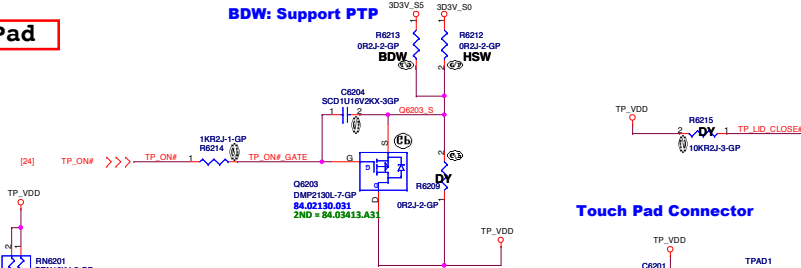


CAP LED Control
LOW activated from KBC GPIO



SSID = Touch.Pad

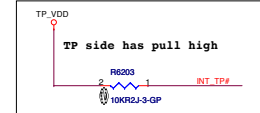
BDW: Support PTP



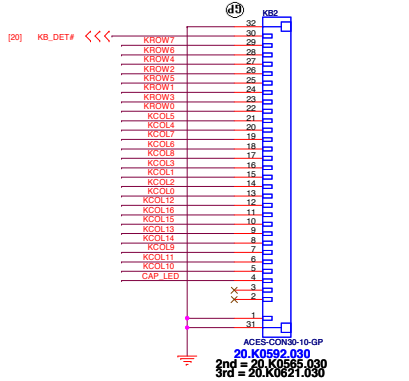
Touch Pad Connector

Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	A*PTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

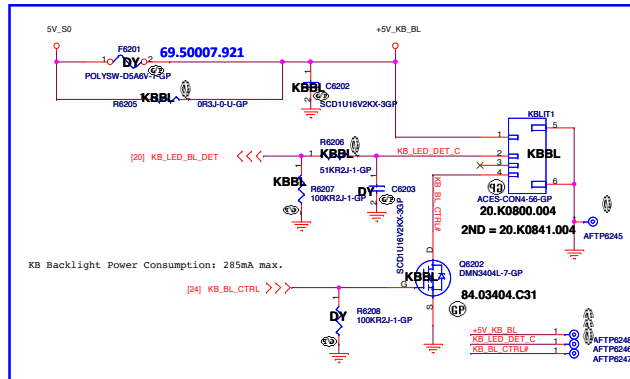
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Internal Keyboard Connector (DVC50/DVC70)



Keyboard Backlight (DVC70)



PS2

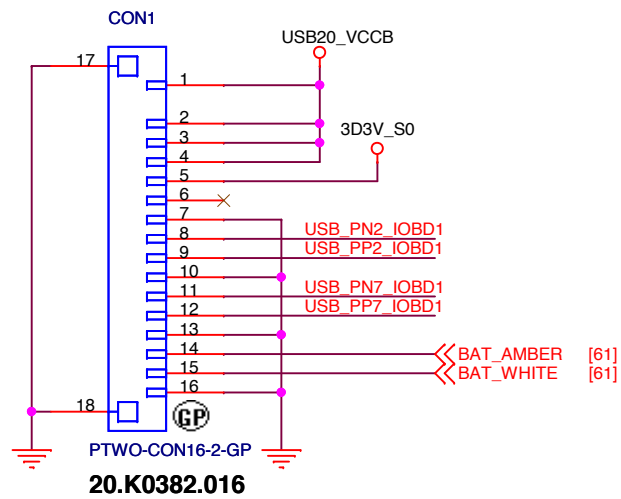
I2C

SMBUS

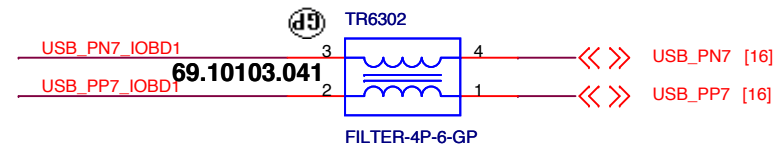
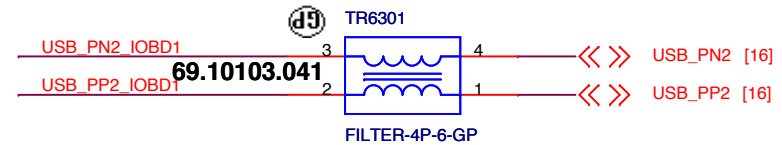
Need to check with SW.

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.0M961.D7C
4th = 84.DM966.D3F

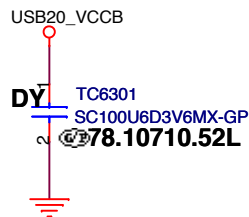
<Core Design>



**USB2.0 Port3
Card Reader
LED**



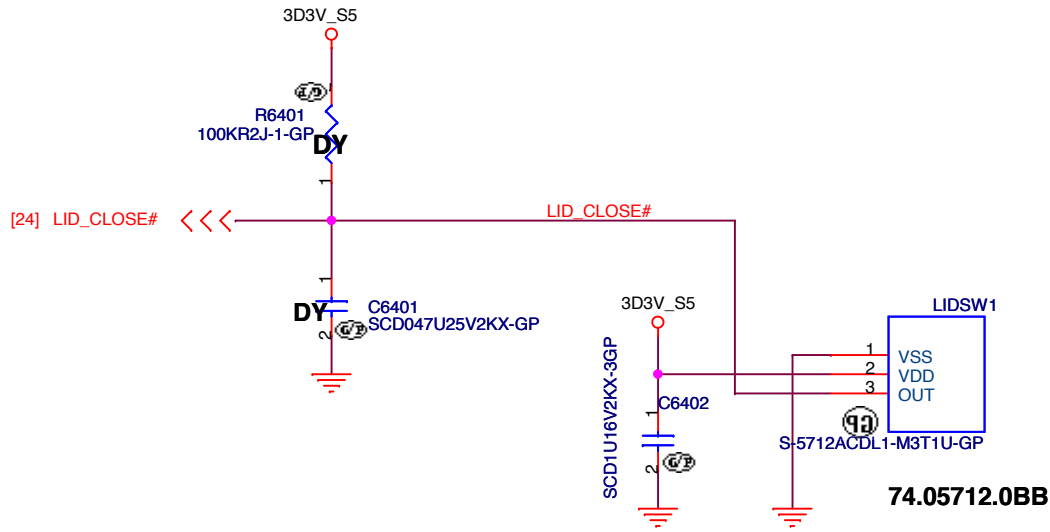
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board Connector			
Size A4	Document Number Janus HSW 40/50/70		Rev A00
Date: Friday, February 07, 2014		Sheet 63 of 104	

SSID = User.Interface

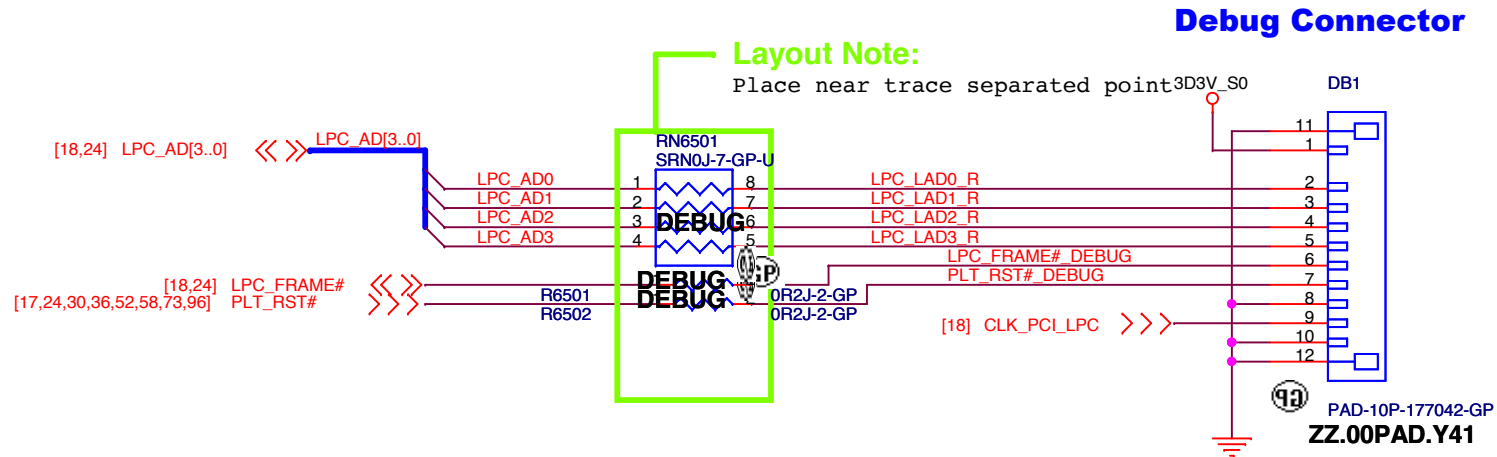


<Core Design>



Title		
Hall Sensor		
Size A4	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 64 of	104

SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

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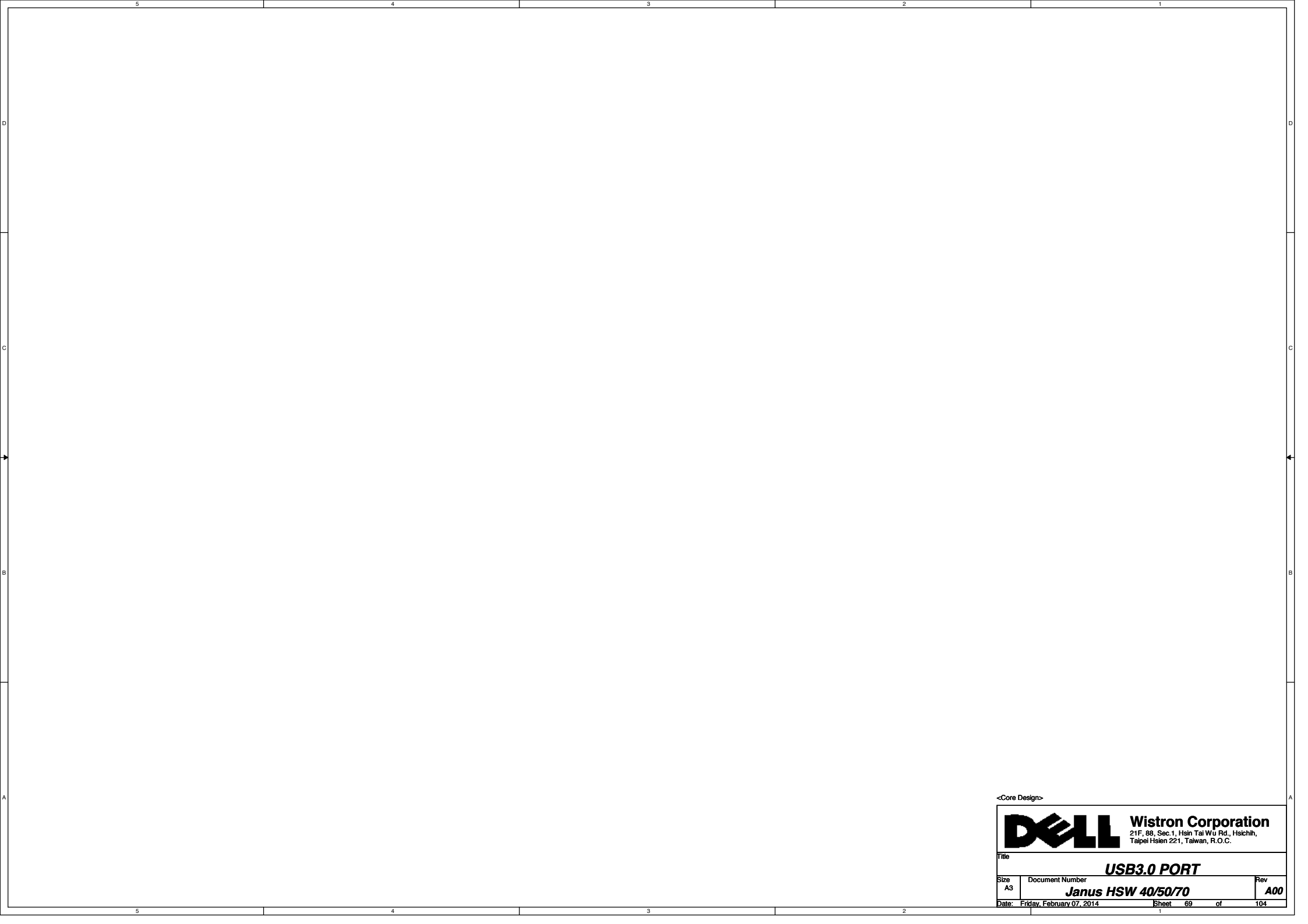
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USB3.0 PORT		
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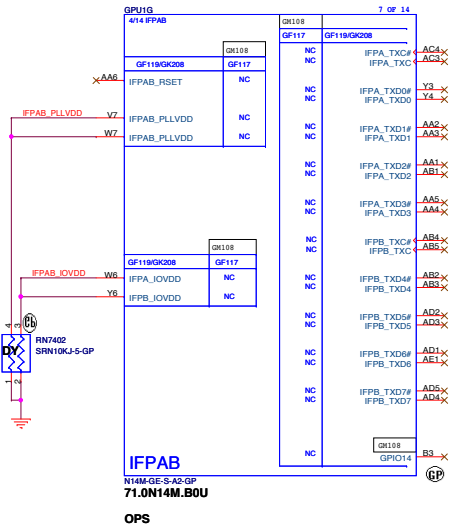
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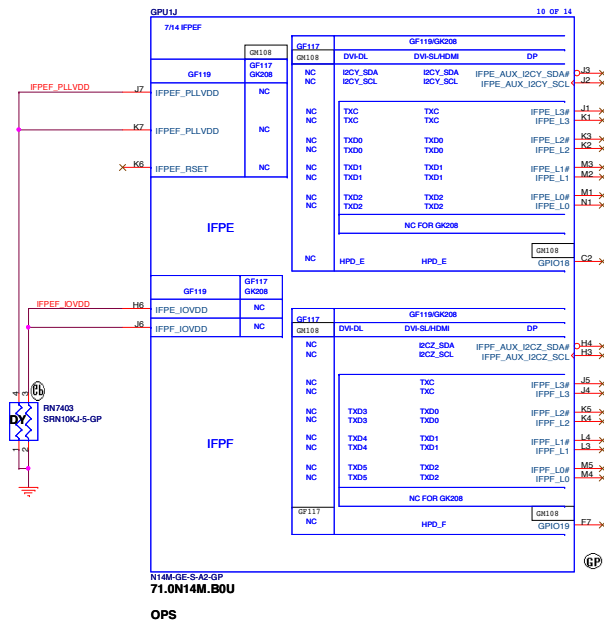
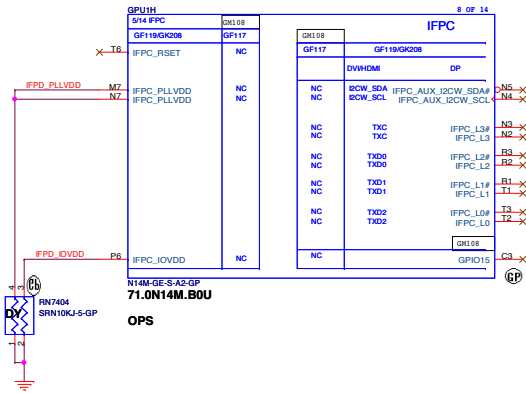
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LVDS Interface



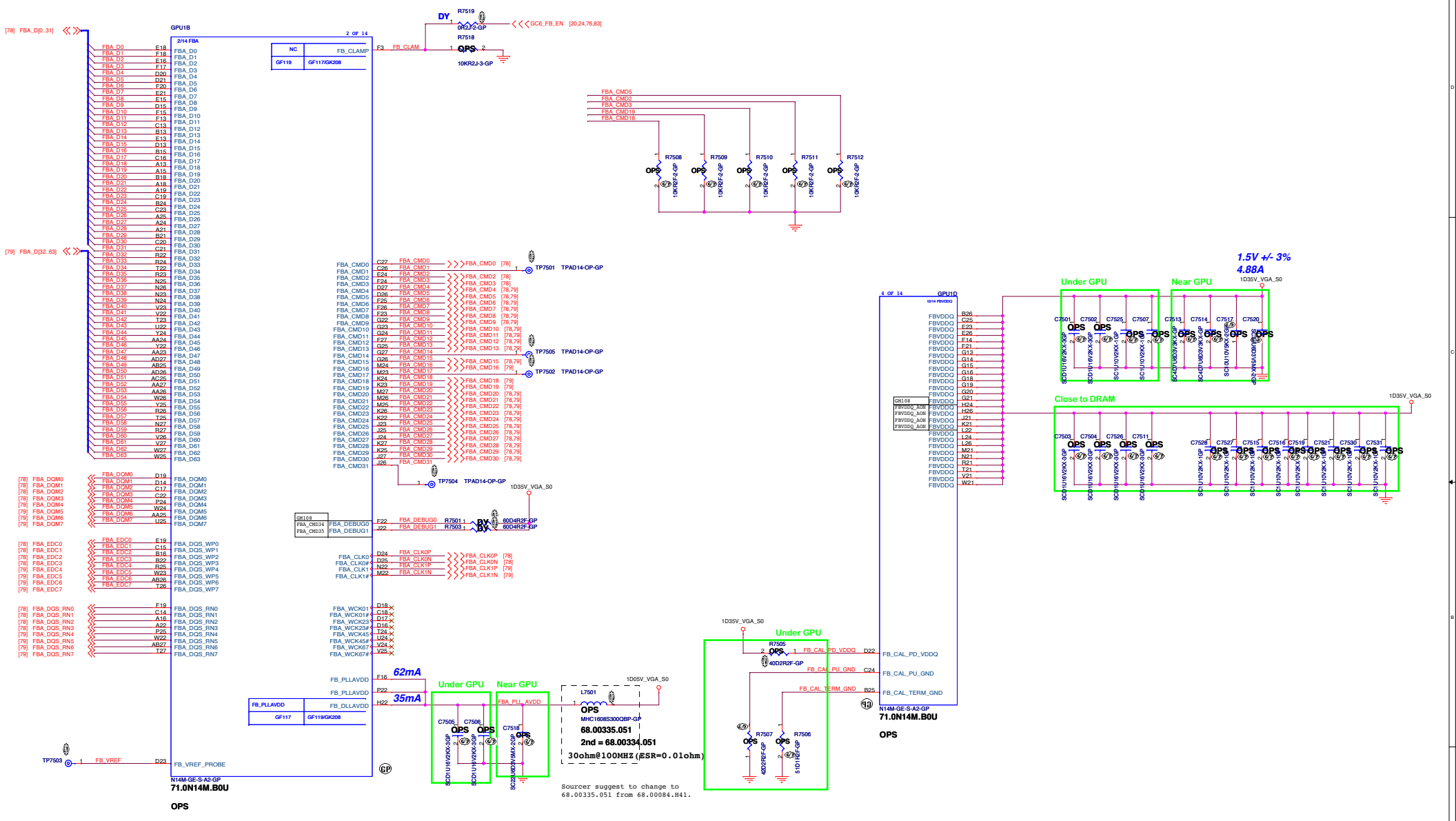
HDMI Interface



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Title			GPU Memory(2/5)		
Size	Document Number	Janus HSW 40/50/70		Rev	A00
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- [78] FBA_D32.63 <<<
- [78] FBA_D0M0 <<<
- [78] FBA_D0M1 <<<
- [78] FBA_D0M2 <<<
- [78] FBA_D0M3 <<<
- [78] FBA_D0M4 <<<
- [78] FBA_D0M5 <<<
- [78] FBA_D0M6 <<<
- [78] FBA_D0M7 <<<
- [78] FBA_EDC0 <<<
- [78] FBA_EDC1 <<<
- [78] FBA_EDC2 <<<
- [78] FBA_EDC3 <<<
- [78] FBA_EDC4 <<<
- [78] FBA_EDC5 <<<
- [78] FBA_EDC6 <<<
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- [78] FBA_DQS_RN0 <<<
- [78] FBA_DQS_RN1 <<<
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- [78] FBA_DQS_RN3 <<<
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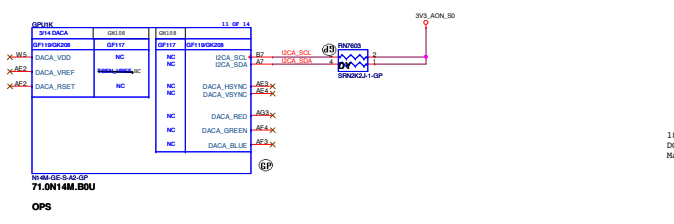
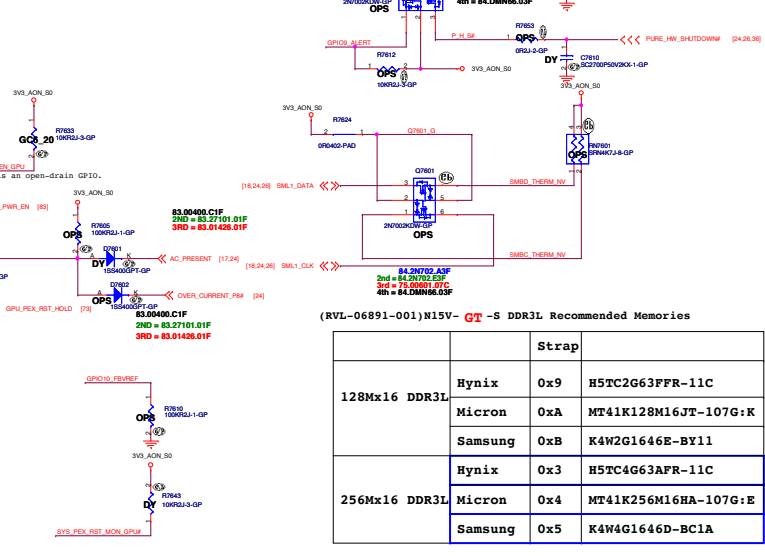
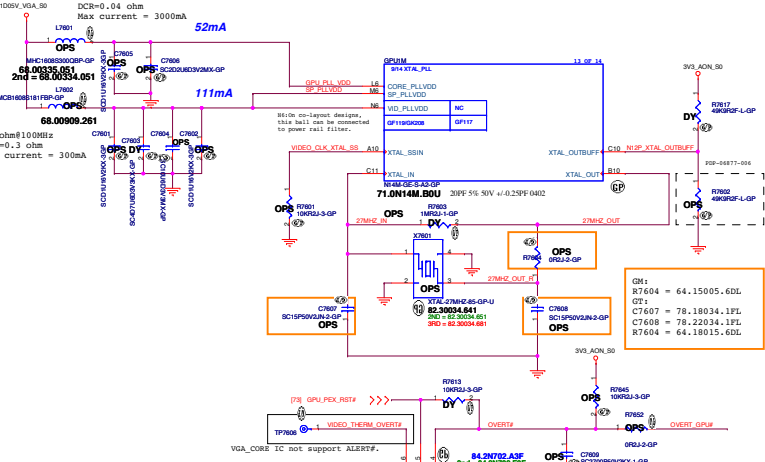
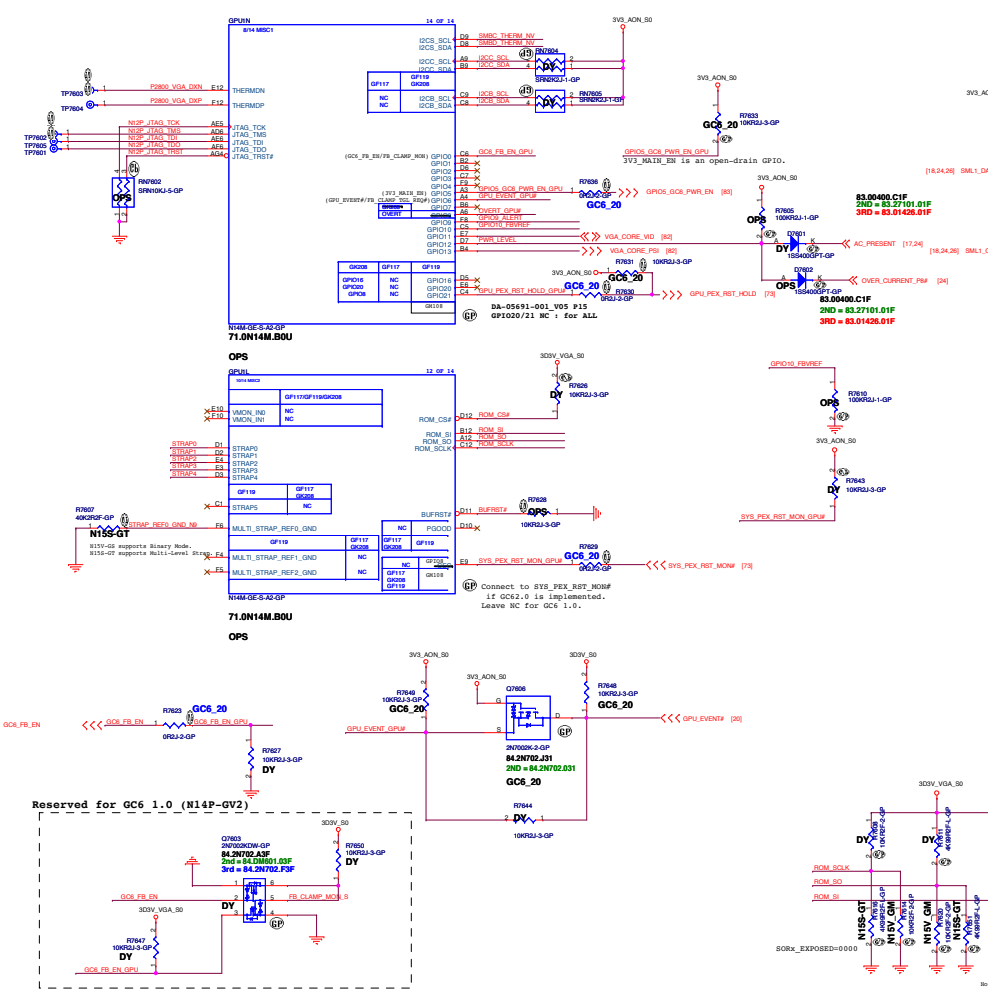


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location	
GB2B-64 and GB4B-128	PLLVDD	0.1 μF	X7R	0402	1	Under GPU
		22 μF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)	0402	1	Hear GPU	

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location	
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 μF	X7R	0402	1 per ball	Under GPU
		4.7 μF	X5R	0603	1	Near GPU
		22 μF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)	0603	1	Near GPU	



Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VEHODOR	10kΩ	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V- GM-S DDR3L Recommended Memories

	Strap	STRAP3	STRAP2	STRAP1	STRAP0		
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FPR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H155-GV	PCI_DEVID[4]	SUB_VEHODOR	PCI_DEVID[5]	PEX_PLL_EH_TERM
ROM_SI	All GB2-64 N14-GM GB2B-64 H15	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	H155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	H155-GM/-GT	USER[2]	USER[2]	USER[1]	USER[0]
STRAP1	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)	3GIO_PADCFCG[1]	3GIO_PADCFCG[0]
STRAP2	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
STRAP3	H155-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	H155-GM/-GT	RESERVED	PCIE_SPEED_CHA	PCIE_MAX_SPEED	PULL_VDD033V

(RVL-06891-001)N15V- GT-S DDR3L Recommended Memories

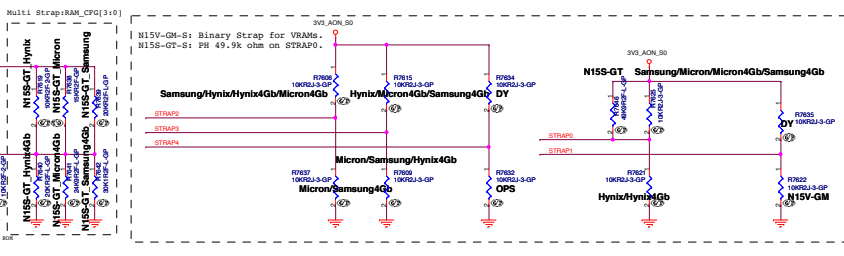
	Strap	
128Mx16 DDR3L	Hynix	0x9
	Micron	0xA
	Samsung	0xB
256Mx16 DDR3L	Hynix	0x3
	Micron	0x4
	Samsung	0x5

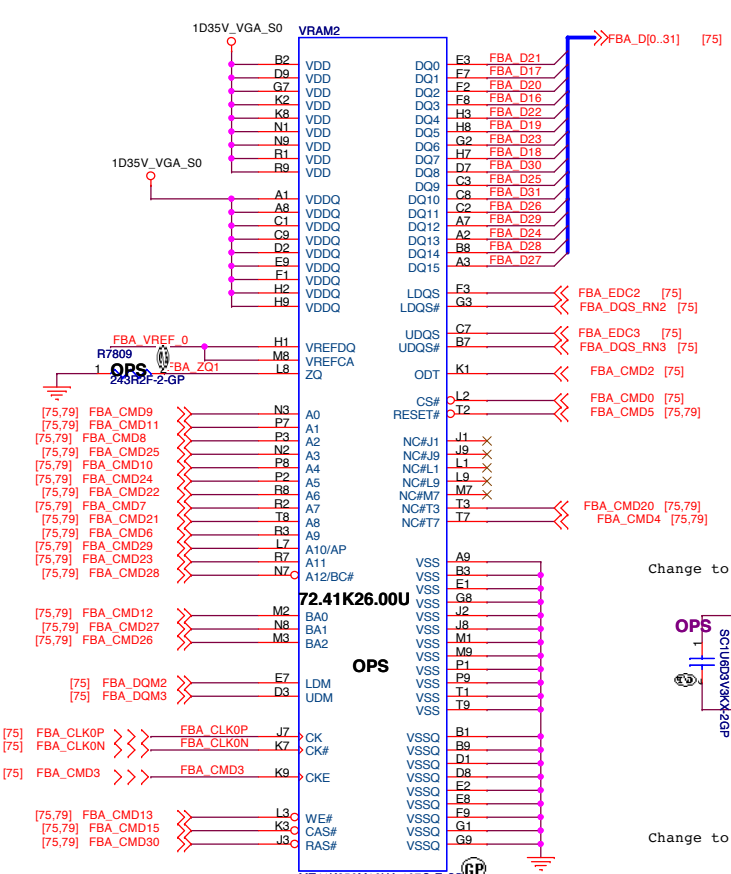
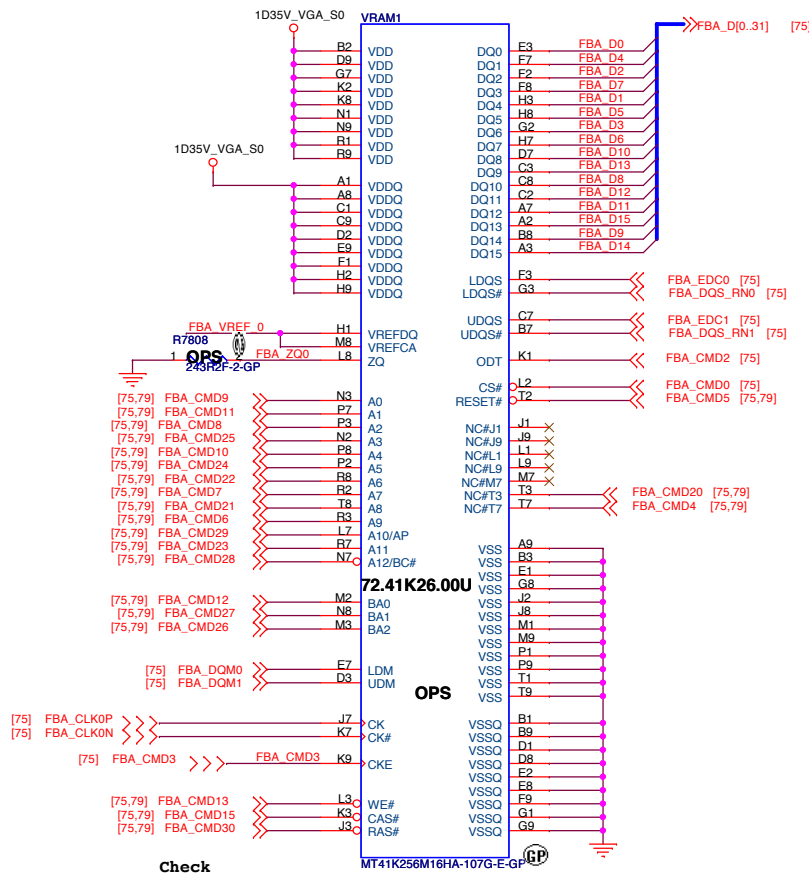
Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

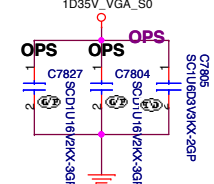
Chip

Chip	N15V-GM	N15V-GT
Device ID	N15V-GM	N15V-GT
Memory interface	sDDR3	sDDR3
Package	595 ball BGA 23x23mm	408 ball BGA 29 x 29 mm

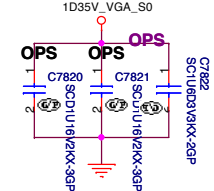




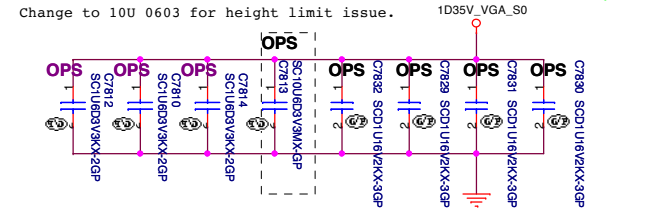
Place close VRAM1 VDD ball



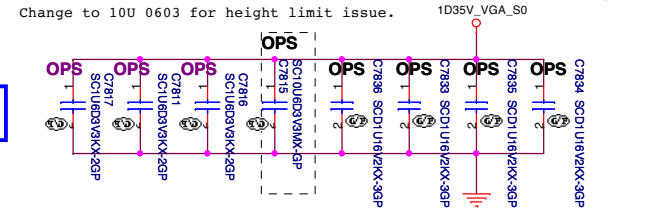
Place close VRAM2 VDD ball



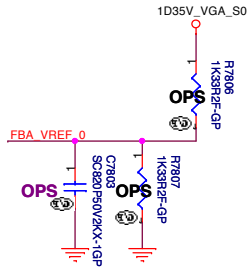
Place close VRAM1VDDQ ball



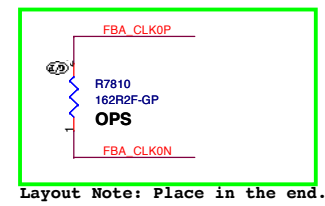
Place close VRAM1VDDQ ball



Frame Buffer Partition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

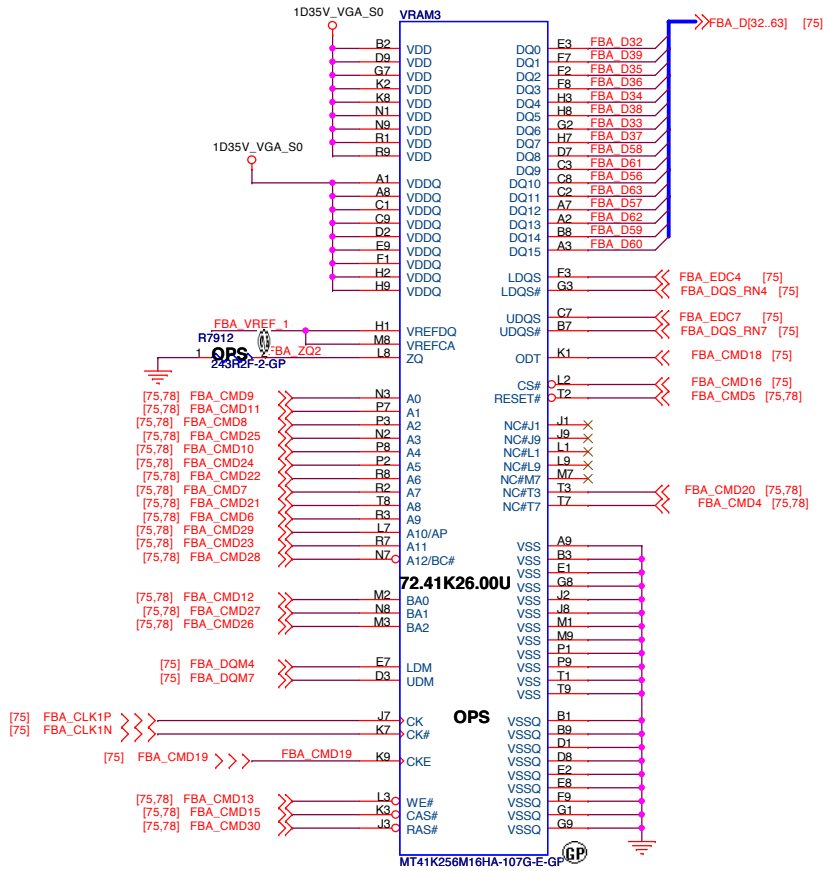
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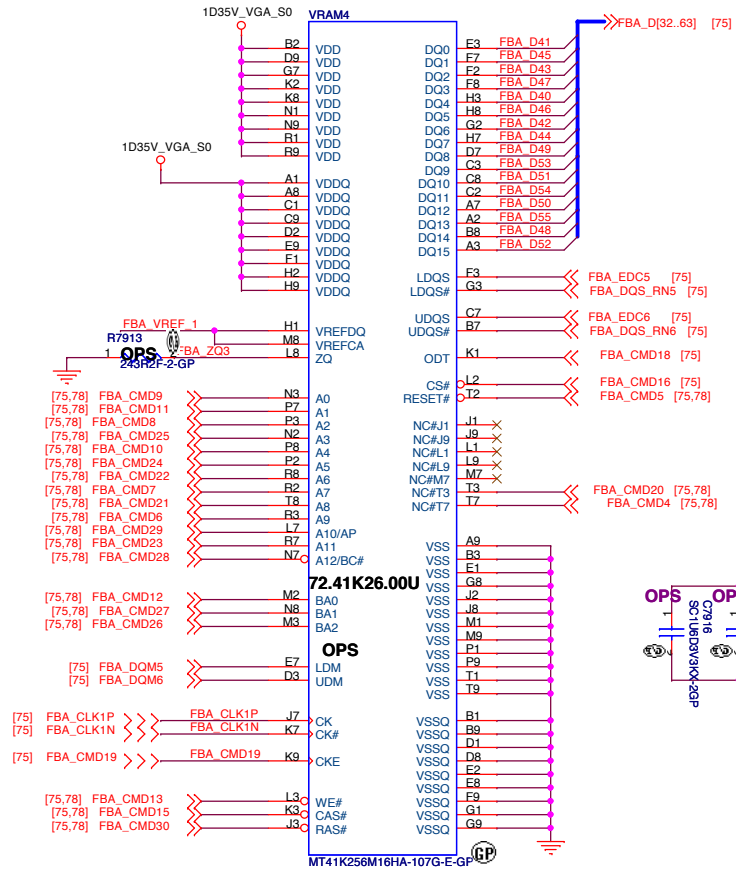
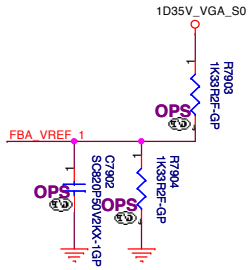
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Title: **GPU-VRAM1,2 (1/4)**

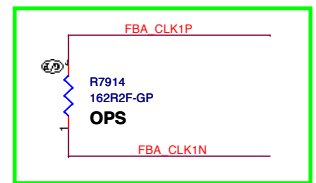
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Frame Buffer Partition A-Lower Half

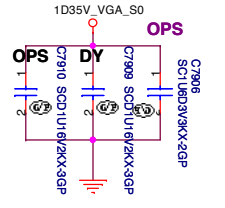


FBCLK Termination place on VRAM side

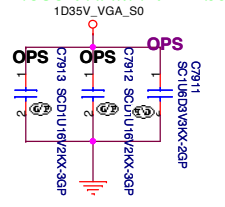


Layout Note: Place in the end.

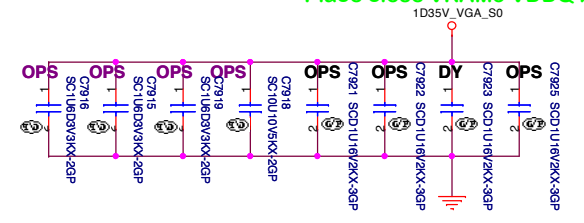
Place close VRAM3 VDD ball



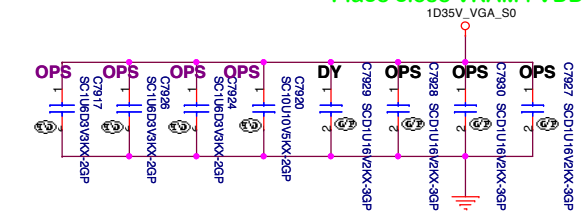
Place close VRAM4 VDD ball

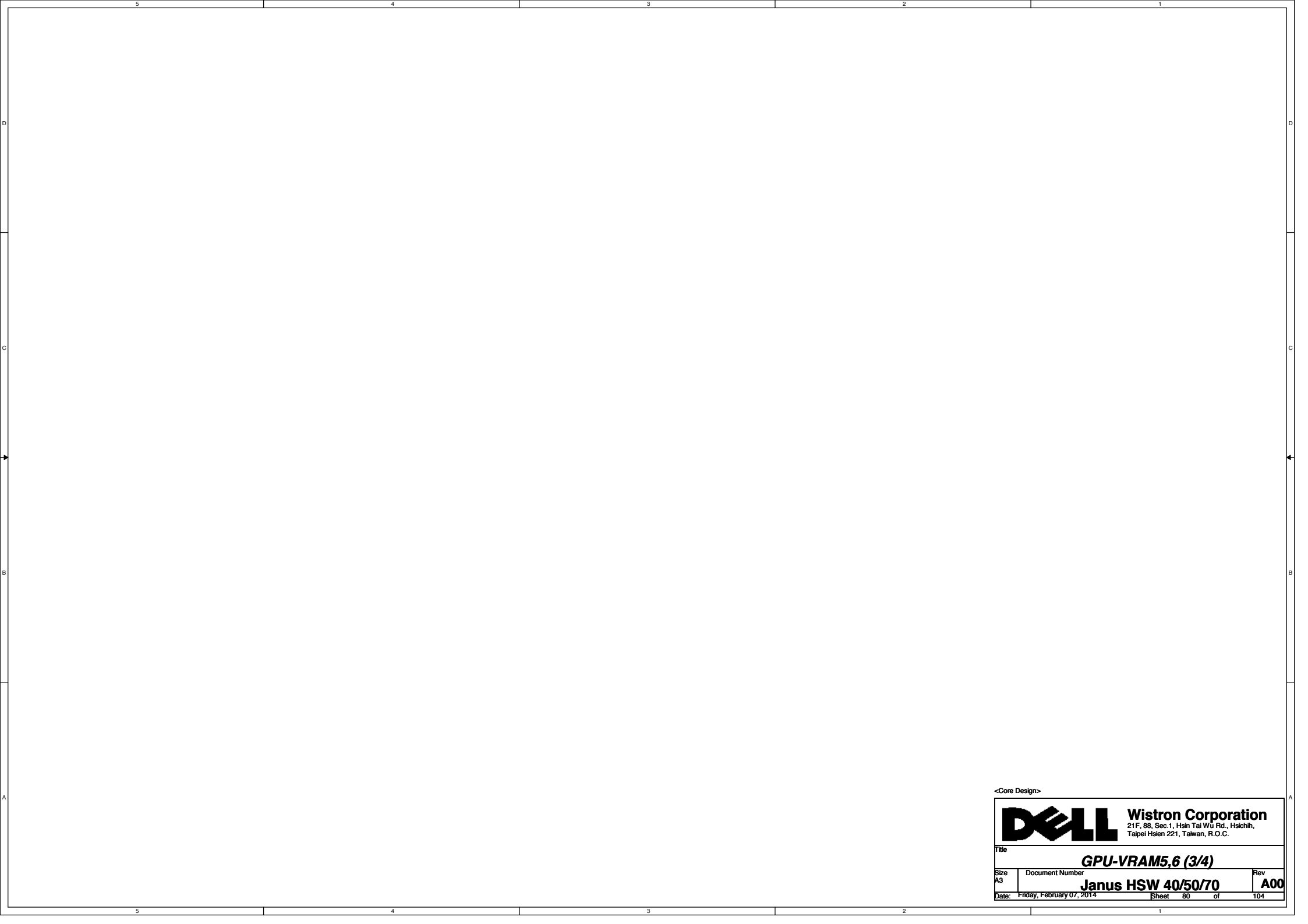


Place close VRAM3 VDDQ ball




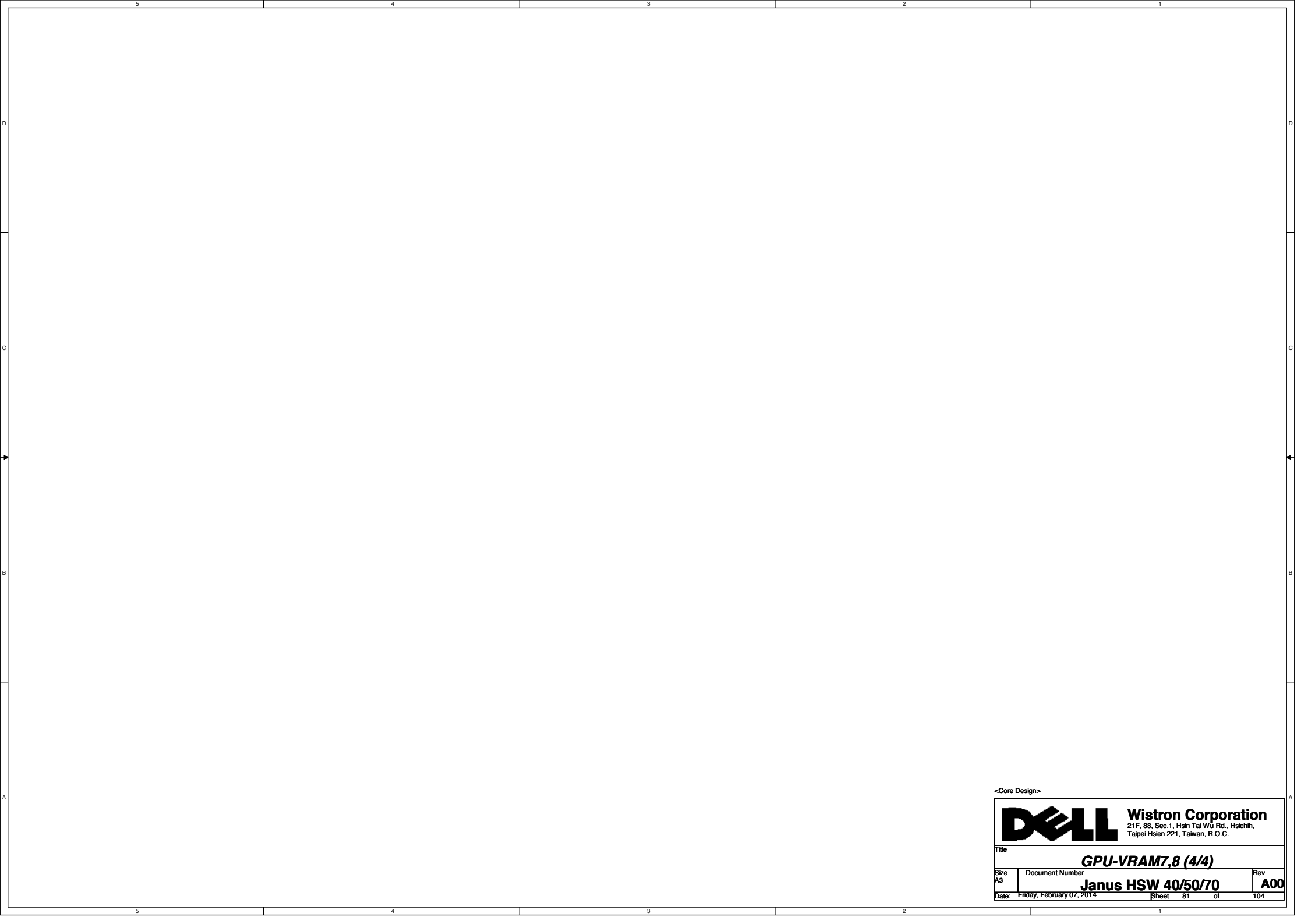
Place close VRAM4 VDDQ ball






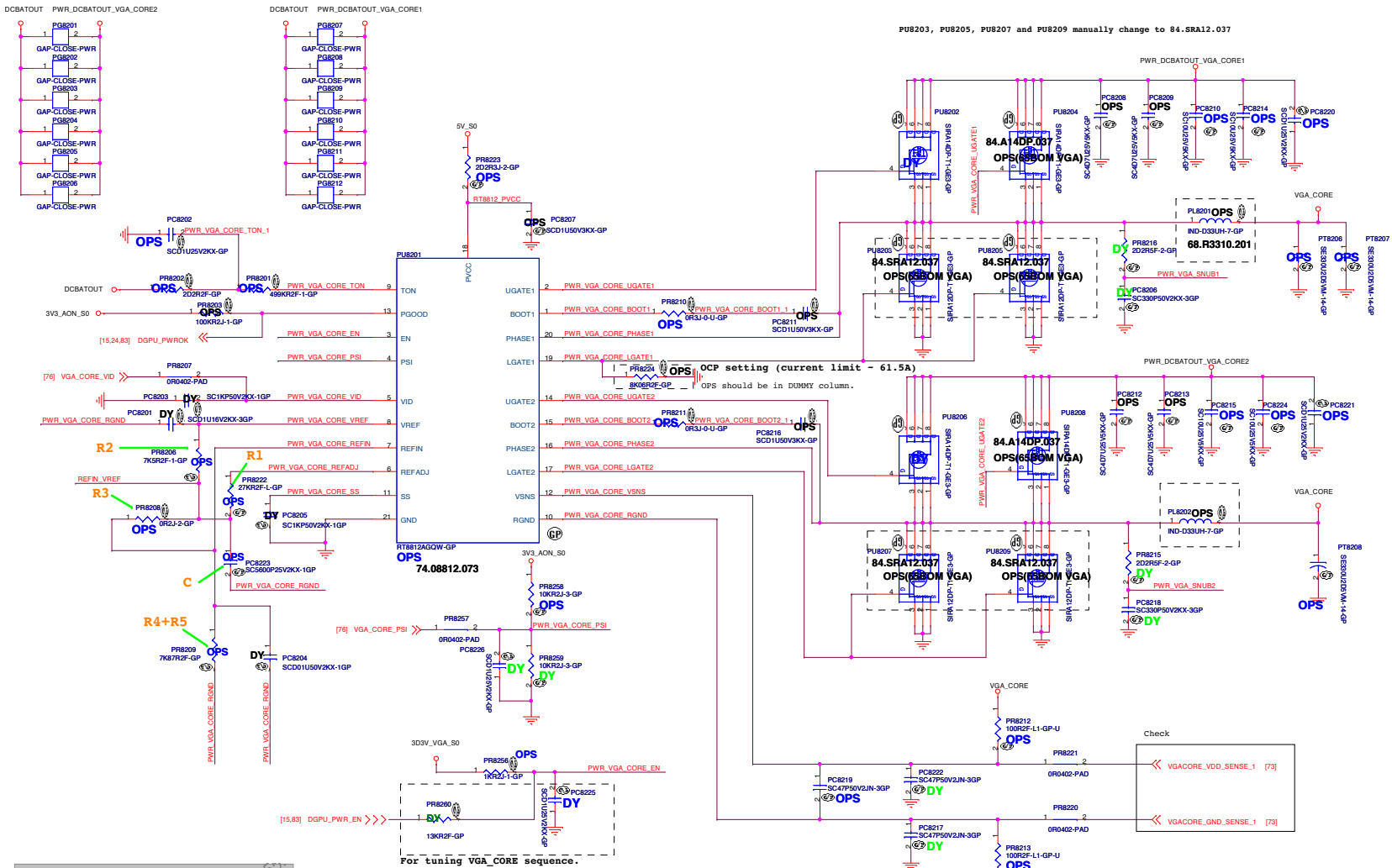
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GPU-VRAM7,8 (4/4)			
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PUR203, PUR205, PUR207 and PUR209 manually change to 84.SRA12.037

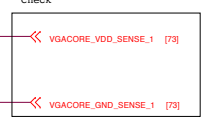
N15V_GM_S
Config D
Design Current=33.5A
56.65A <OPC< 66.7A

Component	N15V-GM-S Config D	N15-GM-S Config B
R1 (PR8222)	27K 64.27025.60L	20K 64.20025.60L
R2 (PR8206)	7.5K 64.75015.60L	20K 64.20025.60L
R3 (PR8208)	0 63.80034.10L	2K 64.20015.60L
R4+R5 (PR8209)	7.375K 64.78715.60L	18K 64.18025.60L
C (PC8223)	5.6pF 78.56222.2FL	2.7pF 78.27224.2FL

PWM-VID Specification	Config A	Config B	Config C	Config D
Vmin	0.5	0.5	0.5	0.5
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV 6.25	6.25	25	12.5
Number of Voltage Levels N	level 96	96	20	20
PWM Frequency F _{min}	MHz 1.125	0.676	0.676	0.676
PWM Minimum Pulse Width T _{min}	ns 9.26	74	74	74
VID Transient Time T	<-100	<-100	<-100	<-100

Component Value	Config A	Config B	Config C	Config D
R1 (1k)	KΩ 39	20	39	27
R2 (1k)	KΩ 39	20	30	7.5
R3 (1k)	KΩ 1.5	2	3	0
R4 (1k)	KΩ 30	18	24	6.2
R5 (1k)	KΩ 1.5	0	3	1.74
C	nF 1.5	2.7	1.8	5.6

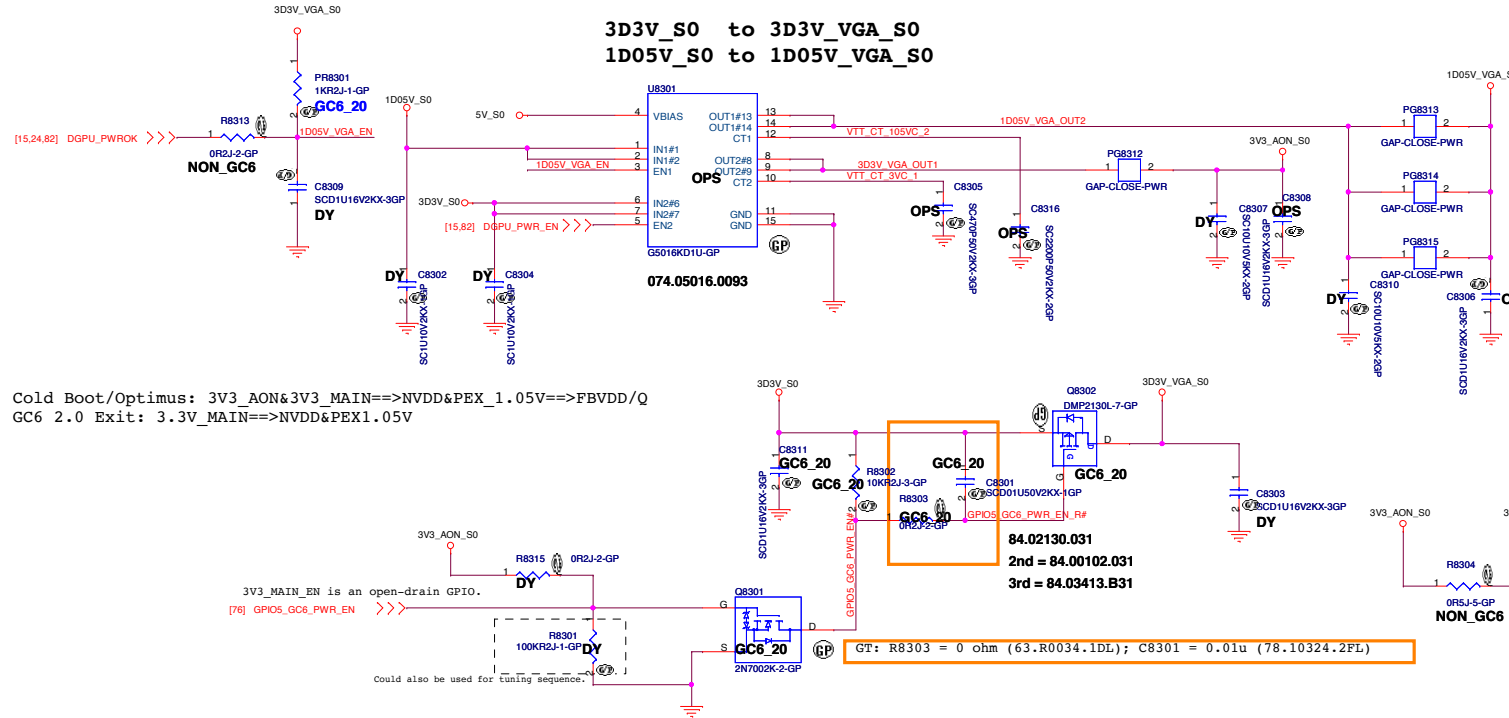
I/P cap: 10u 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHORE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
 O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
 H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm4.5Vgs/ 84.A14DP.037
 L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm4.5Vgs/ 84.SRA06.037



3D3V_VGA_S0 1D05V_VGA_S0

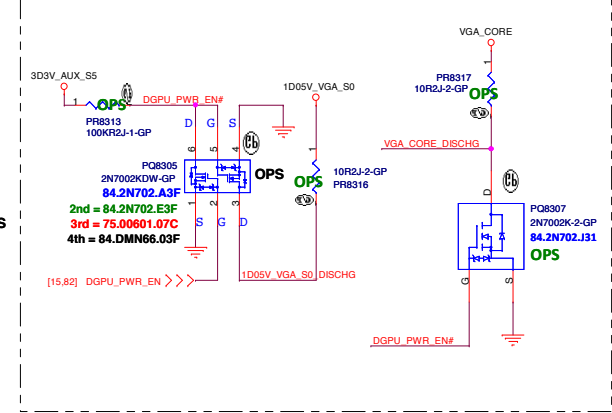
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0 1D05V_S0 to 1D05V_VGA_S0

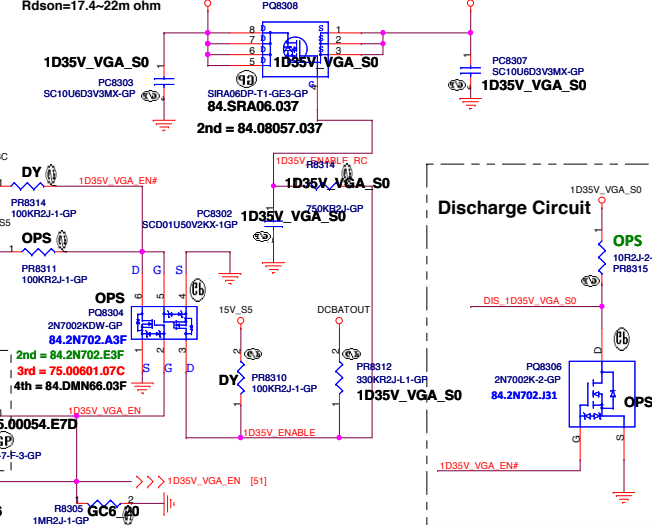


Cold Boot/Optimus: 3V3_AON&3V3_MAIN=>NVDD&PEX_1.05V=>FBVDD/Q
GC6 2.0 Exit: 3.3V_MAIN=>NVDD&PEX1.05V

VGA_CORE&1D05V_VGA_S0 Discharge Circuit



A04468, SO-8
Id=?A, Qg=9-12nC
Rdson=17.4-22m ohm



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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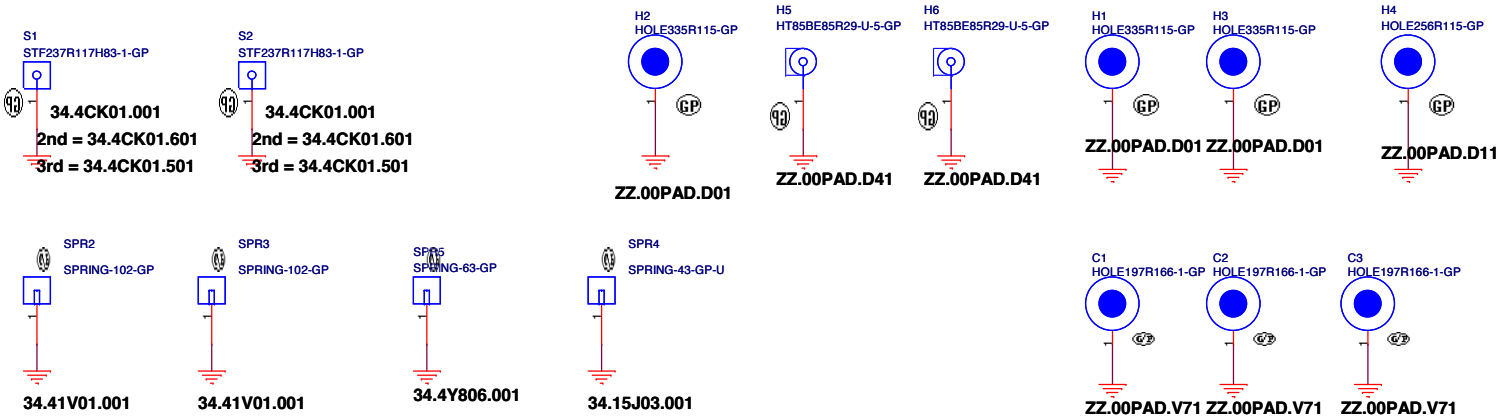
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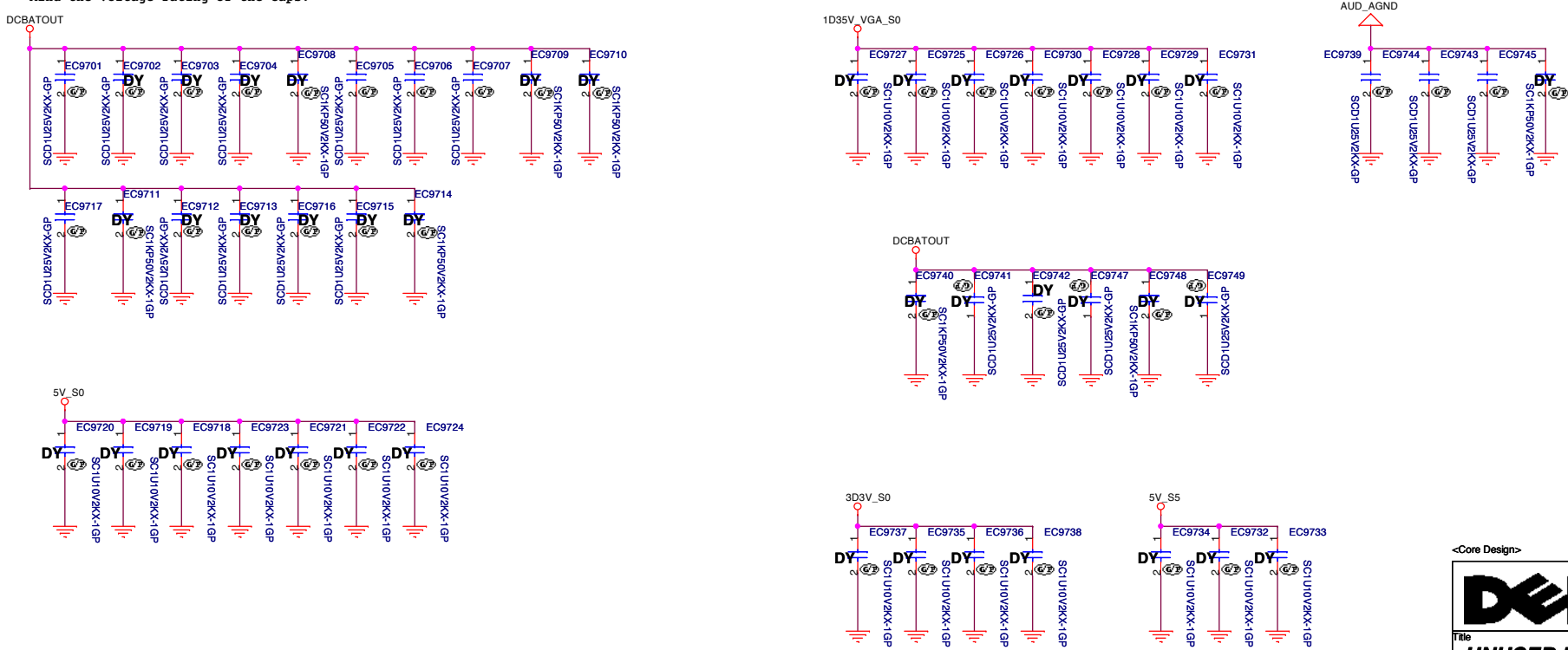
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SSID = Mechanical



SSID = EMI

Mind the voltage rating of the caps.



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Title: **UNUSED PARTS/EMI Capacitors**

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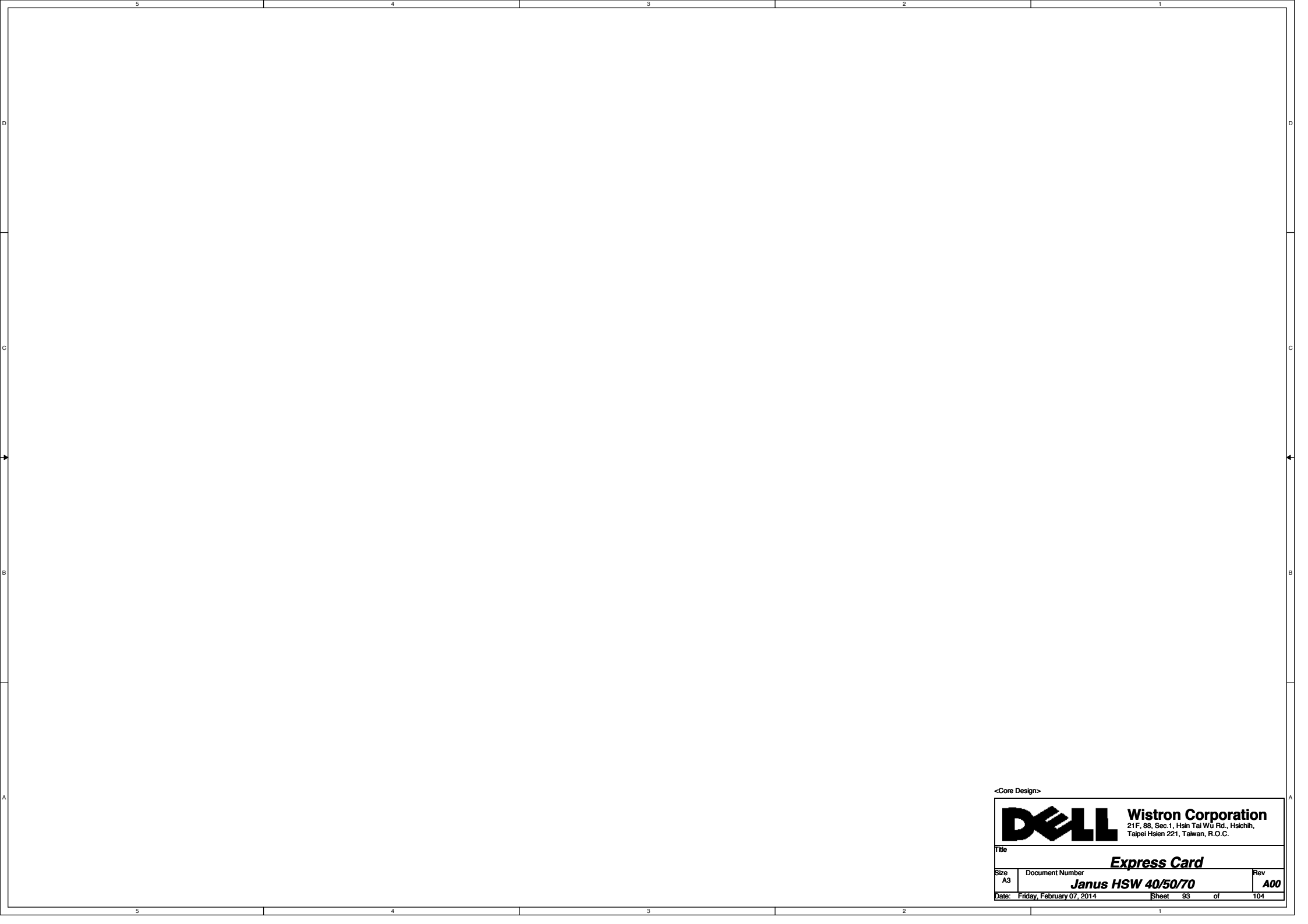
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Express Card			
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LVDS Switch		
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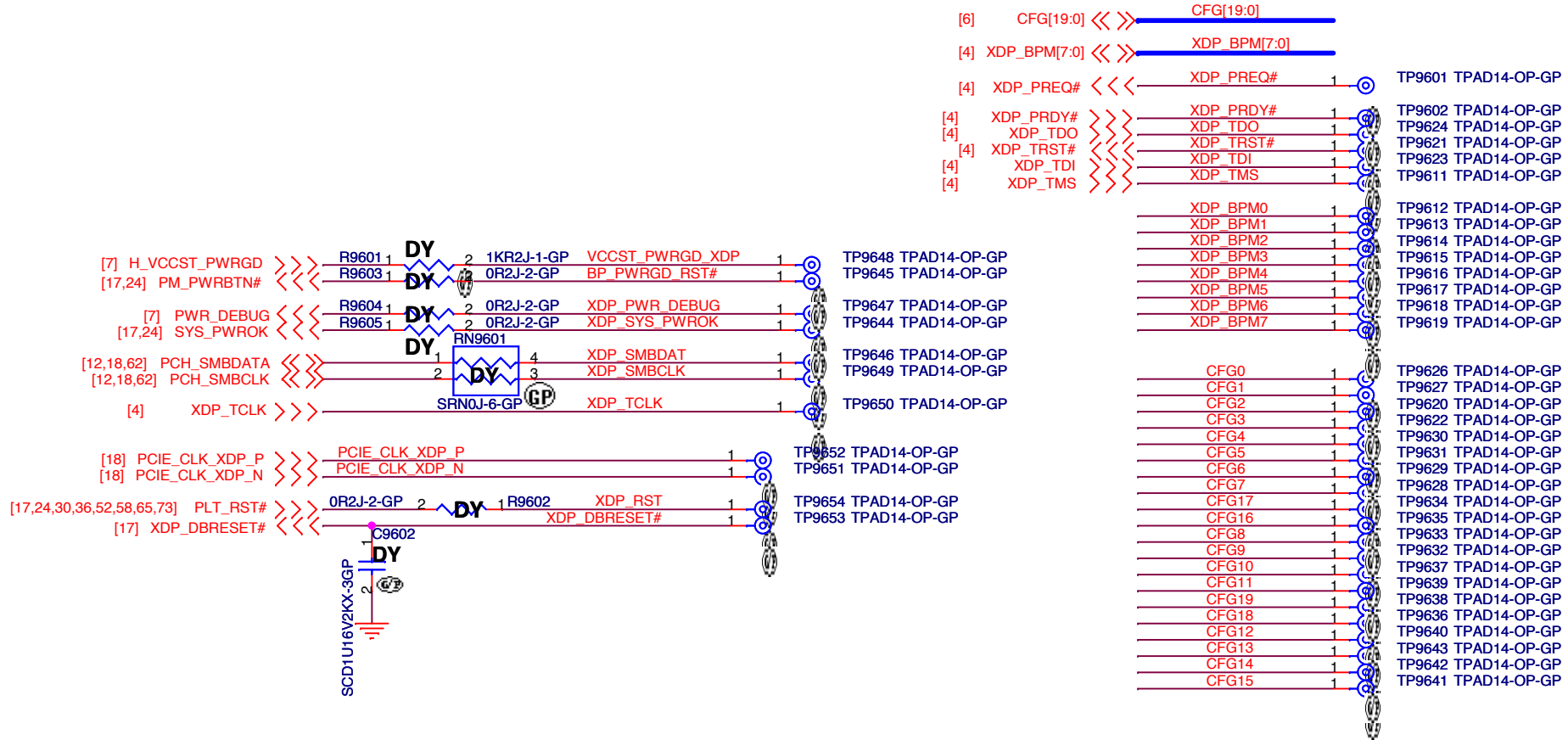
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Title		
CRT Switch		
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SSID = XDP

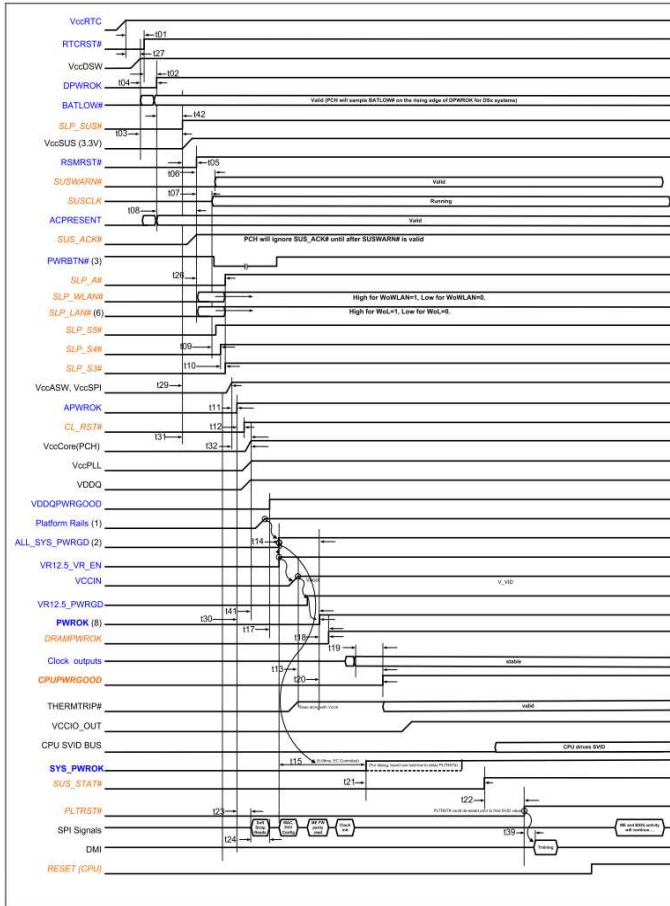
CPU XDP



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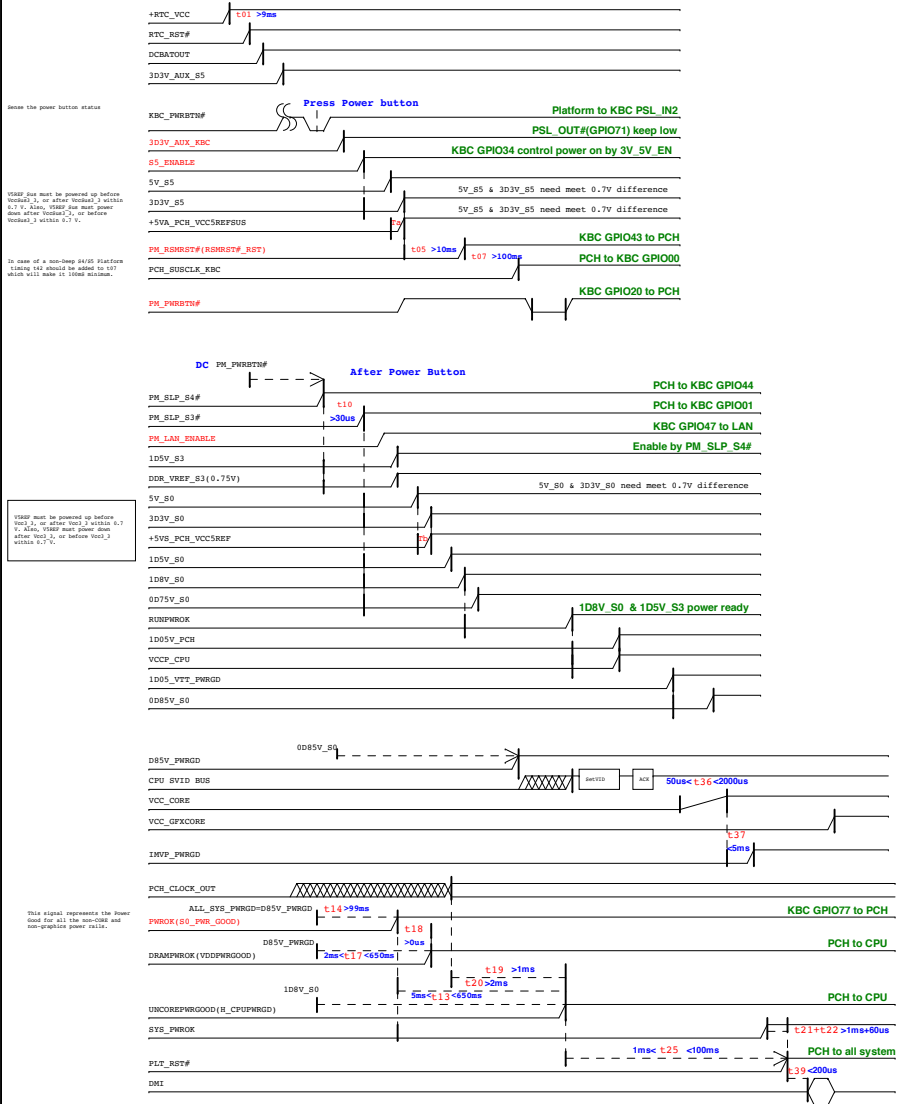
DELL		Wistron Corporation	
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Title			
CPU/PCH XDP			
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Shark Bay Platform Power Sequence

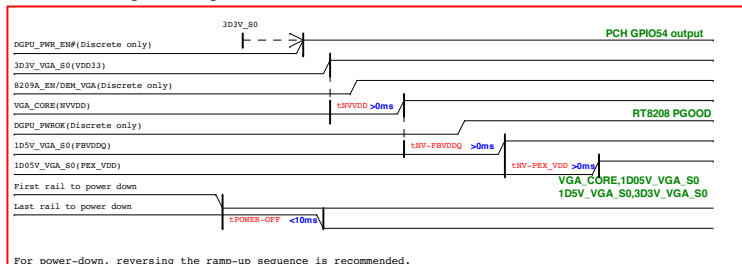


(DC mode)

Red Words: Controlled by RC GPIO

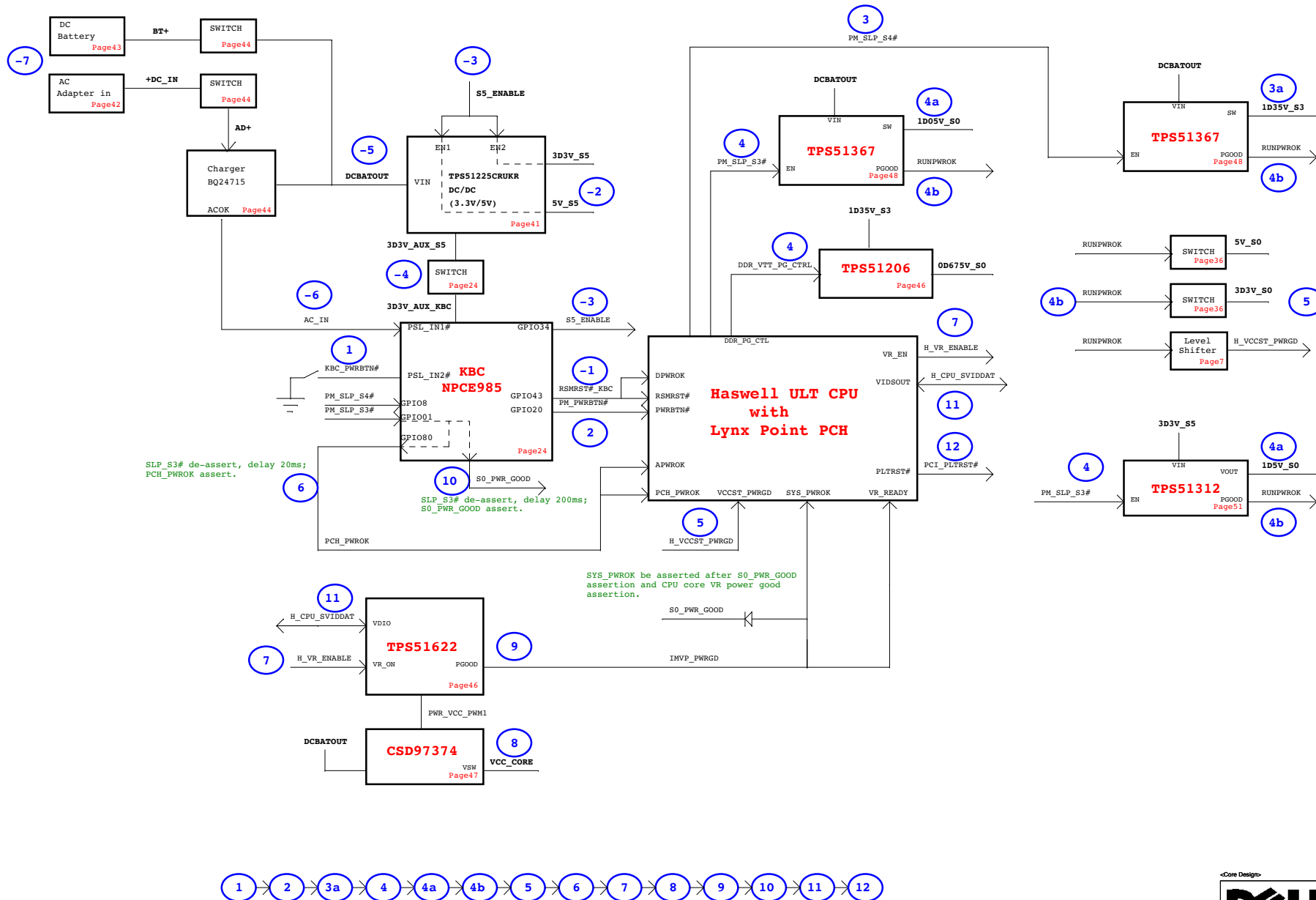


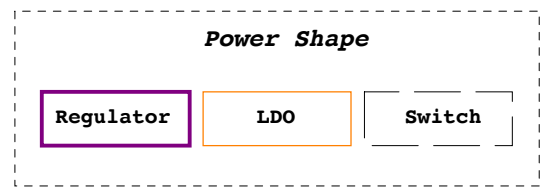
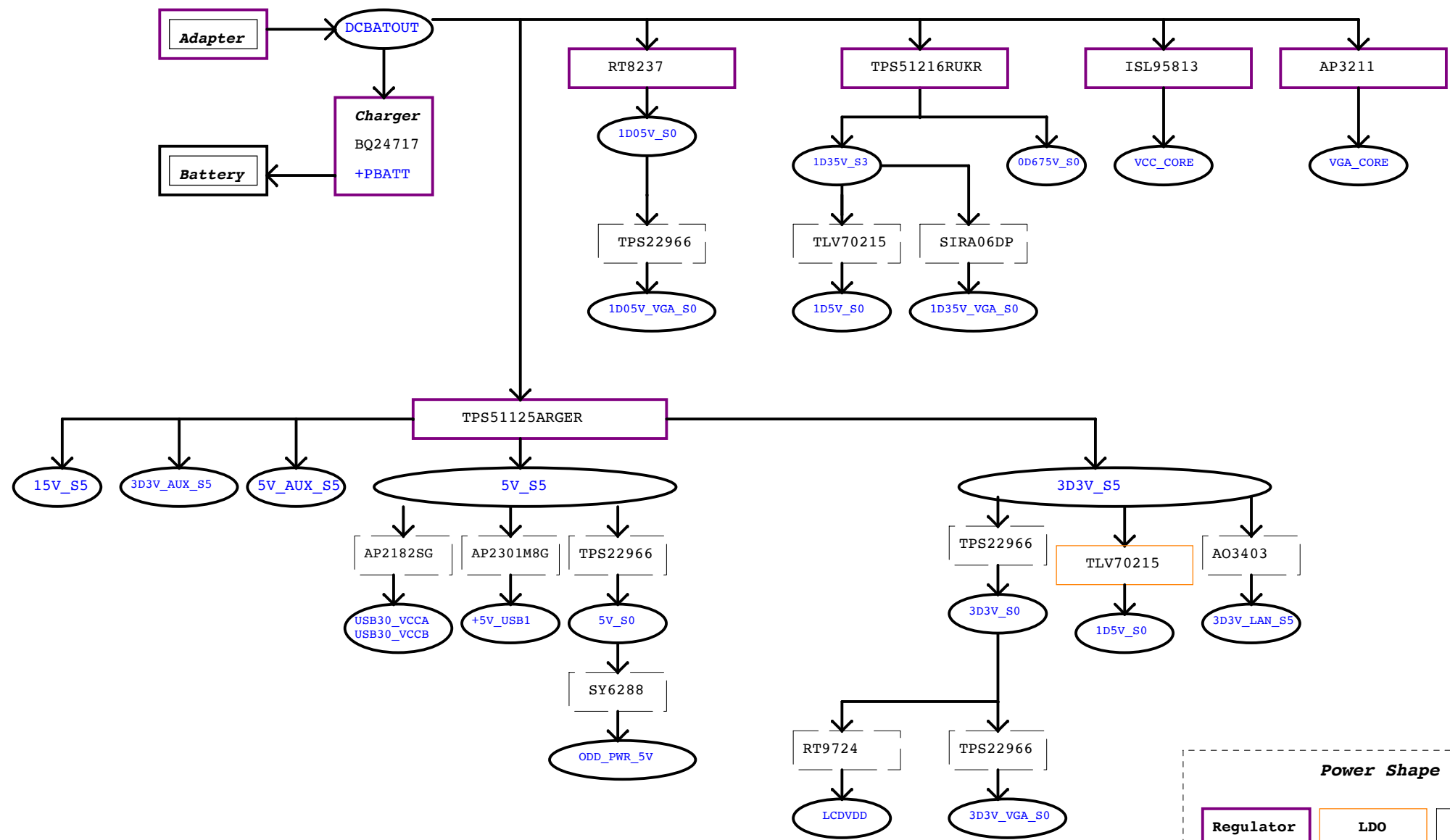
N14P-GT Power-Up/Down Sequence



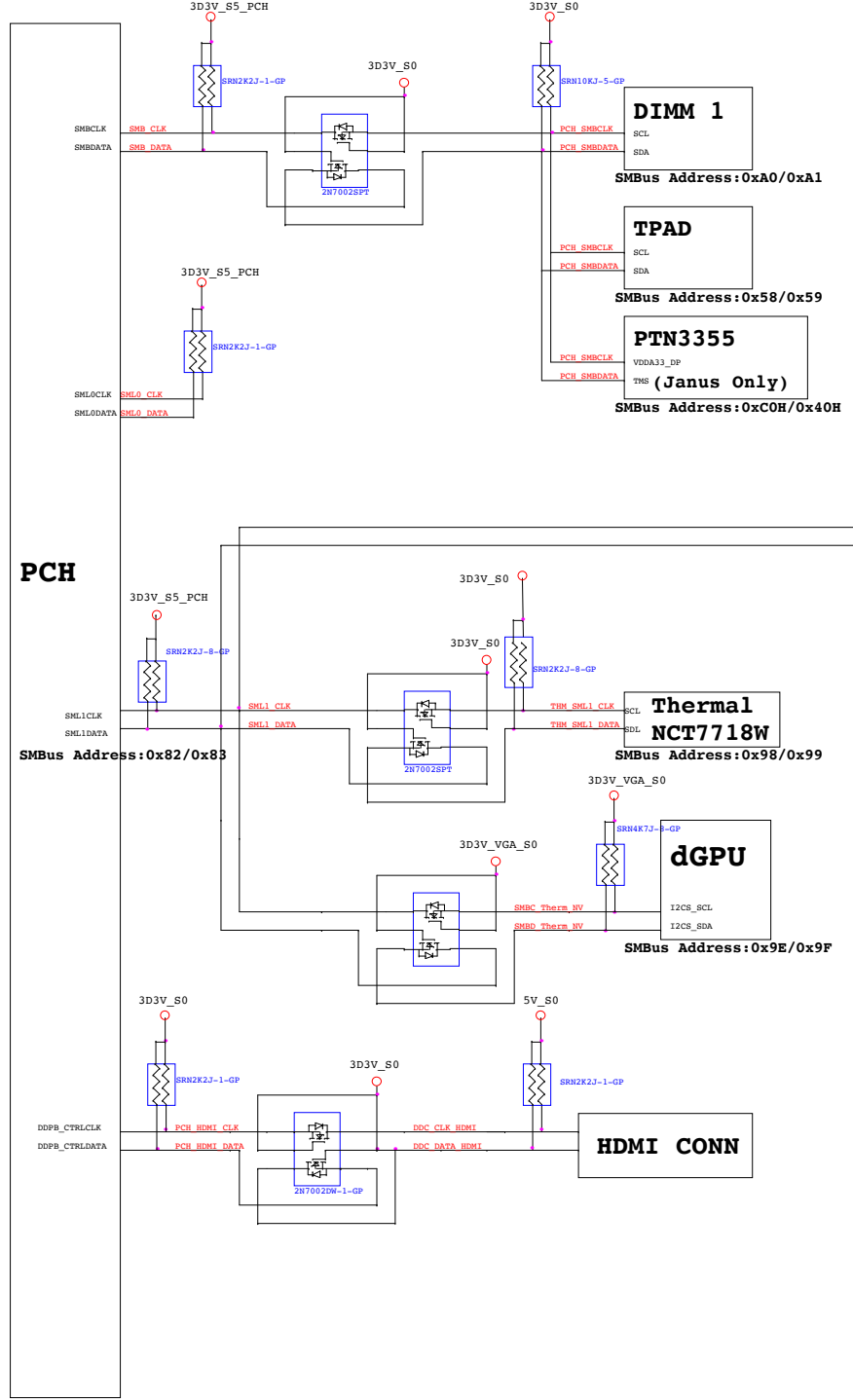
For power-down, reversing the ramp-up sequence is recommended.

Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

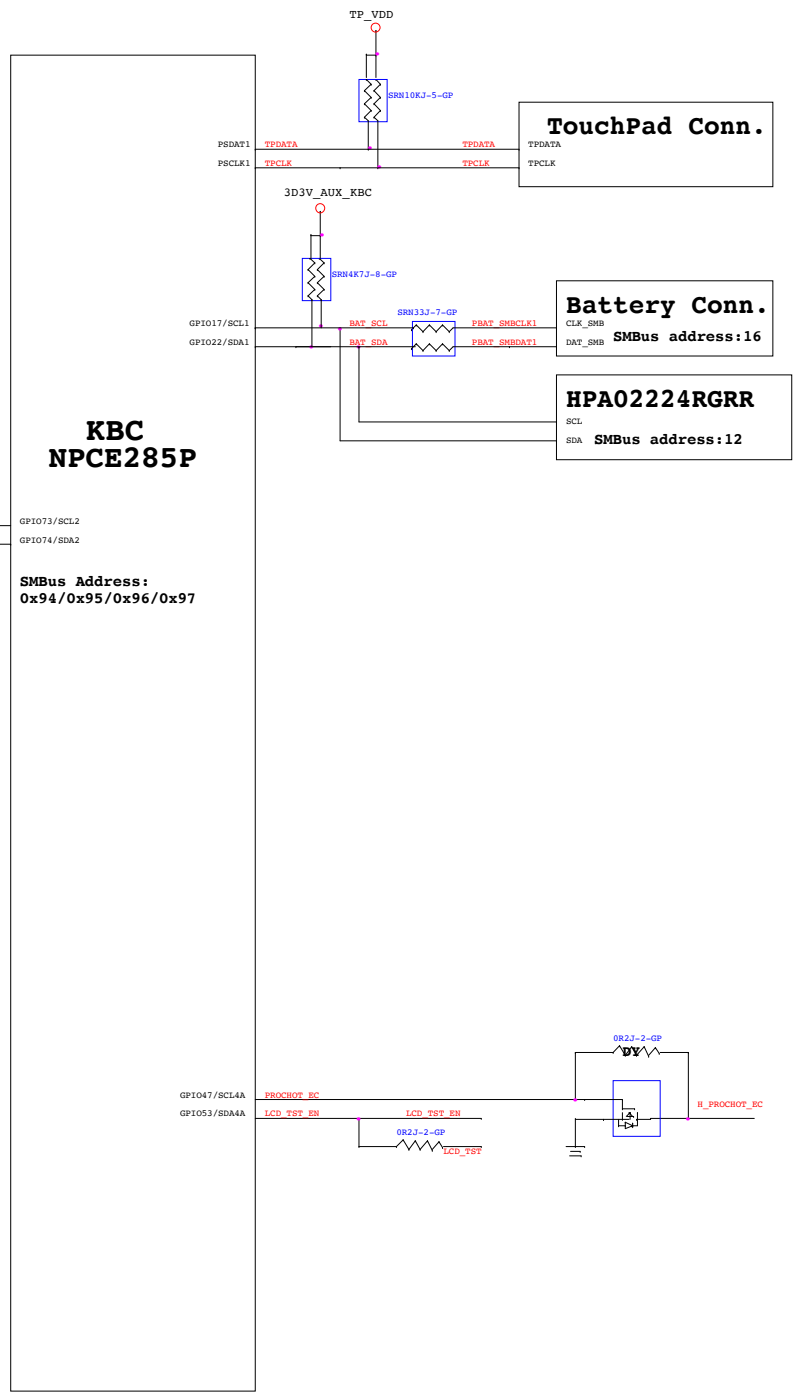




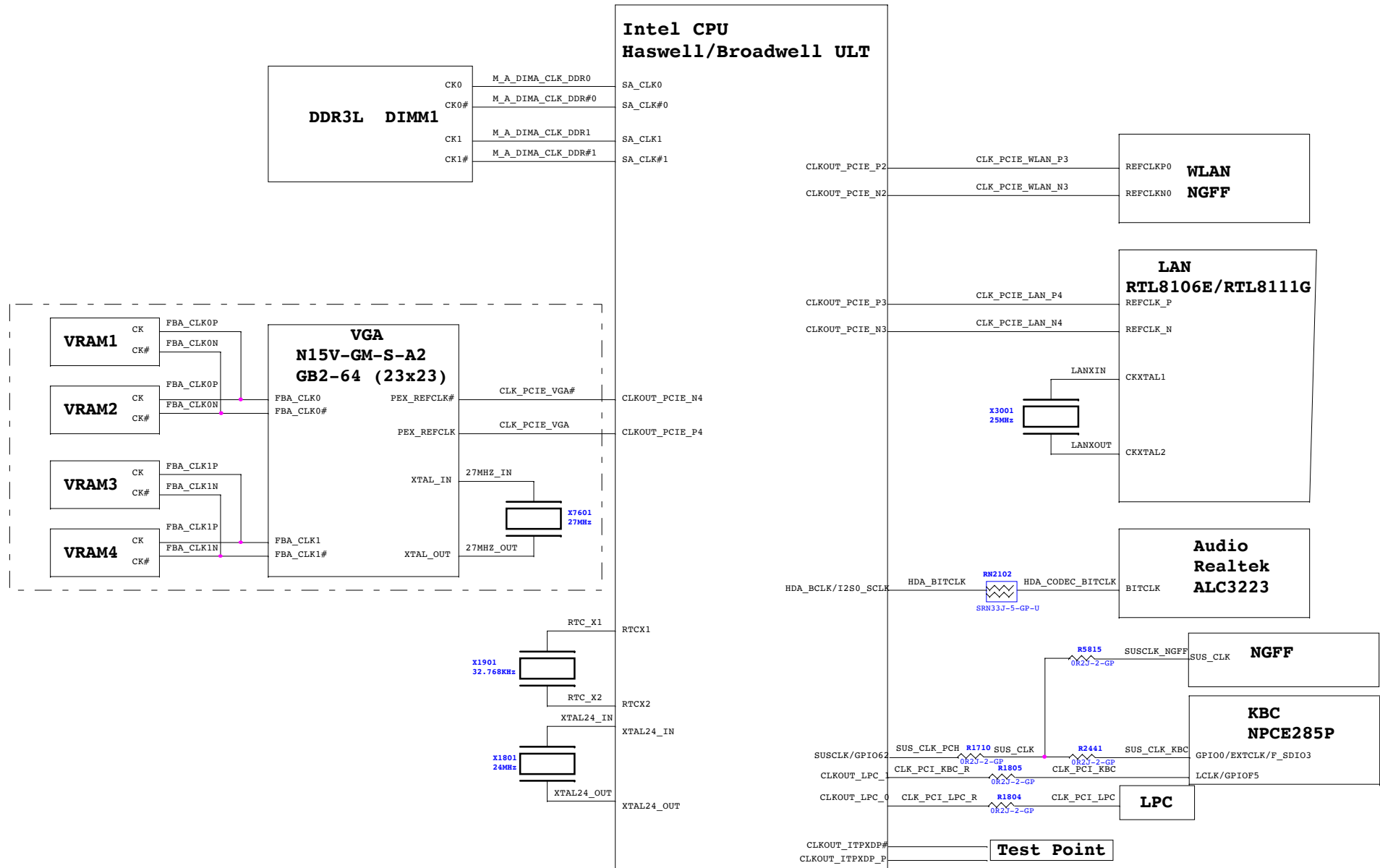
PCH SMBus Block Diagram



KBC SMBus Block Diagram

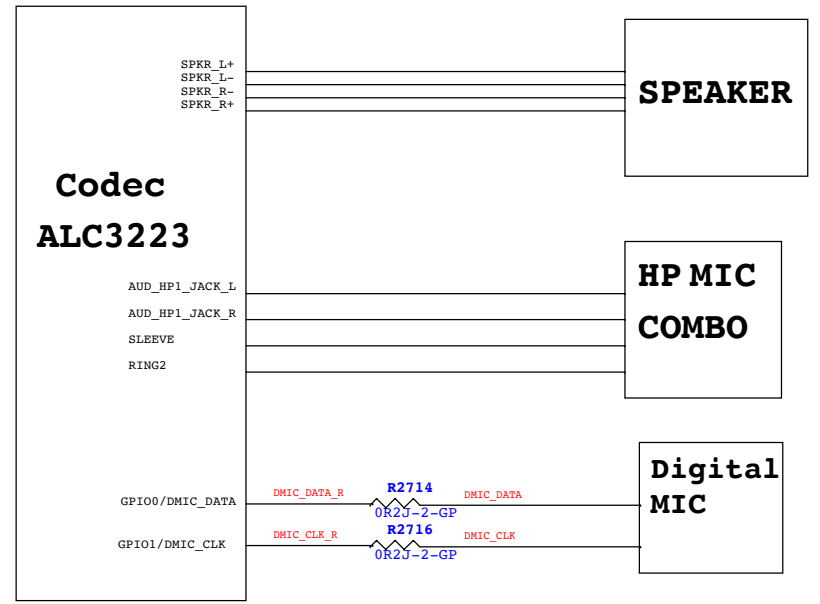
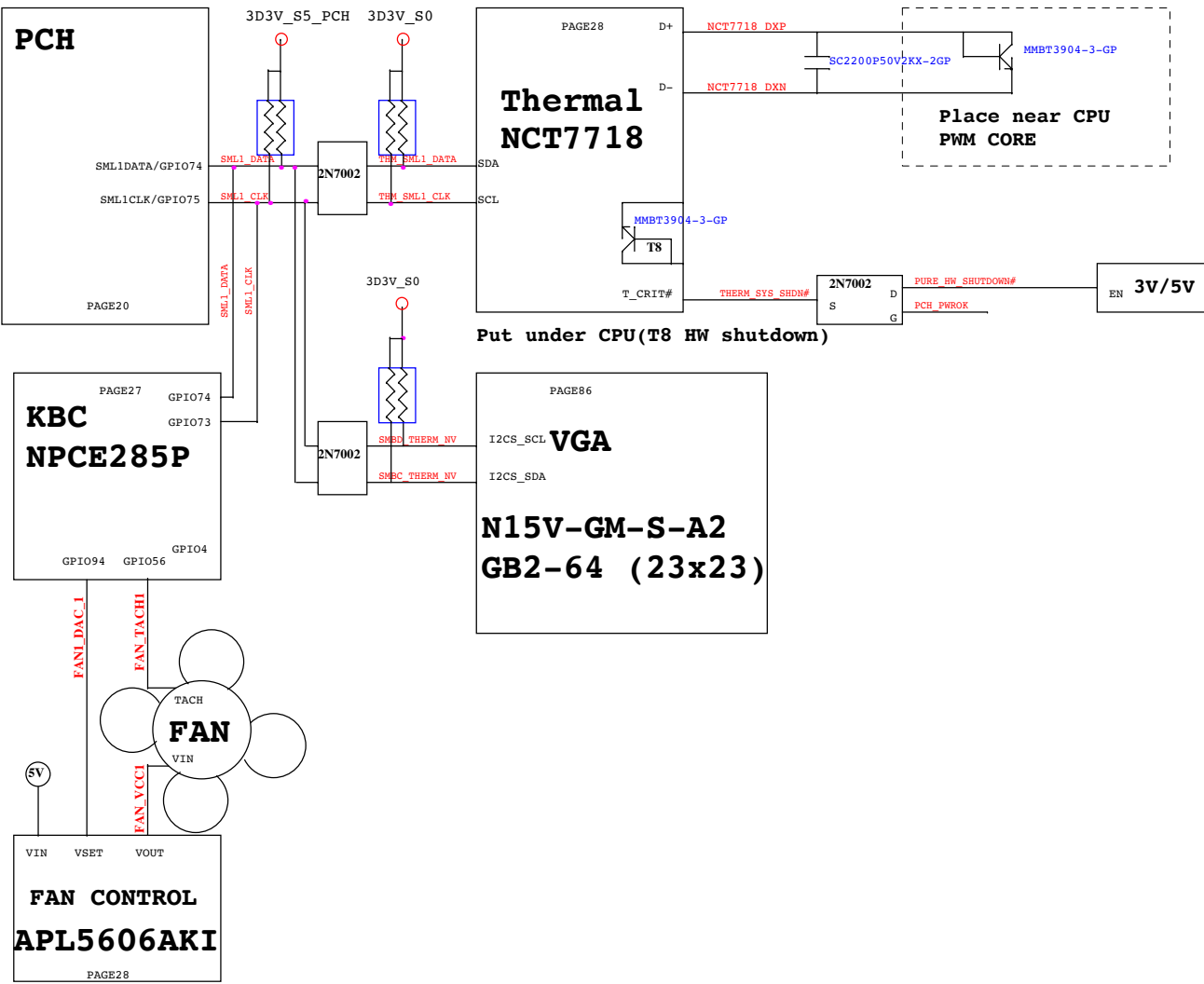


CLK Block Diagram



Thermal Block Diagram

Audio Block Diagram



5

4

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