Hadley15" Schematics Document

Haswell ULT

2013-06-28
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>

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Title	*Cover Page*	
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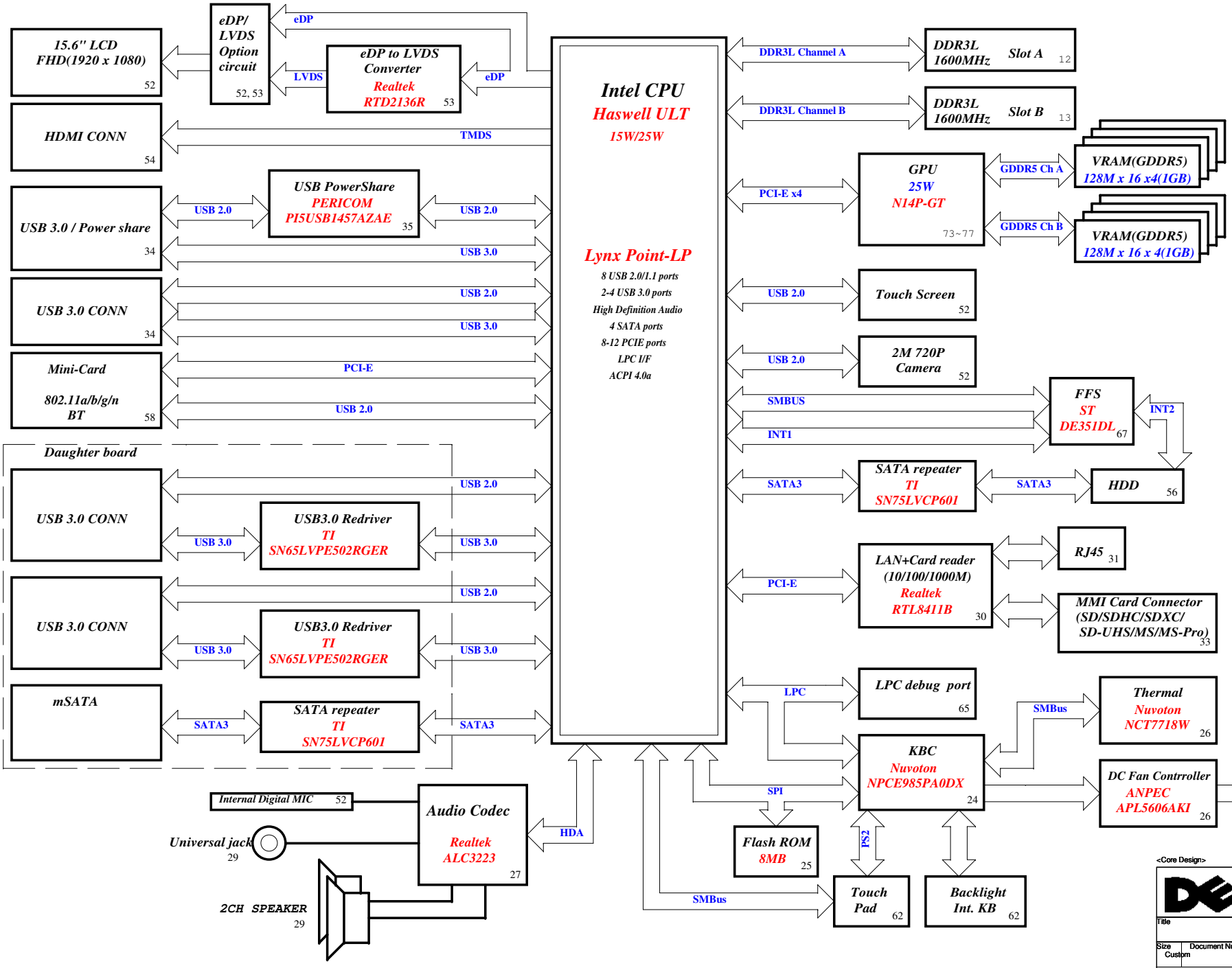
Hadly15 Block Diagram

Project code : 91.47L01.001
PCB P/N : 12311-1
Revision : A00



CHARGER BQ24717 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_CHARGER 3D3V_PWR

CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51216 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

SYSTEM DC/DC NCP81172 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 36, 83	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
3D3V_S0	3D3V_VGA_S0
1D05V_S0	1D05V_VGA_S0
1D35V_S3	1D35V_VGA_S0

LDO TLV70215DBVR 51	
INPUTS	OUTPUTS
3D3V_S5	

PCB LAYER
L1 : TOP
L2 : GND
L3 : Signal
L4 : Signal
L5 : VCC
L6 : Signal
L7 : GND
L8 : Bottom

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Title: *(Reserved)*

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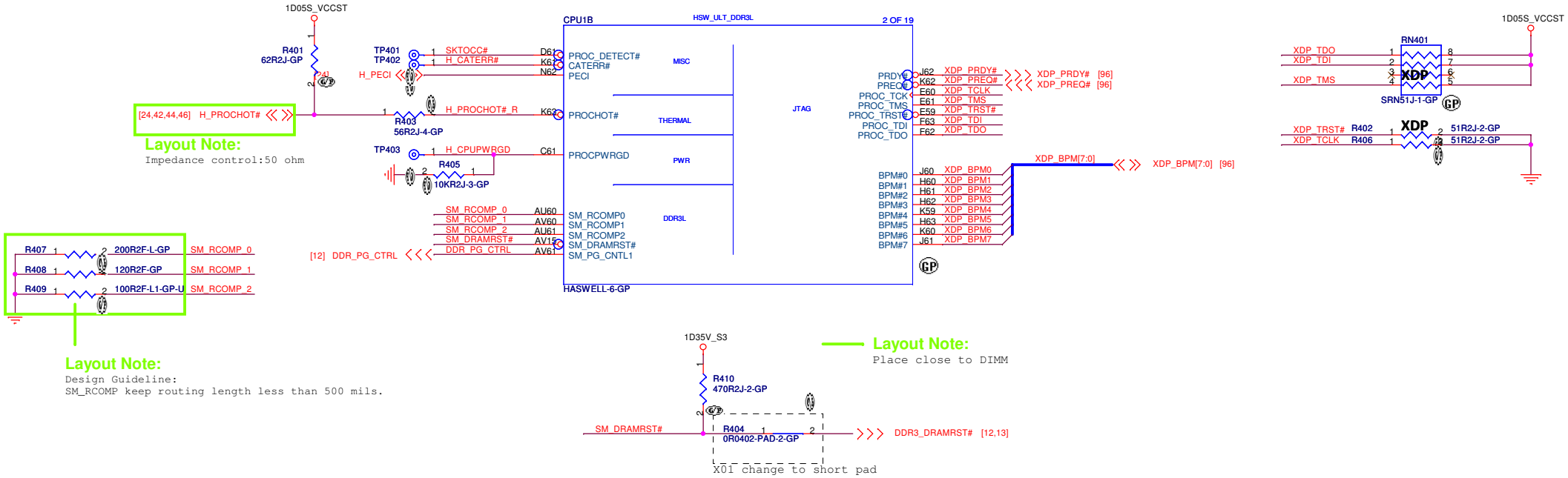
SSID = CPU



<Core Design>

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Title: CPU (THERMAL/CLOCK)

Size	Document Number	Rev
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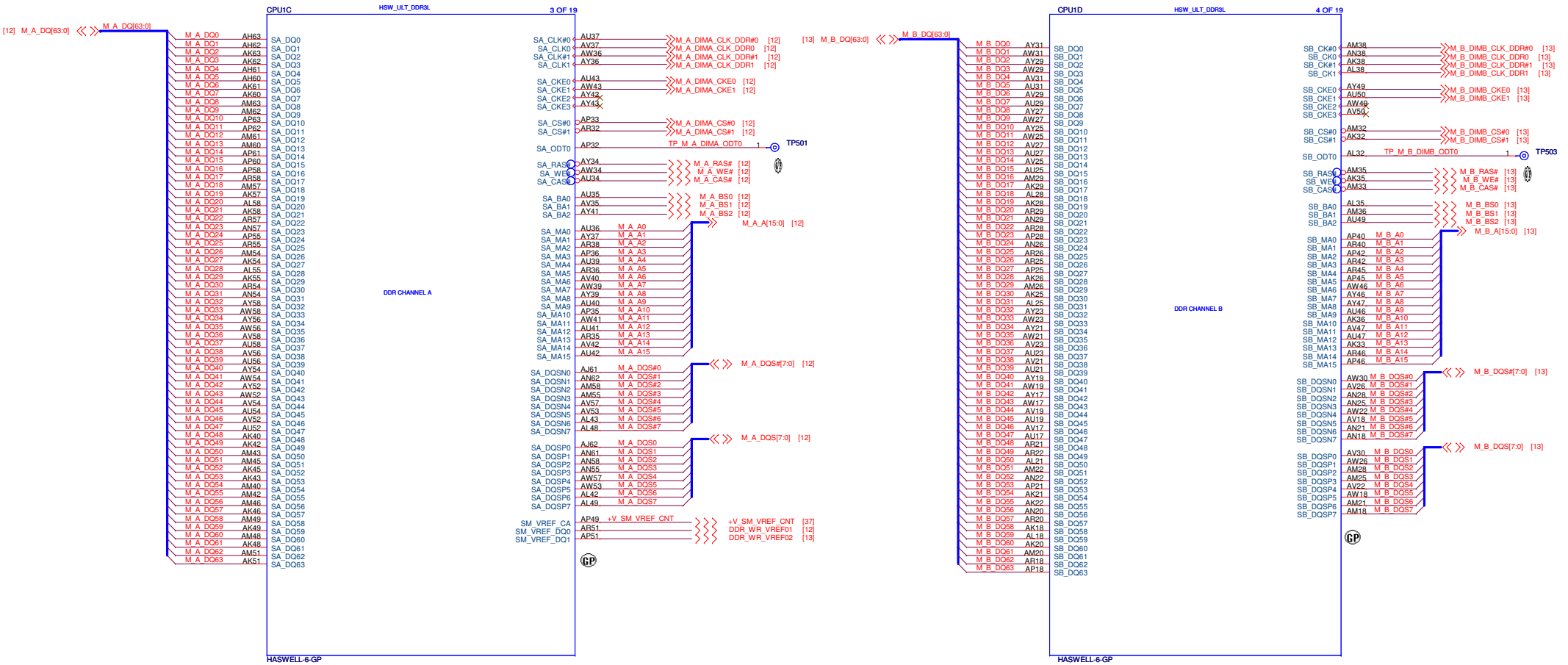
SSID = CPU



<Core Design>

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Title: CPU (DDR)

Size	Document Number	Rev
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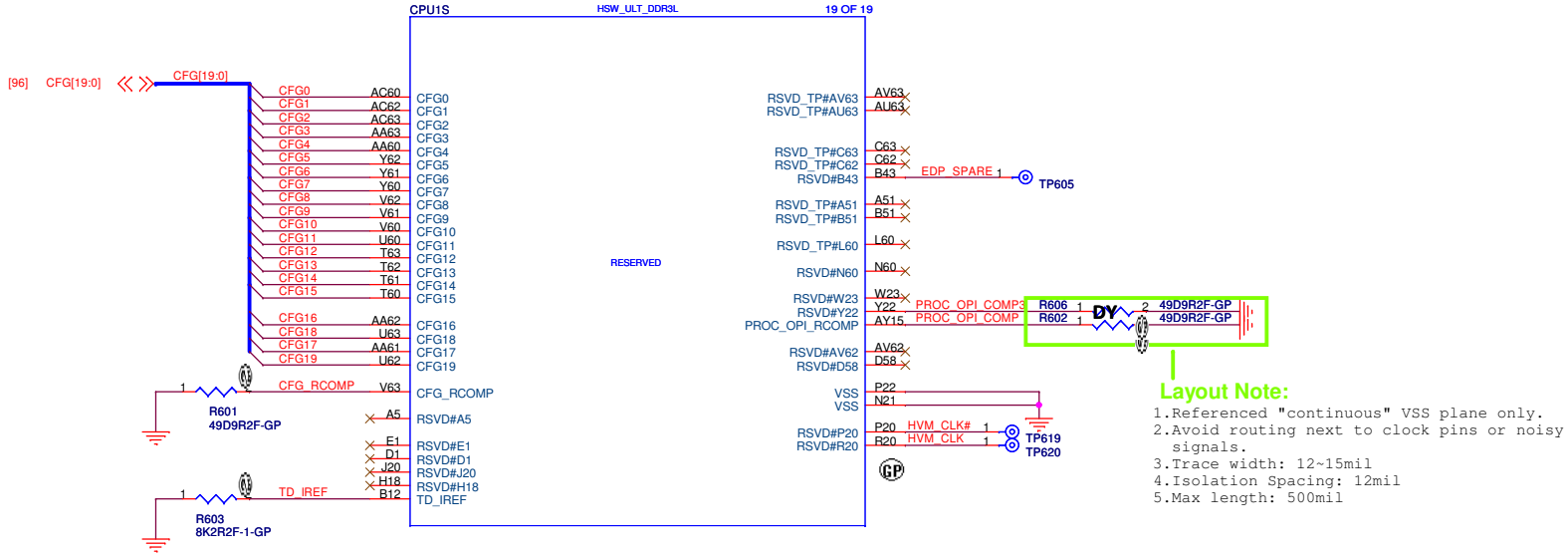
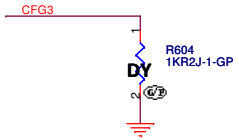
SSID = CPU

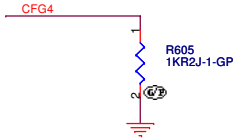


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)

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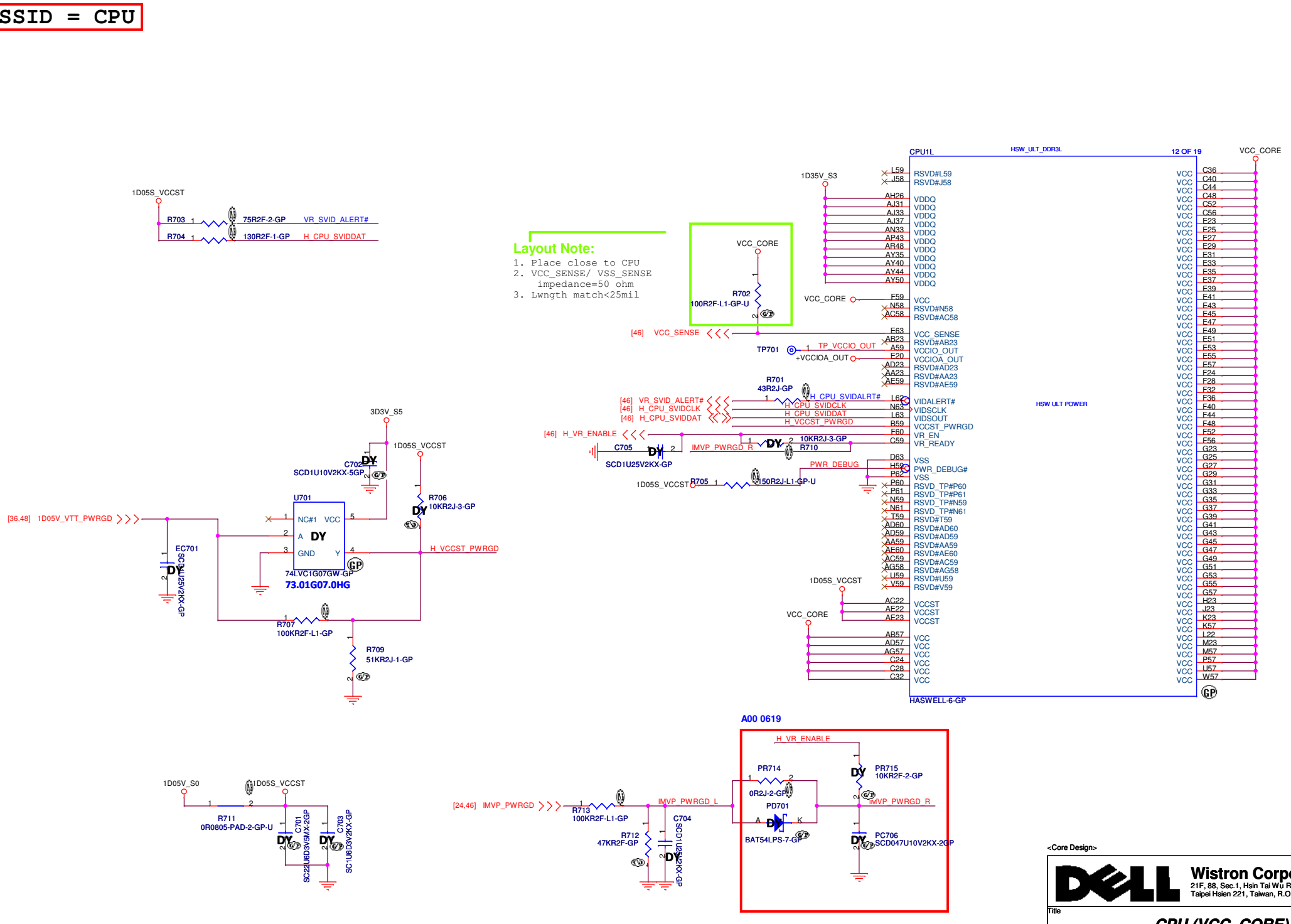
SSID = CPU



<Core Design>

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Title: CPU (VCC_CORE)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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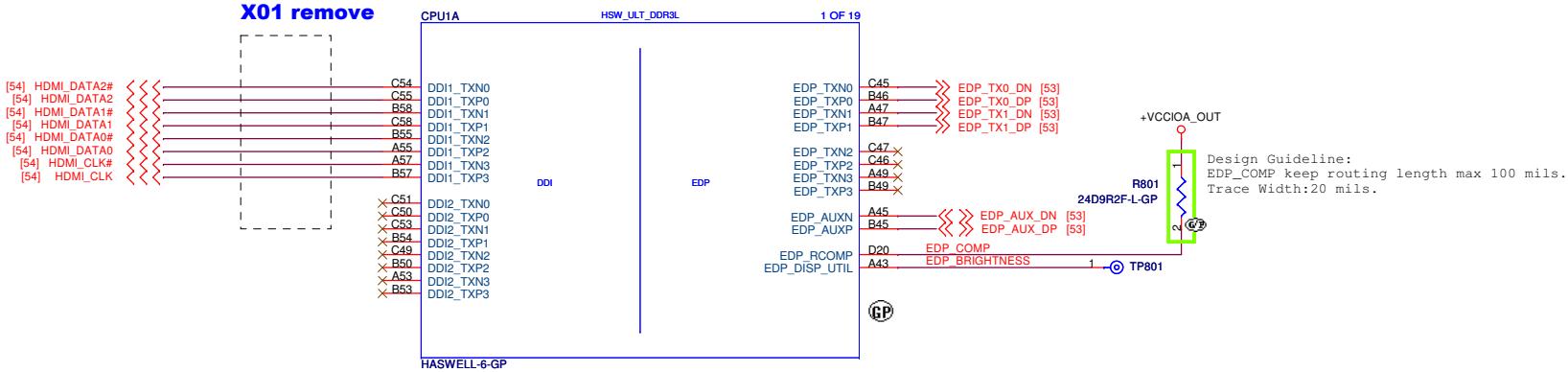
SSID = CPU

HDMI

X01 remove



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Title: CPU (DDI/EDP)

Size	Document Number	Rev
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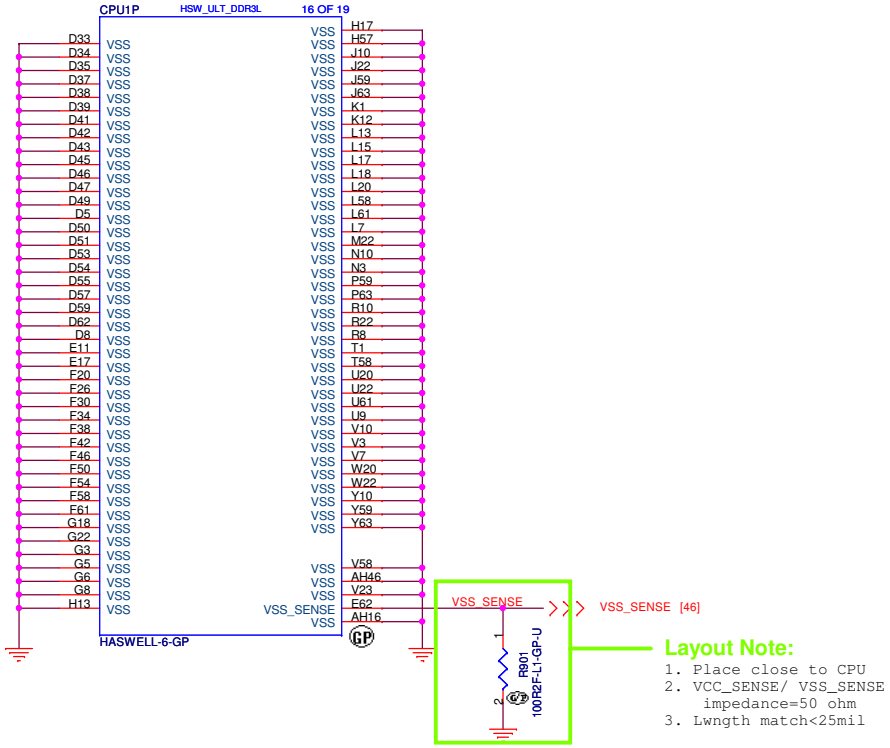
SSID = CPU



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Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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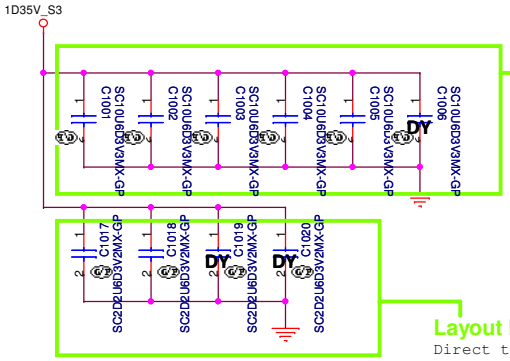
SSID = CPU



Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls

<Core Design>

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Title	CPU(Power CAP1)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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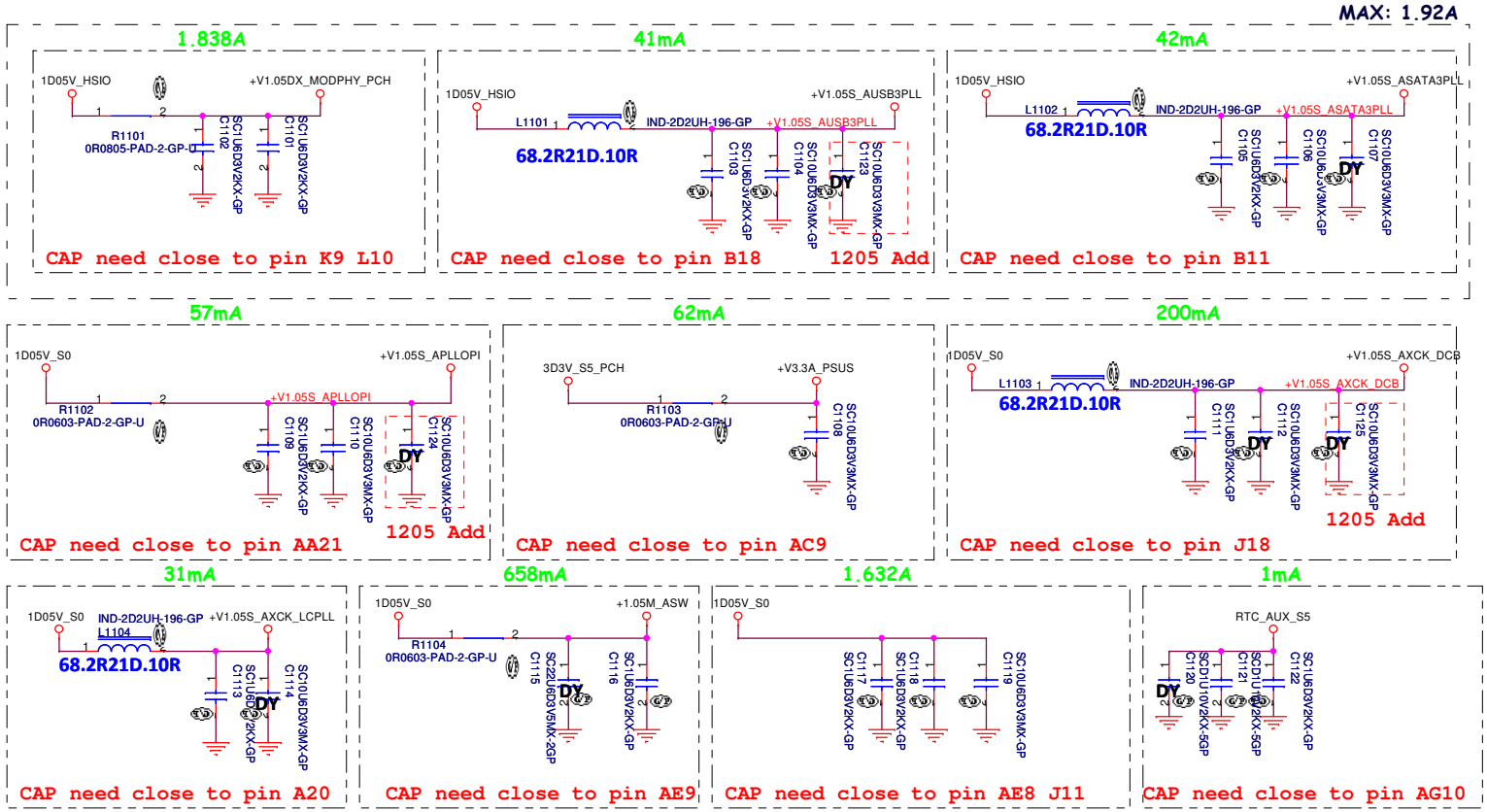
SSID = CPU



<Core Design>

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Title: CPU(Power CAP2)

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SSID = MEMORY

DM1

DDR3-204P-122-GP-U1

62.10017.Z51

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

close to dimm

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

X01 change to short pad

Q1201 Need check Vth=1V

84.05067.031

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Title: DDR3L-SODIMM1

Size: Custom | Document Number: Hadley 15" | Rev: X02

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SSID = MEMORY

DM2

M_B_A[15:0] [5]

M_B_BS2 [5]
M_B_BS0 [5]
M_B_BS1 [5]
M_B_DQ[63:0] [5]

M_B_DQS#[7:0] [5]
M_B_DQS[7:0] [5]

[12] M_B_DIMB_ODT0
[12] M_B_DIMB_ODT1

M_VREF_CA_DIMMB
M_VREF_DQ_DIMMB

[4,12] DDR3_DRAMRST#

0D675V_S0

DDR3-204P-122-GP-U1

62.10017.Z51

M_VREF_CA_DIMMB

Layout Note:
Place these caps close to VREF_CA

M_VREF_DQ_DIMMB

Layout Note:
Place these caps close to VREF_DQ

0D675V_S0

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

close to dimm

M_B_RAS# [5]
M_B_WE# [5]
M_B_CAS# [5]

M_B_DIMB_CS#0 [5]
M_B_DIMB_CS#1 [5]

M_B_DIMB_CKE0 [5]
M_B_DIMB_CKE1 [5]

M_B_DIMB_CLK_DDR0 [5]
M_B_DIMB_CLK_DDR#0 [5]

M_B_DIMB_CLK_DDR1 [5]
M_B_DIMB_CLK_DDR#1 [5]

PCH_SMBDATA [12,18,58,62,67]
PCH_SMBCLK [12,18,58,62,67]

3D3V_S0

SA0_DIMB
SA1_DIMB

1D35V_S3

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

3D3V_S0

R1301 10KR2J-3-GP

SA1_DIMB

SA0_DIMB

R1302 0R0402-PAD-2-GP

C1303 SCD1U10V2KX-5GP

1D35V_S3

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

[5] DDR_WR_VREF02

0D675V_VTTREF 1D35V_S3

R1308 0R2J-2-GP
R1306 1K8R2F-GP
2R2F-GP R1304
M_VREF_DQ_DIMMB
C1320 SCD022U16V2JX-GP
+V_VREF_PATH2
R1307 24D9R2F-L-GP
R1303 1K8R2F-GP

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Title: **DDR3L-SODIMM2**

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Title: M1&M3

Size: A3 | Document Number: Hadley 15" | Rev: X02

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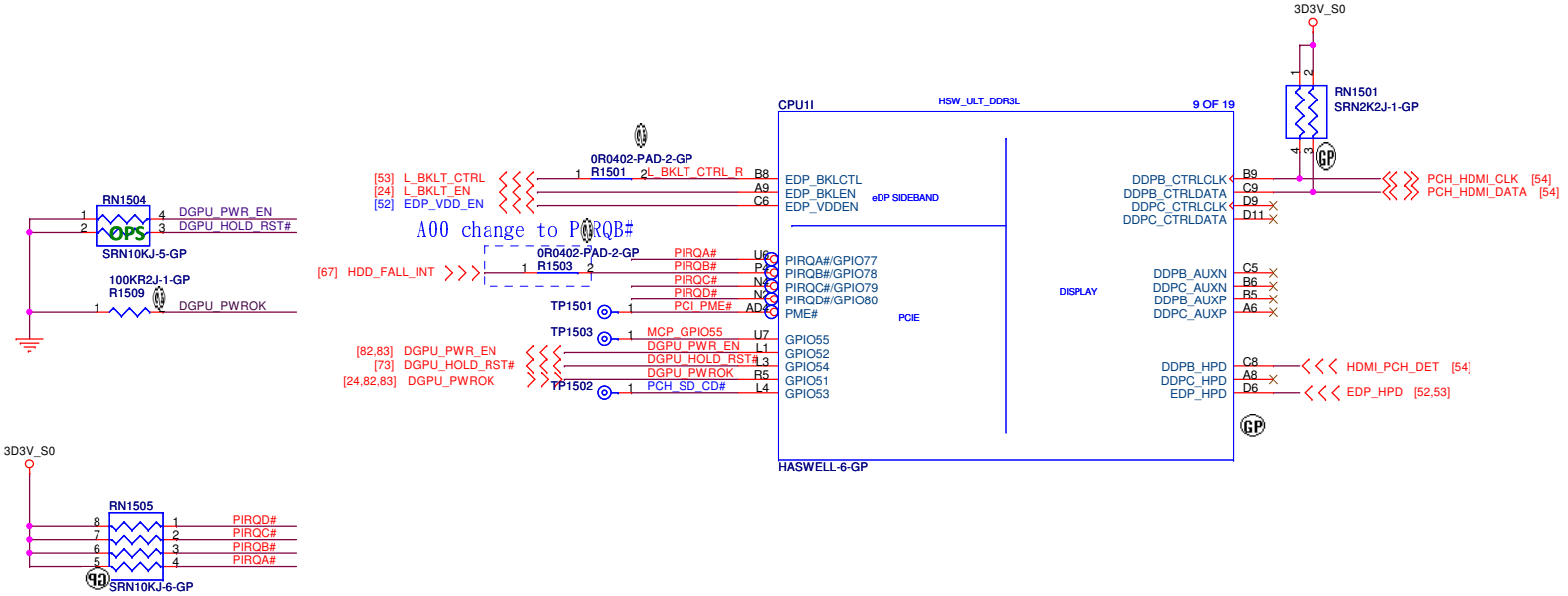
SSID = CPU



<Core Design>

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Title	CPU (EDP SIDEBAND/GPIO/DDI)	
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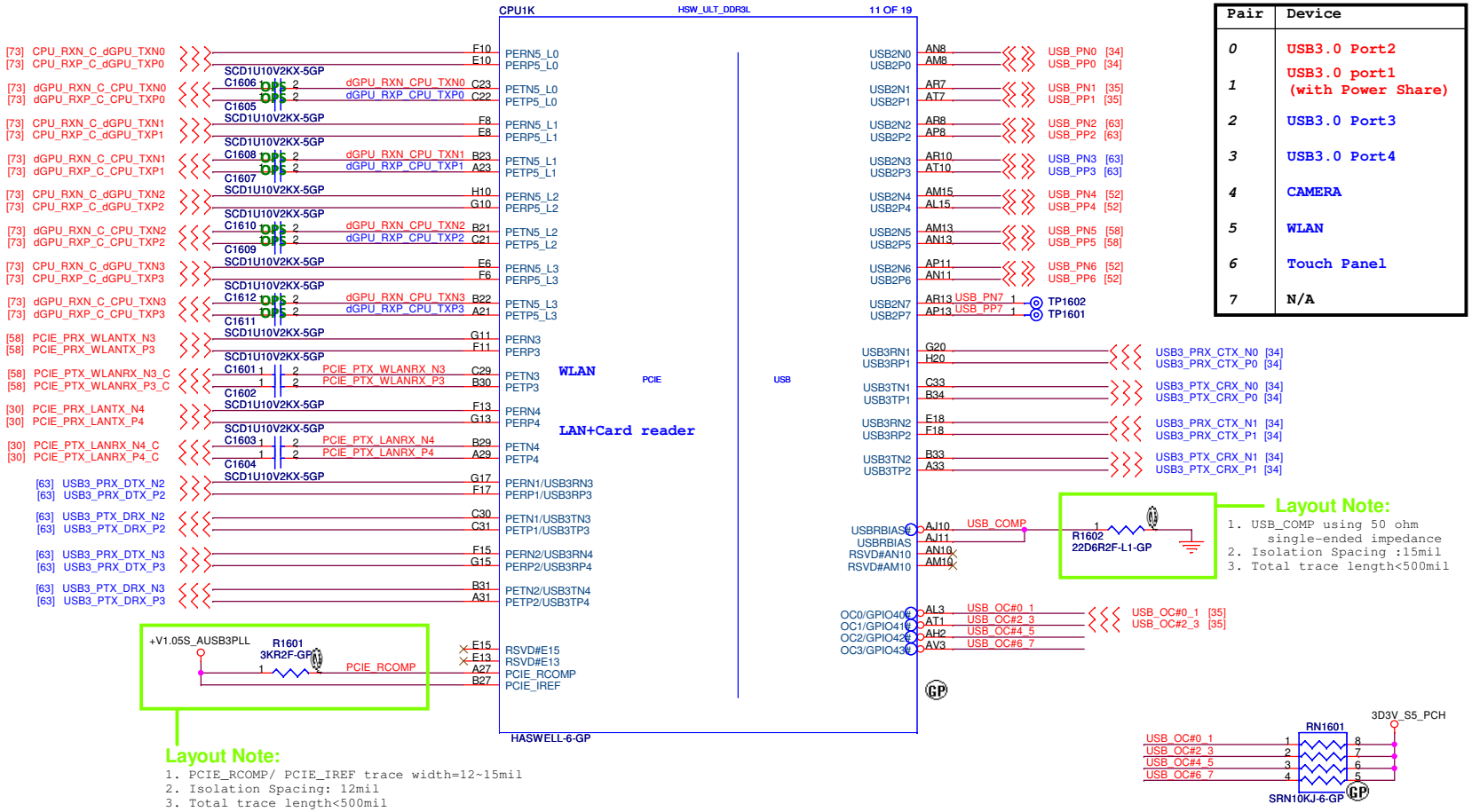
SSID = CPU

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

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Title: CPU (PCIE/USB)

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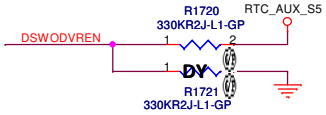
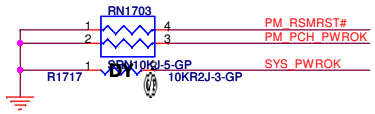
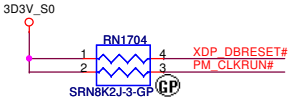
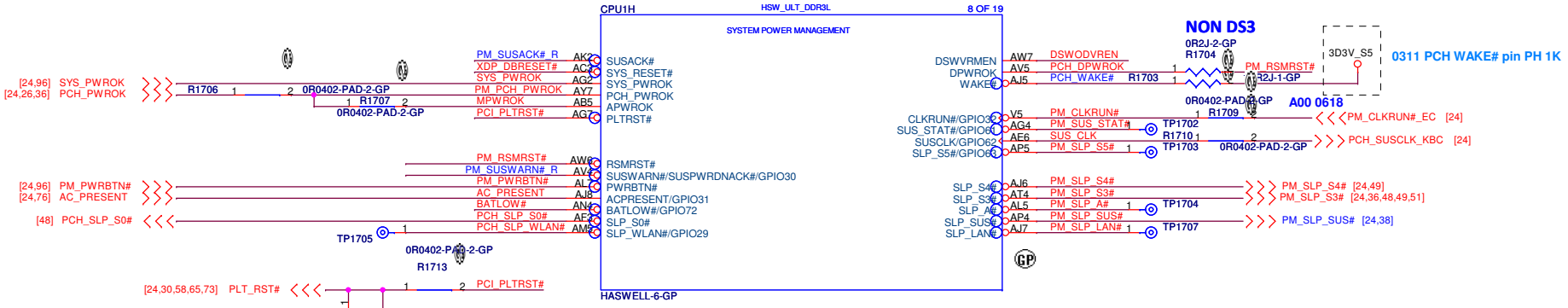
SSID = CPU

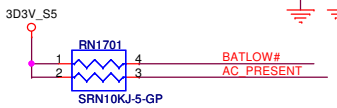
On Die DSW VR Enable	
DSWODVREN	Low = Disable High = Enable (default)

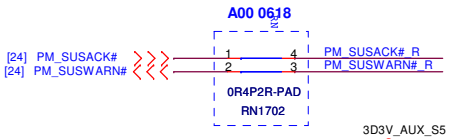


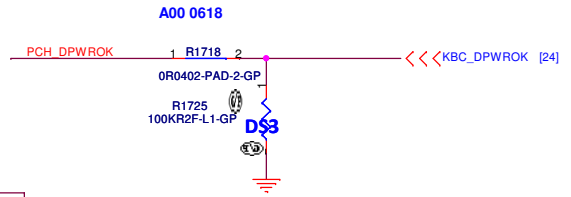


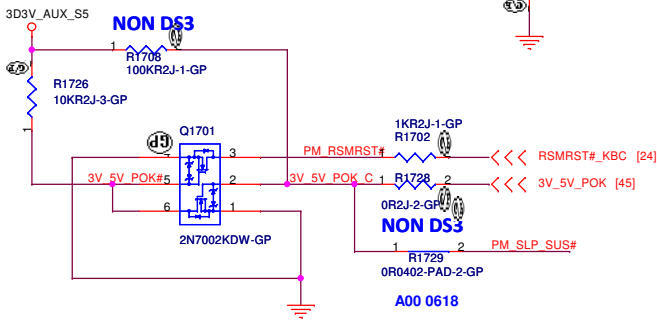


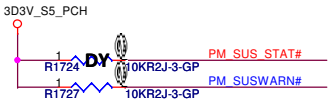












<Core Design>

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Title: CPU (PM)

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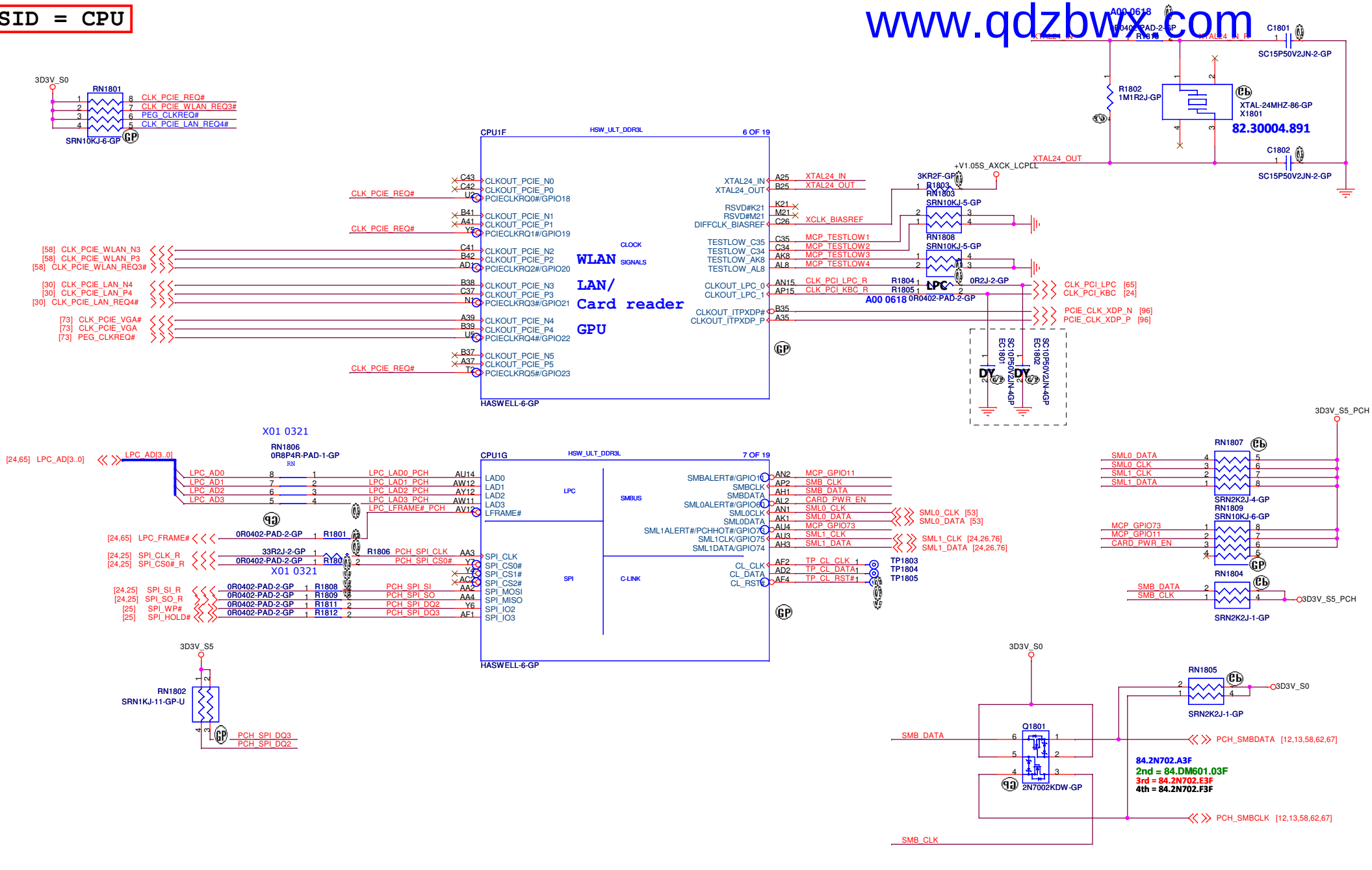
SSID = CPU



<Core Design>

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Title: CPU (CLK/SMB/LPC/SPI)

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SSID = CPU

X02 0502 change C1903 C1904 from 18pF to 15 pF

82.30001.A41
2nd = 82.30001.841

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

HDD1

mSATA

Flash Descriptor Security Overide/ Intel ME Debug Mode

HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Integrated SUS 1V VRM Enable

INTVRMEN	Low = External VRs High = Internal VRs★

Layout Note:

4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.

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Title: CPU (RTC/SATA/HDA/JTAG)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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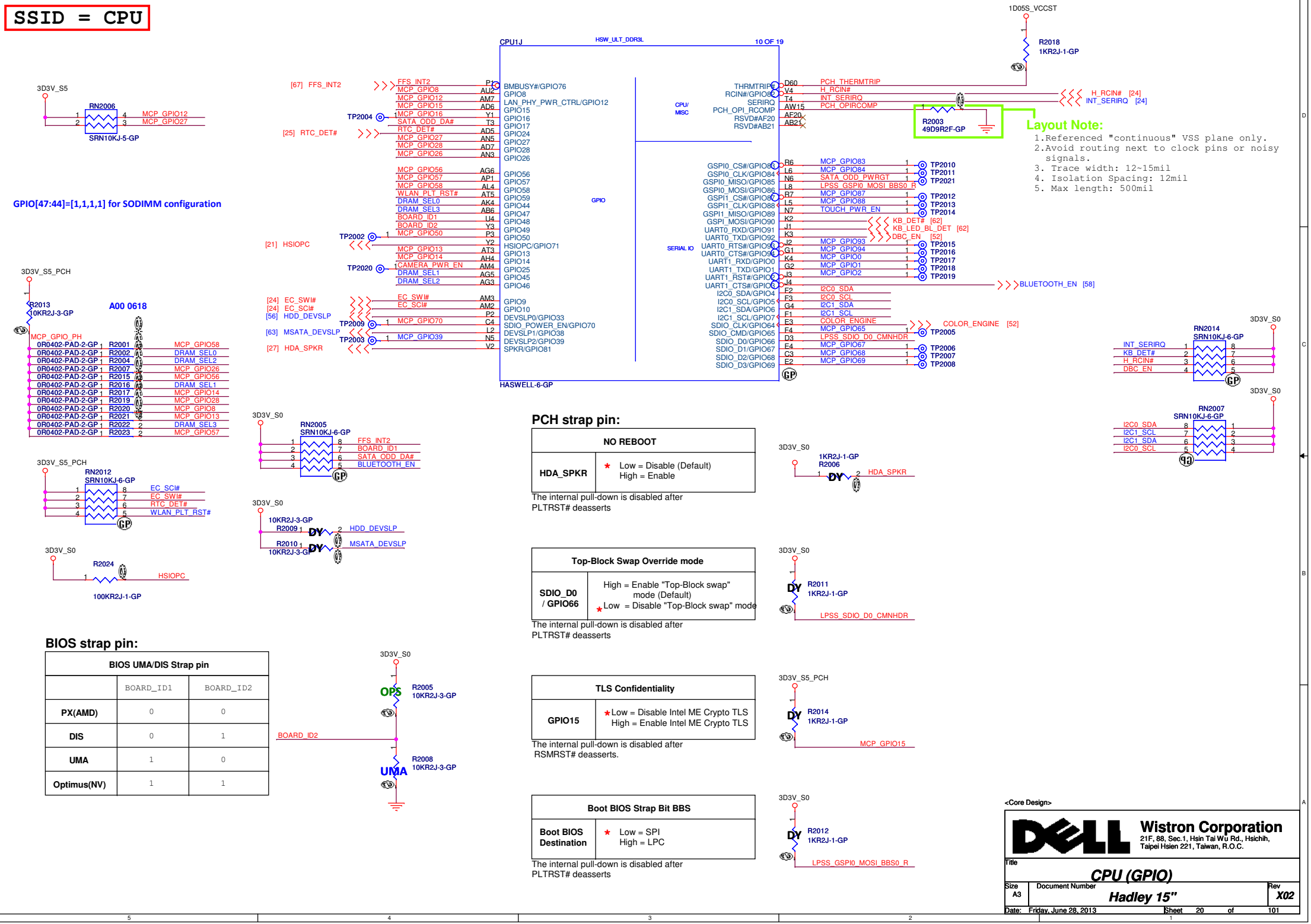
SSID = CPU


CPU1J
HSW_ULT_DDR3L
10 OF 19
HASWELL-6-GP
GPIO
CPU/ MISC
SERIAL IO
1D05S_VCCST
R2018 1KR2J-1-GP
R2003 49D9R2F-GP
Layout Note:
1.Referenced "continuous" VSS plane only.
2.Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil
GPIO[47:44]=[1,1,1,1] for SODIMM configuration
A00 0618
PCH strap pin:
NO REBOOT
HDA_SPKR
Low = Disable (Default)
High = Enable
The internal pull-down is disabled after PLTRST# deasserts
Top-Block Swap Override mode
SDIO_D0 / GPIO66
High = Enable "Top-Block swap" mode (Default)
Low = Disable "Top-Block swap" mode
The internal pull-down is disabled after PLTRST# deasserts
TLS Confidentiality
GPIO15
Low = Disable Intel ME Crypto TLS
High = Enable Intel ME Crypto TLS
The internal pull-down is disabled after RSMRST# deasserts.
Boot BIOS Strap Bit BBS
Boot BIOS Destination
Low = SPI
High = LPC
The internal pull-down is disabled after PLTRST# deasserts
BIOS strap pin:
BIOS UMA/DIS Strap pin
BOARD_ID1
BOARD_ID2
PX(AMD) 0 0
DIS 0 1
UMA 1 0
Optimus(NV) 1 1
OPS
UMA
<Core Design>
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Title
CPU (GPIO)
Size A3
Document Number Hadley 15"
Rev X02
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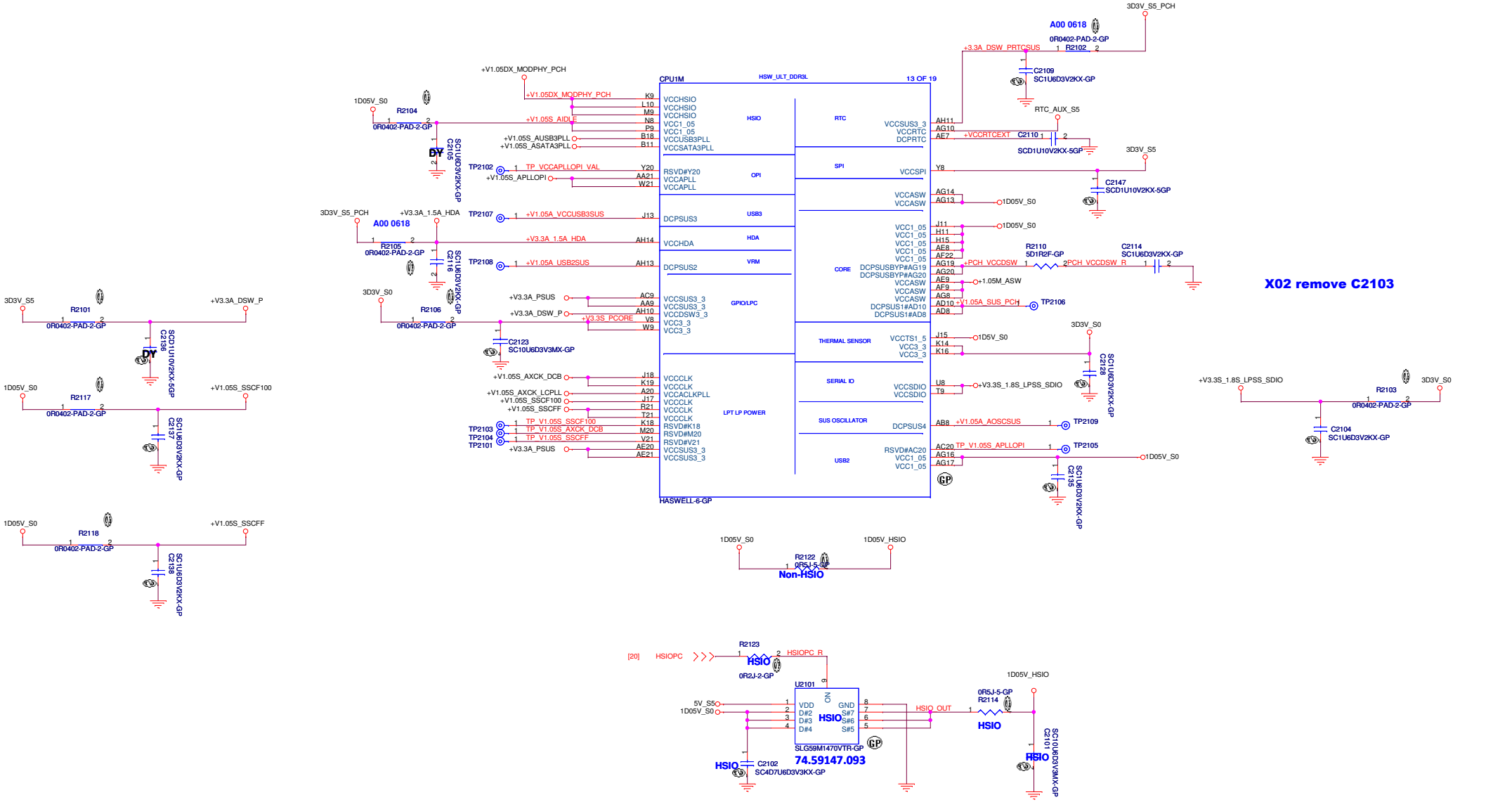
SSID = CPU


CPU1M
HSW_ULT_DDR3L
13 OF 19
HASWELL-6-GP
A00 0618
X02 remove C2103
Non-HSIO
HSIO
74.59147.093
SLG59M1470VTR-GP
<Core Design>
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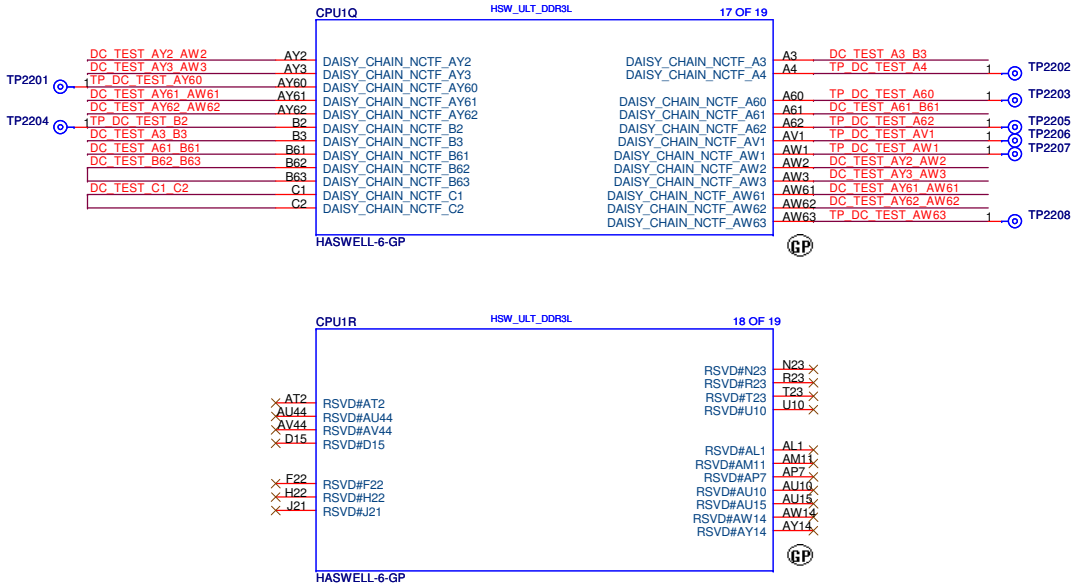
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (POWER2)
Size
Custom
Document Number
Hadley 15"
Rev
X02
Date: Friday, June 28, 2013
Sheet 21 of 101

SSID = CPU



<Core Design>

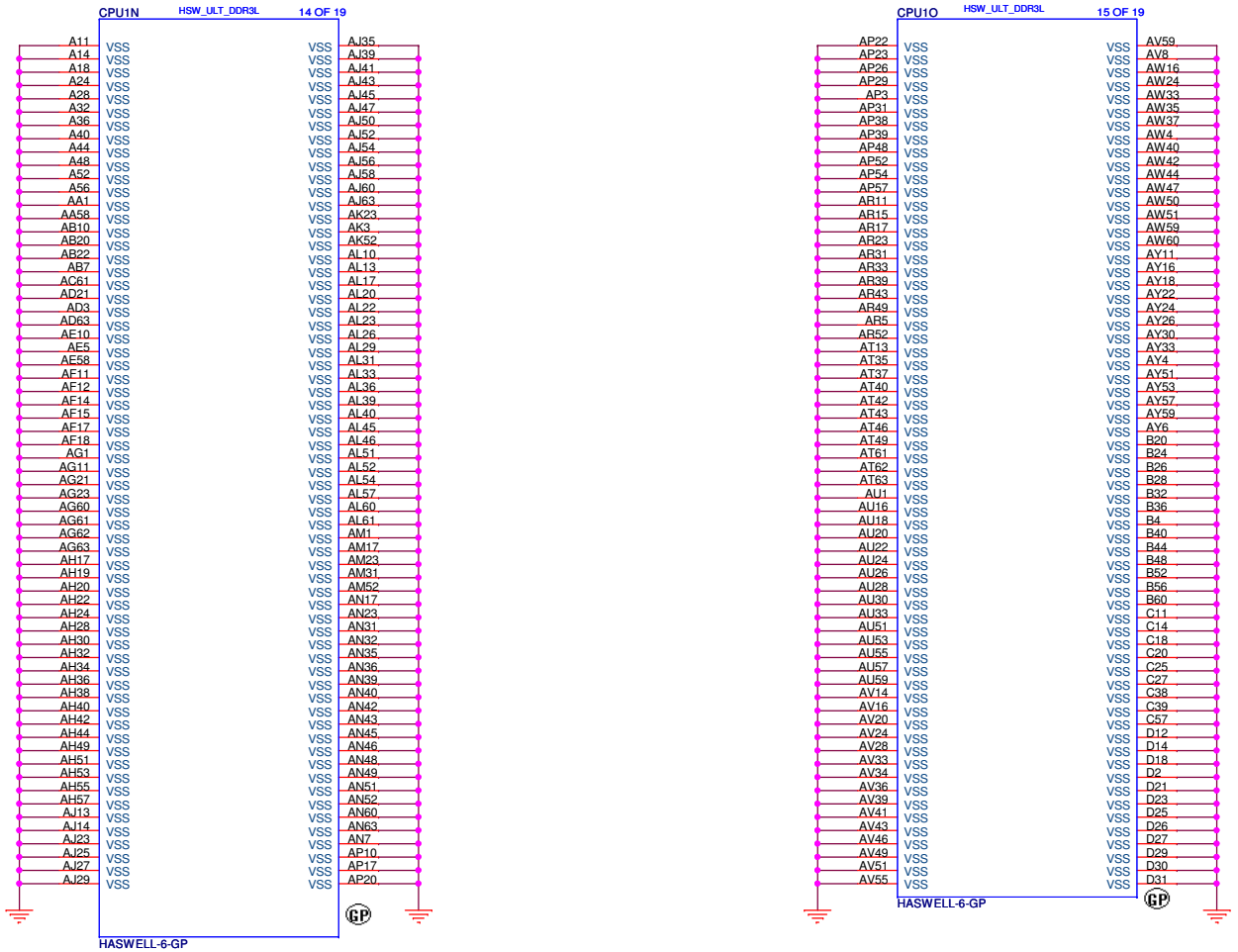
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RSVD

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 22 of 101

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 23 of 101

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
(DOH70)UMA	100.0K	10.0K(64.10025.6DL)	3.0V
(DOH50)UMA/eDP	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
(DOH70)DIS	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
(DOH50)UMA/LVDS	100.0K	49.9K(64.49925.6DL)	2.201V
(DOH50)DIS/eDP	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

Don't PD

ALL_SYS_PWRGD assert, delay 10ms;
PCH_PWROK assert.

ALL_SYS_PWRGD assert, delay 100ms;
SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

Backlight Control from LVDS Converter

AOAC Ambient temperature detect

EC_GPIO47 High Active

X01 0321

A00 0618

83.R0304.A8F

71.00985.C0G

69.60037.011

75.00054.K7D

84.2N702.I31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31

84.T3906.A11
2nd = 84.03906.F11

84.02130.031
2ND = 84.03413.A31

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

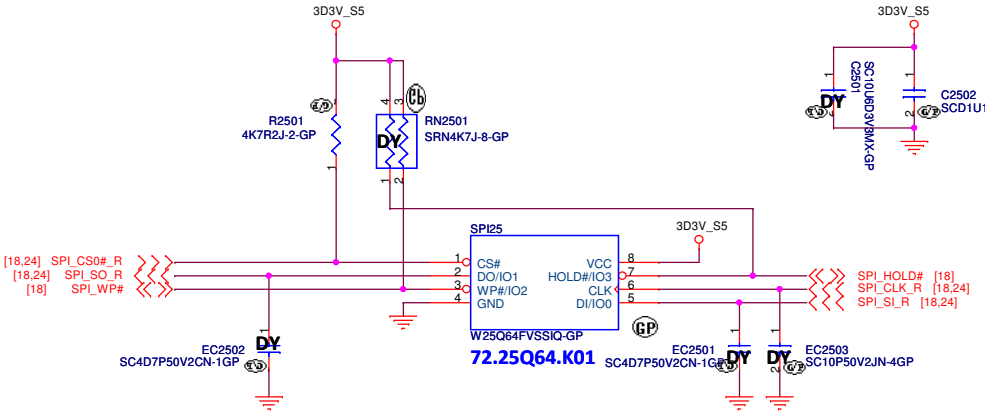
Title: KBC Nuvoton NPCE985

Size: A2 | Document Number: Hadley 15" | Rev: X02

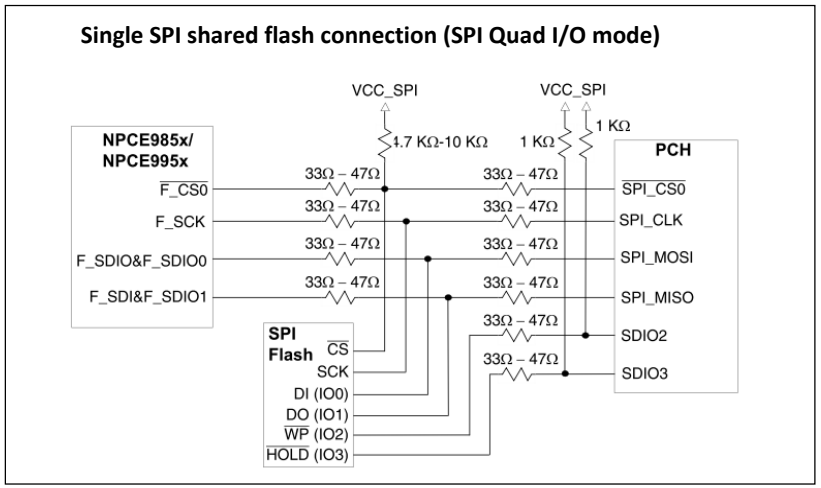
Date: Friday, June 28, 2013 | Sheet 24 of 101

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

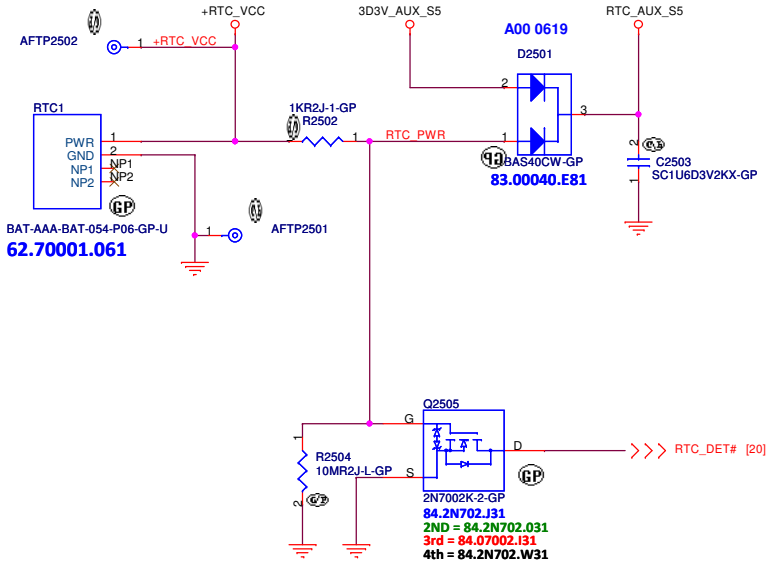


Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

Wistron Corporation
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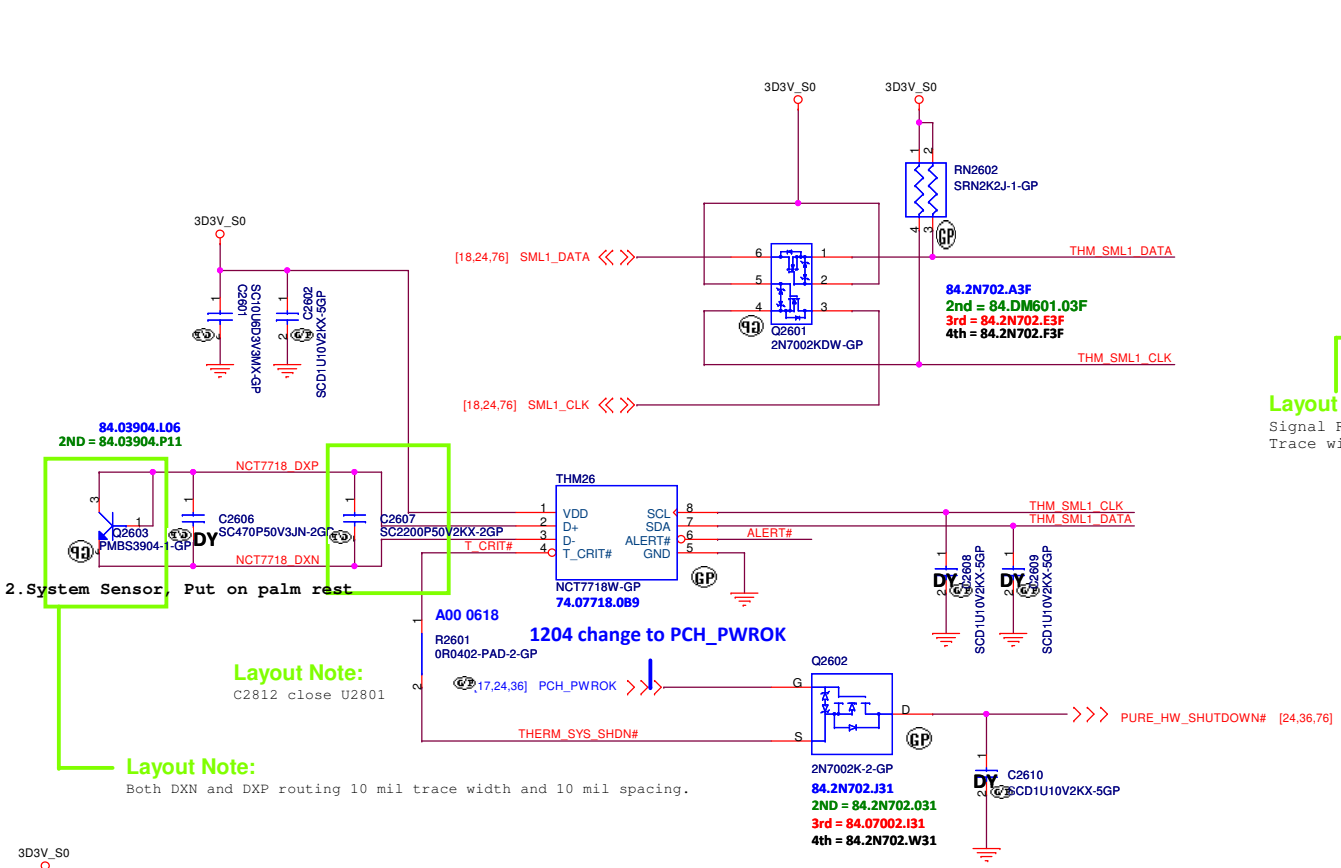
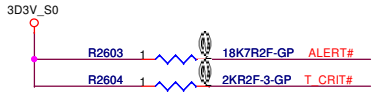
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 25 of 101	

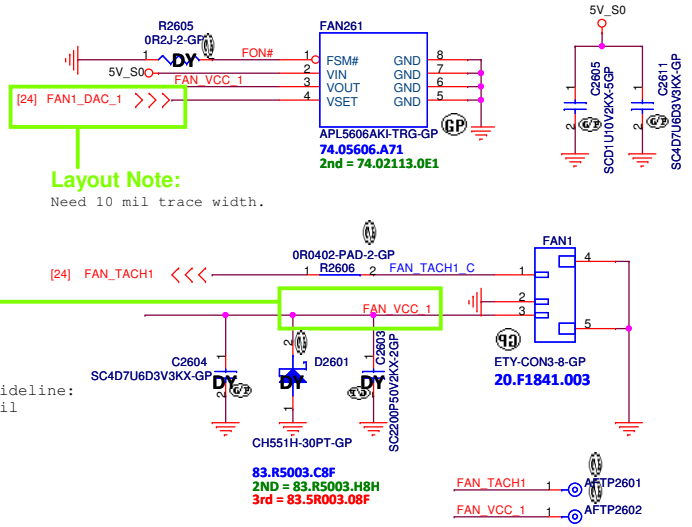
SSID = Thermal





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Fan controller1



<Core Design>

Wistron Corporation
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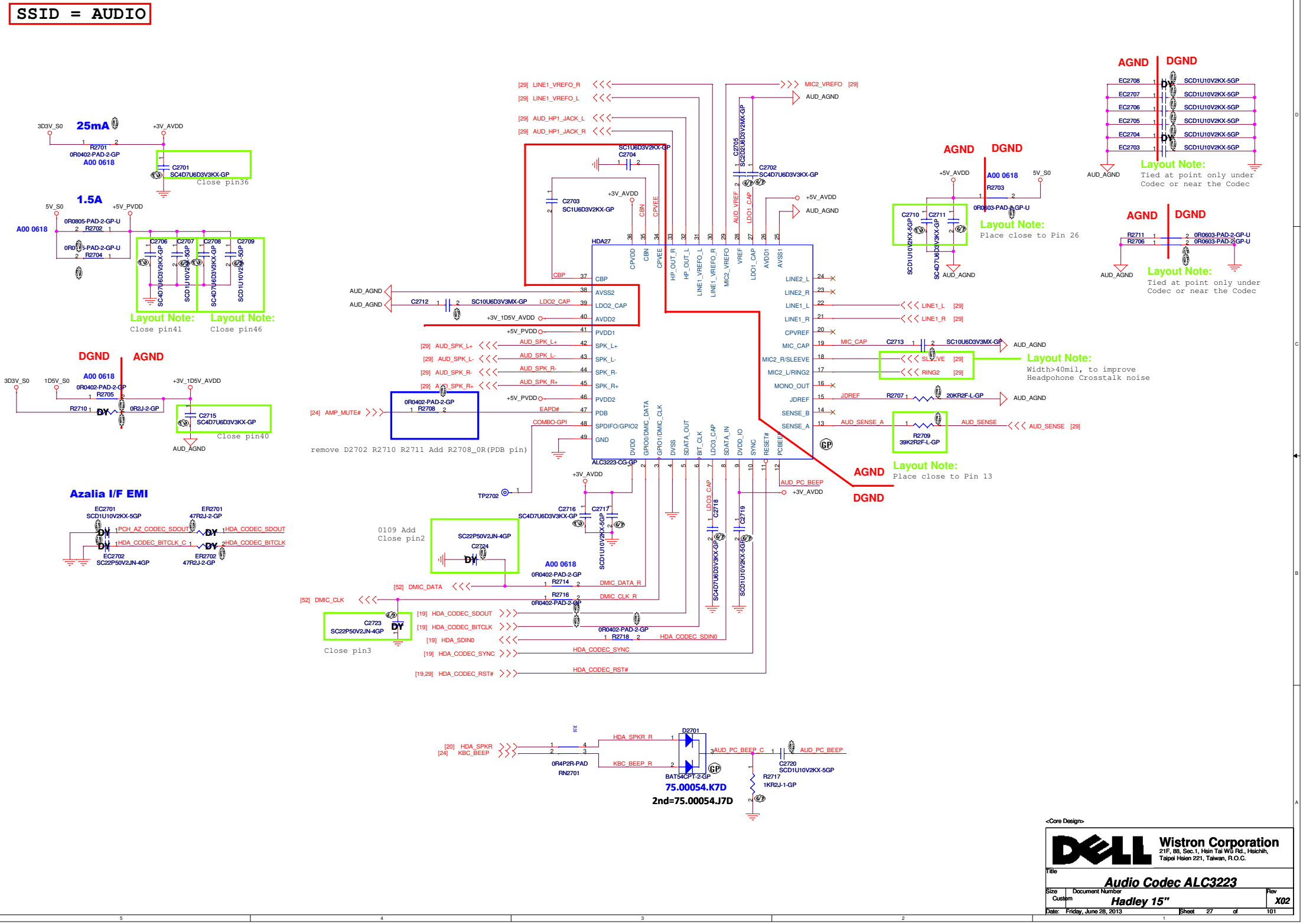
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 26 of 101

SSID = AUDIO



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3223

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 27 of 101

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

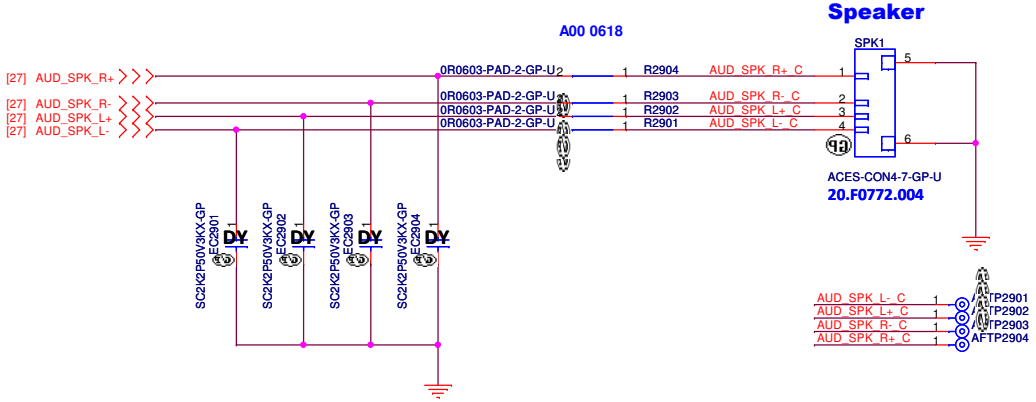
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 28 of 101

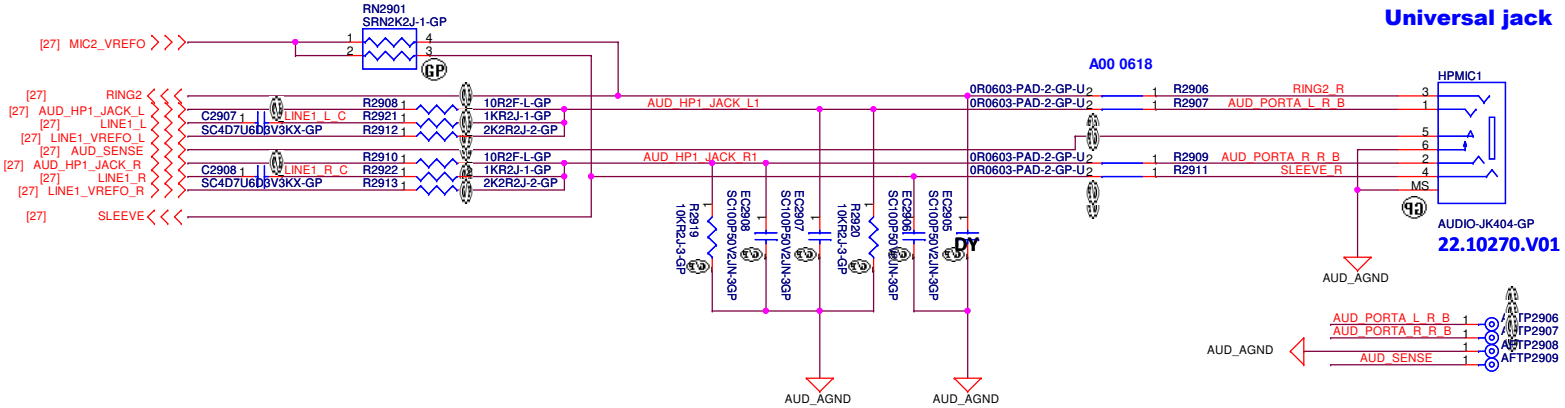
SSID = AUDIO

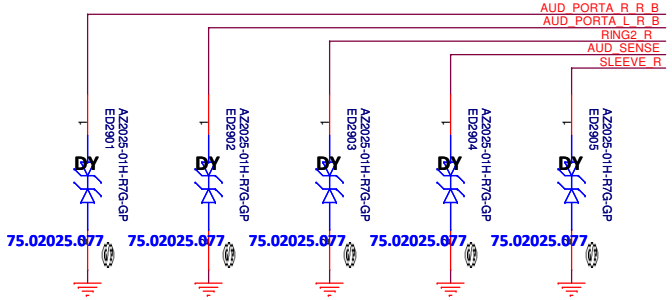
Speaker

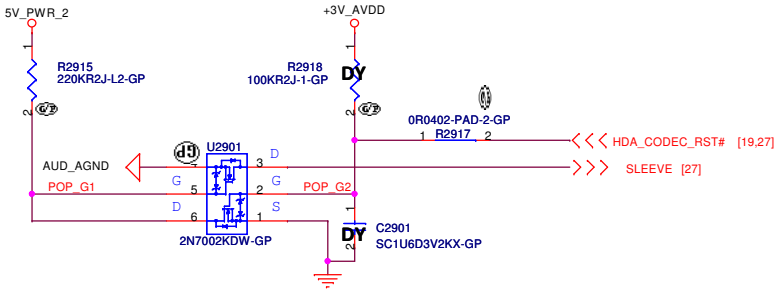


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Universal jack







<Core Design>

Wistron Corporation
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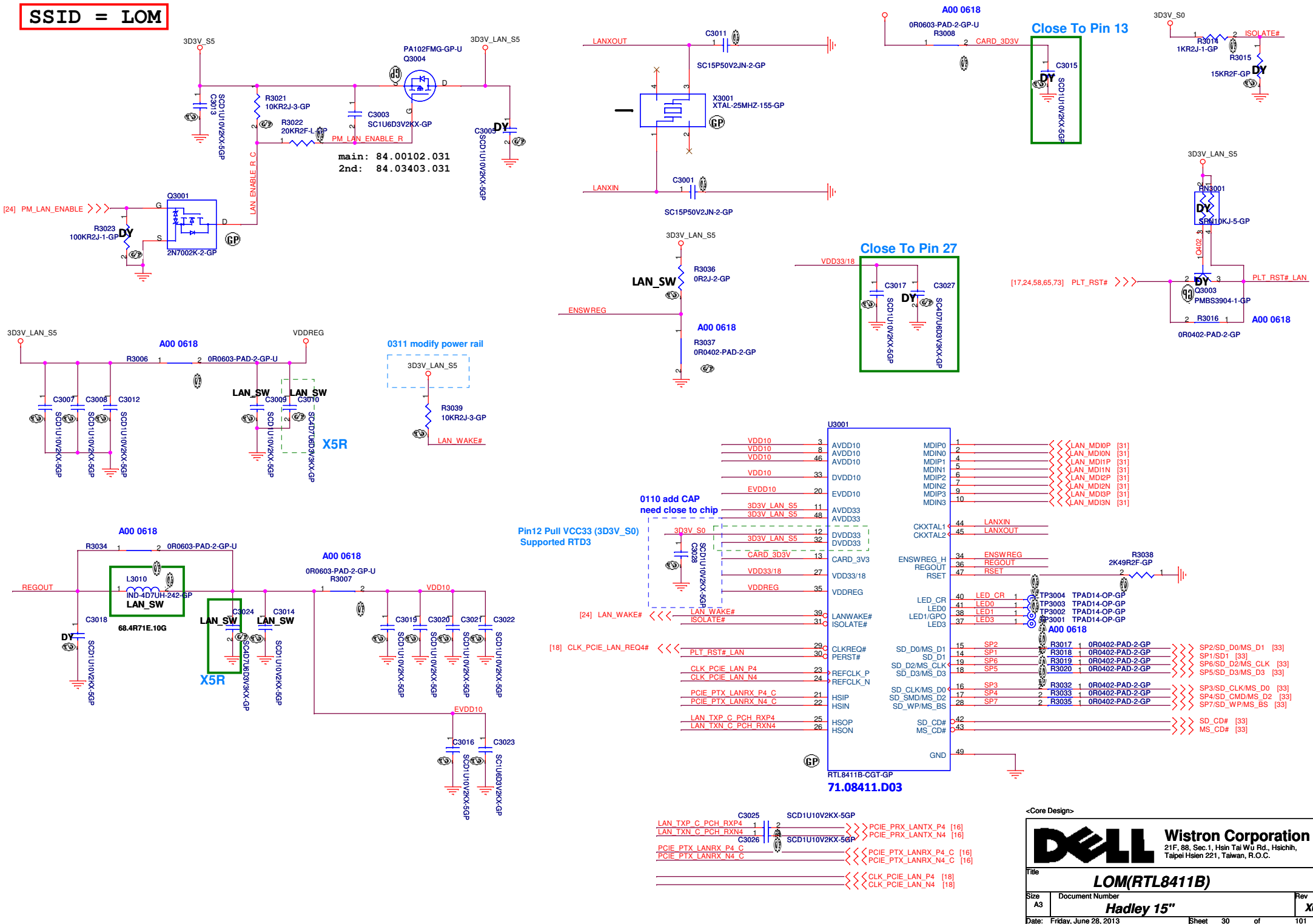
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 29 of 101

SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

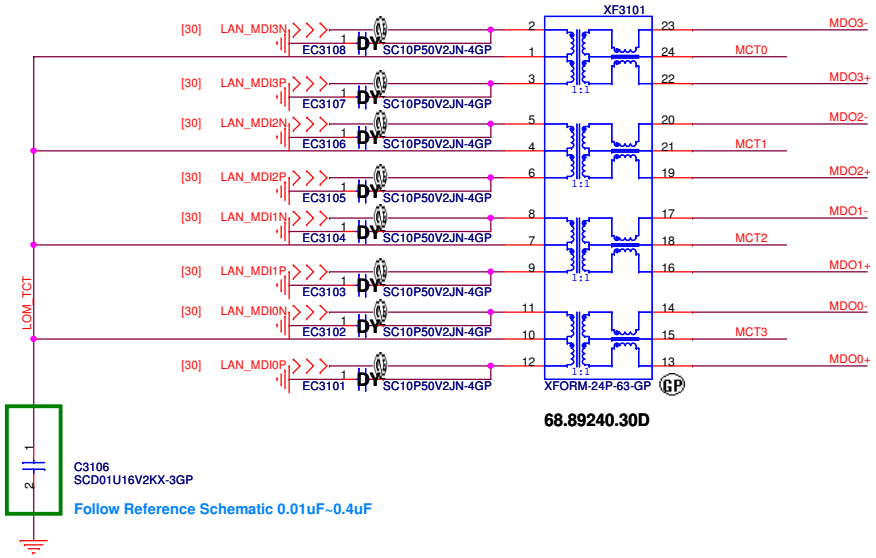
Title: LOM(RTL8411B)

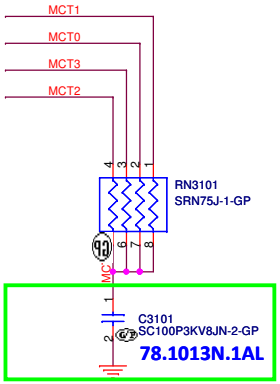
Size	Document Number	Rev
A3	Hadley 15"	X02

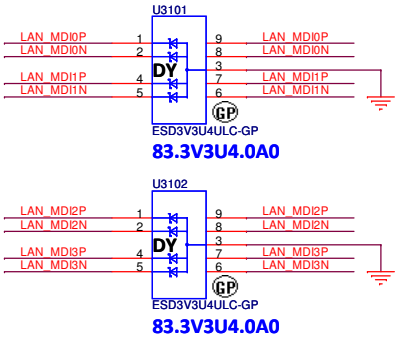
Date: Friday, June 28, 2013 Sheet 30 of 101

SSID = LOM

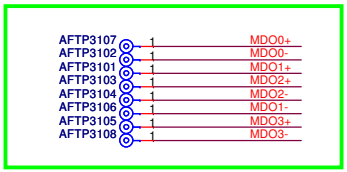
GIGA LAN TransFormer

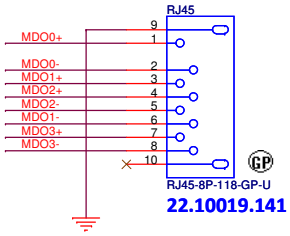






Layout:
Place near RJ45





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 31 of 101

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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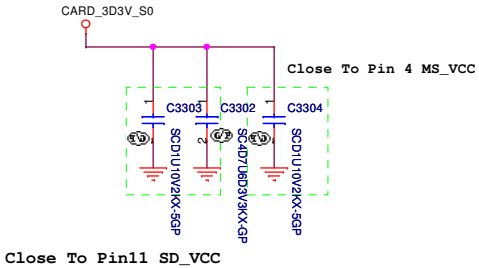
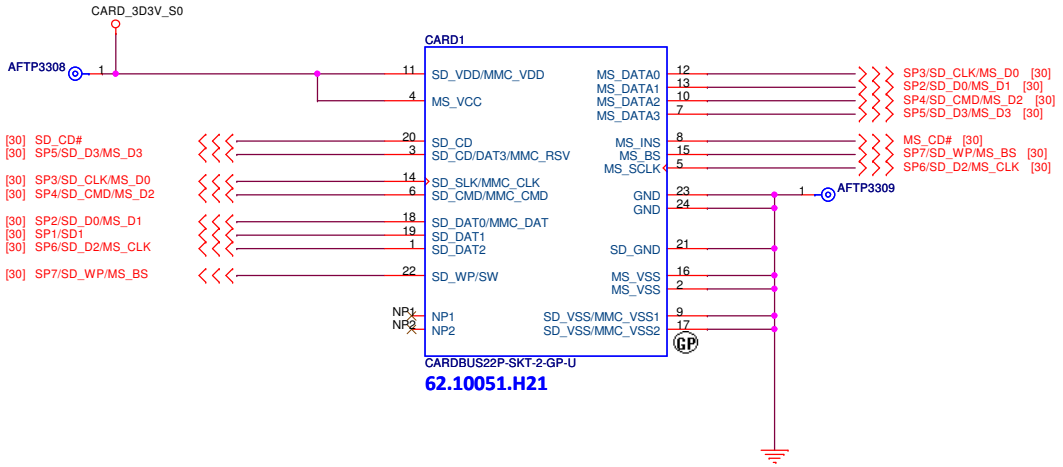
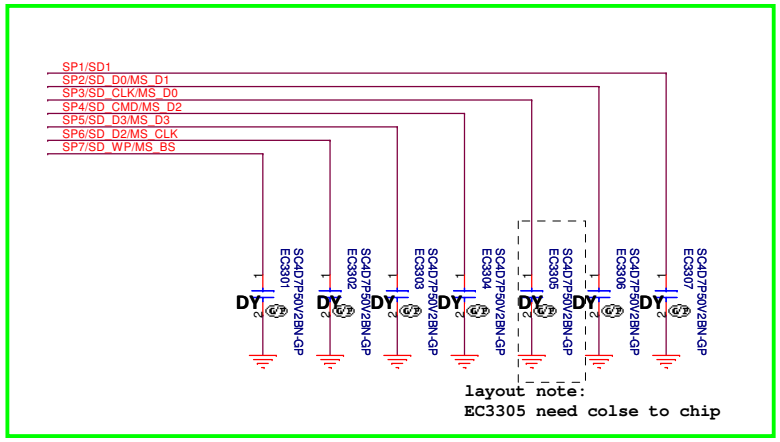
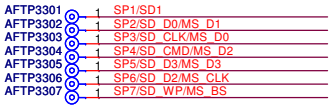
SSID = SDIO





Reserve EMI Cap, 0107 CLK Cap DY





<Core Design>

Wistron Corporation
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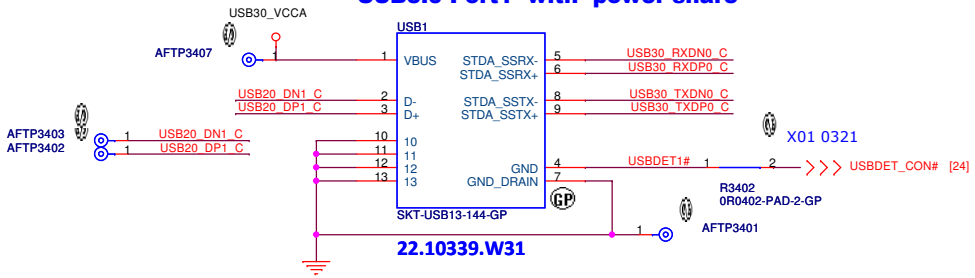
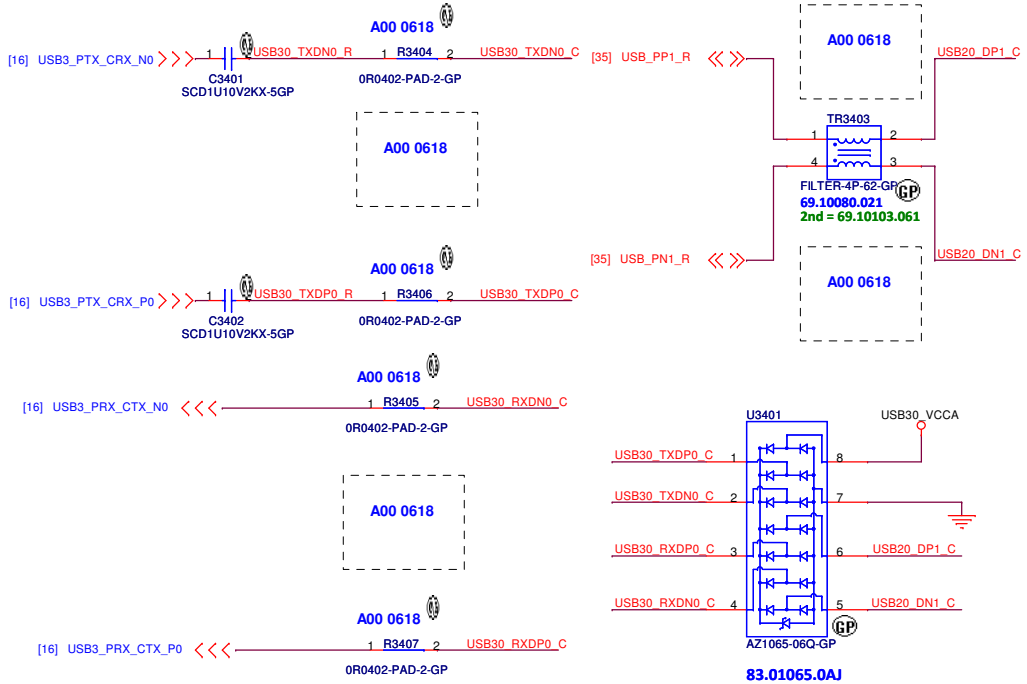
Title	Card Reader CONN	
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 33 of 101	

SSID = USB

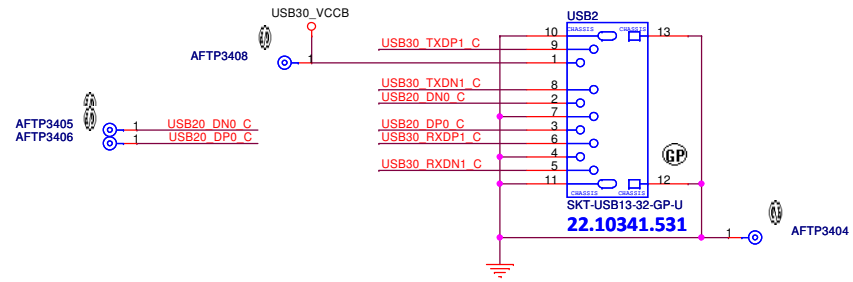
USB3.0 Port1 with power share



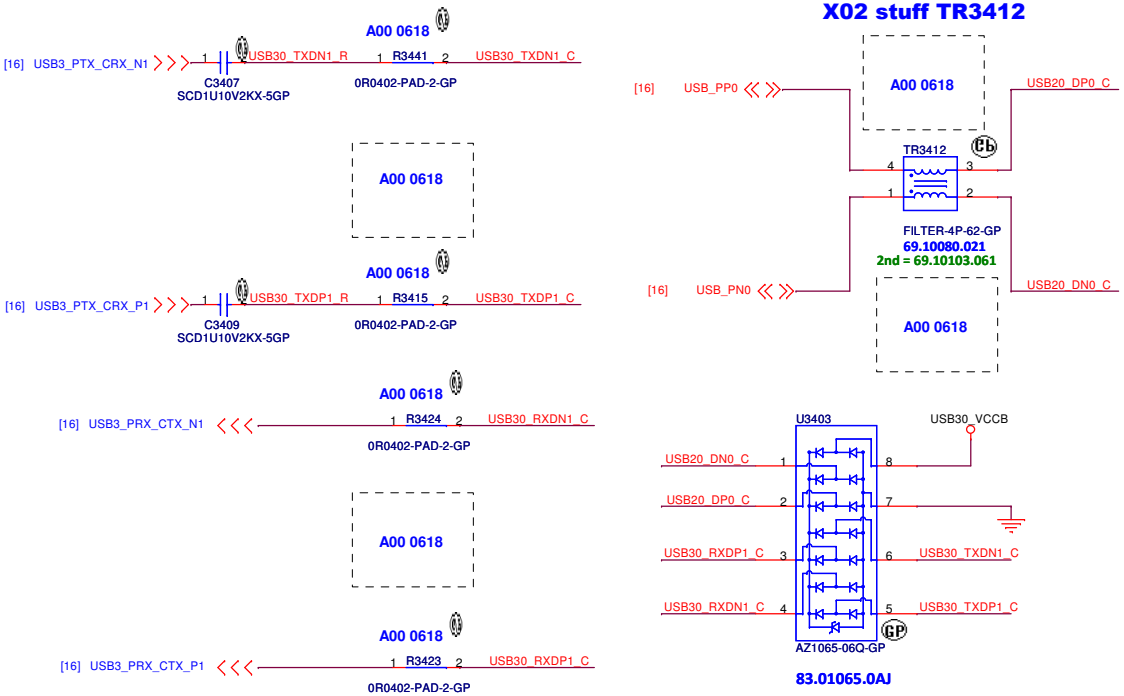
X02 stuff TR3403



USB3.0 Port2



X02 stuff TR3412

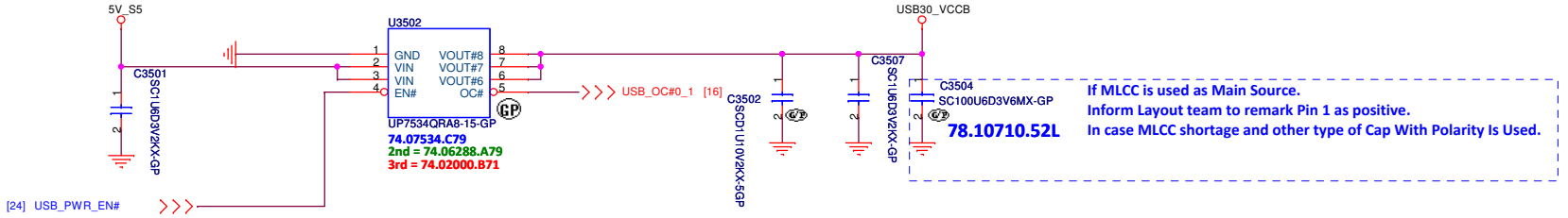


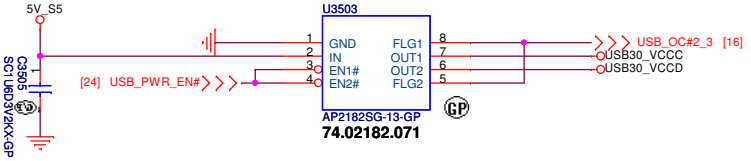
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB3.0(1)		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 34 of 101	

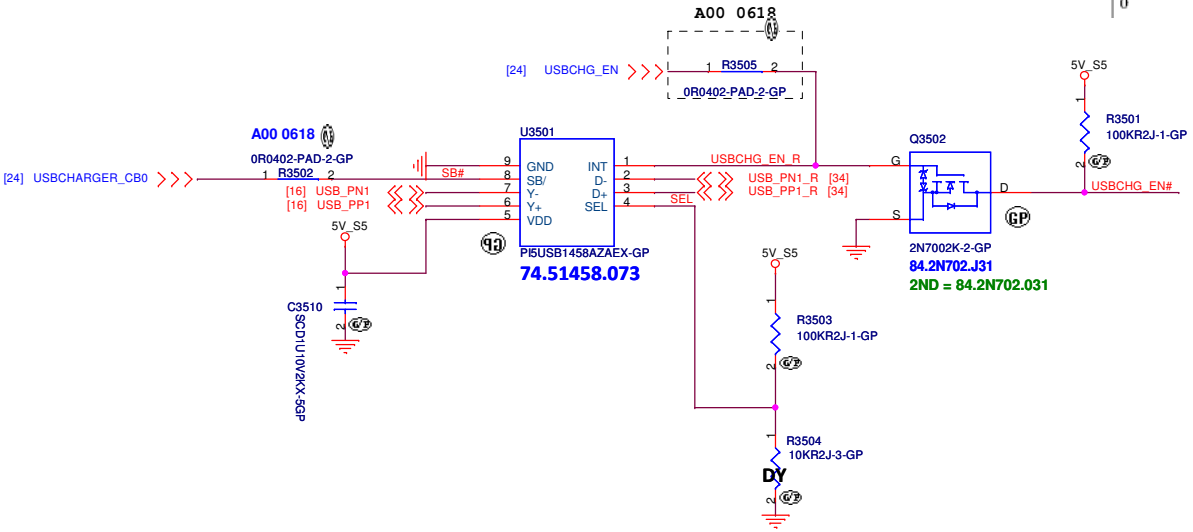
SSID = USB

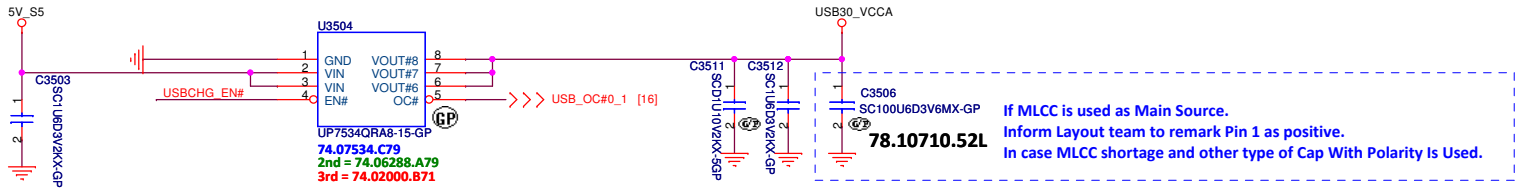




SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M= (1/2)*V_{DD}	Test Mode, M = $V_{DD/2}$ = (1/2)*V_{DD}	

0319 modify USB Charger circuit





USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW
Size: | Document Number: Hadley 15" | Rev: X02
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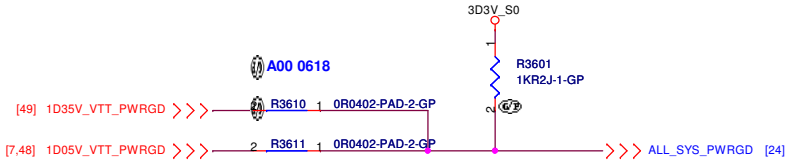
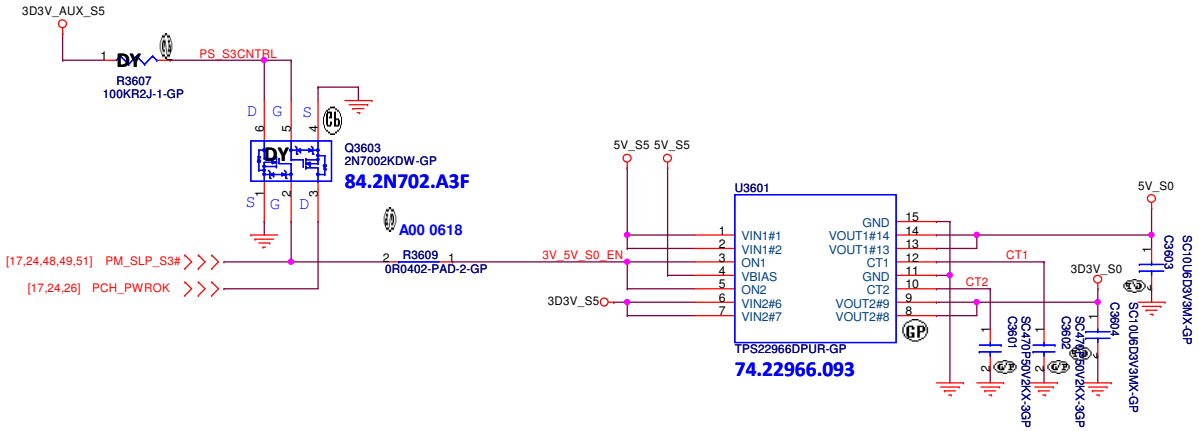
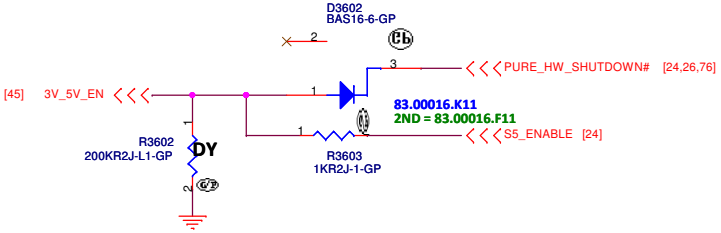
SSID = Reset.Suspend

Power Good



ROSA Run Power





5V_S0

5V_S0 Comsumption
Peak current 4.033A

3D3V_S0

3D3V_S0 Comsumption
Peak current 3A

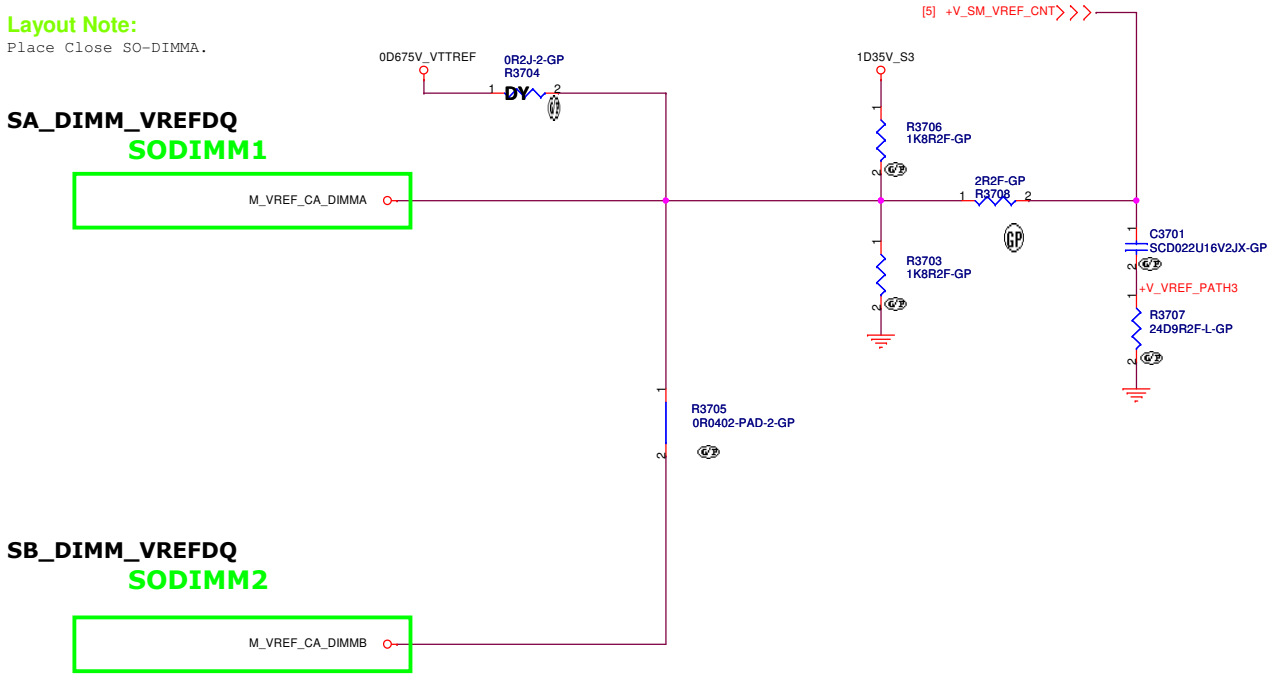
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 36 of 101	

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.



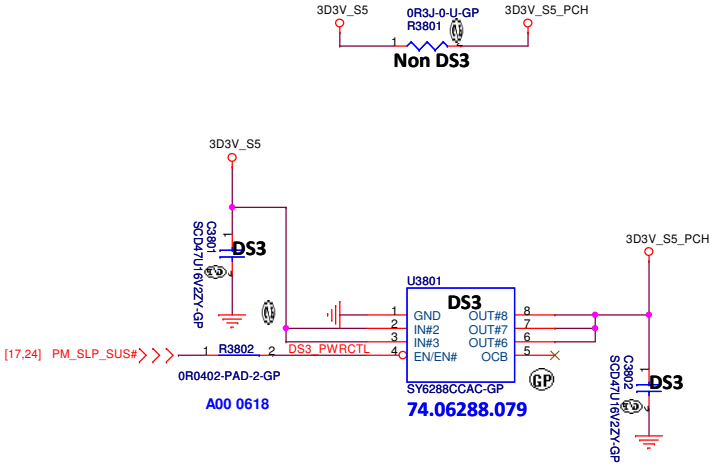
Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S3 Power Reduction	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 37 of 101	

SSID = Reset.Suspend



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DSW	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 38 of 101	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 39 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 40 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 41 of 101

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil

A00 0618

A00 0619

DT MODE

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

<Core Design>

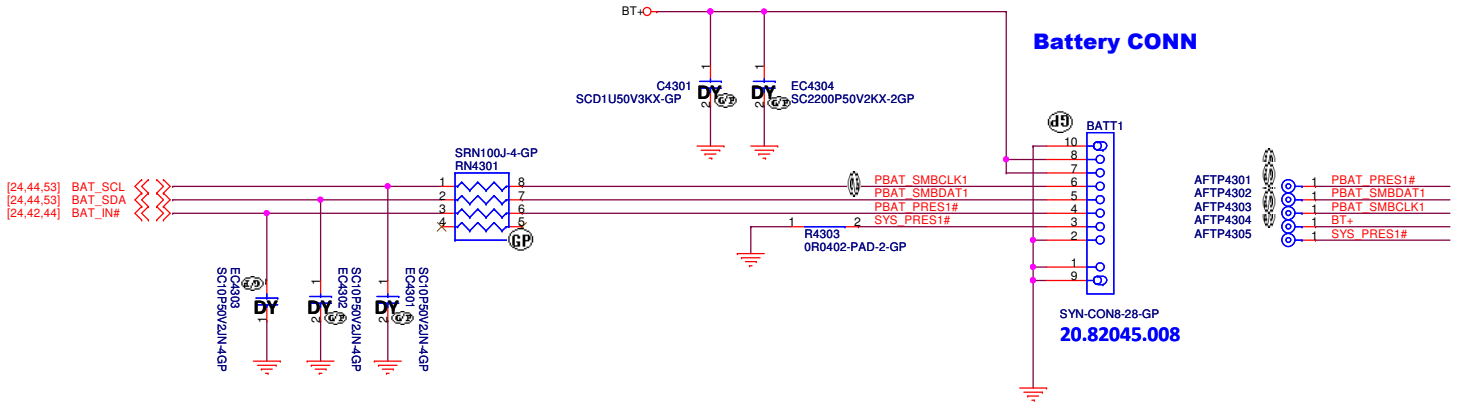
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

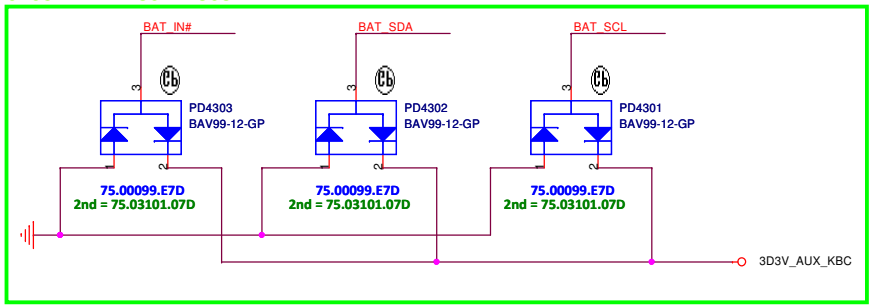
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 42 of 101

SSID = PWR.Support



0109 DY PD4301~4303



Layout Note:
Place near Battery CONN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 43 of 101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

PU4406 and PU4407:
main source: 84.03660.037

ZZ.00215.037

ZZ.00215.037

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
Setting=18.178v

ACAV_IN
H=ACIN
L=UNAC

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=nornal

Follow custormer circuits

Follow custormer circuits

PWR_CHG_ACOK:
PWR_CHG_REGN=6V
V+=6*(PR4404/(PR4410+PR4404))=3.27V

CHECK EE

Close PR4443

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

BATTERY MON

A00 0618

A00 0618

PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.099V

DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PR4447)=9V

CHECK PM ADAPTER TYPE
And setting adapter type

(AD_IA_HW)

(AD_IA_HW_2)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

CHECK EE
follow custormer circuits.

<Core Design>

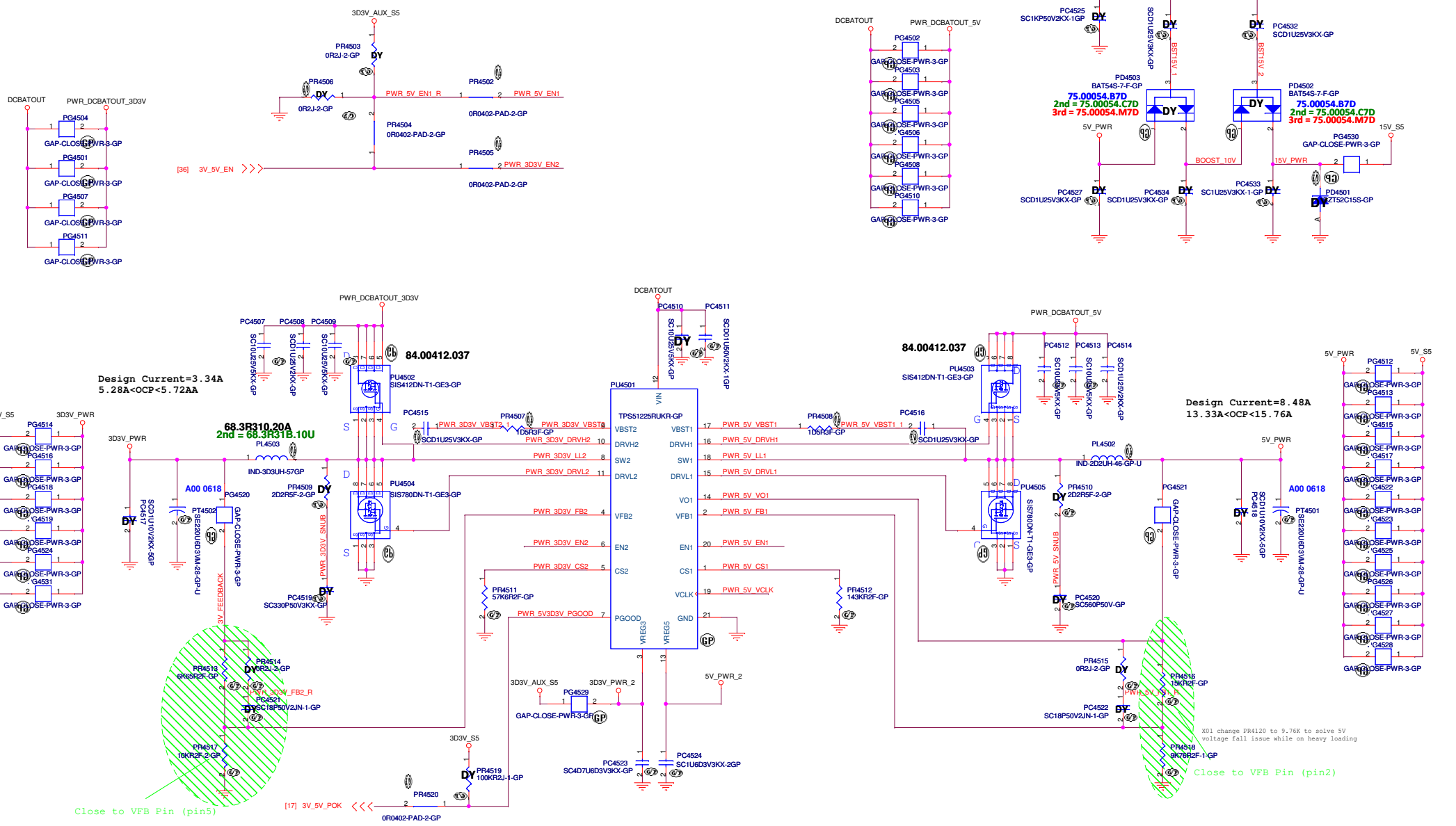
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)

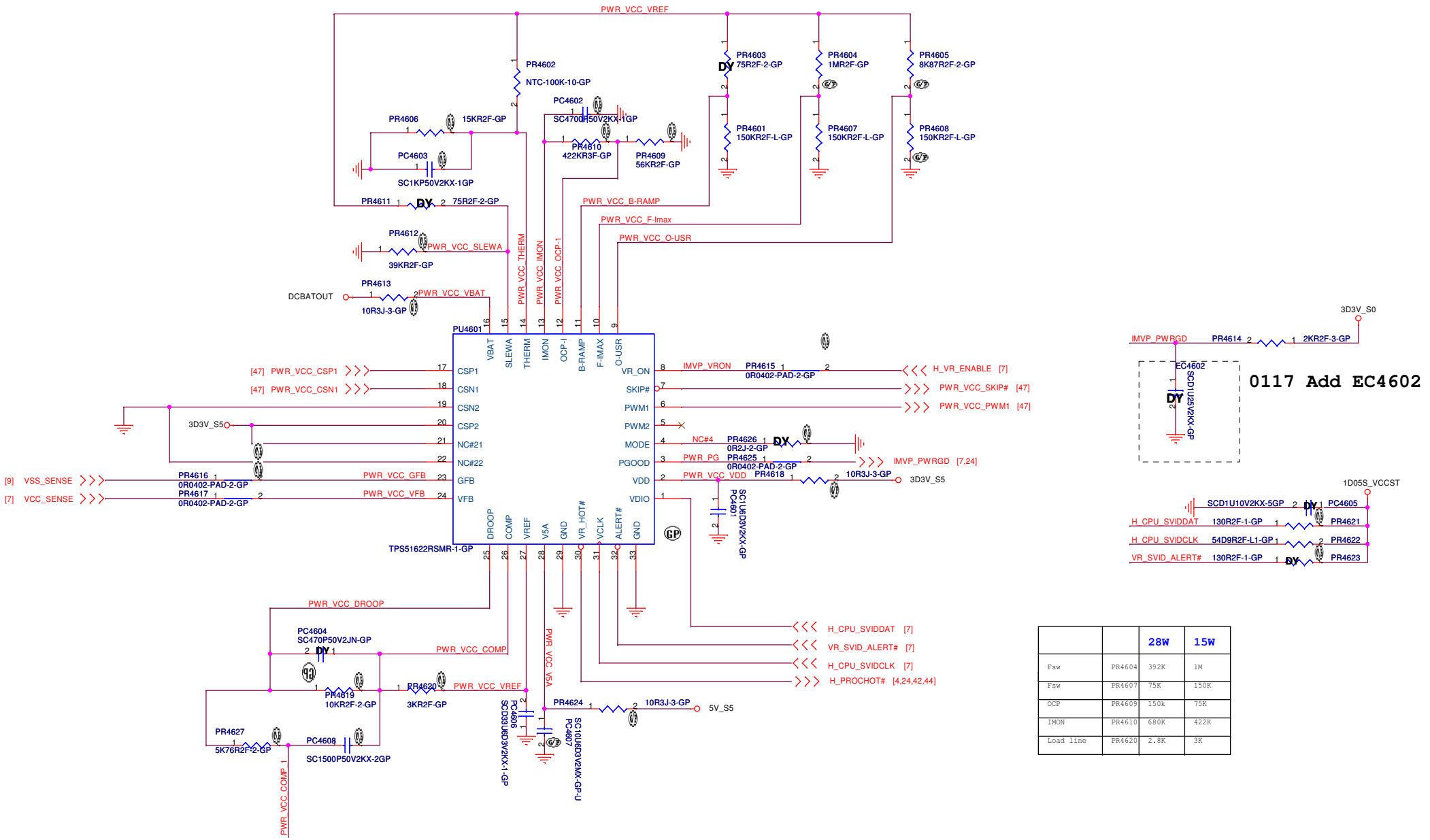
Size: Custom | Document Number | Rev: X02

Date: Friday, June 28, 2013 | Sheet 44 of 101

SSID = PWR.Plane.Regulator_5v3p3v



SSID = CPU.Regulator



		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCP	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>

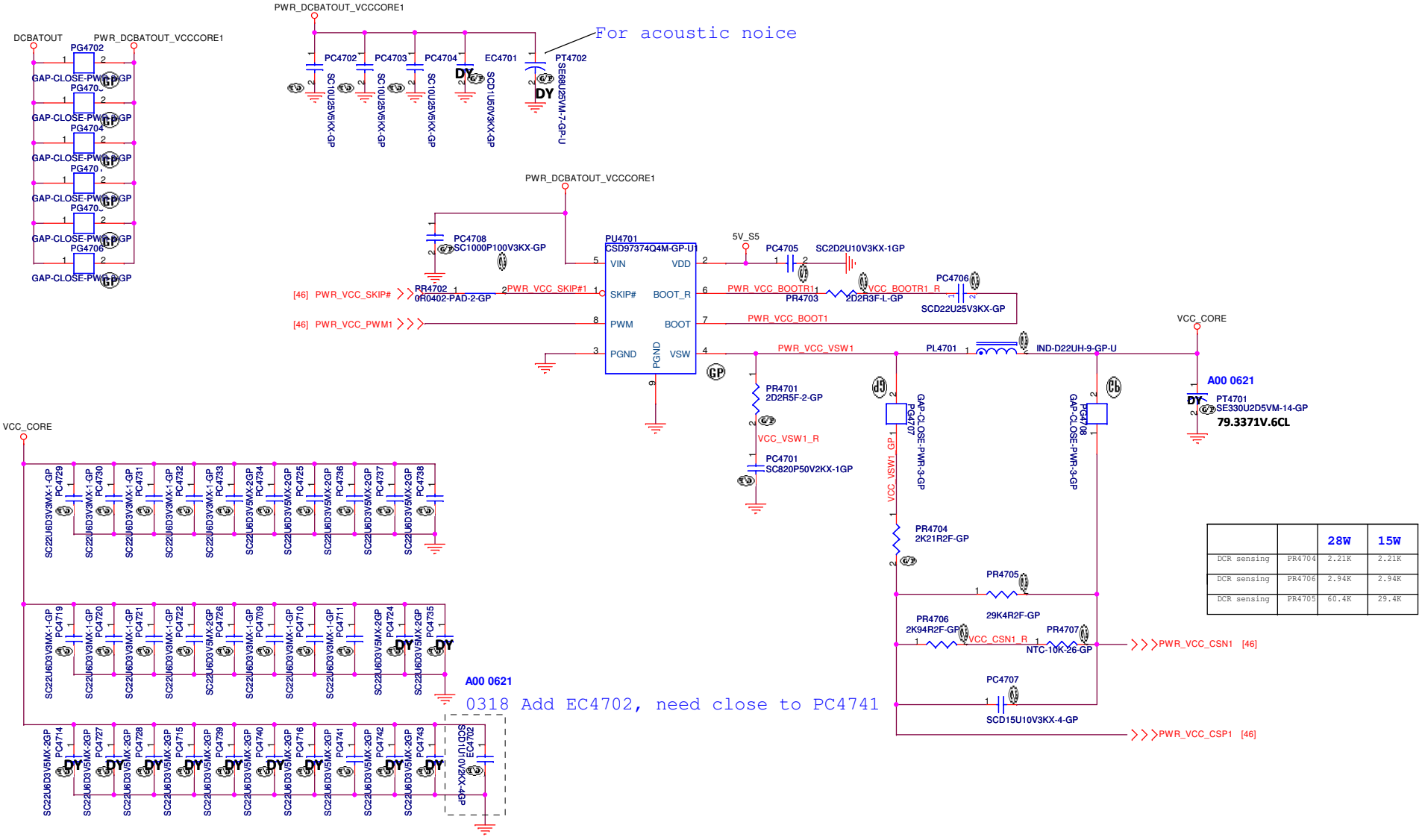
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(1/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 46 of 101

SSID = CPU.Regulator



		28W	15W
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

<Core Design>

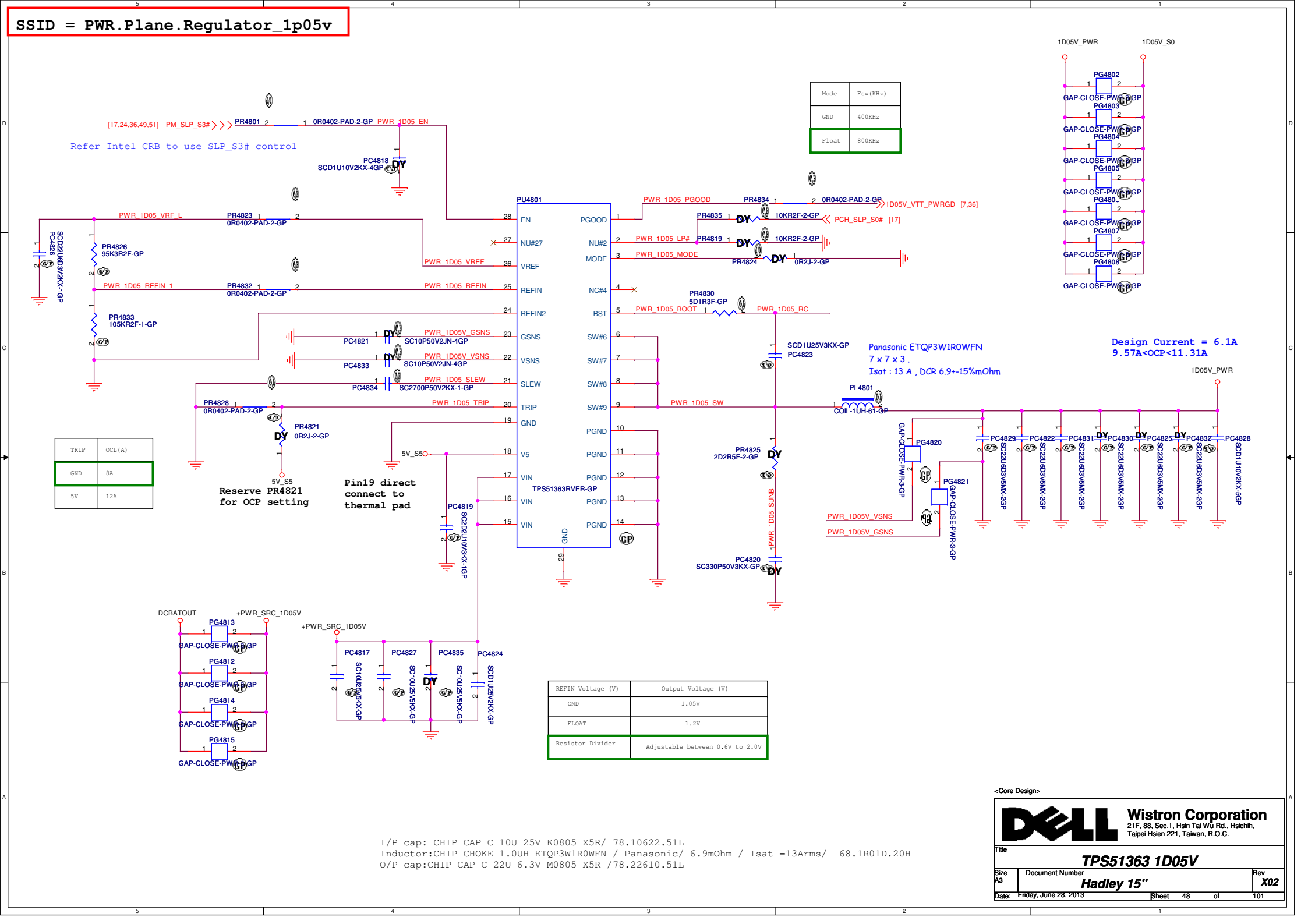
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(2/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 47 of 101

SSID = PWR.Plane.Regulator_1p05v



Mode	Fsw(KHz)
GND	400KHz
Float	800KHz

TRIP	OCL(A)
GND	8A
5V	12A

REFIN Voltage (V)	Output Voltage (V)
GND	1.05V
FLOAT	1.2V
Resistor Divider	Adjustable between 0.6V to 2.0V

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

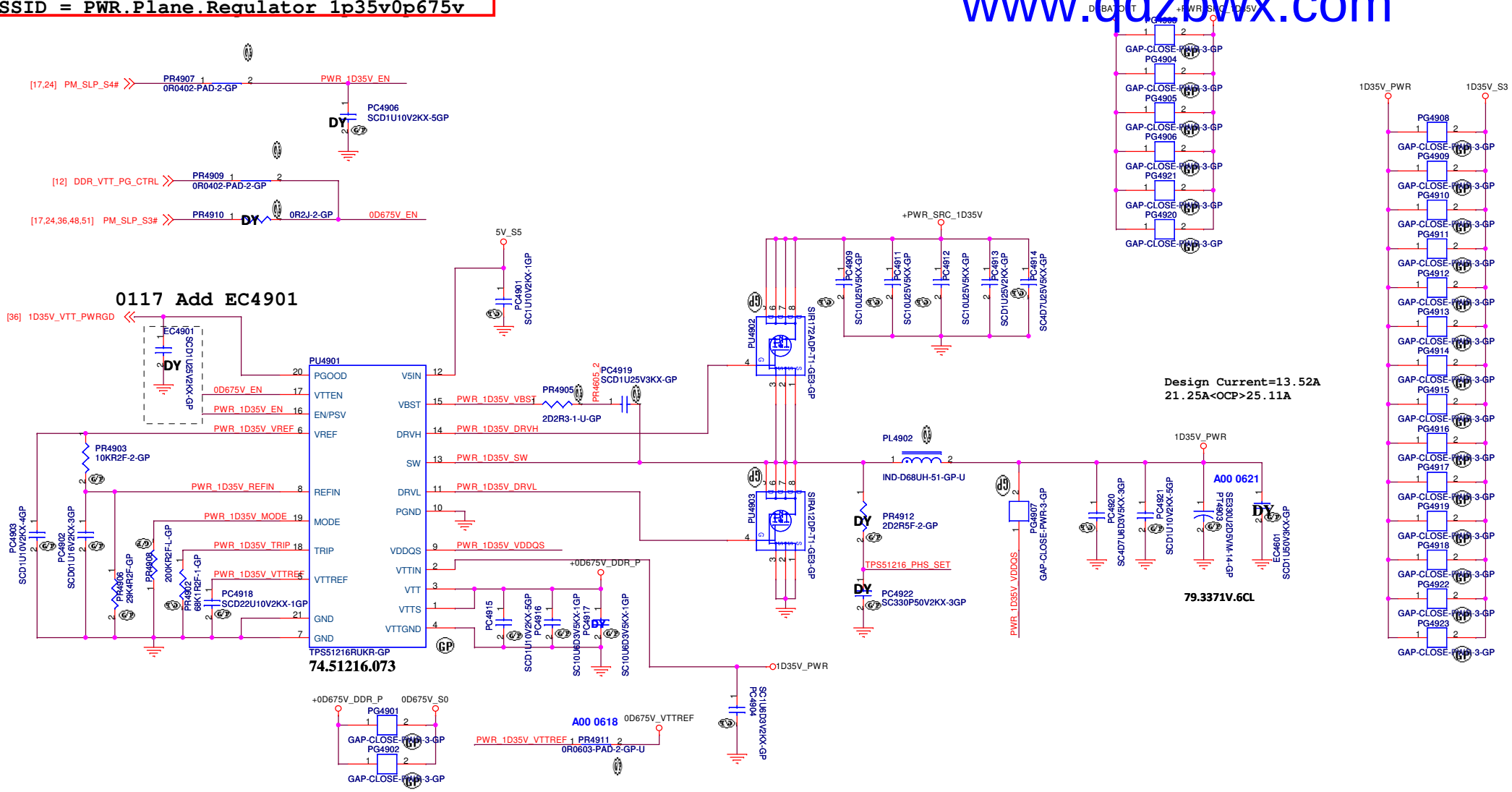
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363 1D05V

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 48 of 101

SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.35V_SUS
Size: A3
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 28, 2013
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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

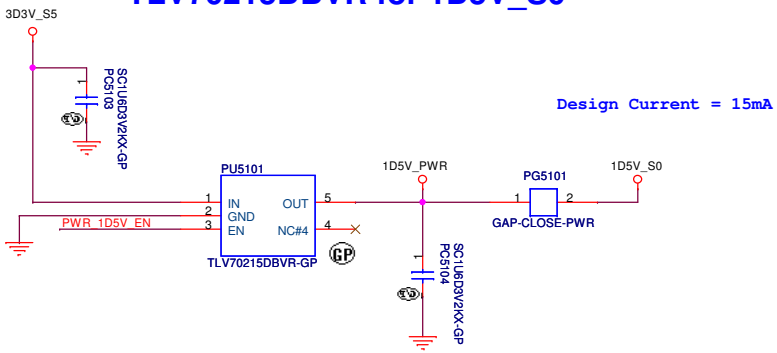
Title: (Reserved)TPS51312 1D8V

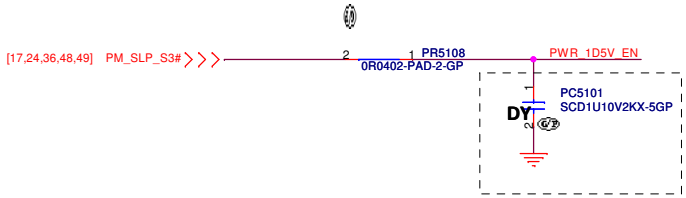
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 50 of 101

SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0





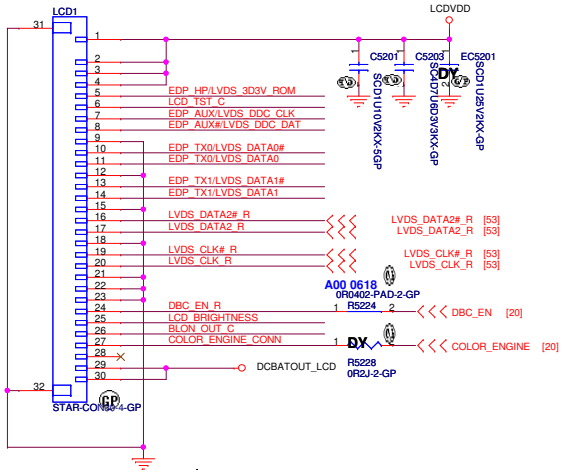
0108 Reserve PC5101

<Core Design>

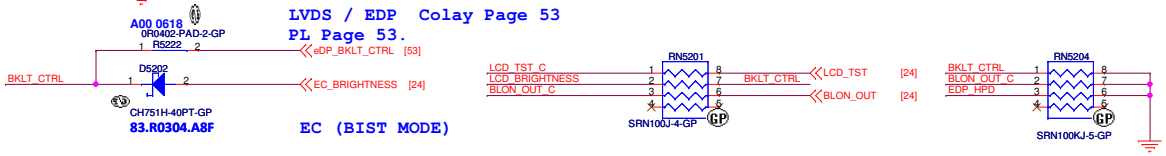
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9198-15PU5R_1D5V	
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 51 of 101	

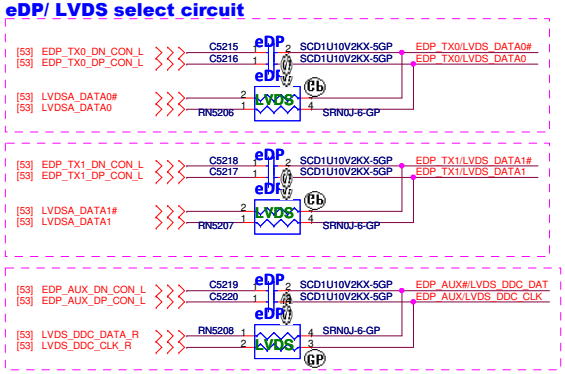
SSID = VIDEO



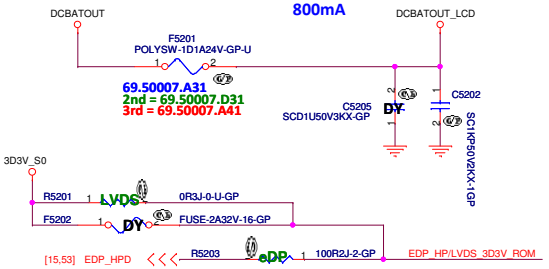
Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2#
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_R
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD



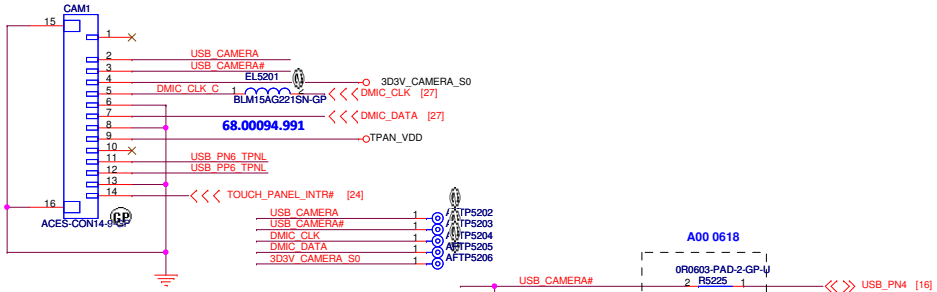
eDP/ LVDS select circuit



INVERTER POWER

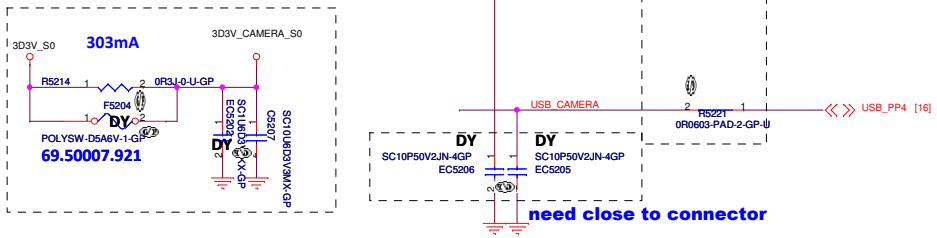


X02 change CAM1 connector



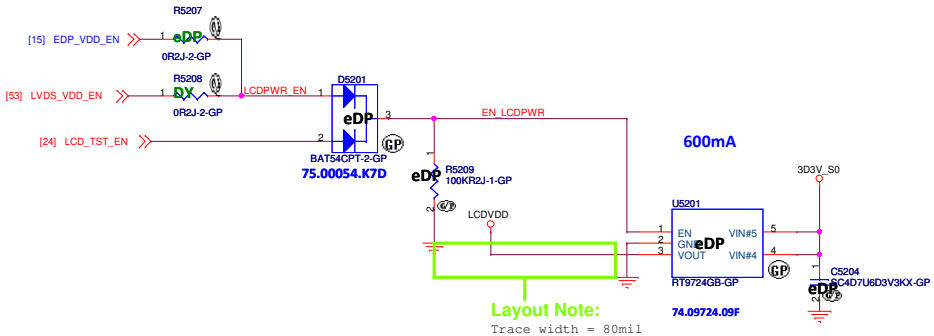
Camera Power

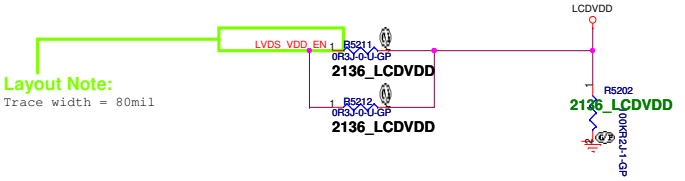
CAMERA



LCDVDD

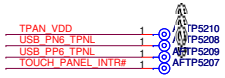
LCD Power

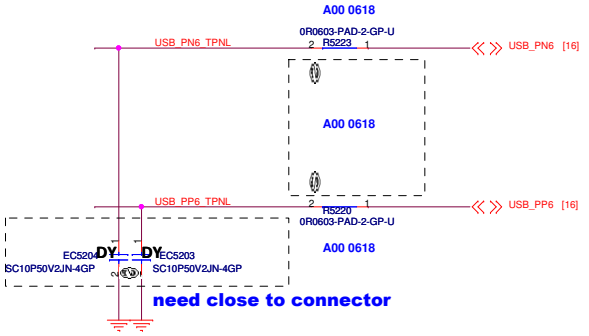




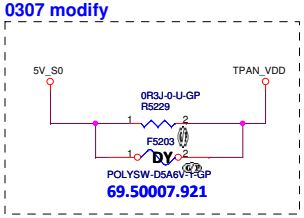
Touch panel

X02 remove TPNL1





0307 modify



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 52 of 101

SSID = VIDEO

LVDS & EDP Colay

Layout Note:
Place near U5301

[8] EDP_TX1_DN
[8] EDP_TX1_DP
C5209 SCD1U10V2KX-5GP EDP_TX1_DN_RTS2136
C5210 SCD1U10V2KX-5GP EDP_TX1_DP_RTS2136
RN5303 SRN0J-6-GP
EDP_TX1_DN_CON_L
EDP_TX1_DP_CON_L
EDP_TX1_DN_CON_L [52]
EDP_TX1_DP_CON_L [52]

[8] EDP_TX0_DN
[8] EDP_TX0_DP
C5211 SCD1U10V2KX-5GP EDP_TX0_DN_RTS2136
C5212 SCD1U10V2KX-5GP EDP_TX0_DP_RTS2136
RN5302 SRN0J-6-GP
EDP_TX0_DN_CON_L
EDP_TX0_DP_CON_L
EDP_TX0_DN_CON_L [52]
EDP_TX0_DP_CON_L [52]

[8] EDP_AUX_DN
[8] EDP_AUX_DP
C5213 SCD1U10V2KX-5GP EDP_AUX_DN_RTS2136
C5214 SCD1U10V2KX-5GP EDP_AUX_DP_RTS2136
RN5304 SRN0J-6-GP
EDP_AUX_DN_CON_L
EDP_AUX_DP_CON_L
EDP_AUX_DN_CON_L [52]
EDP_AUX_DP_CON_L [52]

Brightness

[15] L_BKLT_CTRL
R5319 0R2J-2-GP 2136_PWM_IN
R5320 0R2J-2-GP eDP_BKLT_CTRL
eDP_BKLT_CTRL [52]
R5302 1KR2J-1-GP
[15,52] EDP_HPD
EDP_HPD_RTS2136

3D3V_S0
L5301 MPZ1608S600AT-GP 68.00212.011
DP_AVCC33
C5312 SCD1U10V2KX-5GP
C5303 SCD1U10V2KX-5GP
C5301 SC10U6D3V3MX-GP

3D3V_S0
L5302 MPZ1608S600AT-GP 68.00212.011
DP_DVCC33
C5317 SCD1U10V2KX-5GP
C5313 SCD1U10V2KX-5GP
C5302 SC10U6D3V3MX-GP

L5303 IND-4D7UH-300-GP
SWR_LX
SWR_V12
2136_SW
A00 0618
0R0603-PAD-2-GP-U
R5314
C5304 SC10U6D3V3MX-GP
C5306 SCD1U10V2KX-5GP

X02 change to 4P2R
RN5306 SRN100KJ-6-GP
TEST_MODE
2136_PWM_IN

[24] LVDS_R2136_BKLT_EN
[52] LVDS_DDC_DATA_R
[52] LVDS_DDC_CLK_R
EEPROM_SDA0
EEPROM_SCL0
SWR_V12
C5311 SCD1U10V2KX-5GP

U5301 RTD2136R-CGT-GP 71.02136.B03
GND
MODE_CFG1
MODE_CFG0
MICSDA
MICSCL
BL_EN
VCCK
TXO0-
TXO0+
TXO1-
TXO1+
TXO2-
TXO2+
HPD
TEST
AUX_N
AUX_P
DP_V33
DP_GND
LANE0_P
LANE0_N
LANE1_P
LANE1_N
DP_V12
DP_REXT
TXOC-
TXOC+
TXO3-
TXO3+
TXE0-
TXE0+
TXE1-
TXE1+
TXE2-
TXE2+
TXEC-
TXEC+
CIICSCL
CIICSDA
SWR_VCCK
SWR_GND
SWR_LX
SWR_VDD
PWM_OUT
PANEL_VCC
PWM_IN
PVCC
TXE3+
TXE3-

LVDSA_DATA0# [52]
LVDSA_DATA0 [52]
LVDSA_DATA1# [52]
LVDSA_DATA1 [52]
LVDSA_DATA2# [52]
LVDSA_DATA2 [52]
LVDS_CLK#_R [52]
LVDS_CLK_R [52]

EDP_HPD_RTS2136
TEST_MODE
EDP_AUX_DN_RTS2136
EDP_AUX_DP_RTS2136
DP_AVCC33
EDP_TX0_DP_RTS2136
EDP_TX0_DN_RTS2136
EDP_TX1_DP_RTS2136
EDP_TX1_DN_RTS2136
SWR_V12
DP_REXT

Close to PIN5
DP_AVCC33
C5316 SCD1U10V2KX-5GP
C5310 SCD1U10V2KX-5GP
R5301 12KR2F-L-GP

CIICSCL1
CIICSDA1
SWR_V12
SWR_LX
DP_DVCC33
C5309 SCD1U10V2KX-5GP

[52] eDP_BKLT_CTRL
[52] LVDS_VDD_EN
2136_PWM_IN

DP_DVCC33
C5308 SCD1U10V2KX-5GP
C5307 SCD1U10V2KX-5GP
Close to PIN13

3D3V_S0
R5306 4K7R2J-2-GP
R5317 4K7R2J-2-GP
EEPROM_SCL0
EEPROM_SDA0
R5318 4K7R2J-2-GP
R5307 4K7R2J-2-GP

Operation Mode Table

		PIN47	
		0	1
PIN48	0	X	EP Mode
	1	ROM	EEPOOM

RN5301 SRN4K7J-10-GP
LVDS_DDC_DATA_R
LVDS_DDC_CLK_R
CIICSDA1
CIICSCL1
Q5301 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F
CIICSDA
CIICSCL
RN5307 SRN0J-6-GP
SML0_DATA [18]
SML0_CLK [18]
PCH
PCH
RN5305 SRN0J-6-GP
BAT_SDA [24,43,44]
BAT_SCL [24,43,44]
KBC
KBC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch
Size: Custom
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 28, 2013
Sheet 53 of 101

SSID = VIDEO

0307 change RN5401 RN5402 form 680 ohm to 470 ohm

5V_S0 — F5401 POLYSW-1D1A8V-5-GP — 5V_HDMI_S0

U5401 2N7002K-2-GP 84.2N702.J31 — HDMI_PLL_GND

RN5402 SRN470J-5-GP — RN5401 SRN470J-5-GP

[8] HDMI_CLK#	C5401	SCD1U10V2KX-5GP	HDMI_CLK_R_C#
[8] HDMI_CLK	C5402	SCD1U10V2KX-5GP	HDMI_CLK_R_C
[8] HDMI_DATA0#	C5403	SCD1U10V2KX-5GP	HDMI_DATA0_R_C#
[8] HDMI_DATA0	C5404	SCD1U10V2KX-5GP	HDMI_DATA0_R_C
[8] HDMI_DATA1#	C5405	SCD1U10V2KX-5GP	HDMI_DATA1_R_C#
[8] HDMI_DATA1	C5406	SCD1U10V2KX-5GP	HDMI_DATA1_R_C
[8] HDMI_DATA2#	C5407	SCD1U10V2KX-5GP	HDMI_DATA2_R_C#
[8] HDMI_DATA2	C5408	SCD1U10V2KX-5GP	HDMI_DATA2_R_C

0R3J-0-U-GP R5401 — HDMI_CLK_R_C → HDMI_CLK_R_C_CON — A00 0618 — A00 0619 ER5401 150R2J-L1-GP-U

0R3J-0-U-GP R5402 — HDMI_CLK_R_C# → HDMI_CLK_R_C#_CON

0R3J-0-U-GP R5403 — HDMI_DATA0_R_C → HDMI_DATA0_R_C_CON — A00 0618 — A00 0619 ER5402 150R2J-L1-GP-U

0R3J-0-U-GP R5404 — HDMI_DATA0_R_C# → HDMI_DATA0_R_C#_CON

0R3J-0-U-GP R5406 — HDMI_DATA2_R_C# → HDMI_DATA2_R_C#_CON

0R3J-0-U-GP R5407 — HDMI_DATA1_R_C → HDMI_DATA1_R_C_CON — A00 0618 — A00 0619 ER5404 150R2J-L1-GP-U

0R3J-0-U-GP R5408 — HDMI_DATA1_R_C# → HDMI_DATA1_R_C#_CON

ER5401~04 change to 180R

5V_HDMI_S0 — D5401 BAW56-11-GP — 75.00056.B7D — 2nd = 75.00056.A7D — D5102

RN5203 SRN2K2J-1-GP

3D3V_S0

[15] PCH_HDMI_CLK — DDC_CLK_HDMI

[15] PCH_HDMI_DATA — DDC_DATA_HDMI

Q5401 2N7002KDW-GP 84.2N702.A3F

HDMI CONN

HDMI1 SKT-HDMI23-97-GP 22.10296.A31

HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

5V_HDMI_S0 — AFTP5401 — C5417 SCD1U10V2KX-5GP — TP5411

3D3V_S0

PMBS3904-1-GP Q5402 84.03904.L06 — HDMI_HPD_B — R5411 150KR2J-L1-GP

[15] HDMI_PCH_DET — R5413 0R0402-PAD-2-GP — HDMI_HPD_E

R5414 10KR2J-3-GP

DY R5412 20KR2J-L2-GP

<Core Design>

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Title: HDMI Repeater/Connector

Size: A3 | Document Number: Hadley 15" | Rev: X02

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(Blanking)

<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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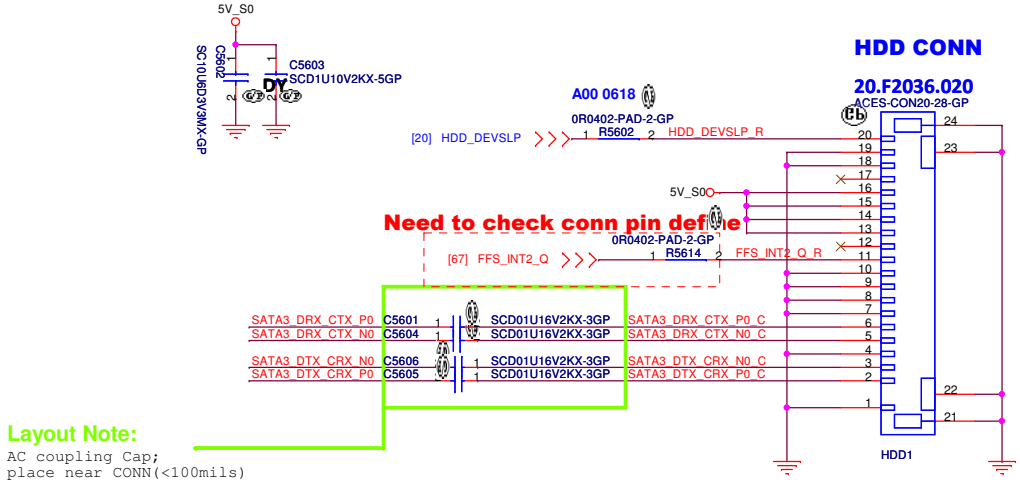
SSID = SATA



Layout Note:

AC coupling Cap;
place near CONN(<100mils)

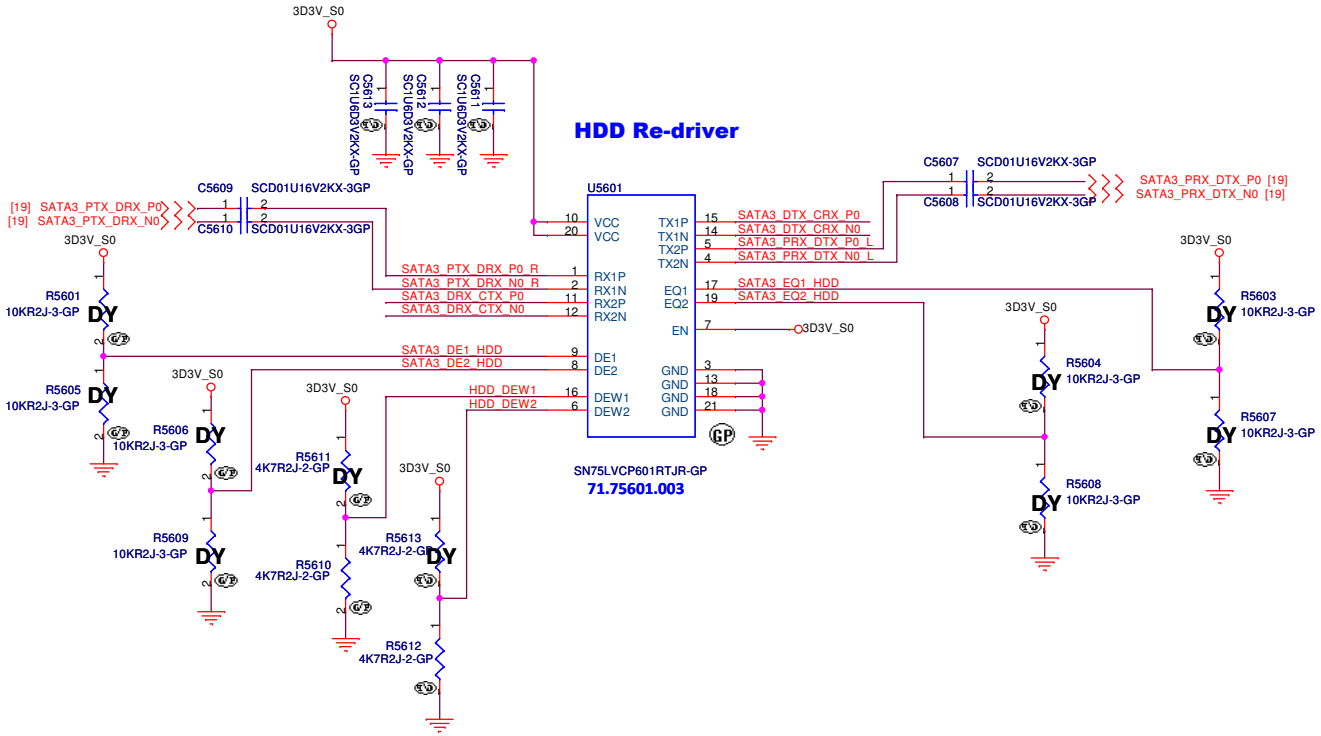


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps
NC (*default*)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (*default*)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (*default*)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

<Core Design>

Wistron Corporation
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Title: HDD

Size: A3 | Document Number: Hadley 15" | Rev: X02

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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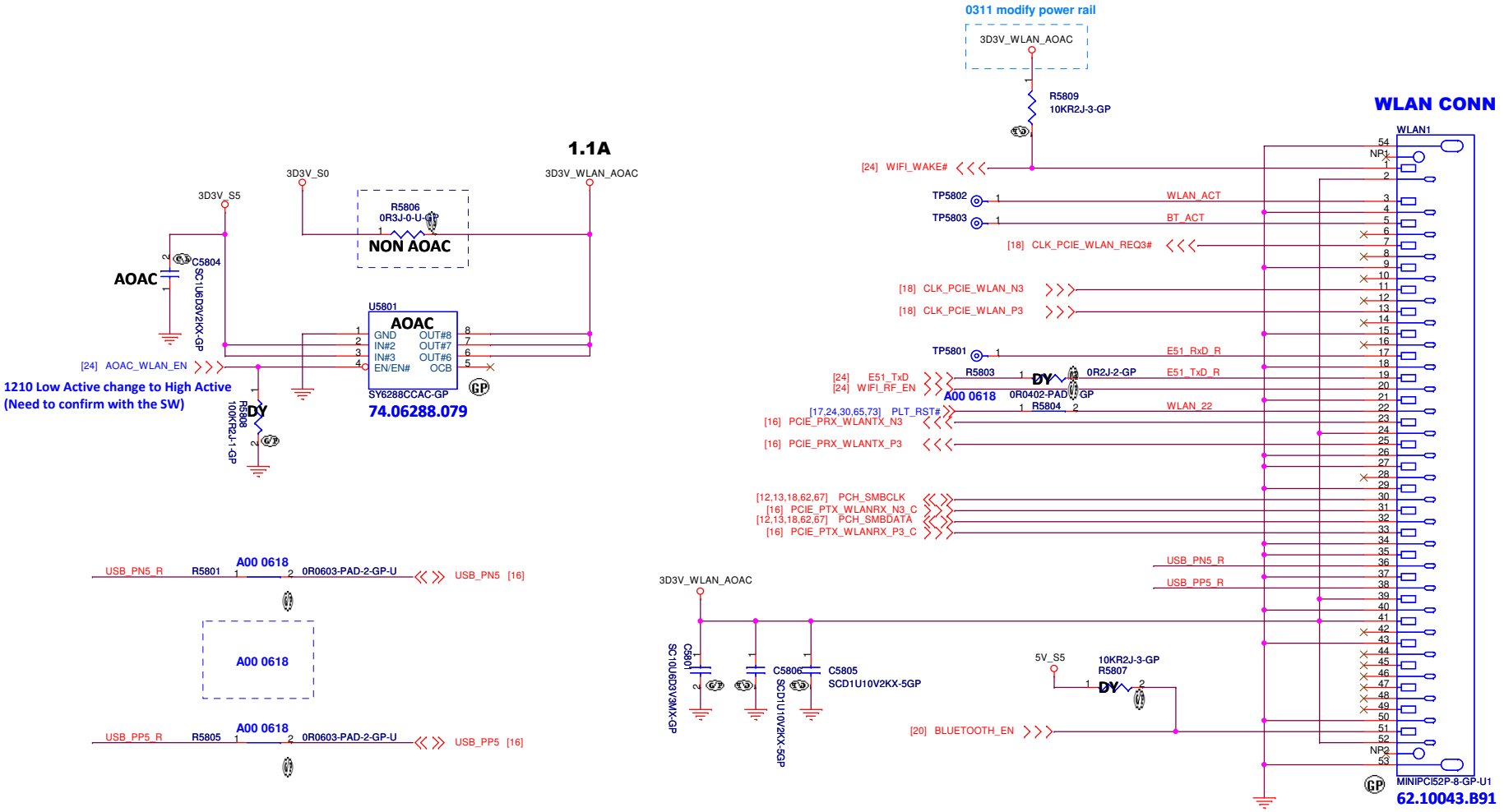
SSID = Wireless



<Core Design>

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Title	WLAN/BT	
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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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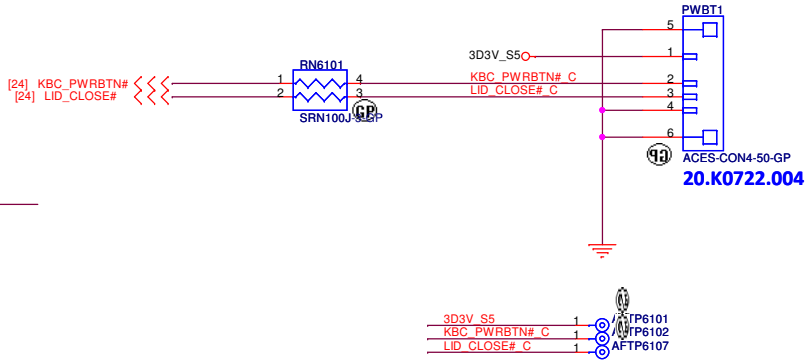
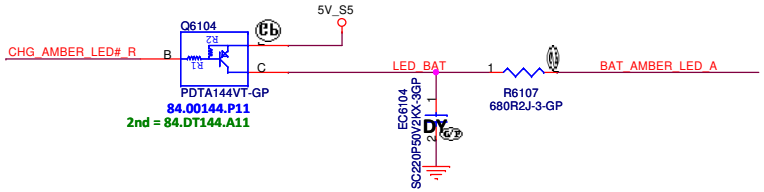
SSID = User.Interface

PWRBTN CONN



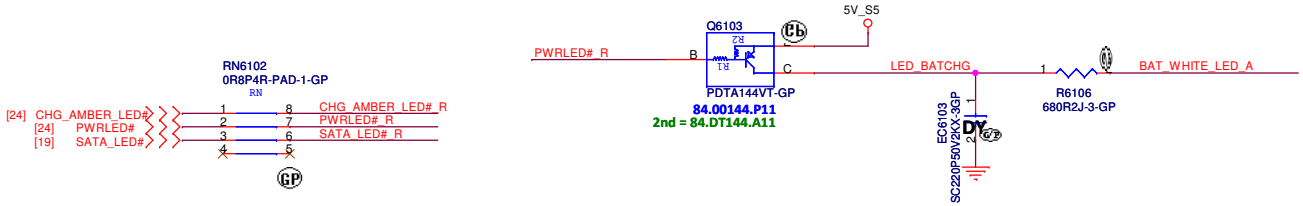
Battery LED1(Amber_LED)

LOW actived from KBC GPIO

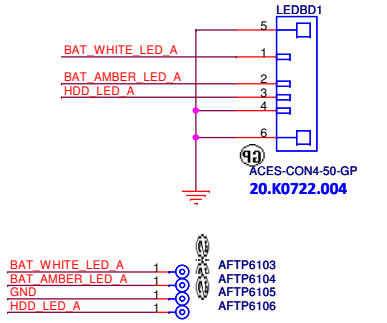


Power & Battery LED2(White_LED)

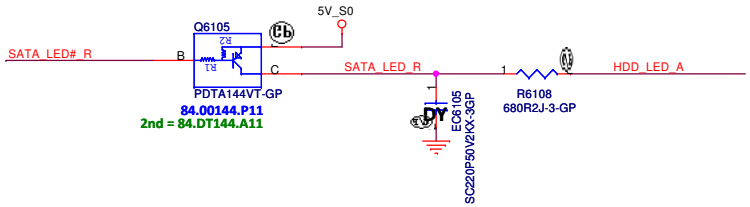
LOW actived from KBC GPIO



LED board CONN



SATA HDD LED



<Core Design>

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Title	LED Bar/Power Button	
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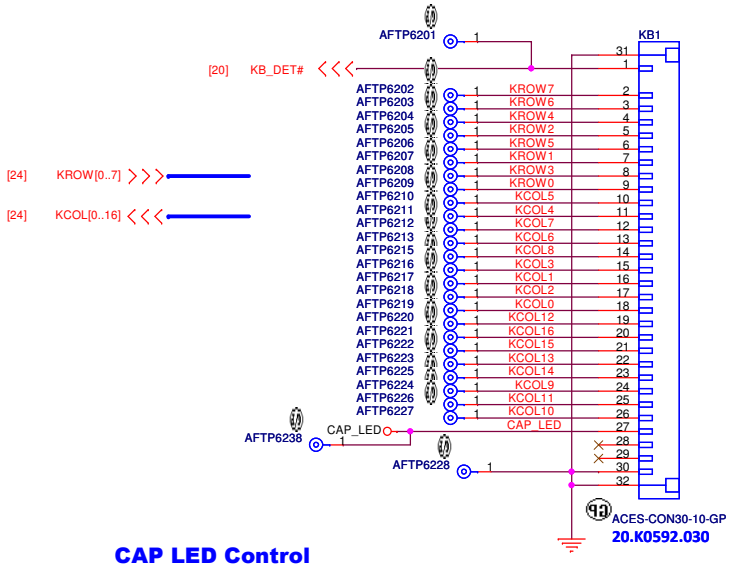
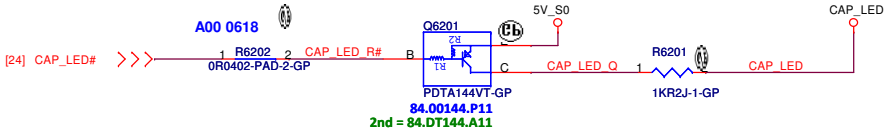
SSID = KBC

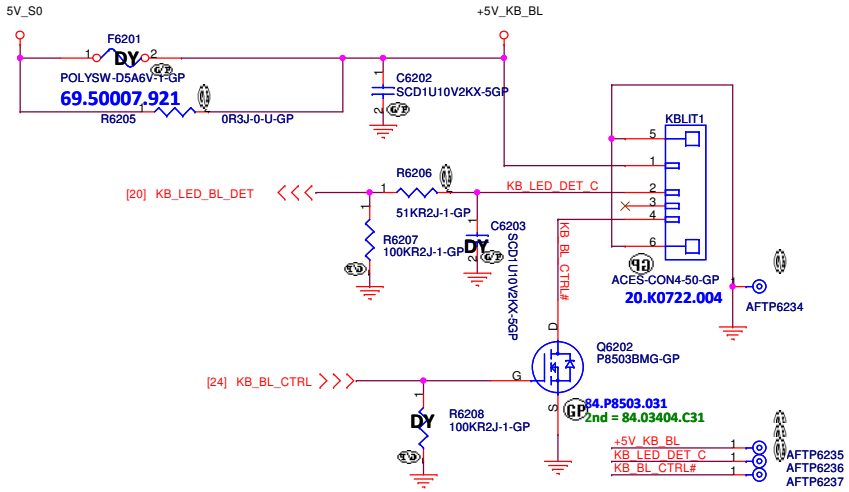
Internal Keyboard Connector



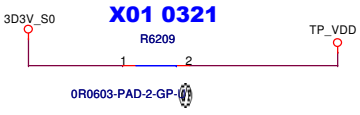
CAP LED Control

LOW actived from KBC GPIO

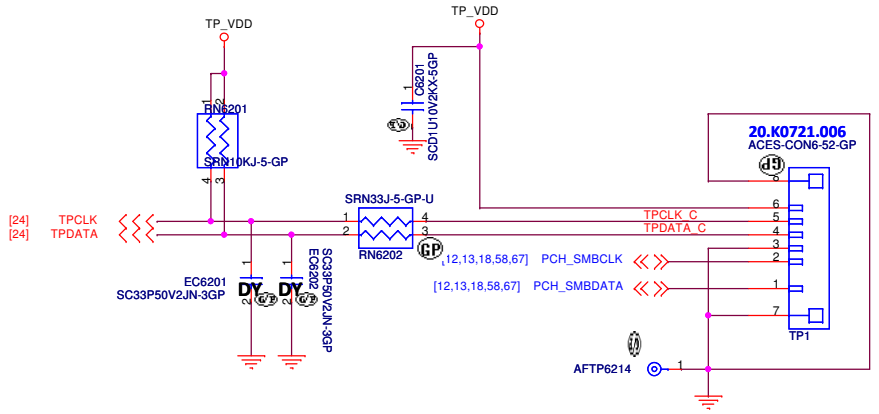


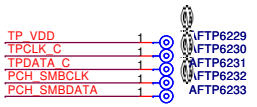


SSID = Touch.Pad



Touch Pad Connector





<Core Design>

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Title: *Reserved*		
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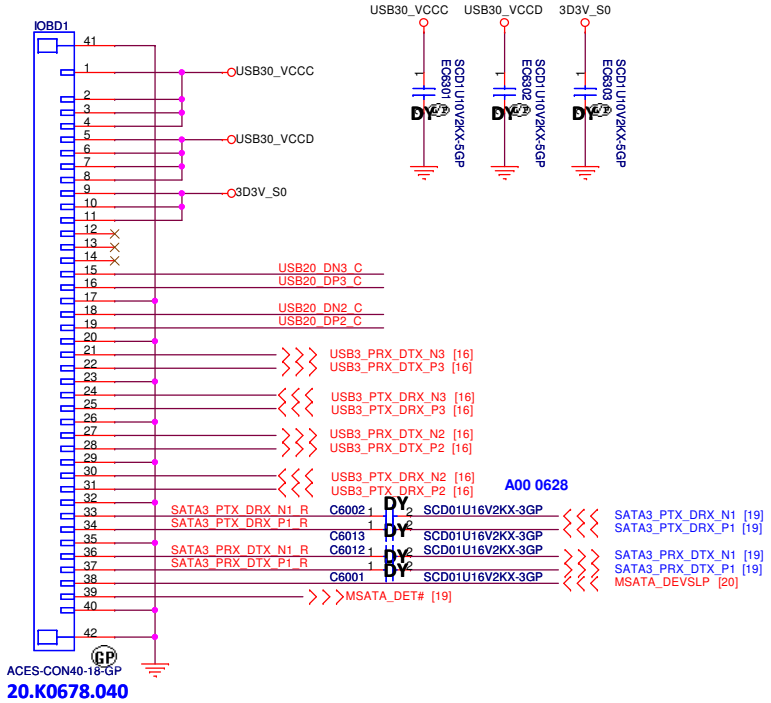
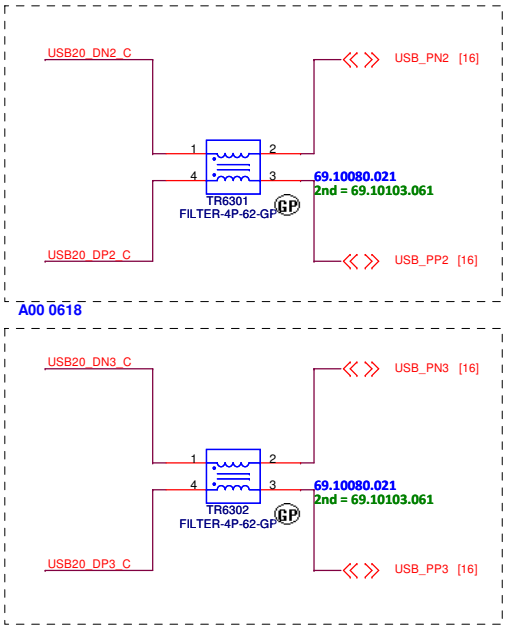
SSID = User.Interface





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Hadley 15"	X02

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

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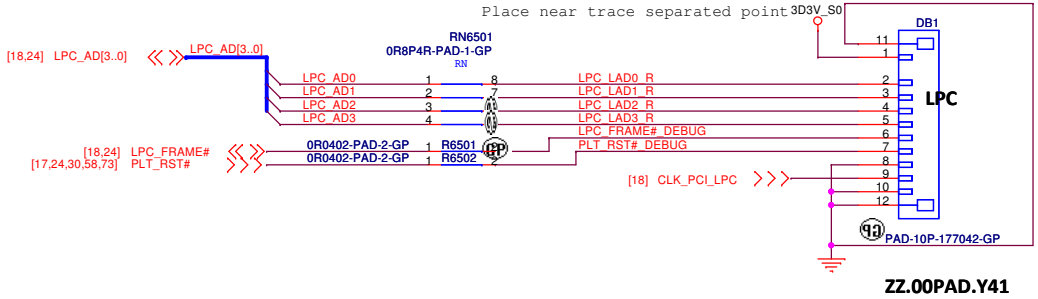
SSID = DEBUG PORT

Debug Connector

A00 0625



ZZ.00PAD.Y41

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*		
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<Core Design>

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Title

Reserved

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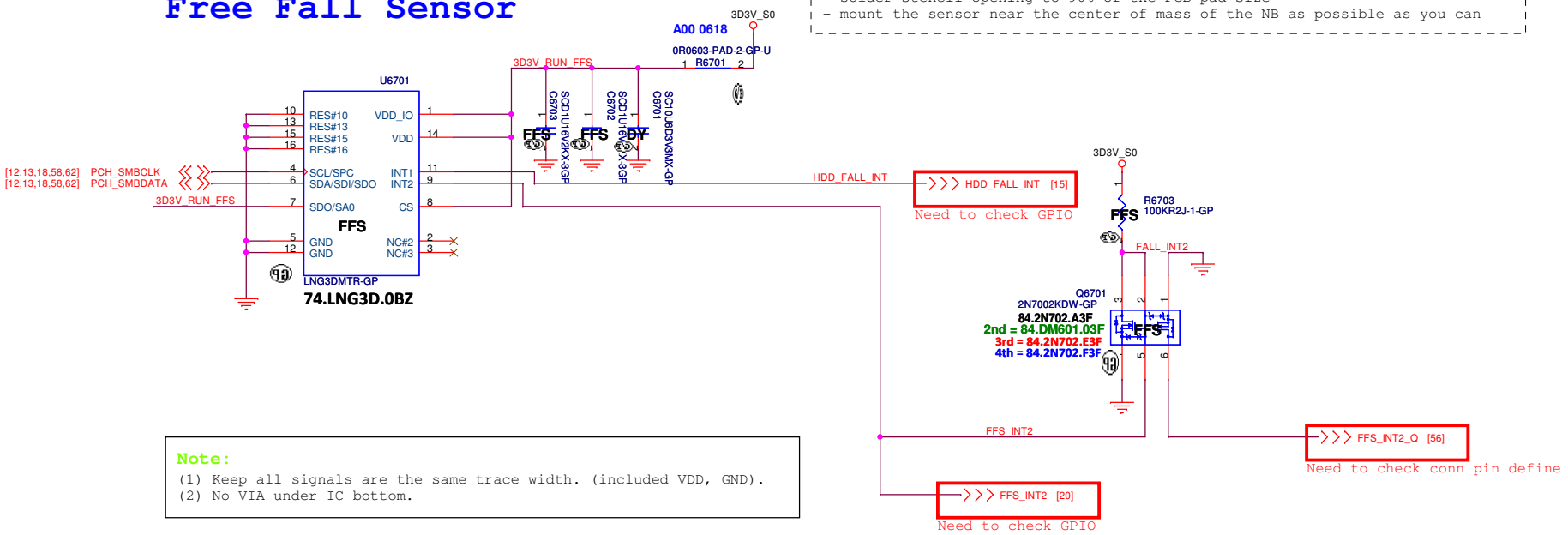
SSID = User.Interface

Free Fall Sensor



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FFS		
Size: A3	Document Number: Hadley 15"	Rev: X02
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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
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<Core Design>

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Title: *Reserved*

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<Core Design>

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<Core Design>

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Title: *Reserved*

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<Core Design>

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SSID = VIDEO

dGPU Reset

[17,24,30,58,65] PLT_RST# → D7301 1SS400GPT-GP 83.00400.C1F → VGA_RST# [76]

2ND = 83.27101.01F

3RD = 83.01426.01F

A00 0618

[15] DGPU_HOLD_RST# → R7304 0R0402-PAD-2-GP

3D3V_VGA_S0

Q7301 2N7002K-2-GP 84.2N702.J31

[18] PEG_CLKREQ# → R7308 10KR2J-3-GP

R7305 0R2J-2-GP

VGA_RST# → PEX_RST#

GPU_CLKREQ# → PEX_CLKREQ#

[18] CLK_PCIE_VGA → PEX_REFCLK

[18] CLK_PCIE_VGA# → PEX_REFCLK#

GPU1A 1 OF 17

1/17 PCI_EXPRESS

GK107/GF108 GK208/GF117

NC — PEX_WAKE#

[16] CPU_RXP_C_dGPU_TXP0	C7301 SCD22U10V2KX-1GP → dGPU_TXP_CPU_RXP0 → PEX_TX0
[16] CPU_RXN_C_dGPU_TXN0	C7302 SCD22U10V2KX-1GP → dGPU_TXN_CPU_RXN0 → PEX_TX0#
[16] dGPU_RXP_C_CPU_TXP0	→ PEX_RX0
[16] dGPU_RXN_C_CPU_TXN0	→ PEX_RX0#
[16] CPU_RXP_C_dGPU_TXP1	C7303 SCD22U10V2KX-1GP → dGPU_TXP_CPU_RXP1 → PEX_TX1
[16] CPU_RXN_C_dGPU_TXN1	C7304 SCD22U10V2KX-1GP → dGPU_TXN_CPU_RXN1 → PEX_TX1#
[16] dGPU_RXP_C_CPU_TXP1	→ PEX_RX1
[16] dGPU_RXN_C_CPU_TXN1	→ PEX_RX1#
[16] CPU_RXP_C_dGPU_TXP2	C7305 SCD22U10V2KX-1GP → dGPU_TXP_CPU_RXP2 → PEX_TX2
[16] CPU_RXN_C_dGPU_TXN2	C7306 SCD22U10V2KX-1GP → dGPU_TXN_CPU_RXN2 → PEX_TX2#
[16] dGPU_RXP_C_CPU_TXP2	→ PEX_RX2
[16] dGPU_RXN_C_CPU_TXN2	→ PEX_RX2#
[16] CPU_RXP_C_dGPU_TXP3	C7307 SCD22U10V2KX-1GP → dGPU_TXP_CPU_RXP3 → PEX_TX3
[16] CPU_RXN_C_dGPU_TXN3	C7308 SCD22U10V2KX-1GP → dGPU_TXN_CPU_RXN3 → PEX_TX3#
[16] dGPU_RXP_C_CPU_TXP3	→ PEX_RX3
[16] dGPU_RXN_C_CPU_TXN3	→ PEX_RX3#

PEX_TX4 PEX_TX4# PEX_RX4 PEX_RX4# PEX_TX5 PEX_TX5# PEX_RX5 PEX_RX5# PEX_TX6 PEX_TX6# PEX_RX6 PEX_RX6# PEX_TX7 PEX_TX7# PEX_RX7 PEX_RX7# PEX_TX8 PEX_TX8# PEX_RX8 PEX_RX8# PEX_TX9 PEX_TX9# PEX_RX9 PEX_RX9# PEX_TX10 PEX_TX10# PEX_RX10 PEX_RX10# PEX_TX11 PEX_TX11# PEX_RX11 PEX_RX11# PEX_TX12 PEX_TX12# PEX_RX12 PEX_RX12# PEX_TX13 PEX_TX13# PEX_RX13 PEX_RX13# PEX_TX14 PEX_TX14# PEX_RX14 PEX_RX14# PEX_TX15 PEX_TX15# PEX_RX15 PEX_RX15#

PEX LANES 8 TO 15 NC FOR GF117/GK208

GF108	GK208/GK107/GF117
NC	PEX_PLL_HVDD

PEX_SVDD_3V3

PEX_IOVDD_1..6 — 1D05V_VGA_S0 — C7323 C7310 C7322 C7312 C7313 C7325 C7326 SC10U6D3V3MX-GP / SC1U6D3V2KX-GP

1.05V +/- 30mV
3.3A

PEX_IOVDDQ_1..14 — 1D05V_VGA_S0 — C7320 C7321 C7309 C7311 C7314 C7327 C7328 SC10U6D3V3MX-GP / SC1U6D3V2KX-GP / SC4D7U6D3V3KX-GP

3.3V +/- 5%
210mA

PEX_PLL_HVDD — 3D3V_VGA_S0 — C7316 SC1U10V2KX-5GP; C7315 C7324 SC4D7U6D3V3KX-GP

X7R, Under GPU.

VDD_SENSE → VGA_SENSE [82]

GND_SENSE → GND_SENSE [82]

POWER IC

NC_3V3AUX — P8

R7303 200R2F-L-GP

PEX_TSTCLK_OUT → PEXTSTCLK_OUT

PEX_TSTCLK_OUT# → PEXTSTCLK_OUT#

1.05V +/- 30mV
150mA

PEX_PLLVDD — 1D05V_VGA_S0 — C7318 SC1U10V2KX-5GP; C7317 SC4D7U6D3V3KX-GP; C7319 SC1U6D3V2KX-GP

0102 remove R7307

TESTMODE — R7302 10KR2J-3-GP

PEX_TERMP — R7301 2K49R2F-GP

N14P-GS-A1-GP
71.0N14P.00U

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: Custom | Document Number: Hadley 15" | Rev: X02

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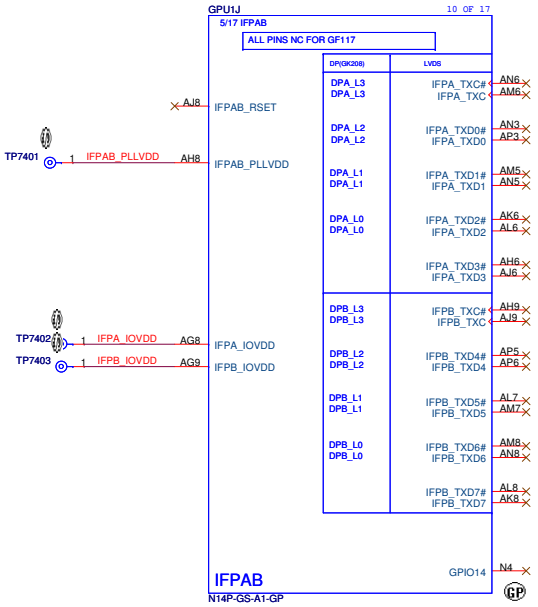
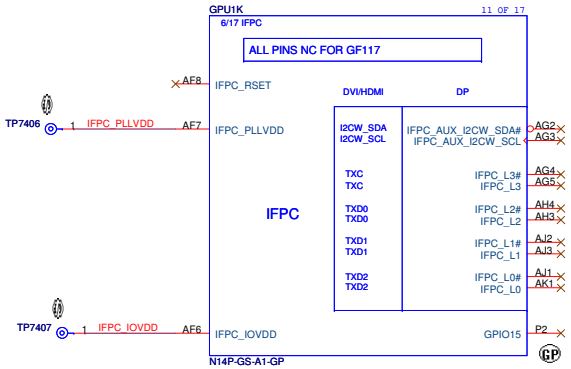
SSID = VIDEO



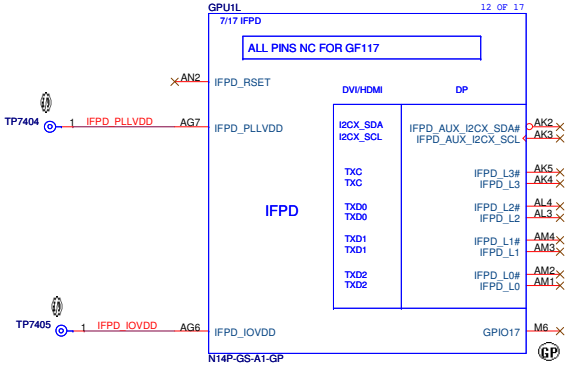
71.0N14P.00U

OPS



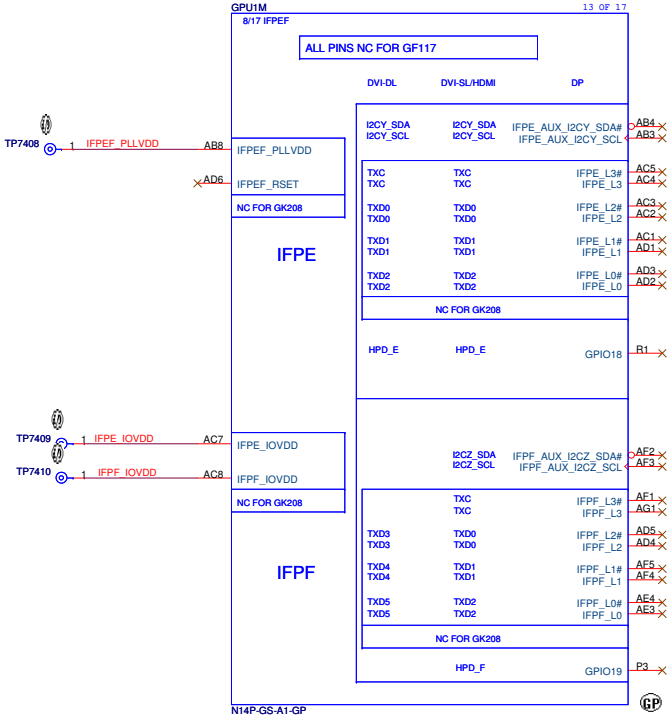
71.0N14P.00U

OPS



71.0N14P.00U

OPS



71.0N14P.00U

OPS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU Memory(2/5)**

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 74 of 101

SSID = VIDEO

A00 0618

Layout note:FBA_PLL_AVDD=16mil
Place close to Ball

0102 remove L7502
change K27 pin net name

0102 remove L7503
change C7506 to 0603 package

Place under GPU near

DA-05691-001_V05 P7

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

ALL PINS NC FOR GF117/GK208

NC	FBA_PLL_AVDD
GF108	GK107

1.35V +/- 3%
4.88A

GPU FBVDDQ Decoupling
PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO GPU BALLS

<Core Design>

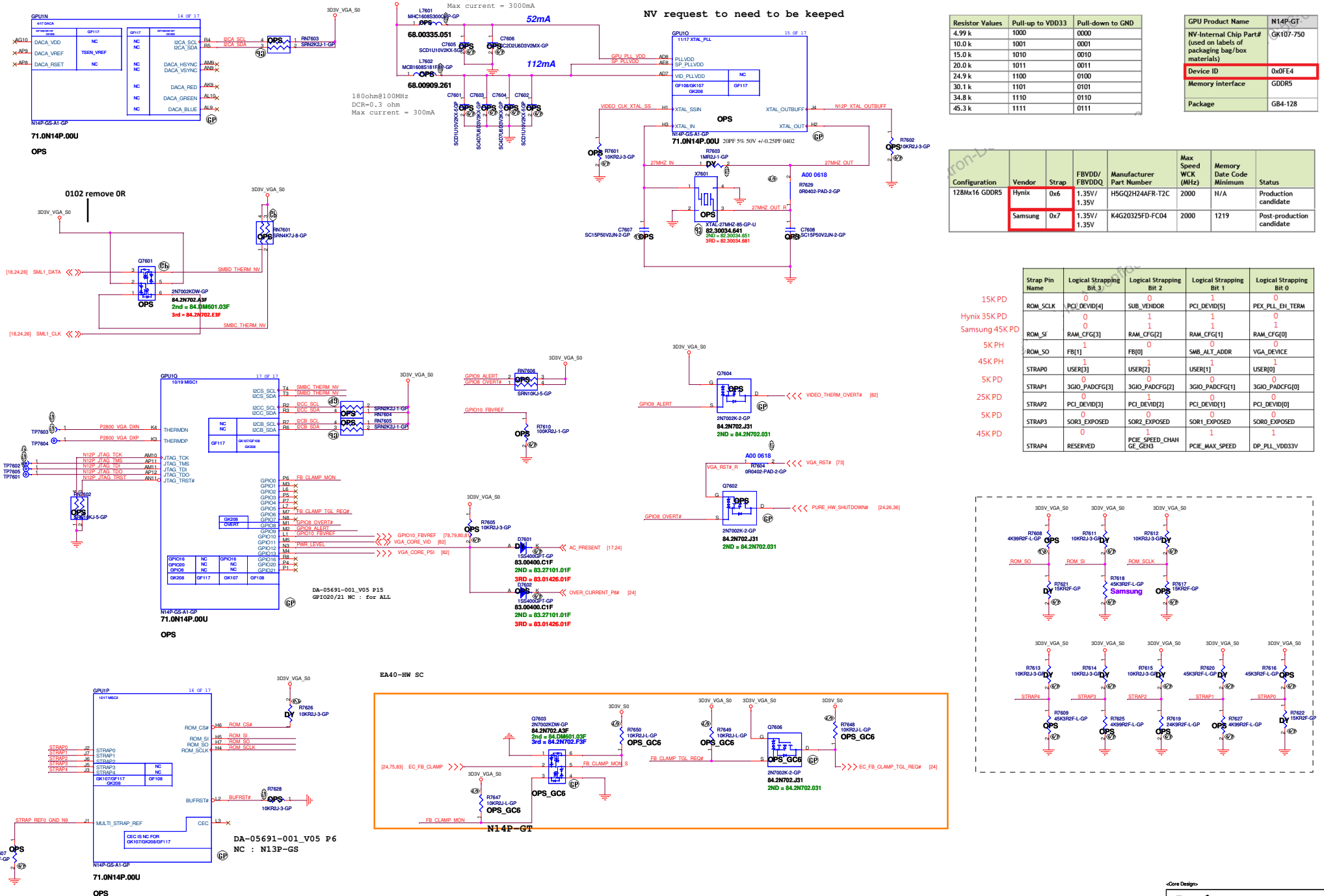
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 75 of 101

SSID = VIDEO



Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Post-production candidate

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

15K PD
Hynix 35K PD
Samsung 45K PD
5K PH
45K PH
5K PD
25K PD
5K PD
45K PD

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 76 of 101

SSID = VIDEO

VGA_CORE

Under GPU

N14P-GT : 45A

C7709 C7707 C7708 C7706 C7702 C7701 — OPS

C7725 C7722 C7723 C7724 C7721 C7720 C7719 — OPS

C7716 C7715 C7718 C7717 C7714 C7713 C7712 C7711 — OPS

NEAR TO GPU

C7703 C7705 C7710 — OPS; R7701 — UMA

GPU1H 8 OF 17 — 13/17 NVVDD

VDD_1 … VDD_72

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1F 6 OF 17 — 15/17 GND_1/2

GND_1 … GND_140

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1G 7 OF 17 — 16/17 GND_2/2

GND_141 … GND_198; AG11 GND_F; GND_H AH11; GND_OPT_1 C16; GND_OPT_2 W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1I 9 OF 17 — 9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1 … XVDD_38

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1E 5 OF 17 — 17/17 NC/VDD33

DA-05691-001_V05 P20
3V3MISC : N13P-GS

GK107	GK208 GF117
3V3MISC	3V3MISC_1
3V3MISC	3V3MISC_2

VDD33_1, VDD33_2

NC#AJ28, NC#C15, NC#D19, NC#D20, NC#D23, NC#D26, NC#H31, NC#V32

DNU#AC6, DNU#AJ4, DNU#AJ5, DNU#AL11, DNU#T8 — DO NOT CONNECT THESE PINS

N14P-GS-A1-GP

71.0N14P.00U

OPS

3.3V +/- 5%
85mA

3D3V_VGA_S0

C7704 C7729 C7727 C7728 — OPS; X7R X7R

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

<Core Design>

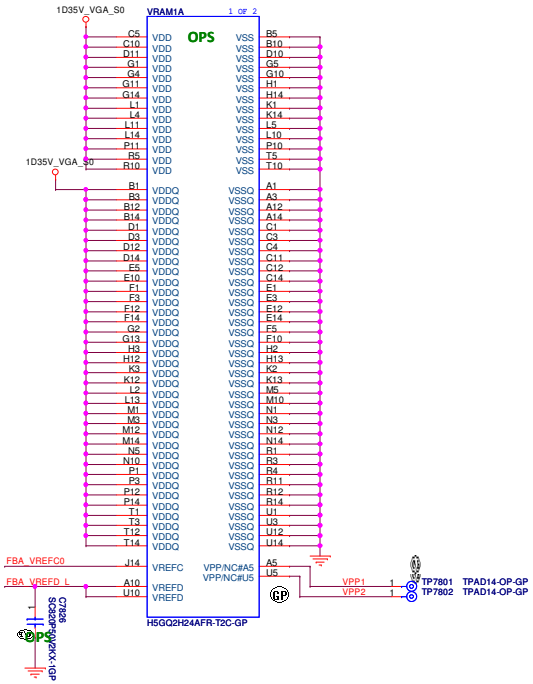
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU_POWER(4/5)*

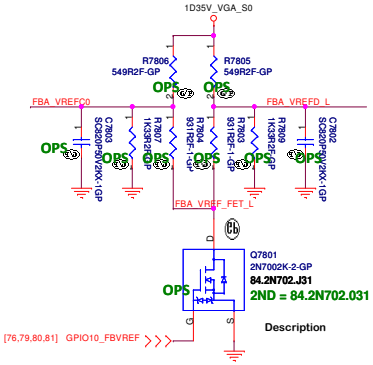
Size: Custom | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 28, 2013 | Sheet 77 of 101

SSID = VIDEO

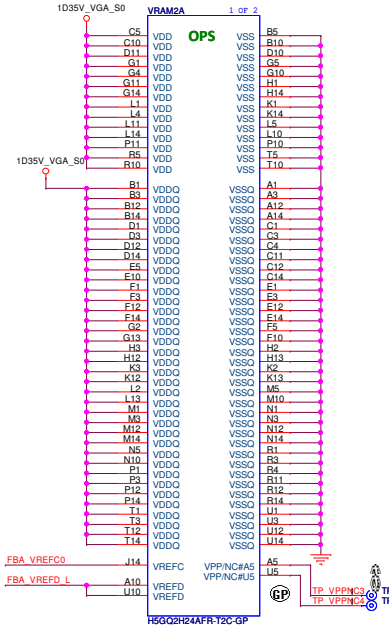


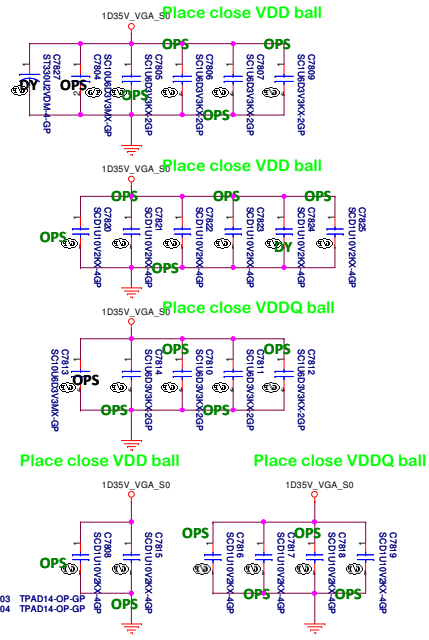
Frame Buffer Patition A-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

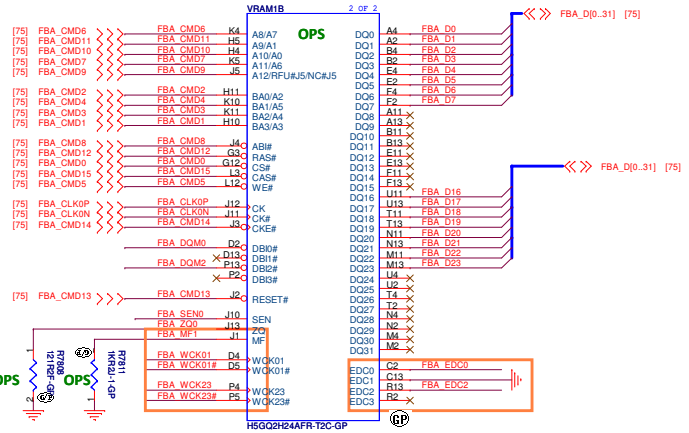




[75] FBA_EDC[0..3] — FBA_EDC0, FBA_EDC1, FBA_EDC2, FBA_EDC3

FBA_DQM0, FBA_DQM1, FBA_DQM2, FBA_DQM3 — FBA_DQM[0..3] [75]

Normal(MF=0)



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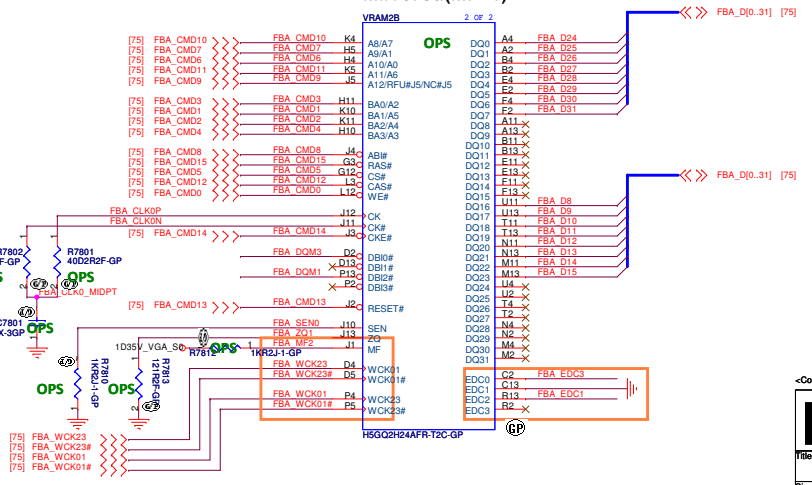


<Core Design>

DELL

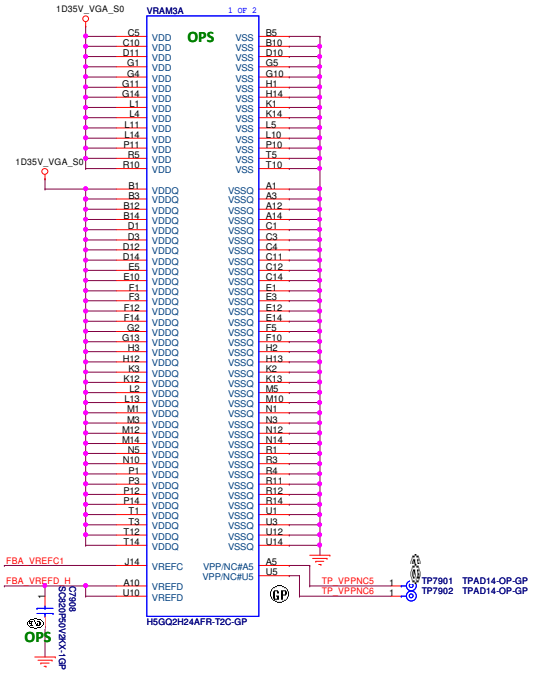
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

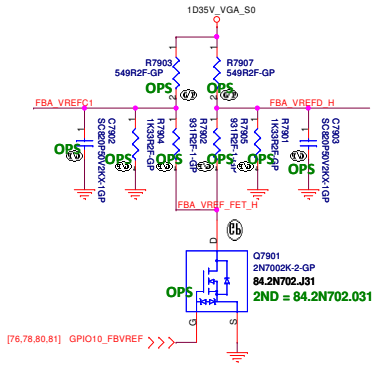
Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 78 of 101

SSID = VIDEO

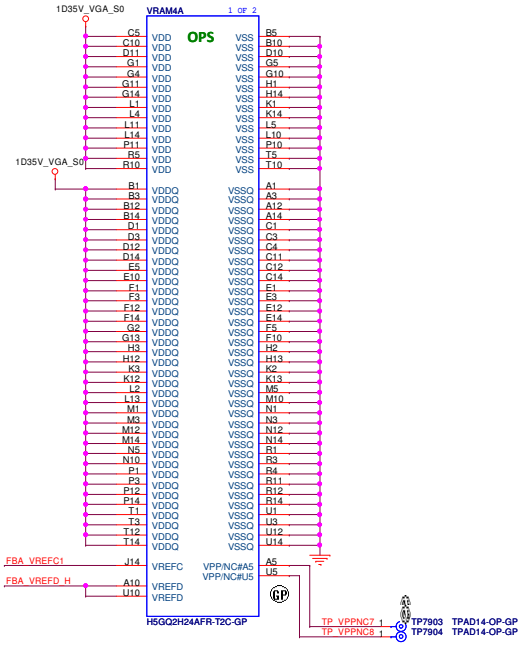


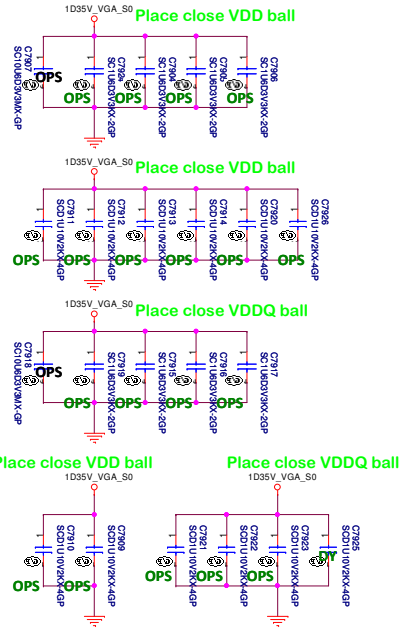
Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

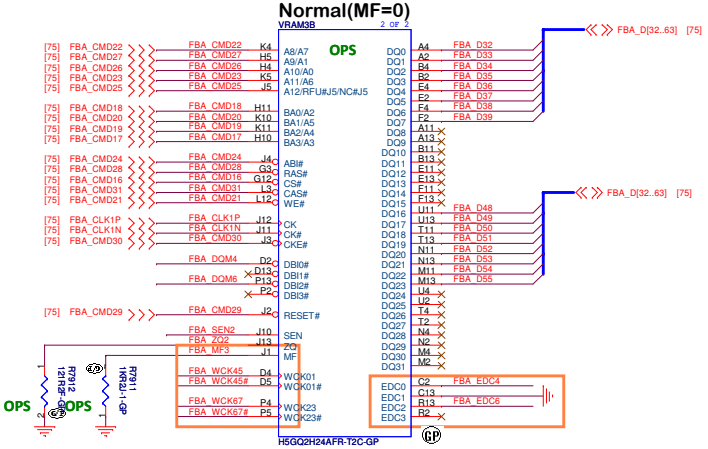




[75] FBA_EDC[4..7] — FBA_EDC4, FBA_EDC5, FBA_EDC6, FBA_EDC7

FBA_DQM4, FBA_DQM5, FBA_DQM6, FBA_DQM7 — FBA_DQM[4..7] [75]

Normal(MF=0)



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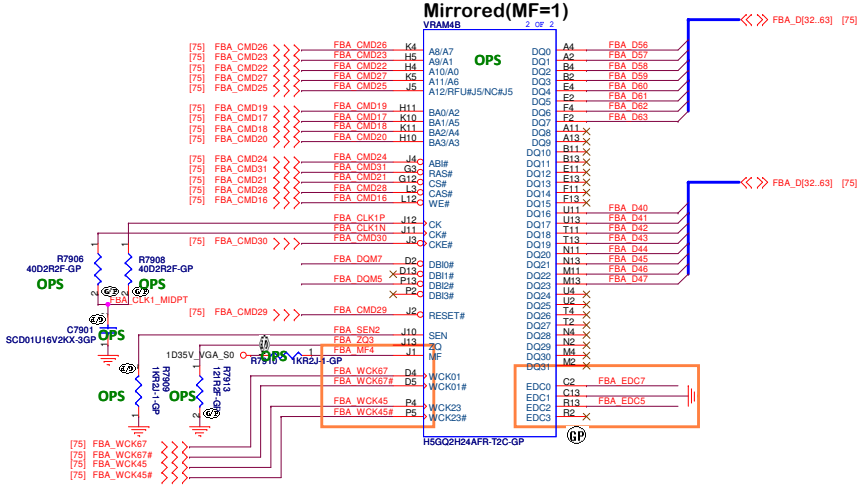

<Core Design>

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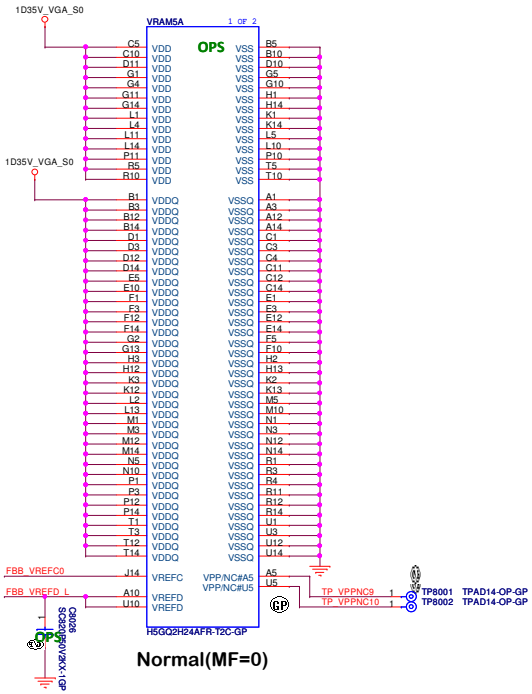
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Hadley 15" | Rev: X02

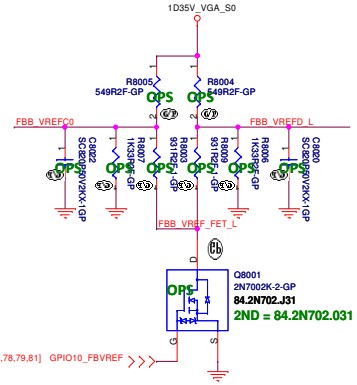
Date: Friday, June 28, 2013 | Sheet 79 of 101

SSID = VIDEO



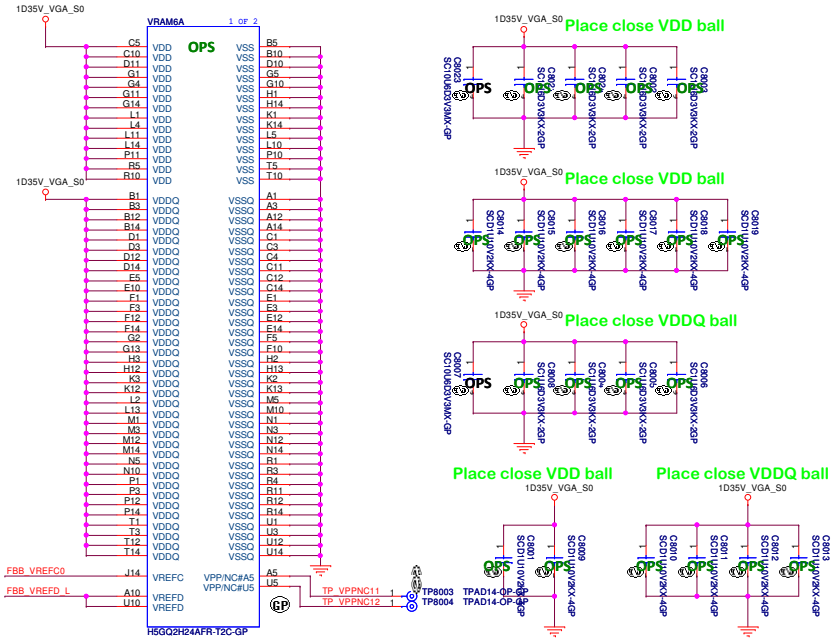
Normal(MF=0)

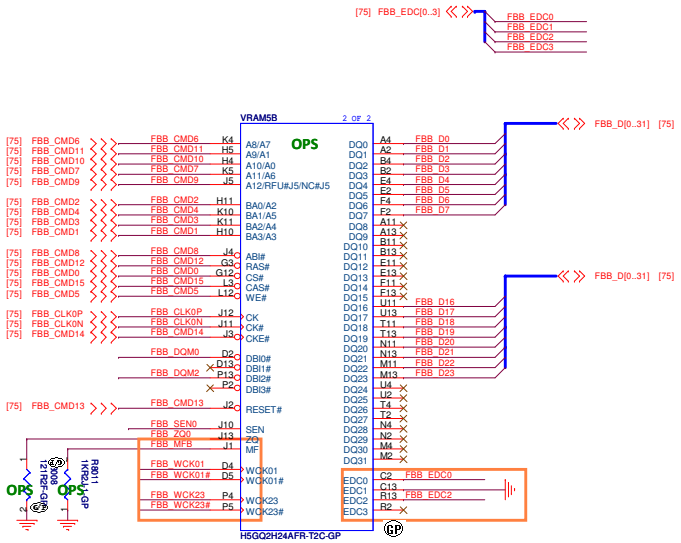
Frame Buffer Patition B-Lower Half

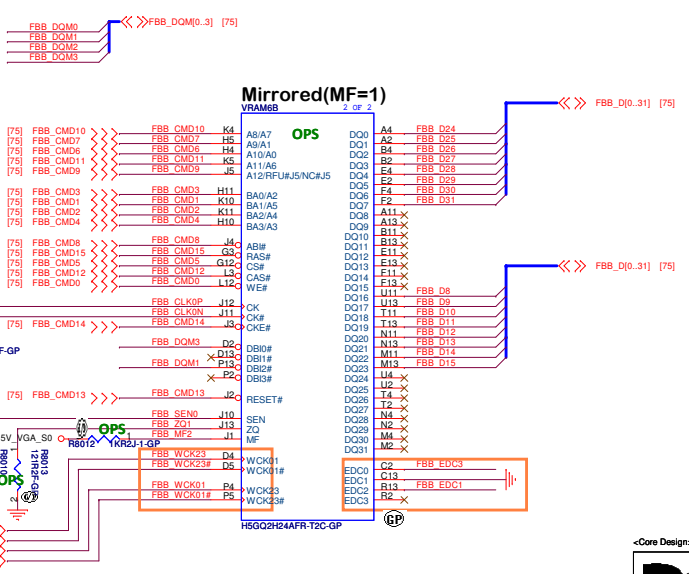


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low







Mirrored(MF=1)

<Core Design>

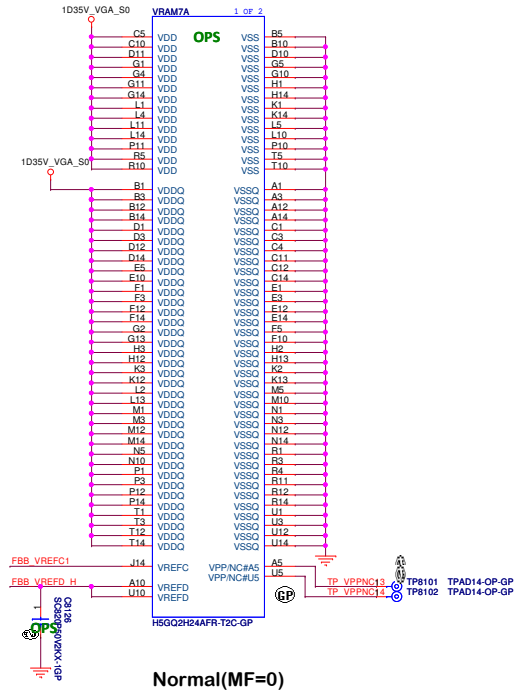
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	Hadley 15"	X02

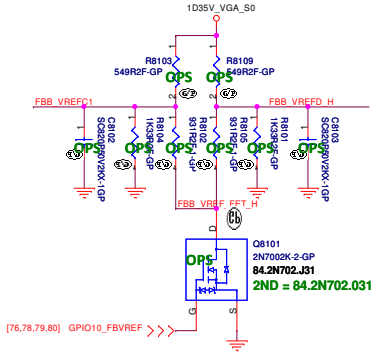
Date: Friday, June 28, 2013 Sheet 80 of 101

SSID = VIDEO



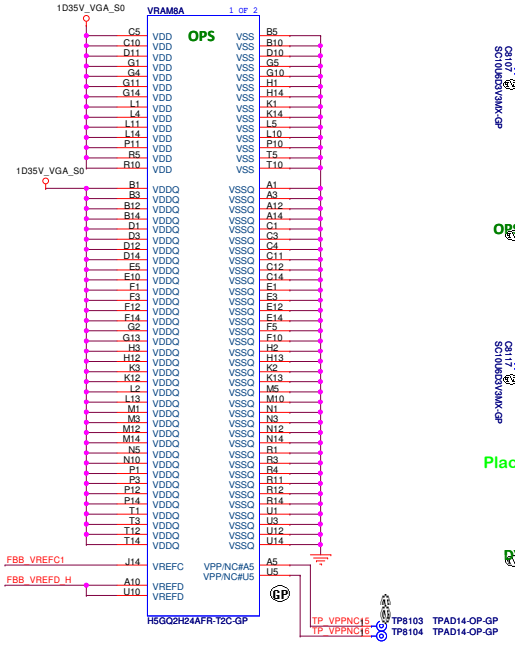
Normal(MF=0)

Frame Buffer Patition B-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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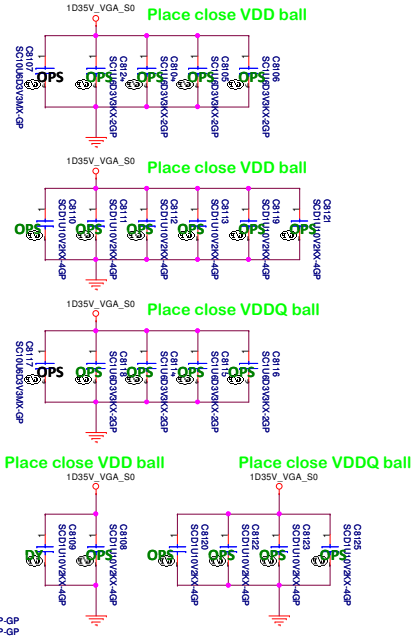
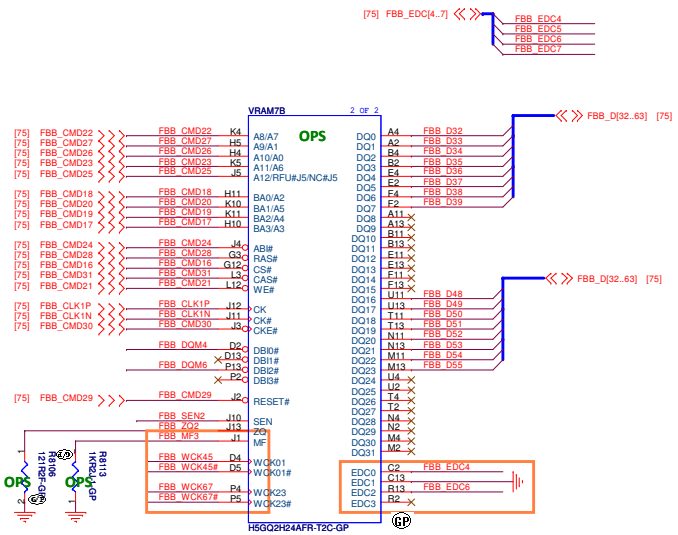
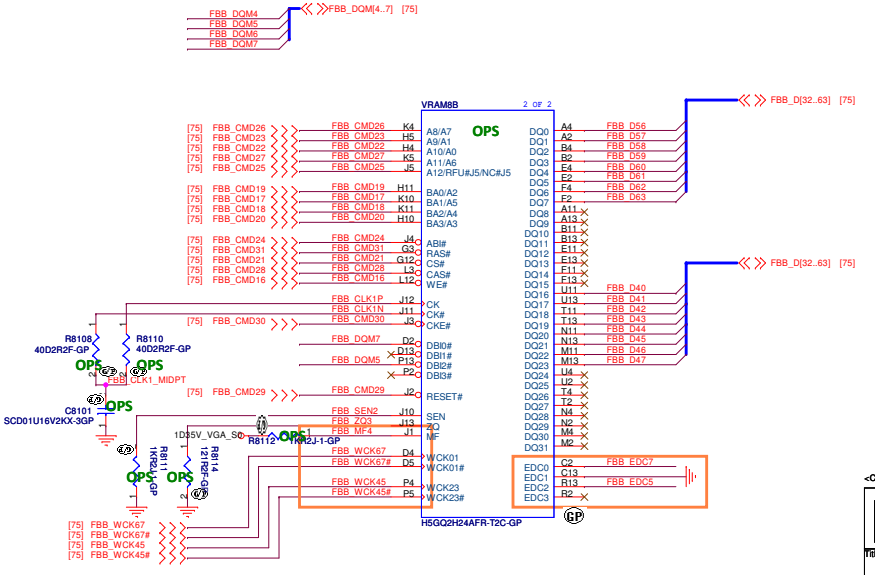






<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

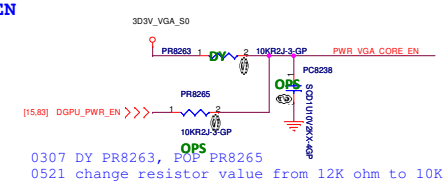
Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 81 of 101

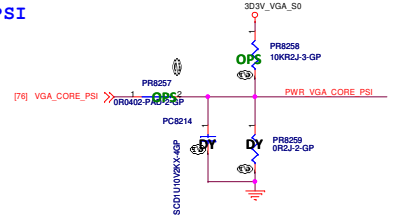
SSID = PWR.Plane.Regulator_vga_core

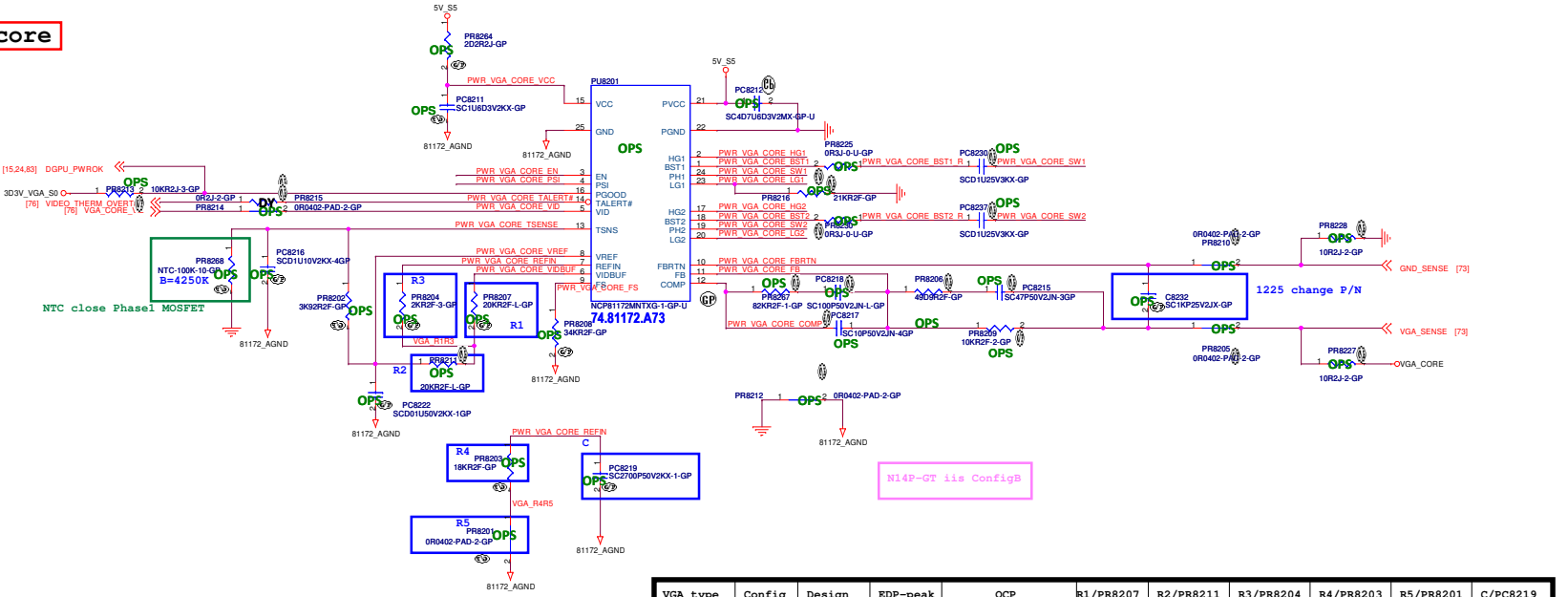
EN



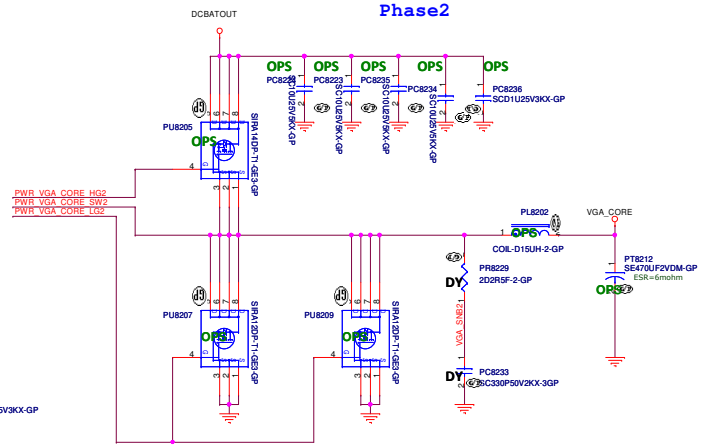
0307 DY PR8263, POP PR8265
0521 change resistor value from 12K ohm to 10K

PSI

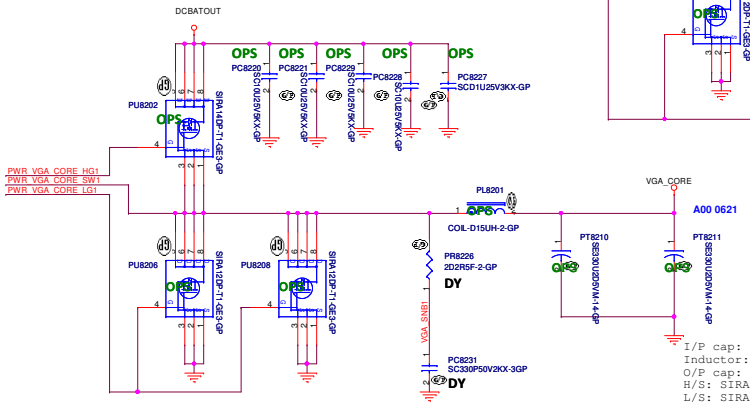




Phase2



Phase1



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.22UH M PCMC063T-R22MN/ 2.8mohm/ Isat =40A rms /68.R2210.10V
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

VGA type	Config	Design Current	EDP-peak	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

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Title: NCP81172_VGA_CORE
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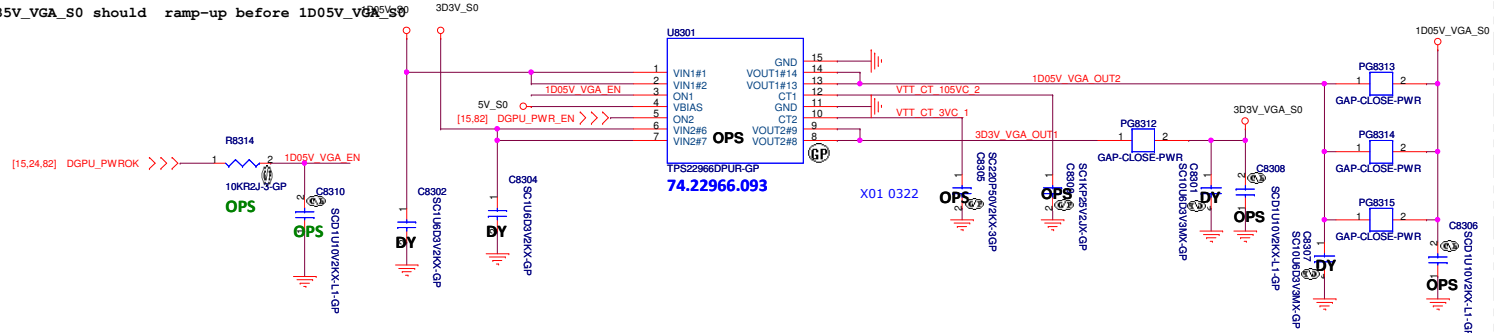
SSID = PWR.Plane.Regulator_3p3v_vga, 1p35v_vga, 1p05v_vga

3D3V_VGA_S0

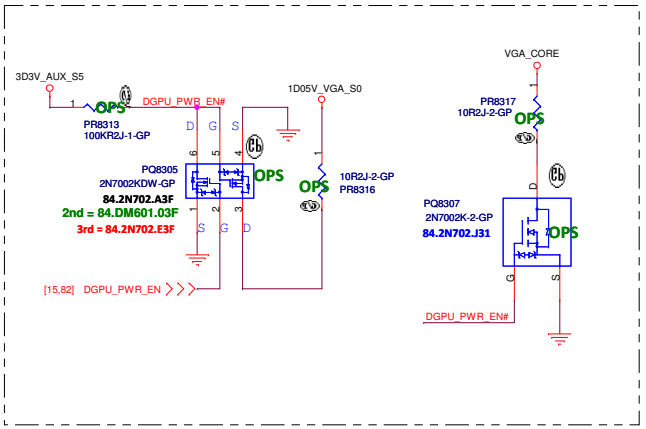
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

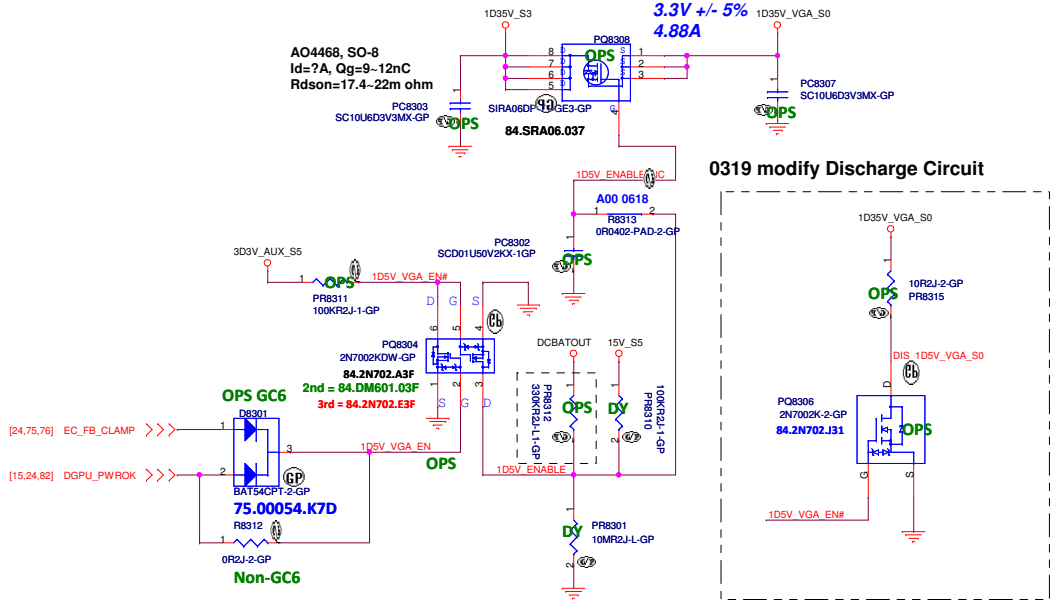
3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



0307 Add Discharge Circuit



1D35V_VGA_S0



0319 modify Discharge Circuit

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Title: DISCRETE VGA POWER

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Custom	Hadley 15"	X02

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Title: *Reserved*

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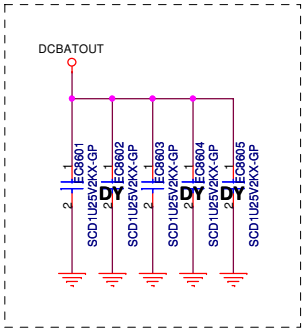
SSID = User.Interface

SO1 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO2 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO3 OPS — STF217R128H83-2-GP — 34.4Y702.301

S1 — SPRING-52-GP — 34.4T025.001
S2 — SPRING-52-GP — 34.4T025.001
S3 — SPRING-52-GP — 34.4T025.001
S4 — SPRING-52-GP — 34.4T025.001

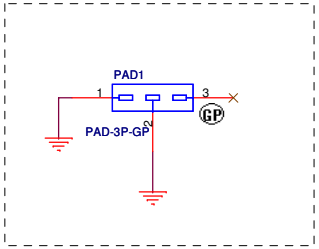
H2 — HOLET256B315R111-GP — ZZ.00PAD.M01
H3 — HT85BE85R29-U-5-GP — ZZ.00PAD.D41
H4 — HOLET256B315R111-GP — ZZ.00PAD.M01

0116 Add RF CAP

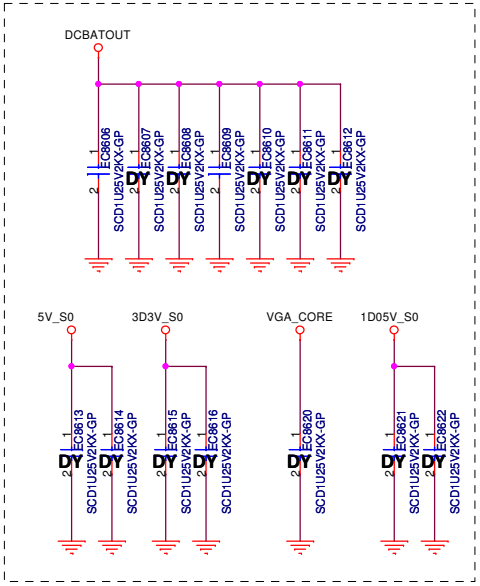


C1 HOLE197R166-1-GP — ZZ.00PAD.V71
C2 HOLE197R166-1-GP — ZZ.00PAD.V71
C3 HOLE197R166-1-GP — ZZ.00PAD.V71

0528 Add NPTH hole



0117 Add EMC CAP



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Title: UNUSED PARTS/EMI Capacitors
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<Core Design>

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Title
Reserved

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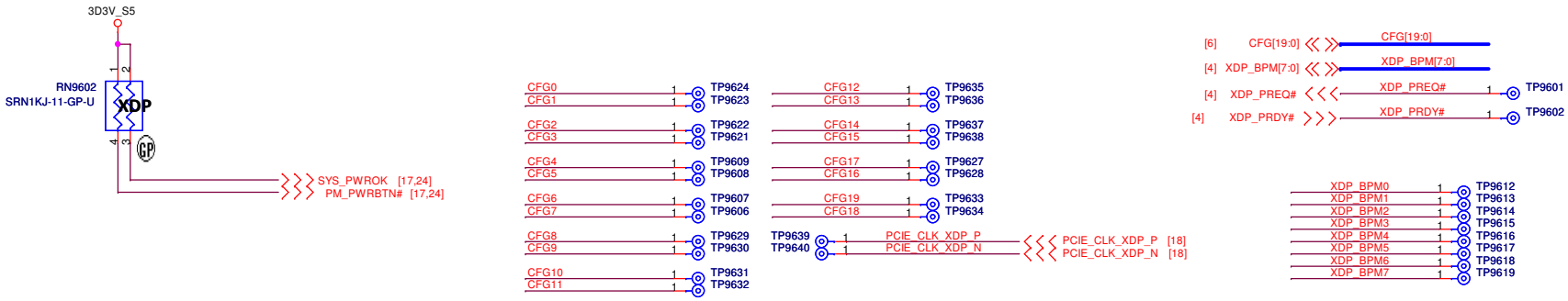
SSID = XDP

CPU XDP



<Core Design>

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Title: CPU XDP		
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PCH Strapping

Name	Schematics Notes

Processor Strapping

Pin Name	Strap Description	(Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION

SMBus ADDRESSES

I²C / SMBus Addresses	CHIEF RIVER ORB	
Device	Address	Bus
EC SMBus 1		
Battery 0	0x16	BAT_SCL/BAT_SDA
CHARGER	0x12	BAT_SCL/BAT_SDA
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA
EC SMBus 2		
Battery 1	0x16	SML1_CLK/SML1_DATA
PCH	0x96 & 0x94	SML1_CLK/SML1_DATA
Discrete VGA Thermal	0x9C or 0x9E	SML1_CLK/SML1_DATA
PS8321 HDMI level shifter	0x96 & 0X97	SML1_CLK/SML1_DATA
NCT7718W	0x98 or 0x99	SML1_CLK/SML1_DATA
EC SMBus 3		SMB2_CLK/SMB2_DATA
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA
PCH SMBus		
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK
G-Sensor		PCH_SMBDATA/PCH_SMBCLK
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	

USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

<Core Design>

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Title: Table of Content

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Title
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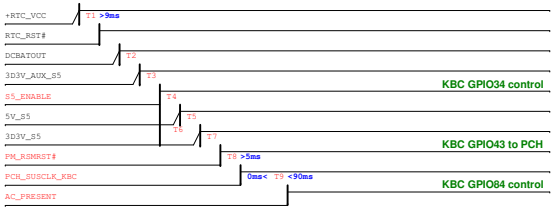
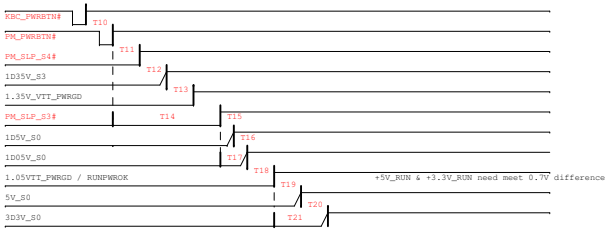
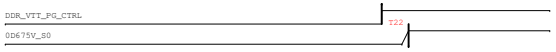
Intel-Power Up Sequence

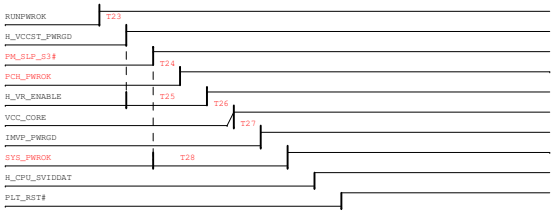
(AC mode)

Red printings:KBC GPIO involved



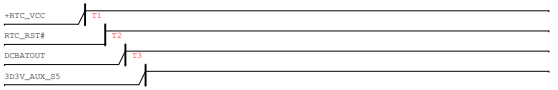


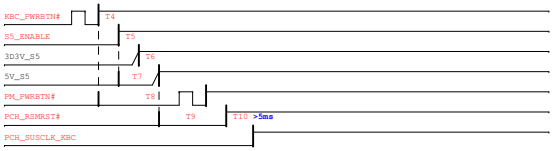


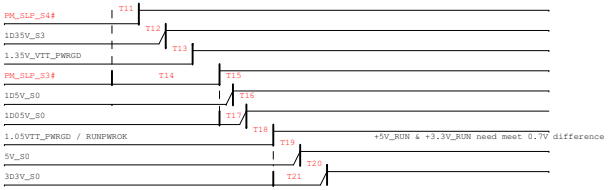


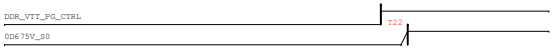
(DC mode)

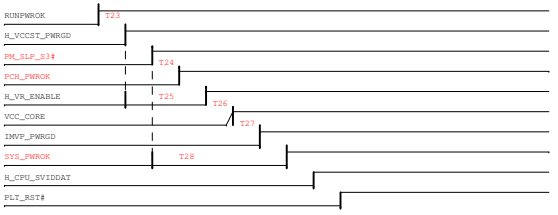
Red printings:KBC GPIO involved











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Title: Power Sequence

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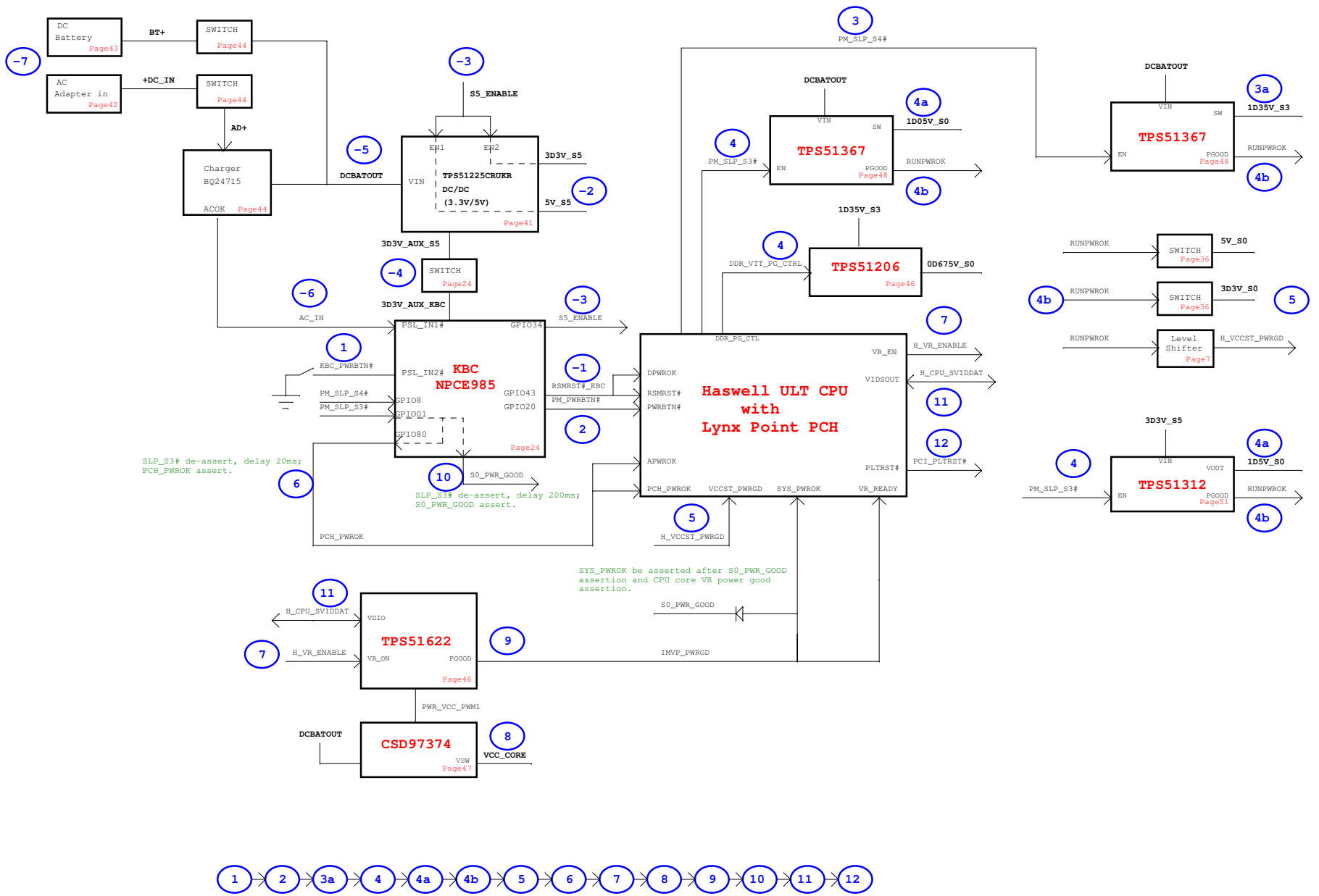
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 9 → 10 → 11 → 12

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Title: Power Block Diagram

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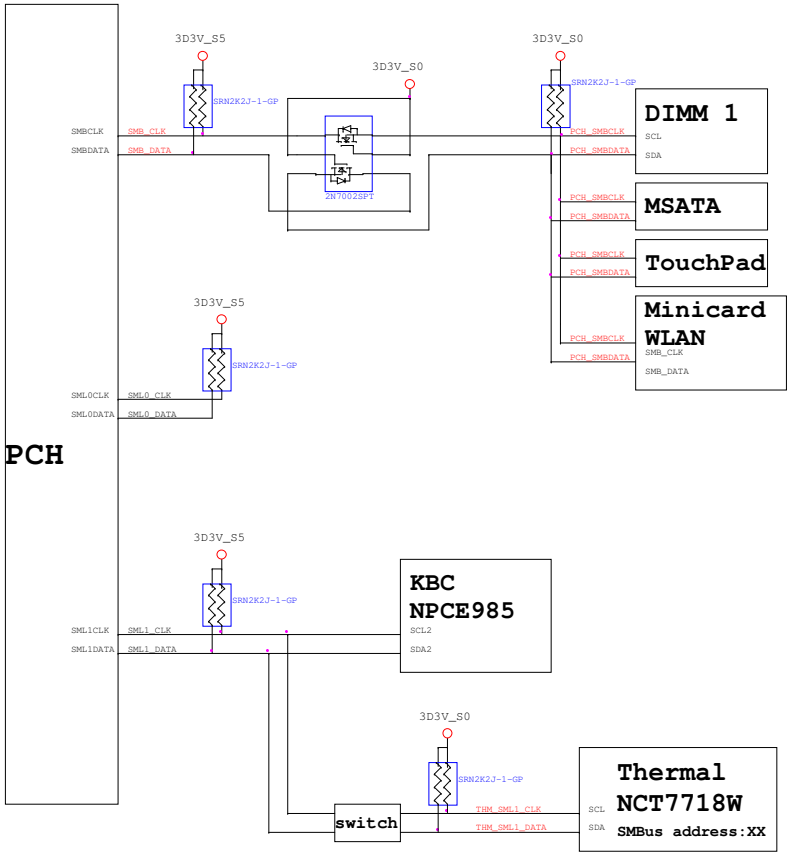
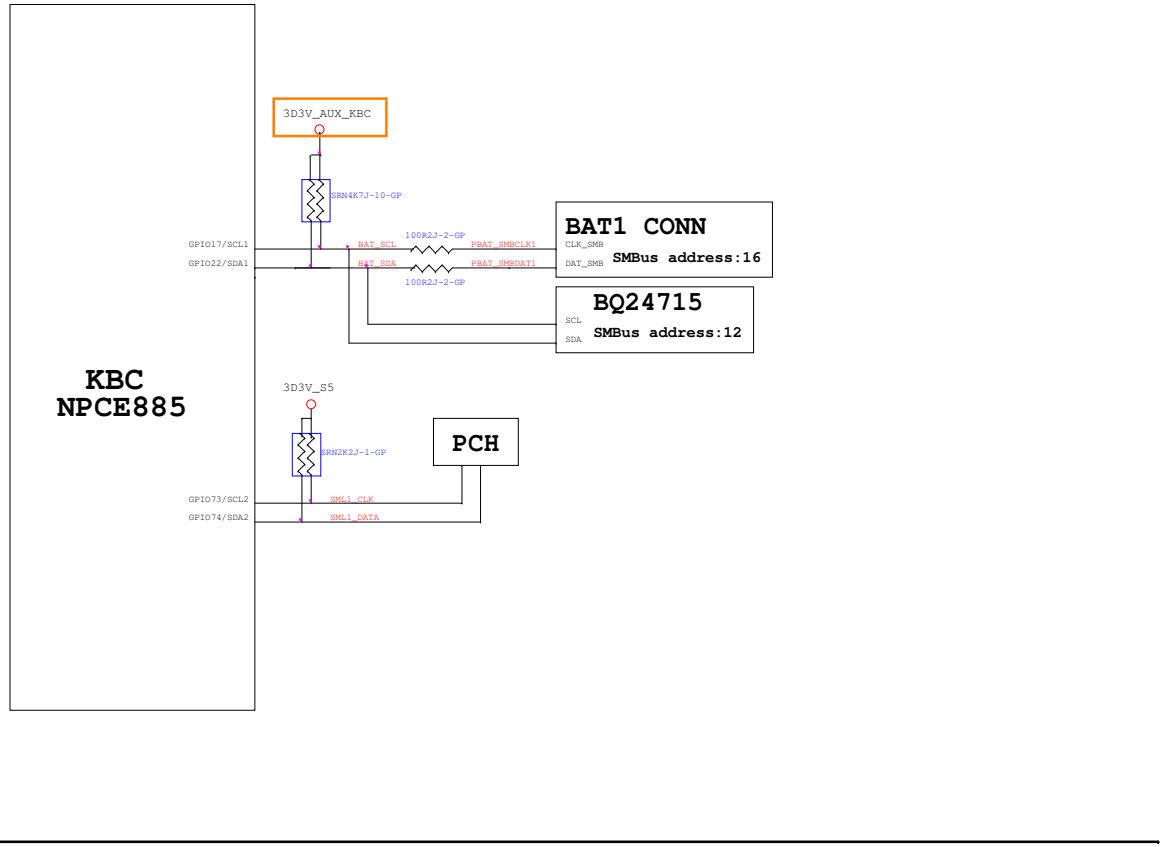
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size | Document Number: Hadley 15" | Rev: X02

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