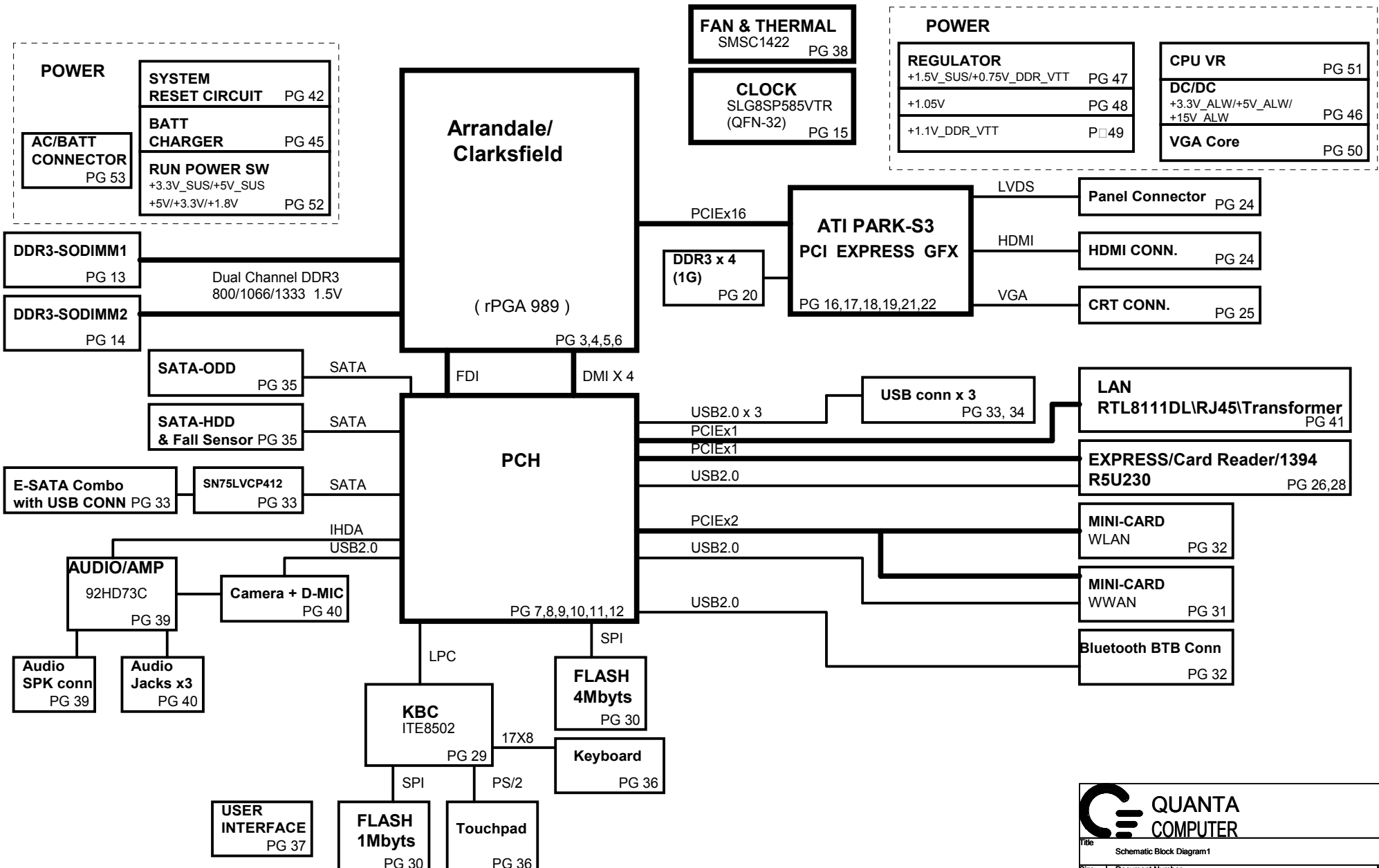
FM9 HANKS Intel PARK Discrete GFX

VER : 1A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Ω ±1% resistor, pulled-down to GND on the board.

U34A

DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]
DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]
DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]
DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

DMI

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]
FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]
FDI_FSYNC[0] FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0] FDI_LSYNC[1]

FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS
PEG_RX#[0..15] PEG_RX[0..15]
PEG_TX#[0..15] PEG_TX[0..15]

PCIE_MRX_GTX_N[0..15] PCIE_MRX_GTX_P[0..15]
PCIE_MTX_GRX_C_N[0..15] PCIE_MTX_GRX_C_P[0..15]

Clarksfield/Auburndale

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor.

R1029 1K 0214 R71 1K

PCIE_MRX_GTX_N[0..15] 16
PCIE_MRX_GTX_P[0..15] 16

PCIE_MTX_GRX_C_N0 16 C554 0.1U PCIE_MTX_GRX_N0
PCIE_MTX_GRX_C_N1 16 C557 0.1U PCIE_MTX_GRX_N1
PCIE_MTX_GRX_C_N2 16 C559 0.1U PCIE_MTX_GRX_N2
PCIE_MTX_GRX_C_N3 16 C562 0.1U PCIE_MTX_GRX_N3
PCIE_MTX_GRX_C_N4 16 C566 0.1U PCIE_MTX_GRX_N4
PCIE_MTX_GRX_C_N5 16 C575 0.1U PCIE_MTX_GRX_N5
PCIE_MTX_GRX_C_N6 16 C579 0.1U PCIE_MTX_GRX_N6
PCIE_MTX_GRX_C_N7 16 C584 0.1U PCIE_MTX_GRX_N7
PCIE_MTX_GRX_C_N8 16 C587 0.1U PCIE_MTX_GRX_N8
PCIE_MTX_GRX_C_N9 16 C595 0.1U PCIE_MTX_GRX_N9
PCIE_MTX_GRX_C_N10 16 C597 0.1U PCIE_MTX_GRX_N10
PCIE_MTX_GRX_C_N11 16 C601 0.1U PCIE_MTX_GRX_N11
PCIE_MTX_GRX_C_N12 16 C605 0.1U PCIE_MTX_GRX_N12
PCIE_MTX_GRX_C_N13 16 C612 0.1U PCIE_MTX_GRX_N13
PCIE_MTX_GRX_C_N14 16 C614 0.1U PCIE_MTX_GRX_N14
PCIE_MTX_GRX_C_N15 16 C618 0.1U PCIE_MTX_GRX_N15

PCIE_MTX_GRX_N[0..15] 16

PCIE_MTX_GRX_C_P0 16 C553 0.1U PCIE_MTX_GRX_P0
PCIE_MTX_GRX_C_P1 16 C555 0.1U PCIE_MTX_GRX_P1
PCIE_MTX_GRX_C_P2 16 C558 0.1U PCIE_MTX_GRX_P2
PCIE_MTX_GRX_C_P3 16 C560 0.1U PCIE_MTX_GRX_P3
PCIE_MTX_GRX_C_P4 16 C563 0.1U PCIE_MTX_GRX_P4
PCIE_MTX_GRX_C_P5 16 C568 0.1U PCIE_MTX_GRX_P5
PCIE_MTX_GRX_C_P6 16 C576 0.1U PCIE_MTX_GRX_P6
PCIE_MTX_GRX_C_P7 16 C580 0.1U PCIE_MTX_GRX_P7
PCIE_MTX_GRX_C_P8 16 C585 0.1U PCIE_MTX_GRX_P8
PCIE_MTX_GRX_C_P9 16 C588 0.1U PCIE_MTX_GRX_P9
PCIE_MTX_GRX_C_P10 16 C596 0.1U PCIE_MTX_GRX_P10
PCIE_MTX_GRX_C_P11 16 C599 0.1U PCIE_MTX_GRX_P11
PCIE_MTX_GRX_C_P12 16 C602 0.1U PCIE_MTX_GRX_P12
PCIE_MTX_GRX_C_P13 16 C606 0.1U PCIE_MTX_GRX_P13
PCIE_MTX_GRX_C_P14 16 C613 0.1U PCIE_MTX_GRX_P14
PCIE_MTX_GRX_C_P15 16 C616 0.1U PCIE_MTX_GRX_P15

PCIE_MTX_GRX_P[0..15] 16

U34B

H_COMP3 AT23 COMP3
H_COMP2 AT24 COMP2
H_COMP1 G16 COMP1
H_COMP0 AT26 COMP0

MISC

29 H_CPUDET# R188 *0_short TP_SKT0CC# AH24 SKTOCC#

H_CATERR# AK14 CATERR#

10 H_PECI R131 *0_short H_PECI_ISO AT15 PECI

H_PROCHOT#_D AN26 PROCHOT#

10 H_THERM R137 *0_short AK15 THERMTRIP#

THERMAL

60 H_CPURST# AP26 RESET_OBS#
7 PM_SYNC AL15 PM_SYNC
10,60 H_PWRGOOD AN14 VCCPWRGOOD_1
AN27 VCCPWRGOOD_0
7 PM_DRAM_PWRGD PM_DRAM_PWRGD AK13 SM_DRAMPWROK
42 H_VTTPWRGD AM15 VTTPWRGOOD
60 H_PWRGD_XDP AM26 TAPPWRGOOD
9,16,26,28,29,31,32,41 PLTRST# R164 1.5K/F AL14 RSTIN#

PWR MANAGEMENT

R163 750/F 0214

Clarksfield/Auburndale

BCLK A16 BCLK
BCLK# B16 BCLK#
BCLK_ITP AR30 BCLK_ITP
BCLK_ITP# AT30 BCLK_ITP#
PEG_CLK E16 PEG_CLK
PEG_CLK# D16 PEG_CLK#
DPLL_REF_SSCLK A18 DPLL_REF_SSCLK
DPLL_REF_SSCLK# A17 DPLL_REF_SSCLK#

CLOCKS

CLK_CPU_BCLK 10
CLK_CPU_BCLK# 10
BCLK_ITP 60
BCLK_ITP# 60
CLK_PCIE_3GPLL 9
CLK_PCIE_3GPLL# 9

DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Auburndale directly if motherboard only supports discrete graphics.

SM_DRAMRST# F6 DDR3_DRAMRST# 13,14
SM_RCOMP[0] AL1 SM_RCOMP_0
SM_RCOMP[1] AM1 SM_RCOMP_1
SM_RCOMP[2] AN1 SM_RCOMP_2

DDR3 MISC

PM_EXT_TS#[0] AN15
PM_EXT_TS#[1] AP15
R135 2 10K 1 +1.1V_VTT
R134 2 10K 1
R136 *0_short
R133 *0_short
PM_EXTTS#0 13
PM_EXTTS#1 14

PRDY# AT28 XDP_PRDY# 60
PREQ# AP27 XDP_PREQ# XDP_PREQ# 60
TCK AN28 XDP_TCLK XDP_TCLK 60
TMS AP28 XDP_TMS XDP_TMS 60
TRST# AT27 XDP_TRST# XDP_TRST# 60
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
T19 T50 T51
R132 *12.4K/F_NC

CRB(v0.71) P.11

JTAG & BPM

DBR# AN25 H_DBR#_R R147 *0_short XDP_DBRESET# 7,60

BPM#[0] AJ22 XDP_OBS0_R R128 *0_short XDP_OBS0
BPM#[1] AK22 XDP_OBS1_R R146 *0_short XDP_OBS1
BPM#[2] AK24 XDP_OBS2_R R126 *0_short XDP_OBS2
BPM#[3] AJ24 XDP_OBS3_R R148 *0_short XDP_OBS3
BPM#[4] AJ25 XDP_OBS4_R R129 *0_short XDP_OBS4
BPM#[5] AH22 XDP_OBS5_R R149 *0_short XDP_OBS5
BPM#[6] AK23 XDP_OBS6_R R127 *0_short XDP_OBS6
BPM#[7] AH23 XDP_OBS7_R R130 *0_short XDP_OBS7
XDP_OBS[0:7] 60

DBR#:
SC(V1.0) P22:Connected to the DBR# pin of the Processor.50-Ω to 5-kΩ pull-up to 3.3VS
CRB(V1.0) P11,P71:CRB uses a 1-kΩ pull-up to 3.3VS.
On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.

DBR#:(Intell feedback)
Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (S0) main power.

SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

VTTPWRGOOD
SC(V1.0)P18:
VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.

RSTIN#:
DG(V1.11)(Doc.# 414014) P10 : Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

+1.5V_SUS R171 1.1K/F PM_DRAM_PWRGD R97 3K/F

+3.3V_RUN R144 10M Q29 2N7002W-7-F H_THERM Q28 MMST3904-7-F C313 0.1U 16 PM_THRMTRIP# 46

T18 +1.1V_VTT
XDP_TMS R158 *51_NC
XDP_TDI_R R493 *51_NC
XDP_PREQ# R157 *51_NC
XDP_TCLK R156 *51_NC
T17

CRB(V1.0) P11: is it necessery?

JTAG MAPPING

XDP_TDI_R R494 0 XDP_TDI 60
XDP_TDO_M R497 0_NC XDP_TDO 60
R496 0
XDP_TDI_M R495 0_NC
XDP_TDO_R R498 0
XDP_TRST# R499 51

Scan Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

DG(v1.0) table 27

TRST#
SC(V1.0)P22: should be routed as a single daisy chain to all loads and terminated at the end of the trace. 51 Ω ± 5% pull down resistor.
CRB()V1.0)P11

Processor Pullups

+1.1V_VTT R100 49.9/F R121 49.9/F R122 *68_NC
H_CATERR#
H_PROCHOT# D
H_CPURST#

SC(1.0V),P17:
H_PROCHOT#D
use: pull to 68 ohm
if it isn'tt used: pull to 50 ohm

SC(1.0V),P17:
H_CATERR#
49.9-Ω ±1% Pull-Up to the VTT rail (+V1.1S_VTT)

Processor Compensation Signals

H_COMP0 H_COMP1 H_COMP2 H_COMP3
R123 49.9/F R72 49.9/F R124 20/F R125 20/F

DG(V1.0),P17:
COMP[0,1] 49.9-Ω ±1% pull-down to GND
COMP[2,3] 20-Ω ±1% pull-down to GND

DDR3 Compensation Signals

SM_RCOMP_2 SM_RCOMP_1 SM_RCOMP_0
R95 130/F R89 24.9/F R94 100/F

Layout Note: Place these resistors near Processor

DG(V1.0),P83:
SM_RCOMP[0] 100-Ω ±1% pull-down to GND
SM_RCOMP[1] 24.9-Ω ±1% pull-down to GND
SM_RCOMP[2] 130-Ω ±1% pull-down to GND

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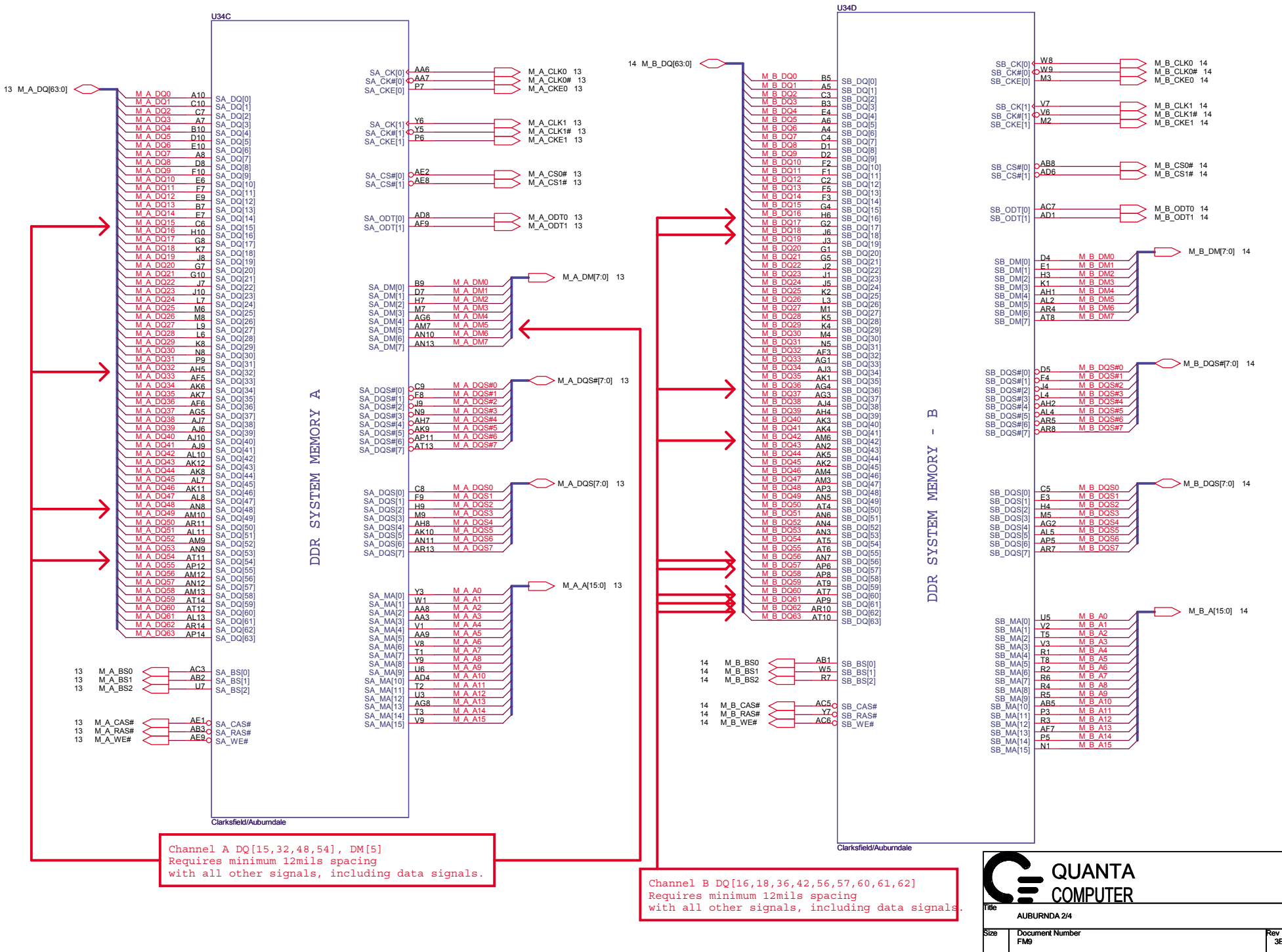
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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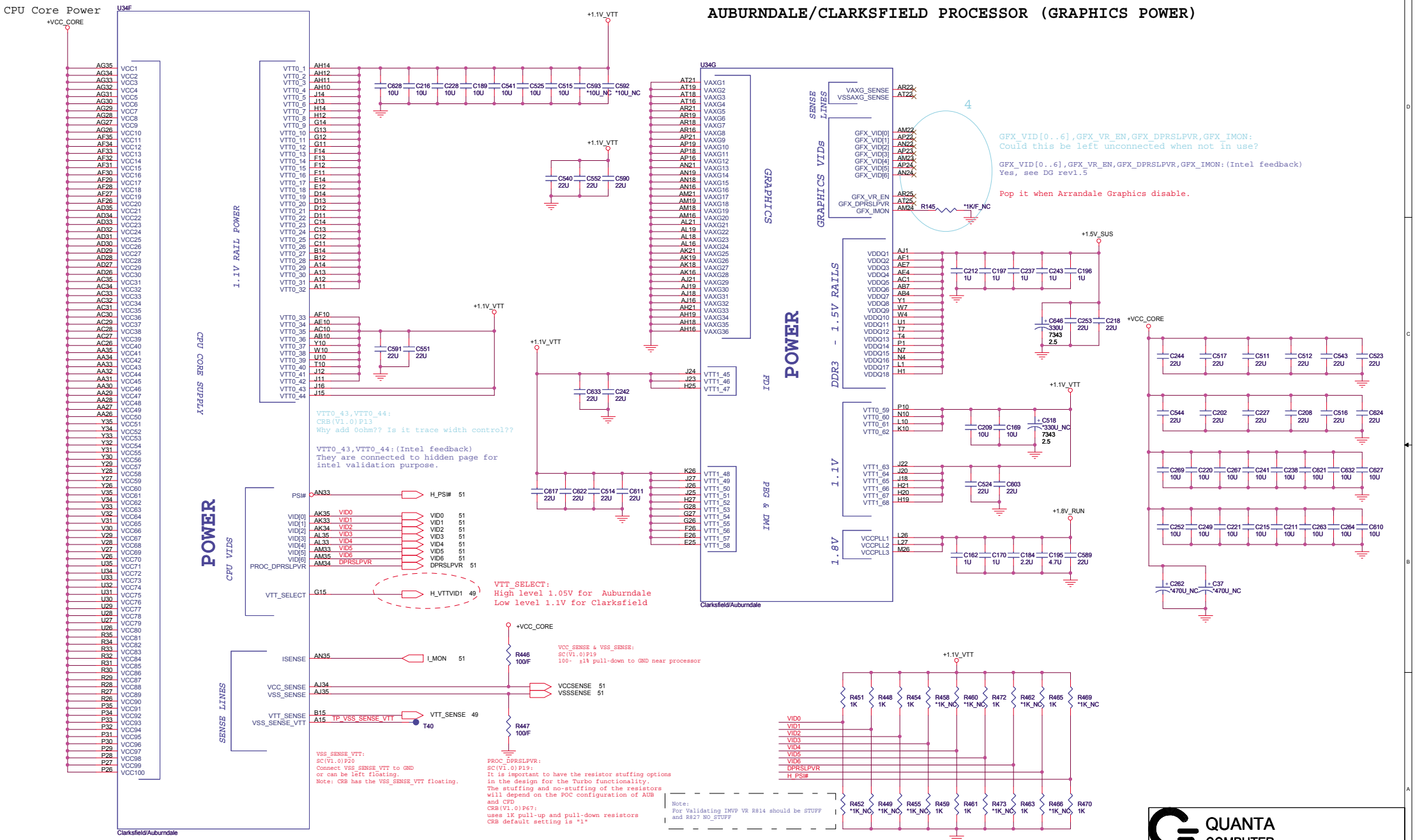
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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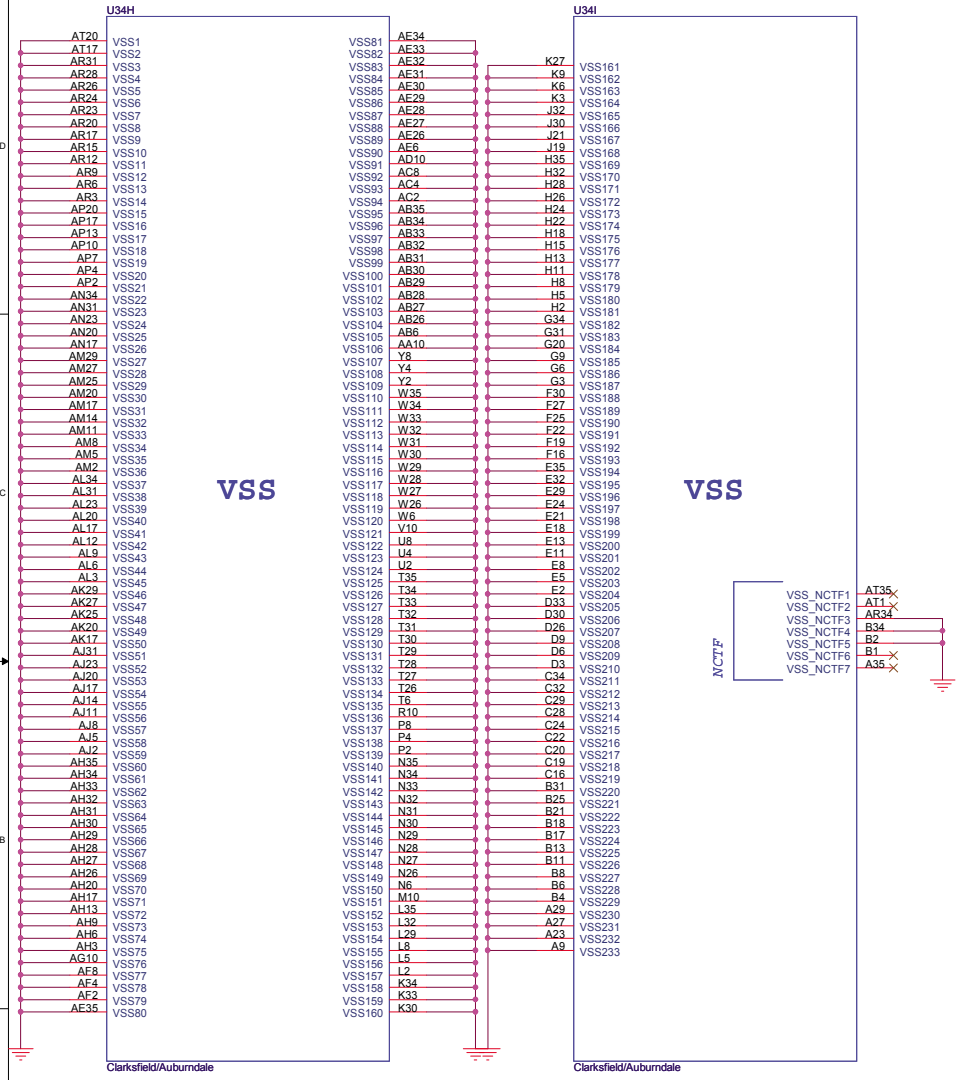
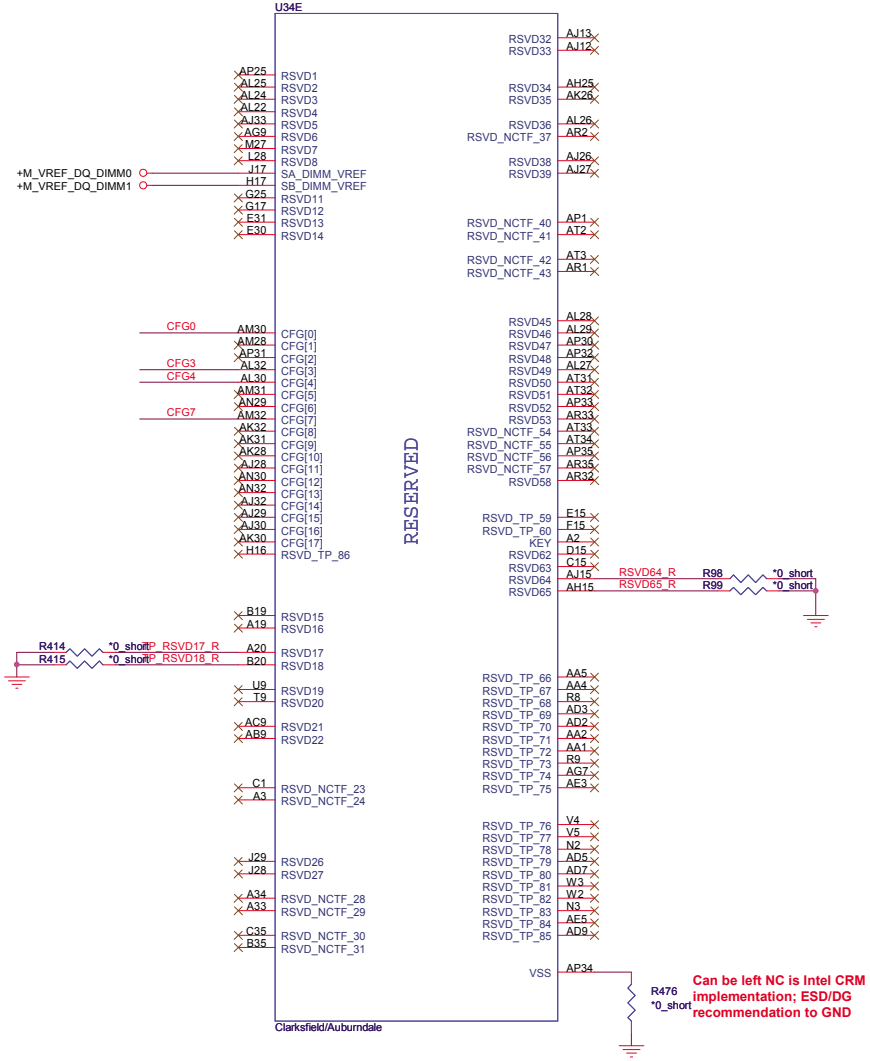
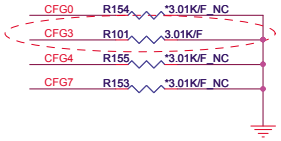
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

QUANTA COMPUTER

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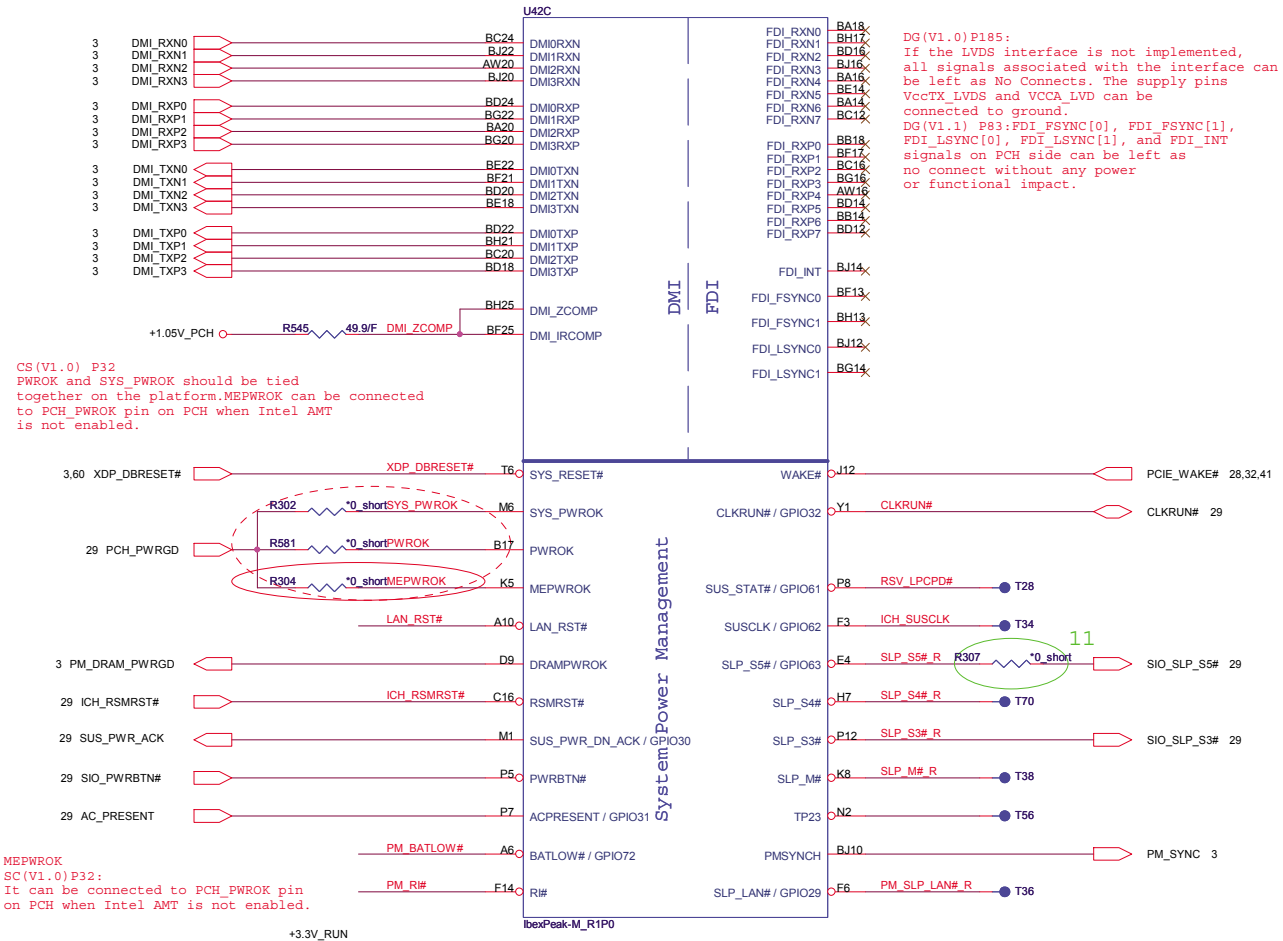
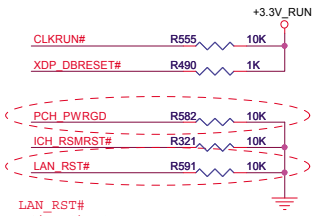
IBEX PEAK-M (DMI,FDI,GPIO)



DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83:FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

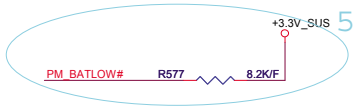
CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform.MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



LAN_RST#
DG(V1.0) P311
If integrated LAN is not used, recommend to connect LAN_RST# to GND via an 8.2-kΩ to 10-kΩ pull-down resistor.
EDS(V1.0)P64
must be grounded if Intel LAN is disabled.

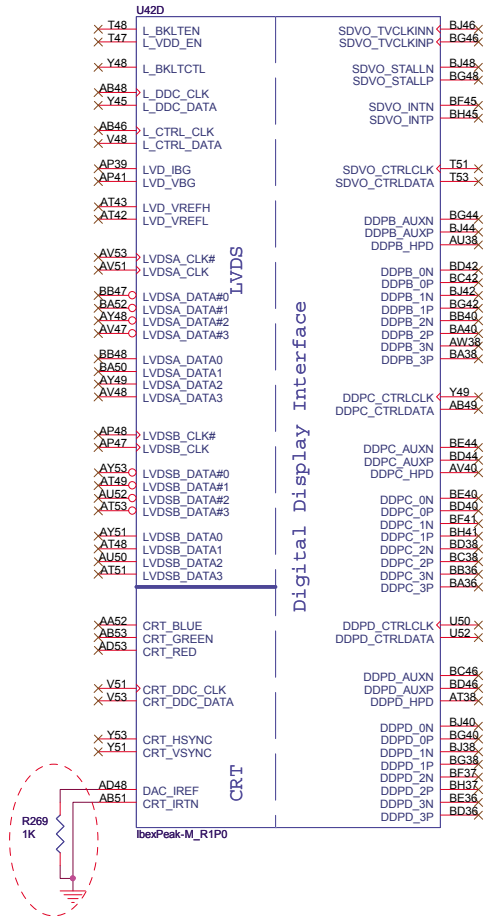
PWROK
SC(V1.0)P32:
8.2 kΩ to 10 kΩ pull-down resistor to GND.
PWROK and SYS_PWROK should be tied together on the platform.



PM_BATLOW#:
EDS(V1.0)P95: 15K~40K (+3.3V_SUS)
CRB(V1.0)P25: 8.2K (+3.3V_ALW)

PM_BATLOW#:(Intel feedback)
15K ~ 40K is a simulation result, the expected value should be 20K
internal pull high in PCH.
8.2K is external pull high.

IBEX PEAK-M (LVDS,DDI)



DG(V1.0)P189:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k ±0.5% pull-down resistor

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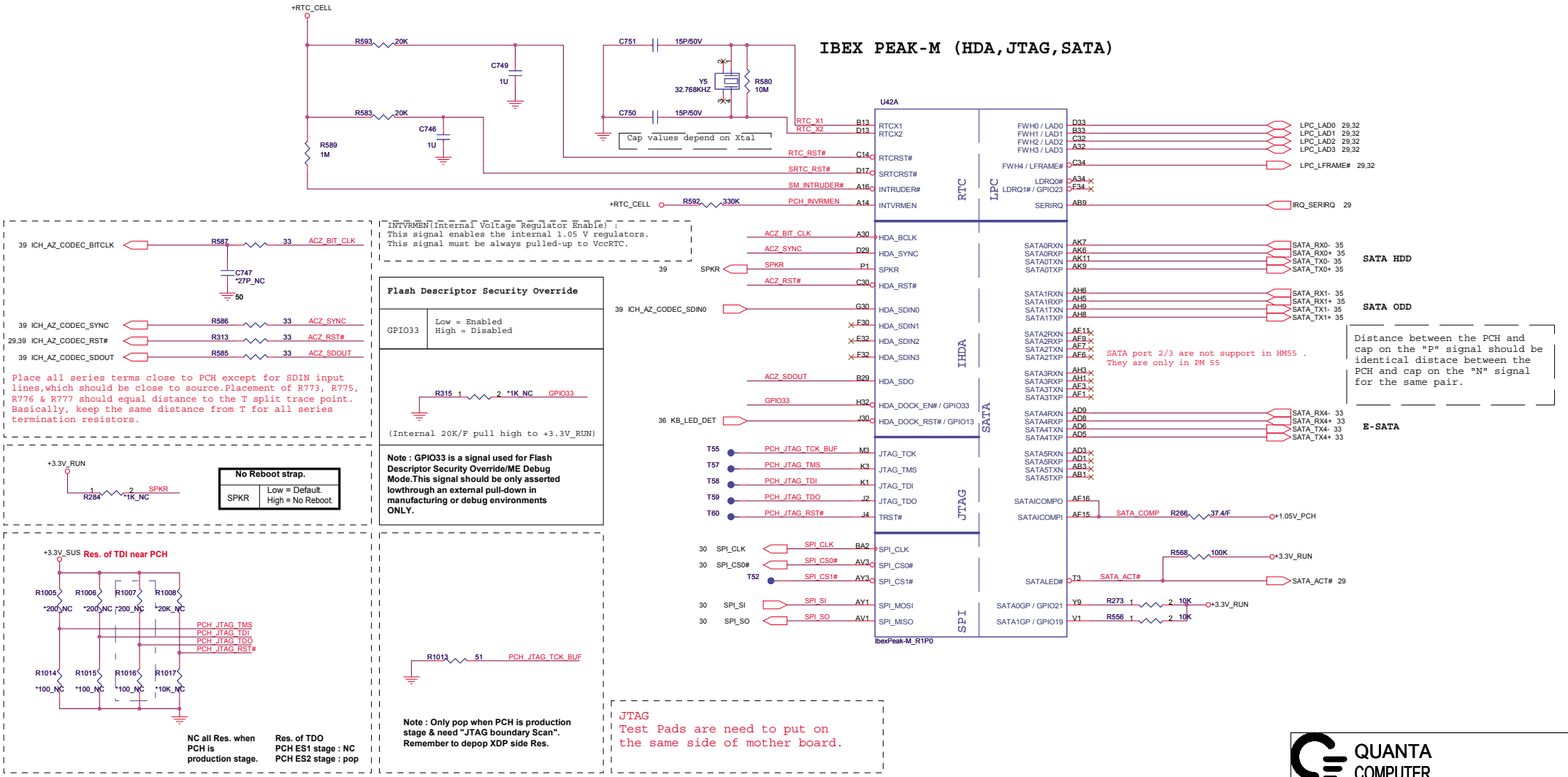
IBEX PEAK-M (HDA,JTAG,SATA)



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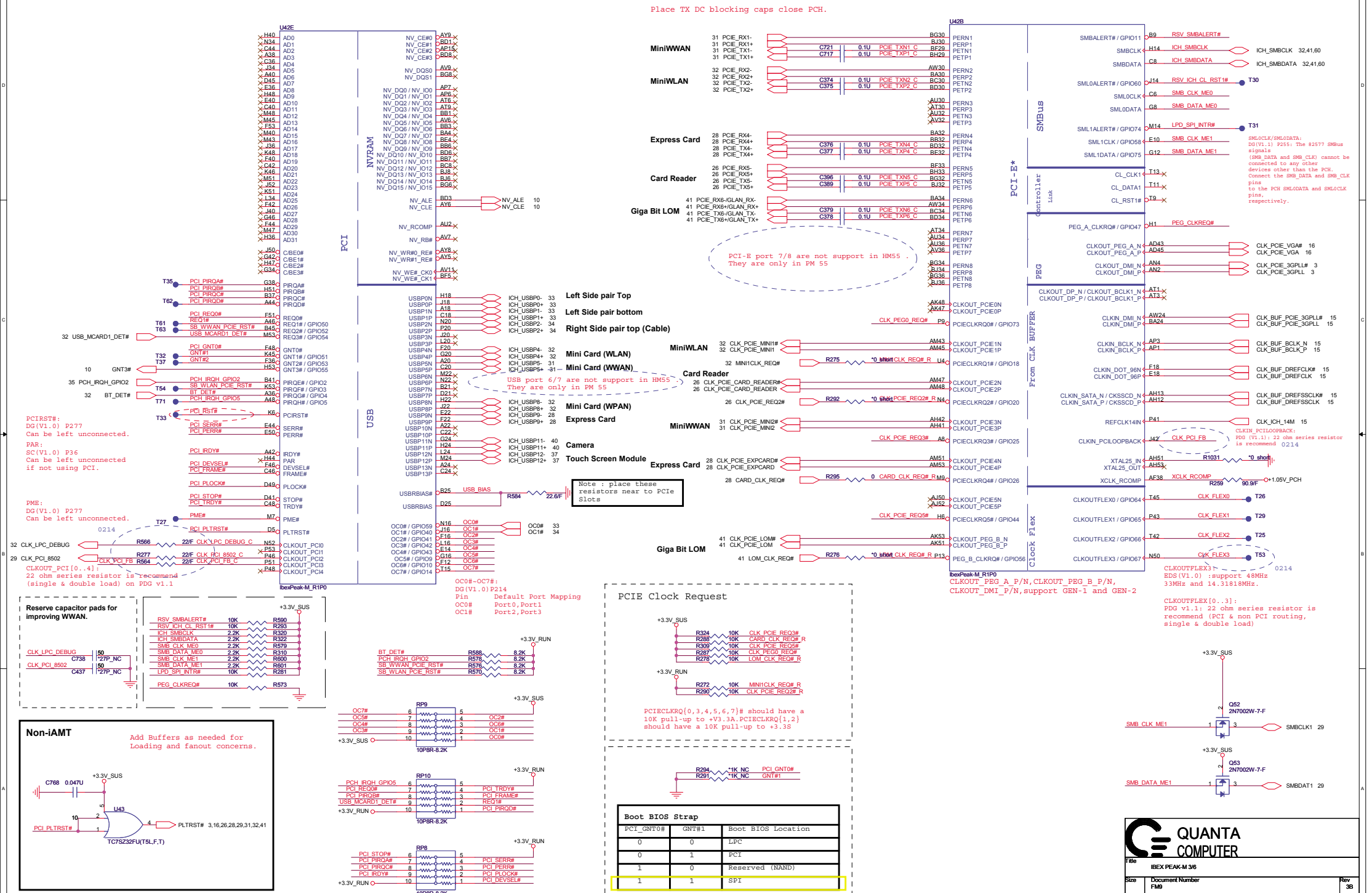
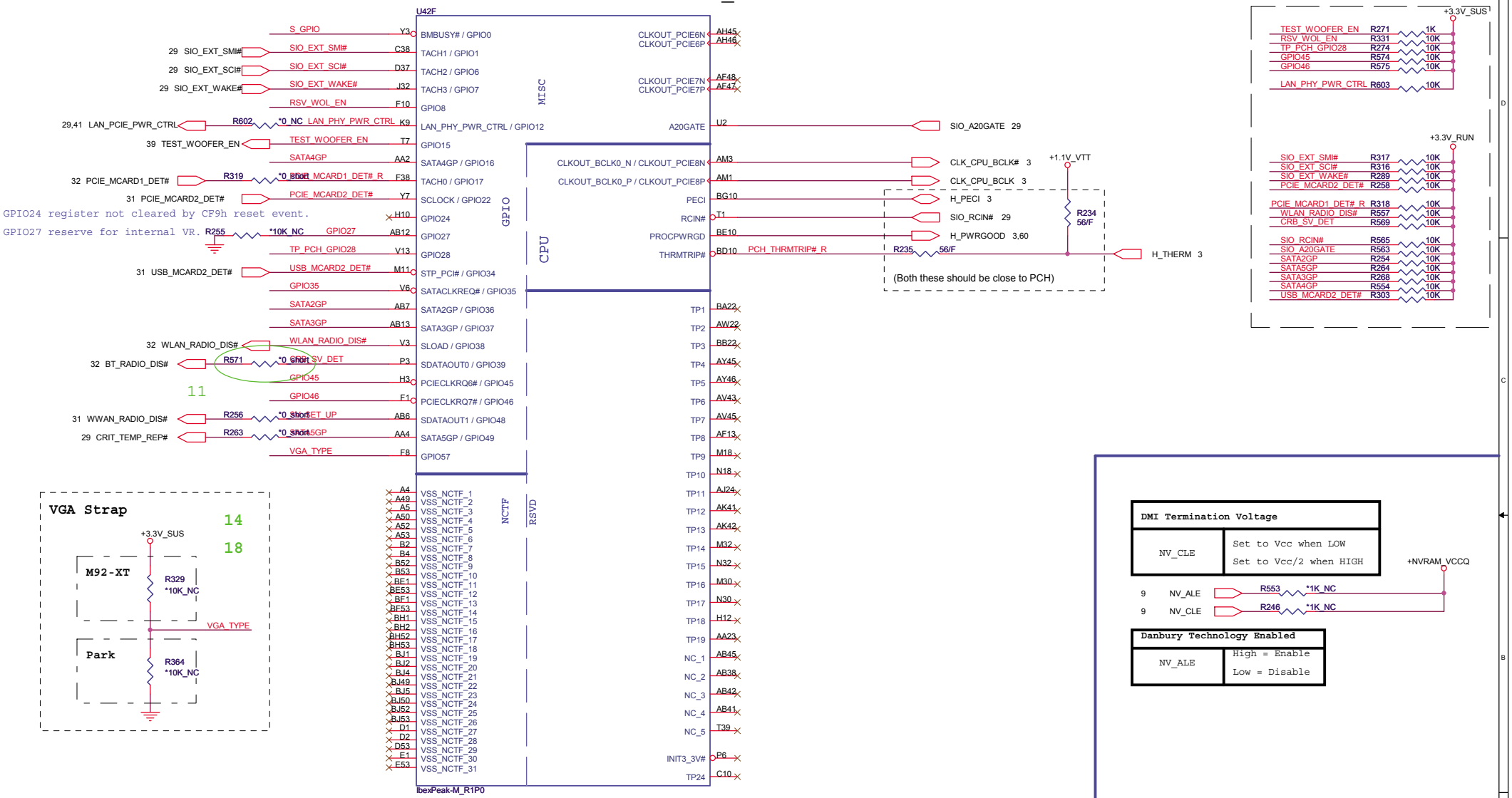
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

9 NV_ALE R553 *1K_NC

9 NV_CLE R246 *1K_NC

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

R267 10K GPIO35

R572 *1K_NC GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

R1009 *1K_NC RSV_WOL_EN

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high

+3.3V_RUN

S_GPIO R270 10K

SV_SET_UP R257 10K

SV_SET_UP	1-X High = Strong (Default)

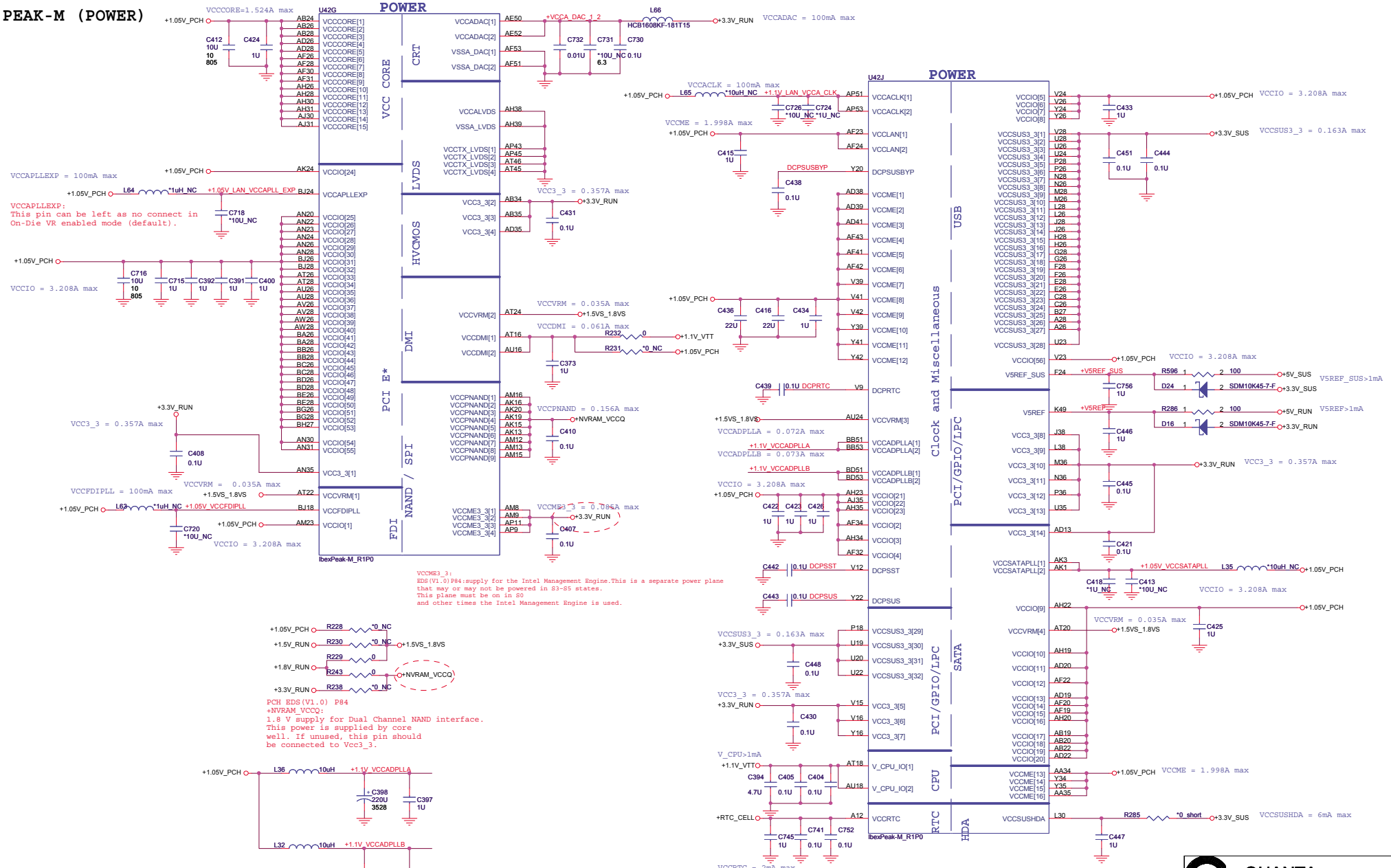
BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up
(8.2~ KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

QUANTA COMPUTER

Title: IBEX PEAK-M 4/6		
Size	Document Number: FM9	Rev: 3B
Date: Wednesday, October 07, 2009	Sheet 10 of 66	

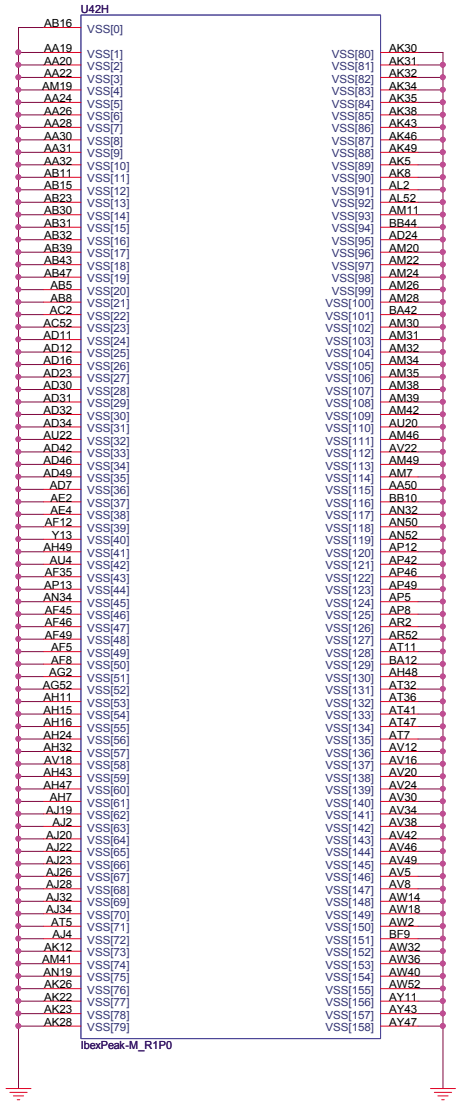
IBEX PEAK-M (POWER)

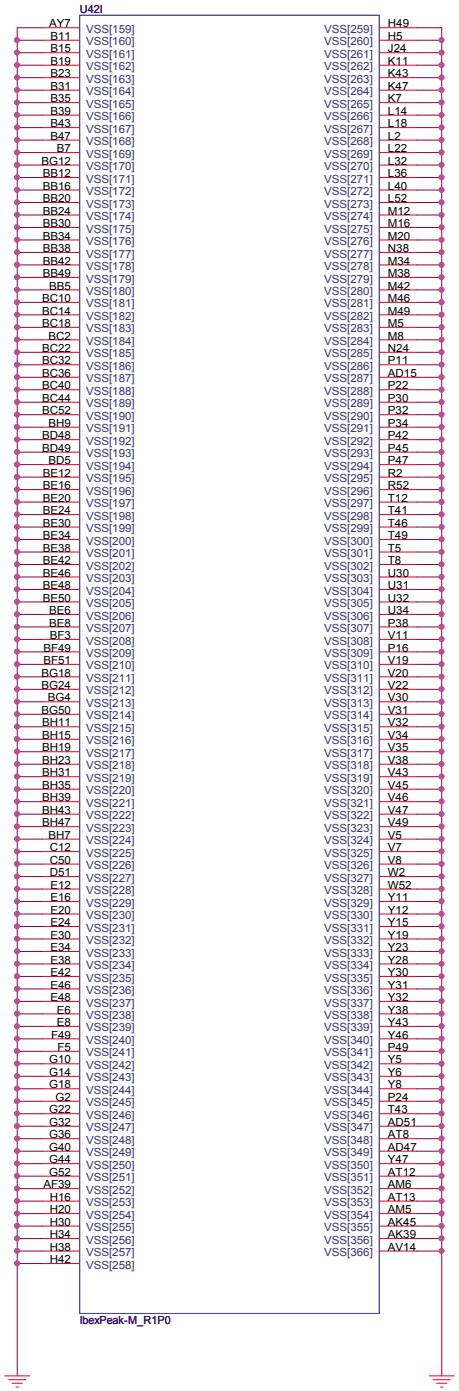


QUANTA COMPUTER

Title	IBEX PEAK-M 5/6	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 11 of 66	

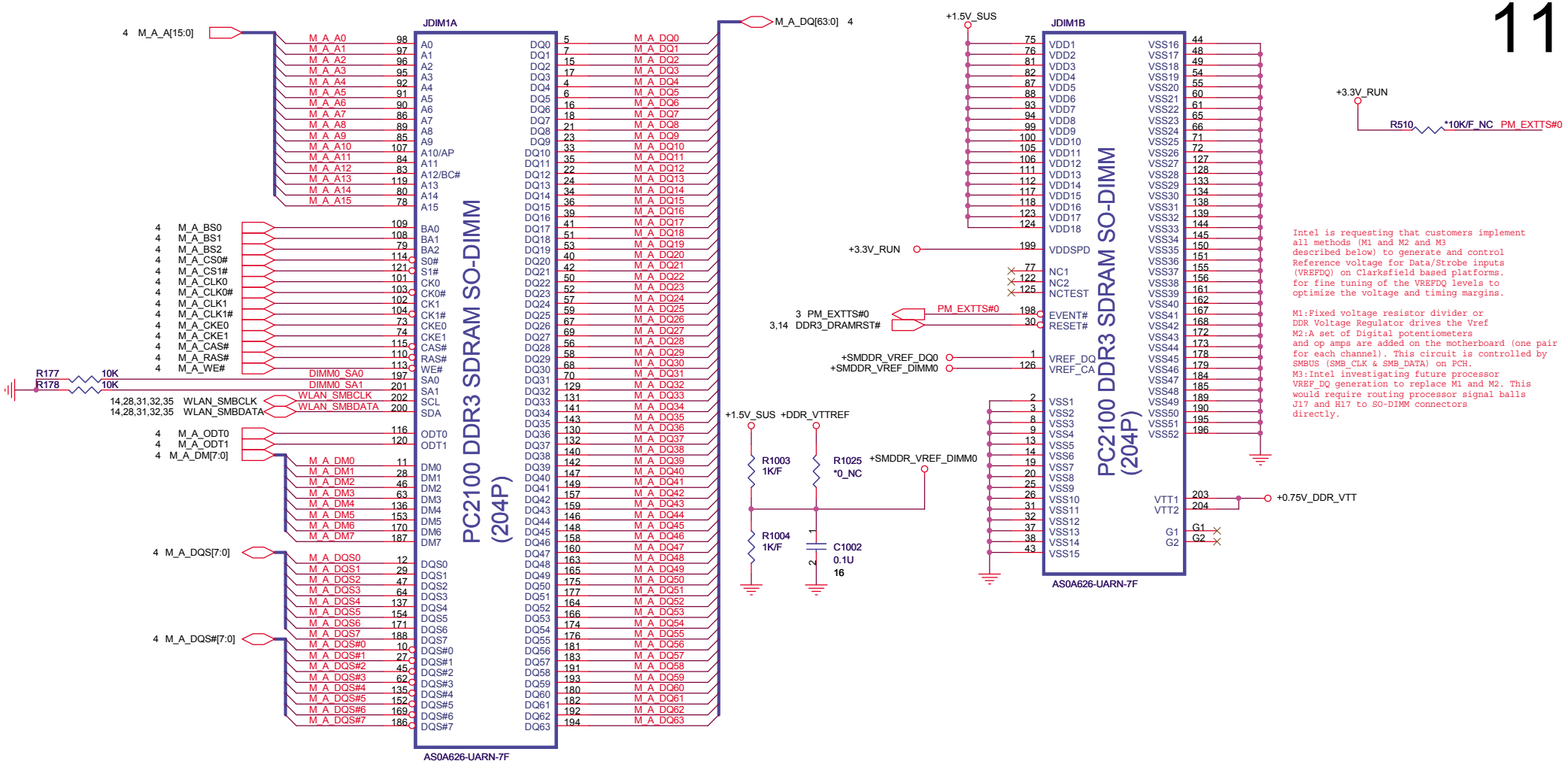
IBEX PEAK-M (GND)



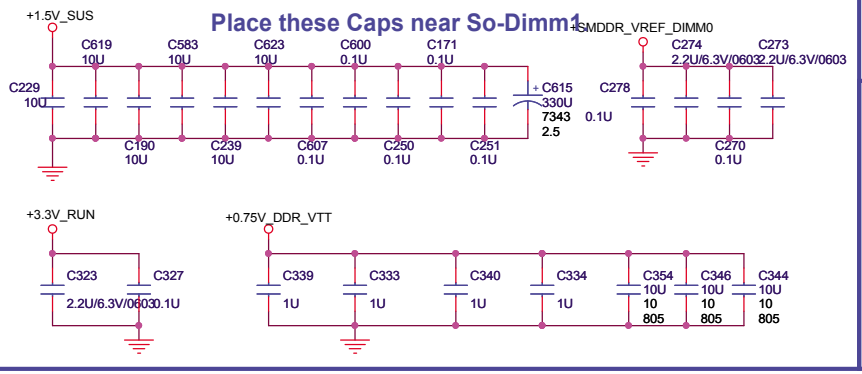


QUANTA COMPUTER

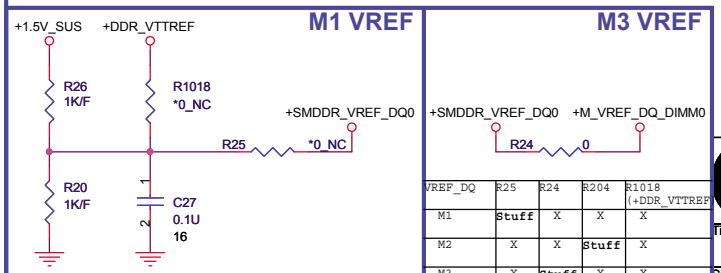
Title	IBEX PEAK-M 6/6	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 12 of 66	



Place these Caps near So-Dimm1



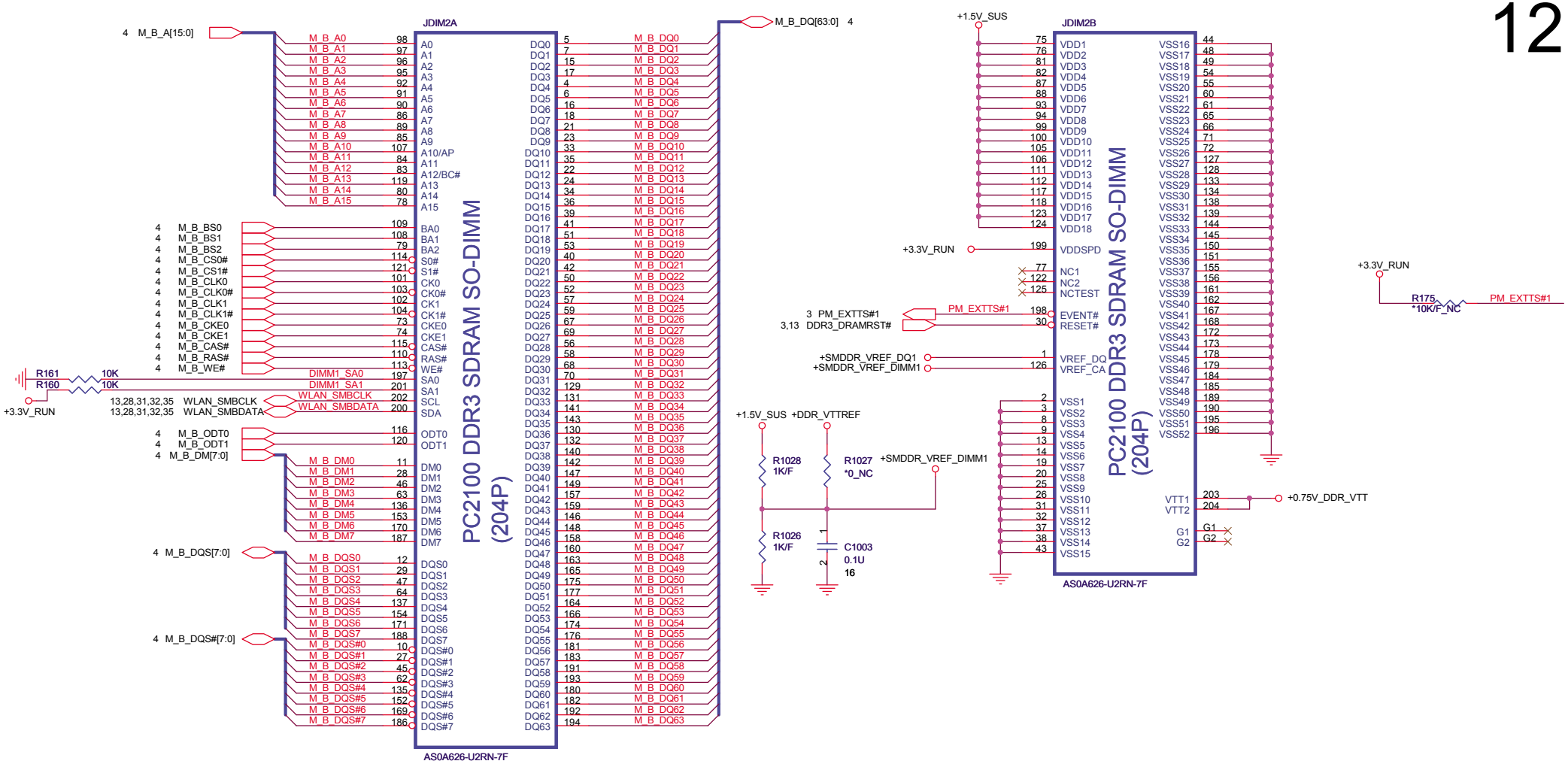
for ARD CPU pop M1, NC M3 component.
for CFD CPU pop M3, NC M1 component

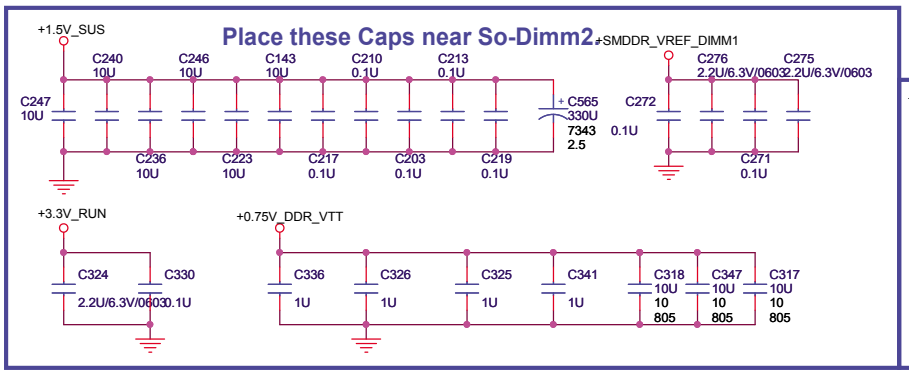


VREF_DQ	R25	R24	R204	R1018 (+DDR_VTTREF)
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

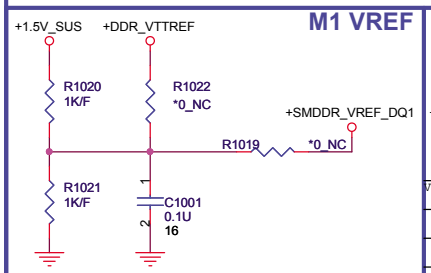
QUANTA COMPUTER

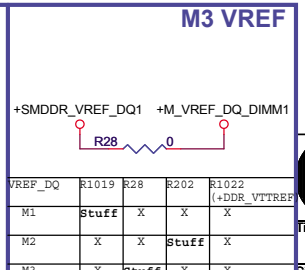
Title	DDR3 DIMM-0	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 13 of 66	





for ARD CPU pop M1, NC M3 component.
for CFD CPU pop M3, NC M1 component

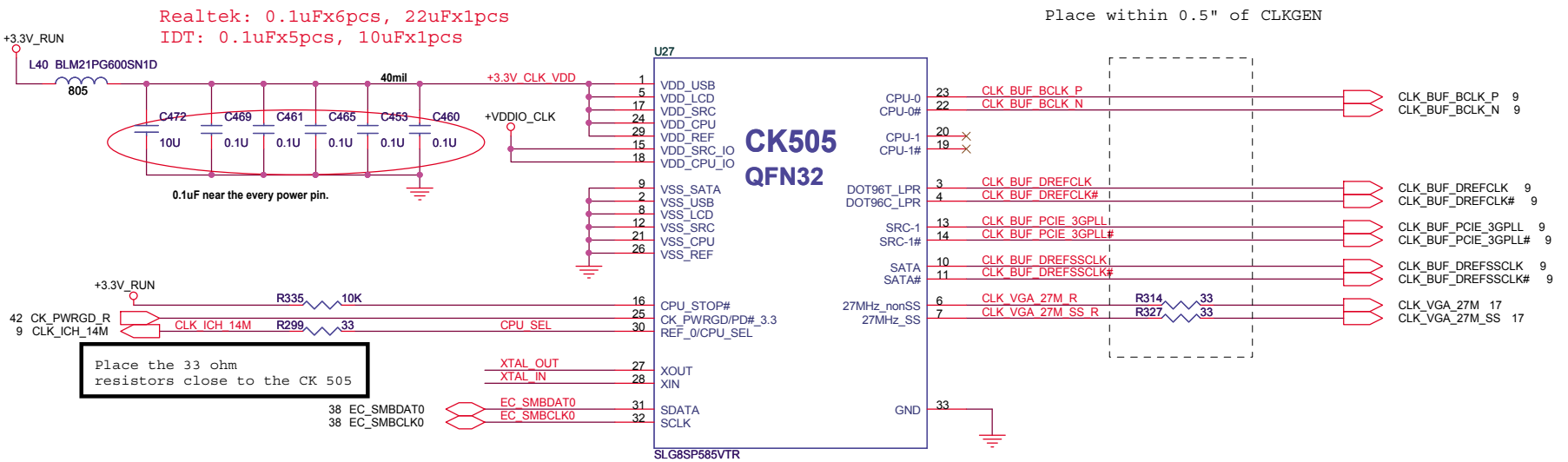




VREF_DQ	R1019	R28	R202	R1022 (+DDR_VTTREF)
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

QUANTA COMPUTER

Title	DDR3 DIMM-1	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 14 of 66	



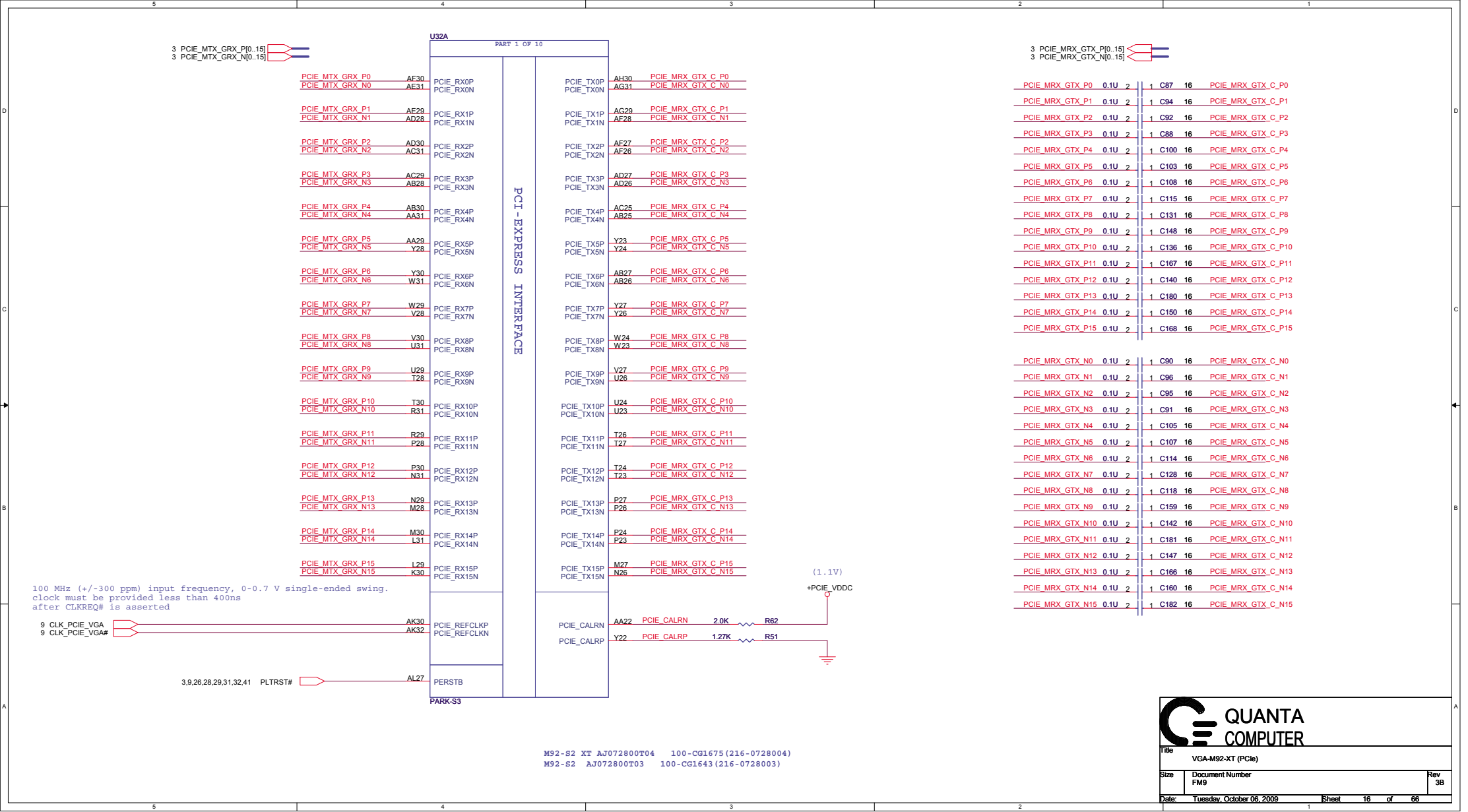
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

QUANTA COMPUTER

Title	Clock Generator	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 15 of 66	


U32A
PART 1 OF 10
PCI-EXPRESS INTERFACE
PARK-S3
3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]
PCIE_MTX_GRX_P0 AF30 PCIE_RX0P
PCIE_MTX_GRX_N0 AE31 PCIE_RX0N
PCIE_MTX_GRX_P1 AE29 PCIE_RX1P
PCIE_MTX_GRX_N1 AD28 PCIE_RX1N
PCIE_MTX_GRX_P2 AD30 PCIE_RX2P
PCIE_MTX_GRX_N2 AC31 PCIE_RX2N
PCIE_MTX_GRX_P3 AC29 PCIE_RX3P
PCIE_MTX_GRX_N3 AB28 PCIE_RX3N
PCIE_MTX_GRX_P4 AB30 PCIE_RX4P
PCIE_MTX_GRX_N4 AA31 PCIE_RX4N
PCIE_MTX_GRX_P5 AA29 PCIE_RX5P
PCIE_MTX_GRX_N5 Y28 PCIE_RX5N
PCIE_MTX_GRX_P6 Y30 PCIE_RX6P
PCIE_MTX_GRX_N6 W31 PCIE_RX6N
PCIE_MTX_GRX_P7 W29 PCIE_RX7P
PCIE_MTX_GRX_N7 V28 PCIE_RX7N
PCIE_MTX_GRX_P8 V30 PCIE_RX8P
PCIE_MTX_GRX_N8 U31 PCIE_RX8N
PCIE_MTX_GRX_P9 U29 PCIE_RX9P
PCIE_MTX_GRX_N9 T28 PCIE_RX9N
PCIE_MTX_GRX_P10 T30 PCIE_RX10P
PCIE_MTX_GRX_N10 R31 PCIE_RX10N
PCIE_MTX_GRX_P11 R29 PCIE_RX11P
PCIE_MTX_GRX_N11 P28 PCIE_RX11N
PCIE_MTX_GRX_P12 P30 PCIE_RX12P
PCIE_MTX_GRX_N12 N31 PCIE_RX12N
PCIE_MTX_GRX_P13 N29 PCIE_RX13P
PCIE_MTX_GRX_N13 M28 PCIE_RX13N
PCIE_MTX_GRX_P14 M30 PCIE_RX14P
PCIE_MTX_GRX_N14 L31 PCIE_RX14N
PCIE_MTX_GRX_P15 L29 PCIE_RX15P
PCIE_MTX_GRX_N15 K30 PCIE_RX15N
PCIE_TX0P AH30 PCIE_MRX_GTX_C_P0
PCIE_TX0N AG31 PCIE_MRX_GTX_C_N0
PCIE_TX1P AG29 PCIE_MRX_GTX_C_P1
PCIE_TX1N AF28 PCIE_MRX_GTX_C_N1
PCIE_TX2P AF27 PCIE_MRX_GTX_C_P2
PCIE_TX2N AF26 PCIE_MRX_GTX_C_N2
PCIE_TX3P AD27 PCIE_MRX_GTX_C_P3
PCIE_TX3N AD26 PCIE_MRX_GTX_C_N3
PCIE_TX4P AC25 PCIE_MRX_GTX_C_P4
PCIE_TX4N AB25 PCIE_MRX_GTX_C_N4
PCIE_TX5P Y23 PCIE_MRX_GTX_C_P5
PCIE_TX5N Y24 PCIE_MRX_GTX_C_N5
PCIE_TX6P AB27 PCIE_MRX_GTX_C_P6
PCIE_TX6N AB26 PCIE_MRX_GTX_C_N6
PCIE_TX7P Y27 PCIE_MRX_GTX_C_P7
PCIE_TX7N Y26 PCIE_MRX_GTX_C_N7
PCIE_TX8P W24 PCIE_MRX_GTX_C_P8
PCIE_TX8N W23 PCIE_MRX_GTX_C_N8
PCIE_TX9P V27 PCIE_MRX_GTX_C_P9
PCIE_TX9N U26 PCIE_MRX_GTX_C_N9
PCIE_TX10P U24 PCIE_MRX_GTX_C_P10
PCIE_TX10N U23 PCIE_MRX_GTX_C_N10
PCIE_TX11P T26 PCIE_MRX_GTX_C_P11
PCIE_TX11N T27 PCIE_MRX_GTX_C_N11
PCIE_TX12P T24 PCIE_MRX_GTX_C_P12
PCIE_TX12N T23 PCIE_MRX_GTX_C_N12
PCIE_TX13P P27 PCIE_MRX_GTX_C_P13
PCIE_TX13N P26 PCIE_MRX_GTX_C_N13
PCIE_TX14P P24 PCIE_MRX_GTX_C_P14
PCIE_TX14N P23 PCIE_MRX_GTX_C_N14
PCIE_TX15P M27 PCIE_MRX_GTX_C_P15
PCIE_TX15N N26 PCIE_MRX_GTX_C_N15
100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted
9 CLK_PCIE_VGA AK30 PCIE_REFCLKP
9 CLK_PCIE_VGA# AK32 PCIE_REFCLKN
3,9,26,28,29,31,32,41 PLTRST# AL27 PERSTB
PCIE_CALRN AA22 PCIE_CALRN 2.0K R62
PCIE_CALRP Y22 PCIE_CALRP 1.27K R51
(1.1V)
+PCIE_VDDC
3 PCIE_MRX_GTX_P[0..15]
3 PCIE_MRX_GTX_N[0..15]
PCIE_MRX_GTX_P0 0.1U 2 1 C87 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C94 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C92 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C88 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C100 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C103 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C108 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C115 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C131 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C148 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C136 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C167 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C140 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C180 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C150 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C168 16 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U 2 1 C90 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C96 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C95 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C91 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C105 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C107 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C114 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C128 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C118 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C159 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C142 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C181 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C147 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C166 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C160 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C182 16 PCIE_MRX_GTX_C_N15
M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)
QUANTA COMPUTER
Title
VGA-M92-XT (PCIe)
Size
Document Number
FM9
Rev
3B
Date: Tuesday, October 06, 2009
Sheet 16 of 66

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

+3.3V_DELAY

R436 1 2 10K RAM_CFG0
R435 1 2 *10K_NC RAM_CFG1
R437 1 2 *10K_NC RAM_CFG2

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Strap Controlled Gen2 (Fixed Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0
HSYNC (AH26) / VSYNC (AJ27)	00: No Audio function 01: Audio for DisplayPort only 10: Audio for DisplayPort only and HDMI if dongle is detected 11: Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. it is the responsibility of the system designer to ensure that the system is entitled to support this feature	11

+3.3V_DELAY

R430 1 2 *10K_NC GPIO0
R426 1 2 *10K_NC GPIO1
R61 1 2 *10K_NC GPIO2
R429 1 2 *10K_NC GPIO3
R428 1 2 *10K_NC GPIO4
R68 1 2 *10K_NC GPIO5

R55 1 2 10K HDMI_HD_EN
R438 1 2 *10K_NC TEMP_FAIL
R432 1 2 10K GFX_CLKREQ#
R384 1 2 10K VGAVSYNC
R383 1 2 *10K_NC VGAHSYNC
R1001 1 2 10K DAC1_VGAVSYNC
R1002 1 2 10K DAC1_VGAHSYNC

15

R440 1 2 10K TEMP_FAIL

DAC1_VGAVSYNC / DAC1_VGAHSYNC	HD Audio straps
0\0	No audio function
0\1	Audio for DisplayPort only
1\0	Audio for DisplayPort and HDMI if dongle is detected
1\1	Audio for both DisplayPort and HDMI

+1.8V_RUN_GFX

R56 1 2 10K RAM_TYPE_CFG0
R422 1 2 *10K_NC RAM_TYPE_CFG1
R419 1 2 *10K_NC RAM_TYPE_CFG2

+3.3V_DELAY R32 *0 short 603 +3.3V_RUN

10

GPU 27 MHz CLK source	
from CLK Gen	from Crystal
NC List: R4,R392,R404,Y4, R394, C534, C535, R477, R88, R80 Pop R45,R410 R417=100/F	NC List: R410,R45 Pop List R4,R392,R404, R394,C534,C535,Y4 R477,R88,R80 R417=0 ohm

1

For Park S3:
Install all components in this Box
R431,R423,R427,L52,C545,L23,C111

For M92-S2: DO NOT Install any Component in this Box.

+1.8V_RUN_GFX L52 BLM15BD121SN1D +1.8V_RUN_GFX_R
C545 1U
+PCIE_VDDC L23 BLM15BD121SN1D
C111 1U
+1.8V_RUN_GFX_R

R431 1 2 0 U1
R423 1 2 0 AA1
R427 1 2 0 AB8

U32B PART 2 OF 10

DVP PORT: DVPCLK, DVPCNTL_0, DVPCNTL_1, DVPCNTL_2, DVPCNTL_MVP_0, DVPCNTL_MVP_1, DVPDATA_0 … DVPDATA_23

RAM_TYPE_CFG0 AD7
RAM_TYPE_CFG1 AB2
RAM_TYPE_CFG2 AC10

DAC1: R AM26 / RB AK26; G AL25 / GB AJ25; B AH24 / BB AG25; HSYNC AH26 DAC1_VGAHSYNC; VSYNC AJ27 DAC1_VGAVSYNC; AVDD AG24; AVSSQ AE22; VDD1DI AE23; VSS1DI AD23; RSET AD22 RSET R49 499R

+1.8V_RUN_GFX C101 0.1U AVDD=70mA max
+1.8V_RUN_GFX C112 *0.1U_NC VDD1DI=45mA max

DIS only
VGA_BLU R398 150/F
VGA_GRN R399 150/F
VGA_RED R400 150/F

Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

+3.3V_DELAY R425 10K R424 10K
HPD1
Q60 MMST3904-7-F
Q59 DTC114TUAT106
HDMI_DET 24
R420 100K

I/O: GPIO_0 … GPIO_23_CLKREQB, JTAG_TRSTB, JTAG_TDI, JTAG_TCK, JTAG_TMS, JTAG_TDO

GPIO0 U6
GPIO1 U10
GPIO2 T10
GPIO3 U8
GPIO4 U7
GPIO5 T9
50 GFX_CORE_CNTRL2 T8
29 PANEL_BKEN T7
HDMI_HD_EN P10
T45 PAD P4
T46 PAD P2
RAM_CFG0 N6
RAM_CFG1 N5
RAM_CFG2 N3
50 GFX_CORE_CNTRL0 Y9
CLK_VGA_27M_SSIN_R N1
19 THERMAL_INT# R433 *0_NC M4
TEMP_FAIL R6
T8 PAD W10
50 GFX_CORE_CNTRL1 18 BB_ENA M2
P7
T10 PAD N8
GFX_CLKREQ# N7
10 +3.3V_DELAY R439 2 1 10K L6
GPIO26_CLK R477 2 1 10K L5
T49 PAD L3
T13 PAD K4

T5 PAD AB13 GENERICA
T44 PAD W8 GENERICB
T41 PAD W9 GENERICC
T43 PAD W7 GENERICD
T2 PAD AD10 GENERICE_HPD4

HPD1 AC14
+1.8V_RUN_GFX R382 2 1 499/F VREFG AC16
R396 1 2 249/F
C527 0.1U

RESERVED: NC_PWRGOOD, RSVD#8, RSVD#9, NC#1, NC#2, RSVD#3, RSVD#2, RSVD#1

1 For M92: No stuff R1011 For Park: Stuff R1011
R1011 1 2 10K N10
R1034 1 2 0 XO_IN AB22 XO_IN AC22

R64 10K 24 ENVDD 24 BIA_PWM
R50 10K
+3.3V_DELAY R88 10K R42 10K
19 TEST_EN AF24
AF24 is TESTEN on both M92S2 and ParkS3. Implement 10K ohm PU and PD for both and connected to K7 pin

T14 PAD L9
T11 PAD N9
T3 PAD AB16
AB12
R396 1 2 *0 short AB11
TESTEN AF24

PARK-S3

DAC2: R2 AM12 / R2B AK12 VGA_RED 25; G2 AL11 / G2B AJ11 VGA_GRN 25; B2 AK10 / B2B AL9 VGA_BLU 25; H2SYNC AL13 VGAHSYNC 25; V2SYNC A13 VGAVSYNC 25; C AH12; Y AM10; COMP AJ9; A2VDD AE20; A2VDDQ AE17; A2VSSQ AE19; VDD2DI AD19; VSS2DI AC19; R2SET AG13 R2SET R401 715

+3.3V_DELAY +A2VDD C548 0.1U A2VDD=130mA max
+1.8V_RUN_GFX +A2VDDQ L48 BLM15BD121SN1D C528 0.1U C522 1U A2VDDQ=1.5mA max

Keep A2VSSQ away from noisy ground.

+1.8V_RUN_GFX +VDD2DI C547 0.1U VDD2DI=50mA max
Place very close to ASIC balls

R408 *0_NC
OSC_SPREAD
R416 *0_NC
15 CLK_VGA_27M_SS CLK_VGA_27M_SSIN_R
10 GPIO26_CLK R4 0
R409 *10K_NC
R45 *0_NC
15 CLK_VGA_27M R417 0
R410 *120/F_NC
OSC_OUT XTALIN 25
R404 0
R406 *1M_NC
R46 *221/F_NC
12 Y4 27MHZ R392 0 XTALOUT 21
R394 1M
C535 27P 50
C534 27P 50

Spread Spectrum
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

+3.3V_RUN
R393 *10K_NC
OSC_OUT
R390 *10K_NC
R391 *10K_NC
U31 XIN/CLKIN XOUT VSS VDD SO PD# SSCLK REFCLK
R411 *0_NC
OSC_SPREAD
*P1819GF-08SR_NC
+3VL
C531 *10U_NC 805 10
L54 *BLM11A05S_NC
C542 *0.1U_NC 10
3.3V_RUN

	S0
-1.75% (DOWN)	0

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 Level ASS'
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502	AKD5LGGT505	K4W1G1646E-HC12	31FM9MB0000_CP 31FM9MB0040_AD
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00	AKD5LZGTW03	H5TQ1G63BFR-12C	31FM9MB0010_CP 31FM9MB0030_AD
Park XT S3:IC CTRL(631)100-CK3374(216-0774009)FCBGA Non-Consign QCI PN : AJ077400T04							
Park XT S3:IC CTRL(631)100-CK3374(216-0774009)FCBGA WIN BSQ QCI PN : AJ077400T05							
800MHz 1GB(128M*16) Samsung	1	1	1	AKD5MGGT501		K4W2G1646B-HC12	31FM9MB0080_CP 31FM9MB0060_AD
800MHz 1GB(128M*16) Hynix	1	1	0				31FM9MB0070_CP 31FM9MB0050_AD
	1	0	1				
	1	0	0				

13

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 3B
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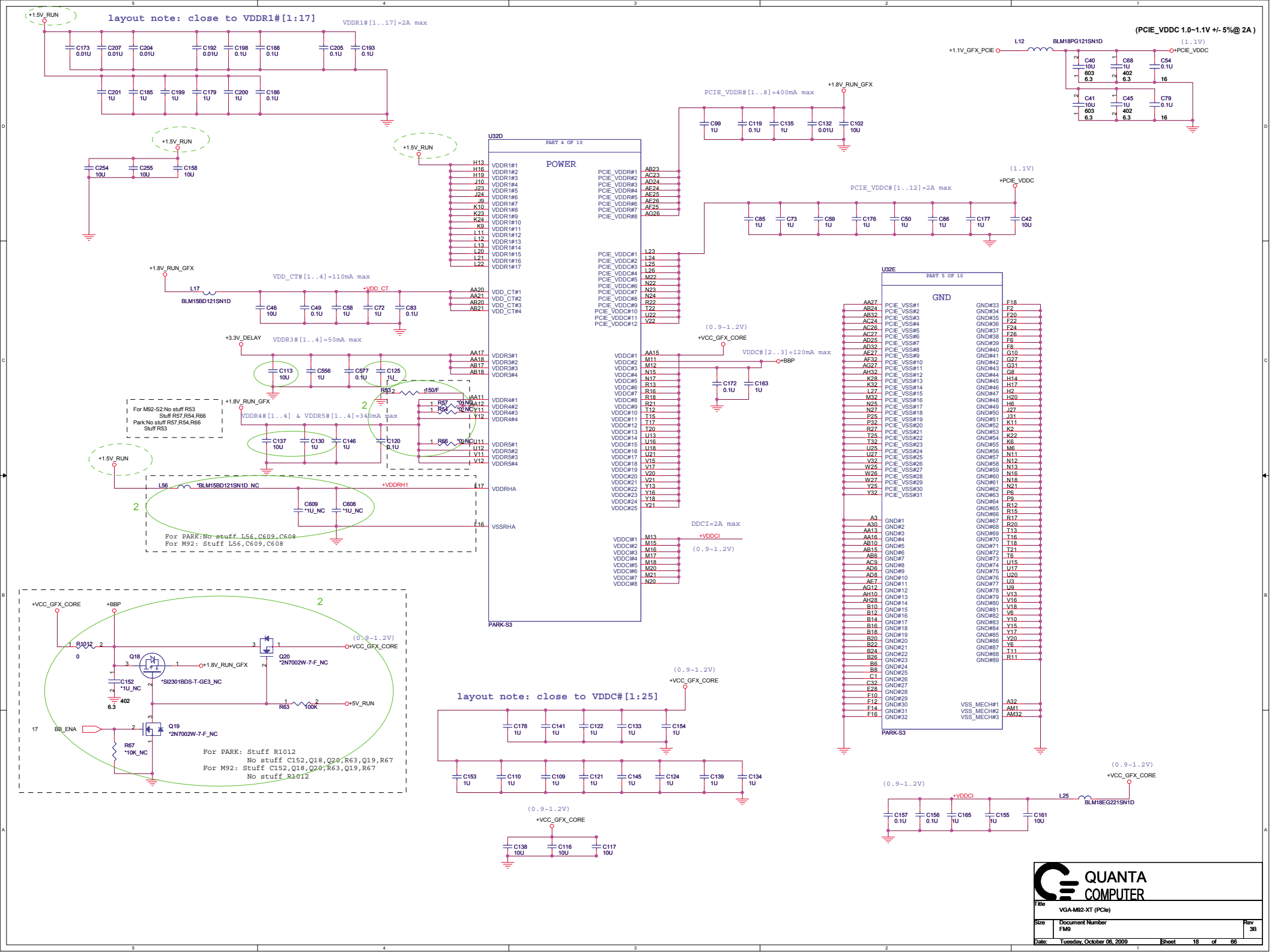
layout note: close to VDDR1#[1:17]
VDDR1#[1..17]=2A max
(PCIE_VDDC 1.0~1.1V +/- 5%@ 2A)
+1.5V_RUN
C173 0.01U
C207 0.01U
C204 0.01U
C192 0.01U
C198 0.1U
C188 0.1U
C205 0.1U
C193 0.1U
C201 1U
C185 1U
C199 1U
C179 1U
C200 1U
C186 0.1U
C254 10U
C255 10U
C158 10U
U32D
PART 4 OF 10
POWER
PARK-S3
VDDR1#1
VDDR1#2
VDDR1#3
VDDR1#4
VDDR1#5
VDDR1#6
VDDR1#7
VDDR1#8
VDDR1#9
VDDR1#10
VDDR1#11
VDDR1#12
VDDR1#13
VDDR1#14
VDDR1#15
VDDR1#16
VDDR1#17
PCIE_VDDR#1
PCIE_VDDR#2
PCIE_VDDR#3
PCIE_VDDR#4
PCIE_VDDR#5
PCIE_VDDR#6
PCIE_VDDR#7
PCIE_VDDR#8
PCIE_VDDR#[1..8]=400mA max
+1.8V_RUN_GFX
C99 1U
C119 0.1U
C135 1U
C132 0.01U
C102 10U
L12
BLM18PG121SN1D
+1.1V_GFX_PCIE
(1.1V)
+PCIE_VDDC
C40 10U 603 6.3
C68 1U 402 6.3
C54 0.1U 16
C41 10U 603 6.3
C45 1U 402 6.3
C79 0.1U 16
PCIE_VDDC#1
PCIE_VDDC#2
PCIE_VDDC#3
PCIE_VDDC#4
PCIE_VDDC#5
PCIE_VDDC#6
PCIE_VDDC#7
PCIE_VDDC#8
PCIE_VDDC#9
PCIE_VDDC#10
PCIE_VDDC#11
PCIE_VDDC#12
PCIE_VDDC#[1..12]=2A max
C85 1U
C73 1U
C59 1U
C176 1U
C50 1U
C86 1U
C177 1U
C42 10U
+1.8V_RUN_GFX
L17
BLM15BD121SN1D
VDD_CT#[1..4]=110mA max
+VDD_CT
C46 10U
C49 0.1U
C58 1U
C72 1U
C83 0.1U
VDD_CT#1
VDD_CT#2
VDD_CT#3
VDD_CT#4
+3.3V_DELAY
VDDR3#[1..4]=50mA max
C113 10U
C556 1U
C577 0.1U
C125 1U
VDDR3#1
VDDR3#2
VDDR3#3
VDDR3#4
R53 2 150/F
+1.8V_RUN_GFX
VDDR4#[1..4] & VDDR5#[1..4]=340mA max
R57 *0.NC
R54 *0.NC
R66 *0.NC
C137 10U
C130 1U
C146 1U
C120 0.1U
VDDR4#1
VDDR4#2
VDDR4#3
VDDR4#4
VDDR5#1
VDDR5#2
VDDR5#3
VDDR5#4
For M92-S2:No stuff R53
Stuff R57,R54,R66
Park:No stuff R57,R54,R66
Stuff R53
+1.5V_RUN
L56
*BLM15BD121SN1D_NC
+VDDRH1
C609 *1U_NC
C608 *1U_NC
VDDRHA
VSSRHA
For PARK:No stuff L56,C609,C608
For M92: Stuff L56,C609,C608
+VCC_GFX_CORE
(0.9~1.2V)
VDDC#[2..3]=120mA max
+BBP
C172 0.1U
C163 1U
VDDC#1
VDDC#2
VDDC#3
VDDC#4
VDDC#5
VDDC#6
VDDC#7
VDDC#8
VDDC#9
VDDC#10
VDDC#11
VDDC#12
VDDC#13
VDDC#14
VDDC#15
VDDC#16
VDDC#17
VDDC#18
VDDC#19
VDDC#20
VDDC#21
VDDC#22
VDDC#23
VDDC#24
VDDC#25
DDCI=2A max
+VDDCI
VDDCI#1
VDDCI#2
VDDCI#3
VDDCI#4
VDDCI#5
VDDCI#6
VDDCI#7
VDDCI#8
U32E
PART 5 OF 10
GND
PARK-S3
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
+VCC_GFX_CORE
+BBP
R1012 0
Q18
Q20 *2N7002W-7-F_NC
+1.8V_RUN_GFX
C152 *1U_NC 402 6.3
*SI2301BDS-T-GE3_NC
R63 100K
+5V_RUN
BB_ENA
Q19 *2N7002W-7-F_NC
R67 *10K_NC
For PARK: Stuff R1012
No stuff C152,Q18,Q20,R63,Q19,R67
For M92: Stuff C152,Q18,Q20,R63,Q19,R67
No stuff R1012
layout note: close to VDDC#[1:25]
C178 1U
C141 1U
C122 1U
C133 1U
C154 1U
C153 1U
C110 1U
C109 1U
C121 1U
C145 1U
C124 1U
C139 1U
C134 1U
C138 10U
C116 10U
C117 10U
L25
BLM18EG221SN1D
C157 0.1U
C156 0.1U
C165 1U
C155 1U
C161 10U
QUANTA COMPUTER
Title
VGA-M92-XT (PCIe)
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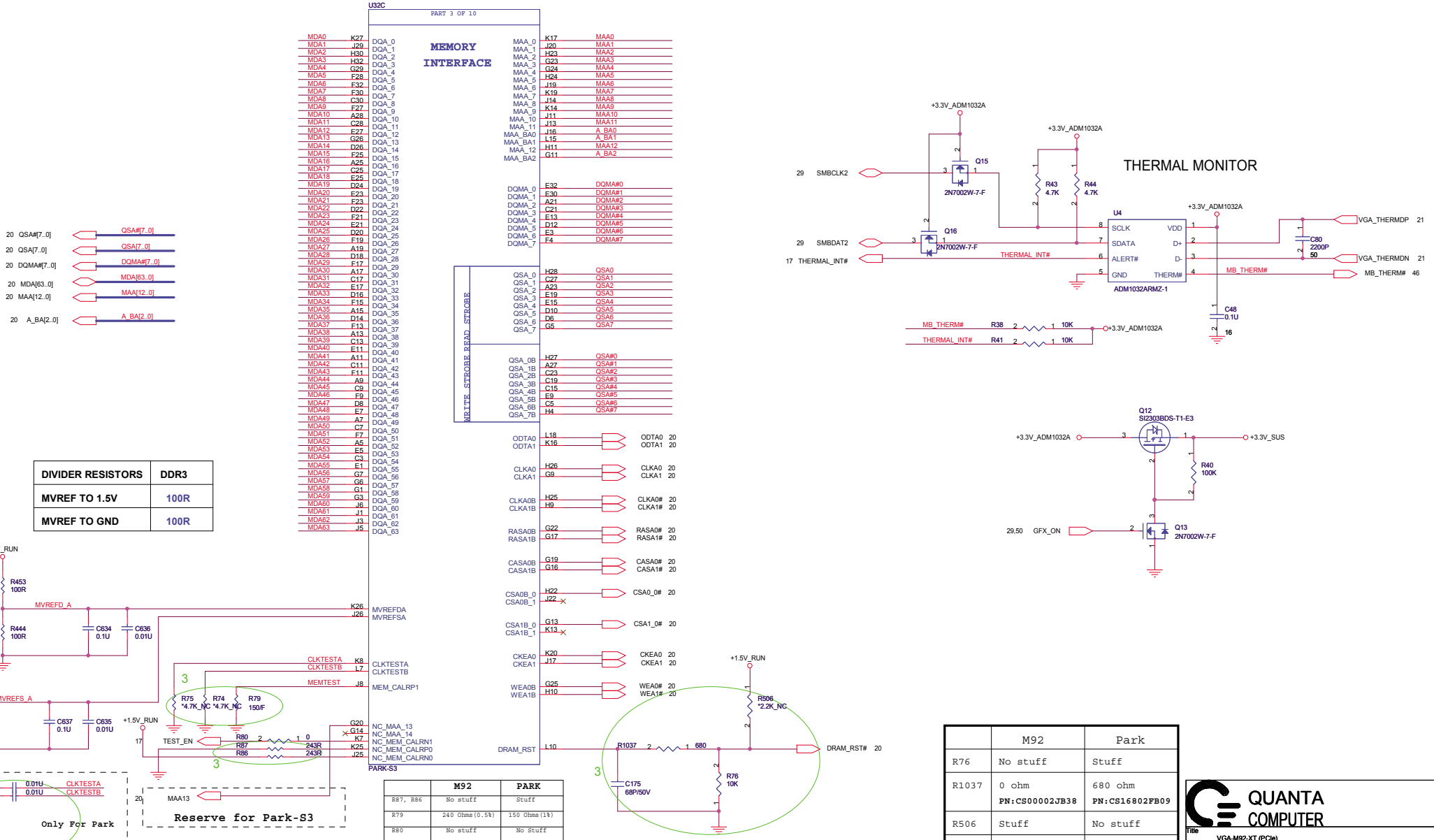
MEMORY INTERFACE



	M92	PARK
R87, R86	No stuff	Stuff
R79	240 Ohms(0.5%)	150 Ohms(1%)
R80	No stuff	No Stuff
C1015,C016 R1036,R1035	No stuff	Stuff
R74,R75	Stuff	No stuff

	M92	Park
R76	No stuff	Stuff
R1037	0 ohm PN:CS00002JB38	680 ohm PN:CS16802FB09
R506	Stuff	No stuff
C175	2200pF PN:CH2226K9B00	68pF PN:CH06806JB01

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DDR3

19 MDA[63..0] — MDA[63..0]
19 MAA[12..0] — MAA[12..0]
19 QSA[7..0] — QSA[7..0]
19 QSA#[7..0] — QSA#[7..0]
19 DQMA#[7..0] — DQMA#[7..0]
19 DRAM_RST# — DRAM_RST#
19 A_BA[2..0] — A_BA[2..0]

U11 / U36 / U10 / U35 — 96-BALL SDRAM DDR3 — K4W2G1646B-HC12

Reserve for Park-S3

+1.5V_RUN

Should be 240 Ohms +-1%

R484 240/F (U11) | R483 240/F (U36) | R138 240/F (U10) | R486 240/F (U35)

Placement has to be close to VRAM

CLKA0 R464 56/F — C653 0.01U 25 — CLKA0# R468 56/F
CLKA1 R118 56/F — C309 0.01U 25 — CLKA1# R120 56/F

R139 4.99K/F — R119 4.99K/F — C302 0.1U 10 — R479 4.99K/F — R475 4.99K/F — C651 0.1U 10 (VREFC_U47 / VREFD_U47)

R504 4.99K/F — R508 4.99K/F — C689 0.1U 10 — R481 4.99K/F — R480 4.99K/F — C656 0.1U 10 (VREFC_U48 / VREFD_U48)

R503 4.99K/F — R507 4.99K/F — C688 0.1U 10 — R116 4.99K/F — R111 4.99K/F — C294 0.1U 10 (VREFC_U49 / VREFD_U49)

R162 4.99K/F — R143 4.99K/F — C310 0.1U 10 — R115 4.99K/F — R112 4.99K/F — C292 0.1U 10 (VREFC_U50 / VREFD_U50)

close to U47

C287 1U — C277 1U — C301 1U
C256 1U — C312 1U — C290 1U
C311 10U 603 — C295 10U 603 — C286 10U 603 — C283 10U 603

close to U48

C629 1U — C640 1U — C650 1U
C639 1U — C630 1U — C683 1U
C671 10U 603 — C685 10U 603 — C647 10U 603 — C643 10U 603

close to U49

C281 1U — C268 1U — C280 1U
C259 1U — C641 1U — C258 1U
C319 10U 603 — C320 10U 603 — C321 10U 603 — C322 10U 603

close to U50

C852 1U — C657 1U — C642 1U
C284 1U — C645 1U — C638 1U
C691 10U 603 — C892 10U 603 — C631 10U 603 — C660 10U 603

QUANTA COMPUTER

Title	VGA-M92-S (VRAM)	
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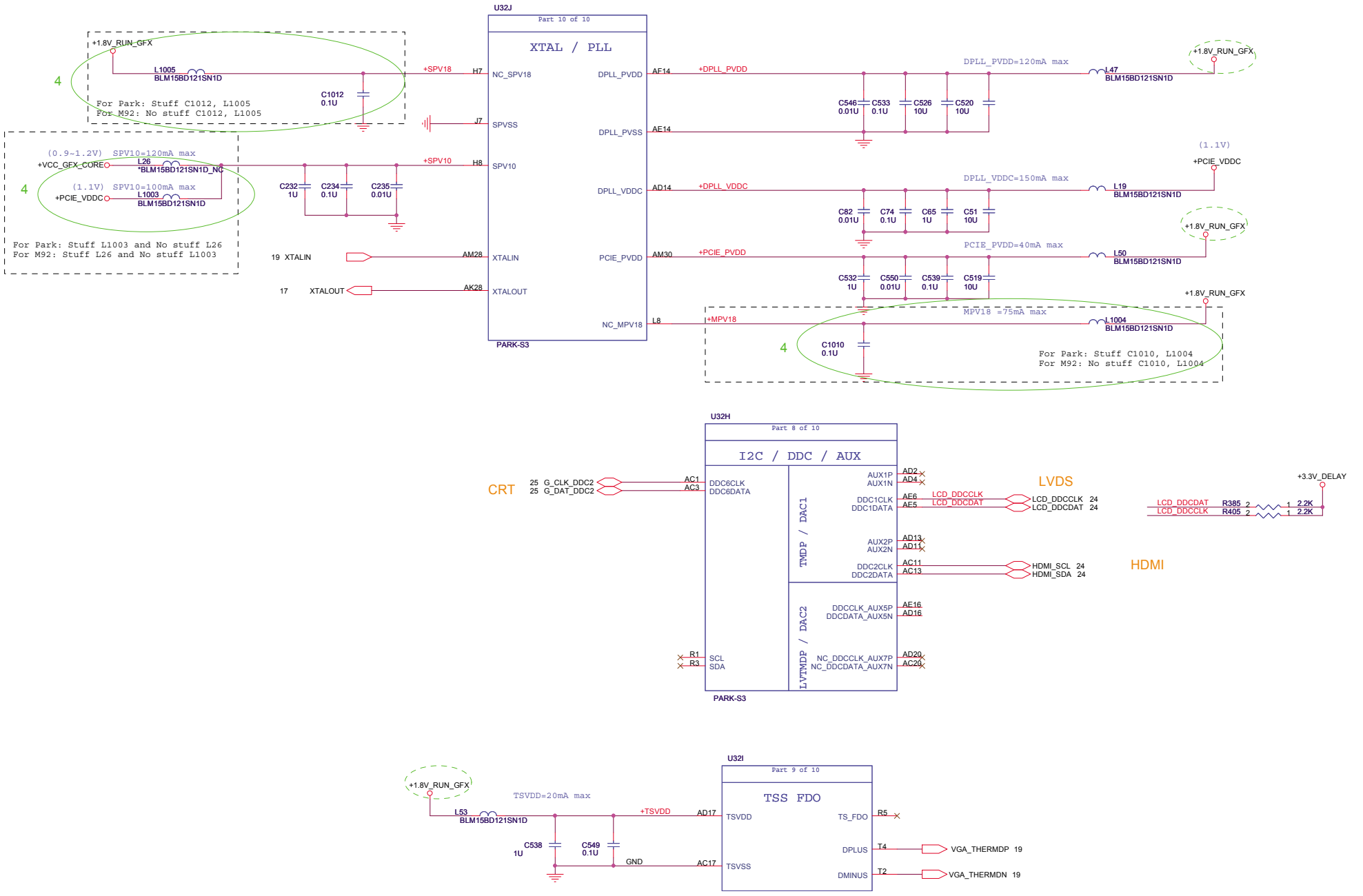

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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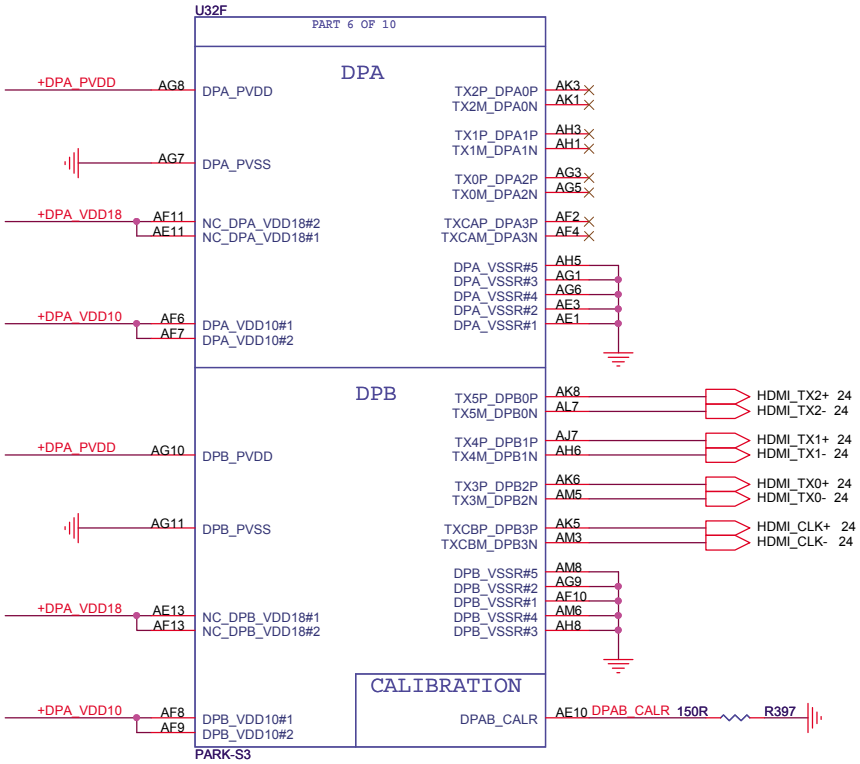
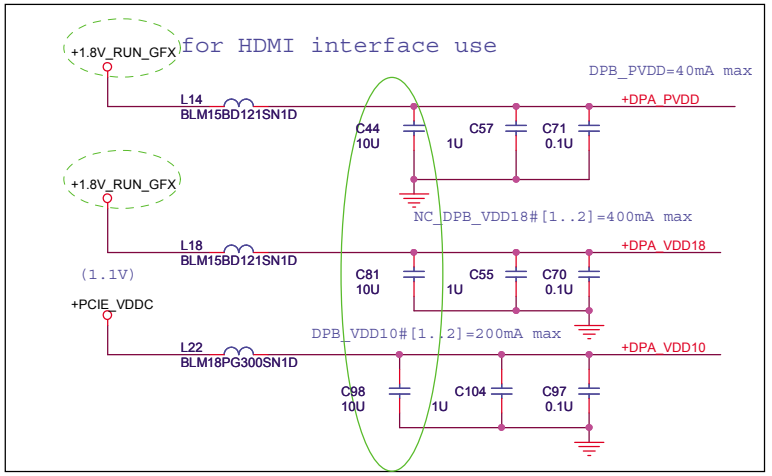
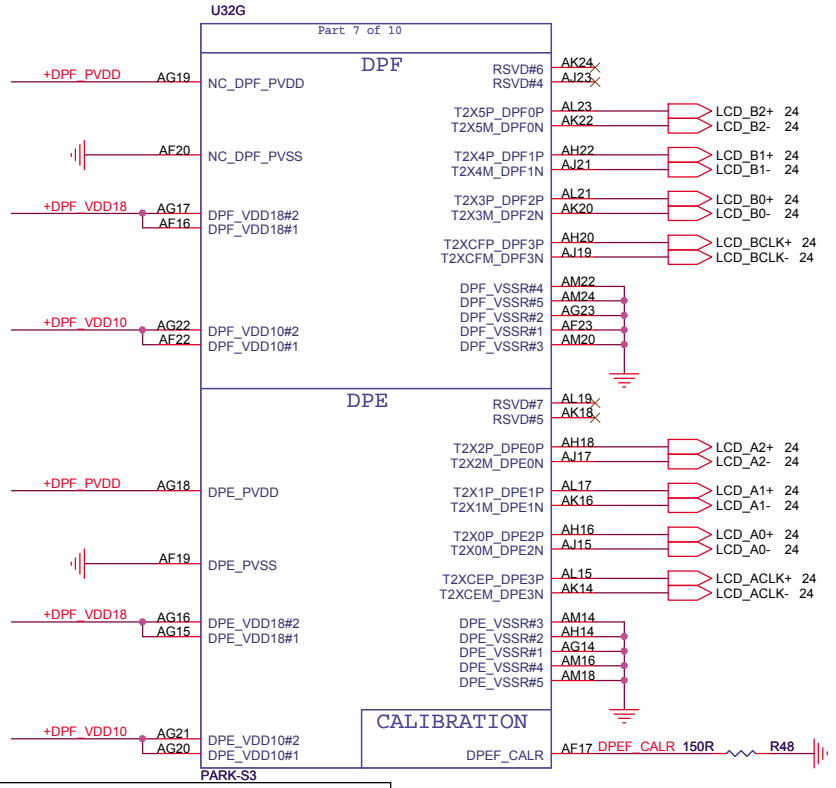
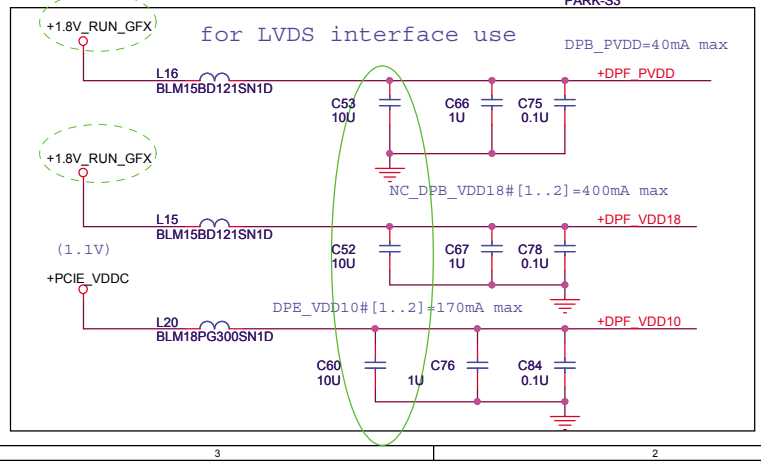
TMDP(HDMI) INTERFACE





LVDS INTERFACE





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QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
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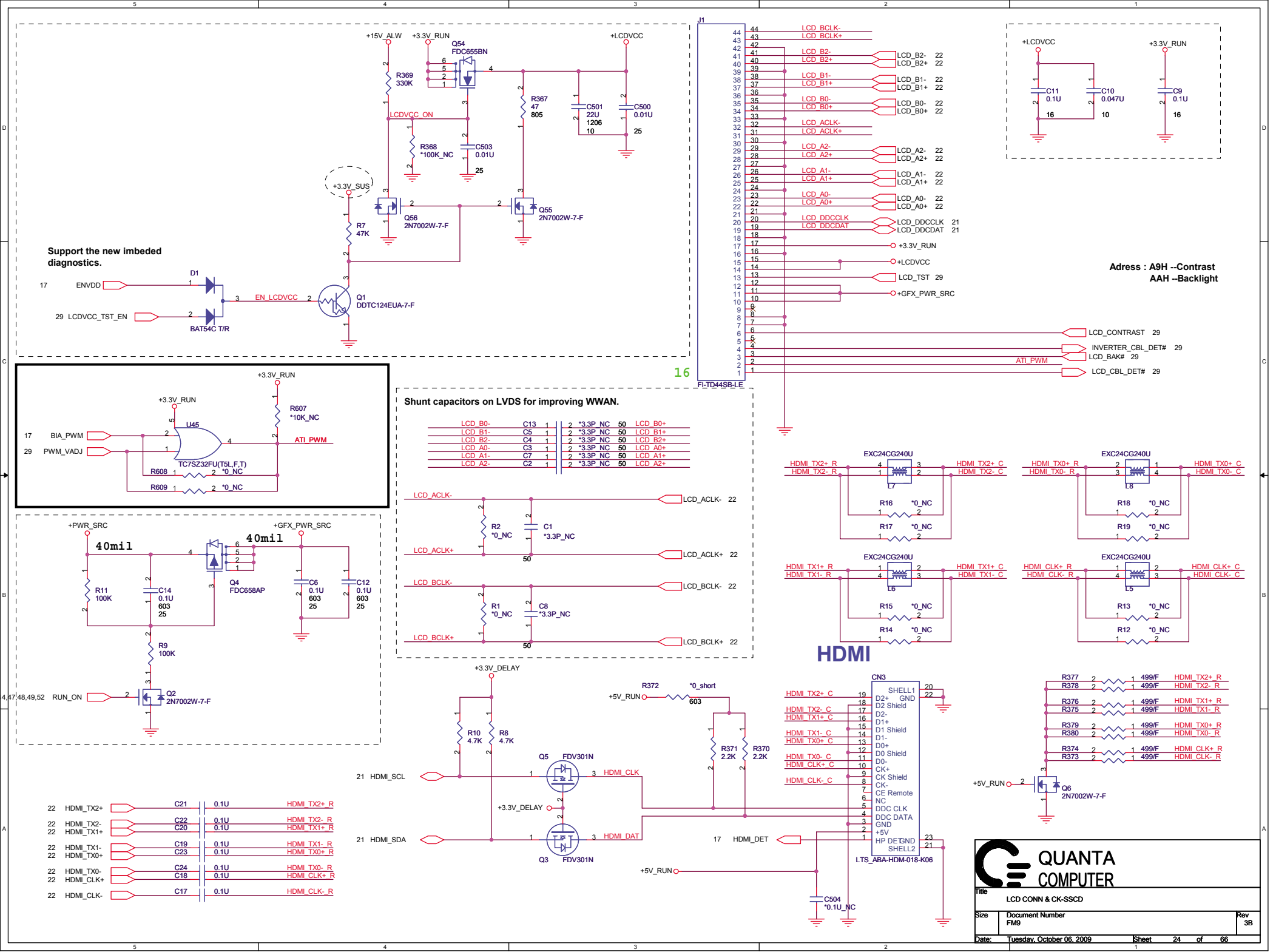
Support the new imbeded diagnostics.
Shunt capacitors on LVDS for improving WWAN.
Adress : A9H --Contrast
AAH --Backlight
HDMI
16
+15V_ALW
+3.3V_RUN
+LCDVCC
+3.3V_SUS
+3.3V_DELAY
+PWR_SRC
+GFX_PWR_SRC
LCDVCC_ON
ENVDD
LCDVCC_TST_EN
EN_LCDVCC
BIA_PWM
PWM_VADJ
ATI_PWM
RUN_ON
HDMI_SCL
HDMI_SDA
HDMI_DET
HDMI_CLK
HDMI_DAT
LCD_TST
LCD_CONTRAST
INVERTER_CBL_DET#
LCD_BAK#
LCD_CBL_DET#
+GFX_PWR_SRC
FI-TD44SB-LE
LTS_ABA-HDM-018-K06
Q54 FDC655BN
Q56 2N7002W-7-F
Q55 2N7002W-7-F
Q1 DDTC124EUA-7-F
D1 BAT54C T/R
Q4 FDC658AP
Q2 2N7002W-7-F
Q5 FDV301N
Q3 FDV301N
Q6 2N7002W-7-F
U45 TC7SZ32FU(T5L,F,T)
40mil
40mil
QUANTA COMPUTER
Title
LCD CONN & CK-SSCD
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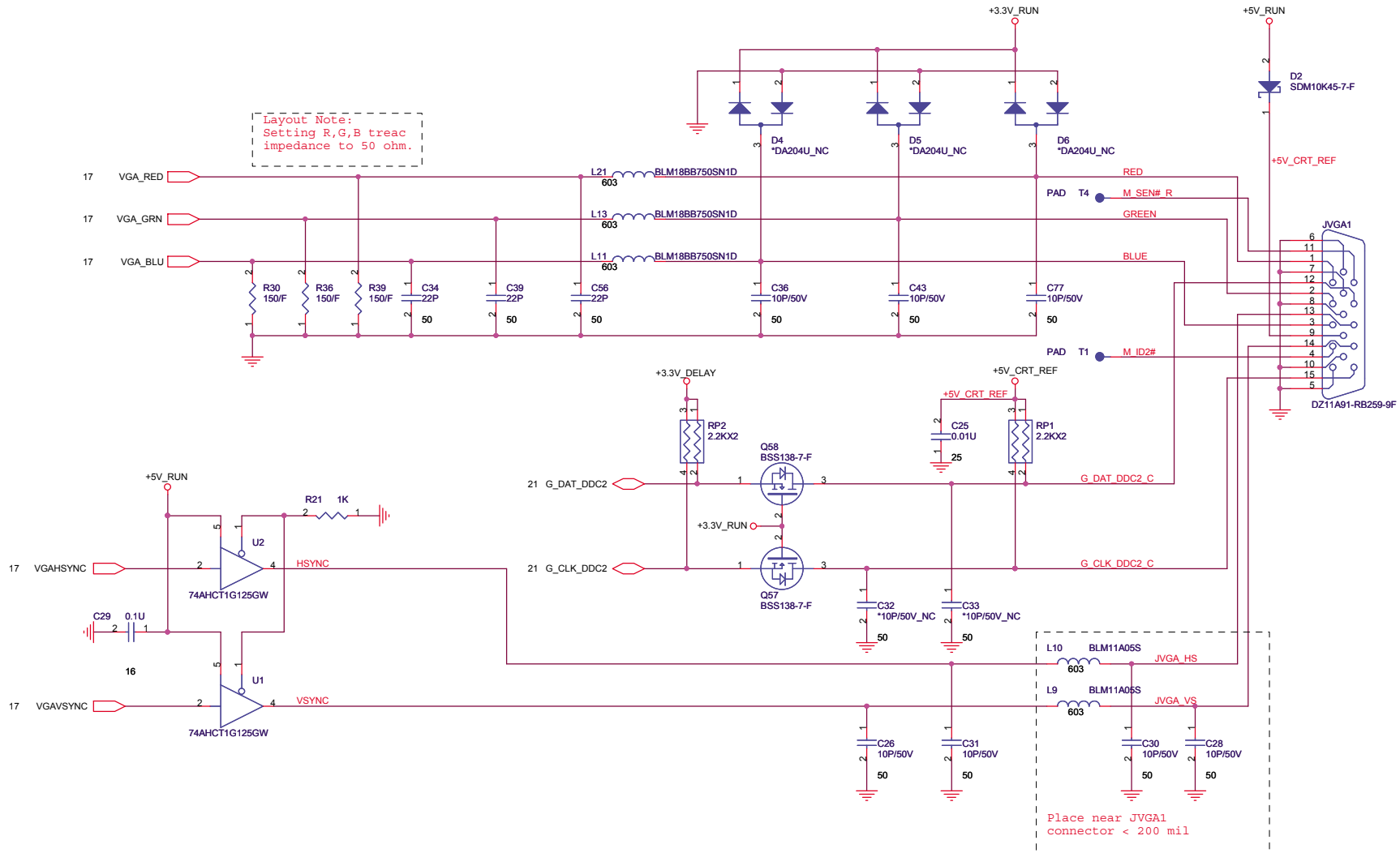

QUANTA COMPUTER

Title	CRT&TV CONN	
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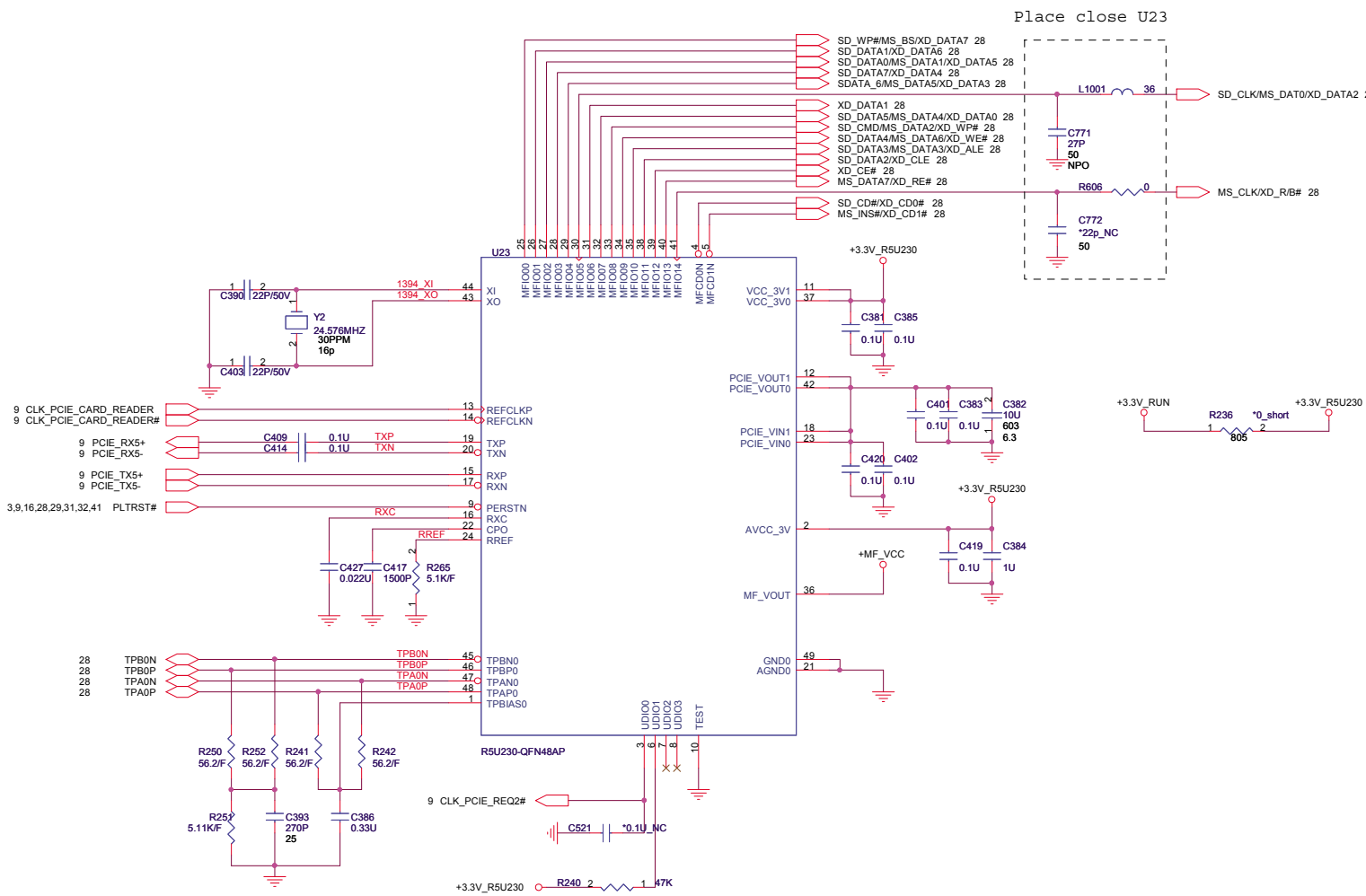

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
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QUANTA COMPUTER

Title	IEEE 1394	
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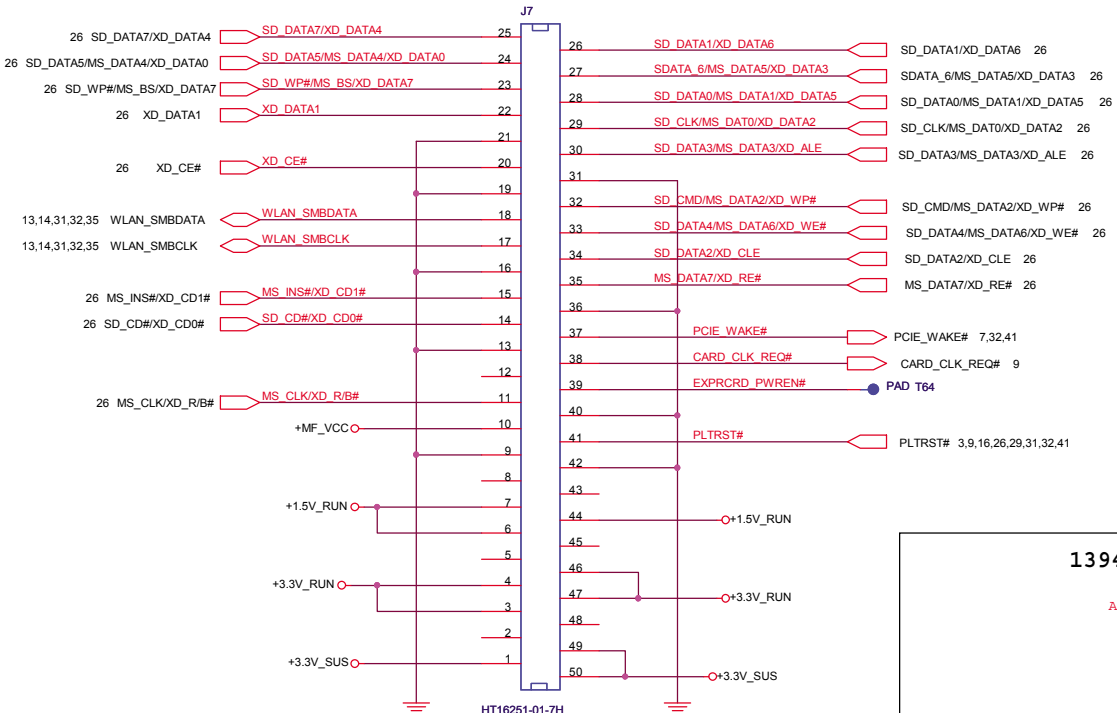
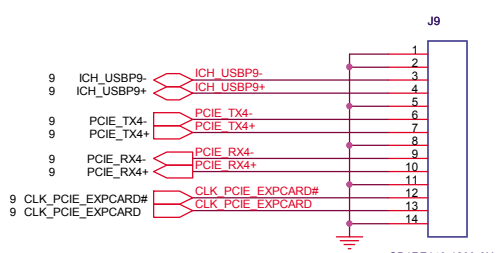
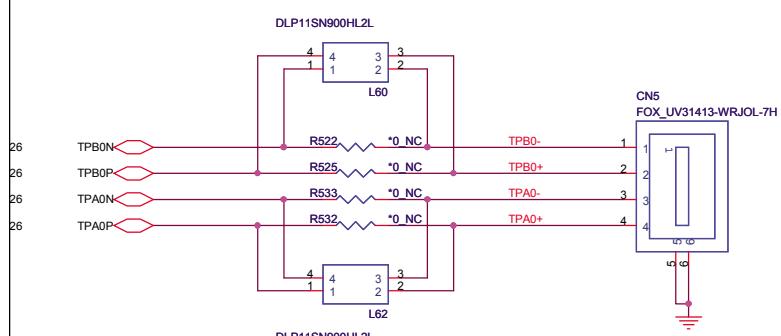
Express Card/CARD READER





1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
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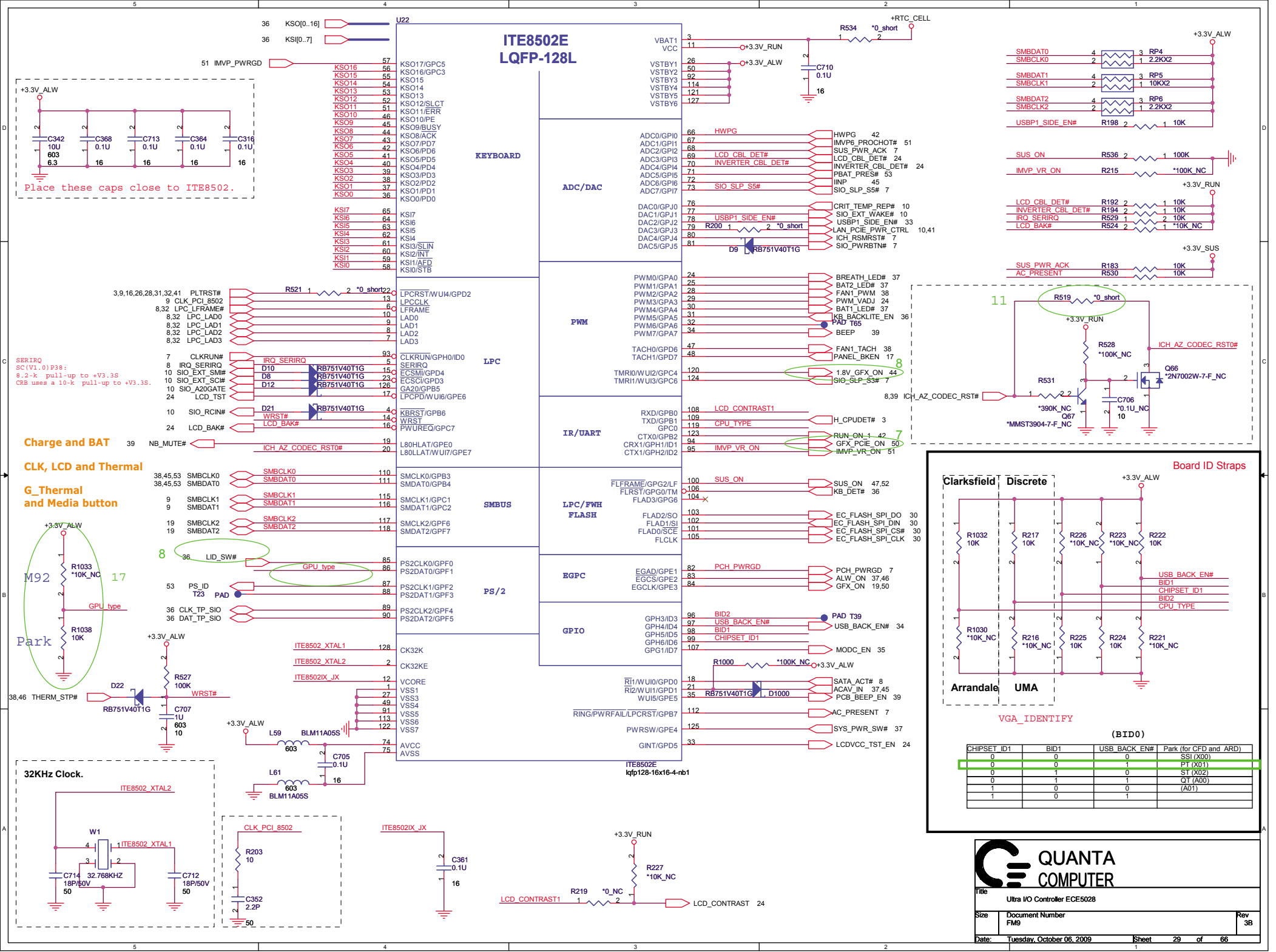

CHIPSET_ID1	BID1	USB_BACK_EN#	Park (for CFD and ARD)
0	0	0	SSI (X00)
0	0	1	PT (X01)
0	1	0	ST (X02)
0	1	1	QT (A00)
1	0	0	(A01)
1	0	1	

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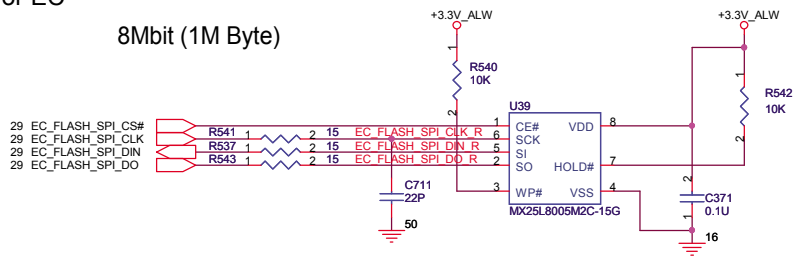
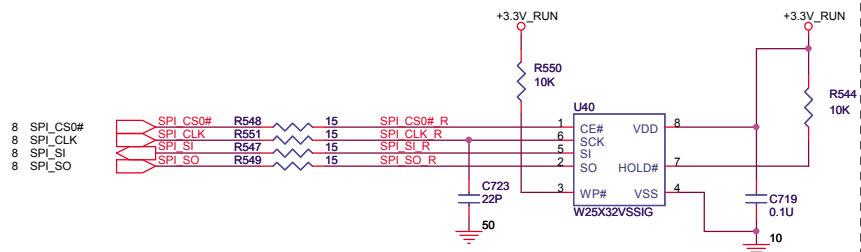
For EC

8Mbit (1M Byte)

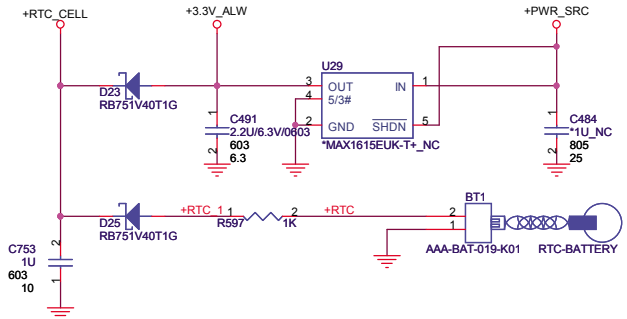


For PCH

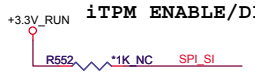
32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
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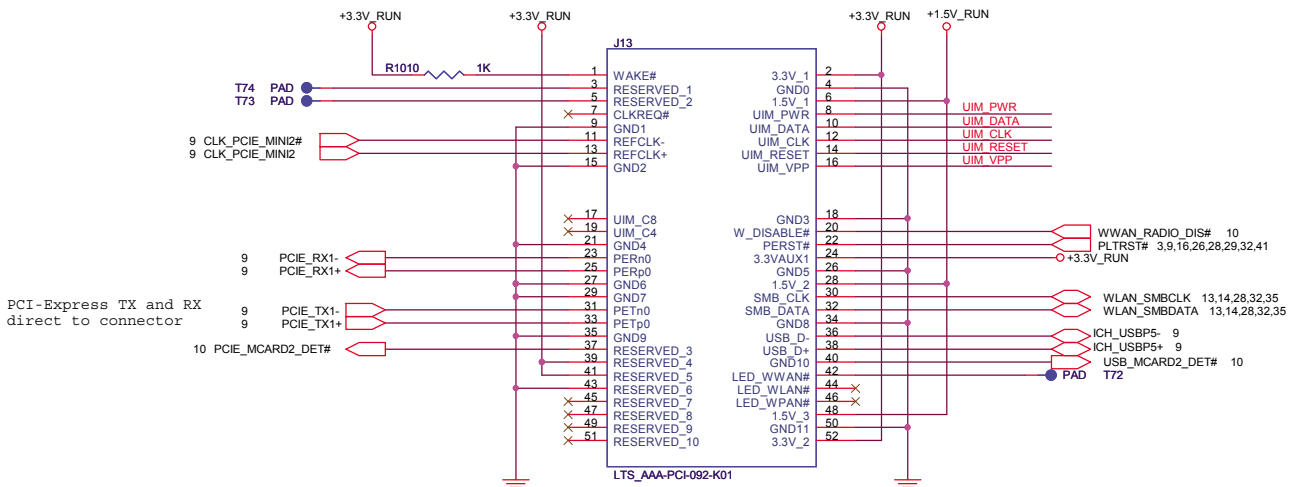
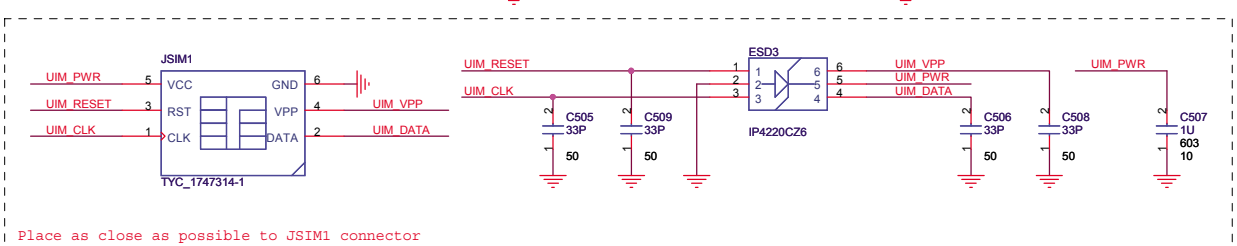
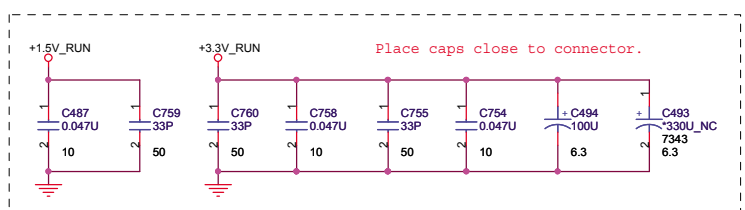
MiniCard WWAN connector







QUANTA COMPUTER

Title	MINI-PCI	
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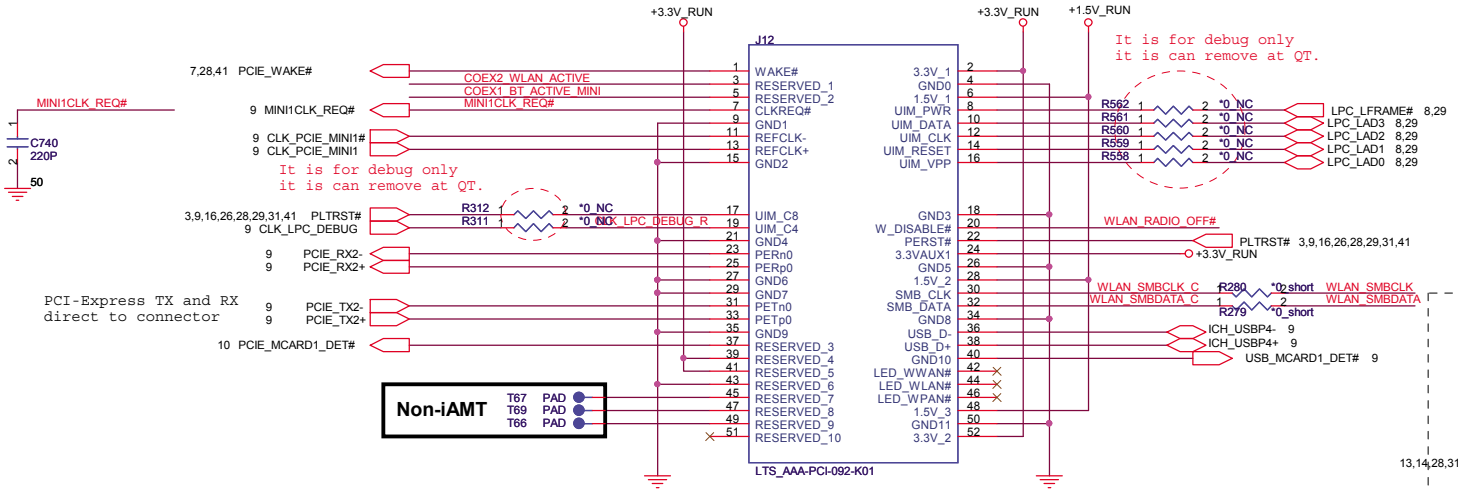
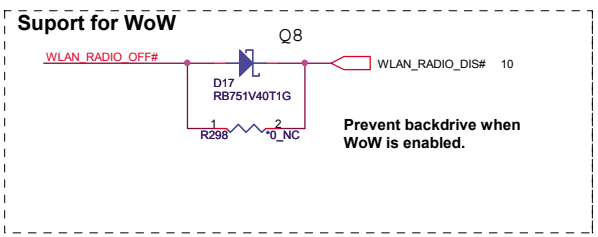
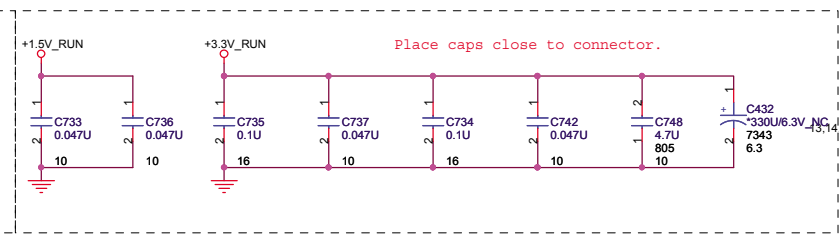
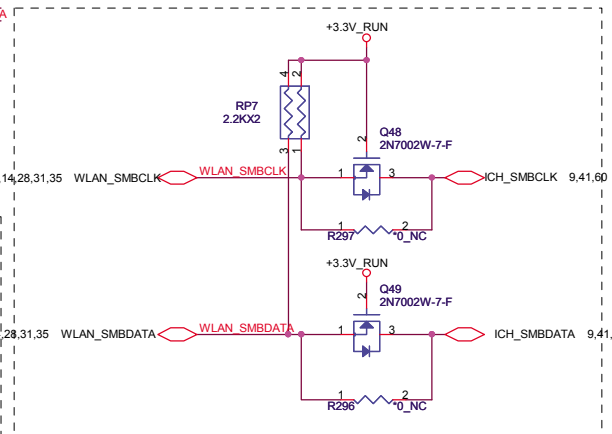
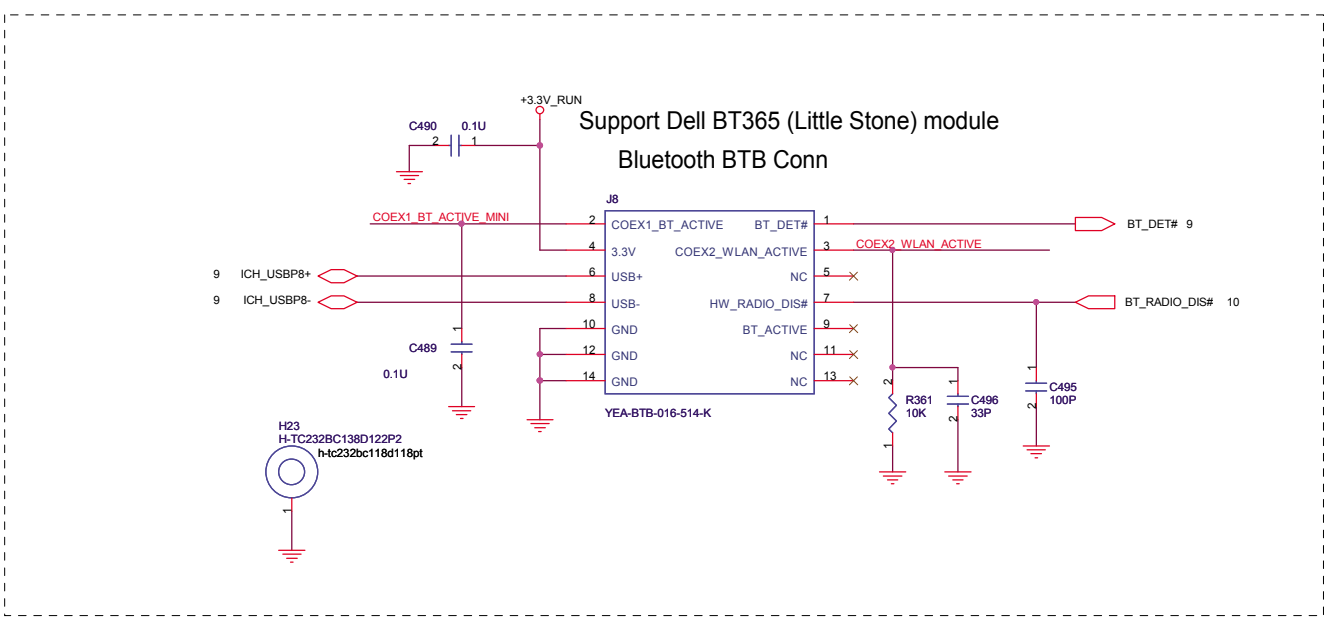
MiniCard WLAN connector





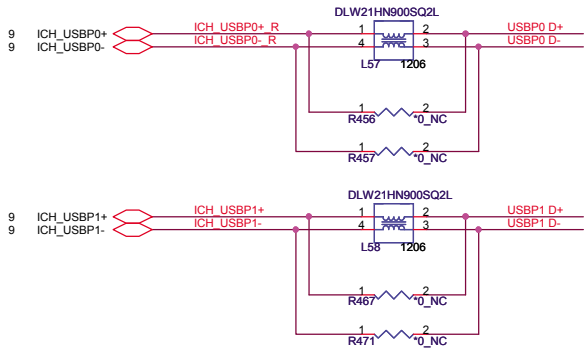






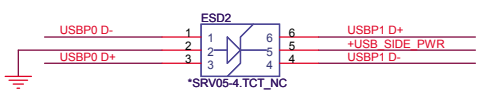
QUANTA COMPUTER		
Title: MDC CONN.		
Size	Document Number: FM9	Rev: 3B
Date: Tuesday, October 06, 2009	Sheet 32 of 66	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



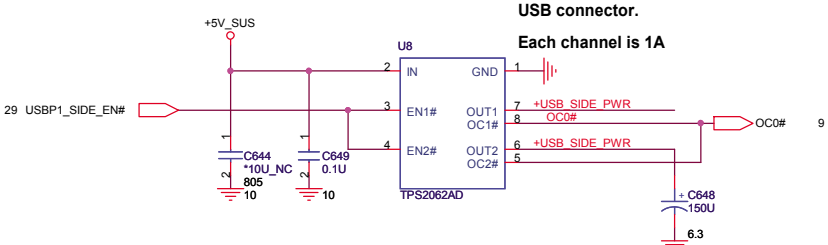
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



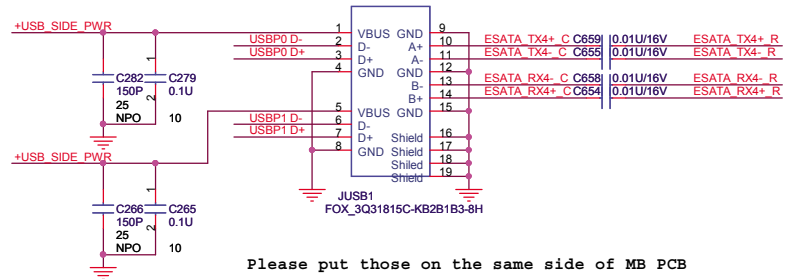
Place one 150uF cap by each USB connector.

Each channel is 1A



Side External USBX2

PN is old, Because New Part can't ready before SST build.

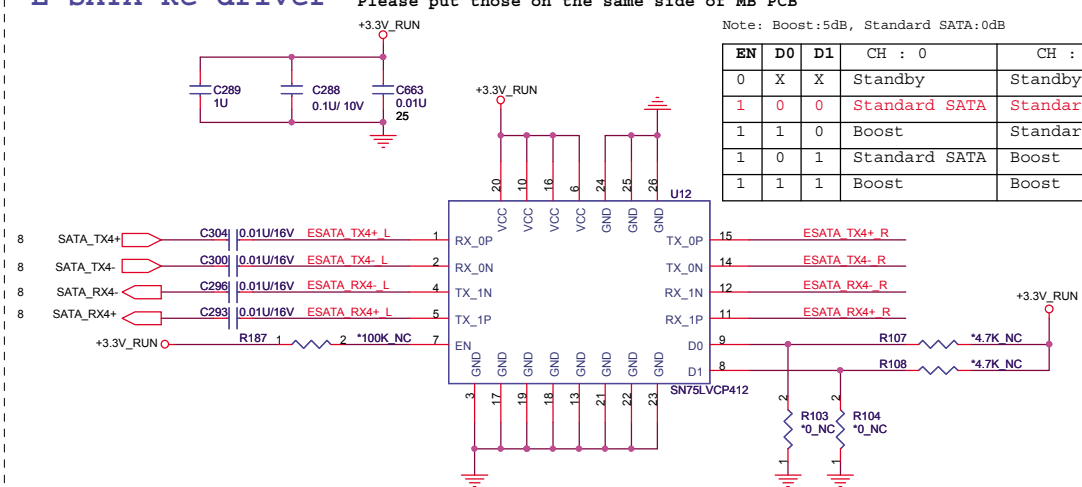


Please put those on the same side of MB PCB

USBx2 & ESATA COMBO

E-SATA Re-driver

Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

QUANTA COMPUTER

Title	SERIAL PORT & USB	
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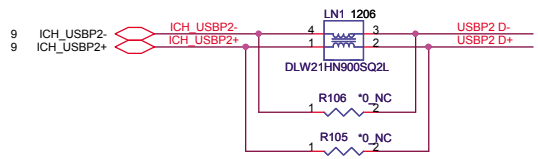
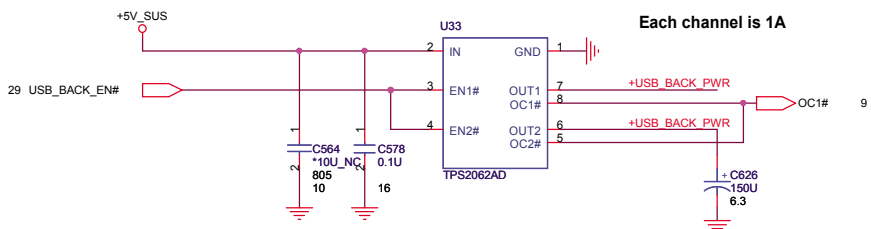
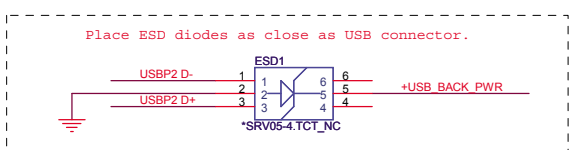
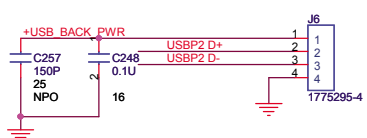


Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
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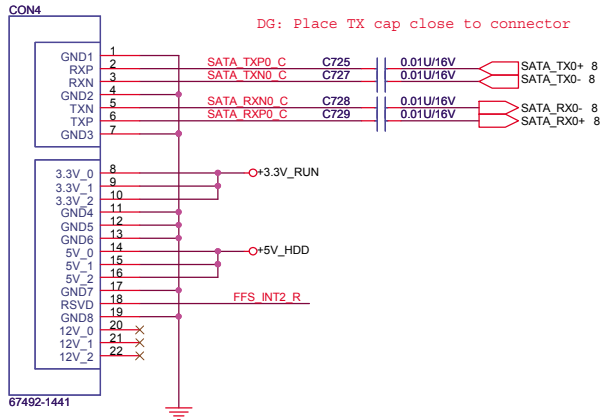
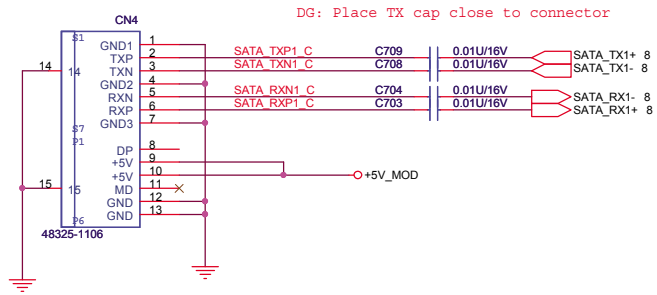
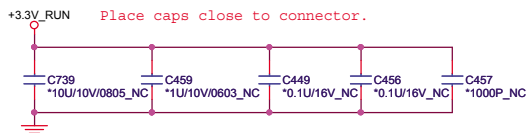
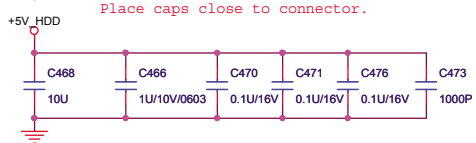
SATA Connector.

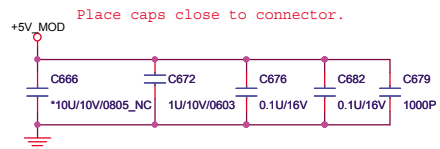


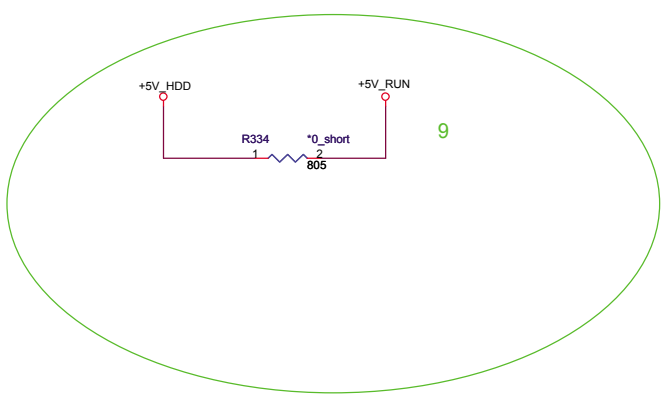
ODD Connector

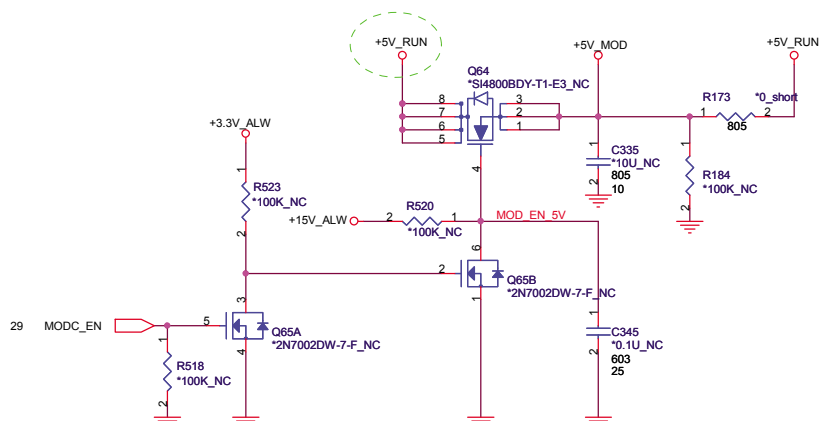


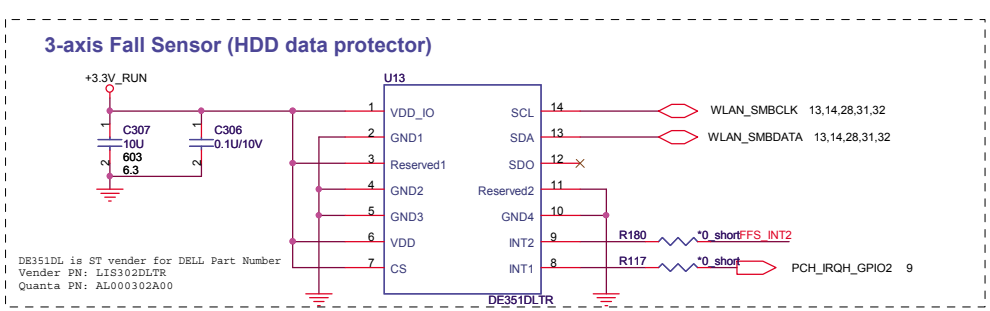


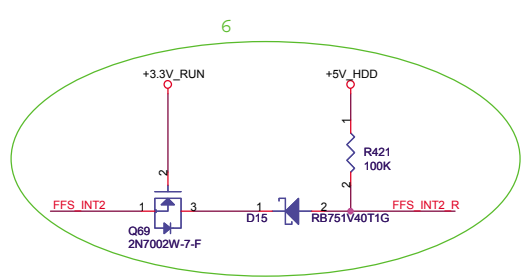












QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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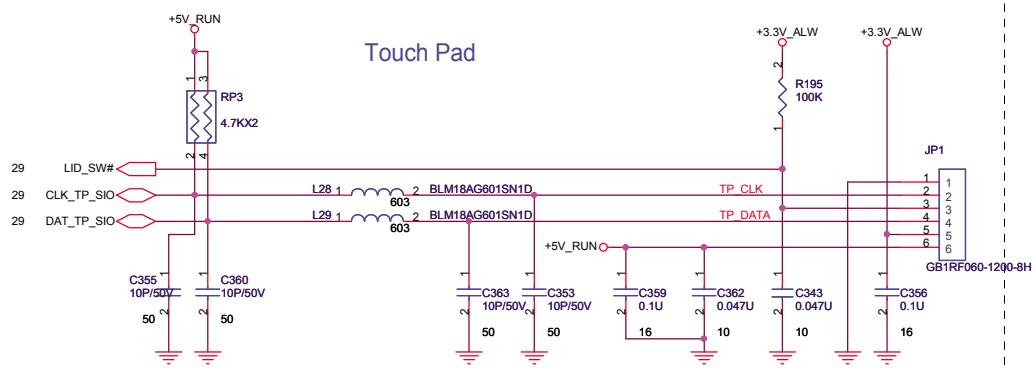
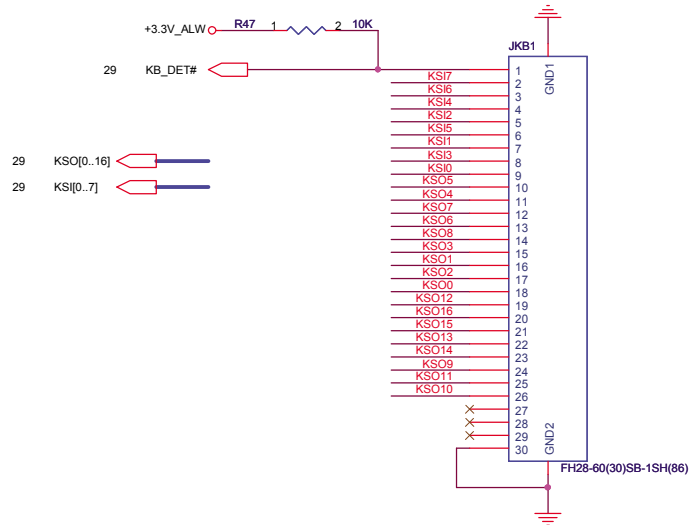
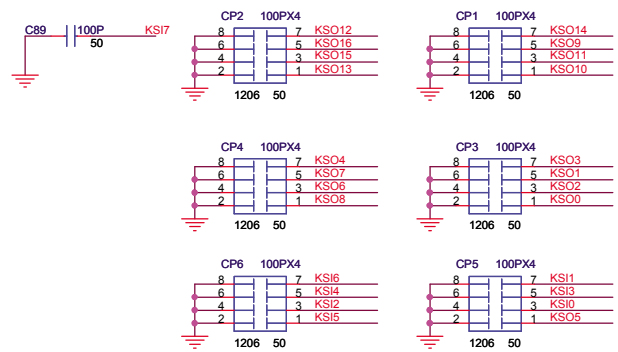
Touch Pad



KEYBOARD CONNECTOR

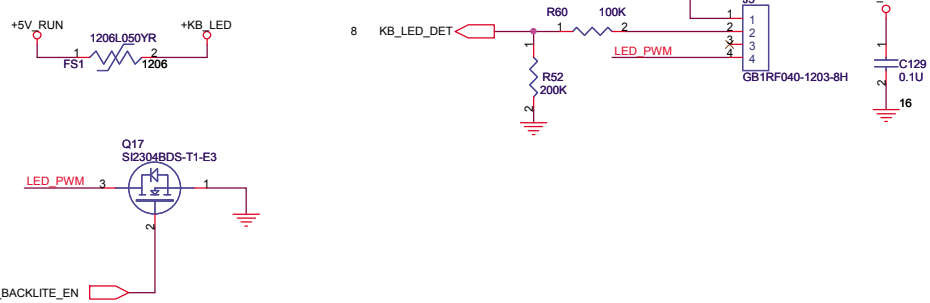




100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil



QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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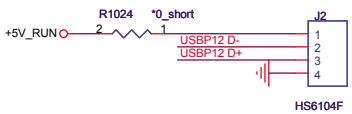
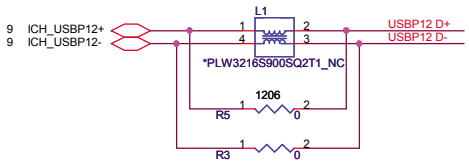
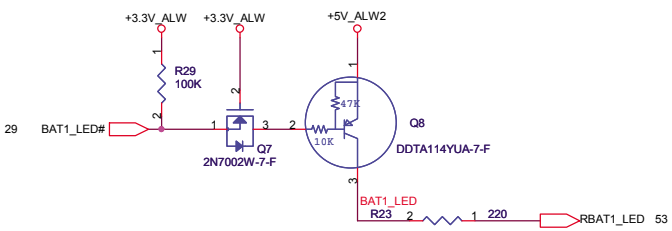
Touch Screen Module

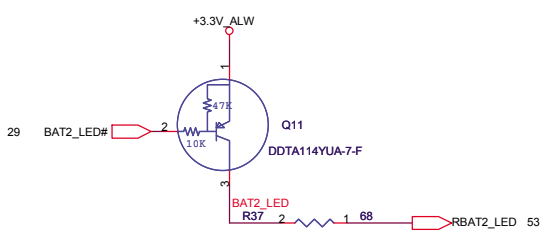
Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

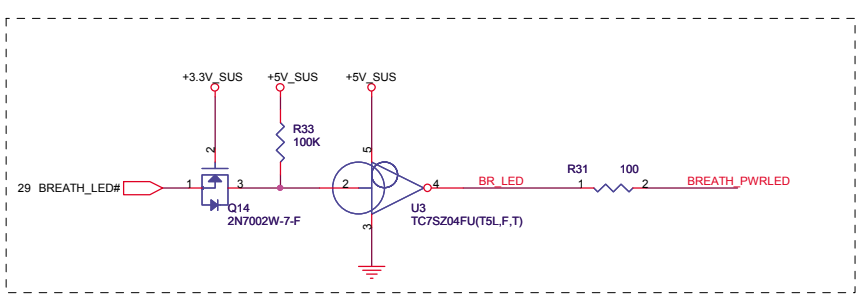




Battery status.

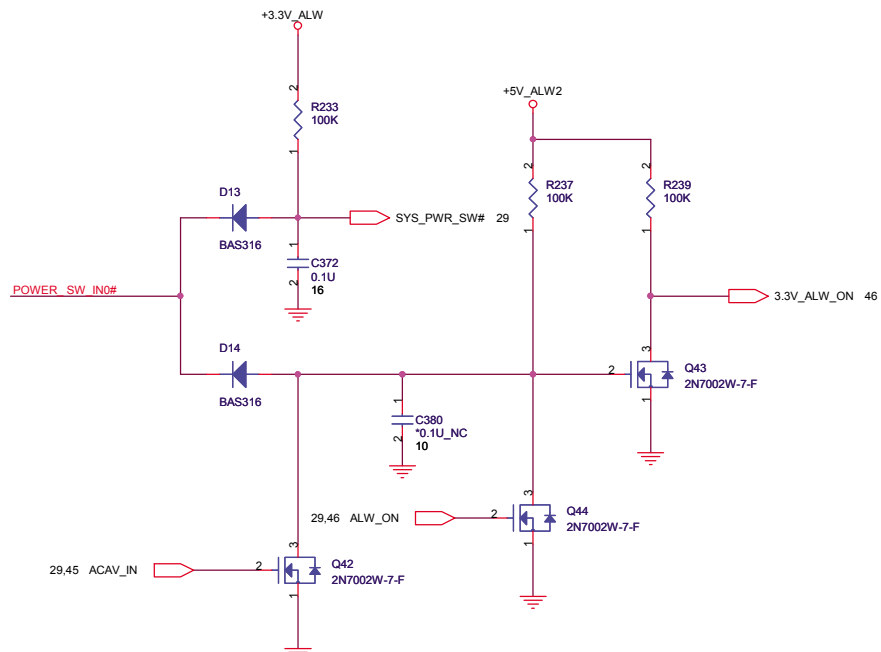


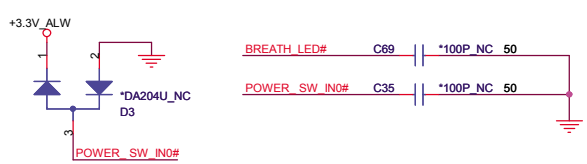




Power button Cable

3VALW ON POWER LOGIC





QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9	Rev 3B
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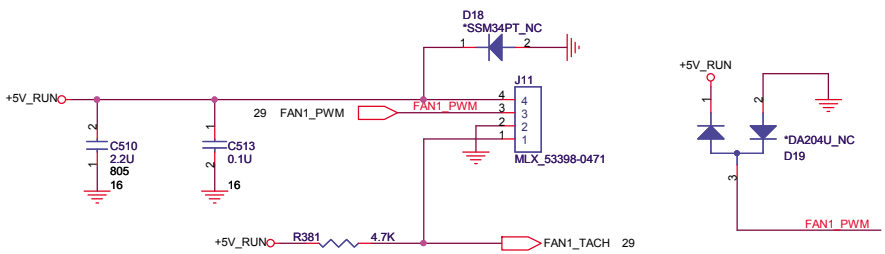

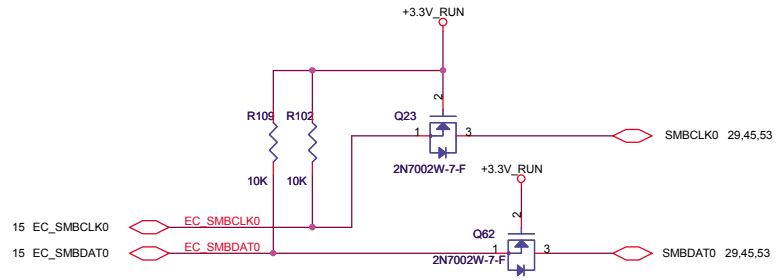

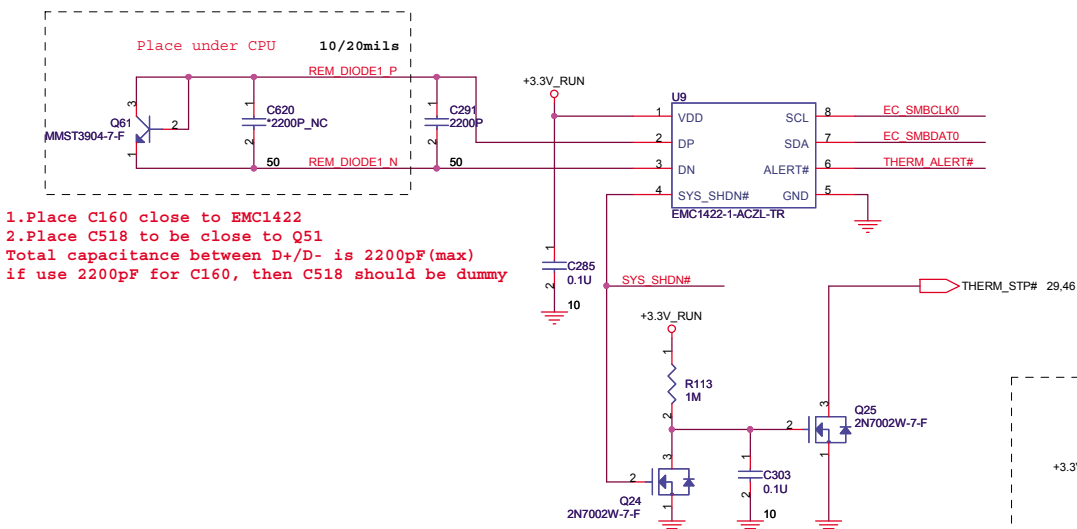

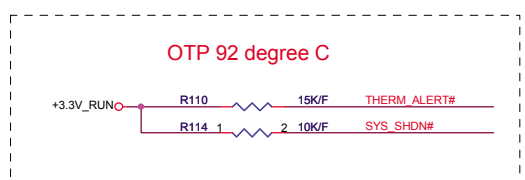

QUANTA COMPUTER

Title	FAN & THERMAL	
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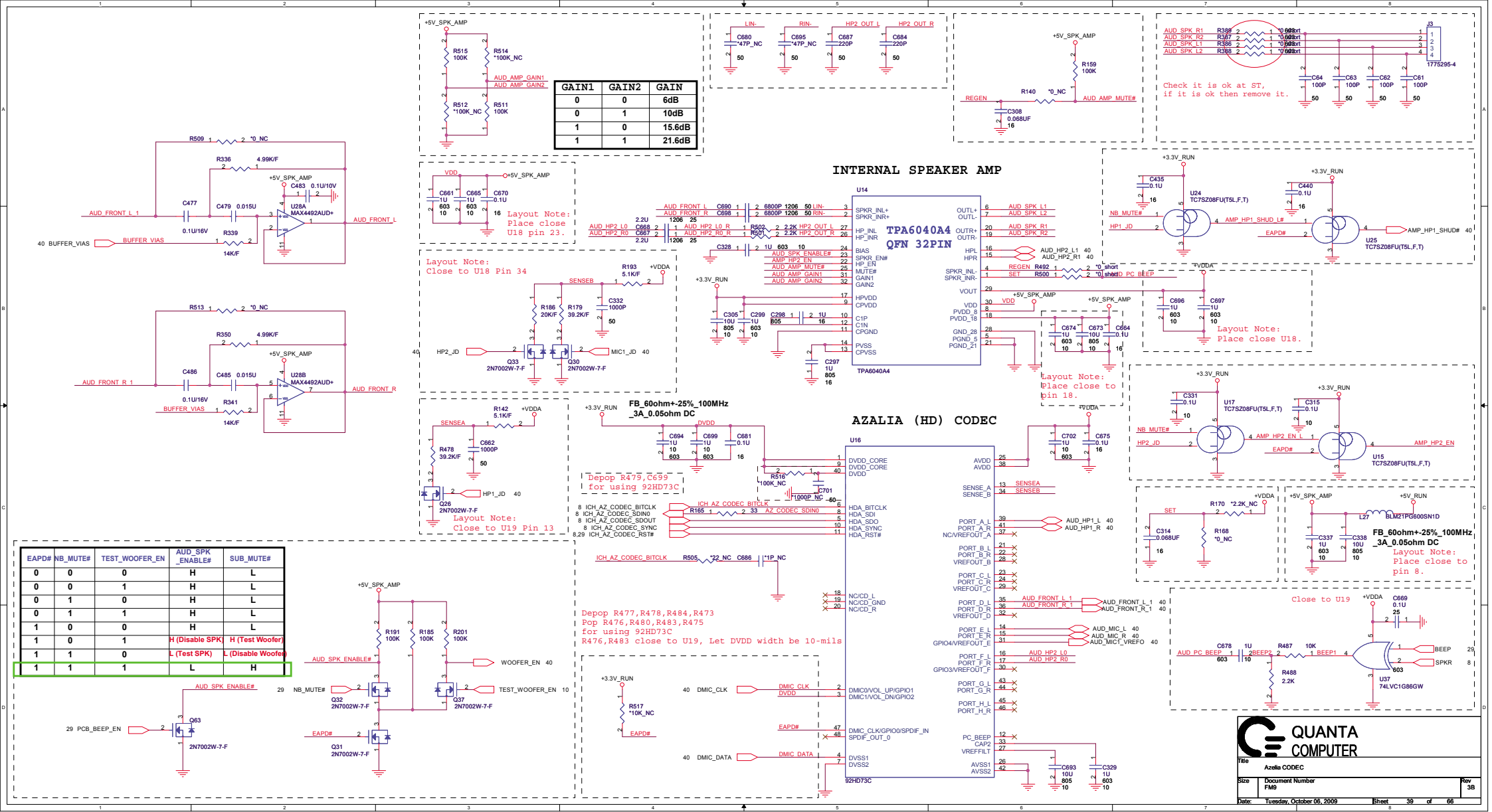
+5V_SPK_AMP
R515 100K
R514 *100K_NC
AUD_AMP_GAIN1
AUD_AMP_GAIN2
R512 *100K_NC
R511 100K
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
LIN- RIN- HP2_OUT_L HP2_OUT_R
C680 *47P_NC
C695 *47P_NC
C687 220P
C684 220P
+5V_SPK_AMP
R159 100K
REGEN
R140 *0_NC
AUD_AMP_MUTE#
C308 0.068UF
AUD_SPK_R1
AUD_SPK_R2
AUD_SPK_L1
AUD_SPK_L2
R388
R387
R386
R385
*0_short
J3
1775295-4
C64 100P
C63 100P
C62 100P
C61 100P
Check it is ok at ST,
if it is ok then remove it.
INTERNAL SPEAKER AMP
U14
TPA6040A4
QFN 32PIN
AUD_FRONT_L
AUD_FRONT_R
AUD_HP2_L0
AUD_HP2_R0
HP2_OUT_L
HP2_OUT_R
AUD_SPK_ENABLE#
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2
LIN-
RIN-
AUD_SPK_L1
AUD_SPK_L2
AUD_SPK_R1
AUD_SPK_R2
AUD_HP2_L1
AUD_HP2_R1
REGEN
SET
R492 *0_short
R500 *0_short
AUD_PC_BEEP
C305 10U
C299 1U
C298 1U
C297 1U
C674 1U
C673 10U
C664 0.1U
C696 1U
C697 1U
Layout Note:
Place close to U18 pin 23.
Layout Note:
Close to U18 Pin 34
Layout Note:
Place close to pin 18.
Layout Note:
Place close U18.
+3.3V_RUN
U24
TC7SZ08FU(T5L,F,T)
U25
TC7SZ08FU(T5L,F,T)
NB_MUTE#
HP1_JD
AMP_HP1_SHUD#
AMP_HP1_SHUD_L#
EAPD#
C435 0.1U
C440 0.1U
R509 *0_NC
R336 4.99K/F
C477 0.1U/16V
C479 0.015U
C483 0.1U/10V
U28A MAX4492AUD+
R339 14K/F
40 BUFFER_VIAS
BUFFER_VIAS
R513 *0_NC
R350 4.99K/F
C486 0.1U/16V
C485 0.015U
U28B MAX4492AUD+
R341 14K/F
R193 5.1K/F
+VDDA
SENSEB
R186 20K/F
R179 39.2K/F
C332 1000P
HP2_JD
MIC1_JD
Q33 2N7002W-7-F
Q30 2N7002W-7-F
R142 5.1K/F
SENSEA
R478 39.2K/F
C662 1000P
HP1_JD
Q26 2N7002W-7-F
FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
DVDD
C694 1U
C699 1U
C681 0.1U
Depop R479,C699
for using 92HD73C
R516 100K_NC
C701 *1000P_NC
AZALIA (HD) CODEC
U16
92HD73C
ICH_AZ_CODEC_BITCLK
ICH_AZ_CODEC_SDIN0
ICH_AZ_CODEC_SDOUT
ICH_AZ_CODEC_SYNC
ICH_AZ_CODEC_RST#
R165 33
R505 *22_NC
C686 *1P_NC
DVDD_CORE
DVDD
AVDD
SENSE_A
SENSE_B
SENSEA
SENSEB
PORT_A_L
PORT_A_R
NC/VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORT_E_L
PORT_E_R
GPIO4/VREFOUT_E
PORT_F_L
PORT_F_R
GPIO3/VREFOUT_F
PORT_G_L
PORT_G_R
PORT_H_L
PORT_H_R
NC/CD_L
NC/CD_GND
NC/CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2
DMIC0/VOL_UP/GPIO1
DMIC1/VOL_DN/GPIO2
DMIC_CLK/GPIO0/SPDIF_IN
SPDIF_OUT_0
DVSS1
DVSS2
AUD_HP1_L
AUD_HP1_R
AUD_MIC_L
AUD_MIC_R
AUD_MIC1_VREFO
AUD_FRONT_L_1
AUD_FRONT_R_1
C702 1U
C675 0.1U
C693 10U
C329 1U
Depop R477,R478,R484,R473
Pop R476,R480,R483,R475
for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils
R517 *10K_NC
DMIC_CLK
DMIC_DATA
U17
TC7SZ08FU(T5L,F,T)
U15
TC7SZ08FU(T5L,F,T)
AMP_HP2_EN_L
AMP_HP2_EN
C331 0.1U
C315 0.1U
R170 *2.2K_NC
C314 0.068UF
R168 *0_NC
L27
BLM21PG600SN1D
C337 1U
C338 10U
FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
Layout Note:
Place close to pin 8.
Close to U19
C669 0.1U
C678 1U
R487 10K
R488 2.2K
BEEP1
BEEP
SPKR
U37
74LVC1G86GW
EAPD# AUD_SPK_ENABLE# BUFFER_VIAS AUD_SPK_ENABLE# AUD_HP2_L0 AUD_HP2_R0 AUD_HP1_L AUD_HP1_R AUD_FRONT_L_1 AUD_FRONT_R_1 AUD_MIC_L AUD_MIC_R AUD_MIC1_VREFO
EAPD# NB_MUTE# HP2_JD AMP_HP2_EN_L AMP_HP2_EN EAPD# AUD_SPK_ENABLE# PCB_BEEP_EN NB_MUTE# EAPD# DMIC_CLK DMIC_DATA
EAPD# NB_MUTE# SUB_MUTE# AUD_SPK_ENABLE#
0 0 0 H L
0 0 1 H L
0 1 0 H L
0 1 1 H L
1 0 0 H L
1 0 1 H (Disable SPK) H (Test Woofer)
1 1 0 L (Test SPK) L (Disable Woofer)
1 1 1 L H
R191 100K
R185 100K
R201 100K
WOOFER_EN
TEST_WOOFER_EN
Q32 2N7002W-7-F
Q37 2N7002W-7-F
Q31 2N7002W-7-F
Q63 2N7002W-7-F
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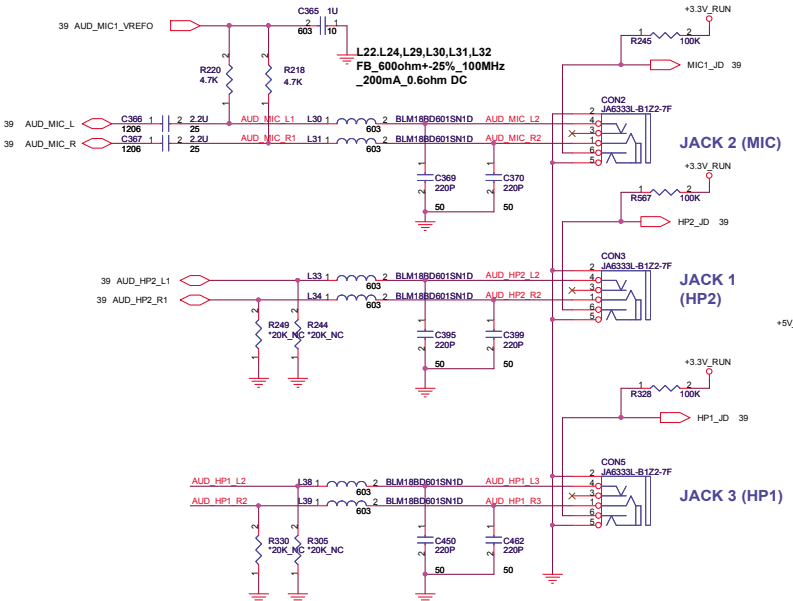
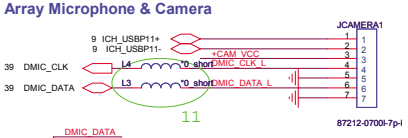
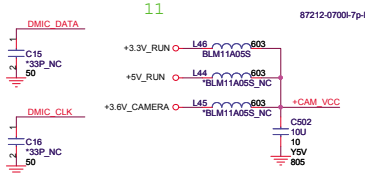
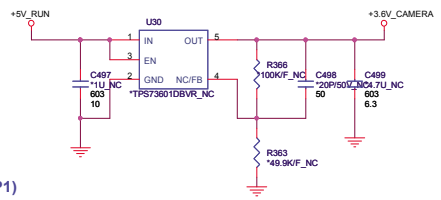
Headphone Jack
Stereo MIC Jack

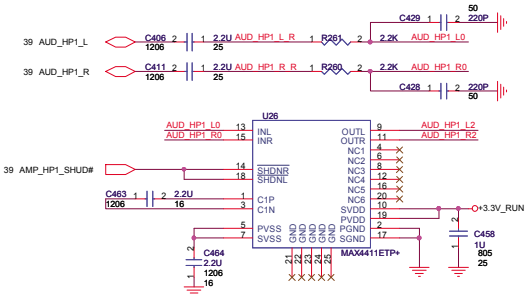


Array Microphone & Camera

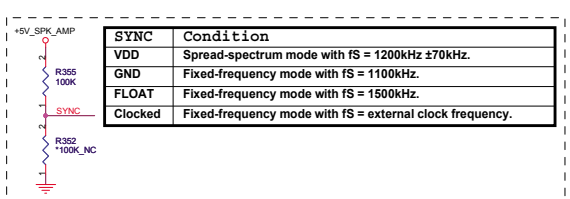






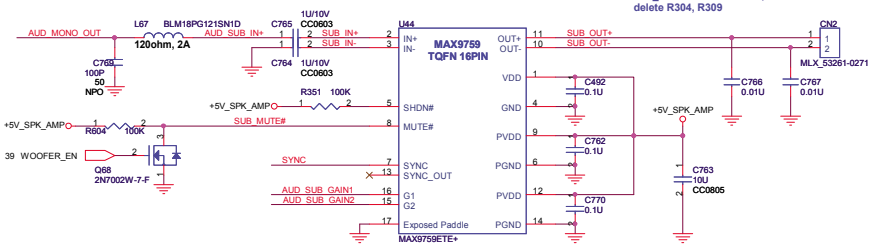


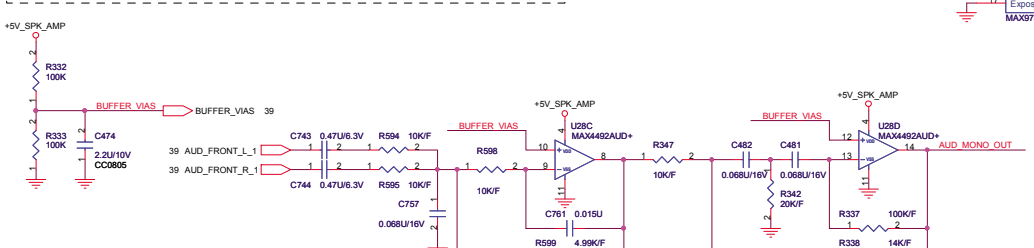
INTERNAL SUBWOOFER AMP

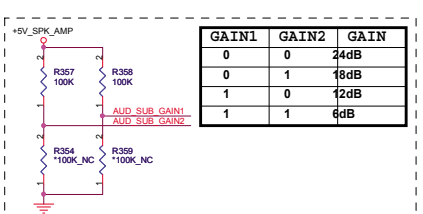


SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

Gur_0808: 0 ohm removal, delete R304, R309



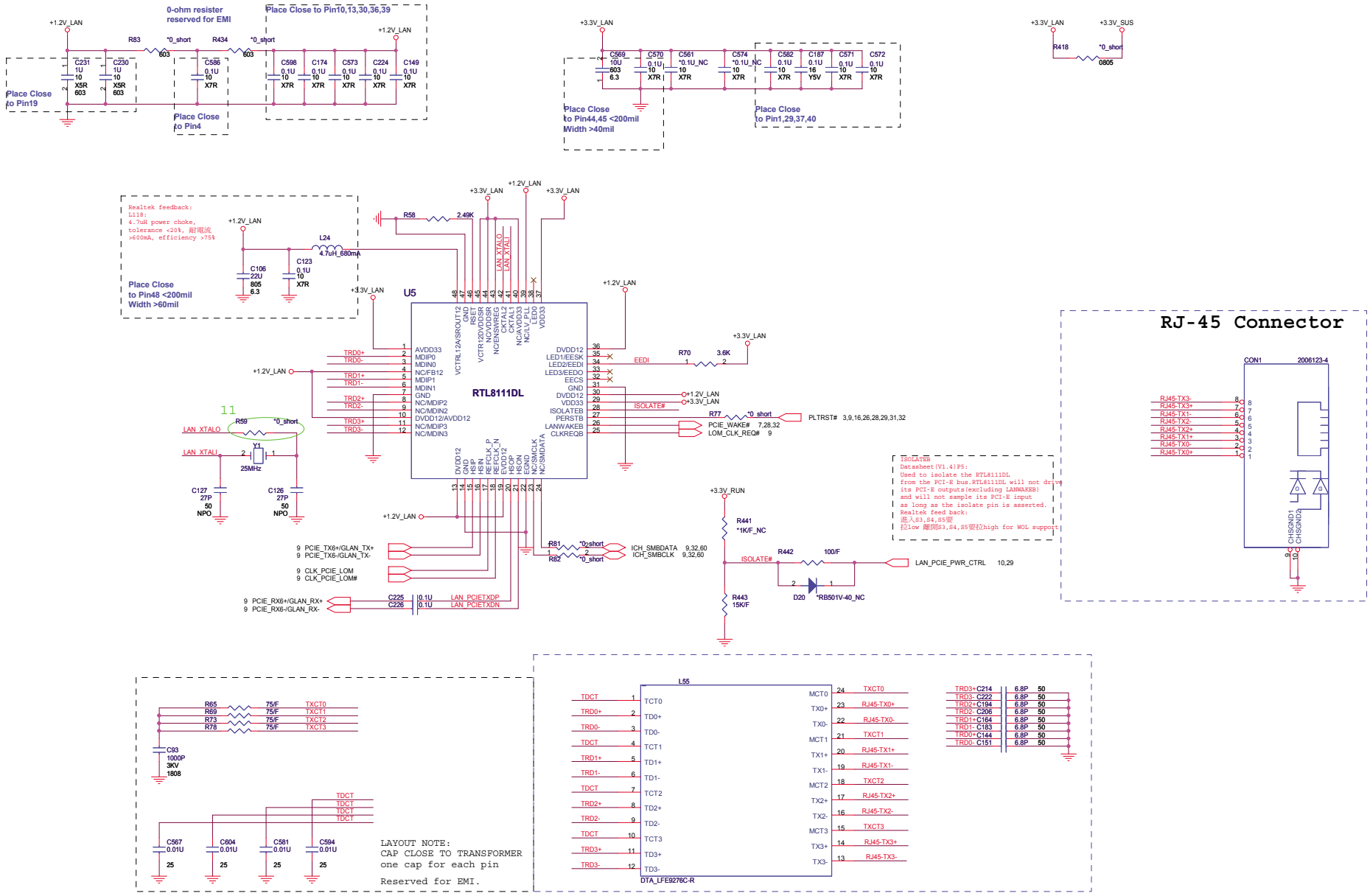


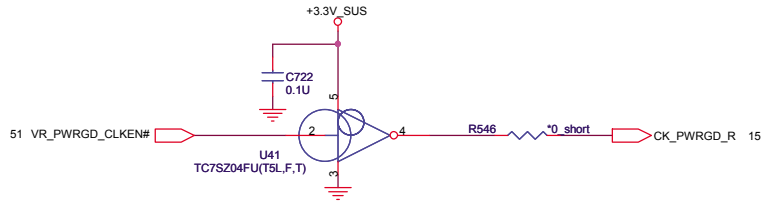


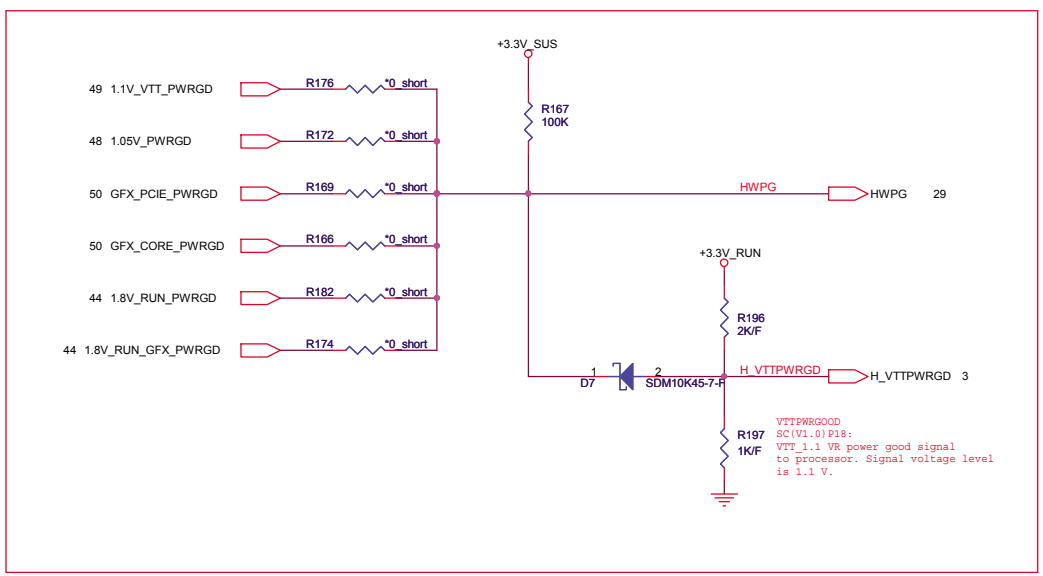
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

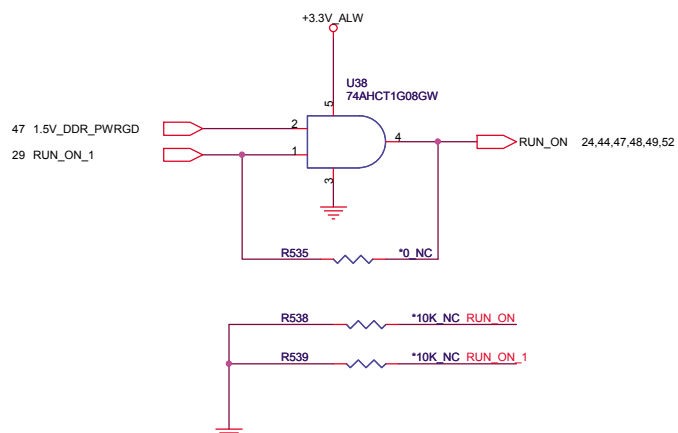
QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 40 of 66	


0-ohm resister reserved for EMI
Place Close to Pin10,13,30,36,39
Place Close to Pin19
Place Close to Pin4
Place Close to Pin44,45 <200mil Width >40mil
Place Close to Pin1,29,37,40
Realtek feedback: L118: 4.7uH power choke, tolerance <20%, 耐電流 >600mA, efficiency >75%
Place Close to Pin48 <200mil Width >60mil
U5
RTL8111DL
RJ-45 Connector
CON1
2006123-4
ISOLATEB Datasheet(V1.4)P5: Used to isolate the RTL8111DL from the PCI-E bus.RTL8111DL will not drive its PCI-E outputs(excluding LANWAKEB) and will not sample its PCI-E input as long as the isolate pin is asserted. Realtek feed back: 進入S3,S4,S5要拉high for WOL support 拉low 關閉S3,S4,S5要拉high for WOL support
LAYOUT NOTE: CAP CLOSE TO TRANSFORMER one cap for each pin
Reserved for EMI.
L55
DTA_LFE9276C-R
QUANTA COMPUTER
Title LAN
Size Document Number FM9 Rev 3B
Date: Tuesday, October 06, 2009 Sheet 41 of 66





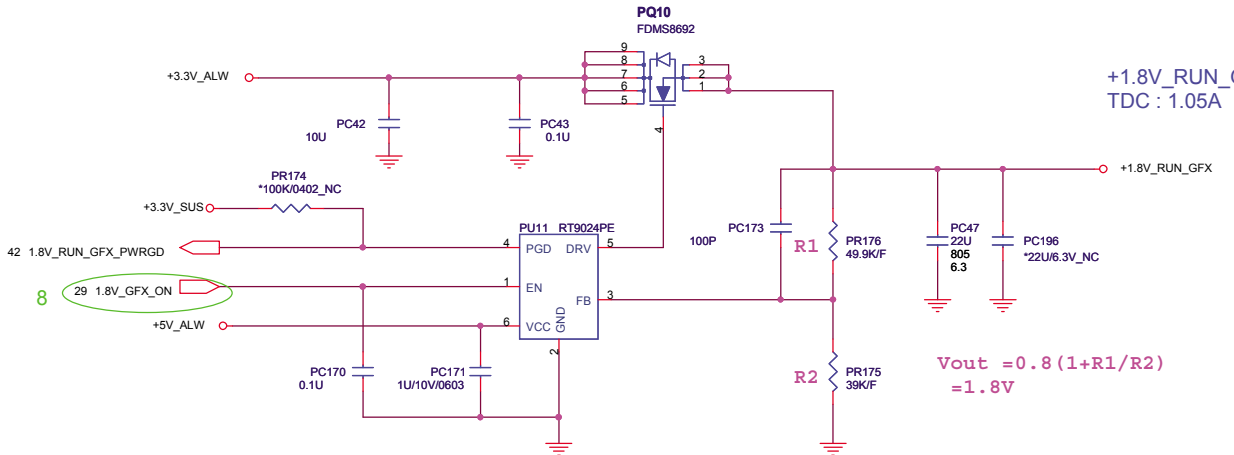


QUANTA COMPUTER

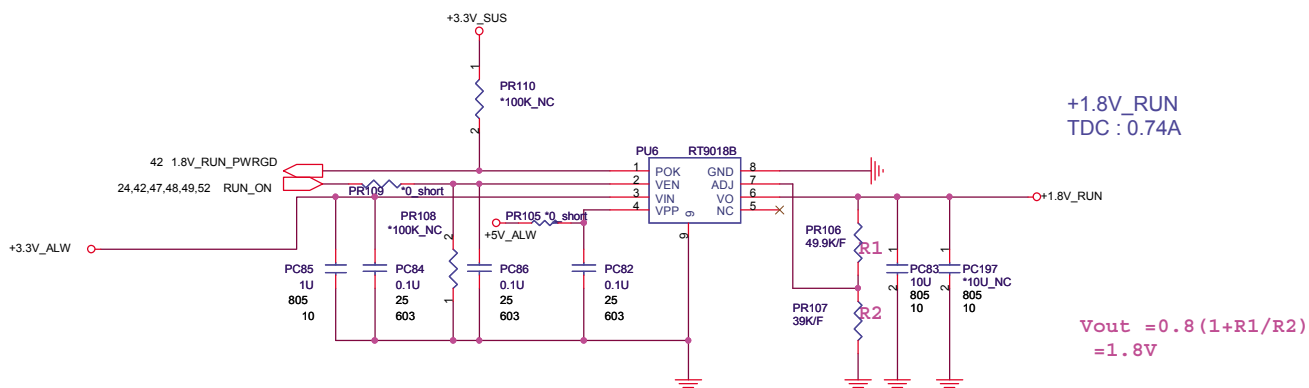
Title	System Reset Circuit	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 42 of 66	

QUANTA COMPUTER

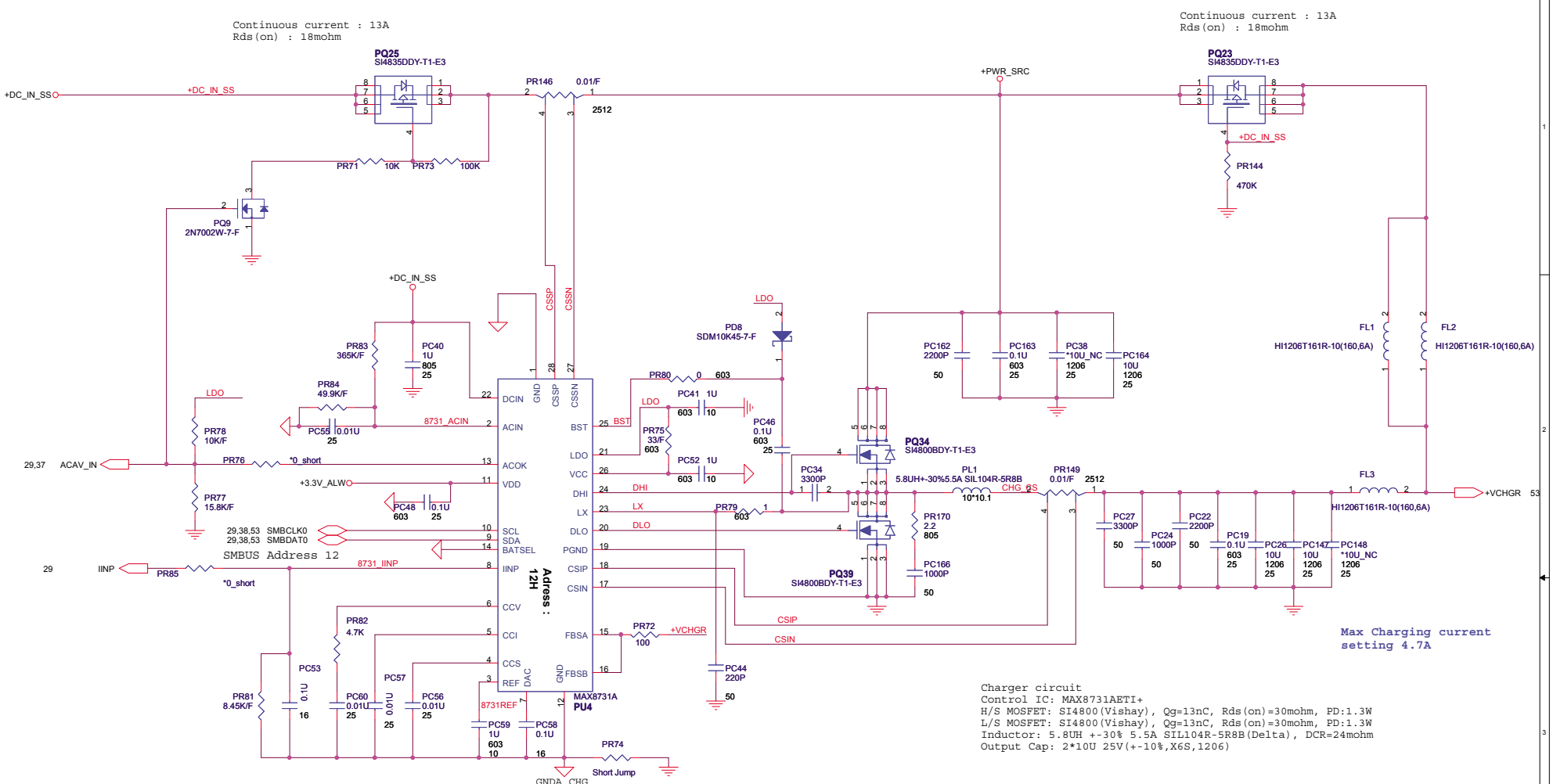
Title	Battery Selector	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 43 of 66	



+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title	+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 44 of 66	



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 45 of 66	

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 1.5U20%17.1A(FDVE1040-H-1R5M=P3)(TOKO), DCR=4.6mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

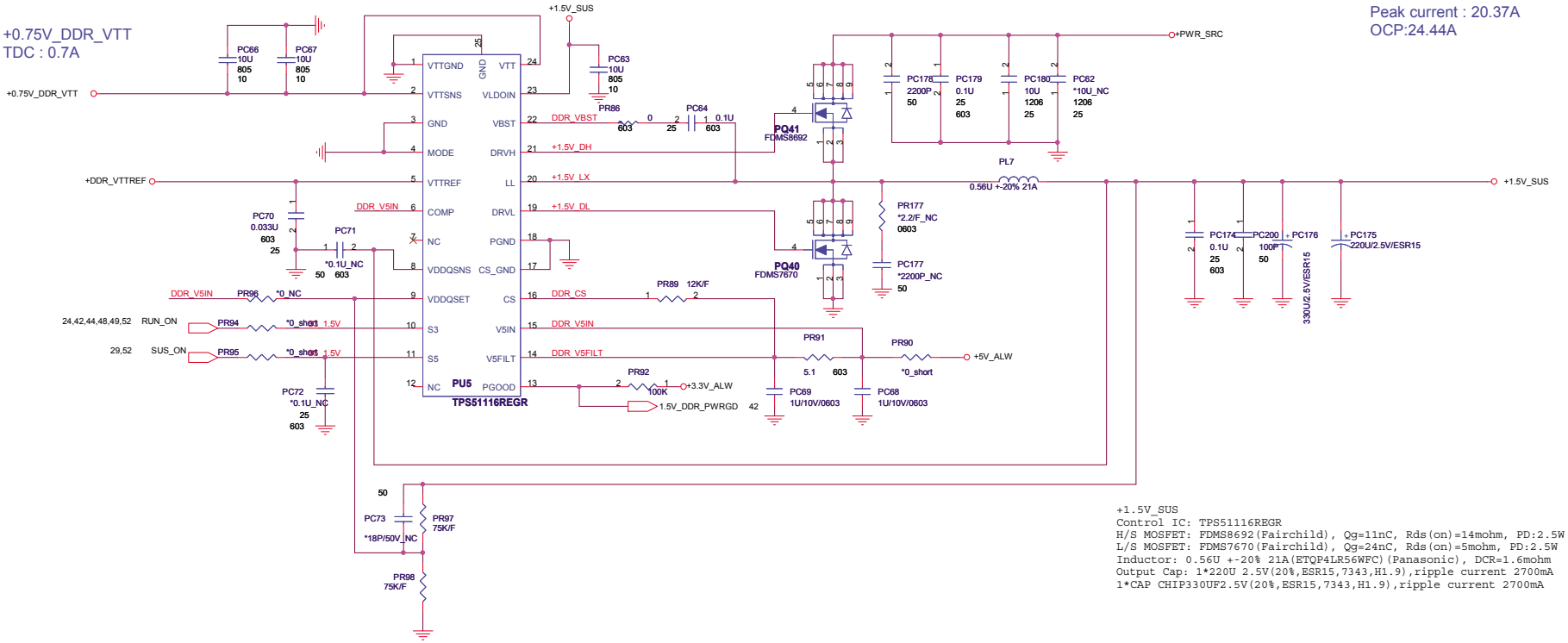
+3.3V_ALW
Fs=300K
TDC : 8.23A
Peak : 11.77A
OCP:14A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 46 of 66	



+1.5V_SUS
Control IC: TPS51116REGR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 1*220U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA
1*CAP CHIP330UF2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

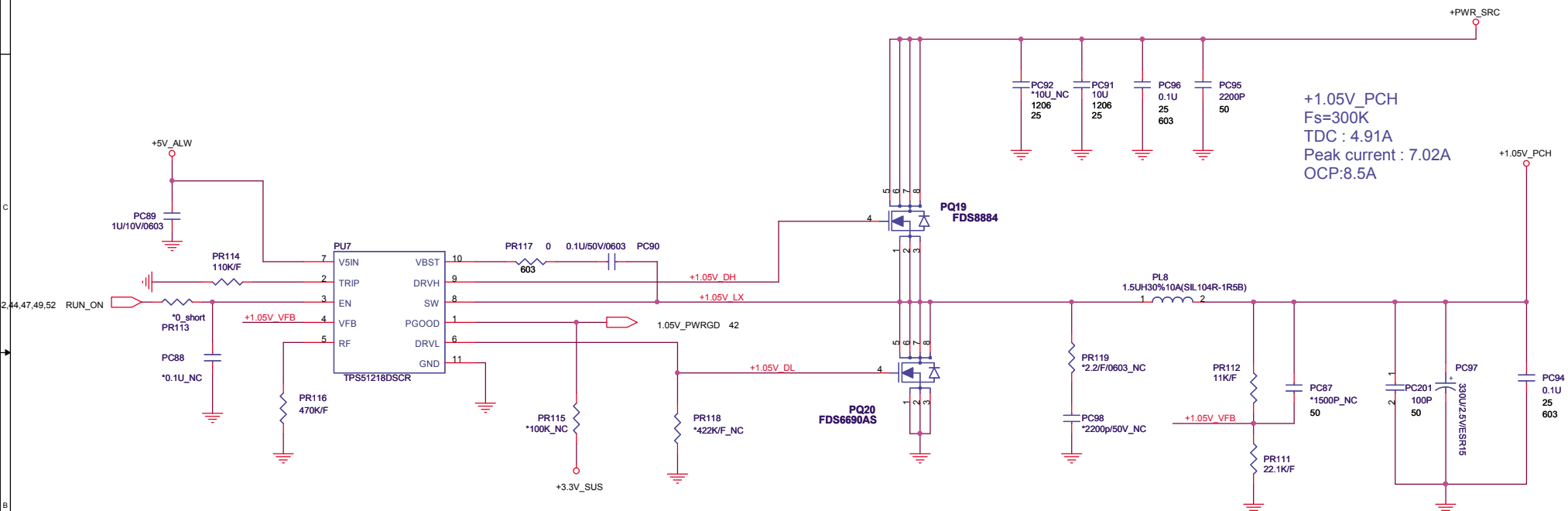
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)		
Size	Document Number FM9		Rev 3B
Date:	Tuesday, October 06, 2009	Sheet 47 of 66	

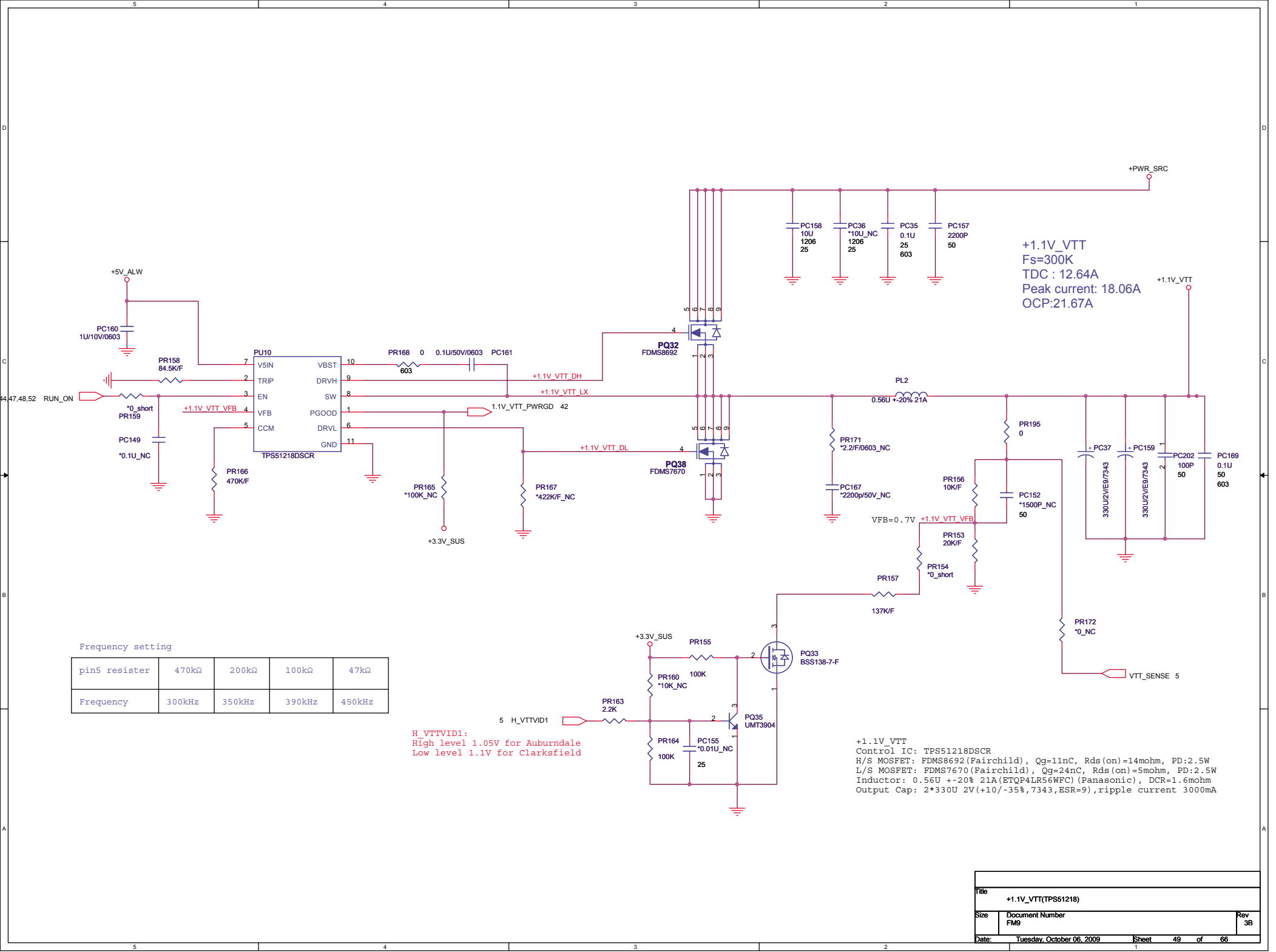


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 48 of 66	



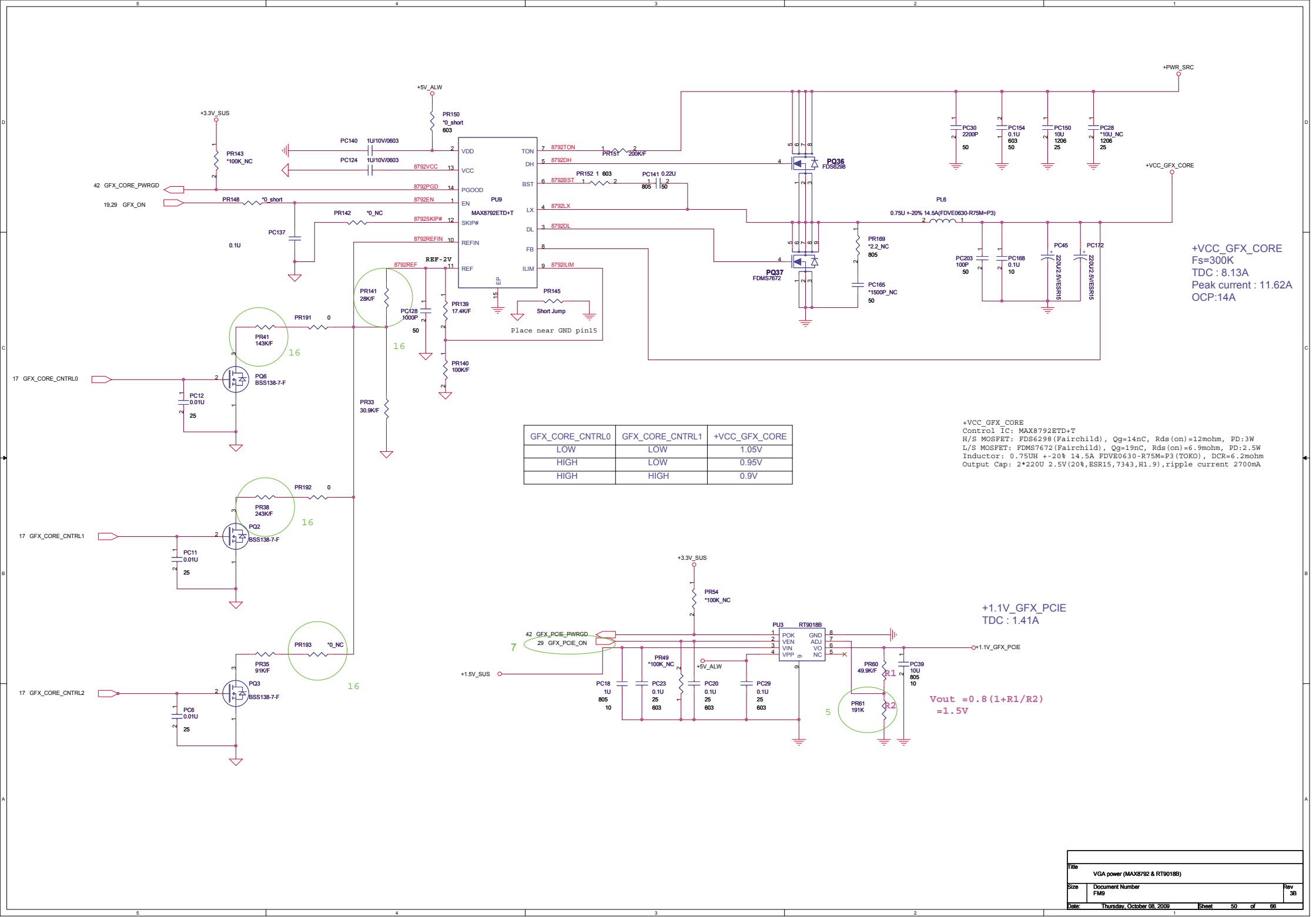
Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

H_VTTVID1:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

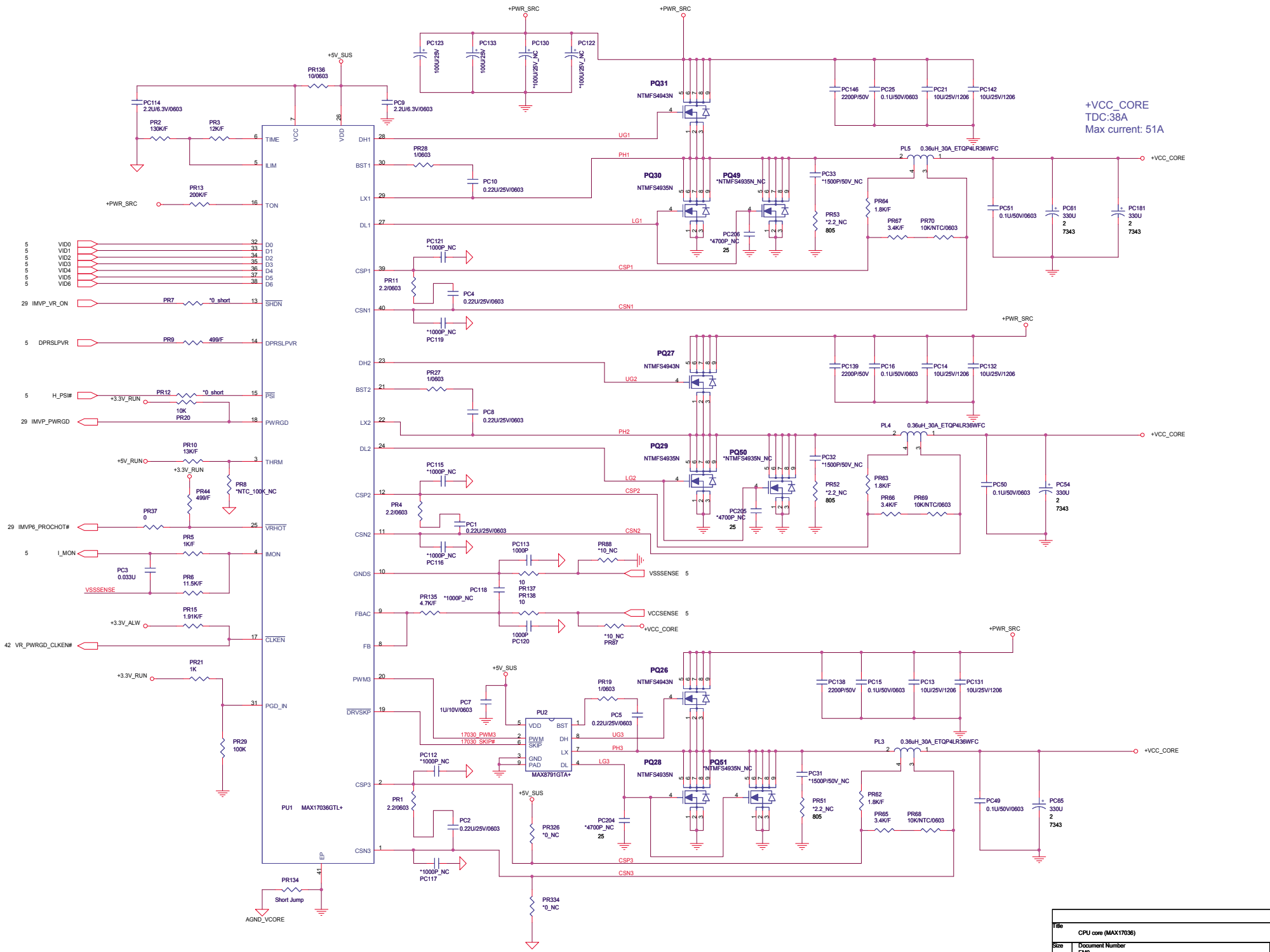
+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

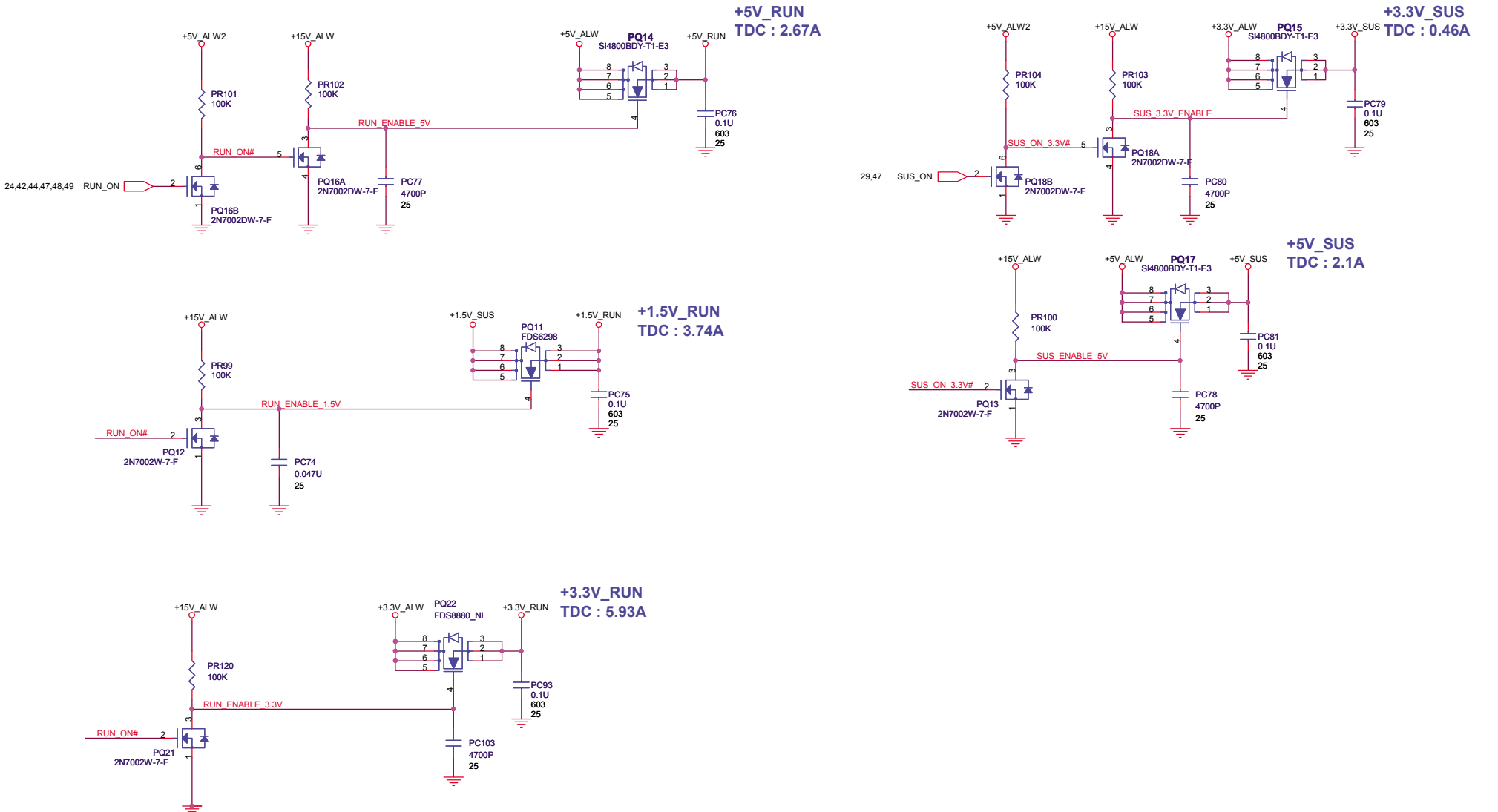
Title	+1.1V_VTT(TPS51218)		
Size	Document Number FM9		Rev 3B
Date: Tuesday, October 06, 2009		Sheet 49 of 66	



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	1.05V
HIGH	LOW	0.95V
HIGH	HIGH	0.9V

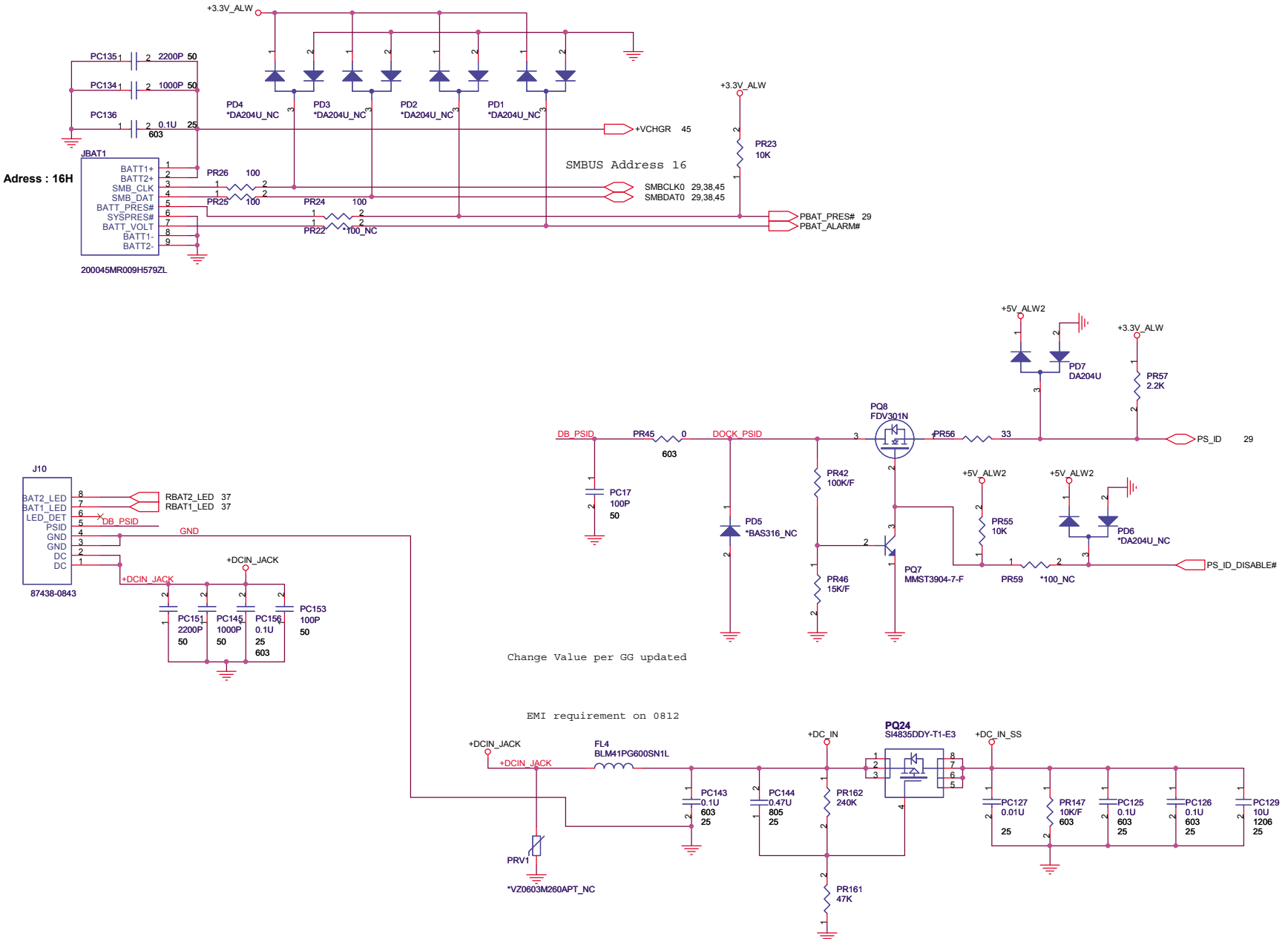
Title	VGA power (MAX8792 & RT9018B)	
Size	Document Number FM9	Rev 3B
Date: Thursday, October 08, 2009	Sheet 50 of 66	


+VCC_CORE
TDC:38A
Max current: 51A
PU1 MAX17036GTL+
PU2 MAX8791GTA+
PQ26 NTMFS4943N
PQ27 NTMFS4943N
PQ28 NTMFS4935N
PQ29 NTMFS4935N
PQ30 NTMFS4935N
PQ31 NTMFS4943N
PQ49 *NTMFS4935N_NC
PQ50 *NTMFS4935N_NC
PQ51 *NTMFS4935N_NC
PL3 0.36uH_30A_ETQP4LR36WFC
PL4 0.36uH_30A_ETQP4LR36WFC
PL5 0.36uH_30A_ETQP4LR36WFC
+PWR_SRC
+5V_SUS
+3.3V_RUN
+3.3V_ALW
AGND_VCORE
Short Jump
TIME
ILIM
TON
VID0
VID1
VID2
VID3
VID4
VID5
VID6
IMVP_VR_ON
DPRSLPVR
H_PSI#
IMVP_PWRGD
IMVP6_PROCHOT#
I_MON
VR_PWRGD_CLKEN#
VSSSENSE
VCCSENSE
17030_PWM3
17030_SKIP#
Title
CPU core (MAX17036)
Size
Document Number
FM9
Rev
3B
Date: Tuesday, October 06, 2009
Sheet 51 of 66



QUANTA COMPUTER

Title	RUN / SUS POWER SW	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 52 of 66	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 53 of 66	

FOR CPU use

H16 *H-C276D177P2_NC H-C276D157P2
H9 *H-C276D177P2_NC H-C276D157P2
H17 *H-C276D177P2_NC H-C276D157P2
H10 *H-C276D177P2_NC H-C276D177P2

TH1 H-TC118BC197D63P2
TH2 H-TC118BC197D63P2
For MiniCard nut use.
on 31' header

H3 *H-TC315BC394D79P2_NC H-TC315BC394D79P2
H1 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H24 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H14 *H-TC315BC335D126P2_NC h-tc315bc295d126p2

H13 *H-C256D154P2_NC H-C256D154P2
H11 *H-C256D154P2_NC H-C256D154P2
For GPU nut use.

H6 *o-o177x472d177x472n_NC o-o177x472d177x472n
H27 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H26 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H19 *h-fm8b-1_NC h-fm8b-1

H22 *H-C256D154P2_NC H-C256D154P2
H20 *H-C256D154P2_NC H-C256D154P2
For PCH nut use.

H21 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H15 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H8 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H2 *h-TC256BC315D110P2_NC h-TC256BC315D110P2

PV1 PAD138X98XH GND
PV2 PAD138X98XH GND
PV3 *PAD138X98XH_NC GND
PV4 PAD138X98XH GND

H5 *h-tc256bc315d126p2_NC h-tc315bc394d126p2

H7 *H-C228D228N_NC H-C228D228N
H4 *H-C228D228N_NC H-C228D228N
H12 *H-C197D197N_NC H-C197D197N
H25 *H-C394D394N_NC H-C394D394N
H18 *H-TC256BC315D126P2_NC H-TC256BC315D126P2

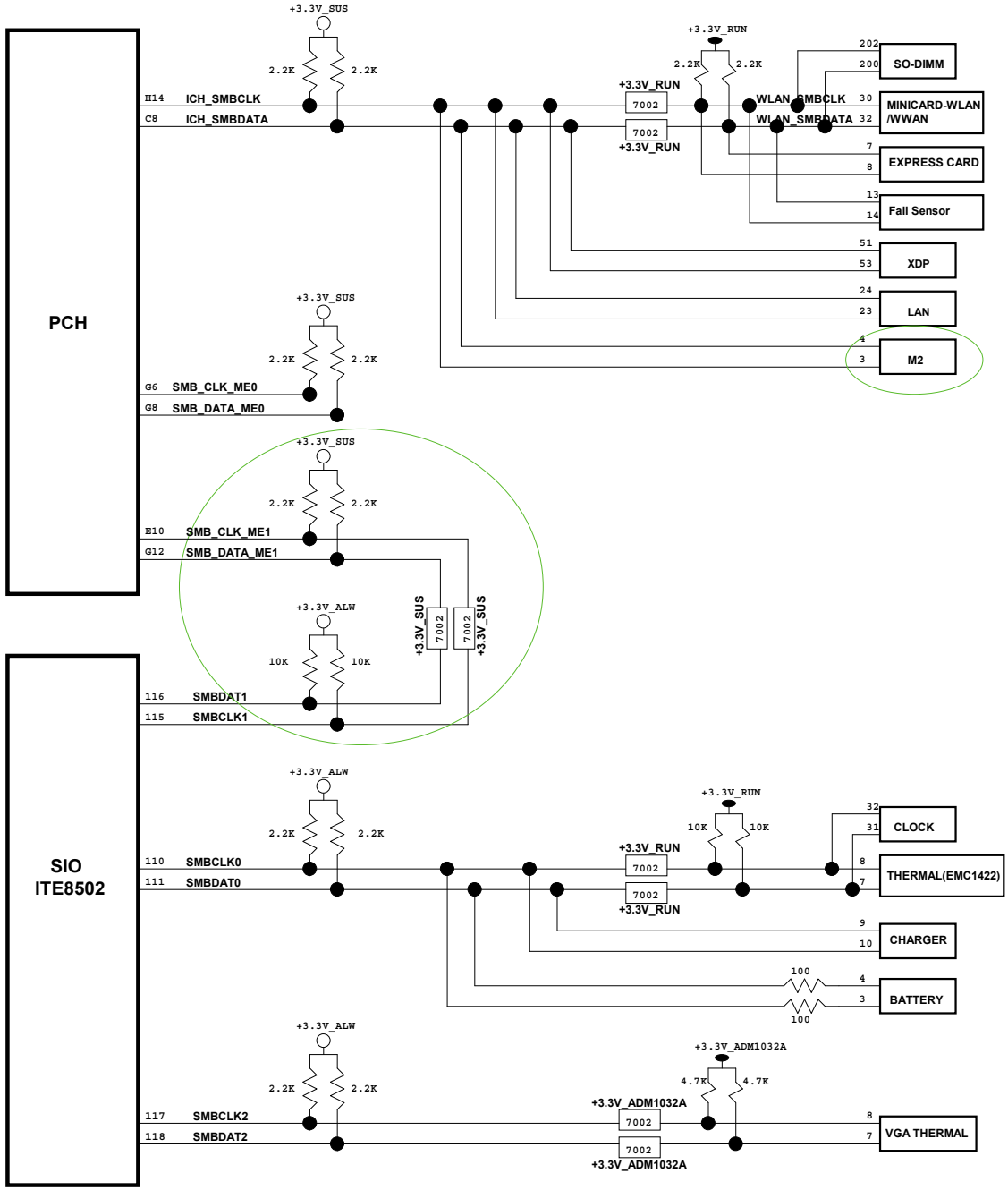
QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 54 of 66	

Reserved for EMI.

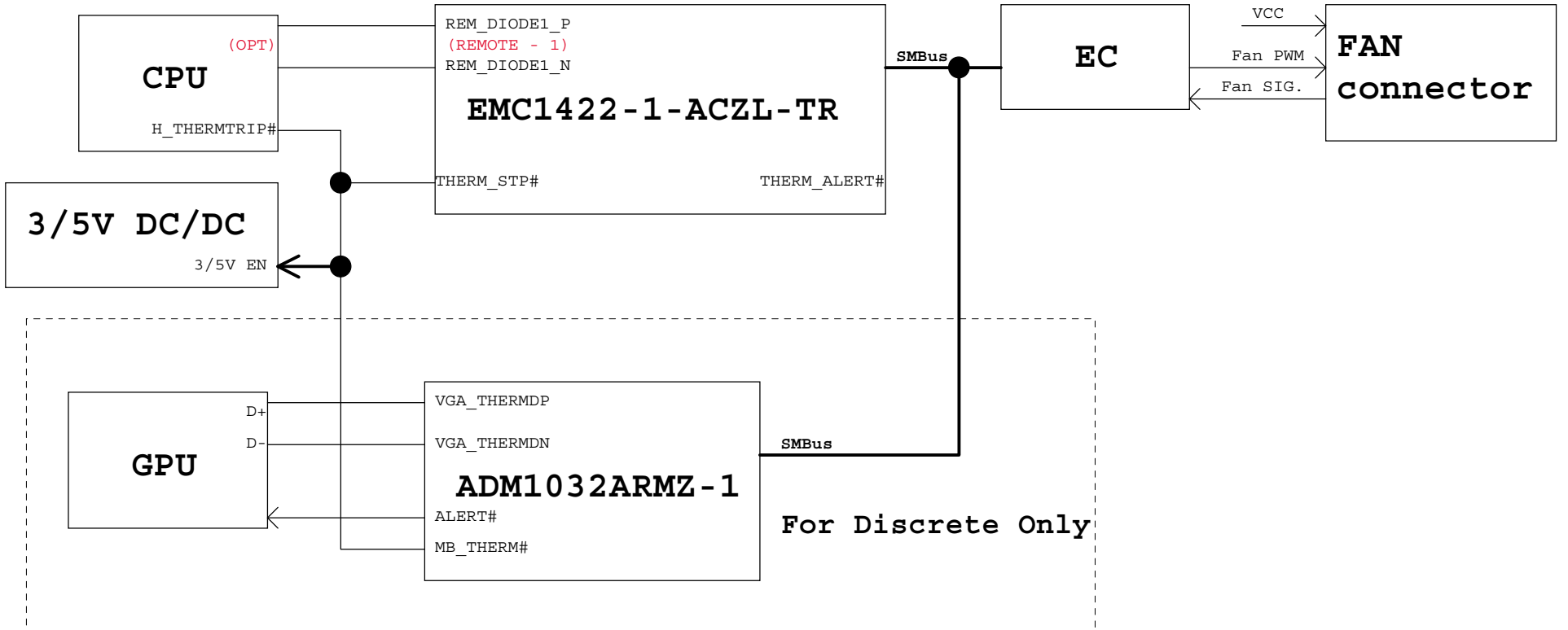
QUANTA COMPUTER

Title	EMI CAP	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 55 of 66	



QUANTA COMPUTER

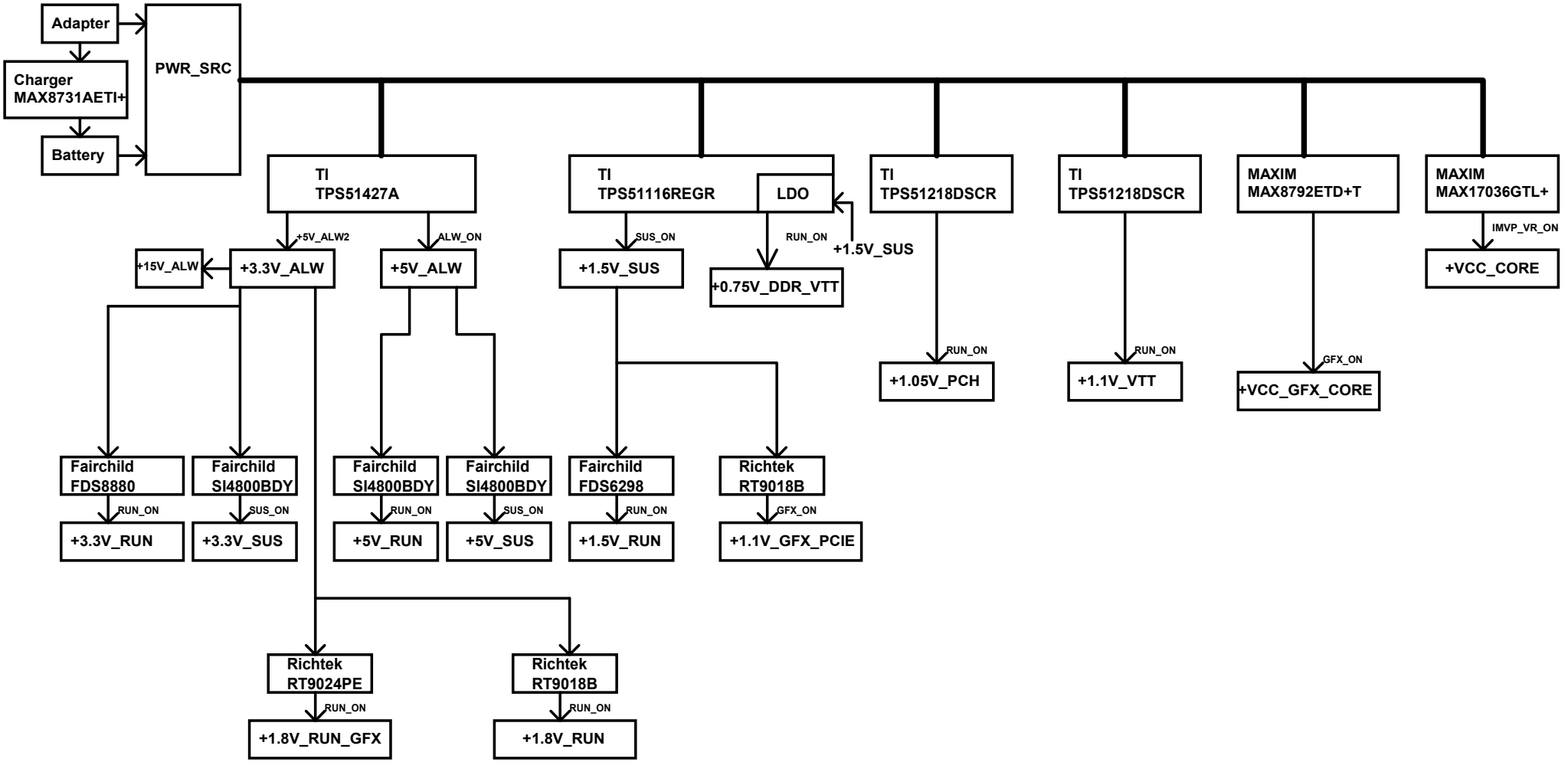
Title:	SMBUS BLOCK		
Size	Document Number FM9		Rev 3S
Date:	Tuesday, October 06, 2009	Sheet 56 of 66	



QUANTA COMPUTER

Title	Thermal Map	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 57 of 66	

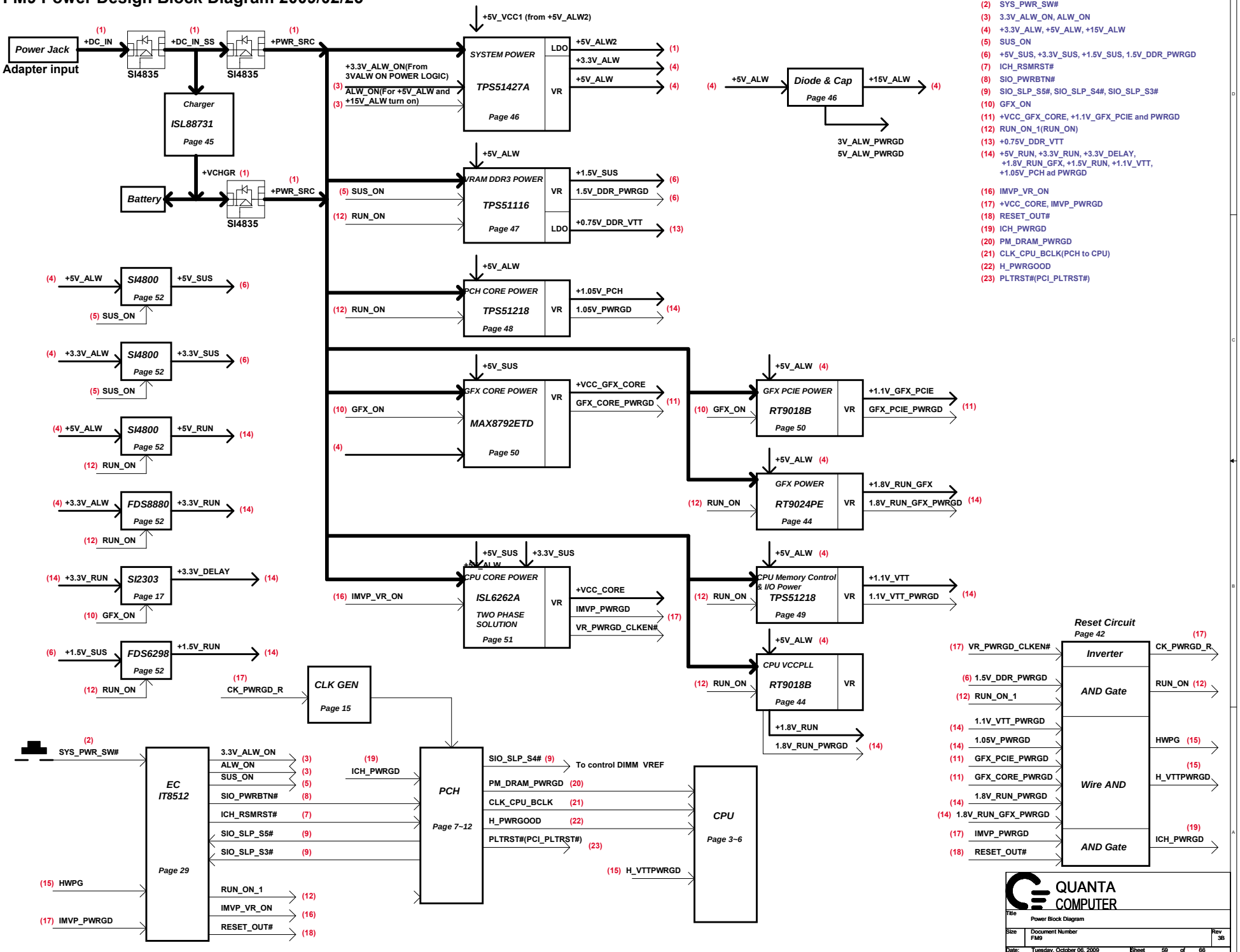
VER : 1A



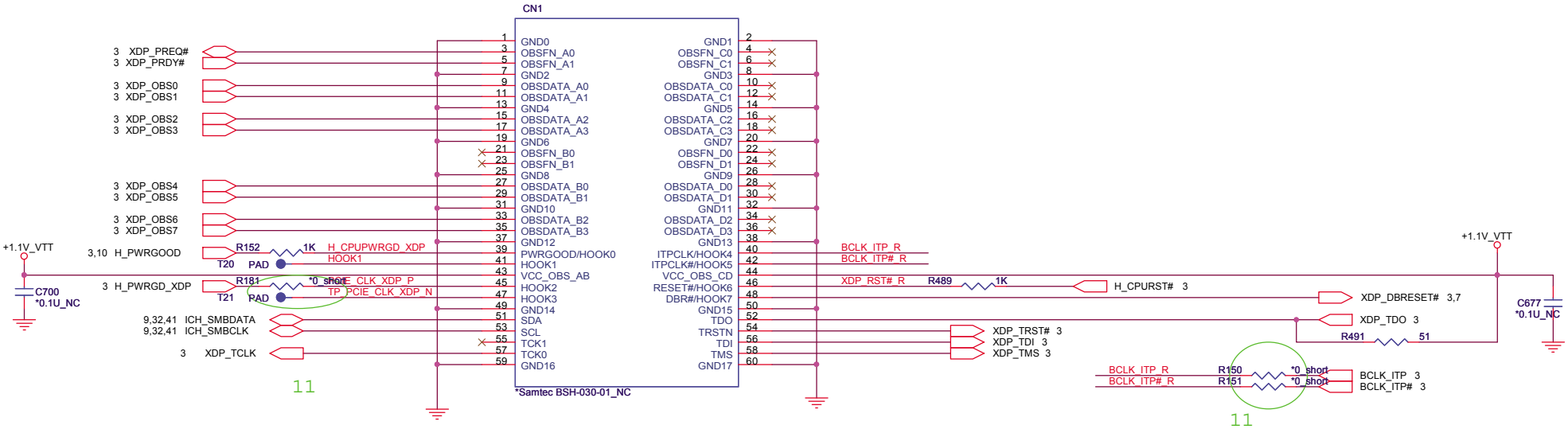
QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 58 of 66	

FM9 Power Design Block Diagram 2009/02/25



Title	Power Block Diagram		
Size	Document Number FM9		Rev 3B
Date: Tuesday, October 06, 2009		Sheet 59 of 66	



It is for debug. requesst vendeer provide 200 pcs sample.

QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FM9	Rev 3B
Date: Tuesday, October 06, 2009	Sheet 60 of 66	