MODEL NAME : VBW11
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WN000 LA-9984P M/B
DA40001FP00 LS-9102P USB/B
DA40001FR00 LS-9104P ODD/B
DA40001G400 LS-9105P POWER BUTTON/B
DA40001FQ00 LS-9106P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus XT

2013-05-17 Rev: 1.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS VENUS : VENUS@,VENUSXT@,DIS@,EMI@,ESD@,RF@,XDP@

ZZZ1 R1@

PCB VBW11 LA9984P/LS9102P/LS9104P/LS9105P/LS9106P
DA8000WN000

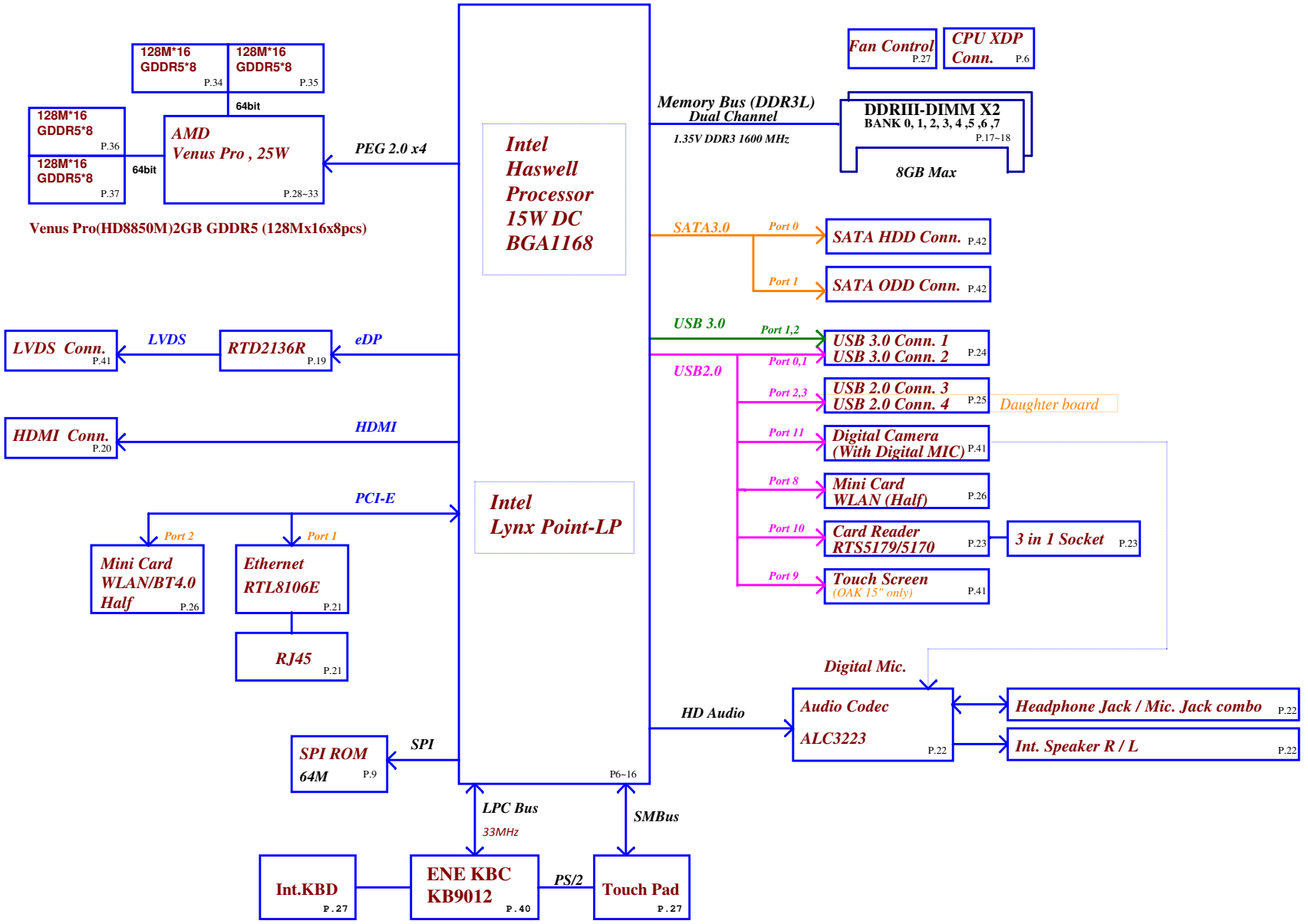
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: Cover Page

Size: Custom | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 1 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	Block diagram		
Size	Document Number		Rev
	LA-9984P		1.0
Date:	Wednesday, May 22, 2013	Sheet	2 of 57

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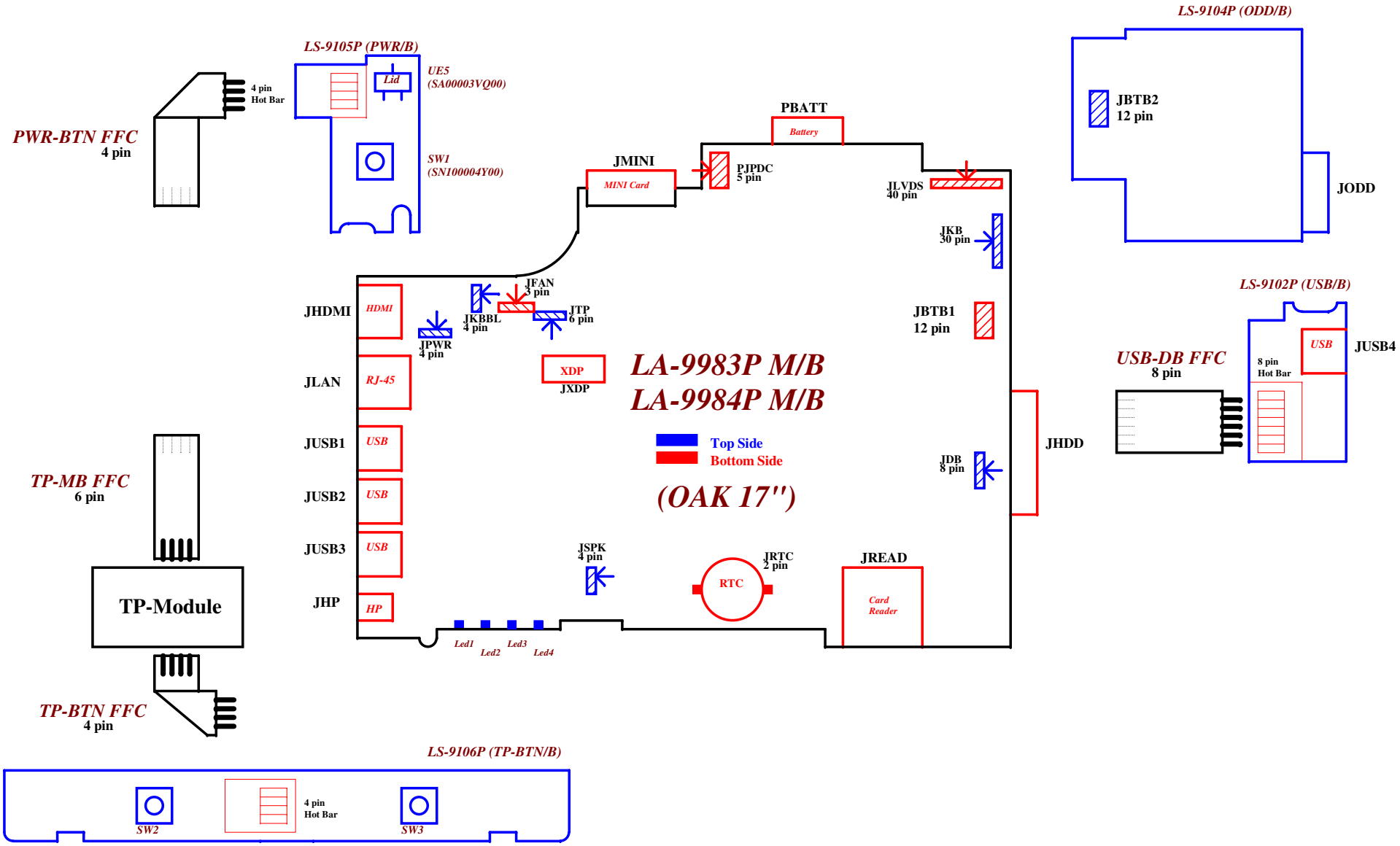
Project Code : VAW10 / VAW11
File Name : LA-9983P / LA-9984P



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	DB block diagram		
Size	Document Number	LA-9984P	Rev 1.0
Date:	Wednesday, May 22, 2013	Sheet 3 of 57	

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 – 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C – 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D – 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 – 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 – 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C – 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 – 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 – 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 – 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 – 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 – 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 – 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 – 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE – 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 – 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 – 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA – 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 – 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD – 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 – 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :

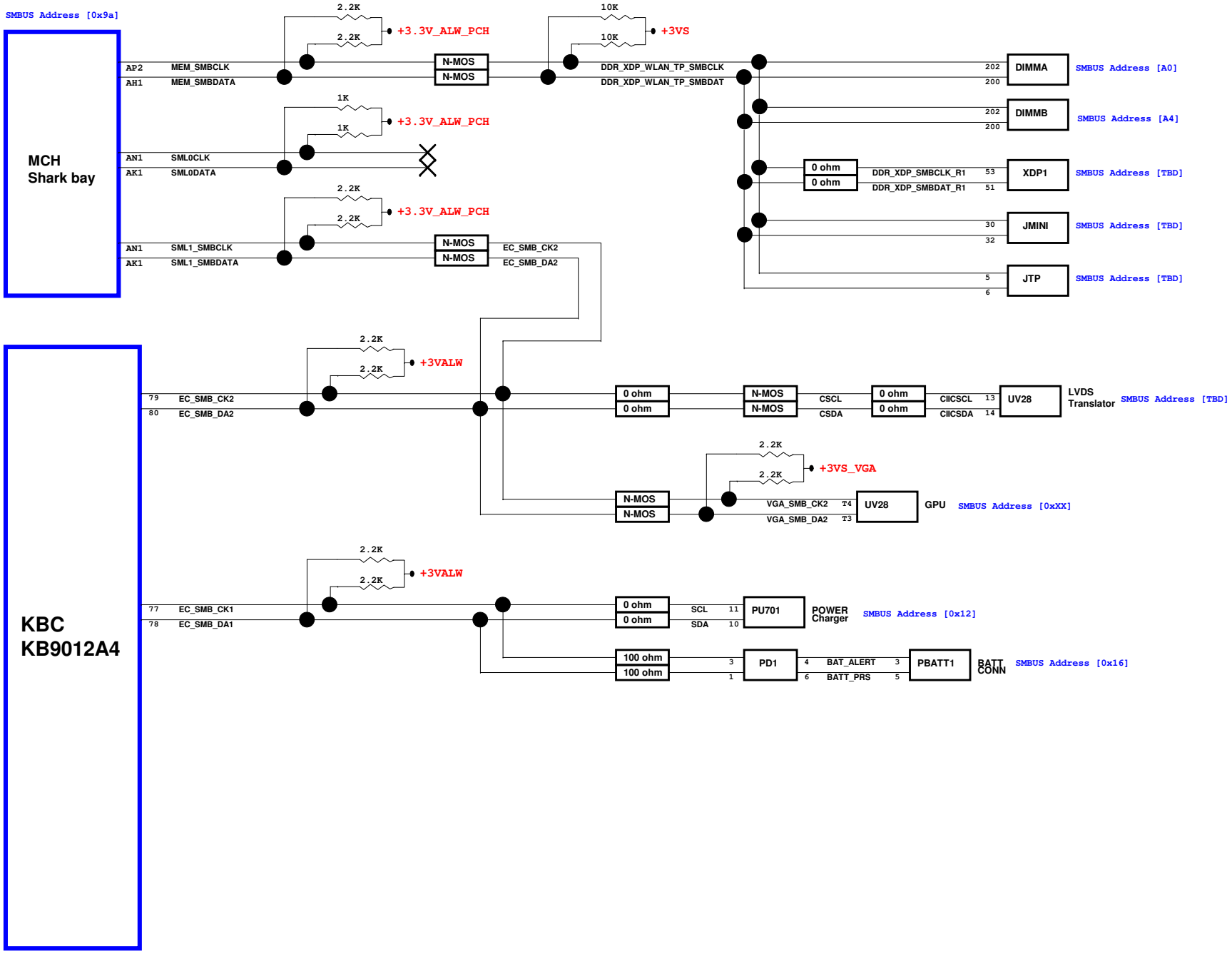
: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT		
	USB3.0	
	Port1	USB connector 2
	Port2	USB connector 1
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 2
	Port1	USB connector 1
	Port2	USB connector 3
	Port3	USB connector 4 (DB)
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (N14P)
	Lane 6	PEG (N14P)
	SATA	
	SATA0	HDD
	SATA1	ODD
	SATA2	
	SATA3	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01
Title	Notes List		
Size	Document Number		Rev
	LA-9984P		1.0
Date:	Wednesday, May 22, 2013	Sheet	4 of 57



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Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: SMBus block diagram

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 5 of 57

i3-4010U-15W-GT2-MP

UC1 4010UI3G2R1@

CL8064701478202 SR16Q C1 1.7G BGA

SA00006SX1L

UC1 4010UI3G2R3@

CL8064701478202 SR16Q C1 1.7G A31!

SA00006SX2L

i5-4200U-15W-GT2-MP

UC1 4200UI5G2R1@

CL8064701477702 SR170 C1 1.6G BGA

SA00006SM2L

UC1 4200UI5G2R3@

CL8064701477702 SR170 C1 1.6G A31!

SA00006SM3L

i7-4500U-15W-GT2-MP

UC1 4500UI7G2R1@

CL8064701477202 SR16Z C1 1.8G BGA

SA00006SL1L

UC1 4500UI7G2R3@

CL8064701477202 SR16Z C1 1.8G A31!

SA00006SL2L

UC1A HASWELL_MCP_E

DDI1_LANE_N0 C54 DDI1_TXN0
DDI1_LANE_P0 C55 DDI1_TXP0
DDI1_LANE_N1 B56 DDI1_TXN1
DDI1_LANE_P1 C58 DDI1_TXP1
DDI1_LANE_N2 B55 DDI1_TXN2
DDI1_LANE_P2 A55 DDI1_TXP2
DDI1_LANE_N3 A57 DDI1_TXN3
DDI1_LANE_P3 B57 DDI1_TXP3
C51 DDI2_TXN0
C52 DDI2_TXP0
C56 DDI2_TXN1
B53 DDI2_TXP1
C49 DDI2_TXN2
B50 DDI2_TXP2
A52 DDI2_TXN3
B52 DDI2_TXP3

DDI

EDP_TXN0 C45 EDP_CPU_LANE_N0
EDP_TXP0 B46 EDP_CPU_LANE_P0
EDP_TXN1 A47 EDP_CPU_LANE_N1
EDP_TXP1 B47 EDP_CPU_LANE_P1
EDP_TXN2 C47
EDP_TXP2 C46
EDP_TXN3 A49
EDP_TXP3 B49
EDP_AUXN A45 EDP_CPU_AUX#
EDP_AUXP B45 EDP_CPU_AUX
EDP_RCOMP D20 EDP_COMP
EDP_DISP_UTIL A43 EDP_DISP_UTIL

EDP

1 OF 19 Rev1p2

COMPENSATION PU FOR eDP

+VCCIOA_OUT — 24.9_0402_1%~D — RC71 — EDP_BIA_PWM <10,19>

@ RC72 0_0402_5%

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

UC4 @ 74CBTLV3126BQ_DHVQFN14_2P5X3

CC13 0.1U_0402_10V7K +3VS

PCH_JTAG_TDO	RC43 0_0402_1%	TDO_XDP	XDP_TDO
PCH_JTAG_TDI	RC44 0_0402_1%	TDI_XDP	XDP_TDI
	RC45 0_0402_1%	TDI_XDP_R	
PCH_JTAG_TMS	RC46 0_0402_1%	TMS_XDP	XDP_TMS
TRST# XDP			XDP_TRST#
RUNPWROK			

1OE 2OE 3OE 4OE VCC GND GND PAD

Place CC29 close to UC4

reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0

+1.05VS — CC14 0.01U_0402_16V7K — XDP@

Place near JXDP1

JXDP1 SAMTE_BSH-030-01-L-D-A CONN@

XDP_PREQ#	RC48 1K_0402_5%	H_CPUPWRGD	XDP@
XDP_PRDY#	RC50 0_0402_5%	CPU_PWR_DEBUG#	XDP@
	RC52 0_0402_5%	SYS_PWROK	XDP@
CFG0 CFG1			
CFG2 CFG3			
XDP_OBS0_R			
XDP_OBS1_R			
CFG4 CFG5			
CFG6 CFG7			
PBTN_OUT#			
CPU_PWR_DEBUG#			
SYS_PWROK			
DDR_XDP_WLAN_TP_SMBDAT	RP46 0_8P4R_5%	DDR_XDP_SMBDAT_R1	
DDR_XDP_WLAN_TP_SMBCLK		DDR_XDP_SMBCLK_R1	
PCH_JTAG_TCK		XDP_TCLK	

GND1 GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16

GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 GND15 TDO TRST# TDI TMS GND17

CFG17 CFG16 CFG8 CFG9 CFG10 CFG11 CFG19 CFG18 CFG12 CFG13 CFG14 CFG15

CLK_XDP RC1391 0_0402_5% CLK_CPU_ITP <9>
CLK_XDP# RC1401 0_0402_5% CLK_CPU_ITP# <9>
XDP_RST# R 2 1 PLT_RST# — PLT_RST# <10,21,26,30,48>
XDP_DBRESET# — RC51 1K_0402_5% XDP@ — RC362 1K_0402_1% — +3VS
TDO_XDP TRST# XDP TDI_XDP TMS_XDP CFG3_R — RC56 XDP@ — CFG3 1K_0402_5%
CC17 0.1U_0402_10V7K

PLT_RST# — CC30 ESD@ 0.047U_0402_16V4Z

Place CC30 close to RC51.1

+1.05VS — RC58 49.9_0402_1% H_CATERR# — RC60 62_0402_5% H_PROCHOT#

PCH_JTAG_RST#	RC57 0_0402_1%	XDP_TRST#	
PCH_JTAG_JTAGX	RC59 0_0402_1%	XDP_TCLK	
	RC62 0_0402_5% XDP@	TDO_XDP	
PCH_JTAG_TDO	RC63 0_0402_5% XDP@	TDI_XDP_R	
PCH_JTAG_TCK	RC65 0_0402_5% XDP@	XDP_TCLK	

+3VALW_PCH — RC64 1K_0402_5% — SYS_PWROK_XDP — ESD@ CC16 0.1U_0402_10V7K

Place near JXDP1.47

XDP_DBRESET# — RC26 0_0402_1% — SYS_RESET# — SYS_RESET# <10>

H_CPUPWRGD — RC66 10K_0402_5% — CC27 100P_0402_50V8J ESD@

ESD solution

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

UC1B HASWELL_MCP_E

CPU_DETECT#	CPU_DETECT# D61	PROC_DETECT	MISC
PECI_EC	H_CATERR# K61	CATERR	
	PECI_EC N62	PECI	
H_PROCHOT#	RC67 56_0402_5% H_PROCHOT#_R K63	PROCHOT	THERMAL
H_CPUPWRGD	C61	PROCPWRGD	PWR
SM_RCOMP0	AU60	SM_RCOMP0	DDR3
SM_RCOMP1	AV60	SM_RCOMP1	
SM_RCOMP2	AU61	SM_RCOMP2	
DDR3_DRAMRST#_CPU	AV15	SM_DRAMRST	
DDR_PG_CTRL	AV61	SM_PG_CNTL1	

JTAG

PRDY J62 XDP_PRDY#
PREQ K62 XDP_PREQ#
PROC_TCK E60 XDP_TCK
PROC_TMS E61 XDP_TMS
PROC_TRST# E59 XDP_TRST#
PROC_TDI K59 XDP_TDI
PROC_TDO F62 XDP_TDO

PCH_JTAG_RST# — R2341 0_0402_5% — PCH_JTAG_RST# <8>

XDP_OBS0_R J60 — RC141 0_0402_1% — XDP_OBS1_R H60

BPM#0 H60 — T111
BPM#1 H61 — T112
BPM#2 H62 — T113
BPM#3 K59 — T114
BPM#4 H63 — T115
BPM#5 K60 — T116
BPM#6 J61
BPM#7

2 OF 19 Rev1p2

PU/PD for JTAG signals

+1.05VS

XDP_TMS XDP_TDI XDP_PREQ# TDO_XDP — RP44 @ 51_8P4R_5%

XDP_TDO XDP_TCK XDP_TRST# — RP45 51_8P4R_5%

DDR3 COMPENSATION SIGNALS

200_0402_1% RC68 SM_RCOMP0
120_0402_1% RC69 SM_RCOMP1
100_0402_1% RC70 SM_RCOMP2

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

DDR3_DRAMRST# CPU — CC35 ESD@ 0.047U_0402_16V4Z

Place CC35 on BOT

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

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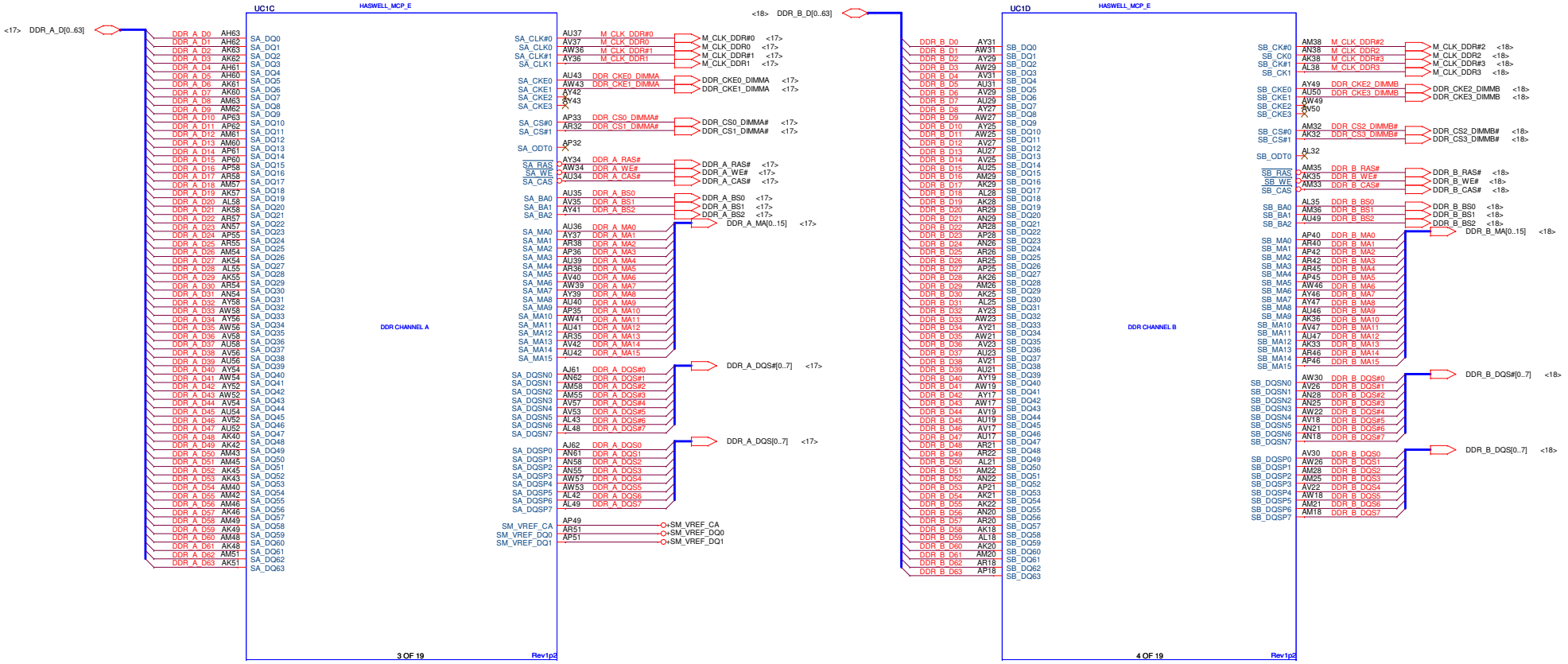
Title: **MCP(1,2/19) eDP,XDP,MISC**

Size: — Document Number: **LA-9984P** — Rev: 1.0

Date: Wednesday, May 22, 2013 — Sheet 6 of 55



confirm by intel request PDG P141

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **MCP(3,4/19) DDR3**

Size | Document Number: **LA-9984P** | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 7 of 57

RTC Battery

+RTCBATT

+CHGRTC

RC10 1K_0402_5%

W=20mils

W=20mils

DC1 BAT54CW_SOT323-3

+RTCVCC

W=20mils

CC26 1U_0603_10V6K

+CHGRTC — JP12 JUMP_43X39 — +3VLP

For GCLK

<29> PCH_RTCX1 — PCH_RTCX1

+RTCVCC

RC1 330K_0402_1%

PCH_INTVRMEN

RC2 330K_0402_1%

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS

@RC3 PCH_AZ_SDOUT 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CC1 15P_0402_50V8J XTAL@

CC2 15P_0402_50V8J XTAL@

XTAL@ YC1 32.768KHZ_12.5PF_Q13FC1350000

XTAL@ RC4 10M_0402_5%

PCH_RTCX1

PCH_RTCX2

INTRUDER#

PCH_INTVRMEN

SRTCRST#

PCH_RTCRST#

+RTCVCC

RC7 1M_0402_5%

RC5 20K_0402_5%

RC6 20K_0402_5%

@ME1 SHORT PADS~D

CC3 1U_0402_6.3V6K

@CMOS1 SHORT PADS~D

CC4 1U_0402_6.3V6K

CMOS place near DIMM

UC1E HASWELL_MCP_E

RTCX1 RTCX2 INTRUDER INTVRMEN SRTCRST RTCRST — RTC

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST/I2S_MCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN/I2S1_TXD
HDA_DOCK_RST/I2S1_SFRM
I2S1_SCLK — AUDIO

PCH_AZ_BITCLK
PCH_AZ_SYNC
PCH_AZ_RST#
PCH_AZ_CODEC_SDIN0

<22> PCH_AZ_CODEC_SDIN0

<30> ME_EN — RC8 1K_0402_5% — PCH_AZ_SDOUT

PCH_TRST
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
RSVD
RSVD
JTAGX
RSVD — JTAG

<6> PCH_JTAG_RST# — PCH_JTAG_RST#
<6> PCH_JTAG_TCK — PCH_JTAG_TCK
<6> PCH_JTAG_TDI — PCH_JTAG_TDI
<6> PCH_JTAG_TDO — PCH_JTAG_TDO
<6> PCH_JTAG_TMS — PCH_JTAG_TMS
<6> PCH_JTAG_JTAGX — PCH_JTAG_JTAGX

SATA_RN0/PERN6_L3
SATA_RP0/PERP6_L3
SATA_TN0/PETN6_L3
SATA_TP0/PETP6_L3 — J5 — SATA_PRX_DTX_N0_C <32> — SATA_PRX_DTX_P0_C <32> — SATA_PTX_DRX_N0_C <32> — SATA_PTX_DRX_P0_C <32> — SATA HDD

SATA_RN1/PERN6_L2
SATA_RP1/PERP6_L2
SATA_TN1/PETN6_L2
SATA_TP1/PETP6_L2 — J8 — SATA_PRX_DTX_N1_C <32> — SATA_PRX_DTX_P1_C <32> — SATA_PTX_DRX_N1_C <32> — SATA_PTX_DRX_P1_C <32> — SATA ODD

SATA_RN2/PERN6_L1
SATA_RP2/PERP6_L1
SATA_TN2/PETN6_L1
SATA_TP2/PETP6_L1 — J6

SATA_RN3/PERN6_L0
SATA_RP3/PERP6_L0
SATA_TN3/PETN6_L0
SATA_TP3/PETP6_L0

SATA0GP/GPIO34
SATA1GP/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37 — SATA

SATA_IREF
RSVD
RSVD
SATA_RCOMP
SATALED

PCH Rx side need use strap pin to update PCIE +/-

+3VS

RC107 10K_0402_5%

EC_SMI# <30>

ODD_DETECT# <32>

+1.05VS_ASATA3PLL

SATA_IREF — RC126 @ 0_0603_1%

SATA_RCOMP — RC131 3.01K_0402_1%

SATA_ACT# <26>

within 500 mils

5 OF 19

Rev1p2

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

+1.05VS

@RC130 PCH_JTAG_JTAGX 1K_0402_1%

@RC135 PCH_JTAG_TCK 51_0402_1%

+1.05VS

RP48 51_8P4R_5%

PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

<22> PCH_AZ_CODEC_SDOUT — EMI@ R2356 33_0402_5% — PCH_AZ_SDOUT
<22> PCH_AZ_CODEC_SYNC — EMI@ R2357 33_0402_5% — PCH_AZ_SYNC
<22> PCH_AZ_CODEC_RST# — EMI@ R2358 33_0402_5% — PCH_AZ_RST#
<22> PCH_AZ_CODEC_BITCLK — EMI@ R2359 33_0402_5% — PCH_AZ_BITCLK

@EMI@ CC5 27P_0402_50V8J

EMI depop location

+3VS

ODD_DETECT#
PCH_GPIO35
PCH_GPIO37

RP37 10K_8P4R_5%

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

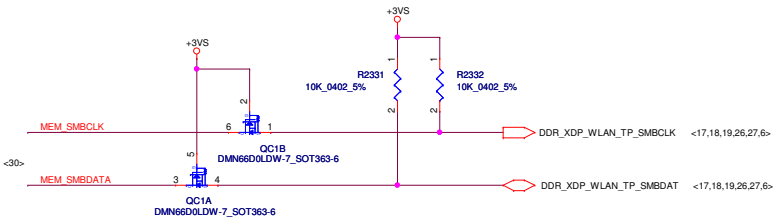
Compal Electronics, Inc.

Title: MCP(5/19) RTC,SATA,HDA,JTAG

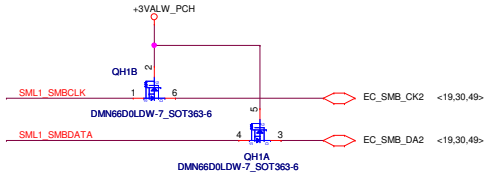
Size: | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 8 of 57

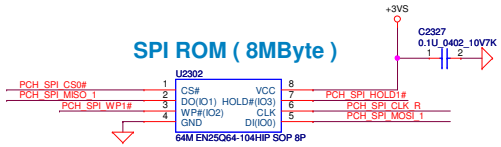
MEM Bus : DDR/XDP/WLAN/TP



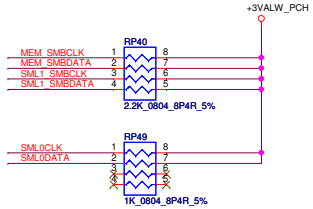
SML1 Bus : EC/Sensors

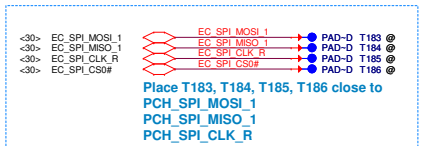


SPI ROM (8MByte)

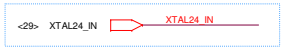


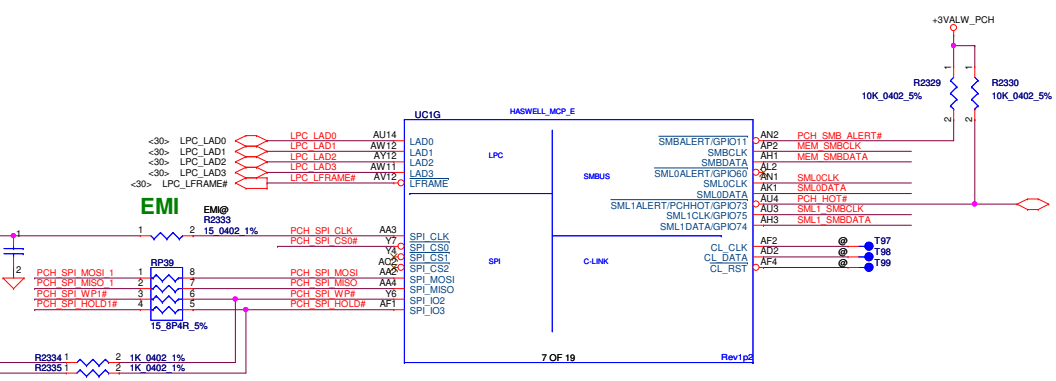
PN : SA000046400 ,64M,EN25Q64-104HIP

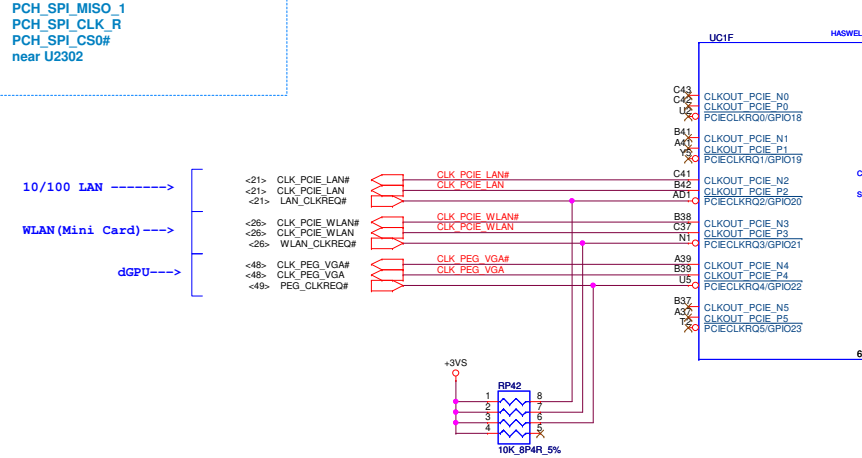




For GCLK







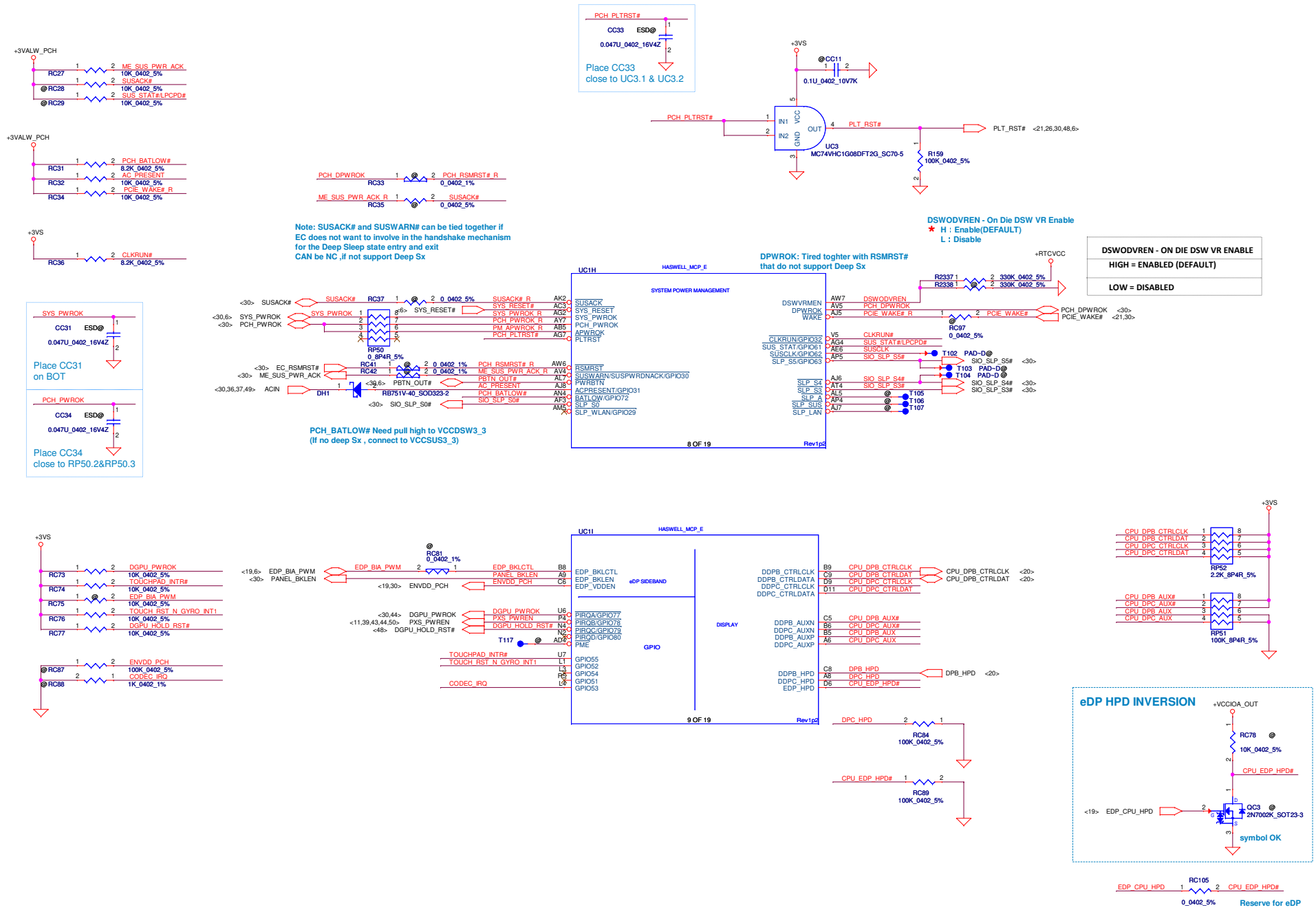
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(6,7/19) CLK,SMB,SPI,LPC

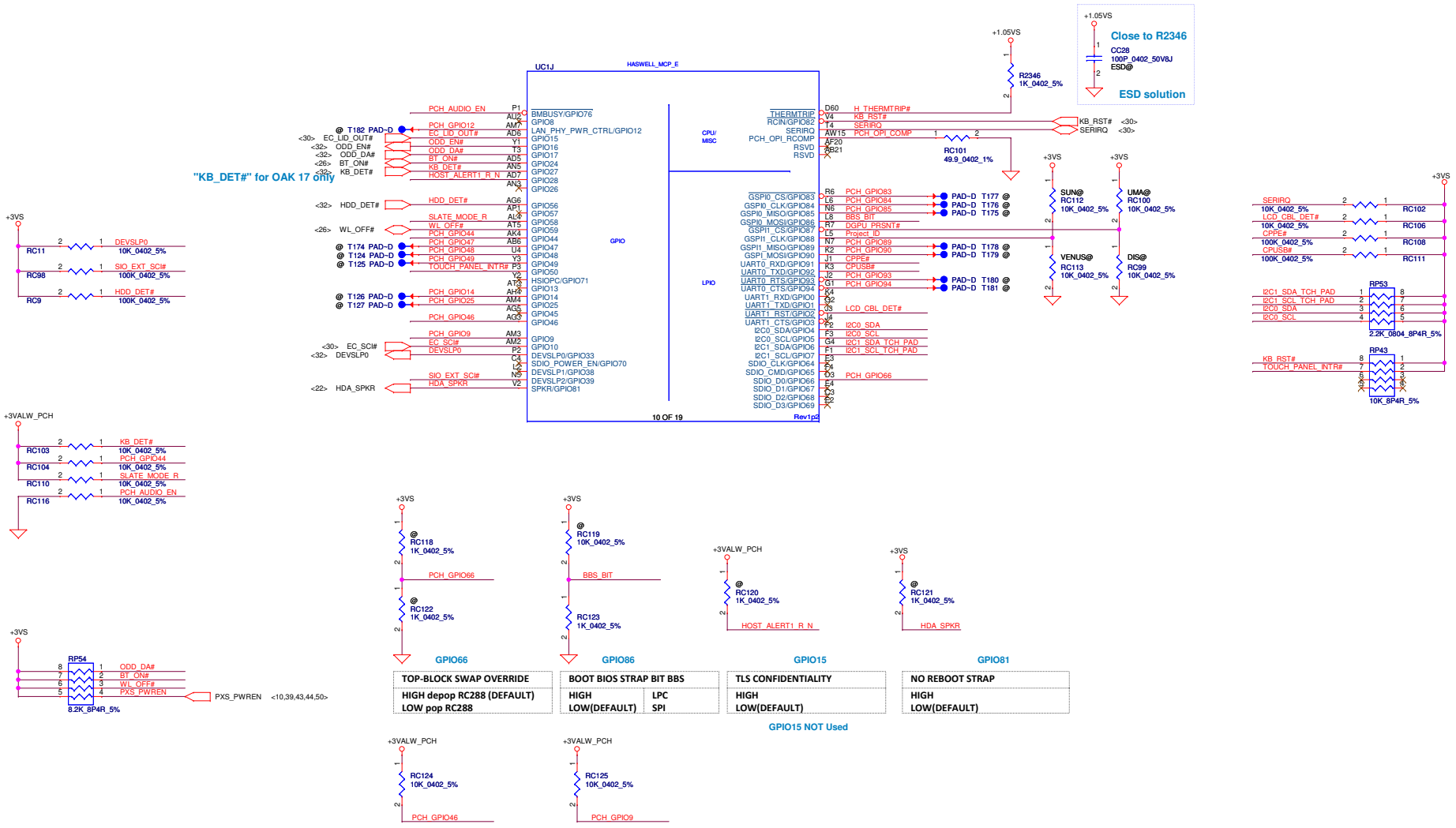
Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 9 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: MCP(8,9/19) DDI,EDP,GPIO			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 10 of 57		



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Size: | Document Number: **LA-9984P** | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 11 of 57

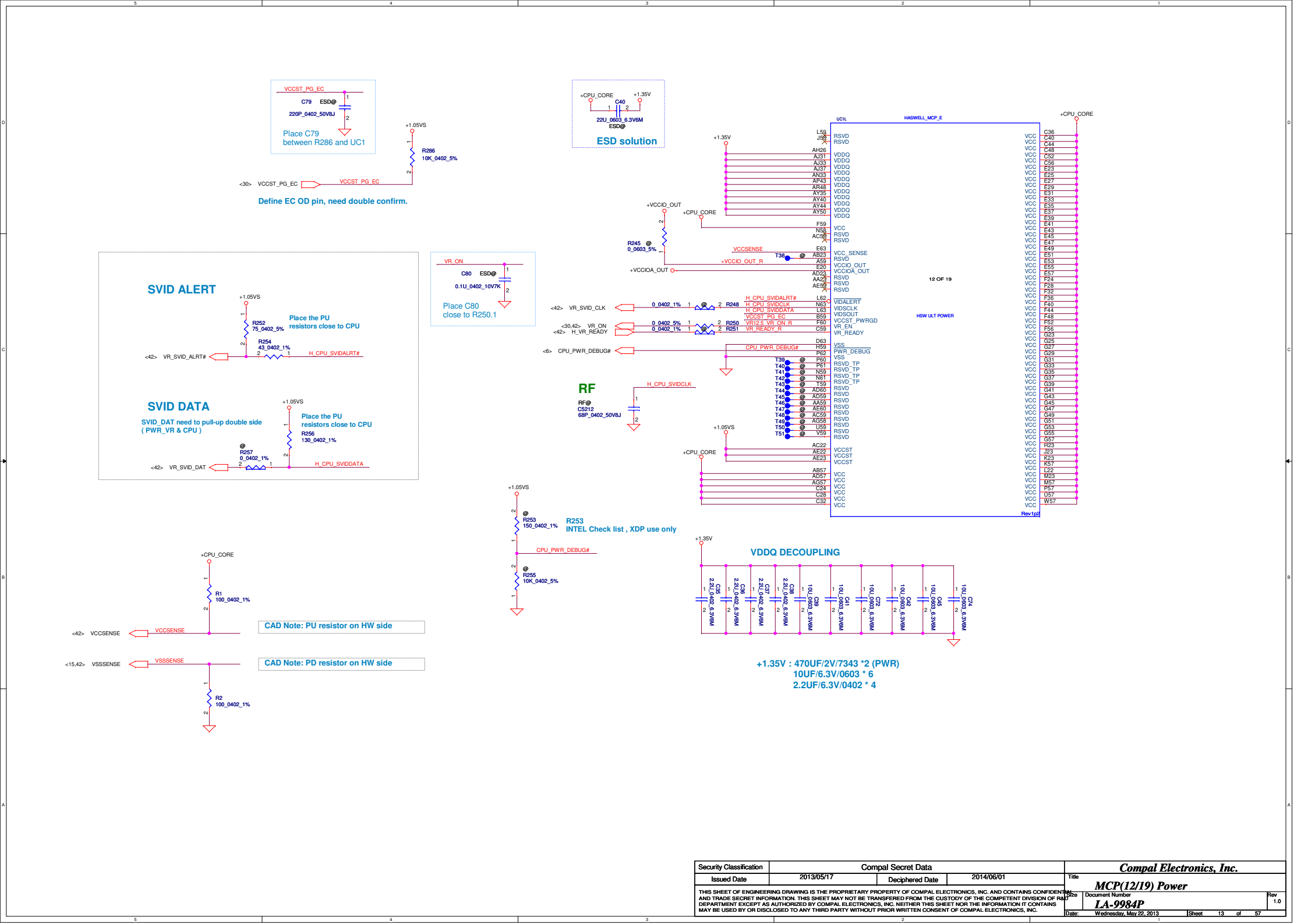
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(11/19) PCIE,USB

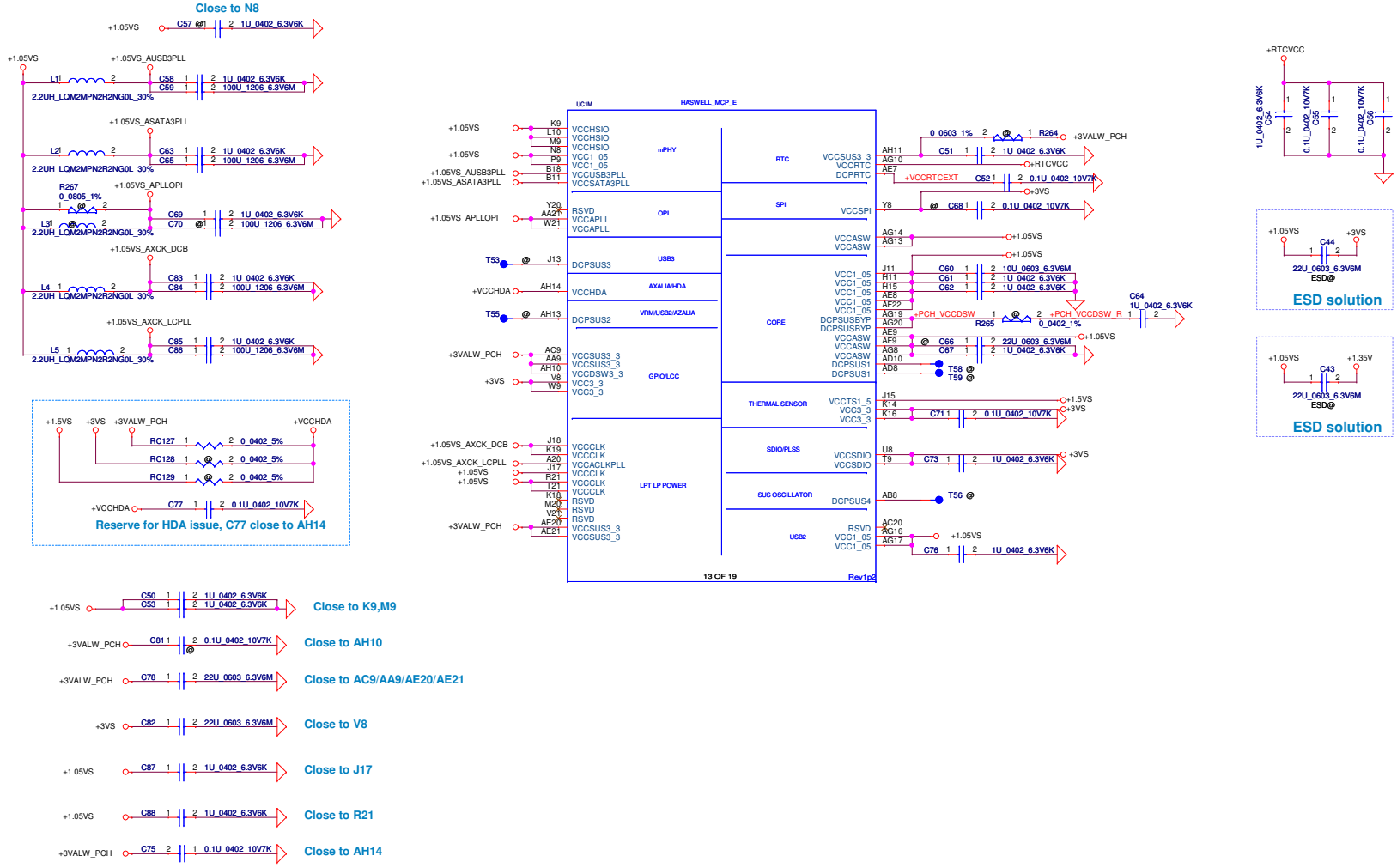
Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 12 of 57



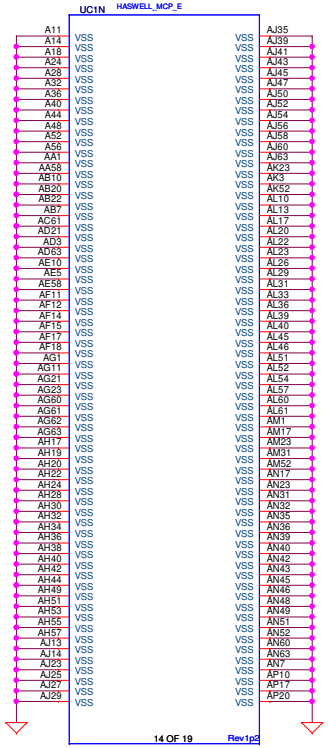
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

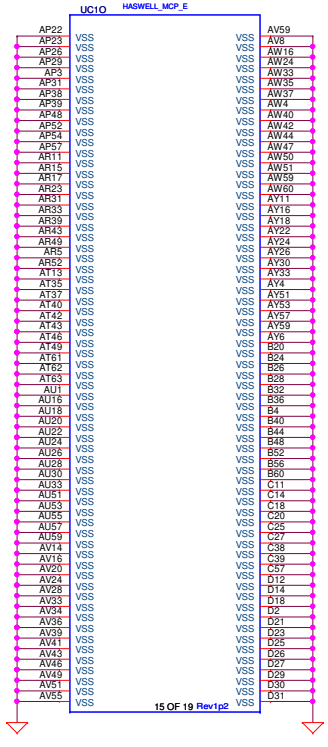
Compal Electronics, Inc.			
Title: MCP(12/19) Power			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 13 of 57		

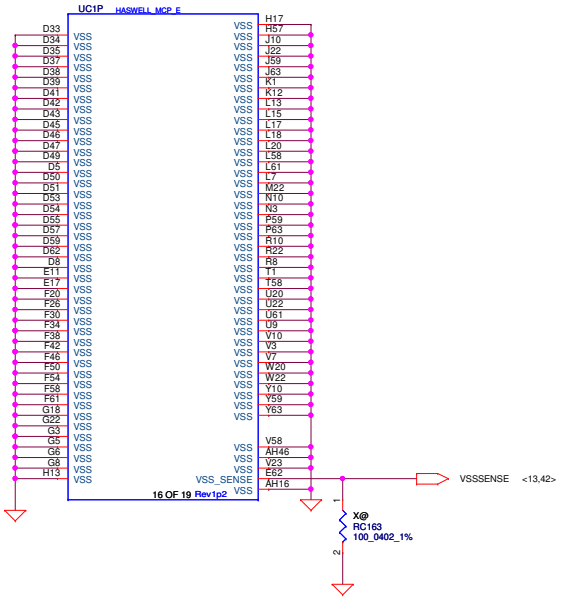


Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: MCP(13/19) Power			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 14 of 57		







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

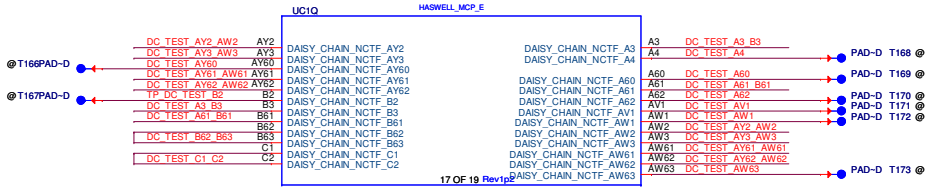
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

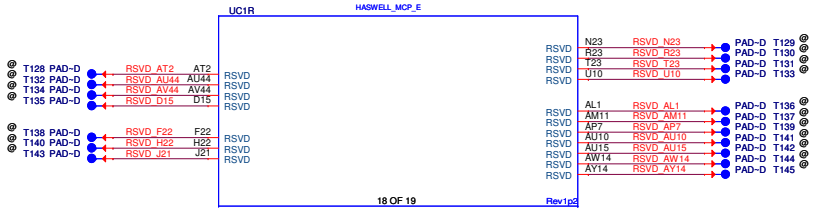
Compal Electronics, Inc.

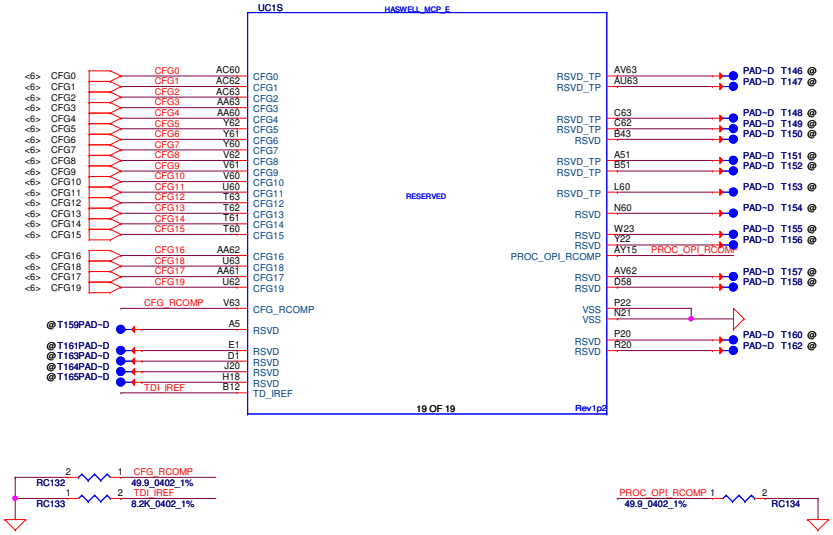
Title: MCP(14,15,16/19) VSS

Size: | Document Number: LA-9984P | Rev: 1.0

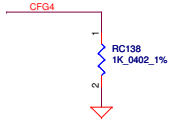
Date: Wednesday, May 22, 2013 | Sheet 15 of 57







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 16 of 57

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

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Compal Electronics, Inc.

Title: DDRIII DIMMA

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 17 of 57

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2 CONN@
LCN_DAN06-K4406-0102

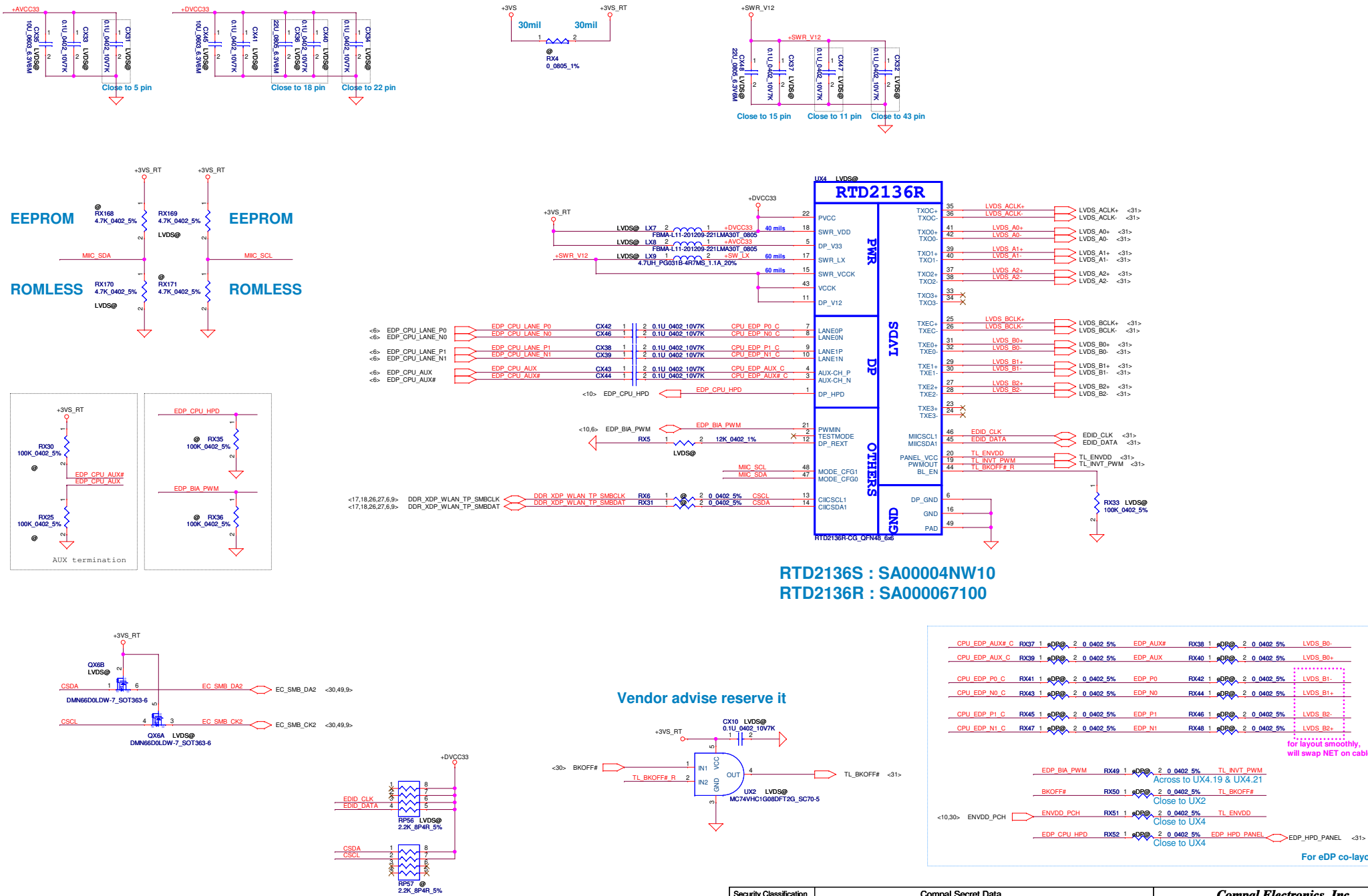
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Document Number: LA-9984P Rev: 1.0

Date: Wednesday, May 22, 2013 Sheet 18 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

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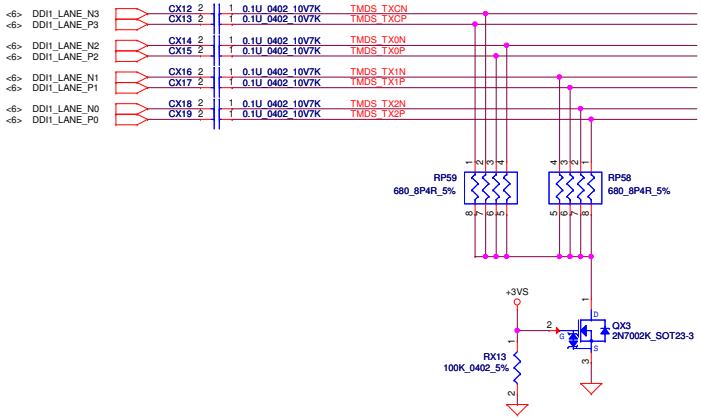
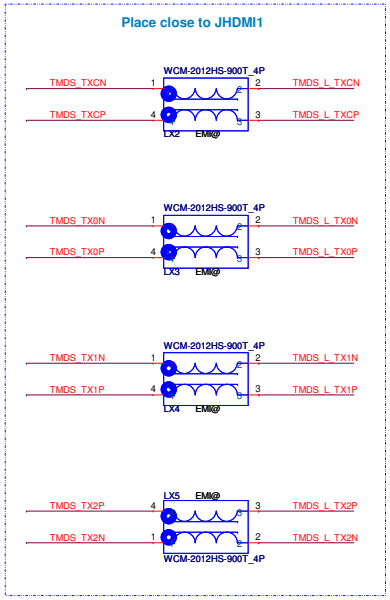
Compal Electronics, Inc.

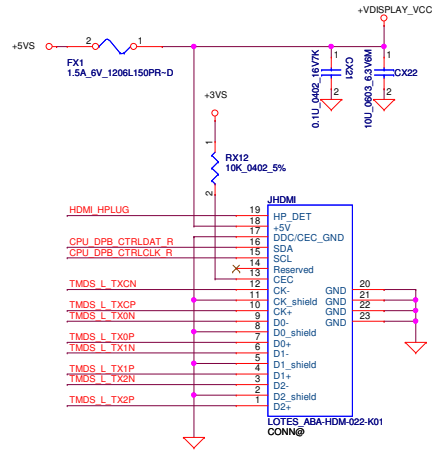
Title: **eDP to LVDS converter**

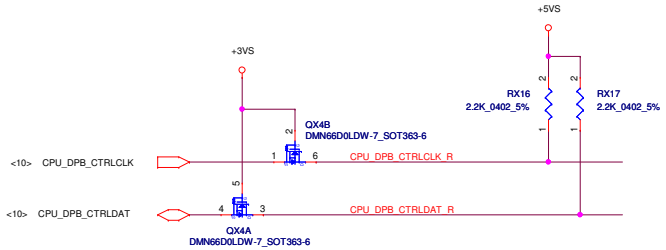
Size | Document Number: **LA-9984P** | Rev: 1.0

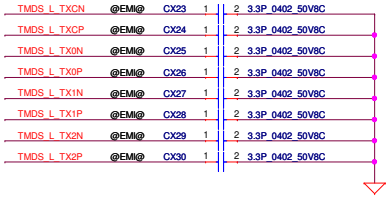
Date: Wednesday, May 22, 2013 | Sheet 19 of 57

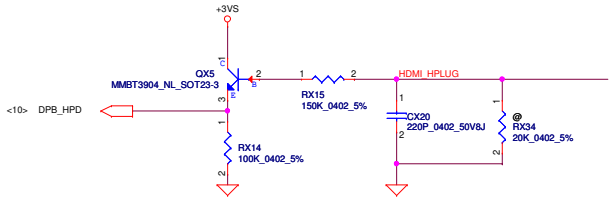












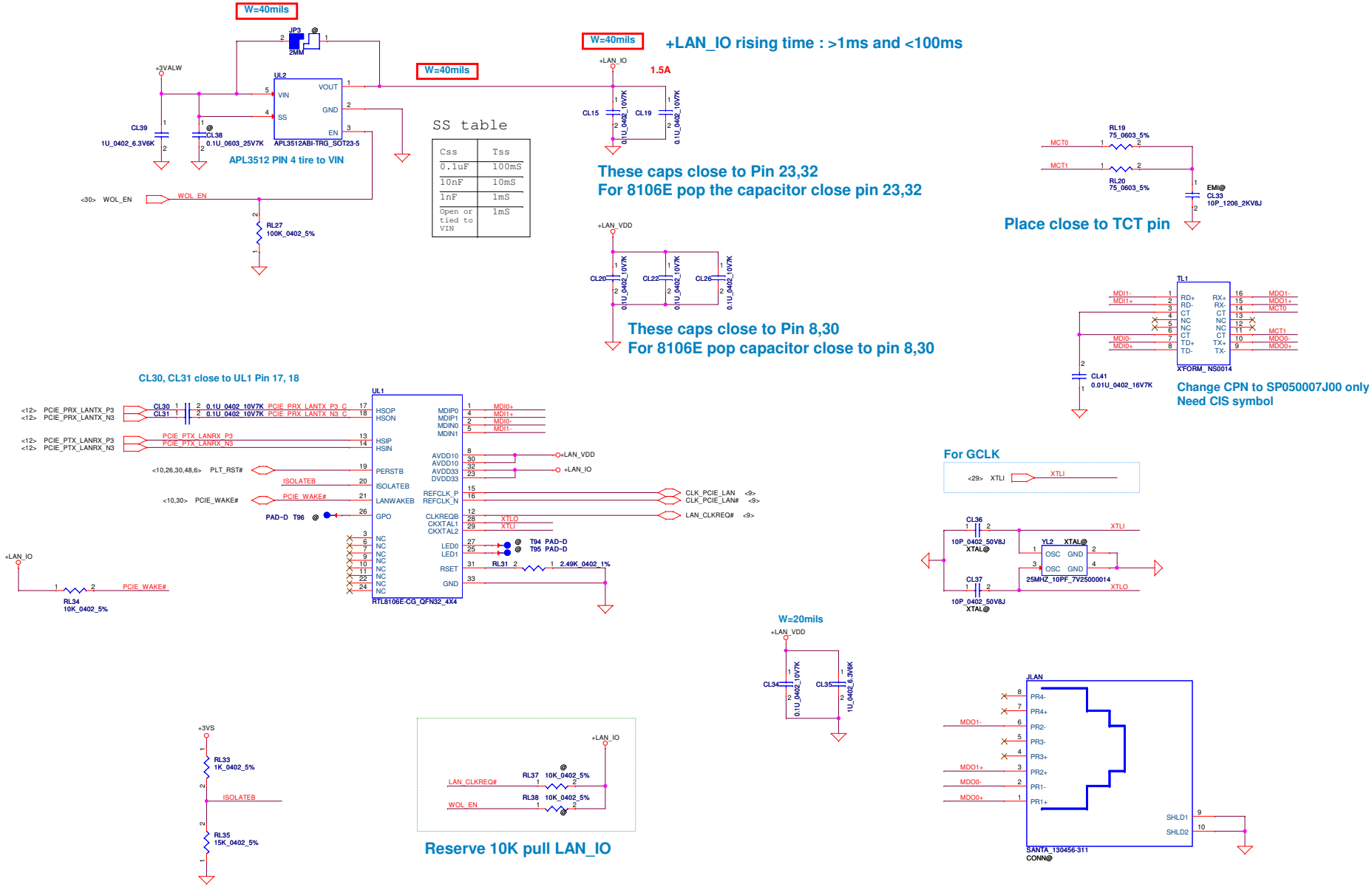
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 20 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: LAN RTL8106E			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 21 of 57		

Reserve for HDA issue

CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

RA51, RA33 place close to UA1

ALC3223-CG_MQFN48_6X6-D

JACK_PLUG Delay circutis

Reserve for cancel Delay circutis

Place on the moat between GND & GNDA.

SM01000BV00
need CIS symbol

EC Beep

MCU Beep

PC Beep

Close to UA1
Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

40mil

40mil

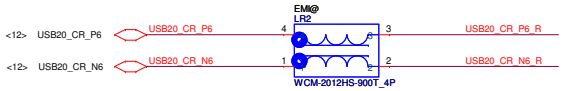
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

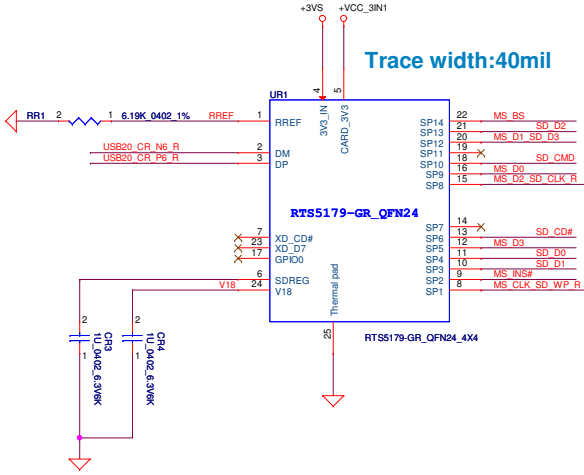
Compal Electronics, Inc.

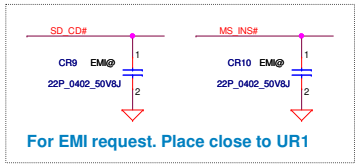
Title: Audio Codec ALC3223

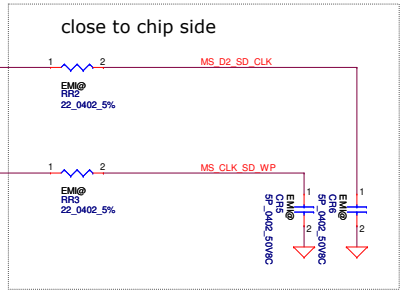
Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 22 of 57



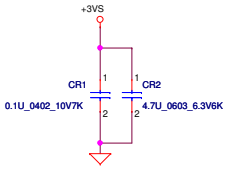


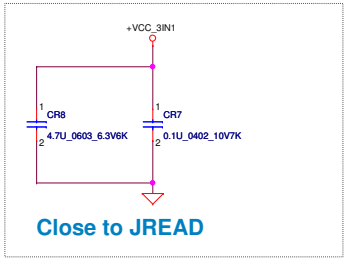


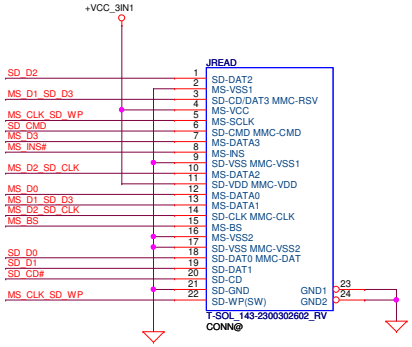


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

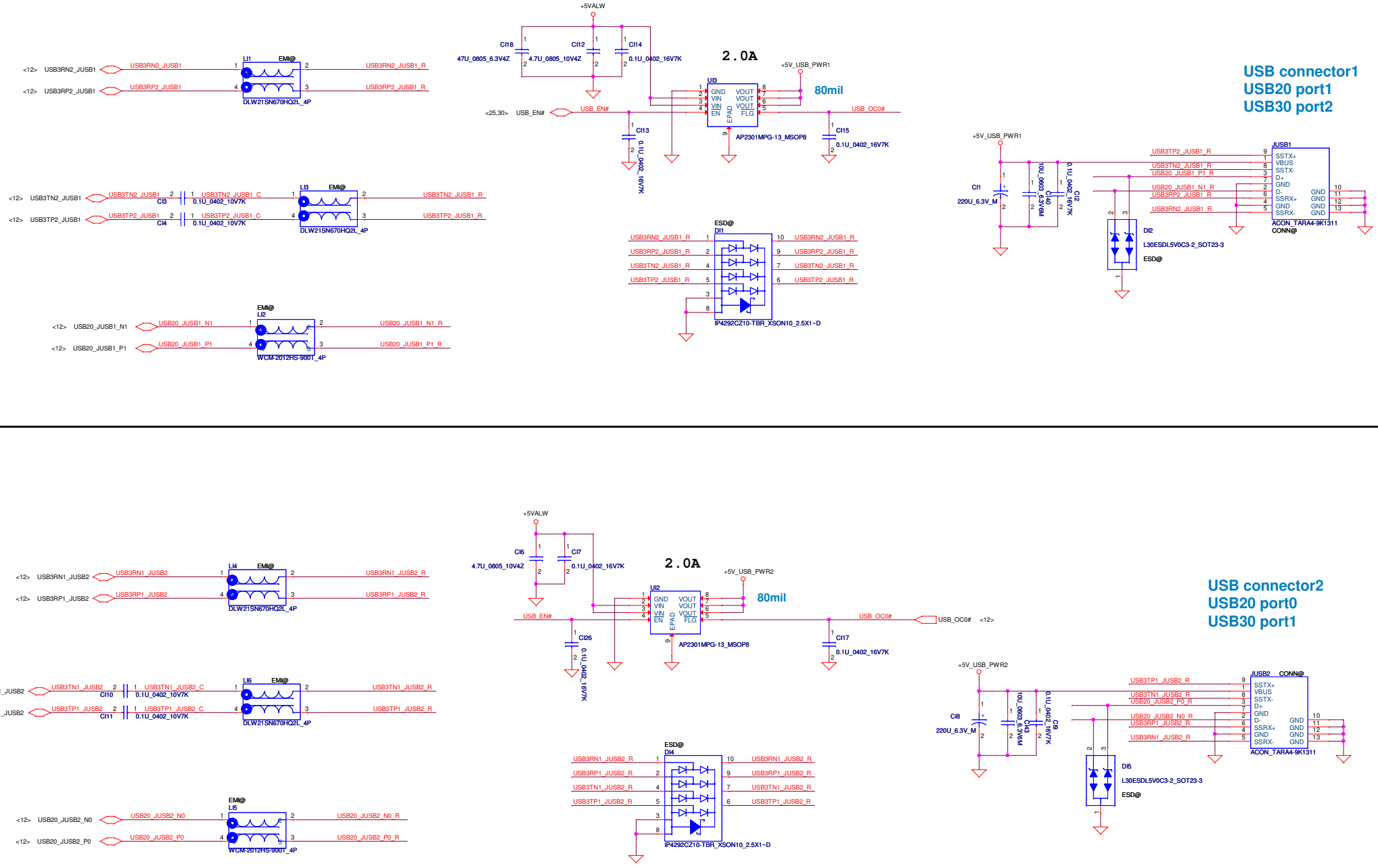






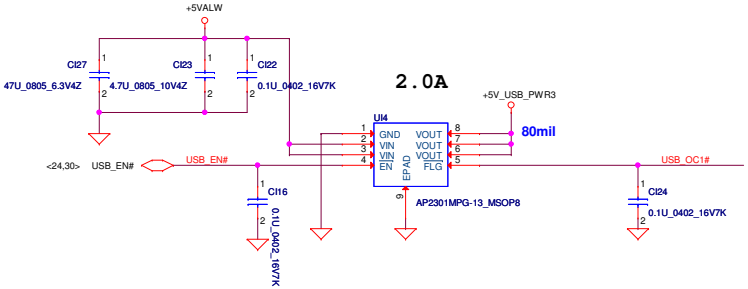
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

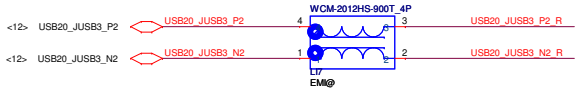
Compal Electronics, Inc.			
Title: Card Reader RTS5179			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 23 of 57		



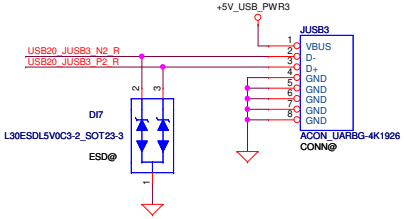
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

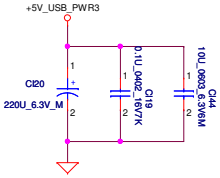
Compal Electronics, Inc.			
Title: USB3.0			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 24 of 57		



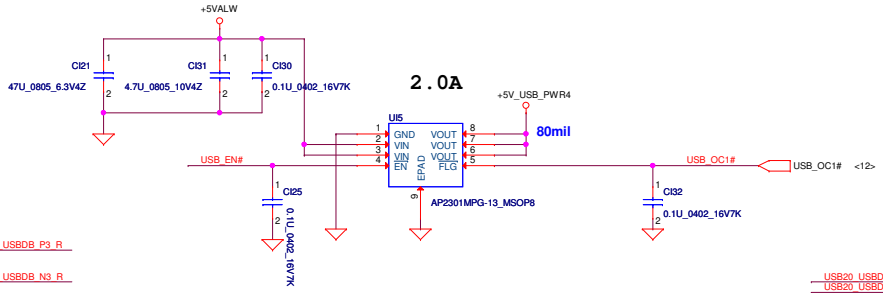


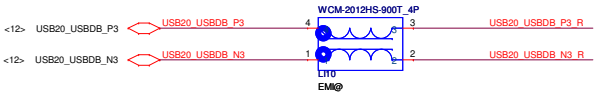
USB connector3
USB20 port2



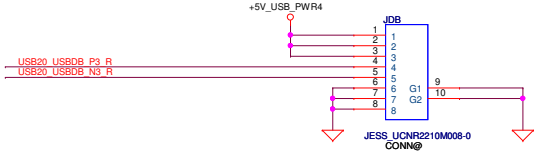


Place close to JUSB3





USB connector4
USB20 port3



2nd: SP01001EX00
Main: SP01001AA00
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

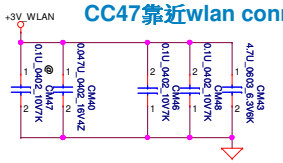
Compal Electronics, Inc.

Title: MB to USB2.0 DB

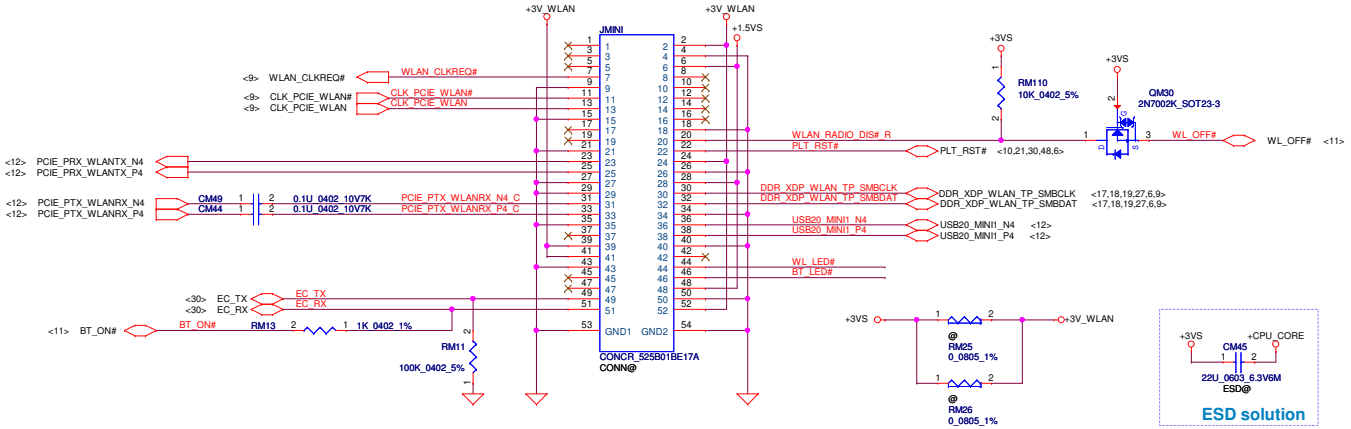
Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 25 of 57

CC47靠近wlan connector

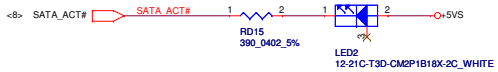


Mini WLAN/WIMAX H=6.7

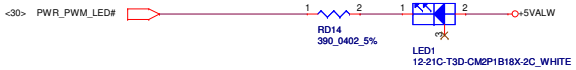


HDD LED

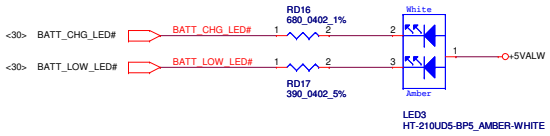
10mils, All pins

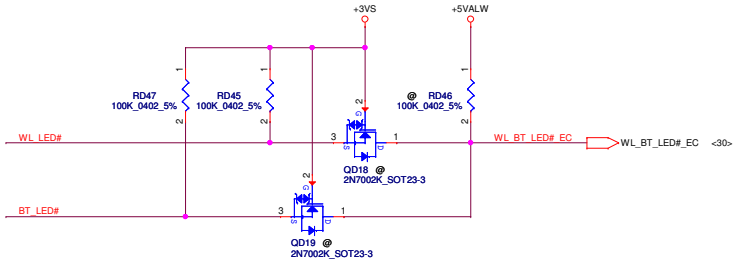


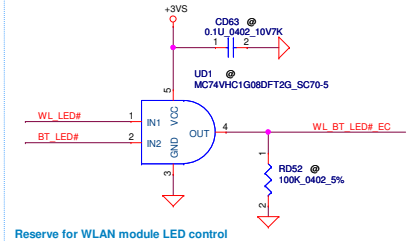
Power LED

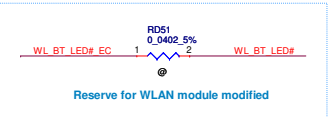


Battery LED

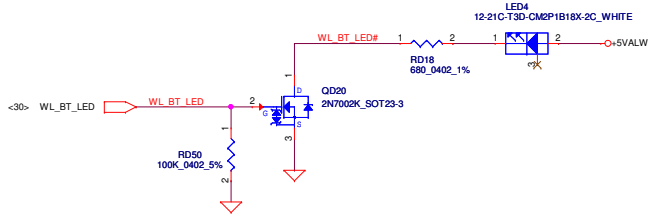








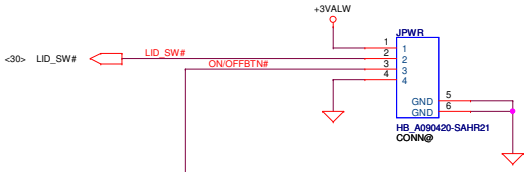
Wireless LED



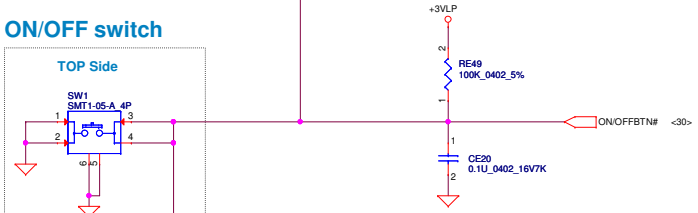
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	Mini Card/LED
Size	Document Number: LA-9984P
Rev	1.0
Date:	Wednesday, May 22, 2013
Sheet	26 of 57

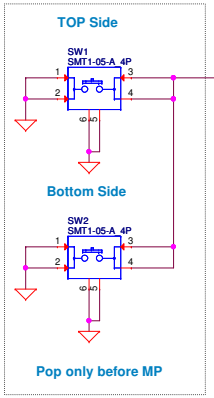
POWER/B



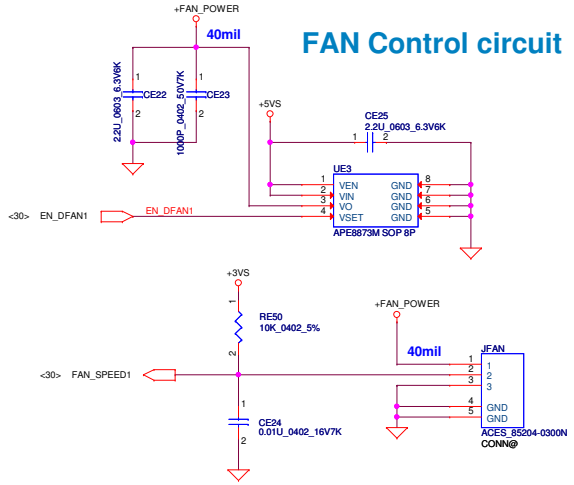
Power ON Circuit



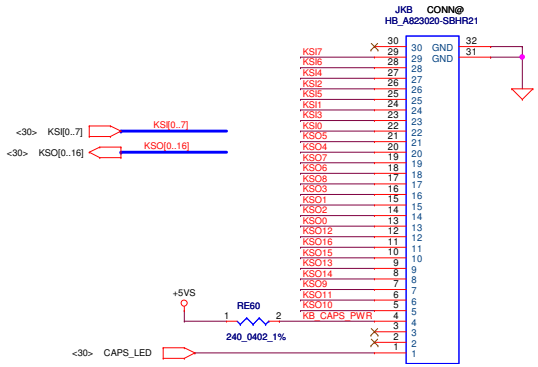
ON/OFF switch



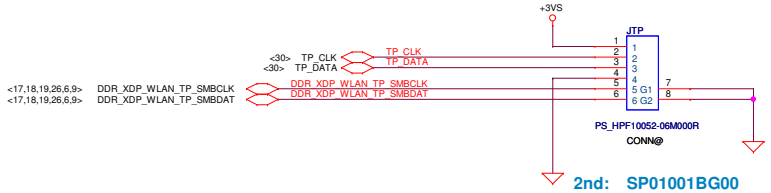
FAN Control circuit



INT_KBD Connector



Touch pad



2nd: SP01001BG00
Main: SP01000R910
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

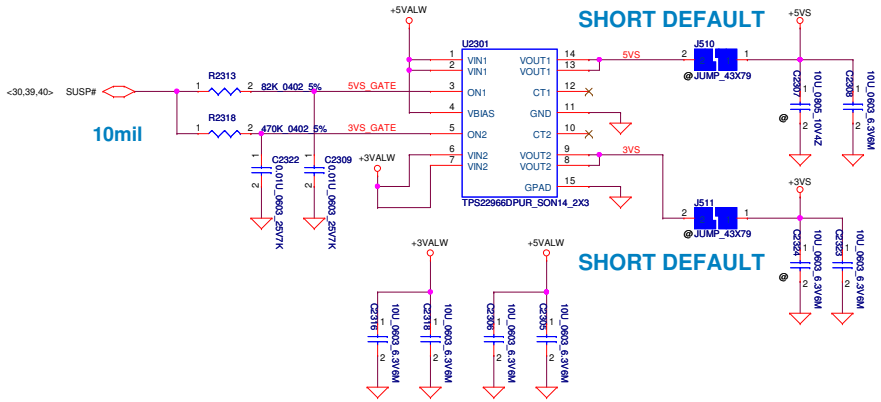
Compal Electronics, Inc.

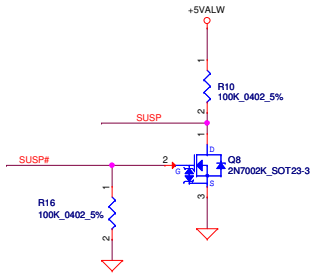
Title: **FAN/TP/PWR SW**

Size | Document Number: **LA-9984P** | Rev: 1.0

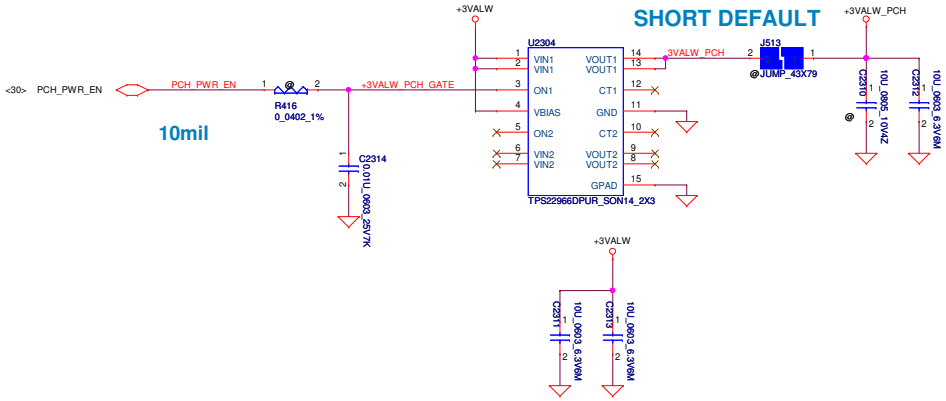
Date: Wednesday, May 22, 2013 | Sheet 27 of 57

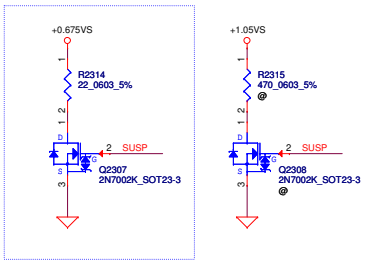
+5VS and +3VS switch





+3VALW_PCH switch





For Intel S3 Power Reduction

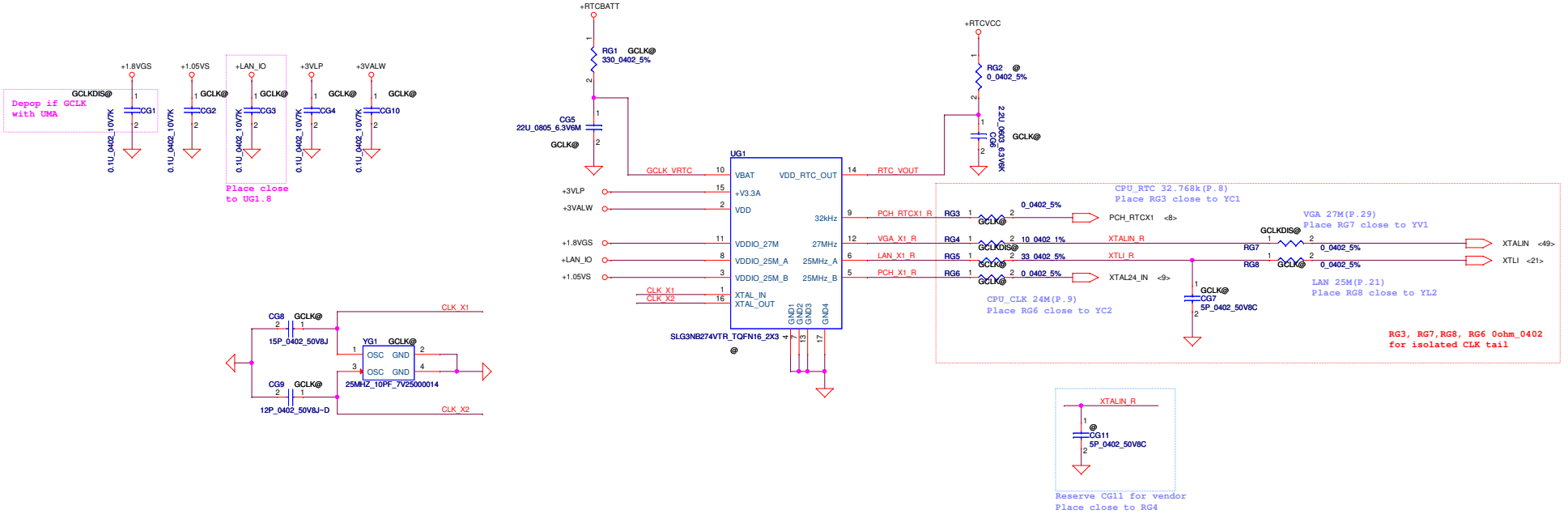
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 28 of 57		

UG1 GCLKUMA@ SLG3NB244VTR TQFN 16P CLK GEN

UG2 GCLKDIS@ SLG3NB244VTR TQFN 16P CLK GEN

SLG3NB3374V is for DIS by output 24M*1,25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: GCLK

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 23 of 57

SD028000080	0_0402_5%
SD034120280	12K_0402_1%
SD034100300	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD000001B80	240K_0402_1%
SD00000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%

Board ID
Venus DIS@
UMA UMA@

RE5 DIS@ 330K_0402_1%
SD034330380

+3VALW
RE3 100K_0402_1% Ra
AD_BID0
RE5 200K_0402_1% UMA@ Rb
CE8 0.1U_0402_10V7K

PLT_RST#
CE36 ESD@ 0.047U_0402_16V4Z
Place CC30 close to RC51.1

+3VALW
CE1 0.1U_0402_10V7K
CE2 0.1U_0402_10V7K
@EMI@ CE5 1000P_0402_50V7K
@EMI@ CE6 1000P_0402_50V7K
EMI@ LE1 FBMA-L11-160808-800LMT_0603
+EC_VCCA
CE7 0.1U_0402_10V7K
+3VLP
ECAGND

UE1

"KB_LED_PWM" for OAK 17 only

PWM Output
AD Input
PC & MISC
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI

GATEA20/GPIO00	WL_BT_LED	<26> WL_BT_LED
KBRST#/GPIO01	KB_RST#	<11> KB_RST#
SERIRQ	SERIRQ	<11> SERIRQ
LPC_FRAME#	LPC_LFRAME#	<9> LPC_LFRAME#
LPC_AD3	LPC_LAD3	<9> LPC_LAD3
LPC_AD2	LPC_LAD2	<9> LPC_LAD2
LPC_AD1	LPC_LAD1	<9> LPC_LAD1
LPC_AD0	LPC_LAD0	<9> LPC_LAD0
CLK_PCI_EC	CLK_PCI_LPC	<9> CLK_PCI_LPC
PCIRST#/GPIO05	PLT_RST#	<10,21,26,48,6> PLT_RST#
EC_RST#	EC_RST#	
EC_SCI#/GPIO0E	EC_SCI#	<11> EC_SCI#
GPIO1D	TOUCH_RST	<11> TOUCH_RST
GPIO0F	KB_LED_PWM	KB_LED_PWM <32>
BEEP#/GPIO10	BEEP#	BEEP# <22>
GPIO12	USB_EN#	USB_EN# <24,25>
ACOFF/GPIO13	ACOFF	ACOFF <37>
BATT_TEMP/GPIO38	BATT_TEMP	BATT_TEMP <36,37>
GPIO39	WL_BT_LED# EC	WL_BT_LED# EC <26>
ADP_I/GPIO3A	ADP_I	ADP_I <36,37>
GPIO3B	AD_BID0	
GPIO42	PANEL_BKLEN	PANEL_BKLEN <10>
IMON/GPIO43		
DAC_BRIG/GPIO3C	EN_INVPWR	EN_INVPWR <31>
EN_DFAN1/GPIO3D	EN_DFAN1	EN_DFAN1 <27>
IREF/GPIO3E	EC_ENVDD	EC_ENVDD <31>
CHGVADJ/GPIO3F	LCD_TEST	LCD_TEST <31>
EC_MUTE#/GPIO4A	EC_MUTE#	EC_MUTE# <22>
USB_EN#/GPIO4B	SIO_SLP_S4#	SIO_SLP_S4# <10>
CAP_INT#/GPIO4C	IMVP_PWRGD	IMVP_PWRGD <42>
EAPD/GPIO4D	SYS_PWROK	SYS_PWROK <10,6>
TP_CLK/GPIO4E	TP_CLK	TP_CLK <27>
TP_DATA/GPIO4F	TP_DATA	TP_DATA <27>
CPU1.5V_S3_GATE/GPIOA00	SUSACK#	SUSACK# <10>
WOL_EN/GPXIOA01	WOL_EN	WOL_EN <21>
ME_EN/GPXIOA02	ME_EN	ME_EN <8>
VCIN0_PH/GPXIOD00	VCIN0_PH	VCIN0_PH <36>
SPID/GPIO5B	EC_SPI_MOSI_1	EC_SPI_MOSI_1 <9>
SPIDO/GPIO5C	EC_SPI_MISO_1	EC_SPI_MISO_1 <9>
SPICLK/GPIO5B	EC_SPI_CLK_R	EC_SPI_CLK_R <9>
SPICS#/GPIO5A	EC_SPI_CS0#	EC_SPI_CS0# <9>
ENBKL/GPIO40	ERP_LOT6	ERP_LOT6 <36>
PECI_KB930/GPIO41	WL_BT_LED# EC2	WL_BT_LED# EC2 <26>
FSTCHG/GPIO50	SIO_SLP_S0#	SIO_SLP_S0# <10>
BATT_CHG_LED#/GPIO52	BATT_CHG_LED#	BATT_CHG_LED# <26>
CAPS_LED#/GPIO53	CAPS_LED	CAPS_LED <27>
PWR_LED#/GPIO54	PWR_PWM_LED#	PWR_PWM_LED# <26>
BATT_LOW_LED#/GPIO55	BATT_LOW_LED#	BATT_LOW_LED# <26>
SYSON/GPIO56	SYSON	SYSON <41>
VR_ON/GPIO57	VR_ON_EC	
PM_SLP_S4#/GPIO59	CPU_DETECT#	CPU_DETECT# <6>
EC_RSMRST#/GPXIOA03	EC_RSMRST#	EC_RSMRST# <10>
EC_LID_OUT#/GPXIOA04	EC_LID_OUT#	EC_LID_OUT# <11>
PROCHOT_IN/GPXIOA05	VCIN1_PH	VCIN1_PH <36>
H_PROCHOT#_EC/GPXIOA06	VCOUT1_PH	VCOUT1_PH <36>
VCOUT0_PH/GPXIOA07	VCOUT0_PH#	VCOUT0_PH# <38>
BKOFF#/GPXIOA08	BKOFF#	BKOFF# <19>
PBTN_OUT#/GPXIOA09	PBTN_OUT#	PBTN_OUT# <10,6>
PCH_APWROK/GPXIOA10	PCH_PWR_EN	PCH_PWR_EN <28>
SA_PGOOD/GPXIOA11	ACIN_65W	ACIN_65W <49>
AC_IN/GPXIOD01	ACIN	ACIN <10,36,37,49>
EC_ON/GPXIOD02	EC_ON	EC_ON <38>
ON/OFFBTN#/GPXIOD03	ON/OFFBTN#	ON/OFFBTN# <27>
LID_SW#/GPXIOD04	LID_SW#	LID_SW# <27>
SUSP#/GPXIOD05	SUSP#	SUSP# <28,39,40>
GPXIOD06	65W/90W#	65W/90W# <36>
PECI_KB9012/GPXIOD07	PECI_KB9012	PECI_EC <6>
V18R	+V18R	
KSI0	KSI[0..7]	<27> KSI[0..7]
KSI1	KSO[0..16]	<27> KSO[0..16]
KSI2		
KSI3		
KSI4		
KSI5		
KSI6		
KSI7		
KSO0		
KSO1		
KSO2		
KSO3		
KSO4		
KSO5		
KSO6		
KSO7		
KSO8		
KSO9		
KSO10		
KSO11		
KSO12		
KSO13		
KSO14		
KSO15		
KSO16	PCH_DPWROK	<10> PCH_DPWROK
KSO17/GPIO49		
EC_SMB_CK1/GPIO44	EC_SMB_CK1	<36,37> EC_SMB_CK1
EC_SMB_DA1/GPIO45	EC_SMB_DA1	<36,37> EC_SMB_DA1
EC_SMB_CK2/GPIO46	EC_SMB_CK2	<19,49,9> EC_SMB_CK2
EC_SMB_DA2/GPIO47	EC_SMB_DA2	<19,49,9> EC_SMB_DA2
PM_SLP_S3#/GPIO04	SIO_SLP_S3#	<10> SIO_SLP_S3#
PM_SLP_S5#/GPIO07	SIO_SLP_S5#	<10> SIO_SLP_S5#
EC_SMI#/GPIO08	EC_SMI#	<8> EC_SMI#
GPIO0A	PS_ID	<36> PS_ID
GPIO0B	CE_EN	<31> CE_EN
GPIO0C	DGPU_PWROK	<10,44> DGPU_PWROK
GPIO0D	ENVDD_PCH	<10,19> ENVDD_PCH
EC_INVT_PWM/GPIO11	DBC_EN	<31> DBC_EN
FAN_SPEED1/GPIO14	FAN_SPEED1	<27> FAN_SPEED1
EC_PME#/GPIO15	PCIE_WAKE#	<10,21> PCIE_WAKE#
EC_TX/GPIO16	EC_TX	<26> EC_TX
EC_RX/GPIO17	EC_RX	<26> EC_RX
PCH_PWROK/GPIO18	PCH_PWROK	<10> PCH_PWROK
SUSP_LED#/GPIO19	ME_SUS_PWR_ACK	<10> ME_SUS_PWR_ACK
NUM_LED#/GPIO1A	RUNPWROK	<6> RUNPWROK
XCLKI/GPIO5D	+1.05V_PGOOD	<40> +1.05V_PGOOD
XCLKO/GPIO5E	VCCST_PG_EC	<13> VCCST_PG_EC

KB9012QF-A4_LQFP128_14X14

CE9 100P_0402_50V8J ECAGND
RE7 0_0402_5%
TP_CLK 4.7K_0402_5% RE9
TP_DATA 4.7K_0402_5% RE10

RE8 47K_0402_5%
CE11 0.1U_0402_10V7K
"TOUCH_RST" for OAK 15 only

+3VALW
RE71 10K_0402_5% LID_SW#

RP36 2.2K_0804_8P4R_5%
EC_SMB_CK1
EC_SMB_DA1
EC_SMB_CK2
EC_SMB_DA2

RE37 0_0402_1%

Reserve for ESD
CE27 ESD@ 0.1U_0402_10V7K SIO_SLP_S3#
CE28 ESD@ 0.1U_0402_10V7K SIO_SLP_S5#
Please close to EC

RE18 10K_0402_5% PCH_PWROK

FAN_SPEED1
CE29 220P_0402_50V8J
Please close to EC

VR_ON
CE34 ESD@ 0.1U_0402_10V7K
Place CE34 between DE1 and RE12

VCCST_PG_EC
CE35 ESD@ 220P_0402_50V8J
Place CE35 between DE1 and UE1

VR_ON
VCCST_PG_EC
DE1 @ESD@ L03ESDL5V0CG3-2_SOT-523-3
Place DE1 close to UE1

RE12 0_0402_5%
RE1 10K_0402_5%
CE26 0.1U_0402_10V7K
RE11 100K_0402_5%
RE2 10K_0402_5%
RE38 43_0402_1%
RE43 43_0402_1%
CE16 4.7U_0805_10V4Z

LID_SW# CE30 ESD@ 0.1U_0402_10V7K
PCH_PWROK CE31 ESD@ 0.1U_0402_10V7K
SYS_PWROK CE32 ESD@ 0.1U_0402_10V7K
CPU_DETECT# CE33 ESD@ 0.1U_0402_10V7K
Place CE30,CE31,CE32,CE33 close to UE1

LE2 FBMA-L11-160808-800LMT_0603 ECAGND
20mil

<42> VR_HOT# VR_HOT#
RE44 @ 0_0402_1%
<36,6> H_PROCHOT# H_PROCHOT#
UE2 SN74LVC1G06DCKR_SC70-5
CE19 47P_0402_50V8J
CE15 0.01U_0402_16V7K
VCOUT1_PH
RE47 100K_0402_5%

KB9012A3 change to KB9012A4 SA00004OB30

ME_FWP PCH has internal 20K PD. (suspend power rail)

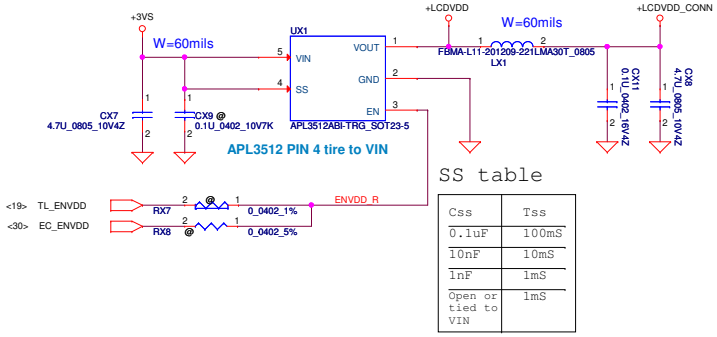
ME_EN
RE326 @ 1K_0402_5%

ACIN CE18 100P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

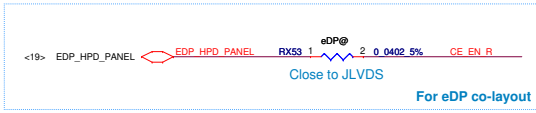
Compal Electronics, Inc.
Title: EC ENE-KB9012
Size: Document Number: LA-9984P
Rev: 1.0
Date: Wednesday, May 22, 2013 Sheet 30 of 57

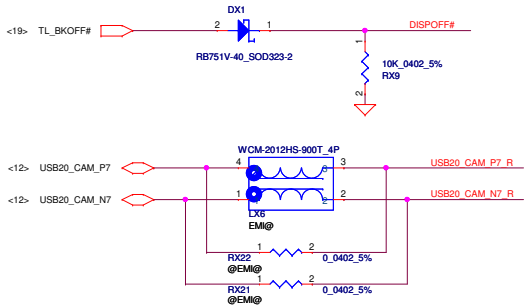
LCD PWR CTRL



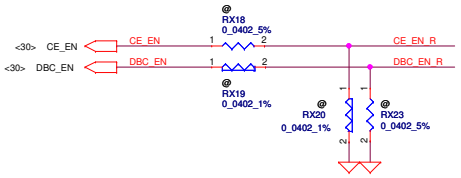
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

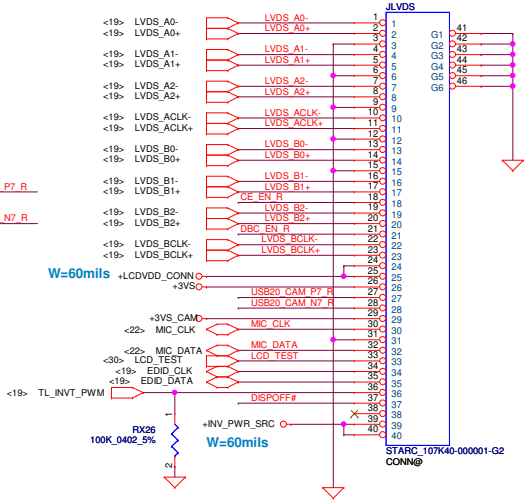




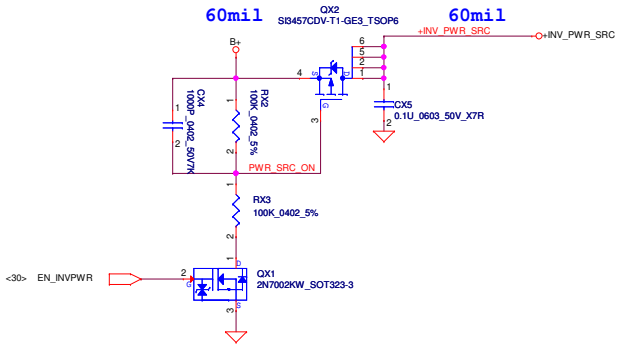
CE_EN_R only for reserve.

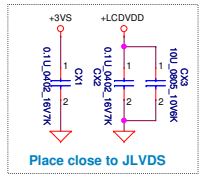


LVDS Connector

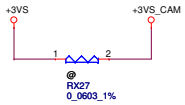


LCD backlight PWR CTRL





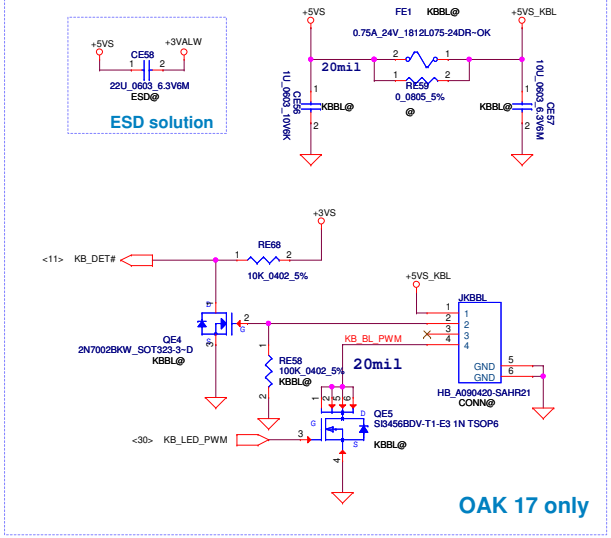
Webcam PWR CTRL



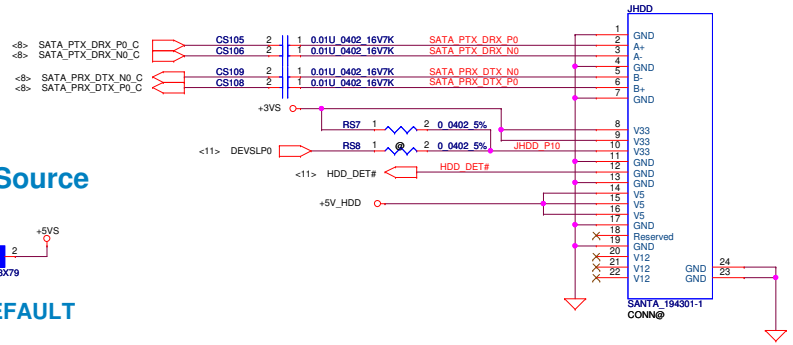
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: LVDS/webcam			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 31 of 57		

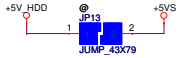
* Key Board Back Light



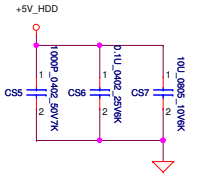
SATA HDD Connector



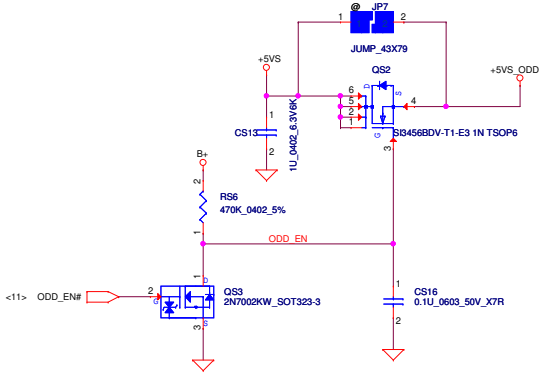
+5V_HDD Source



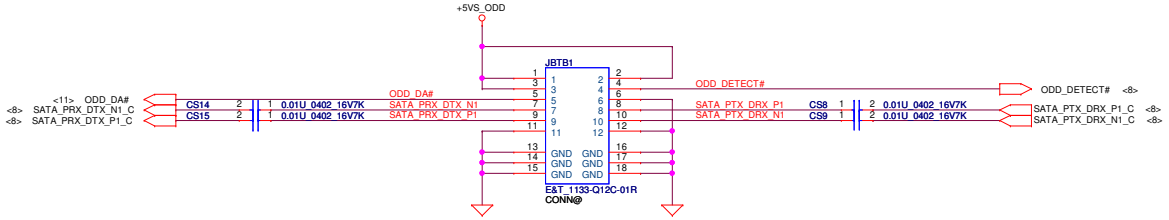
SHORT DEFAULT

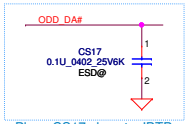


ODD Power Control

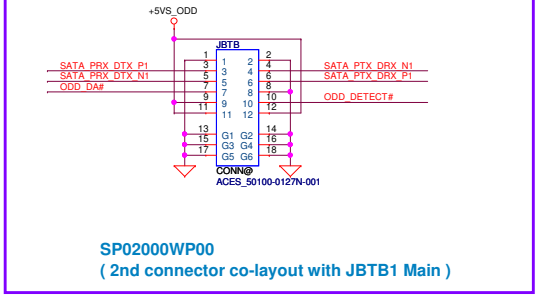


ODD BTB Connector

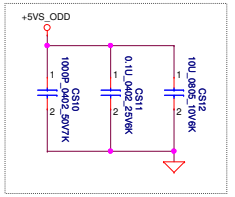




Place CS17 close to JBTB



SP02000WP00
(2nd connector co-layout with JBTB1 Main)



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

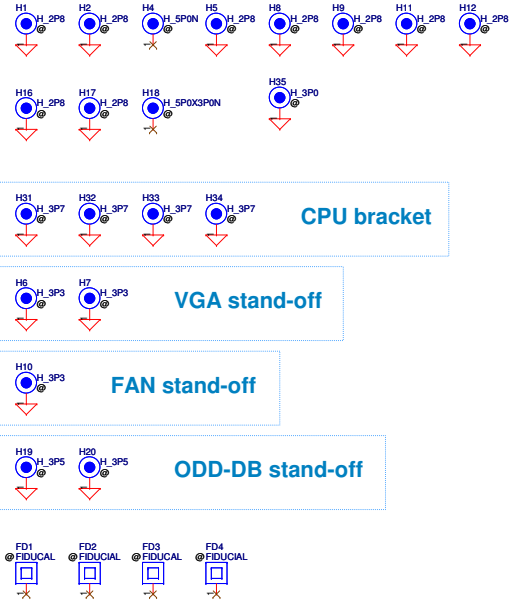
Compal Electronics, Inc.

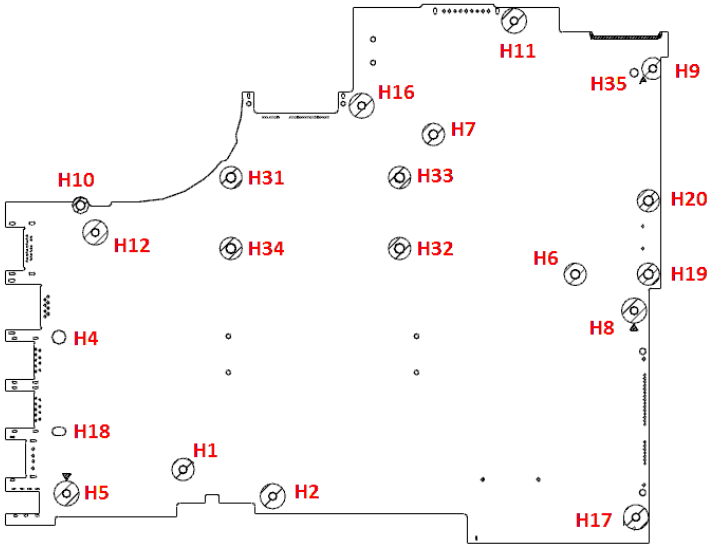
Title: HDD/ODD/KB-BL

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 32 of 57

Screw Hole





Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: Screw Hole			
Size	Document Number: LA-9984P		Rev: 1.0
Date: Wednesday, May 22, 2013	Sheet 33 of 57		

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
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31							
32							
33							
34							
35							
36							
37							
38							
39							
40							
41							

Compal Electronics, Inc.

Title: HW-PIR Page.1

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 34 of 57

Version Change List (P. I. R. List) Page 2

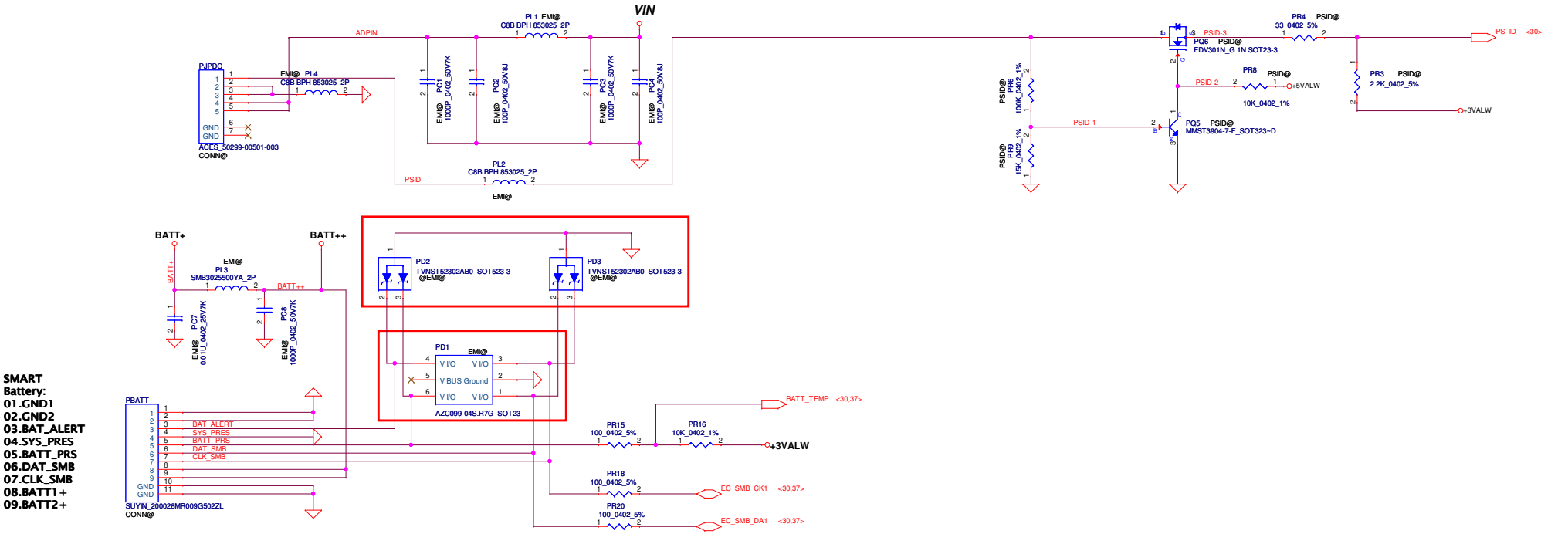
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							

Compal Electronics, Inc.

Title: HW-PIR Page.2

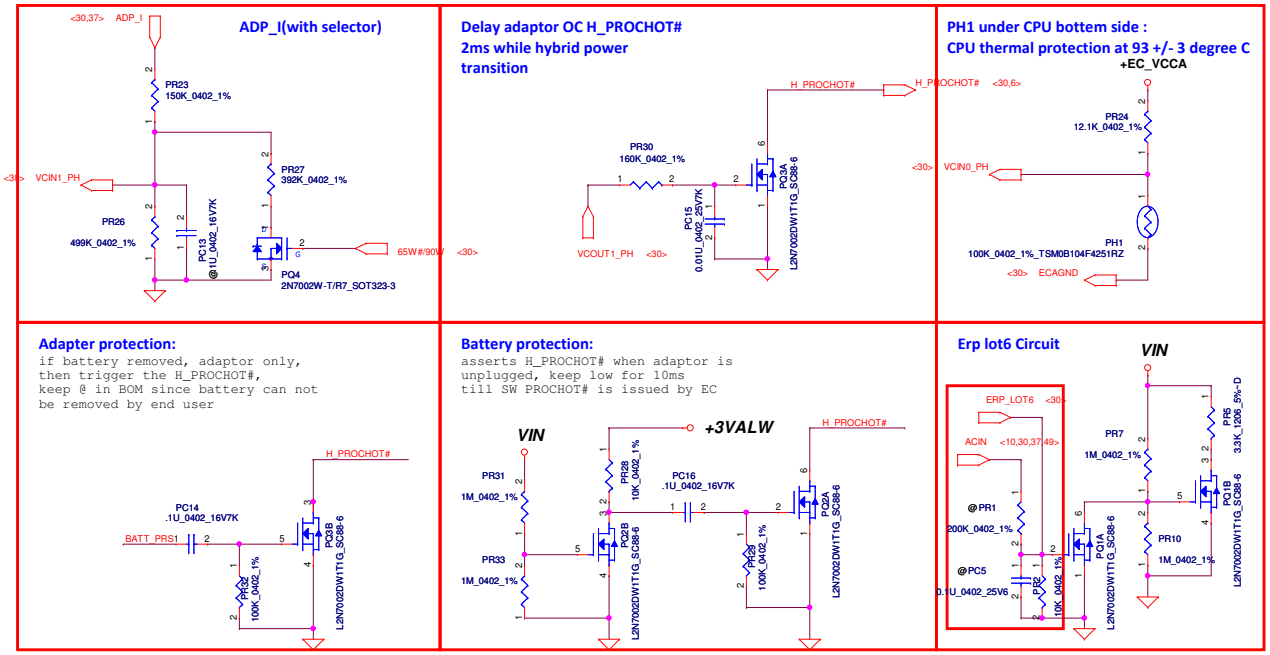
Size | Document Number: LA-9984P | Rev: 1.0

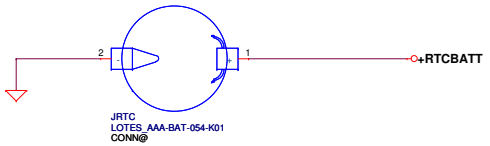
Date: Wednesday, May 22, 2013 | Sheet 35 of 57



SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

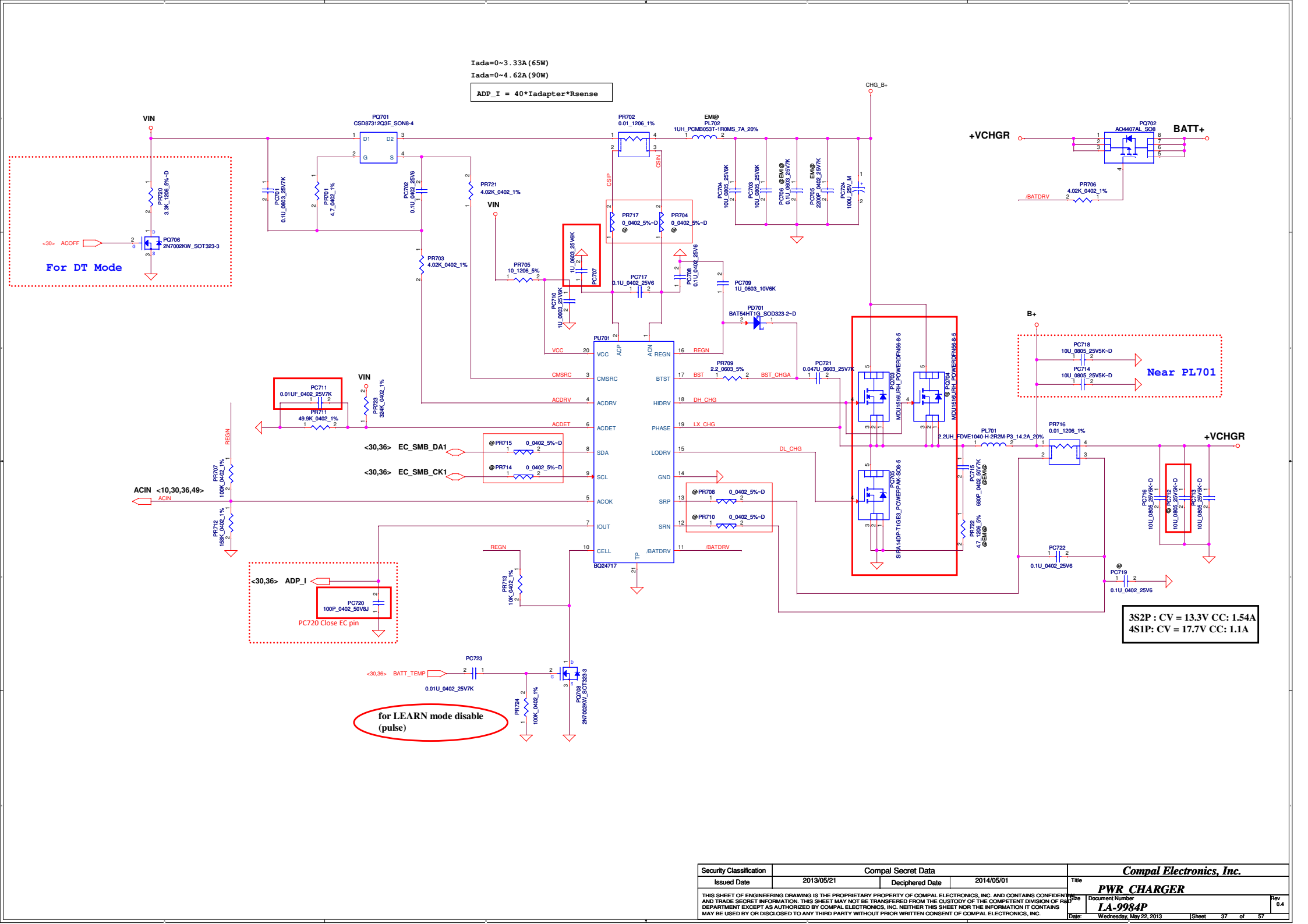
Other component (37.1)



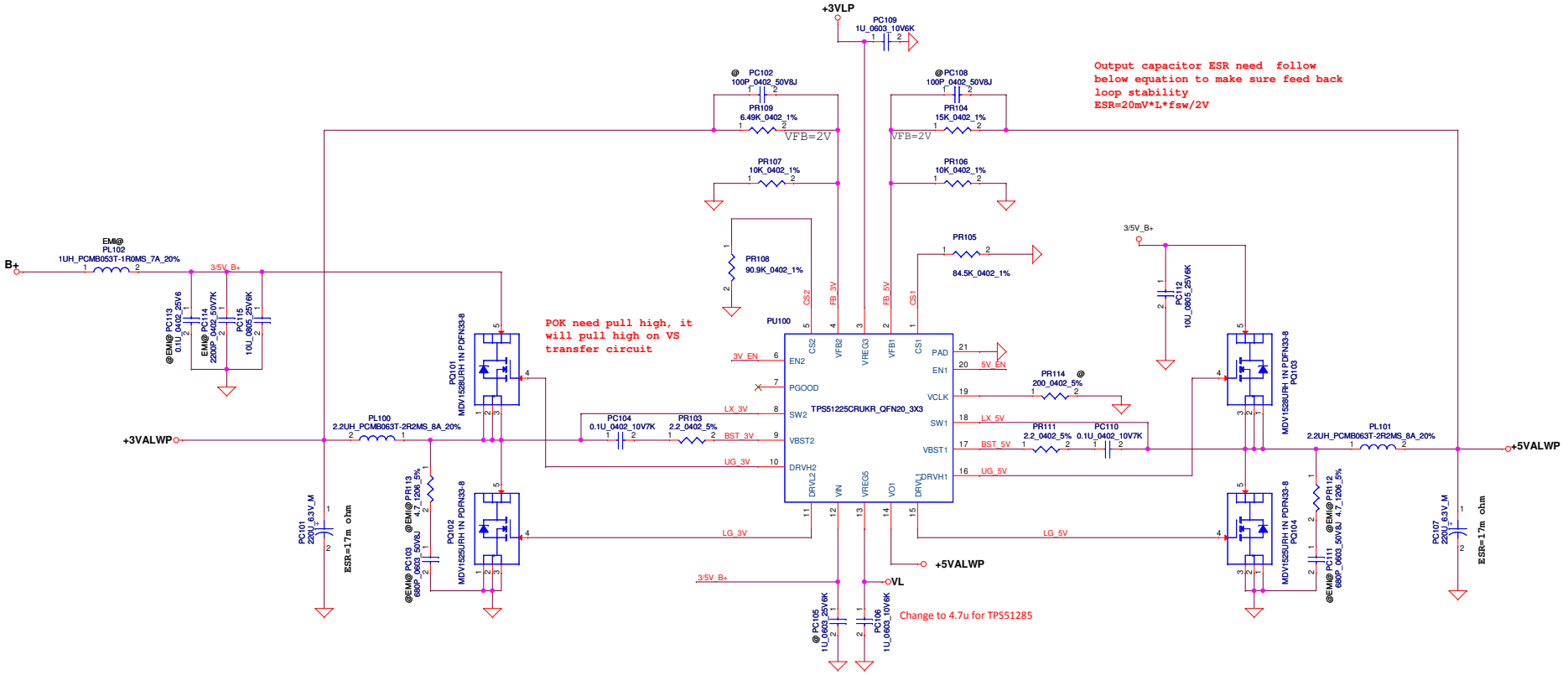


Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.	
Title	PWR_DCIN/BATT CONN/OTP
Size	Document Number: LA-9984P
Rev	0.4
Date:	Wednesday, May 22, 2013
Sheet	36 of 57

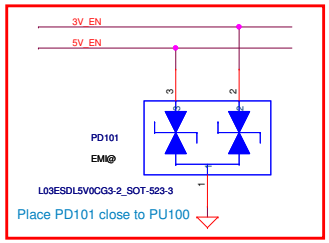


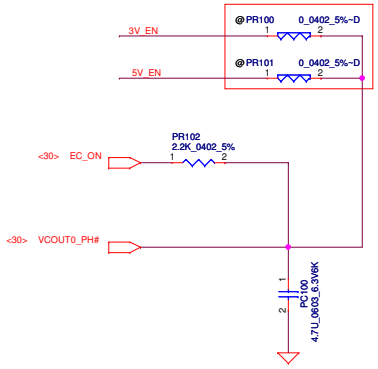
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date 2014/05/01	Title: PWR_CHARGER
Size	Document Number: LA-9984P		Rev: 0.4
Date: Wednesday, May 22, 2013	Sheet 37 of 57		

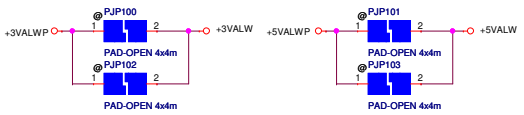


3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm







5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

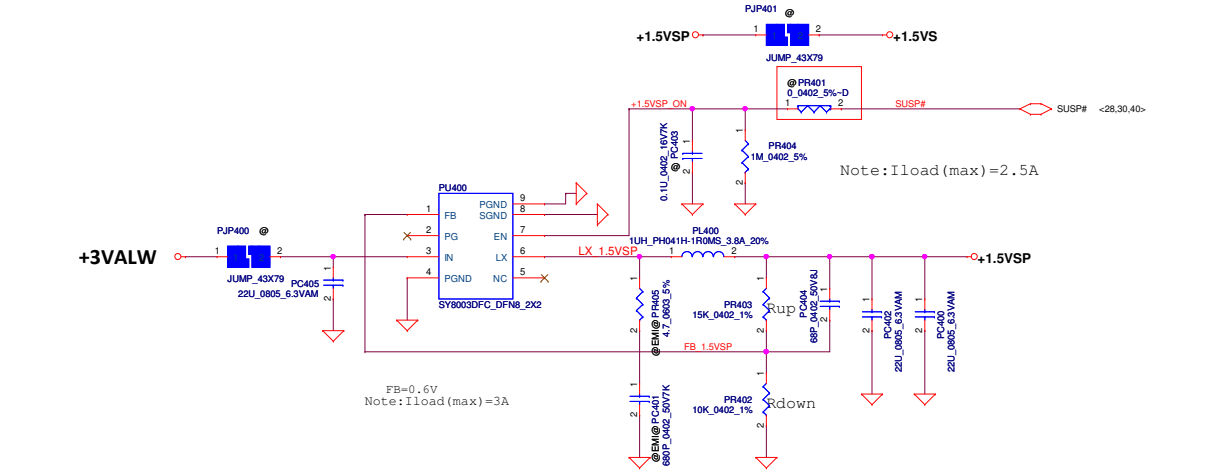
Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

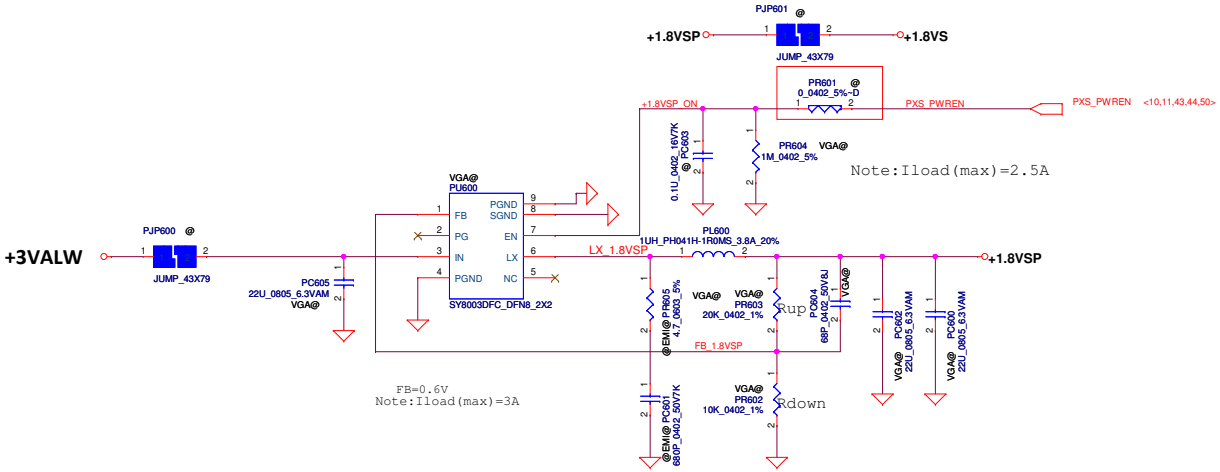
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-9984P | Rev: 0.4

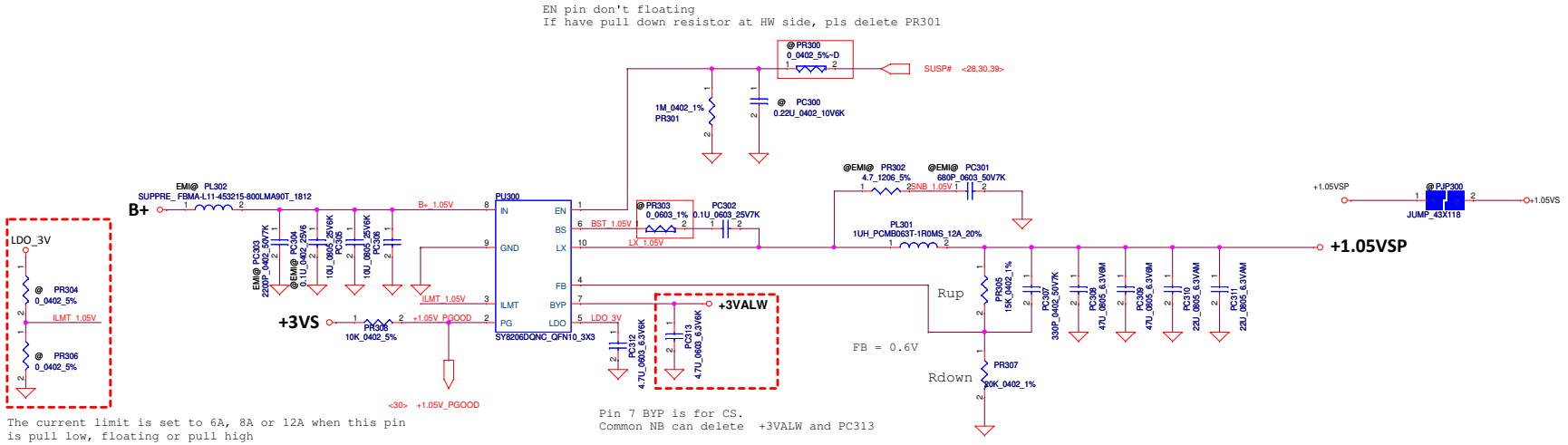
Date: Wednesday, May 22, 2013 | Sheet 38 of 57





Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.	
Title	PWR_1.5VSP / 1.8VSP
Size	Document Number: LA-9984P
Rev	0.4
Date:	Wednesday, May 22, 2013
Sheet	39 of 57

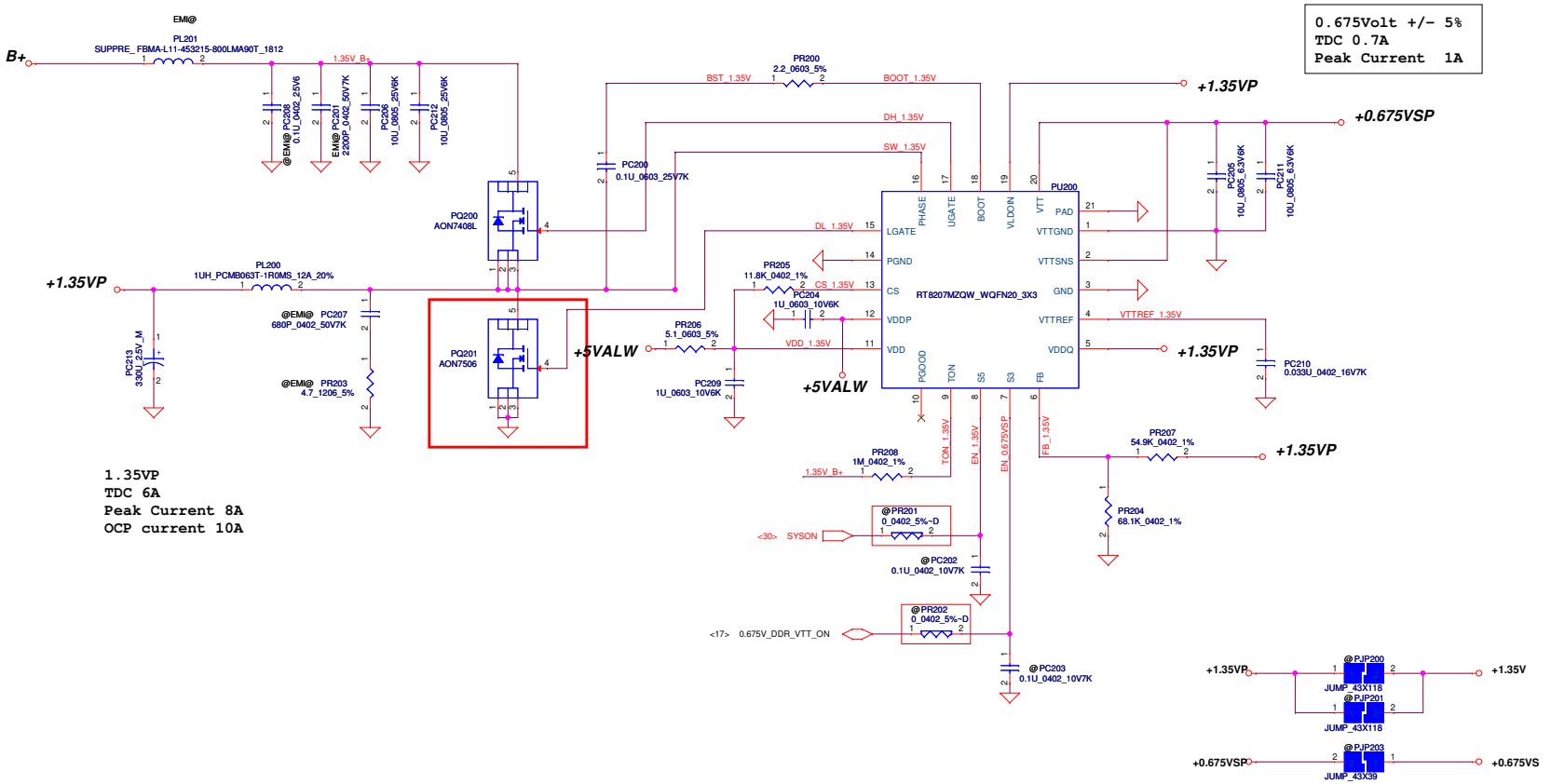


Compal Electronics, Inc.

Title: PWR_+VCCIO

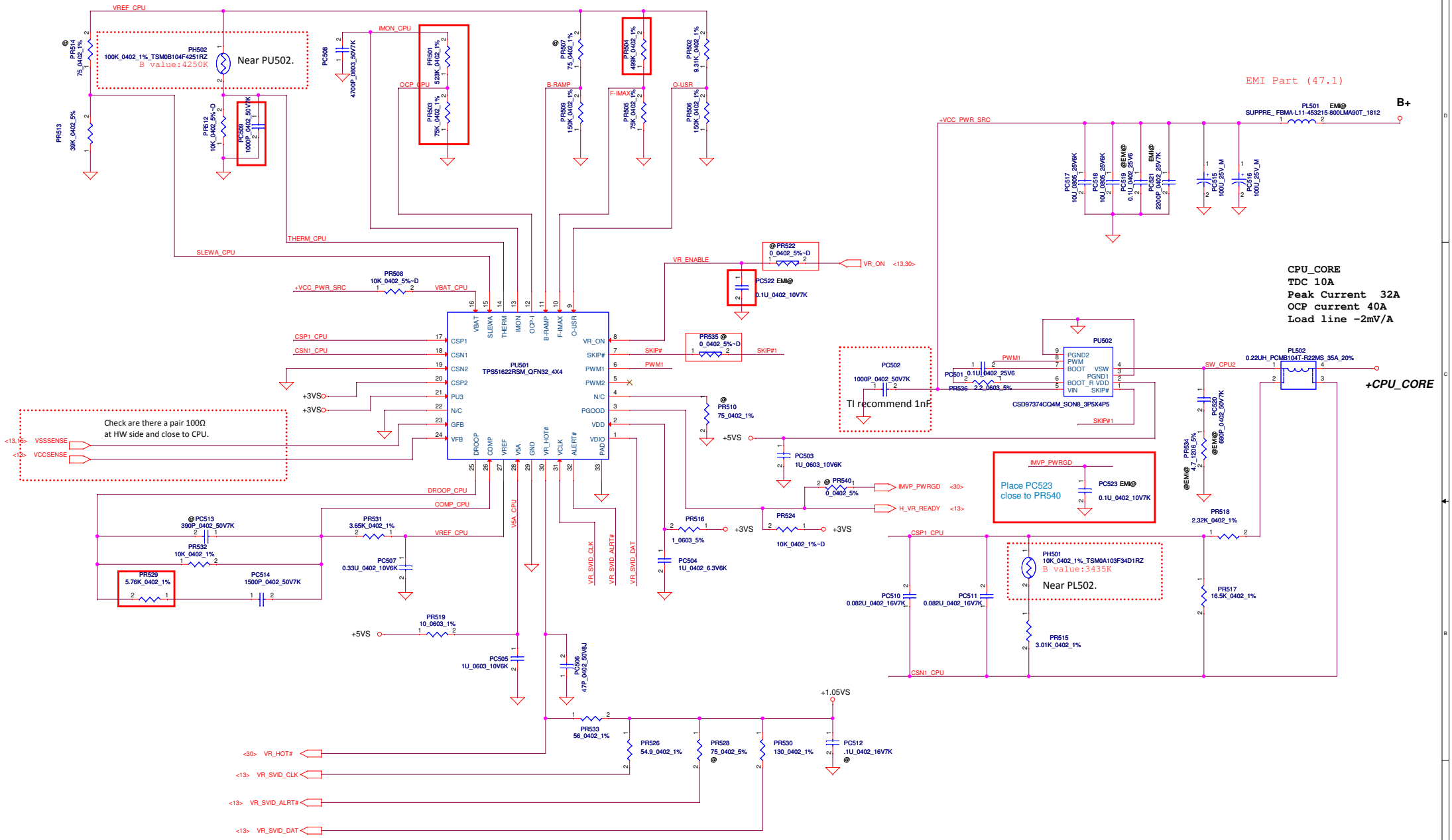
Size: C | Document Number | Rev: 0.4

Date: Wednesday, May 22, 2013 | Sheet 40 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.	
Title	PWR_+1.35VP/0.675VSP
Size	Document Number: LA-9984P
Rev	0.4
Date:	Wednesday, May 22, 2013
Sheet	41 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.

Title: PWR_VCORE

Size | Document Number: LA-9984P | Rev: 0.4

Date: Wednesday, May 22, 2013 | Sheet 42 of 57

TDC=9A
Peak Current=13A
OCP=16A

+3VS
@ PR1110 100K_0402_5%
PU1100 VGA@
PGOOD VBST
TRIP DRVH
EN SW
VFB VSIN
TST DRVL
TP
TPS51212DSCR_SON10_3X3
PR1102 VGA@ 154K_0402_1%
@PR1103 0_0402_5%~D
PXS_PWREN
TRIP +1.2VSP
EN +1.2VSP
FB +1.2VSP
RF +1.2VSP
BST +1.2VSP
UG +1.2VSP
SW +1.2VSP
LG +1.2VSP
VGA@ PR1101 2.2_0603_5%
VGA@ PC1103 0.1U_0603_25V7K
+1.2VSP_B+
VGA@_EMI@ PL1100 HCB2012KF-121T50_0805
B+
PC1100 0.1U_0402_25V6
PC1101 2200P_0402_50V7K
PC1102 10U_0805_25V6K
VGA@ PQ1100 AON7408L
@PJP1100 JUMP_43X118
@PJP1101 JUMP_43X118
+1.35VGPUP
+1.35VS_VGA
VGA@ PL1101 1UH_PCMB063T-1R0MS_12A_20%
+1.35VGPUP
PC1104 @ 0.1U_0402_16V7K
PR1105 VGA@ 470K_0402_1%
VGA@ PC1105 1U_0603_10V6K
+5VALW
VGA@ PQ1101 AON7506
PR1104 @EMI@ 4.7_1206_5%
PC1106 @EMI@ 680P_0402_50V7K
VGA@ PC1108 330U_2.5V_M
PR1107 VGA@ 9.09K_0402_1%
PR1108 VGA@ 10K_0402_1%

	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

@PR1206 0_0402_5%~D
PXS_PWREN
PXS_PWREN <10,11,39,44,50>
1M_0402_1% PR1201 VENUS@
@ PC1200 0.22U_0402_10V6K
+VDDCIP
@PJP1200 JUMP_43X118
+VDDCI

VENUS@_EMI@ PL1201 SUPPRE_FBMA-L11-453215-800LMA90T_1812
B+
PU1200
IN EN
BS
GND LX
FB
ILMT BYP
PG LDO
SY8208DQNC_QFN10_3X3
VENUS@
B+_VDDCI
BST_VDDCI
LX_VDDCI
ILMT_VDDCI
LDO_3V_VDDCI
@PR1200 0_0603_1%
VENUS@ PC1210 0.1U_0603_25V7K
VENUS@ PC1209 2200P_0402_50V7K
@EMI@ PC1203 0.1U_0402_25V6
VENUS@ PC1202 10U_0805_25V6K
VENUS@ PC1204 10U_0805_25V6K
VENUS@ PC1213 4.7U_0603_6.3V6K
VENUS@ PC1205 4.7U_0603_6.3V6K
+3VALW
@EMI@ PR1207 4.7_1206_5%
@EMI@ PC1212 680P_0603_50V7K
SNB_VDDCI
VENUS@ PL1200 1UH_PCMB063T-1R0MS_12A_20%
+VDDCIP
+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A
Rup
VENUS@ PR1209 10K_0402_1%
@PR1210 0_0402_5%~D
VDDCI_SEN <52>
PR1211 VENUS@ 120K_0402_1%
Rdown
VENUS@ PR1204 20K_0402_1%
PQ1201 VENUS@ 2N7002W-T/R7_SOT323-3
+3VGS
PR1213 VENUS@ 10K_0402_5%
PR1212 VENUS@ 10K_0402_5%
GPU_GPIO6 <49>
@ PC1214 4700P_0402_25V7K
PR1214 @ 100K_0402_5%
VENUS@ PR1208 10_0402_5%
VENUS@ PC1211 47U_0805_6.3V6M
VENUS@ PC1207 47U_0805_6.3V6M
VENUS@ PC1201 22U_0805_6.3V6M
VENUS@ PC1206 22U_0805_6.3V6M

LDO_3V_VDDCI
VENUS@ PR1203 0_0402_5%
ILMT_VDDCI
@ PR1202 0_0402_5%

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

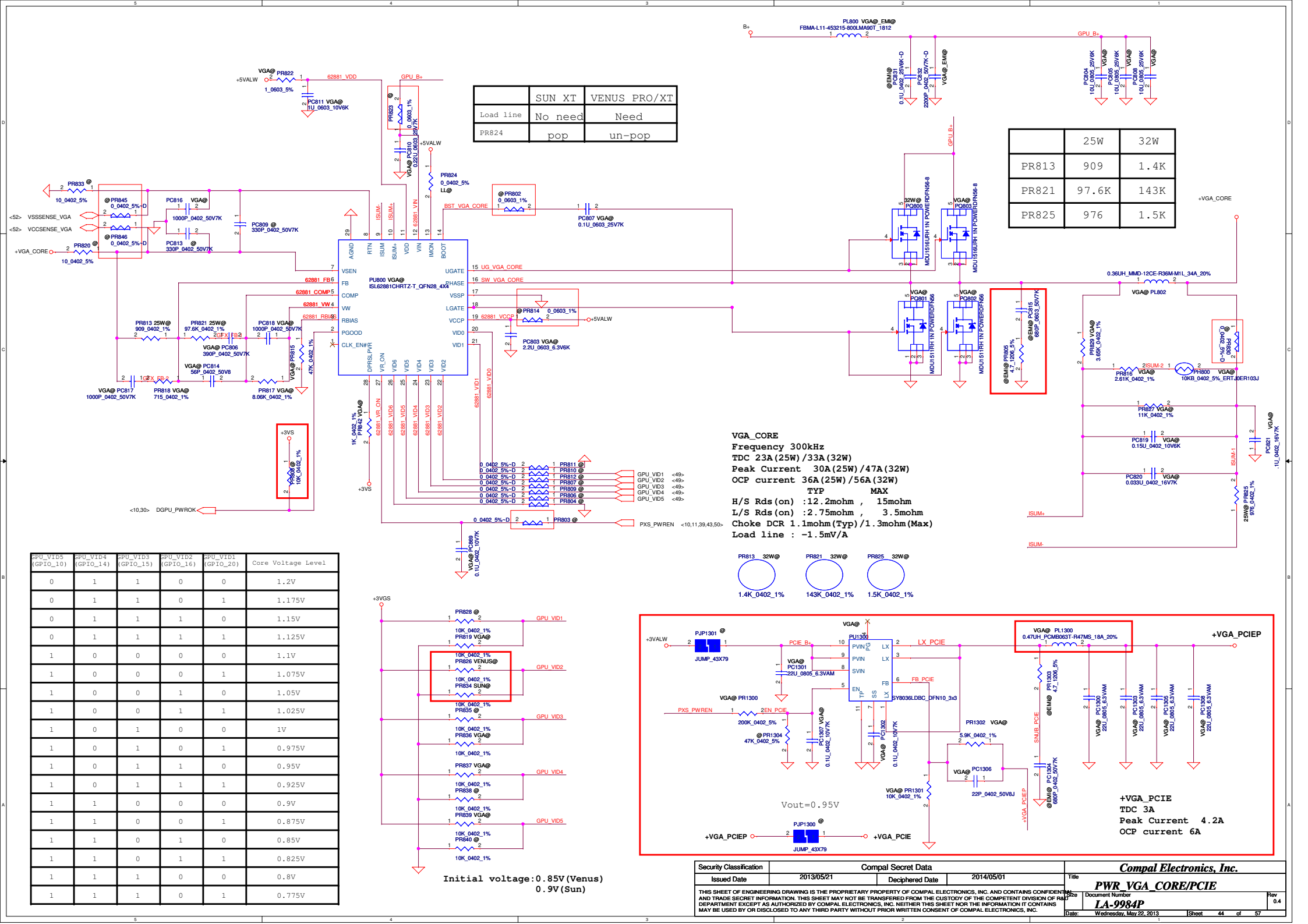
FB = 0.6V

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.
Title: PWR +1.35VGPU/VDDCIP
Size: | Document Number: LA-9984P | Rev: 0.4
Date: Wednesday, May 22, 2013 | Sheet 43 of 57



	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A(25W)/33A(32W)
Peak Current 30A(25W)/47A(32W)
OCP current 36A(25W)/56A(32W)

	TYP	MAX
H/S Rds(on)	12.2mohm ,	15mohm
L/S Rds(on)	2.75mohm ,	3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)
Load line : -1.5mV/A

PR813 32W@ 1.4K_0402_1%
PR821 32W@ 143K_0402_1%
PR825 32W@ 1.5K_0402_1%

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

Initial voltage:0.85V(Venus)
0.9V(Sun)

+VGA_PCIE
TDC 3A
Peak Current 4.2A
OCP current 6A

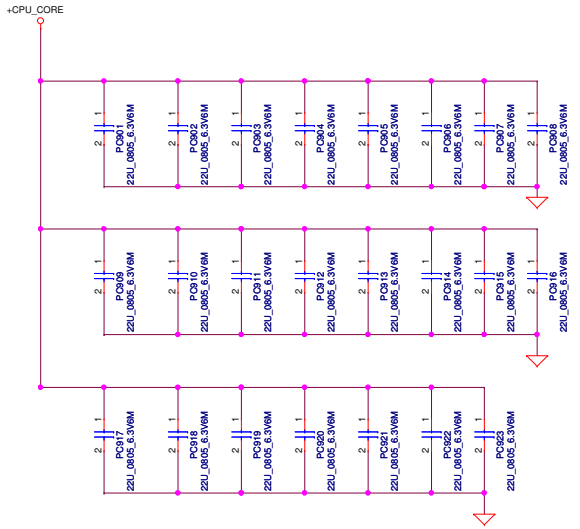
Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

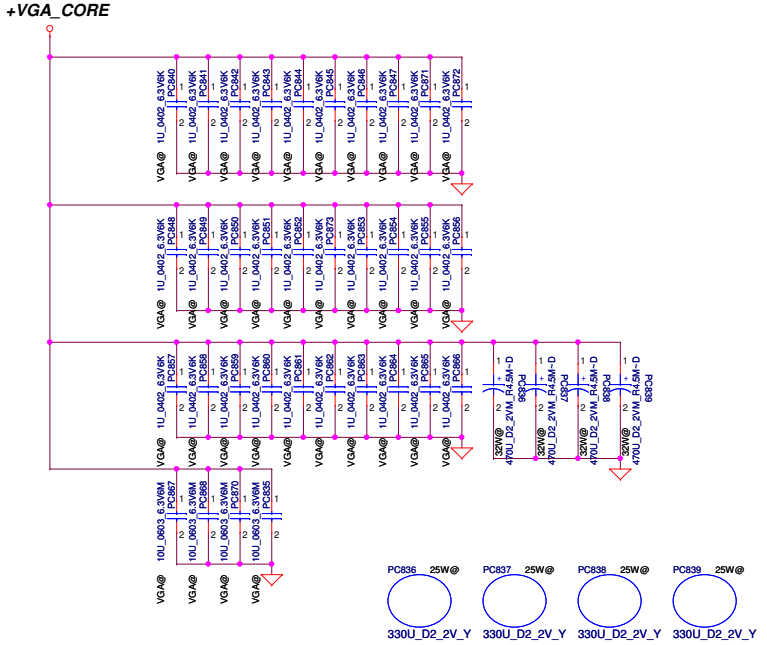
Compal Electronics, Inc.

Title: PWR_VGA_CORE/PCIE

Size: | Document Number: LA-9984P | Rev: 0.4

Date: Wednesday, May 22, 2013 | Sheet 44 of 57

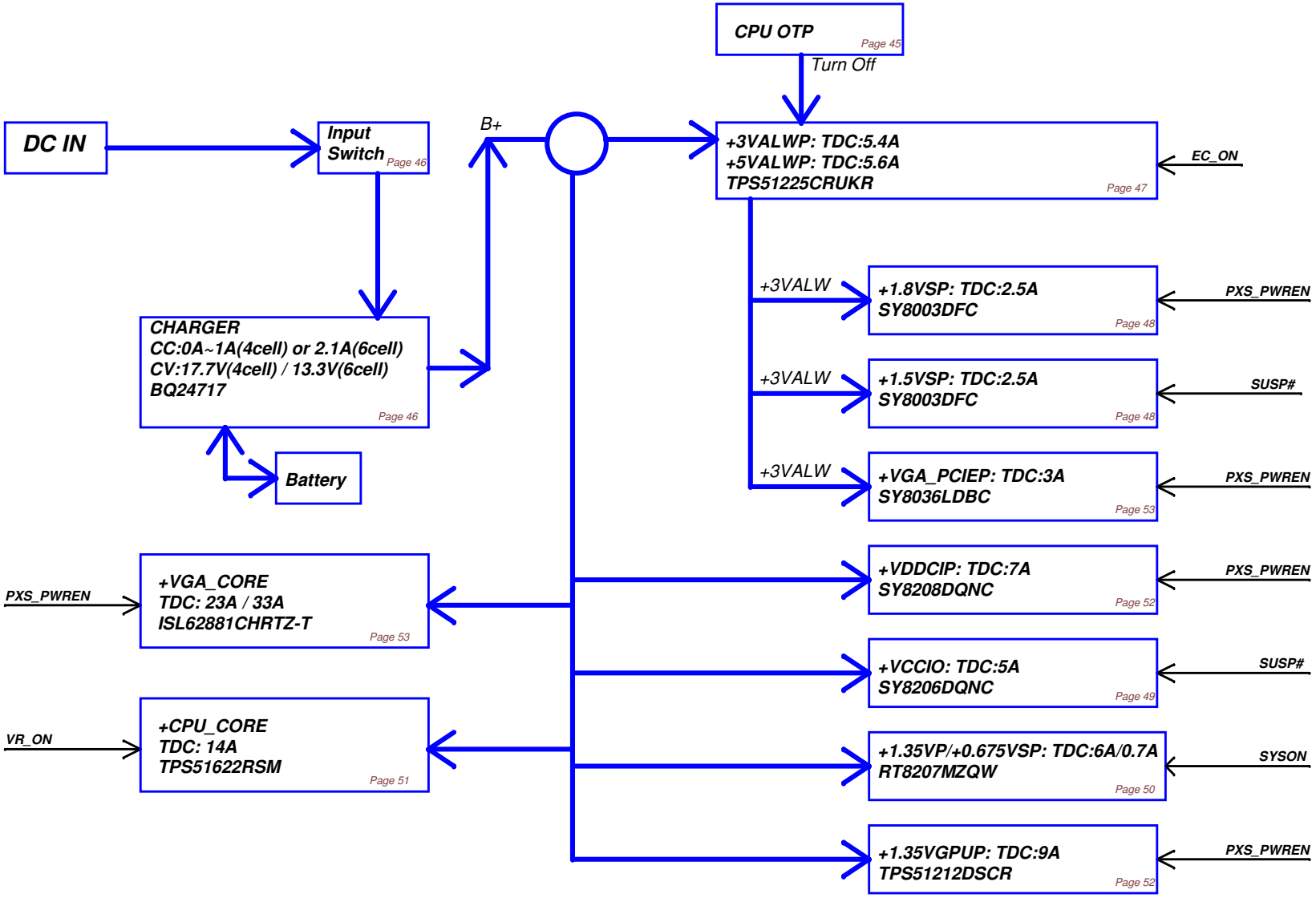




Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.			
Title: PWR_PROCESSOR DECOUPLING			
Size	Document Number: LA-9984P		Rev: 0.4
Date: Wednesday, May 22, 2013	Sheet 45 of 57		

Power block



Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
	LA-9984P		0.4
Date:	Wednesday, May 22, 2013	Sheet	46 of 57

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.3
8	37 38 39 40 41 42	CHARGER 3.3VALWP/5VALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100,PR101,PR201,PR202,PR300,PR303,PR401,PR522,PR535, PR704,PR708,PR710,PR714,PR715,PR717	0.4
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	0.4
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	0.4
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601,PR802,PR803,PR814,PR823,PR830,PR845,PR846, PR1103,PR1200,PR1206,PR1210	0.4
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EEverify ok only for Sun XT	unpop PL1200,PL1201,PU1200,PQ1201,PR1201,PR1203,PR1204,PR1208,PR1209, PR1211,PR1212,PR1213,PC1201,PC1202,PC1204,PC1205,PC1206,PC1207, PC1209,PC1210,PC1211,PC1213 (only for Sun XT)	0.4
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	0.4
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10Kohm	0.4
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	0.4

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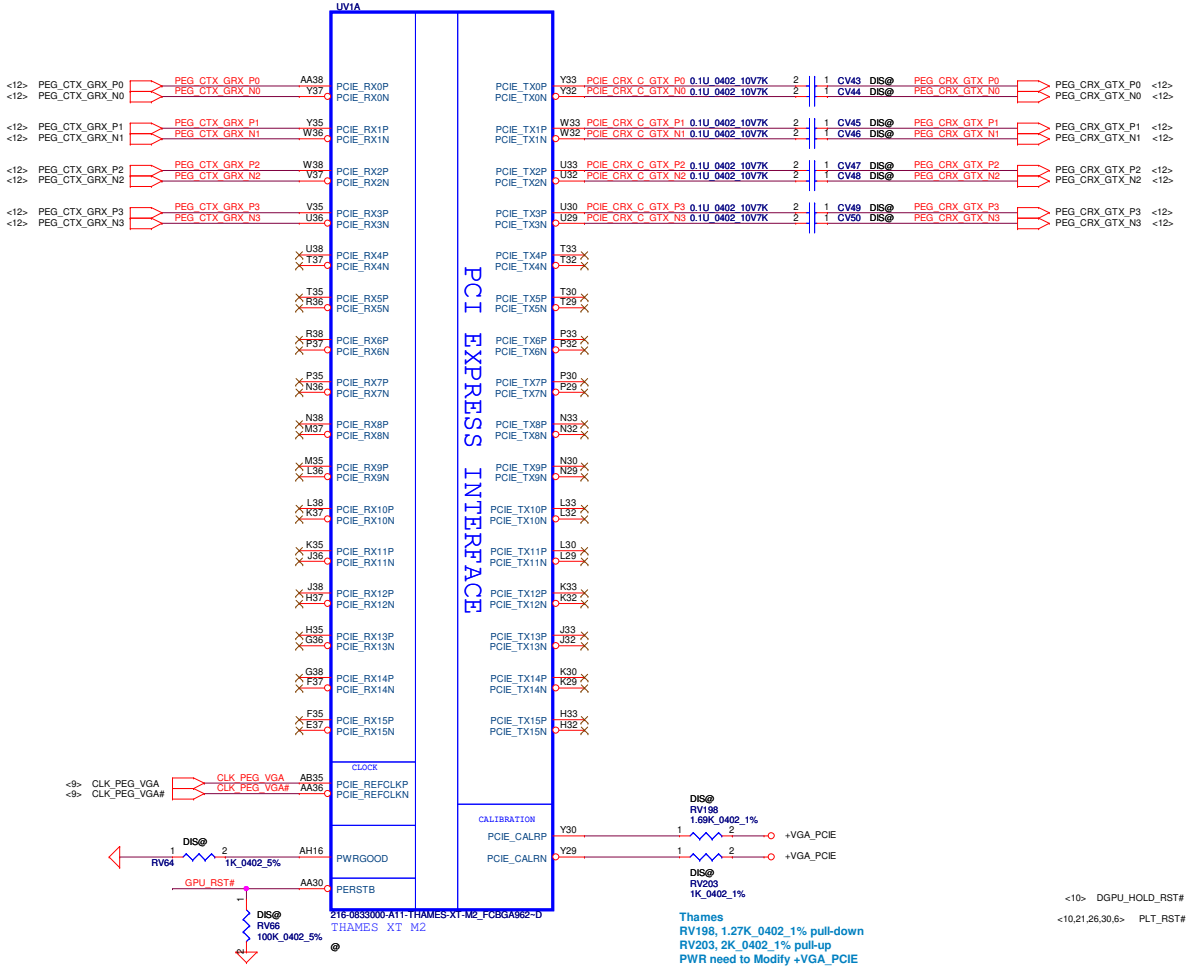
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.			
Title: PWR-PIR			
Size	Document Number: LA-9984P		Rev: 0.4
Date: Wednesday, May 22, 2013	Sheet 47 of 57		

GFX PCIE LANE REVERSAL



Thames
RV198, 1.27K_0402_1% pull-down
RV203, 2K_0402_1% pull-up
PWR need to Modify +VGA_PCIE

UV1 VENUSXT@

216-0846000 A1 VENUS XT M2 FCBGA 962P 0FD

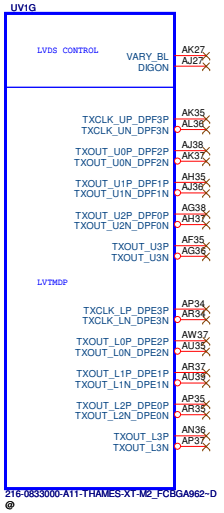
SA00006KW0L

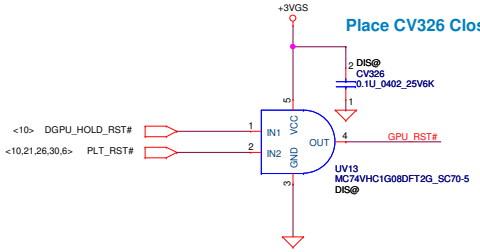
UV1 VENUSPRO@

216-0846009 A1 VENUS PRO M2 FCBGA 962P 0FD

SA00006MW0L

LVDS Interface





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Title	ATI_Venus Pro_M2_PCIE/LVDS		
Size	Document Number	LA-9984P	Rev 1.0
Date:	Wednesday, May 22, 2013	Sheet 48 of 57	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalt setting for desktop)

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
* 128Mx16bits (64Mx32bits) GDDR5 Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3)	RV67 1	RV69 1	RV71 1
128Mx16bits (64Mx32bits) GDDR5 Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV68 0	RV69 1	RV71 1
	RV67 1	RV70 0	RV71 1
128MX16bits DDR3 Hynix 1Gb SA00006H40L(R1) SA00006H41L(R3)			
128MX16bits DDR3 Samsung 1Gb SA00005SH0L(R1) SA00005SH1L(R3)			
128MX16bits DDR3 Micron 1Gb SA00005XB0L(R1) SA00005XB1L(R3)			

SUN MLPs PS_3	RV241	RV242	Bits [3:1]
* Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs
PS_3 used default

SUN internal VGA Thermal Sensor
Address 0x714

Address:100_1101b
Main : SA000012710
2nd : SA0000 3PU00

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_Main_MSIC

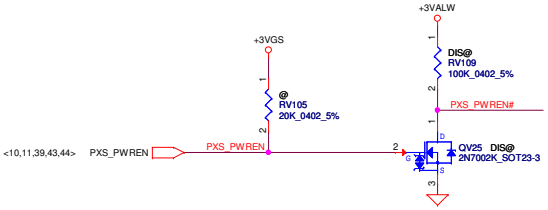
Size: | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 49 of 57

PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

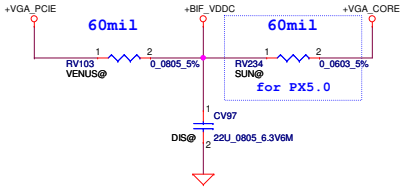
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

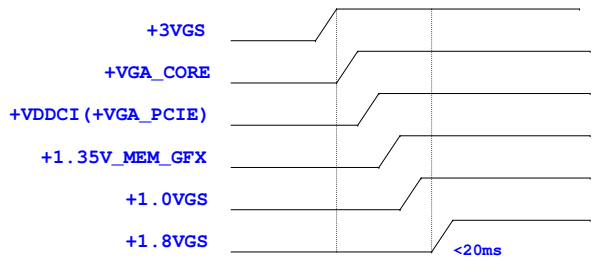


for PX4.0 and PX5.0

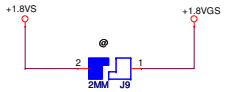
Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode



Power seguence of Sun XT,Venus Pro,Venus XT

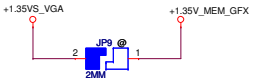


+1.8VS TO +1.8VGS



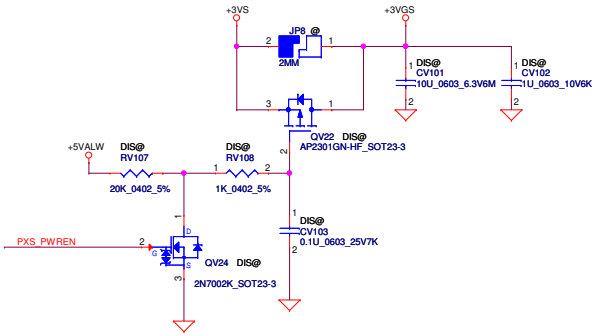
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX

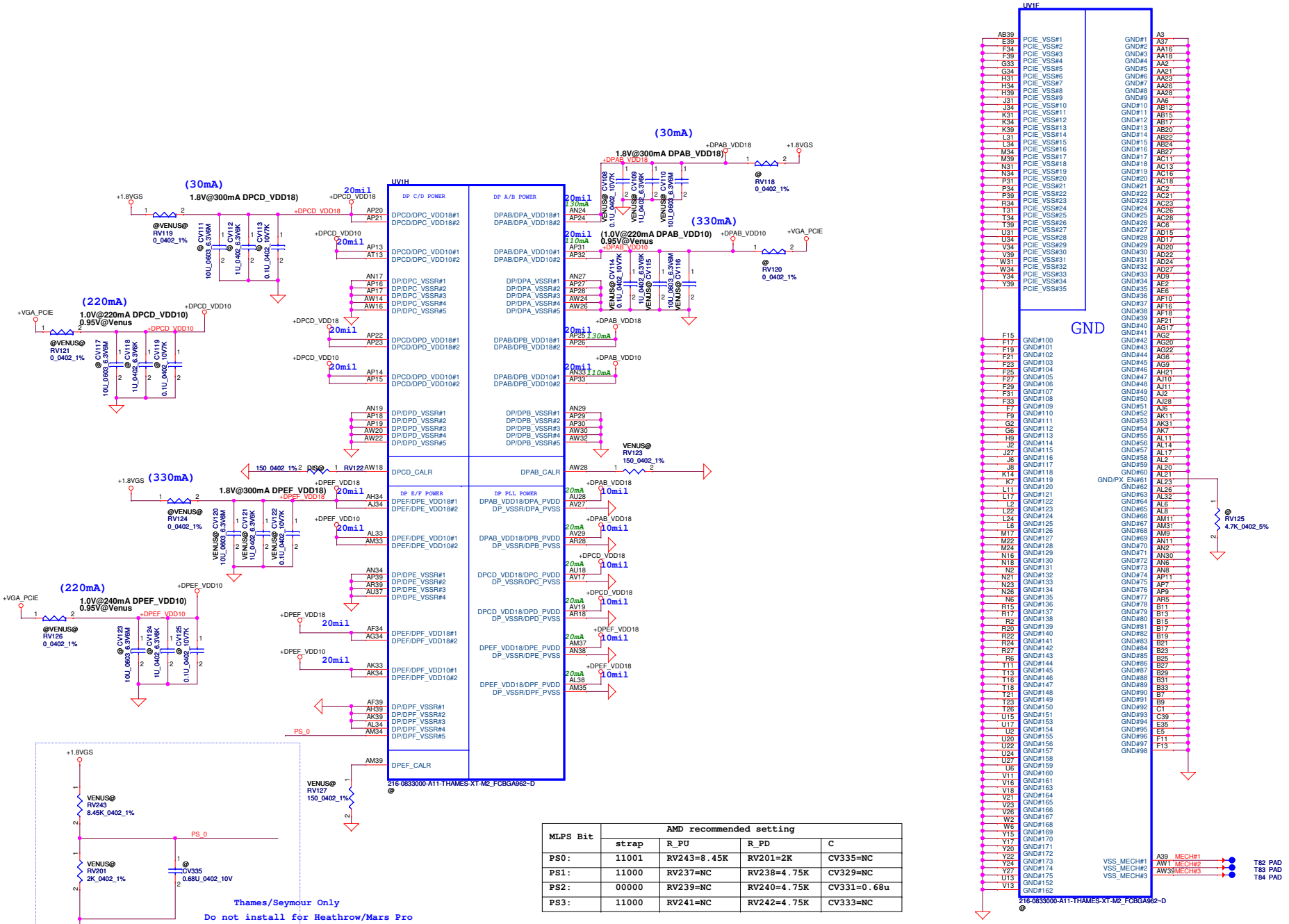


SHORT DEFAULT

+3VS TO +3VGS



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: ATI_Venus Pro_M2_BACO POWER
				Size: Document Number: LA-9984P Rev: 1.0
				Date: Wednesday, May 22, 2013 Sheet 50 of 57



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

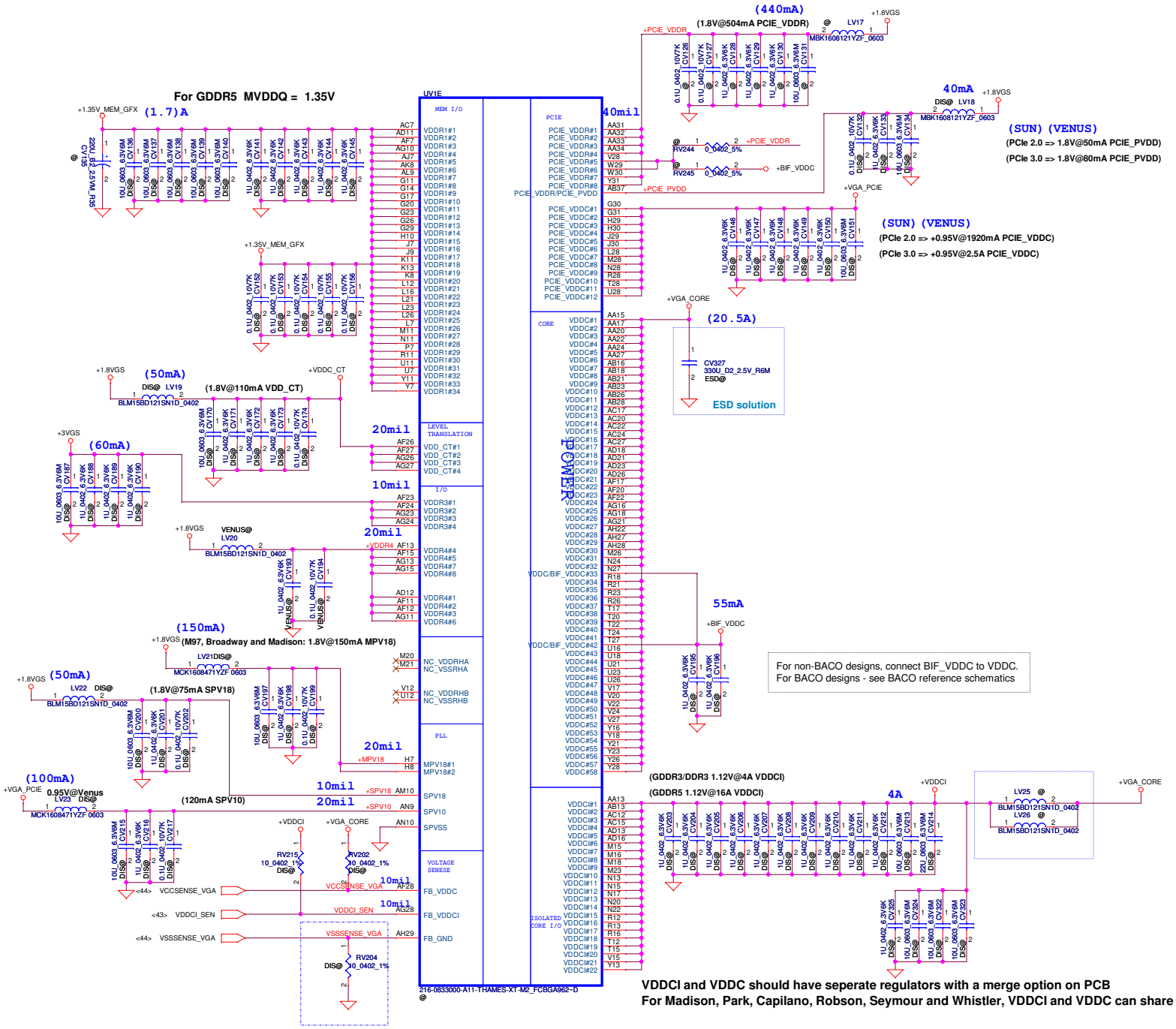
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_PWR_GND

Size: | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 51 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_Power

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 52 of 57

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A12_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil 5mil

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

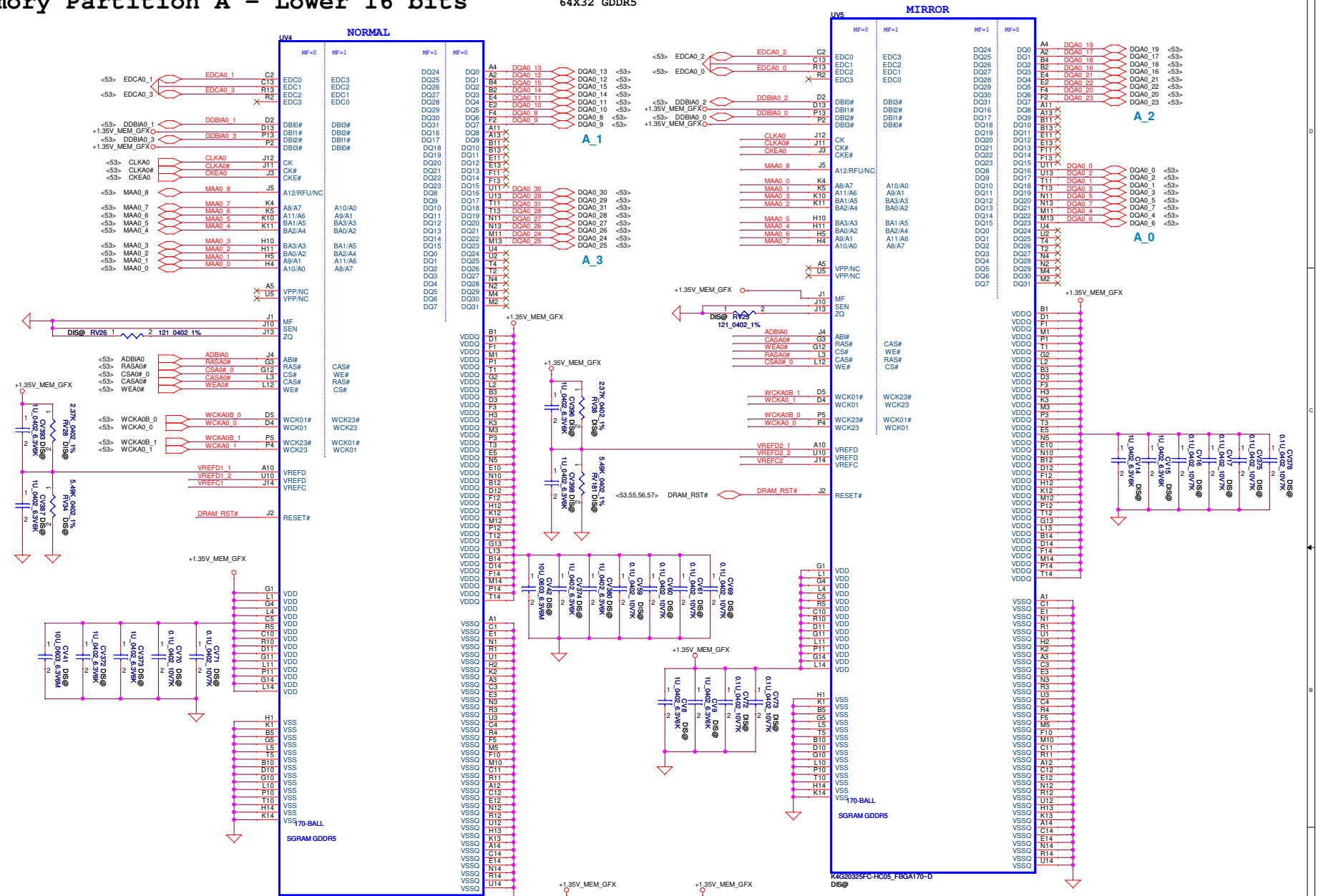
Title: ATI_Venus Pro_M2_MEM IF

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 53 of 57

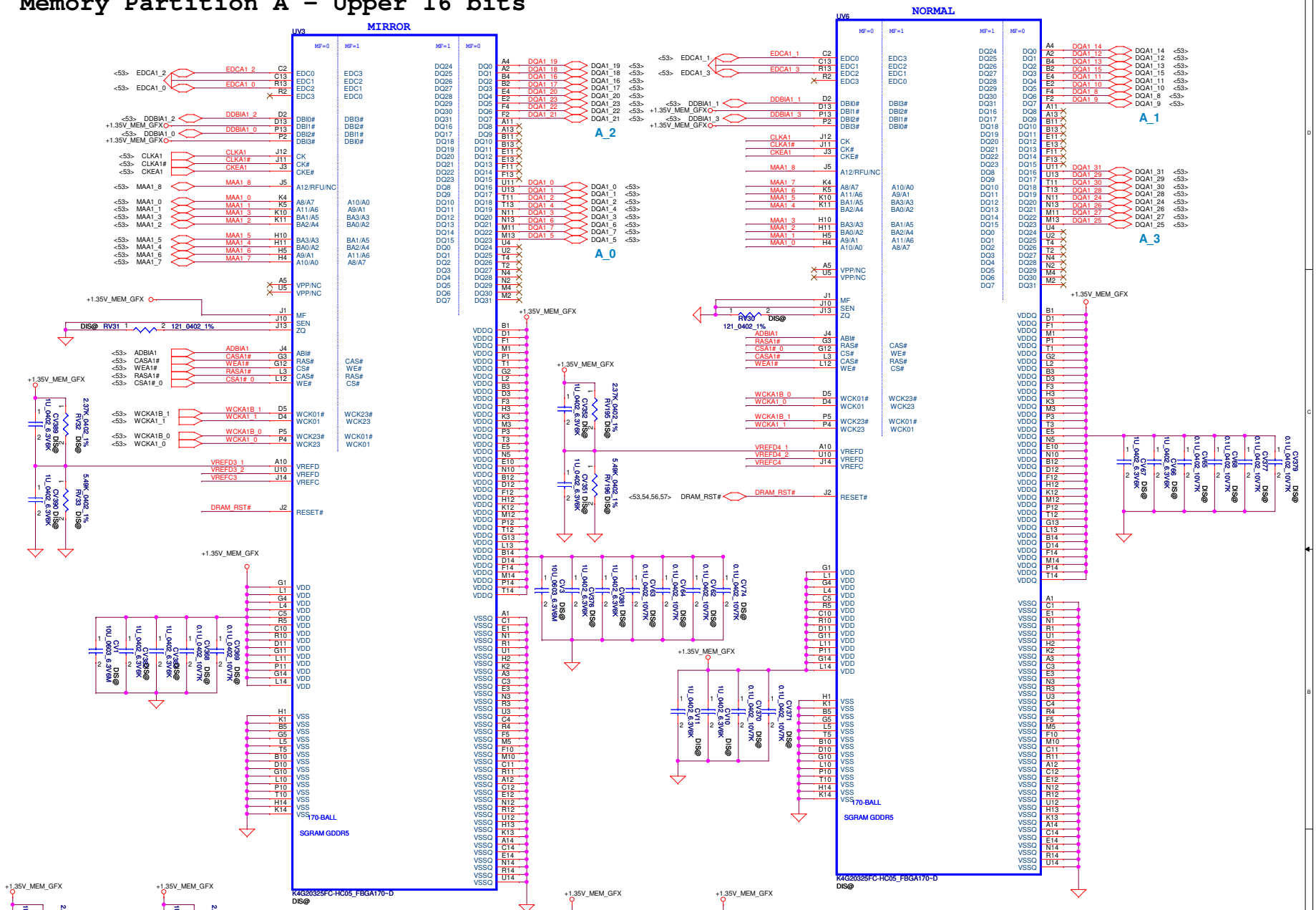
Memory Partition A – Lower 16 bits

64X32 GDDR5



Compal Electronics, Inc.	
Title	VRAM_A Lower_UV4,UV5
Size	Document Number: LA-9984P
Rev	1.0
Date:	Wednesday, May 22, 2013
Sheet	54 of 57

Memory Partition A – Upper 16 bits



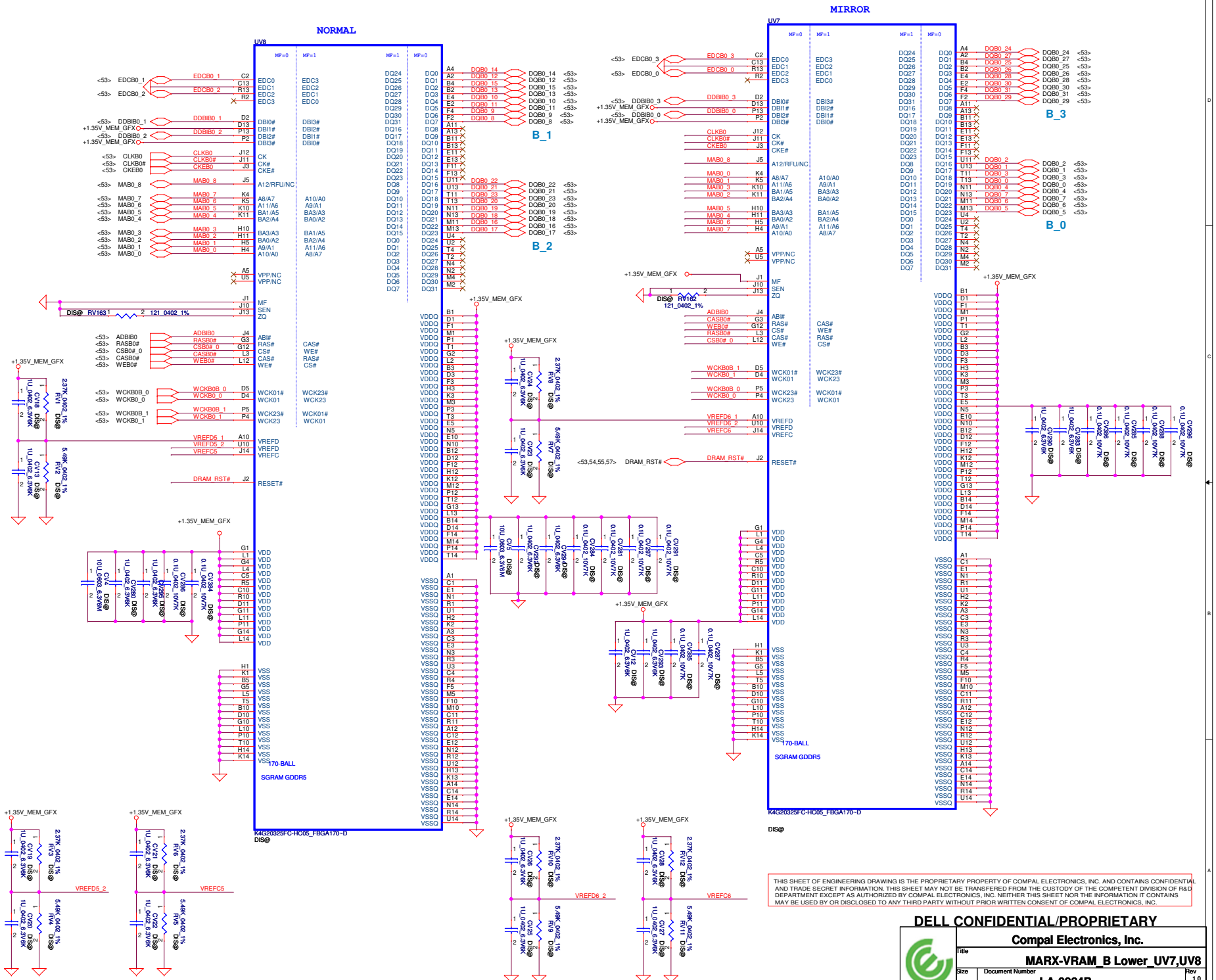
Compal Electronics, Inc.

Title: MARX-VRAM_A Upper_UV3,UV6

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 55 of 57

Memory Partition B - Lower 16 bits



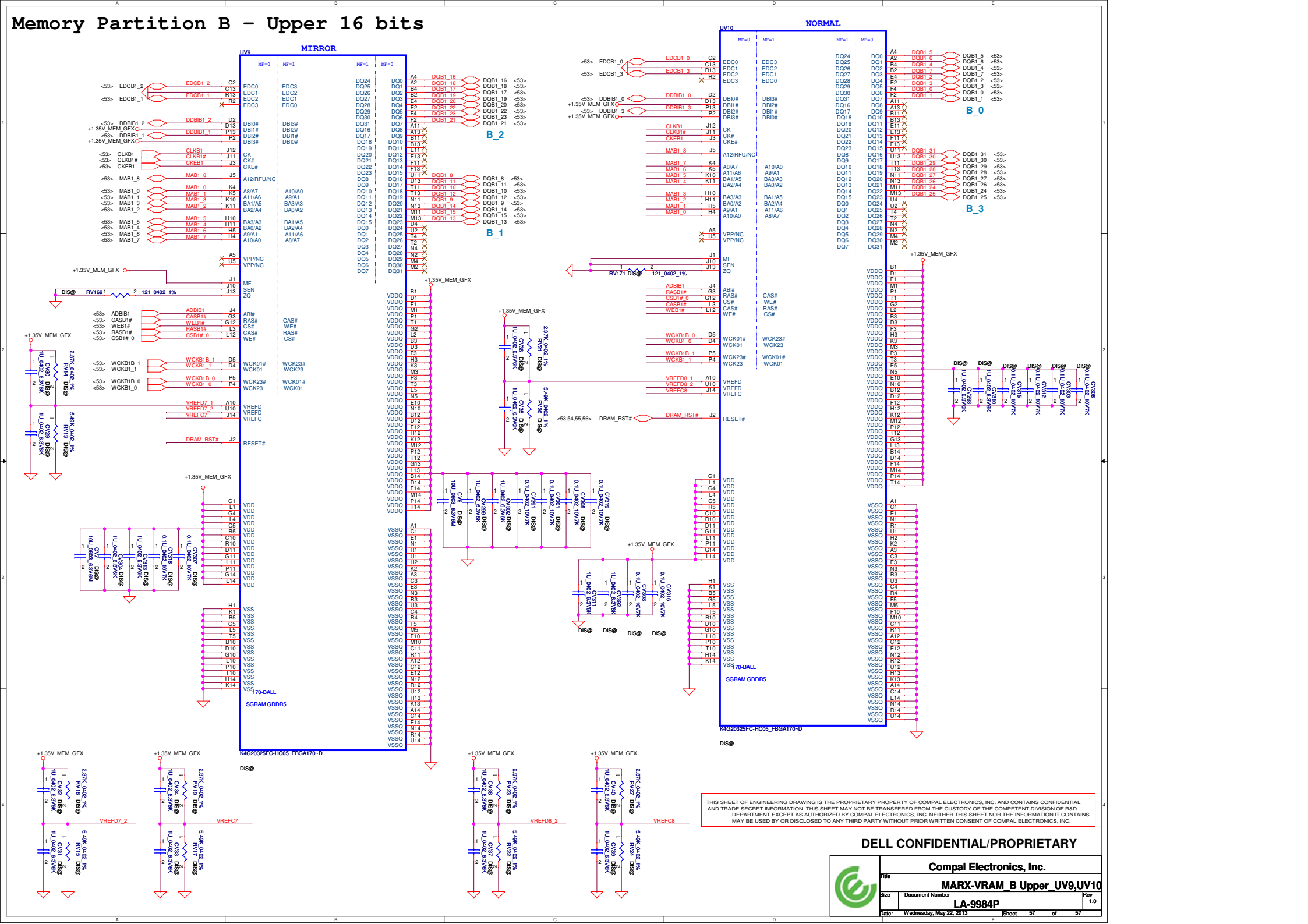
Compal Electronics, Inc.

Title: MARX-VRAM_B Lower_UV7,UV8

Size | Document Number: LA-9984P | Rev: 1.0

Date: Wednesday, May 22, 2013 | Sheet 56 of 57

Memory Partition B – Upper 16 bits



Compal Electronics, Inc.	
Title	MARX-VRAM_B Upper_UV9,UV10
Size	Document Number: LA-9984P
Rev	1.0
Date:	Wednesday, May 22, 2013
Sheet	57 of 57