Compal Confidential

Intel Haswell rPGA Processor with Lynx Point-H

Viper MXM

Date : 2012/12/20
Version 0.5

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: Cover Page
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				Date: Thursday, December 20, 2012 / Sheet 1 of 56

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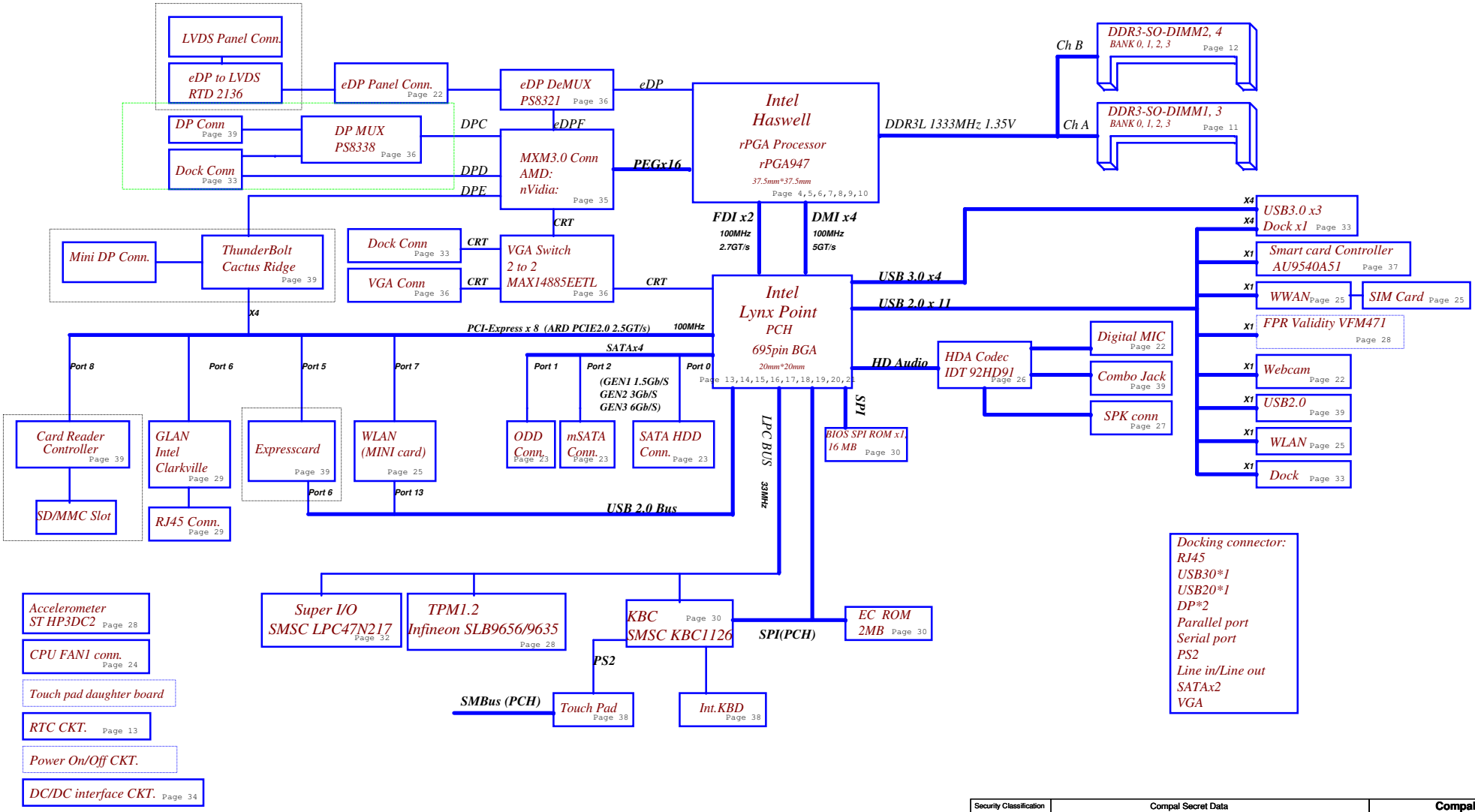
Model Name :

File Name :



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			Date: Thursday, December 20, 2012; Sheet 2 of 56

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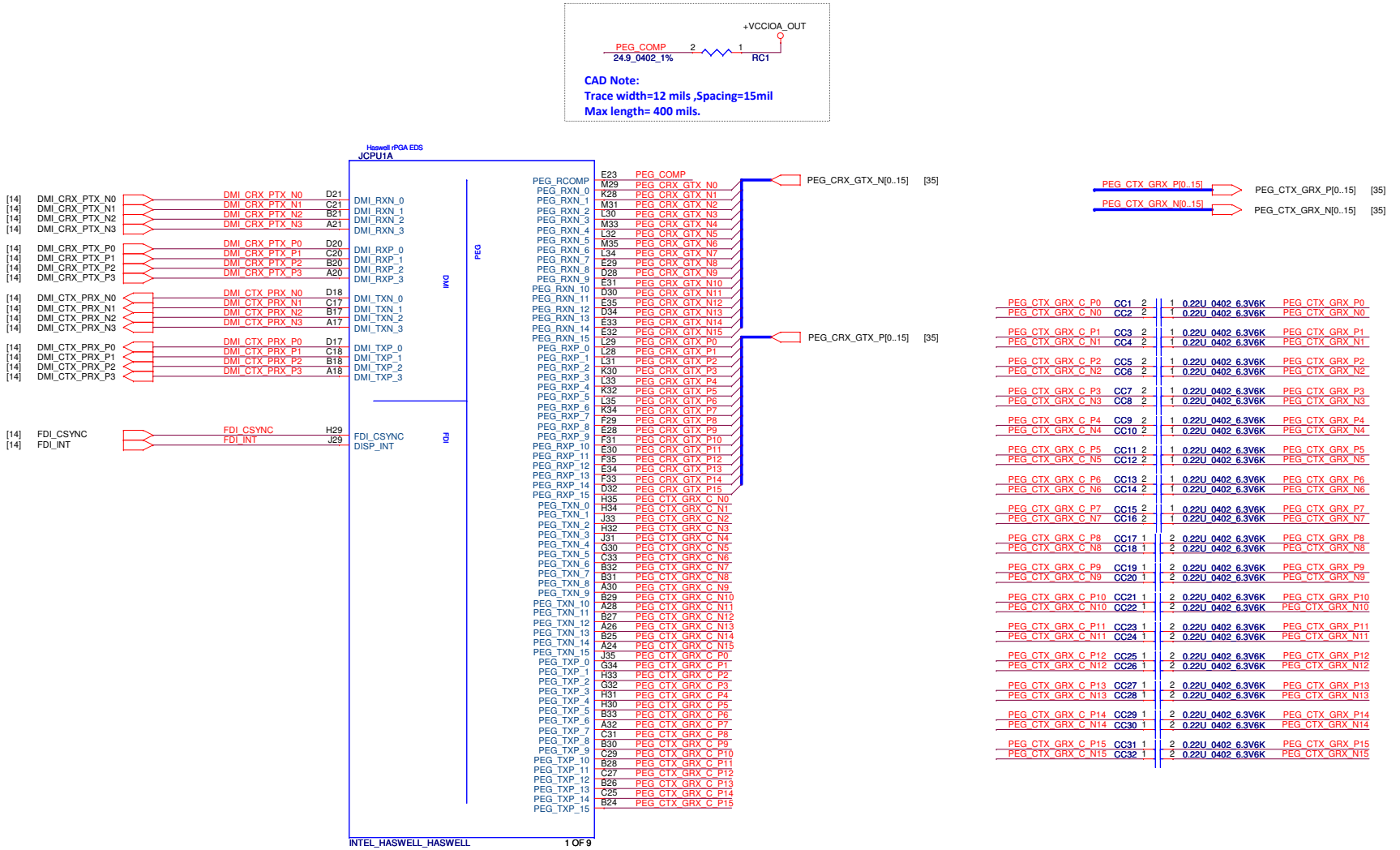
Title: SMBus block diagram_DSC

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 3 of 56



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Title: DMI,PEG

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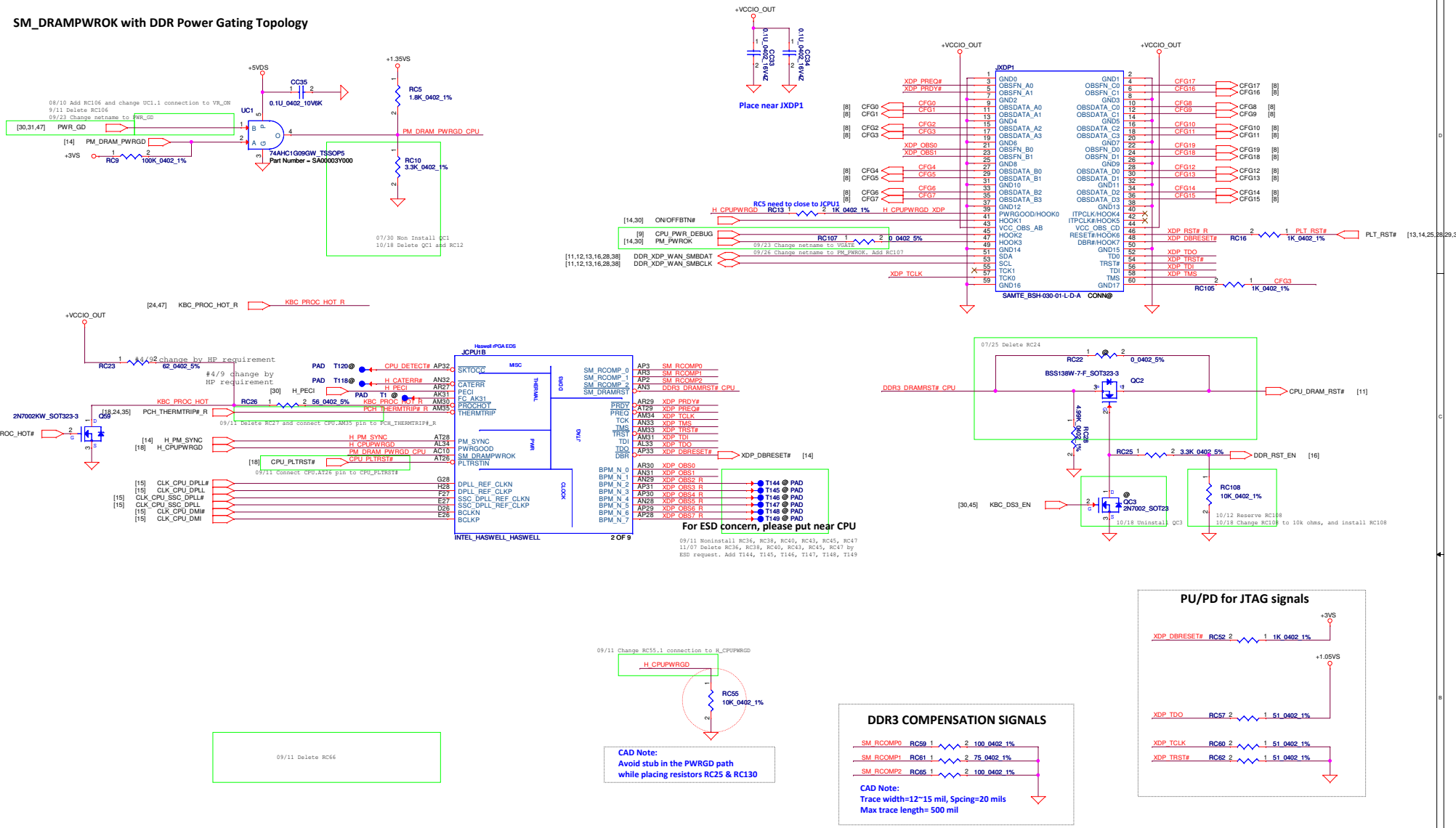
Date: Thursday, December 20, 2012 | Sheet 4 of 56

SM_DRAMPWROK with DDR Power Gating Topology



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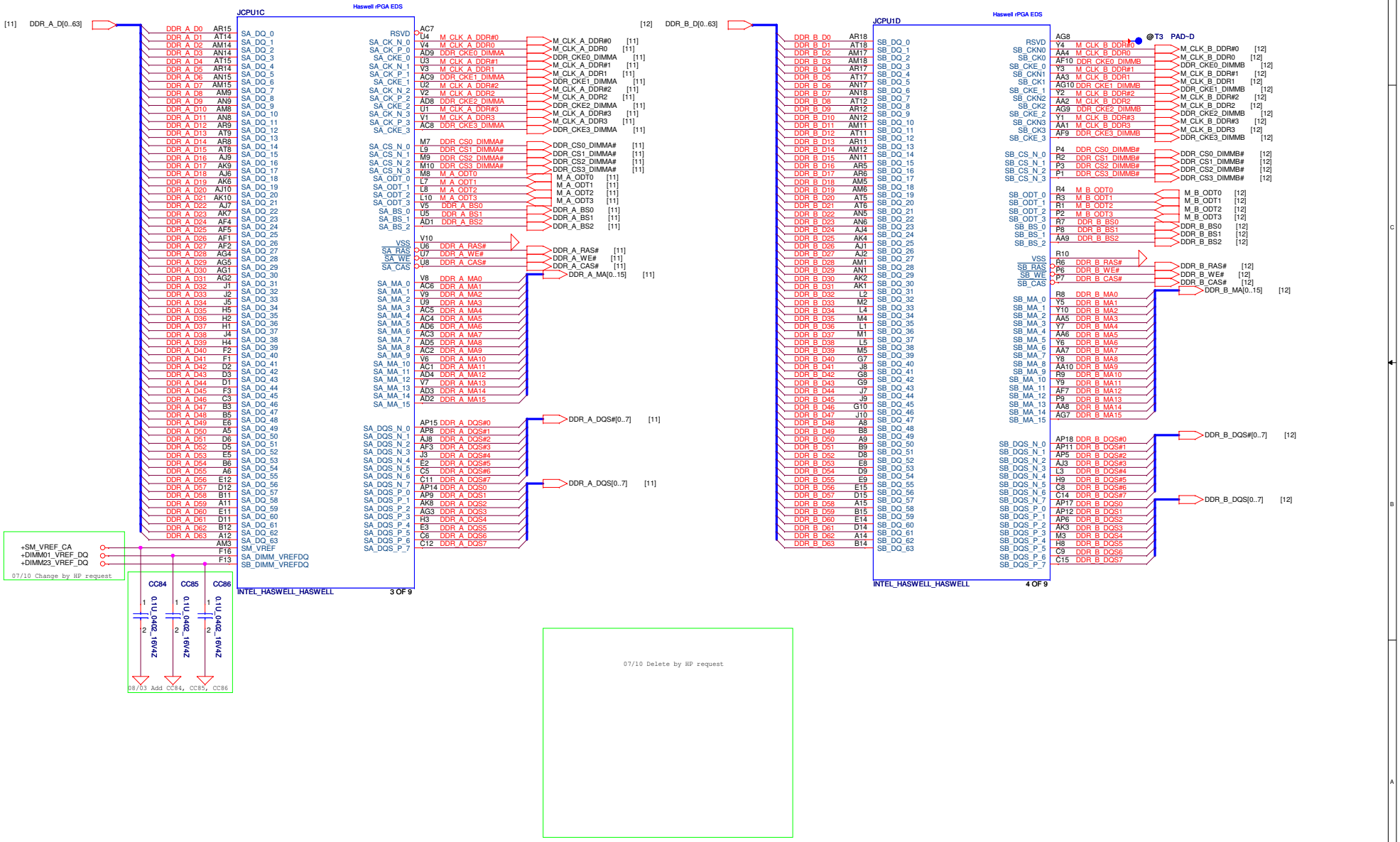
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: PM,XDP,CLK			
Size: Custom	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 5 of 56		



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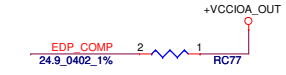
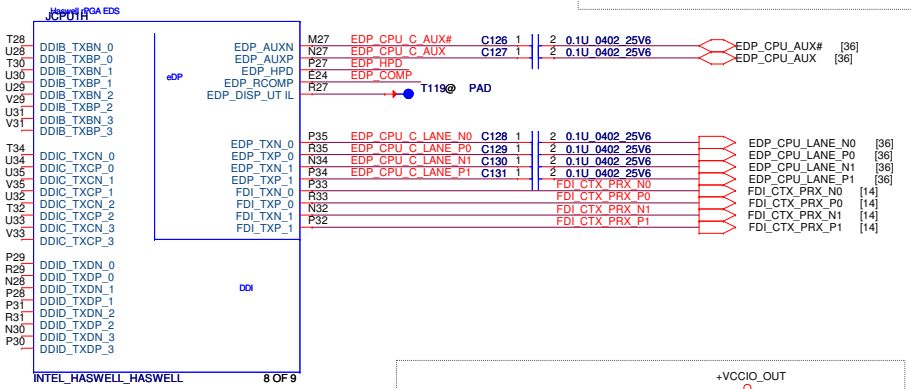
Title	DDRIII		
Size: Custom	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 6 of 56		

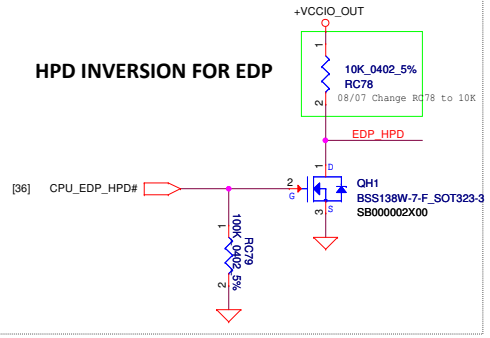
COMPENSATION PU FOR eDP



CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



HPD INVERSION FOR EDP



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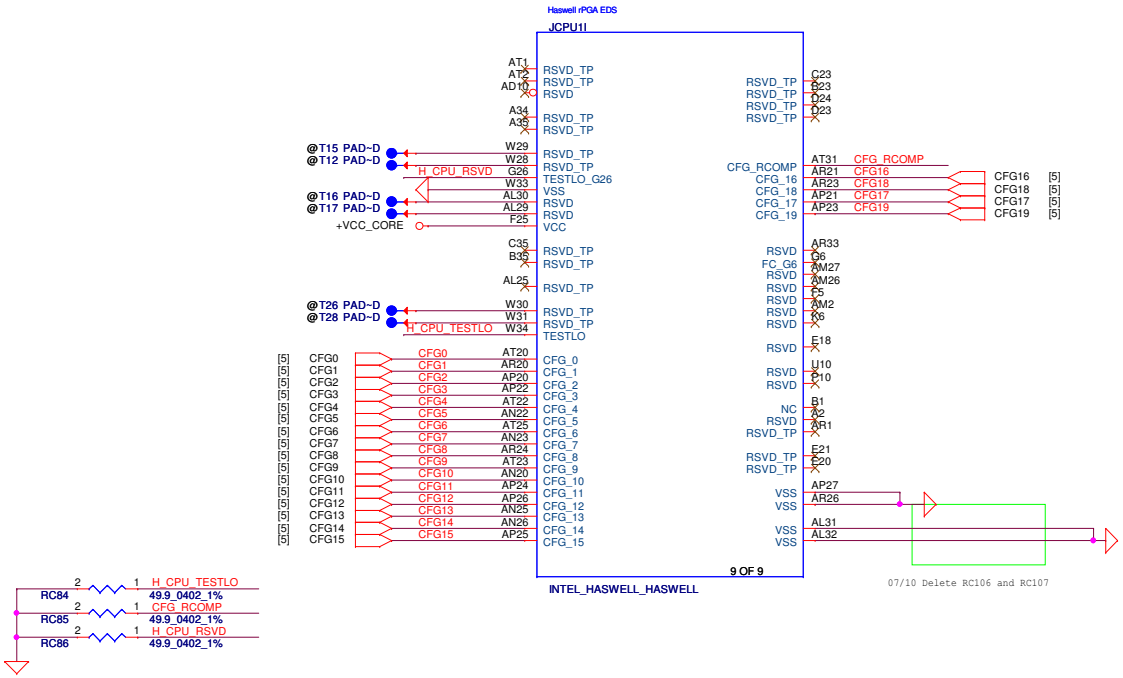
Compal Electronics, Inc.

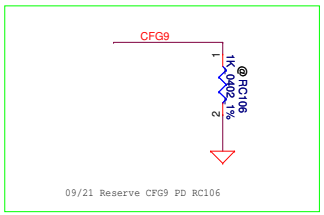
Title: CPU-FDI,eDP,DDI

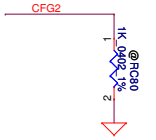
Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 Sheet 7 of 56

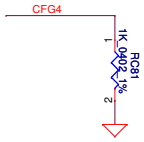
CFG STRAPS for CPU



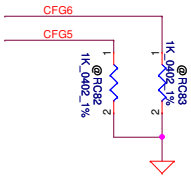




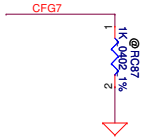
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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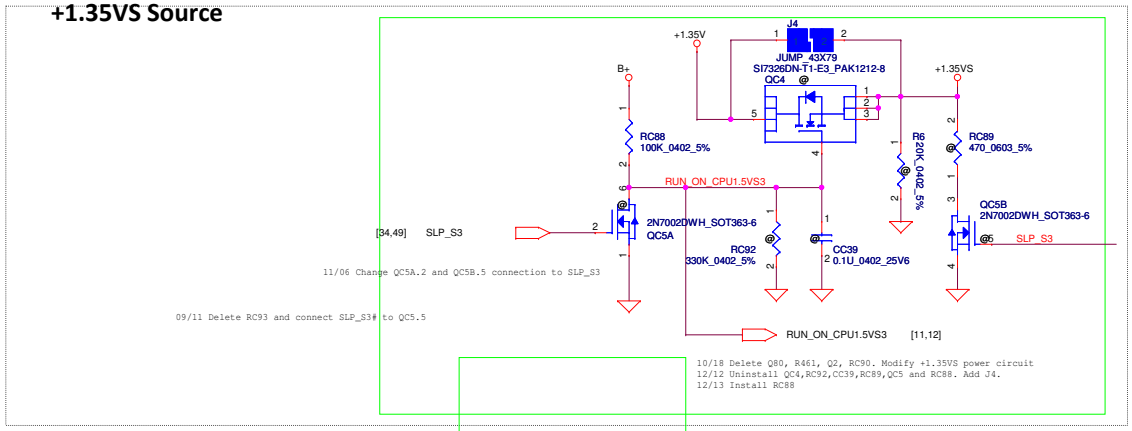
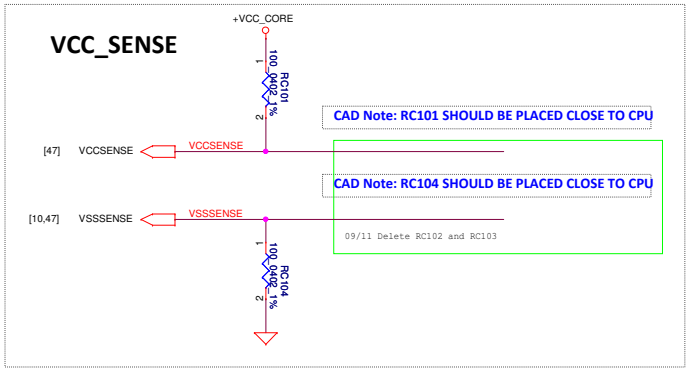
			Date: Thursday, December 20, 2012 / Sheet 8 of 56

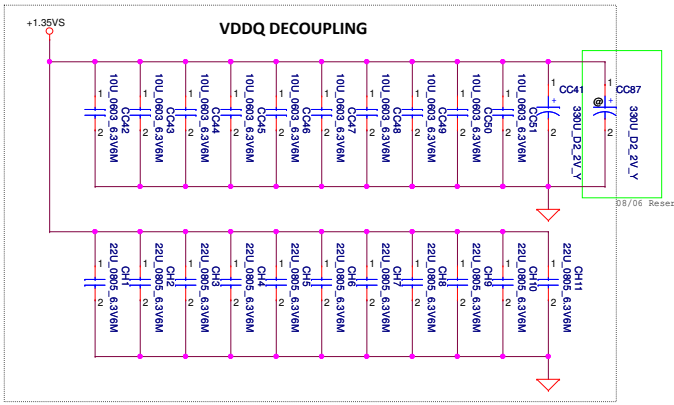
+1.35VS Source

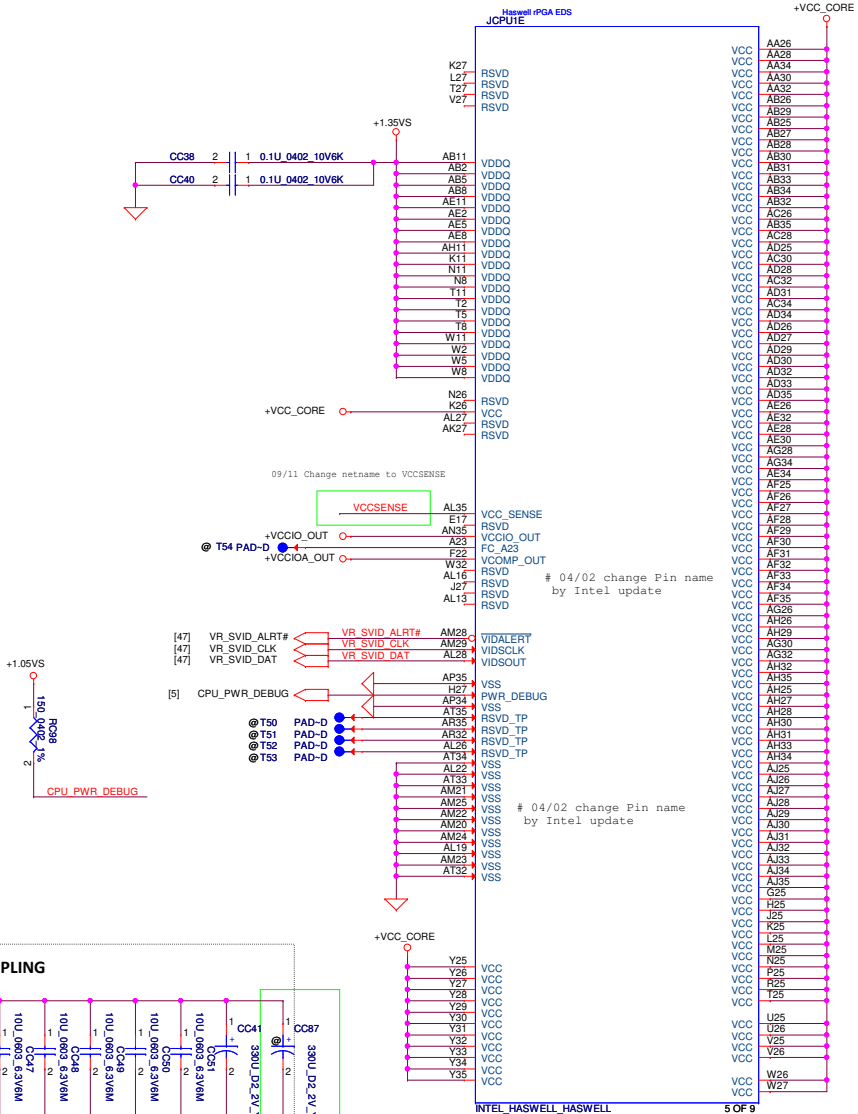


VCC_SENSE



VDDQ DECOUPLING





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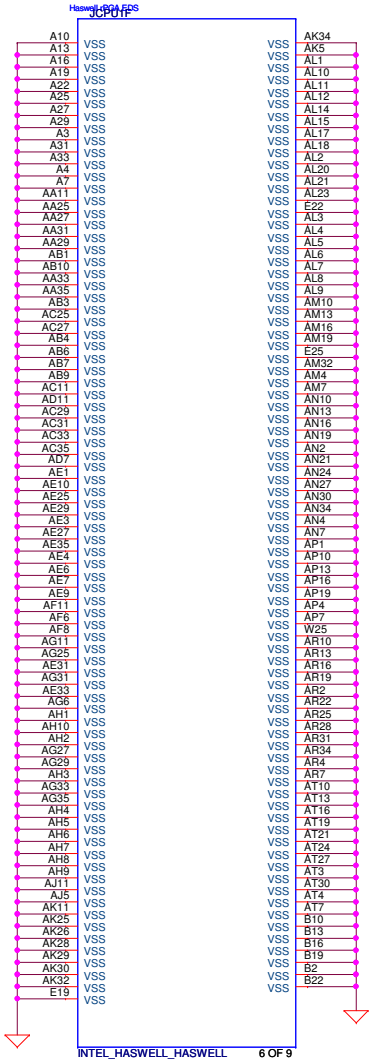
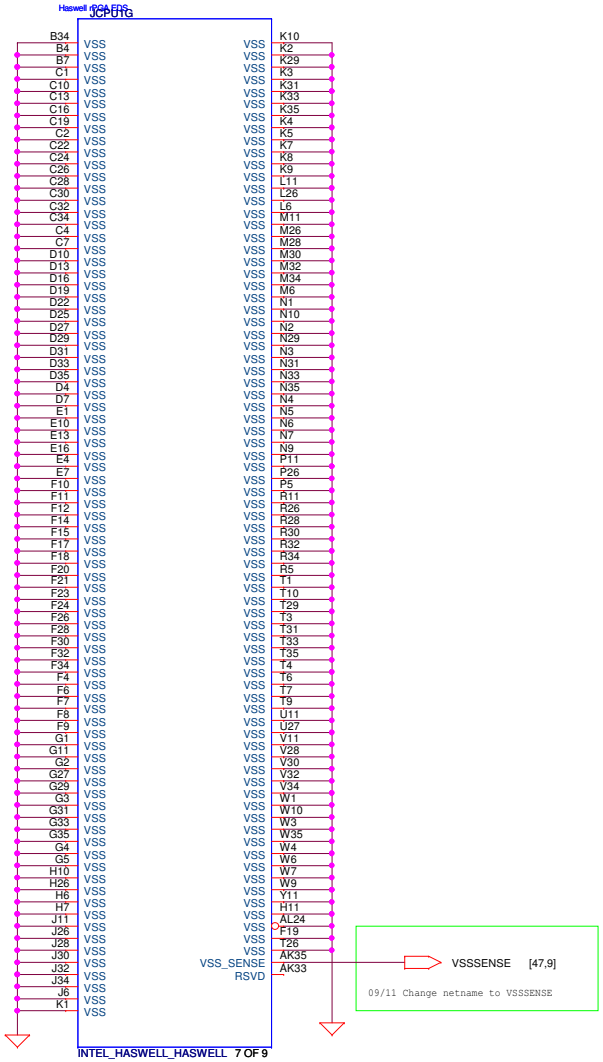
Compal Electronics, Inc.

Title: CPU- PWR

Size: Custom | Document Number: LA-9241P | Rev: 0.5

Date: Thursday, December 20, 2012 | Sheet 9 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: CPU-VSS

Size	Document Number	Rev
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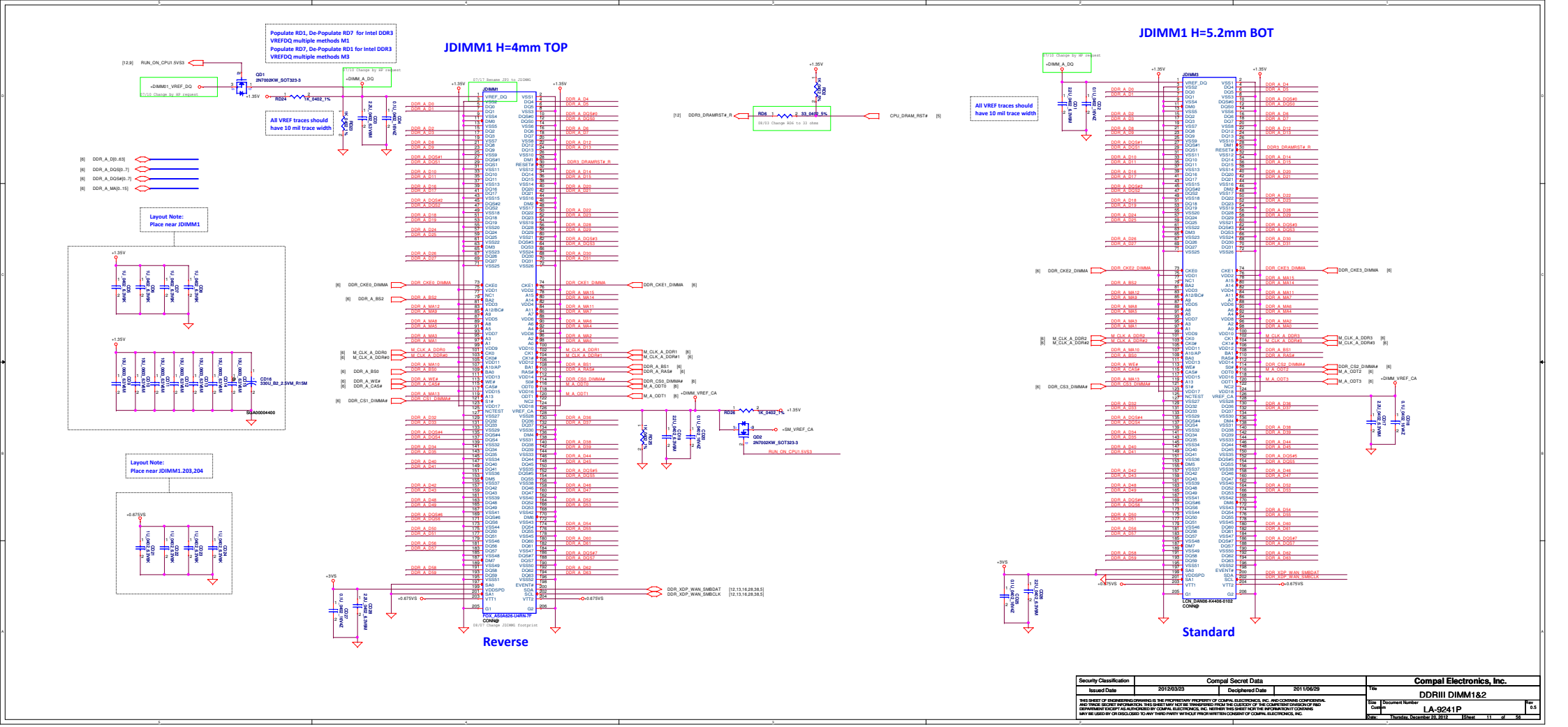
Date: Thursday, December 20, 2012 Sheet 10 of 56



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Compal Electronics, Inc.			
Title: DDRIII DIMM1&2			
Size:	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 11 of 56		

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

JDIMM2 H=9.2mm TOP

07/10 Change by HP request

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

11/06 Add C511 by rf request

Layout Note: Place near JDIMM2.203,204

Reverse

07/10 Change by HP request

All VREF traces should have 10 mil trace width

JDIMM4 H=5.2mm BOT

4/16 change by HP requirement

Reverse

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Compal Electronics, Inc.

Title: DDRIII DIMM3&4

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 12 of 56

+RTCVCC
RH16 30K_0402_5%
PCH_INTVRMEN

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

07/09 Delete by HP request.

07/09 Delete by HP request.

[11,12,16,28,38,5] DDR_XDP_WAN_SMBDAT
[11,12,16,28,38,5] DDR_XDP_WAN_SMBCLK
RH37 10K_0402_5%
RH38 10K_0402_5%
+3VS

+3VS
RH29 HDA_SPKR 10K_0402_5%

NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

07/09 Change by HP request.
10/26 Swap QH11A.2 and QH11B.5 connection
[30,39] BAT_GRNLED#
+3V_PCH
RH30 2.2K_0402_5%
QH11A MESS84DW-G_SC88-6
QH11B MESS84DW-G_SC88-6
PLT_RST#
HDA_SDOUT
09/03 Instal RH31
09/19 Change QH11 to P MOS, change RH30 to 2.2K ohms

PCH_RTCX1
PCH_RTCX2
RH28 10M_0402_5%
YH1 32.768KHZ_12.5PF_Q13FC1350000500
CH13 18P_0402_50V8J
CH14 18P_0402_50V8J
11/01 Change YH1 to small package

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

RH33 HDD_HALTLED 100K_0402_5%
08/03 RH33.1 connection to GND

+RTCVCC
RH34 20K_0402_5%
RH35 1M_0402_5%
RH36 20K_0402_5%
[25] WWAN_DET#
RH230 0_0402_5%

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

@ME1 SHORT PADS
CH15 1U_0402_6.3V6K
@CMOS1 SHORT PADS
CH16 1U_0402_6.3V6K
CMOS place near DIMM

UH1A LPT_PCH_M_EDS REV = 5

PCH_RTCX1	B5	RTCX1	RTC
PCH_RTCX2	B4	RTCX2	
SRTCRST#	B9	SRTCRST#	
INTRUDER#	A8	INTRUDER#	
PCH_INTVRMEN	G10	INTVRMEN	
PCH_RTCRST#	D9	RTCRST#	
HDA_BIT_CLK	B25	HDA_BCLK	AZALIA
HDA_SYNC	A22	HDA_SYNC	
HDA_SPKR	AL10	SPKR	
HDA_RST#	C24	HDA_RST#	
HDA_SDI0	L22	HDA_SDI0	
	K22	HDA_SDI1	
	G22	HDA_SDI2	
	F22	HDA_SDI3	
HDA_SDOUT	A24	HDA_SDO	
HDD_HALTLED	B17	DOCKEN#/GPIO33	
ISO_PREP#	C22	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK	AB3	JTAG_TCK	JTAG
PCH_JTAG_TMS	AD1	JTAG_TMS	
PCH_JTAG_TDI	AE2	JTAG_TDI	
PCH_JTAG_TDO	AD3	JTAG_TDO	
PCH_TP25	F8	TP25	
	C26	TP22	
	AB6	TP20	

[14] PCH_RTCRST#
[26] HDA_SPKR
[26] HDA_SDI0
07/06 Follow HP's GPIO table
[39] HDD_HALTLED
[33,36] ISO_PREP#

SATA_RXN_0 / SATA_RXP_0	BC8 / BE8	SATA_PRX_DTX_N0 / SATA_PRX_DTX_P0	SATA_PRX_DTX_N0 / SATA_PRX_DTX_P0 [23]
SATA_TXN_0 / SATA_TXP_0	AW8 / AY8	SATA_PTX_DRX_N0 / SATA_PTX_DRX_P0	SATA_PTX_DRX_N0 / SATA_PTX_DRX_P0 [23]
SATA_RXN_1 / SATA_RXP_1	BC10 / BE10	SATA_PRX_DTX_N1 / SATA_PRX_DTX_P1	SATA_PRX_DTX_N1 / SATA_PRX_DTX_P1 [23]
SATA_TXN_1 / SATA_TXP_1	AV10 / AW10	SATA_PTX_DRX_N1 / SATA_PTX_DRX_P1	SATA_PTX_DRX_N1 / SATA_PTX_DRX_P1 [23]
SATA_RXN_2 / SATA_RXP_2	BB9 / BD9	SATA_PRX_DTX_N2 / SATA_PRX_DTX_P2	SATA_PRX_DTX_N2 / SATA_PRX_DTX_P2 [33]
SATA_TXN_2 / SATA_TXP_2	AY13 / AW13	SATA_PTX_DRX_N2 / SATA_PTX_DRX_P2	SATA_PTX_DRX_N2 / SATA_PTX_DRX_P2 [33]
SATA_RXN_3 / SATA_RXP_3	BC12 / BE12	SATA_PRX_DTX_N3 / SATA_PRX_DTX_P3	SATA_PRX_DTX_N3 / SATA_PRX_DTX_P3 [33]
SATA_TXN_3 / SATA_TXP_3	AR13 / AT13	SATA_PTX_DRX_N3 / SATA_PTX_DRX_P3	SATA_PTX_DRX_N3 / SATA_PTX_DRX_P3 [33]
SATA_RXN4/PERN1 / SATA_RXP4/PERP1	BD13 / BB13		
SATA_TXN4/PETN1 / SATA_TXP4/PETP1	AV15 / AW15		
SATA_RXN5/PERN2 / SATA_RXP5/PERP2	BC14 / BE14	SATA_PRX_DTX_N5 / SATA_PRX_DTX_P5	SATA_PRX_DTX_N5 / SATA_PRX_DTX_P5 [23]
SATA_TXN5/PETN2 / SATA_TXP5/PETP2	AP15 / AR15	SATA_PTX_DRX_N5 / SATA_PTX_DRX_P5	SATA_PTX_DRX_N5 / SATA_PTX_DRX_P5 [23]
SATA_RCOMP	AY5	SATA_COMP	R463 10K_0402_5% +3VS
SATALED#	AP3	SATA_ACT#	SATA_ACT# [33,39]
SATA0GP/GPIO21	AT1	SG_IN	SG_IN [22]
SATA1GP/GPIO19	AU2	FN9	PAD~D T72 @
SATA_IREF	BD4	SATA_IREF	RH42 0_0402_5% +1.5VS
TP9	BA2		
TP8	BB2		

HDD
ODD
DOCK_SATA5
DOCK_SATA3
mSATA

LYNXPOINT_BGA695 1 OF 11

+3VS
10K_0402_5% R7
10K_0402_5% R8
UMA@
RH237 10K_0402_5% +3VS
[14,25,28,29,30,35,37,39,5] PLT_RST#
Q70 2N7002KW_SOT323-3

SATA Impedance Compensation
SATA_COMP 7.5K_0402_1%
+1.5VS
RH49
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

HDA_SYNC Isolation Circuit
+5VS
HDA_SYNC_R
QH2 SB000002X00 BSS138W-7-F_SOT323-3
HDA_SYNC
RH43 1M_0402_5%

+3V_PCH
RH39 51_0402_1%
RH40 200_0402_5%
RH41 200_0402_5%
RH44 200_0402_5%
09/21 Non-install RH39, RH40, RH41, RH44, RH48, RH47, RH46
RH45 0_0402_5%
RH46 100K_0402_5%
RH47 100K_0402_5%
RH48 100K_0402_5%

[26] HDA_SYNC_AUDIO
RH51 33_0402_5%
HDA_SYNC_R
[26] HDA_SDOUT_AUDIO
[26] HDA_RST_AUDIO#
[26] HDA_BITCLK_AUDIO
RP6 33_8P4R_5%
HDA_SDOUT
HDA_RST#
HDA_BIT_CLK
CH17 27P_0402_50V8J
10/25 Delete RH50, RH52, RH53. Add RP6

+RTCVCC
W=20mils
CH102 1U_0603_10V4Z
Place near PCH
+3VDS
D40 DAN202U_SC70
+BATT_D
+BATT1.1
RH233 1K_0402_5%
W=20mils
JBATT1 ACES_50271-00201-001
CONN@
08/07 Change JBATT1 footprint

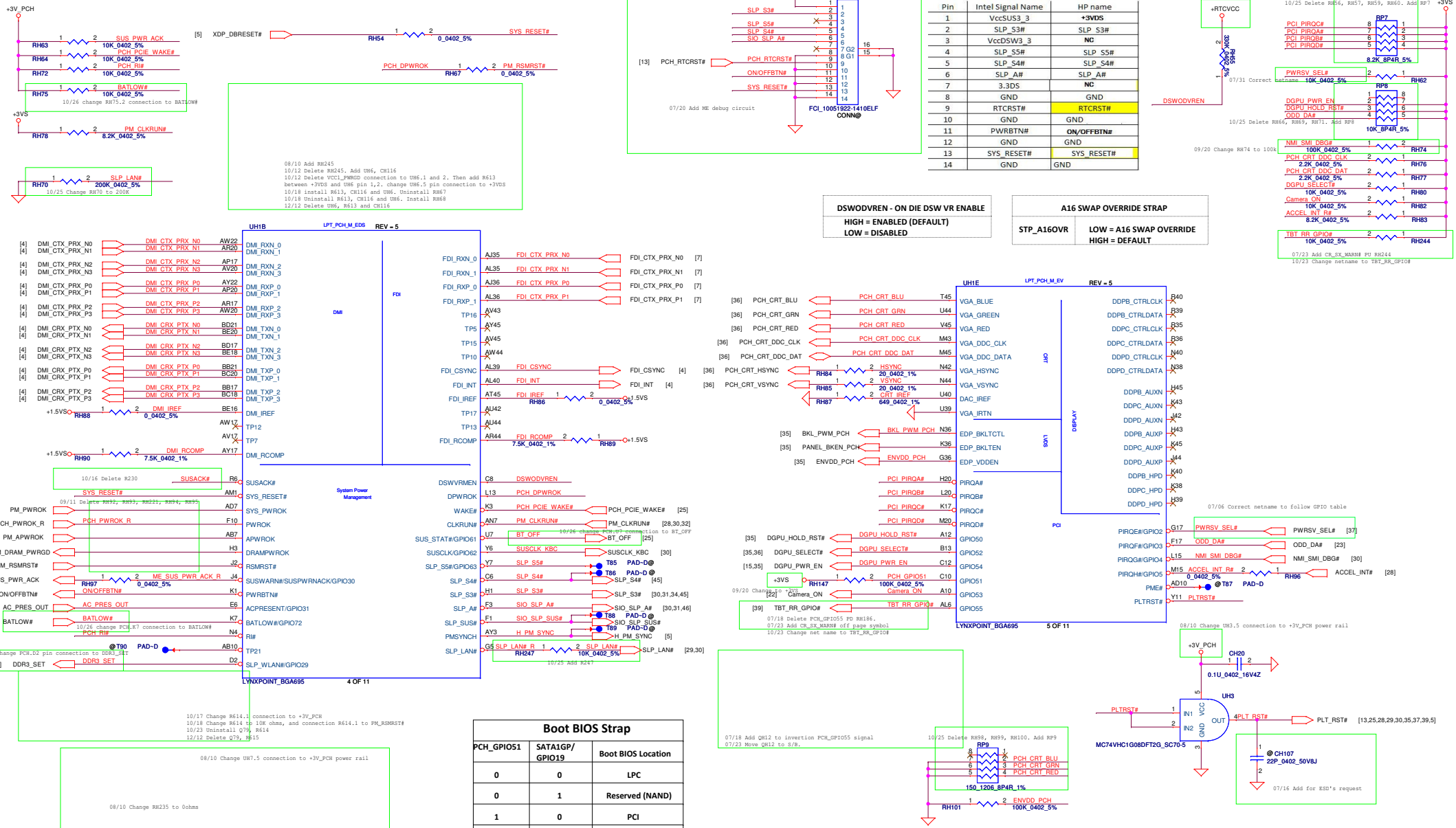
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH-RTC,HDA,SATA,XDP

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 Sheet 13 of 56



Pin	Intel Signal Name	HP name
1	VccSUS3_3	+3VDS
2	SLP_S3#	SLP_S3#
3	VccDSW3_3	NC
4	SLP_S5#	SLP_S5#
5	SLP_S4#	SLP_S4#
6	SLP_A#	SLP_A#
7	3.3DS	NC
8	GND	GND
9	RTCRST#	RTCRST#
10	GND	GND
11	PWRBTN#	ON/OFFBTN#
12	GND	GND
13	SYS_RESET#	SYS_RESET#
14	GND	GND

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

A16 SWAP OVERRIDE STRAP	
STP_A16OVR	LOW = A16 SWAP OVERRIDE HIGH = DEFAULT

Boot BIOS Strap		
PCH_GPIO51	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

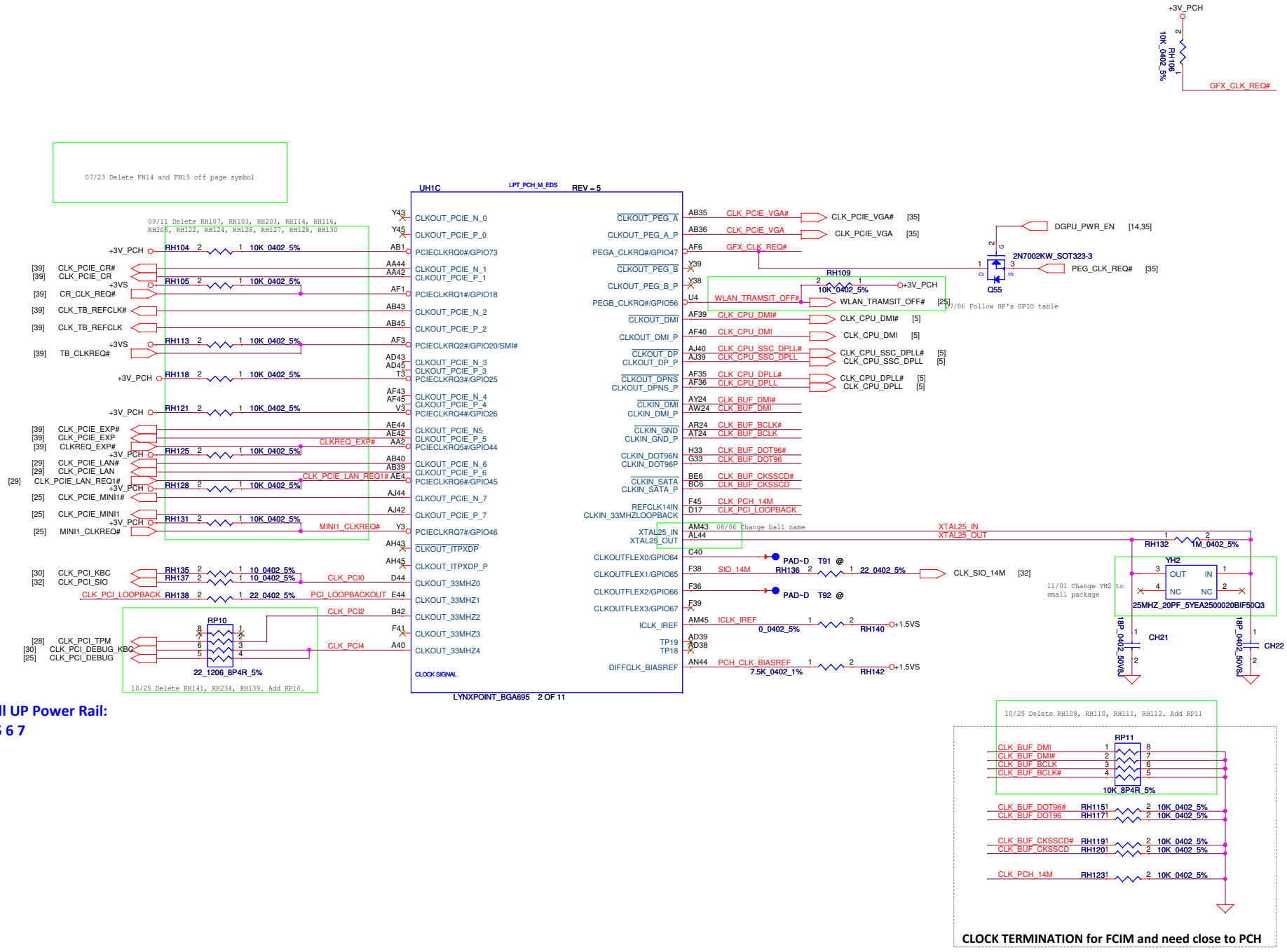
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH -DMI,FDI,PM,DP,CRT

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 14 of 56



PCIECLK REQ Pull UP Power Rail:
SUS Rail : 0 3 4 5 6 7
Core Rail: 1 2

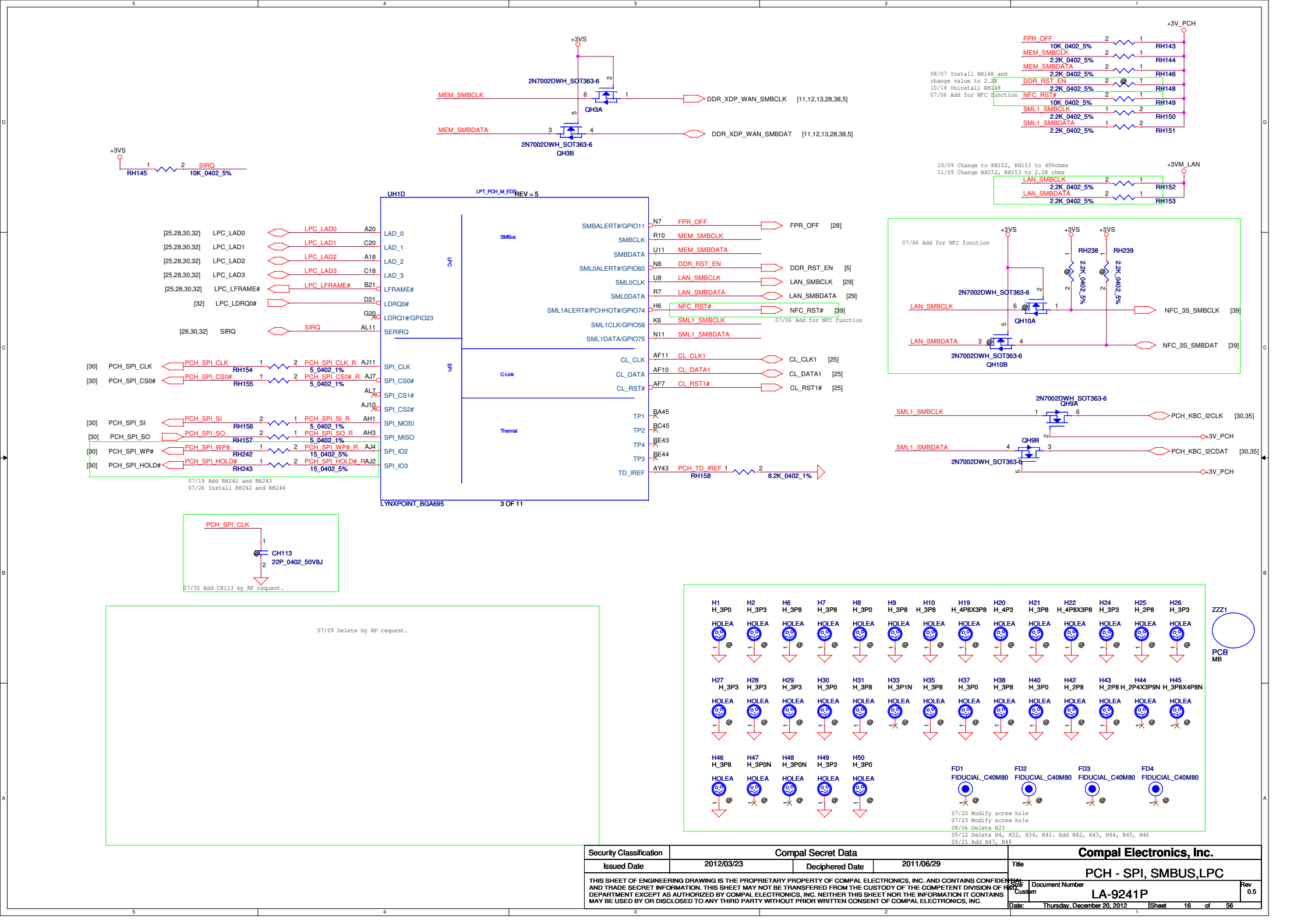
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH- CLK

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 Sheet 15 of 56



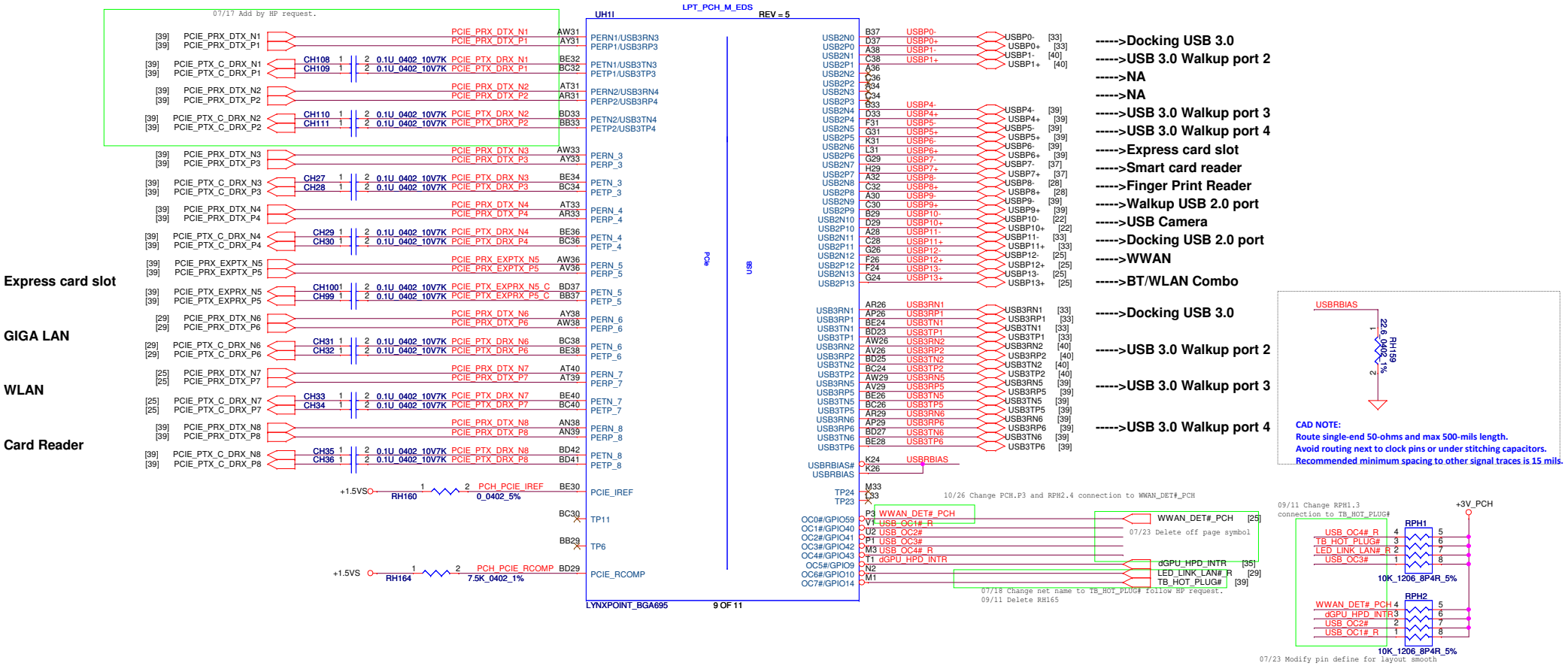
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH - SPI, SMBUS,LPC

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 16 of 56



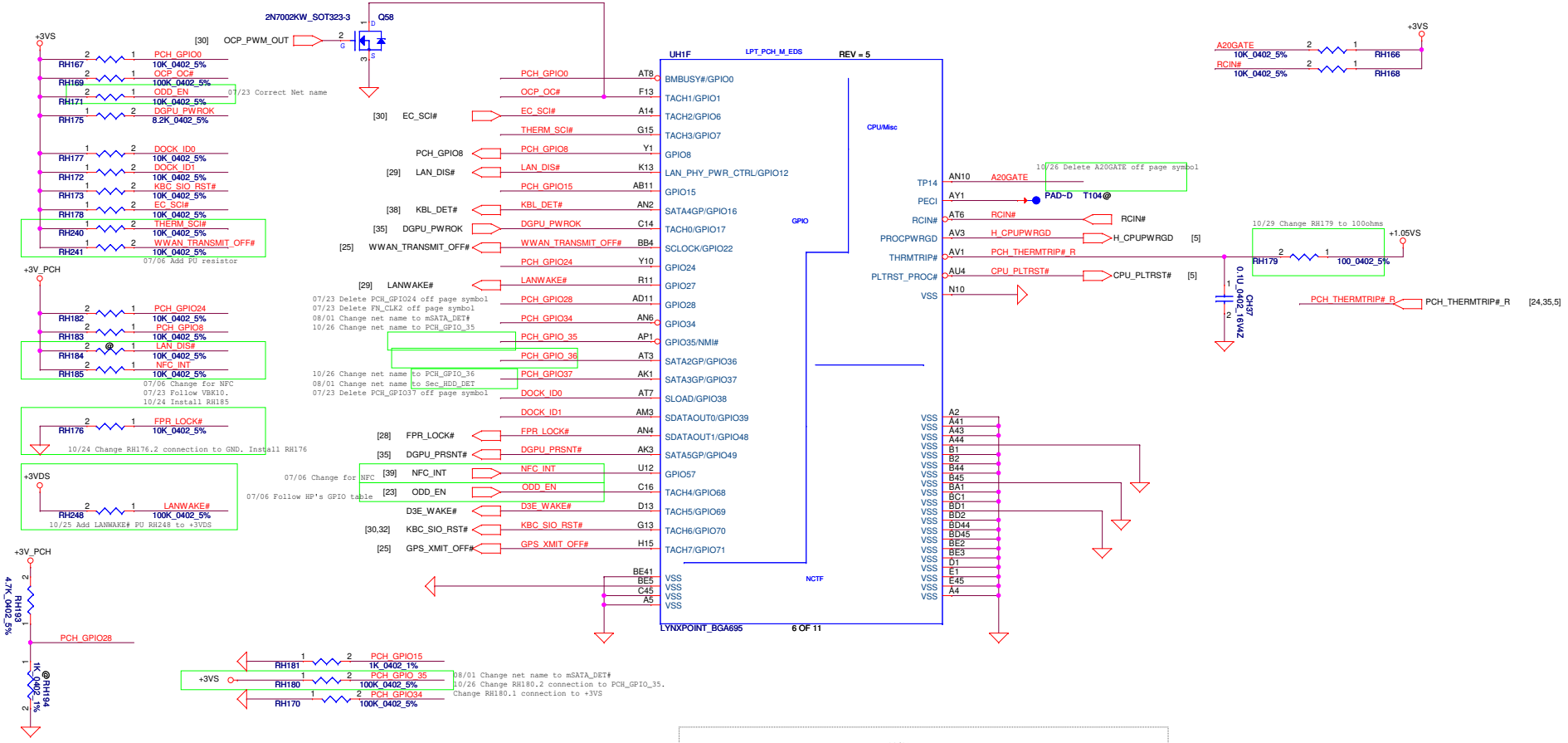
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH-PCIE,USB

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 Sheet 17 of 56



Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

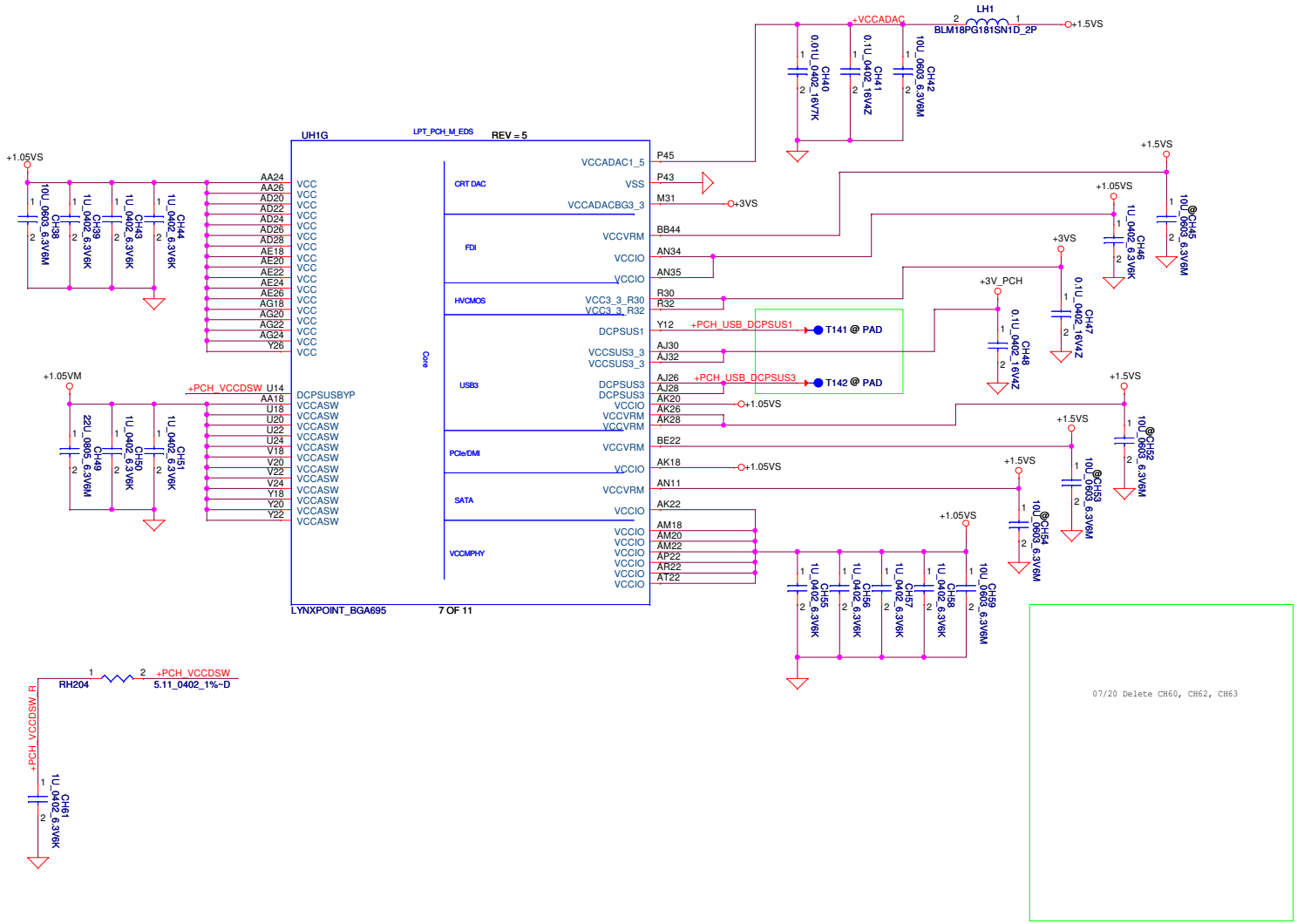
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH -GPIO,MISC,NTFC

Size: Custom | Document Number: LA-9241P | Rev: 0.5

Date: Thursday, December 20, 2012 | Sheet 18 of 56



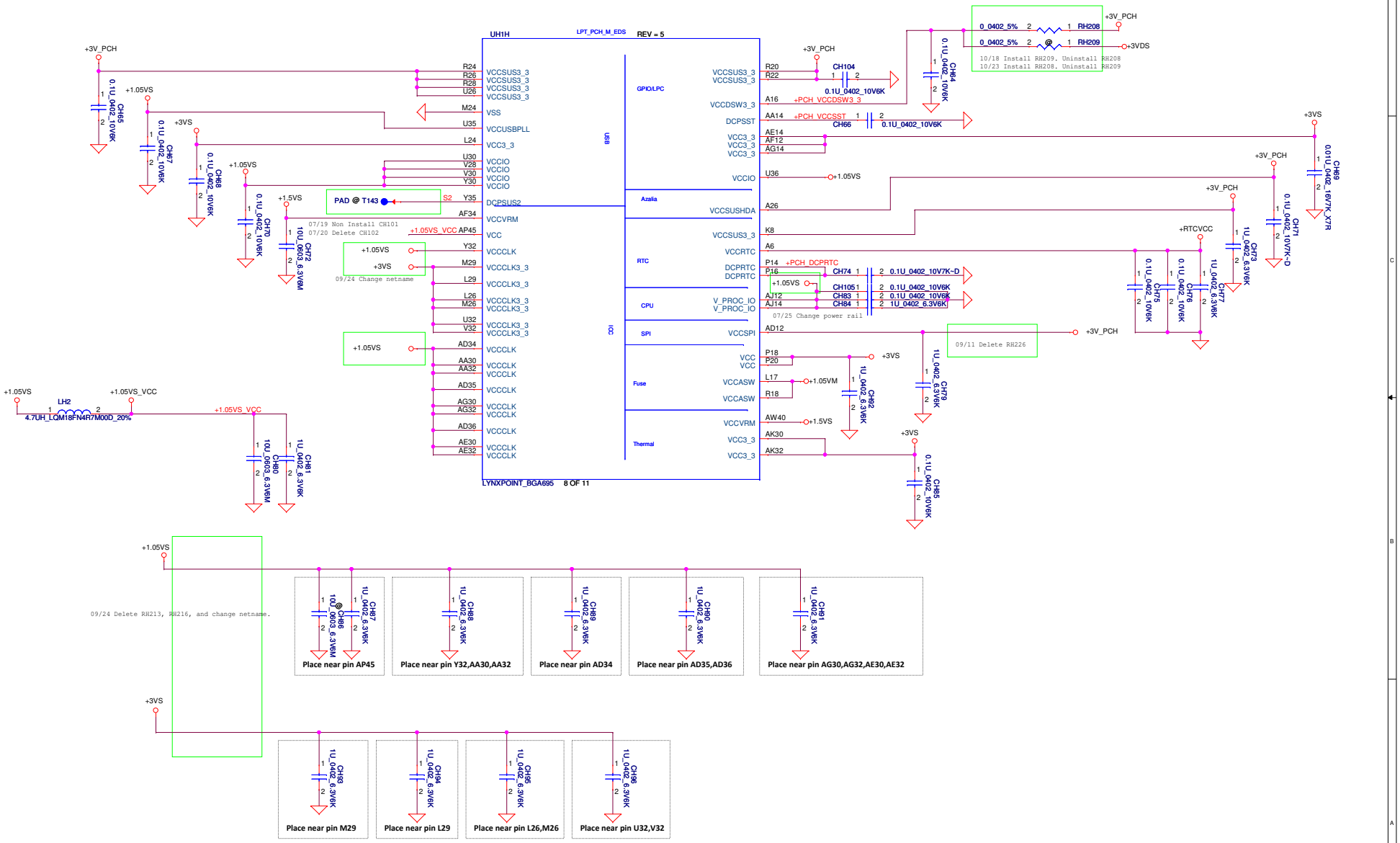
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH- Power

Size: Custom | Document Number: LA-9241P | Rev: 0.5

Date: Thursday, December 20, 2012 | Sheet 19 of 56



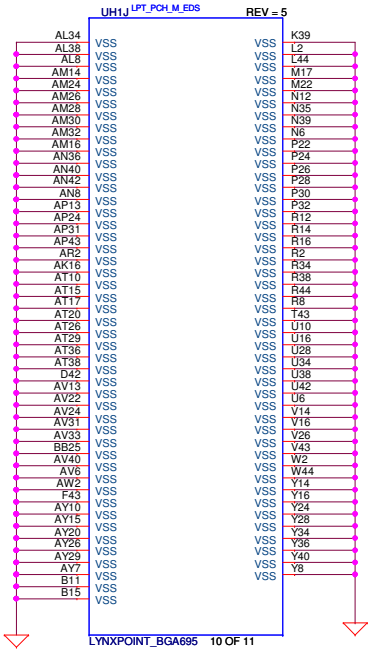
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

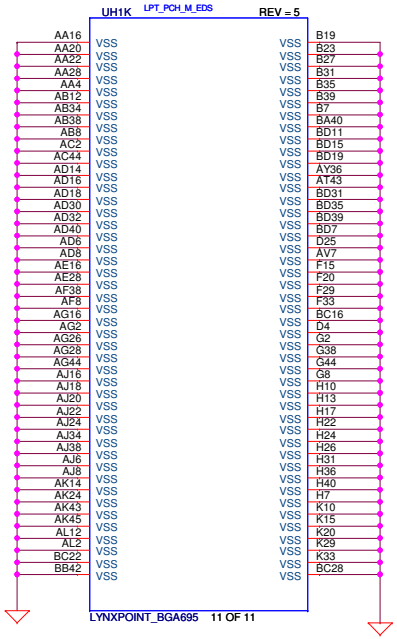
Compal Electronics, Inc.

Title: PCH - Power

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 Sheet 20 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

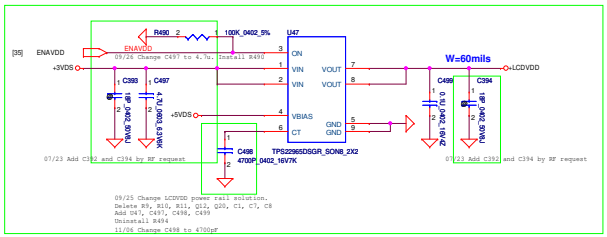
Compal Electronics, Inc.

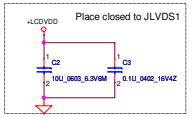
Title: PCH - GND

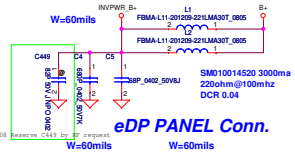
Size	Document Number	Rev
Custom	LA-9241P	0.5

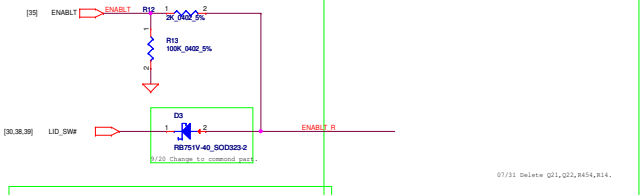
Date: Thursday, December 20, 2012 Sheet 21 of 56

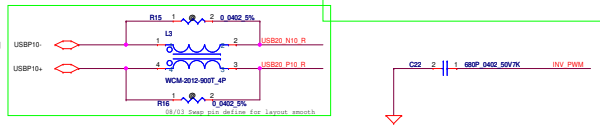
LCD POWER CIRCUIT

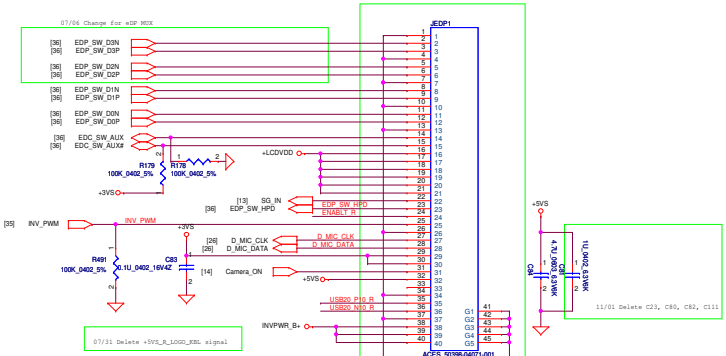


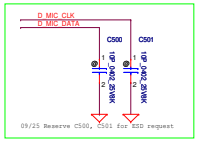












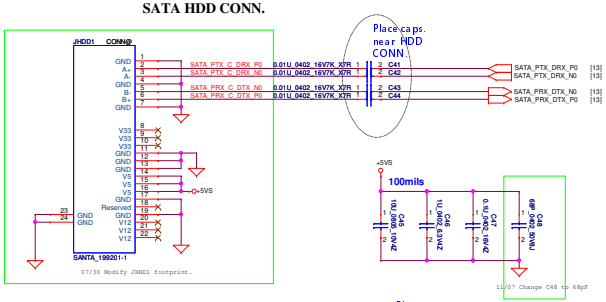
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: eDP/LVDS CONN & Camera

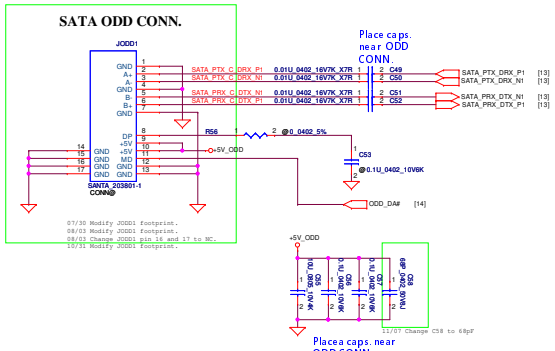
Size	Document Number	Rev
	LA-9241P	0.5
Date: Thursday, December 20, 2012	Sheet 22 of 56	

SATA HDD CONN.

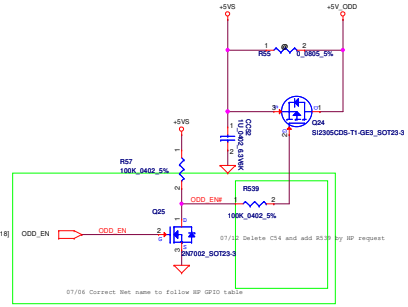


Placea caps. near HDD CONN.

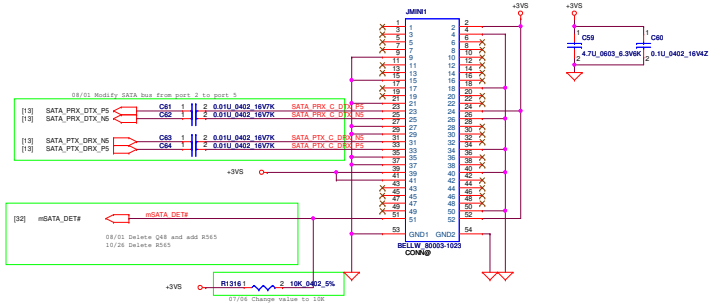
SATA ODD CONN.



Placea caps. near ODD CONN.



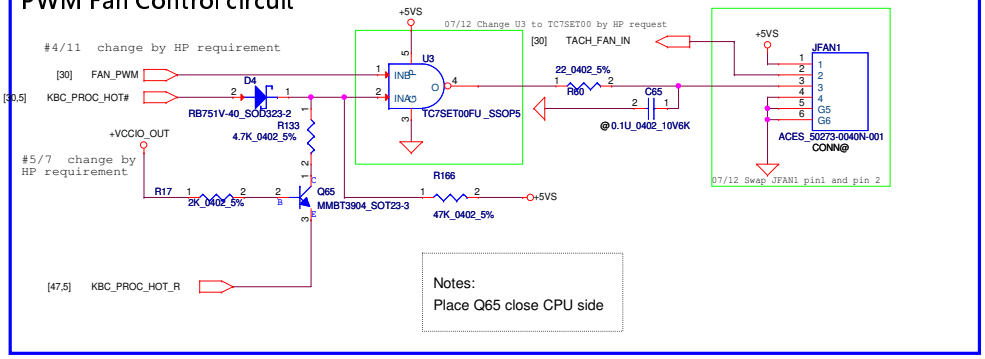
mSATA Conn.

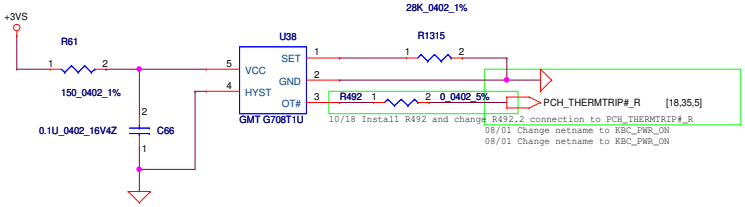


Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2010/03/31

Compal Electronics, Inc.	
Title	IBEX-M(1/6)-HDA/JTAG/SATA
Size	Document Number: LA-9241P
Rev	0.5
Date: Thursday, December 20, 2012	Sheet 23 of 56

PWM Fan Control circuit





Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/12/31

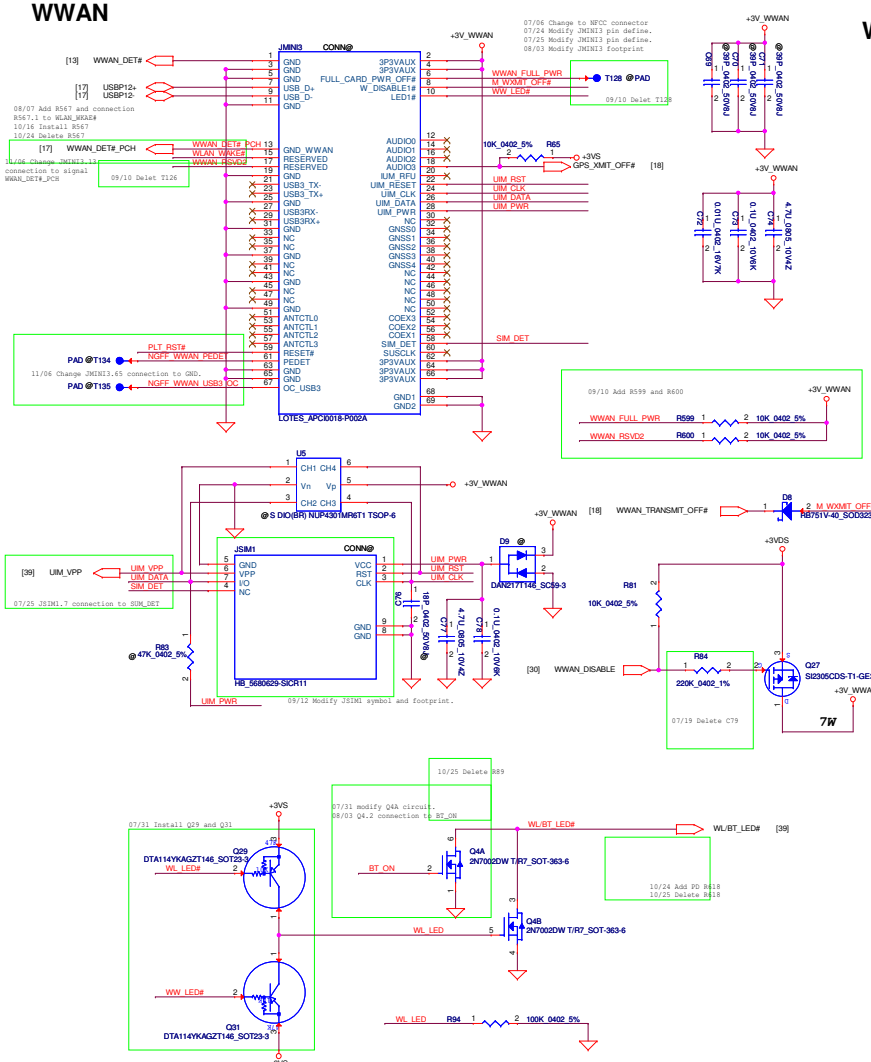
Compal Electronics, Inc.

Title: **Thermal/FAN**

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 24 of 56

WWAN

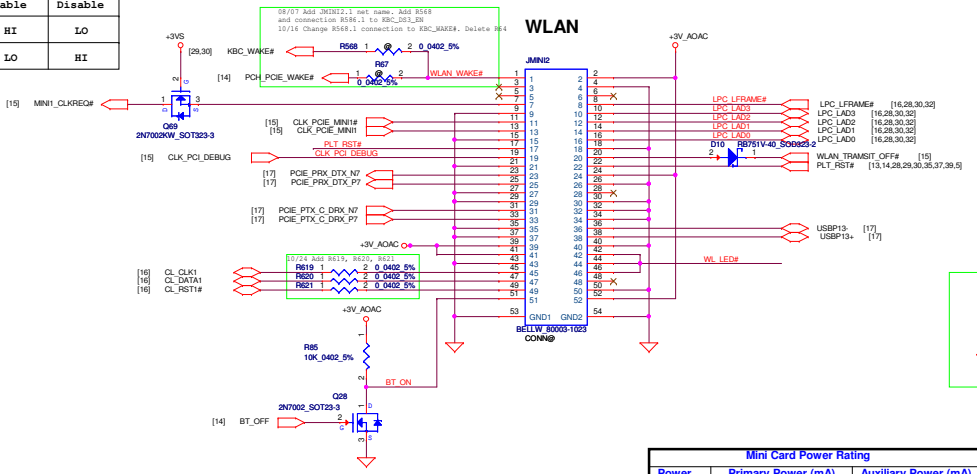


WLAN

WLAN&BT Combo module circuits

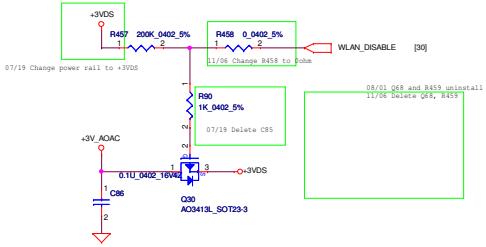
	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_ON#	LO	HI

#4/13 change by HP requirement



For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2010/03/31

Compal Electronics, Inc.			
Title: WWAN/NAND mini			
Size: C	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 25 of 56		

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place AVDD ,PVDD,and DVDD capacitor close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

RA3 2.49K_0402_1% +AVDD_CODEC
07/23 Delete RA7
SENSE_A CA1 1000P_0402_50V7K

SENSE_B RA4 2.49K_0402_1% +AVDD_CODEC
CA13 1000P_0402_50V7K @
PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

UA1 92HD91B2X5NLGXWCX8_QFN48_7X7

External MIC
Combo Jack
Headphone

07/06 Delete MIC_SENSE# circuit

Internal SPKR(front stereo speaker)

07/06 Delete MUTE LED circuit

09/20 Delete RA13, CA20

Place close to Codec

09/03 Change UA1 P/N

Place C209,C210,CA87,CA89 close to Codec

SB Beep

RA53 need under or near UA5

07/20 HP's request.

W=40Mil

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

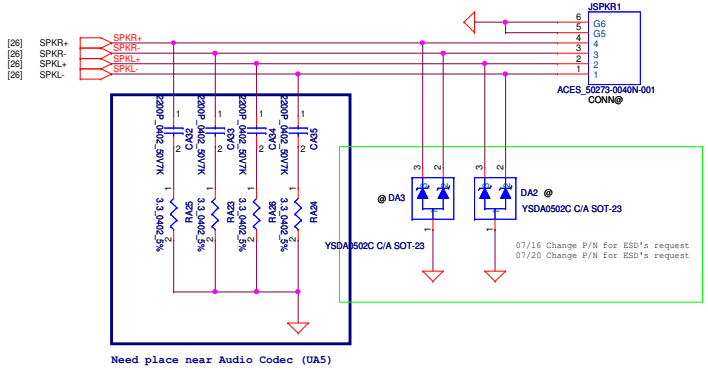
Compal Electronics, Inc.

Title: Audio IDT 92HD91

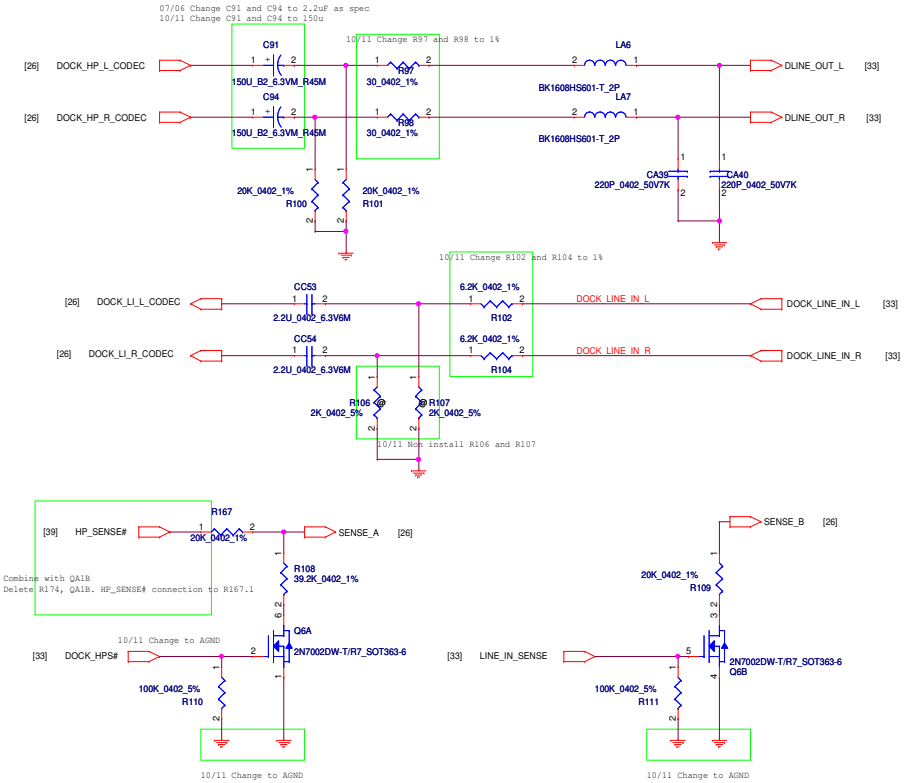
Size	Document Number	Rev
Custom	LA-XXXXP	0.5

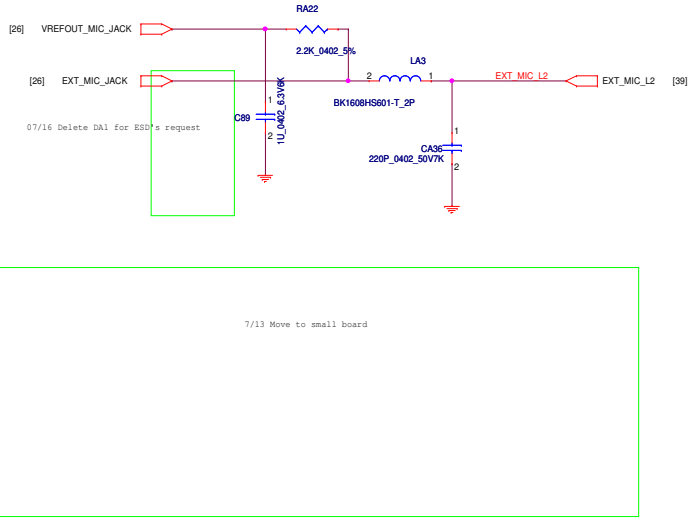
Date: Thursday, December 20, 2012 Sheet 26 of 56

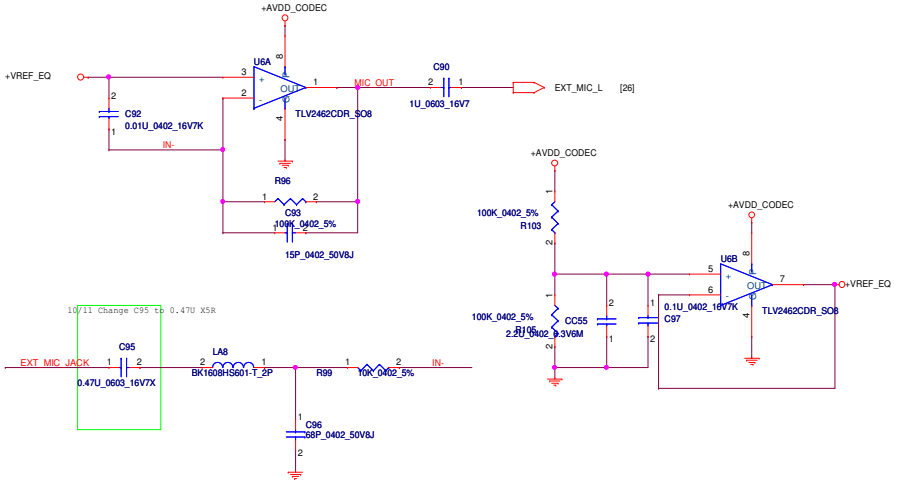
Speaker Connector



DOCK Audio

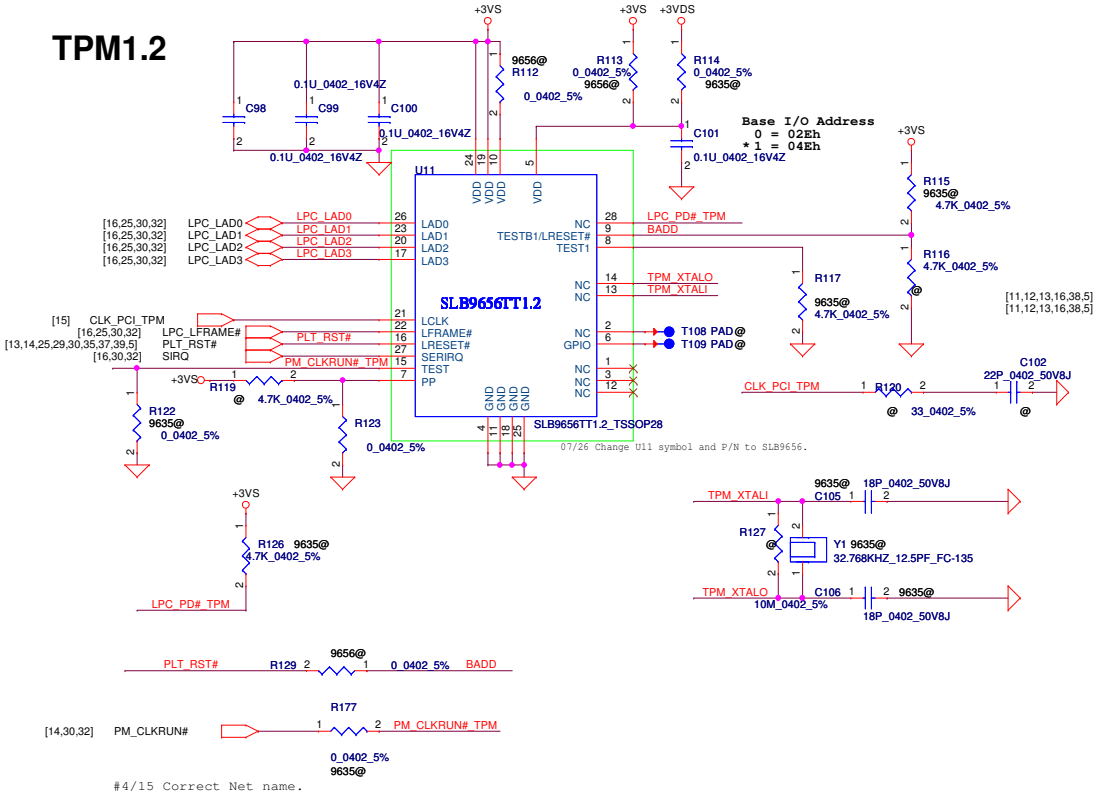




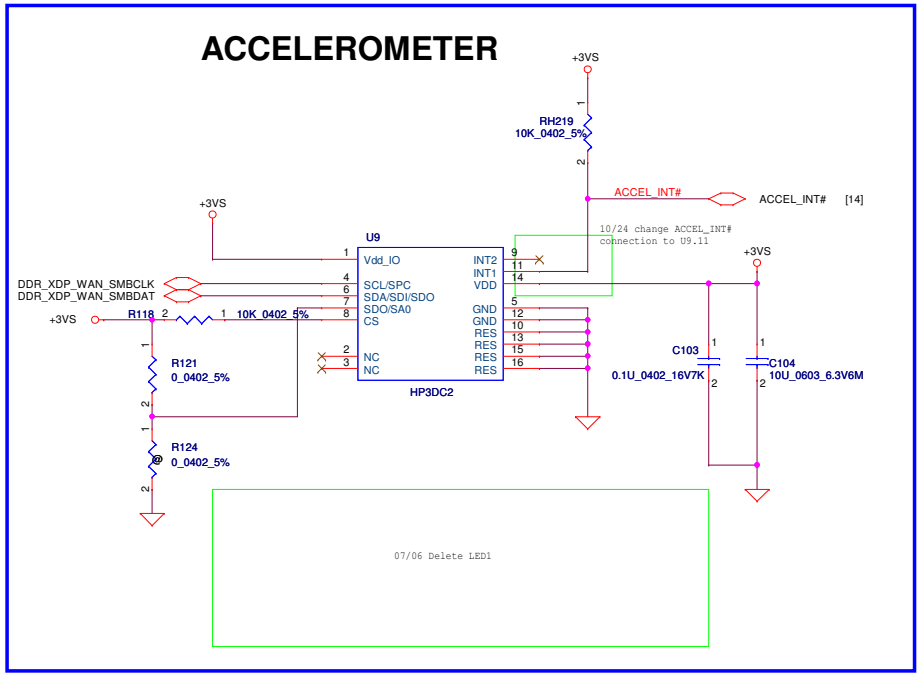


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2012/10/21
Title	Audio SPK Conn/Jack/MIC		
Size C	Document Number LA-9241P		Rev 0.5
Date: Thursday, December 20, 2012	Sheet 27 of 56		

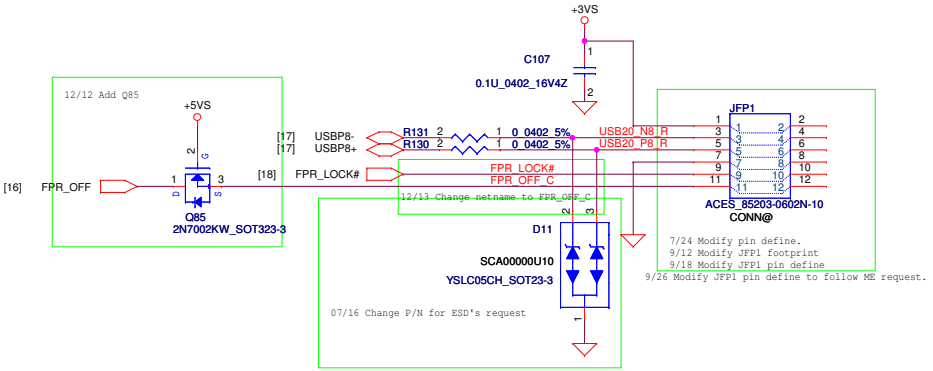
TPM1.2



ACCELEROMETER



Finger printer



Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2006/09/25

Compal Electronics, Inc.			
Title: TPM/Gsensor			
Size:	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 28 of 56		

W=60mils

+3VM_LAN

C108 1U_0402_6.3V6K

C109 0.1U_0402_16V4Z

C110 22U_0603_6.3V6K

07/20 Change C110 to 22UF

07/23 Change R128 to 4.7K ohms

+3VDS

10/26 Change R376 to 10k. Change R376.1 connection to +3VDS

R376 10K_0402_5%

[34] SLP_LAN — SLP_LAN

[14,30] SLP_LAN# — AMT@ Q7A 2N7002DWH_SOT363-6

07/20 Change location to Q7A

RJ-45 CONN.

U10

[15] CLK_PCIE_LAN_REQ1#
[13,14,25,28,30,35,37,39,5] PLT_RST#
[15] CLK_PCIE_LAN
[15] CLK_PCIE_LAN#
[17] PCIE_PRX_DTX_P6
[17] PCIE_PRX_DTX_N6
[17] PCIE_PTX_C_DRX_P6
[17] PCIE_PTX_C_DRX_N6
[16] LAN_SMBCLK
[16] LAN_SMBDATA

07/11 Delete R135 by HP request
07/11 Delete R139 by HP request

C115 0.1U_0402_10V7K — PCIE_PRX_DTX_P6_C
C116 0.1U_0402_10V7K — PCIE_PRX_DTX_N6_C

CLK_REQ_N, PE_RST_N, PE_CLKP, PE_CLKN, PETp, PETn, PERp, PERn — PCIE

LAN_SMBCLK, LAN_SMBDATA — SMBUS

+3VM_LAN — R128 4.7K_0402_5%

MMBT3904_SOT23-3 Q63

[18] LANWAKE#
[25,30] KBC_WAKE#
[18] LAN_DIS#

R569 @ 0_0402_5%

07/11 Delete R151, R152 by HP request
08/07 Add R569 and connection R569.1 to KBC_DS3_EN
10/16 Change R569.1 connection to KBC_WAKE#
10/25 Add Q63

10/26 Delete R153

[33] LAN_ACT#

LED_LINK_LAN#, LAN_ACT# — LED0, LED1, LED2 — LED

T110 JTAG_TDI
T111 JTAG_TDO
JTAG_TMS
JTAG_TCK — JTAG

+3VM_LAN — R154 @ 10K_0402_5% — LAN_JTAG_TMS
R155 @ 10K_0402_5% — LAN_JTAG_TCK

XTAL2
XTAL1 — XTAL_OUT, XTAL_IN

R158 1K_0402_5%
R159 3.01K_0402_1%

TEST_EN, RBIAS

CLARKVILLE

MDI_PLUS0/MINUS0 — LAN_MDIP0/MDIN0
MDI_PLUS1/MINUS1 — LAN_MDIP1/MDIN1
MDI_PLUS2/MINUS2 — LAN_MDIP2/MDIN2
MDI_PLUS3/MINUS3 — LAN_MDIP3/MDIN3

07/11 Delete R140, R142 by HP request

SVR_EN_N
RSVD1_VCC3P3 — 47K_0402_5% R145 — +3VM_LAN
VDD3P3_IN, VDD3P3_4, VDD3P3_15, VDD3P3_19, VDD3P3_29

C117 1000P_0402_50V7K
C505 10U_0603_6.3V6M

11/02 Add C505

VDD0P9_8, VDD0P9_11, VDD0P9_16, VDD0P9_22, VDD0P9_37, VDD0P9_40, VDD0P9_43, VDD0P9_46, VDD0P9_47

+1.05VM_LAN

SHI00004C00 L15 4.7UH +-5% 1008HC-472EJFS-A
DELTA_1008HC-472EJFS-A_2P

CTRL_0P9

C504 @ 10U_0603_6.3V6M
C373 0.1U_0402_16V4Z
C350 47U_0805_6.3V6M

07/06 Add by HP request

11/02 Reserve C504. Change C350 to 47u.

[17] LED_LINK_LAN#_R

LED_LINK_LAN# R — Q34 2N7002_SOT23-3 — LED_LINK_LAN# — R625 0_0402_5% — LED_LINK_LAN_DOCK# [33]

LAN_DIS#

10/26 Connect Q34.3 to LED_LINK_LAN_DOCK# with R625, and delete LED_LINK_LAN_DOCK# connection to Q34.1. Delete R157 and connect Q34.1 and signal LED_LINK_LAN#_R.

+3VM_LAN — R136 10K_0402_5%

LAN_ACT# — R138 300_0603_5% — @680P_0402_50V7K C114

+3VM_LAN — R144 10K_0402_5%

LED_LINK_LAN# — R150 300_0603_5% — @680P_0402_50V7K C118

JP4 ACES_87212-14G0 CONN@

MDO3-, MDO3+, MDO2+, MDO2-, MDO1+, MDO1-, MDO0+, MDO0-

D12 @ SCA00000U10 YSLC05CH_SOT23-3

07/16 Change P/N for ESD's request

TS1 350UH_NA0069RLF SP050006Y00

LAN_MDIP0/MDIN0, LAN_MDIP1/MDIN1, LAN_MDIP2/MDIN2, LAN_MDIP3/MDIN3
+V_DAC
TD1+/TD1-/TD2+/TD2-/TD3+/TD3-/TD4+/TD4-
TDCT1/TDCT2/TDCT3/TDCT4
TX1+/TX1-/TX2+/TX2-/TX3+/TX3-/TX4+/TX4-
TXCT1/TXCT2/TXCT3/TXCT4
MDO0+/MDO0-/MDO1+/MDO1-/MDO2+/MDO2-/MDO3+/MDO3-

C120 0.01U_0402_16V7K
C389 0.1U_0402_16V4Z
C390 0.1U_0402_16V4Z
C391 0.1U_0402_16V4Z
C392 1U_0402_6.3V4Z

07/23 Add C389, C390, C391, C392.

10/25 Delete R160, R161, R162, R163. Add RP12

RP12 75_1206_8P4R_5%

07/23 Change C121 to 1000pF

C121 SE120102K90 1000P_1808_3KV
C122 0.1U_0402_16V4Z
C123 4.7U_0603_6.3V6K
L16 100UH_SSC0301101MCF_0.18A_20%

D13 @ SCA00000U10 YSLC05CH_SOT23-3

07/16 Change P/N for ESD's request

XTAL1
XTAL2

C124 33P_0402_50V8J
C125 33P_0402_50V8J

Y2 25MHZ 18PF +-20PPM CRG3202518

9/27 Change Y2 to 3225 package.

MDO0+ [33]
MDO0- [33]
MDO1+ [33]
MDO1- [33]
MDO2+ [33]
MDO2- [33]
MDO3+ [33]
MDO3- [33]

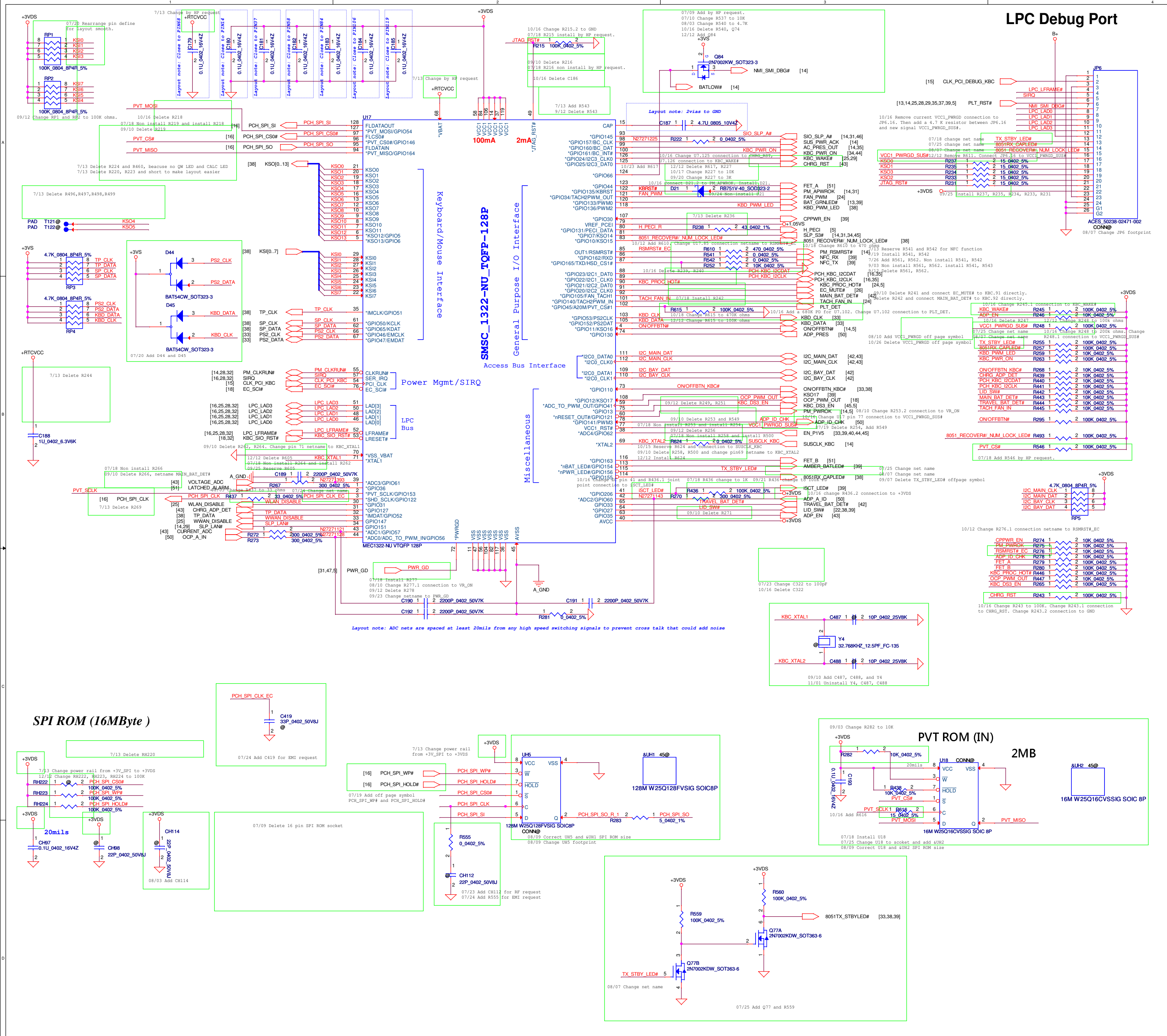
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Intel 82566 Nineveh

Size: — Document Number: LA-9241P — Rev: 0.5

Date: Thursday, December 20, 2012 — Sheet 29 of 56



MEC1322 Pin#	2013/2012 KBC Pin Definition SMSC MEC1322 (KBC 1126)	2013 KBC SMSC MEC1322 Pin Assignment
1	GPIO36	LATCHED_ALARM (Dual battery) CHRG_ADP_DET (Single battery)
2	PVT_SCLK/GPIO153 (GPIO41)	PVT_SPI_CLK
3	SHD_SCLK/GPIO122	SPI_CLK_FLH
4	GPIO11 (GPIO24)/KSO16	PWR_BTN_OUT#
5	KSO13/GPIO6 (GPIO18)	KSO 13
6	KSO12/GPIO5 (GPIO00)	KSO 12
7	KSO11	KSO 11
8	KSO10	KSO 10
9	KSO09	KSO 9
10	KSO08	KSO 8
11	VSS	VSS
12	KSO07	KSO 7
13	KSO06	KSO 6
14	VCC1	VCC1
15	CAP	CAP
16	KSO05	KSO 5
17	KSO04	KSO 4
18	KSO3/JTAG_TDO	KSO 3
19	KSO2/JTAG_TDI	KSO 2
20	KSO1/JTAG_TMS	KSO 1
21	KSO0/JTAG_TCK	KSO 0
22	KSI7	KSI7
23	KSI6	KSI6
24	KSI5	KSI5 (Volume Down - Tablet Only)
25	KSI4/TRACECLK	KSI4 (Volume Up - Tablet Only)
26	KSI3/TRACEDATA0	KSI3 (QUICKX)
27	KSI2/TRACEDATA1	KSI2 (CALCULATOR)
28	KSI1/TRACEDATA2	KSI1 (WIRELESS)
29	KSI0/TRACEDATA3	KSI0 (MUTE)
30	GPIO31 (GPIO39)	WLAN_DISABLE (O, MC2)
31	GPIO127 (GPIO42)	ADP_DET
32	IMDAT/GPIO52	IMDAT
33	GPIO147 (GPIO38)	WWAN_DISABLE (O, MC1)
34	GPIO151 (GPIO37)	SLP_LAN# (I, AMT)
35	IMCLK/GPIO51	IMCLK
36	VSS	VSS
37	VCC1	VCC1
38	ADC4/GPIO62 (GPIO50)	SLP_S4# (I, AMT)
39	ADC3/GPIO61 (GPIO23)	VOLTAGE_ADC
40	AVCC	AVCC
41	GPIO206 (ADC_VREF)	5VA_PWR_EN
42	ADC2/GPIO60 (GPIO40)	ADP_ID_ADC
43	ADC1/GPIO57 (GPIO46)	CURRENT_ADC
44	ADC0/ADC_TO_PWM_IN/GPIO56	OCP_IN_ADC
45	AVSS	AVSS
46	LAD0	LPC_3S_AD0
47	VSS	VSS
48	LAD1	LPC_3S_AD1
49	JTAG_RST# (VCC2)	JTAG_RST#
50	LAD2	LPC_3S_AD2
51	LAD3	LPC_3S_AD3
52	LFRAME#	LPC_3S_FRAME#
53	LRESET#	LPC_RESET#
54	PCI_CLK	CLK_R3S_KBPCI
55	CLKRUN#	PCI_3S_CLKRUN#
56	VSS	VSS
57	SER_IRQ	PCI_3S_SERIRQ_R
58	VCC1	VCC1
59	ADC_TO_PWM_OUT/GPIO41 (GPIO19)	OCP_PWM_OUT
60	nRESET_OUT/GPIO121 (GPIO06)	PM_PWROK
61	GPIO50/KCLK	TP_CLK
62	GPIO65/KDAT	TP_DAT
63	GPIO35	ADP_EN (O)
64	GPIO27 (GPIO34)	LID_SW# (I)
65	GPIO33	TRAVEL_BAT_DET# (Dual battery) FREE (Single battery)
66	GPIO46/EMCLK	DOCK_EMCLK, FREE
67	GPIO47/EMDAT	DOCK_EMDAT, FREE
68	VBAT	VCC0
69	XTAL2 (TEST_PIN)	XTAL2
70	VSS_VBAT (PWMOK_PWMDEAD# [CKT#2]/GPIO51)	VSS_VBAT
71	XTAL1 (32KHZ_INPUT)	SUSCLK32_KBC
72	PWRGD (GPIO52/PWM3)	PWR_GOOD_3
73	GPIO110 (GPIO25)	ON/OFFBTN_KBC# (I)
74	GPIO130 (ADP_PRES [CKT#2]/GPIO27)	ADP_PRES (I)
75	GPIO13 (32KHZ_OUT/GPIO22)	KBC_DS3_PWR_EN
76	nEC_SCI	RUNSCI_EC#
77	VCC1_RST#	VCC1_RST#
78	GPIO141/PWM3 (PWRGD)	ADP_ID_CHK (AeroSmith & Van Halen only) AMD_SPI_SECURITY (Tesla & Toto Only)
79	VREF_PECI	VREF_PECI connects to 1.05S_VCCP
80	GPIO131/PECI_DATA (GPIO03)	PECI_DATA
81	GPIO7 (GPIO04)/KSO14	SLP_S3# (I)
82	VSS	VSS
83	GPIO10 (GPIO05)/KSO15	8051_RECOVER#/ NUM_LOCK_LED#
84	VCC1	VCC1
85	OUT1/RSMRST#	PM_RSMRST#
86	GPIO162 (GPIO08)/RXD	NFC_RX
87	GPIO165 (GPIO09)/TXD/SHD_CS1#	NFC_TX
88	GPIO23 (GPIO11)/I2C1_DAT0 (AB2_DATA)	PCH_KBC_DATA
89	GPIO22 (GPIO12)/I2C1_CLK0 (AB2_CLK)	PCH_KBC_CLK
90	GPIO21 (GPIO13)/I2C2_DAT0 (AB4_DATA)	PROCHOT_KBC (O)
91	GPIO20 (GPIO14)/I2C2_CLK0 (AB4_CLK)	A_SD (O)
92	GPIO105 (GPIO15)/FAN_TACH1	MAIN_BAT_DET# (I)
93	GPIO145 (GPIO28)	PM_SLP_A# (I, AMT)
94	PVT_MISO/GPIO164 (HSTDATAIN/GPIO43)	PVT_SPI_MISO
95	SHD_FLDATAIN	SPI_SO_FLASH
96	PVT_CS0#/GPIO146 (HSTCS0#/GPIO44)	PVT_SPI_CS0#
97	SHD_FLCS0#	SPI_CS0#_FLASH
98	GPIO157 (GPIO29)/BC_CLK	SUS_PWR_ACK (I, ME)
99	GPIO160 (GPIO30)/BC_DAT	ADP_PRES_OUT (C)
100	GPIO161 (GPIO31)/BC_INT#	KBC_PWR_ON (O)
101	GPIO140 (GPIO16)/TACH2PWM_IN	TACH_FAN_IN
102	GPIO45 (GPIO17)/A20M/PVT_CS#1	PLT_DET
103	GPIO53 (GPIO20)/PS2CLK	DOCK_KBD_CLK, FREE
104	VSS	VSS
105	GPIO152 (GPIO21)/PS2DAT	DOCK_KBD_DATA, FREE
106	VCC1	VCC1
107	GPIO30 (GPIO01)	CPPWR_EN (O)
108	GPIO12 (GPIO26)/KSO17	KSO17 Buttons: Mute/Wireless
109	IC20_DATA1 (AB1B_DATA)	SDA_MBAY (W & B only), FREE
110	IC20_CLK1 (AB1B_CLK)	SCL_MBAY (W & B only), FREE
111	IC20_DATA0 (AB1A_DATA)	BAT_CHGR_I2C_DAT (S, M, & P only)
112	I2C0_CLK0 (AB1A_CLK)	BAT_CHGR_I2C_CLK (S, M, & P only)
113	nBAT_LED/GPIO154	AMBER_BATLED#
114	GPIO155 (nFDD_LED/8051RX)	CAPS_LED#/8051RX
115	nPWR_LED /GPIO156 (nPWR_LED/8051TX)	S3_LED#/8051TX
116	GPIO163 (CFETB/GPIO10)	FET_B (O)
117	VSS	VSS
118	GPIO136/PWM2 (CHRGCTL_PWM/OUT11)	KBD_PWM_LED#
119	VCC1	VCC1
120	GPIO133/PWM0 (OUT10/PWM0)	BAT_GRNLED# (O)
121	GPIO34/TACH2PWM_OUT (OUT9)	FAN_PWM (O)
122	GPIO135/KBRST (OUT8)	M_PWROK_EN
123	GPIO44 (CFETA/OUT7/nSMI)	FET_A (O)
124	GPIO66 (OUT0)	NMI_SMI_DBG# (O)
125	GPIO25/I2C3_DAT0 (GPIO53/AB3_DATA)	FREE
126	GPIO24/I2C3_CLK0 (GPIO32/AB3_CLK)	FREE
127	PVT_MOSI/GPIO54 (HSTDATAOUT/GPIO45)	PVT_SPI_MOSI
128	SHD_FLDATAOUT	SPI_SI_FLASH

Security Classification	Compal Secret Data		
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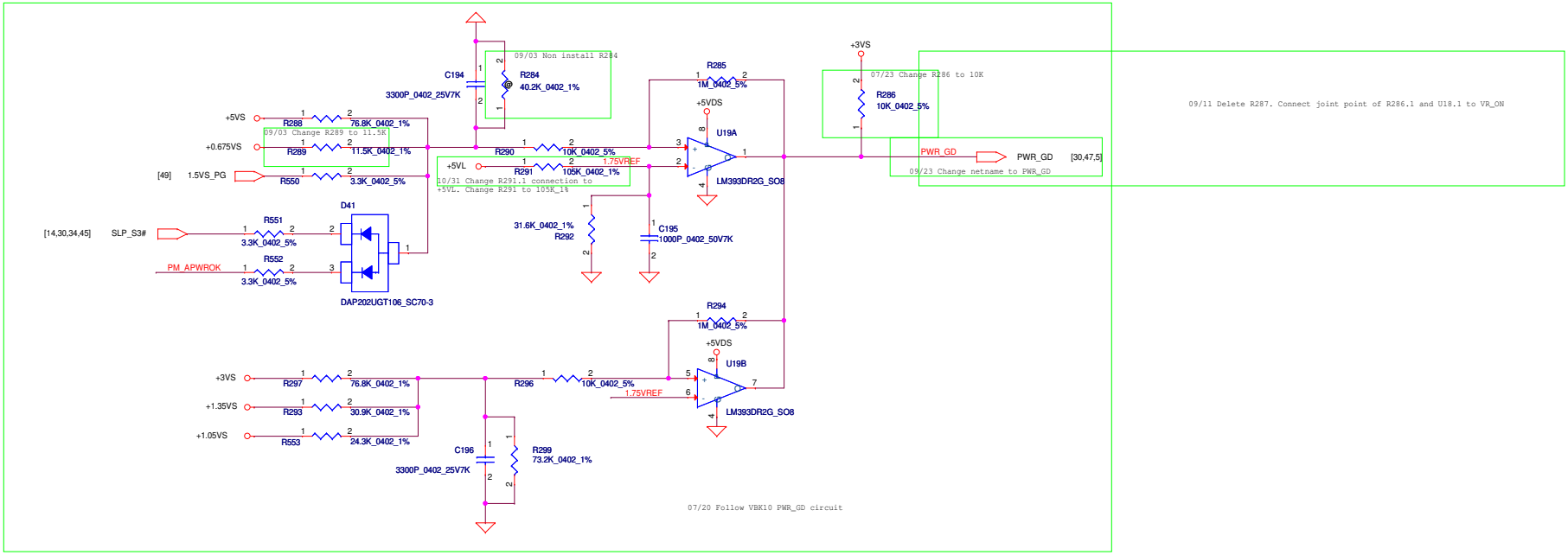
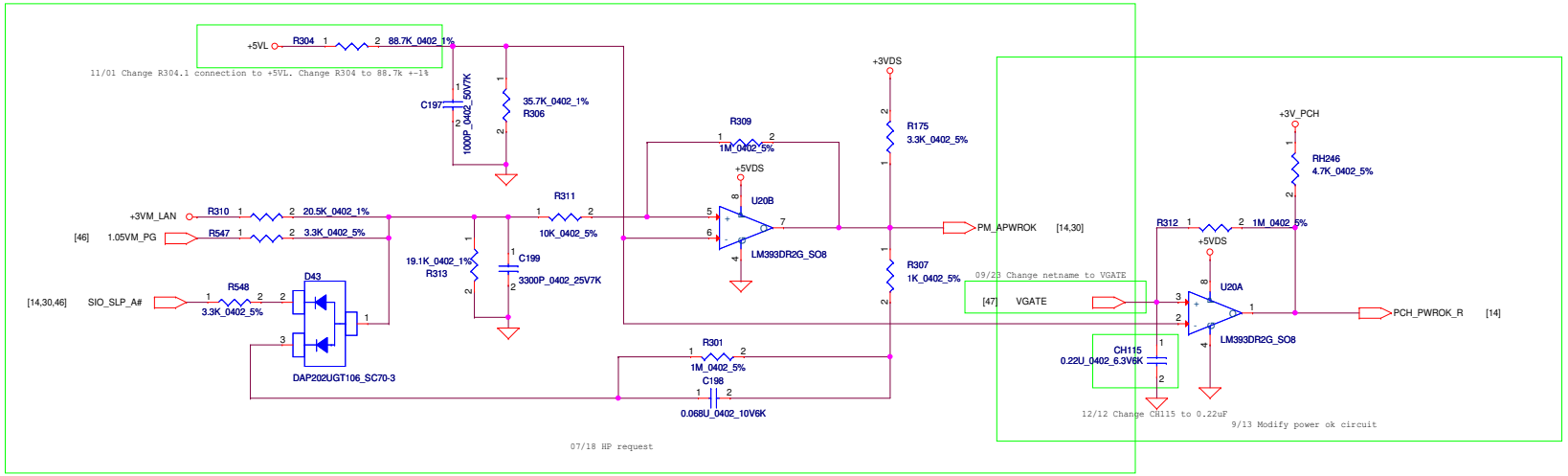
Compal Electronics, Inc.

Title: KBC1322

Document Number: LA-9241P — Rev 0.5

Date: Thursday, December 20, 2012 — Sheet 30 of 56





Security Classification	Compal Secret Data		
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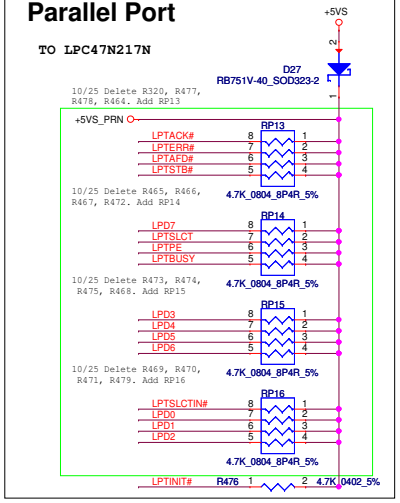
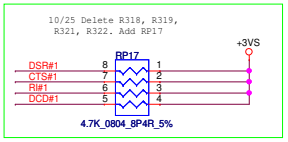
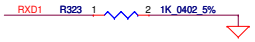
Compal Electronics, Inc.			
Title	POK CKT		
Size	Document Number		Rev
	LA-9241P		0.5
Date:	Thursday, December 20, 2012	Sheet	31 of 56

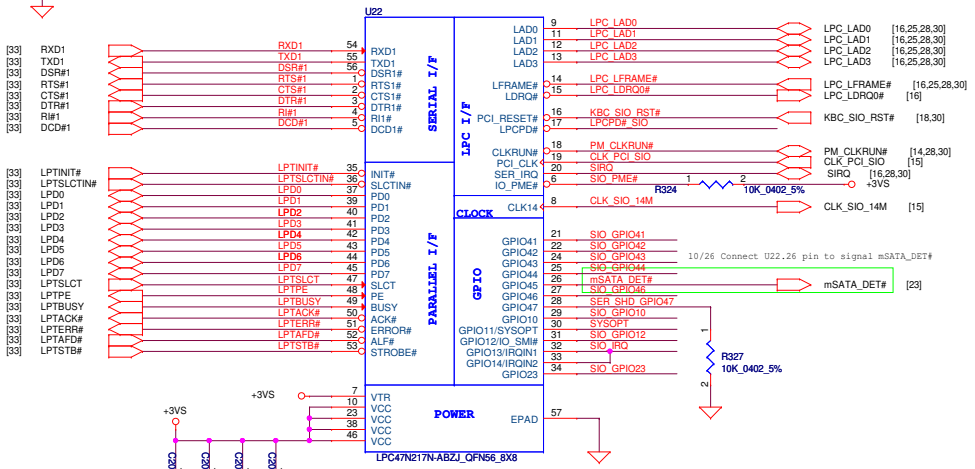
Parallel Port

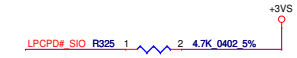
TO LPC47N217N

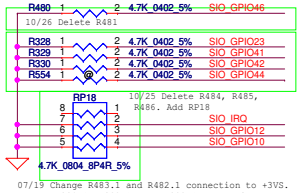




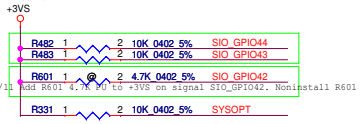






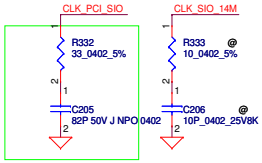


07/19 Change R483.1 and R482.1 connection to +3VS.
Change R330.1, R329.1, and R328.1 connection to GND
07/20 Reserve SIO_GPIO44 PD R554, and modify R328, R329, R330 value to 4.7K. Modify R482, R483 value to 10K



09/11 Add R601 4.7K 5% to +3VS on signal SIO_GPIO42. Noninstall R601

Base I/O Address
0 = 02Eh
1 = 04Eh



11/07 Change R332 to 33 ohms, C205 to 82pF and install R332 and C205

GPIO44	GPIO43	GPIO42	GPIO41	GPIO23	
0	1	0	0	0	Viper 4 DIMM
1	1	1	0	0	Viper 2 DIMM

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2009/09/09

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Title: SUPER I/O LPC47N217N-ABZJ

Size | Document Number: LA-9241P | Rev: 0.5

Date: Thursday, December 20, 2012 | Sheet 32 of 56

DOCK CONN. 184PIN

DOCKING CONNECT

(1) PCI Express x1 channels
(2) PS/2 Interfaces
(2) USB 2.channels
(2) SATA Channels
(2) Display Port Channels
(1) Serial Port
(1) Parallel Port
(1) Line In
(1) Line Out
(1) RJ45 (10/100/1000)
(1) VGA
(1) 2 LAN indicator LED's
(1) Power Button
(1) I2C interface

Quick SW

GPU

IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2009/12/31

Compal Electronics, Inc.

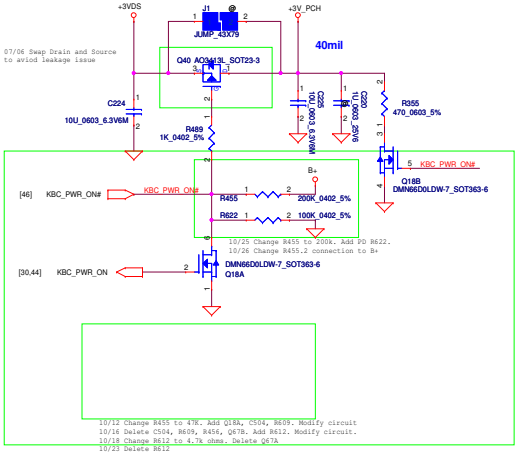
Title: DOCK CONN

Size: Custom | Document Number: LA-9241P | Rev: 0.5

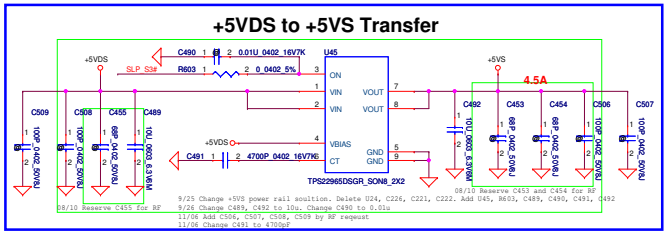
Date: Thursday, December 20, 2012 | Sheet 33 of 56

+3VALW TO +3VALW(PCH AUX Power)

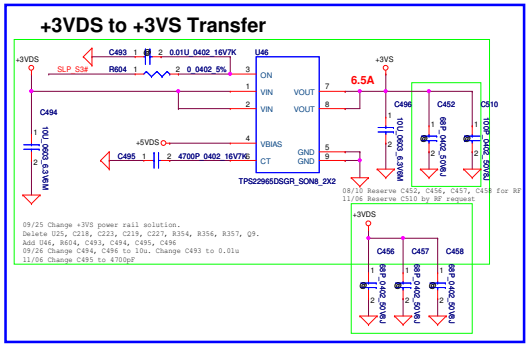
Short J1 for PCH VCCSUS3.3



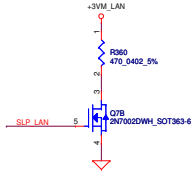
+5VDS to +5VS Transfer



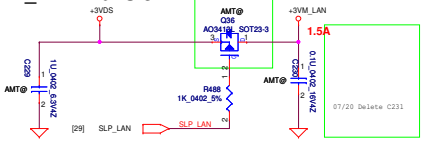
+3VDS to +3VS Transfer

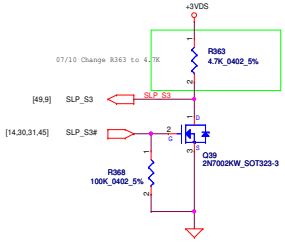


Discharge circuit-2 for V-M

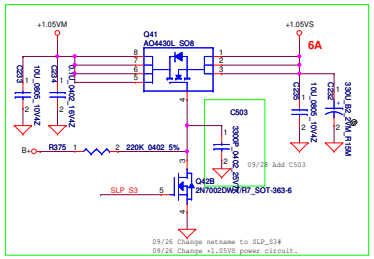


+3VALW to +3VM_LAN Transfer

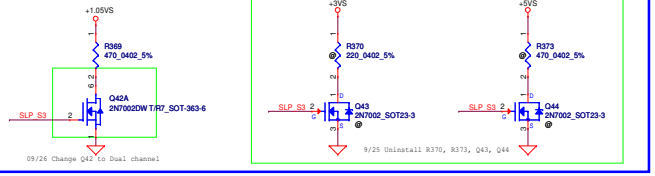




+1.05VM to +1.05VS Transfer



Discharge circuit-1



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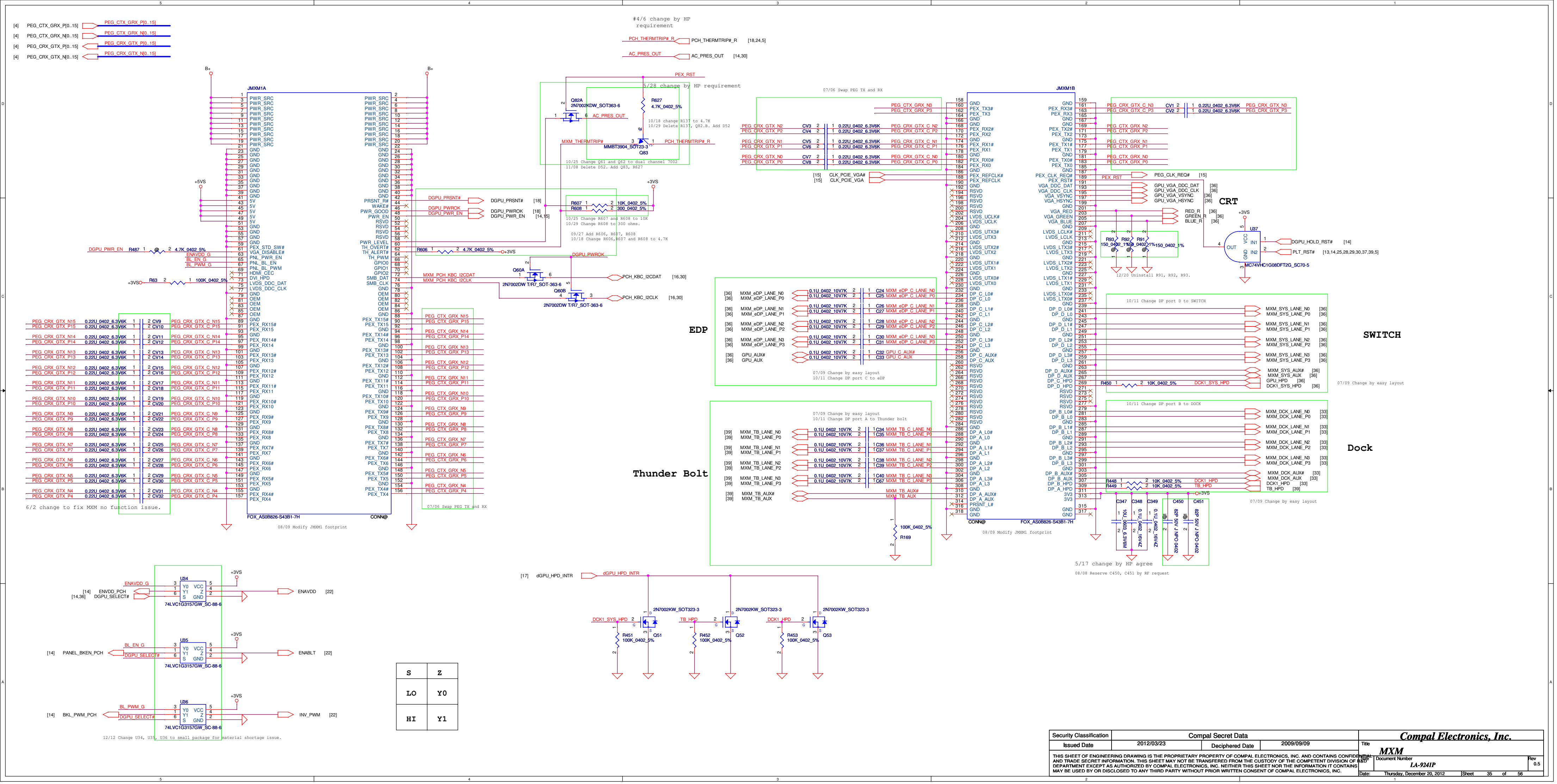
Issued Date	2012/03/23	Deciphered Date	2009/12/31

Compal Electronics, Inc.	
Title	DC/DC Circuits
Size	Document Number: LA-9241P
Rev	0.5
Date: Thursday, December 20, 2012	Sheet 34 of 56



S	Z
LO	Y0
HI	Y1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2009/09/09	Title: MXM
			Size / Document Number: LA-9241P / Rev 0.5
			Date: Thursday, December 20, 2012 / Sheet 35 of 56

eDP MUX

07/17 Modify eDP MUX solution to PI3VDP12413

From CPU

From GPU

07/27 Add R563, R564

07/23 Modify net name

07/19 Delete CC70, CC71, CC75, CC76, CC77, CC78, CC79, CC80, CC81, CC82

07/23 Delete R516 and CC84

07/23 Change to dual channel MOS Q76

Truth Table for 42 pin package

OE	GPU_SEL	AUX_HPD_SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down

DP MUX

07/17 Modify DP MUX solution to PI3VDP12412

M/B DP

Docking

07/23 Modify net name

07/23 Delete R545 and C371

07/23 Change dual channel MOS Q76

Truth Table for 42 pin package

OE	GPU_SEL	AUX_HPD_SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down

Table 1. DDC Truth Table

EN	S01	S00	FUNCTION
0	X	X	ALL SWITCHES HIGH IMPEDANCE
1	0	0	SDAA to SDA1 SCLA to SCL1
1	0	1	SDAB to SDA1 SCLB to SCL1
1	1	0	SDAA to SDA2 SCLA to SCL2
1	1	1	SDAB to SDA2 SCLB to SCL2

X = don't care

Table 2. RGB/HSYNC, VSYNC Truth Table

EN	S11	S10	FUNCTION	
0	X	X	ALL SWITCHES HIGH IMPEDANCE, AND SH1,SH2,SV1, SV2 = 0V	
1	0	0	REDA to RED1 GRNA to GRN1 BLUA to BLU1	SHA to SH1 SVA to SV1
1	0	1	REDB to RED1 GRNB to GRN1 BLUB to BLU1	SHB to SH1 SVB to SV1
1	1	0	REDA to RED2 GRNA to GRN2 BLUA to BLU2	SHA to SH2 SVA to SV2
1	1	1	REDB to RED2 GRNB to GRN2 BLUB to BLU2	SHB to SH2 SVB to SV2

X = don't care

MAX14885E

09/07 Delete VGA_RED, VGA_GRN, VGA_BLU, VGA_DDCCLK, VGA_DDCDATA, CRT_HSYNC, and CRT_VSYNC off page symbol

07/25 Combine Q56 and Q57 to Q79

09/07 Add JVGA2 circuit

9/21 Correct netname.

10/25 Delete R570, R571, R572. Add RP19

12/20 Change RP19 to 150ohms

09/12 Modify JVGA2 footprint

10/31 Modify JVGA2 footprint

CONN@

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2009/12/31

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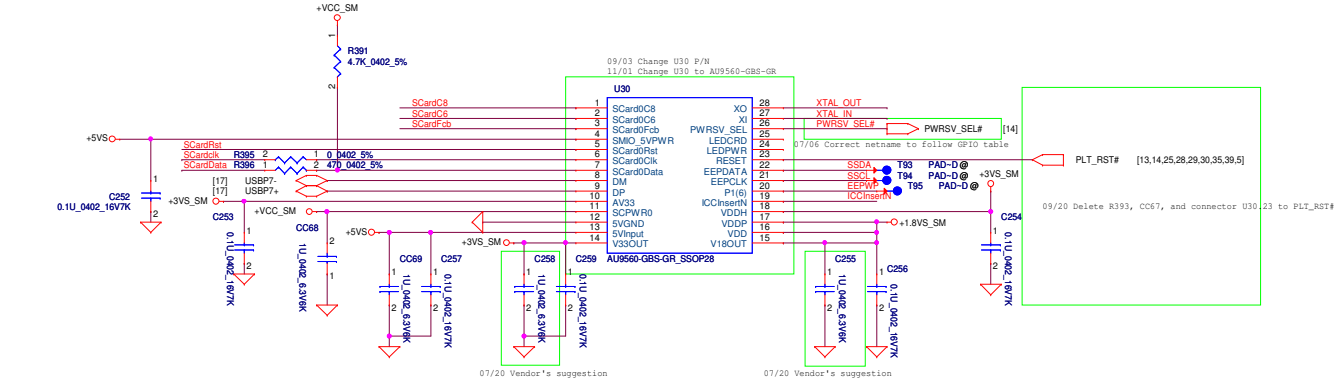
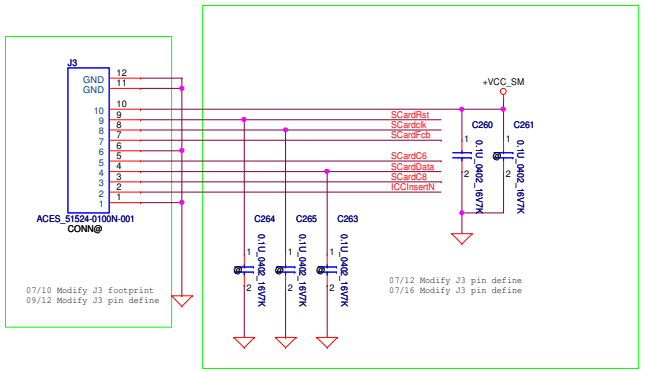
Compal Electronics, Inc.

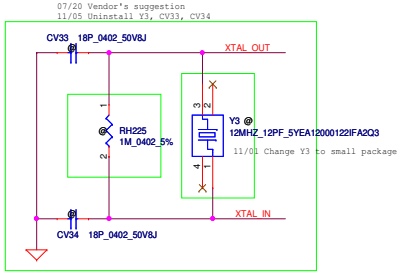
Title: Switch/MUX/VGA

Size: C | Document Number: LA-9241P | Rev: 0.5

Date: Thursday, December 20, 2012 | Sheet 36 of 56







Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/06/29

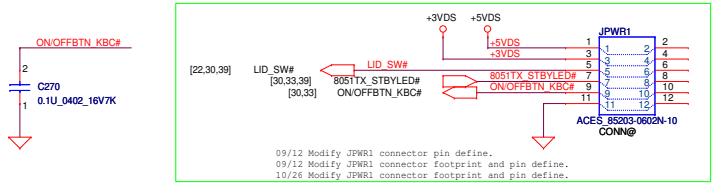
Compal Electronics, Inc.

Title: Smart Card

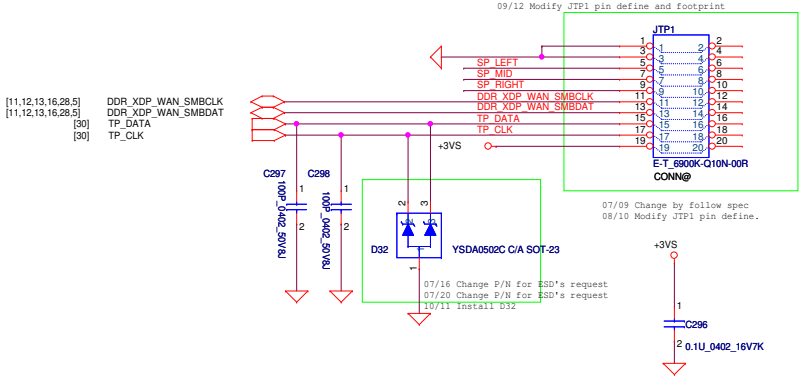
Size	Document Number	Rev
C		0.5

Date: Thursday, December 20, 2012 | Sheet 37 of 56

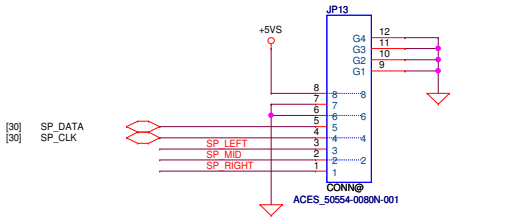
Power Board Conn

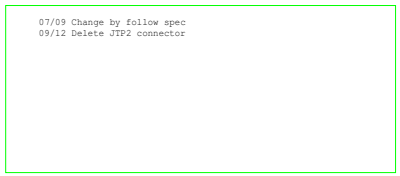


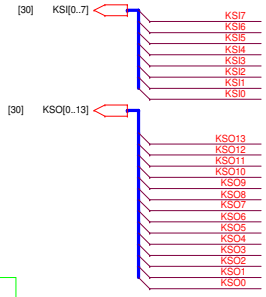
TP/B Conn

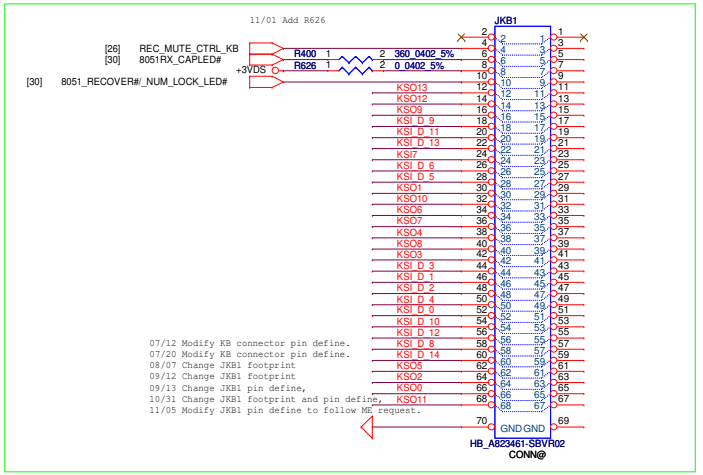


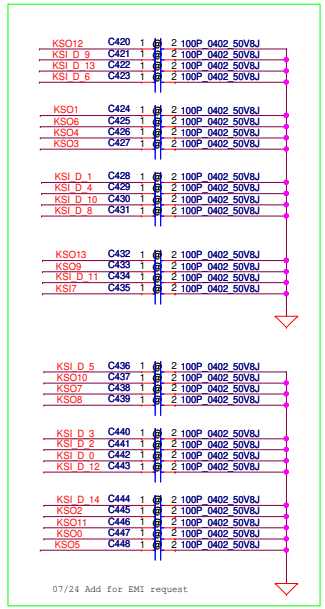
Stick Point CONN

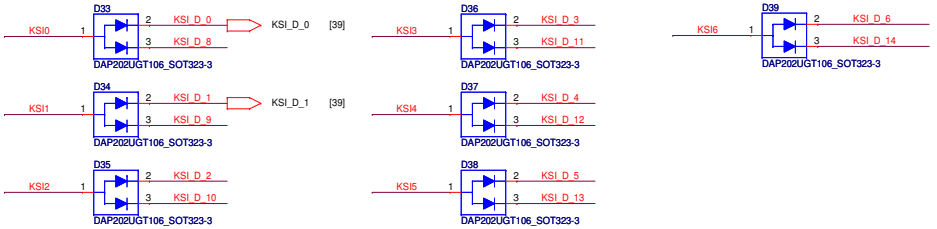




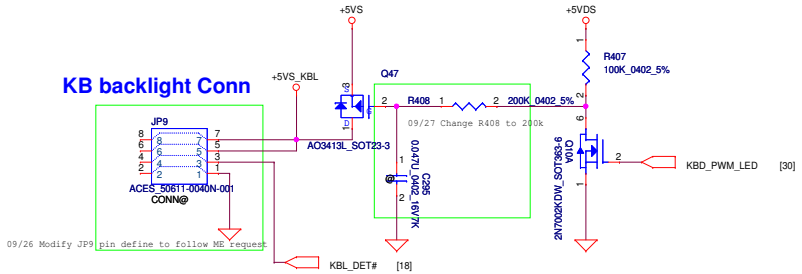








KB backlight Conn



Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: KB/TP/LED

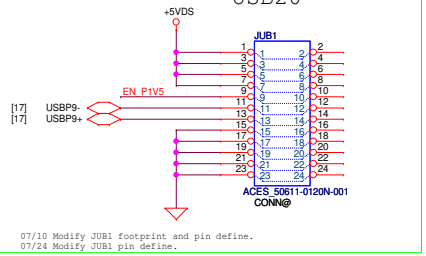
Size	Document Number	Rev
Custom		0.5

Date: Thursday, December 20, 2012 | Sheet 38 of 56

VGA+Function Board

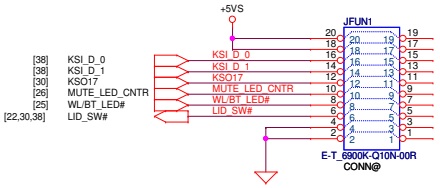
9/07 Remove JVGA1 BTB connector

USB20



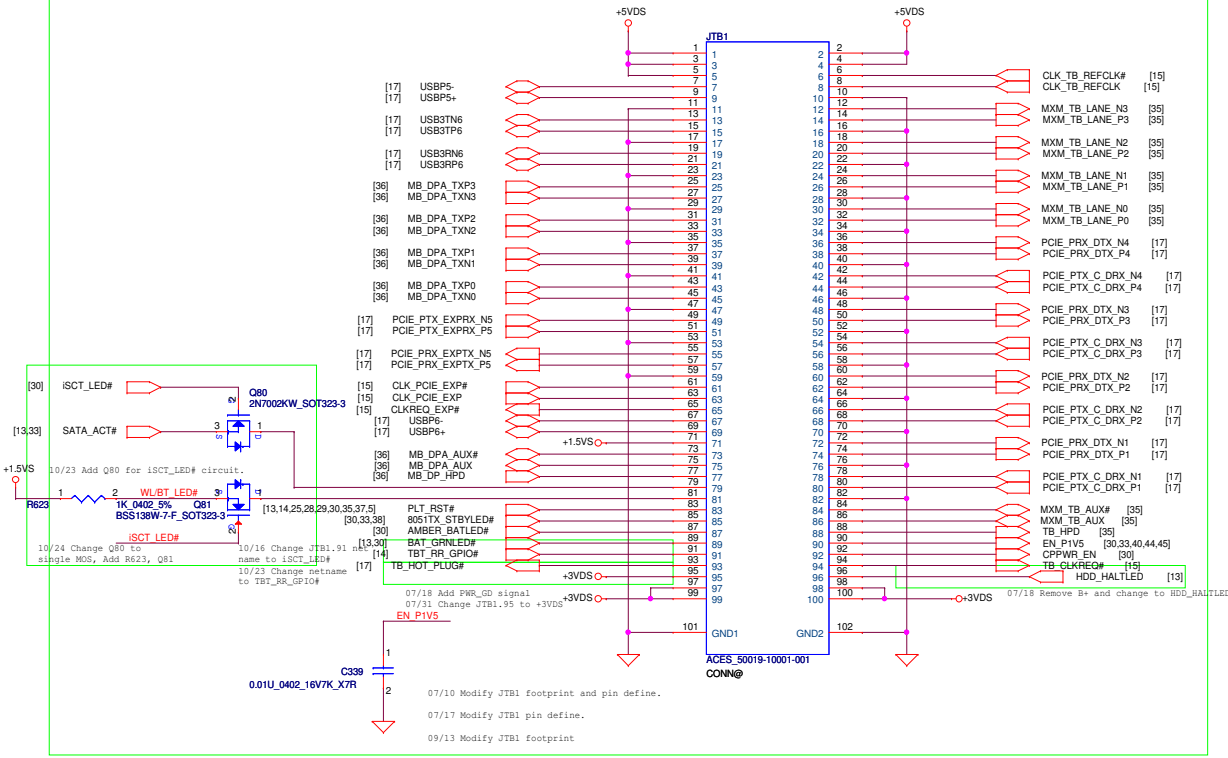
07/10 Modify JUB1 footprint and pin define.
07/24 Modify JUB1 pin define.

Function Board

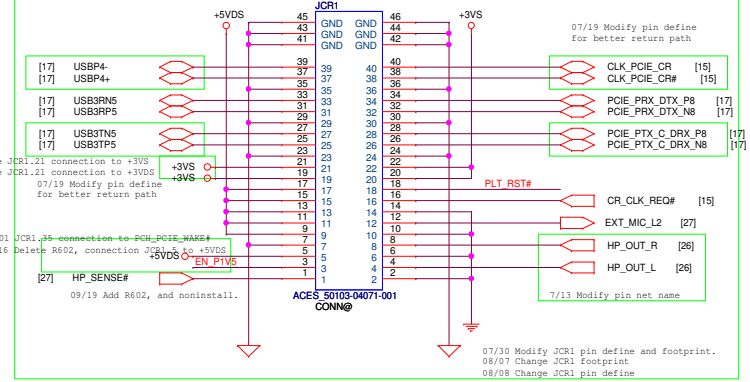


9/07 Add JFUN1 connector
9/12 Modify JFUN1 pin define and footprint
09/26 Modify JFUN1 pin define to follow ME request

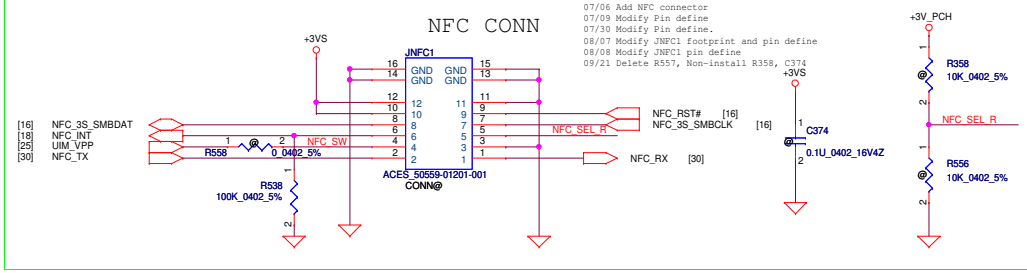
Thunderbolt



Card Reader Board



NFC CONN



07/06 Add NFC connector
07/09 Modify Pin define
07/30 Modify Pin define.
08/07 Modify JNFC1 footprint and pin define
08/08 Modify JNFC1 pin define
09/21 Delete R557, Non-install R358, C374

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2010/03/31

Compal Electronics, Inc.

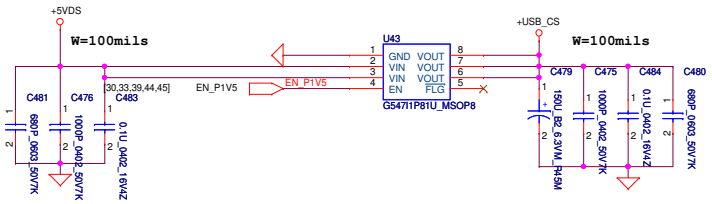
Title: **I/O CONN**

Size	Document Number	Rev
	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 39 of 56

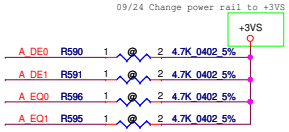
USB Power Switch

9/07 Add USB3.0 repeater and connector



change power switch to high active parts
20120803

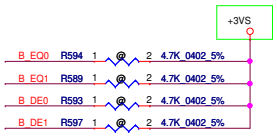
09/24 Change power rail to +3VS



Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~150K次
[A_EQ1, A_EQ0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 5dB de-emphasis
HH: Reserved

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~150K次
[A_EQ1, A_EQ0] ==
LL: adaptive EQ enable
LH: program EQ at 3.5dB
HL: program EQ at 6dB
HH: program EQ at 10dB

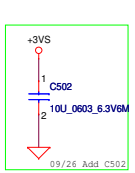
09/24 Change power rail to +3VS



Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~150K次
[B_EQ1, B_EQ0] ==
LL: adaptive EQ enable
LH: program EQ at 3.5dB
HL: program EQ at 6dB
HH: program EQ at 10dB

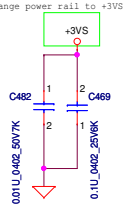
Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~150K次
[B_EQ1, B_EQ0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 5dB de-emphasis
HH: Reserved

09/24 Change power rail to +3VS



09/26 Add C502

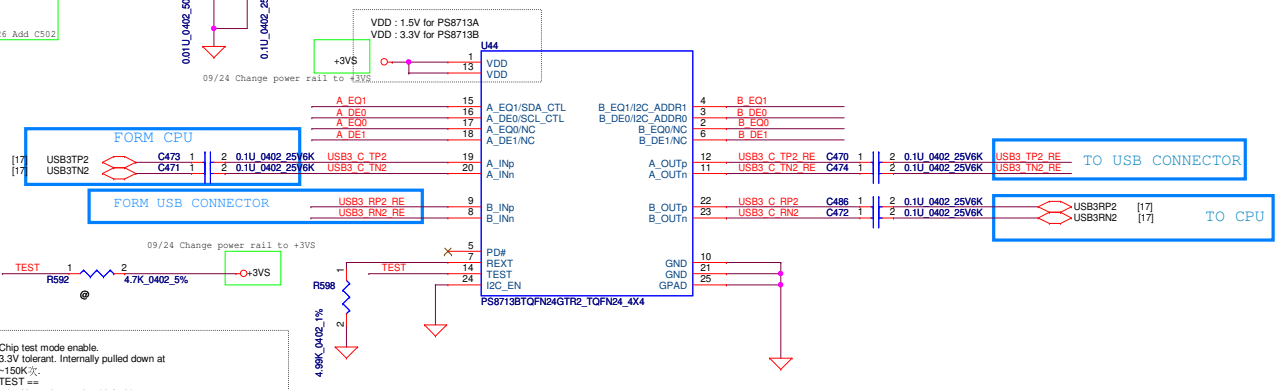
09/24 Change power rail to +3VS



USB3.0 Repeater

09/24 Delete Q79, Q80, C475, C477, C478, R588, R587.

Add DC to DC interface
2012/8/3

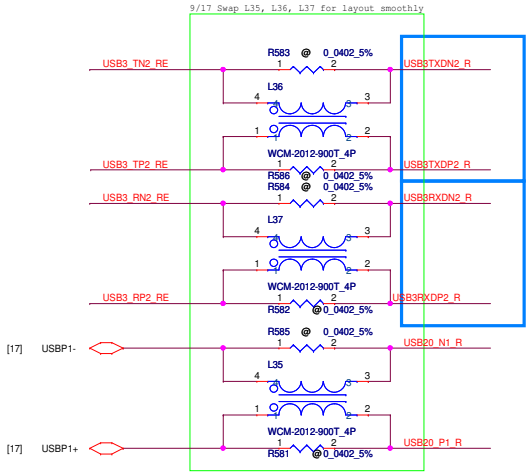


Chip test mode enable.
3.3V tolerant. Internally pulled down at ~150K次.
TEST ==
L: Normal operation (default)
H: Test mode enable

Folow ESD team recommeend change ESD diode D5 D6
20120713

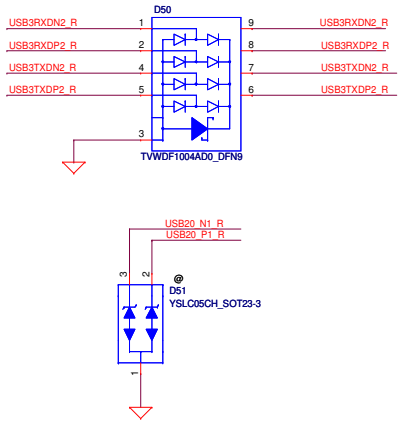
USB3.0 Connector

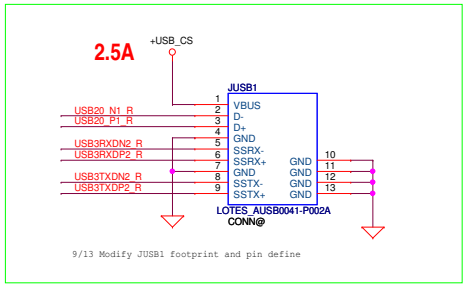
9/17 Swap L35, L36, L37 for layout smoothly



TO USB connector TX

TO USB connector RX





9/13 Modify JUSB1 footprint and pin define

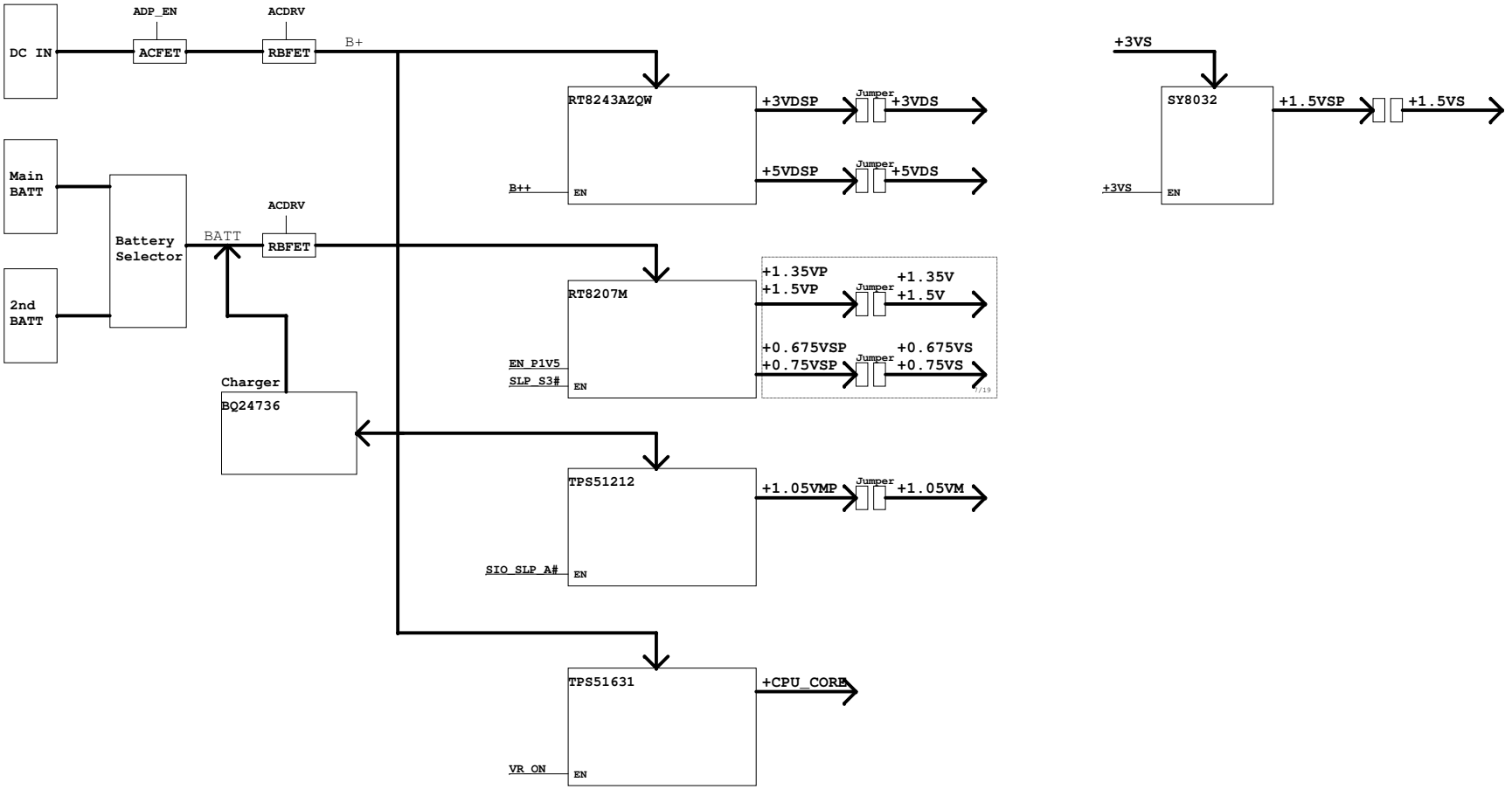
Security Classification	Compal Secret Data		
Issued Date	2012/05/11	Deciphered Date	2013/05/11

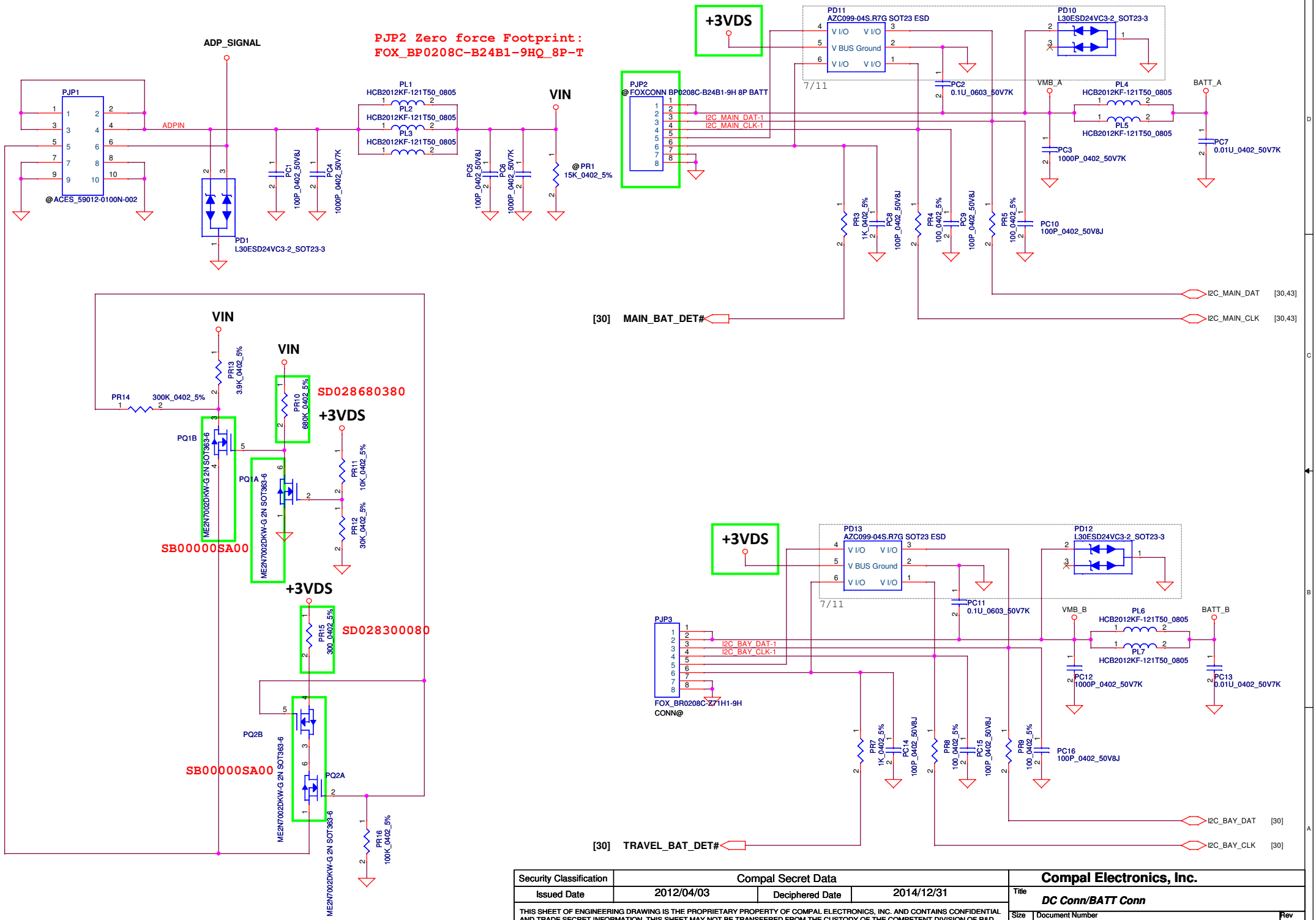
Compal Electronics, Inc.

Title: USB3.0 CONN/Repeater

Size	Document Number	Rev
Custom	LA-9241P	0.5

Date: Thursday, December 20, 2012 | Sheet 40 of 56

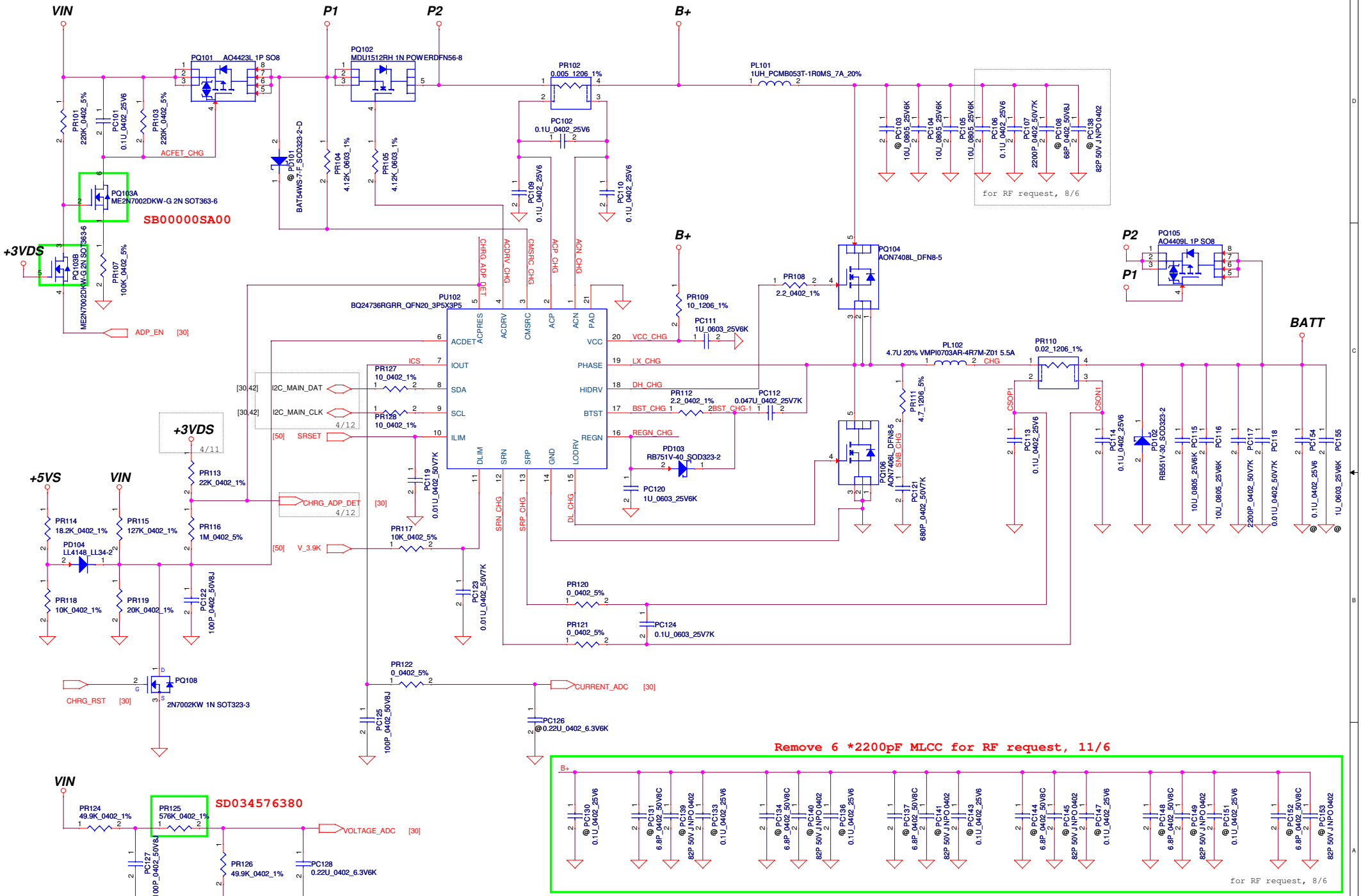

DC IN
ADP_EN
ACFET
ACDRV
RBFET
B+
Main BATT
2nd BATT
Battery Selector
BATT
ACDRV
RBFET
Charger
BQ24736
RT8243AZQW
B++
EN
+3VDSP
Jumper
+3VDS
+5VDSP
Jumper
+5VDS
RT8207M
EN_P1V5
SLP_S3#
EN
+1.35VP
+1.5VP
Jumper
+1.35V
+1.5V
+0.675VSP
+0.75VSP
Jumper
+0.675VS
+0.75VS
TPS51212
SIO_SLP_A#
EN
+1.05VMP
Jumper
+1.05VM
TPS51631
VR_ON
EN
+CPU_CORE
+3VS
SY8032
+3VS
EN
+1.5VSP
+1.5VS



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*DC Conn/BATT Conn*	
Size	Document Number: **15W**	Rev: 0.3
Date: Thursday, December 20, 2012	Sheet 42 of 52	



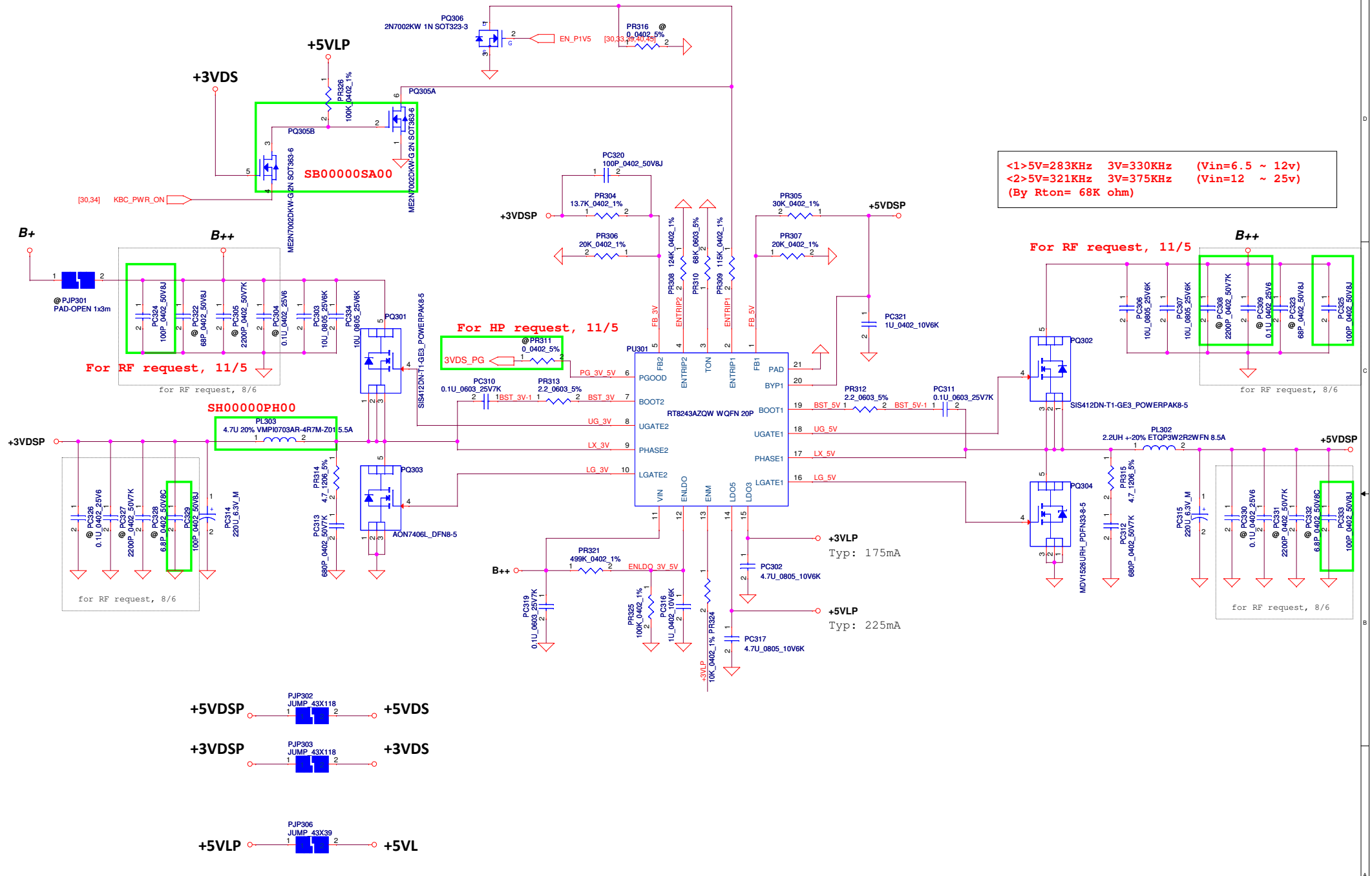
Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***CHARGER***

Size: Document Number: **15W** Rev: **0.3**

Date: Thursday, December 20, 2012 Sheet 43 of 52



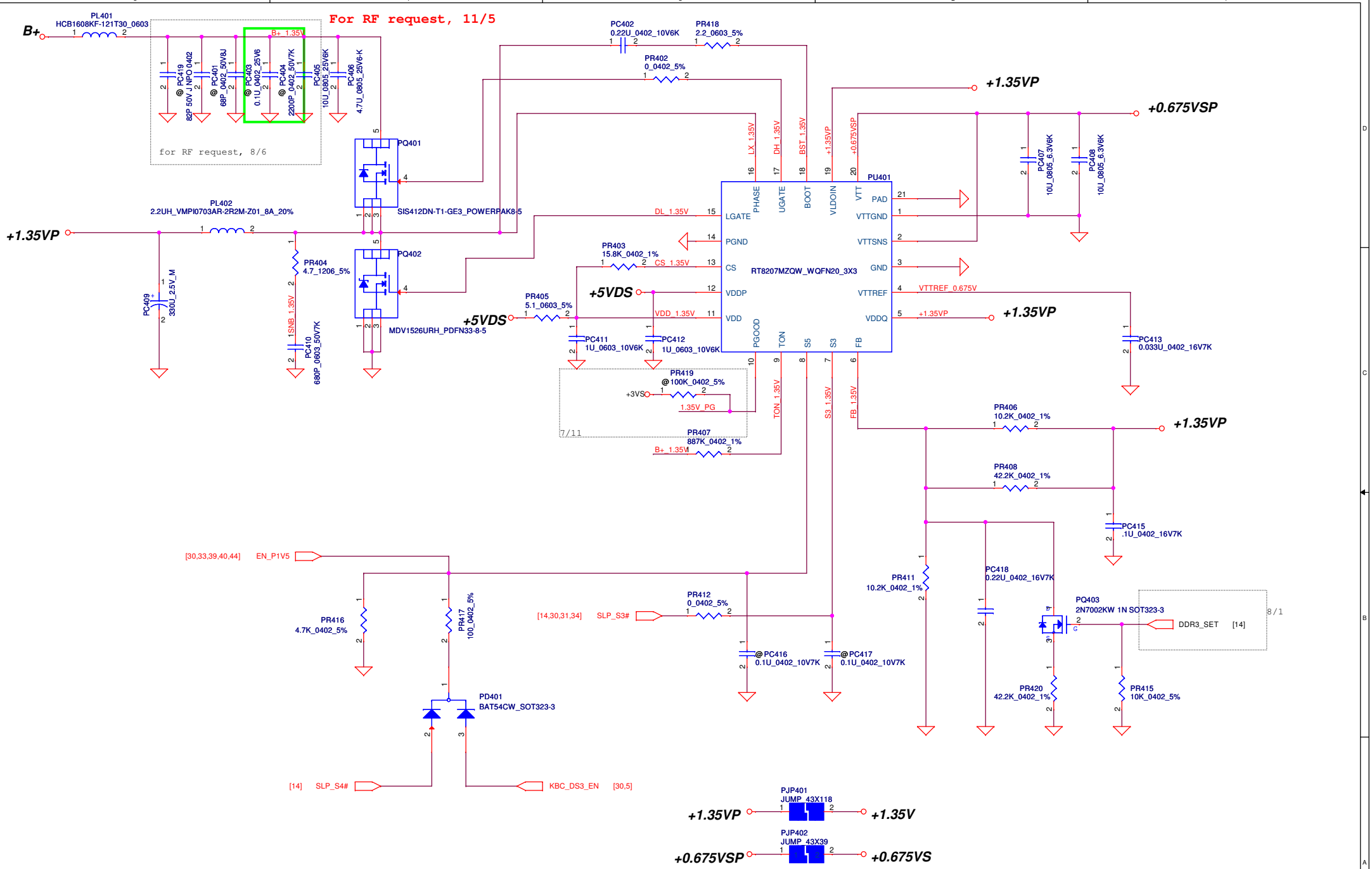
Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: 3VDSP/5VDSP

Size	Document Number	Rev
Custom	15W	0.3

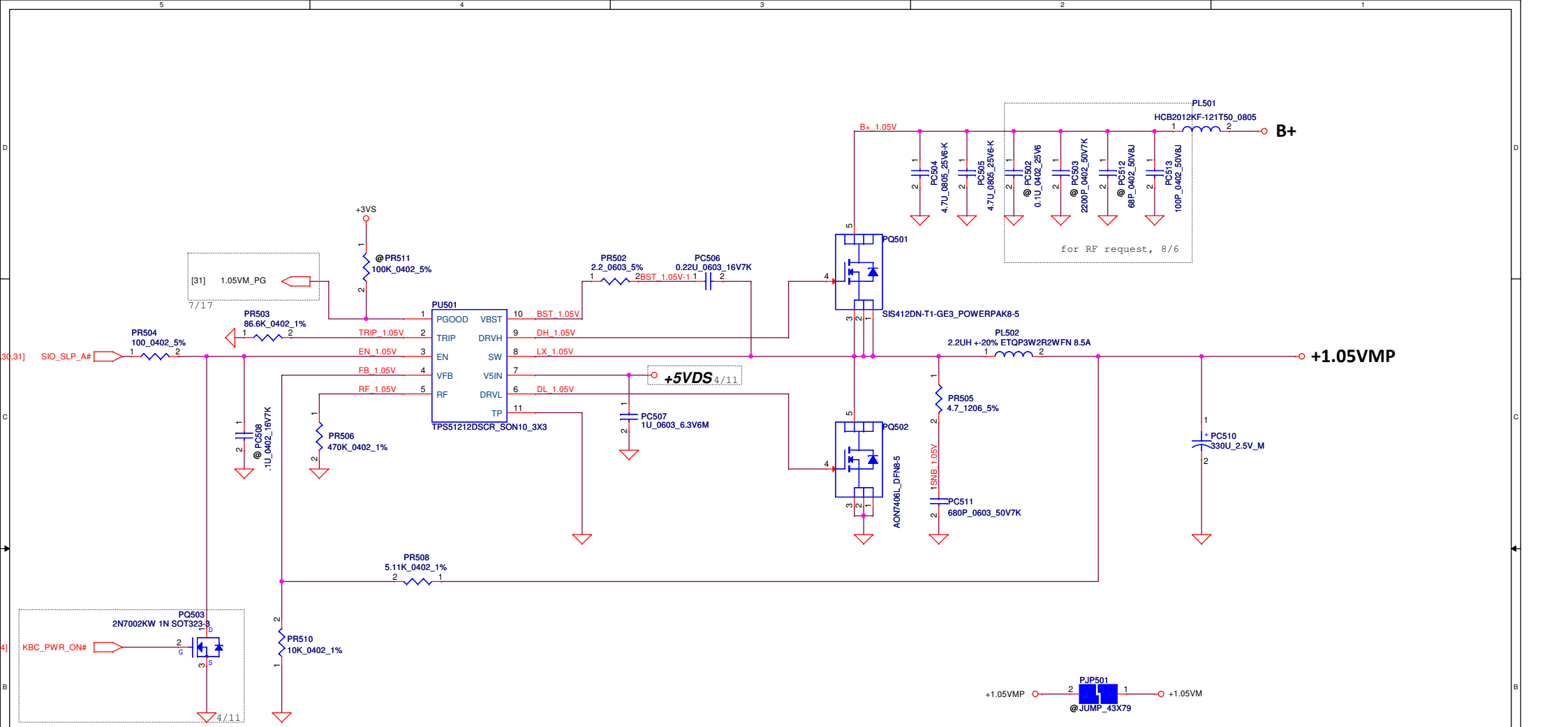
Date: Thursday, December 20, 2012 | Sheet 44 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

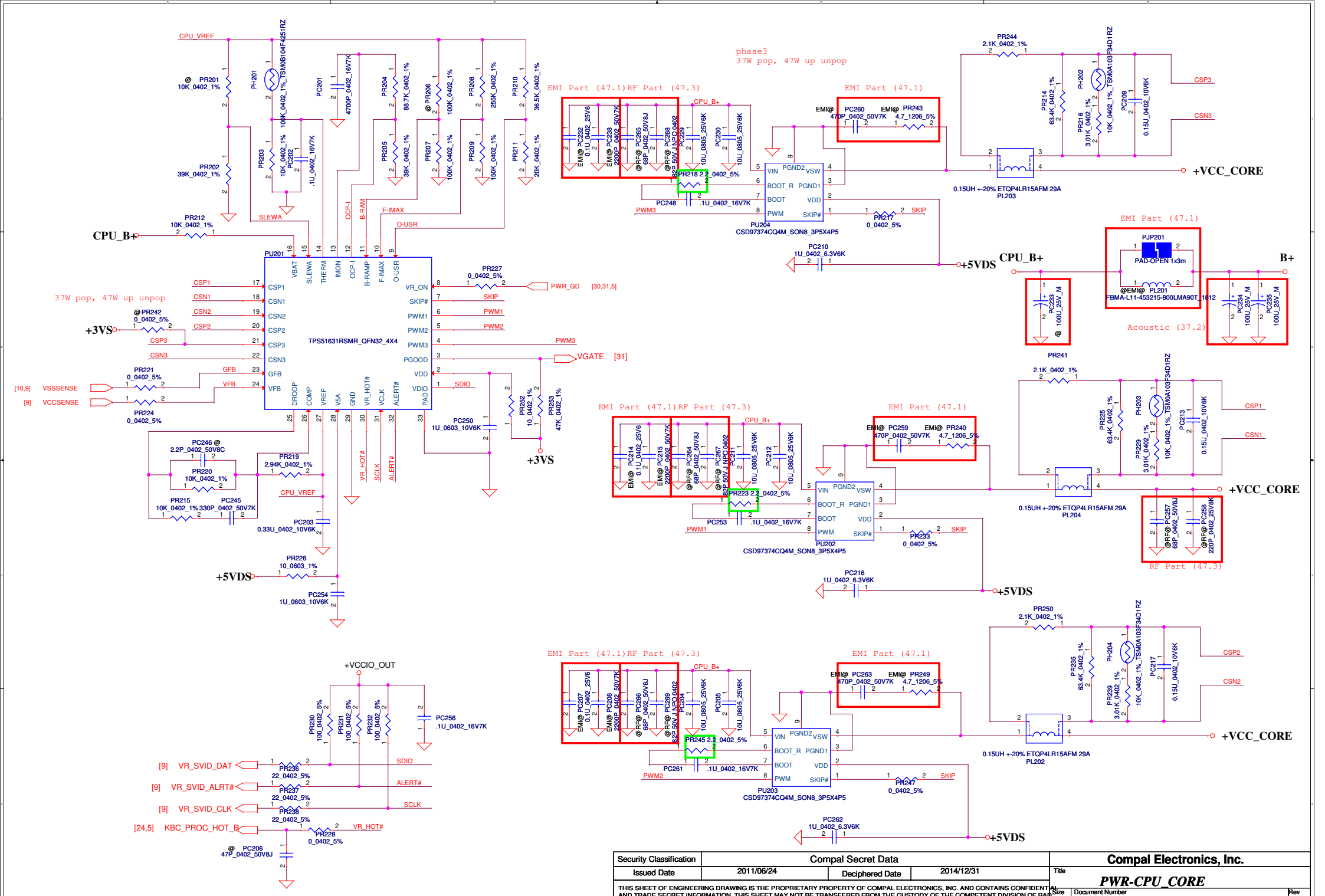
Title	***DDR Power***	
Size	Document Number **15W**	Rev 0.3
Date: Thursday, December 20, 2012	Sheet 45 of 52	



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*1.05VMP*	
Size	Document Number: **15W**	Rev: 0.3
Date: Thursday, December 20, 2012	Sheet 46 of 52	



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2014/12/31

Compal Electronics, Inc.

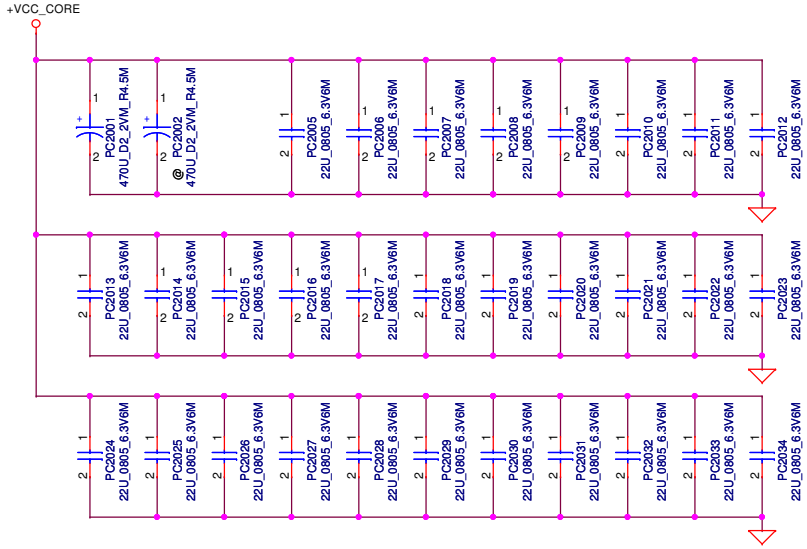
Title: ***PWR-CPU_CORE***

Size: Custom | Document Number | Rev: 0.3

Date: | Sheet 47 of 52

+VCC_CORE

2 X 470u/4m
30 X 22u/0805

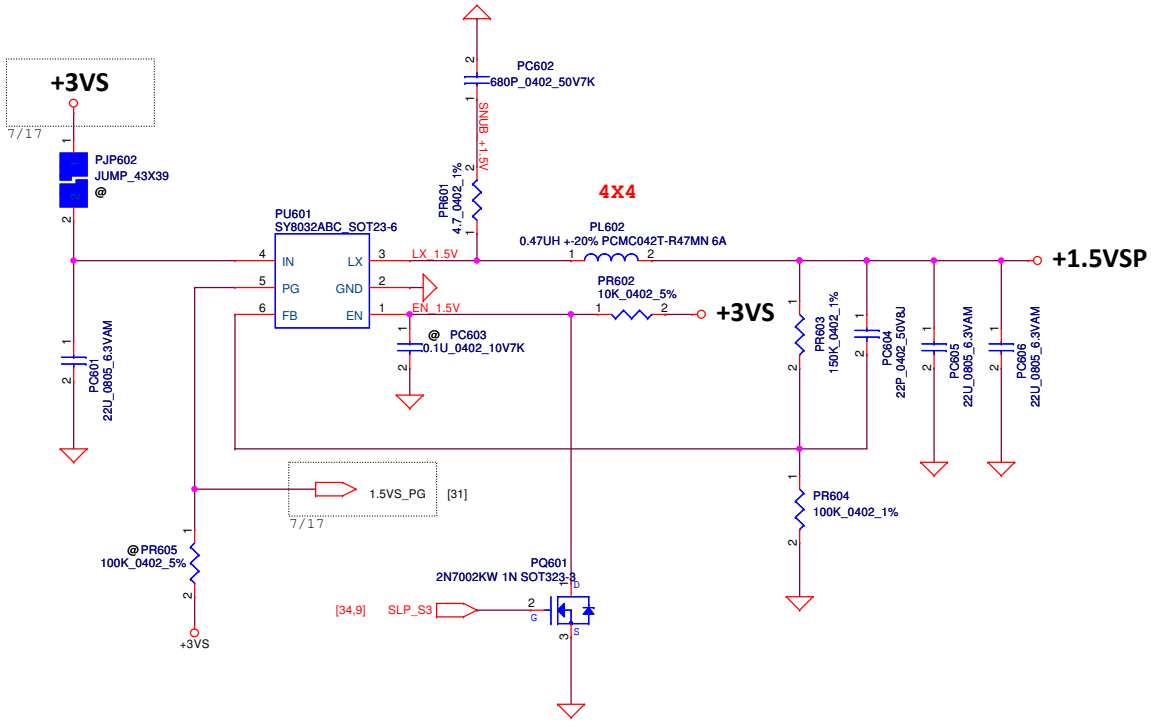


Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **LA-9371P** | Rev: 0.3

Date: Thursday, December 20, 2012 | Sheet 48 of 52

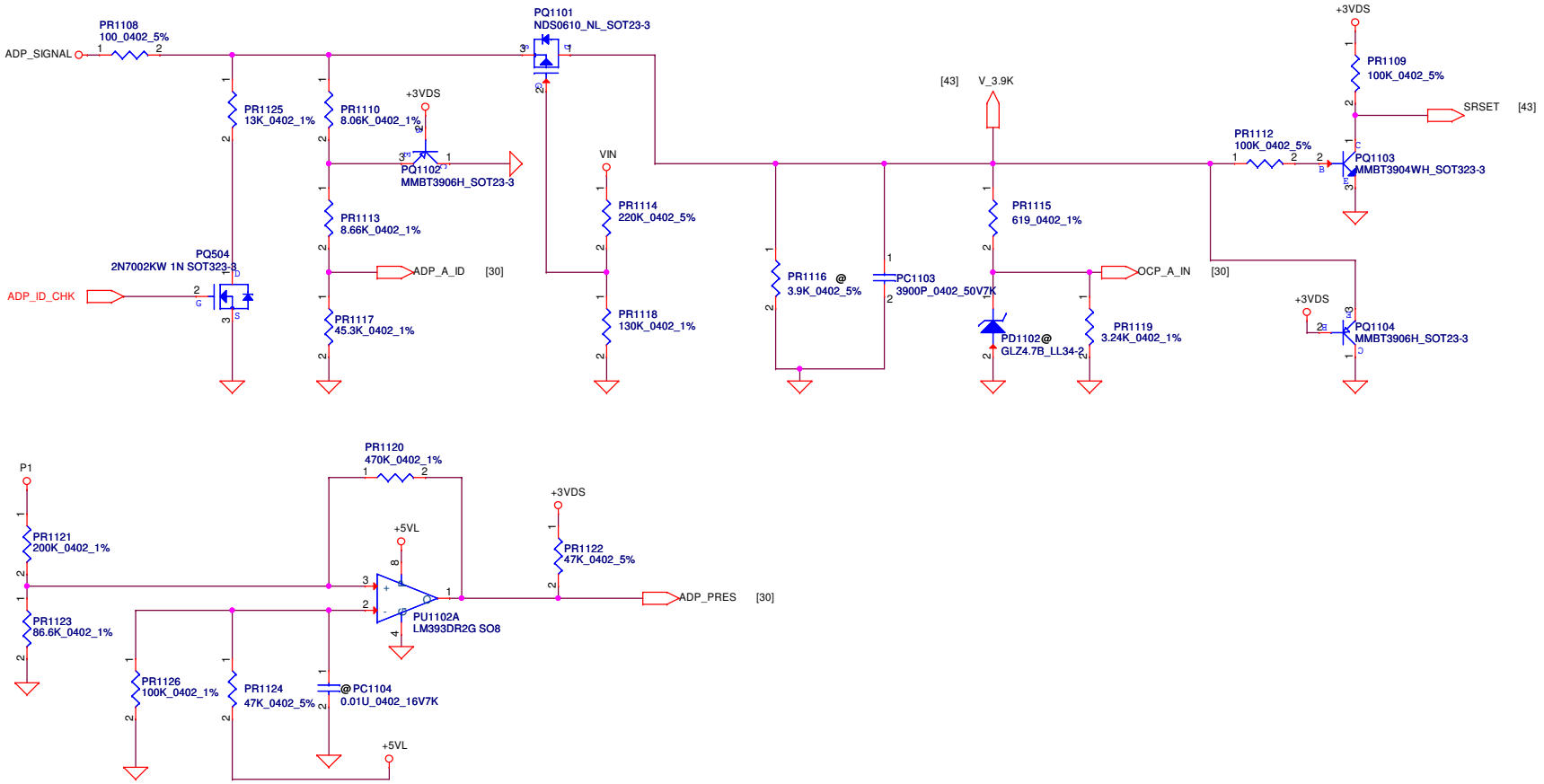


+1.5V_PCIEP
TDC=0.46A
Peak Current=0.66A

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

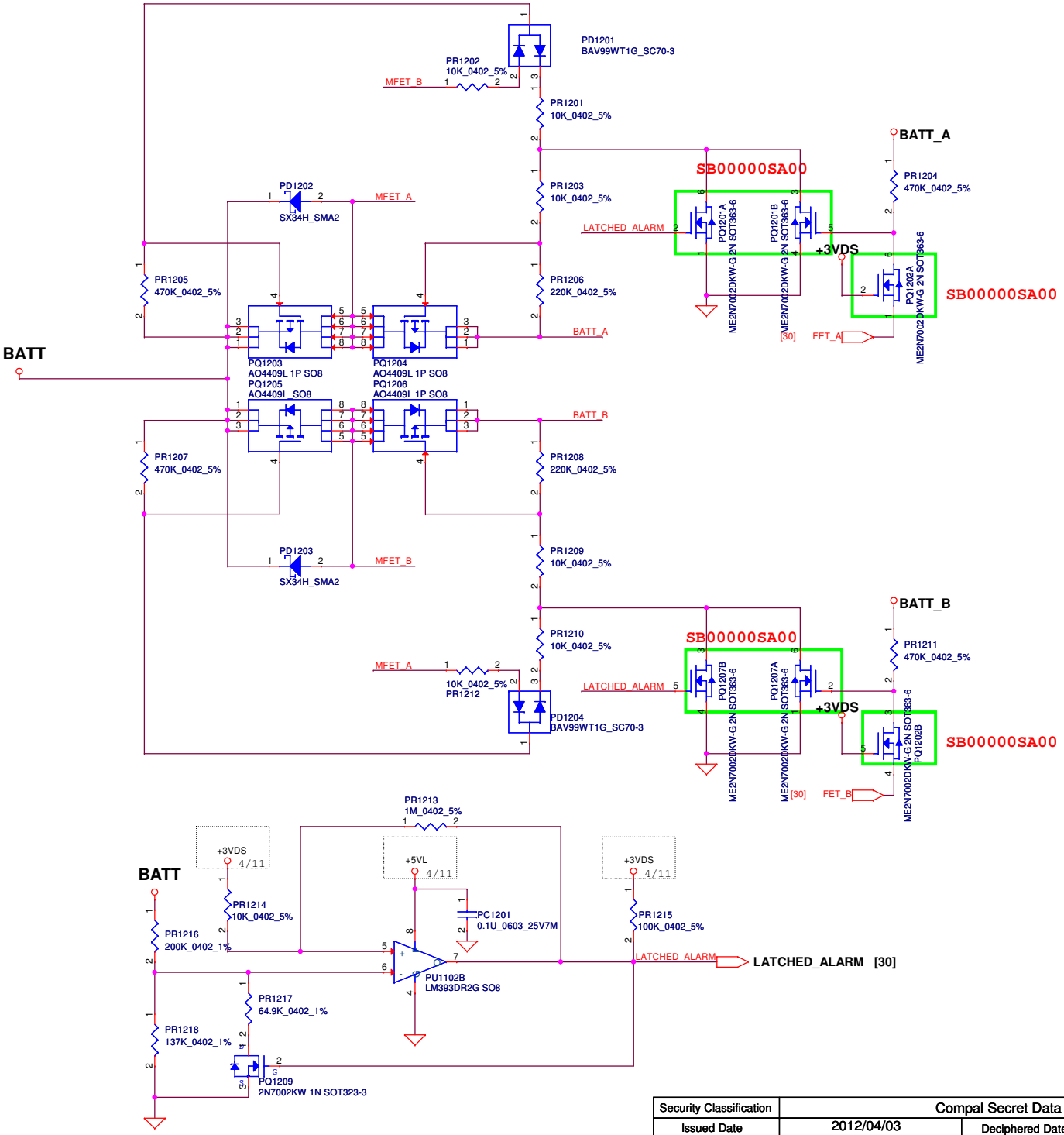
Title	*1.5VSP*	
Size	Document Number: **15W**	Rev: 0.3
Date: Thursday, December 20, 2012	Sheet 49 of 52	



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*ADP_OCP*	
Size	Document Number: **15W**	Rev: 0.3
Date: Thursday, December 20, 2012	Sheet 50 of 52	



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***Battery selector***

Size	Document Number	Rev
	15W	0.3

Date: Thursday, December 20, 2012 | Sheet 51 of 52

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
			2012/08/06				
1	43	Reserve PC130,129,131,139,133,132,134,140,136,135,137,141,143,142,144,145,146,147,148,149,151,150,152,153,138	2012/08/06			RF solution	
2	44	Reserve PC324,322,323,325326,327,328,329,330,331,332,333	2012/08/06			RF solution	
3	44	Add PC305,304,308,309	2012/08/06			RF solution	
4	45	Reserve PC419,401	2012/08/06			RF solution	
5	45	Add PC403,404,405	2012/08/06			RF solution	
6	46	Reserve PC512,513	2012/08/06			RF solution	
7	46	Add PC502,503	2012/08/06			RF solution	
8	48	Reserve PC264,267,266,269,265,268	2012/08/06			RF solution	
9	48	Add PC214,215,207,203,232,236	2012/08/06			RF solution	
10	48	Change PC233,234 from SF000001280 to SF000004M00	2012/08/09			Change the hieght to 6mm	
11	47	Change PR234 from 19.1K to 62K	2012/08/10			HP suggestion	
12	48	Change PQ203,204,211 from SB00000K300 to SB00000U200	2012/09/11			Design change	
13	48	Change PQ201,205,209 from SB00000SJ00 to SB00000W200	2012/09/13			Design change	
14	44	Change PQ301,302 from SB00000JM00 to SB00000IA00	2012/09/17			Design change	
15	44	Change PQ303 from SB00000CT00 to SB00000H700	2012/09/17			Design change	
16	44	Change PQ304 from SB00000N800 to SB00000TZ00	2012/09/17			Design change	
17	45	Change PQ401 from SB00000H800 to SB00000IA00	2012/09/17			Design change	
18	45	Change PQ402 from SB00000N800 to SB00000TZ00	2012/09/17			Design change	
19	46	Change PQ501 from SB00000H800 to SB00000IA00	2012/09/17			Design change	
20	46	Change PQ502 from SB00000N800 to SB00000H700	2012/09/17			Design change	
21	51	Reserve PR1101,1102,1103,1104,1105,1106,1107,PC1101,1102,PD1101	2012/09/25			HP suggestion	
22	45	Change PD401 from SC600000D00 to SCS00006400	2012/10/2			HP suggestion	
23	45	Change PR416 from SD034100380 to SD028470180	2012/10/2			HP suggestion	
24	43	Change PL101 from SH00000MR00 to SH00000NW00	2012/10/2			Design change	
25	23	Change PR240,243,249 from SD001470B80 to SD000010280	2012/10/2			Design change	
26	23	Reserve PL201	2012/10/2			Design change	
27	25	Reserve PL301	2012/10/2			Design change	

Compal Electronics, Inc.

Title: PWR - PIR

Size: B/25 | Document Number: LA-9241P | Rev: 0.3

Date: Thursday, December 20, 2012 | Sheet 52 of 52

VBL20 from DB0 to DB1 LA-9241P REV:0.1 -> 0.2 Modify <2012.07.04.~2012.08.07. >

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	7/6	CKT	13	-Follow HP GPIO table	-Change UH1.B17 to HDD_HALTLED
0.2	2	7/6	CKT	14,37	-Follow HP GPIO table	-Change UH1.G17 and U30.26 to PWRSV_SEL#.
0.2	3	7/6	CKT	15	-Follow HP GPIO table	-Change UH1.U4 to WLAN_TRAMSIT_OFF#
0.2	4	7/6	CKT, LAYOUT	16	-For NFC function	-Change UH1.H6 to NFC_RST#, and add QH10, RH238, RH239 for NFC SMBUS level shift
0.2	5	7/6	CKT, LAYOUT	18,23	-Follow HP GPIO table	-Change UH1.C16 to ODD_EN. Change Q25.1 netname to ODD_EN and Q25.2 netname to ODD_EN#
0.2	6	7/6	CKT, LAYOUT	18	-Follow HP GPIO table	-Change UH1.U12 and RH185.1 to NFC_INT
0.2	7	7/6	CKT, LAYOUT	19	-Add PU resistor to avoid issue.	-Add RH240 and RH241PU resistor of THERM_SCI# and WWAN_TRANSMIT_OFF#
0.2	8	7/6	CKT, LAYOUT	22	-eDP MUX	-Modify eDP connector signal source from eDP MUX.
0.2	9	7/6	CKT	23	-Power driving	-Change R1316 from 100K to 10K ohms
0.2	10	7/6	CKT, LAYOUT	25	-Change WWAN connector to NFCC	-Modify JMINI3 connector type and pin define
0.2	11	7/6	CKT, LAYOUT	26	-Move Mute circuit to S/B	-Move QA2 and R95 to S/B
0.2	12	7/6	CKT, LAYOUT	26	-Audio Combo Jack	-Delete MIC_SENSE# circuit.
0.2	13	7/6	CKT, LAYOUT	27	-Follow reference design	-Change C91 and C94 to 2.2uF as spec
0.2	14	7/6	CKT, LAYOUT	28	-No ACCELEROMETER LED	-Delete LED1
0.2	15	7/6	CKT, LAYOUT	29	-NIC yellow ban issue	-Add C350 and C373 to +1.05VM_LAN
0.2	16	7/6	CKT, LAYOUT	30	-Follow HP KBC pin define.	-Modify U17 pin define.
0.2	17	7/6	CKT, LAYOUT	34	-Avoid leakage issue	-Swap Q40 drain and source
0.2	18	7/6	CKT, LAYOUT	35	-MXM no display out issue	-Swap JMXM1 PEG TX and RX bus
0.2	19	7/6	CKT, LAYOUT	36	-Avoid eDP signal quality fail issue	-Change U42 to PS8321 which had include repeater function
0.2	20	7/6	CKT, LAYOUT	36	-To support DP1.2a	-Change U26 to PS8338 to support DP1.2a spec.
0.2	21	7/6	CKT, LAYOUT	39	-Add NFC function	-Add JNFC1 circuit.
0.2	22	7/9	CKT, LAYOUT	13	-HP request	-Delete PCH XDP circuit
0.2	23	7/9	CKT, LAYOUT	13	-HP request	-Add QH11
0.2	24	7/9	CKT, LAYOUT	16	-HP request	-Delete U39, U40, RH232
0.2	25	7/9	CKT, LAYOUT	30	-HP request	-Delete 16pin SPI ROM socket
0.2	26	7/9	CKT, LAYOUT	30	-HP request	-Add R537,Q73
0.2	27	7/9	CKT, LAYOUT	35	-HP request	-Swap MXM port A and port C for layout smoothly
0.2	28	7/9	CKT, LAYOUT	38	-Follow spec pin define	-Modify JTP1 and JTP2 pin define
0.2	29	7/9	CKT, LAYOUT	39	-Follow spec pin define	-Modify JNFC1 pin define
0.2	30	7/10	CKT, LAYOUT	6,11,12	-Following Intel CRB by HP request	-Modify JCPU1 pin AM3,F16,F13 netname. Delete RC73,RC76,C13,C75. Add QD3,RD27,RD28
0.2	31	7/10	CKT, LAYOUT	8	-HP request	-Delete RC106, RC107
0.2	32	7/10	CKT, LAYOUT	30	-HP request	-Modify R537 to 10K ohms
0.2	33	7/10	CKT, LAYOUT	34	-HP request	-Modify R363 to 4.7K ohms
0.2	34	7/11	CKT, LAYOUT	36	-Follow vendor request	-Add CC75,CC76,CC77,CC78,CC79,CC80,CC81,CC82. Modify U26 circuit
0.2	35	7/11	CKT, LAYOUT	29	-HP request	-Delete R135, R139, R151, R152, R140, R142 for layout.
0.2	36	7/12	CKT, LAYOUT	22	-HP request	-Delete C6
0.2	37	7/12	CKT, LAYOUT	23	-HP request	-Delete C54. Add R539.
0.2	38	7/12	CKT, LAYOUT	24	-HP request	-Change U3 to TC7SET00
0.2	39	7/12	CKT, LAYOUT	24	-FAN module pin define wrong.	-Modify JFAN1 pin define by follow latest spec.
0.2	40	7/12	CKT, LAYOUT	37	-Follow latest Smart card module pin define.	-Modify J3 pin define.
0.2	41	7/12	CKT, LAYOUT	38	-Follow latest KB connector pin 1 location.	-Modify JKB1 pin define.
0.2	42	7/13	CKT, LAYOUT	27,39	-Reduce layout spacing	-Move R494,R495,LA5,LA9,CA37,CA38,DA4 to sub board
0.2	43	7/13	CKT, LAYOUT	30	-Correct KBC circuit	-Change U17.68, C179.1, C188.1 to +RTCVCC. -Delete R224, R460, R220, R223, R496, R497, R498, R499, R244, R269, R236, RH220. -Change RH222.1, RH223.1, RH224.1, CH97.1, CH98.1, UH5.8 to +3VDS -Reserve R541, R542 for NFC TX/RX
0.2	44	7/13	CKT, LAYOUT	39	-Follow ME connector list	-Modify JVGA1 footprint and pin define.
0.2	45	7/13	CKT, LAYOUT	39	-Follow ME connector list	-Modify JTB1 pin define, add WL/BT_LED# signal.
0.2	46	7/16	CKT, LAYOUT	14	-ESD request	-Reserve CH107
0.2	47	7/16	CKT, LAYOUT	25	-ESD request	-Reserve C375
0.2	48	7/16	CKT, LAYOUT	27	-ESD request	-Change DA2 and DA3 P/N.
0.2	49	7/16	CKT, LAYOUT	27	-ESD request	-Delete DA1
0.2	50	7/16	CKT, LAYOUT	28	-ESD request	-Change D11 P/N
0.2	51	7/16	CKT, LAYOUT	29	-ESD request	-Change D12 and D13 P/N
0.2	52	7/16	CKT, LAYOUT	33	-ESD request	-Add D42
0.2	53	7/16	CKT, LAYOUT	37	-Follow HP latest generation smart card connector pin define.	-Modify J3 pin define.
0.2	54	7/16	CKT, LAYOUT	38	-ESD request	-Change D32 P/N.
0.2	55	7/17	CKT	11	-Correct connector name	-Change JP3 to JDIMM1
0.2	56	7/17	CKT, LAYOUT	36	-Change DP and eDP MUX to passive solution	-Modify U26 and U42 to PI3VDP12412ZHEX and releate circuit.
0.2	57	7/17	CKT, LAYOUT	17,39	-Follow HP request	-Modify JTB1 pin define. Add CH108, CH109, CH110, CH111. Connect PCIE port 1 and port 2 to JTB1.
0.2	58	7/18	CKT, LAYOUT	14	-Follow HP request	-Delete RH186, and add QH12 to invertion PCH_GPIO56 signal for CR_SX_WARN#
0.2	59	7/18	CKT, LAYOUT	17	-Follow HP request	-Change RH165.2 net name to TB_HOT_PLUG# for TBT function.
0.2	60	7/18	CKT, LAYOUT	30,32	-Follow HP request	-Change JP6.13 connection to 8051TX_STBYLED# (instead of 8051TX_STBLED#) -Change Q35.2 connection to 8051TX_STBYLED# (instead of 8051TX_STBLED#) -Add a 100K pullup resistor between signal PVT_CS# and +3VDS power rail. -Make these resistors as non-install (from Install): R219,R266,R258,R253,R216,R264 -Make R215 install -Change R436 to 1K (from 10 ohm) -Make these resistors as install (from un-install): R242,R254,R500,R277,R269,R262,R218 -Make U18 as install.

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Issued Date	2011/11/5	Deciphered Date	2010/12/01

Title	HW_PIR1		
Size C	Document Number LA-9241P		Rev 0.5
Date: Thursday, December 20, 2012	Sheet 53 of 56		

VBL20 from DB0 to DB1 LA-9241P REV:0.1 -> 0.2 Modify <2012.07.04.~2012.08.07. >

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	61	7/18	CKT, LAYOUT	31	-Follow HP request	-Modify PM_APWROK circuit
0.2	62	7/18	CKT, LAYOUT	39	-Follow HP request	-Modify JTB1 connector pin define. Add HDD_HALTLED and PWR_GD
0.2	63	7/19	CKT, LAYOUT	16,30	-Follow HP request	-Reserve RH242 and RH243. Add off page symbol of PCH_SPI_WP# and PCH_SPI_HOLD#
0.2	64	7/19	CKT	20	-Follow Intel reference schematic V1.2	-Non-install CH101
0.2	65	7/19	CKT,LAYOUT	25	-Follow HP request	-Delete C79 and C85. Change R457.1 power rail to +3VDS
0.2	66	7/19	CKT,LAYOUT	30	-Follow HP request	-Delete R254
0.2	67	7/19	CKT,LAYOUT	32	-Follow HP request	-Change R483.1 and R482.1 connection to +3VS. Change R330.1, R329.1, and R328.1 connection to GND
0.2	68	7/19	CKT,LAYOUT	36	-Follow HP request	-Delete CC70, CC71, CC75, CC76, CC77, CC78, CC79, CC80, CC81, CC82
0.2	69	7/19	CKT,LAYOUT	39	-Follow HP request	-Modify pin define JVGA1 and JCR1 pin define for better return path
0.2	70	7/19	CKT,LAYOUT	40	-Follow HP request	- Connect signal ADP_ID_CHK to pin 78 of KBC via a 0 ohm resistor (install this resistor). - Connect NFC_RX to pin 86 of KBC directly, and then move R541 (install) between ADP_ID_CHK and pin 86 of KBC. - Connect NFC_TX to pin 87 of KBC directly, and then move R542 (install) between pin 87 of KBC and signal PLT_SEL.
0.2	71	7/20	CKT,LAYOUT	14	-Follow HP request	-Add ME debug connector JME1
0.2	72	7/20	CKT,LAYOUT	16	-Follow latest ME drawing.	-Correct screw hole size.
0.2	73	7/20	CKT,LAYOUT	19,20	-Follow HP request.	-Delete CH60, CH62, CH63, CH102
0.2	74	7/20	CKT,LAYOUT	19,21,38	-Follow HP request.	-Add RA28 and Q75 for REC_MUTE_CTRL_KB signal. Modify JKB1 pin define.
0.2	75	7/20	CKT	27,38	-Follow ESD request.	-Change DA2, DA3, D32 P/N
0.2	76	7/20	CKT,LAYOUT	29,34	-Follow HP request.	-Change C110 to 22uF, Delete C231. Change Q170A lcation to Q7A
0.2	77	7/20	CKT,LAYOUT	30	-Layout smooth	-Modify RP1 pin define.
0.2	78	7/20	CKT,LAYOUT	30	-Follow HP request.	-Add D44 and D45
0.2	79	7/20	CKT,LAYOUT	31	-Follow HP request.	-Modify PWR_GD circuit.
0.2	80	7/20	CKT	37	-Vendor's suggestion	-Change C258 and C255 to 1uF. Non install RH225.
0.2	81	7/20	CKT	38	-Modify for 2 DIMM and 4 DIMM SKU.	-Reserve SIO_GPIO44 PD R554, and modify R328, R329, R330 value to 4.7K. Modify R482, R483 value to 10K
0.2	82	7/23	CKT,LAYOUT	14	-Schematic wrong.	-Connection RH55.2 to power rail +RTCVCC
0.2	83	7/23	CKT,LAYOUT	14	-Follow HP request.	-Move QH12 to sub board. Add CR_SX_WARN# PU 10K ohms RH244
0.2	84	7/23	CKT,LAYOUT	15,17,18	-No connection to other page.	-Delete FN14, FN15, USB_OC0#_R, USB_OC1#_R, USB_OC2#, USB_OC3#, USB_OC4#_R, PCH_GPIO24, FN_CLK2, PCH_GPIO37 off page symbol.
0.2	85	7/23	CKT,LAYOUT	16	-Follow latest ME drawing.	-Modify screw hole size.
0.2	86	7/23	CKT,LAYOUT	17	-Correct net name	-Change RH171.1 connection to ODD_EN
0.2	87	7/23	CKT,LAYOUT	18,29,30,34	-Follow VBK10	-Non install RH184 and RH185. Add C389, C390, C391, C392. Change C121 to 1000pF. Change C322 to 100pF. Delete Q37, R366, R361.
0.2	88	7/23	CKT,LAYOUT	22,30	-Follow RF request.	-Reserve C393, C394, CH112
0.2	89	7/23	CKT,LAYOUT	26	-MIC_SENSE circuit had been removed.	-Delete RA7.
0.2	90	7/23	CKT,LAYOUT	27	-Reduce layout spacing	-Combine QA2B with QA1A.
0.2	91	7/23	CKT,LAYOUT	31	-Follow HP request.	-Change R286 to 10K
0.2	92	7/23	CKT,LAYOUT	36	-Follow HP request.	-Combine Q63 and Q72 to Dual channel Q76. Delete R516, R545, CC84, C371.
0.2	93	7/23	CKT,LAYOUT	36	-Modify netname to more clear.	-Change SEL to SEL_eDP_MUX. Change SEL_DP to SEL_DP_MUX
0.2	94	7/23	CKT,LAYOUT	17	-Layout smooth	-Modify RPH1 and RPH2 pin define
0.2	95	7/24	CKT,LAYOUT	25	-Follow latest NGFF pin define.	-Modify JMINI3 pin define.
0.2	96	7/24	CKT,LAYOUT	28	-Follow latest FP spec.	-Modify JFP1 pin define.
0.2	97	7/24	CKT,LAYOUT	30,38	-Follow EMI request	-Add C420, C421, C422, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, R555 and C419. Change R437.2 netname to PCH_SPI_CLK_EC.
0.2	98	7/24	CKT,LAYOUT	39	-Follow HP request	-Modify JUB1 pin define.
0.2	99	7/25	CKT,LAYOUT	5,9,20	-Follow HP request	-Delete RC24, RC96. Change UH1 pin AJ12 and AJ14 connection to +1.05VS
0.2	100	7/25	CKT,LAYOUT	30	-Follow HP request	-Change U18 to socket and add &UH2 for KBC ROM
0.2	101	7/25	CKT,LAYOUT	30	-Follow HP request	-Connect JP6.13, U17.115, and R255.1 to TX_STBY_LED. Add R559, R560, and Q77
0.2	102	7/25	CKT,LAYOUT	36	-Reduce layout spacing	-Combine Q56 and Q57 to dual channel Q79
0.2	103	7/25	CKT,LAYOUT	25	-Follow latest NGFF spec	-Modify JMINI3 and JSIM1 pin define.
0.2	104	7/26	CKT,LAYOUT	16,30	-Follow HP request	-Install RH242, RH244. Add R561, R562. Noninstall R541, R542
0.2	105	7/26	CKT,LAYOUT	28	-Follow RFQ spec	-Change U11 to SLB9656
0.2	106	7/27	CKT,LAYOUT	36	-Follow HP request	-Add R563, R564
0.2	107	7/30	CKT,LAYOUT	5	-Follow Intel reference schematic	-Non install QC1
0.2	108	7/30	CKT,LAYOUT	16	-Follow RF request	-PCH_SPI_CLK reserve CH113 to GND
0.2	109	7/30	CKT,LAYOUT	22,39	-Follow HP request	-Change R10.1 to +5VDS and Q20.3 to +3VDS for layout easy. Modify JVGA1 and JCR1 pin define.
0.2	110	7/30	CKT,LAYOUT	23	-Follow latest connector list	-Modify JHDD1, JODD1 and JCR1 footprint.
0.2	111	7/30	CKT,LAYOUT	39	-Correct JNFC1 pin define	-Modify JNFC1 pin define.
0.2	112	7/31	CKT,LAYOUT	25,39	-Follow HP request	-Modify Q4A circuit. Change JTB1.95 connection to +3VDS.
0.2	113	7/31	CKT	25	-Wireless LED fail issue.	-Install Q29 and Q31
0.2	114	7/31	CKT,LAYOUT	26	-No LOGO KBL function	-Delete Q21,Q22,R454,R14. Delete JEDP1.35 signal
0.2	115	7/31	CKT,LAYOUT	14	-Correct netname	-Change RH62.2 netname to PWRSV_SEL#
0.2	116	8/01	CKT,LAYOUT	23,33,39	-HP request	-Swap SATA bus port 2 and port 5. JCR1.35 connection to PCH_PCIE_WAKE#
0.2	117	8/01	CKT,LAYOUT	18,23,25	-HP request	-Uninstall Q68, R459. Change PCH.AT3 and RH198.2 netname to Sec_HDD_DET. Change PCH.AP1 and RH180.2 to mSATA_DET#. Delete Q48. Add R565.
0.2	118	8/01	CKT,LAYOUT	24	-PWR request	-Change R492.2 connection to KBC_PWR_ON
0.2	119	8/01	CKT	30	-Follow RFQ spec	-Change KBC symbol to SMC1322
0.2	120	8/03	CKT,LAYOUT	6,11,13,18	-HP request	-Add CC84, CC85, CC86. Change RD6 to 33ohms. RH33.1 connection to GND. Delete RH201, RH202. Q4.2 connection to BT_ON
0.2	121	8/03	CKT,LAYOUT	22	-Layout smooth	-Swap L3 pin define for layout smooth
0.2	122	8/03	LAYOUT	23	-Follow ME connector list	-Modify JODD1, JMINI3 footprint
0.2	123	8/03	CKT,LAYOUT	25,30,39	-HP request	-Q4.2 connection to BT_ON. Change R437 to 33 ohms. Change R540 to 4.7K. Change JVGA1 pin 39 and 40 connection to +3VDS
0.2	124	8/03	CKT,LAYOUT	30	-RF request	-Add CH114
0.2	125	8/06	CKT,LAYOUT	9,15	-HP request	-Reserve CC87. Change JCPU1 pin AM43 and pin AL44 ball name

Compal Electronics, Inc.			
Title: HW_PIR2			
Size: C	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 54 of 56		

VBL20 from DB0 to DB1 LA-9241P REV:0.1 -> 0.2 Modify <2012.07.04.~2012.08.14. >

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	126	8/07	CKT, LAYOUT	7,16,25,29	-Follow HP request	-Change RC78 to 10Kohms. Install RH148 and change to 2.2Kohms. Add R567, R568 and R569.
0.2	127	8/07	CKT, LAYOUT	30	-Correct netname	-Change TX_STBY_LED net name to TX_STBY_LED#
0.2	128	8/07	CKT, LAYOUT	11,12,13, 30,38,39	-Follow latest ME connector list	-Modify JDIMM1, JDIMM2, JBATT1, JKB1, JCR1, JNFC1, JP6 connector footprint
0.2	129	8/08	CKT, LAYOUT	22,35	-RF request	-Reserve C449, C450, C451
0.2	130	8/08	CKT, LAYOUT	39	-Follow latest ME connector list	-Modify JCR1 and JNFC1 pin define.
0.2	131	8/09	CKT	39	-Follow latest ME connector list	-Modify JMXM1 footprint
0.2	132	8/10	CKT, LAYOUT	5,14,30	-Follow HP request	-Add RC106 and change UC1.1 connection to VR_ON. Change UH7.5 and UH3.5 connection to +3V_PCH power rail. Change RH235 to 0ohms. Add RH245 and connection to VCC1_PWRGD. Change R277.1 and R253.2 connection to VR_ON
0.2	133	8/10	CKT	39	-Add +3VDS power rail for USB repeater	-Change JCR1.21 connection to +3VDS
0.2	134	8/10	CKT	38	-Follow TP module pin define	-Modify JTP1 pin define.
0.2	135	8/10	CKT, LAYOUT	34	-RF request	-Reserve C452, C453, C454, C455, C456, C457, C458
0.2	136	8/14	CKT		-Material EOL	-Change Q59, Q70, Q55, Q58, Q68, Q75, Q39, Q61, Q51, Q52, Q53 to SB000009Q80 (S TR 2N7002KW 1N SOT323-3)
0.2	137	8/14	CKT	24,25,30,32	-Material EOL	-Change D4, D8, D10, D21, D27 to SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)

VBL20 from DB1 to DB2 LA-9241P REV:0.2 -> 0.3 Modify <2012.09.03.~ 2012.09.28 >

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	1	9/03	CKT	26	-Chang UA1 to HP P/N	-Change UA1 P/N to 92HD91B2X5NLGXWCX8
0.3	2	9/03	CKT	30,31	-Follow HP request	-Install R451, R452. Noninstall R561, R562, R284. Change R282 to 10K ohms. Change R289 to 11.5k ohms
0.3	3	9/07	CKT	30,36	-No used	-Delete TX_STBY_LED#, VGA_RED, VGA_GRN, VGA_BLU, VGA_DDCCLK, VGA_DDCDATA, CRT_HSYNC, and CRT_VSYNC off page symbol
0.3	4	9/07	CKT, LAYOUT	36,39,40	-Follow latest ME drawing	-Add VGA circuit and connector. Remove JVGA1 BTB connector. Add JFUN1 connector. Add USB3.0 repeater and connector
0.3	5	9/10	CKT, LAYOUT	25	-Follow HP request	-Add WWAN_FULL_PWR and WWAN_RSVD2 PU R599 and R600 to +3V_WWAN. Delete T126 and T128
0.3	6	9/10	CKT, LAYOUT	30	-Follow HP request	-Delete R219, R258, R500, R262, R264, R266, R216, R241, R242, R253, R549, R271. Change U17 pin69 to KBC_XTA2, pin 71 to KBC_XTAL1. Add C487, C488, Y4 Connect EC_MUTE# to KBC.91. MAIN_BAT_DET# to KBC.92. pin 70 of KBC to GND. ADP_ID_CHK signal to KBC.78. A\DP_EN signal to KBC.63
0.3	7	9/11	CKT, LAYOUT	5,9,10,14, 15,17,20, 31,32, 33	-Follow HP request	-Delete RC102 and RC103. Connect CPU.AL35 pin to VCCSENSE. Connect CPU.AK35 pin to VSSSENSE. Delete RH165 and connect PCH.M1 to TB_HOT_PLUG# directly. Connect RPH1.3 to TB_HOT_PLUG# directly. Delete RH226 and connect pin AD12 of PCH to +3V_PCH power rail. Delete RC106 and connect UC1.1 to VR_ON. Noninstall RC36,RC38,RC40,RC43,RC45,RC47. Delete RC66. Connect CPU.AT26 pin to CPU_PLTRST#. Delete RC30. Connect CPU.AL34 pin to H_CPUPWRGD. Change RC55.1 connection to H_CPUPWRGD. Delete RC27. Connect CPU.AM35 pin to PCH_THERMTRIP#_R. Delete RC93 and connect SLP_S3# to QC5.5. Delete R351. Connect EN_P1V5 to JDOCK1.140. Change C299 to 0.01uF. Delete R336 and connect C299.1 to ON/OFFBTN_KBC# . Connect ON/OFFBTN_KBC# to JDOCK1.49. Delete R287. Connect joint point of R286.1 and U18.1 to VR_ON. Add R601 4.7K PU to +3VS on signal SIO_GPIO42. Noninstall R601. Delete RH92, RH93, RH221, RH94, RH95, RH107, RH103, RH203, RH114, RH116, RH205, RH122, RH124, RH126, RH127, RH128, RH130
0.3	8	9/12	CKT, LAYOUT	30	-Follow HP request	-Delete R543, R561, R562. Delete signal ADP_ID_CHK connection to KBC.86 pin. Delete R249 and connect signal OCP_PWM_OUT to KBC.59 pin. Delete R251 and connect signal PM_PWROK to KBC.60 pin. Delete R256 and connect signal EN_P1V5 to KBC.38 pin. Delete R277 and connect signal VR_ON to KBC.72. Change RP1 and RP2 to 100K.
0.3	9	9/12	CKT, LAYOUT	38,	-ME move LID SW from Power board to Function baord.	-Modify JPWR1 and JFUNC1 connector pin defein.
0.3	10	9/12	CKT, LAYOUT	37	-ME rotate Smart connector 90 degree.	-Modify J3 pin define.
0.3	11	9/13	CKT, LAYOUT	16	-Follow latest ME drawing	-Delete H4, H32, H34, H41, JP2. Add H42, H43, H44, H45, H46. Modify JEDP1, JSIM1, JFP1, JVGA2, J3, JKB1, JTP1. JFUN1 pin define and footprint.
0.3	12	9/14	CKT, LAYOUT	14,31	-Follow HP request	-Delete UH7, RH235. Move RH236, CH106 to page 31. Modify POWER OK circuit
0.3	13	9/14	CKT, LAYOUT	22,30,38,39,40	-Follow ME and DFX request	-Modify JEDP1, UH5, JTB1, JUSB1 and JKB1 pin define and footprint.
0.3	14	9/17	CKT, LAYOUT	40	-Layout request	-Swap L35, L36, L37 for layout smoothly.
0.3	15	9/17	CKT, LAYOUT	38	-Follow ME connector list	-Change JPWR1 footprint and pin define.
0.3	16	9/17	CKT, LAYOUT	38	-Follow Keyboard spec	-Modify JKB1 pin define.
0.3	17	9/18	CKT, LAYOUT	28	-Follow ME drawing	-Modify JFP1 pin define.
0.3	18	9/19	CKT, LAYOUT	13,39	-Follow HP request	-Add a 0ohm resistor between JCR1.5 and signal PCH_PCIE_WAKE#. Then make this resistor open. Change QH11 to P MOS. Change RH30 to 2.2K ohms
0.3	19	9/19	CKT, LAYOUT	34	-Layout smooth	-Delete J2
0.3	20	9/20	CKT, LAYOUT	14,26,30,37	-Follow HP request	-Change RH74 to 100K. Change RH147.1 power rail to +3VS. Delete RA13, CA20. Change R227 to 3K. Delete R393, CC67, and connector U30.23 to PLT_RST#.
0.3	21	9/20	CKT, LAYOUT	22	-Correct circuit short issue	-Modify JEDP1 connector circuit. Add one more +3VS power pin for power consumption
0.3	22	9/20	CKT, LAYOUT	22,26	-Change to common part.	-Change D3 and DH1 to RB751V-40_SOD323-2
0.3	23	9/21	CKT, LAYOUT	8,13,30,39	-Follow HP request	-Reserve CFG9 PD resistance RC106. Non-install RH39, RH40, RH41, RH44, RH48, RH47, RH46. Change R436 to 100K and connection R436.2 to GND. Delete R557, Non-install R358, C374
0.3	24	9/21	CKT, LAYOUT	36	-Netname issue.	-Change L29.2 netname to DAC_RED. L30.2 netname to DAC_GRN. L31.2 netname to DAC_BLU
0.3	25	9/23	CKT, LAYOUT	5,30,31,47	-Follow HP request	-Change netname VR_ON to PWR_GD, change netname PWR_GOOD_3 to VGATE
0.3	26	9/24	CKT, LAYOUT	20,30	-Follow HP request	-Non install D21. Delete RH213, RH216, and change netname
0.3	27	9/24	CKT, LAYOUT	40	-No need another DC/DC circuit to provide +3VDS_P to U44.	-Delete Q79, Q80, C475, C477, C478, R588, R587. Change +3VDS_P power rail to +3VS.
0.3	28	9/25	CKT, LAYOUT	22	-Change +3VS, +5VS and +LCDVDD power rail soultion	-Delete R9, R10, R11, Q12, Q20, C1, C7, C8, U24, C226, C221, C222, U25, C218, C223, C219, C227, R354, R356, R357, Q9. Add U47, C497, C498, C499, U45, R603, C489, C490, C491, C492, U46, R604, C493, C494, C495, C496, Uninstall R370, R373, Q43, Q44, R490
0.3	29	9/25	CKT, LAYOUT	30	-Follow HP request	-Install R237, R235, R234, R233, R231
0.3	30	9/25	CKT, LAYOUT	31	-Reserve for EC CLK issue	-Reserve R605 and connect R605.1 to SUSCLK_KBC
0.3	31	9/26	CKT, LAYOUT	5,22,34,40	-Follow HP request	-Change JXDP1.47 connection to PM_PWROK via a 0ohm resistor. Add a C502 (10uF cap) for +3VS decoupling. Change C489 and C492 value to 10uF or 4.7uF. Change C494 and C496 to 10uF or 4.7uF. Change C499 value to 4.7uF and make R480 as install. Change C493 and C490 to 0.01uF
0.3	32	9/26	CKT, LAYOUT	34	-Correct Netname	-Change R375.1 connection netname to SLP_S3#
0.3	33	9/26	CKT, LAYOUT	38,39	-Follow ME request	-Modify JP9 and JFUN1 pin define.
0.3	34	9/26	CKT, LAYOUT	34	-Follow HP request.	-Modify +1.05VS power circuit.
0.3	35	9/27	CKT, LAYOUT	33,35,38	-Follow HP request.	-Delete R339, R340, R341, R342. Add R606, R607, R608 PU to +3VS. Change R408 to 200K ohms. Uninstall C295.
0.3	36	9/27	CKT, LAYOUT	29	-Material shortage issue	-Change Y2 to smaller (32x25 mm) package.
0.3	37	9/28	CKT, LAYOUT	34	-Follow HP request.	-Add C503
0.3	38	10/09	ckT	16	-Follow HP request.	-Change RH152, RH153 to 499ohms.

Compal Electronics, Inc.			
Title: HW_PIR3			
Size: C	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 55 of 56		

VBL20 from DB1R to SI1 LA-9241P REV:0.3 -> 0.4 Modify <2012.10.11.~ 2012.11.09>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.4	1	10/11	CKT, LAYOUT	26,27	-Follow IDT request	-Change RA14 to 0 ohm. Change C91, C94 to 150u. Change R97, R98, R102, R104 to 1%. Non-install R106, R107. Change C95 to 0.47u X5R. Change QA1.4, R110.2, Q6.1, R111.2, Q6.4 to AGND.
0.4	2	10/11	CKT,	33	-Follow ESD request.	-Non-install D42. Install D32.
0.4	3	10/11	CKT, LAYOUT	35	-Follow HP request	-Re-arrange MXM DP port. Port A for Thunder Bolt. Port B for Dock. Port C for EDP. Port D for SWITCH
0.4	4	10/12	CKT, LAYOUT	5,14,30,34	-Follow HP request	-Reserve RC108, UH6, CH116, R610. Change U17.85 and R276.1 connection netname to RSMRST#_EC. Change R455 to 47K. Add Q18A, C504, R609. Modify +3V_PCH power circuit
0.4	5	10/16	CKT, LAYOUT	9,14,25,29, 30,34,39	-Follow HP request	-Install R567, D21. Add R612, R616, Q80, R614, Q79. Delete R602, C504, R609, R456, Q67B, R218, R239, R240, R540, Q74, R247, C322, C186, R230, R64. Change R568.1, R569.1 and R245.1 connection to KBC_WAKE#. Remove current VCC1_PWRGD connection to JP6.16. Then add a 4.7 K resistor between JP6.16 and new signal VCC1_PWRGD_SUS#. Change R215.2 to GND. Change R227 to 3.3K. Add a R615 PD for U7.102. Change U7.102 connection to PLT_DET. Change R248 to 200k ohms. Change R248.1, U17.77 connection to VCC1_PWRGD_SUS#. Change R243.1 and U7.125 connection to CHRG_RST. Change R243 to 100K. Change R243.2 connection to GND. change R436.2 connection to +3VDS. Change JTB1.91, U17.41 and R436.1 connection to iSCT_LED#. Change D21.2 connection to PM_APWROK. Modify +3V_PCH power circuit. Change JCR1.5 connection to +5VDS.
0.4	6	10/17	CKT, LAYOUT	14,30	-Follow HP request	-Change R614.1 connection to +3V_PCH. Correct R227 to 10K.
0.4	7	10/18	CKT, LAYOUT	5,9,14,16 20,24,25 30,34,35	-Follow HP request	-Change R615 to 470K, R610 to 470 ohm, R614 to 10K ohms, R612, R137, R606, R607 and R608 to 4.7K ohms, RC108 to 10K ohms . Delete Q67A, QC1, RC12, Q80, R461, Q2, RC90. Install RH209, R492, RC108, R613, CH116 and UH6. Uninstall QC3, RH148, RH67, RH208. Change R492.2 connection to PCH_THERMTRIP#_R Connection R614.1 to PM_RSMRST#. Modify +1.35VS power circuit
0.4	8	10/23	CKT, LAYOUT	14,20,30 34,39	-Follow HP request	-Delete R612. Reserve R616 between KBC. 124 pin and signal SIO_SLP_SUS#. Uninstall RH209, Q79, R614, R613, CH116 and UH6. Install RH67, RH208. Change PCH.AL6, JTB1.91 and RH244.2 connection to TBT_RR_GPIO#. Add Q80 for iSCT_LED# circuit
0.4	9	10/24	CKT, LAYOUT	18,25,28	-Follow HP request	-Add R618, R619, R620, R621. Delete R567, and connect JMINI3.15 to WLAN_WAKE# directly. Change ACCEL_INT# connection to U9.11. Change RH176.2 connection to GND and make RH176 install. Change RH185 as install
0.4	10	10/25	CKT, LAYOUT	14,18,25 29,34,35	-Follow HP request	-Add R247, Q63. Change RH70 to 200k ohms. Add LANWAKE# PU RH248 to +3VDS. Delete R618, R89. Change R455 to 200k. Add PD R622. Change Q61 and Q62 to dual channel 7002
0.4	11	10/25	CKT, LAYOUT	30	-Solve KBC external crystal can not work issue.	-Reserve R624 and connection to SUSCLK_KBC
0.4	12	10/26	CKT, LAYOUT	13,14,15 29,32,36	-Follow Compal HW request	-Delete RH56, RH57, RH59, RH60, RH66, RH69, RH71, RH98, RH99, RH100, RH141, RH234, RH139, RH108, RH110, RH111, RH112, R160, R161, R162, R163, R320, R477, R478, R464, R465, R466, R467, R472, R473, R474, R475, R468, R469, R470, R471, R479, R484, R485, R486, R318, R319, R321, R322, R570, R571, R572. Add RP7, RP8, RP9, RP10, RP11, RP12, RP13, RP14, RP15, RP16, RP17, RP18, RP19.
0.4	13	10/26	CKT, LAYOUT	13,14,15 29,32,36	-For layout smoothly.	-Rearrange RP11, RP8, RP17, RP13, RP14, RP15, RP16, RP12, RP10, RP7 pin assignment for layout smoothly.
0.4	14	10/26	CKT, LAYOUT	38	-Move LID switch to PWR board by ME reqesut.	-Change JPWR1 to 6 pin, and modify the JPWR1 pin define.
0.4	15	10/26	CKT, LAYOUT	13,14,17 18,23,29 30,32,34 38,	-Follow HP request.	-Delete R153, R481, R565. Swap QH11A.2 and QH11B.5 connection. Change RH75.2 and PCH.K7 connect to BATLOW#. Change PCH.U7 connect to BT_OFF. Change PCH.P3 and RPH2.4 connect to WWAN_DET#_PCH. Delete A20GATE and VCC1_PWRGD_SUS# off page symbol. Change RH180.2 and UH1.AP1 connect to PCH_GPIO_35. Change RH198.1 and UH1.AT3 connect to PCH_GPIO_36. Change R376 to 10k. Change R376.1 connect to +3VDS. Connect Q34.3 to LED_LINK_LAN_DOCK# with R625, and delete LED_LINK_LAN_DOCK# connection to Q34.1. Delete R157 and connect Q34.1 and signal LED_LINK_LAN#_R. Connect U22.26 pin to signal mSATA_DET#. Change R455.2 connection to B+. Change Q36 to AO3413.
0.4	16	10/29	CKT, LAYOUT	18,35	-Follow HP request.	-Change RH179 to 100ohms. Delete R137, Q82.B. Add D52
0.4	17	10/31	CKT, LAYOUT	18,36	-Follow ME request.	-Change JODD1, JVGA2, JKB1 footprint
0.4	18	10/31	CKT, LAYOUT	18,37	-Follow HP request.	-Change R291.1 connection to +5VL. Change R291 to 105K_1%
0.4	19	11/01	CKT, LAYOUT	31	-Follow HP request.	-Change R304.1 connection to +5VL. Change R304 to 88.7k +-1%. Uninstall R306.
0.4	20	11/01	CKT, LAYOUT	13,15,37	-Material shortage issue	-Change Y3, YH1, YH2 to small package
0.4	21	11/01	CKT, LAYOUT	22,30,37,38	-Follow HW request	-Uninstall Y4, C487, C488. Delete C23, C80, C82, C111. Change U30 to AU9560-GBS-GR. Add R626
0.4	22	11/02	CKT, LAYOUT	29	-Follow HP request.	-Reserve C504. Add C505
0.4	23	11/05	CKT, LAYOUT	27	-Audio Jack change to normal open type	-Delete R174, QA1B. HP_SENSE# connection to R167.1
0.4	24	11/05	CKT, LAYOUT	38	-Follow ME request	-Modify JKB1 pin define to follow ME request.
0.4	25	11/05	CKT, LAYOUT	39	-Smart Card Reader AU9560-GBS-GR no need external crystal	-Uninstall Y3, CV33, CV34
0.4	26	11/06	CKT, LAYOUT	9,14,22, 25	-Follow HP request	-Change QC5A.2 and QC5B.5 connection to SLP_S3. Change PCH.D2 pin connection to DDR3_SET. Delete Q68, R459. Change R458 to 0ohm. Change JMINI3.13 connection to signal WWAN_DET#_PCH. Change JMINI3.65 connection to GND. Change C498 to 4700pF
0.4	27	11/06	CKT, LAYOUT	12	-Follow RF request	-Add C506, C507, C508, C509, C510, C511
0.4	28	11/07	CKT, LAYOUT	5	-Follow ESD request	-Delete RC36, RC38, RC40, RC43, RC45, RC47 by ESD request. Add T144, T145, T146, T147, T148, T149
0.4	29	11/07	CKT, LAYOUT	23,32	-Follow RF request	-Change C48 and C58 to 68pF. Change R332 to 33 ohms, C205 to 82pF and install R332 and C205
0.4	30	11/08	CKT, LAYOUT	23,33	-Follow HP request	-Delete D52. Add Q83, R627
0.4	31	11/09	CKT	16,34,35	-Follow HP request	-Change RH152 and RH153 value to 2.2K. Change C491 and C495 to 4700pF. Change R627 to 4.7K.

VBL20 from SI1 to SI2 LA-9241P REV:0.4 -> 0.5 Modify <2012.12.12.~ >

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.5	1	12/12	CKT, LAYOUT	9,14,28,30 31	-Follow HP request	-Uninstall QC4, RC92, CC39, RC89, QC5 and RC88. Add J4, Q84, Q85. Delete Q79, R615, UH6, R613, R617, R227 , CH116, R605. Change RH222, RH223, RH224, R615, R248 to 100K. Remove R611. Connect JP6.16 to VCC1_PWRGD_SUS#. Install R624. Change CH115 to 0.22uF
0.5	2	12/12	CKT, LAYOUT	35	-Material shortage issue.	-Change U34, U35, U36 to small package
0.5	3	12/13	CKT	9,28	-Follow HP request	-Install RC88. Change JFP1.11 netname to FPR_OFF_C
0.5	4	12/20	CKT	35,36	-Solve CRT switch issue	-Uninstall R91,R92,R93. Change RP19 to150 ohms

Compal Electronics, Inc.			
Title: HW_PIR3			
Size: C	Document Number: LA-9241P		Rev: 0.5
Date: Thursday, December 20, 2012	Sheet 56 of 56		