

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document

Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH

Nvidia N13P GS/GL

2012-02-03b

REV : 0 . 3

MB PCB

Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B

ZZZ2 1G@



X78344BOL01

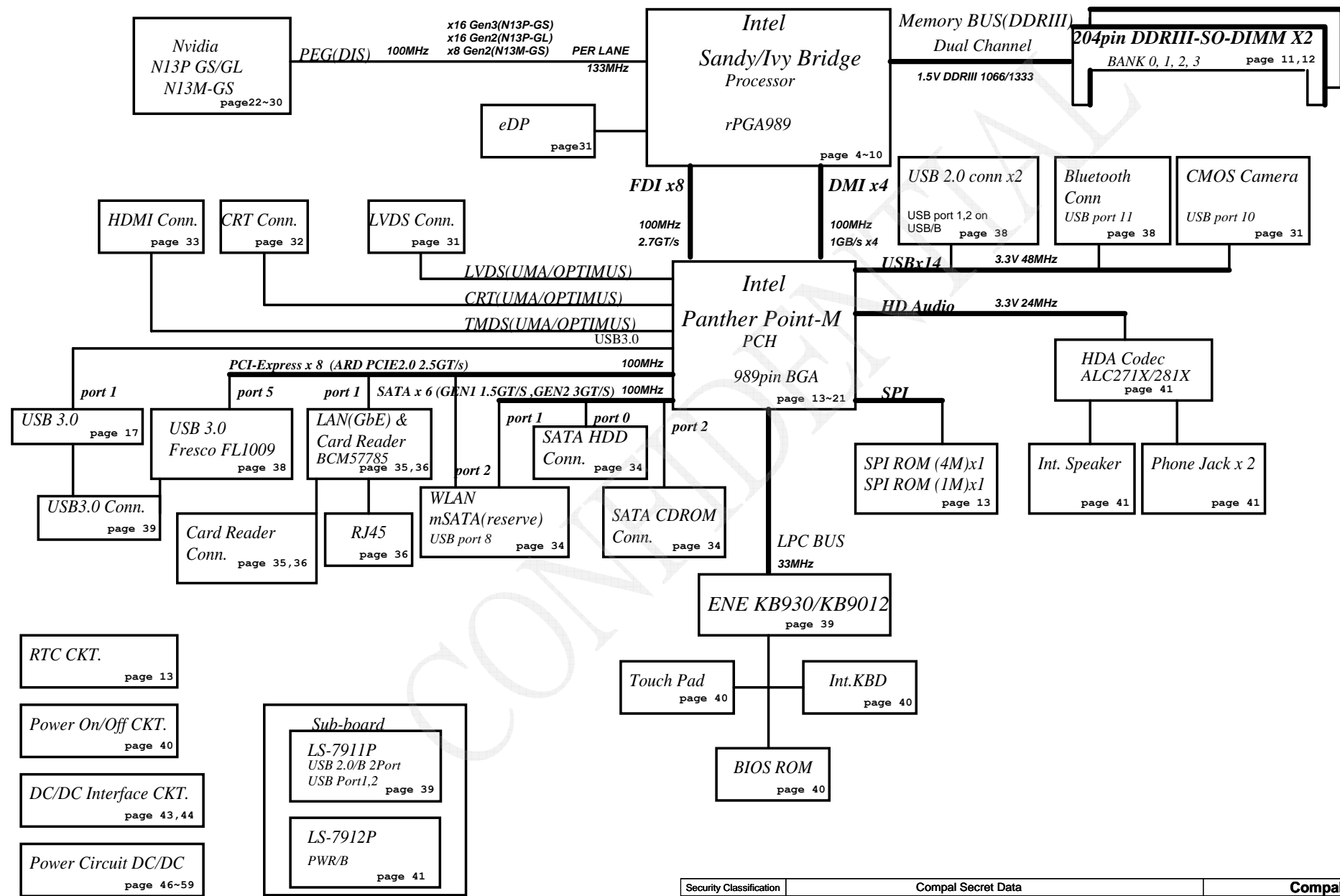
ZZZ3 2G@



X78344BOL02

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

4319IDBOL01SMT MB A7912 Q5WV1 HM77 QC UMA 3
4319IDBOL02SMT MB A7912 Q5WV1 HM77 QC 13PGL1G 3
4319IDBOL03SMT MB A7912 Q5WV1 HM77 QC 13PGL2G 3
4319IDBOL04SMT MB A7912 Q5WV1 HM77 QC 13PGS1G 3
4319IDBOL05SMT MB A7912 Q5WV1 HM77 QC 13PGS2G 3
4319IDBOL06SMT MB A7912 Q5WV1 HM77 DC UMA 2
4319IDBOL07SMT MB A7912 Q5WV1 HM77 DC UMA 3
4319IDBOL08SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 2
4319IDBOL09SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 3
4319IDBOL10SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 2
4319IDBOL11SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 3
4319IDBOL12SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 2
4319IDBOL13SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 3
4319IDBOL14SMT MB A7912 Q5WV1 HM77 DC 13PGS2G 3

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

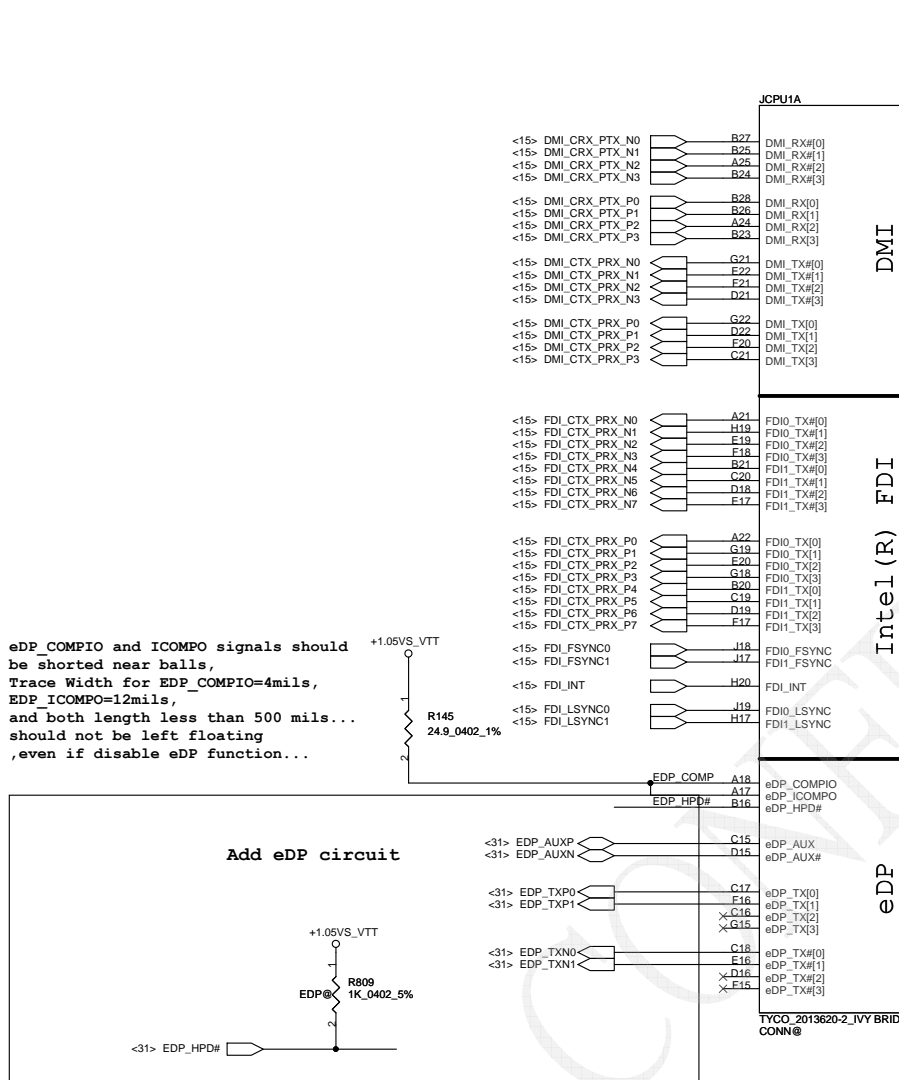
BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB3@
Internal USB 2.0	PUSB@
USB 2.0 flag	PUSB2@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@
N13P-GS & GL	GSGL@
N13M-GS	GM@
support AC function	AC@
no AC function	NOAC@

USB Port Table

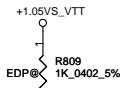
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
		5	
		6	
EHCI2	UHCI3	7	
		8	Mini Card 1(WLAN)
	UHCI4	9	
		10	Camera
		11	BlueTooth
		12	
		13	

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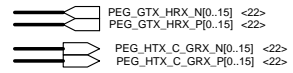
eDP_COMP# and ICOMPO signals should be shorted near balls, Trace Width for EDP_COMP# = 4mils, EDP_ICOMPO = 12mils, and both length less than 500 mils... should not be left floating, even if disable eDP function...

Add eDP circuit

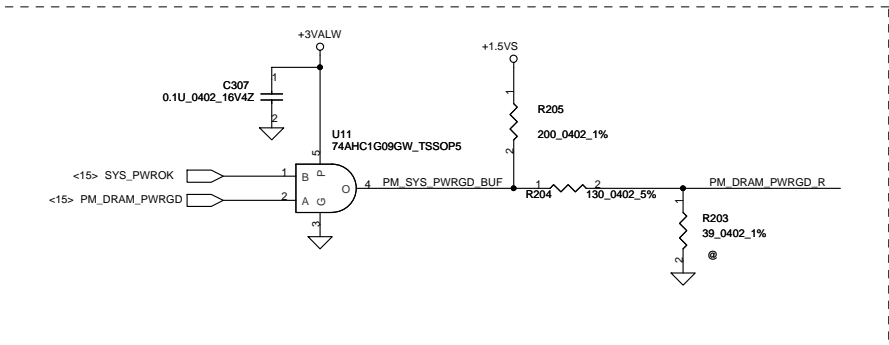
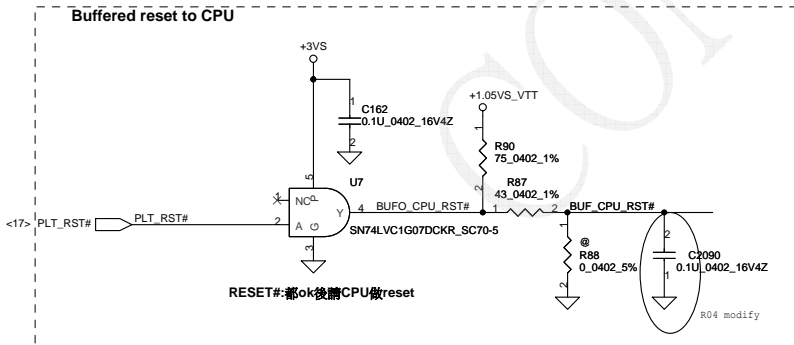
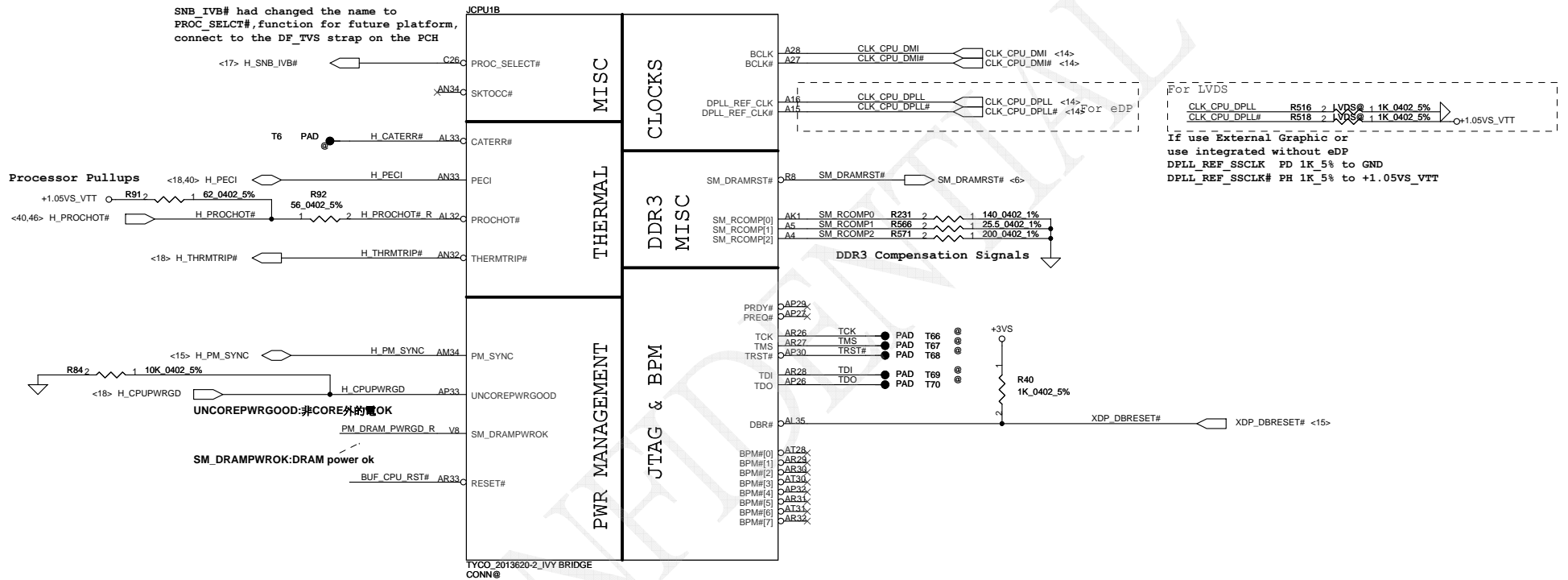


Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed, max length = 500 mils, trace width=4mils PEG_ICOMPO signals should be routed with - max length = 500 mils, trace width=12mils spacing = 15mils



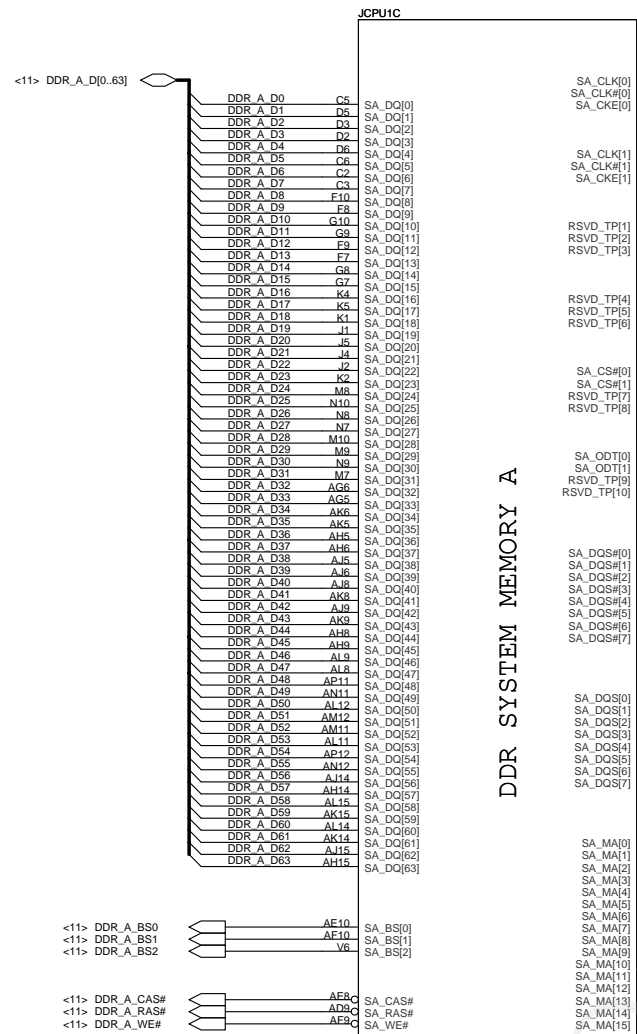
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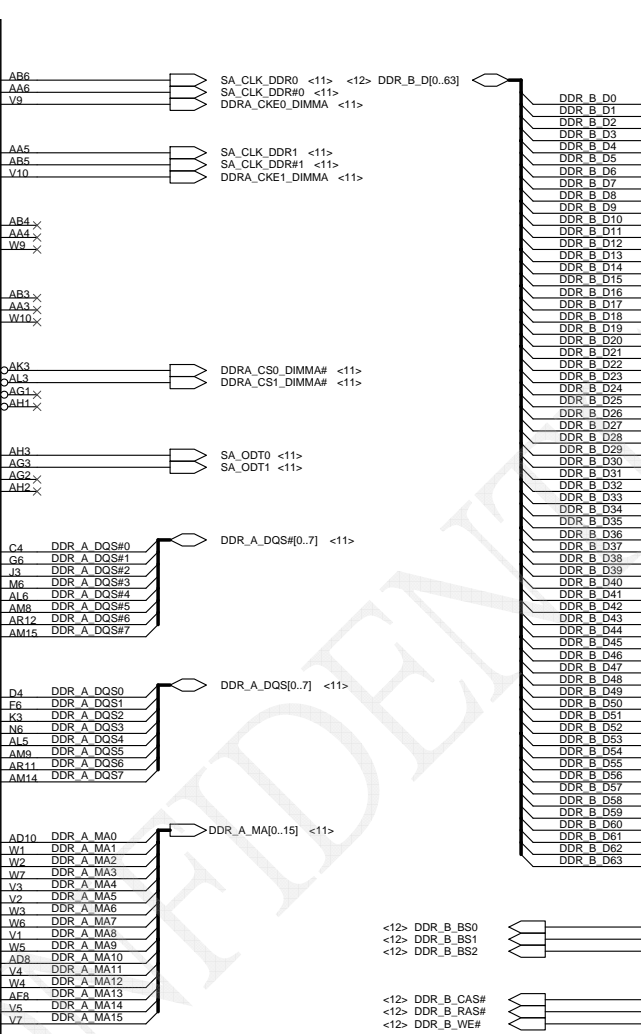
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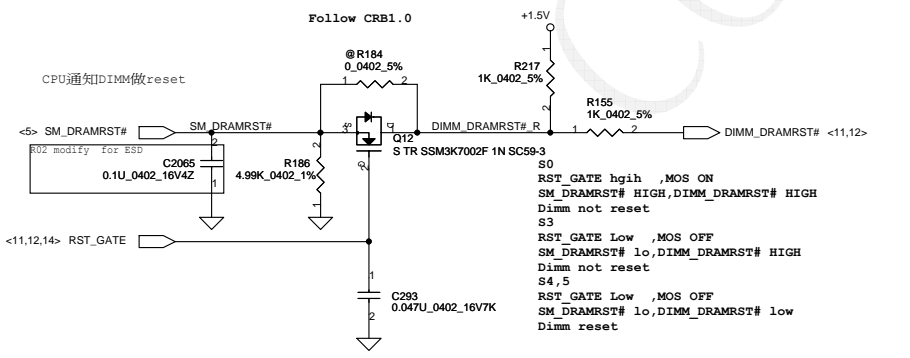
DDR SYSTEM MEMORY A

TYCO_2013620-2_IVY BRIDGE
CONN@



DDR SYSTEM MEMORY B

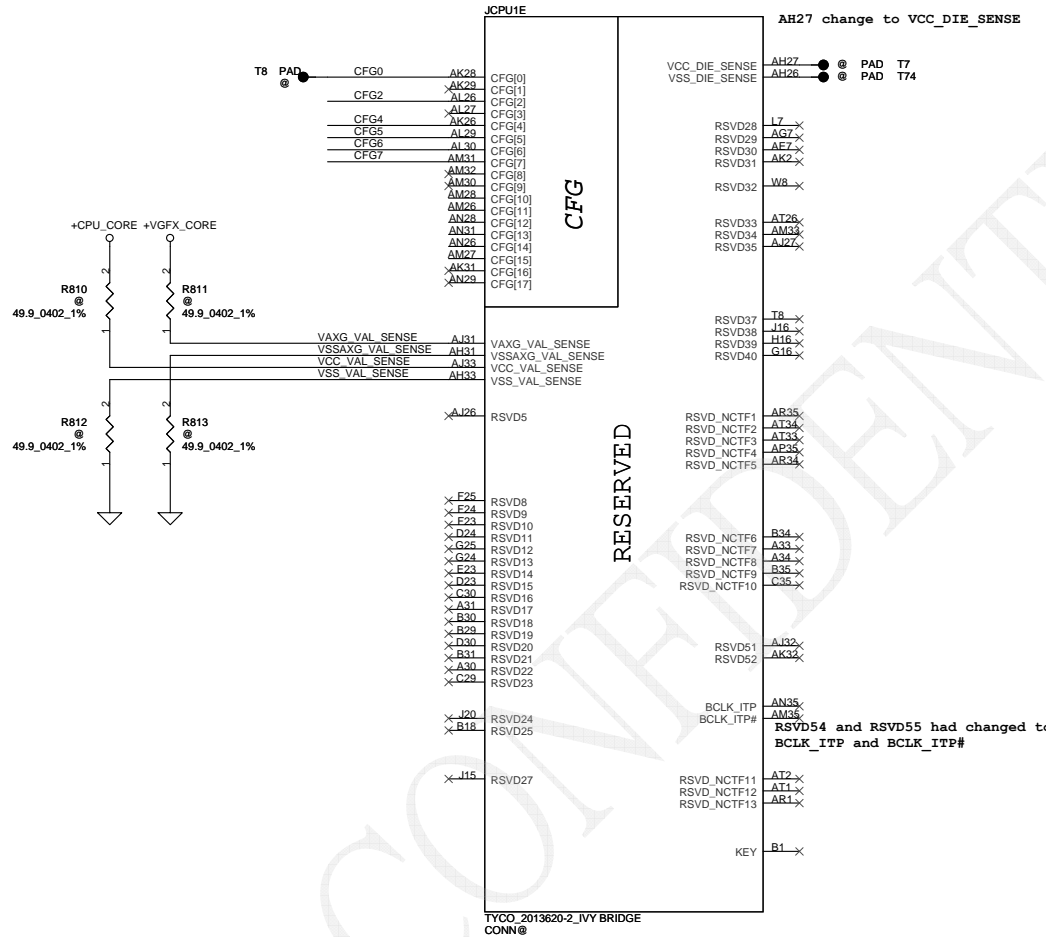
TYCO_2013620-2_IVY BRIDGE
CONN@



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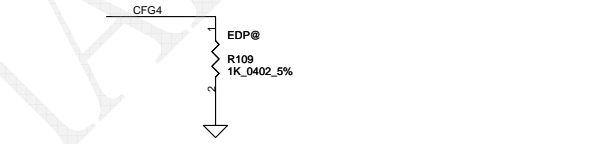
CFG Straps for Processor

AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE



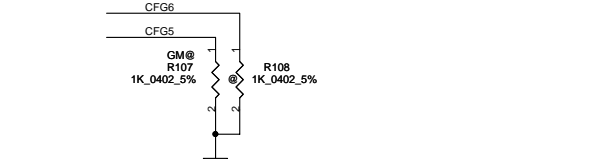
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed



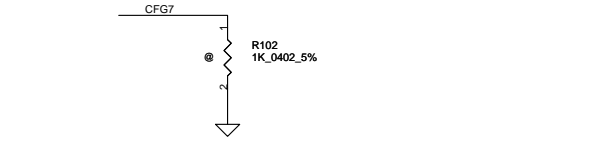
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps

CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

SV type CPU

JCPU1F

POWER

+CPU_CORE
QC 53A
DC 53A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- P25 VCC100

CORE SUPPLY

PEG AND DDR

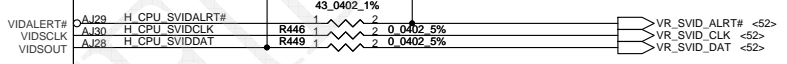
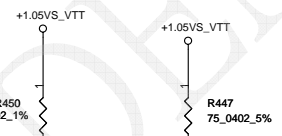
SVID

SENSE LINES

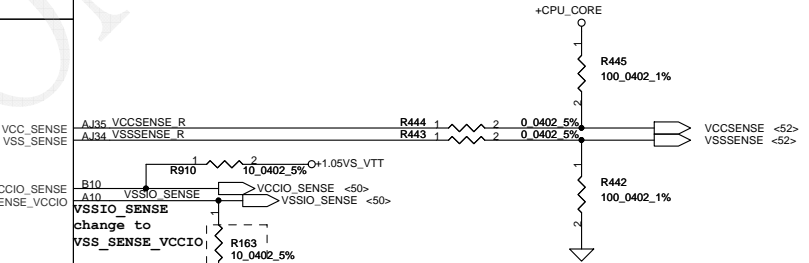
- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AC10
- VCCIO4 Y10
- VCCIO5 LH10
- VCCIO6 L10
- VCCIO7 J12
- VCCIO8 J14
- VCCIO9 J12
- VCCIO10 J12
- VCCIO11 H14
- VCCIO12 H14
- VCCIO13 H14
- VCCIO14 H12
- VCCIO15 H11
- VCCIO16 G14
- VCCIO17 G13
- VCCIO18 G12
- VCCIO19 F14
- VCCIO20 F13
- VCCIO21 F12
- VCCIO22 F11
- VCCIO23 E14
- VCCIO24 E12
- VCCIO25 E11
- VCCIO26 D14
- VCCIO27 D13
- VCCIO28 D12
- VCCIO29 D11
- VCCIO30 C14
- VCCIO31 C13
- VCCIO32 C12
- VCCIO33 C11
- VCCIO34 B14
- VCCIO35 B12
- VCCIO36 A14
- VCCIO37 A13
- VCCIO38 A12
- VCCIO39 A11
- VCCIO40 J23

8.5A

+1.05VS_VTT



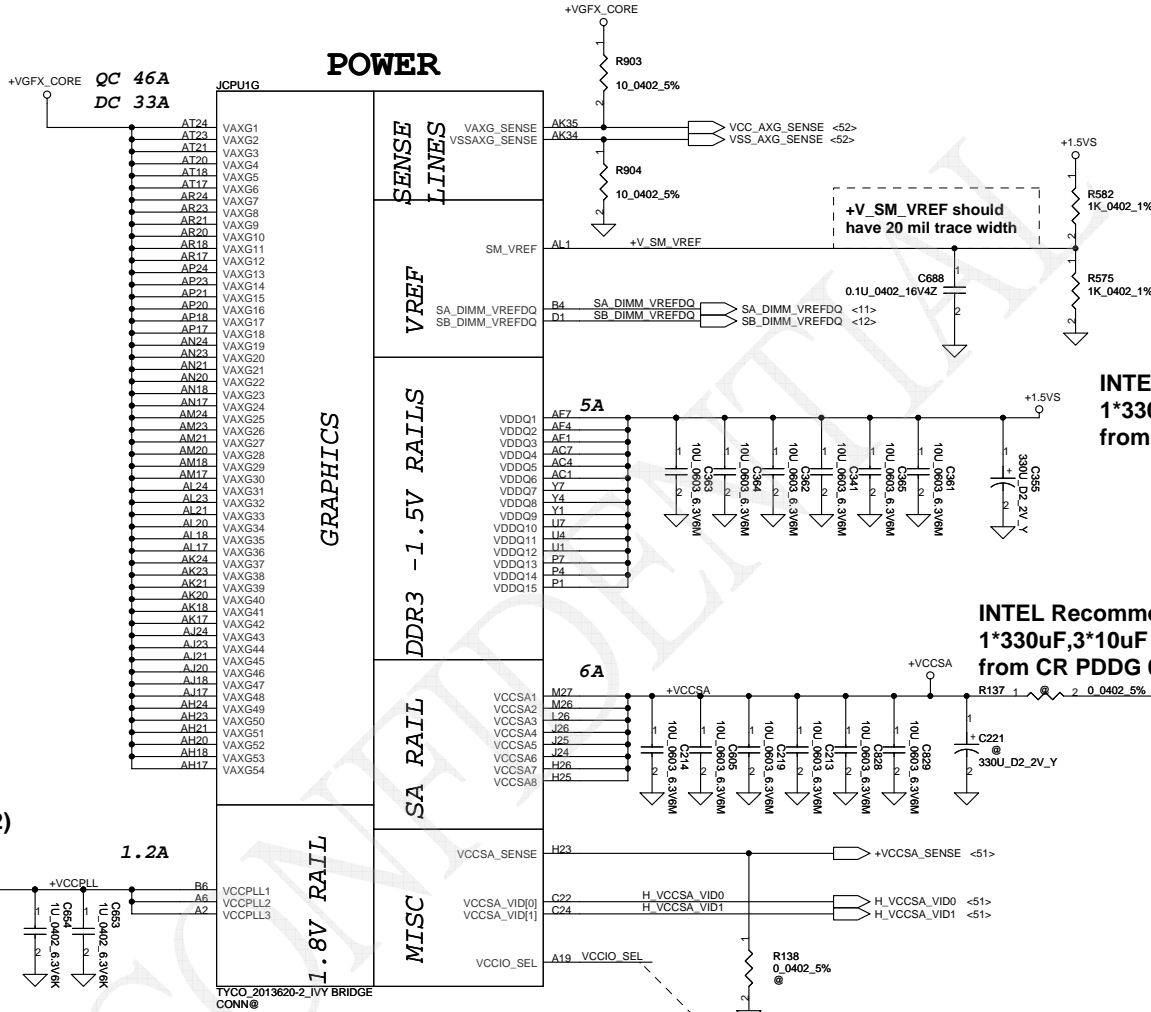
Place the PU resistors close to CPU



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INTEL Recommend
1*330uF, 1*10uF and 2*1uF(0402)
from CR PDDG 0.8

INTEL Recommend
1*330uF, 6*10uF
from CR PDDG 0.8

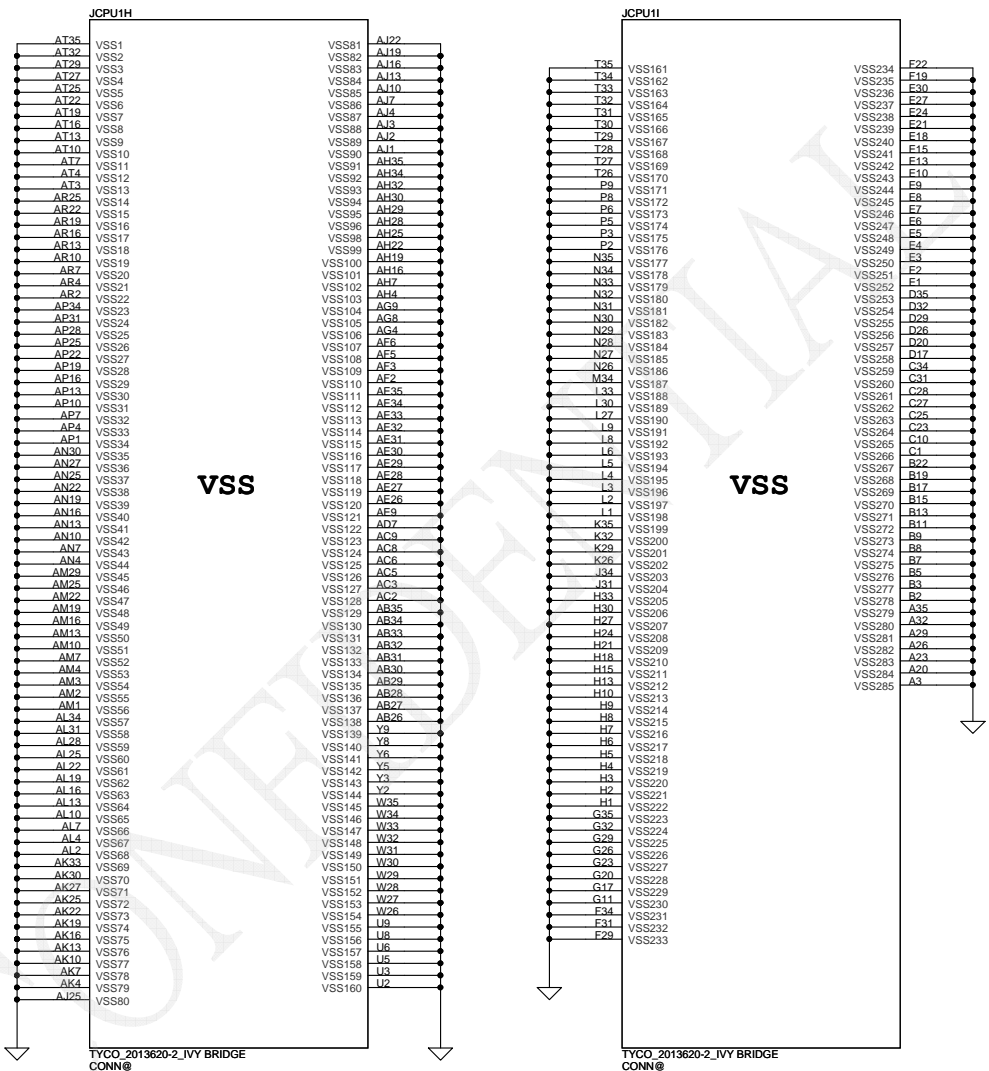
INTEL Recommend
1*330uF, 3*10uF
from CR PDDG 0.8

VCCSA				
VID0	VID1	Vout	Sandy	Ivy
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

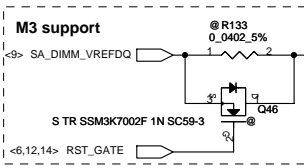
VCCIO_SEL For 2012 CPU support	
A19 *	1/NC : (Default) +1.05VS_VTT
	0: +1.0VS_VTT

RSVD26 had changed the name to VCCIO_SEL
 Need PH +3VALW 10K at +1.05VS_VTT source
 for 2012 processor +1.05V and +1.0V select

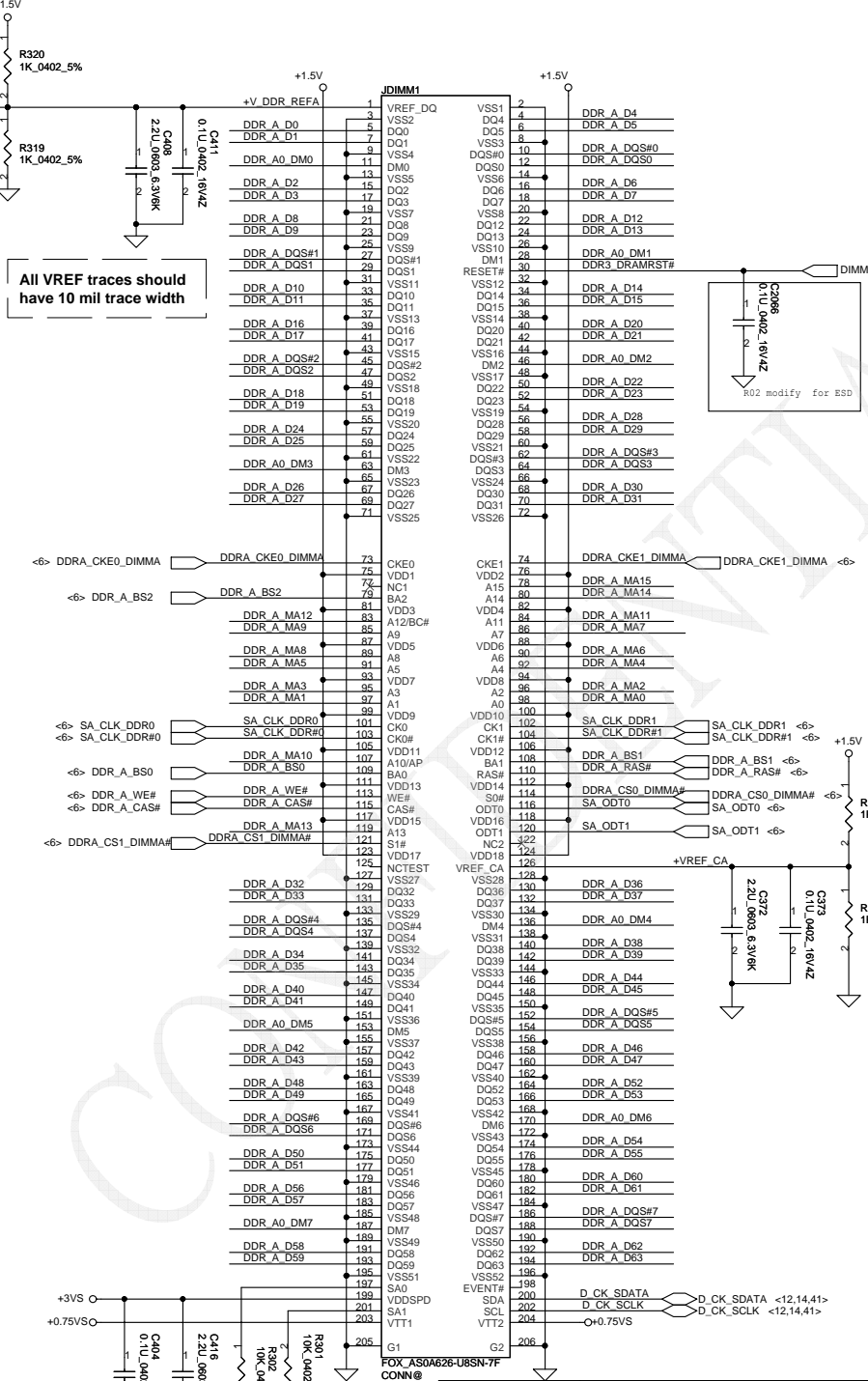
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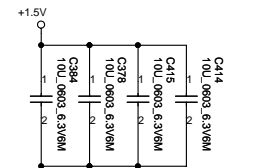
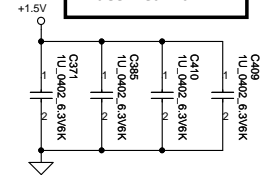
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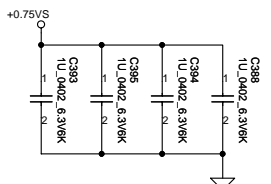
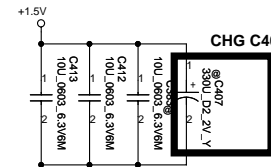
All VREF traces should have 10 mil trace width



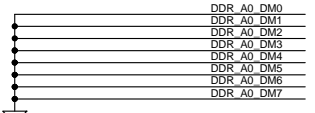
Layout Note:
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CHG C407 to oscon



Layout Note:
Place near JDIMM1.203,204



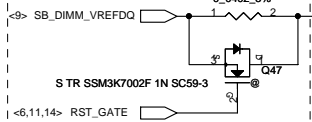
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DIMM_1 Reserve H:8mm

Classification	Compal Secret Data	
Issued Date	2011/06/02	Deciphered Date
		2012/06/02

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M3 support



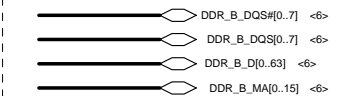
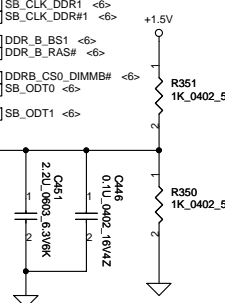
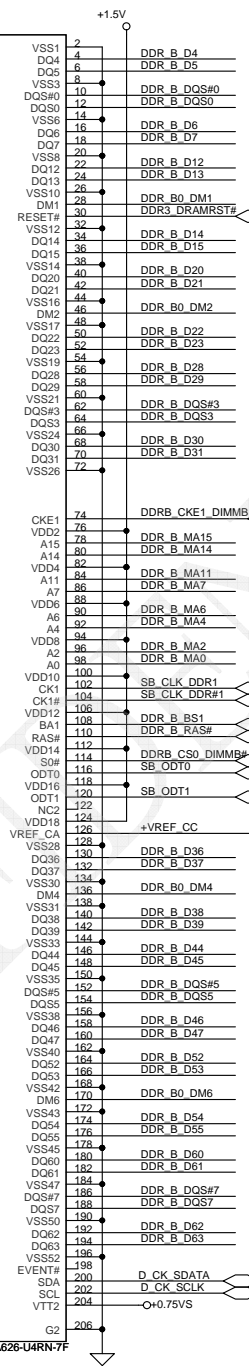
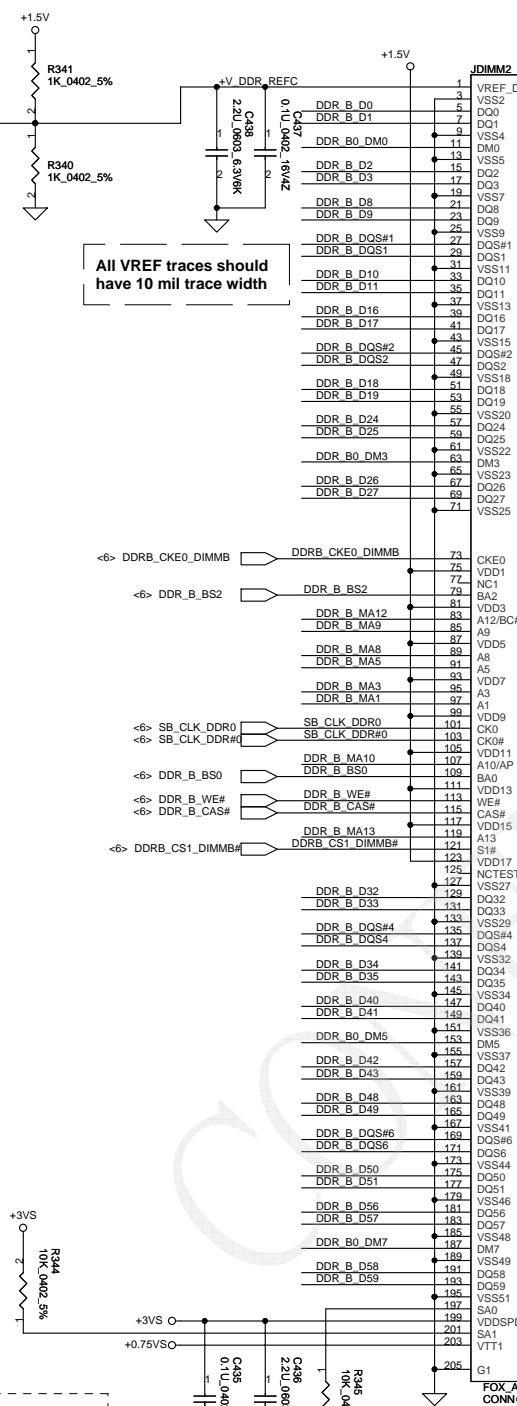
All VREF traces should have 10 mil trace width

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<6> DDRB_CS1_DIMMB#

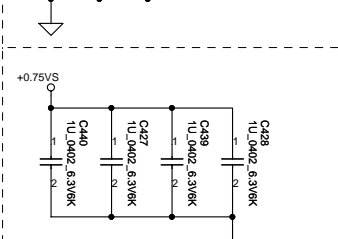
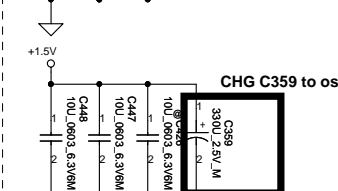
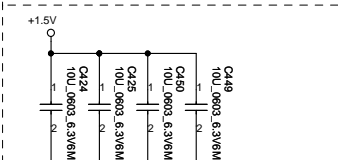
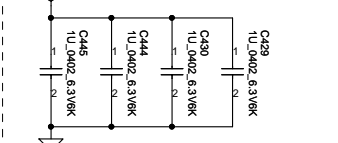
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DDR B D33
DDR B DOS#4
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DDR B D42
DDR B D43
DDR B D48
DDR B D49
DDR B DOS#6
DDR B DOS6
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DDR B D58
DDR B D59

+3VS
+0.75VS

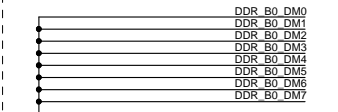
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DIMM_2 Reserve H:4mm



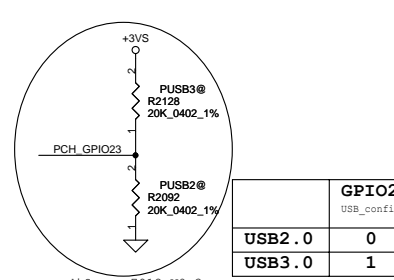
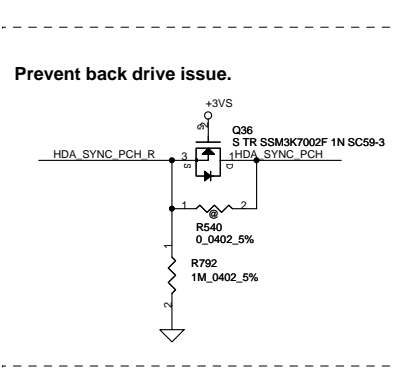
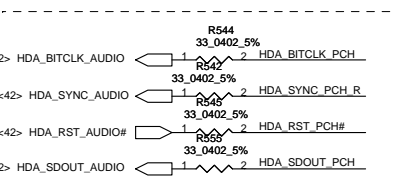
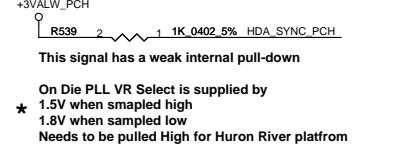
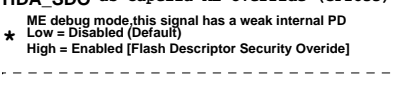
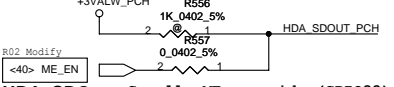
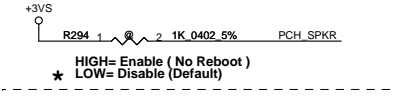
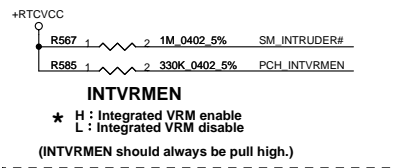
Layout Note:
Place near JDIMM2



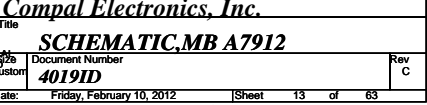
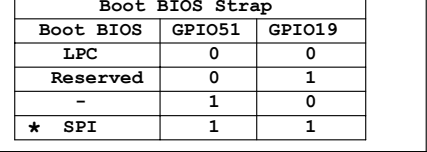
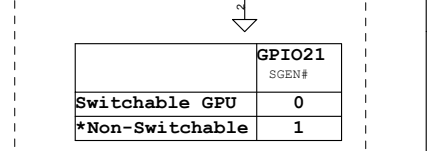
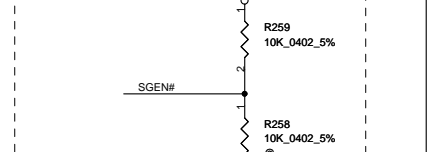
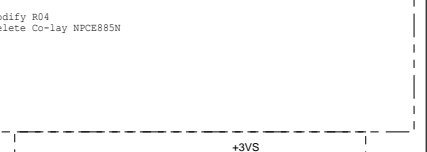
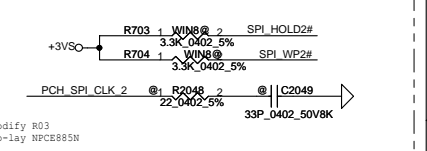
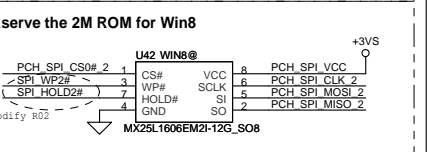
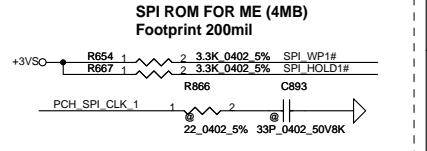
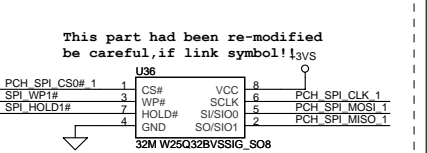
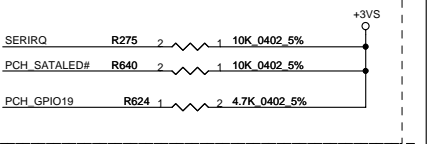
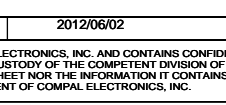
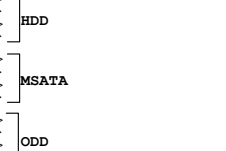
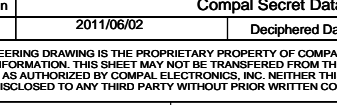
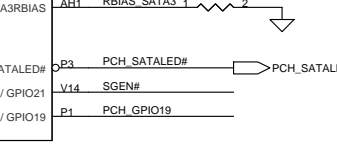
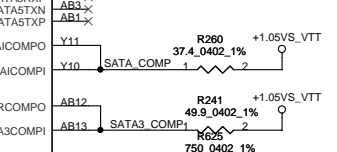
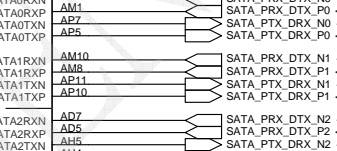
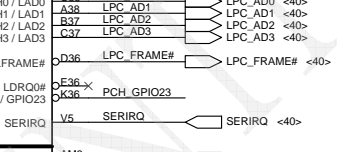
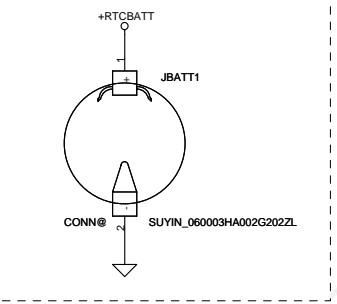
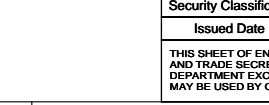
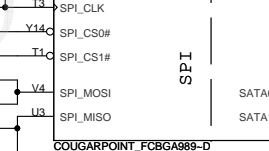
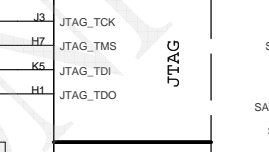
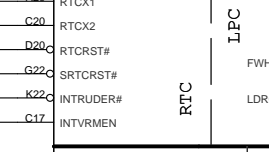
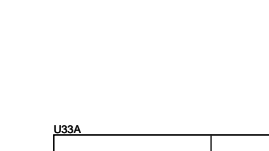
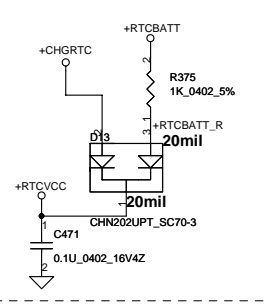
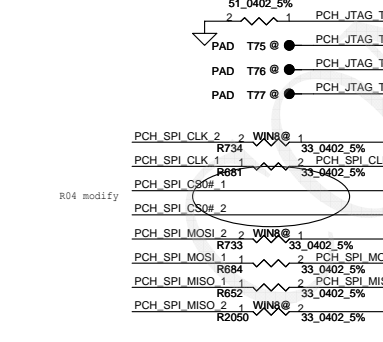
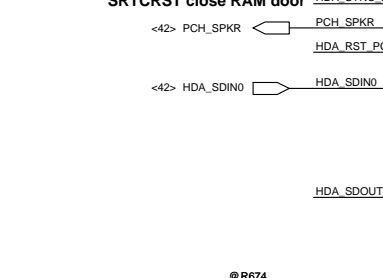
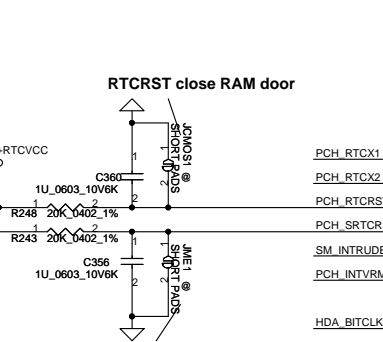
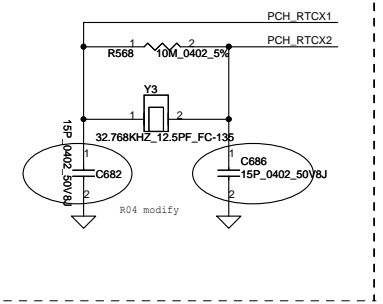
Layout Note:
Place near JDIMM2.203,204



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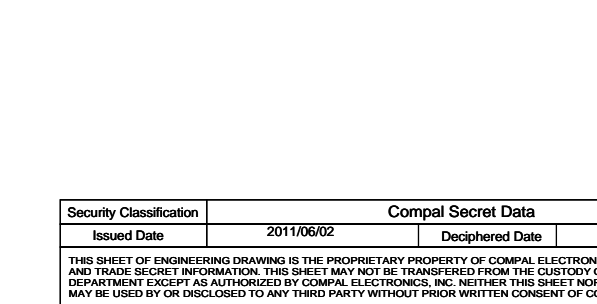
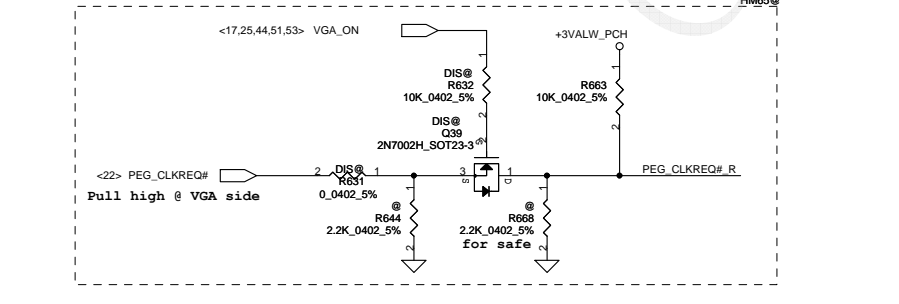
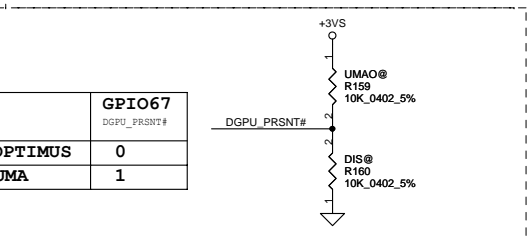
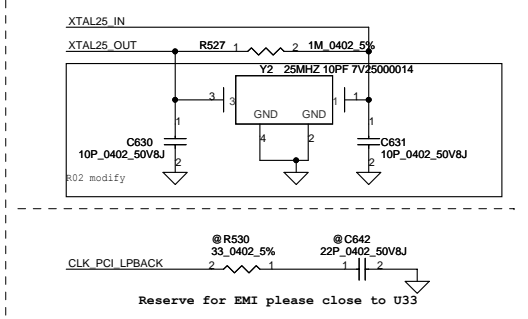
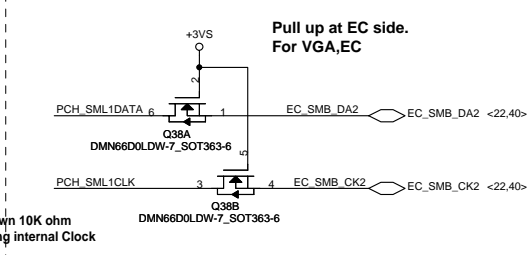
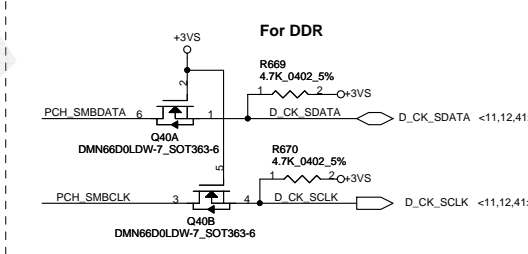
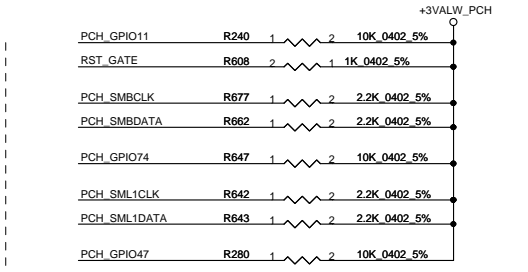
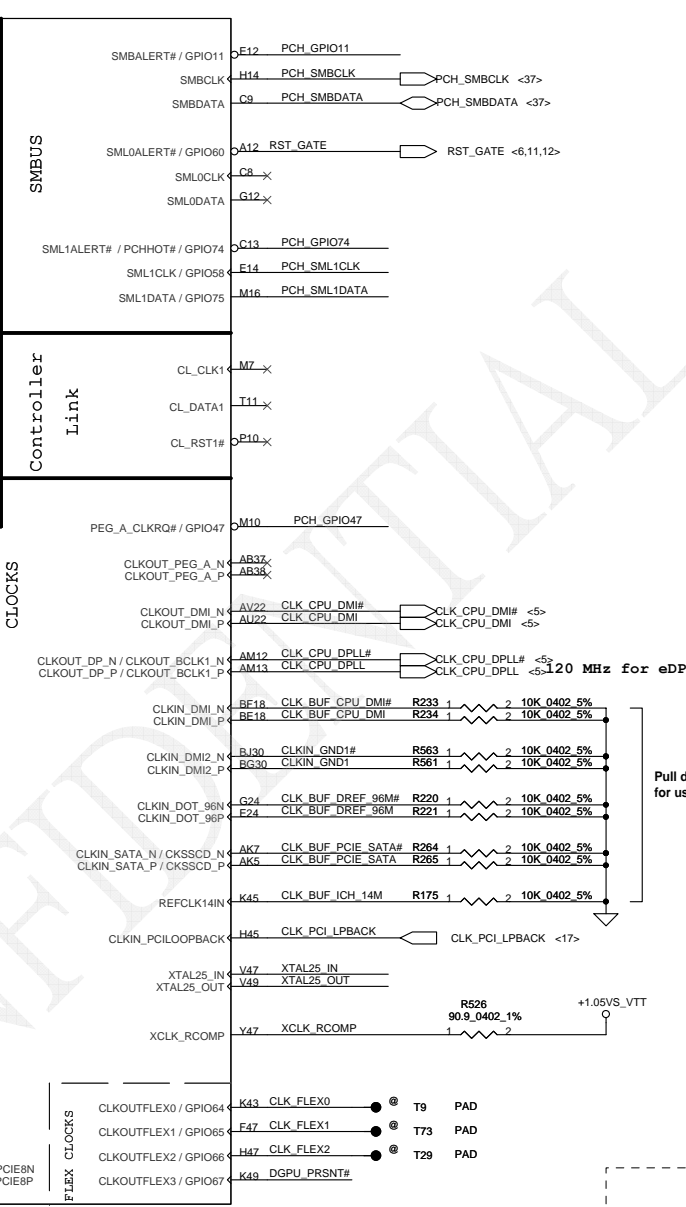
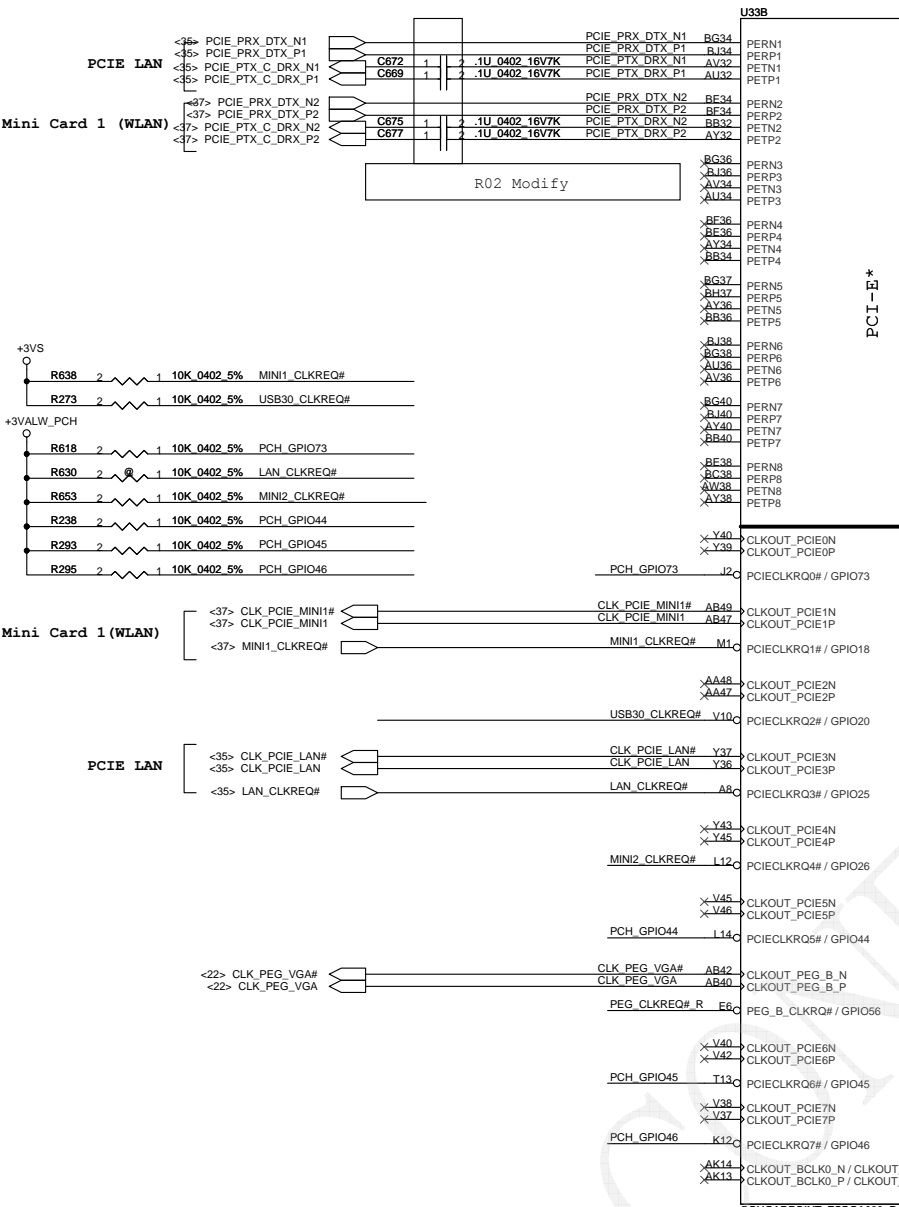
modify on 7912 V0.3



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Issued Date	2011/06/02	Deciphered Date
		2012/06/02

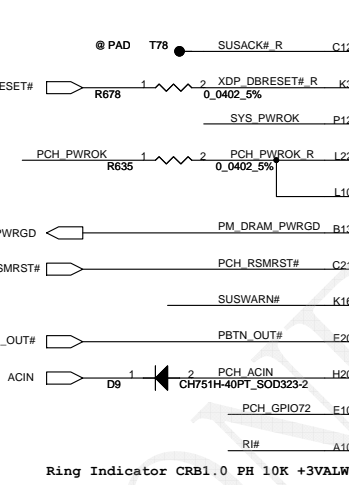
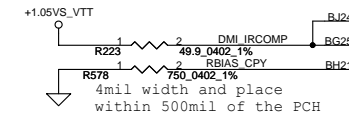
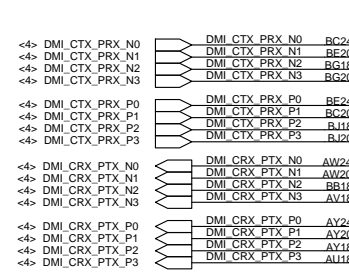
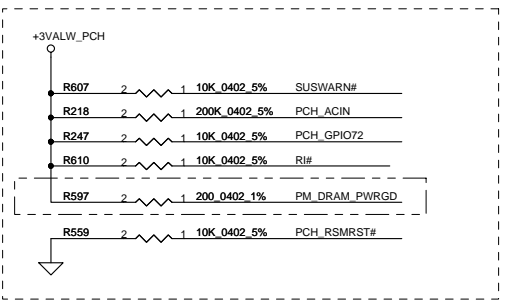
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Compal Electronics, Inc.		
Title		
SCHEMATIC, MB A7912		
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Date:	Friday, February 10, 2012	Sheet 13 of 63



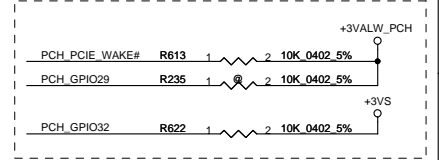
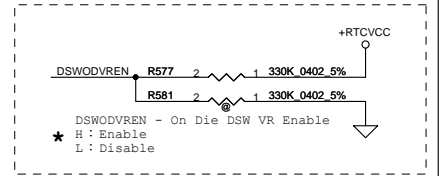
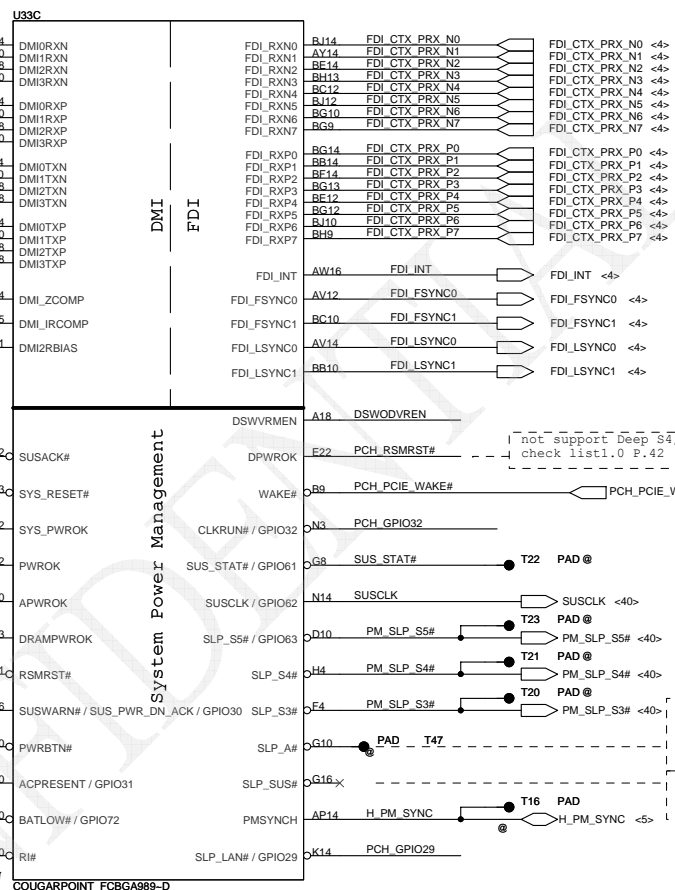
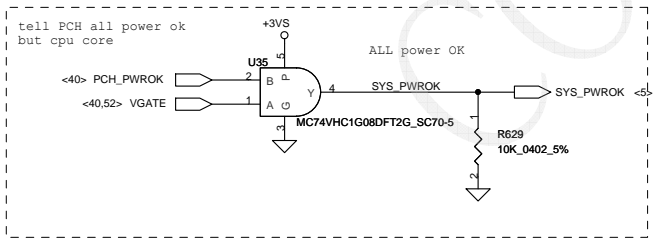
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		UMAO@	R159
		10K_0402_5%	
DGPU_PRSN#		↓	
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		10K_0402_5%	
		↓	

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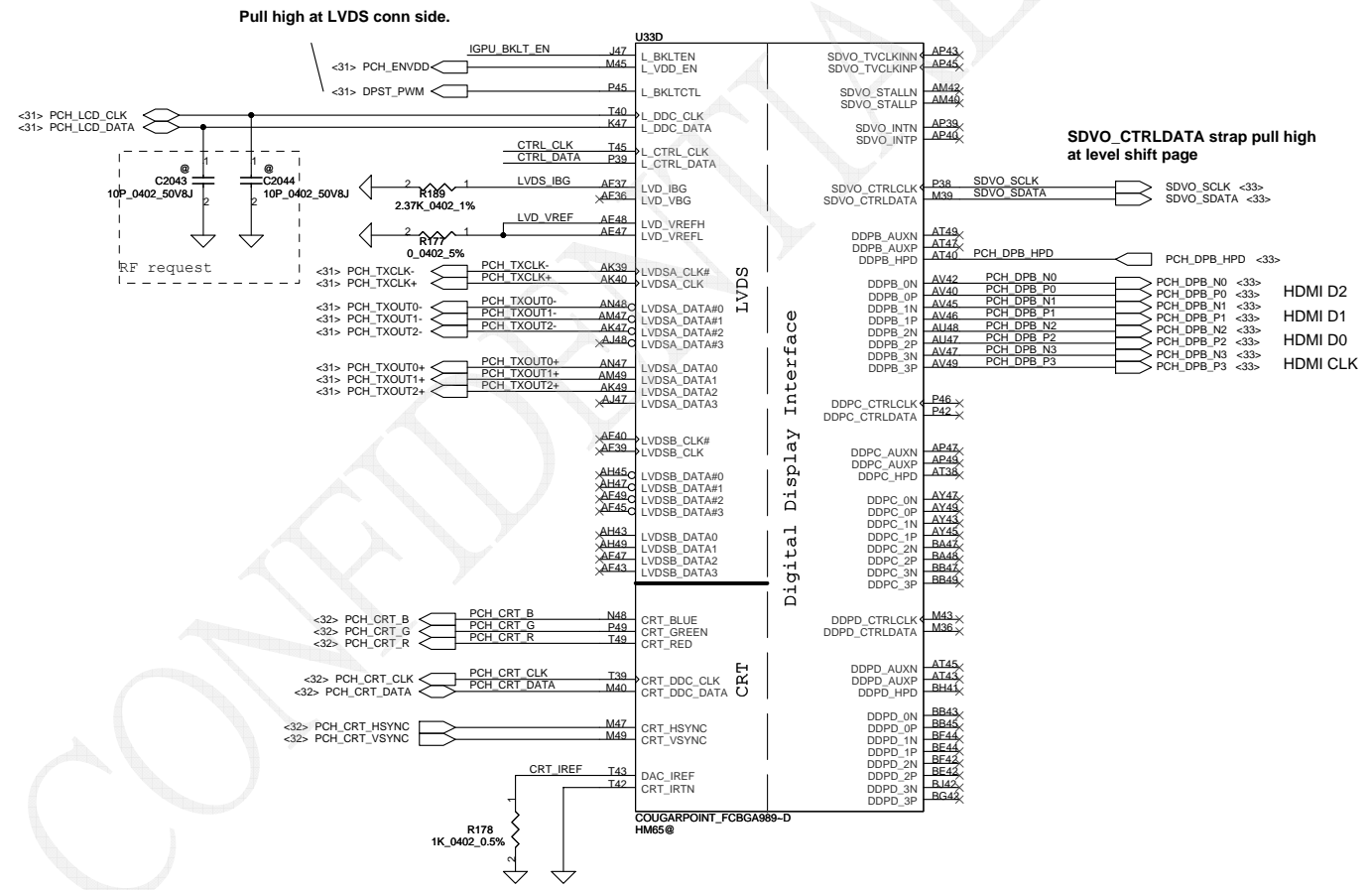
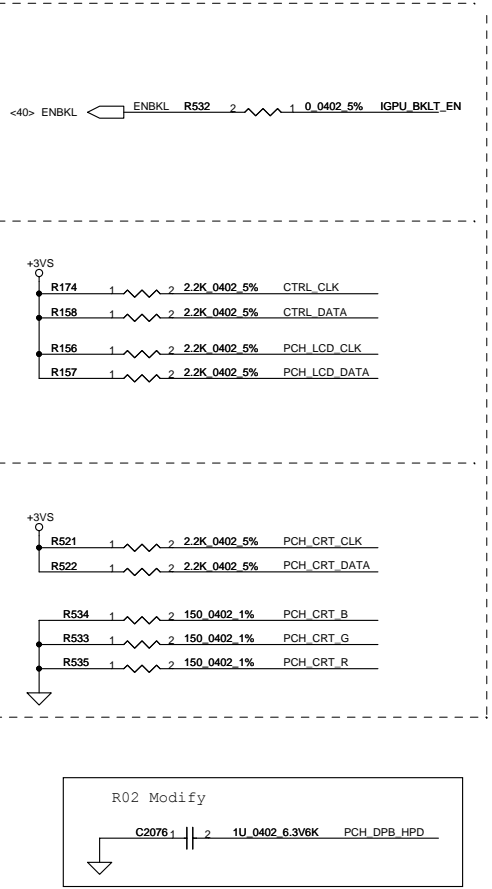
not support AMT APWROK can mux with PWROK (check list1.0 P.40)

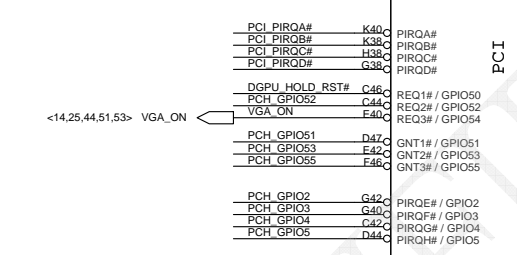
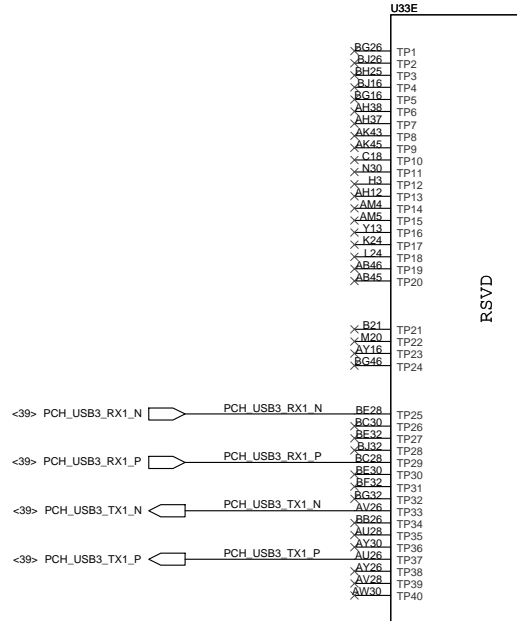
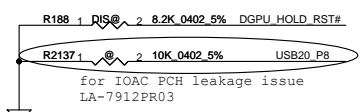
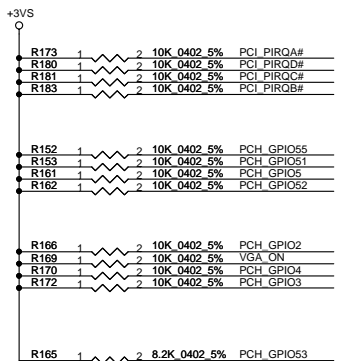
Can be left NC when IAMT is not support on the platform
not support Deep S4,S5 can NC PCH EDS1.2 P.74



COUGARPOINT_FCBGA989-D HM65@

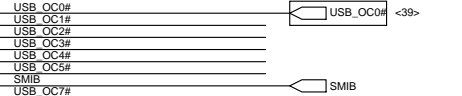
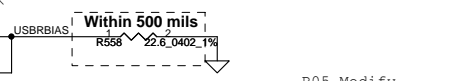
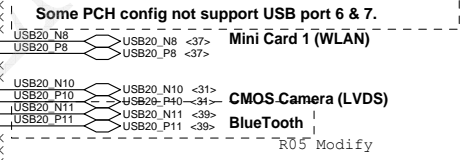
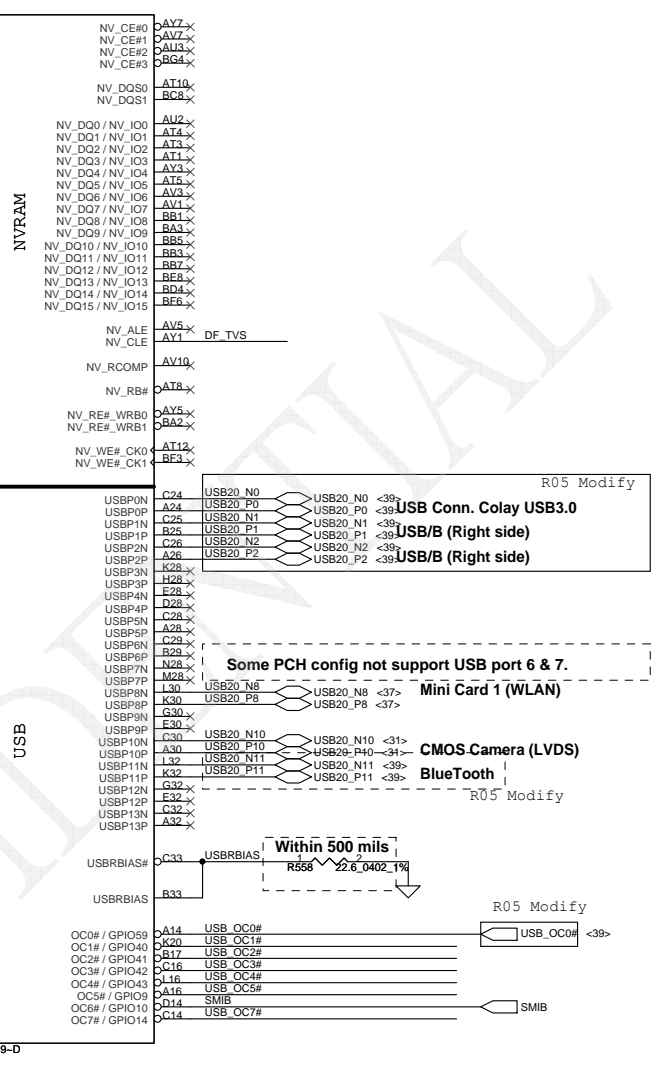
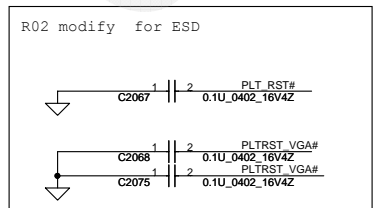
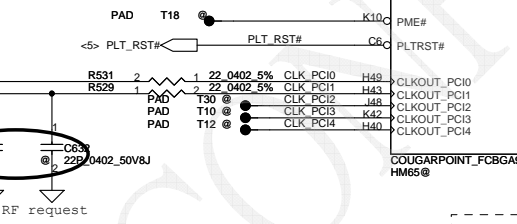
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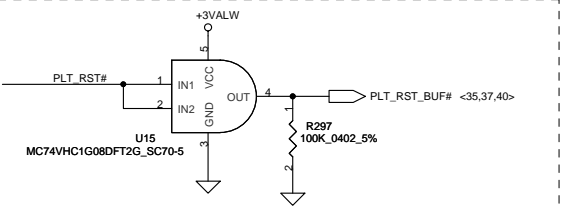
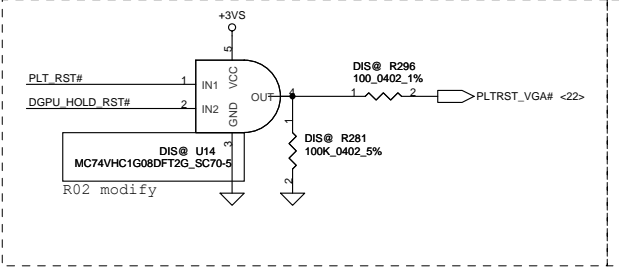
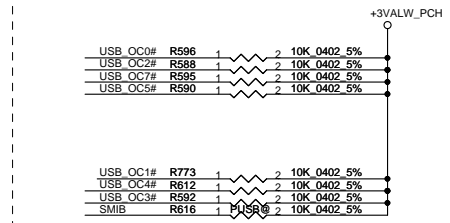
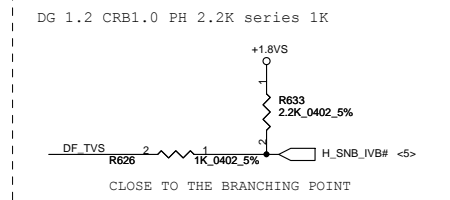
GPIO51 Internal pull high

Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



DMI Termination Voltage

DF_TV5	Set to Vcc when HIGH
	Set to Vss when LOW

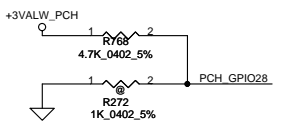


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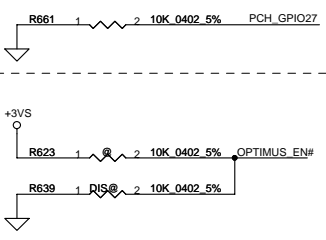
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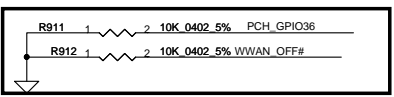
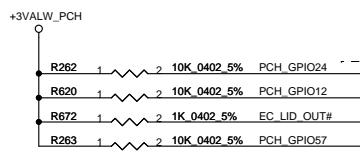
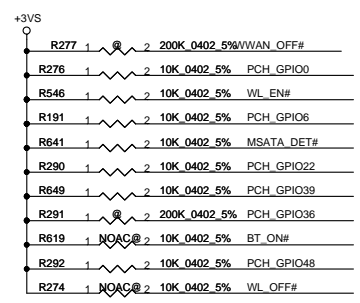
GPIO28 HDA_SYNC PH(PLL =+1.5VS)
 On-Die PLL Voltage Regulator
 This signal has a weak internal pull up
 * H : On-Die voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal
 No use PD to GND Check list1.0 P.70

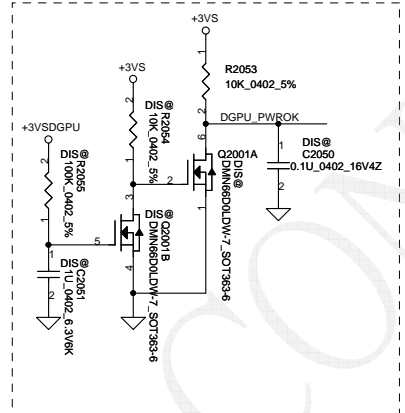


	GPIO38
	OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1



GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
 CRB1.0 PH10K to +3VALW

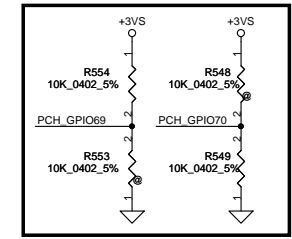
GPIO36/GPIO37 is Strap functionality that requires internal pull down to be sampled at rising PWROK. When uses as SATA2GP/SATA3GP for mechanical presence detect -use an external pull up 150K-200K ohm to Vcc3_3
 When used as GP input -ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP -use 8.2K-10K pull-down
 check list page 47



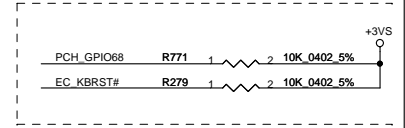
Signal	Pin	Component
PCH_GPIO0	TZ	BMBUSY# / GPIO0
<39> WL_EN#	A42	TACH1 / GPIO1
PCH_GPIO6	H36	TACH2 / GPIO6
<40> EC_SCI#	E38	TACH3 / GPIO7
<40> EC_SMI#	C10	GPIO8
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
<40> EC_LID_OUT#	G2	GPIO15
<37> MSATA_DET#	U2	SATA4GP / GPIO16
DGPU_PWROK	D40	TACH0 / GPIO17
PCH_GPIO22	T5	SCLOCK / GPIO22
PCH_GPIO24	E8	GPIO24 / MEM_LED
PCH_GPIO27	F16	GPIO27
PCH_GPIO28	P8	GPIO28
<37,39,40> BT_ON#	K1	STP_PC# / GPIO34
PCH_GPIO36	V8	GPIO35
WWAN_OFF#	M5	SATA2GP / GPIO36
OPTIMUS_EN#	N2	SATA3GP / GPIO37
PCH_GPIO39	M3	SLOAD / GPIO38
PCH_GPIO48	V13	SDATAOUT0 / GPIO39
<37,40> WL_OFF#	V3	SDATAOUT1 / GPIO48
PCH_GPIO57	D6	SATA5GP / GPIO49
GPIO57	D6	GPIO57

Signal	Pin	Component
TACH4 / GPIO68	C40	PCH_GPIO68
TACH5 / GPIO69	B41	PCH_GPIO69
TACH6 / GPIO70	C41	PCH_GPIO70
TACH7 / GPIO71	A40	PCH_GPIO71
PCH_GPIO71	<31>	PCH_GPIO71
A20GATE	P4	GATEA20 <40>
PECI	AU16	PCH_PECI R
RCIN#	B5	EC_KBRST#
PROC_PWRGD	AY11	H_CPU_PWRGD <5>
THRMTRIP#	AY10	PCH_THRMTRIP# R
INIT3_3V#	T14	H_THRMTRIP# <5>
NC_1	AH8	
NC_2	AK11	
NC_3	AH10	
NC_4	AK10	
NC_5	P37	
VSS_NCTF_15	BG2	
VSS_NCTF_16	BG48	
VSS_NCTF_17	BH3	
VSS_NCTF_18	BH47	
VSS_NCTF_19	B4	
VSS_NCTF_20	B44	
VSS_NCTF_21	B45	
VSS_NCTF_22	B46	
VSS_NCTF_23	B45	
VSS_NCTF_24	B15	
VSS_NCTF_25	B16	
VSS_NCTF_26	C2	
VSS_NCTF_27	C48	
VSS_NCTF_28	D1	
VSS_NCTF_29	D49	
VSS_NCTF_30	E1	
VSS_NCTF_31	F1	
VSS_NCTF_32	E49	

INIT3_3V# Check list 1.0 P.59
 This signal has weak internal PU, can't pull low, leave NC
 TS_VSS1-4
 PD to GND



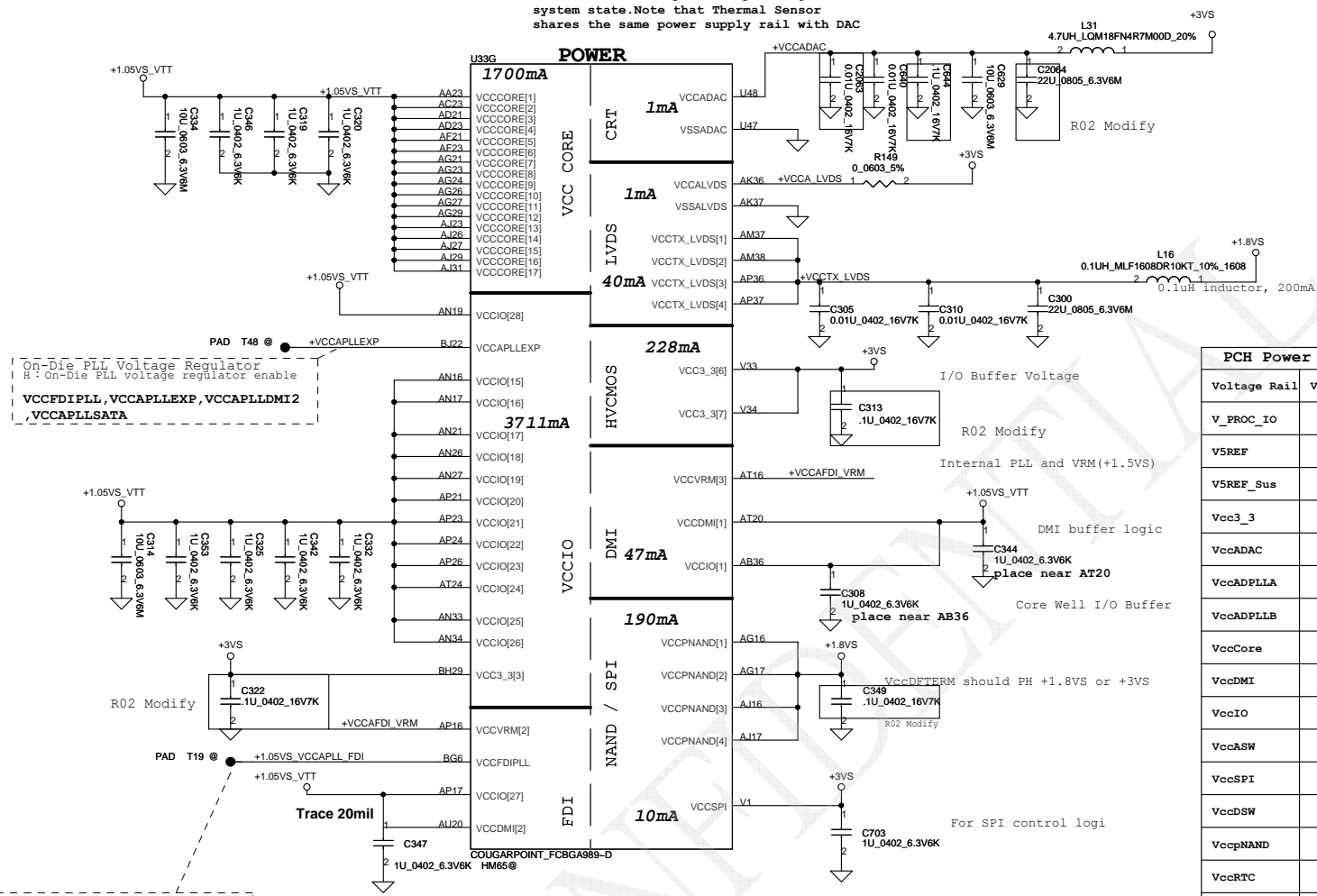
Project ID	GPIO69	GPIO70
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1



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4019ID <td colspan="2">Rev C</td>		Rev C	
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+VCCADAC should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC

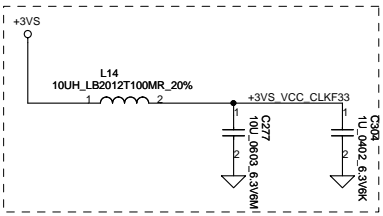


PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

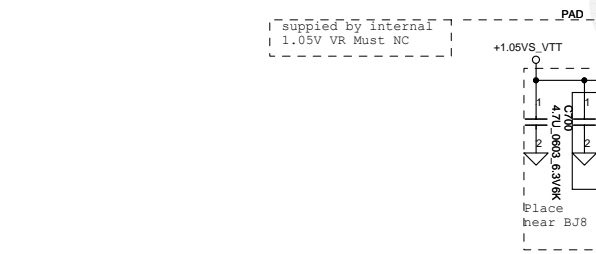
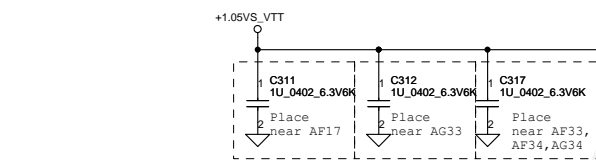
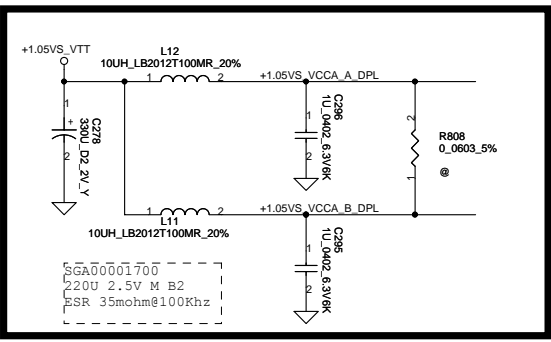
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

GPI028
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2

+1.5VS
R257 0.0603 5% +VCCAFDI_VRM
+VCCAFDI_VRM
VCCVRM=>1.5V FOR MOBILE
VCCVRM=>1.8V FOR DESKTOP
VCCVRM = 160mA dotal waiting for newest spec
HDA_SYNC PH (PLL =>1.5VS)



GPIO28
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

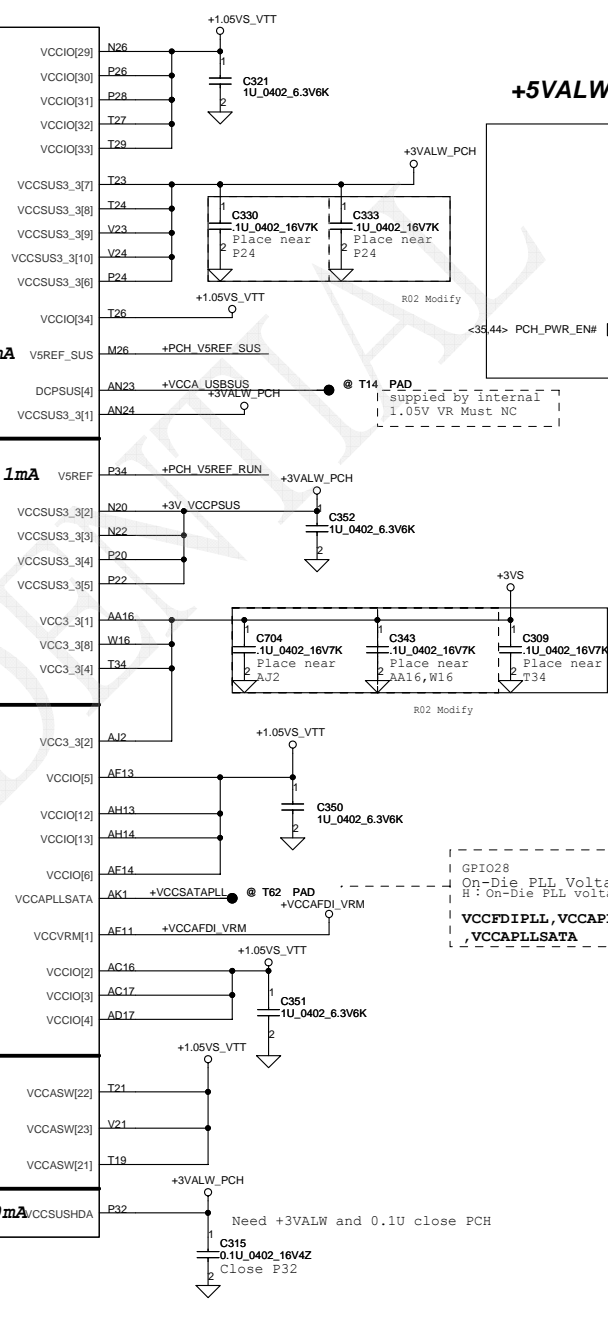
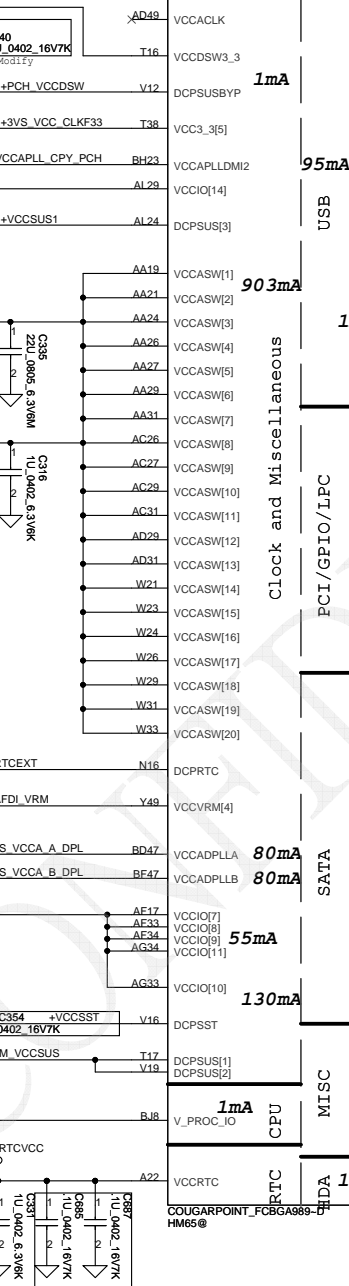


Not support Deep S4,S5 connect to +3VALW

supplied by internal 1.05V VR must NC

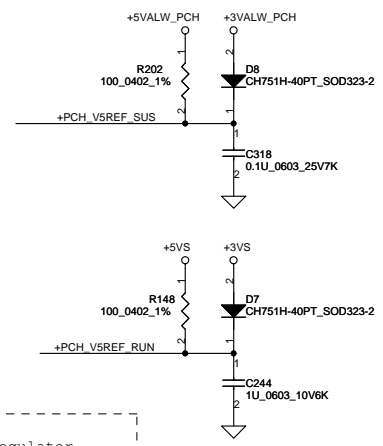
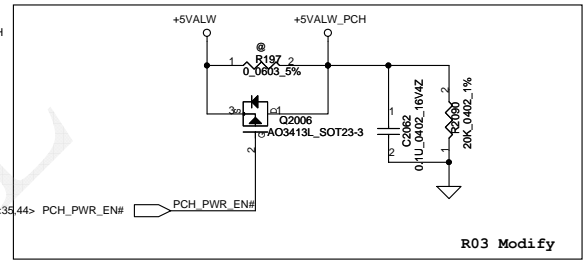
GPIO28
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

POWER



VCC3_3 = 266mA detail waiting for newest spec
VCCDMI = 42mA detail waiting for newest spec

+5VALW TO +5VALW_PCH(PCH AUX Power)



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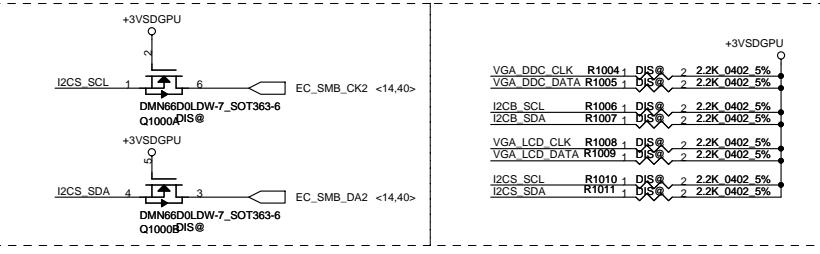
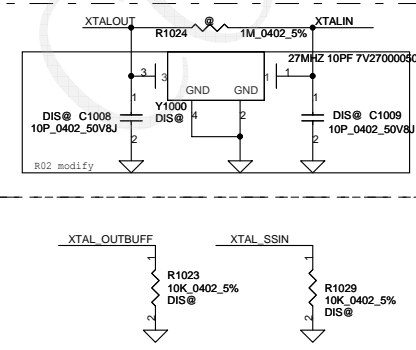
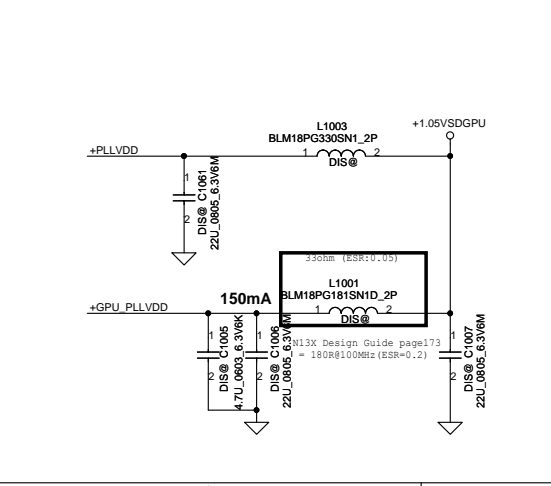
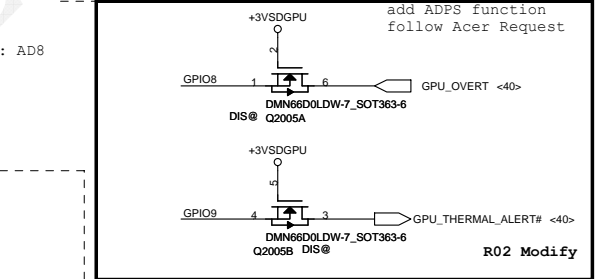
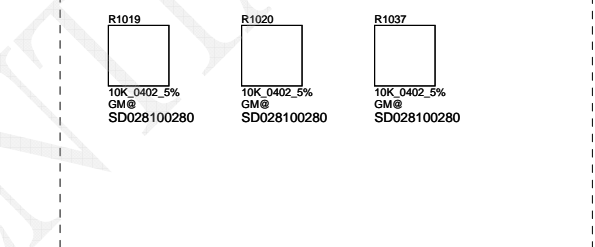
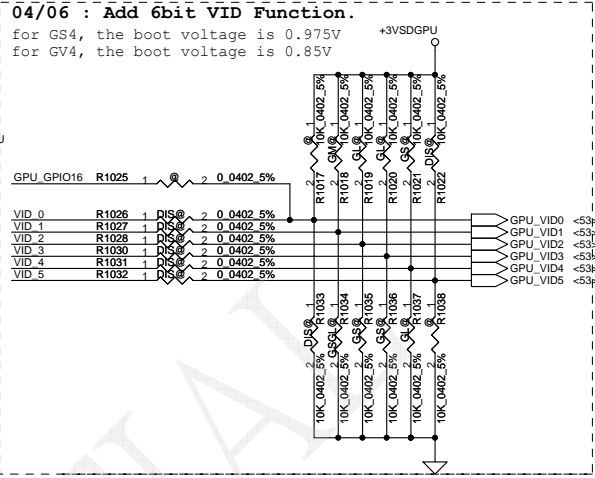
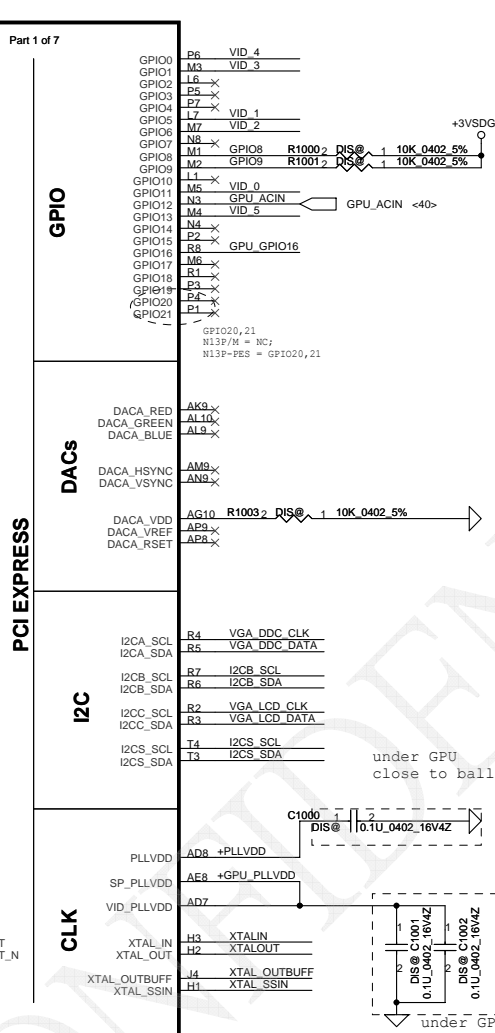
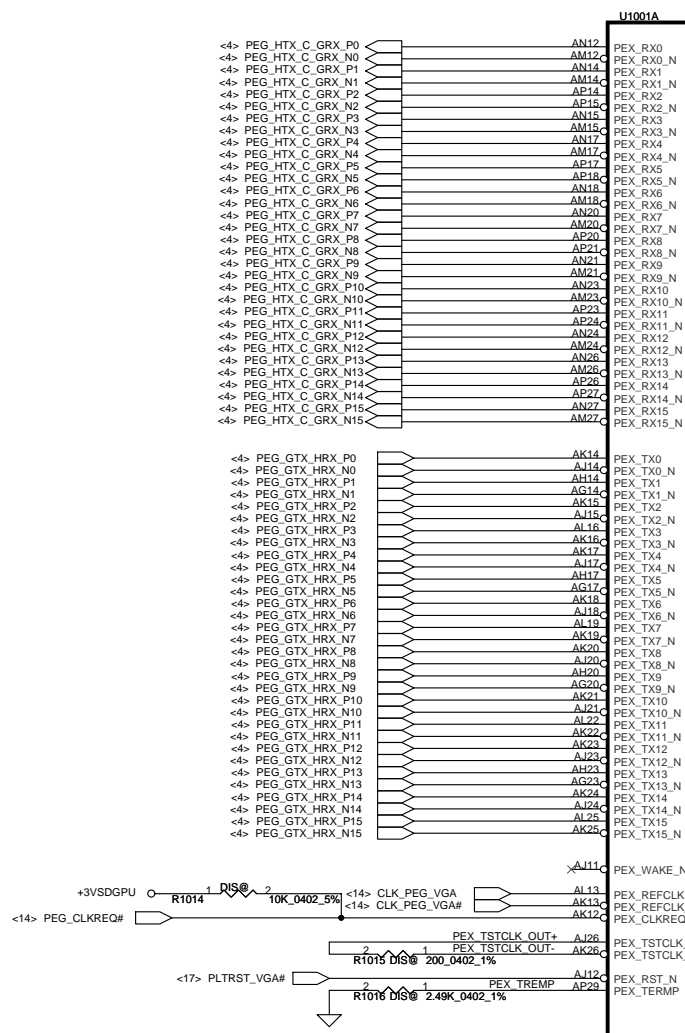
U33H		U33I	
H5	VSS[0]		
AA17	VSS[1]	AK38	
AA2	VSS[2]	AK4	
AA3	VSS[3]	AK42	
AA33	VSS[4]	AK46	
AA34	VSS[5]	AK5	
AB11	VSS[6]	AL16	
AB14	VSS[7]	AL17	
AB39	VSS[8]	AL19	
AB4	VSS[9]	AL2	
AB43	VSS[10]	AL21	
AB5	VSS[11]	AL23	
AB7	VSS[12]	AL26	
AC19	VSS[13]	AL27	
AC2	VSS[14]	AL31	
AC21	VSS[15]	AL33	
AC24	VSS[16]	AL34	
AC33	VSS[17]	AL46	
AC34	VSS[18]	AM11	
AC48	VSS[19]	AM14	
AD10	VSS[20]	AM36	
AD11	VSS[21]	AM39	
AD12	VSS[22]	AM43	
AD13	VSS[23]	AM45	
AD19	VSS[24]	AM46	
AD24	VSS[25]	AM7	
AD26	VSS[26]	AN2	
AD27	VSS[27]	AN29	
AD33	VSS[28]	AN3	
AD34	VSS[29]	AN31	
AD36	VSS[30]	AP12	
AD37	VSS[31]	AP19	
AD38	VSS[32]	AP28	
AD39	VSS[33]	AP30	
AD4	VSS[34]	AP32	
AD40	VSS[35]	AP38	
AD42	VSS[36]	AP4	
AD43	VSS[37]	AP42	
AD45	VSS[38]	AP46	
AD46	VSS[39]	AP8	
AD8	VSS[40]	AR2	
AE2	VSS[41]	AR48	
AE3	VSS[42]	AT11	
AF10	VSS[43]	AT13	
AF12	VSS[44]	AT18	
AD14	VSS[45]	AT22	
AD16	VSS[46]	AT26	
AF16	VSS[47]	AT28	
AF19	VSS[48]	AT30	
AF24	VSS[49]	AT32	
AF26	VSS[50]	AT34	
AF27	VSS[51]	AT39	
AF29	VSS[52]	AT42	
AF31	VSS[53]	AT46	
AF38	VSS[54]	AT7	
AF4	VSS[55]	AU24	
AF42	VSS[56]	AU30	
AF46	VSS[57]	AV16	
AF5	VSS[58]	AV20	
AF7	VSS[59]	AV24	
AF8	VSS[60]	AV30	
AG19	VSS[61]	AV32	
AG2	VSS[62]	AV38	
AG31	VSS[63]	AV4	
AG48	VSS[64]	AV8	
AH11	VSS[65]	AW14	
AH3	VSS[66]	AW18	
AH36	VSS[67]	AW2	
AH39	VSS[68]	AW22	
AH40	VSS[69]	AW26	
AH42	VSS[70]	AW28	
AH46	VSS[71]	AW32	
AH7	VSS[72]	AW34	
AJ19	VSS[73]	AW36	
AJ21	VSS[74]	AW40	
AJ24	VSS[75]	AW48	
AJ33	VSS[76]	AY11	
AJ34	VSS[77]	AY12	
AK12	VSS[78]	AY22	
AK3	VSS[79]	AY28	

COUGARPOINT_FCBGA989-D
HM65@

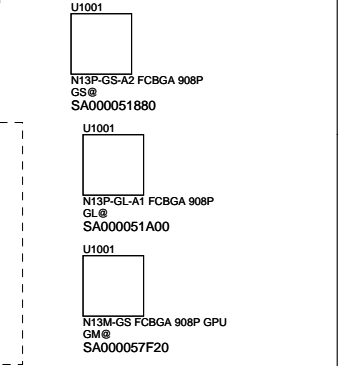
U33I		U33H	
AY4	VSS[159]	H46	
AY42	VSS[160]	K18	
AY48	VSS[161]	K26	
AY8	VSS[162]	K30	
B11	VSS[163]	K46	
B15	VSS[164]	K7	
B19	VSS[165]	L18	
B23	VSS[166]	L2	
B27	VSS[167]	L20	
B31	VSS[168]	L26	
B35	VSS[169]	L28	
B39	VSS[170]	L36	
B7	VSS[171]	L48	
F45	VSS[172]	M12	
FB12	VSS[173]	P16	
FB16	VSS[174]	M18	
FB20	VSS[175]	M22	
FB22	VSS[176]	M24	
FB24	VSS[177]	M30	
FB28	VSS[178]	M32	
FB30	VSS[179]	M34	
FB38	VSS[180]	M38	
FB4	VSS[181]	M4	
FB46	VSS[182]	M42	
RC14	VSS[183]	M46	
BC18	VSS[184]	M8	
BC2	VSS[185]	N18	
BC22	VSS[186]	P30	
BC26	VSS[187]	N47	
BC32	VSS[188]	P11	
BC34	VSS[189]	P18	
BC36	VSS[190]	T33	
BC40	VSS[191]	P40	
BC42	VSS[192]	P43	
BC48	VSS[193]	P47	
BC46	VSS[194]	P7	
BD5	VSS[195]	R2	
BE2	VSS[196]	R48	
BE26	VSS[197]	T12	
BE40	VSS[198]	T31	
BE10	VSS[199]	T37	
BE12	VSS[200]	T4	
BE16	VSS[201]	W34	
BE20	VSS[202]	T46	
BE22	VSS[203]	T47	
BE24	VSS[204]	TR	
BE26	VSS[205]	V11	
BE28	VSS[206]	V17	
BD3	VSS[207]	V26	
BE30	VSS[208]	V27	
BE38	VSS[209]	V29	
BE40	VSS[210]	V31	
BE8	VSS[211]	V36	
BG17	VSS[212]	V39	
BG24	VSS[213]	V43	
BG33	VSS[214]	v7	
BG44	VSS[215]	W17	
BG8	VSS[216]	W19	
BH11	VSS[217]	W2	
BH15	VSS[218]	W27	
BH17	VSS[219]	W48	
BH19	VSS[220]	Y12	
H10	VSS[221]	Y28	
BH27	VSS[222]	Y4	
BH31	VSS[223]	Y42	
BH33	VSS[224]	Y46	
BH35	VSS[225]	Y8	
BH39	VSS[226]	BG29	
BH43	VSS[227]	N24	
BH7	VSS[228]	AJ3	
D3	VSS[229]	AD47	
D12	VSS[230]	B43	
D16	VSS[231]	BE10	
D18	VSS[232]	BG41	
D22	VSS[233]	G14	
D24	VSS[234]	H16	
D26	VSS[235]	T36	
D30	VSS[236]	BG22	
D32	VSS[237]	BG24	
D34	VSS[238]	C22	
D38	VSS[239]	AP13	
D42	VSS[240]	M14	
D8	VSS[241]	AP3	
E18	VSS[242]	AP1	
E26	VSS[243]	BE16	
G18	VSS[244]	BC16	
G20	VSS[245]	BG28	
G26	VSS[246]	RJ28	
G28	VSS[247]		
G36	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

COUGARPOINT_FCBGA989-D
HM65@

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Date: Friday, February 10, 2012			Sheet 21 of 63	Rev C

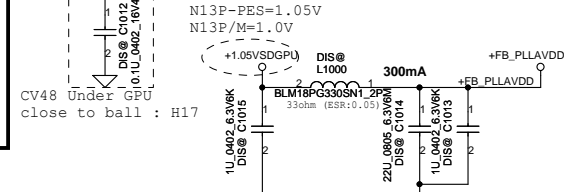
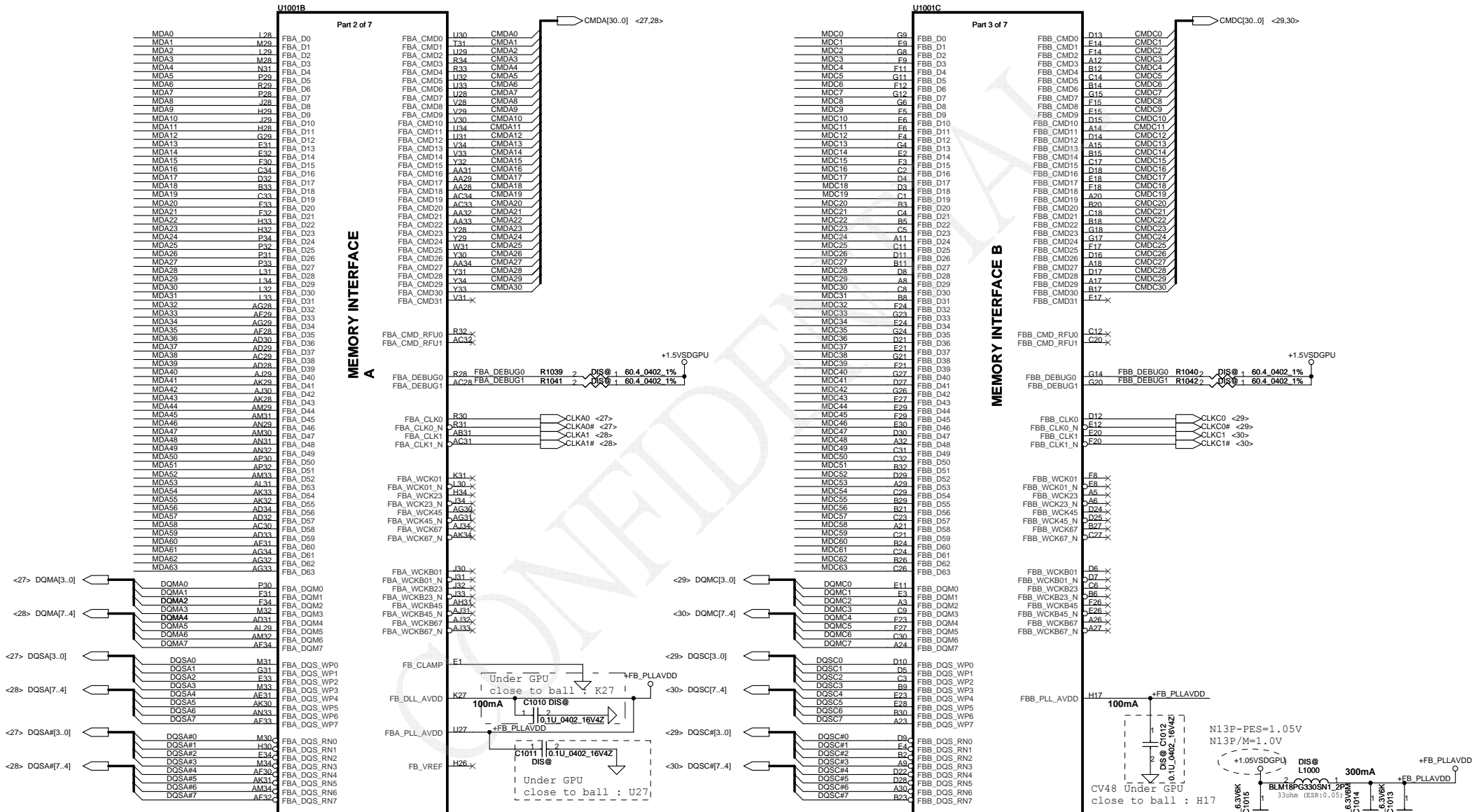
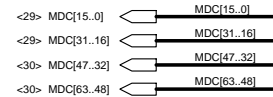
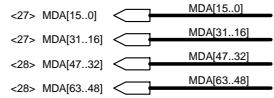


GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		



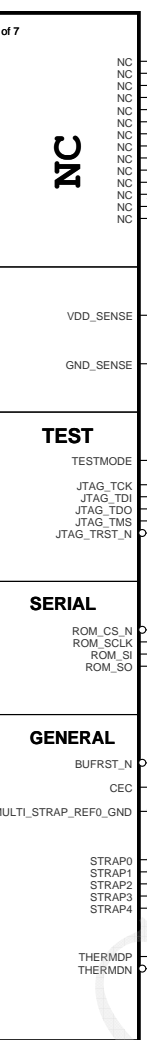
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VRAM Interface



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- U1001D
Part 4 of 7
- ×AM6 IFPA_TXC
 - ×AN6 IFPA_TXC_N
 - ×AP3 IFPA_TXD0
 - ×AN4 IFPA_TXD0_N
 - ×AM5 IFPA_TXD1
 - ×AL6 IFPA_TXD2
 - ×AG6 IFPA_TXD2_N
 - ×A16 IFPA_TXD3
 - ×AH6 IFPA_TXD3_N
 - ×A10 IFPB_TXC
 - ×AH9 IFPB_TXC_N
 - ×AP6 IFPB_TXD4
 - ×AM7 IFPB_TXD4_N
 - ×AL7 IFPB_TXD5
 - ×AN8 IFPB_TXD5_N
 - ×AM8 IFPB_TXD6
 - ×AG8 IFPB_TXD7
 - ×AL8 IFPB_TXD7_N
 - ×AK1 IFPC_L0
 - ×AJ1 IFPC_L0_N
 - ×A13 IFPC_L1
 - ×AJ2 IFPC_L1_N
 - ×AH3 IFPC_L2
 - ×AJ4 IFPC_L2_N
 - ×AG5 IFPC_L3
 - ×AG4 IFPC_L3_N
 - ×AM1 IFPD_L0
 - ×AM2 IFPD_L0_N
 - ×AM3 IFPD_L1
 - ×AJ4 IFPD_L1_N
 - ×AL3 IFPD_L2
 - ×AL4 IFPD_L2_N
 - ×AK4 IFPD_L3
 - ×AK5 IFPD_L3_N
 - ×AD2 IFPE_L0
 - ×AD3 IFPE_L0_N
 - ×AD1 IFPE_L1
 - ×AC1 IFPE_L1_N
 - ×AC2 IFPE_L2
 - ×AC3 IFPE_L2_N
 - ×AG4 IFPE_L3
 - ×AC5 IFPE_L3_N
 - ×AE3 IFPF_L0
 - ×AE4 IFPF_L0_N
 - ×AE5 IFPF_L1
 - ×AD4 IFPF_L1_N
 - ×AD5 IFPF_L2
 - ×AG1 IFPF_L2_N
 - ×AE1 IFPF_L3
 - ×AE2 IFPF_L3_N
 - ×AG3 IFPC_AUX_I2CW_SCL
 - ×AG2 IFPC_AUX_I2CW_SDA_N
 - ×AK3 IFPD_AUX_I2CX_SCL
 - ×AK2 IFPD_AUX_I2CX_SDA_N
 - ×AB3 IFPE_AUX_I2CY_SCL
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 - ×AE3 IFPF_AUX_I2C_SCL
 - ×AE2 IFPF_AUX_I2C_SDA_N



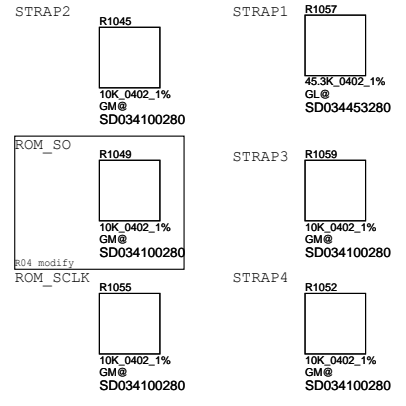
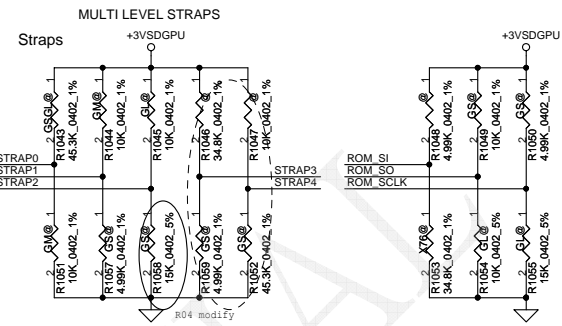
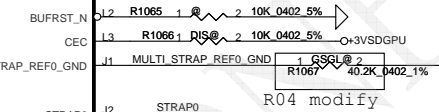
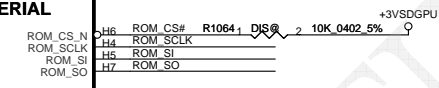
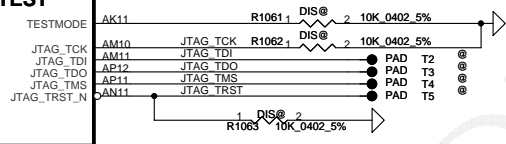
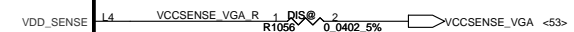
NC

TEST

SERIAL

GENERAL

LVDS/TMDS



For N13P-GS(QS) strap table (PN:SA000051880)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL(QS) strap table (PN:SA000051A00)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

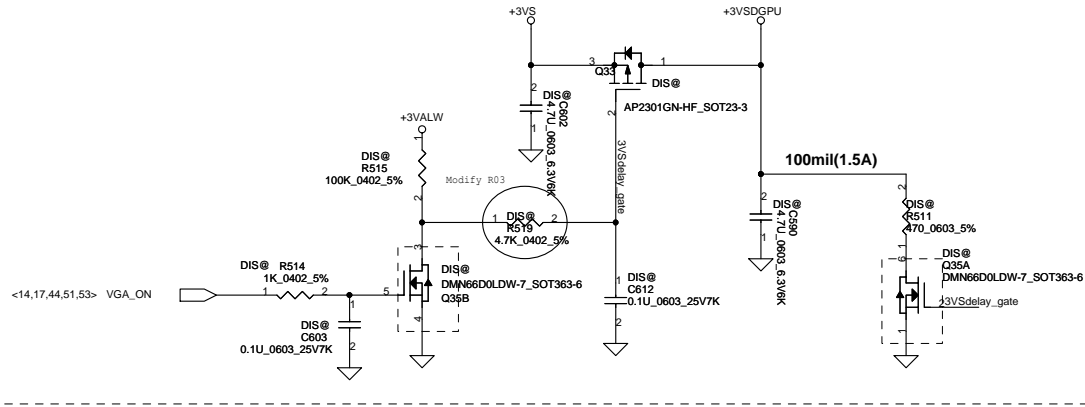
For N13M-GS(QS) strap table (PN:SA000051A00)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

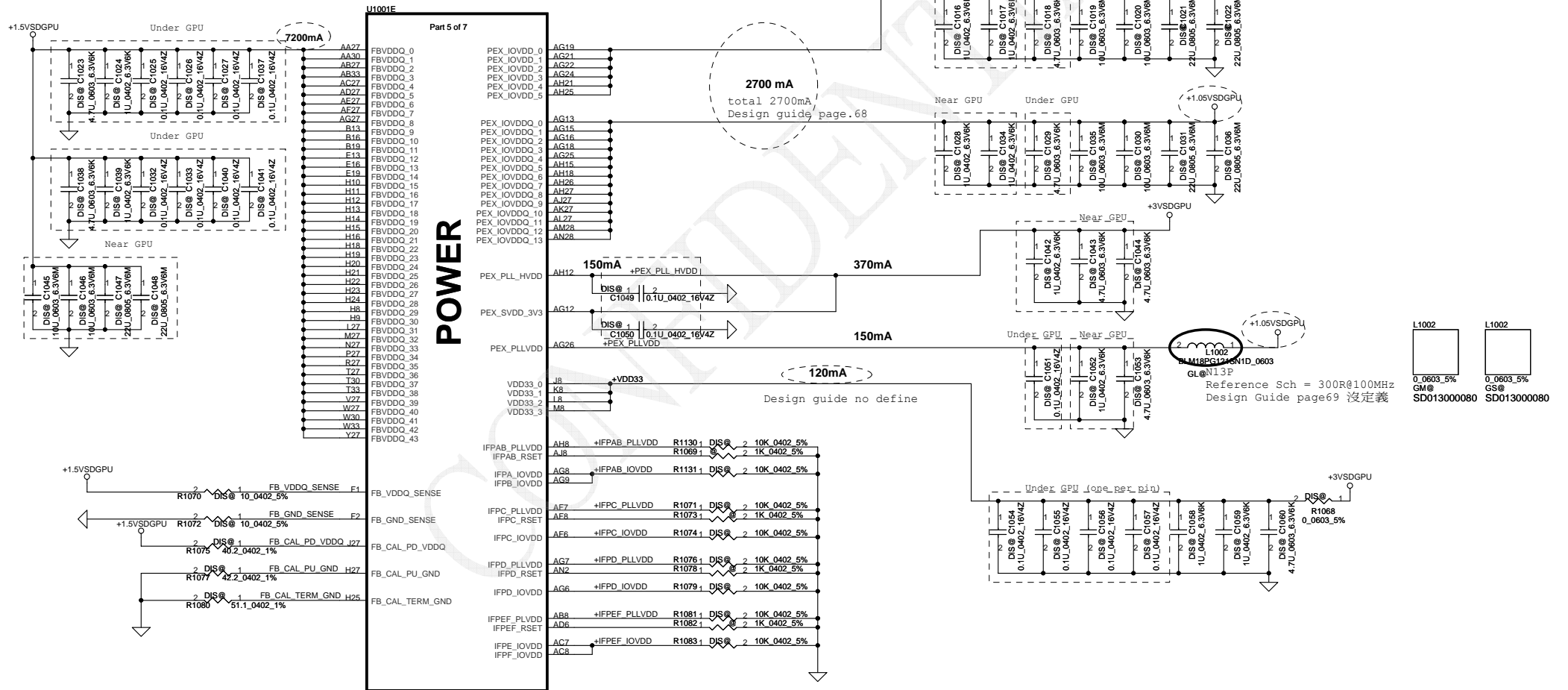
N13P-PES-A1_FCBGA908
GF108@

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Date:	Friday, February 10, 2012	Sheet	24	of	63

+3VS to +3VSDGPU for GPU

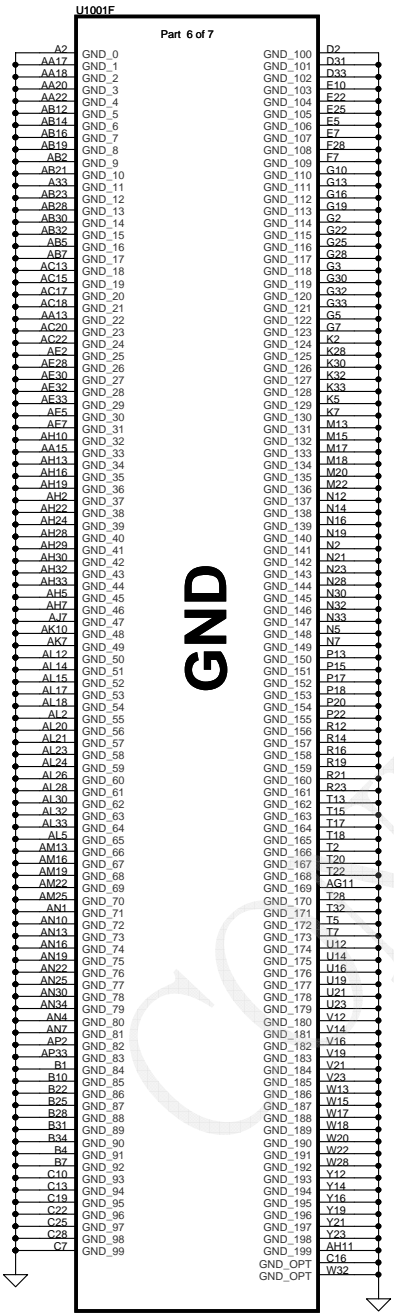


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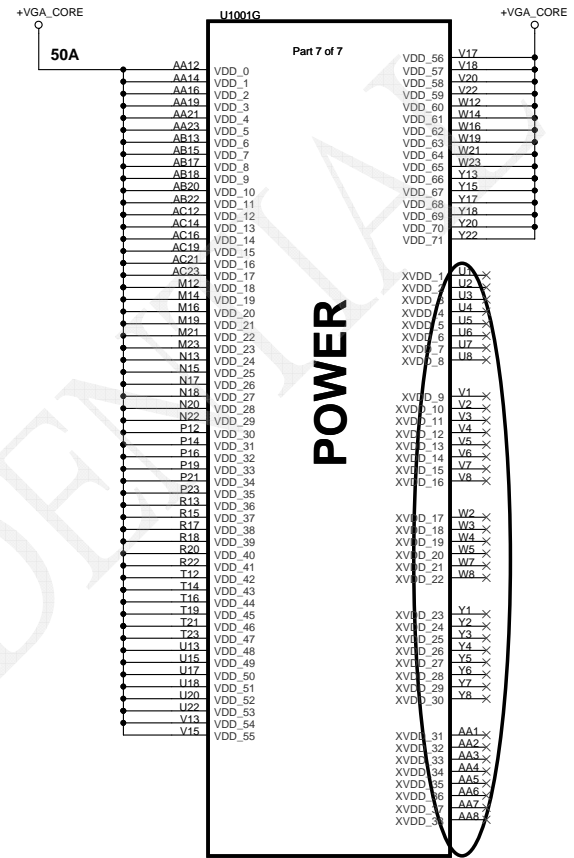


N13P-PES-A1_FCBGA908
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				4019ID	C
				Date: Friday, February 10, 2012	Sheet 25 of 63



N13P-PES-A1_FCBGA908
GF108@



N13P-PES-A1_FCBGA908
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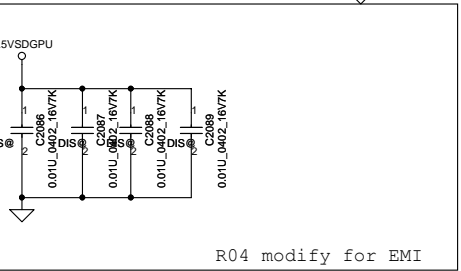
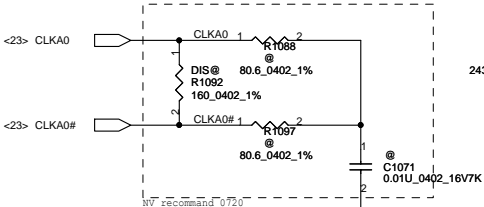
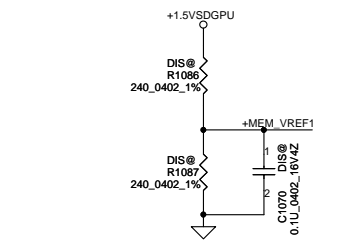
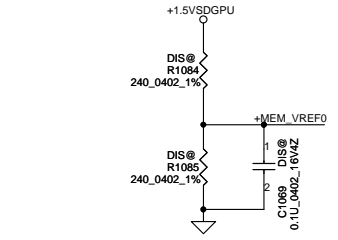
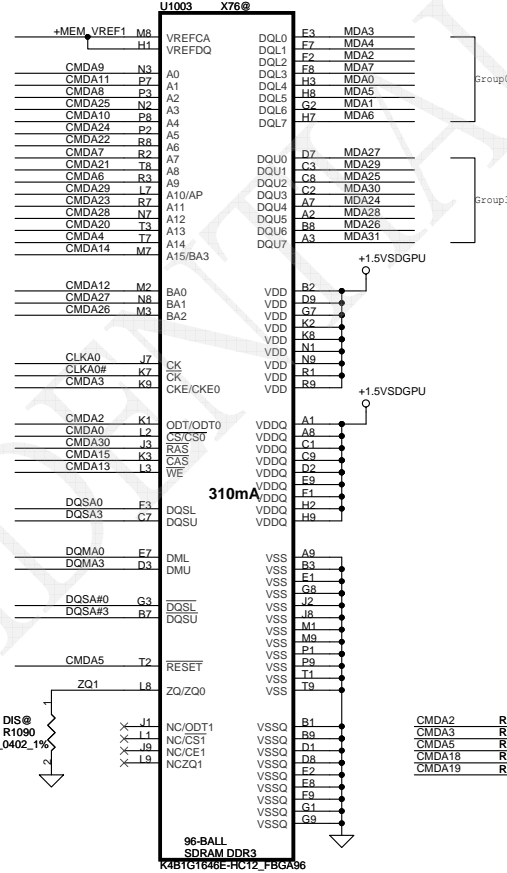
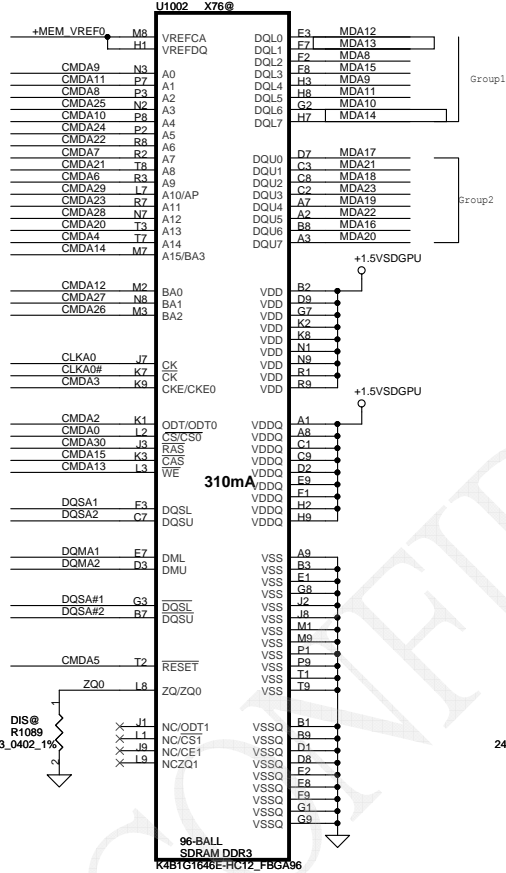
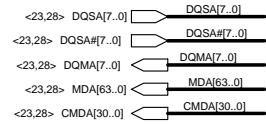
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Revision	1	Customer	4019ID	Date	Friday, February 10, 2012
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VRAM DDR3 chips (1GB)

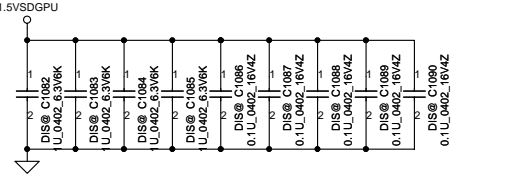
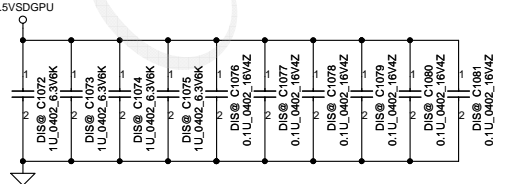
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

R02 modify
Swap MDA13 and MDA14



R04 modify for EMI



Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination

Hynix : SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA)
Hynix : SA000041S40 (S IC D3 64Mx16 H5TQ1G63DFR-11C FBGA)

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Date: Friday, February 10, 2012				Sheet 27 of 63

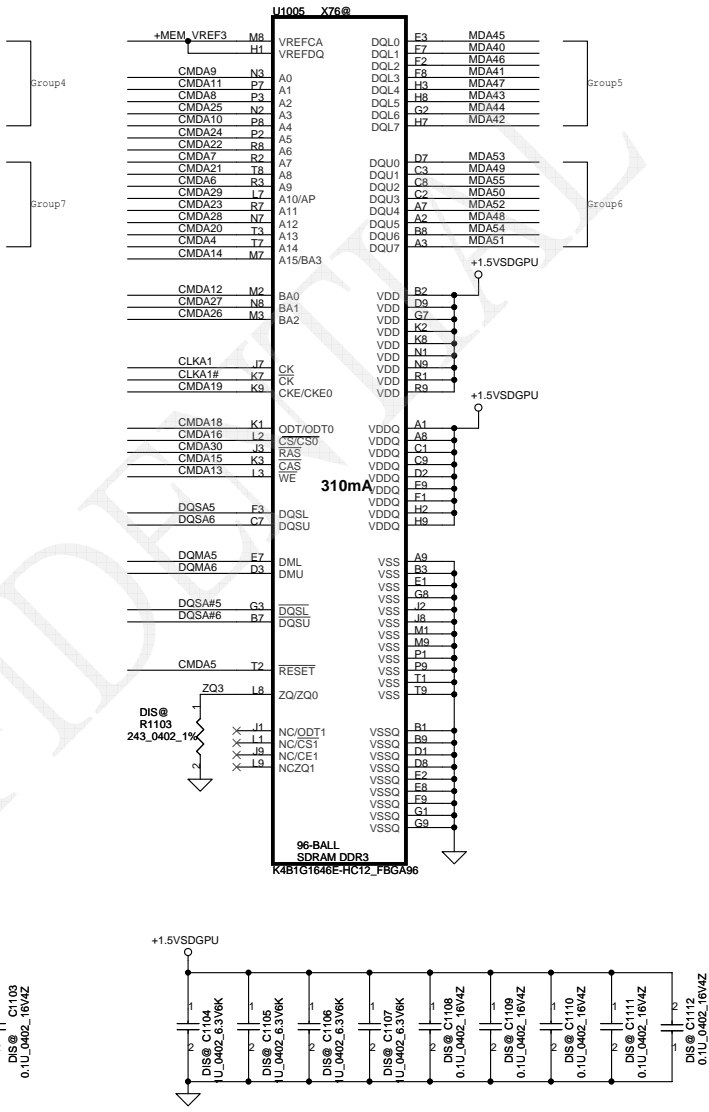
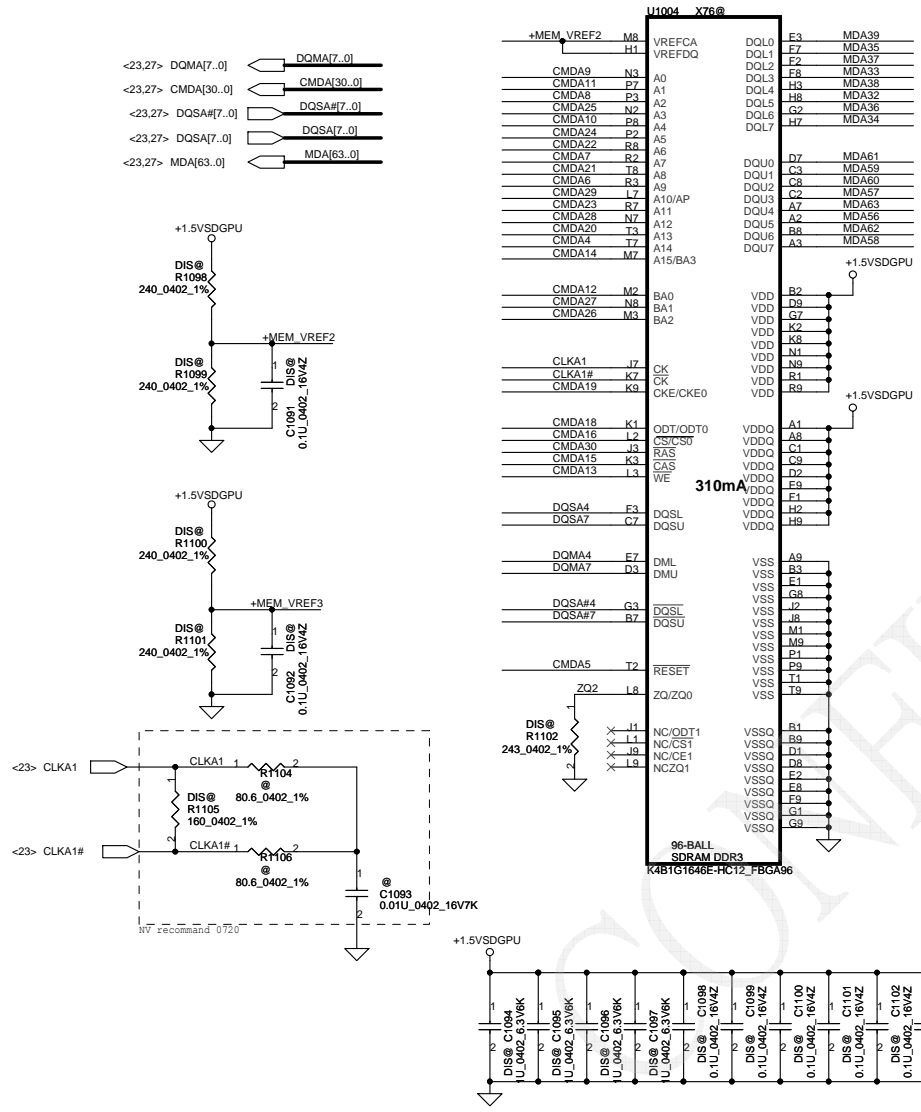
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

Not Available LOW HIGH



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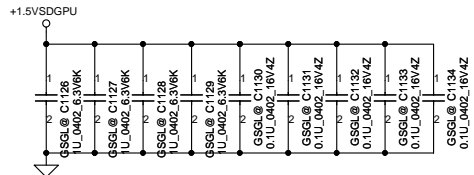
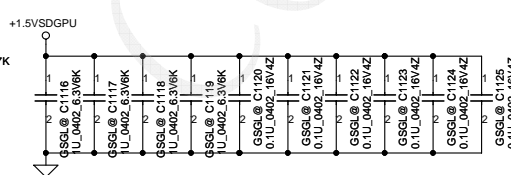
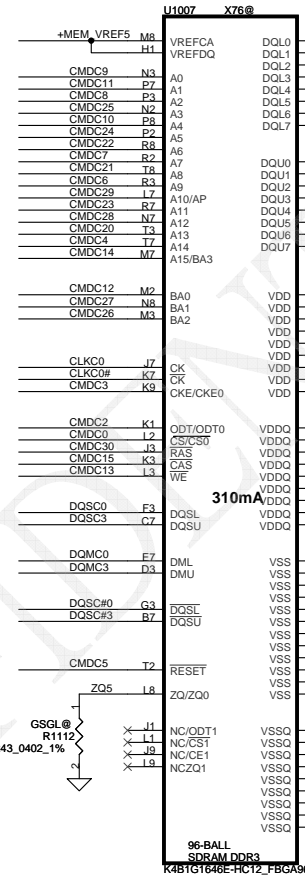
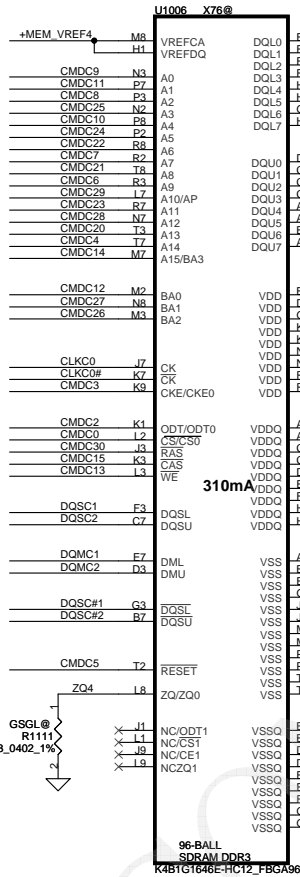
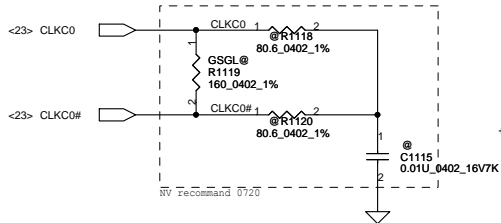
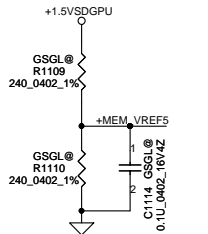
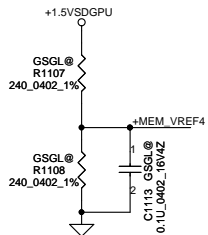
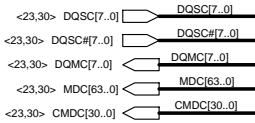
Compal Electronics, Inc.	
Title	SCHEMATIC, MB A7912
Document Number	40191D
Date	Friday, February 10, 2012
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Rev C

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

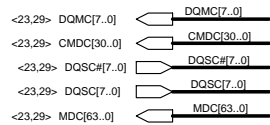
Command Bit	Default Full-down
ODT#	10k
CKE#	10k
RST	10k
C#*	No Termination

Security Classification Issued Date: 2011/06/02 Deciphered Date: 2012/06/02	Compal Secret Data	Title: SCHEMATIC, MB A7912 Document Number: 40191D Date: Friday, February 10, 2012
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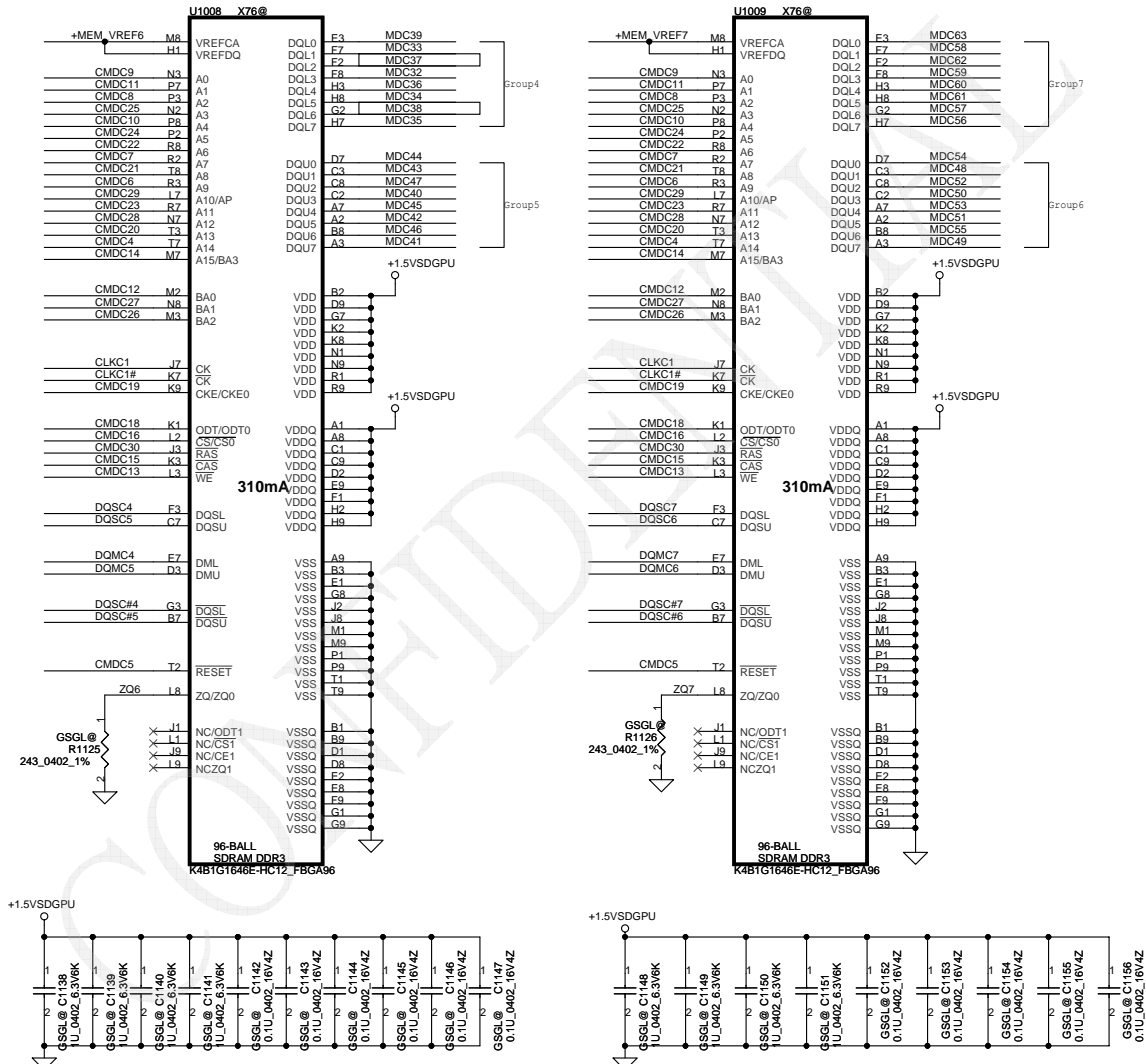
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

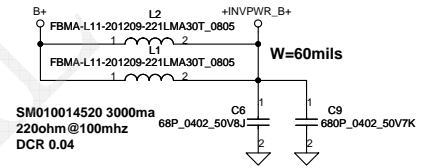
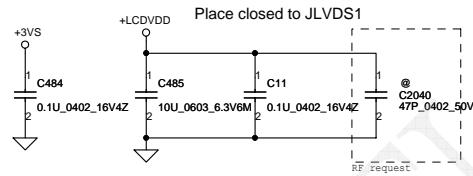
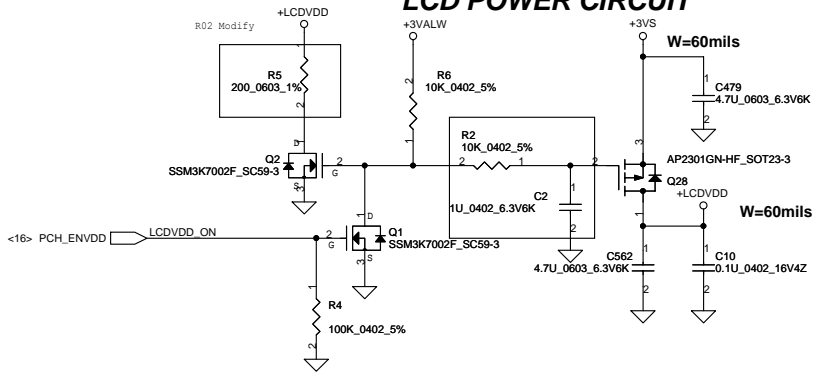


R02 modify
Swap MDC37 and MDC38

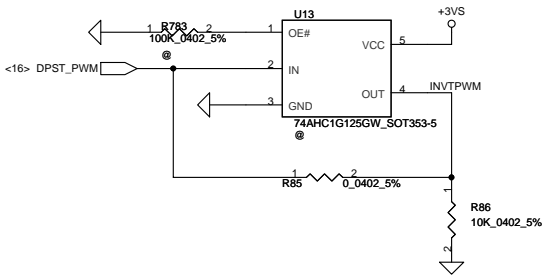
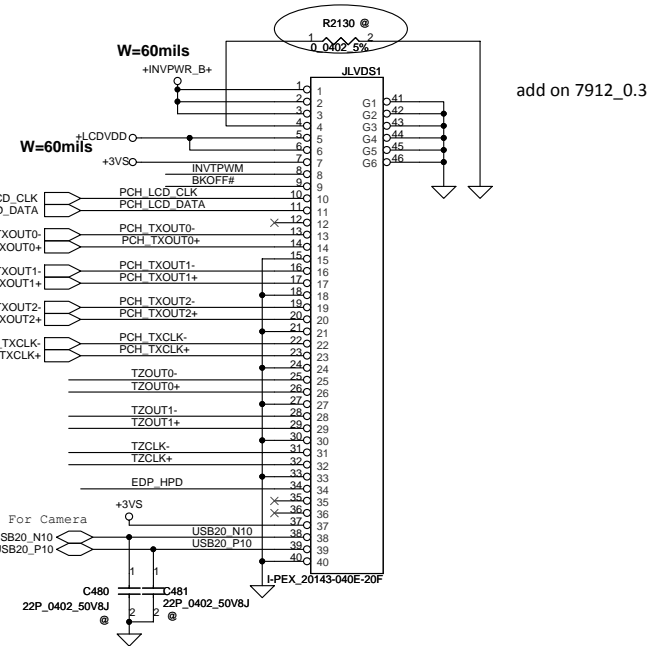


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

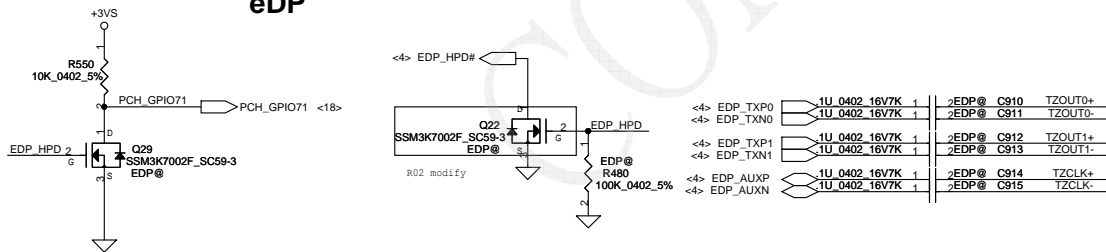
LCD POWER CIRCUIT



LCD/LED PANEL Conn.

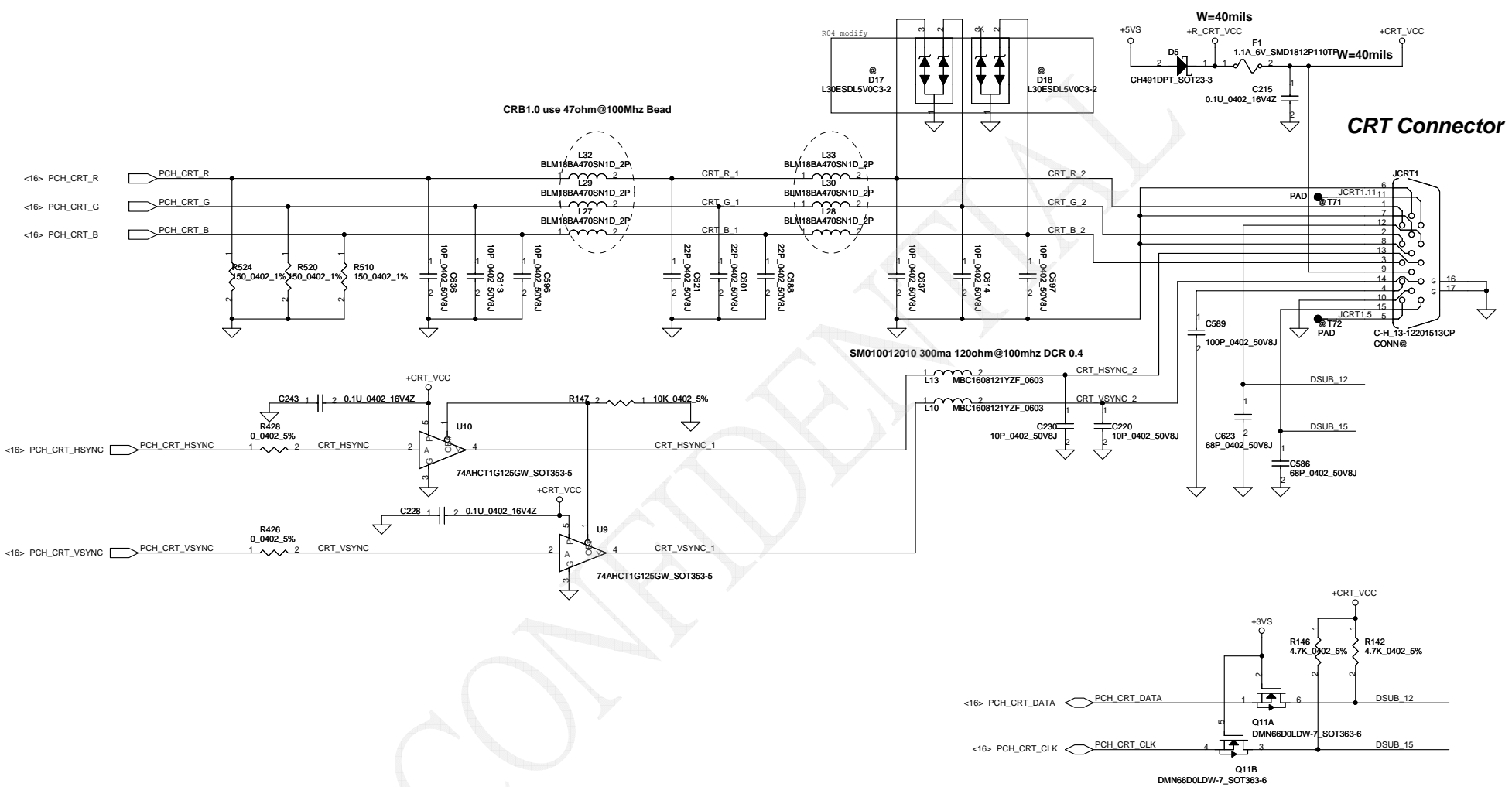


eDP

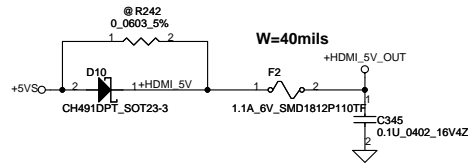


	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1

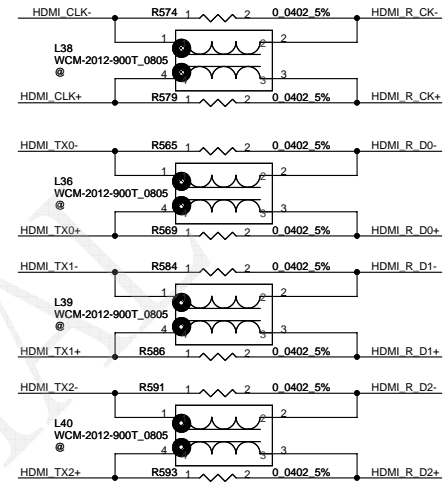
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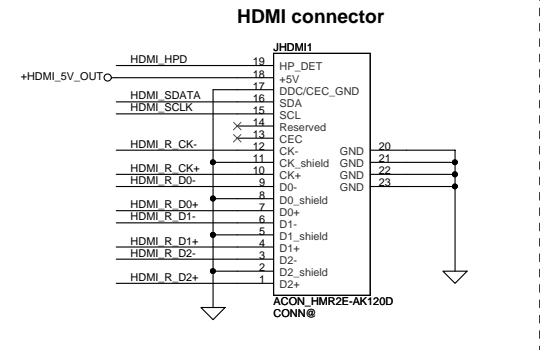
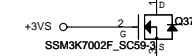
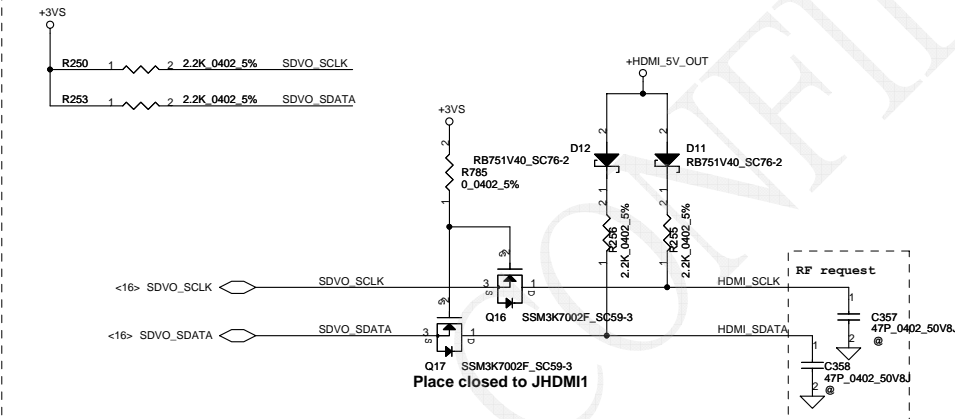
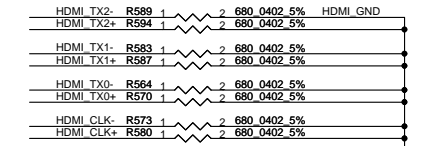
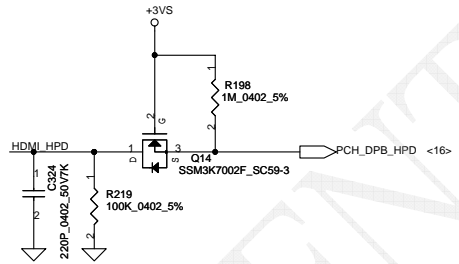
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Date: Friday, February 10, 2012				Sheet	32 of 63



SM070001310 400ma 90ohm@100mhz DCR 0.3



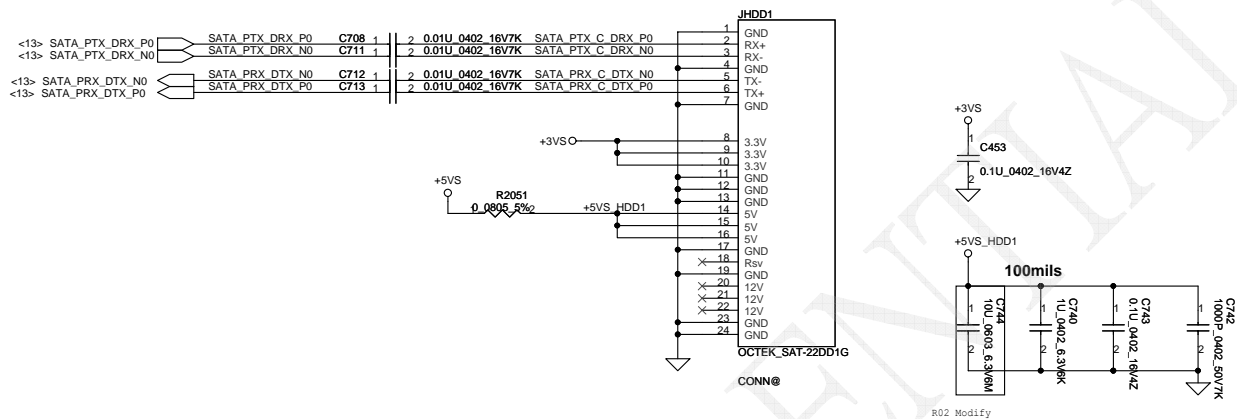
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<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+



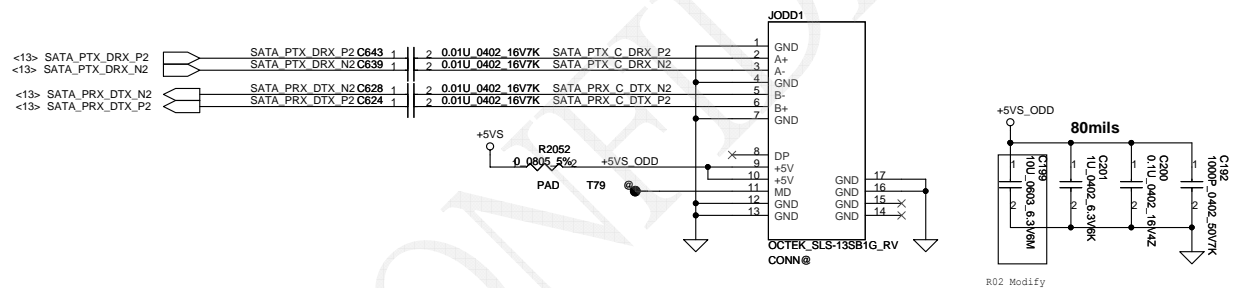
Security Classification	Compal Secret Data		Title	Schematics, MB A7912	
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SATA HDD1 Conn.

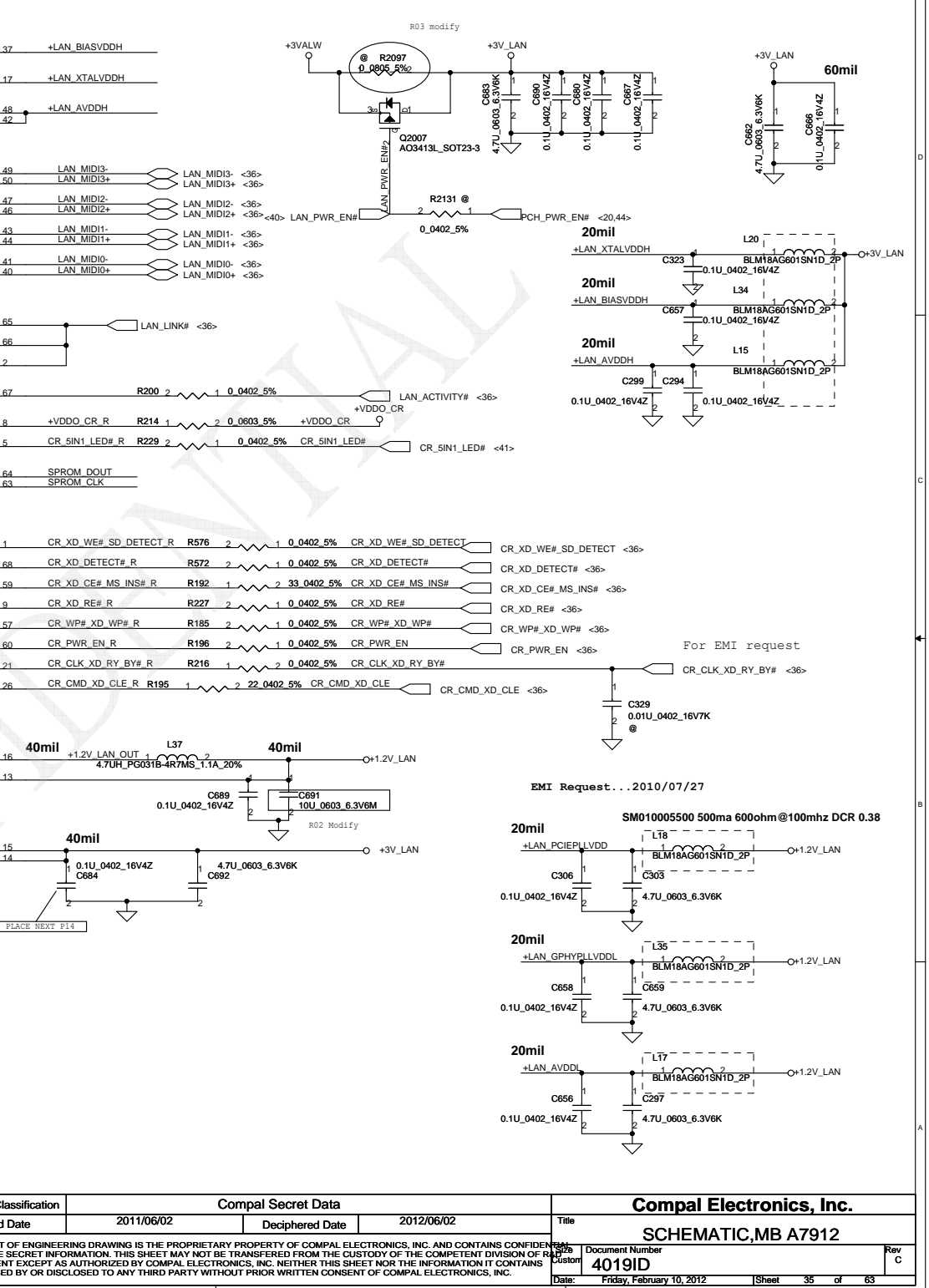
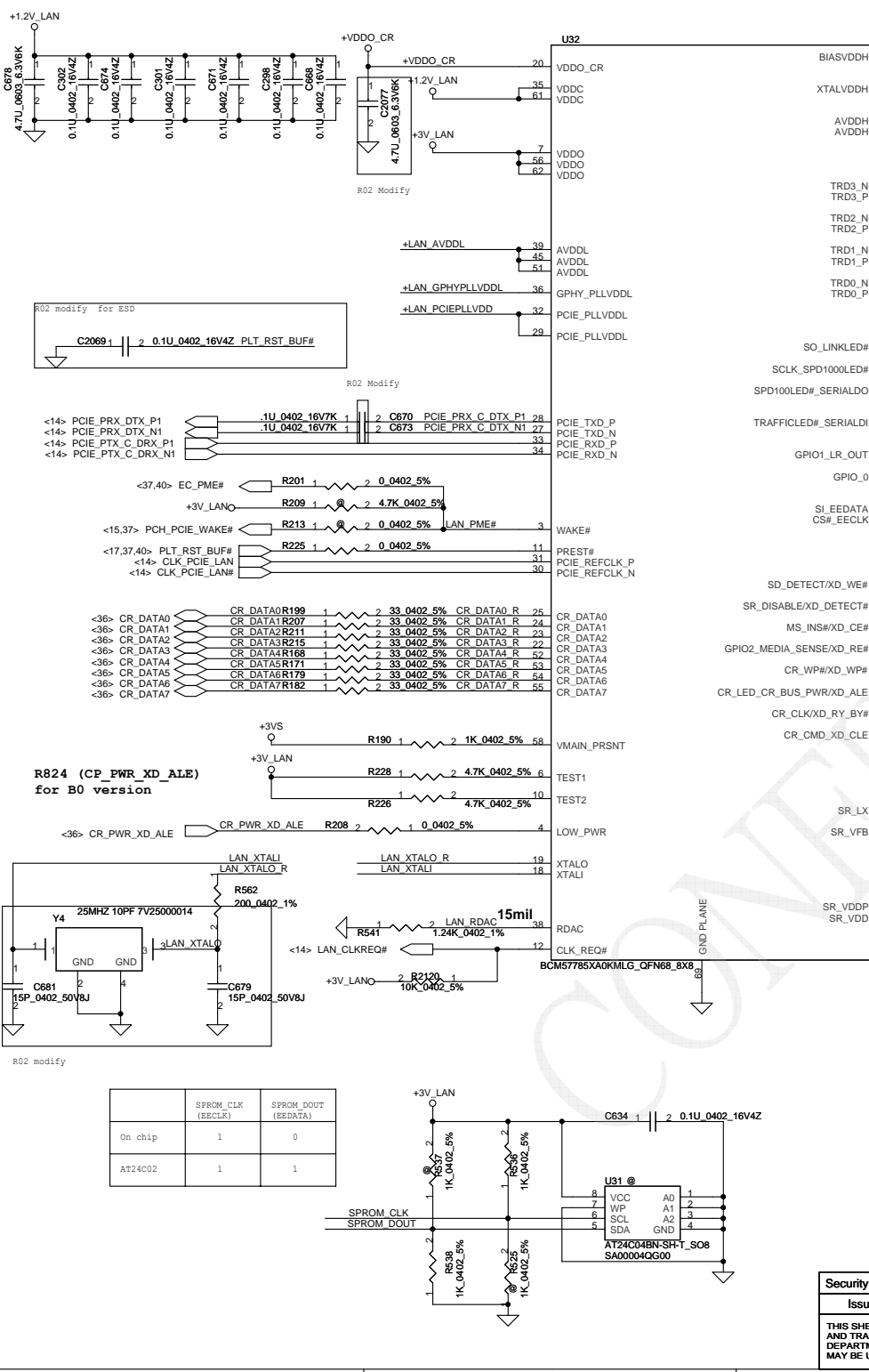
CL 4.0 mm



SATA ODD Conn.



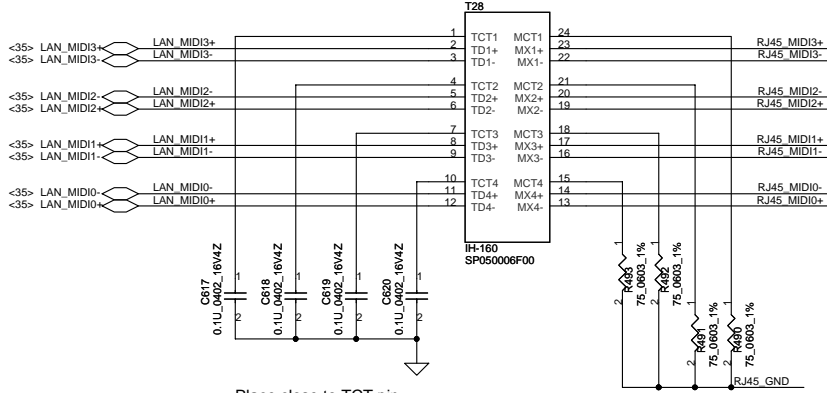
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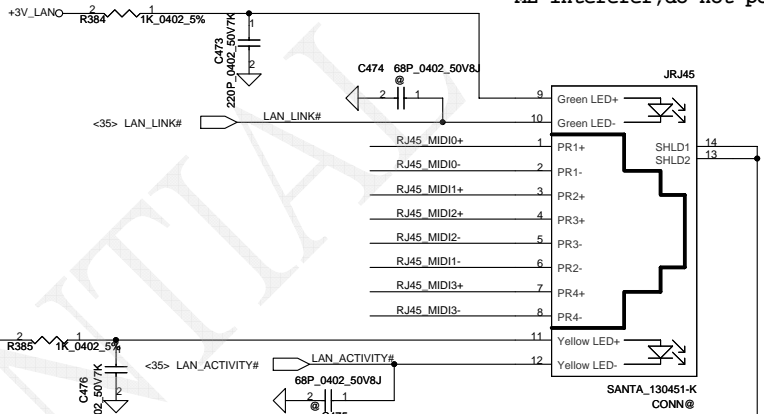
LAN Connector

C474, C475 and D14
ME interfere, do not pop!!

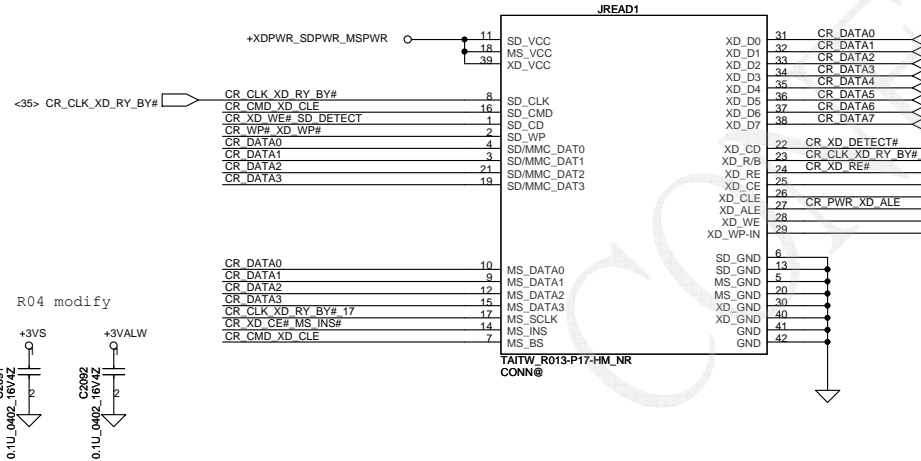


Place close to TCT pin

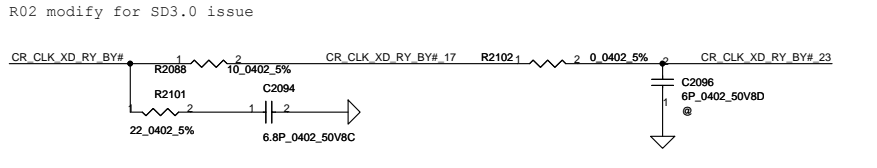
BOTH HAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN , SP050006F00



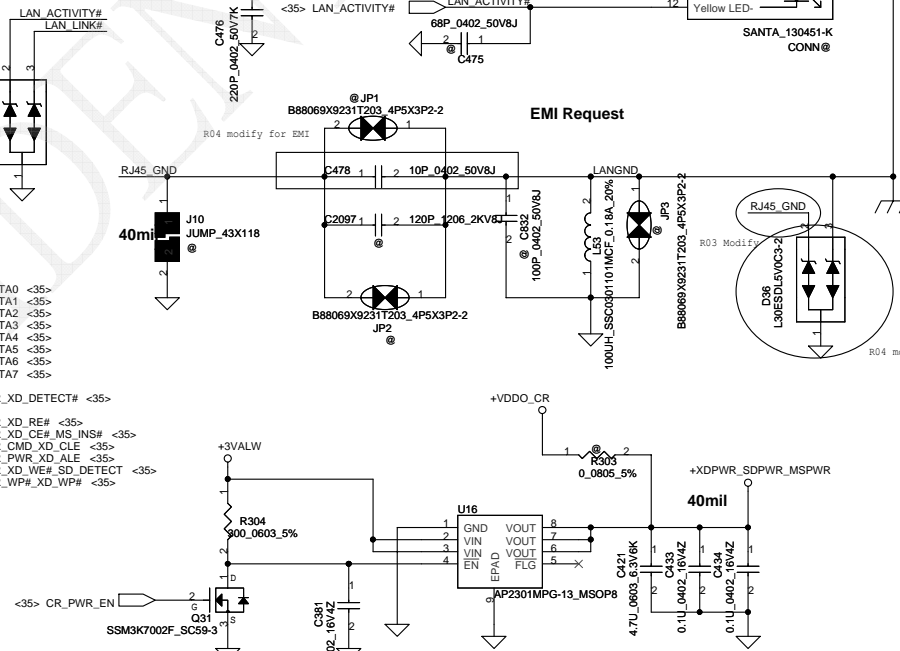
Card Reader Connector



R04 modify

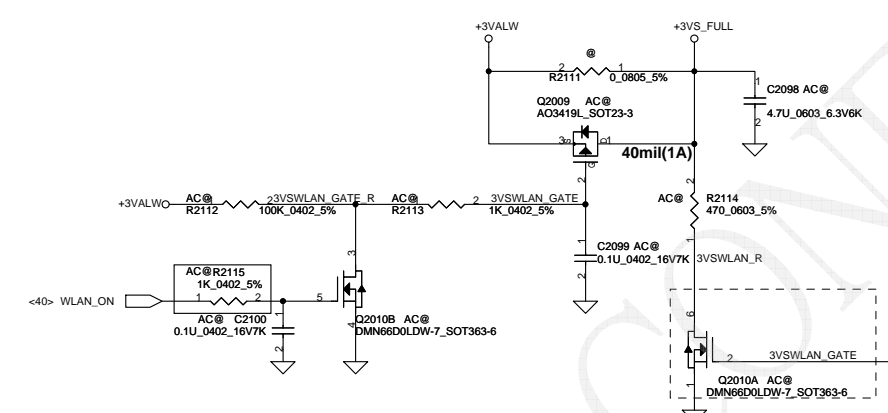
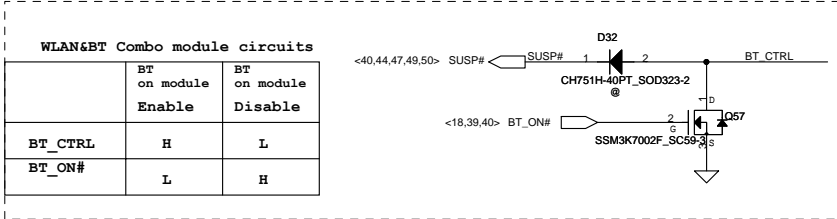
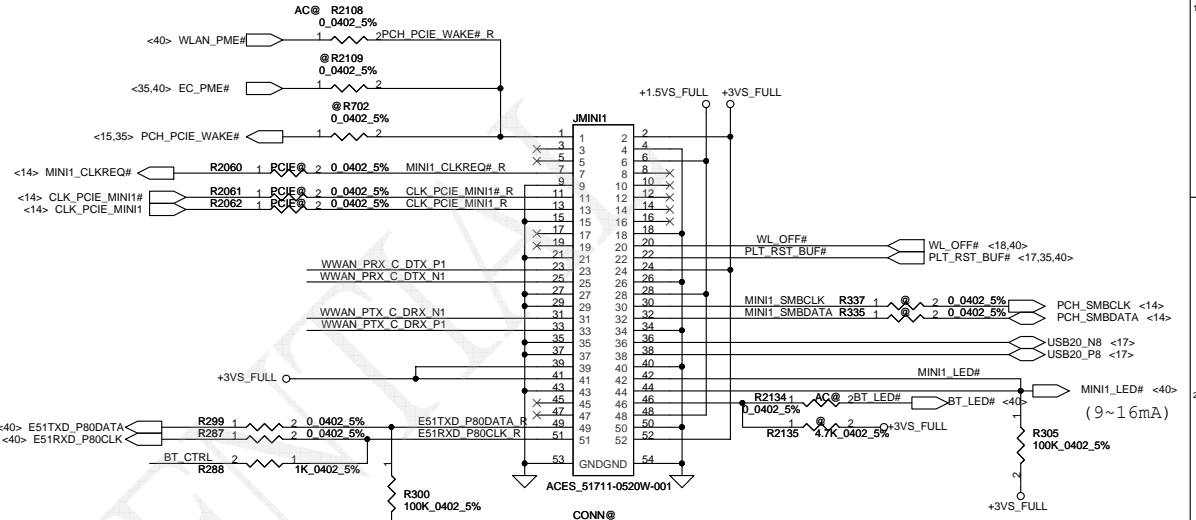
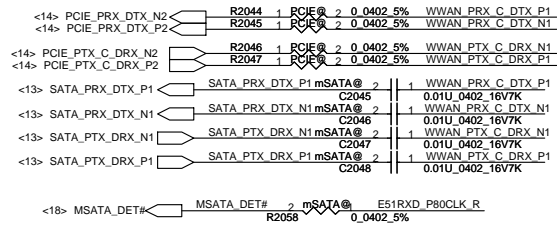
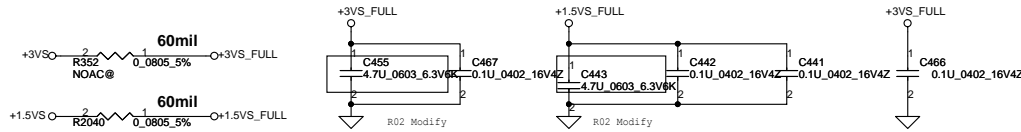


R02 modify for SD3.0 issue



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For Wireless LAN or MSATA

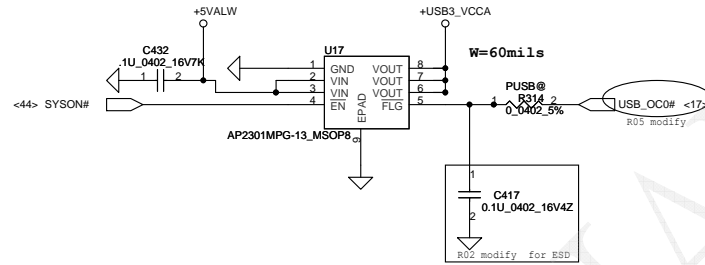
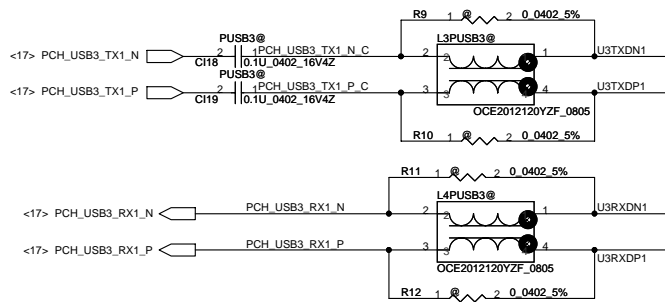


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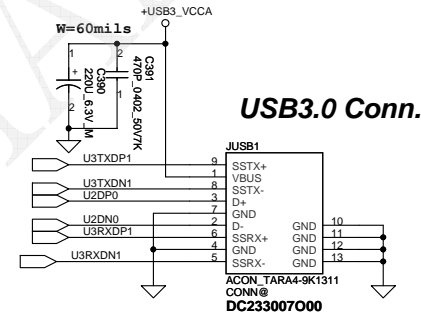
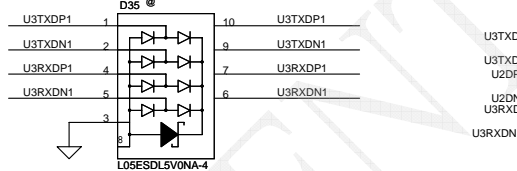
CONFIDENTIAL

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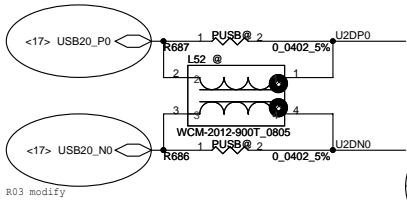
Default use PCH side USB3.0 signal



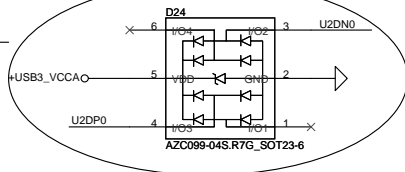
For ESD request



USB3.0 Conn.

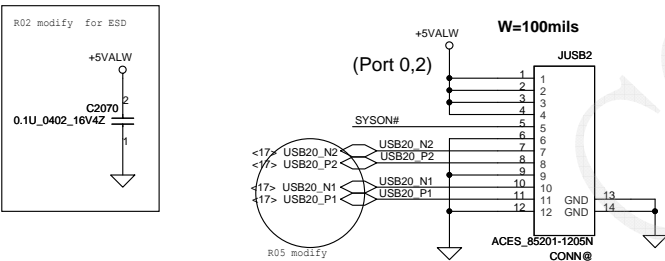


For USB2.0 ESD request

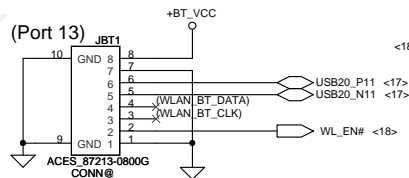


R04 modify

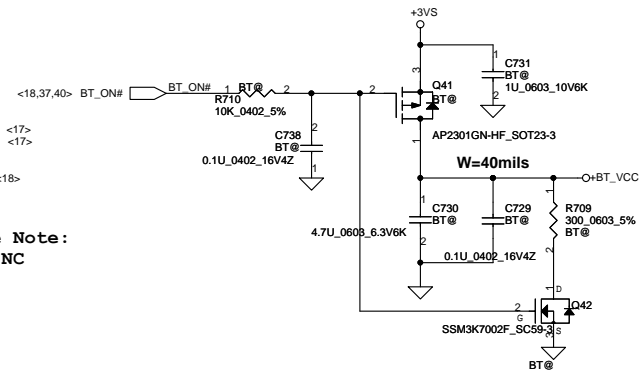
USB/B Conn.



BT Conn.



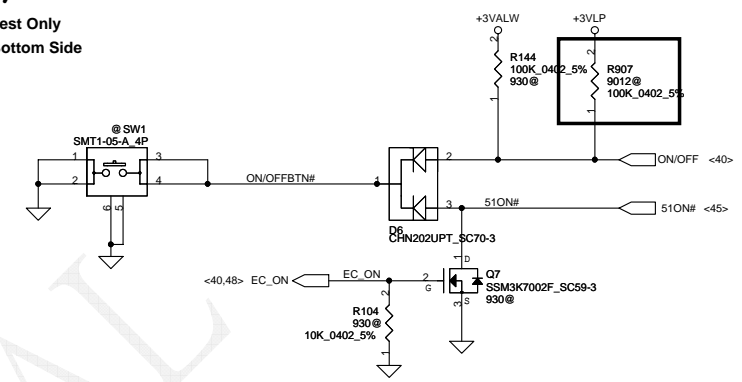
BT Wire Cable Note:
Pin 3, Pin 4 NC



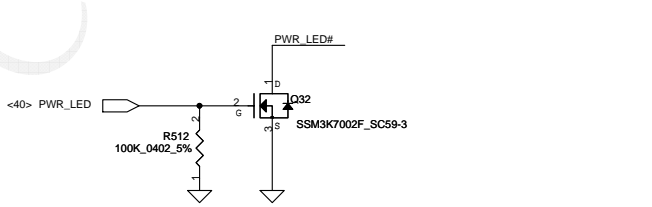
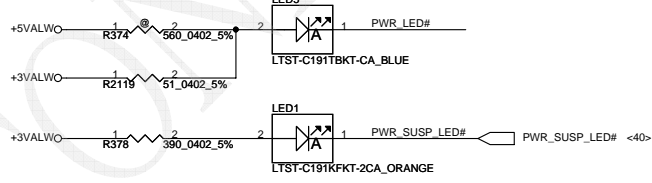
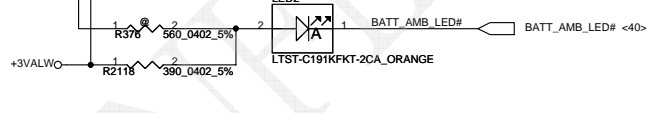
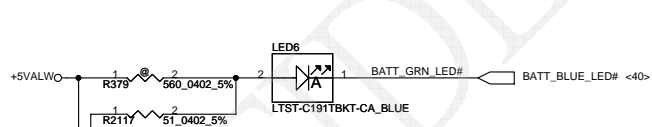
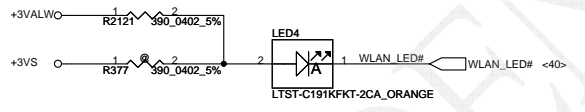
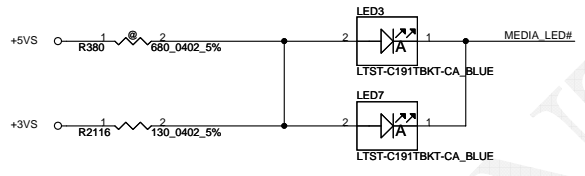
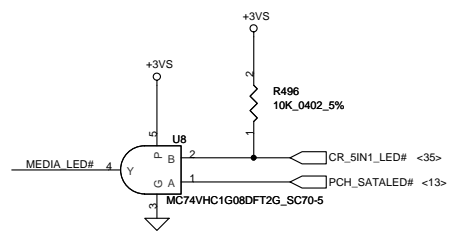
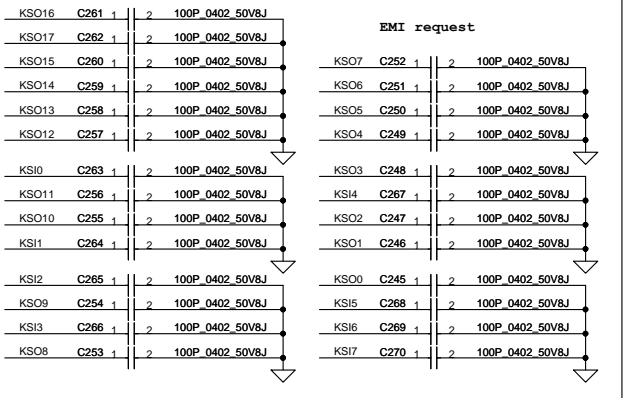
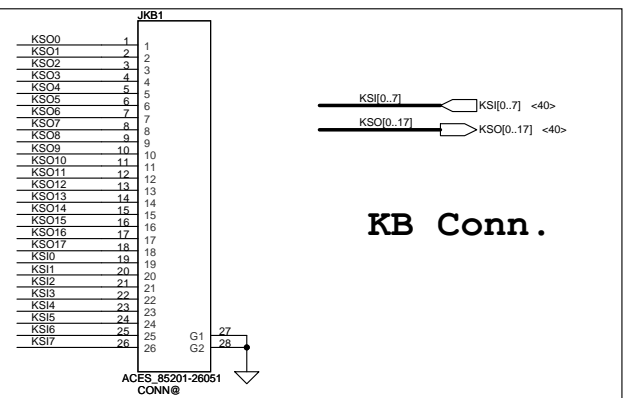
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ON/OFF BTN

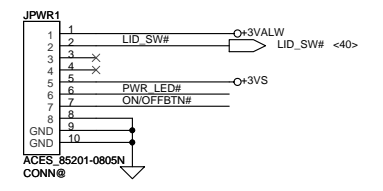
Test Only
Bottom Side



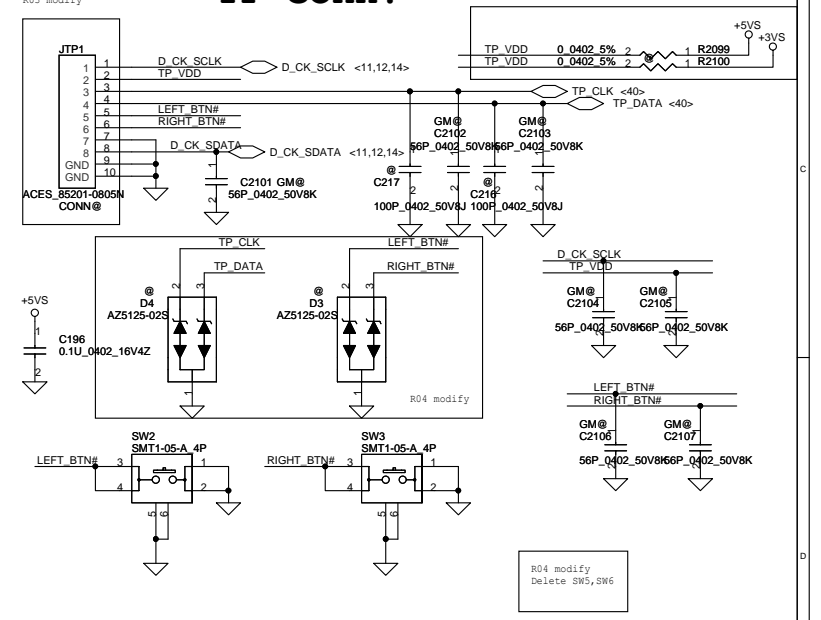
KB Conn.



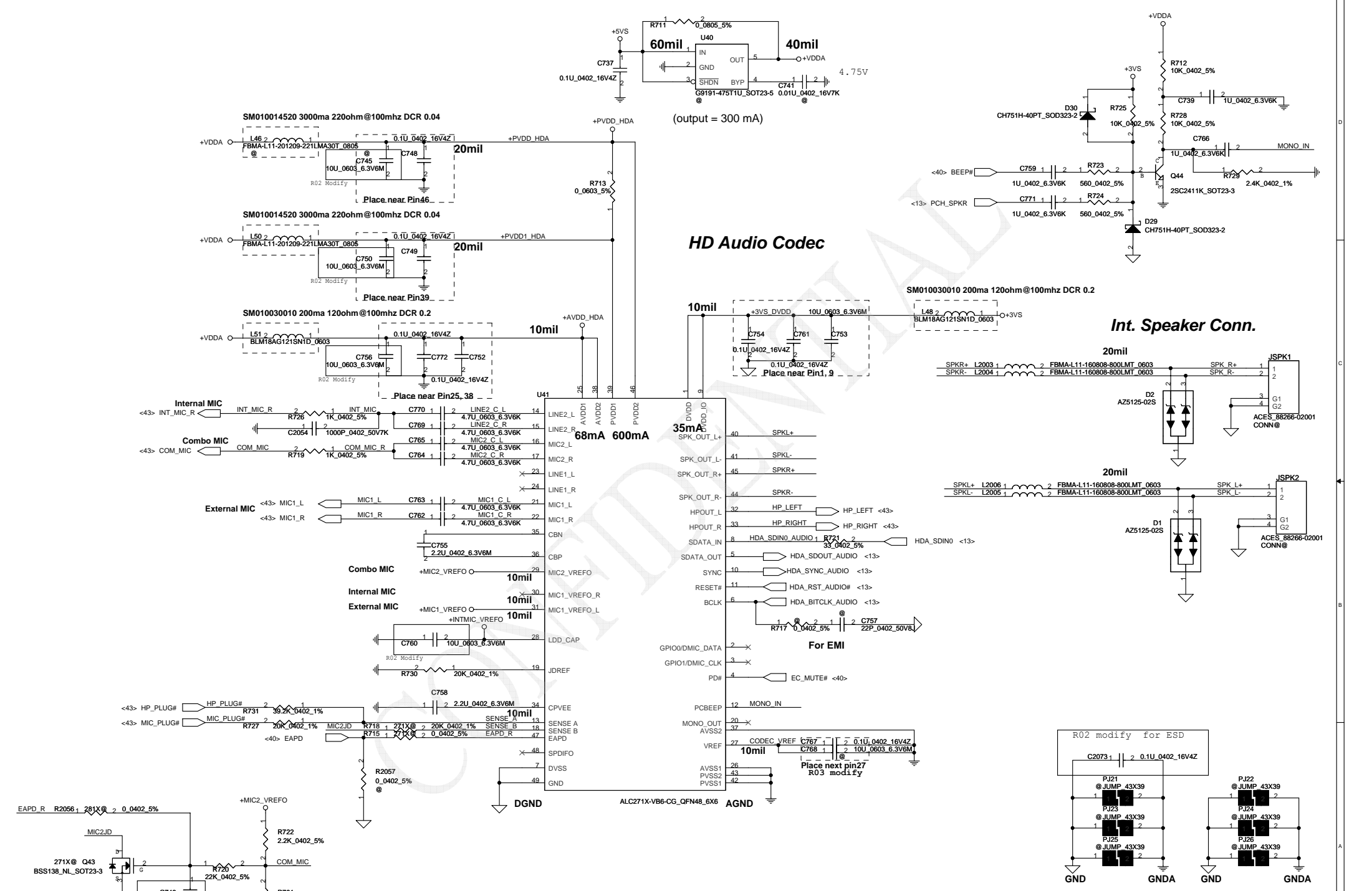
PWR/B



TP Conn.



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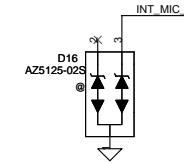
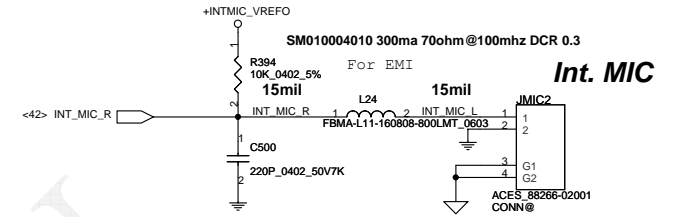
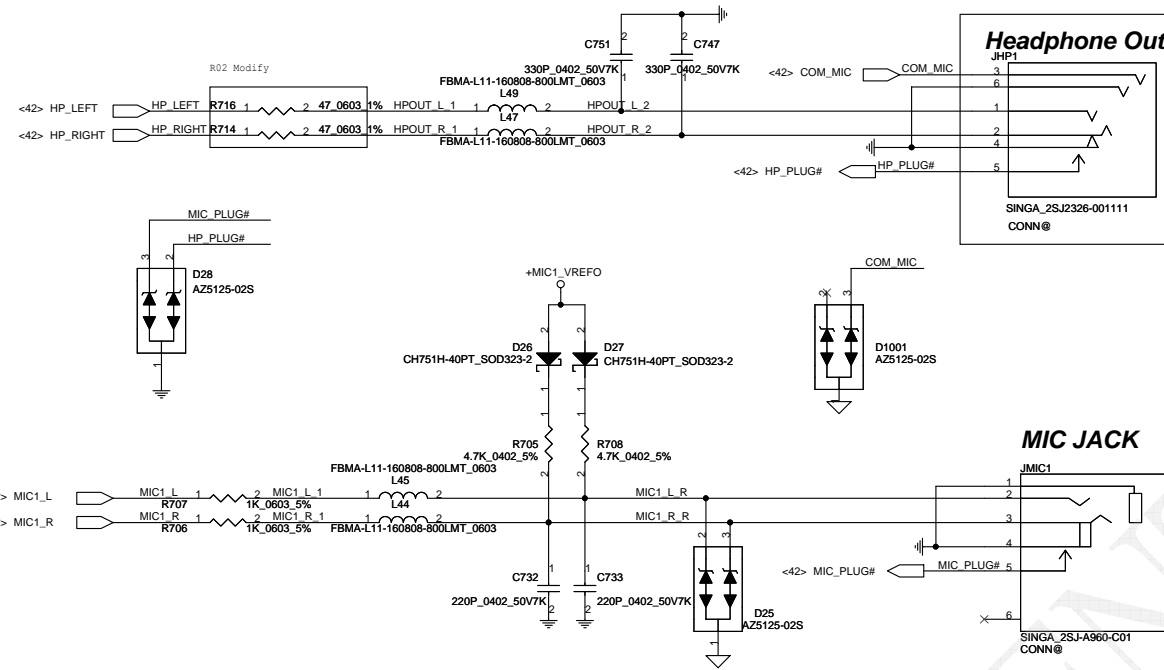
HD Audio Codec

Int. Speaker Conn.

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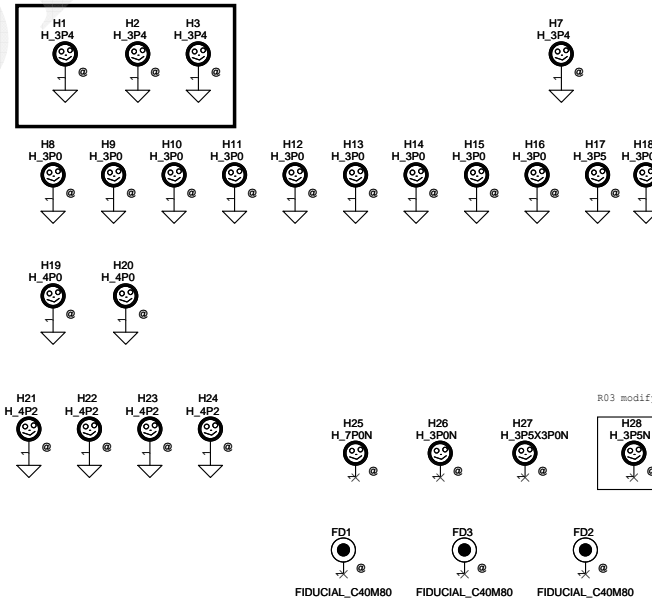
Compal Electronics, Inc.	
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Singatron 2SJ2326
DC021007151

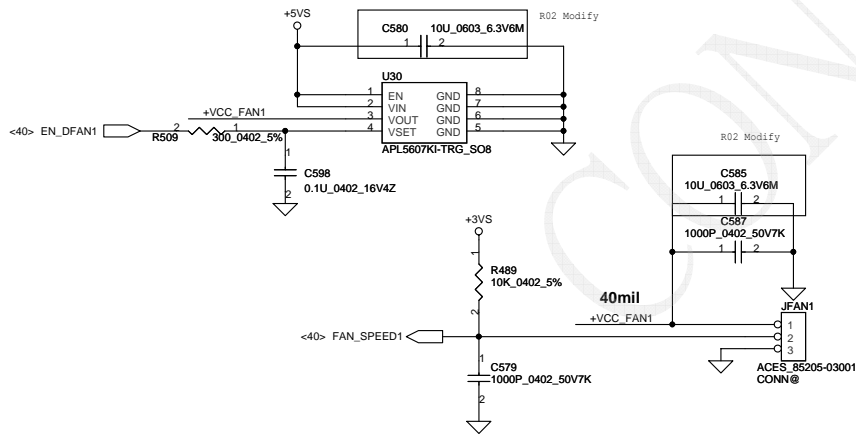


FAN Stand-Off

USB3 Stand-Off

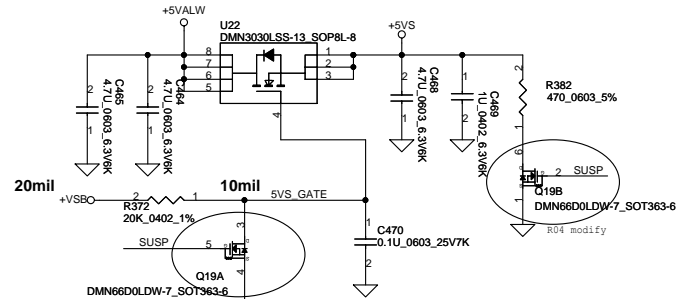


FAN1 Conn

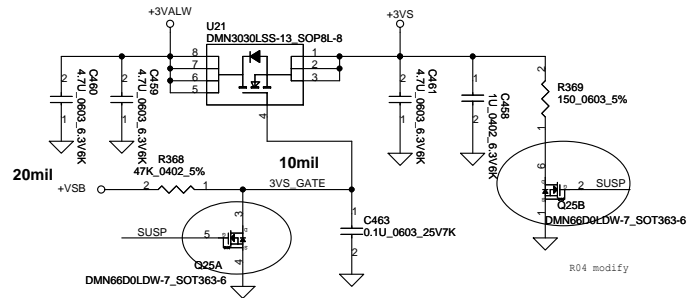


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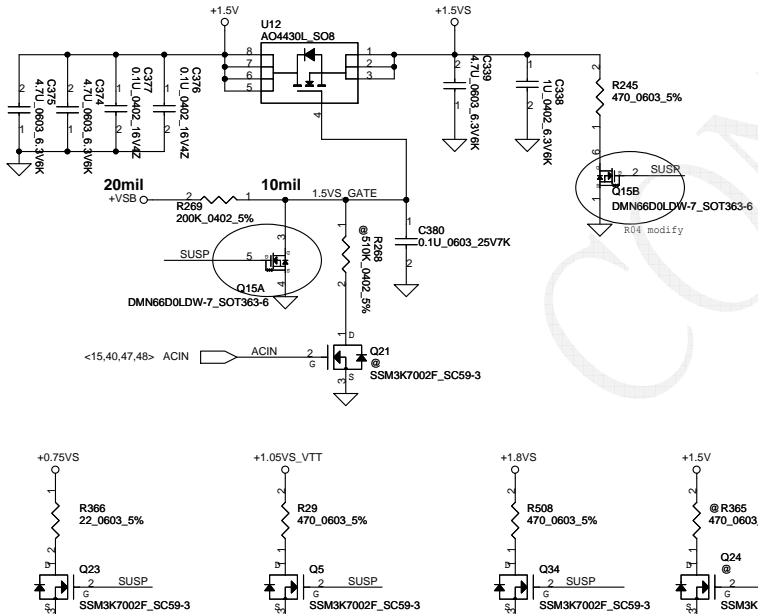
+5VALW TO +5VS



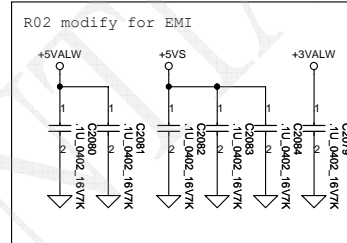
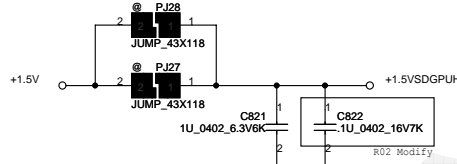
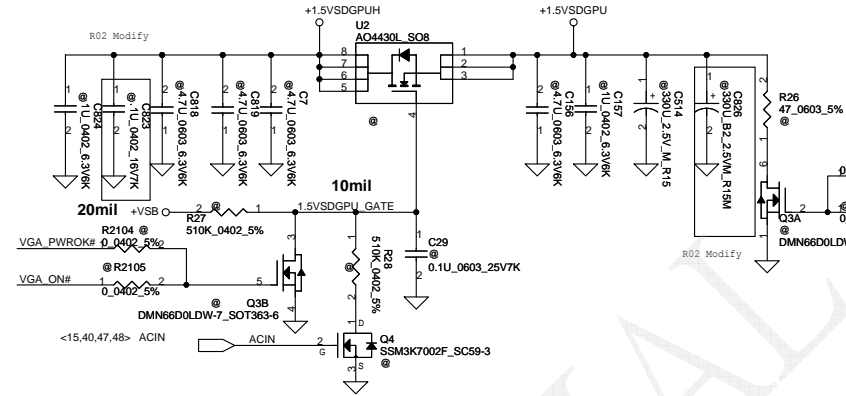
+3VALW TO +3VS



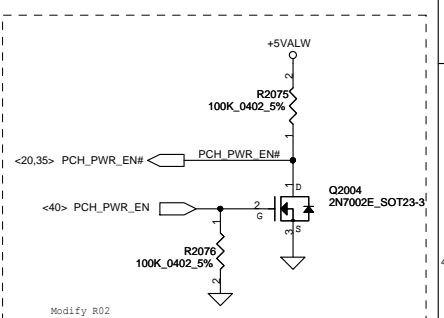
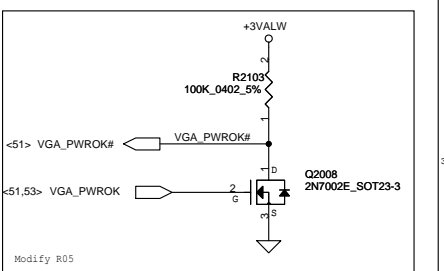
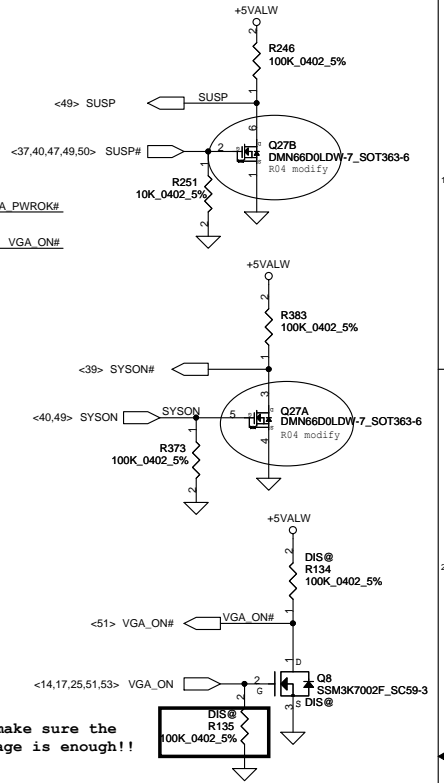
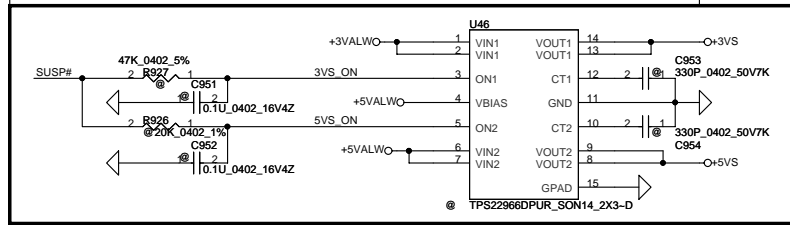
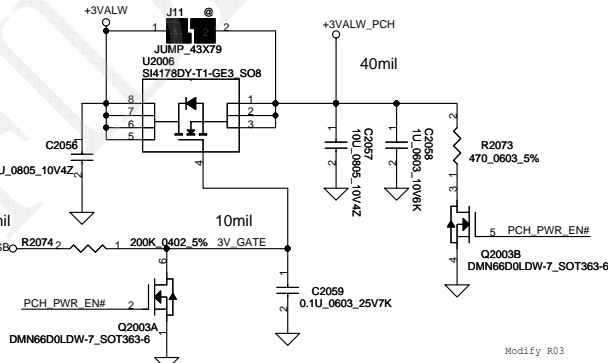
+1.5V to +1.5VS



+1.5VSDGPU to +1.5VSDGPU for GPU



+3VALW TO +3VALW(PCH AUX Power)



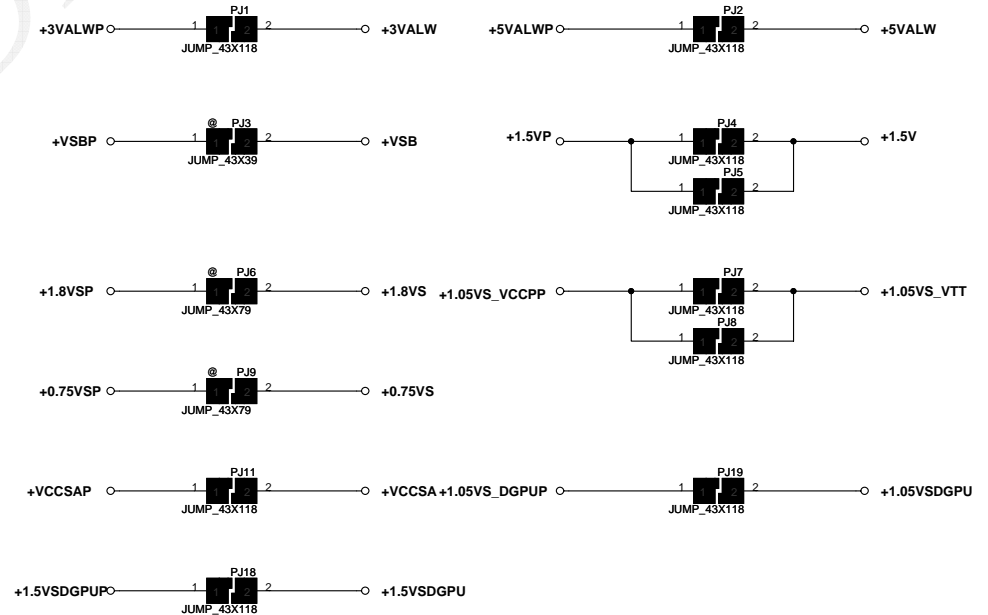
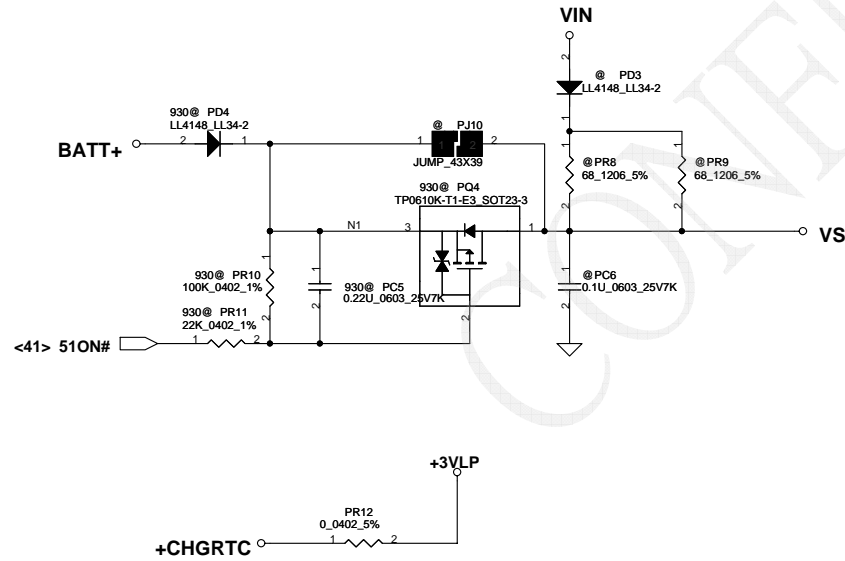
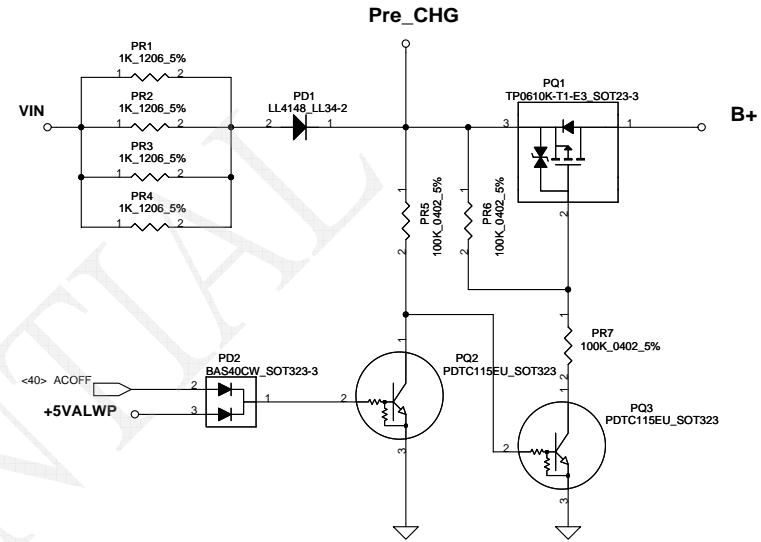
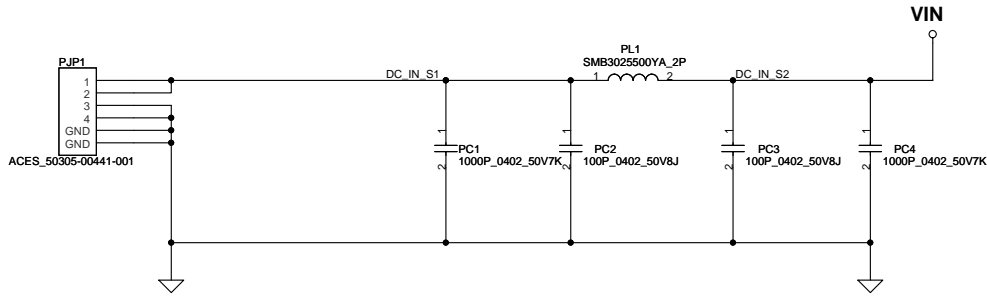
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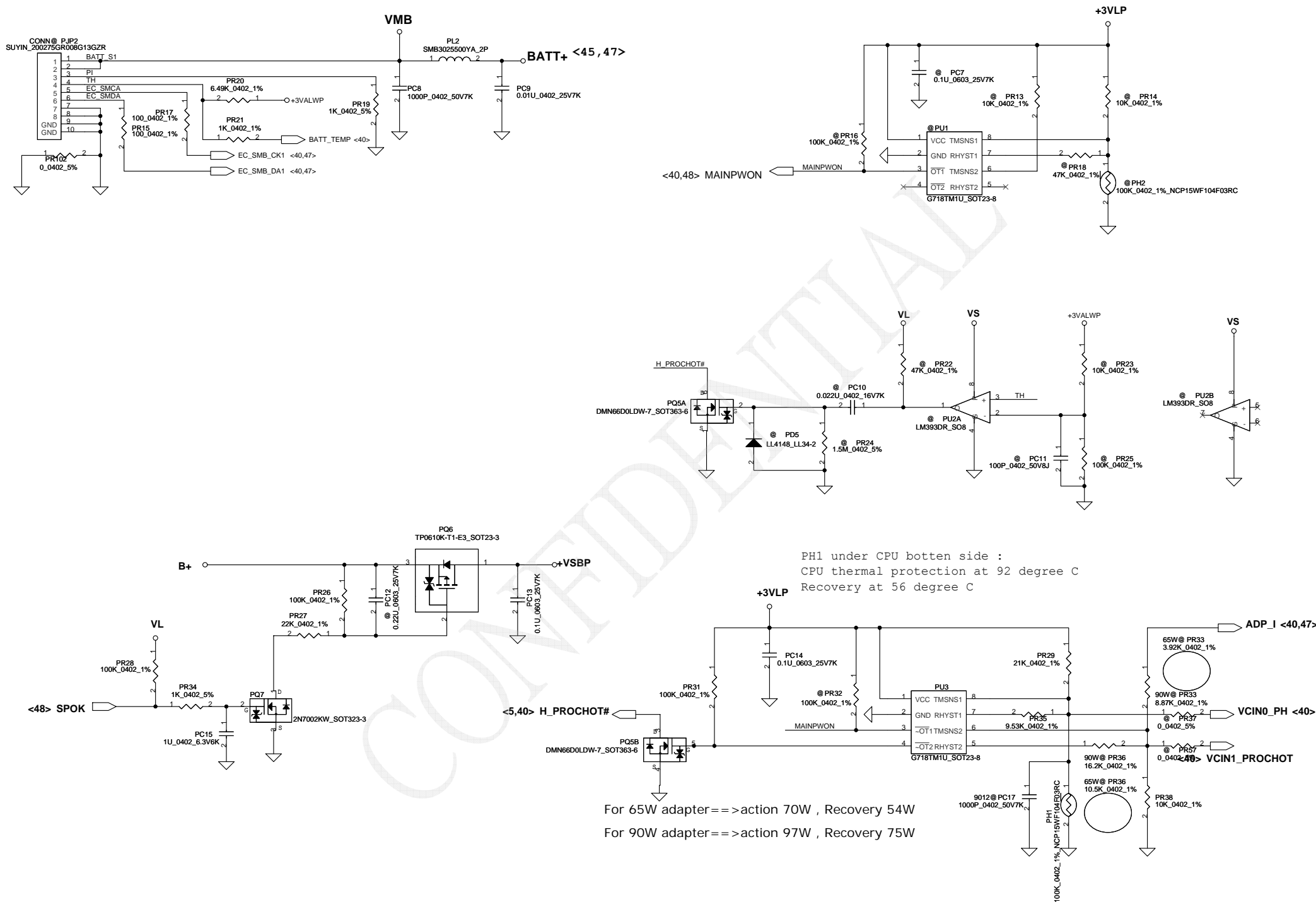
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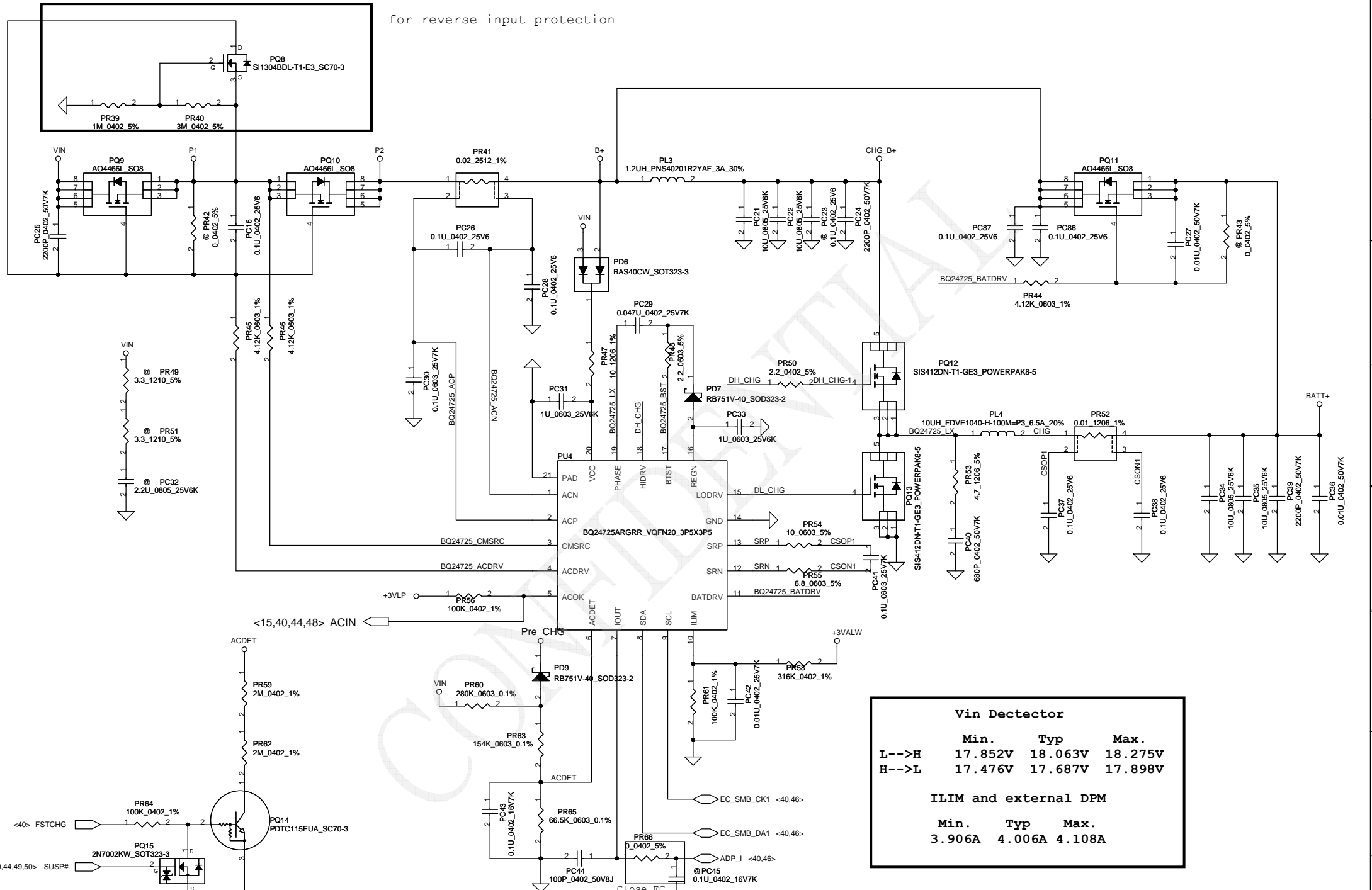


PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

For 65W adapter ==> action 70W , Recovery 54W
 For 90W adapter ==> action 97W , Recovery 75W

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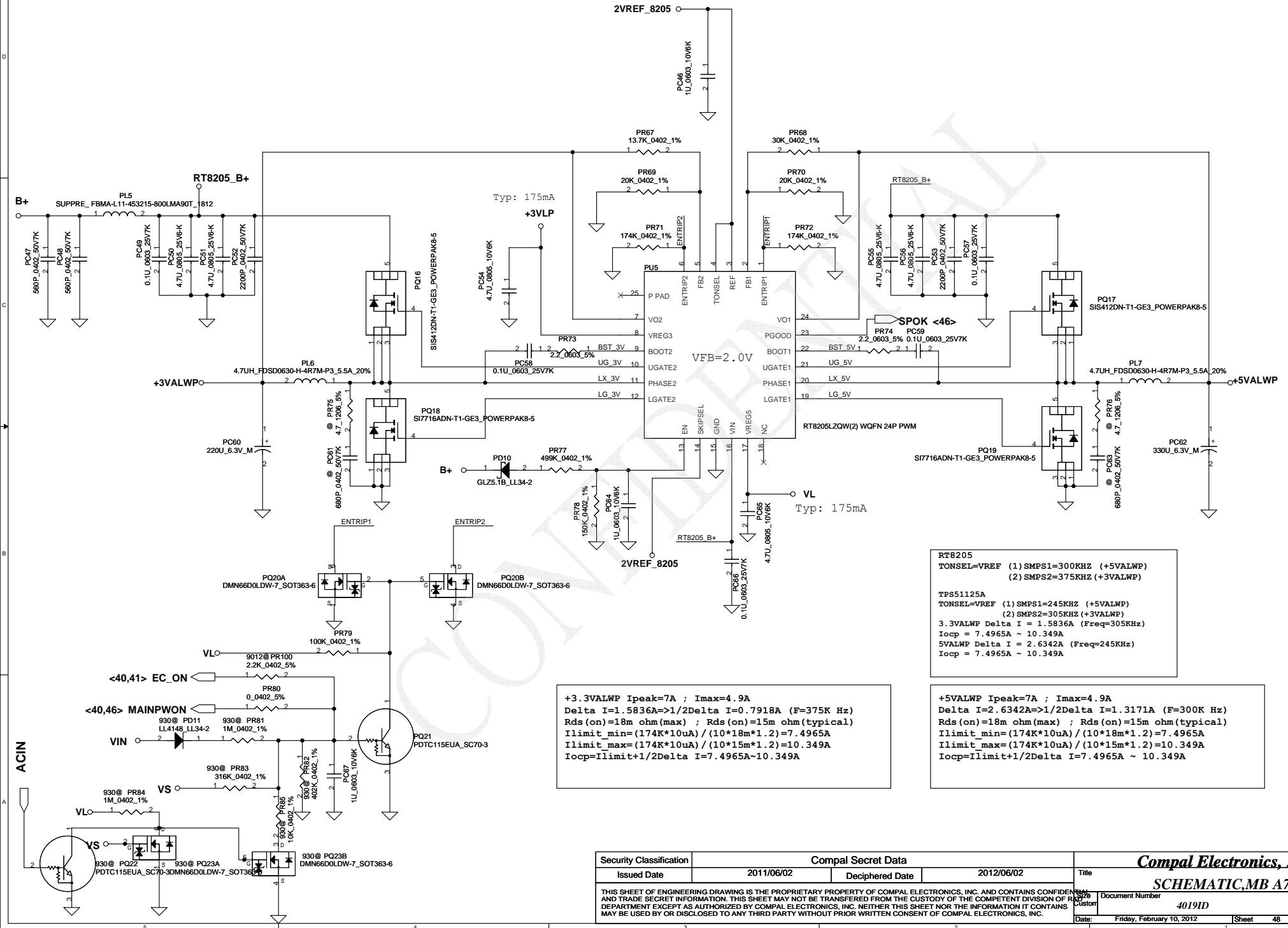
for reverse input protection



Vin Detector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V
ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



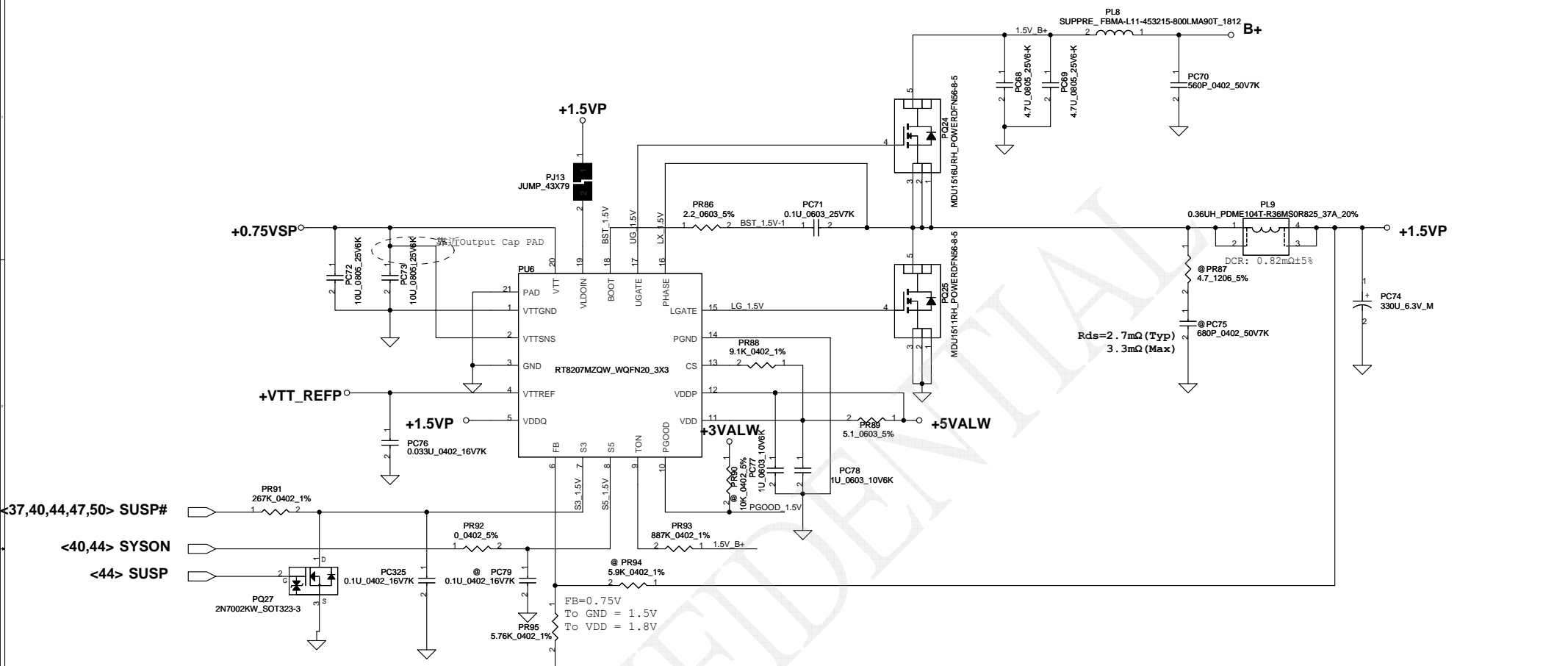
RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)
 3.3VALWP Delta I = 1.5836A (Freq=305KHZ)
 Iocp = 7.4965A ~ 10.349A
 5VALWP Delta I = 2.6342A (Freq=245KHZ)
 Iocp = 7.4965A ~ 10.349A

+3.3VALWP Ipeak=7A ; Imax=4.9A
 Delta I=1.5836A=>1/2Delta I=0.7918A (F=375K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
 Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
 Iocp=Ilimit+1/2Delta I=7.4965A~10.349A

+5VALWP Ipeak=7A ; Imax=4.9A
 Delta I=2.6342A=>1/2Delta I=1.3171A (F=300K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
 Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
 Iocp=Ilimit+1/2Delta I=7.4965A ~ 10.349A

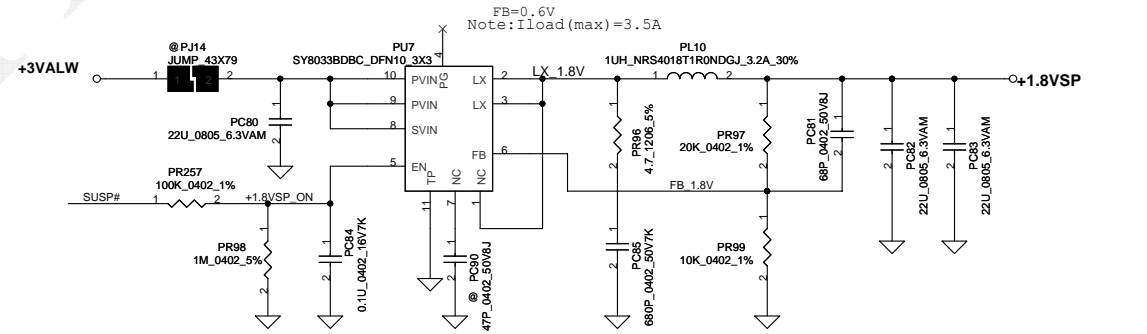
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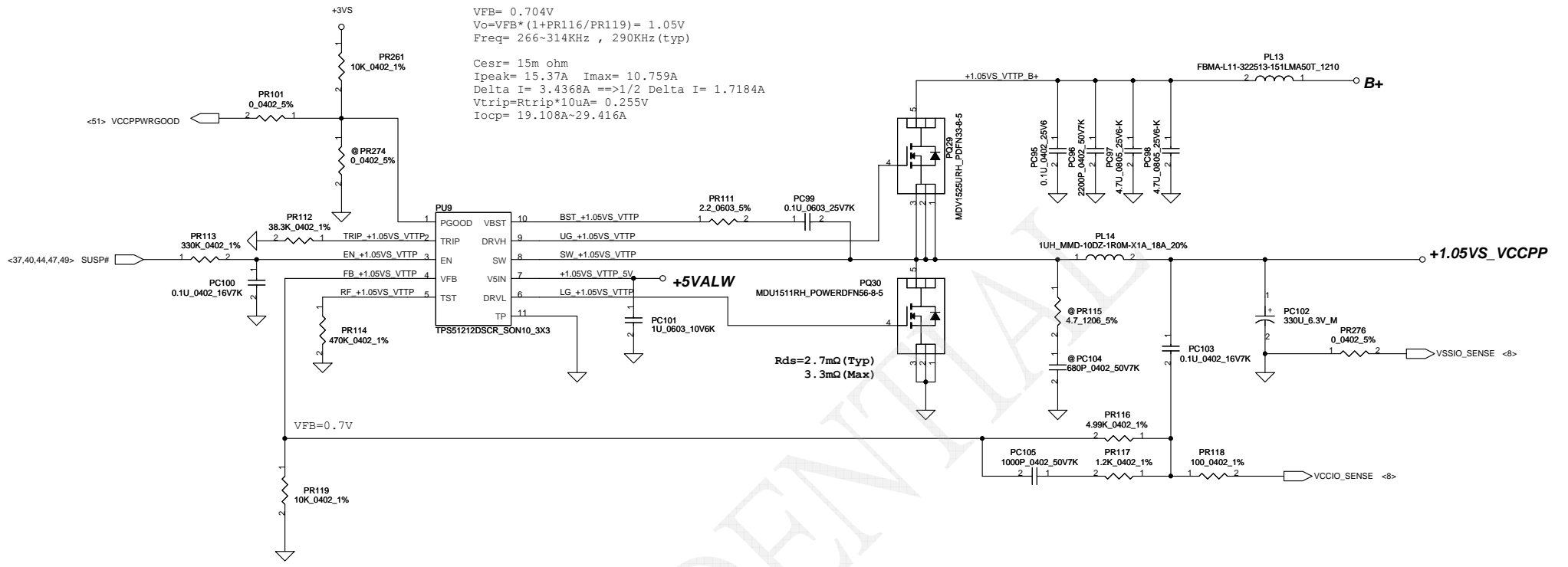
<37,40,44,47,50> SUSP#
 <40,44> SYSON
 <44> SUSP

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

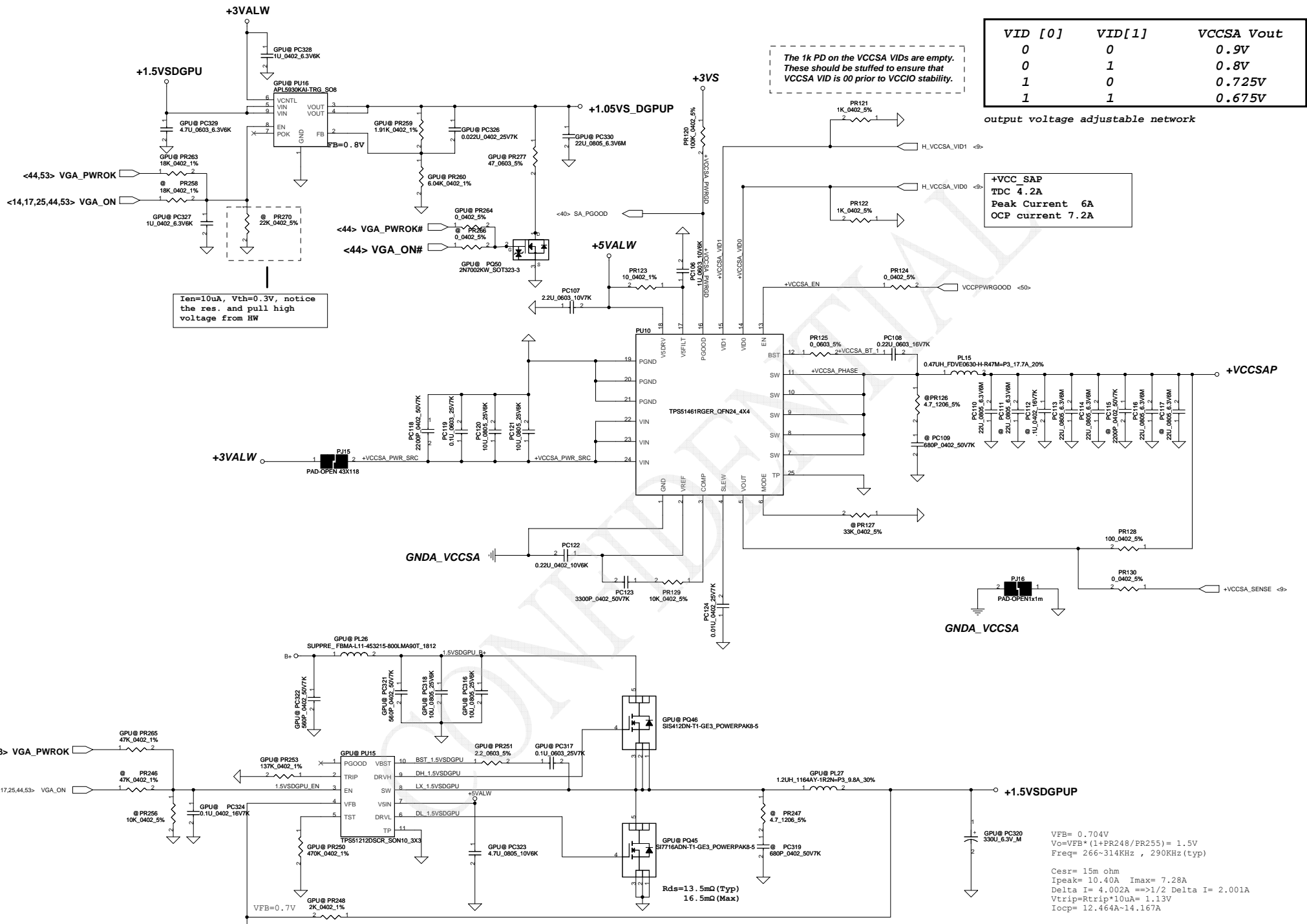
Note: S3 - sleep ; S5 - power off



Notice: Internal resistance about 500K on 2nd EN pin



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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

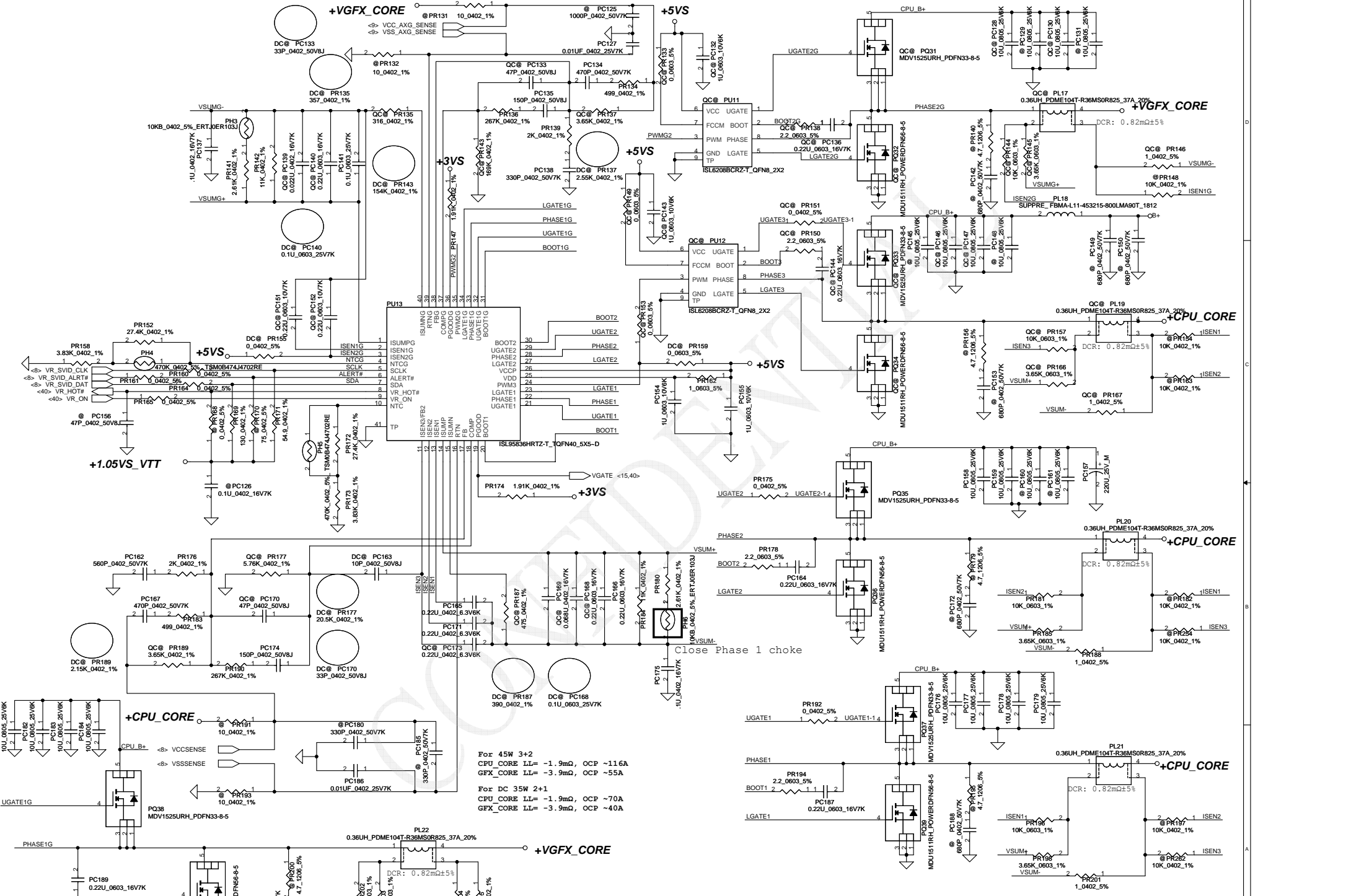
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

Ien=10uA, Vth=0.3V, notice
the res. and pull high
voltage from HW

VFB= 0.704V
Vo=VFB*(1+PR248/PR255) = 1.5V
Freq= 266~314KHz , 290KHz (typ)

Cesr= 15m ohm
Ipeak= 10.40A Imax= 7.28A
Delta I= 4.002A ==>1/2 Delta I= 2.001A
Vtrip=Rtrip*10uA= 1.13V
Iocp= 12.464A~14.167A

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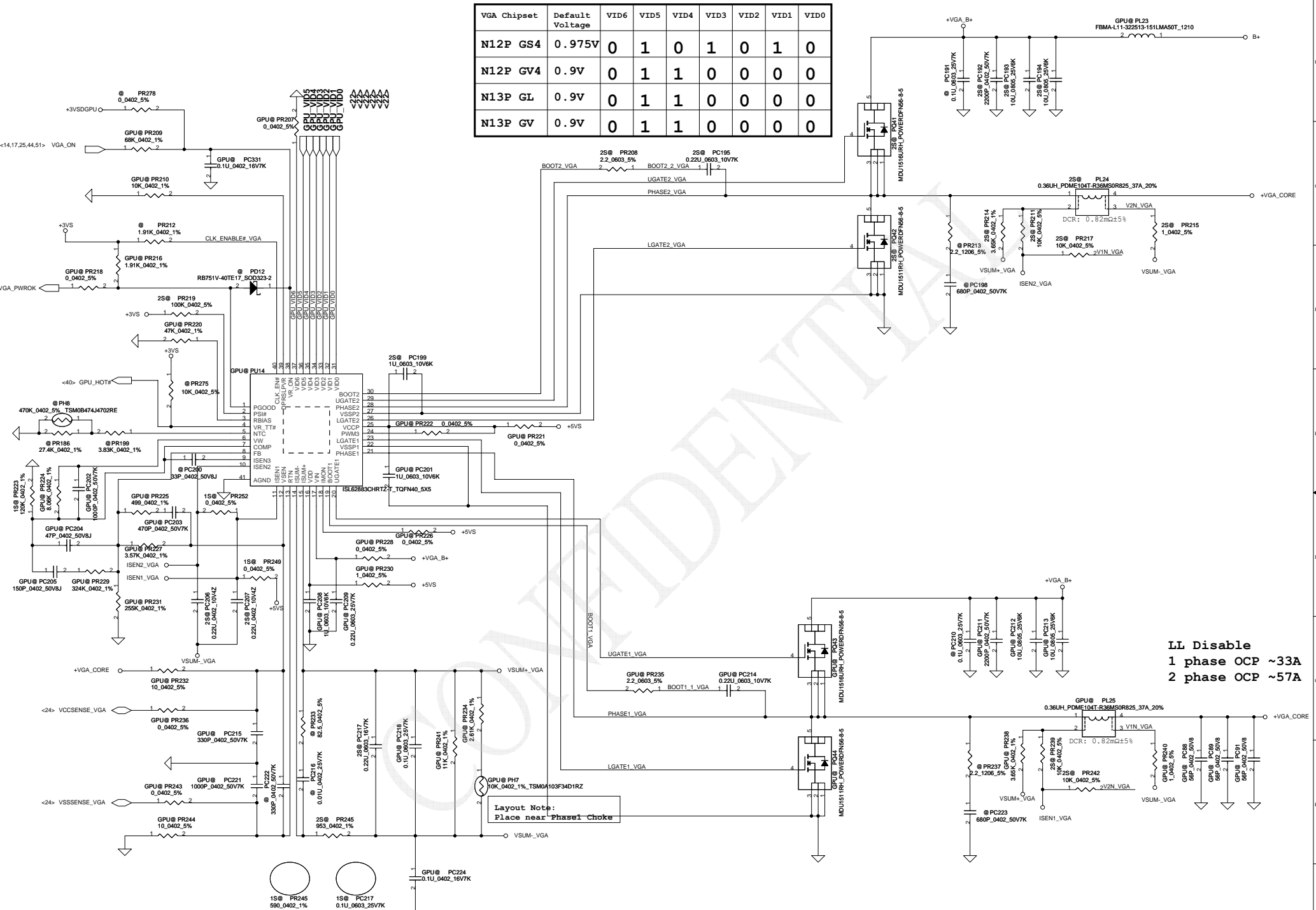
For 45W 3+2
 CPU_CORE LL = -1.9mΩ, OCP ~116A
 GFX_CORE LL = -3.9mΩ, OCP ~55A

For DC 35W 2+1
 CPU_CORE LL = -1.9mΩ, OCP ~70A
 GFX_CORE LL = -3.9mΩ, OCP ~40A

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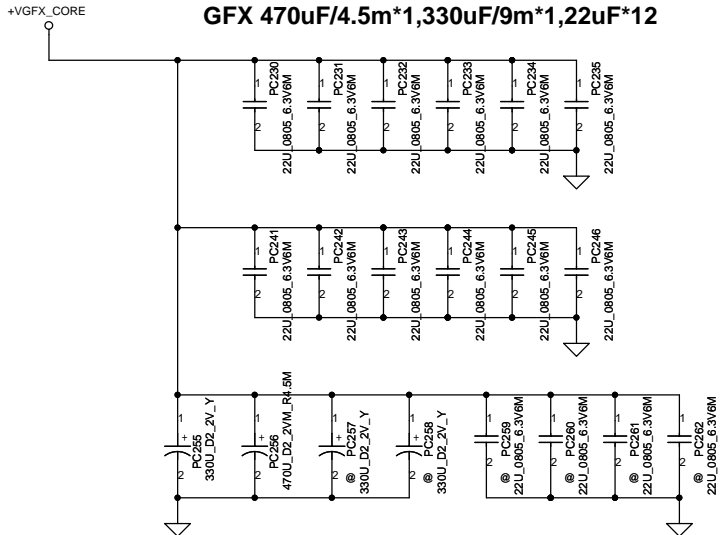
VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0



LL Disable
 1 phase OCP ~33A
 2 phase OCP ~57A

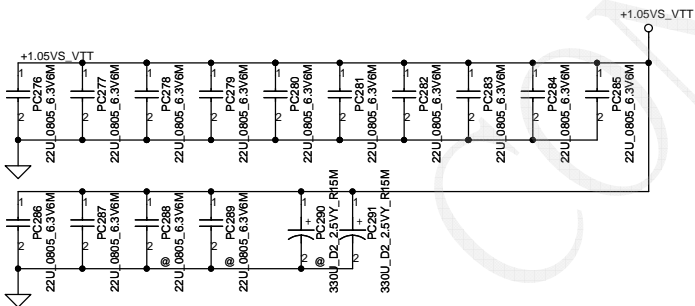
Layout Note:
 Place near Phase1 Choke

PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

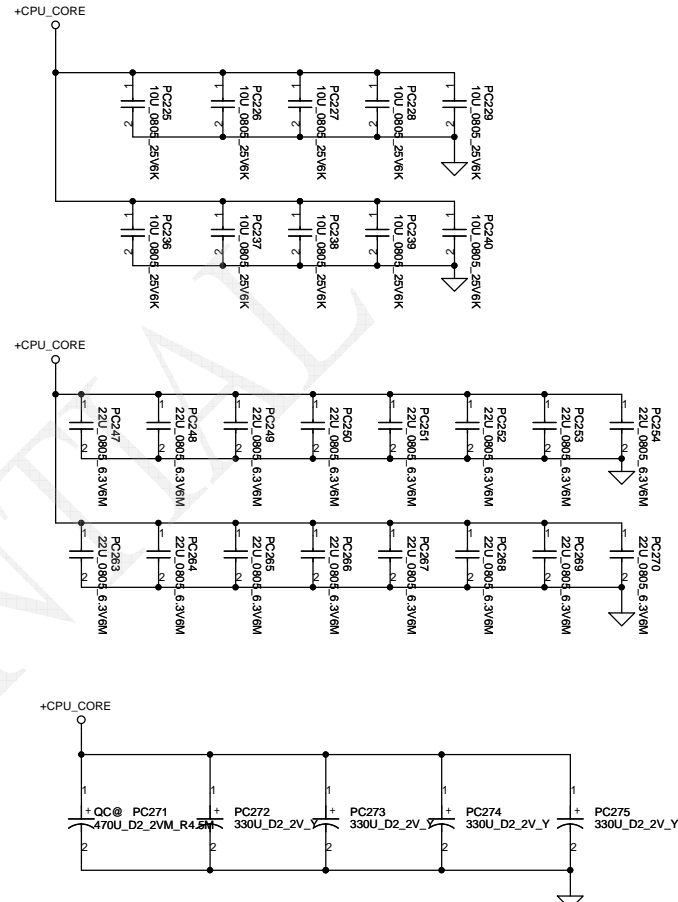


Vaxg

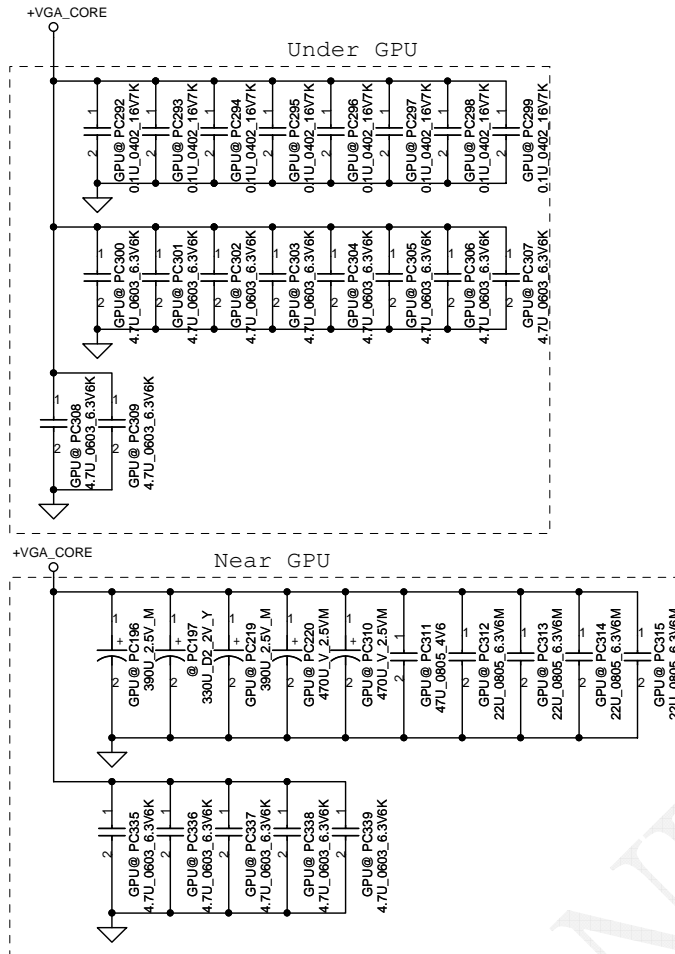
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2	2011 1208	DVT
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	FVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	FVT
8		Consider part rating		51	Change PR277 from 0402 to 0603	2011 1222	FVT
9		Tune transient character		52	Add PC139, PC169 Swap PC271 & PC275	2011 1222	FVT
10		PH1 OTP and ADP_I throttling by H/W control		46	Delete PR37, PR57	2011 1222	FVT
11		Follow Power design		55	Add PC313, PC314, PC315	2011 1222	FVT
12	VGA sequence meet nVidia SPEC			51	Swap PR258 & PR263, PR266 & PR264, PR246 & PR265	2011 1223	FVT
13	Cut-in EMI solution			47	Add PR53, PC40	2012 0104	FVT2
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
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17							

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)		0.2
7	P.44		9/7	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU_ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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25	P. 44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P. 36		9/20	HW	For SD3.0 issue (Add R2088.R2089)		0.2
27	P. 20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic (Q2006.C2062.R2090)		0.3
28	P. 44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic (U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P. 40		10/17	HW	Board ID error. Add R353.		0.3
30	P. 40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P. 17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P. 18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P. 13. 40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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43	P. 41		11/16	ME		Delete SW5, SW6, Pop SW2, SW3	0.4
44	P. 05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P. 35		11/17	HW	LAN SPROM on Chip	De-pop U31, R537 Pop R538	0.4
46	P. 36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P. 13		11/17	HW	RTC issue	Change C682, C686 to 15P	0.4
48	P. 31, 32, 41		11/17	ESD		De-pop D3, D4, D17, D18, D15 Pop D24, D36	0.4
49	P. 40		11/17	HW		De-pop R891, R893	0.4
50	P. 24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P. 13		11/21	HW		Chip Select Change R651, R2049 to 0ohm	0.4
52	P. 13, 40		11/21	HW		Delete NPCE885N (R2091, R2092, R2094, R2095, R2096, R698, R699, R692, C2085)	0.4
53	P. 45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P. 35, 36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525, R536, R537, R538 to 1k	0.4
56	P. 13		11/23	HW		Delete R2093, R2049, R651 (0ohm)	0.4
57	P. 13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P. 35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P. 36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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58	P. 24. 25		12/02			Change R1057 from 35kohm to 45kohm Change R1077 from 40.2ohm to 42.2ohm Change R1080 from 60.4ohm to 51.1ohm	0.4
59	P. 22		12/02			for N13P_GS, the boot voltage is 0.9V pop R1022,R1021,R1036,R1035,R1034,R1033 for N13P_GL, the boot voltage is 0.95V pop R1022,R1037,R1020,R1019,R1034,R1033 for N13M_GS, the boot voltage is 0.925V pop R1022,R1037,R1020,R1019,R1018,R1033	0.4
60	P. 44		12/02			Change R369 from 470ohm to 150ohm Change R26 from 470ohm to 47ohm Pop Q3	0.4
61	P. 13		12/02			BIOS ROM(4M) Change U36 to SA00003K800	0.4
62	P. 35		12/06			EMI suggestion for Card Reader Change R195 from 33ohm to 22ohm Change R216 from 22ohm to 0ohm Change C2094 from 6pF to 6.8pF Change R2101 from 0ohm to 22ohm Change R2088 from 47ohm to 75ohm Change R2102 from 47ohm to 0ohm De-pop C2096	0.4
63	P. 36		12/07			EMI request for 家電下鄉 Add C2097	0.5
64	P. 39		12/07			For PCH HM70 Change USB port0 to co-lay USB3.0 Change USB port2 to USB2.0 Change USB port 11 to BT	0.5
65	P. 44		12/07			Change 1.5VSDGPU EN from VGA_ON# to VGA_PWROK# Add R2103,Q2008	0.5
66	P. 18		12/09			For eDP Change Q2007 from SB501380020 to SB501110010	0.5

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67	P. 31		12/16	EE		change Q2007 to 2N7002 for eDP_HPD circuit	LA-7912 0.2
68	P. 40		12/16	EE		add WLAN_PME# on pin85. add wlan_on signal on EC pin38 add AC circuit	LA-7912 0.2
69	P. 35		12/16	EE		reserve Q2007 for open +3V_LAN by PCH_PWREN#	LA-7912 0.2
70	P. 40		12/16	EE		add R2063 for pull high VCIN0_PH to +3VL 10k add R2059 for pull low VCIN1 10k	LA-7912 0.2
71	P. 41		12/20	EE		resever R2116 ~ R2119 for change LED power to 3VLA-7912 resever C2101~C2107 56pF on T/P for EMI	0.2
72	P. 36, 14		12/22	EE		change R384 & R385 power to +3V_LAN unpop R630 & reserve R2120 to pull high +3V_LAN	LA-7912 0.2
73	P. 42, 35		12/22	EE		change Q43 from 2n7002 to BSS138 unpop R209	LA-7912 0.2
74	P. 40		12/23	PWR		change R353 to 56k for board ID 0.2 power request pop R2063, R2059 un-pop R880, R891, R893	LA-7912 0.2
75	P. 39		12/23	EMI		change USB3 signal pass by chock (SM070001600)	LA-7912 0.2
76	P. 41		12/23	ME		Change LED (Blue) SC591NB5A30 to SC591TBKA10 Change LED (AMBEL) SC500007700 to SC500005930 change (R2116=130ohm), (R377,2118,378=390ohm) (R2117,2119 = 51 ohm)	LA-7912 0.2
78	P. 36		12/23	EMI		R2088 change to 10ohm	LA-7912 0.2
79	P. 25		12/23	EMI		L1002 use SM010028800 (for N13P_GL) use 0ohm on N13P_GS,N13M_GS	LA-7912 0.2
80	P. 44		12/24	EE		POP R2104, R2106 unpop R2105, R2107 for VGA sequence	LA-7912 0.2
81	P. 41, 24		12/24	EMI, EE		De-pop C217, C216 EMI request. add R1019, R1020, R1037 for GM@ (VGA_CORE)	LA-7912 0.2
82	P. 40, 27		12/27	EE		change R2059&R2063 to 10k ohm for EC request C2086~C2089 change bom sturte to DIS@	LA-7912 0.2
83	P. 40		12/27	EE		add R2125, R2123 for option WL_OFF# to EC or PCH add R2122, R2124 for option BT_ON# to EC or PCH reserve R2126 to pull high 3VALW reserve R2127 to pull high 3VALW	LA-7912 0.3

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83	P. 41		01/02	EE		reserve R2121 for WLAN_LED connect +3VALW change C2101~2107 bomstructure to GM@	LA-7912 0.3
84	P. 13		01/09	EE		add GPIO23 for define USB config. (R2128 & R2092)	LA-7912 0.3
85	P. 45~56		01/09	PWR		update power circuit	LA-7912 0.3
86	P. 37		01/09	EE		change R2110 to pull high +3VS_FULL	LA-7912 0.3
87	P. 31		01/10	EE		add R2130 reserve for lvds short issue	LA-7912 0.3
88	P. 40		01/10	EE		change board ID to 0.3 (R353 100k)	LA-7912 0.3
89	P. 37		01/11	EE		change R2110 to pull high +3VALW	LA-7912 0.3
90	P. 37		01/11	EE		pop +3VS_FULL 開電線路	LA-7912 0.3
91	P. 13		01/11	EE		add new bom structer usb2@ for usb flag	LA-7912 0.3
92	P. 44		01/11	EE		UNPOP +1.5VSDGPUH to +1.5VSDGPU circuit	LA-7912 0.3
93	P. 35, 40		01/12	EE		add R2131,R2132 for option turn off 3VLAN power by PCH_PWR_EN# or LAN_PWR_EN# (from EC)	LA-7912 0.3
94	P. 37, 40		01/18	EE		add R2134~R2136 reserve for AOIC for ACER request	LA-7912 0.3
95	P. 17		01/18	EE		reserve R2137 pull low USB_P8 for PCH leakage	LA-7912 0.3
96	P. 32		02/02	EE		change R428 & R426 to 0 ohm for CRT issue	LA-7912 0.3

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