

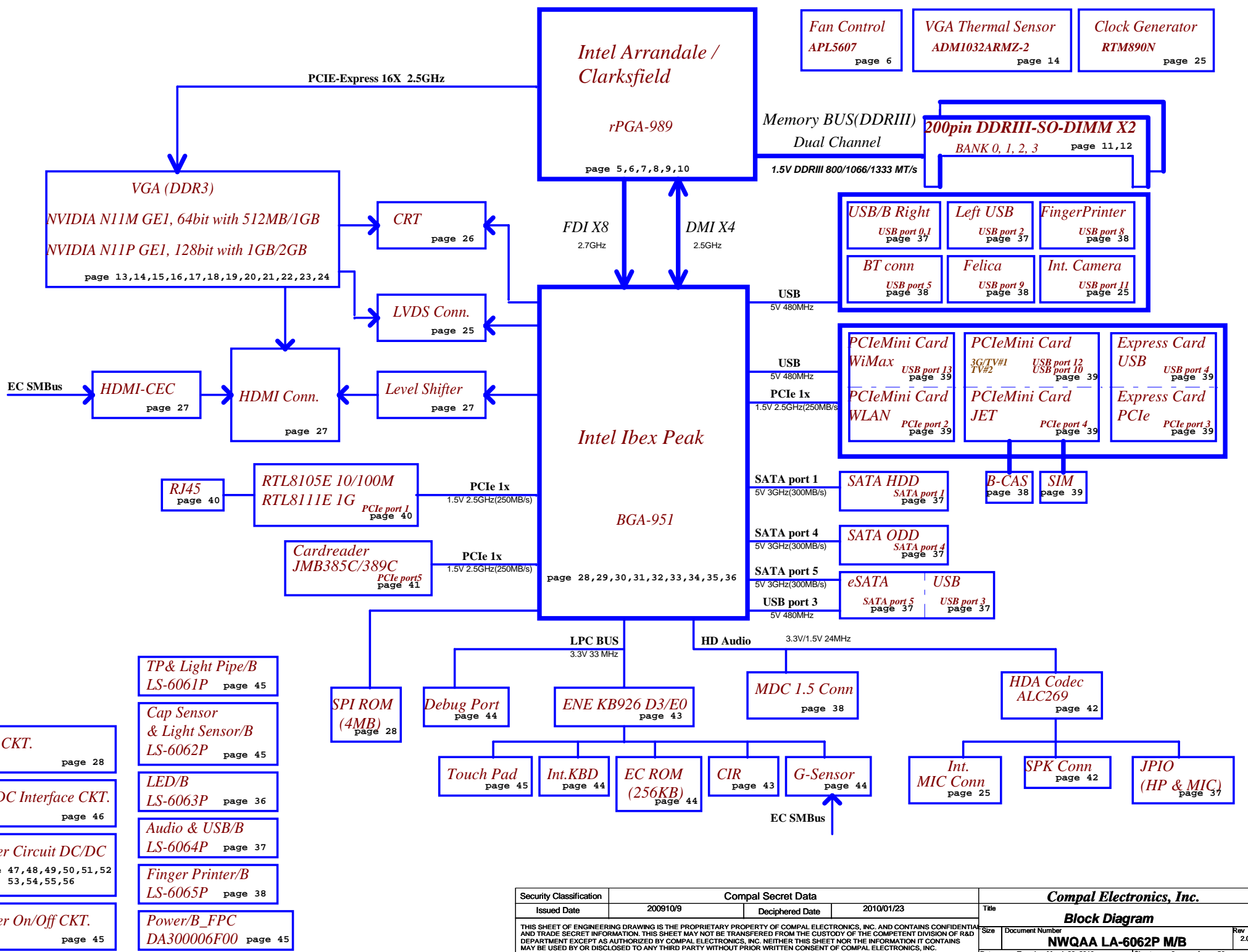
NWQAA

Marseille 10G

LA-6062P REV 2.0 Schematic

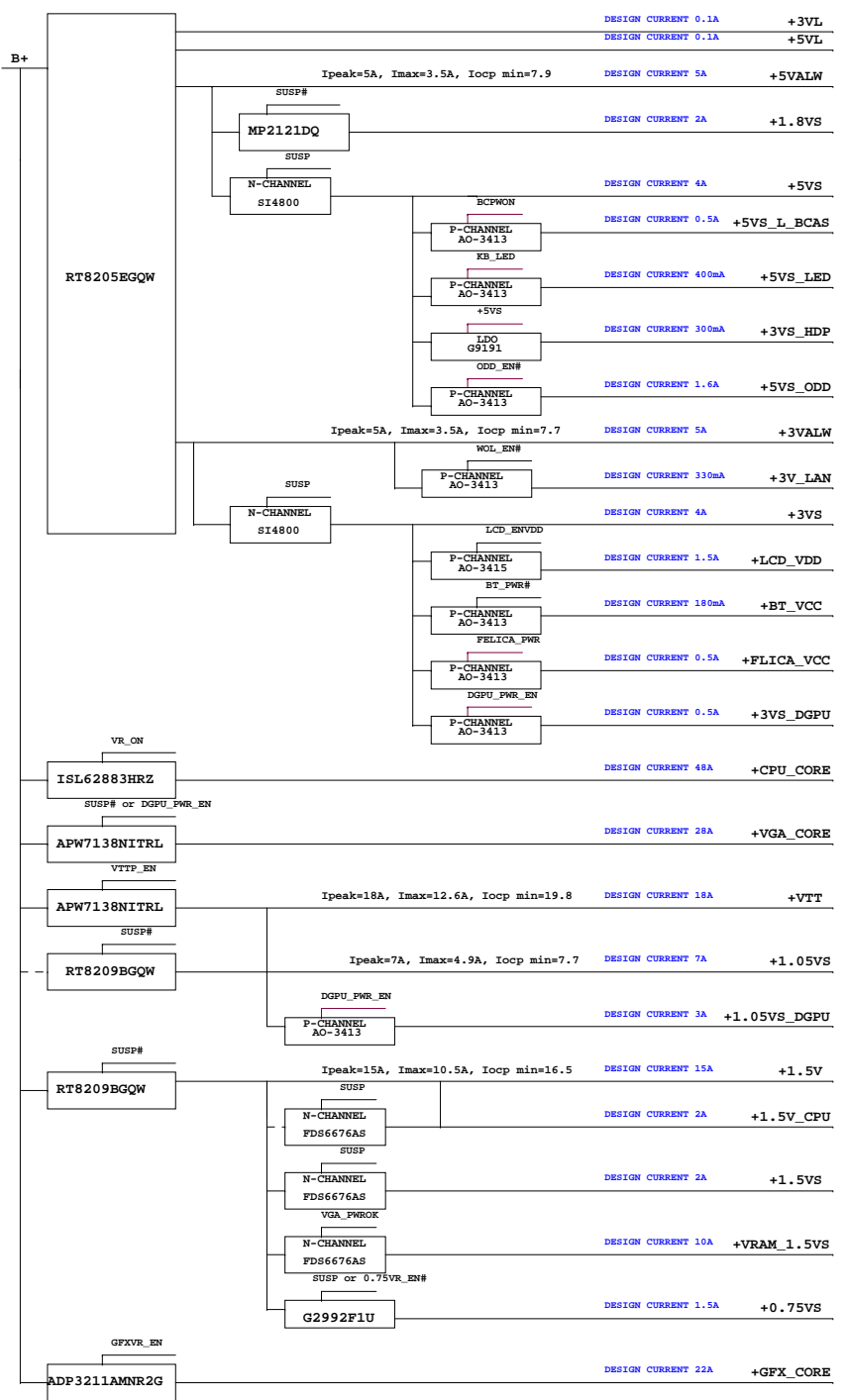
Intel Processor (CFD/ARD) / PCH (HM57/HM55/PM55)
2010-03-24 Rev 2.0

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- DC/DC Interface CKT. page 46
- Power Circuit DC/DC page 47, 48, 49, 50, 51, 52, 53, 54, 55, 56
- Power On/Off CKT. page 45
- TP & Light Pipe/B LS-6061P page 45
- Cap Sensor & Light Sensor/B LS-6062P page 45
- LED/B LS-6063P page 36
- Audio & USB/B LS-6064P page 37
- Finger Printer/B LS-6065P page 38
- Power/B_FPC DA300006F00 page 45

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
State						
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

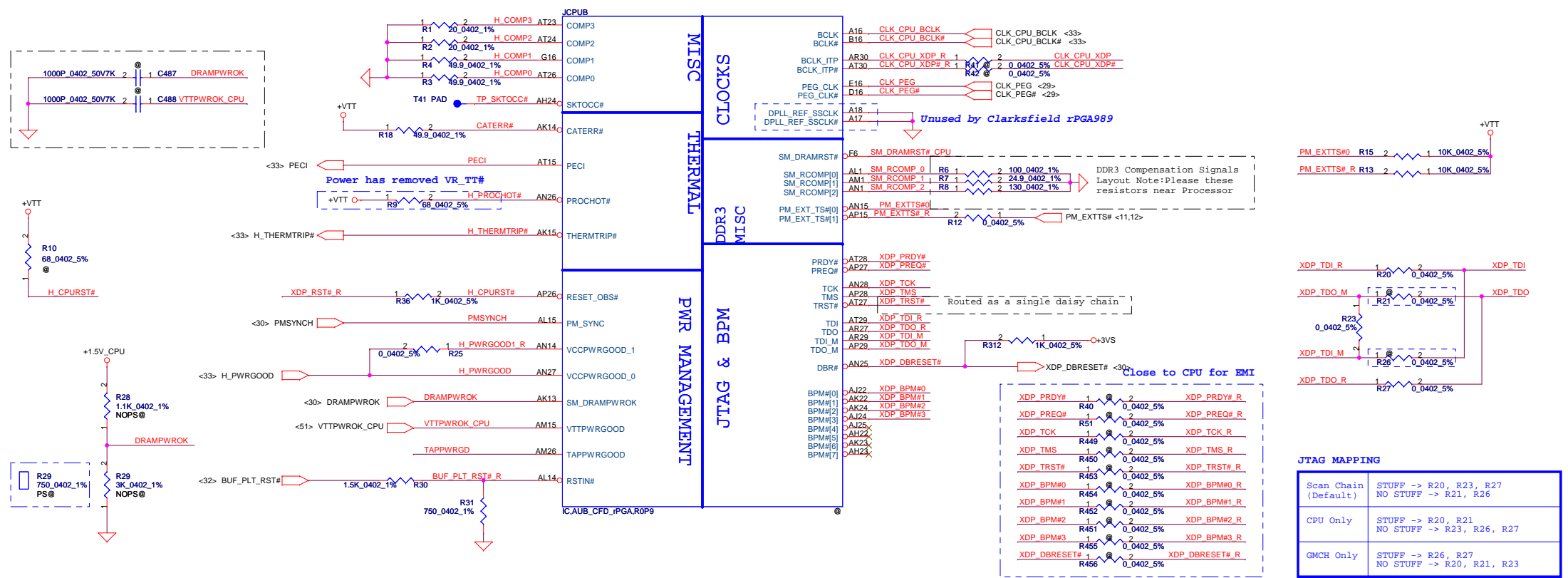
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete	Optimus	Camera & Mic	
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving			GPU				New Card
description	S3 Power Saving			N11P & N11E		N11M		New Card
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-OP1	New Card
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE@	N11MOP@	NEW@

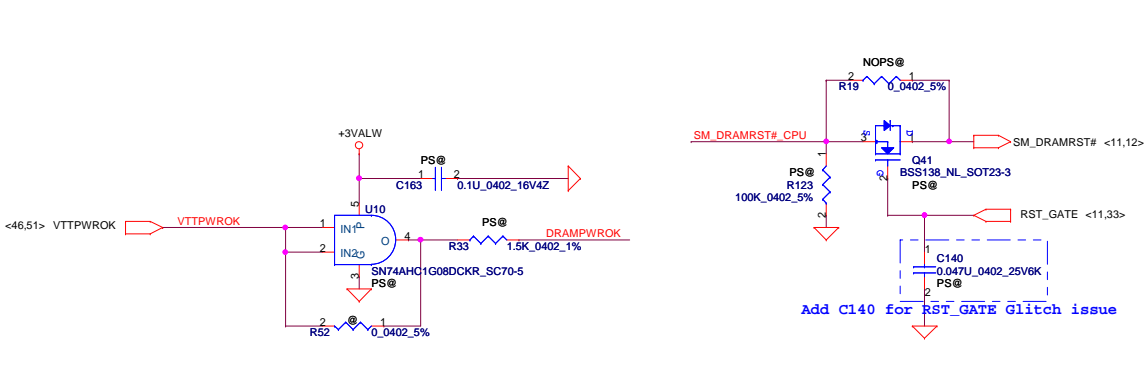
Function	Card reader	
description	JMB385C/389C	
explain	JMB385C	JMB389C
BTO	JMB385@	JMB389@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

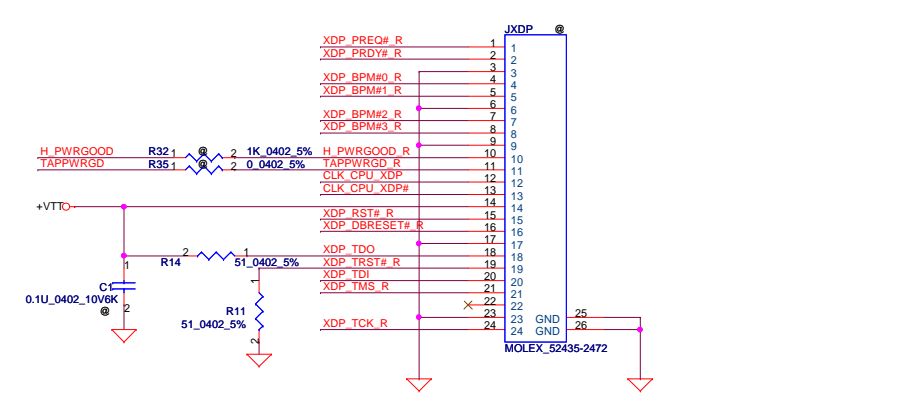
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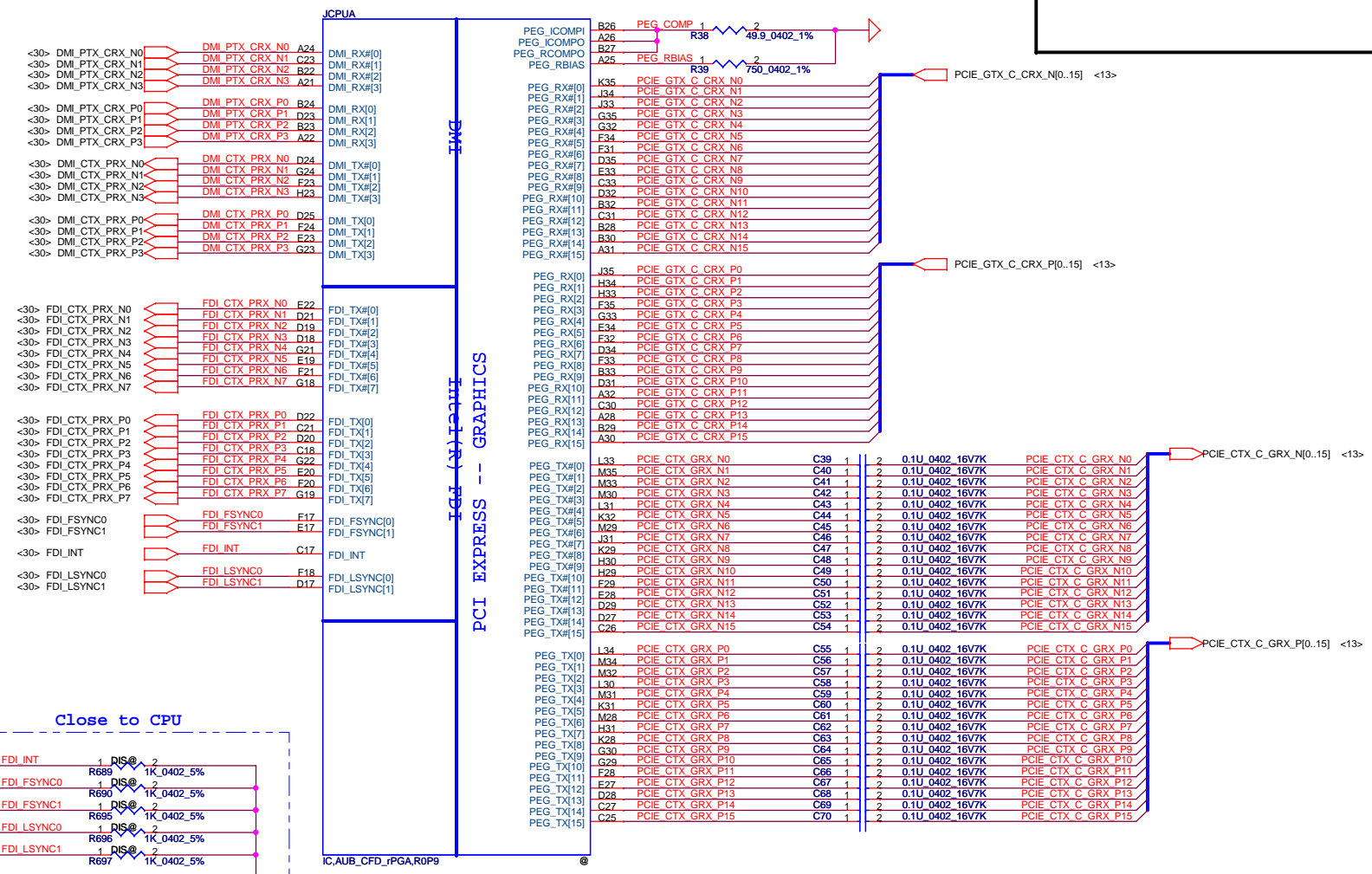
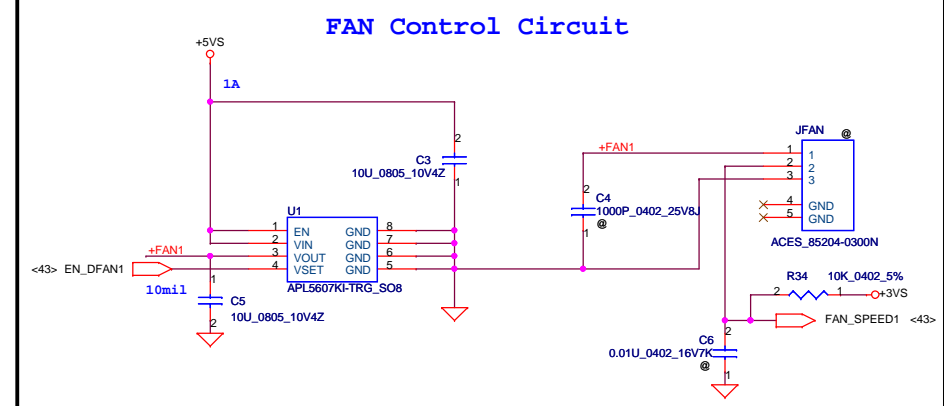
For S3 CPU Power Saving



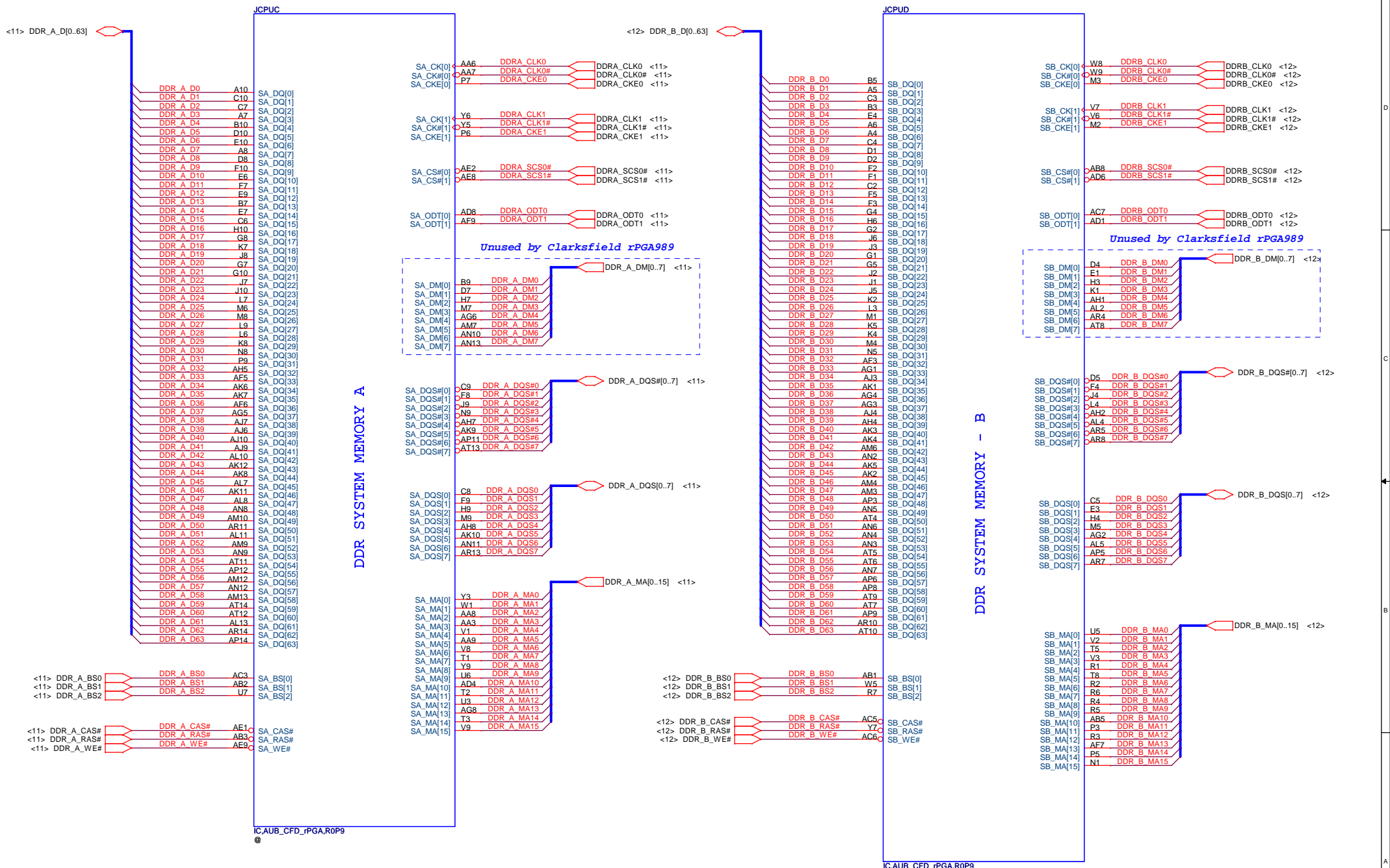
XDP Connector



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				CPU_CLK/MISC/JTAG/XDP
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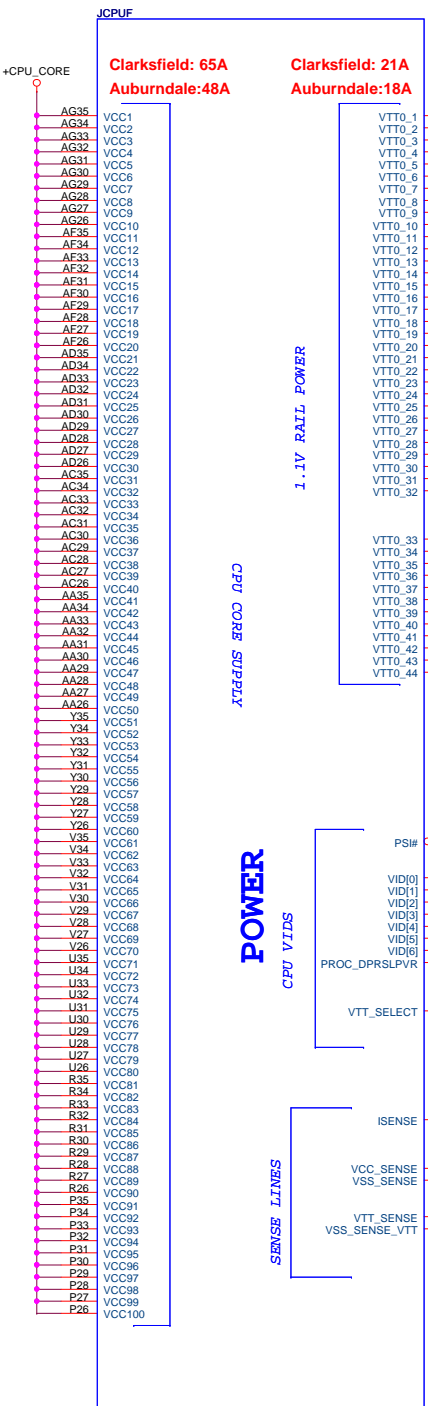
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				CPU_DMI/FDI/PEG/FAN
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Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)



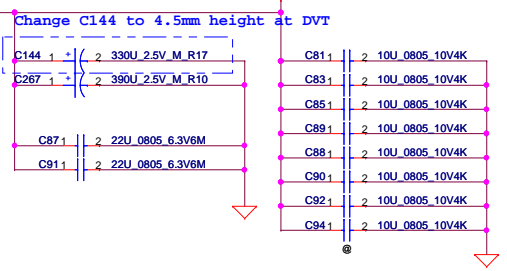
1.1V RAIL POWER

CPU CORE SUPPLY

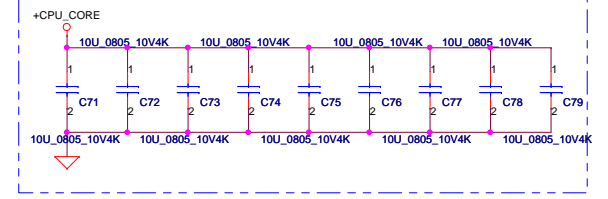
POWER

CPU VID5

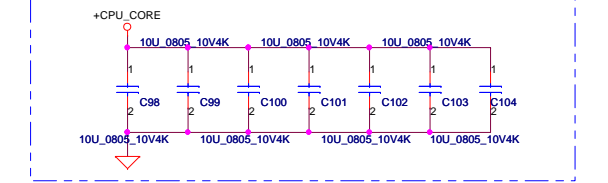
SENSE LINES



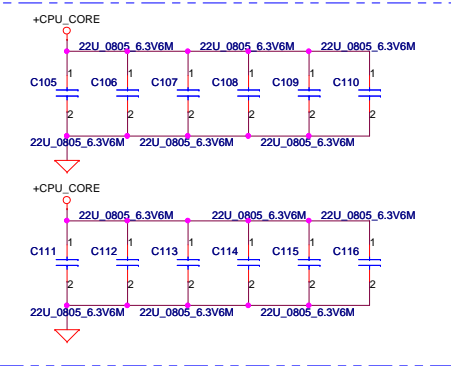
(Place these capacitors between inductor and socket on Bottom)



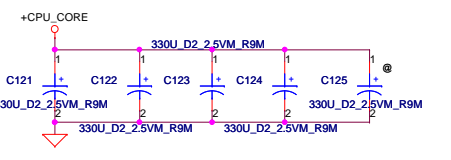
(Place these capacitors under CPU socket, top layer)



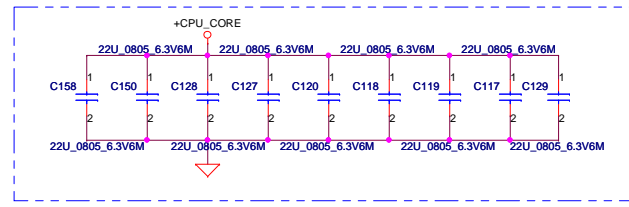
(Place these capacitors on CPU cavity, Bottom Layer)



TOP side (under inductor)



5/25: Add for power team request.

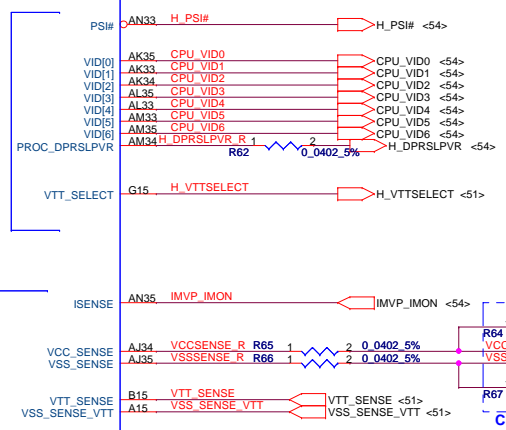


CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarkfield +1.1VS_VTT=1.1V

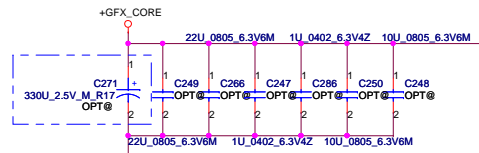
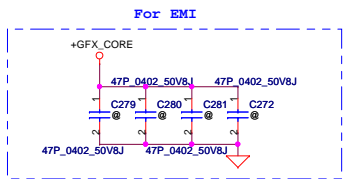
H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V



Close to CPU

Check list:
+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

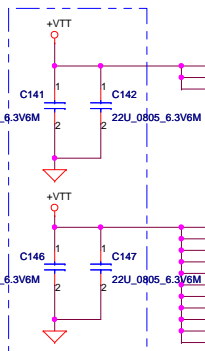
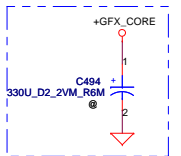
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				CPU_POWER-1
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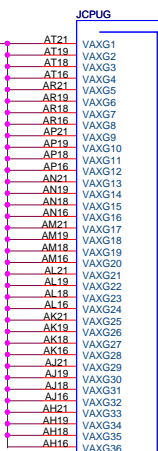
Change C271 to OS-CON at PVT



Co-layout with C271



(Place these capacitors under CPU socket, top layer)



22A GRAPHICS

POWER

Clarksfield: 21A
Auburdale: 18A

FDI

PEG & DMT

Clarksfield: 1.35A
Auburdale: 1.35A

IC:AUB_CFD_PGA:R0P9

SENSE LINES

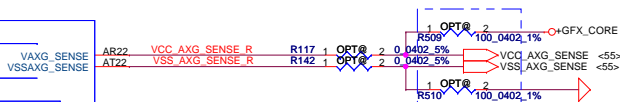
GRAPHICS VIDS

DDR3 - 1.5V RAILS

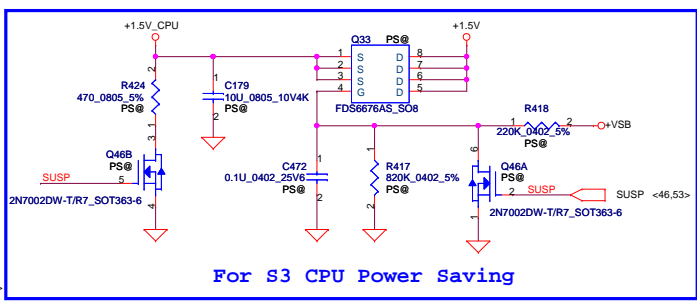
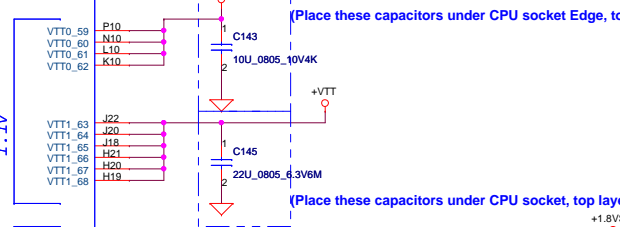
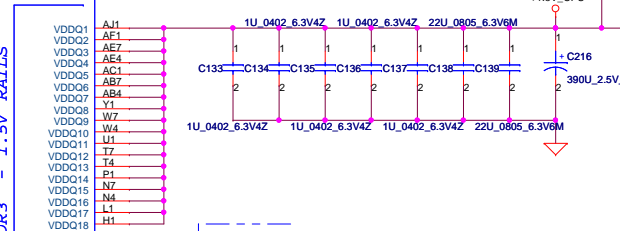
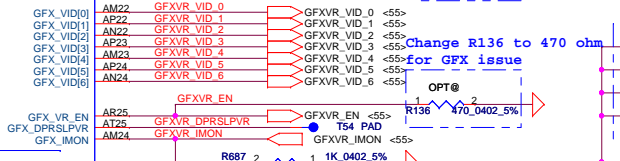
1.1V

1.8V

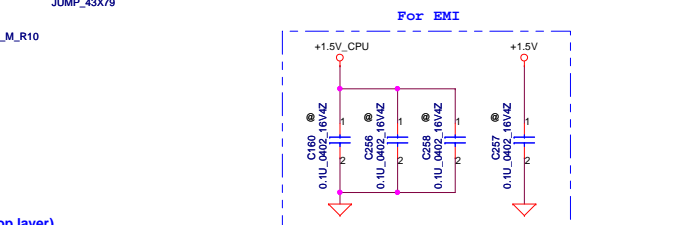
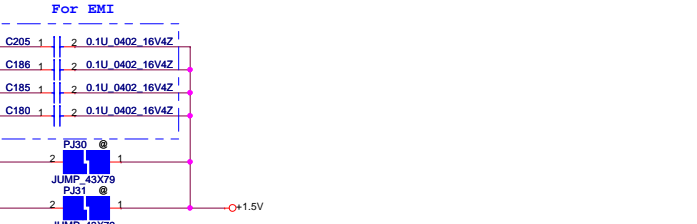
Clarksfield: 1.35A
Auburdale: 1.35A



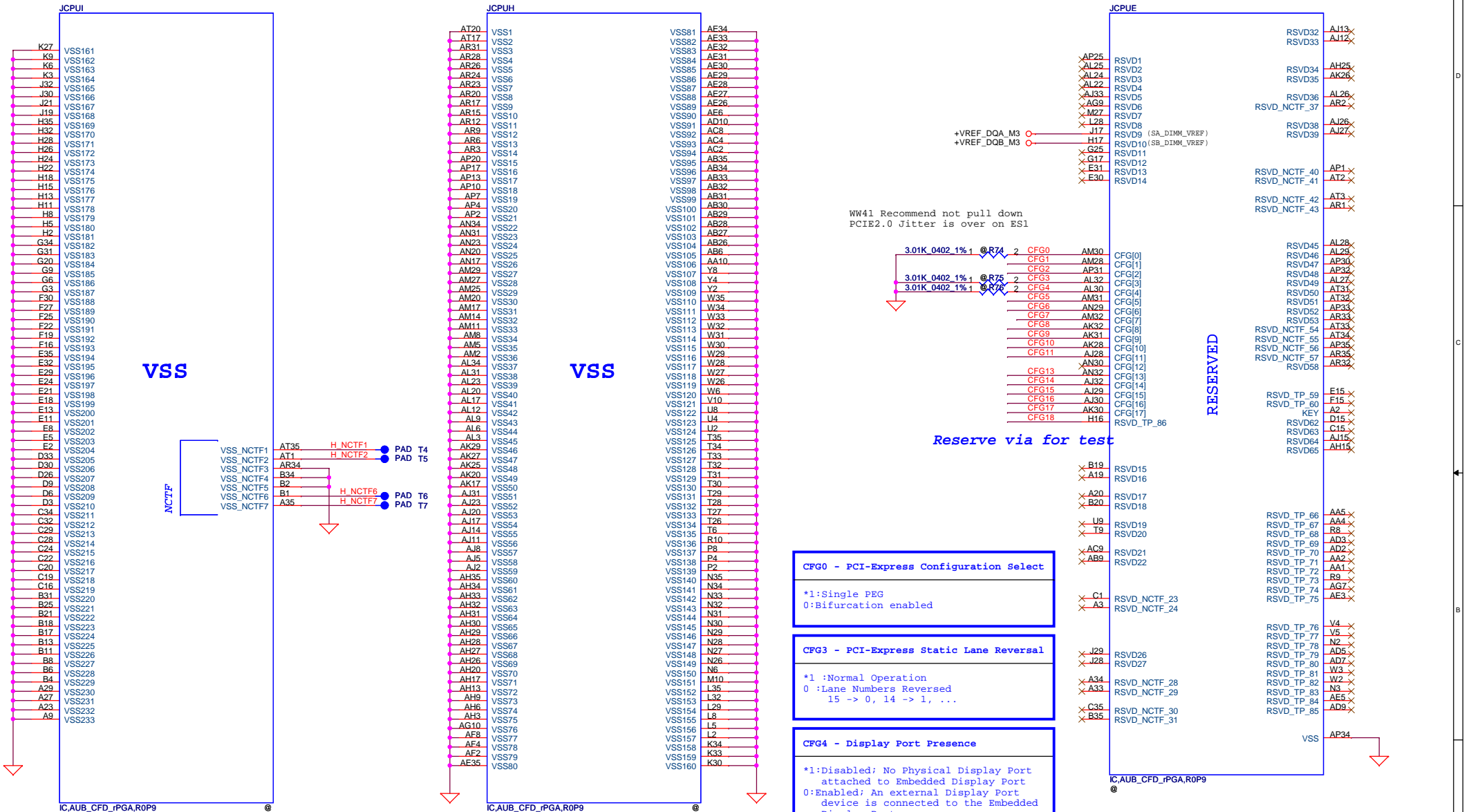
Change R136 to 470 ohm for GFX issue



For S3 CPU Power Saving



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CFG0 - PCI-Express Configuration Select

*1: Single PEG
 0: Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

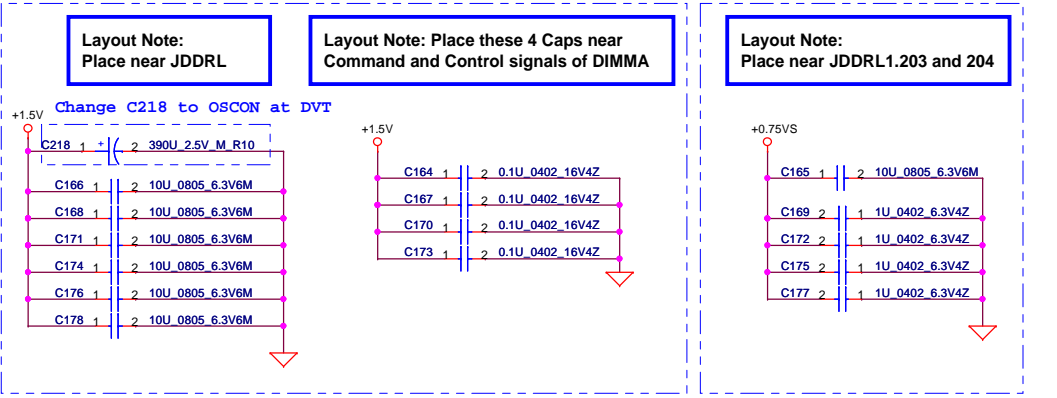
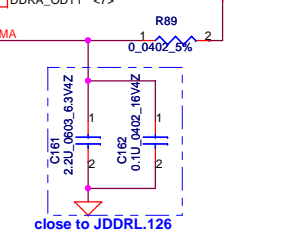
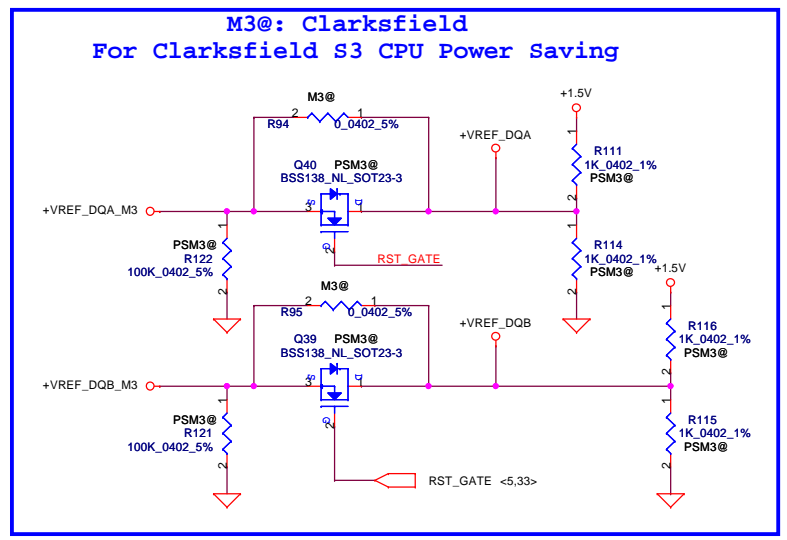
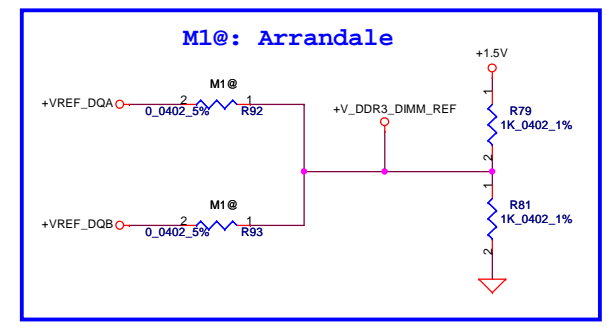
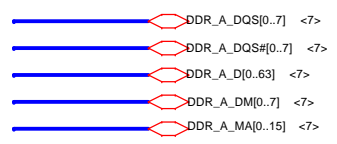
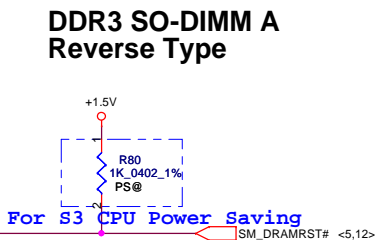
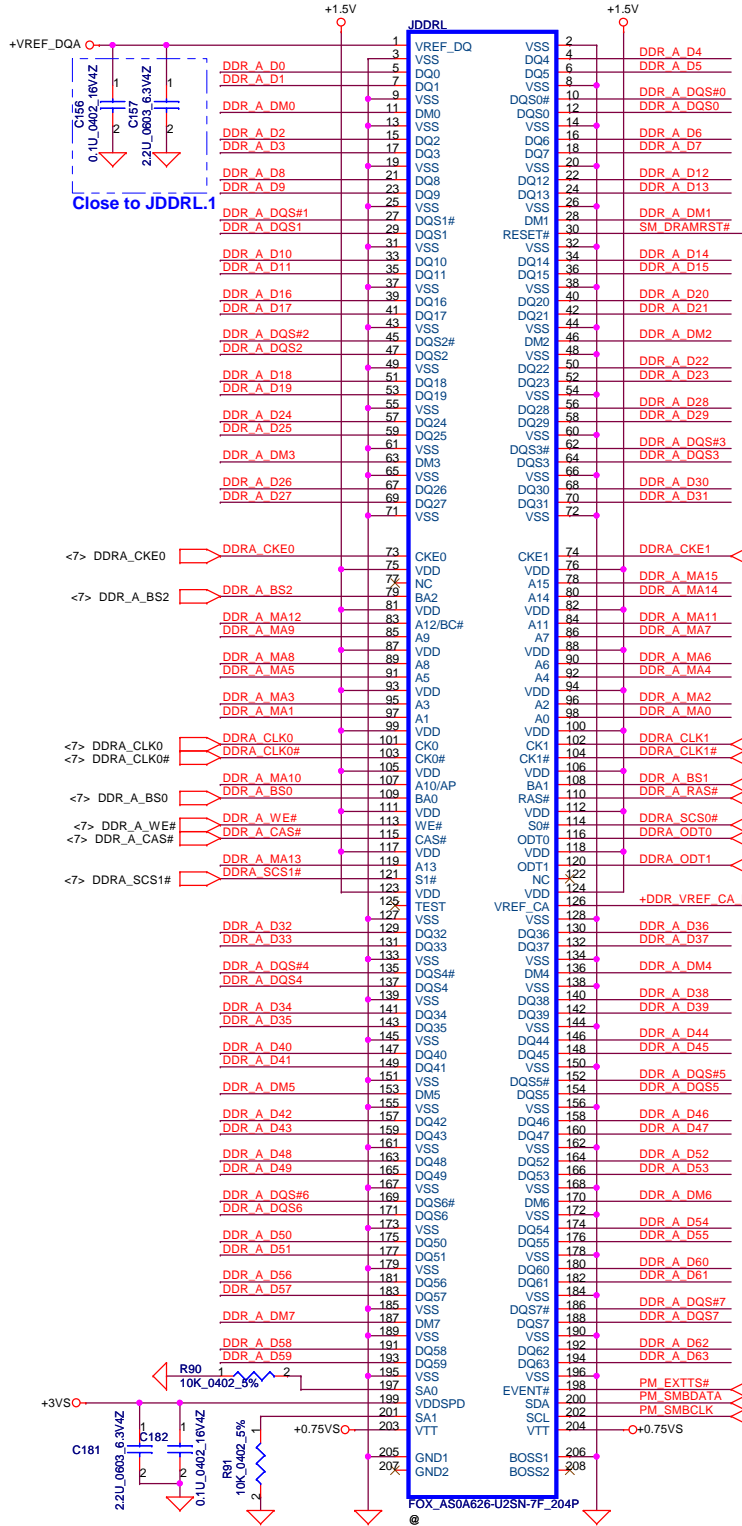
*1 : Normal Operation
 0 : Lane Numbers Reversed
 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1: Disabled; No Physical Display Port attached to Embedded Display Port
 0: Enabled; An external Display Port device is connected to the Embedded Display Port

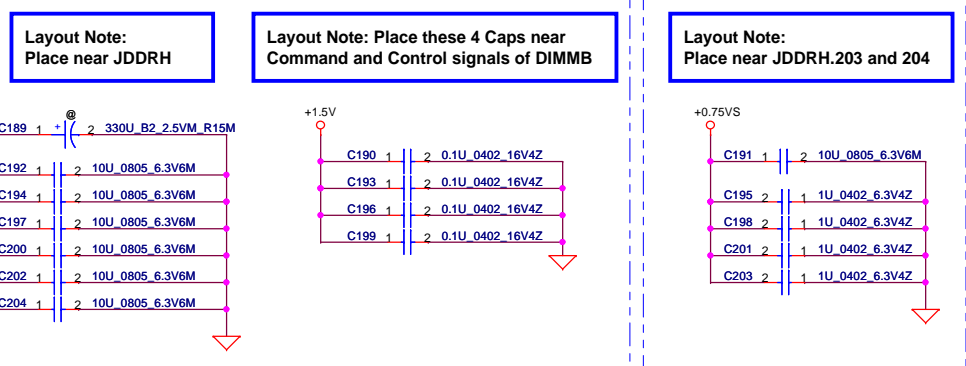
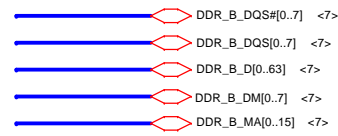
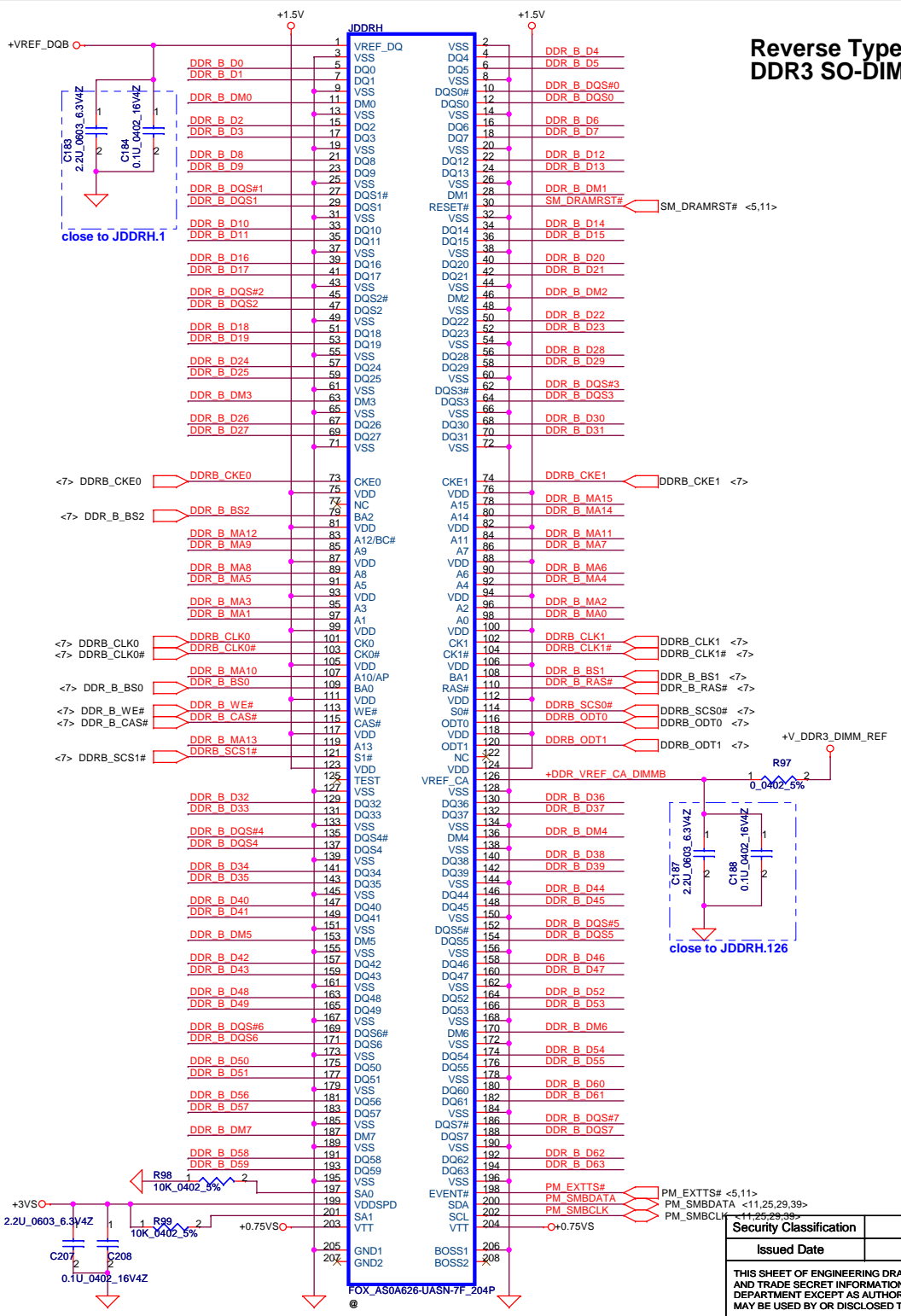
**Default

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				CPU_GND/RESERVED	
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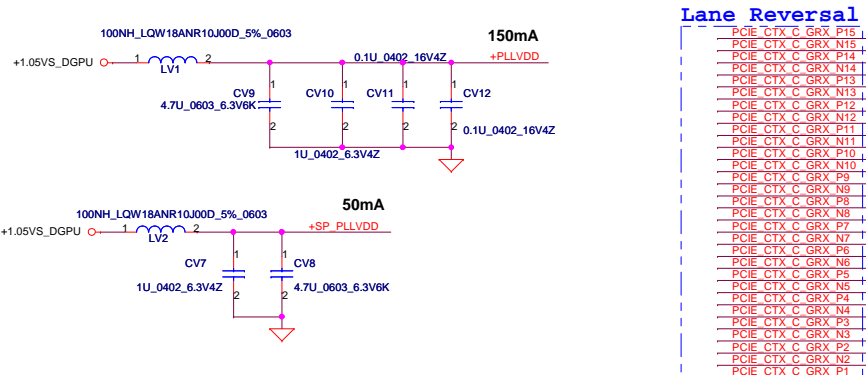


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Reverse Type DDR3 SO-DIMM B

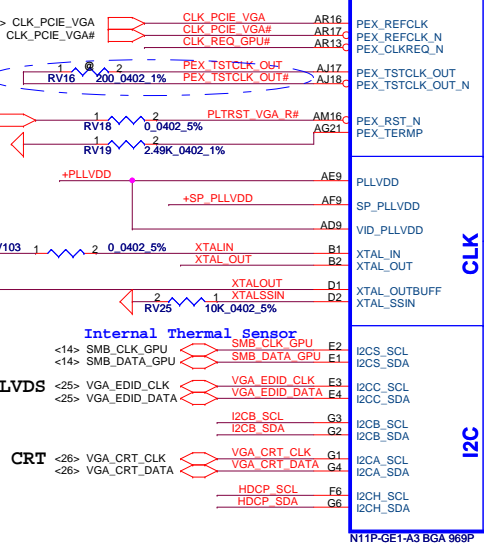
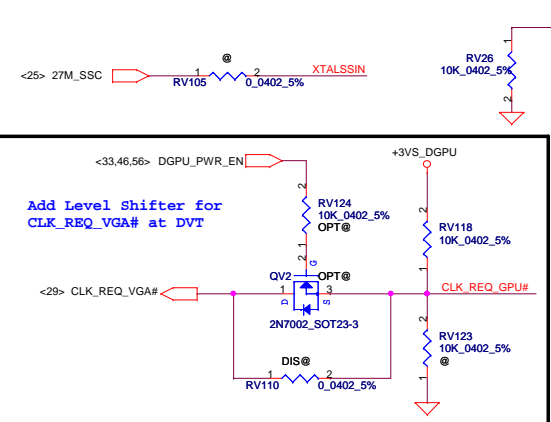
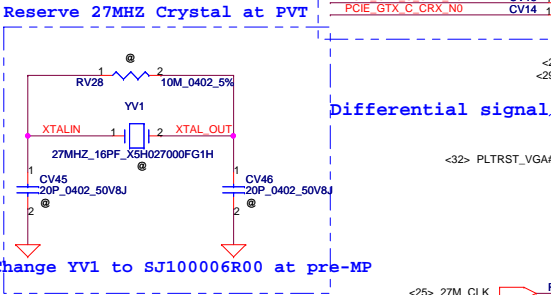


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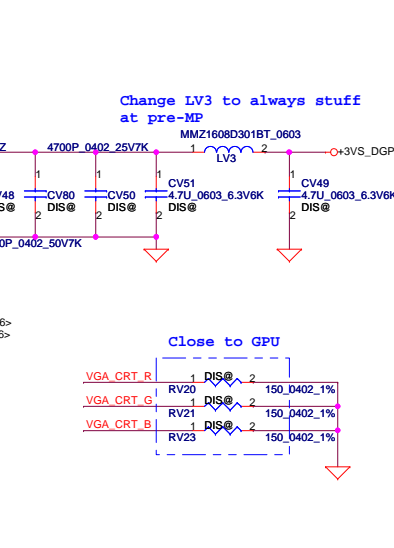
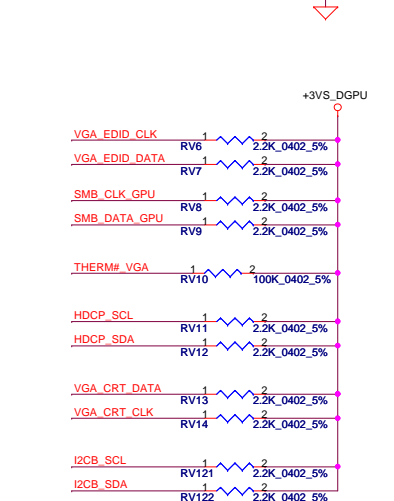
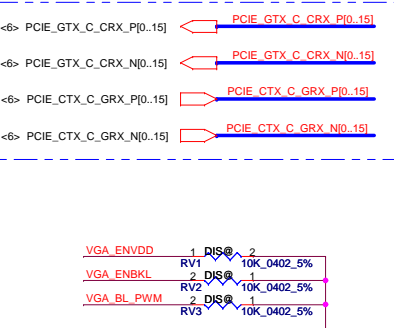
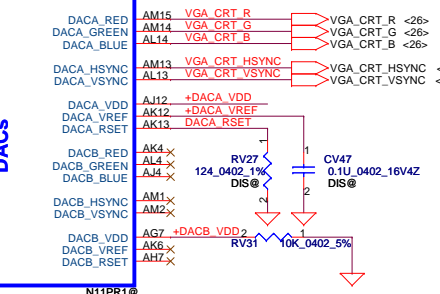
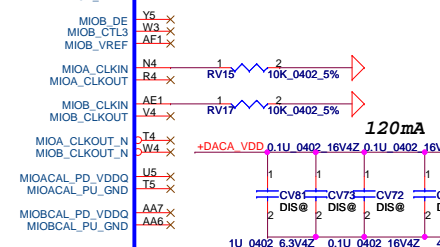
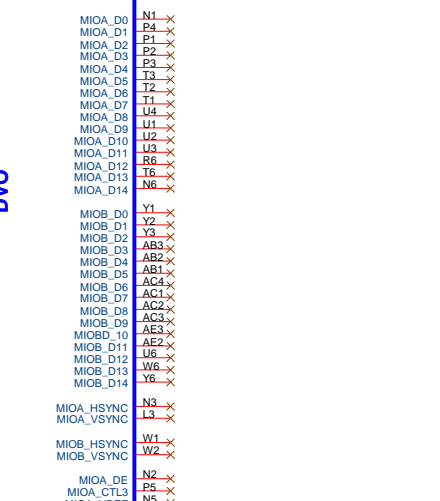
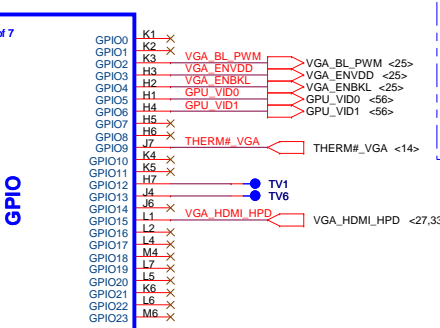
Lane Reversal

PCIE GTX C CRX P15	CV43	1	2	0.1U_0402_16V7K	PCIE GTX CRX P15	AL17
PCIE GTX C CRX N15	CV44	1	2	0.1U_0402_16V7K	PCIE GTX CRX N15	AN17
PCIE GTX C CRX P14	CV41	1	2	0.1U_0402_16V7K	PCIE GTX CRX P14	AL19
PCIE GTX C CRX N14	CV42	1	2	0.1U_0402_16V7K	PCIE GTX CRX N14	AN19
PCIE GTX C CRX P13	CV39	1	2	0.1U_0402_16V7K	PCIE GTX CRX P13	AL19
PCIE GTX C CRX N13	CV40	1	2	0.1U_0402_16V7K	PCIE GTX CRX N13	AN19
PCIE GTX C CRX P12	CV37	1	2	0.1U_0402_16V7K	PCIE GTX CRX P12	AL20
PCIE GTX C CRX N12	CV38	1	2	0.1U_0402_16V7K	PCIE GTX CRX N12	AN20
PCIE GTX C CRX P11	CV35	1	2	0.1U_0402_16V7K	PCIE GTX CRX P11	AL21
PCIE GTX C CRX N11	CV36	1	2	0.1U_0402_16V7K	PCIE GTX CRX N11	AN21
PCIE GTX C CRX P10	CV33	1	2	0.1U_0402_16V7K	PCIE GTX CRX P10	AL22
PCIE GTX C CRX N10	CV34	1	2	0.1U_0402_16V7K	PCIE GTX CRX N10	AN22
PCIE GTX C CRX P9	CV31	1	2	0.1U_0402_16V7K	PCIE GTX CRX P9	AL23
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PCIE GTX C CRX P5	CV23	1	2	0.1U_0402_16V7K	PCIE GTX CRX P5	AL27
PCIE GTX C CRX N5	CV24	1	2	0.1U_0402_16V7K	PCIE GTX CRX N5	AL28
PCIE GTX C CRX P4	CV21	1	2	0.1U_0402_16V7K	PCIE GTX CRX P4	AL28
PCIE GTX C CRX N4	CV22	1	2	0.1U_0402_16V7K	PCIE GTX CRX N4	AL28
PCIE GTX C CRX P3	CV19	1	2	0.1U_0402_16V7K	PCIE GTX CRX P3	AL29
PCIE GTX C CRX N3	CV20	1	2	0.1U_0402_16V7K	PCIE GTX CRX N3	AL29
PCIE GTX C CRX P2	CV17	1	2	0.1U_0402_16V7K	PCIE GTX CRX P2	AL29
PCIE GTX C CRX N2	CV18	1	2	0.1U_0402_16V7K	PCIE GTX CRX N2	AL29
PCIE GTX C CRX P1	CV15	1	2	0.1U_0402_16V7K	PCIE GTX CRX P1	AL30
PCIE GTX C CRX N1	CV16	1	2	0.1U_0402_16V7K	PCIE GTX CRX N1	AL32
PCIE GTX C CRX P0	CV13	1	2	0.1U_0402_16V7K	PCIE GTX CRX P0	AL32
PCIE GTX C CRX N0	CV14	1	2	0.1U_0402_16V7K	PCIE GTX CRX N0	AL32



Lane Reversal

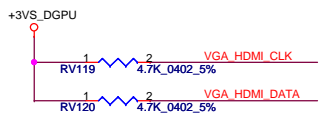
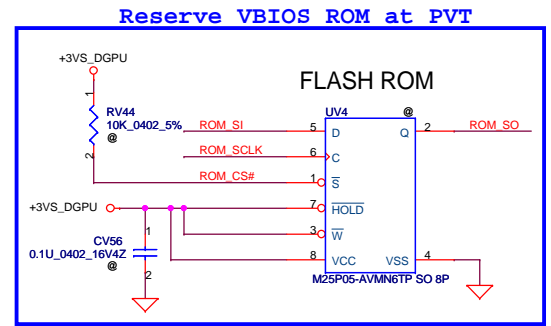
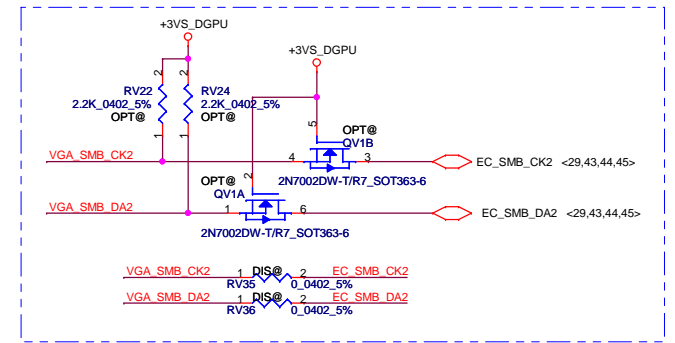
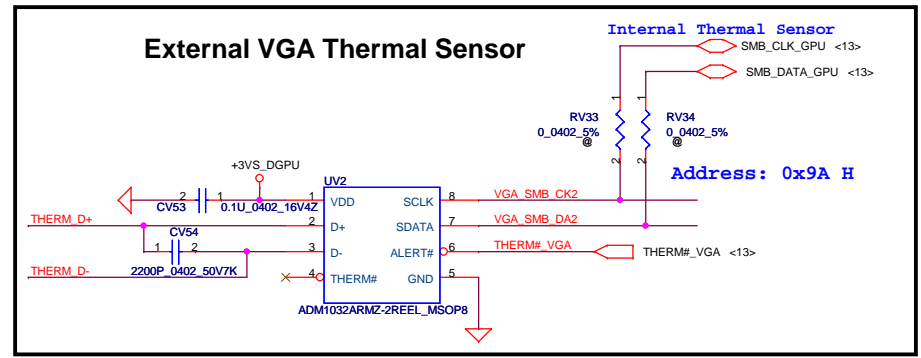
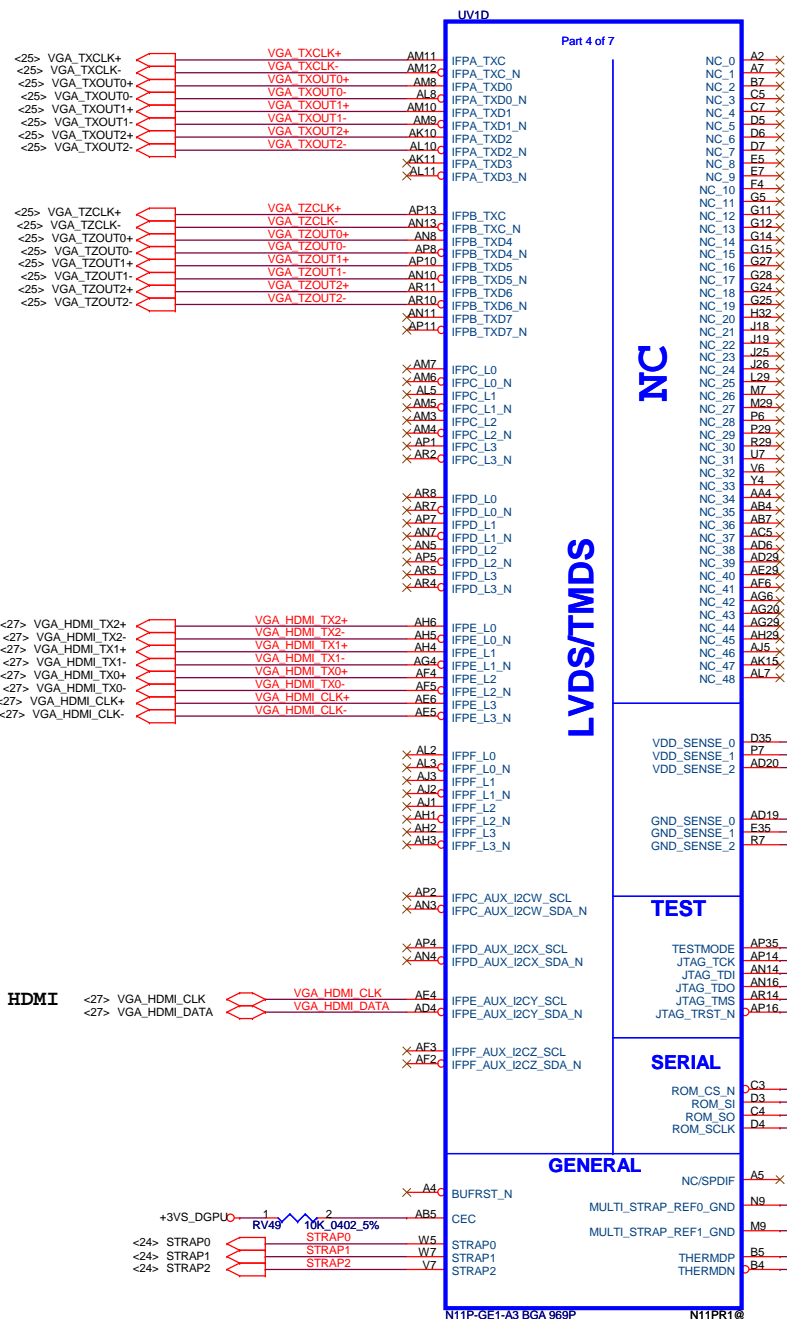
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PCIE GTX C GRX P13	AR19
PCIE GTX C GRX N13	AR20
PCIE GTX C GRX P12	AR20
PCIE GTX C GRX N12	AN22
PCIE GTX C GRX P11	AN22
PCIE GTX C GRX N11	AP22
PCIE GTX C GRX N10	AR22
PCIE GTX C GRX P9	AP23
PCIE GTX C GRX N9	AN23
PCIE GTX C GRX N8	AN25
PCIE GTX C GRX P7	AR25
PCIE GTX C GRX N7	AR26
PCIE GTX C GRX P6	AP26
PCIE GTX C GRX N6	AN26
PCIE GTX C GRX P5	AN26
PCIE GTX C GRX N5	AP28
PCIE GTX C GRX P4	AR28
PCIE GTX C GRX N4	AN29
PCIE GTX C GRX P3	AP29
PCIE GTX C GRX N3	AN29
PCIE GTX C GRX P2	AN31
PCIE GTX C GRX N2	AR31
PCIE GTX C GRX P1	AR32
PCIE GTX C GRX N1	AN32
PCIE GTX C GRX P0	AR34
PCIE GTX C GRX N0	AP34



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Compal Secret Data		Compal Electronics, Inc.	
PCIE/DAC/GPIO			
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Title		Compal Electronics, Inc.	
		LVDS/HDMI/DP/THM	
Document Number	NWQAA LA-6062P M/B		
Date	Wednesday, March 24, 2010	Sheet	14 of 59

N11E-GE1-LP Performance Mode

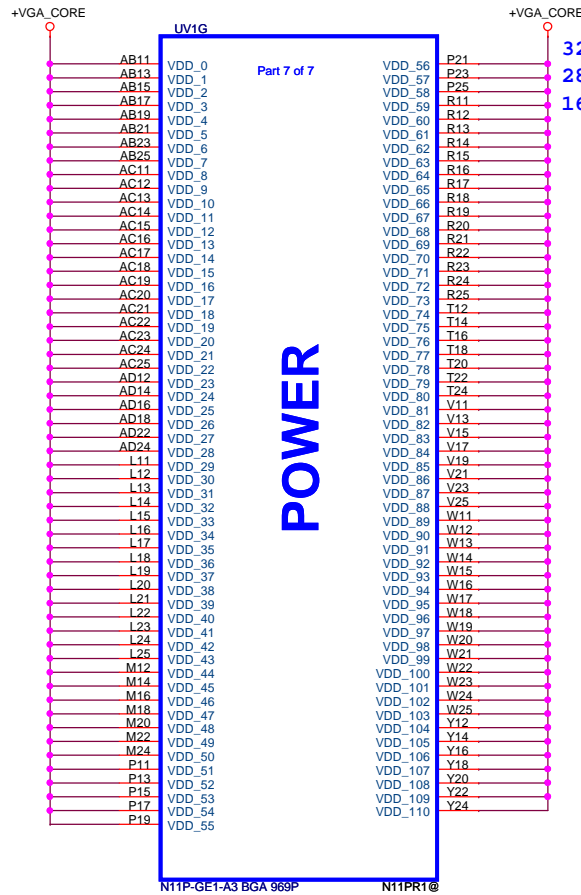
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	450	790	0.90 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11P-GE1 Performance Mode

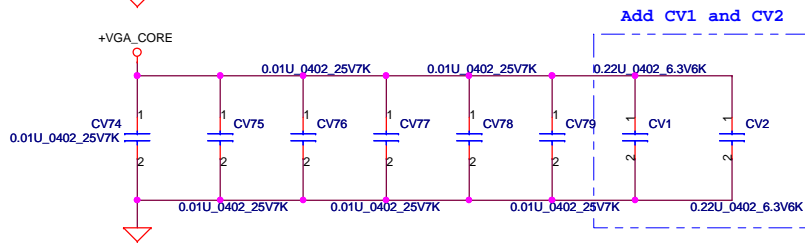
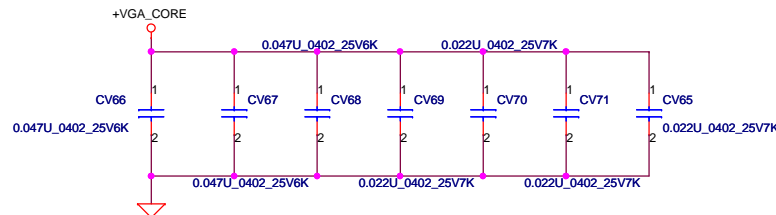
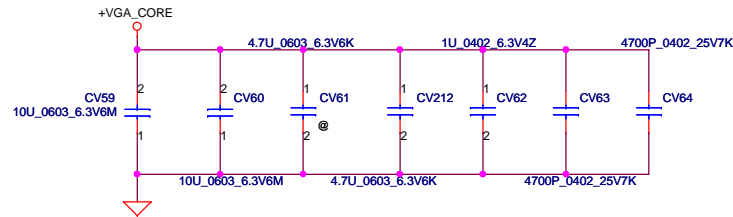
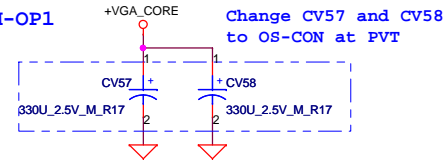
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	575	790	0.95 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11M-GE1 & N11M-OP1 Performance Mode

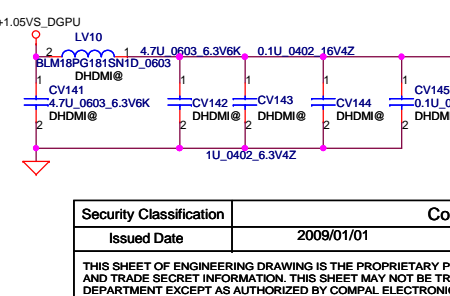
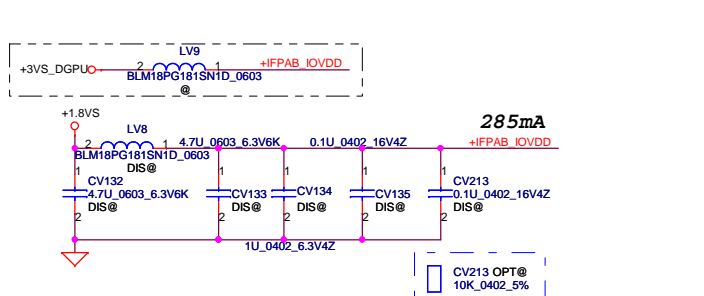
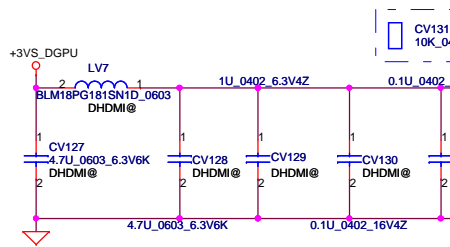
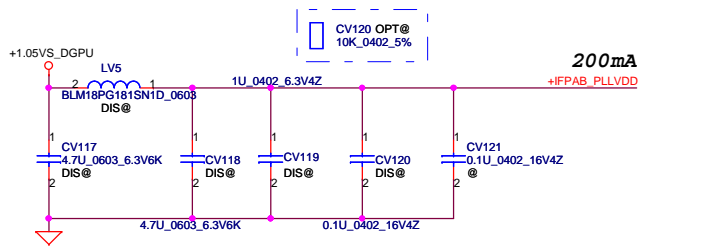
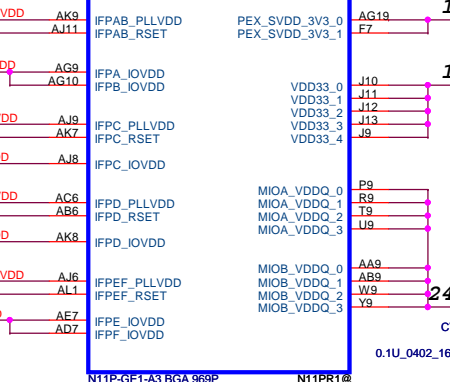
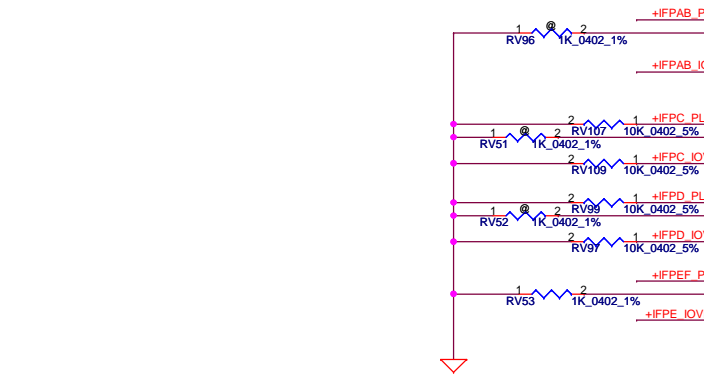
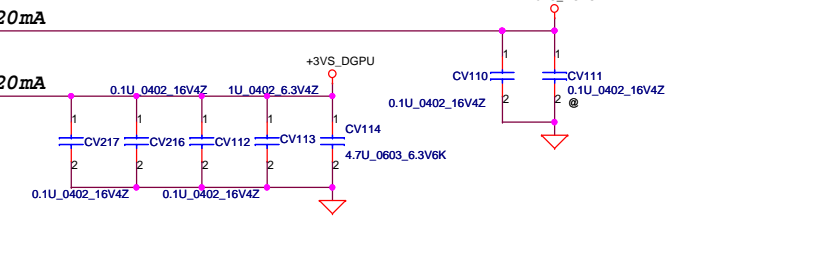
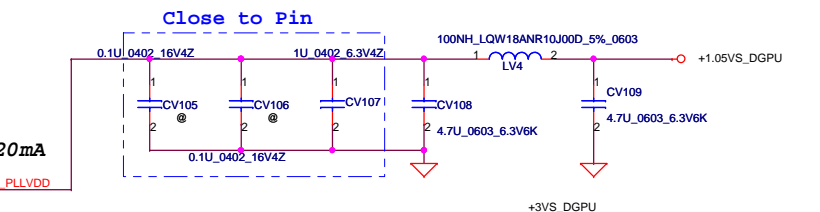
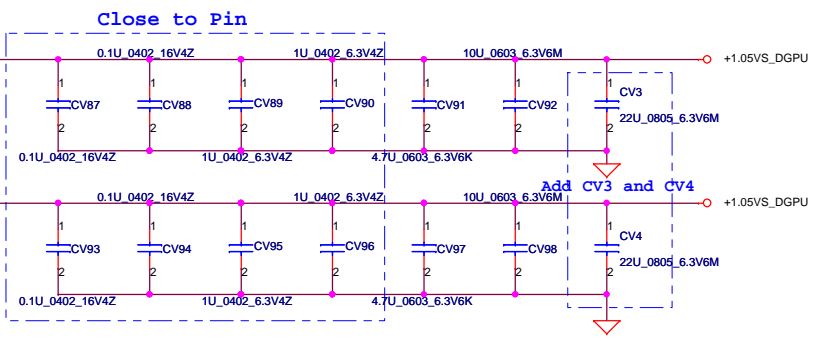
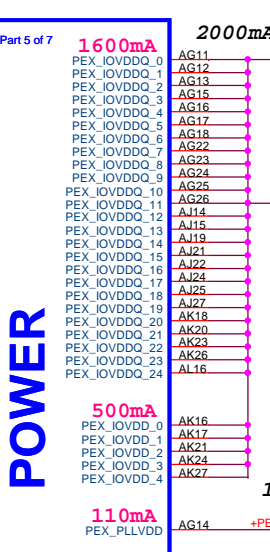
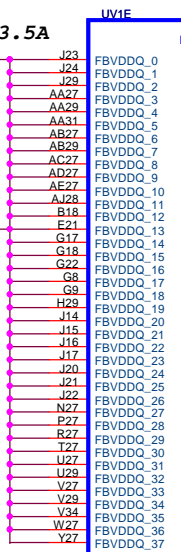
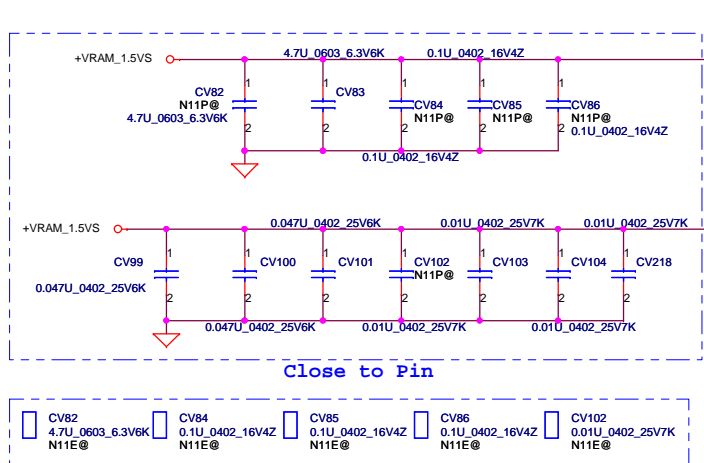
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	625	790	1.03 V
P8	405	405	0.85 V
P12	135	135	0.85 V



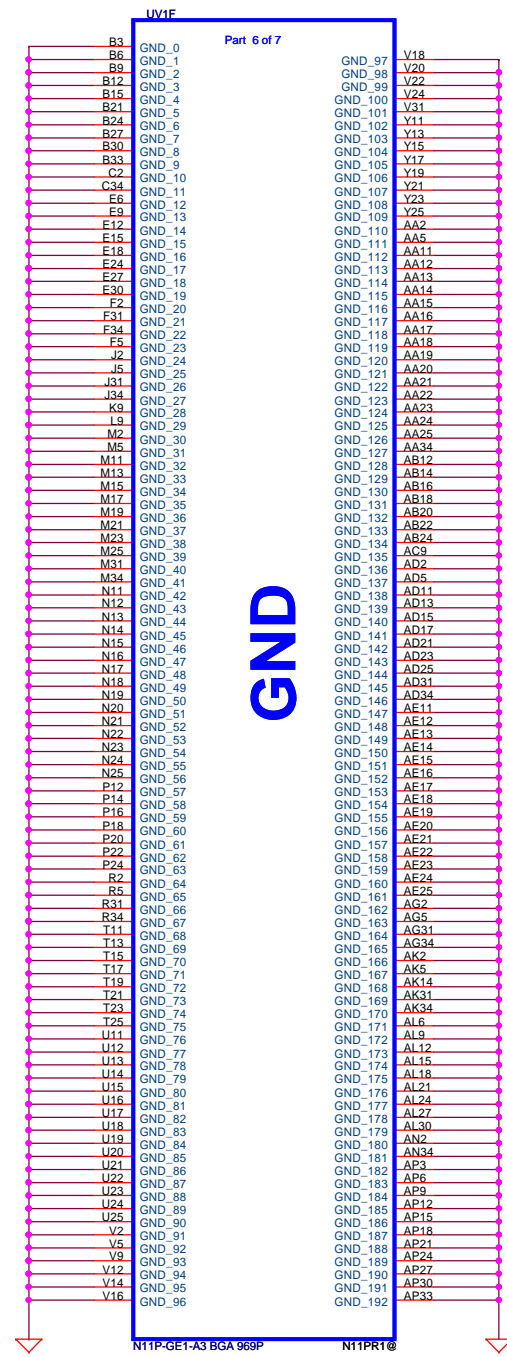
32A for N11E-GE1-LP
 28A for N11P-GE1
 16A for N11M-GE1 & N11M-OP1



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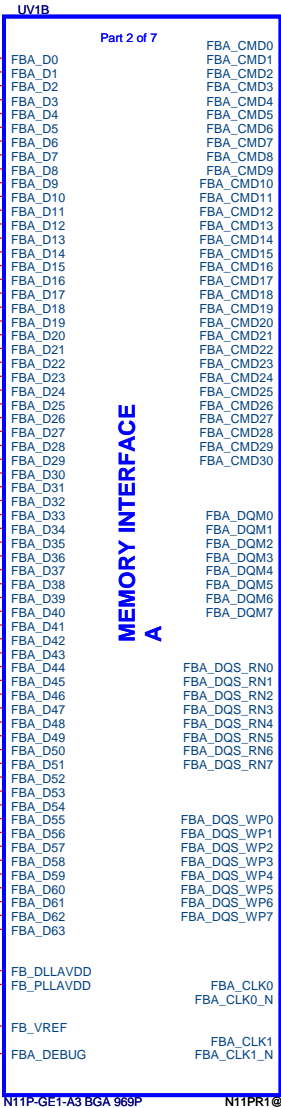


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				NWQAA LA-6062P M/B	
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				Tuesday, March 23, 2010	2.0
				Sheet	of
				16	59



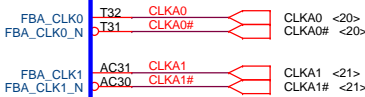
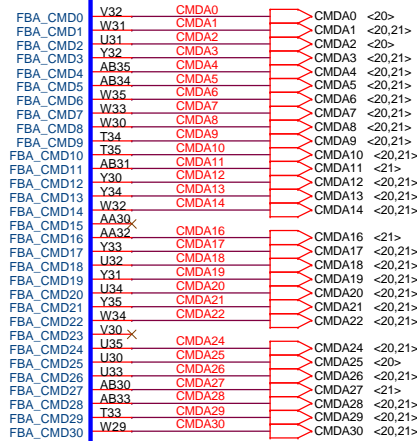
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GND		
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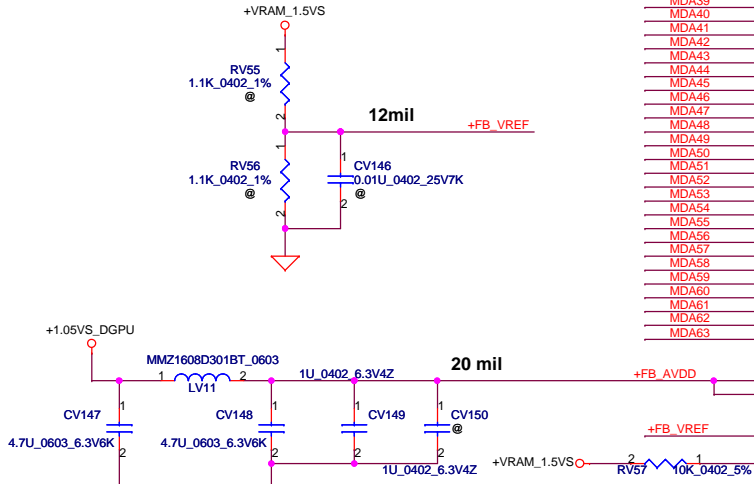
MEMORY INTERFACE A

Part 2 of 7



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2



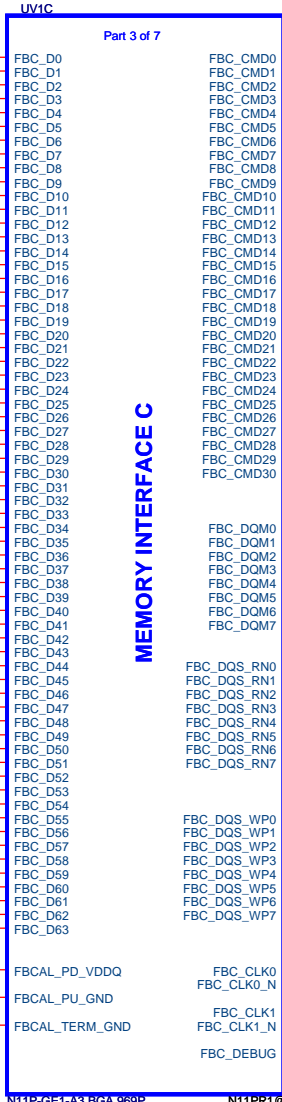
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Compal Electronics, Inc.	
MEM Interface A	
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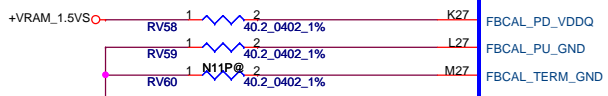
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- MDB2 A13
- MDB3 FBC_D3
- MDB4 C16
- MDB5 B16
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- MDB7 D16
- MDB8 C13
- MDB9 B11
- MDB10 A11
- MDB11 D11
- MDB12 C10
- MDB13 B8
- MDB14 A8
- MDB15 E8
- MDB16 F8
- MDB17 A9
- MDB18 D18
- MDB19 C19
- MDB20 B12
- MDB21 D11
- MDB22 E11
- MDB23 D12
- MDB24 F13
- MDB25 B13
- MDB26 F14
- MDB27 E15
- MDB28 E16
- MDB29 F16
- MDB30 F17
- MDB31 D29
- MDB32 F27
- MDB33 E28
- MDB34 D26
- MDB35 F25
- MDB36 D24
- MDB37 E25
- MDB38 F32
- MDB39 E32
- MDB40 D33
- MDB41 E31
- MDB42 C33
- MDB43 F29
- MDB44 D30
- MDB45 E29
- MDB46 B29
- MDB47 C31
- MDB48 C29
- MDB49 B31
- MDB50 C32
- MDB51 B32
- MDB52 B35
- MDB53 B34
- MDB54 A29
- MDB55 B28
- MDB56 A28
- MDB57 C28
- MDB58 C26
- MDB59 D25
- MDB60 B25
- MDB61 A25
- MDB62 FBC_D62
- MDB63 FBC_D63



- C17 CMDB0
- B19 CMDB1
- F21 CMDB3
- A23 CMDB4
- D21 CMDB5
- B23 CMDB6
- E20 CMDB7
- G21 CMDB8
- F20 CMDB9
- F19 CMDB10
- F23 CMDB11
- A22 CMDB12
- C22 CMDB13
- B17 CMDB14
- F24 X CMDB16
- C25 X CMDB17
- E22 CMDB18
- B22 CMDB19
- A19 CMDB20
- D22 CMDB21
- D20 CMDB22
- E19 X CMDB24
- F18 CMDB25
- C19 CMDB26
- F22 CMDB27
- C23 CMDB28
- B20 CMDB29
- A20 CMDB30

- A16 DQMB0
- D10 DQMB1
- F11 DQMB2
- D15 DQMB3
- D27 DQMB4
- D34 DQMB5
- A34 DQMB6
- D28 DQMB7
- B14 DQSB#0
- B10 DQSB#1
- D9 DQSB#2
- E14 DQSB#3
- F26 DQSB#4
- D31 DQSB#5
- A31 DQSB#6
- A26 DQSB#7
- C14 DQSB0
- A10 DQSB1
- F10 DQSB2
- D14 DQSB3
- E26 DQSB4
- D32 DQSB5
- A32 DQSB6
- B26 DQSB7

- E17 CLKB0
- D17 CLKB0#
- D23 CLKB1
- E23 CLKB1#
- G19 N11P@



- RV60 N11MGE@ 60.4_0402_1%
- RV60 N11MOP@ 60.4_0402_1%
- RV60 N11E@ 40.2_0402_1%

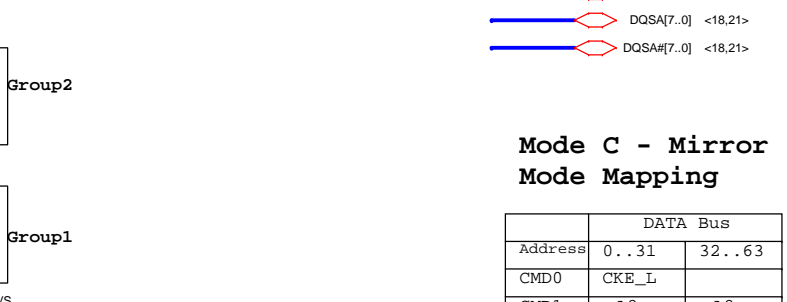
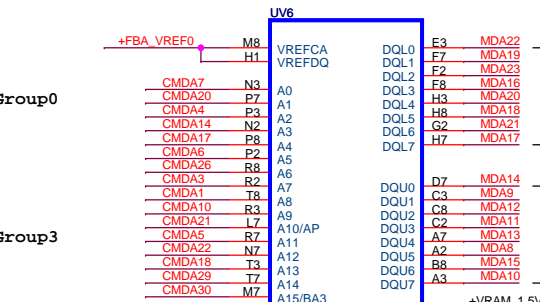
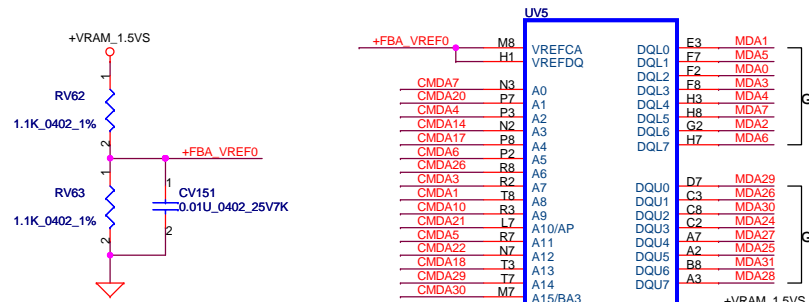
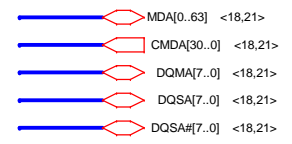
- RV61 N11E@ 10K_0402_5%

Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT#	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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				Document Number	NWQAA LA-6062P M/B
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				Sheet	19 of 59
				Rev	2.0

Memory Partition A - Lower 32 bits

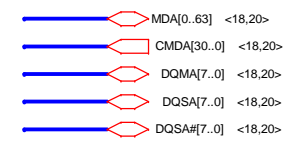
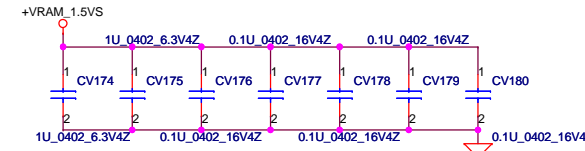
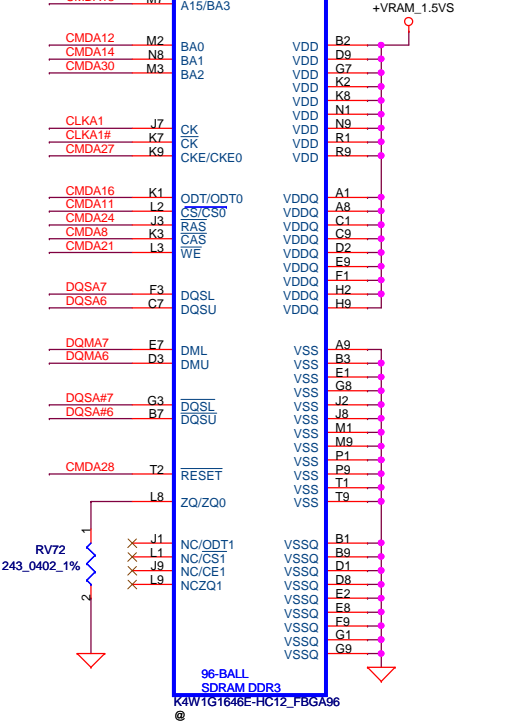
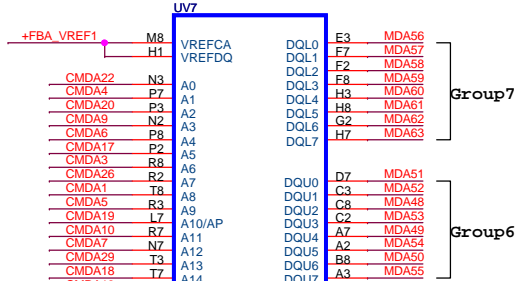
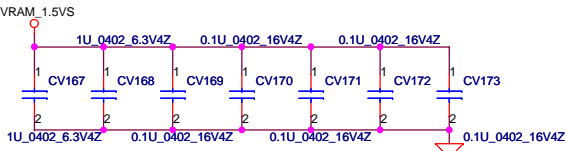
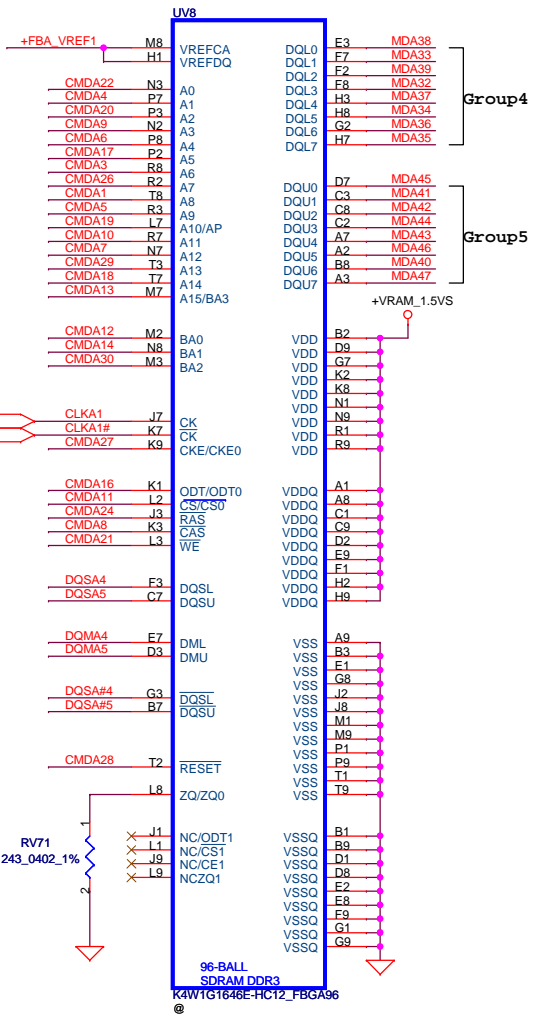
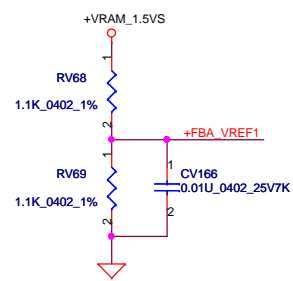


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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Memory Partition A - Upper 32 bits

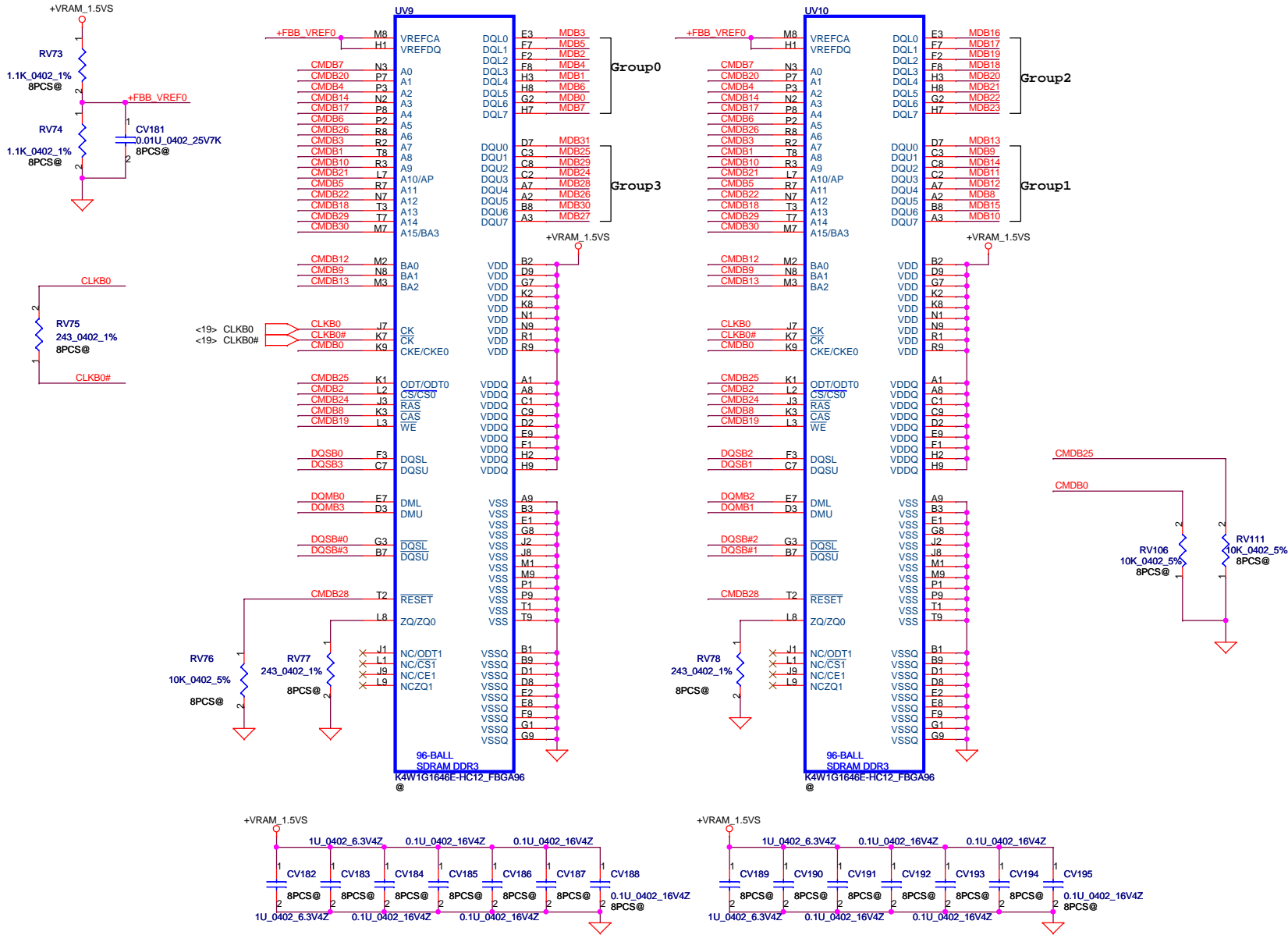


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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				NWQAA LA-6062P M/B	2.0
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Memory Partition C - Lower 32 bits



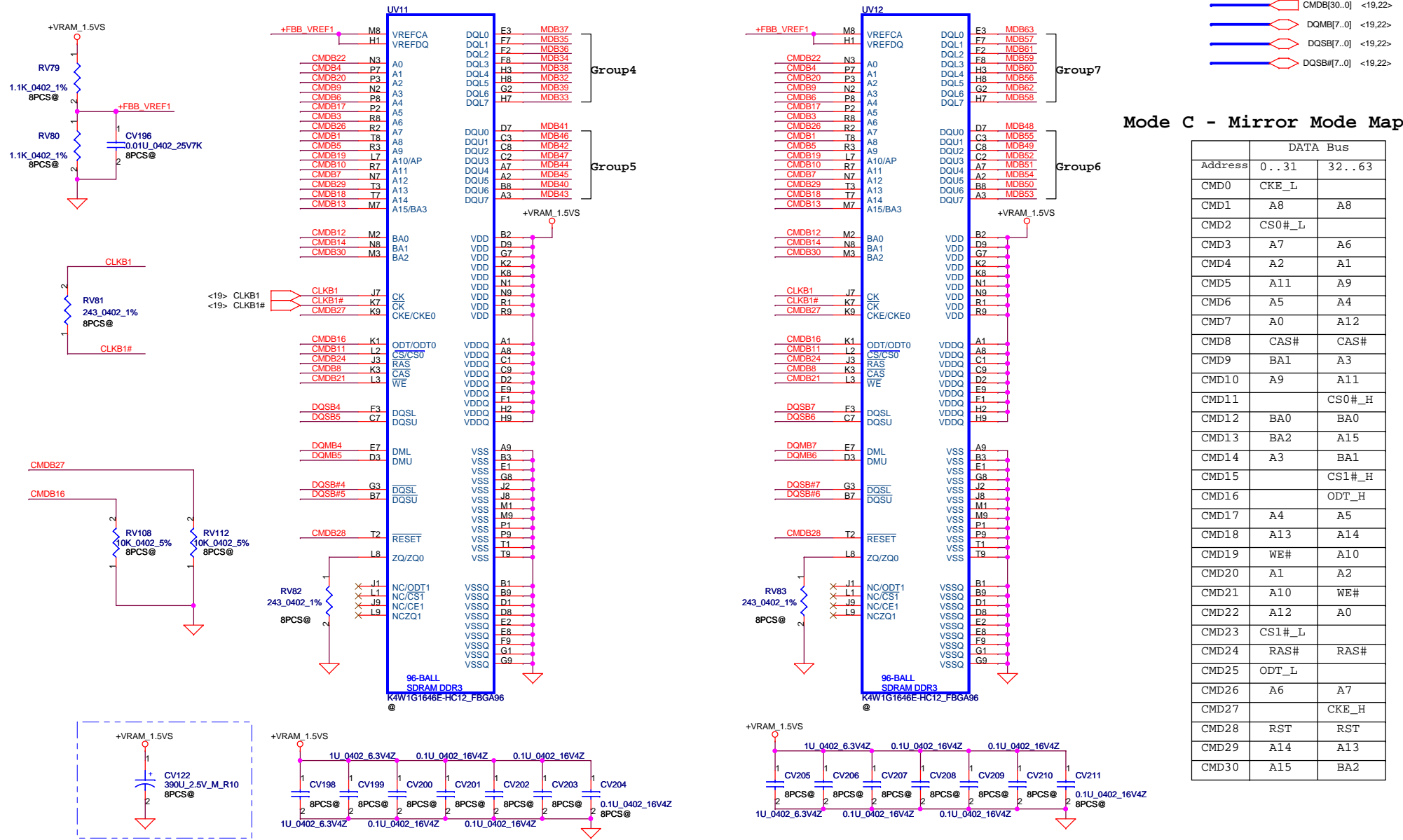
Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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VRAM C Lower	
Document Number	Rev 2.0
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Date: Wednesday, March 24, 2010	Sheet 22 of 59

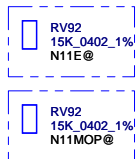
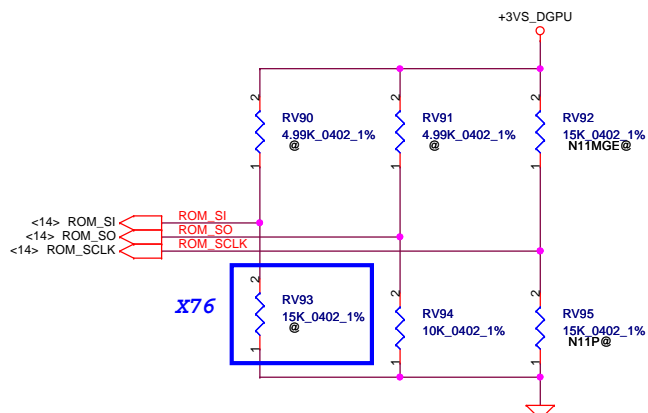
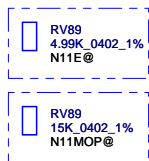
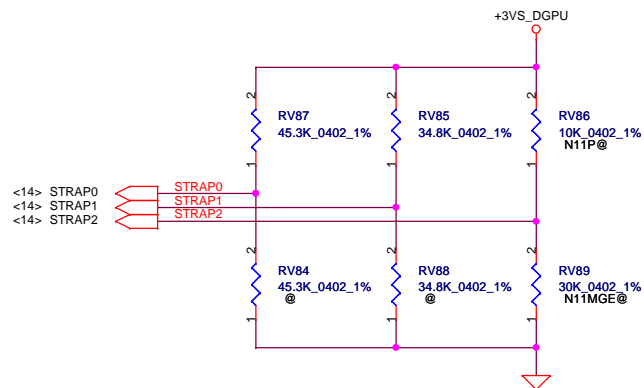
Memory Partition C - Upper 32 bits



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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



X76

	DeviceID	ROM_SCLK	STRAP2
N11M-GE1	0xA75	Pull up 15K	Pull down 30K
N11P-GE1	0xA29	Pull down 15K	Pull up 10K
N11M-OP1	0xA72	Pull up 15K	Pull down 15K
N11E-GE1(LP)	0xCB0	Pull up 15K	Pull down 5K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K	SD034150280
	1G	0010	PD 15K	
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K	SD034200280
	1G	0011	PD 20K	

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

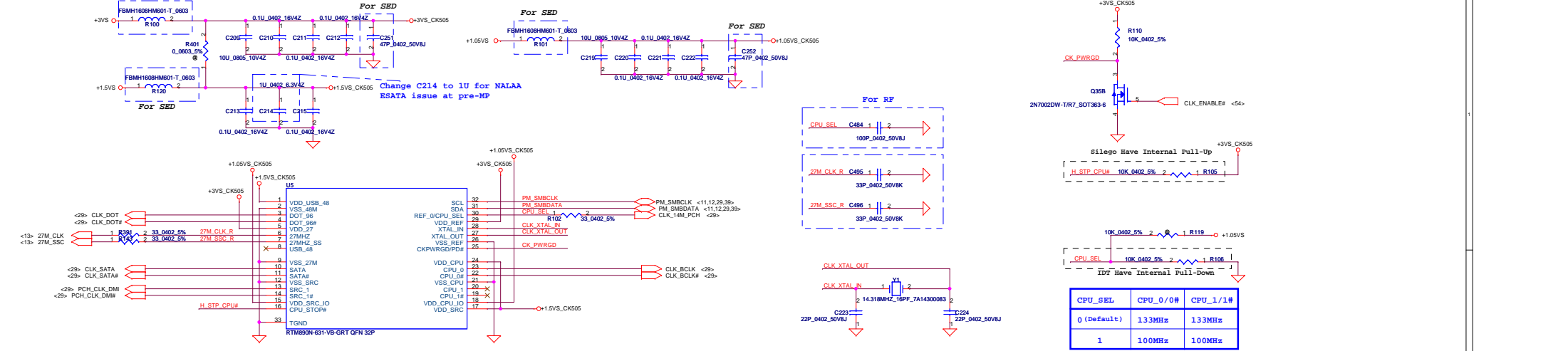
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

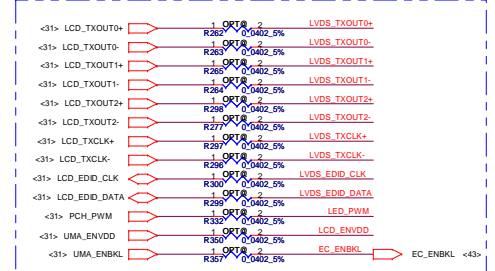
Security Classification	Compal Secret Data	
Issued Date	2009/01/01	Deciphered Date
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Title	MSIC
Document Number	NWQAA LA-6062P M/B
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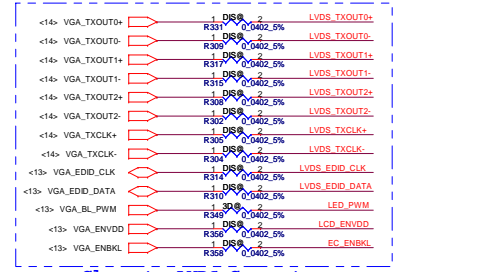
Clock Generator



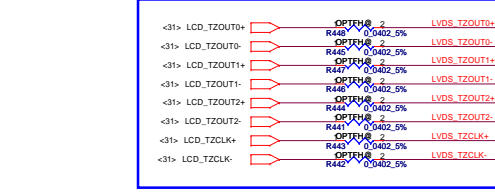
OPTIMUS



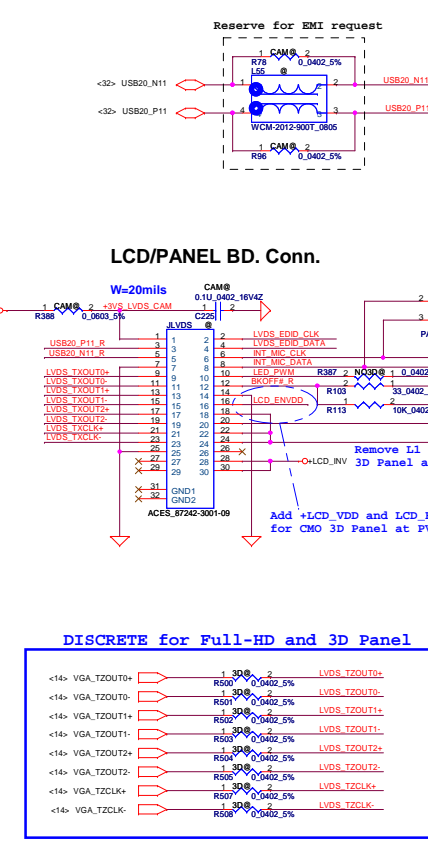
DISCRETE



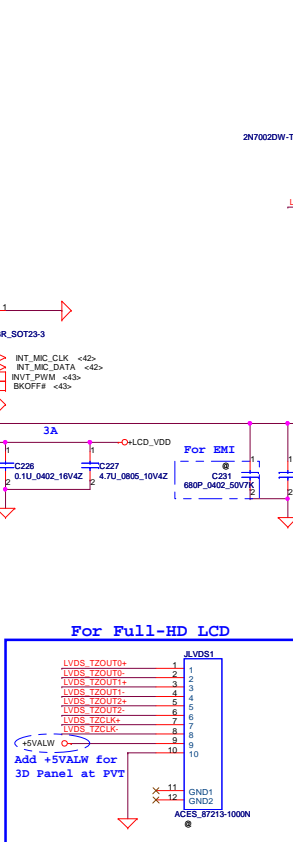
OPTIMUS for Full-HD



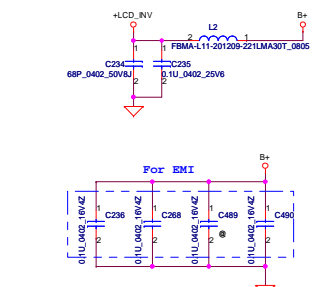
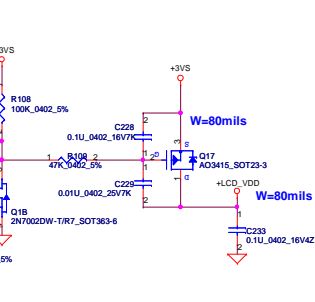
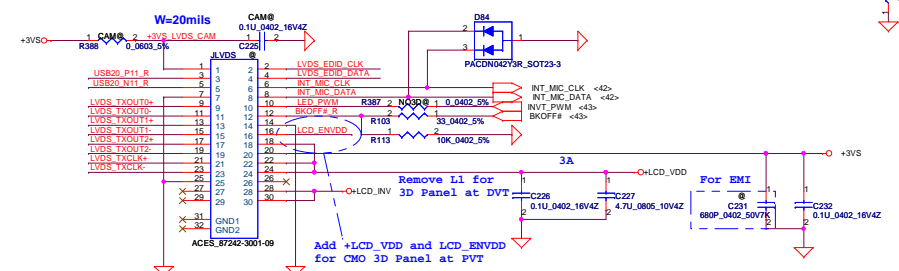
DISCRETE for Full-HD and 3D Panel



For Full-HD LCD



LCD/PANEL BD. Conn.



CRT CONNECTOR

OPTIMUS

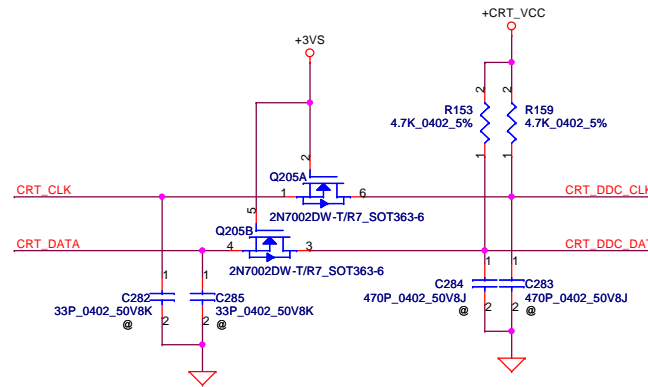
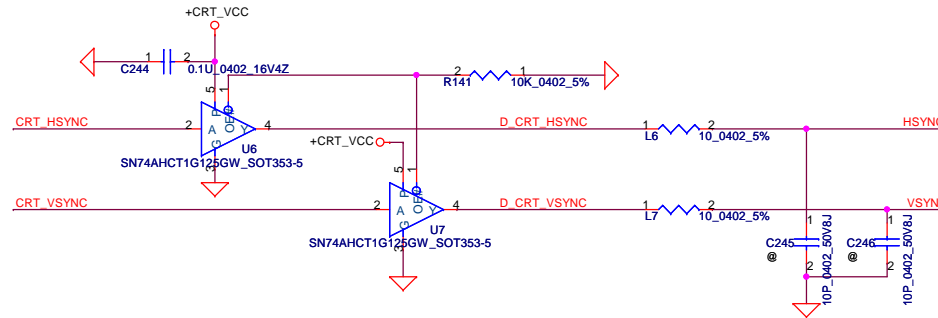
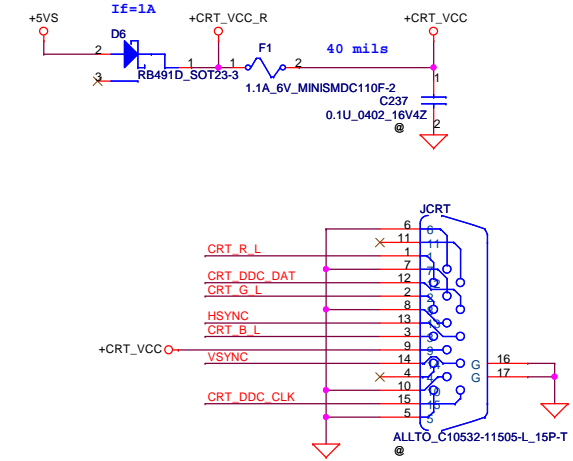
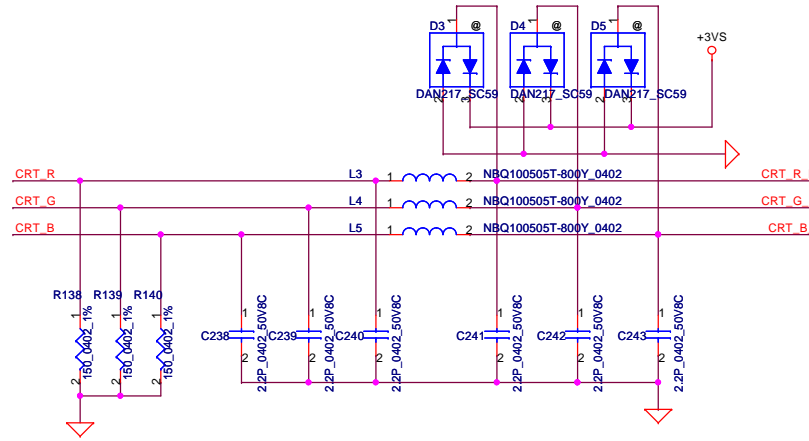
<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

Close to CRT Connector

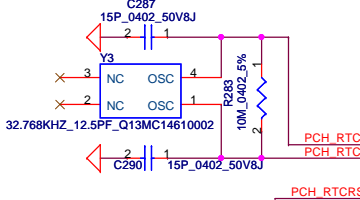
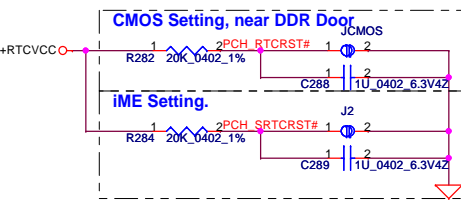
DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector



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Integrated SUS 1.05V VRM Enable

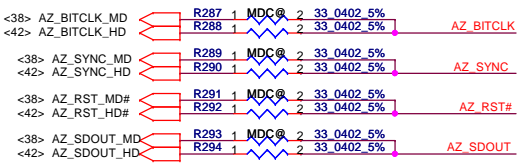
PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO
This signal has a weak internal pull down.
This signal can't PU

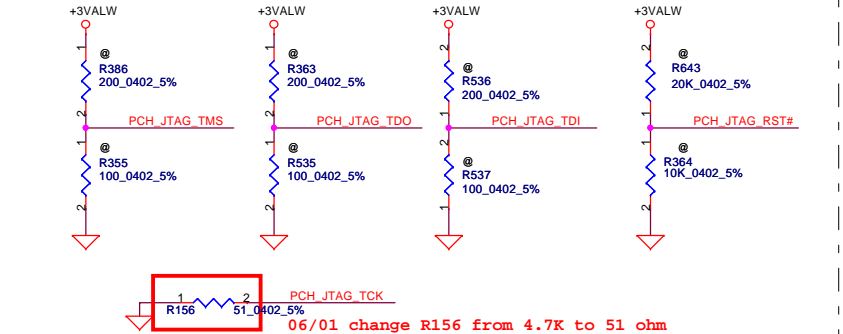
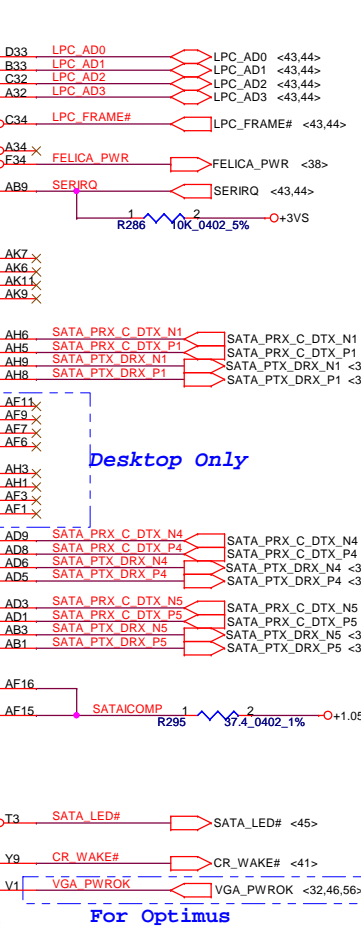
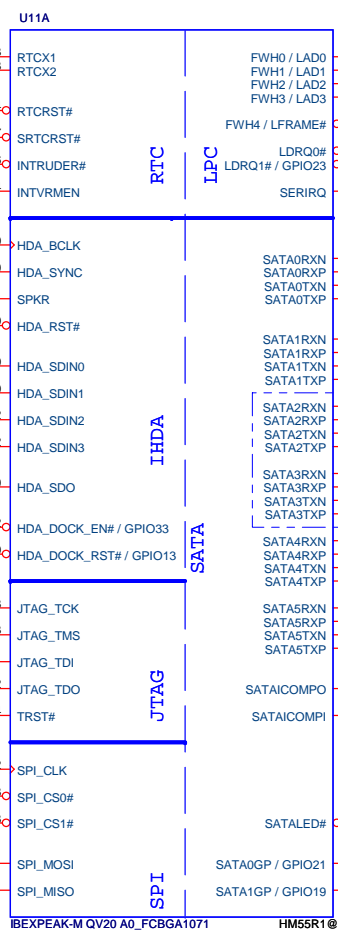
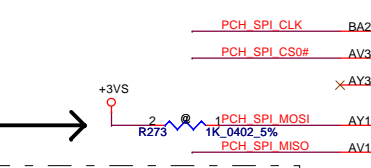
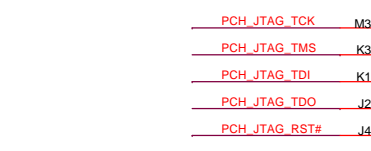
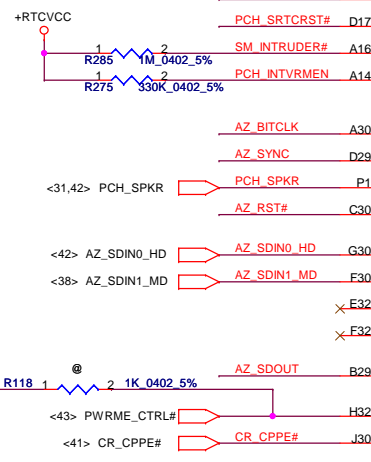
Flash Descriptor Security Override

HDA_DOCK_EN# Low = Enabled High = Disabled *

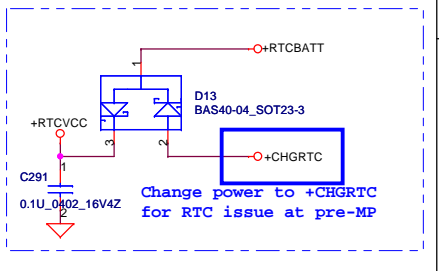
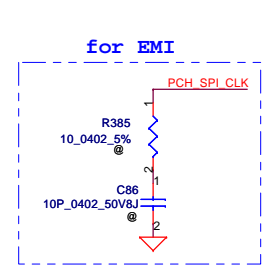
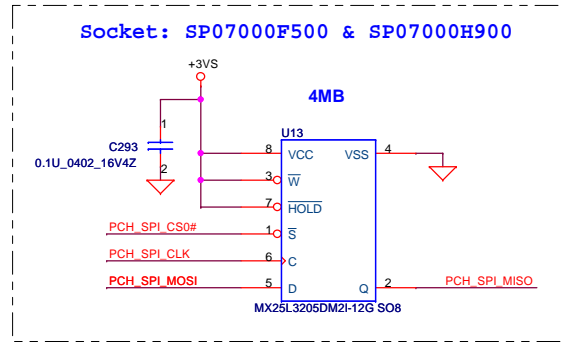


ITPM Enabled Internal: Pull down 20k

SPI_MOSI High = Enabled Low = Disabled (Default)



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDO	R536	200ohm	200ohm	20kohm	No Install
PCH_JTAG_TDI	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
PCH_JTAG_RST#	R353	10kohm	10kohm	No Install	No Install

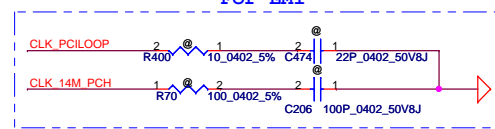
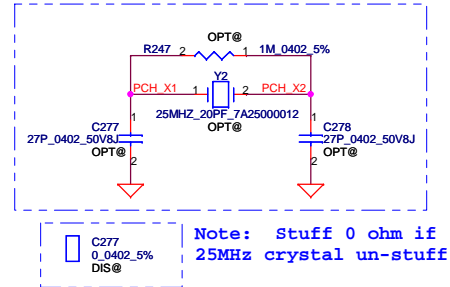
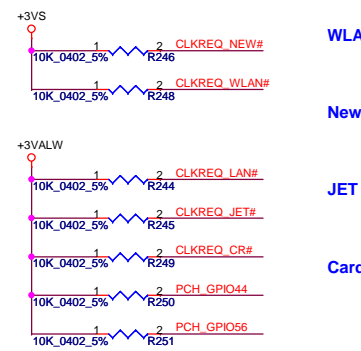
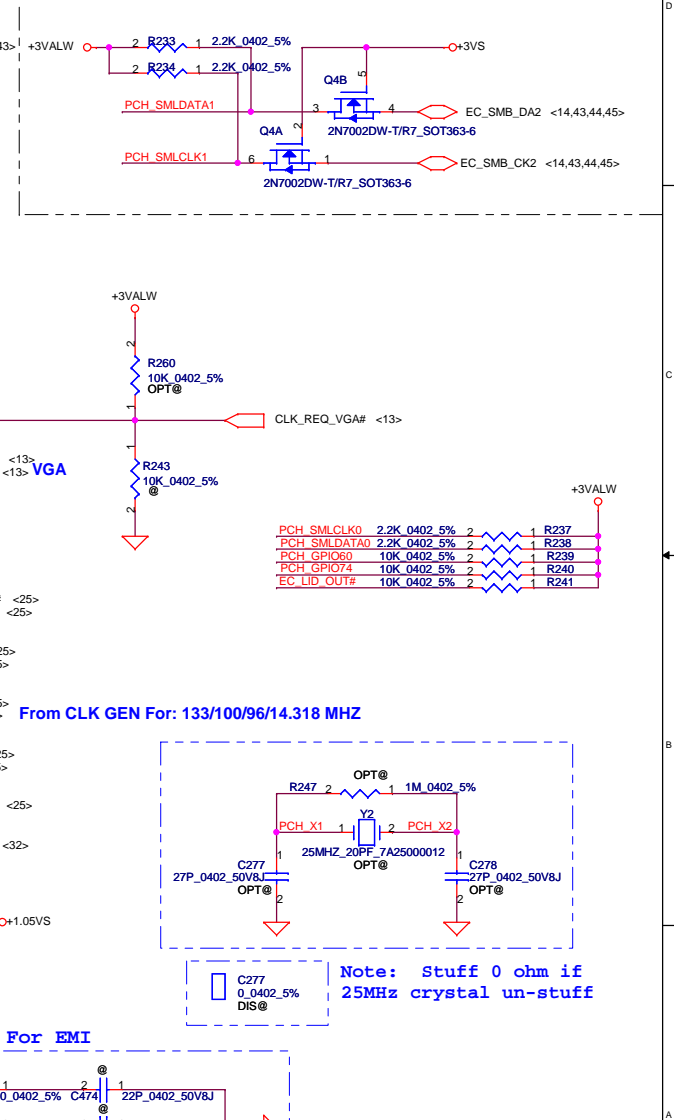
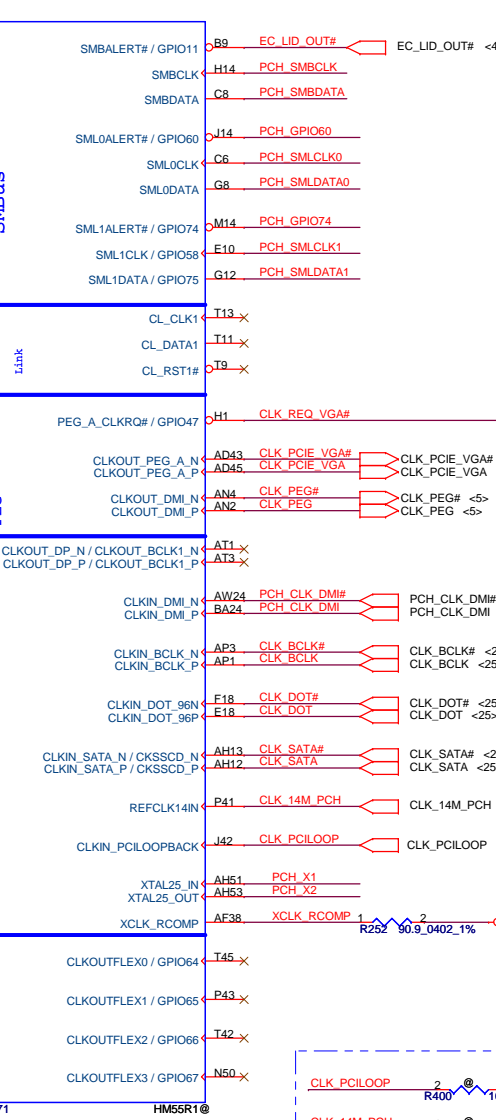
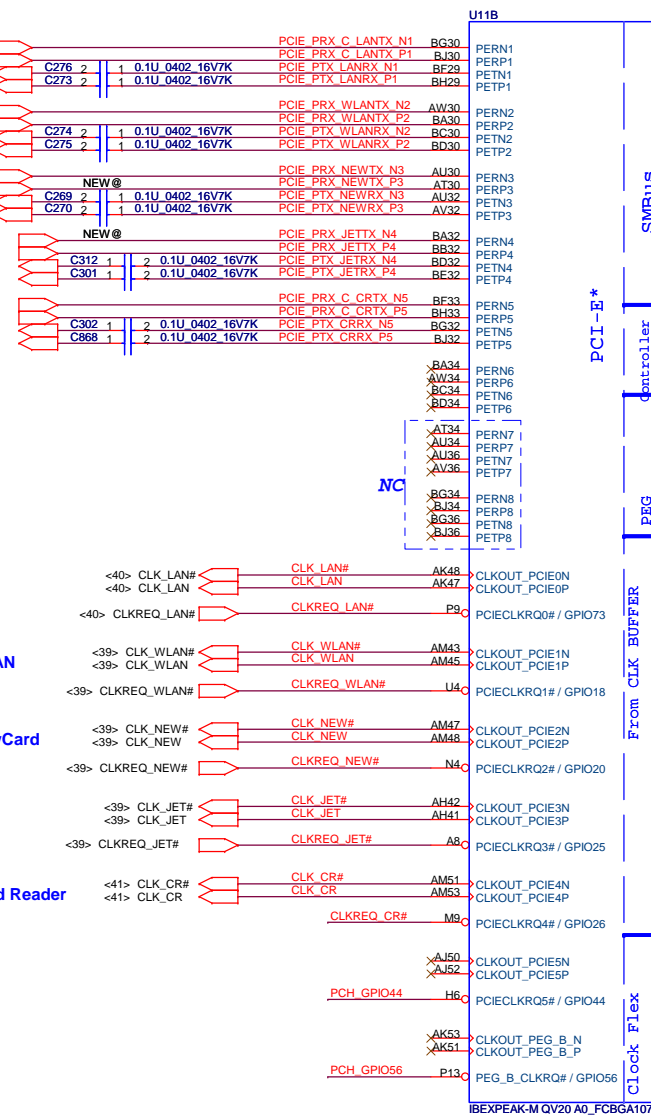


Security Classification		Compal Secret Data	
Issued Date	200910/9	Deciphered Date	2010/01/23

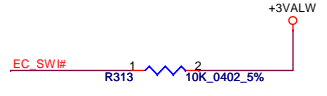
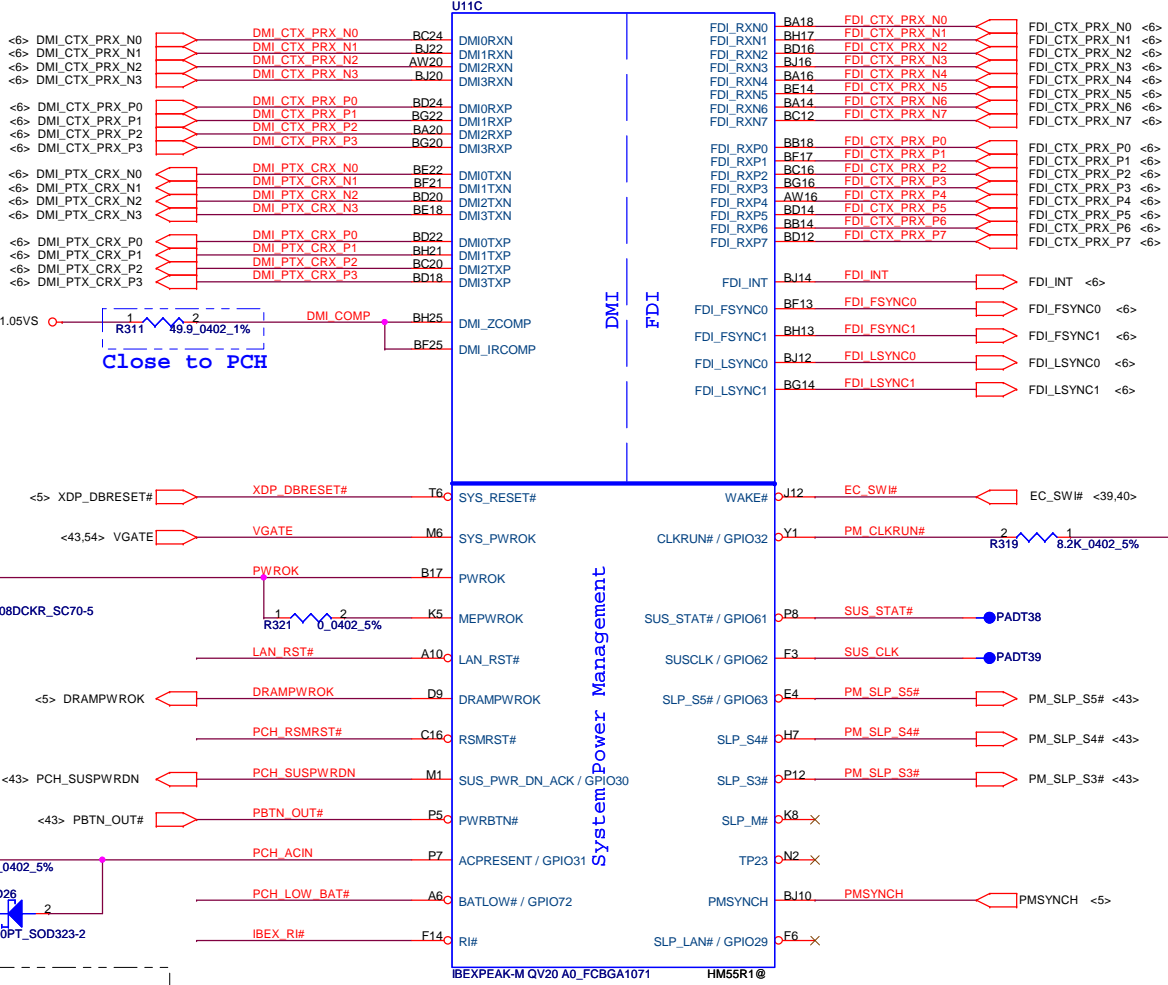
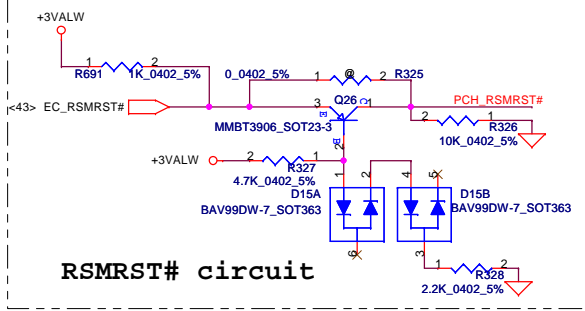
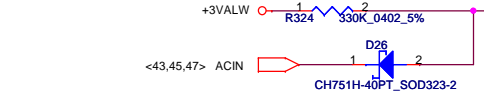
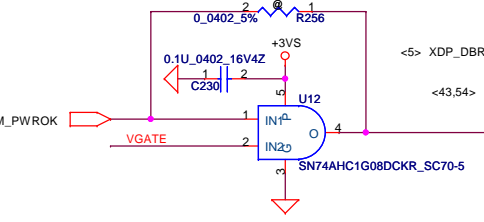
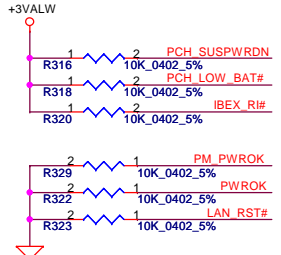
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Compal Electronics, Inc.			
PCH_SPI/SATA/LPC/RTC/HDA			
Size B	Document Number	Rev 2.0	
NWQAA LA-6062P M/B			
Date:	Wednesday, March 24, 2010	Sheet	28 of 59

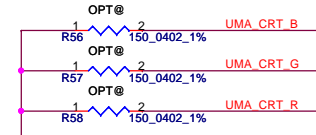
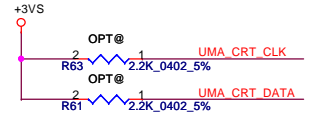
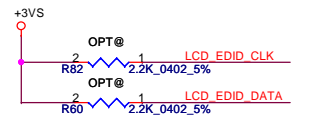
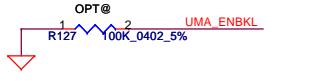
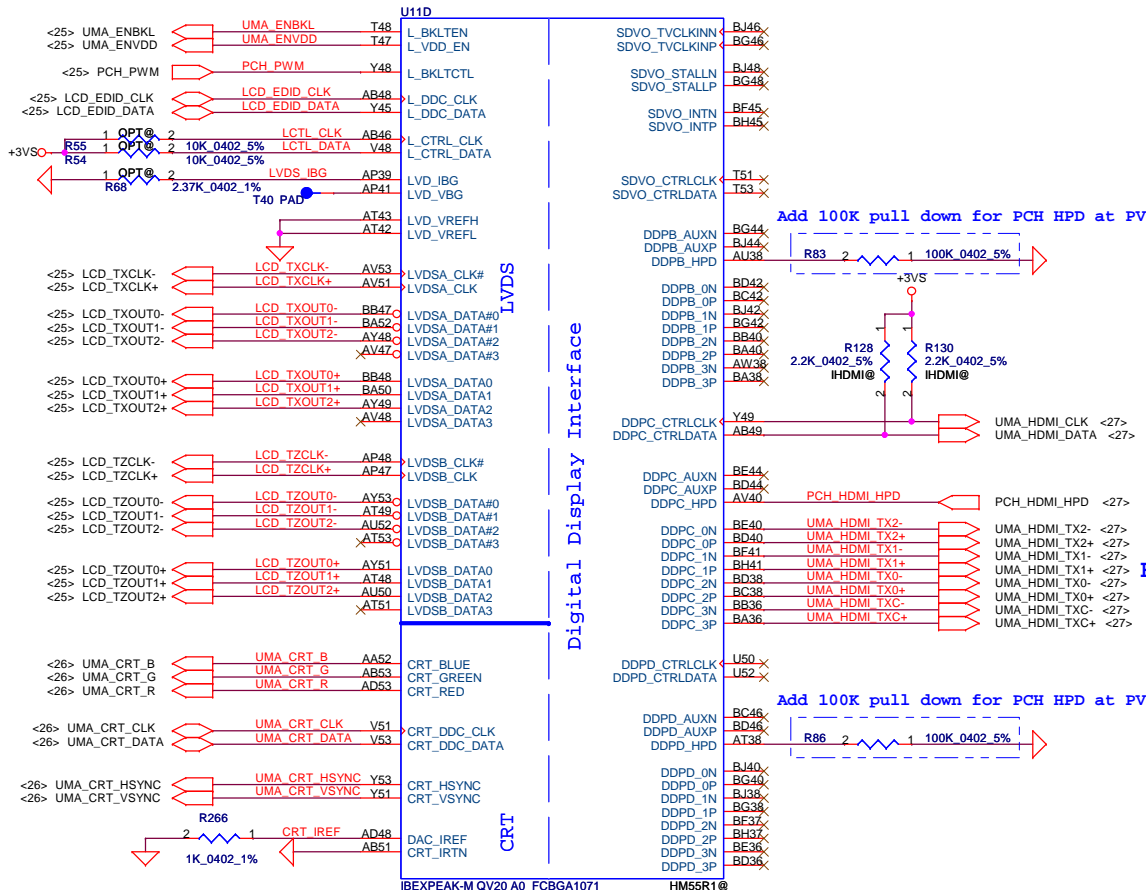
- For LAN**
 - <40> PCIE_PRX_C_LANTX_N1
 - <40> PCIE_PRX_C_LANTX_P1
 - <40> PCIE_PTX_C_LANRX_N1
 - <40> PCIE_PTX_C_LANRX_P1
- For WLAN**
 - <39> PCIE_PRX_WLANTX_N2
 - <39> PCIE_PRX_WLANTX_P2
 - <39> PCIE_PTX_C_WLANRX_N2
 - <39> PCIE_PTX_C_WLANRX_P2
- For NewCard**
 - <39> PCIE_PRX_NEWTX_N3
 - <39> PCIE_PRX_NEWTX_P3
 - <39> PCIE_PTX_C_NEWRX_N3
 - <39> PCIE_PTX_C_NEWRX_P3
- For JET**
 - <39> PCIE_PRX_JETTX_N4
 - <39> PCIE_PRX_JETTX_P4
 - <39> PCIE_PTX_C_JETRX_N4
 - <39> PCIE_PTX_C_JETRX_P4
- For Card Reader**
 - <41> PCIE_PRX_C_CRTX_N5
 - <41> PCIE_PRX_C_CRTX_P5
 - <41> PCIE_PTX_C_CRRX_N5
 - <41> PCIE_PTX_C_CRRX_P5



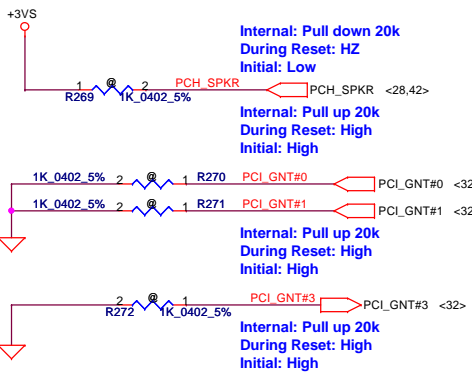
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
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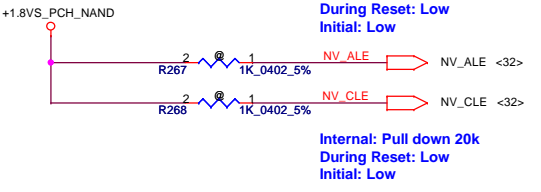
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

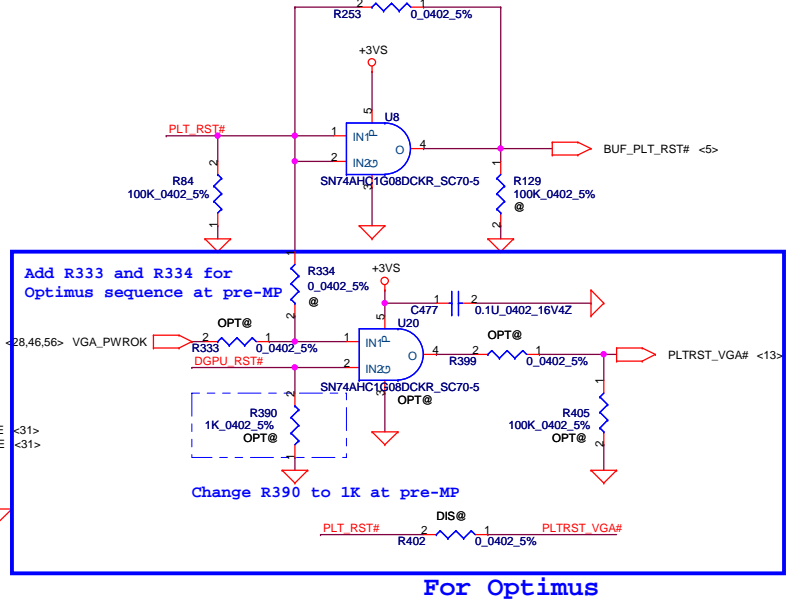
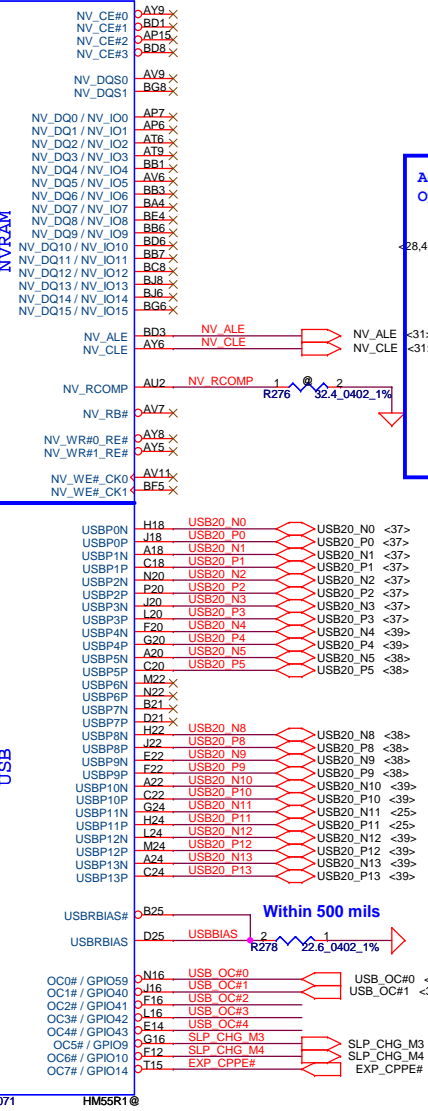
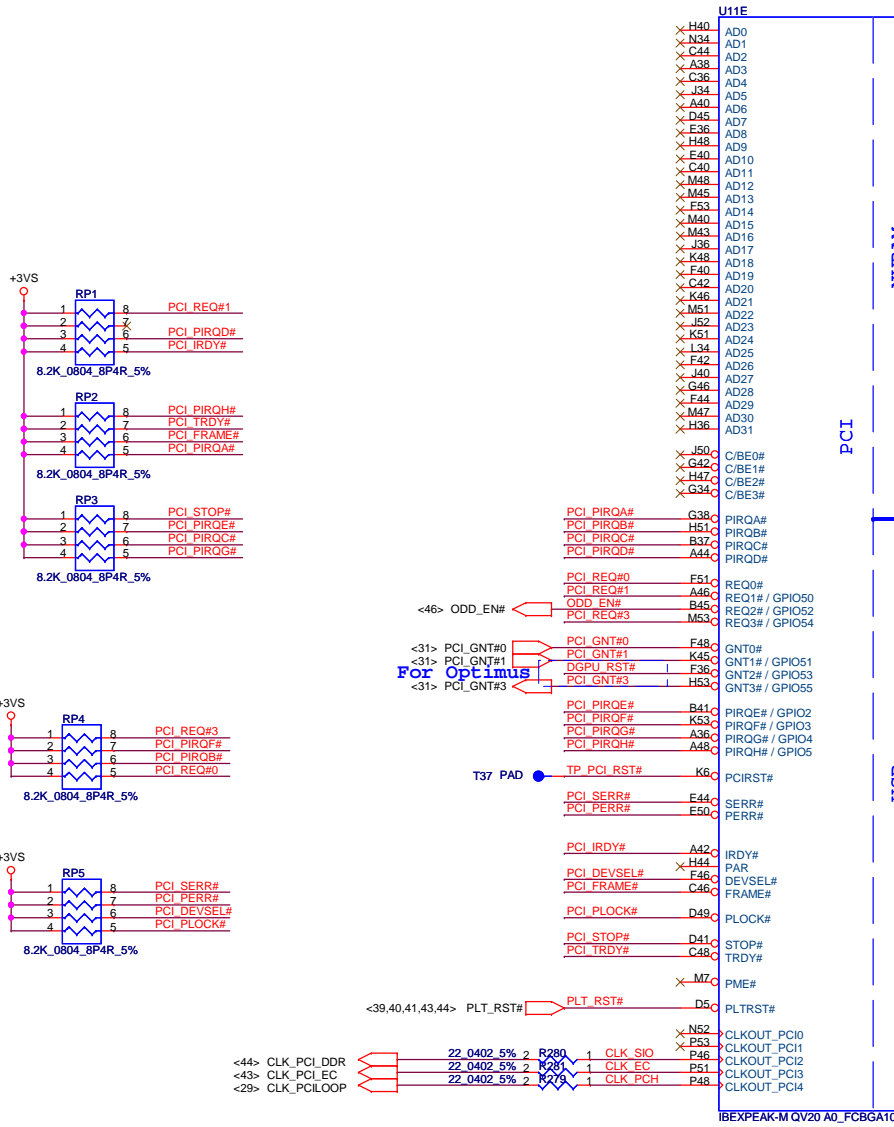
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable
	High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled
	Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default)
	High= Set to Vcc



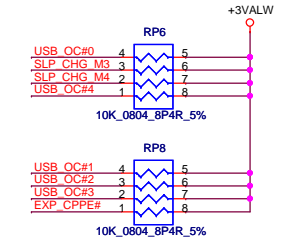
Add R333 and R334 for Optimus sequence at pre-MP

Change R390 to 1K at pre-MP

For Optimus

USB-RIGHT1
USB-RIGHT2
USB-Left1
eSATA-USB
NewCard
BT

Finger Printer
Felica
TV Tuner
Int. Camera
3G/ TV tuner
WiMax(WLAN)



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200910/9		2010/01/23		NWQA LA-6062P M/B	
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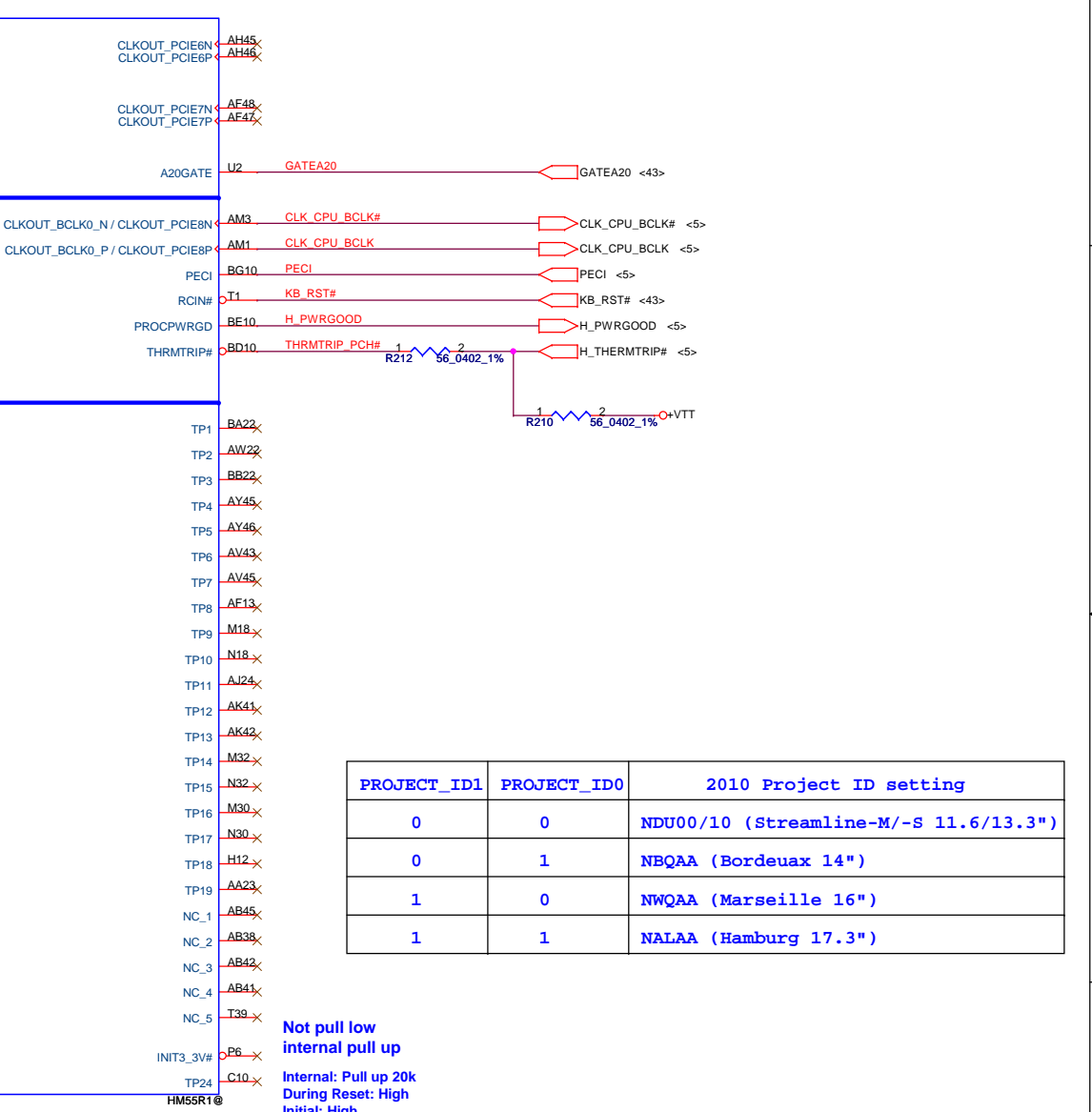
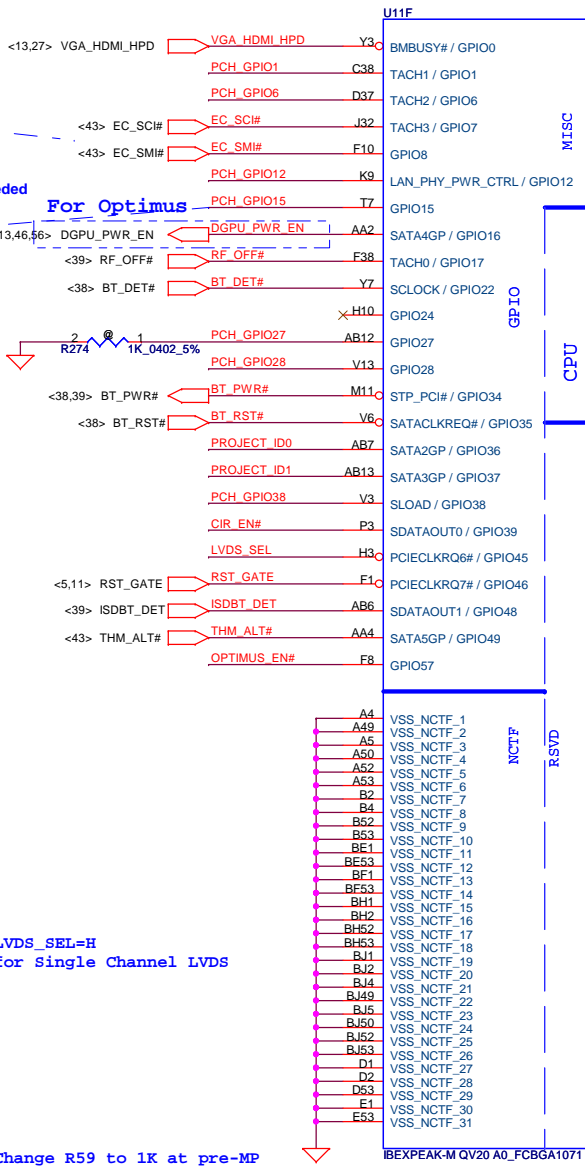
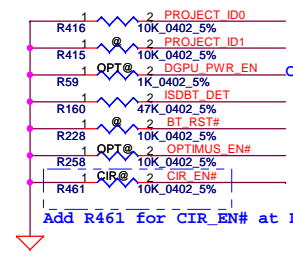
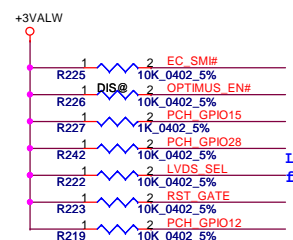
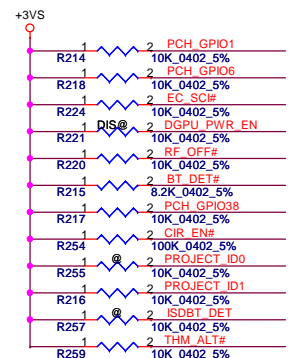
**GPIO8
Not pull down**

Internal: Pull up 20k
During Reset: High
Initial: High

**GPIO15
a Strong pull up may be needed
for GPIO Functionality**

Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR
PCH_GPIO27 High = Enabled (Default)
Low = Disabled



For Optimus

LVDS_SEL=H for Single Channel LVDS

Change R59 to 1K at pre-MP

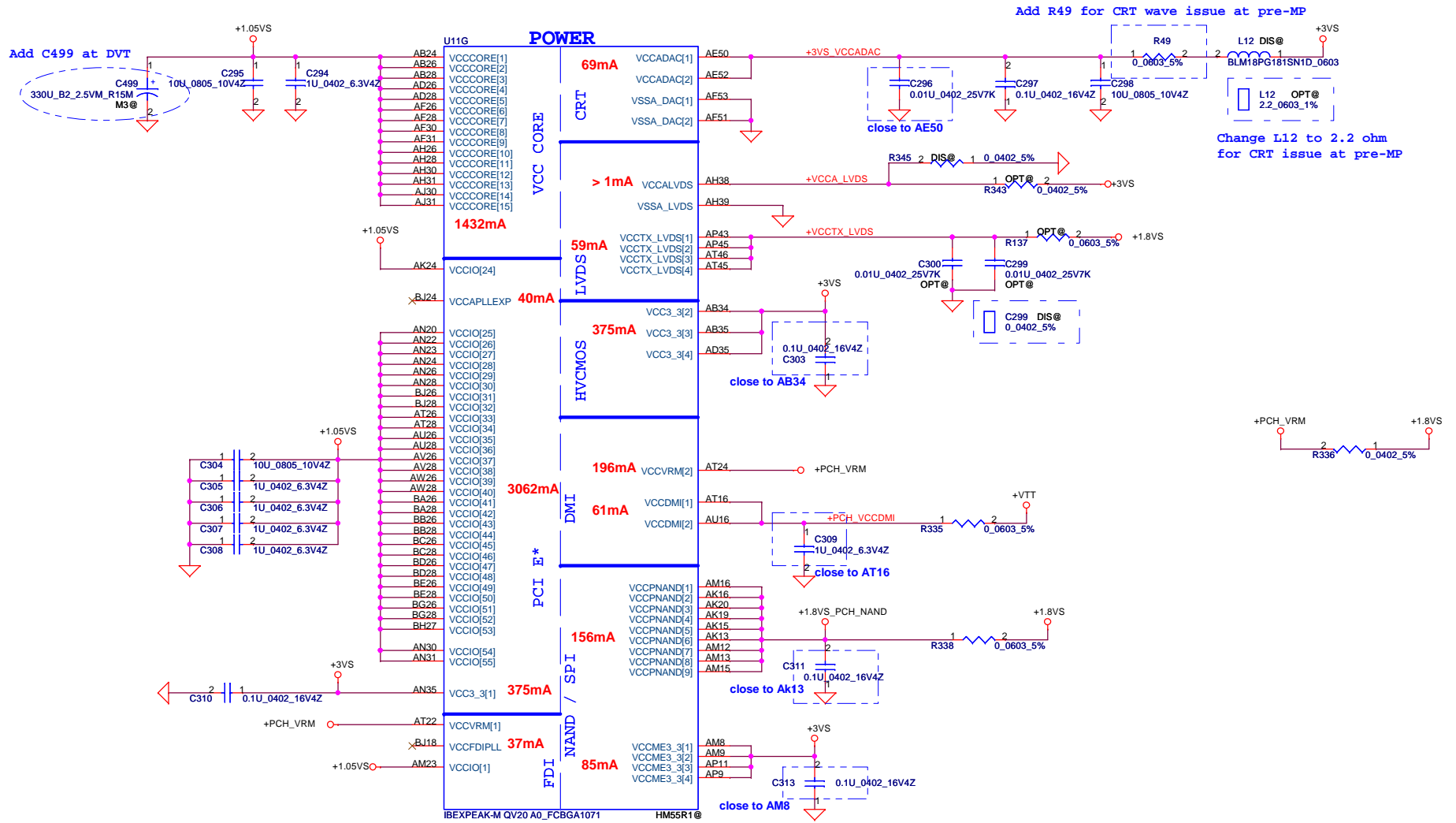
Add OPTIMUS_EN# at DVT

OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

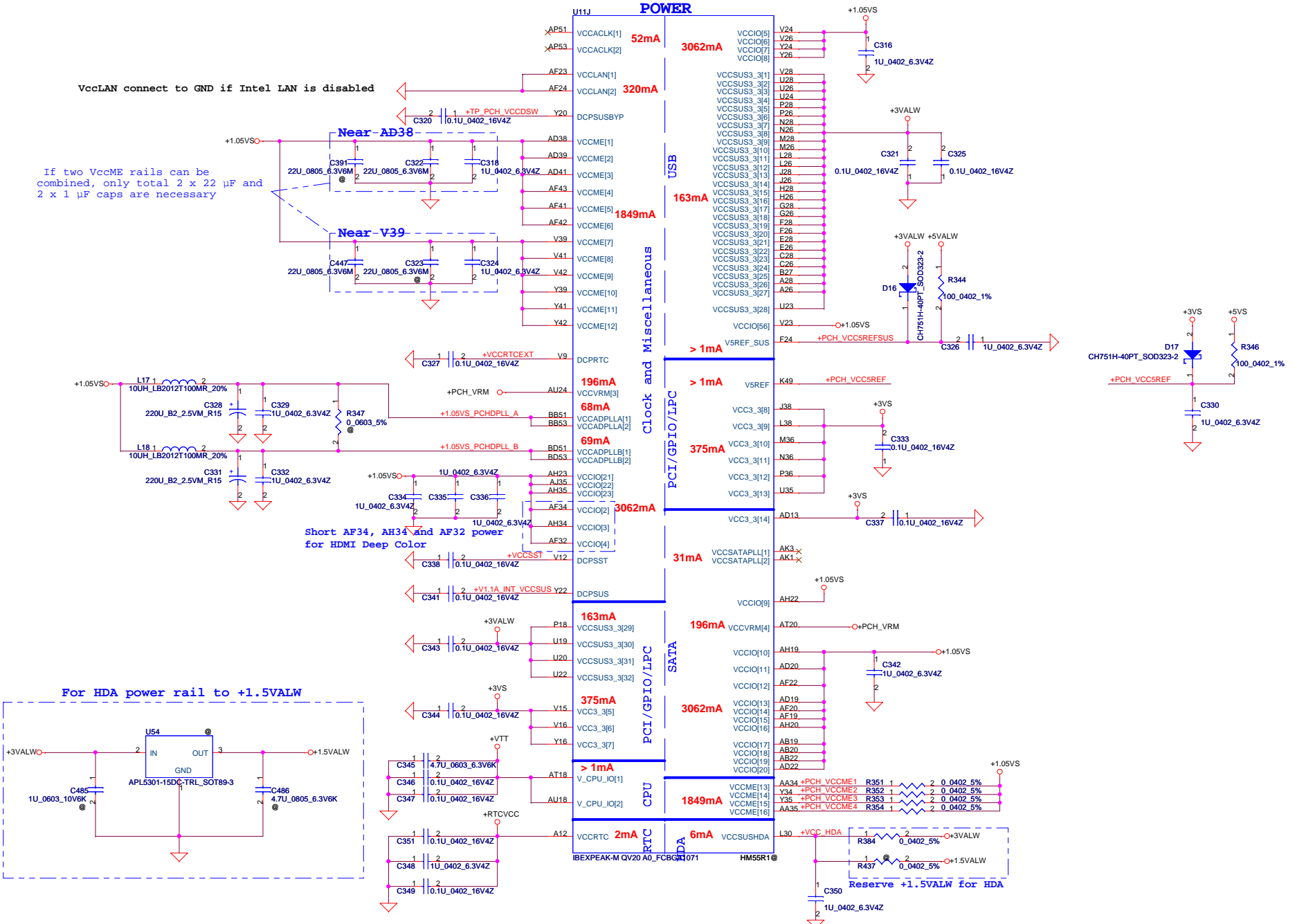
PROJECT_ID1	PROJECT_ID0	2010 Project ID setting
0	0	NDU00/10 (Streamline-M/-S 11.6/13.3")
0	1	NBQAA (Bordeaux 14")
1	0	NWQAA (Marseille 16")
1	1	NALAA (Hamburg 17.3")

Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

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VccLAN connect to GND if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary

Near-AD38

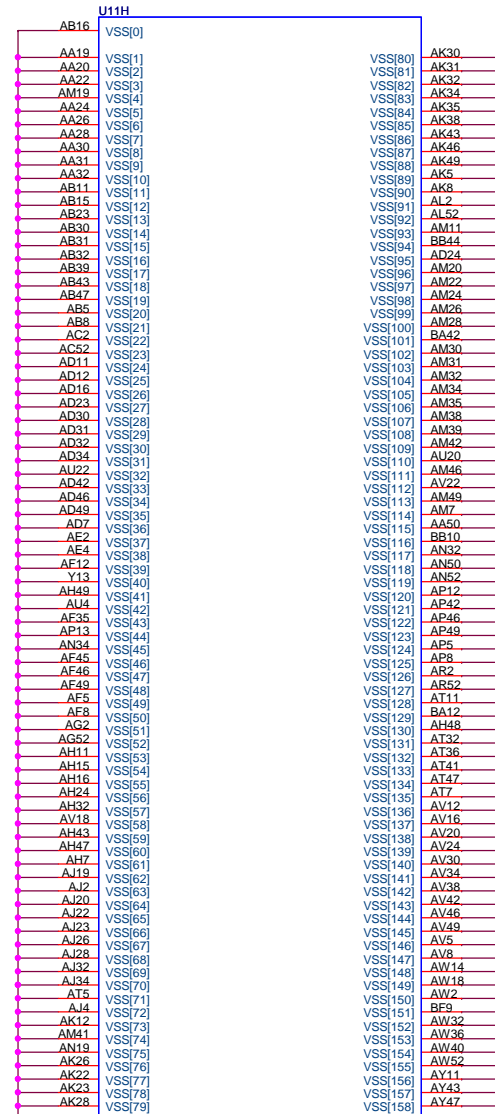
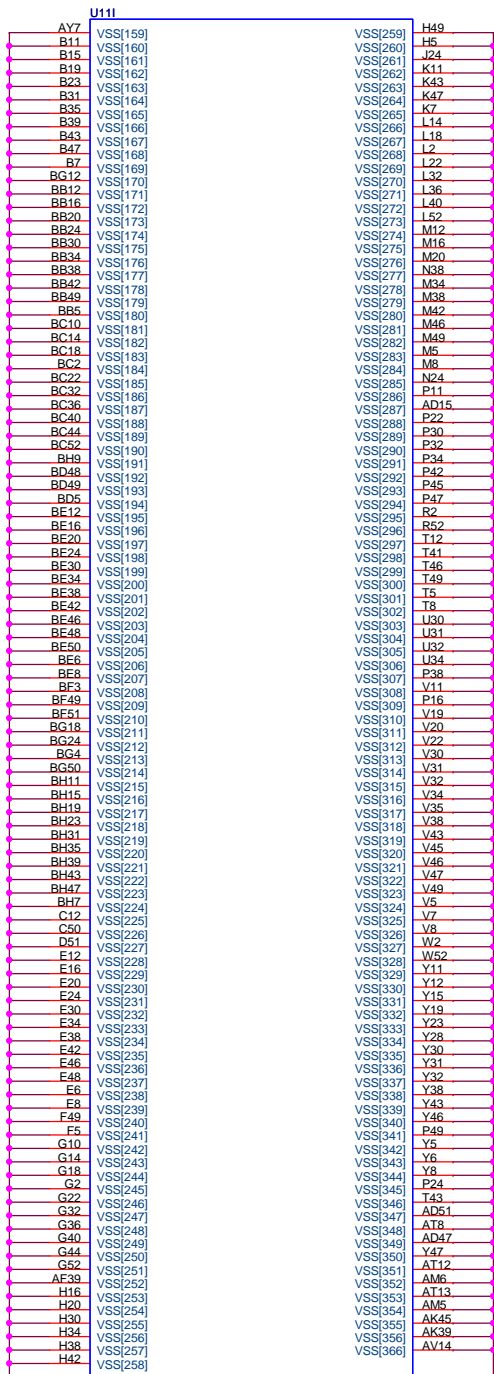
Near-V39

Short AF34, AH34 and AF32 power for HDMI Deep Color

For HDA power rail to +1.5VALW

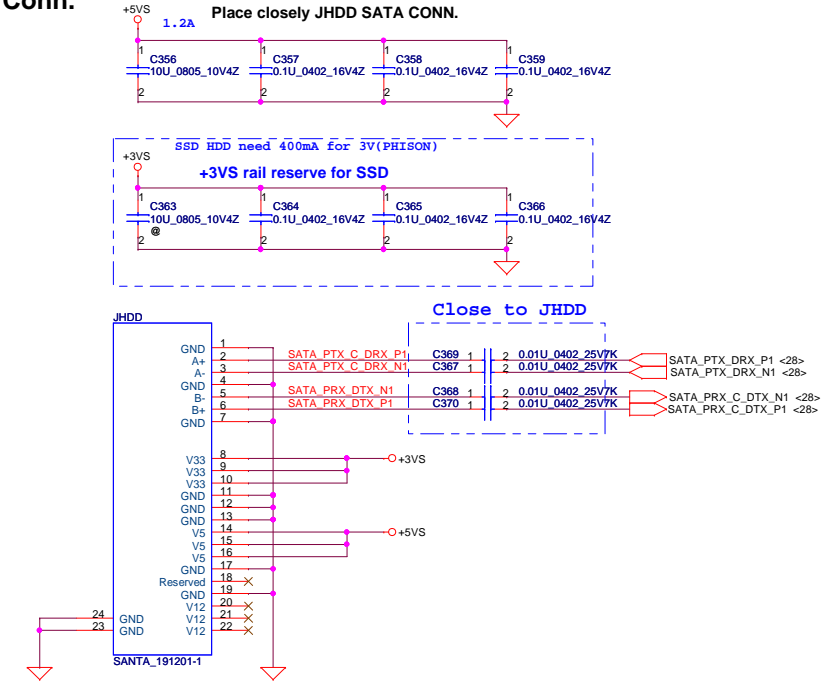
Reserve +1.5VALW for HDA

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				Custom	2.0
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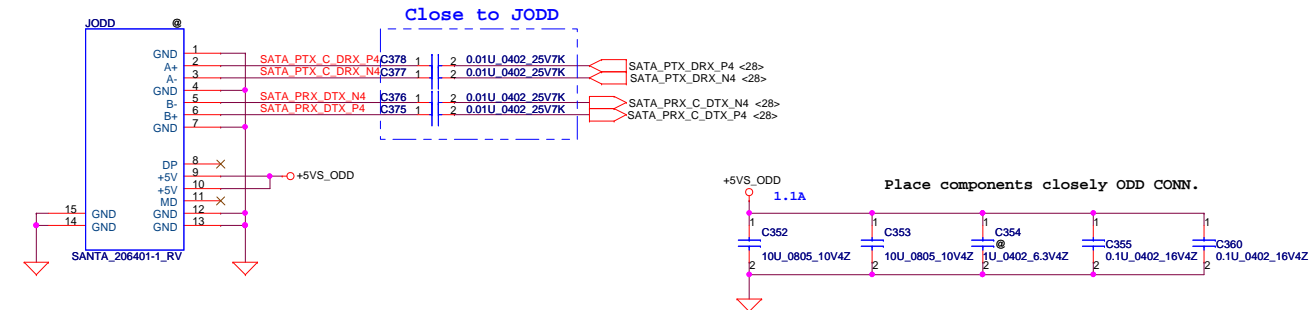


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Size	Document Number			Rev	2.0
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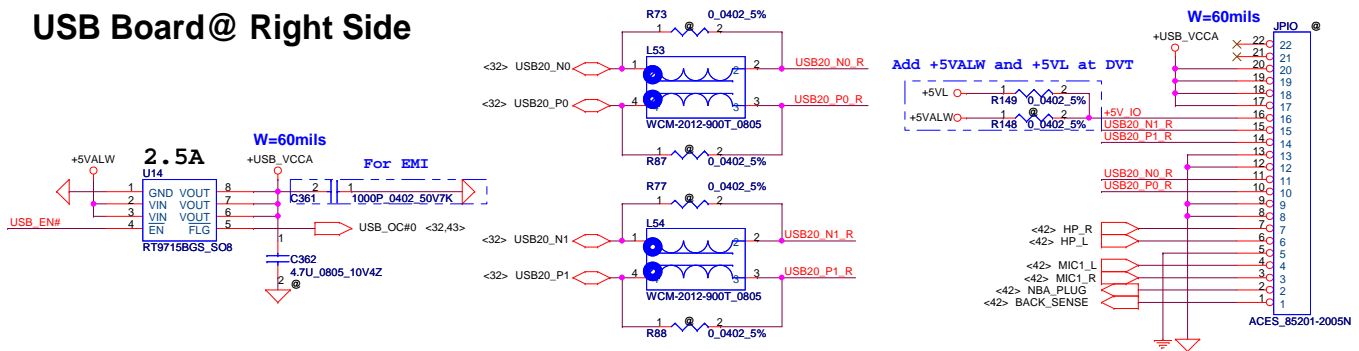
SATA HDD Conn.



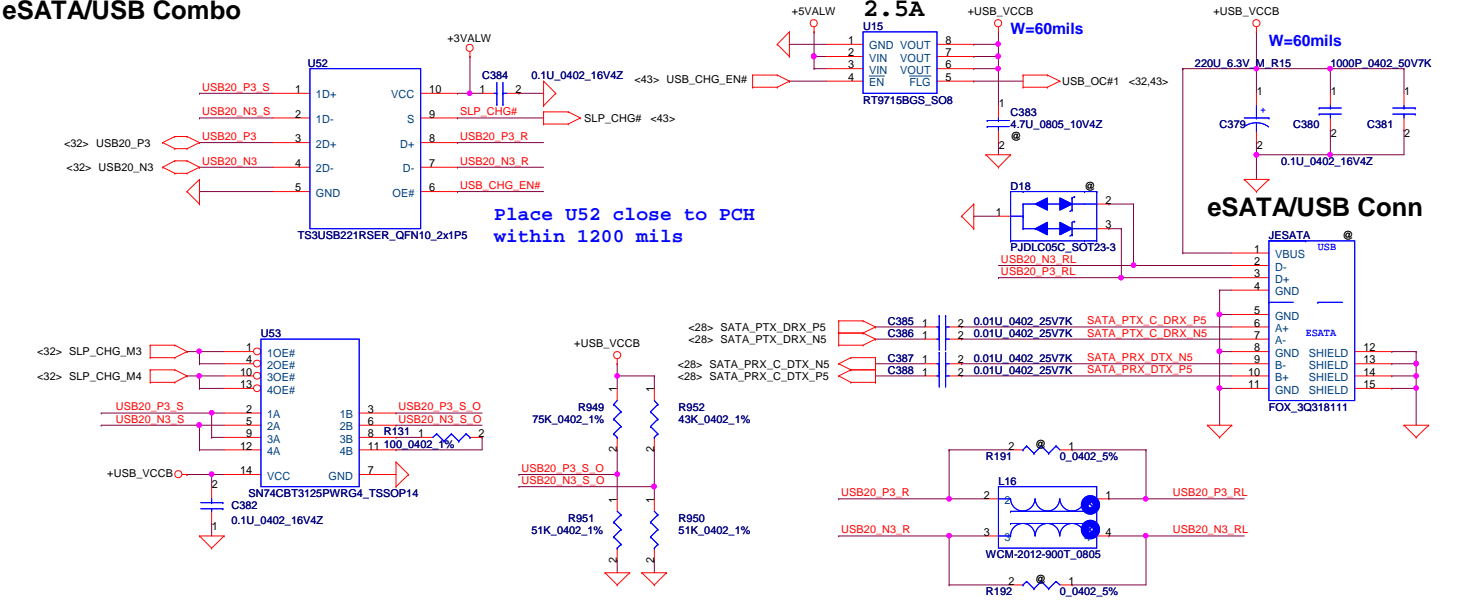
SATA ODD Conn



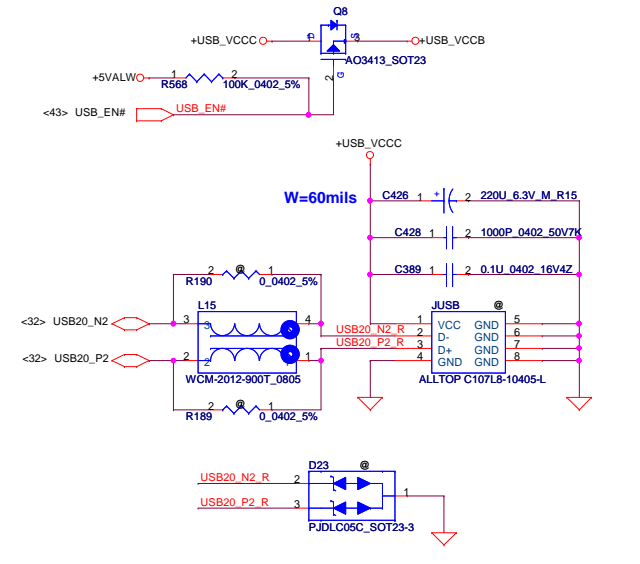
USB Board@ Right Side



eSATA/USB Combo



USB Board@ Left Side

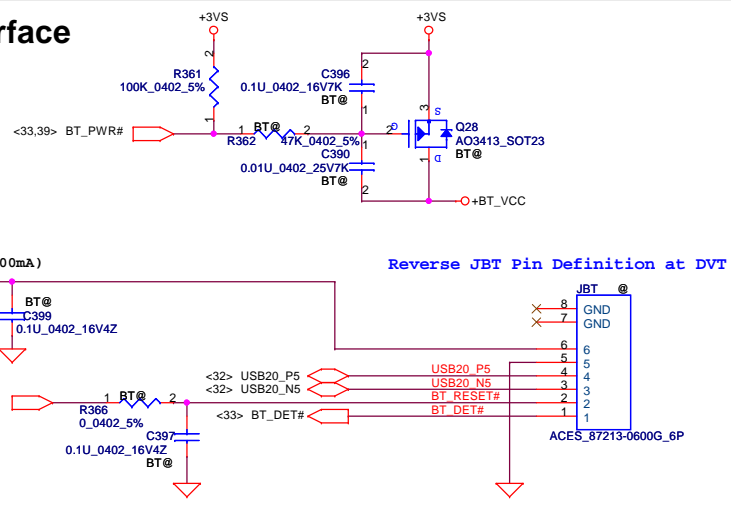


SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

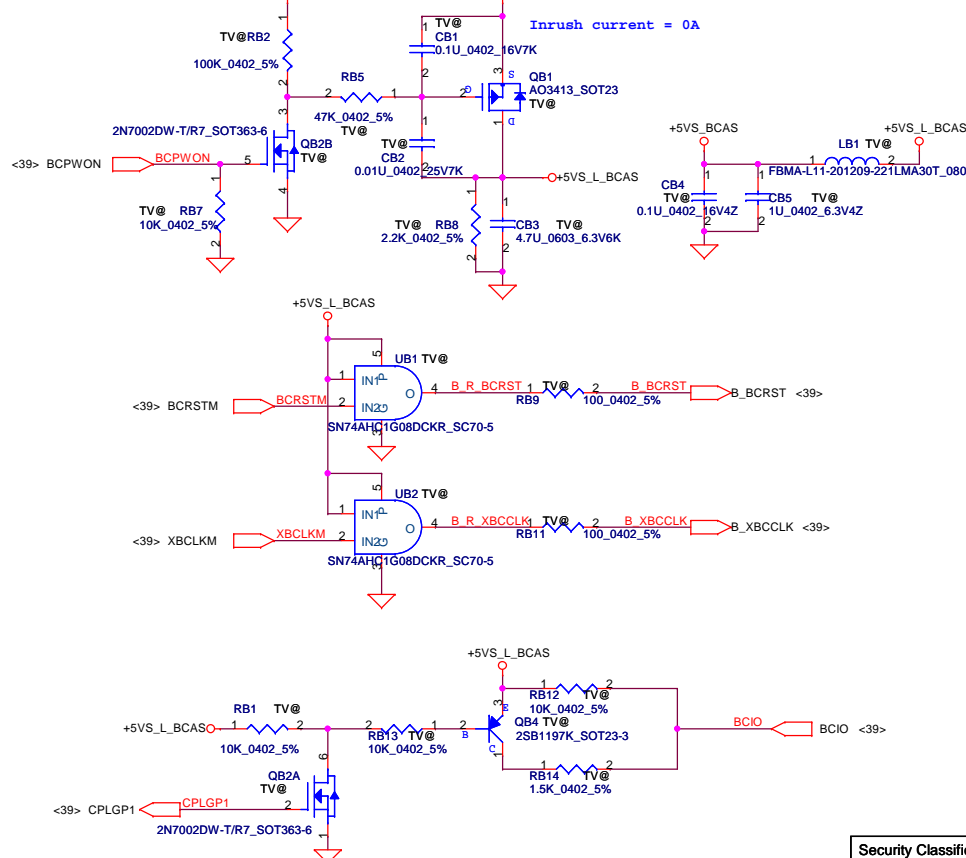
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

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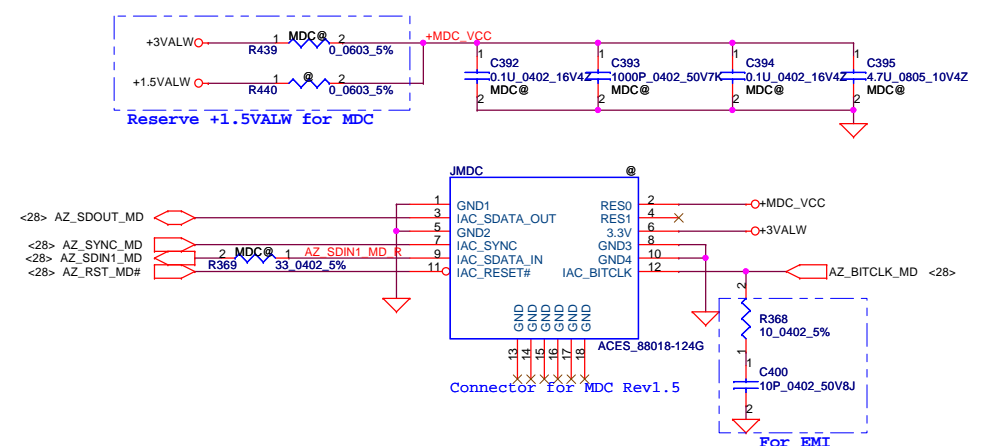
BlueTooth Interface



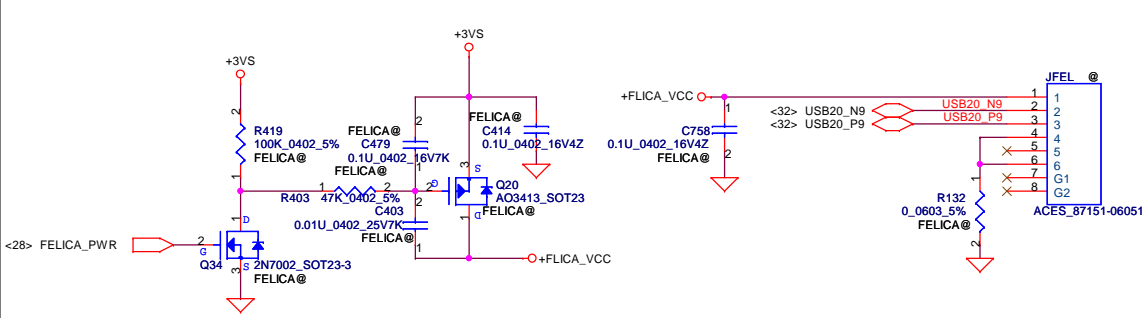
B-CAS Circuit



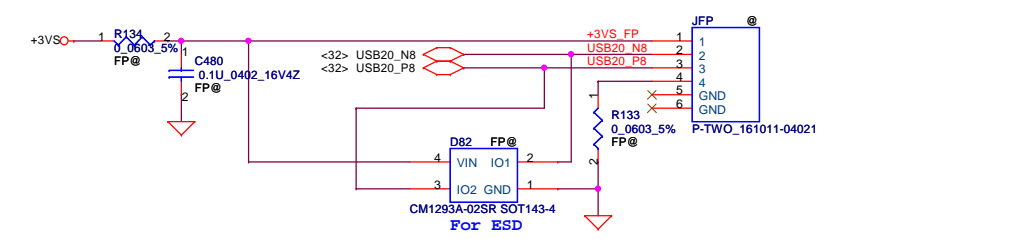
MDC 1.5 Conn.



Felica

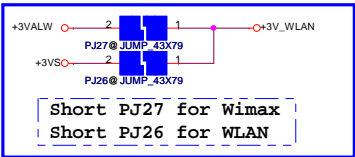


Finger printer



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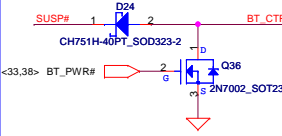
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



WLAN&BT Combo module circuits

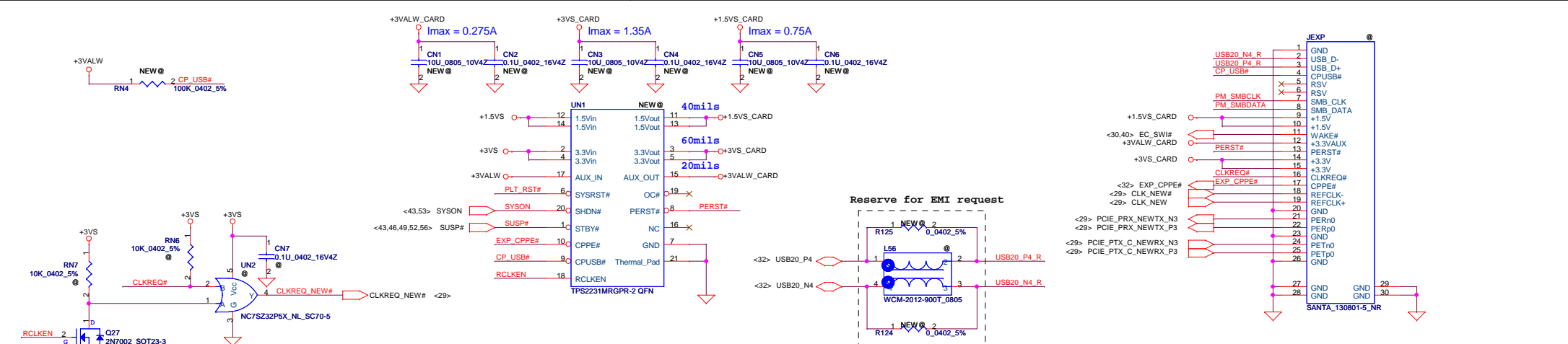
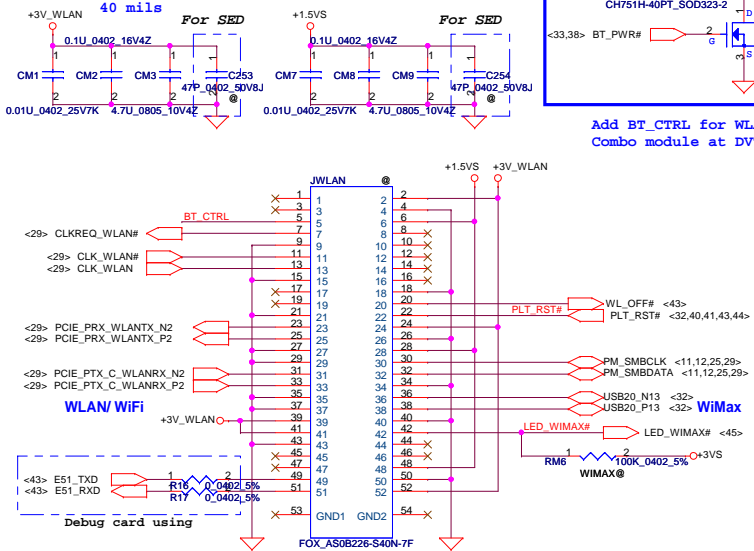
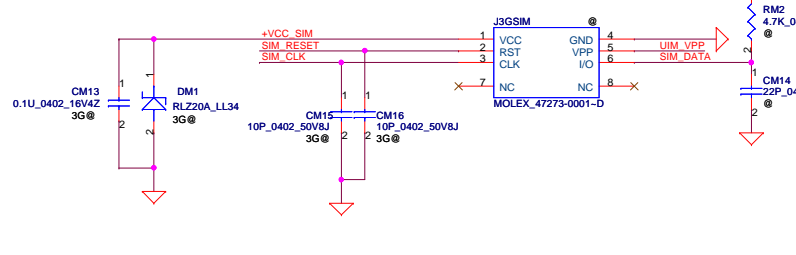
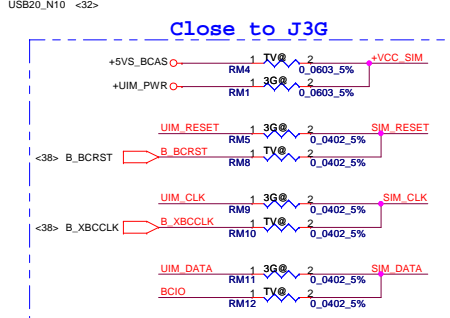
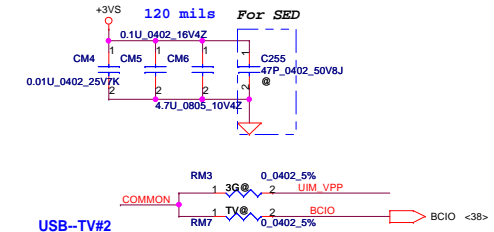
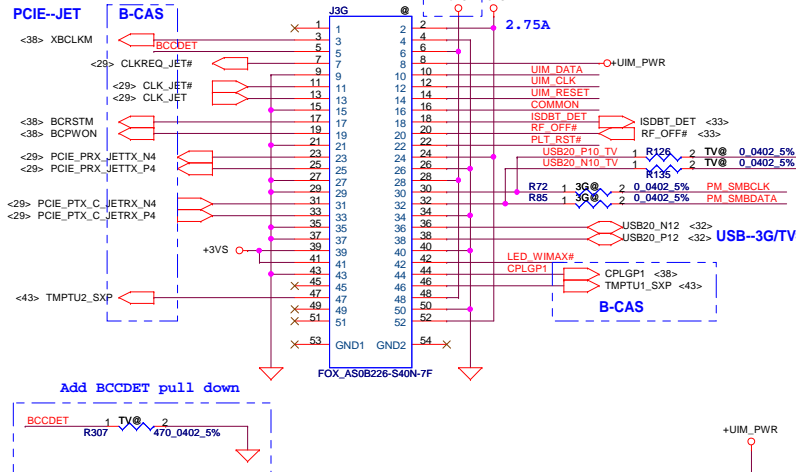
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove D24



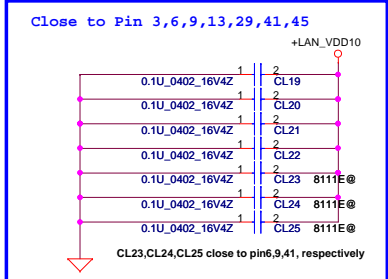
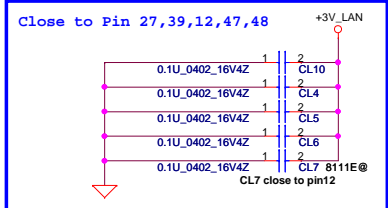
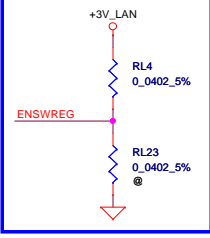
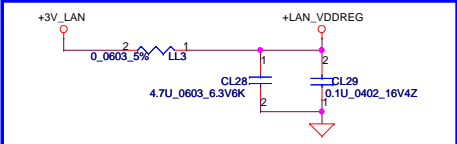
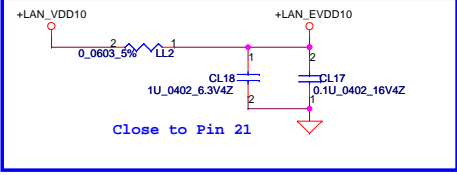
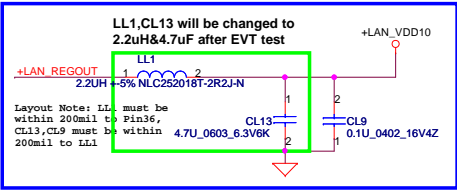
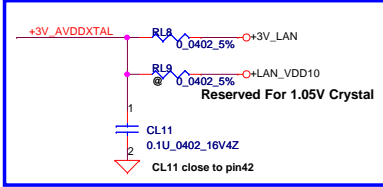
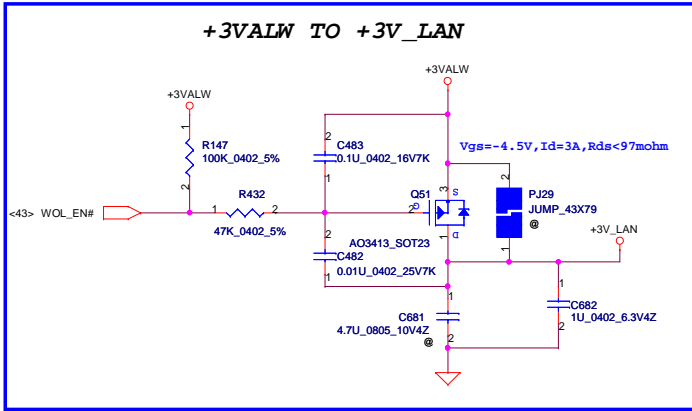
Add BT_CTRL for WLAN & BT Combo module at DVT

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner Half PCIe Mini Card- JET



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Size	Document Number	Rev	2.0	
	NWQAA LA-6062P M/B			
Date:	Wednesday, March 24, 2010	Sheet	39	of 59

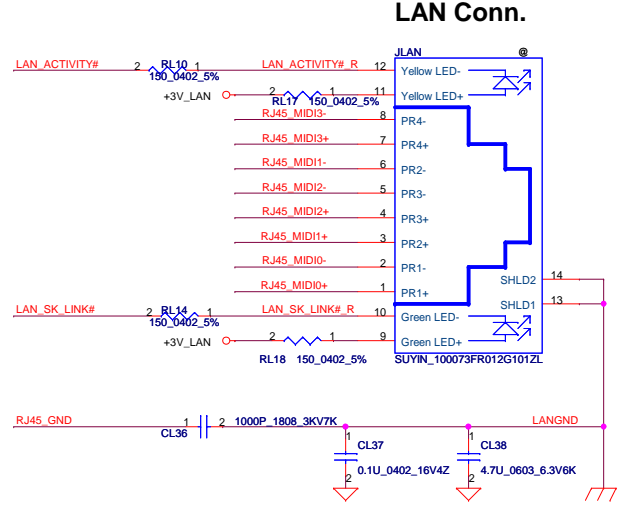
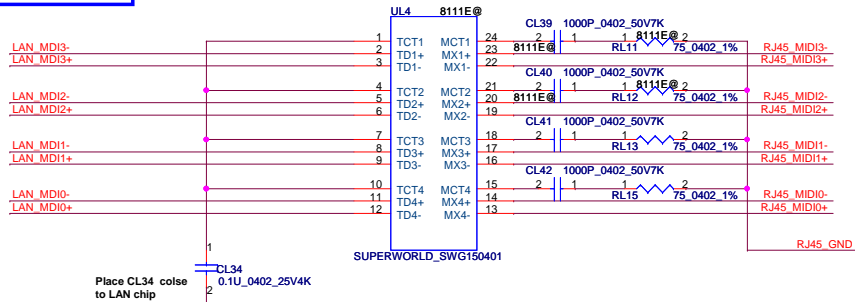
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



For P/N and footprint
Please place them to ISPDP page

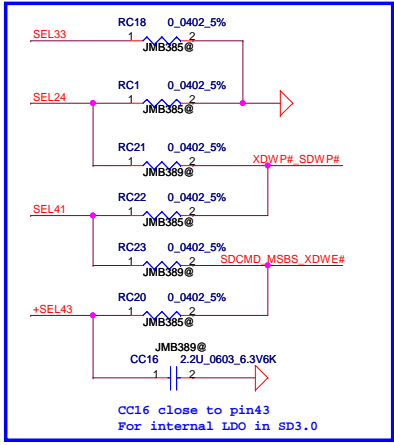
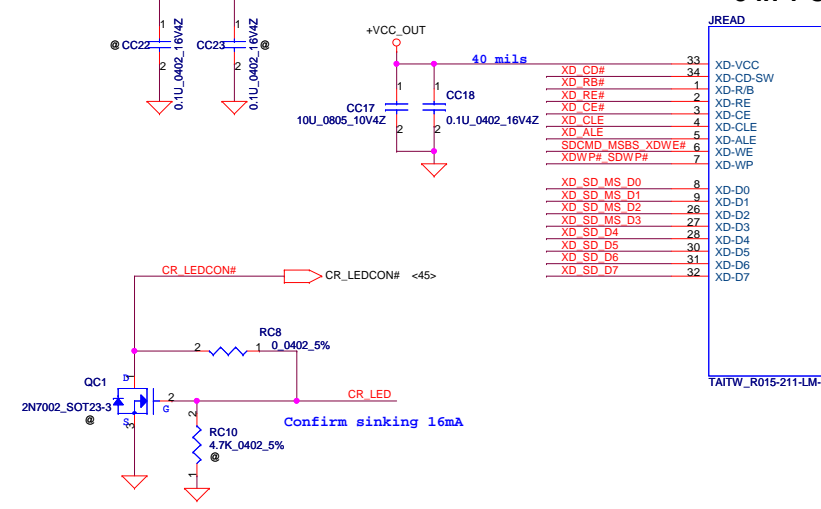
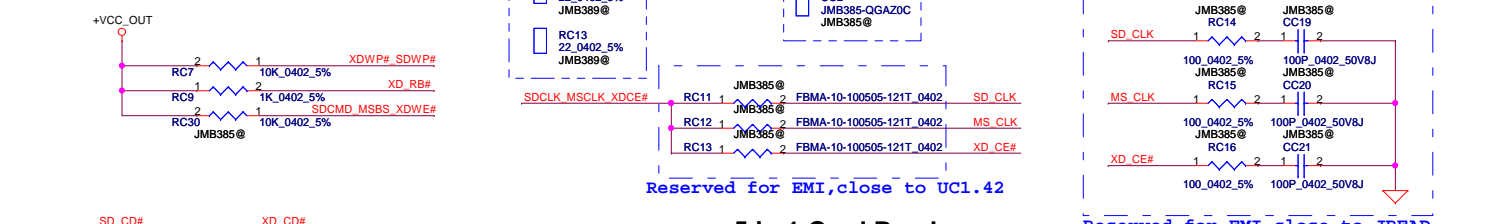
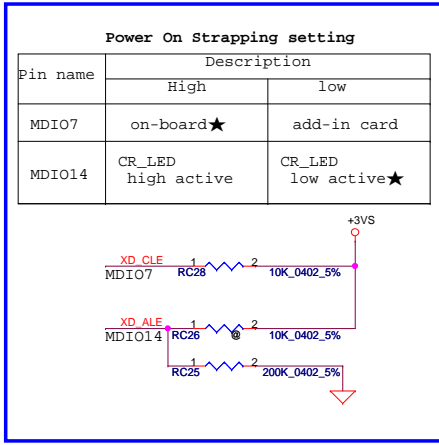
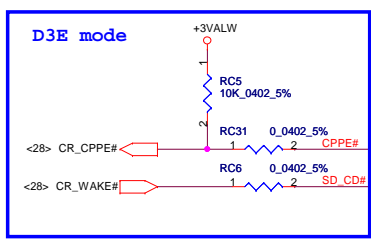
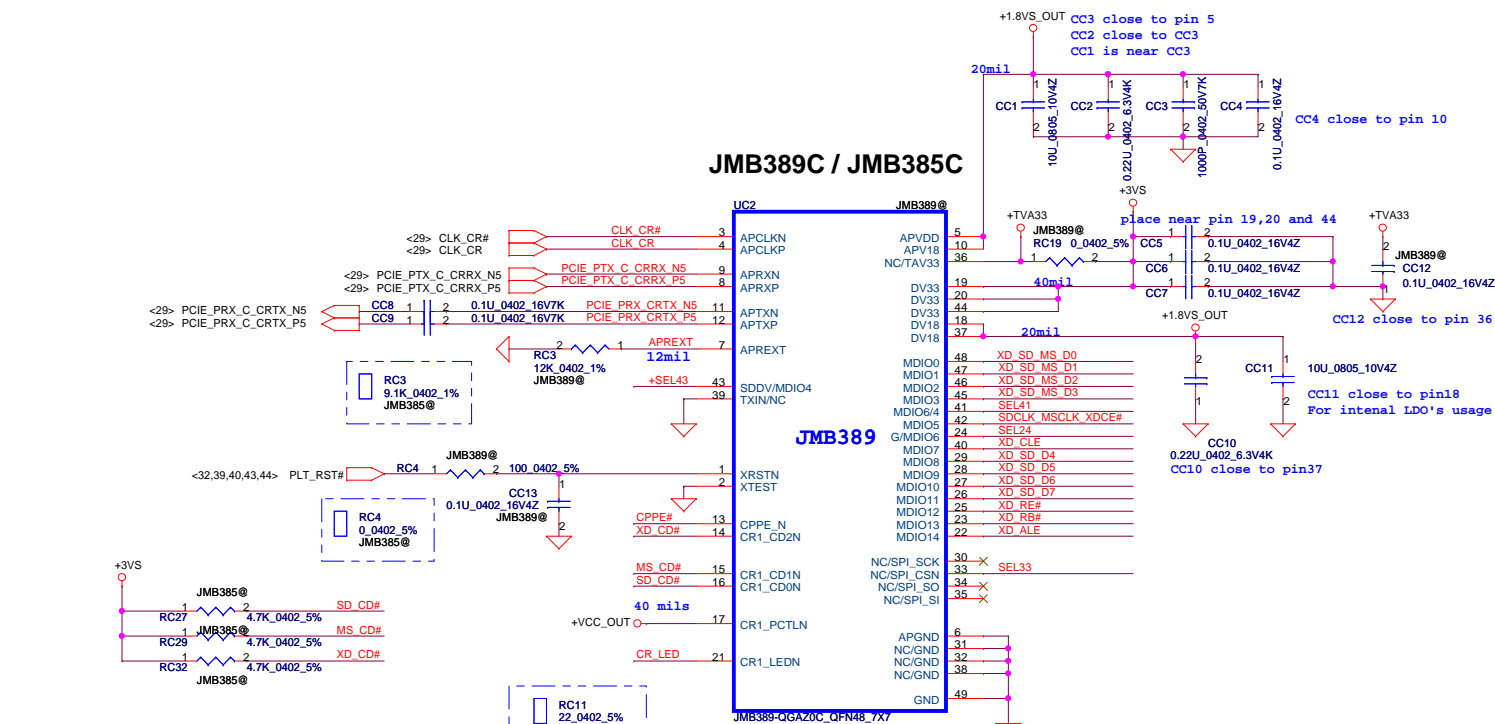
UL1
8105E 10/100M
8105E@

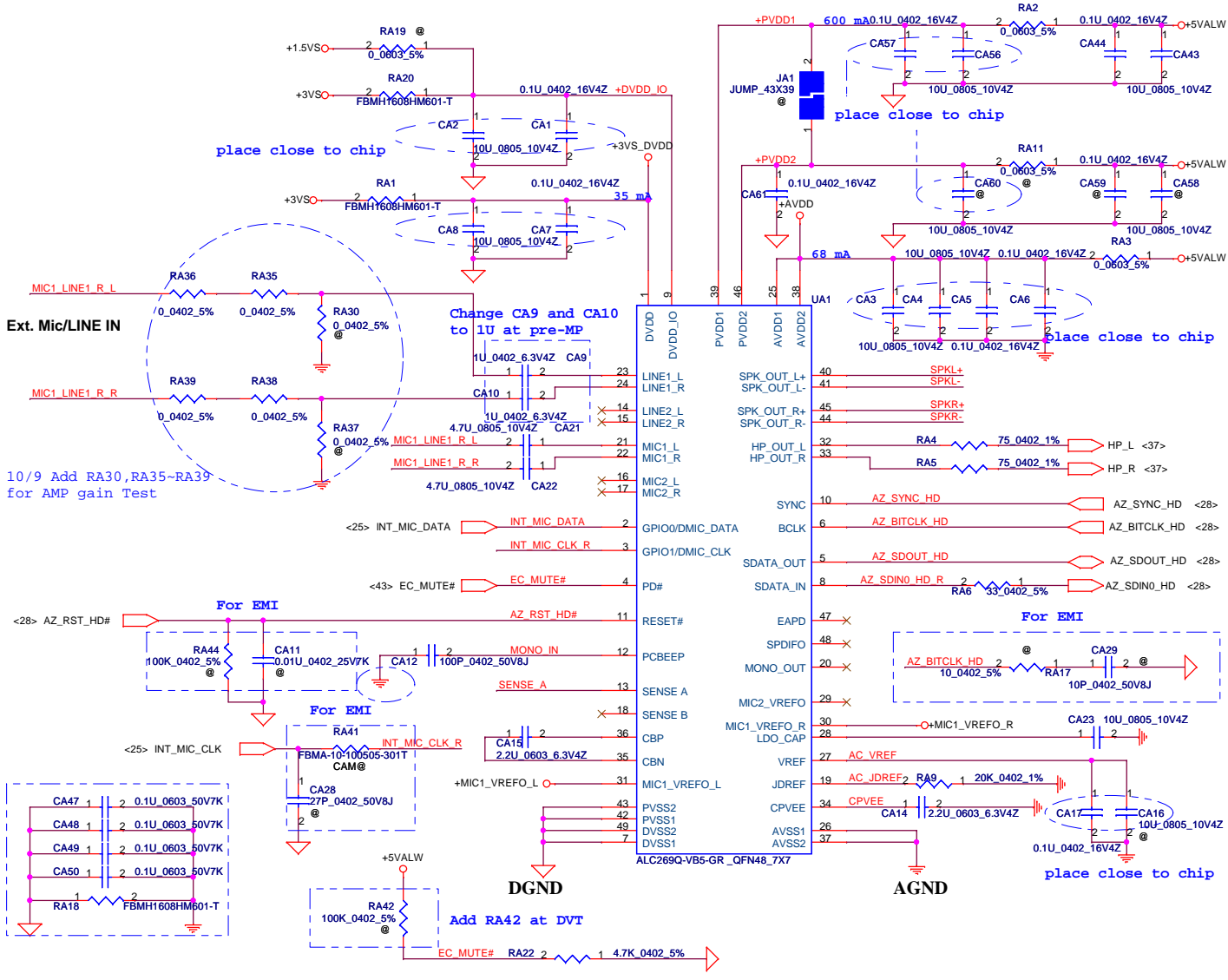
UL4
10/100M transformer
8105E@



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Date:	Wednesday, March 24, 2010	Sheet	40	Rev	2.0	

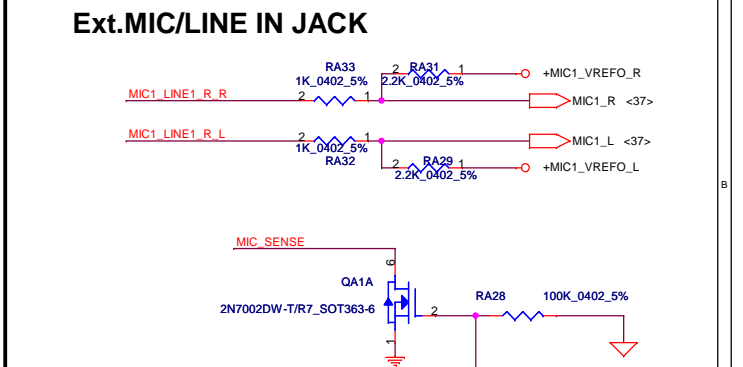
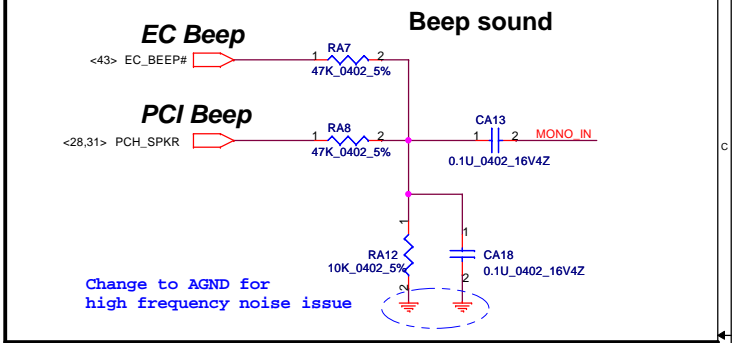
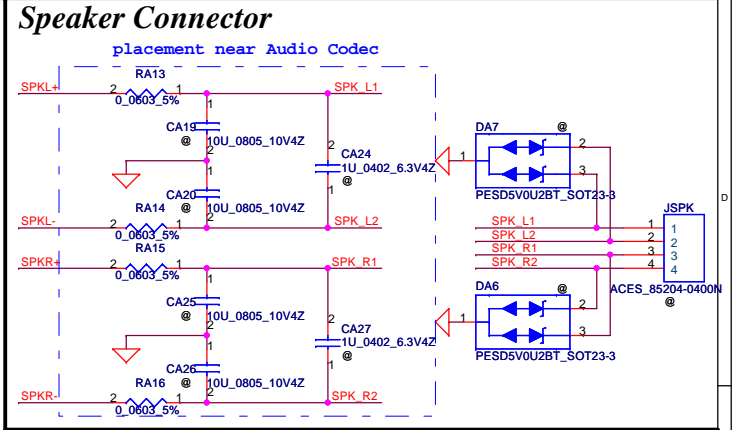
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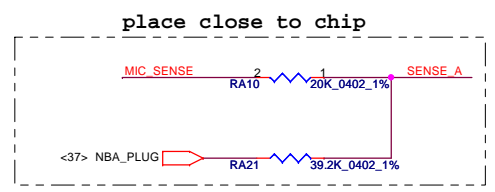


Ext. Mic/LINE IN

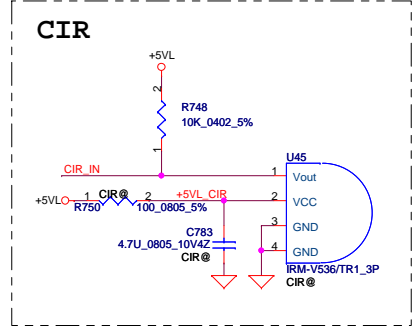
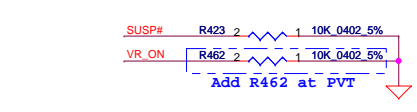
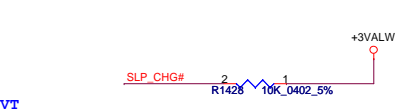
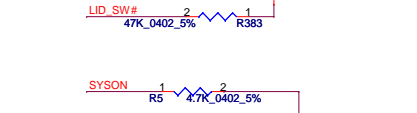
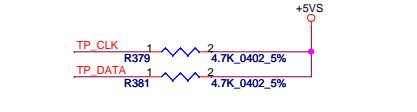
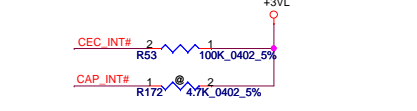
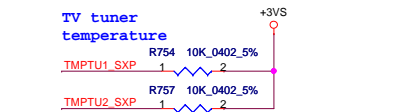
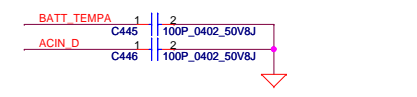
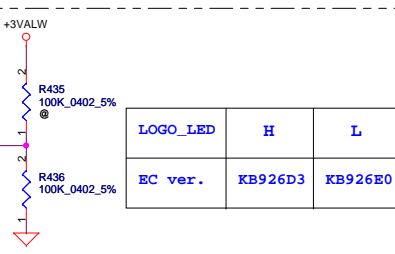
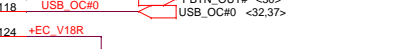
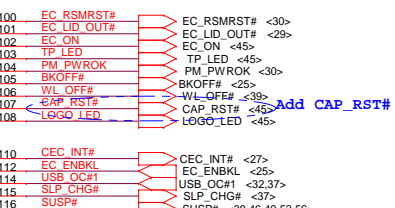
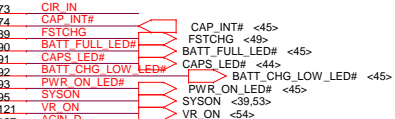
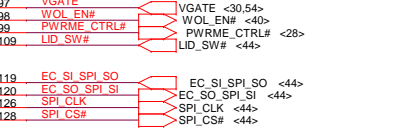
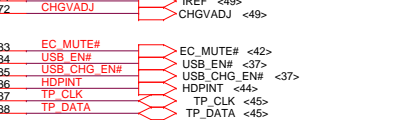
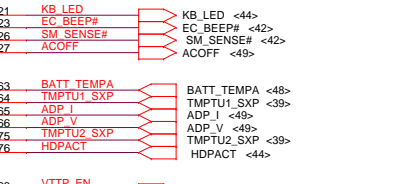
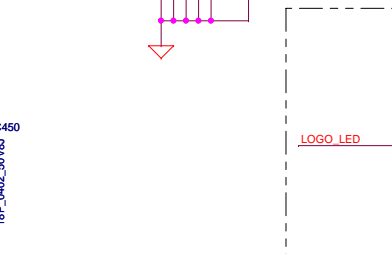
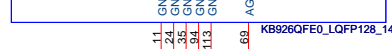
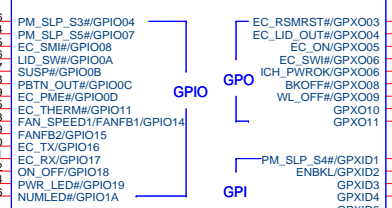
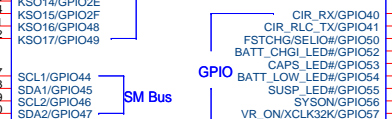
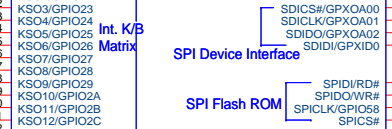
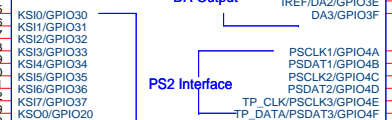
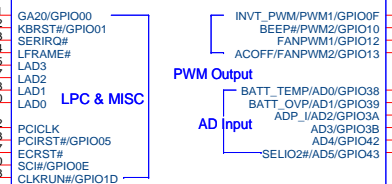
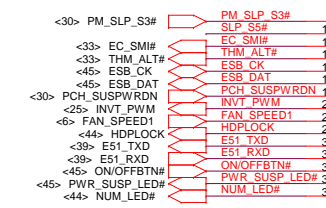
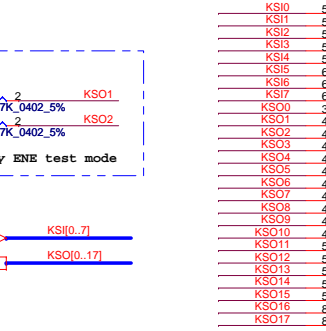
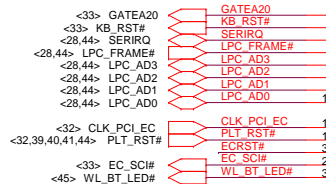
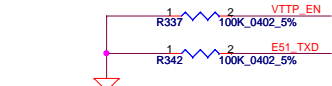
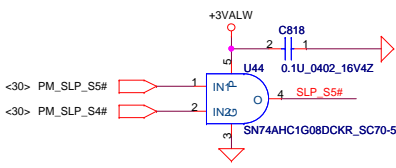
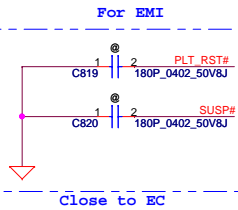
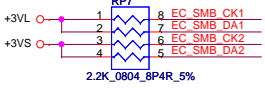
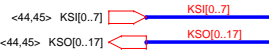
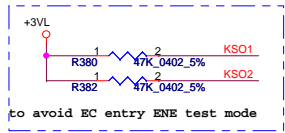
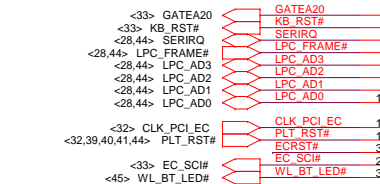
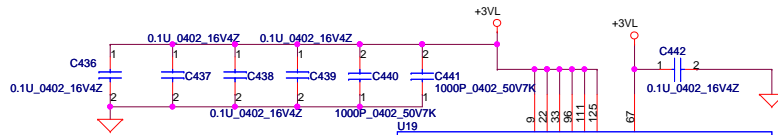
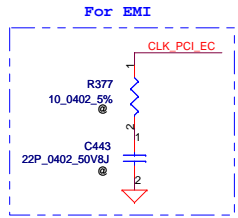
10/9 Add RA30, RA35~RA39 for AMP gain Test



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



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Size	Document Number	Date		Rev	
	NWQAA LA-6062P M/B	Wednesday, March 24, 2010		2.0	
				Sheet 42 of 59	

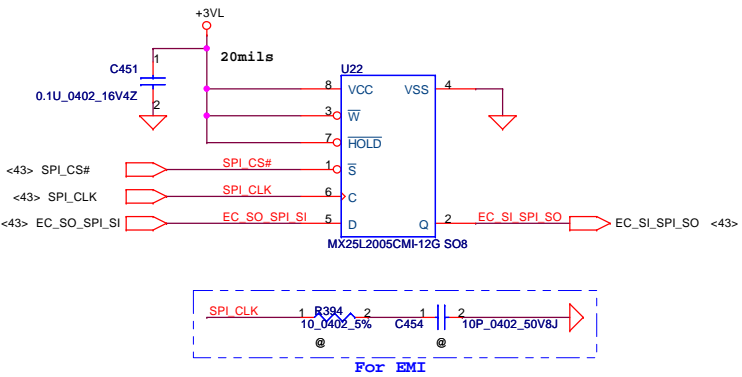


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		2010/01/23

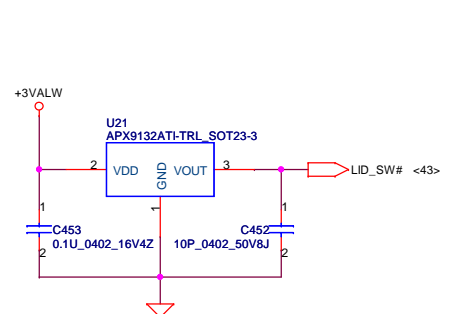
Compal Electronics, Inc.		
ENE-KB926 RevD2		
Title	Document Number	Rev
	NWQAA LA-6062P M/B	2.0
Date	Wednesday, March 24, 2010	Sheet 43 of 59

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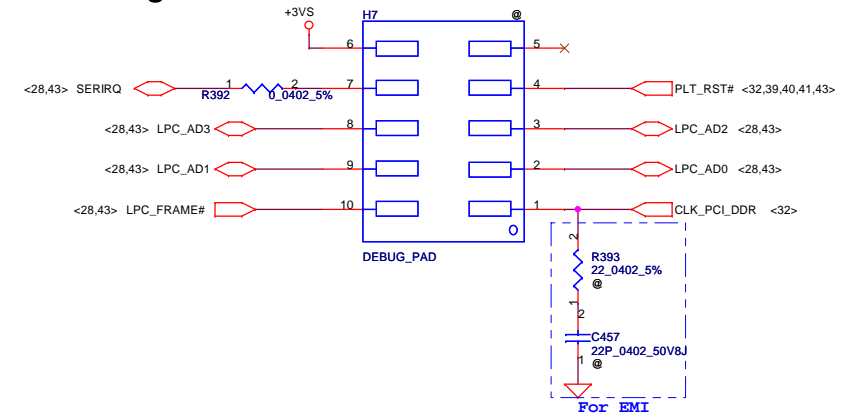
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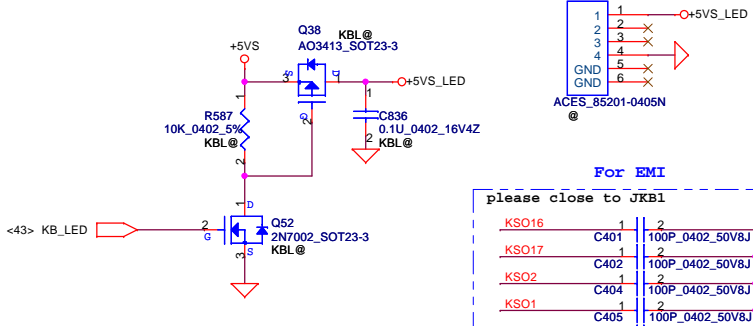
Lid SW



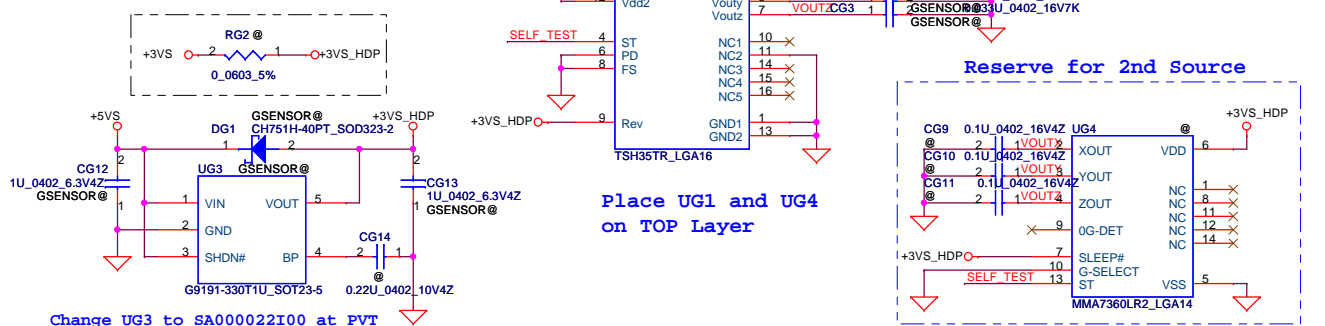
LPC Debug Port



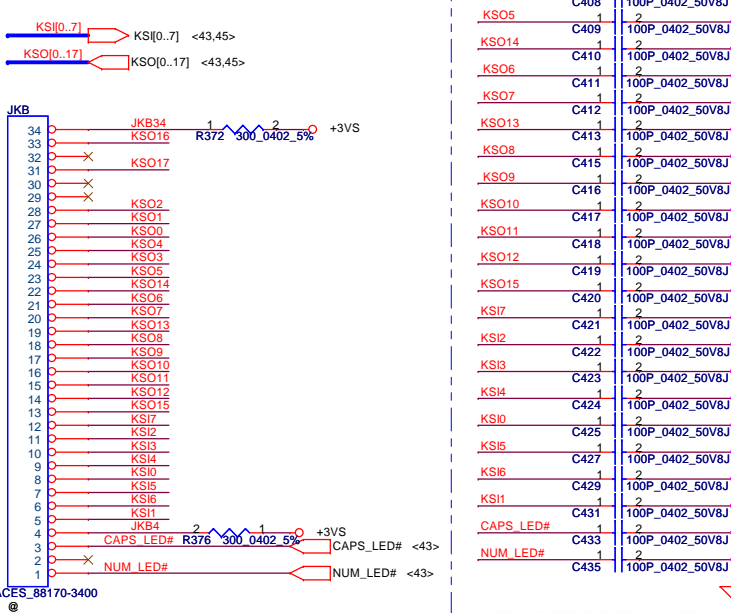
Keyboard LED



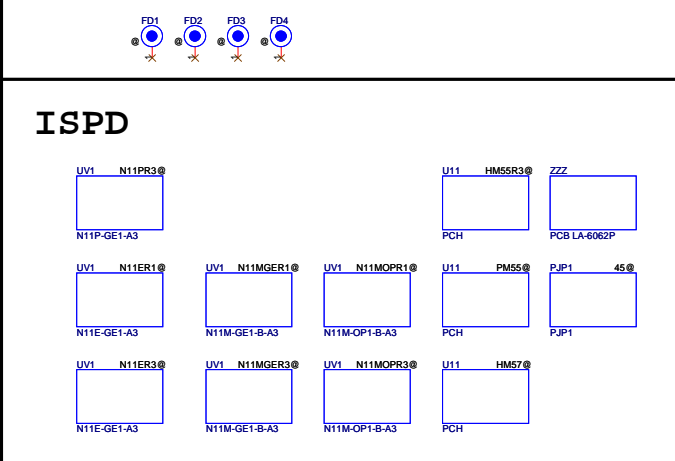
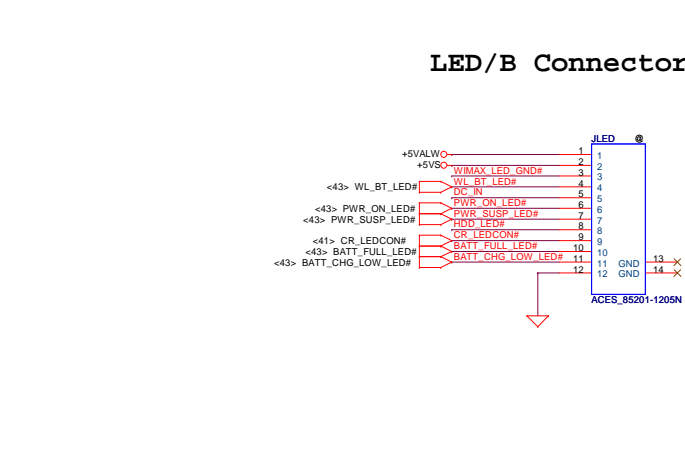
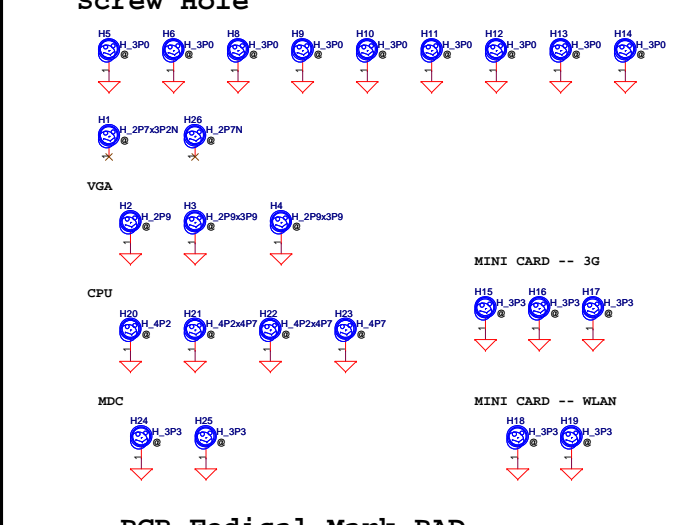
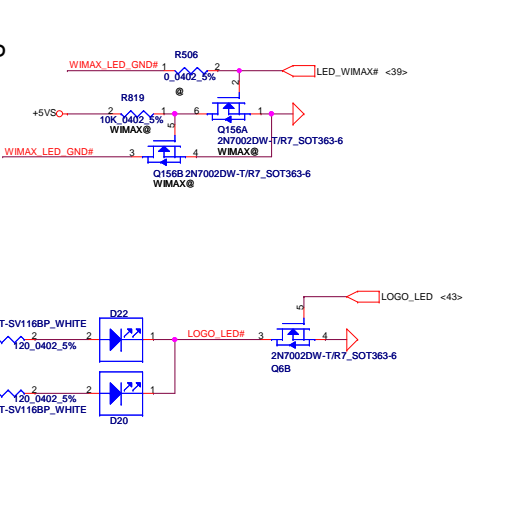
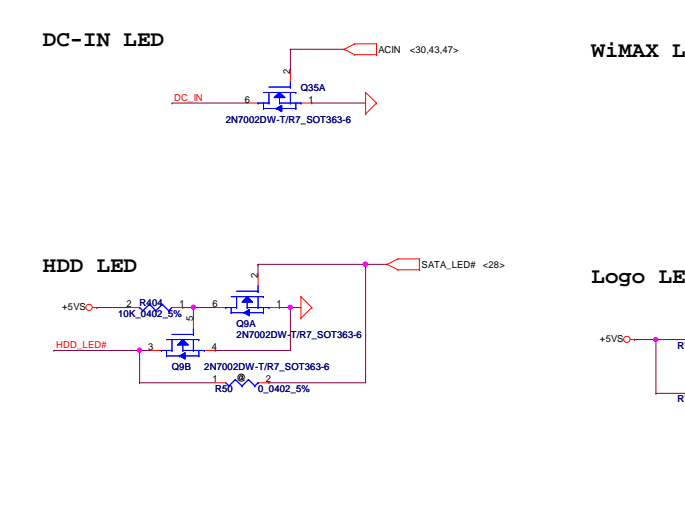
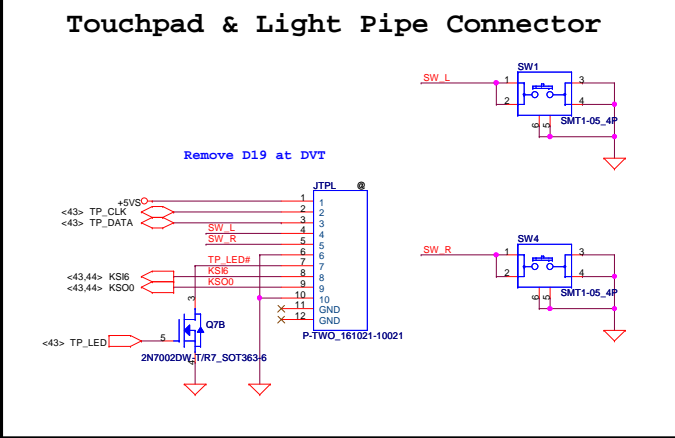
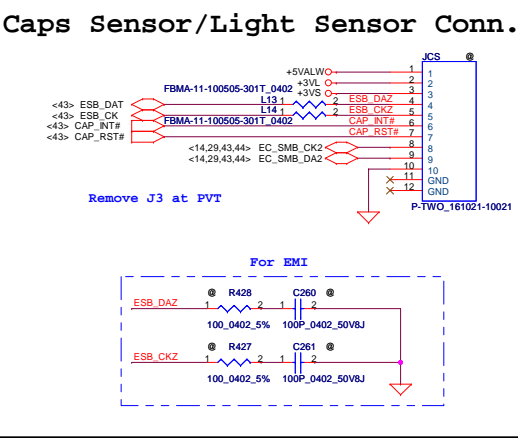
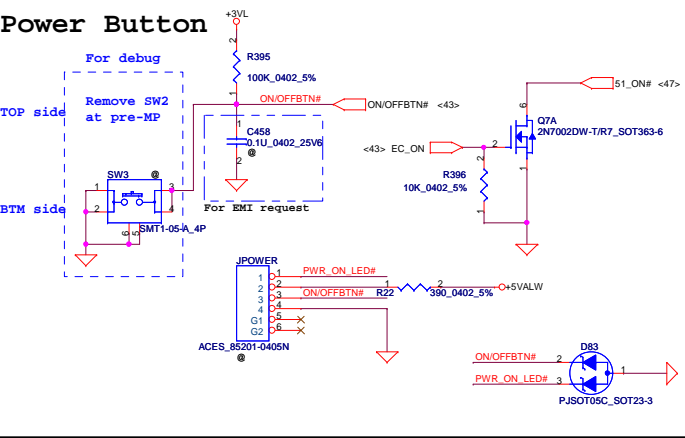
G-Sensor



KEYBOARD CONN.

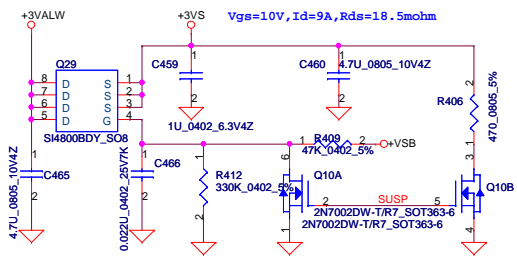


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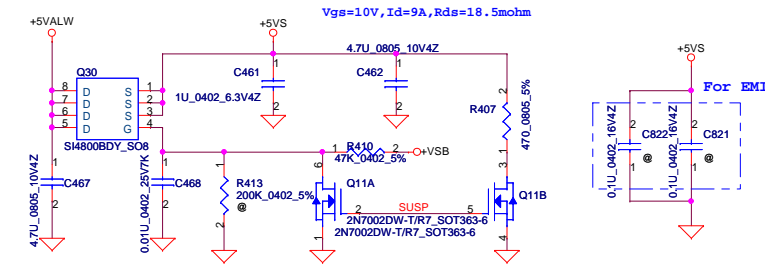


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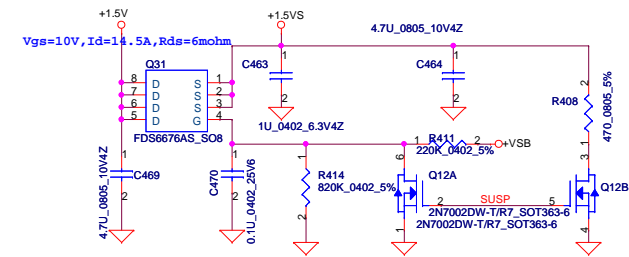
+3VALW TO +3VS



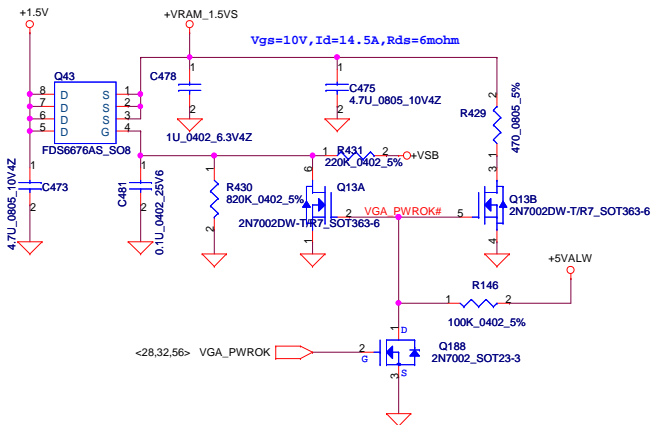
+5VALW TO +5VS



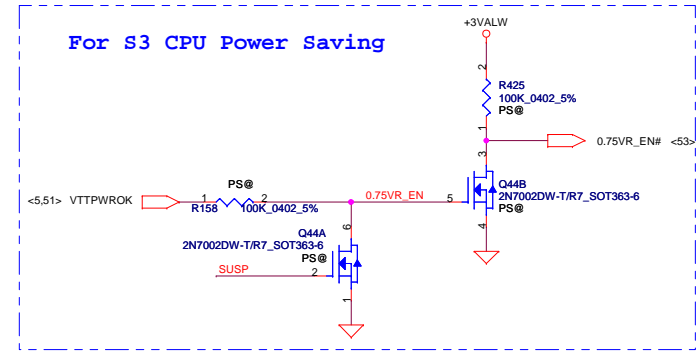
+1.5V to +1.5VS



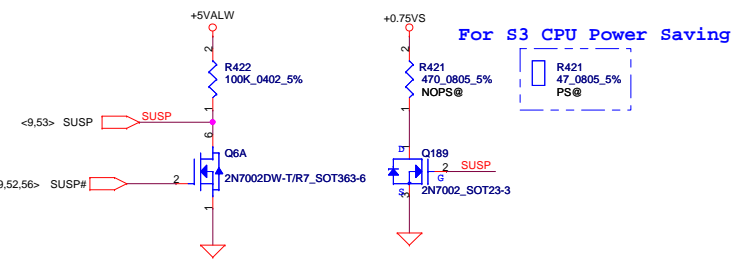
+1.5V to +VRAM_1.5VS



For S3 CPU Power Saving

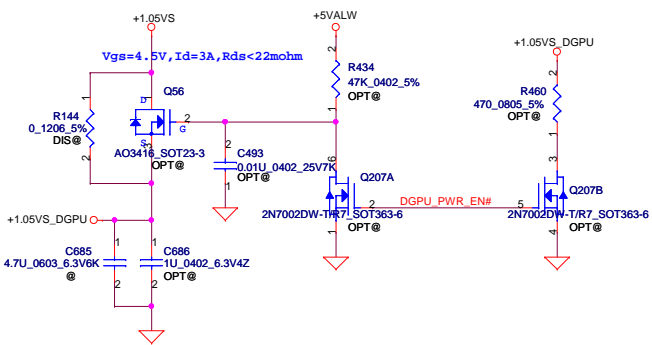


For S3 CPU Power Saving

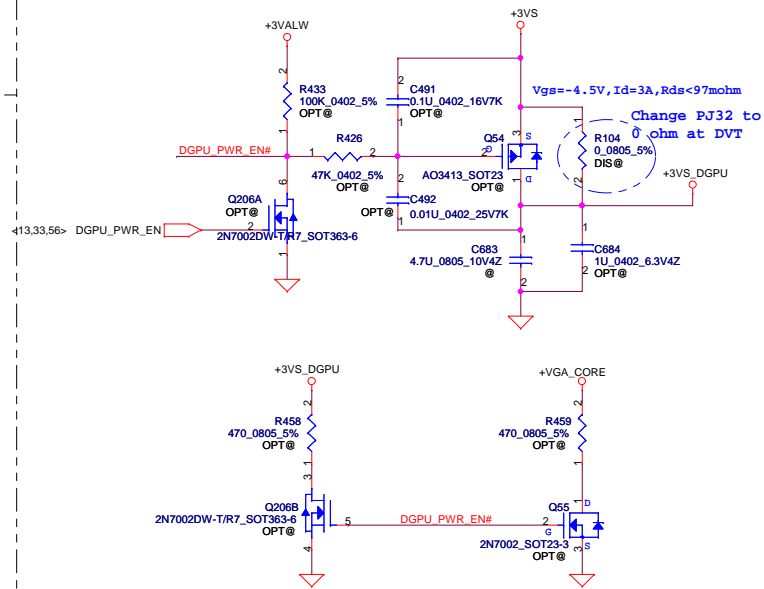


+1.05VS to +1.05VS_DGPU

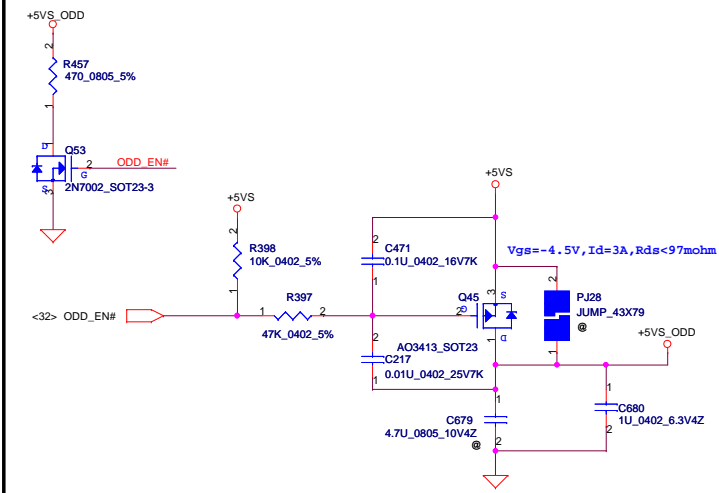
Change +1.05VS_DGPU circuit to N-channel MOS at PVT



+3VS to +3VS_DGPU

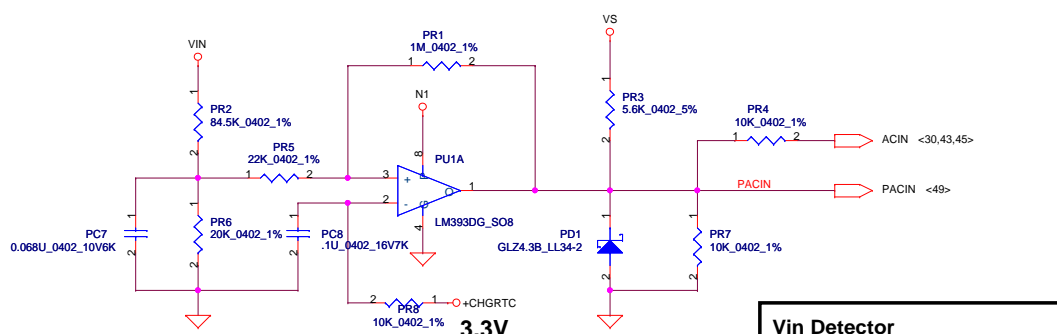
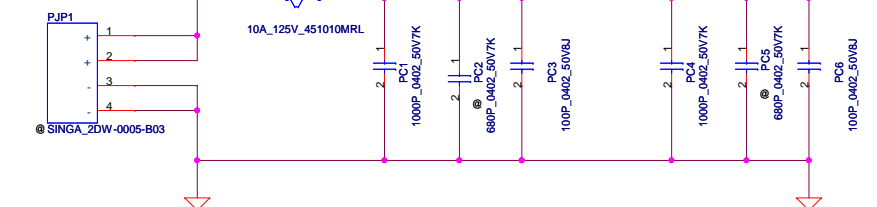


+5VS TO +5VS_ODD

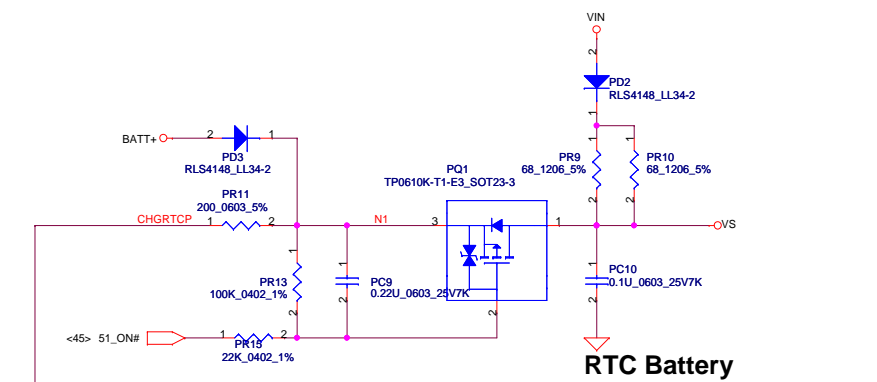


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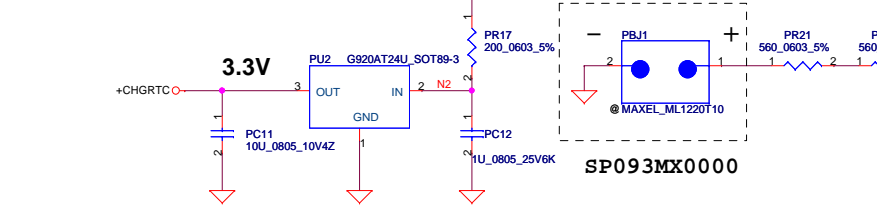
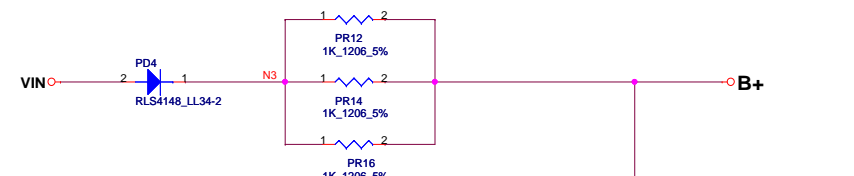
DC301001M80



Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976

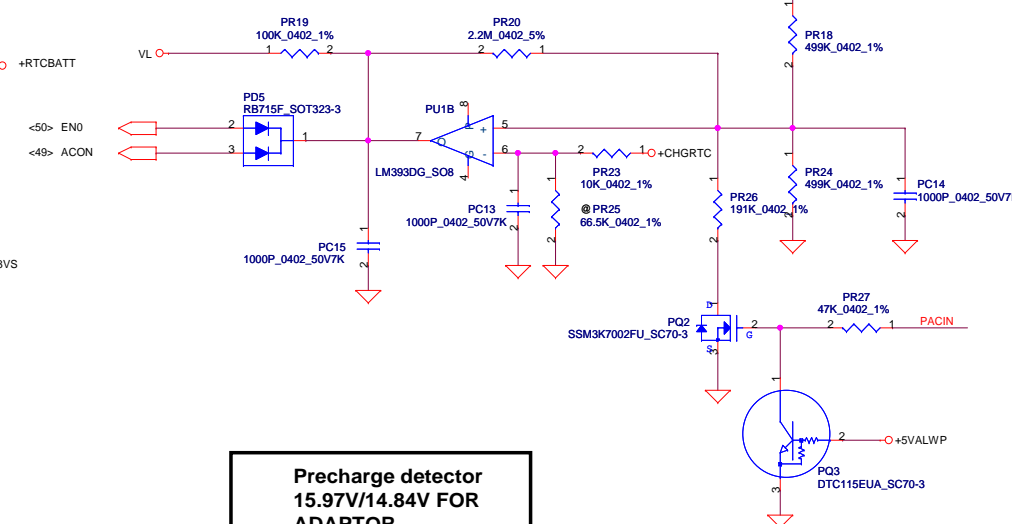


RTC Battery

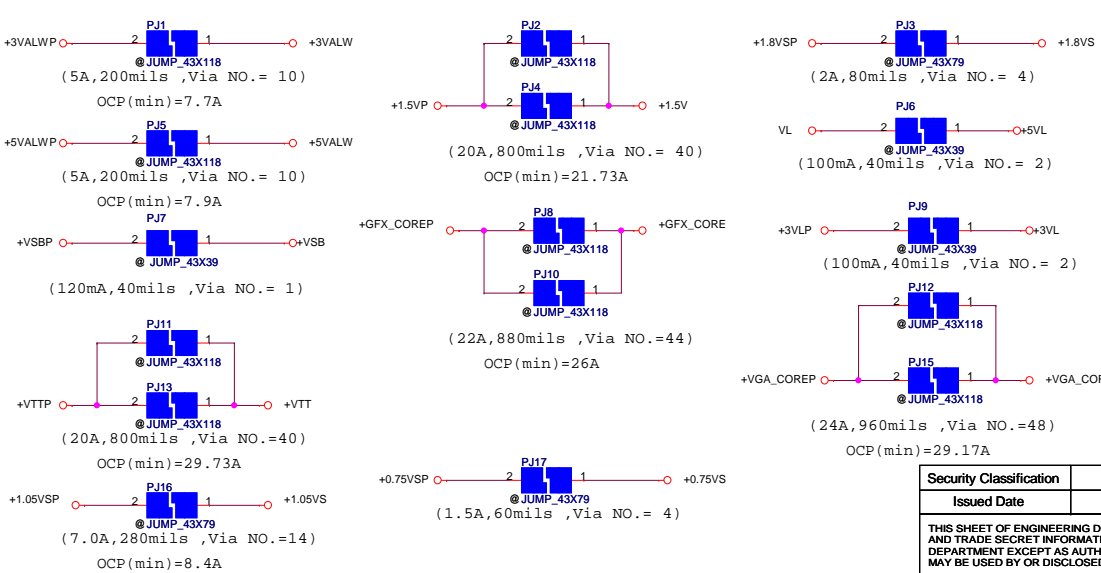


3.3V

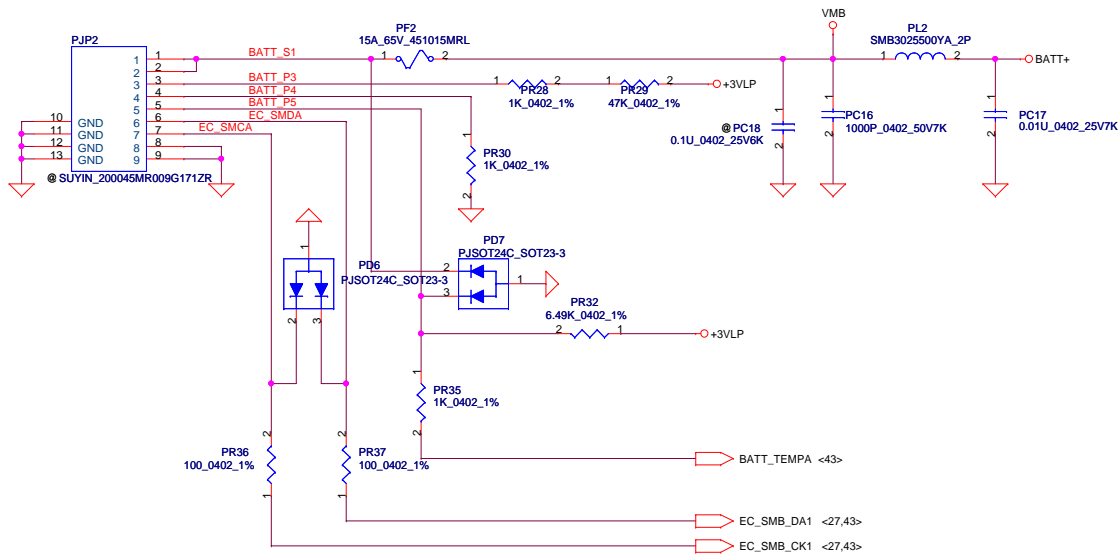
SP093MX0000



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

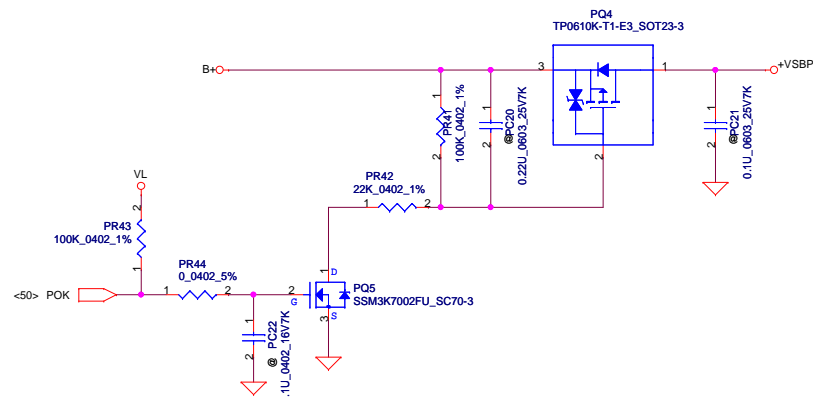
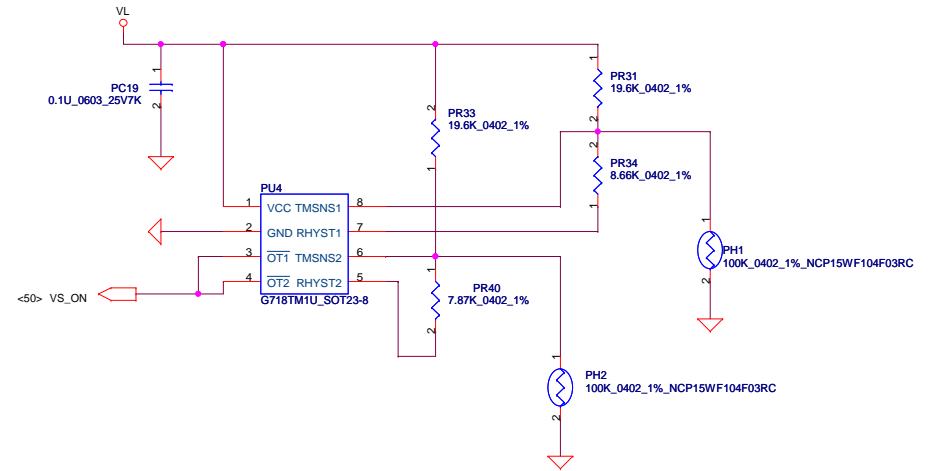


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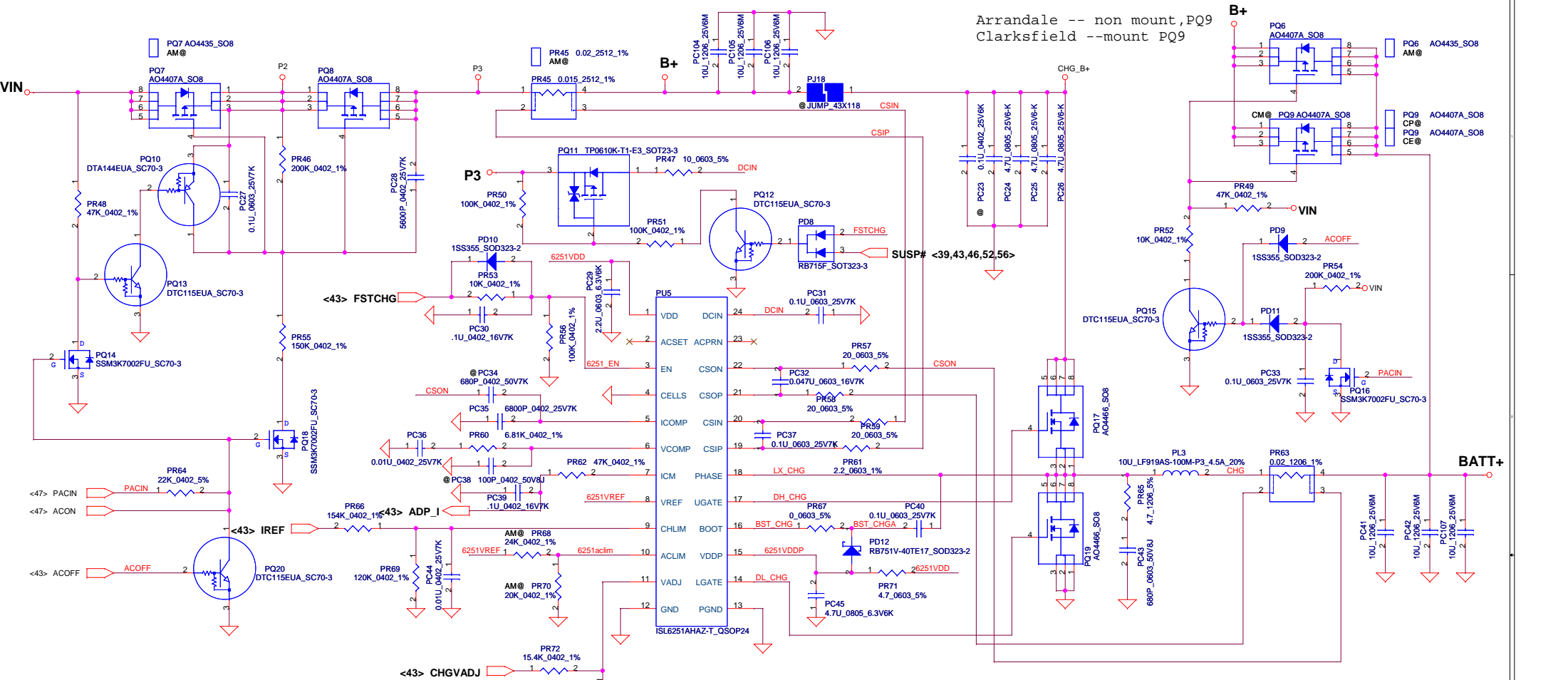
PH1 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C

PH2 near main Battery CONN :
 BAT. thermal protection at 95 degree C
 Recovery at 48 degree C



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Arrandale -- non mount, PQ9
 Clarksville -- mount PQ9

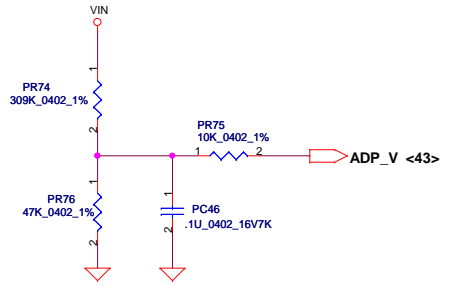


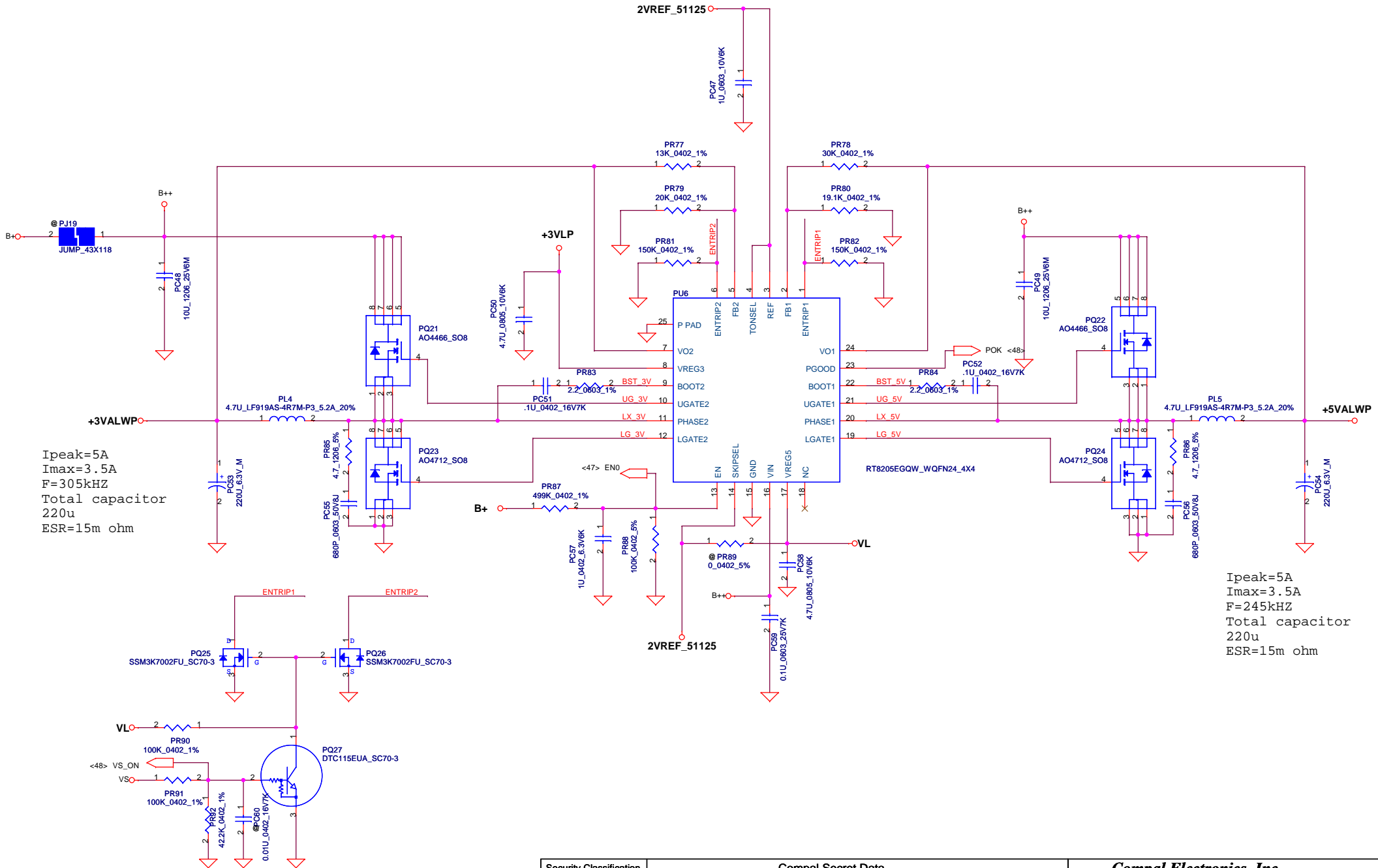
CP mode
 $I_{ada} = 0 - 3.947A (75W)$ $CP = 92\% * I_{ada}$; $CP = 3.63A$
 $V_{aclim} = 0.736V (75W)$ $PR68 = 24k$ $PR70 = 20k$ $PR49 = 0.02$
 $I_{ada} = 0 - 4.737A (90W)$ $CP = 92\% * I_{ada}$; $CP = 4.36A$
 $V_{aclim} = 0.736V (90W)$ $PR68 = 53.6k$ $PR70 = 20k$ $PR49 = 0.015$
 $I_{ada} = 0 - 6.316A (120W)$ $CP = 92\% * I_{ada}$; $CP = 5.81A$
 $V_{aclim} = 0.736V (120W)$ $PR68 = 8.25k$ $PR70 = 26.7k$ $PR49 = 0.015$

$CC = 0.25A - 3A$
 $I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.254V - 3.048V$
 V_{CHLIM} need over 95mV

$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

- PR68 8.25K_0402_1%
- PR70 26.7K_0402_1%
- CP@
- CP@
- PR68 8.25K_0402_1%
- CE@
- PR68 53.6K_0402_1%
- PR70 20K_0402_1%
- AP@
- AP@
- PR68 53.6K_0402_1%
- APOP@
- APOP@
- PR68 53.6K_0402_1%
- CM@
- CM@

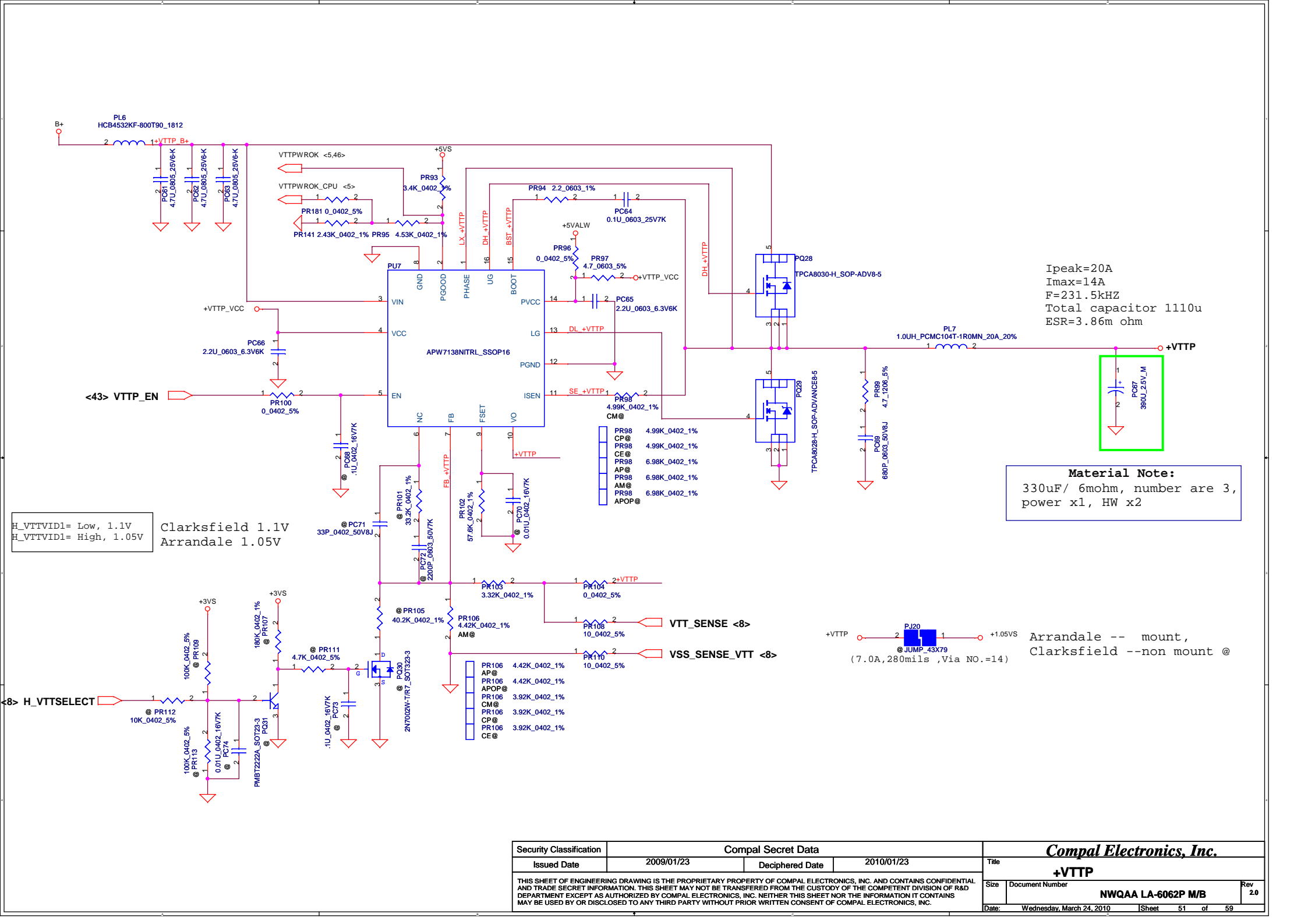




Ipeak=5A
 Imax=3.5A
 F=305kHz
 Total capacitor
 220u
 ESR=15m ohm

Ipeak=5A
 Imax=3.5A
 F=245kHz
 Total capacitor
 220u
 ESR=15m ohm

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Issued Date	2009/01/23	Deciphered Date	2010/01/23	3VALWP/5VALWP	
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Ipeak=20A
 Imax=14A
 F=231.5kHz
 Total capacitor 1110u
 ESR=3.86m ohm

Material Note:
 330uF/ 6mohm, number are 3,
 power x1, HW x2

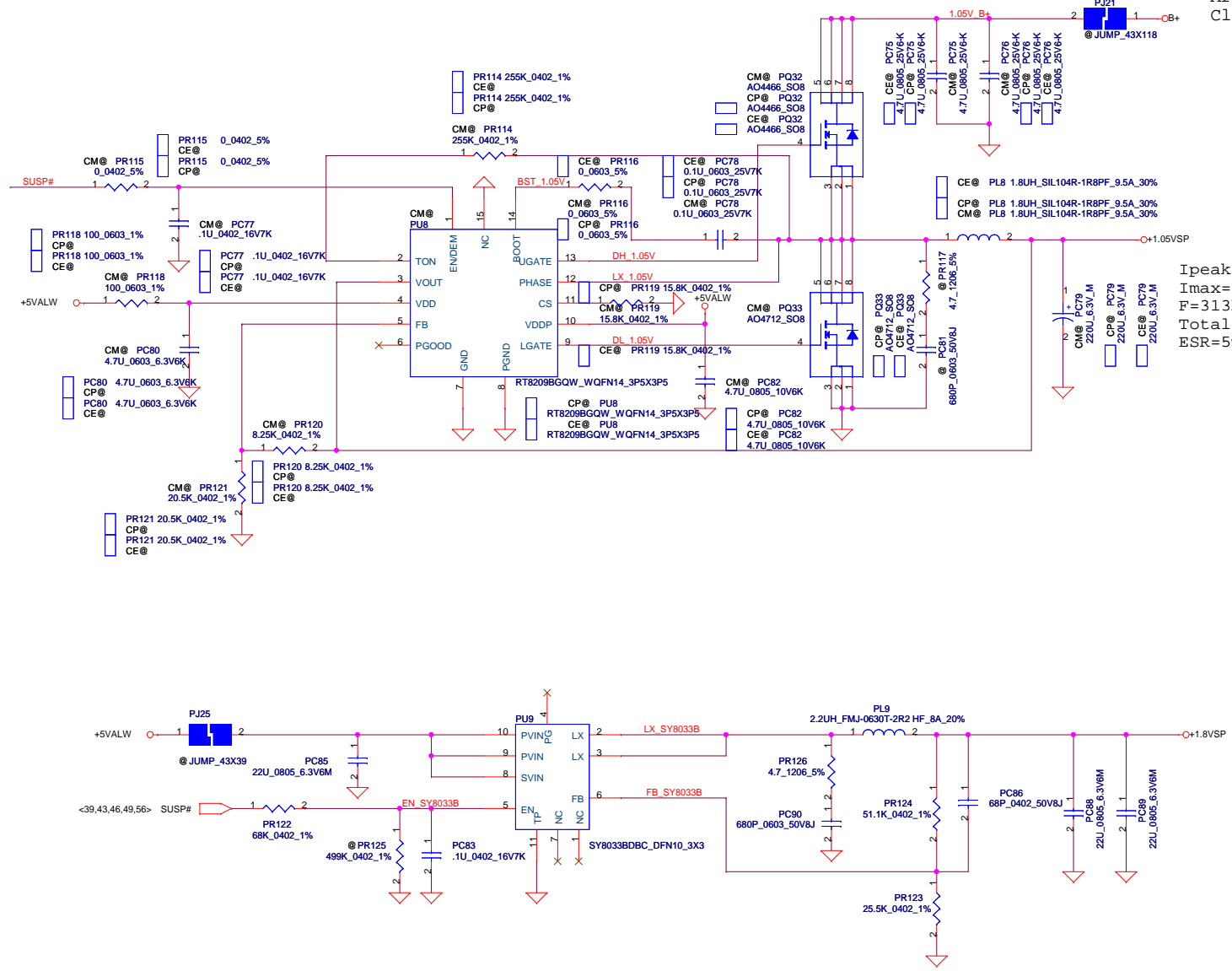
Arrandale -- mount,
 Clarkfield --non mount @

H_VTTVID1= Low, 1.1V
 H_VTTVID1= High, 1.05V

Clarkfield 1.1V
 Arrandale 1.05V

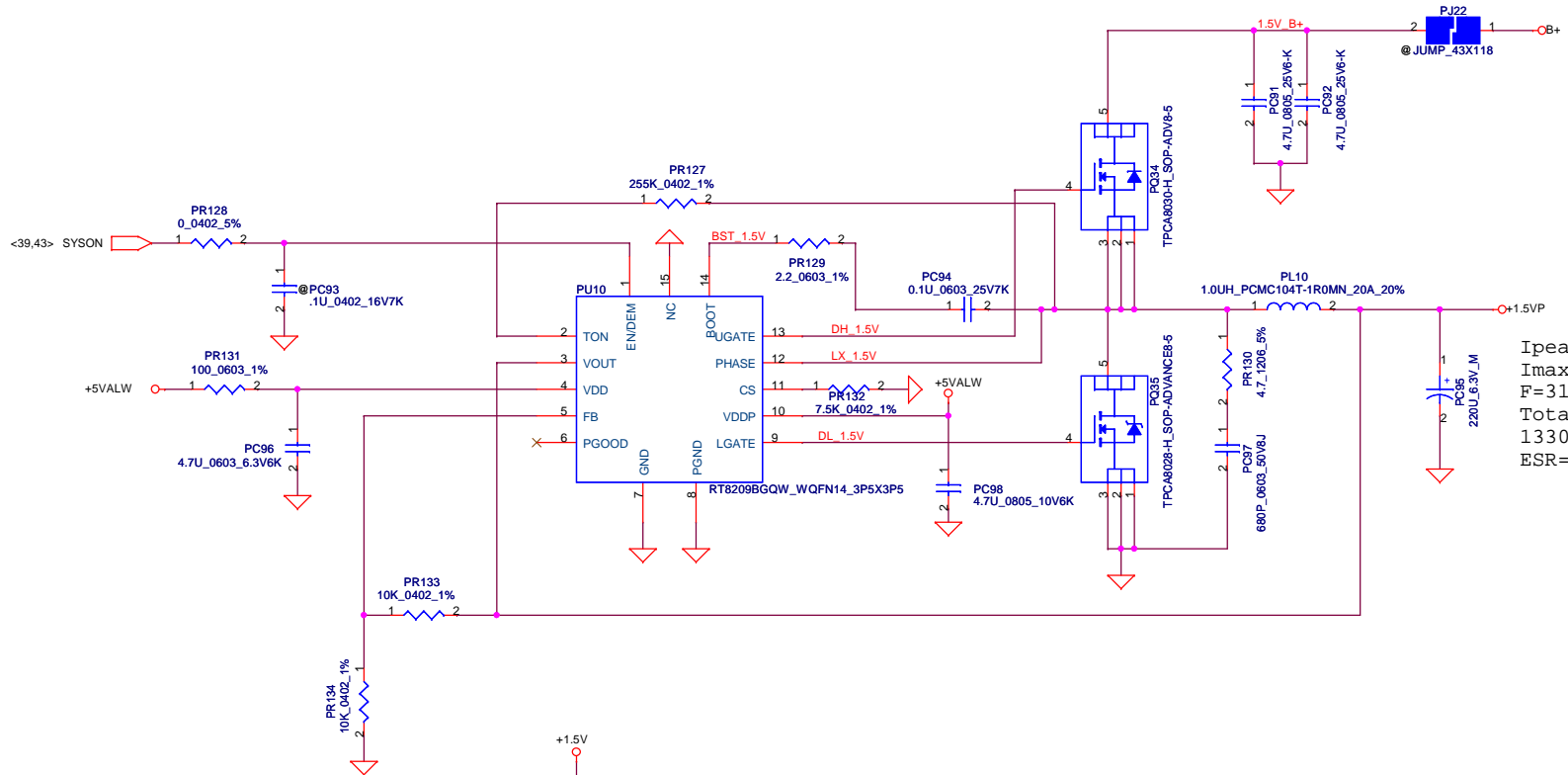
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	+VTTTP	
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Arrandale -- non mount, @
Clarksfield --mount

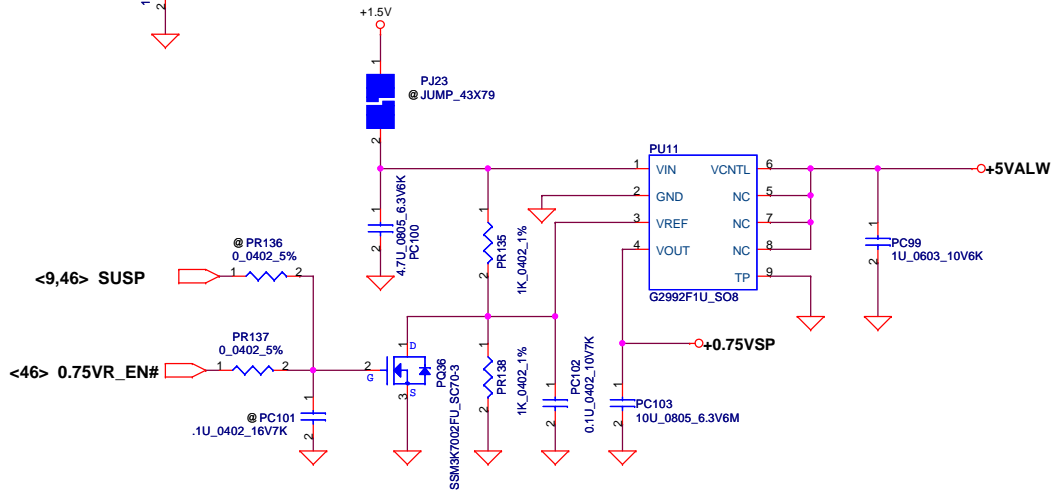


Ipeak=7A
Imax=4.9A
F=31.3kHz
Total capacitor 550u
ESR=5m ohm

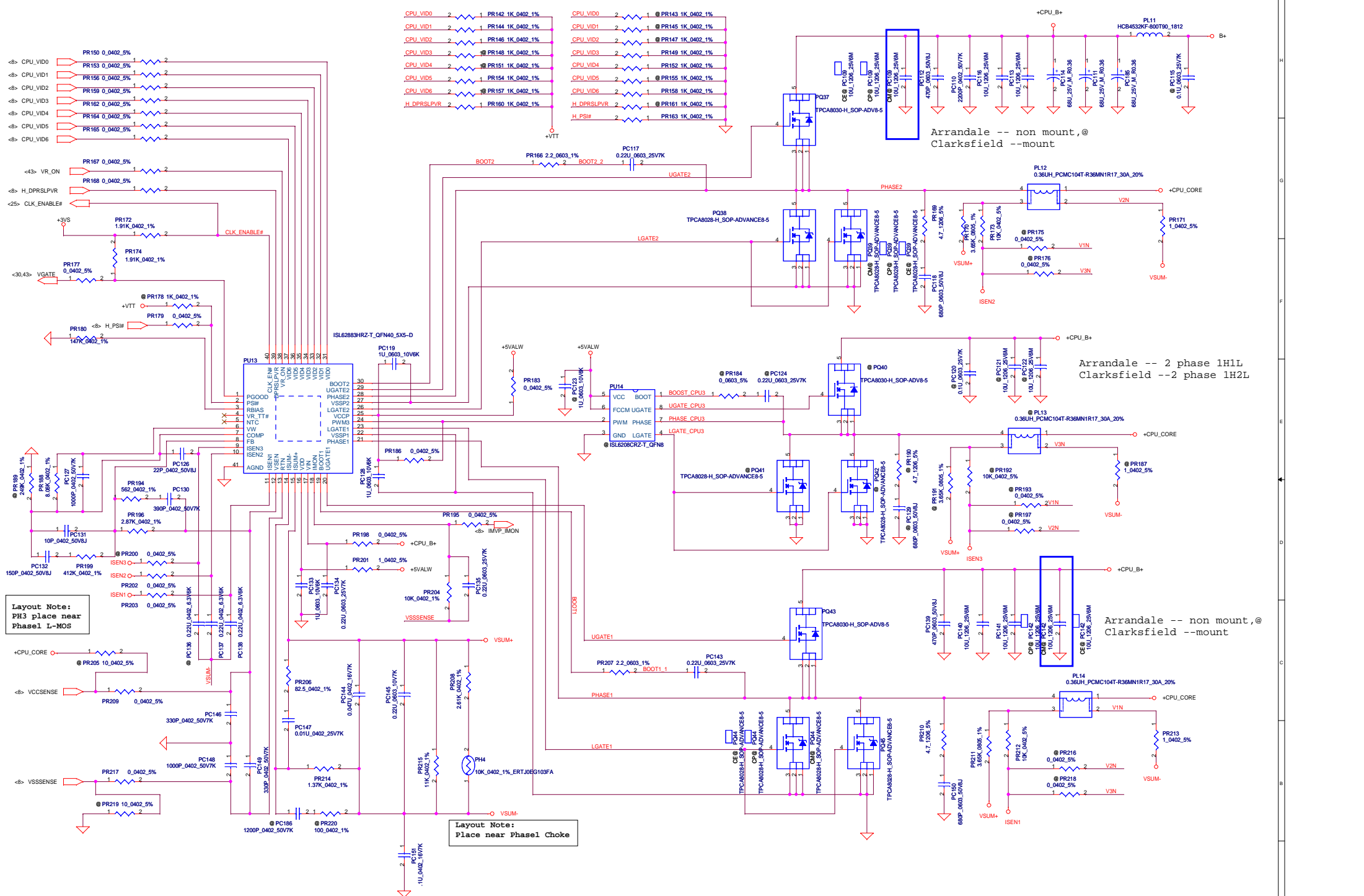
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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Ipeak=20A
 Imax=14A
 F=313kHz
 Total capacitor
 1330u
 ESR=2.55m ohm



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Layout Note:
PH3 place near
Phasel L-MOS

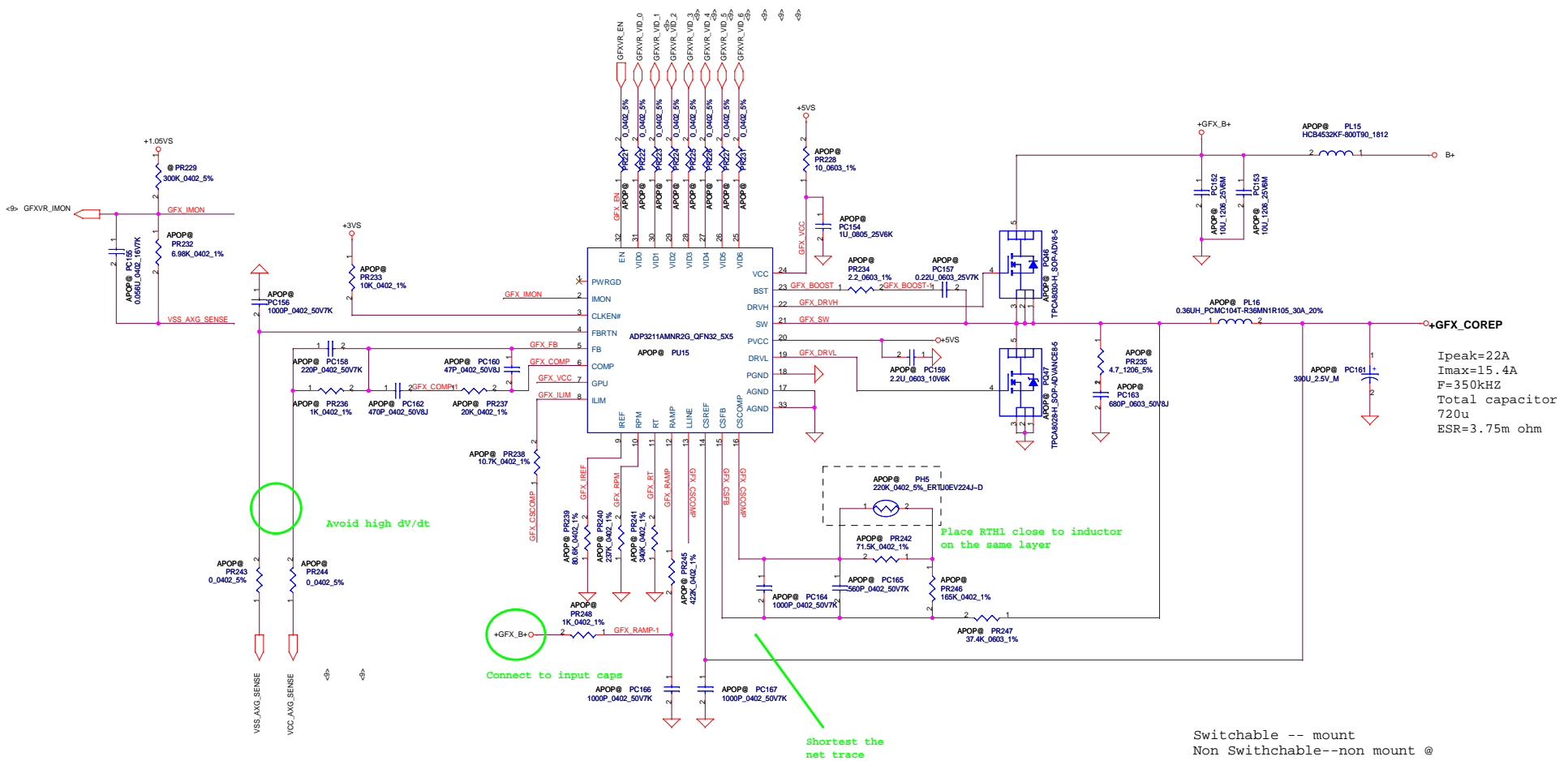
Layout Note:
Place near Phasel Choke

Arrandale -- non mount,
Clarksfield --mount

Arrandale -- 2 phase 1H1L
Clarksfield --2 phase 1H2L

Arrandale -- non mount,
Clarksfield --mount

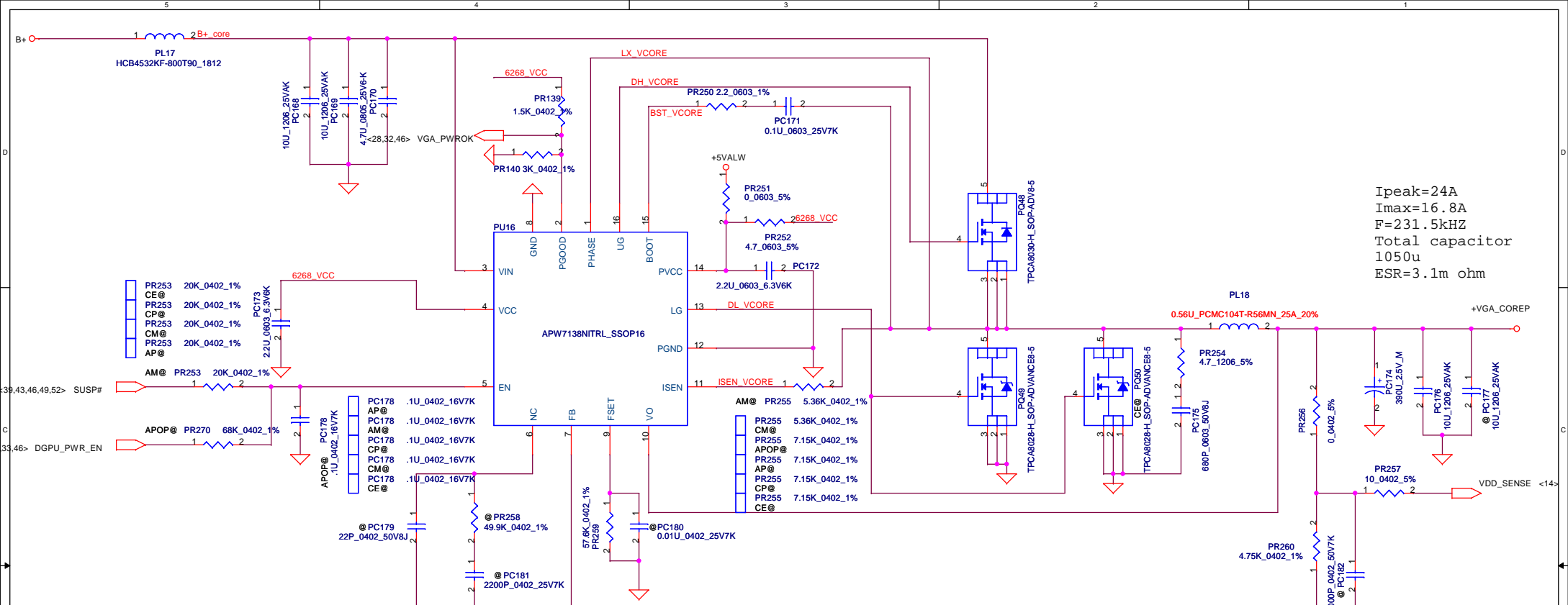
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Issued Date	2009/01/23	+CPU_CORE	
	Deciphered Date	2010/01/23	
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Ipeak=22A
 Imax=15.4A
 F=350kHz
 Total capacitor
 720u
 ESR=3.75m ohm

Switchable -- mount
 Non Switchable--non mount @

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Title	+GFX COREP			Rev
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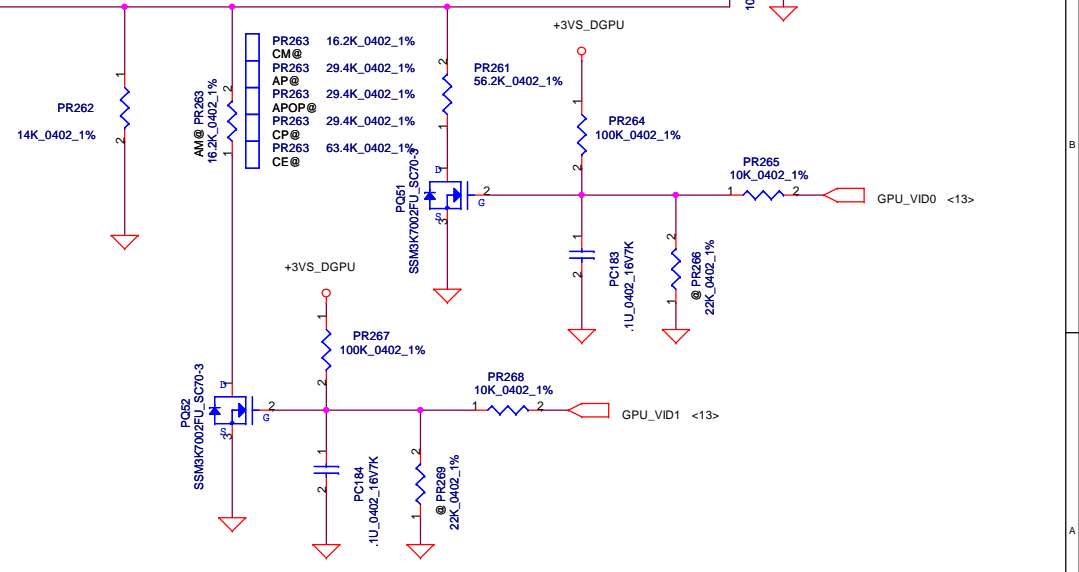
Ipeak=24A
 Imax=16.8A
 F=231.5kHz
 Total capacitor
 1050u
 ESR=3.1m ohm

$FSW = 1 / (75E-12 * 57.6K) = 231.48KHz$

N11M-GE1/OP1	N11P-GE1	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=29.17A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K PQ50=unpop

$VFB(0.6) = Vout * Rbottom / (Rtop + Rbottom)$

GPU_VID0	GPU_VID1	N11M-GE1/N11M-OP1	N11P-GE1	N11E-GE1-LP
0	0		0.80V	0.80V
1	0	0.85V	0.85V	0.85V
0	1		0.95V	0.9V
1	1	1.03V	0.95V	0.9V
		PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 16.2K	PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 29.4K	PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 63.4K



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				+VGA_COREP	
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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT	P53-PWR_1.5VP/0.75VSP	Change PR132 18k to 6.19k	Modify 1.5V OCP to 18.09A (2009/11/25)
EVT	P56-PWR_VGA_COREP	Change PR270 0 to 100 Ohm	Adjust RC for Optimus sequence (2009/11/25)
		Change PC178 0.1U to 0.01U	
EVT	P39-PWR_+VTTP	Change PR141 2.26k to 2.43k	Modify VTTPWROK voltage (2009/11/25)
EVT	P39-PWR_+VTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT	P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT	P56-PWR_VGA_COREP	Remove PC179 22P, PC181 2200P, PR258 49.9k	APW7138 not use this function (2009/11/25)
EVT	P56-PWR_VGA_COREP	Change PR255 7.15k to 9.09k	Modify VGA 11P OCP to 38.03A (2009/11/25)
EVT	P56-PWR_VGA_COREP	Remove PC177 10U	FAE suggest to remove 1 10U cap for IC on time control (2009/11/25)
EVT	P42-PWR_CPU_CORE	Change PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT	P43-PWR_GM VGA_CORE	Change PH5 SL20000058L to SL200000500	Use Compal PN (2009/11/25)
DVT	P56-PWR_VGA_COREP	Change PR255 9.09k to 7.15k	Modify VGA 11P OCP to 29.17A (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT	P39-PWR_+VTTP	Change PR106 4.42k to 3.92k	Modify VTT voltage to 1.1V for Clarkfield (2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PC161 to SGA00002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT	P56-PWR_VGA_COREP	Change PR253 0 to 20k	For VGA sequence(2009/12/28)
DVT	P56-PWR_VGA_COREP	Change PR270 0 to 20k	For VGA sequence(2009/12/28)
DVT	P52-PWR_1.05VSP/1.8VSP	Add PC83 0.1U and change PR122 0 to 68k	For VGA sequence(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT	P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	Reserve for EMI solution(2009/12/28)
DVT	P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR169,PR210 4.7 and PC118,PC150 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P56-PWR_VGA_COREP	Add PR254 4.7 and PC175 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT	P42-PWR_CPU_CORE	Add PQ39,PQ44 TPCA8028-H	Use 1H 2L MOS solution for Clarksfield (2009/12/31)
DVT	P42-PWR_CPU_CORE	Add PC109,PC142 10U input cap	For Clarksfield solution (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR214 1.2k to 1.37k	Adjust CPO_CORE OCP to 65A (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR196 2.43k to 2.87k	Adjust CPU_CORE load line (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR204 8.25k to 10k	Adjust resistor for Imon (2009/12/31)
DVT	P39-PWR_+VTTP	Change PR98 4.99k to 6.98k	Adjust VTT_DIS_Arrandale OCP to 29.73A (2009/12/31)
DVT	P53-PWR_1.5VP/0.75VSP	Change PR132 6.19k to 7.5k	Adjust 1.5V OCP to 21.73A(2009/12/31)
DVT	P52-PWR_1.05VSP/1.8VSP	Change PQ33 from FDS6670 to AO4712	Change design rating(2009/12/31)
DVT	P39-PWR_+VTTP	Change PR98 6.98k to 4.99k	Adjust VTT_DIS_Clarksfield OCP to 20.64A (2009/12/31)
DVT	P55-PWR_GM VGA_CORE	Change PR247 34.8k to 37.4k	Adjust GFX load line (2009/12/31)
DVT	P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
DVT	P56-PWR_VGA_COREP	Change PR270 20k to 68k, PC178 0.01U to 0.1U	Adjust Optimus sequence (2010/01/06)
PVT	P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PC161 to SF000002000	Change to original type for PVT (2010/02/03)
PVT	P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT	P52-PWR_1.05VSP/1.8VSP	Change PR119 10k to 15.8k	Adjust 1.05V OCP to 8.47A (2010/02/03)

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
			Change PC85 from 0.1U to 22U	
			Delete PC87 10UF, PC84 0.1U	
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP		P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PR68 from 53.6k to 24k, PR45 from 0.015 to 0.02 Ohm	Change CP from 90W to 75W(For cost down)(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PQ6,PQ7 from AO4407A to AO4435	Change MOS reting for 75W adapter(For cost down)(2010/03/07)
Pre MP		P56-PWR_VGA_COREP	Add PR264,PR267 100k	Use 100k resistor to pull high +3VS_DGPU(Set initial VID to P0 state)(2010/03/07)

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				Calpella common	
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HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 0.2
 GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	37	Add +5VALW and +5VL for JPIO pin5	For BACK_SENSE detect
2	12/7	46	Change PJ32 to R104 and PJ33 to R144	For discrete BOM structure
3	12/7	25	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
4	12/8	45	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
5	12/8	13	Add QV2, RV110, RV123 and RV124	For CLK_REQ VGA# level shifter
6	12/14	25	Add C495 and C496	For RF request
7	12/15	33	Add R258	For OPTIMUS_EN#
8	12/15	34	Add C499	For power team request
9	12/17	45	Remove D19	Move D19 to LS-6061P
10	12/18	38	Reverse JBT pin definition	Due to pin reverse
11	12/18	42	Add RA42	For codec EC_MUTE# issue
12	12/21	41	Change JREAD to Push-push type (R015-211-LM-A)	For PRD update
13	12/21	25	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
14	12/22	44	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
15	12/23	39	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
16	12/23	33	Add R461	For CIR_EN#
17	12/24	25	Mount C236 and C268	For ESD request
18	12/24	37	Change JPIO footprint and reverse its pin definition	For ME request
19	12/24	27	Add R145	For U9 ESD damage issue
20	12/24	41	Add F3	For connector short issue
21	12/28	42	Change RA41 to SM01000CY00 (FEMA-10-100505-301T)	For EMI request
22	12/28	25	Remove L1	For 3D panel
23	12/29	42	Change RA1, RA18 and RA20 to SM01000B200	For RF request
24	12/29	25	Change C484 to 100P	For RF request
25	1/6	37	Change C426 to SF000001500	For cost down
26	1/12	38	Change R132 BOM from FLICA@ to FELICA@	For Felica issue
27	1/12	11	Change C218 to SF000002000	For cost down
28	1/12	8	Change C144 to SF000002200	For thermal interfere issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.2 TO 0.3
 GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	42	Add RA43	For sleep & music on battery mode
2	1/15	46	Change +1.05VS_DGPU to N-MOS	For +1.05VS_DGPU drop issue
3	1/21	43	Add R462	Avoid VR_ON floating
4	1/25	44	Change UG3 to SA000022I00	For LDO issue
5	1/25	45	Change SW2 to @	For ME interfere issue
6	1/27	9	Change CV57, CV58 abd C271 to OS-CON	For cost down
7	2/1	25	Add +LCD_VDD to JLVDS pin18	For CMO 3D Panel
8	2/1	27	Add R208	For AOC monitor issue
9	2/1	43	Change U19 to SA00001J5A0	For KB926 E0 version
10	2/1	39	Add +1.5VS for J3G	For TV tuner MC770A
11	2/1	41	Remove F3	For UCL ES2 sample
12	2/2	43	Add CAP_RST# to EC	For ESD issue
13	2/3	41	Change RC7 to 33 ohm	For EMI request
14	2/4	42	Remove RA40, add RA44 and RA22	For audio issue
15	2/4	14	Reserve VBIOS ROM	For SW request
16	2/5	32	Swap USB port4 and port8	For customer request
17	2/5	13	Reserve 27MHz crystal	For HDMI issue
18	2/9	40	Change L11 to 2.2U and C113 to 4.7U	For Realtek request
19	2/10	41	Change RC7-RC14 to 22 ohm	For O2 request
20	2/10	27	Remove HDMI common mode choke	For cost down

NWQAA LA-6062P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.3 TO 1.0
 GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	32	Change R390 to 1K	For Optimus sequence
2	3/6	33	Change R59 to 1K	For Optimus sequence
3	3/6	27	Change Q18 and Q19 power to +3VS_DGPU	For GPU power rail
4	3/6	41	Add QC2 and RC16	For O2 B0 workaround
5	3/7	28	Change D13.2 power to +CHGRTC	For RTC issue
6	3/8	32	Add R333 and R334	For Optimus sequence
7	3/8	25	Add BOM structure 3D@ and NO3D@	For 3D SKU PWM
8	3/8	13	Change YV1 to SJ100006R00	For cost down
9	3/11	46	Change C685 to 0603 size	For ME height limit
10	3/11	45	Change H15-H19 to H_3P3	For ME request
11	3/15	45	Remove SW2	For ESD request
12	3/15	42	Change CA9 and CA10 to 1U	For cut-off frequency
13	3/16	42	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 1.0 TO 2.0
 GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	41	Change cardreader to JMB385/389	For customer request
2	3/18	34	Add R49	For CRT wave issue
3	3/19	13	Change LV3 to always stuff	For NVIDIA request
4	3/19	34	Change L12 to 2.2 ohm for Optimus SKU	For CRT wave issue
5	3/22	27	Add D54	For HDMI CEC issue
6	3/24	25	Change C214 to 1U	For NALAA ESATA performance low issue

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