

Compal Confidential

NAL90/NALG0 M/B Schematics Document

Intel Auburndale/Clarksville Processor with DDRIII + Ixex Peak-M

2009-10-20

REV: 1.0

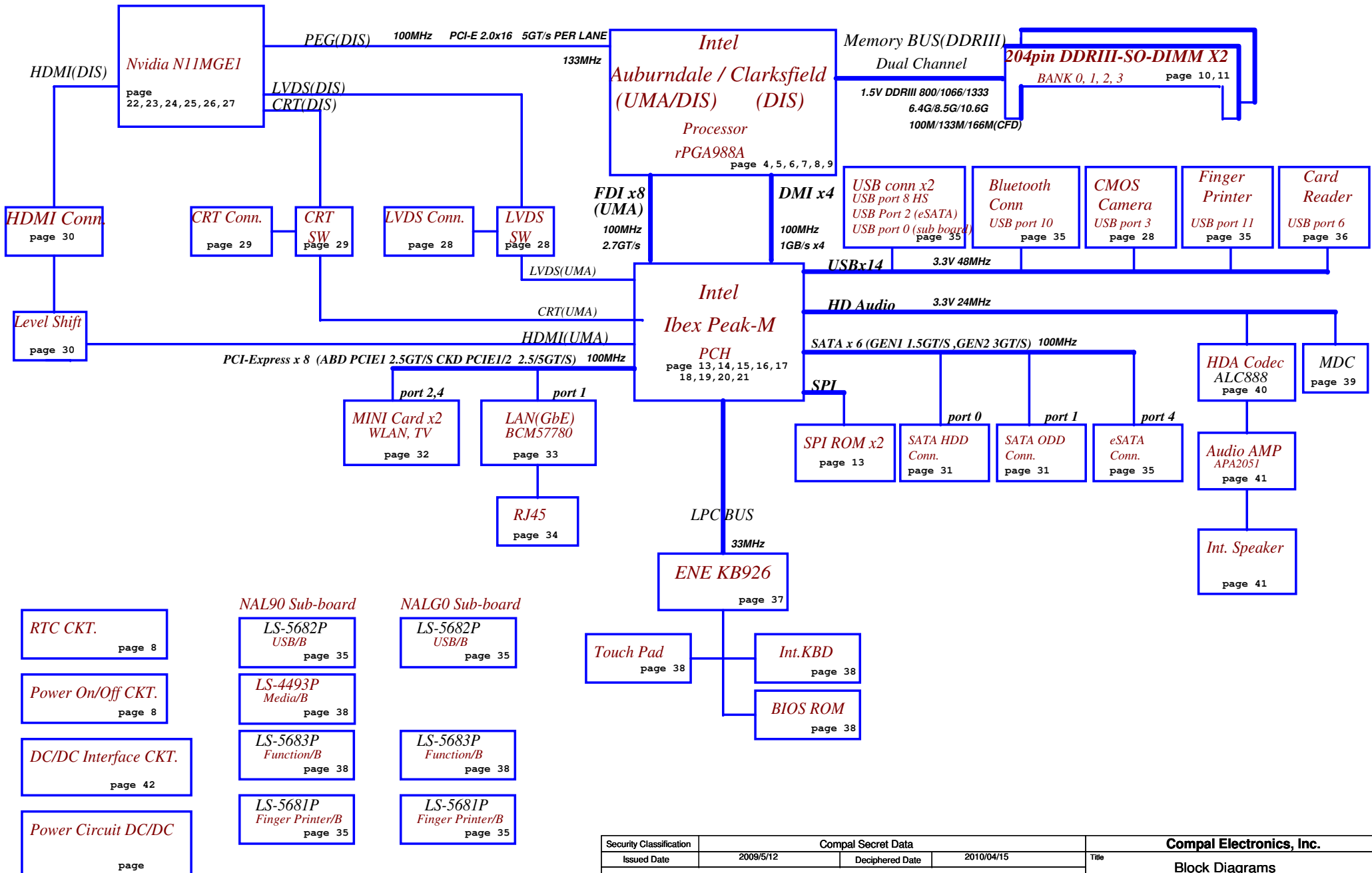
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	Cover Page
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Model Name NALG0
File Name : LA5681P

Fan Control
page 41

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHz to PCH
48MHz to CardReader
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+GFX_core	Core voltage for CPU	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+VGA_CORE	Core voltage for N11M VGA	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5VS	1.5V power rail for DDRIII	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	PCH	
		VGA	

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Mini card	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA only	UMA only@
DIS	DIS@
DIS Only	DIS only@
Switchable	SG@
	XDP@
	NonSG@
	MINI2@
	FP@
	eDriver@
	Dmic@
	Caps@
	X76@
	HDCP@
	AMIC@
S3 power	S3@
	non S3@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	Ext4 HS USB
		1	sub Board
	UHCI1	2	
		3	Camera
		4	1st Min-Card
		5	2st Min-Card
EHCI2	UHCI2	6	
		7	
	UHCI3	8	Ext4 HS USB
		9	Card Reader
	UHCI4	10	Blue Tooth
		11	Finger Print
12			
13			

BOM Config

UMA only
UMA@/UMA only@/FP@/Dmic@/XDP@/S3@

DIS ONLY

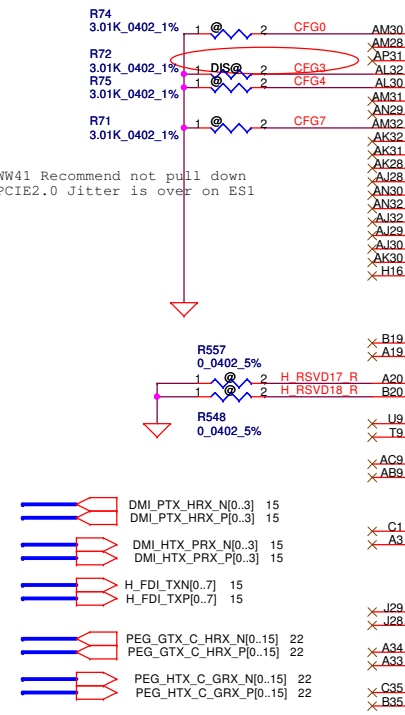
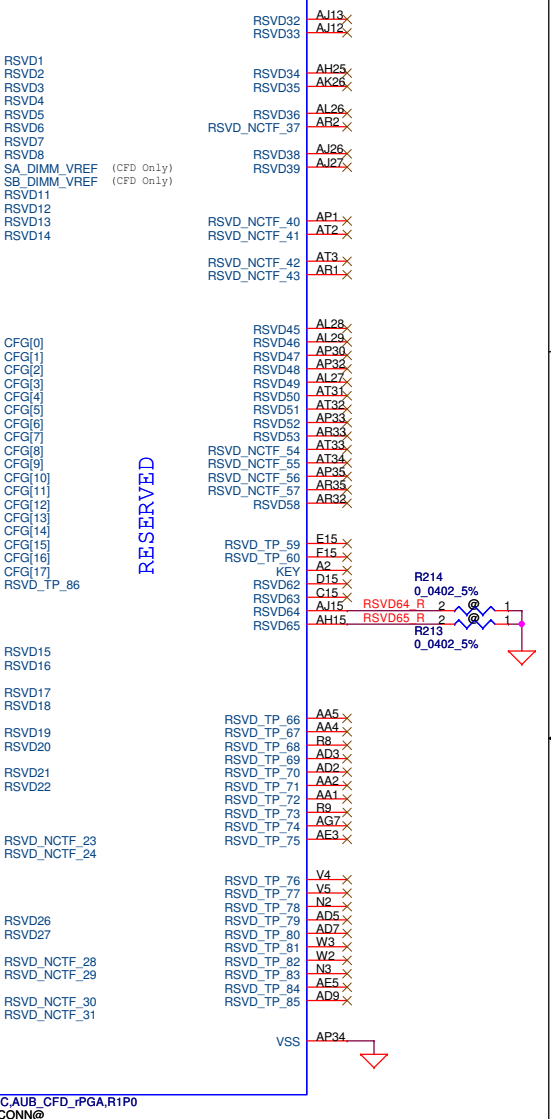
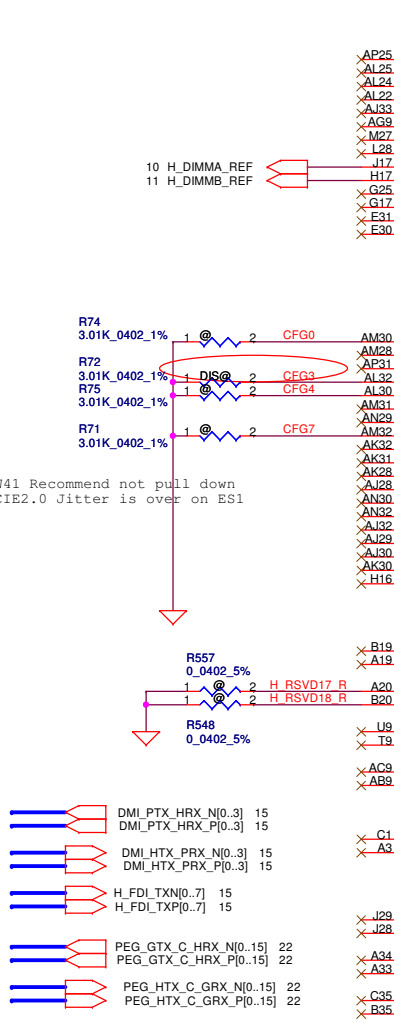
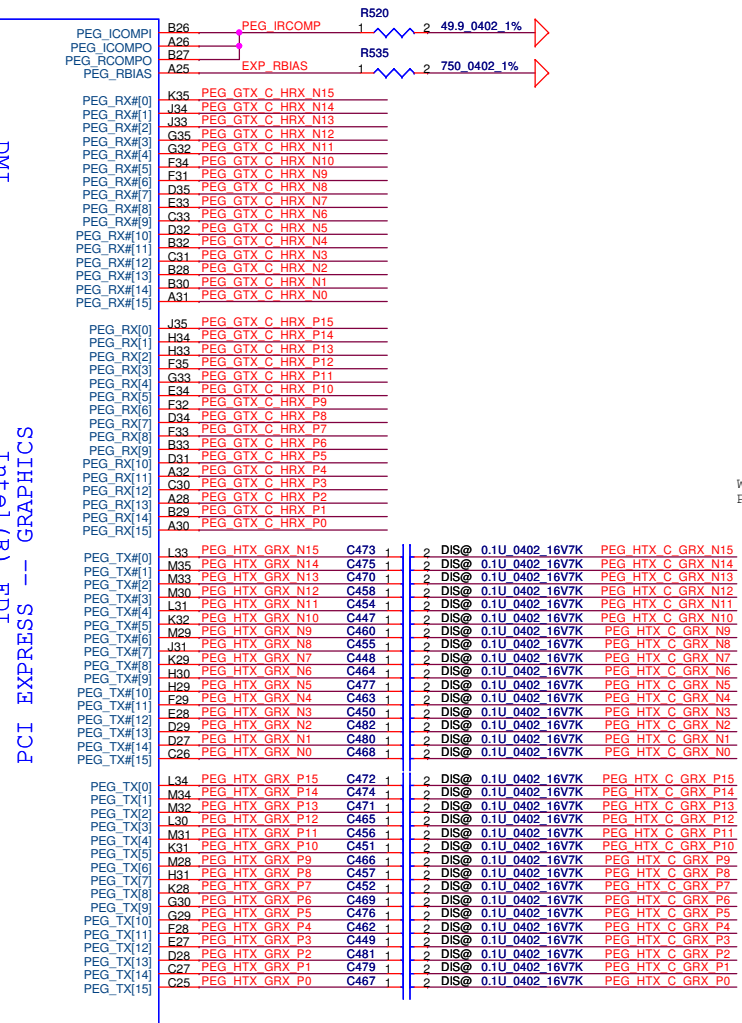
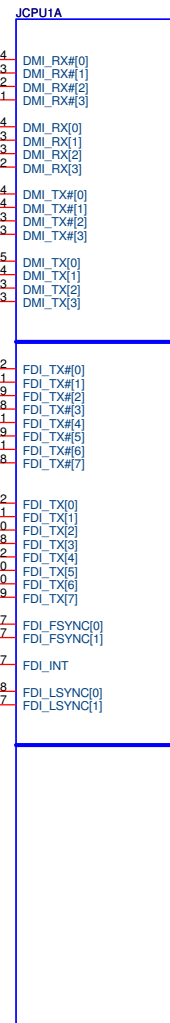
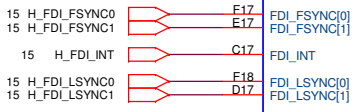
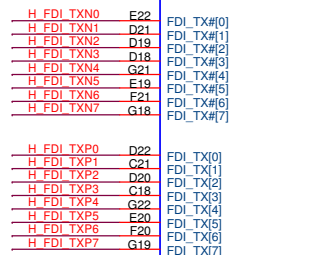
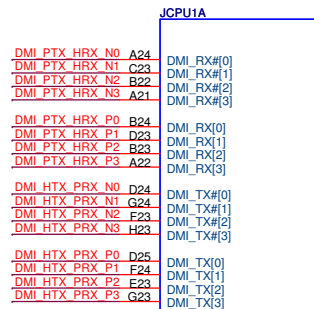
DIS@/DIS only@/FP@/Dmic@/XDP@/S3@

Switchable Graphics

SG@/UMA@/DIS@/FP@/Dmic@/XDP@/S3@

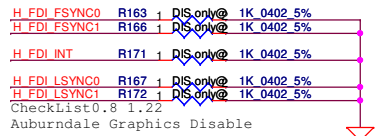
Note:do cost BOM add X76@

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eDP Signals MAPPING

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HPD#	PEG GTX_C_HRX_P12	PEG GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

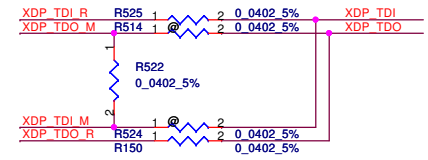
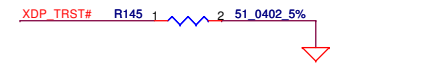
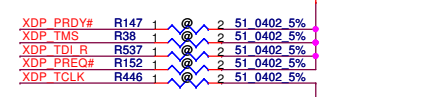
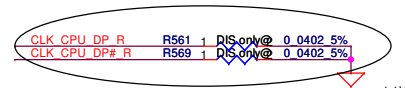
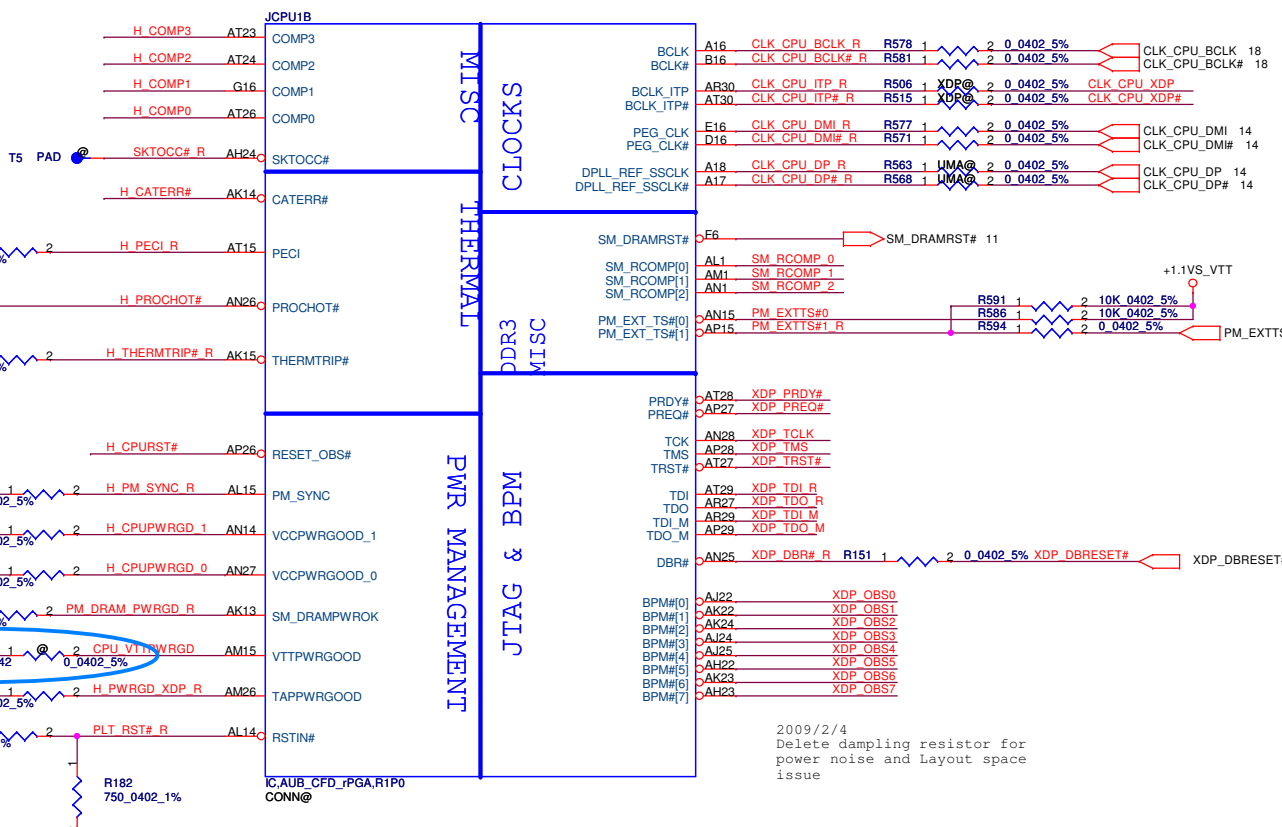
CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

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JTAG MAPPING

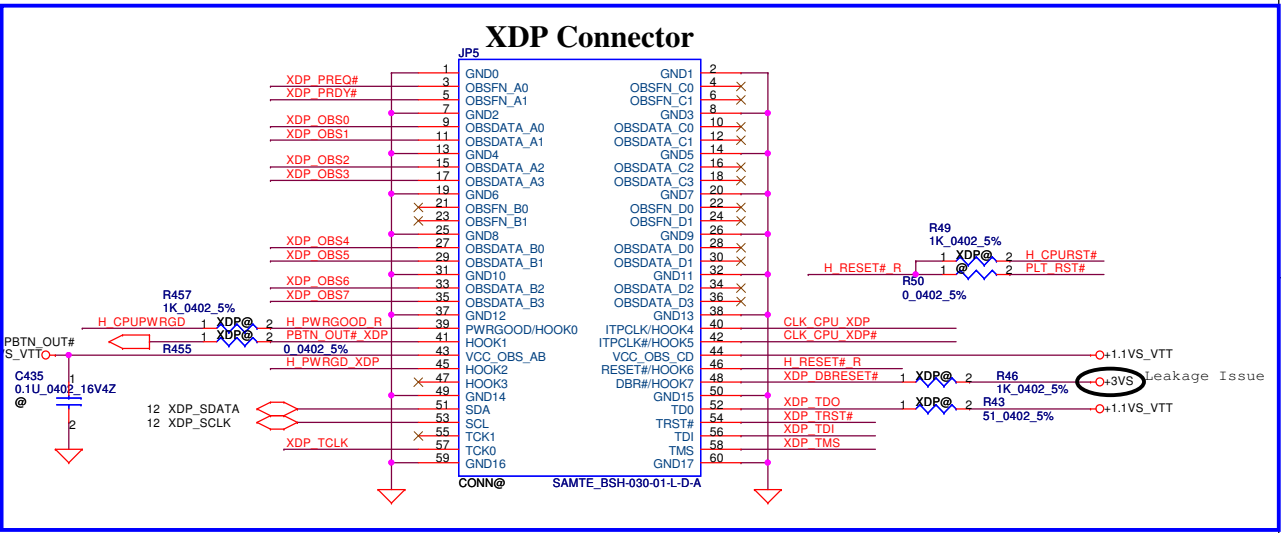
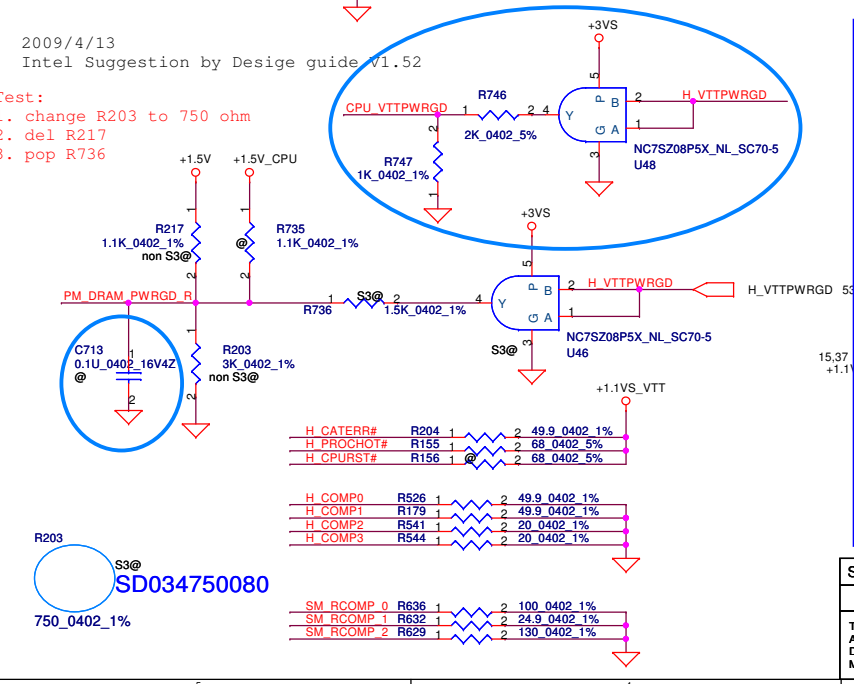
Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657

2009/2/4
Delete damping resistor for power noise and layout space issue

2009/2/4
#414044 DG
Update Rev1.11

2009/4/13
Intel Suggestion by Design guide V1.52

- Test:
- change R203 to 750 ohm
 - del R217
 - pop R736



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10 DDR_A_D[0..63]
 10 DDR_A_DM[0..7]
 10 DDR_A_DQS[0..7]
 10 DDR_A_DQS[0..7]
 10 DDR_A_MA[0..15]

JCPU1C

DDR A D0 A10
 DDR A D1 C10
 DDR A D2 C7
 DDR A D3 A7
 DDR A D4 B10
 DDR A D5 D10
 DDR A D6 E10
 DDR A D7 A8
 DDR A D8 D8
 DDR A D9 F10
 DDR A D10 E6
 DDR A D11 E2
 DDR A D12 E9
 DDR A D13 B7
 DDR A D14 E7
 DDR A D15 C6
 DDR A D16 H8
 DDR A D17 G8
 DDR A D18 K7
 DDR A D19 J8
 DDR A D20 G7
 DDR A D21 G10
 DDR A D22 J7
 DDR A D23 J10
 DDR A D24 L7
 DDR A D25 M6
 DDR A D26 M8
 DDR A D27 L9
 DDR A D28 L6
 DDR A D29 K8
 DDR A D30 N8
 DDR A D31 P9
 DDR A D32 AH5
 DDR A D33 AF5
 DDR A D34 AK6
 DDR A D35 AK7
 DDR A D36 AF6
 DDR A D37 AG5
 DDR A D38 AI7
 DDR A D39 AI6
 DDR A D40 AJ10
 DDR A D41 AI9
 DDR A D42 AL10
 DDR A D43 AK12
 DDR A D44 AK8
 DDR A D45 AL7
 DDR A D46 AK11
 DDR A D47 AL8
 DDR A D48 AN8
 DDR A D49 AM10
 DDR A D50 AR11
 DDR A D51 AL11
 DDR A D52 AM9
 DDR A D53 AN9
 DDR A D54 AT11
 DDR A D55 AP12
 DDR A D56 AM12
 DDR A D57 AN12
 DDR A D58 AM13
 DDR A D59 AT14
 DDR A D60 AT12
 DDR A D61 AL13
 DDR A D62 AR14
 DDR A D63 AP14
 SA_DQ[0]
 SA_DQ[1]
 SA_DQ[2]
 SA_DQ[3]
 SA_DQ[4]
 SA_DQ[5]
 SA_DQ[6]
 SA_DQ[7]
 SA_DQ[8]
 SA_DQ[9]
 SA_DQ[10]
 SA_DQ[11]
 SA_DQ[12]
 SA_DQ[13]
 SA_DQ[14]
 SA_DQ[15]
 SA_DQ[16]
 SA_DQ[17]
 SA_DQ[18]
 SA_DQ[19]
 SA_DQ[20]
 SA_DQ[21]
 SA_DQ[22]
 SA_DQ[23]
 SA_DQ[24]
 SA_DQ[25]
 SA_DQ[26]
 SA_DQ[27]
 SA_DQ[28]
 SA_DQ[29]
 SA_DQ[30]
 SA_DQ[31]
 SA_DQ[32]
 SA_DQ[33]
 SA_DQ[34]
 SA_DQ[35]
 SA_DQ[36]
 SA_DQ[37]
 SA_DQ[38]
 SA_DQ[39]
 SA_DQ[40]
 SA_DQ[41]
 SA_DQ[42]
 SA_DQ[43]
 SA_DQ[44]
 SA_DQ[45]
 SA_DQ[46]
 SA_DQ[47]
 SA_DQ[48]
 SA_DQ[49]
 SA_DQ[50]
 SA_DQ[51]
 SA_DQ[52]
 SA_DQ[53]
 SA_DQ[54]
 SA_DQ[55]
 SA_DQ[56]
 SA_DQ[57]
 SA_DQ[58]
 SA_DQ[59]
 SA_DQ[60]
 SA_DQ[61]
 SA_DQ[62]
 SA_DQ[63]

DDR SYSTEM MEMORY A

SA_CK[0] AA6
 SA_CK#0 AA7
 SA_CKE[0] P7
 SA_CK[1] Y6
 SA_CK#1 Y5
 SA_CKE[1] P6
 SA_CS#0 CAE2
 SA_CS#1 CAE8
 SA_ODT[0] AD8
 SA_ODT[1] AF9
 SA_DM[0] B9
 SA_DM[1] D7
 SA_DM[2] LH7
 SA_DM[3] M7
 SA_DM[4] AG6
 SA_DM[5] AM7
 SA_DM[6] AN10
 SA_DM[7] AN13
 SA_DQS#0 C9
 SA_DQS#1 CE8
 SA_DQS#2 CJ9
 SA_DQS#3 CH9
 SA_DQS#4 CAK9
 SA_DQS#5 CAP11
 SA_DQS#6 CAT13
 SA_DQS#7
 SA_DQS[0] C8
 SA_DQS[1] F9
 SA_DQS[2] LH9
 SA_DQS[3] MH9
 SA_DQS[4] AK10
 SA_DQS[5] AN11
 SA_DQS[6] AR13
 SA_DQS[7]
 SA_MA[0] Y3
 SA_MA[1] W1
 SA_MA[2] AA8
 SA_MA[3] AA3
 SA_MA[4] V1
 SA_MA[5] AA9
 SA_MA[6] V8
 SA_MA[7] T1
 SA_MA[8] Y9
 SA_MA[9] U6
 SA_MA[10] AD4
 SA_MA[11] T2
 SA_MA[12] U3
 SA_MA[13] AG8
 SA_MA[14] T3
 SA_MA[15] V9
 DDR A DM0
 DDR A DM1
 DDR A DM2
 DDR A DM3
 DDR A DM4
 DDR A DM5
 DDR A DM6
 DDR A DM7
 DDR A DQS#0
 DDR A DQS#1
 DDR A DQS#2
 DDR A DQS#3
 DDR A DQS#4
 DDR A DQS#5
 DDR A DQS#6
 DDR A DQS#7
 DDR A DQS0
 DDR A DQS1
 DDR A DQS2
 DDR A DQS3
 DDR A DQS4
 DDR A DQS5
 DDR A DQS6
 DDR A DQS7
 DDR A MA0
 DDR A MA1
 DDR A MA2
 DDR A MA3
 DDR A MA4
 DDR A MA5
 DDR A MA6
 DDR A MA7
 DDR A MA8
 DDR A MA9
 DDR A MA10
 DDR A MA11
 DDR A MA12
 DDR A MA13
 DDR A MA14
 DDR A MA15
 DDR A CLK0 10
 DDR A_CLK0# 10
 DDR A_CKE0 10
 DDR A_CLK1 10
 DDR A_CLK1# 10
 DDR A_CKE1 10
 DDR A_CS0# 10
 DDR A_CS1# 10
 DDR A_ODT0 10
 DDR A_ODT1 10
 DDR A_DM0
 DDR A_DM1
 DDR A_DM2
 DDR A_DM3
 DDR A_DM4
 DDR A_DM5
 DDR A_DM6
 DDR A_DM7
 DDR A_DQS#0
 DDR A_DQS#1
 DDR A_DQS#2
 DDR A_DQS#3
 DDR A_DQS#4
 DDR A_DQS#5
 DDR A_DQS#6
 DDR A_DQS#7
 DDR A_DQS0
 DDR A_DQS1
 DDR A_DQS2
 DDR A_DQS3
 DDR A_DQS4
 DDR A_DQS5
 DDR A_DQS6
 DDR A_DQS7
 DDR A_MA0
 DDR A_MA1
 DDR A_MA2
 DDR A_MA3
 DDR A_MA4
 DDR A_MA5
 DDR A_MA6
 DDR A_MA7
 DDR A_MA8
 DDR A_MA9
 DDR A_MA10
 DDR A_MA11
 DDR A_MA12
 DDR A_MA13
 DDR A_MA14
 DDR A_MA15

IC_AUB_CFD_rPGA,R1P0
 CONN@

11 DDR_B_D[0..63]
 11 DDR_B_DM[0..7]
 11 DDR_B_DQS#0[0..7]
 11 DDR_B_DQS[0..7]
 11 DDR_B_MA[0..15]

JCPU1D

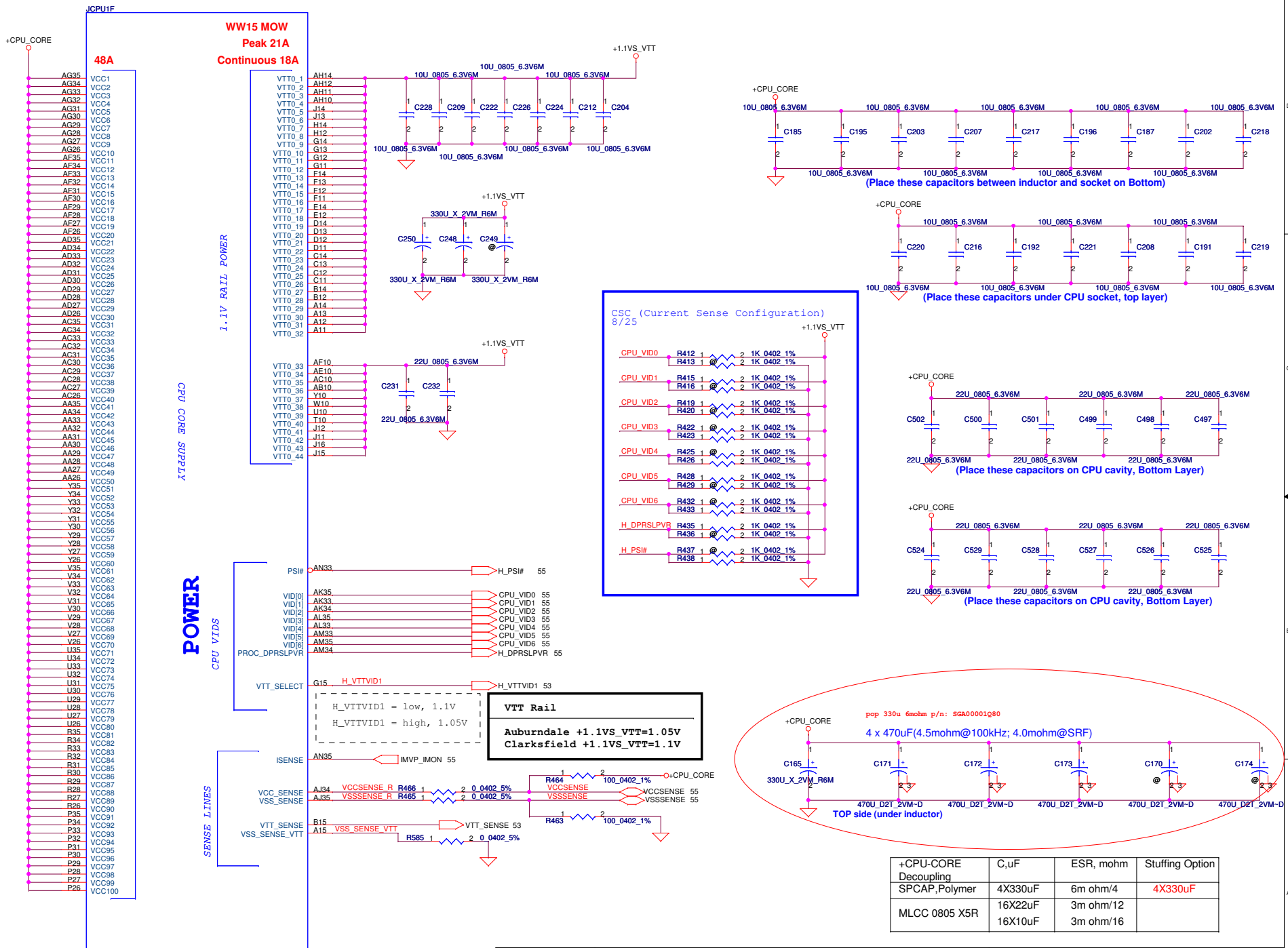
DDR B D0 B5
 DDR B D1 A5
 DDR B D2 C3
 DDR B D3 B3
 DDR B D4 E4
 DDR B D5 A6
 DDR B D6 C4
 DDR B D7 D4
 DDR B D8 D1
 DDR B D9 D2
 DDR B D10 F2
 DDR B D11 F1
 DDR B D12 C2
 DDR B D13 F5
 DDR B D14 F3
 DDR B D15 G4
 DDR B D16 H6
 DDR B D17 G2
 DDR B D18 J6
 DDR B D19 J3
 DDR B D20 G1
 DDR B D21 G5
 DDR B D22 J2
 DDR B D23 J1
 DDR B D24 J5
 DDR B D25 L3
 DDR B D26 K2
 DDR B D27 M1
 DDR B D28 K5
 DDR B D29 K4
 DDR B D30 M4
 DDR B D31 N5
 DDR B D32 AG1
 DDR B D33 AG1
 DDR B D34 AG1
 DDR B D35 AK1
 DDR B D36 AG4
 DDR B D37 AG3
 DDR B D38 AJ4
 DDR B D39 AH4
 DDR B D40 AK3
 DDR B D41 AK4
 DDR B D42 AM6
 DDR B D43 AN2
 DDR B D44 AK5
 DDR B D45 AK2
 DDR B D46 AM4
 DDR B D47 AM3
 DDR B D48 AP3
 DDR B D49 AN5
 DDR B D50 AT4
 DDR B D51 AN6
 DDR B D52 AN4
 DDR B D53 AN5
 DDR B D54 AT5
 DDR B D55 AT6
 DDR B D56 AN7
 DDR B D57 AP6
 DDR B D58 AP8
 DDR B D59 AT9
 DDR B D60 AT7
 DDR B D61 AP9
 DDR B D62 AR10
 DDR B D63 AT10
 SB_DQ[0]
 SB_DQ[1]
 SB_DQ[2]
 SB_DQ[3]
 SB_DQ[4]
 SB_DQ[5]
 SB_DQ[6]
 SB_DQ[7]
 SB_DQ[8]
 SB_DQ[9]
 SB_DQ[10]
 SB_DQ[11]
 SB_DQ[12]
 SB_DQ[13]
 SB_DQ[14]
 SB_DQ[15]
 SB_DQ[16]
 SB_DQ[17]
 SB_DQ[18]
 SB_DQ[19]
 SB_DQ[20]
 SB_DQ[21]
 SB_DQ[22]
 SB_DQ[23]
 SB_DQ[24]
 SB_DQ[25]
 SB_DQ[26]
 SB_DQ[27]
 SB_DQ[28]
 SB_DQ[29]
 SB_DQ[30]
 SB_DQ[31]
 SB_DQ[32]
 SB_DQ[33]
 SB_DQ[34]
 SB_DQ[35]
 SB_DQ[36]
 SB_DQ[37]
 SB_DQ[38]
 SB_DQ[39]
 SB_DQ[40]
 SB_DQ[41]
 SB_DQ[42]
 SB_DQ[43]
 SB_DQ[44]
 SB_DQ[45]
 SB_DQ[46]
 SB_DQ[47]
 SB_DQ[48]
 SB_DQ[49]
 SB_DQ[50]
 SB_DQ[51]
 SB_DQ[52]
 SB_DQ[53]
 SB_DQ[54]
 SB_DQ[55]
 SB_DQ[56]
 SB_DQ[57]
 SB_DQ[58]
 SB_DQ[59]
 SB_DQ[60]
 SB_DQ[61]
 SB_DQ[62]
 SB_DQ[63]

DDR SYSTEM MEMORY - B

SB_CK[0] W8
 SB_CK#0 W9
 SB_CKE[0] M3
 SB_CK[1] V7
 SB_CK#1 V6
 SB_CKE[1] M2
 SB_CS#0 AB8
 SB_CS#1 AD6
 SB_ODT[0] AC7
 SB_ODT[1] AD1
 SB_DM[0] D4
 SB_DM[1] E1
 SB_DM[2] H3
 SB_DM[3] K1
 SB_DM[4] AH1
 SB_DM[5] AL2
 SB_DM[6] AR4
 SB_DM[7] AT8
 SB_DQS#0 D5
 SB_DQS#1 E4
 SB_DQS#2 D4
 SB_DQS#3 L4
 SB_DQS#4 AH2
 SB_DQS#5 AR5
 SB_DQS#6 AR8
 SB_DQS#7
 SB_DQS[0] C5
 SB_DQS[1] E3
 SB_DQS[2] H4
 SB_DQS[3] M5
 SB_DQS[4] AG2
 SB_DQS[5] AP5
 SB_DQS[6] AR7
 SB_DQS[7]
 SB_MA[0] U5
 SB_MA[1] V2
 SB_MA[2] T6
 SB_MA[3] V3
 SB_MA[4] B1
 SB_MA[5] TR
 SB_MA[6] R2
 SB_MA[7] R6
 SB_MA[8] R4
 SB_MA[9] R5
 SB_MA[10] AB5
 SB_MA[11] P3
 SB_MA[12] R3
 SB_MA[13] AF7
 SB_MA[14] P5
 SB_MA[15] N1
 DDR B CLK0 11
 DDR B_CLK0# 11
 DDR B_CLK1 11
 DDR B_CLK1# 11
 DDR B_CKE0 11
 DDR B_CKE1 11
 DDR B_CS0# 11
 DDR B_CS1# 11
 DDR B_ODT0 11
 DDR B_ODT1 11
 DDR B_DM0
 DDR B_DM1
 DDR B_DM2
 DDR B_DM3
 DDR B_DM4
 DDR B_DM5
 DDR B_DM6
 DDR B_DM7
 DDR B_DQS#0
 DDR B_DQS#1
 DDR B_DQS#2
 DDR B_DQS#3
 DDR B_DQS#4
 DDR B_DQS#5
 DDR B_DQS#6
 DDR B_DQS#7
 DDR B_DQS0
 DDR B_DQS1
 DDR B_DQS2
 DDR B_DQS3
 DDR B_DQS4
 DDR B_DQS5
 DDR B_DQS6
 DDR B_DQS7
 DDR B_MA0
 DDR B_MA1
 DDR B_MA2
 DDR B_MA3
 DDR B_MA4
 DDR B_MA5
 DDR B_MA6
 DDR B_MA7
 DDR B_MA8
 DDR B_MA9
 DDR B_MA10
 DDR B_MA11
 DDR B_MA12
 DDR B_MA13
 DDR B_MA14
 DDR B_MA15

IC_AUB_CFD_rPGA,R1P0
 CONN@

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Size	Document Number	Date		Rev	
B	NALG0 M/B LA-5681P Schematic	Friday, October 23, 2009		1.0	
Date				Sheet 6 of 60	

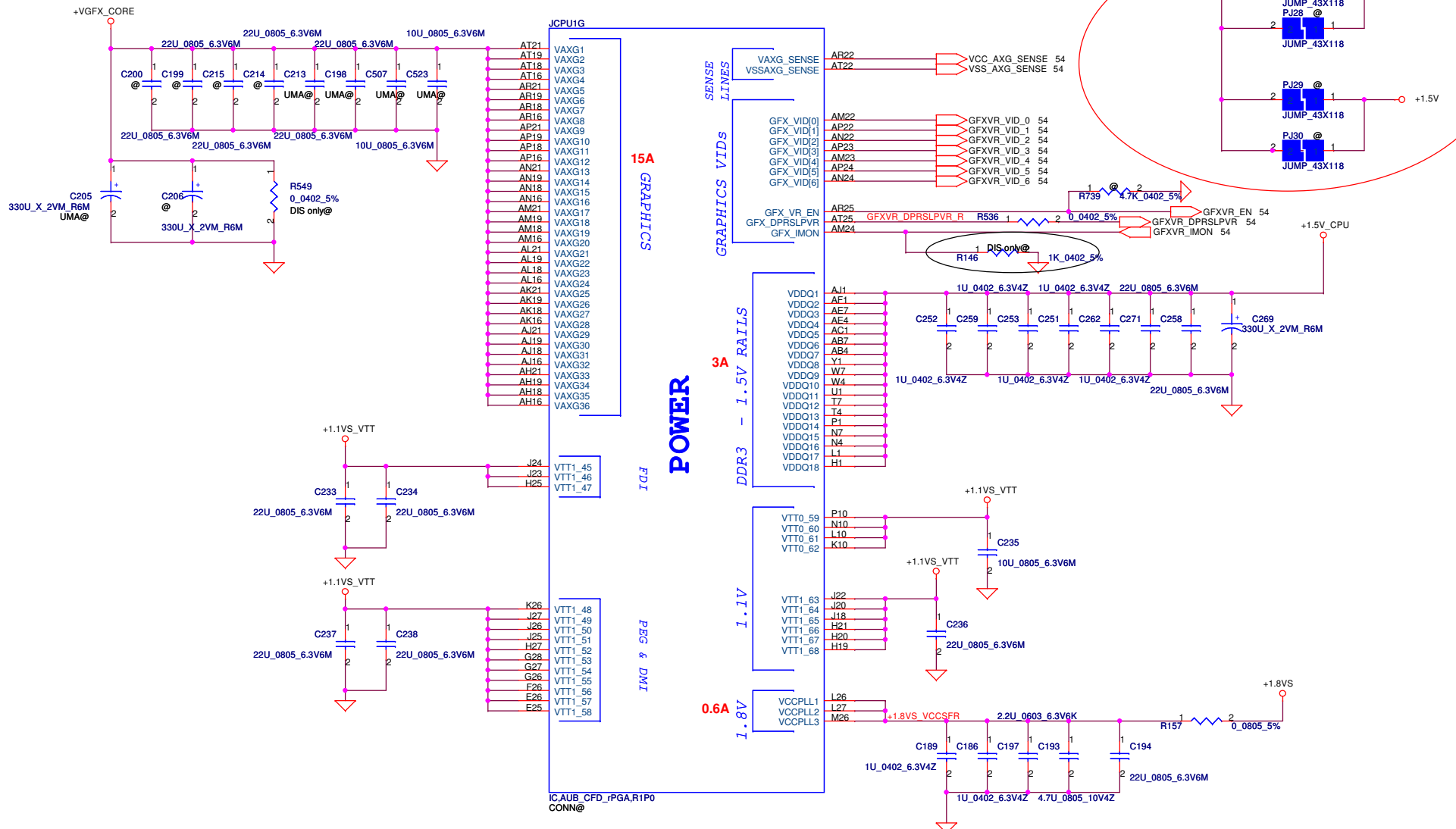


CSC (Current Sense Configuration) 8/25

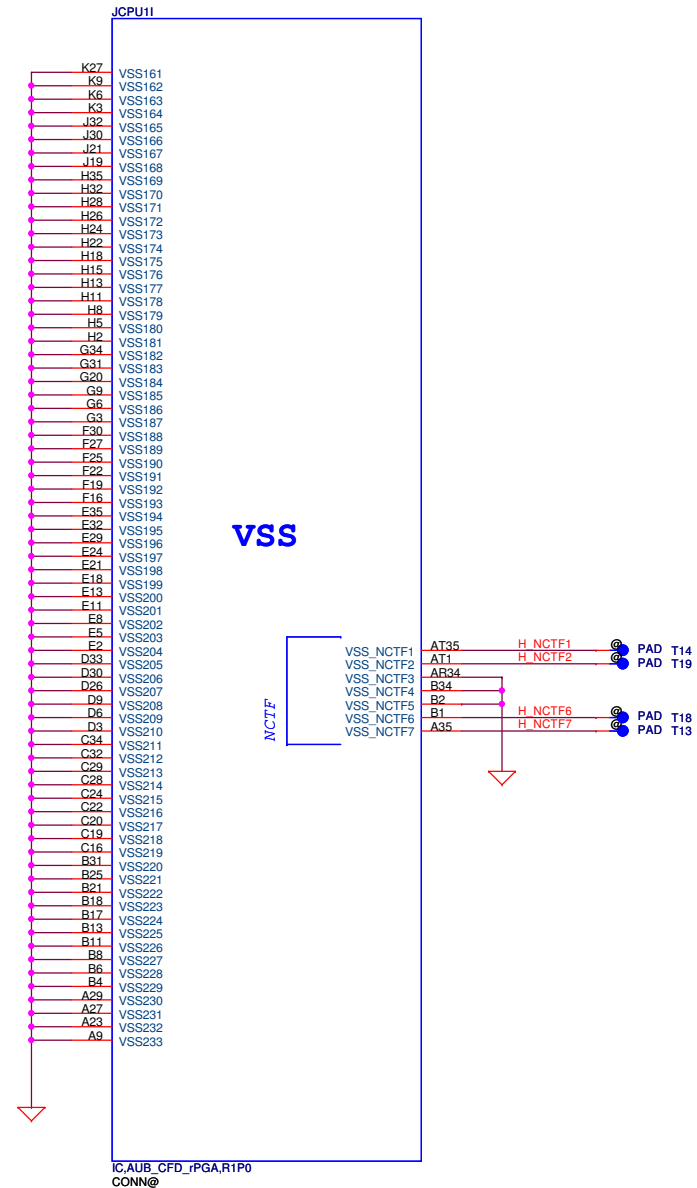
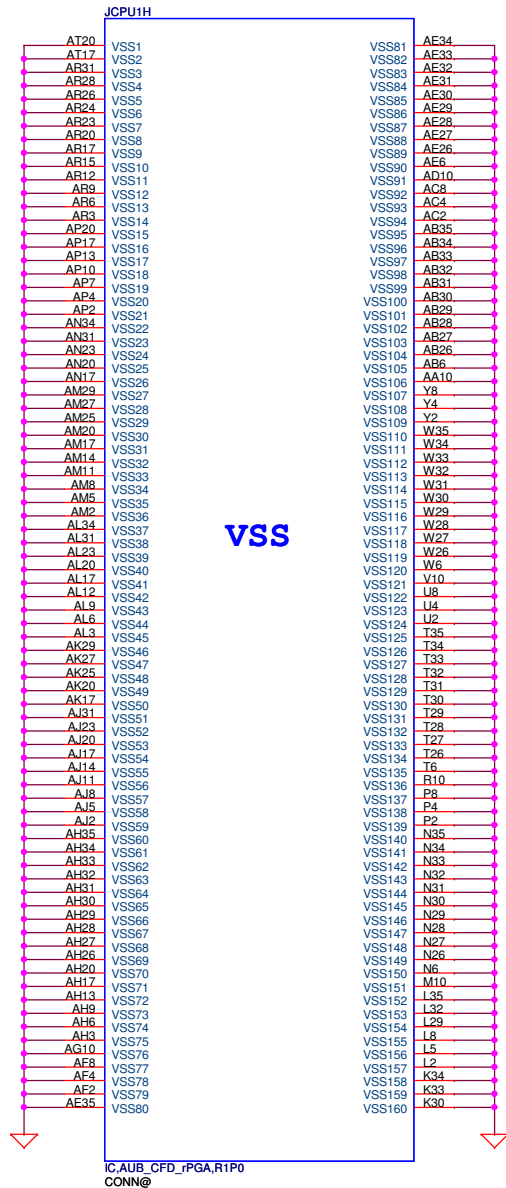
CPU VID0	R412	2	1K	0402	1%
CPU VID1	R415	2	1K	0402	1%
CPU VID2	R419	2	1K	0402	1%
CPU VID3	R422	2	1K	0402	1%
CPU VID4	R425	2	1K	0402	1%
CPU VID5	R428	2	1K	0402	1%
H DPRSLPVR	R435	2	1K	0402	1%
H PSI#	R437	2	1K	0402	1%

VTT Rail
 Auburndale +1.1VS_VTT=1.05V
 Clarksfield +1.1VS_VTT=1.1V

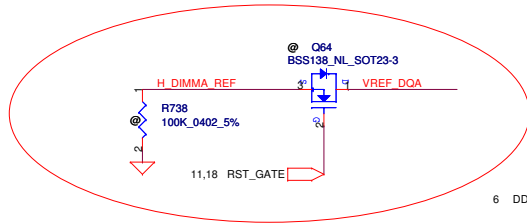
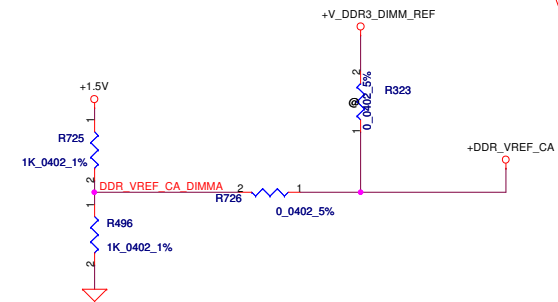
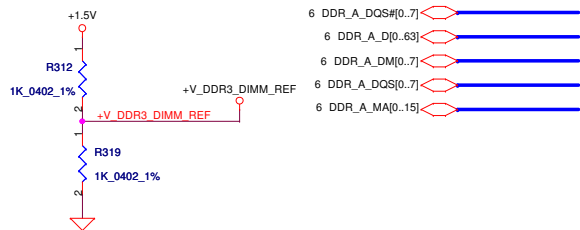
+CPU-CORE Decoupling	C, uF	ESR, mohm	Stuffing Option
SPCAP, Polymer	4X330uF	6m ohm/4	4X330uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	



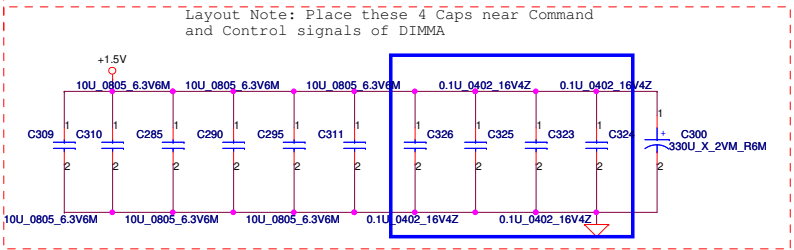
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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Size	Document Number	Customer		Rev	
	NALG0 M/B LA-5681P Schematic			1.0	
Date:	Friday, October 23, 2009	Sheet	8	of 60	



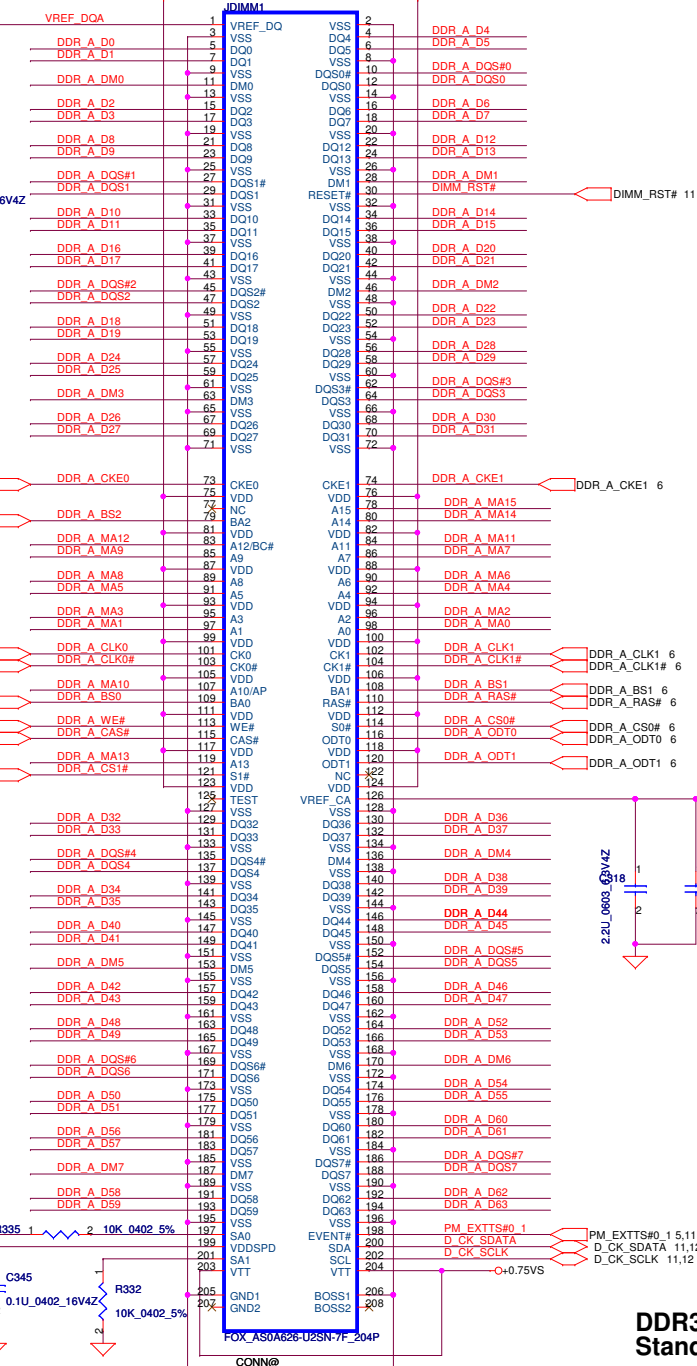
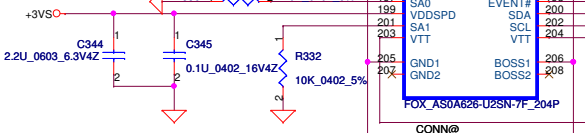
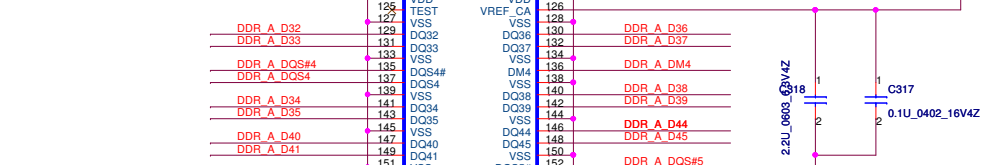
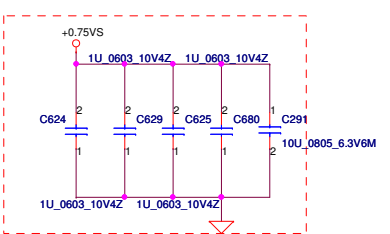
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title PROCESSOR (6/6) VSS	
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Date:	Friday, October 23, 2009	Sheet	9	of	60



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



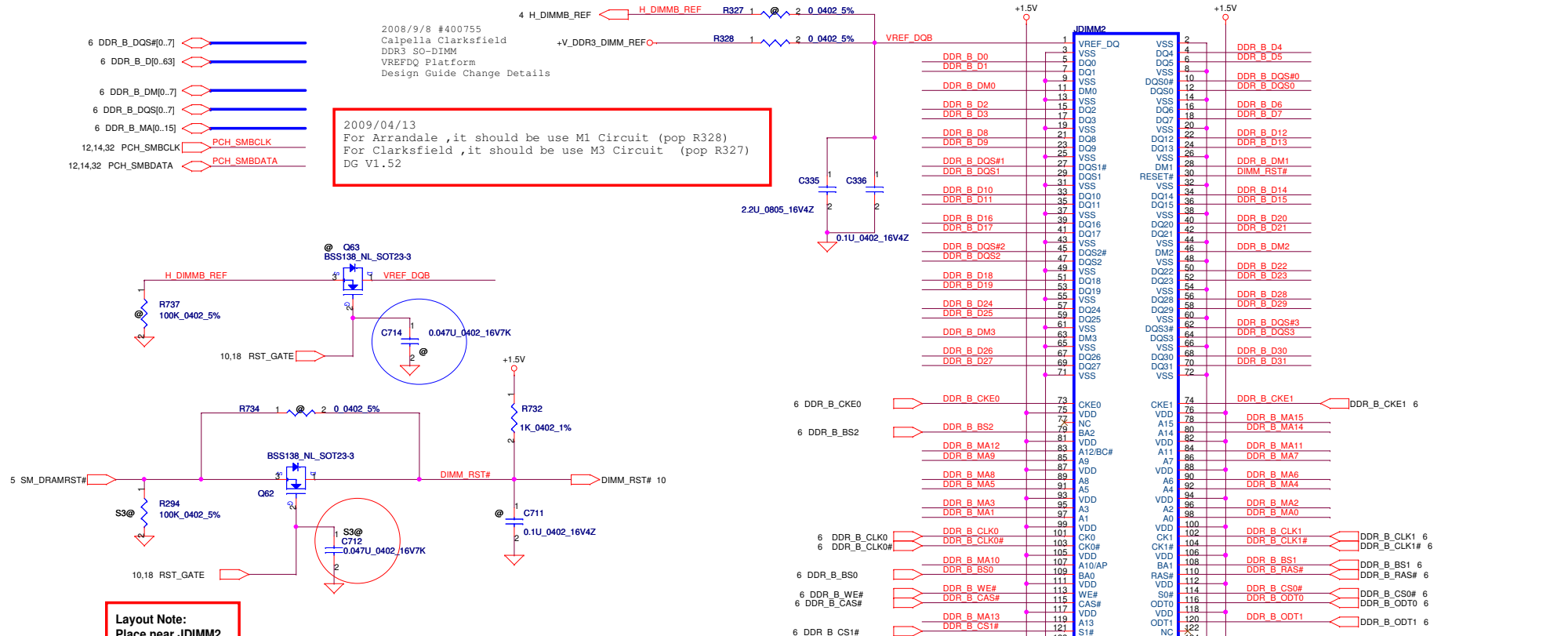
**DDR3 SO-DIMM A
Standard Type**

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				1006	NALGO M/B LA-5681P Schematic	1.0
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- 6 DDR_B_DQS#0..7
- 6 DDR_B_D0..63
- 6 DDR_B_DM0..7
- 6 DDR_B_DQS#0..7
- 6 DDR_B_MA0..15
- 12,14,32 PCH_SMBCLK
- 12,14,32 PCH_SMBDATA

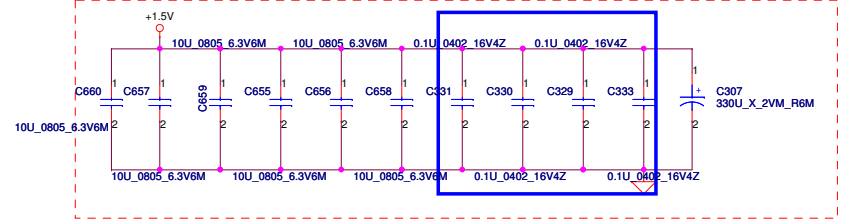
2008/9/8 #400755
Calpella Clarksville
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

2009/04/13
For Arrandale, it should be use M1 Circuit (pop R328)
For Clarksville, it should be use M3 Circuit (pop R327)
DG V1.52

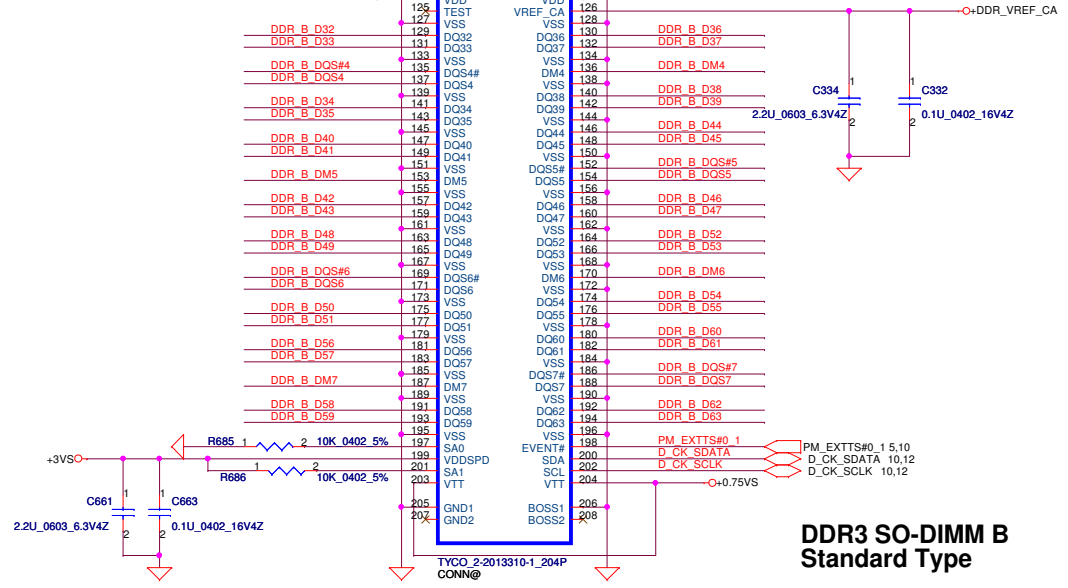
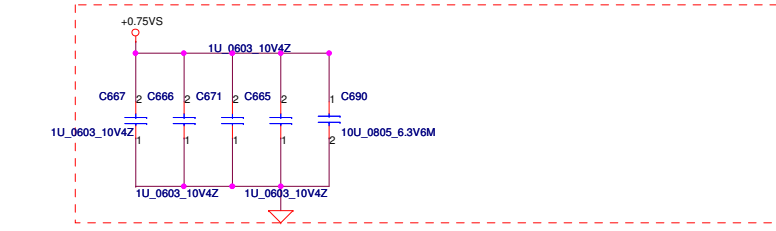


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMM2

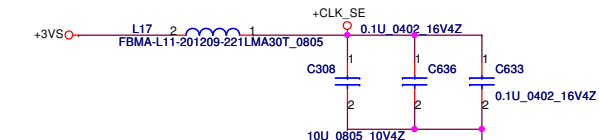
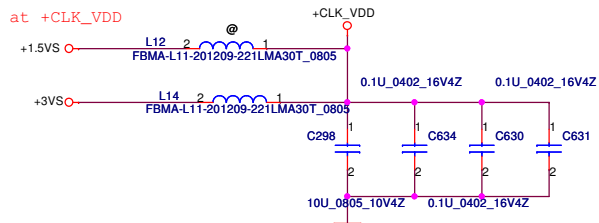
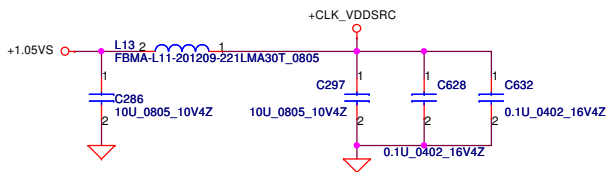


Layout Note:
Place near JDIMM2.203 & JDIMM2.204

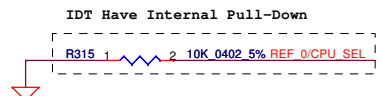
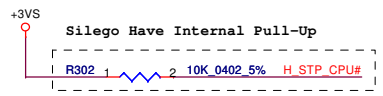
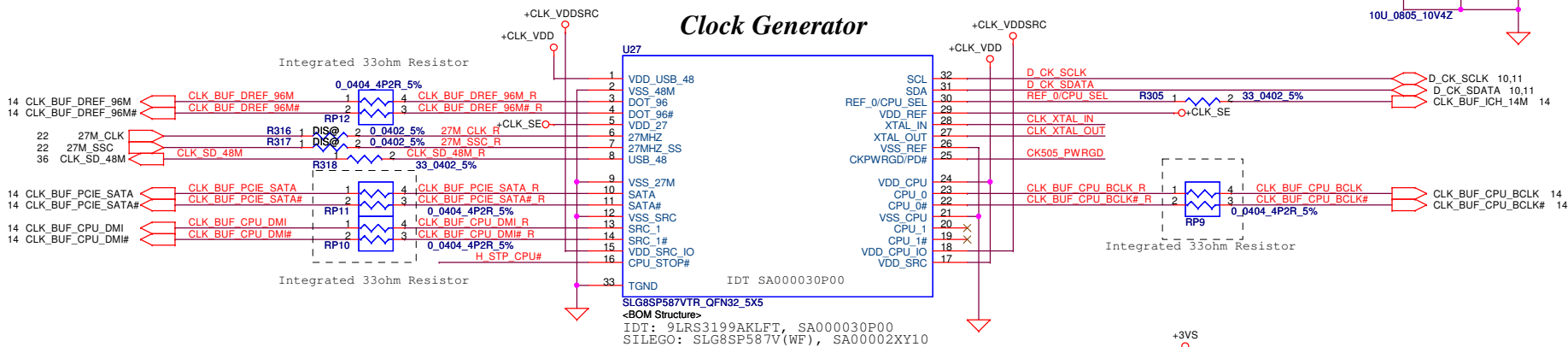


DDR3 SO-DIMM B Standard Type

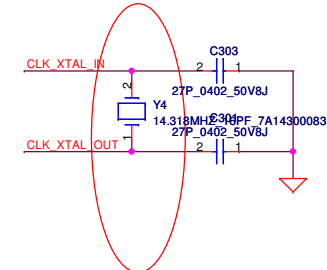
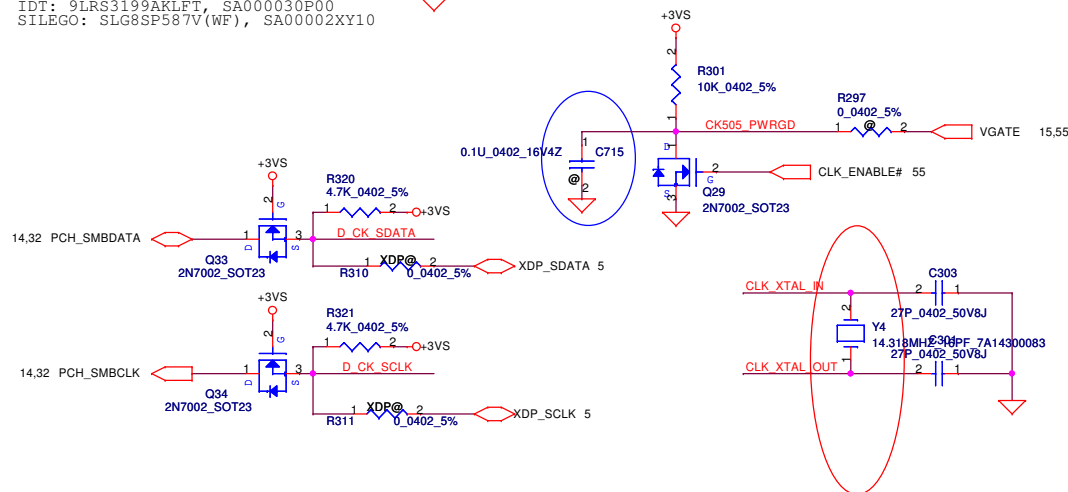
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Document Number				Rev 1.0	
NALGO M/B LA-5681P Schematic				Date: Friday, October 23, 2009	
				1 Sheet 11 of 60	

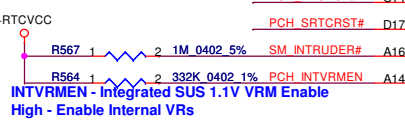
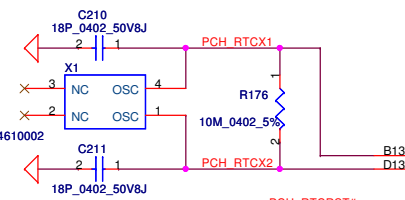
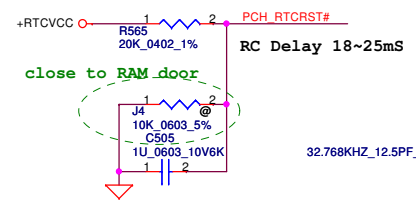


Clock Generator

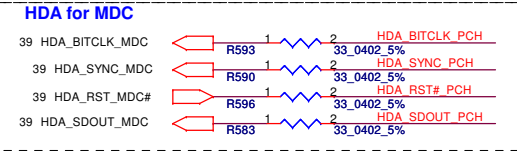
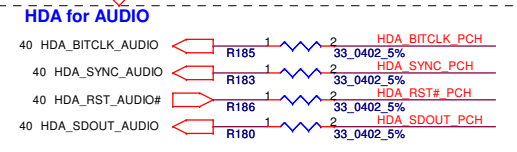


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

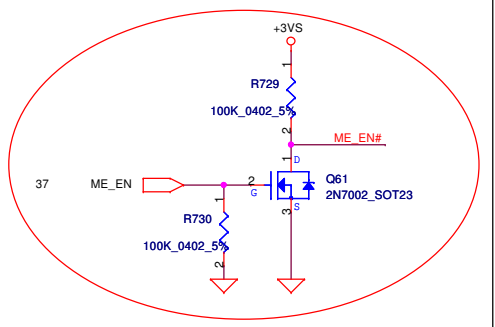
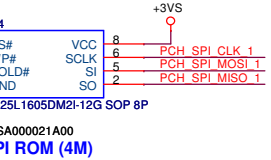
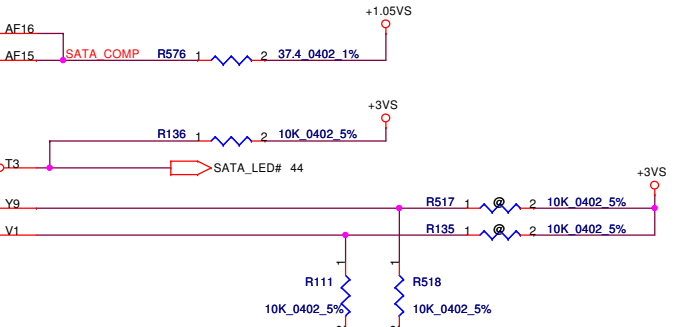
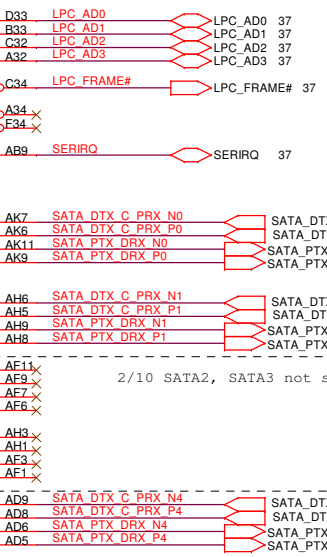
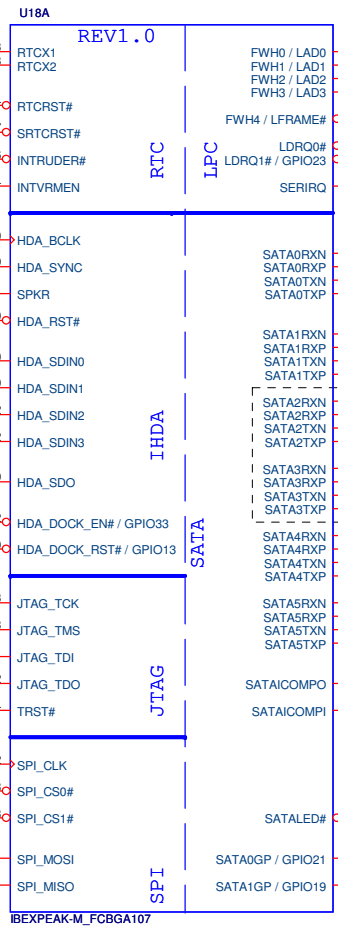
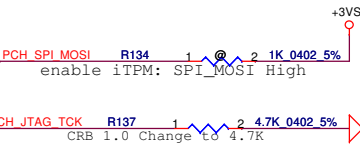
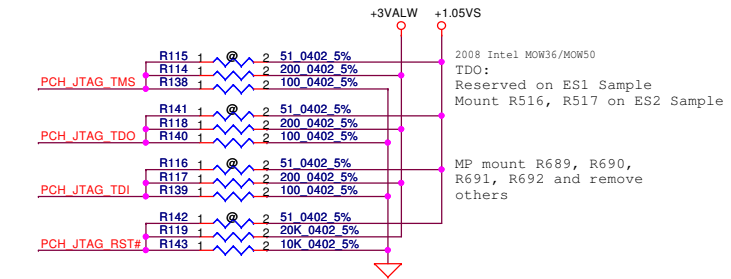
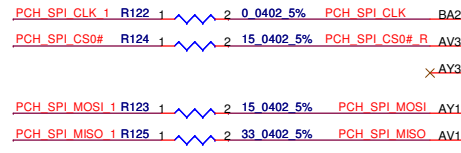
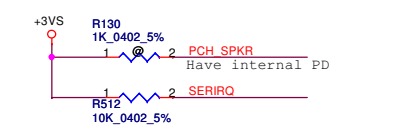




INTVRMEN - Integrated SUS 1.1V VRM Enable High - Enable Internal VRs



If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.



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Compal Electronics, Inc.			
Title: PCH (1/9) SATA,HDA,SPI, LPC			
Size	Document Number	Rev	
Customer	NALG0 M/B LA-5681P Schematic	1.0	
Date:	Friday, October 23, 2009	Sheet	13 of 60

For PCIE LAN

For Wireless LAN

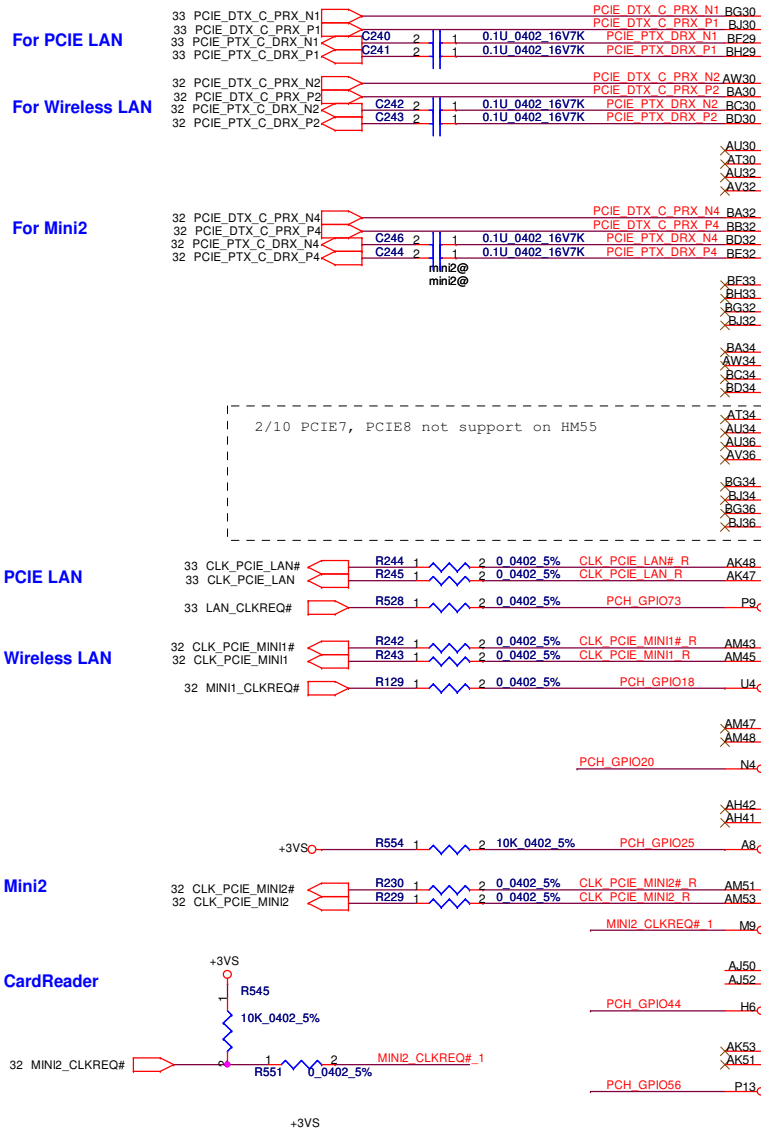
For Mini2

For PCIE LAN

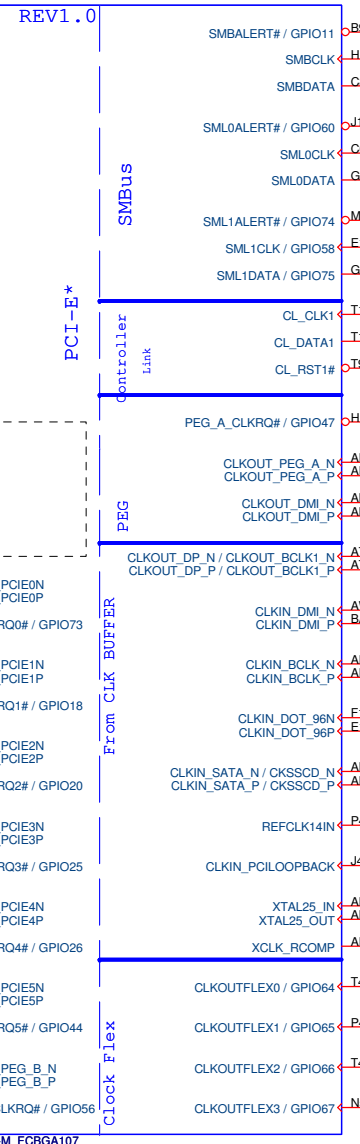
For Wireless LAN

For Mini2

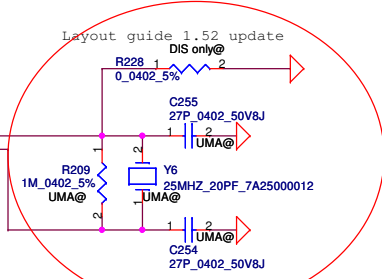
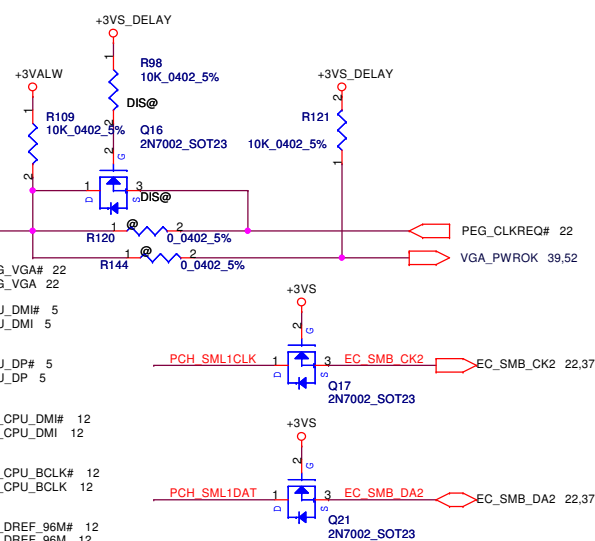
For CardReader



2/10 PCIE7, PCIE8 not support on HM55



1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP



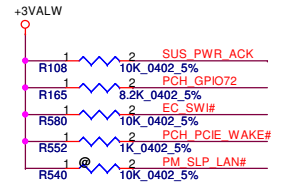
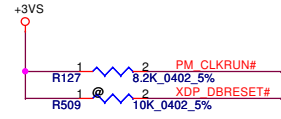
Project ID		
ID1	ID0	Project
1	0	JV 40
1	1	JM 40

EC LID_OUT#	R170	1	2	10K 0402 5%
PCH SMBCLK	R178	1	2	2.2K 0402 5%
PCH SMBDATA	R547	1	2	2.2K 0402 5%
PCH GPIO060	R572	1	2	10K 0402 5%
PCH SML1CLK	R546	1	2	2.2K 0402 5%
PCH SML1DAT	R148	1	2	2.2K 0402 5%
PCH GPIO74	R573	1	2	10K 0402 5%
PCH GPIO18	R727	1	2	10K 0402 5%
PCH GPIO44	R534	1	2	10K 0402 5%
PCH GPIO56	R574	1	2	10K 0402 5%
PCH GPIO73	R538	1	2	10K 0402 5%

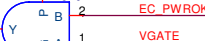
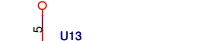
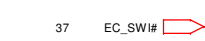
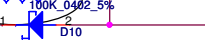
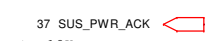
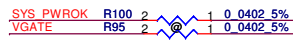
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Size	Document Number	Customer		Rev	
Date:	Friday, October 23, 2009	Sheet		14 of 60	

4 DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
 4 DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
 4 DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
 4 DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] H_FDI_TXN[0..7]
 4 H_FDI_TXP[0..7] H_FDI_TXP[0..7]

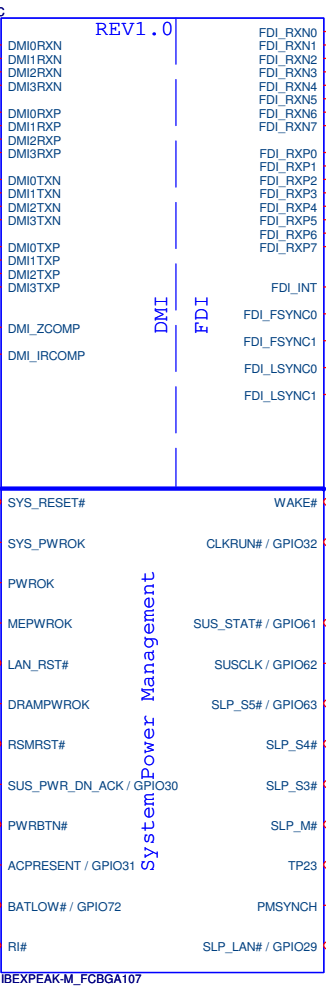


+1.05VS

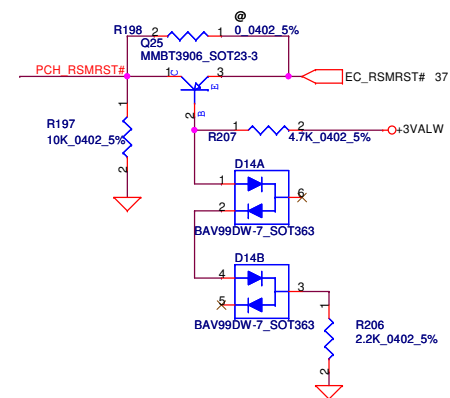


**No used Integrated LAN,
connecting LAN_RST# to GND**

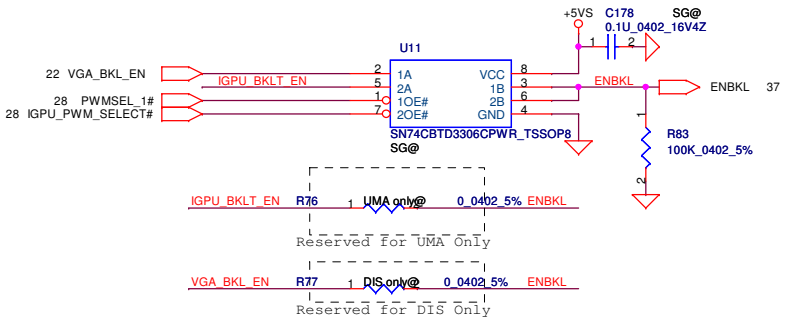
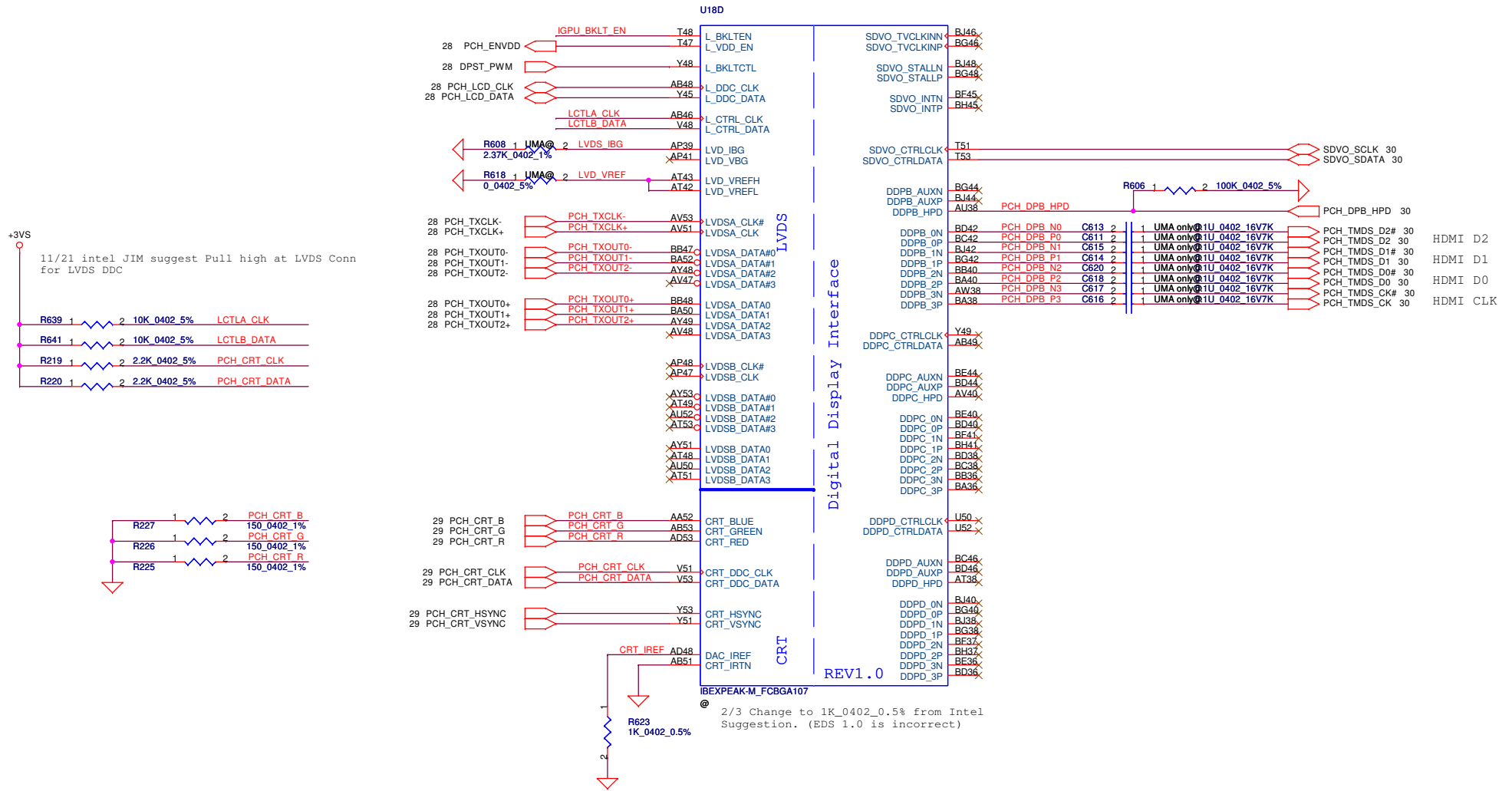
U18C
 REV1.0
 DMI
 FDI



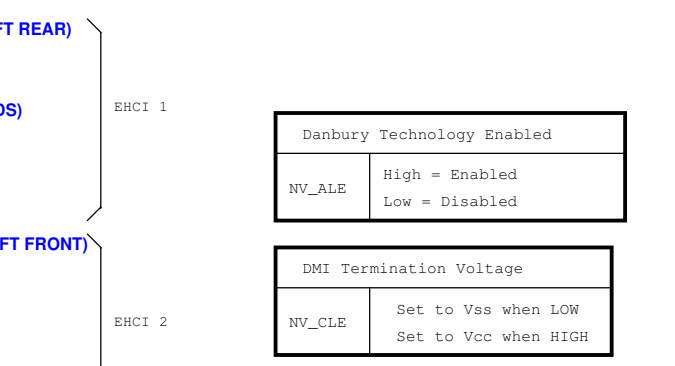
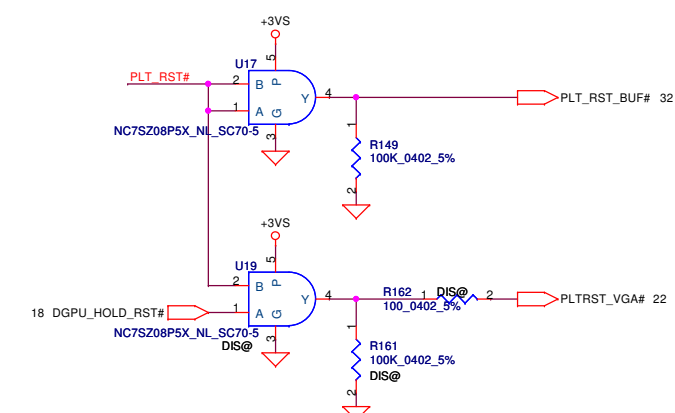
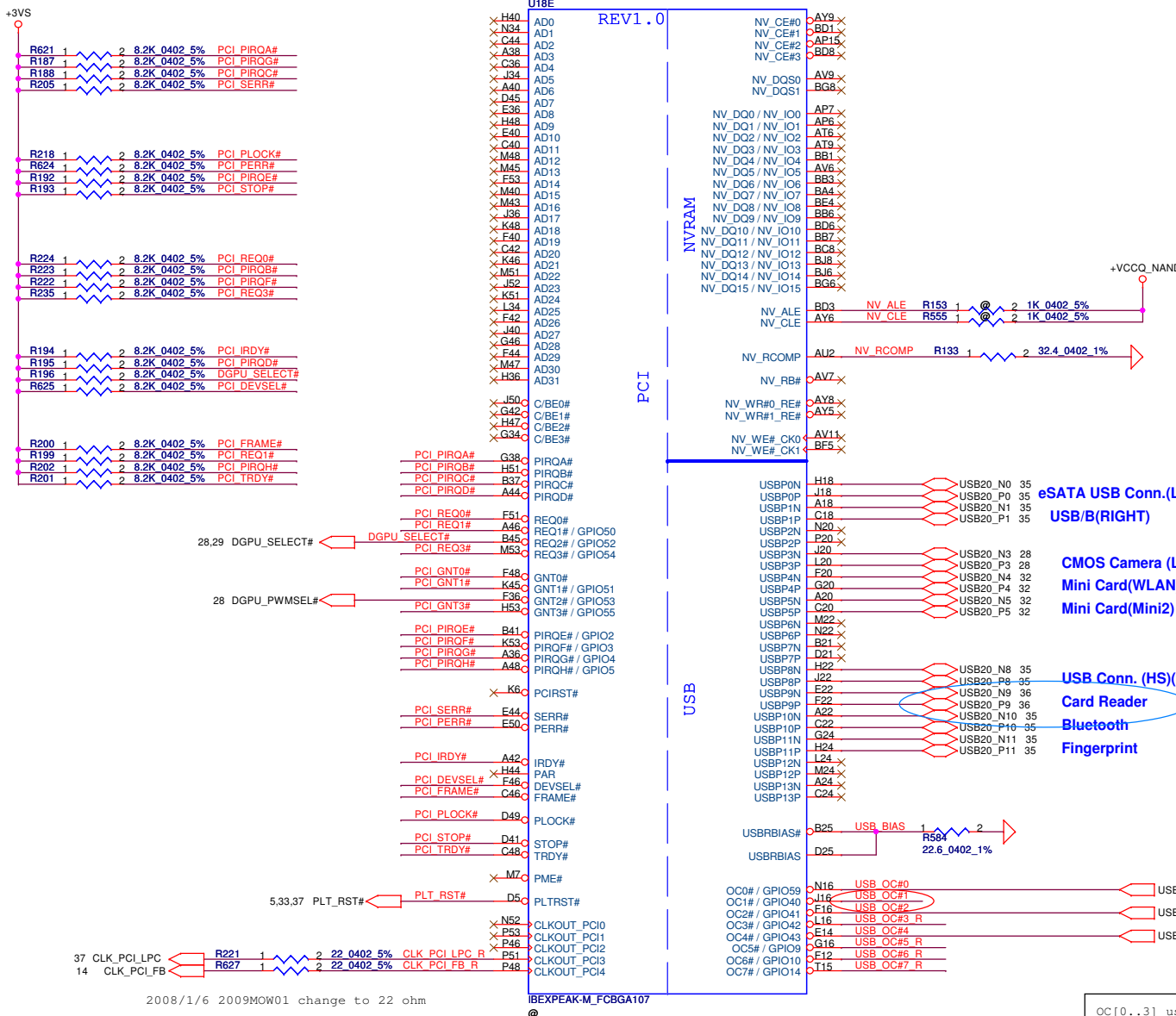
BA18 H_FDI_TXN0
 BH17 H_FDI_TXN1
 BD16 H_FDI_TXN2
 FDI_RXN1 H_FDI_TXN3
 BJ16 H_FDI_TXN4
 FDI_RXN2 H_FDI_TXN5
 BA16 H_FDI_TXN6
 BE14 H_FDI_TXN7
 BA14 H_FDI_TXN8
 BC12 H_FDI_TXN9
 BB18 H_FDI_TXP0
 BE17 H_FDI_TXP1
 BC16 H_FDI_TXP2
 BG16 H_FDI_TXP3
 AW16 H_FDI_TXP4
 BD14 H_FDI_TXP5
 BB14 H_FDI_TXP6
 BD12 H_FDI_TXP7
 BU14 H_FDI_INT 4
 BE13 H_FDI_FSYNC0 4
 BH13 H_FDI_FSYNC1 4
 BU12 H_FDI_LSYNC0 4
 BG14 H_FDI_LSYNC1 4
 J12 PCH_PCIE_WAKE# PCH_PCIE_WAKE# 32,33
 Y1 PM_CLKRUN# PM_CLKRUN# 37
 P8 PCH_GPIO61 @ PAD T17
 F3 PCH_GPIO62 @ PAD T15
 E4 PM_SLP_S5# 37
 H7 PM_SLP_S4# 37
 F12 PM_SLP_S3# 37
 K8 PM_SLP_M# @ PAD T16
 N2 PM_SLP_DSW# @ PAD T4
 B110 H_PM_SYNC 5
 F6 PM_SLP_LAN#



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Size	Document Number	Customer		Rev	
Date:	Friday, October 23, 2009	Sheet		15 of 60	
				NALG0 M/B LA-5681P Schematic 1.0	

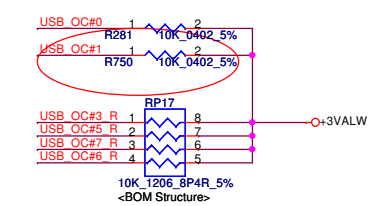


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Size	Document Number	Date		Rev	
Customer	NALGO M/B LA-5681P Schematic	Friday, October 23, 2009		1.0	
Date				Sheet 16 of 60	



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

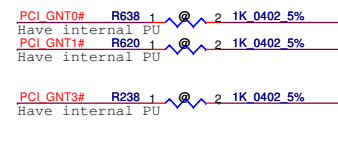


OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

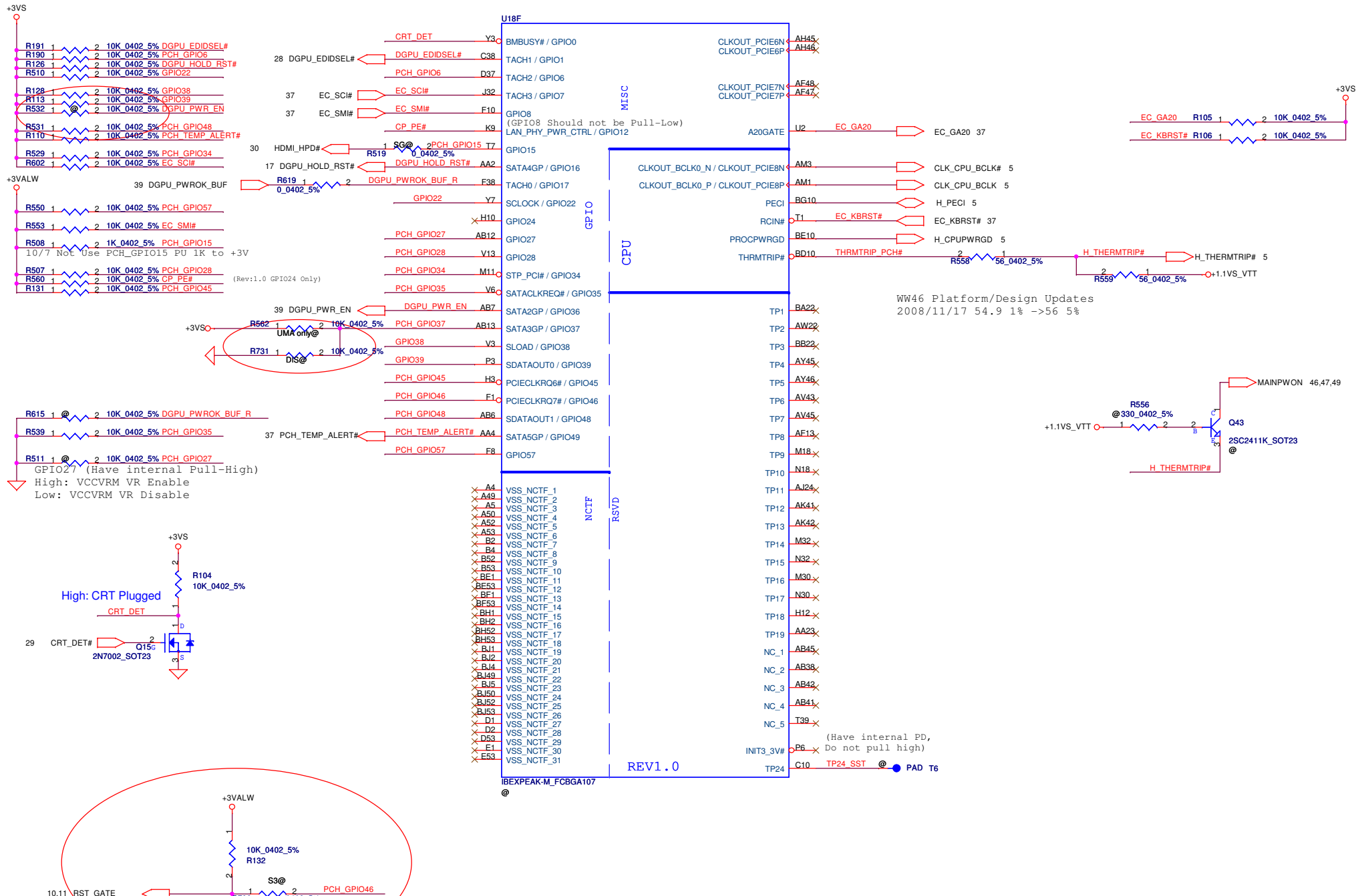
2008/1/6 2009MOW01 change to 22 ohm

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



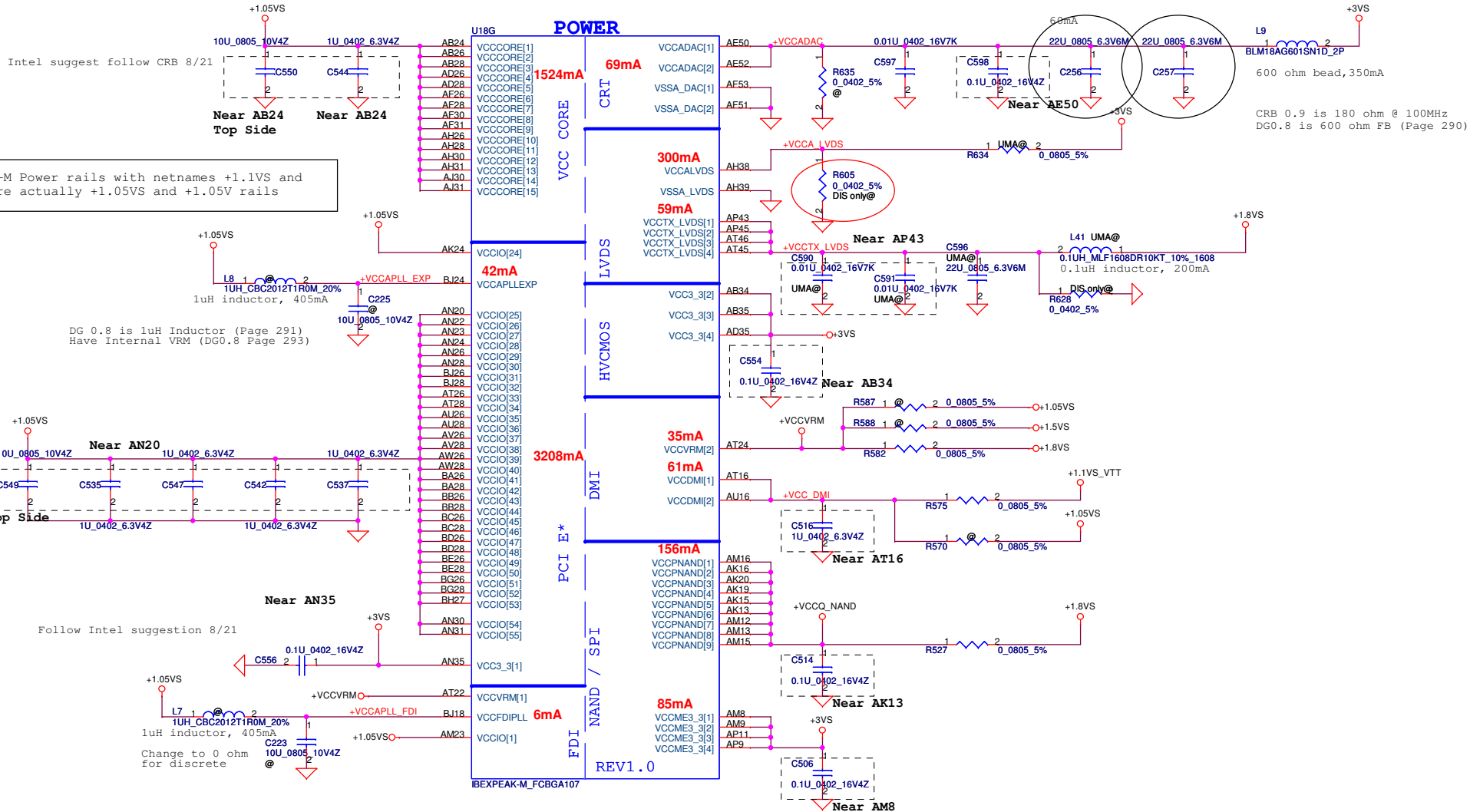
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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				NALG0 M/B LA-5681P Schematic	
				1.0	



WW46 Platform/Design Updates
2008/11/17 54.9 1% ->56 5%

REV1.0

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				Customer	1.0
				Date:	Friday, October 23, 2009
				Sheet	18 of 60



All Ibox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

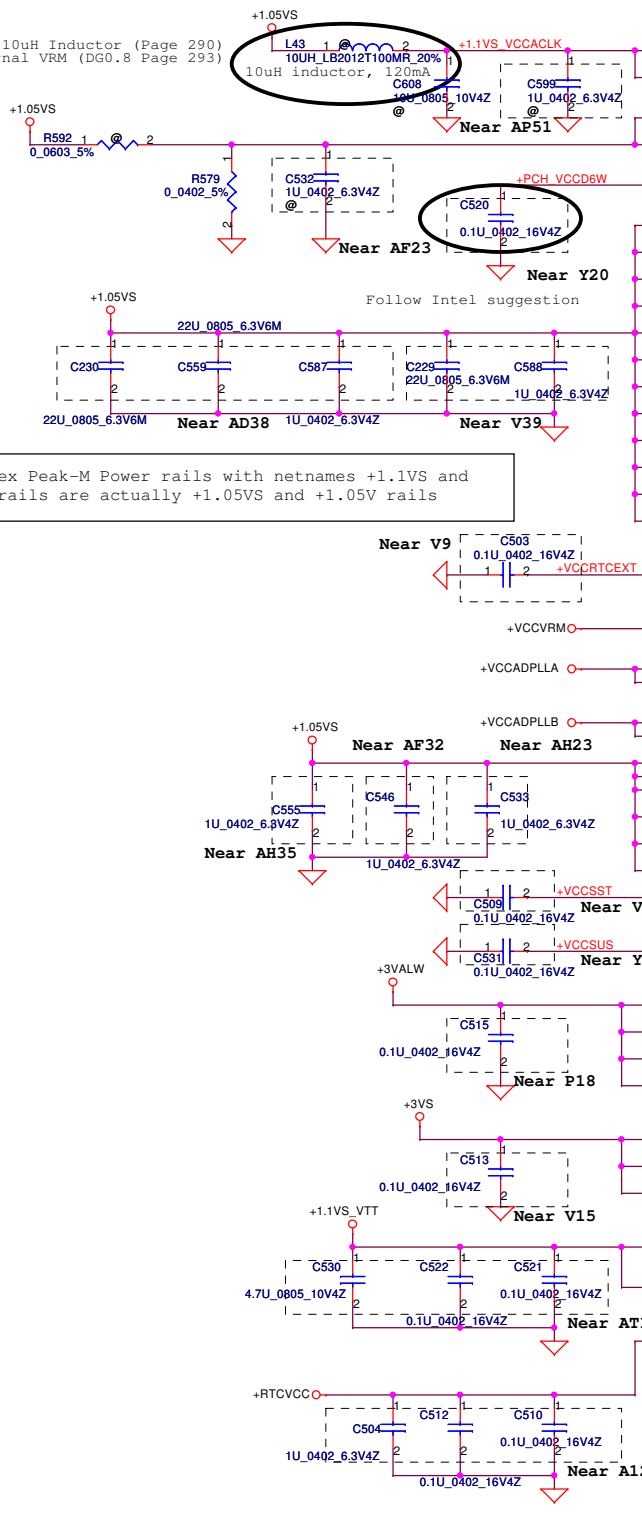
DG 0.8 is 1uH Inductor (Page 291)
Have Internal VRM (DG0.8 Page 293)

Follow Intel suggestion 8/21

DG 0.8 is 1uH Inductor (Page 291)
Have Internal VRM (DG0.8 Page 293)

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Size	Document Number	Customer		Rev	
	NALG0 M/B LA-5681P Schematic	Date:		1.0	
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DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)



All Ixbox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

POWER

- 52mA VCCACLK[1]
- 344mA VCCACLK[2]
- 1998mA DCPSUSBYP
- 163mA V5REF_SUS
- >1mA V5REF
- 357mA VCC3_3[8]
- 73mA VCCADPLL
- 32mA VCCSATAPLL
- >1mA V_CPU_I0[1]
- 2mA VCCRTC
- 6mA VCCSUSHDA

USB

Clock and Miscellaneous

PCI/GPIO/LPC

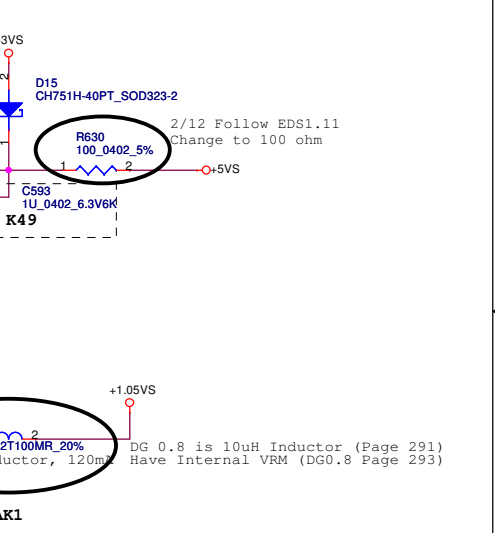
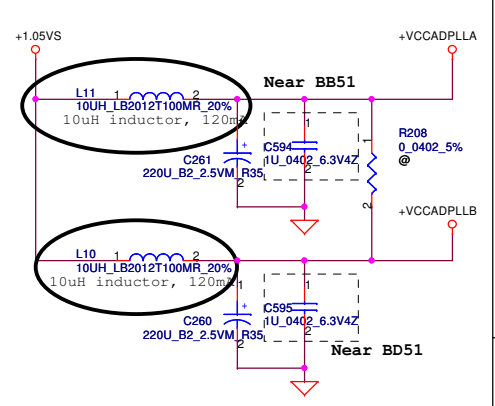
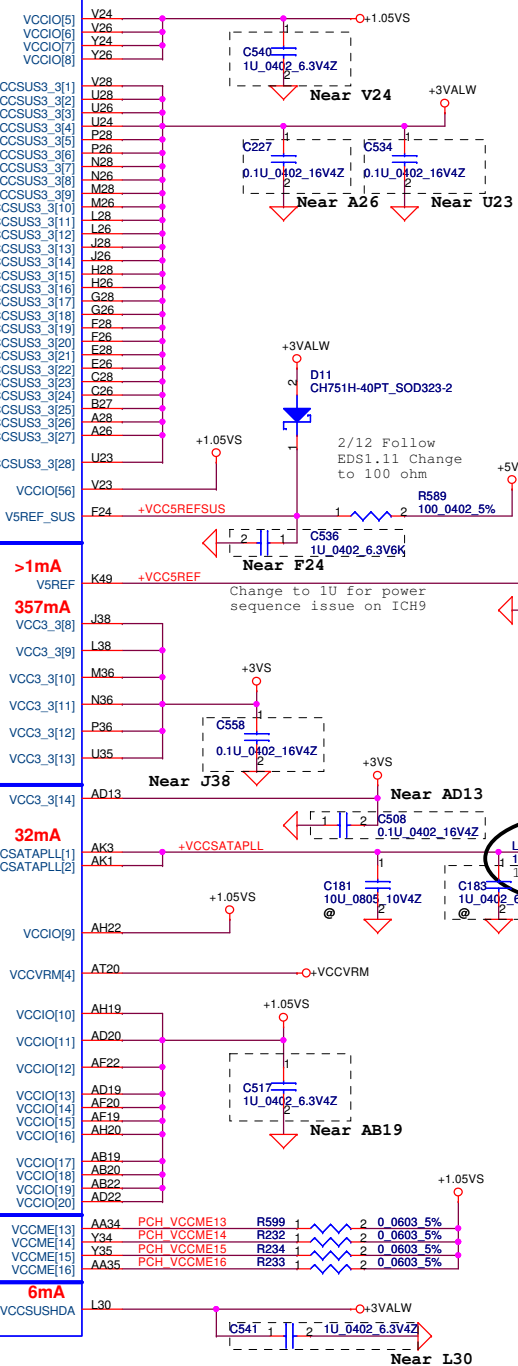
SATA

PCI/GPIO/LPC

CPU

IRIC

HDA



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				Customer	NALGO M/B LA-5681P Schematic	1.0
Date:	Friday, October 23, 2009	Sheet	20	of 60		

U18I		H49	
AY7	VSS[159]	VSS[259]	H5
B11	VSS[160]	VSS[260]	H24
B15	VSS[161]	VSS[261]	K11
B19	VSS[162]	VSS[262]	K43
B23	VSS[163]	VSS[263]	K47
B31	VSS[164]	VSS[264]	K24
B35	VSS[165]	VSS[265]	L14
B39	VSS[165]	VSS[265]	L18
B43	VSS[166]	VSS[266]	L2
B47	VSS[167]	VSS[267]	L22
B5	VSS[168]	VSS[268]	L32
B7	VSS[169]	VSS[269]	L36
BG12	VSS[170]	VSS[270]	L40
BB12	VSS[171]	VSS[271]	L52
BB16	VSS[172]	VSS[272]	M12
BB20	VSS[173]	VSS[273]	M16
BB24	VSS[174]	VSS[274]	M20
BB30	VSS[175]	VSS[275]	M38
BB34	VSS[176]	VSS[276]	M42
BB38	VSS[177]	VSS[277]	M46
BB42	VSS[178]	VSS[278]	M49
BB49	VSS[178]	VSS[278]	M5
BB5	VSS[179]	VSS[279]	M8
BC10	VSS[180]	VSS[280]	N24
BC14	VSS[181]	VSS[281]	P11
BC18	VSS[182]	VSS[282]	P22
BC2	VSS[183]	VSS[283]	P30
BC22	VSS[184]	VSS[284]	P32
BC32	VSS[185]	VSS[285]	P34
BC36	VSS[186]	VSS[286]	P42
BC40	VSS[187]	VSS[287]	P45
BC44	VSS[188]	VSS[288]	P47
BC52	VSS[189]	VSS[289]	R2
BH9	VSS[190]	VSS[290]	R52
BD48	VSS[191]	VSS[291]	T12
BD49	VSS[192]	VSS[292]	AE2
BD5	VSS[193]	VSS[293]	AE4
BE12	VSS[194]	VSS[294]	AE12
BE16	VSS[195]	VSS[295]	I46
BE20	VSS[196]	VSS[296]	I49
BE24	VSS[197]	VSS[297]	T5
BE30	VSS[198]	VSS[298]	T8
BE34	VSS[199]	VSS[299]	U30
BE38	VSS[200]	VSS[300]	U31
BE42	VSS[201]	VSS[301]	U32
BE46	VSS[202]	VSS[302]	U34
BE48	VSS[203]	VSS[303]	AF45
BE50	VSS[204]	VSS[304]	AF46
BE6	VSS[205]	VSS[305]	V11
BE8	VSS[206]	VSS[306]	P16
BF3	VSS[207]	VSS[307]	AF8
BF49	VSS[208]	VSS[308]	V19
BF51	VSS[209]	VSS[309]	AG2
BG18	VSS[210]	VSS[310]	AG52
BG24	VSS[211]	VSS[311]	V30
BG4	VSS[212]	VSS[312]	AH15
BG50	VSS[213]	VSS[313]	V32
BH11	VSS[214]	VSS[314]	V34
BH15	VSS[215]	VSS[315]	AH32
BH19	VSS[216]	VSS[316]	V38
BH23	VSS[217]	VSS[317]	AH43
BH31	VSS[218]	VSS[318]	AH47
BH35	VSS[219]	VSS[319]	AH7
BH39	VSS[220]	VSS[320]	AJ19
BH43	VSS[221]	VSS[321]	AJ2
BH47	VSS[222]	VSS[322]	V5
BH7	VSS[223]	VSS[323]	AJ22
C12	VSS[224]	VSS[324]	V7
C50	VSS[225]	VSS[325]	V8
D51	VSS[226]	VSS[326]	W2
E12	VSS[227]	VSS[327]	W52
E16	VSS[228]	VSS[328]	Y11
E20	VSS[229]	VSS[329]	AJ34
E24	VSS[230]	VSS[330]	Y12
E30	VSS[231]	VSS[331]	Y15
E34	VSS[232]	VSS[332]	A4
E38	VSS[233]	VSS[333]	Y19
E42	VSS[234]	VSS[334]	Y23
E46	VSS[235]	VSS[335]	Y28
E48	VSS[236]	VSS[336]	Y30
E6	VSS[237]	VSS[337]	AK26
E8	VSS[238]	VSS[338]	Y32
F49	VSS[239]	VSS[339]	AK22
F5	VSS[240]	VSS[340]	AK23
G10	VSS[241]	VSS[341]	AK28
G14	VSS[242]	VSS[342]	Y43
G18	VSS[243]	VSS[343]	Y46
G2	VSS[244]	VSS[344]	P49
G22	VSS[245]	VSS[345]	Y5
G32	VSS[246]	VSS[346]	Y6
G36	VSS[247]	VSS[347]	Y8
G40	VSS[248]	VSS[348]	P24
G44	VSS[249]	VSS[349]	T43
G52	VSS[250]	VSS[350]	AD51
H16	VSS[251]	VSS[351]	AT8
H20	VSS[252]	VSS[352]	AD47
H30	VSS[253]	VSS[353]	Y47
H34	VSS[254]	VSS[354]	AT12
H38	VSS[255]	VSS[355]	AM6
H42	VSS[256]	VSS[356]	AT13
	VSS[257]	VSS[356]	AM5
	VSS[258]	VSS[366]	AK45
			AK39
			AV14

U18H		AB16		AK30	
VSS[0]		VSS[0]		VSS[1]	AK31
				VSS[2]	AK32
				VSS[3]	AK34
				VSS[4]	AK35
				VSS[5]	AK38
				VSS[6]	AK43
				VSS[7]	AK46
				VSS[8]	AK49
				VSS[9]	AK5
				VSS[10]	AK8
				VSS[11]	AL2
				VSS[12]	AL52
				VSS[13]	AM11
				VSS[14]	BB44
				VSS[15]	AD24
				VSS[16]	AM20
				VSS[17]	AM22
				VSS[18]	AM24
				VSS[19]	AM26
				VSS[20]	AM28
				VSS[21]	BA42
				VSS[22]	AM30
				VSS[23]	AM31
				VSS[24]	AM32
				VSS[25]	AM34
				VSS[26]	AM35
				VSS[27]	AM38
				VSS[28]	AM39
				VSS[29]	AM42
				VSS[30]	AM44
				VSS[31]	AM46
				VSS[32]	AV22
				VSS[33]	AM7
				VSS[34]	AA50
				VSS[35]	BB10
				VSS[36]	AN32
				VSS[37]	AN50
				VSS[38]	AN52
				VSS[39]	AP12
				VSS[40]	AP42
				VSS[41]	AP46
				VSS[42]	AP49
				VSS[43]	AP5
				VSS[44]	AP8
				VSS[45]	AR2
				VSS[46]	AR52
				VSS[47]	AT11
				VSS[48]	BA12
				VSS[49]	AH48
				VSS[50]	AT32
				VSS[51]	AT36
				VSS[52]	AT41
				VSS[53]	AT47
				VSS[54]	AT7
				VSS[55]	AV12
				VSS[56]	AV16
				VSS[57]	AV20
				VSS[58]	AV24
				VSS[59]	AV30
				VSS[60]	AV34
				VSS[61]	AV38
				VSS[62]	AV42
				VSS[63]	AV46
				VSS[64]	AV49
				VSS[65]	AV5
				VSS[66]	AV8
				VSS[67]	AW14
				VSS[68]	AW18
				VSS[69]	AW2
				VSS[70]	BF9
				VSS[71]	AW32
				VSS[72]	AW36
				VSS[73]	AW40
				VSS[74]	AW52
				VSS[75]	AY11
				VSS[76]	AY43
				VSS[77]	AY47
				VSS[78]	
				VSS[79]	
				VSS[158]	

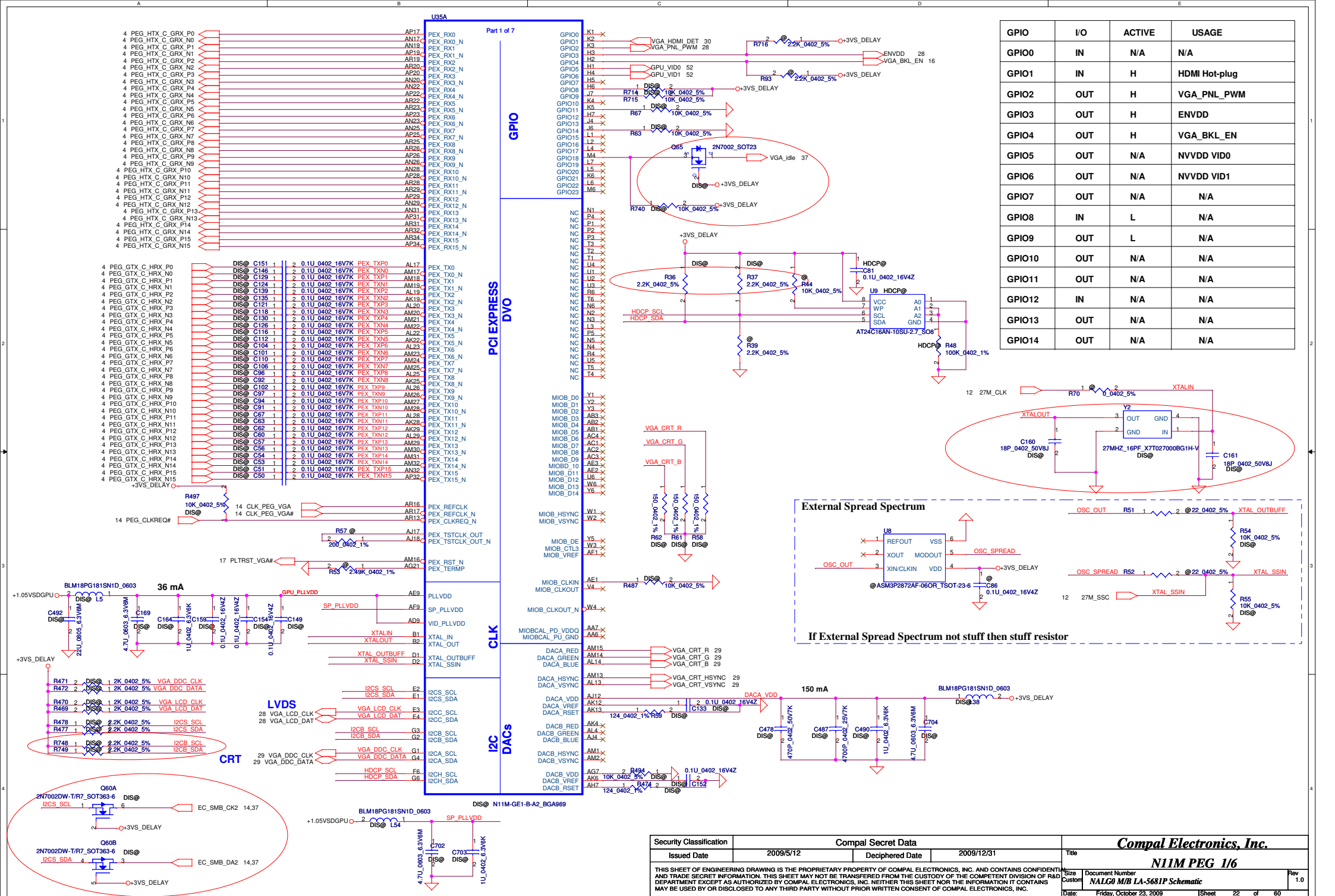
REV1.0

@EXPEAK-M_FCBGA107

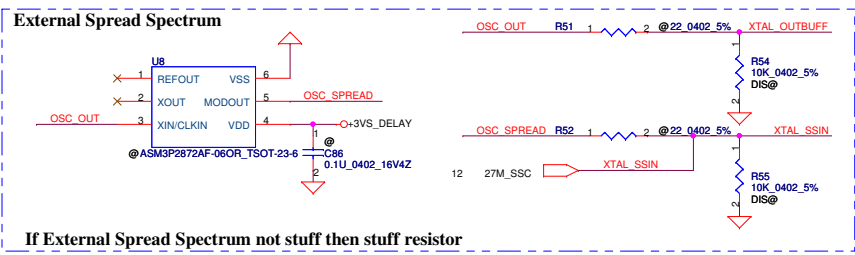
REV1.0

@EXPEAK-M_FCBGA107

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Size	Document Number	Customer		Rev	
	NALG0 M/B LA-5681P Schematic			1.0	
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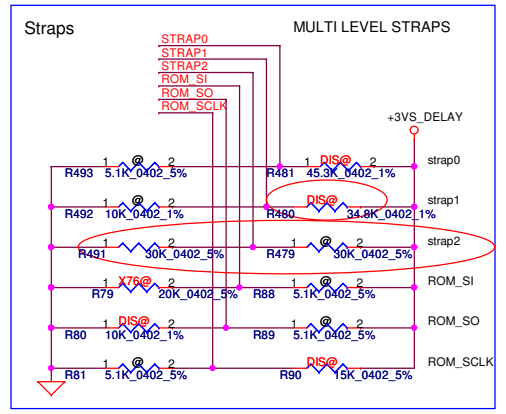
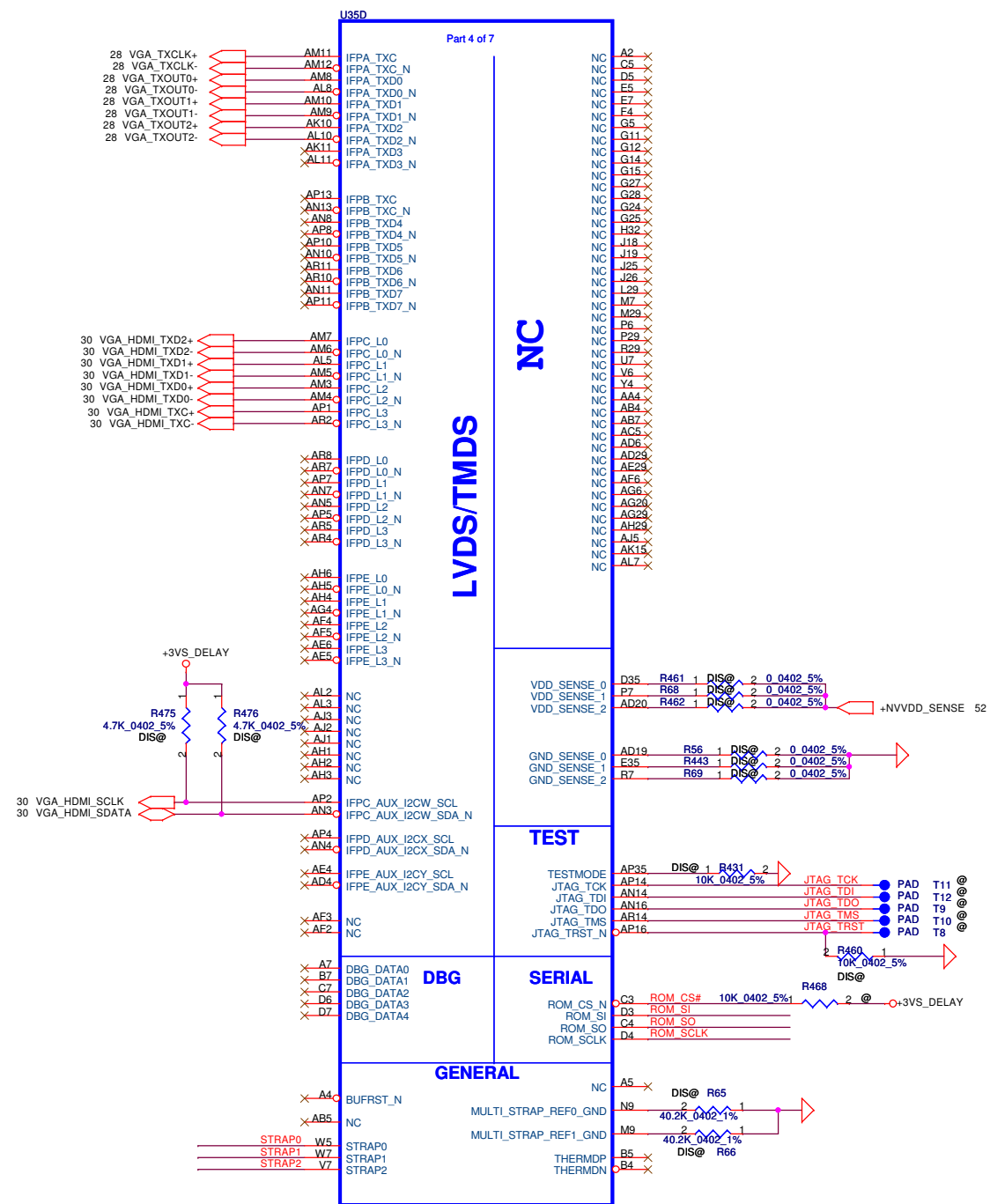
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A



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		2009/12/31

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N11M PEG 1/6	
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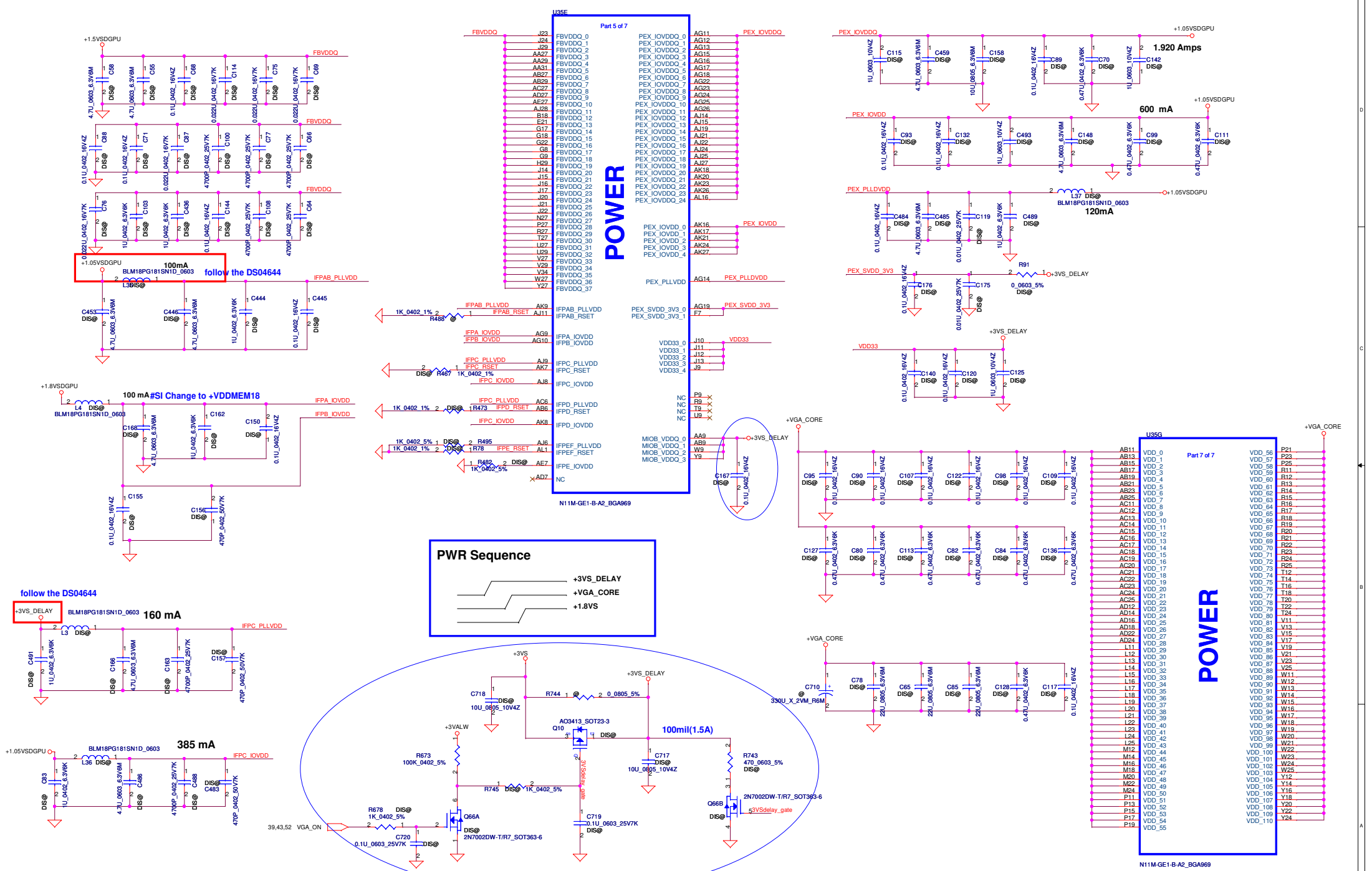


ES: pop R479 30K ohm
 GS: pop R491 30K ohm
 MP ID check R491 and R479

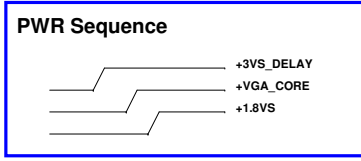
	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	H 35K	L 30K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	H 35K	L 30K	L 15K	L 10K	H 15K

N11M-GE1-B-A2_BGA969

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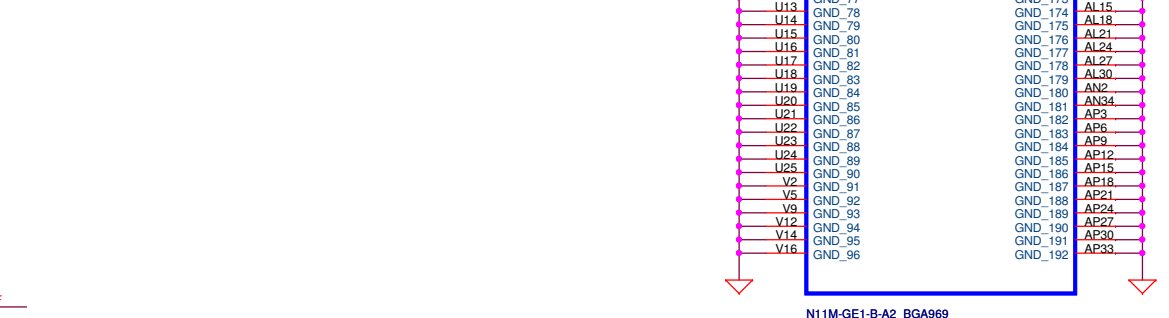
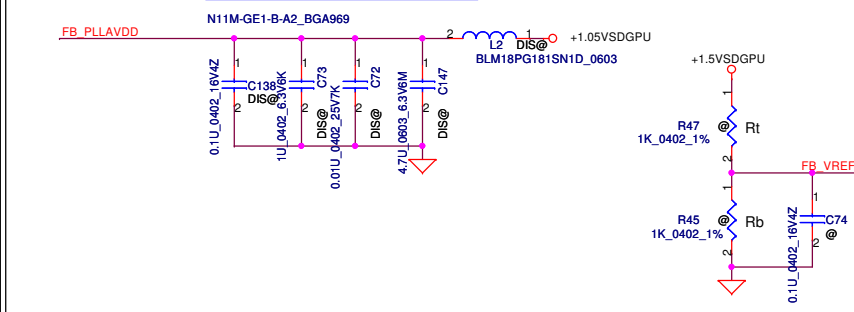
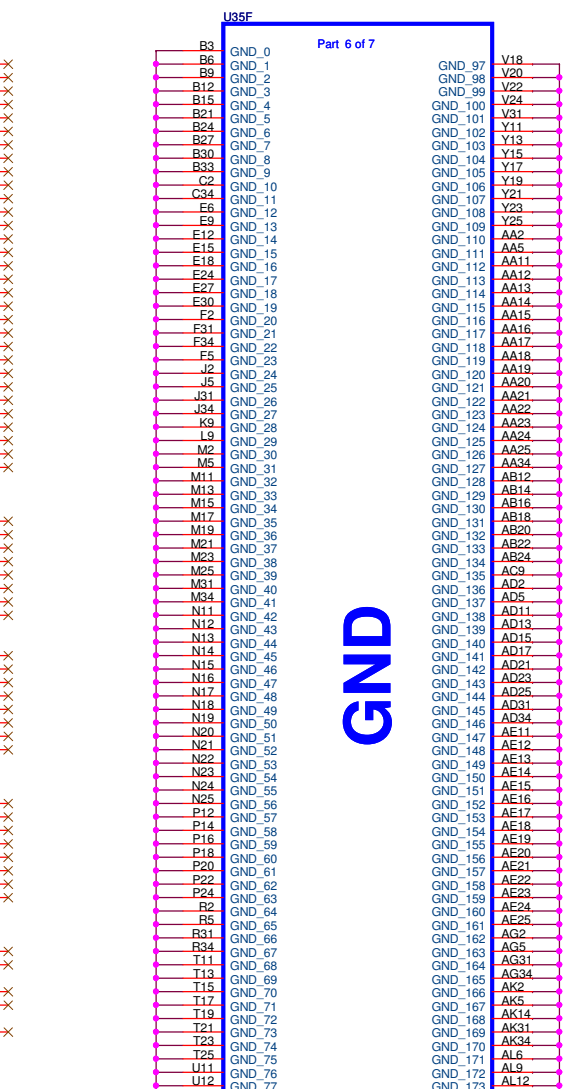
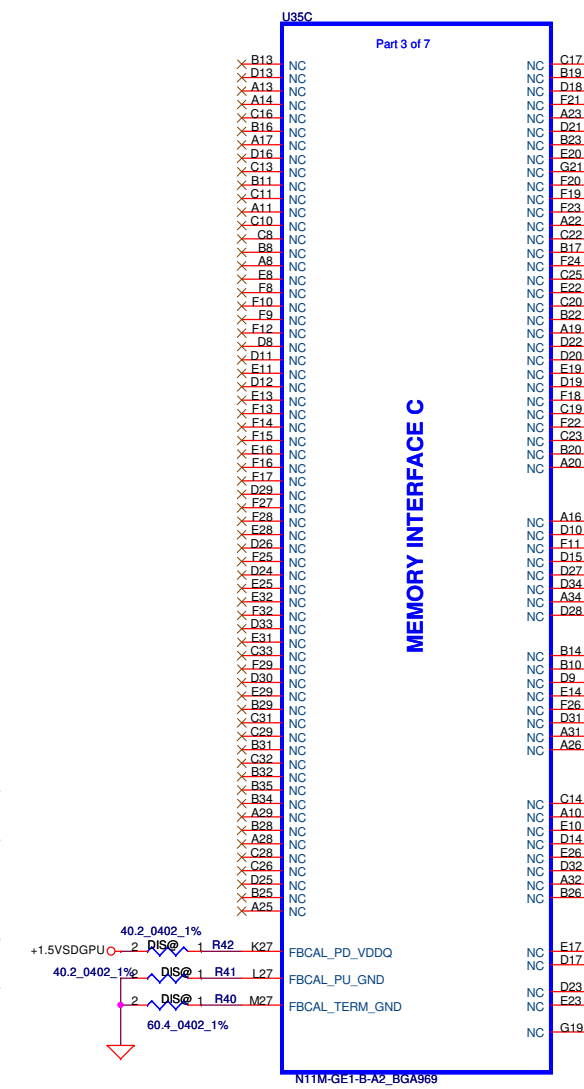
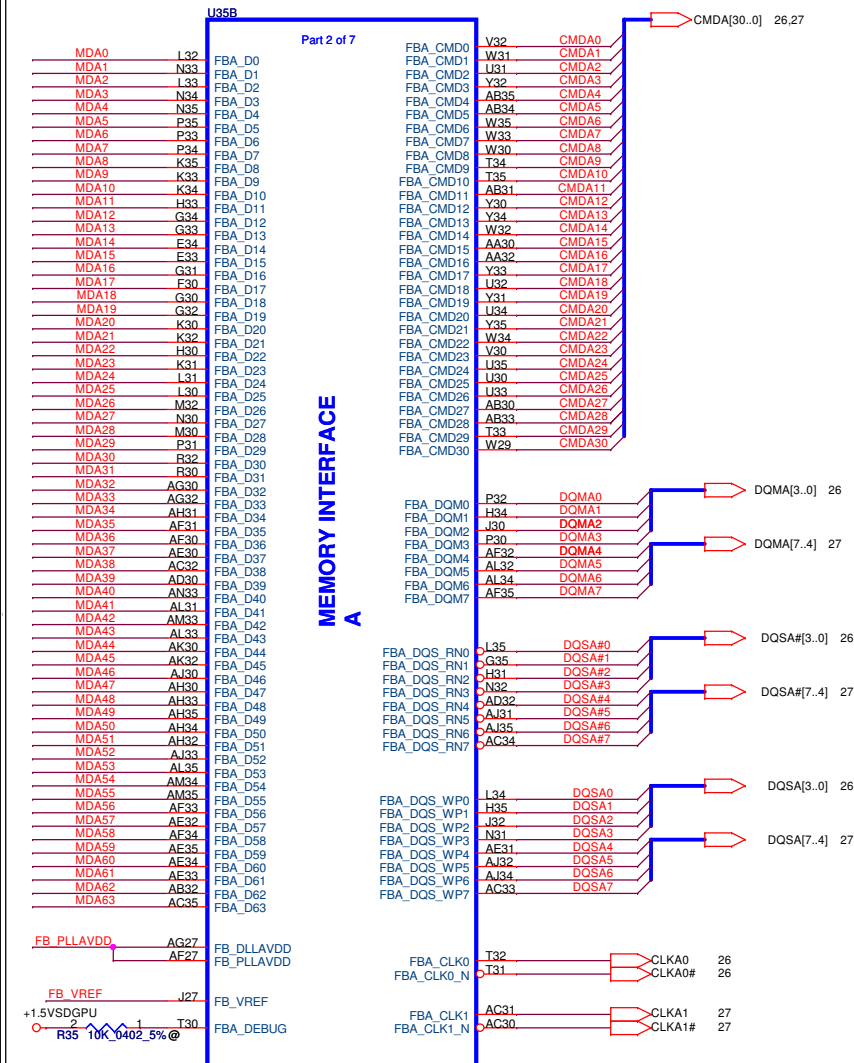
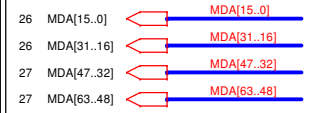


POWER



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Issued Date	2009/5/12	Deciphered Date	2009/12/31	Size	Document Number
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VRAM Interface

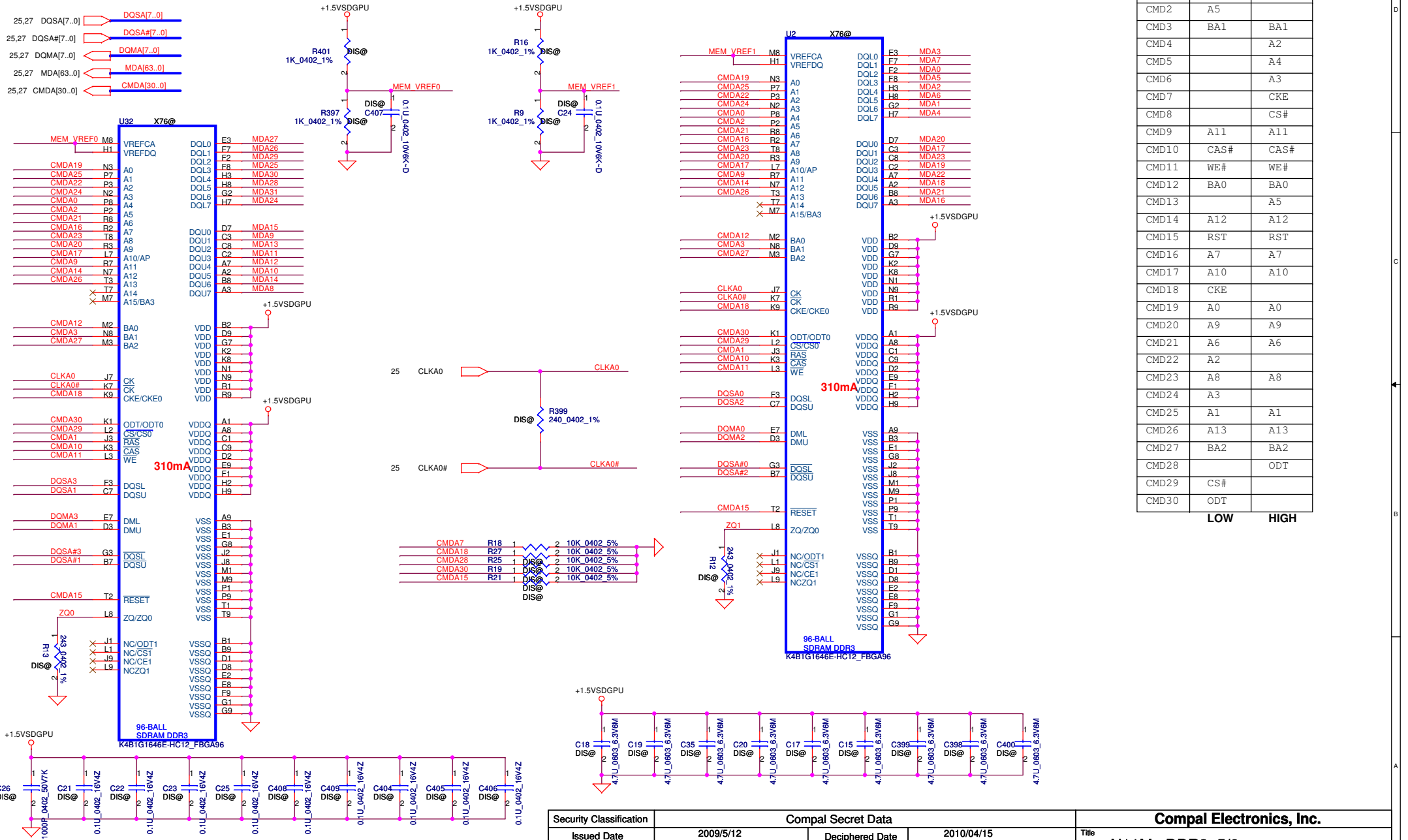


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Issued Date	2009/5/12	Deciphered Date	2009/12/31
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Compal Electronics, Inc.			
Title N11M VRAM 4/6			
Size	Document Number	Rev	
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VRAM gDDR3 chips (256MB & 512MB)

32Mx16 gDDR2 *4==>256MB

64Mx16 gDDR3 *4==>512MB



Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	

LOW HIGH

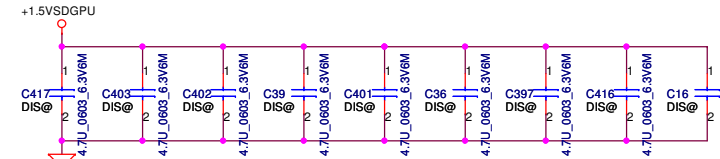
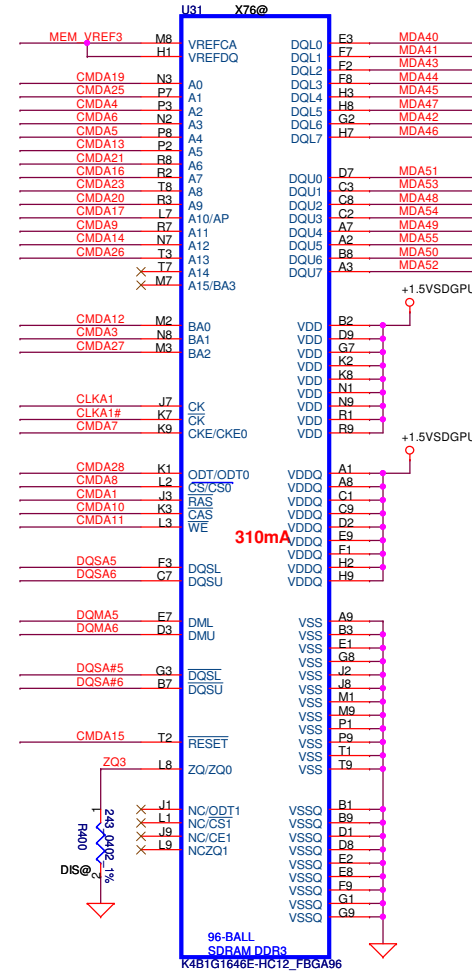
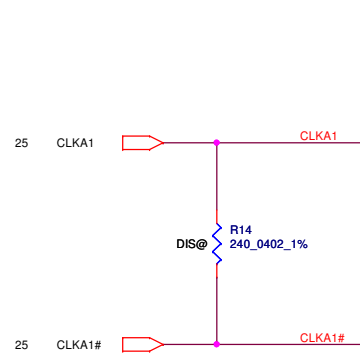
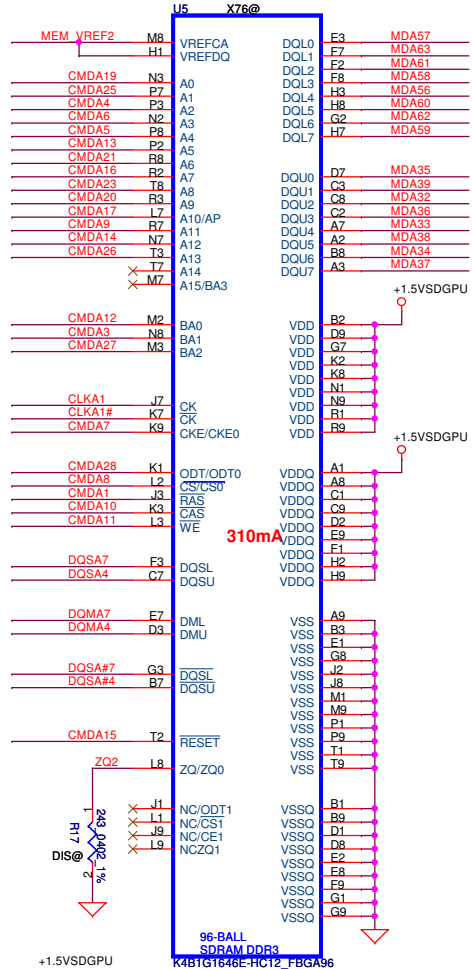
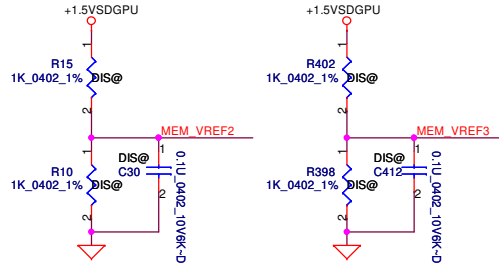
Security Classification		Compal Secret Data		Title	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	N11M gDDR3 5/6	
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VRAM DDR3 chips (256MB & 512MB)

32Mx16 DDR3 *4==>256MB

64Mx16 DDR3 *4==>512MB

- 25,26 DQMA[7..0] <-> DQMA[7..0]
- 25,26 CMDA[30..0] <-> CMDA[30..0]
- 25,26 DQSA# [7..0] <-> DQSA# [7..0]
- 25,26 DQSA [7..0] <-> DQSA [7..0]
- 25,26 MDA[63..0] <-> MDA[63..0]

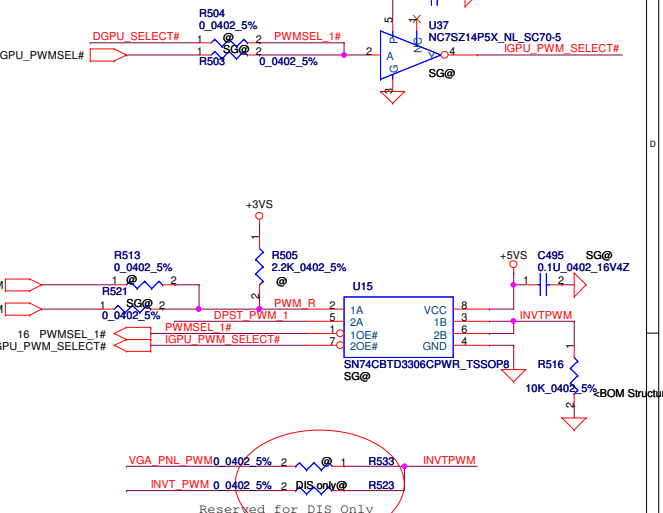
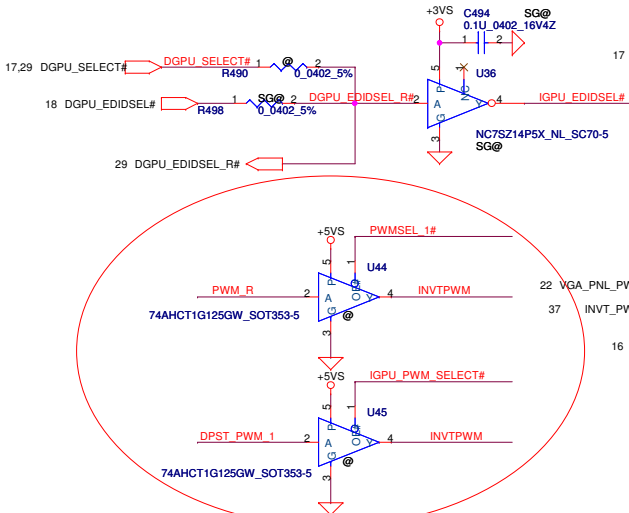
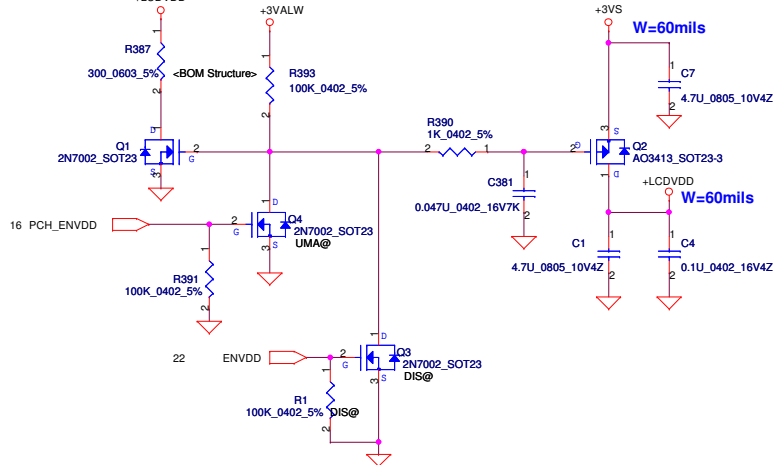


Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	A1
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	

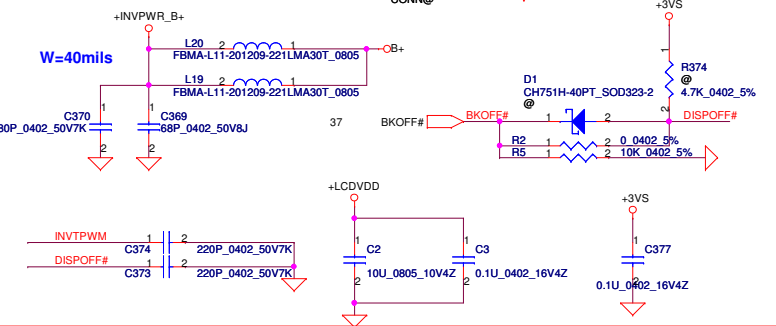
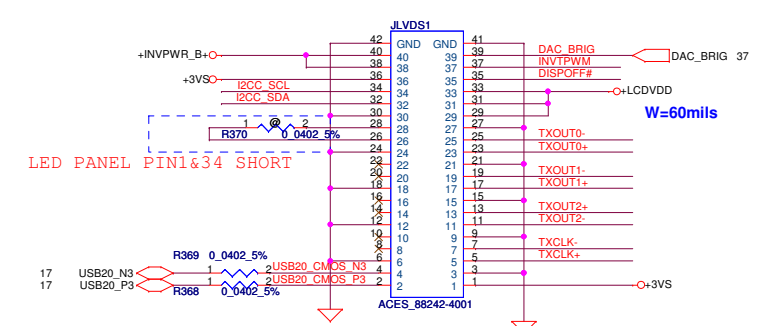
LOW HIGH

Security Classification		Compal Secret Data		Title	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	N11M gDDR3 6/6	
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				Customer	1.0
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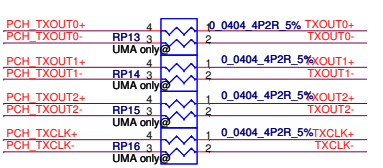
LCD POWER CIRCUIT



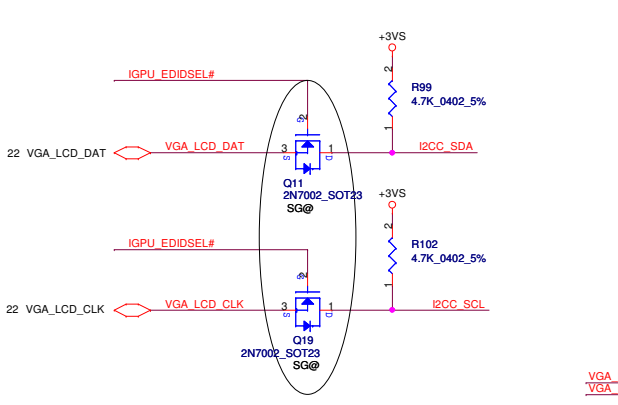
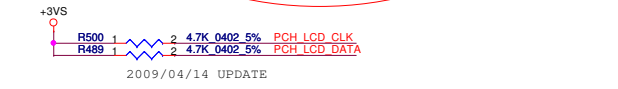
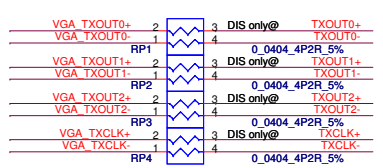
LED PANEL Conn.



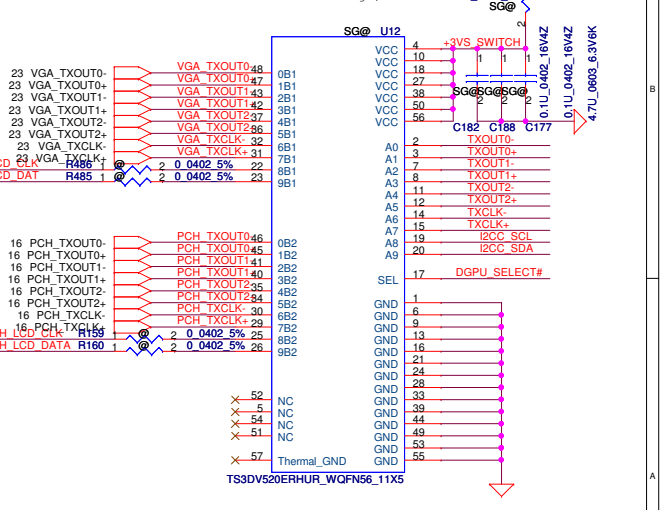
UMA ONLY



DIS ONLY

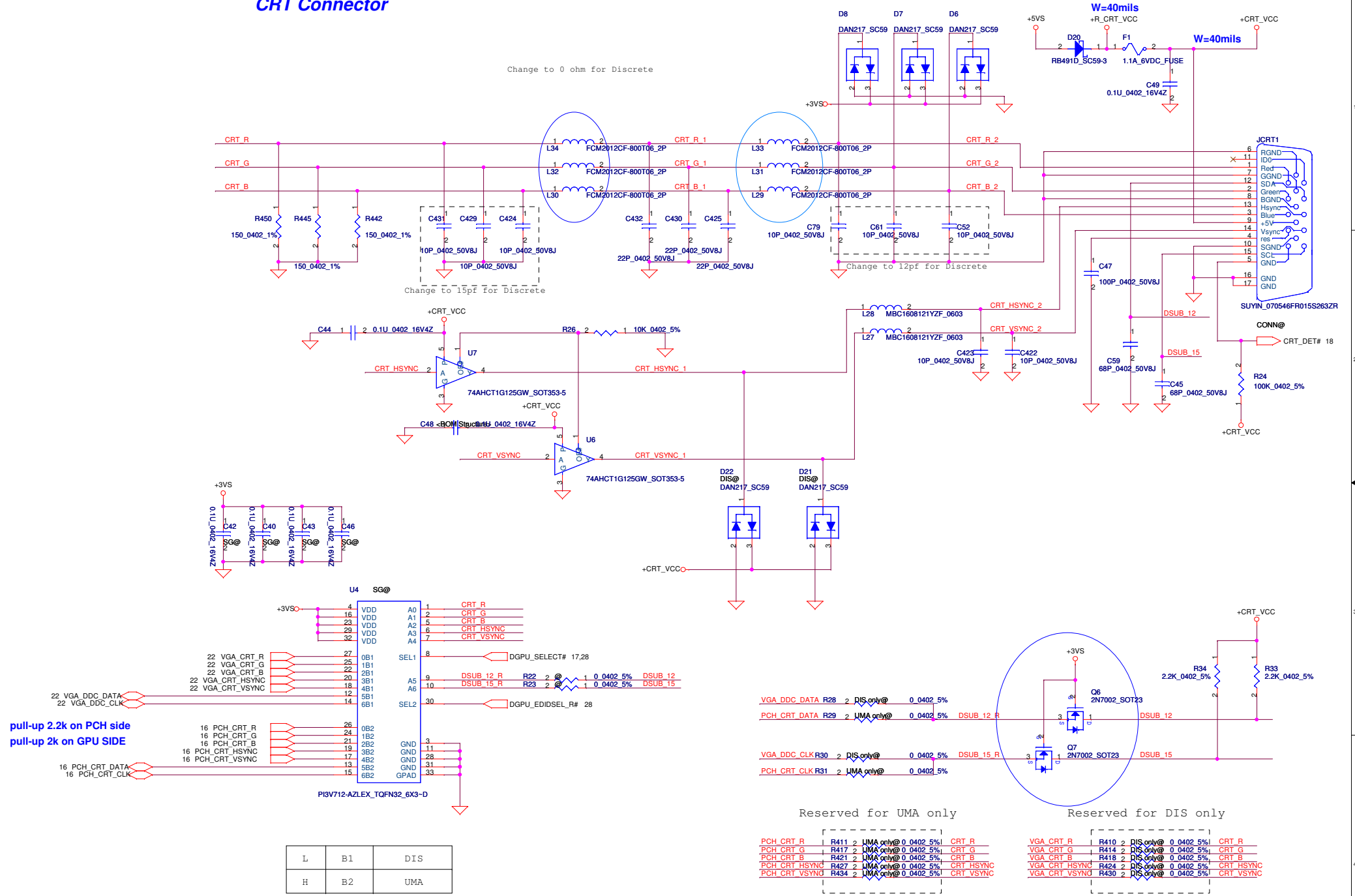


SG For LVDS

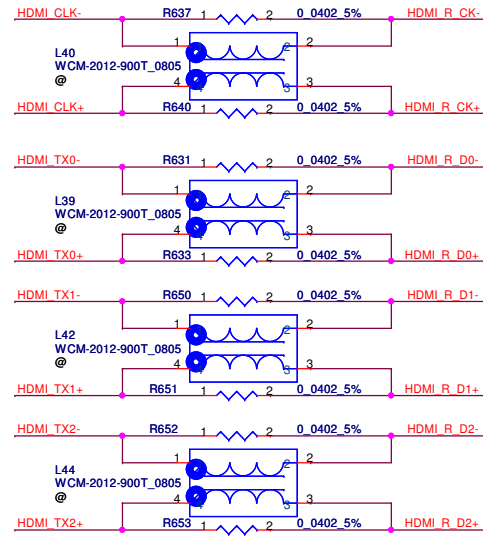
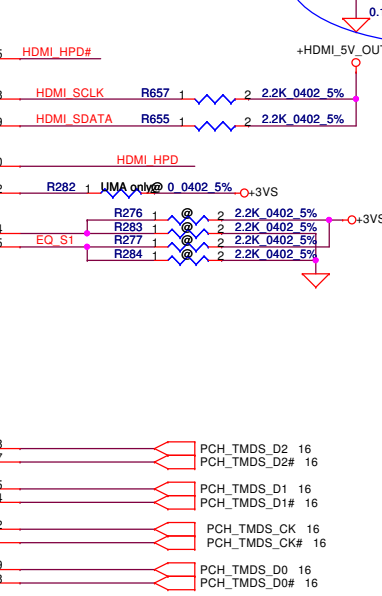
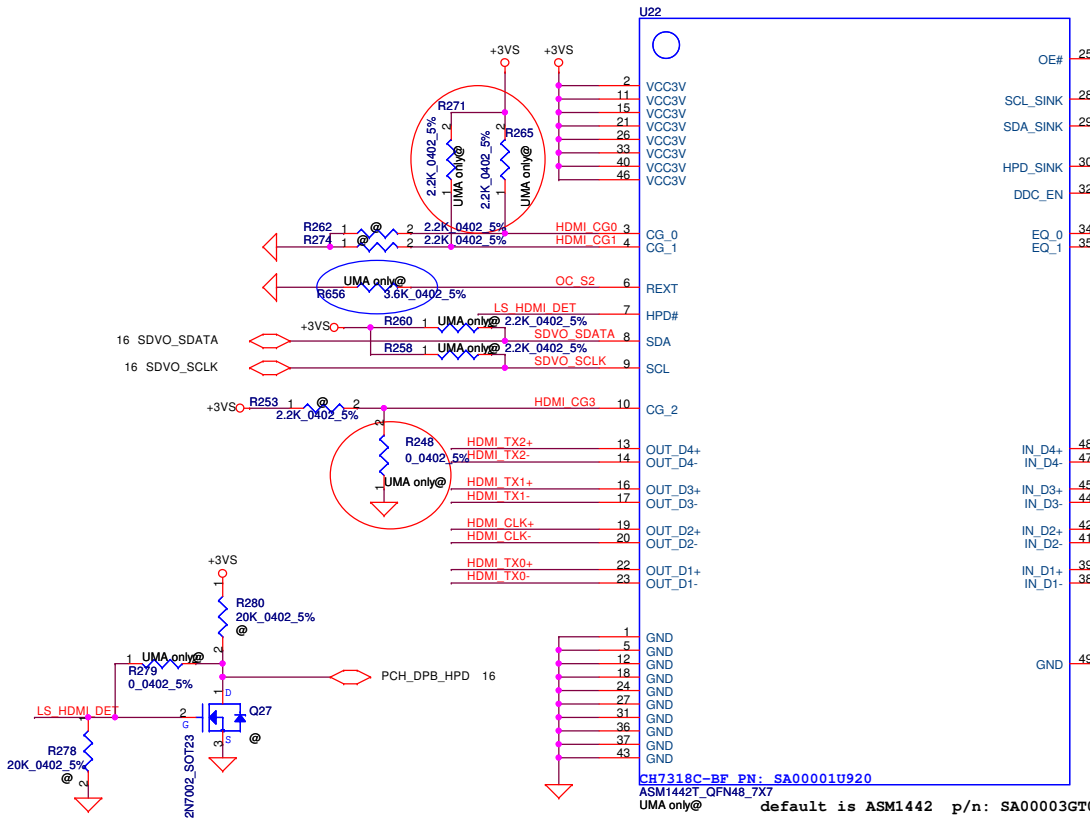
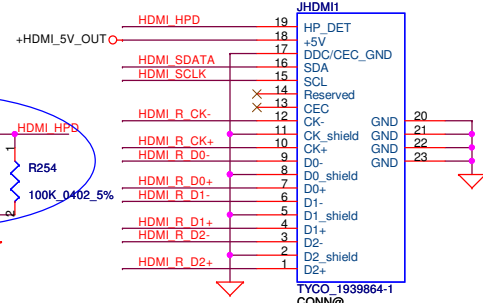
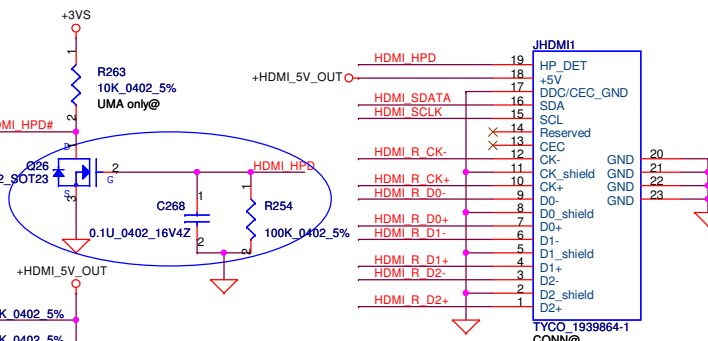
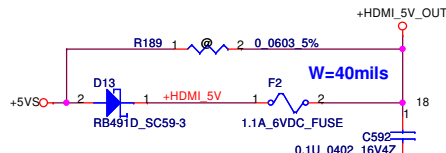
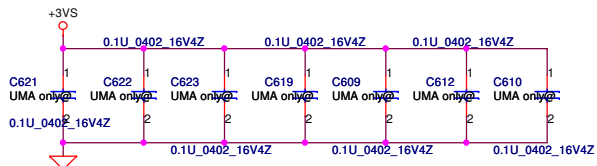


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CRT Connector

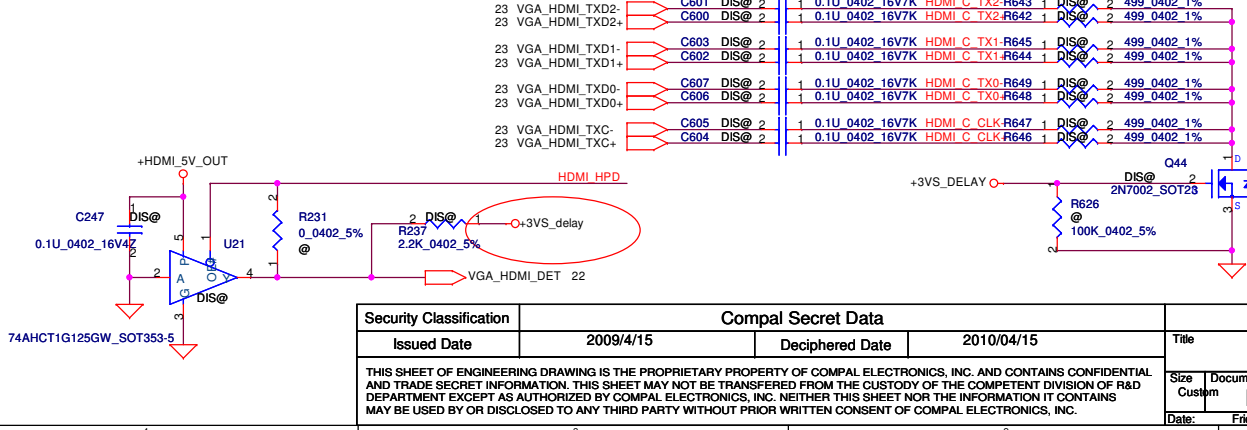
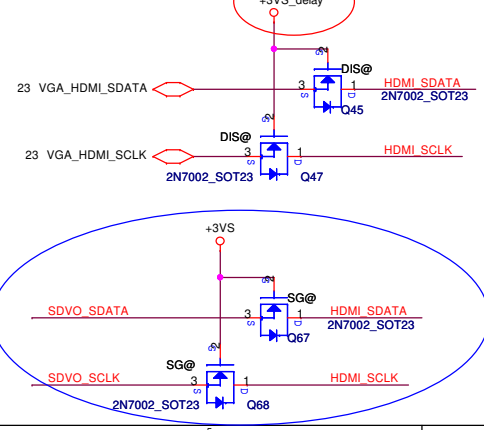


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				Rev 1.0 E Sheet 29 of 60



CH7318C-BF PN: SA00001U920
 ASM1442T_OFN48_TX7
 default is ASM1442 p/n: SA00003GT00

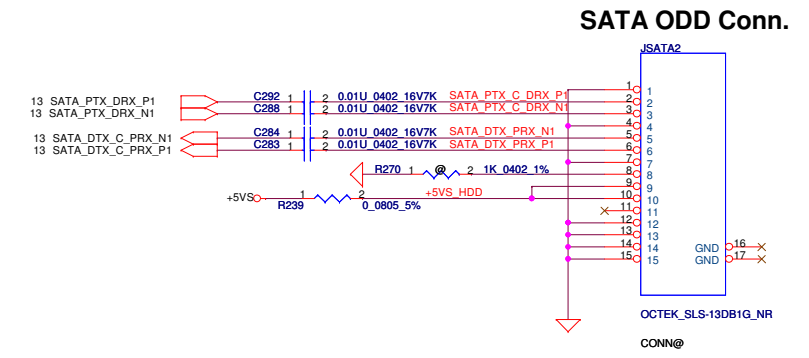
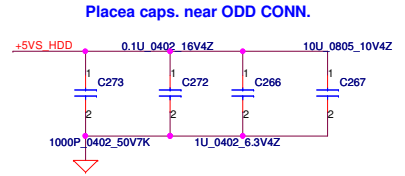
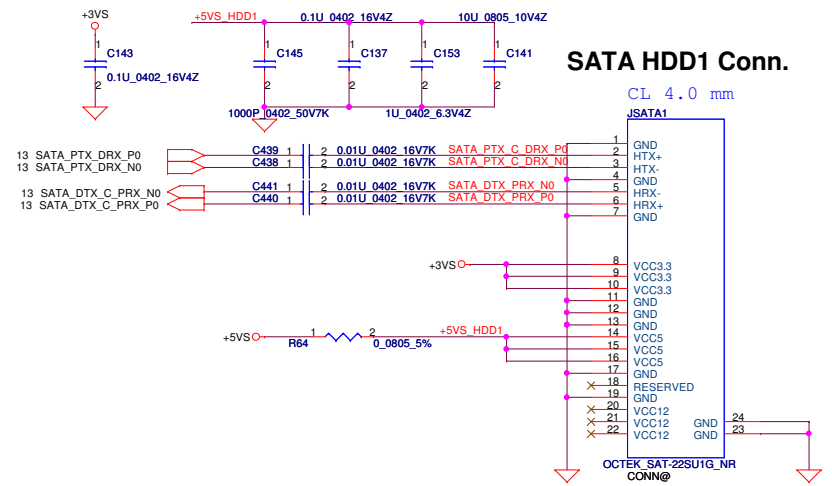
Discrete use



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Issued Date	2009/4/15	Deciphered Date	2010/04/15

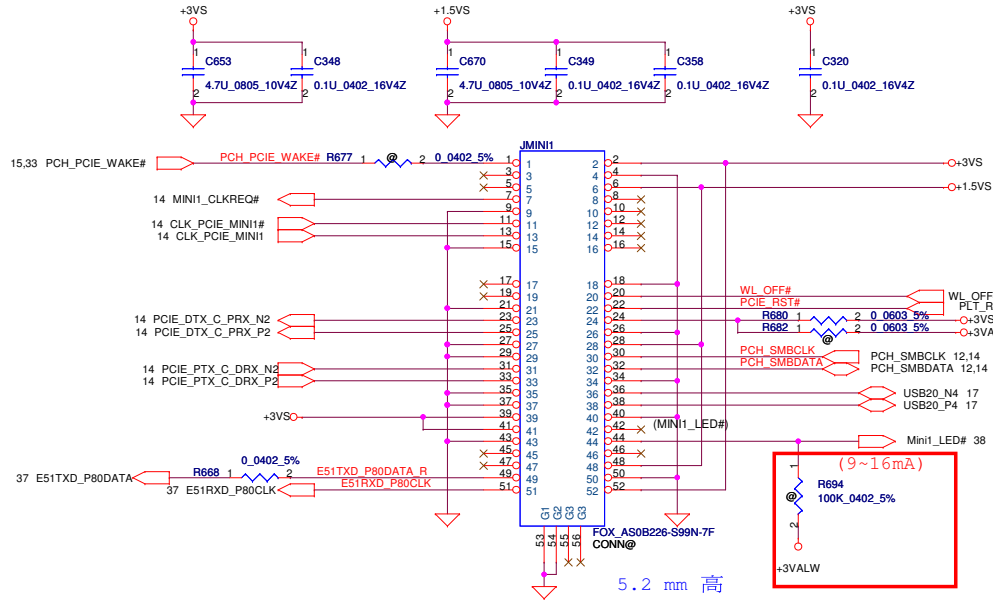
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Compal Electronics, Inc.			
HDMI Level Shife & Conn			
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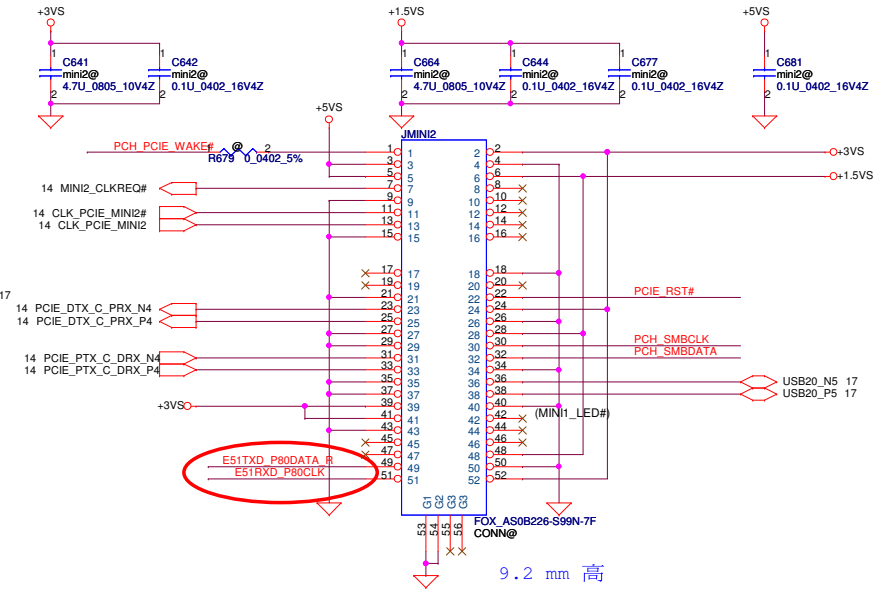
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	HDD & ODD & MINI CARD & CARDREADER Connector	
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Date: Friday, October 23, 2009				Sheet	31 of 60

For Wireless LAN



5.2 mm 高

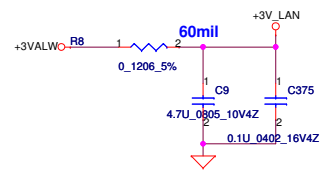
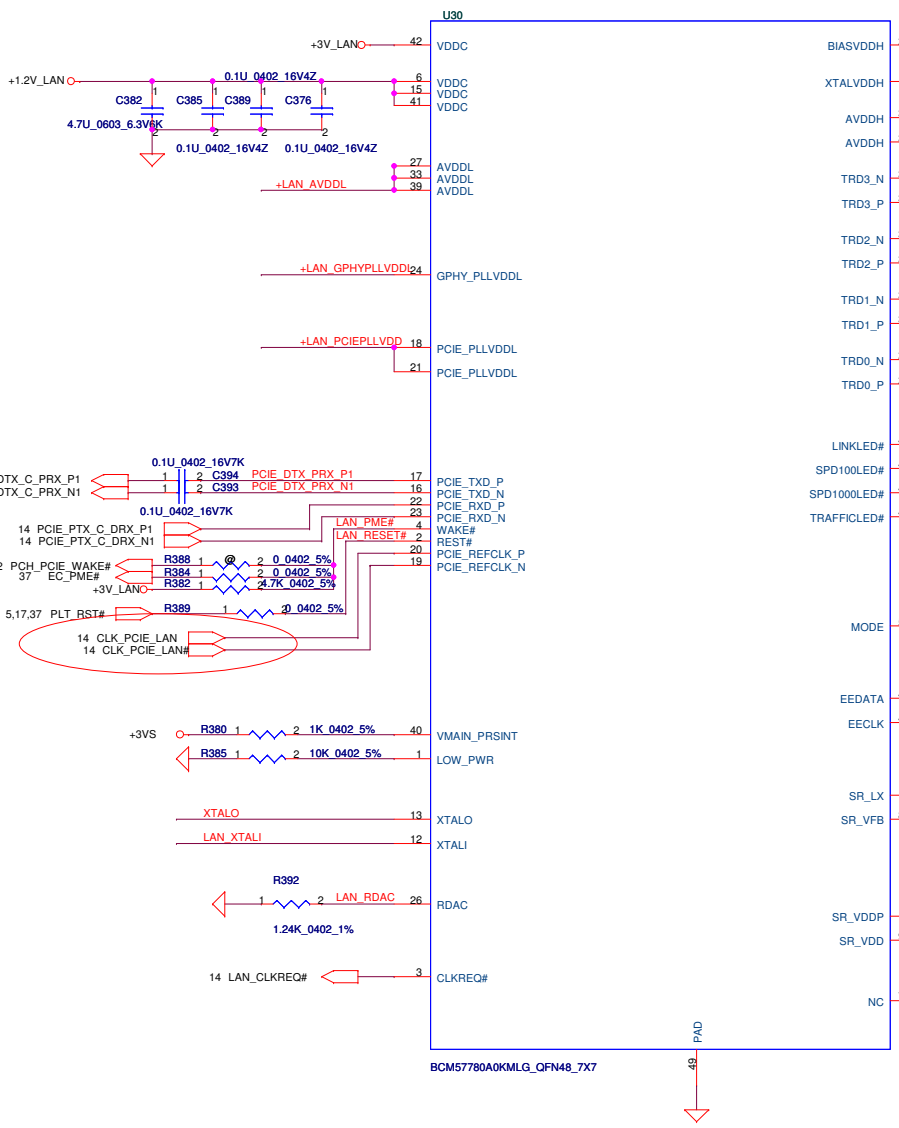
For TV-Tuner/HW MPEG



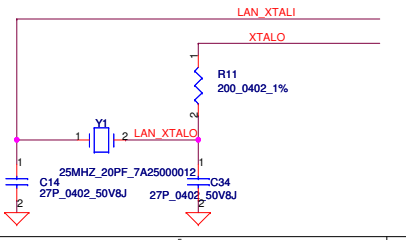
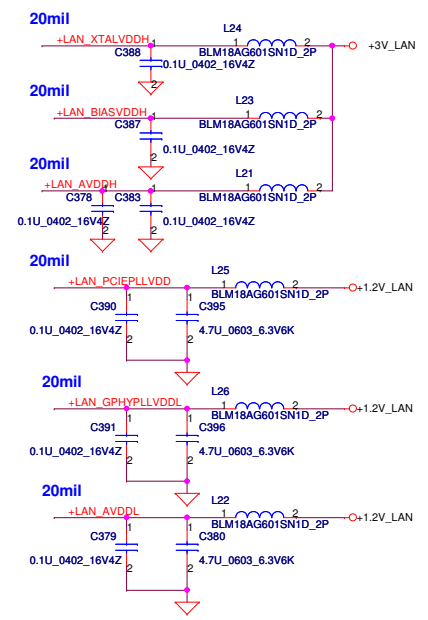
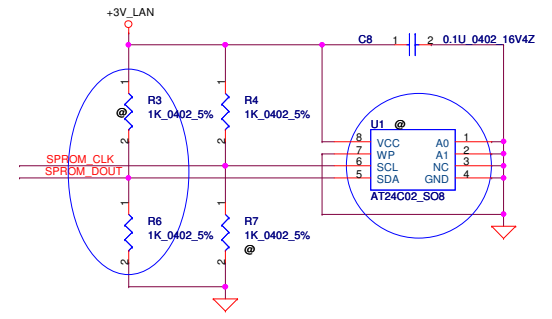
9.2 mm 高

Mini Card Power Rating

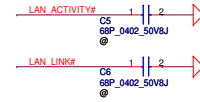
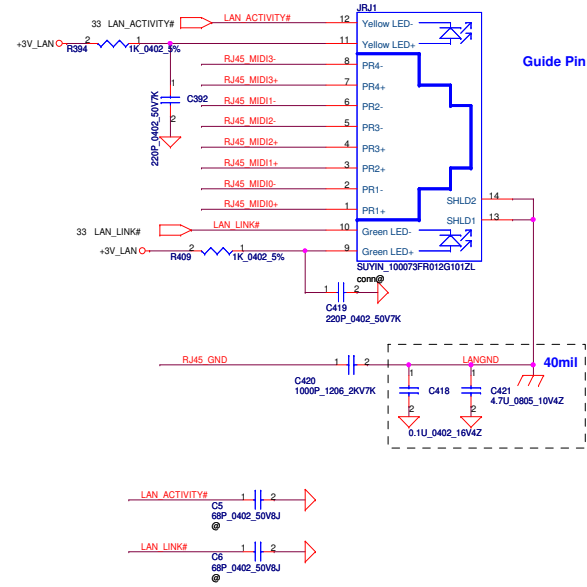
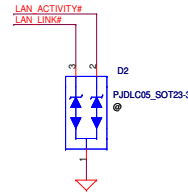
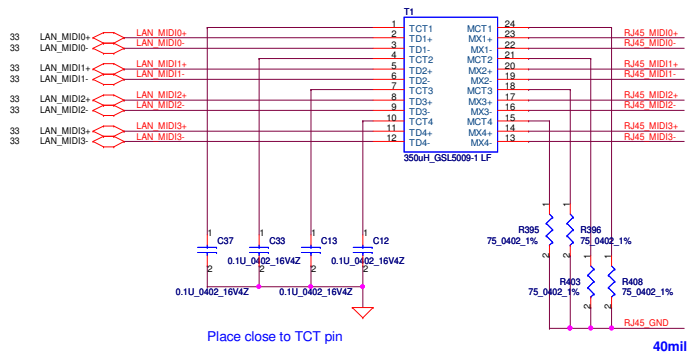
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

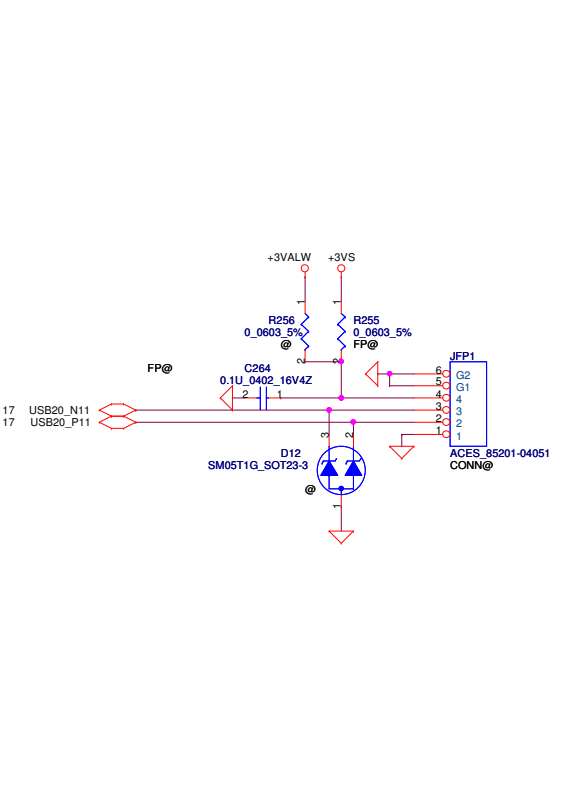


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				NALGO M/B LA-5681P Schematic	1.0
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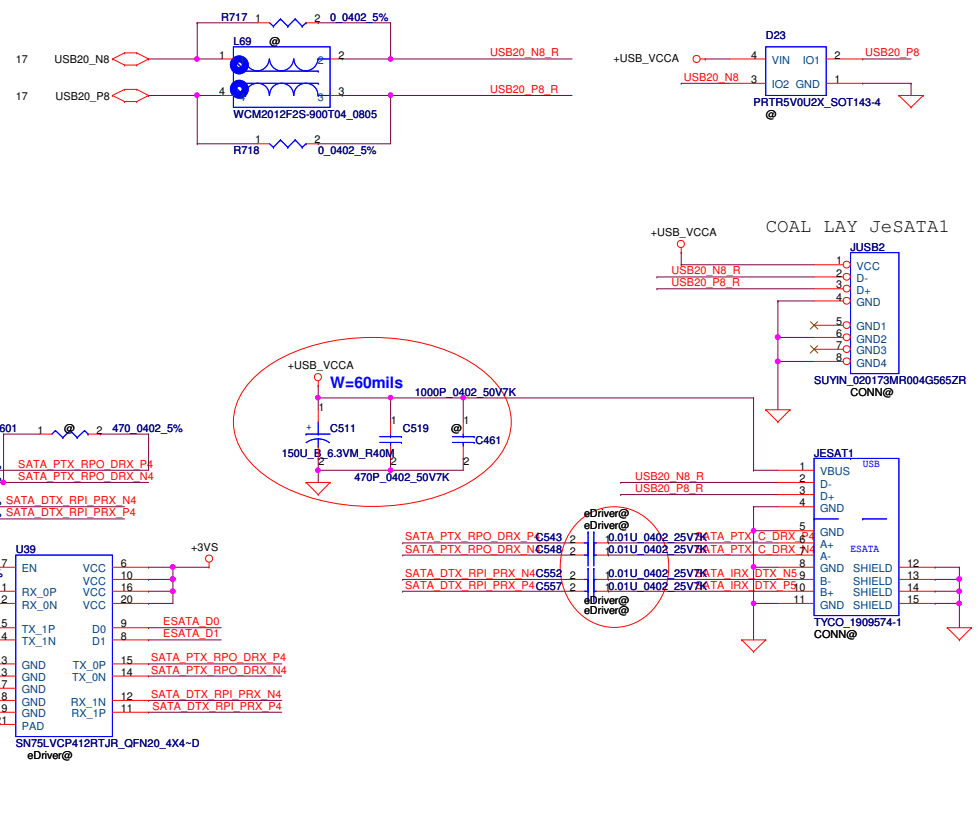
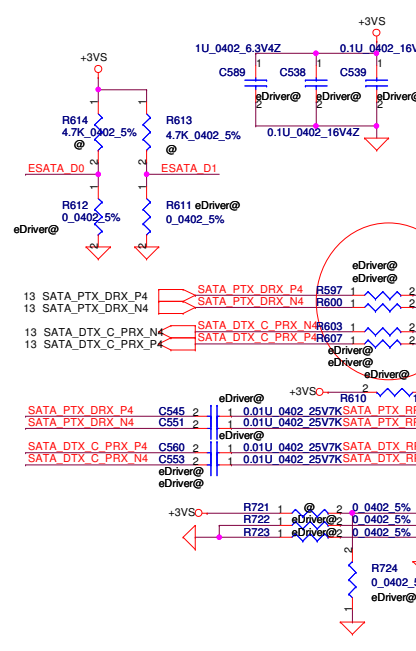
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title
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Finger Print Conn.

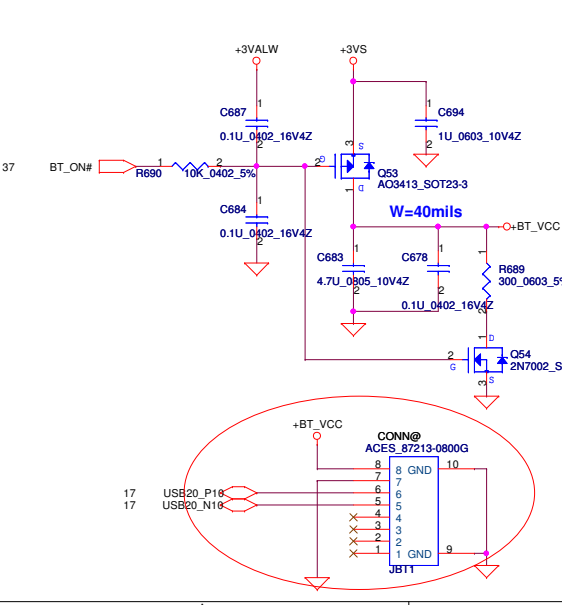


ESATA CONN

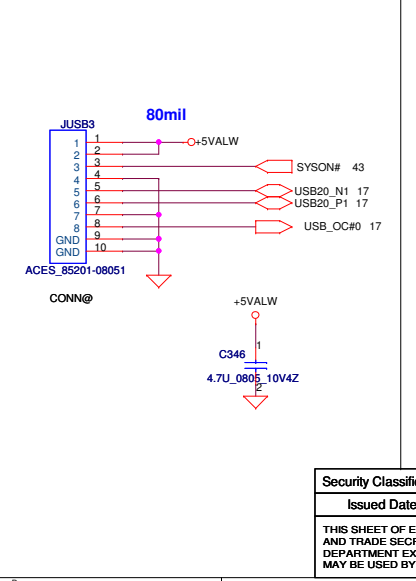
D0	D1	Function
0	0	default; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis



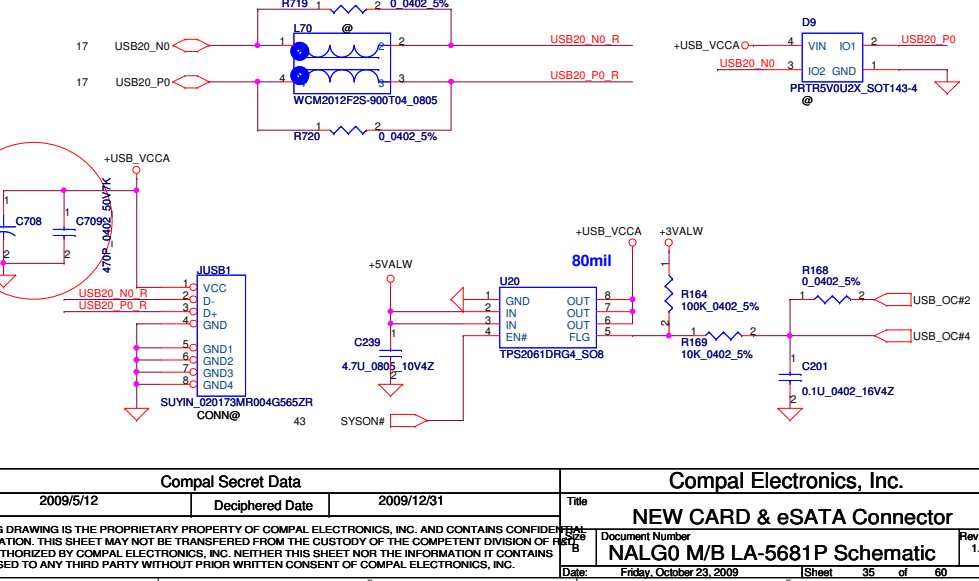
Bluetooth Conn.



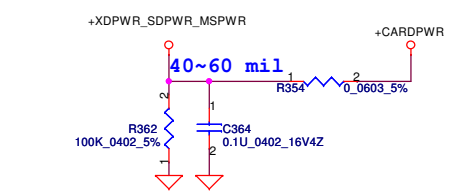
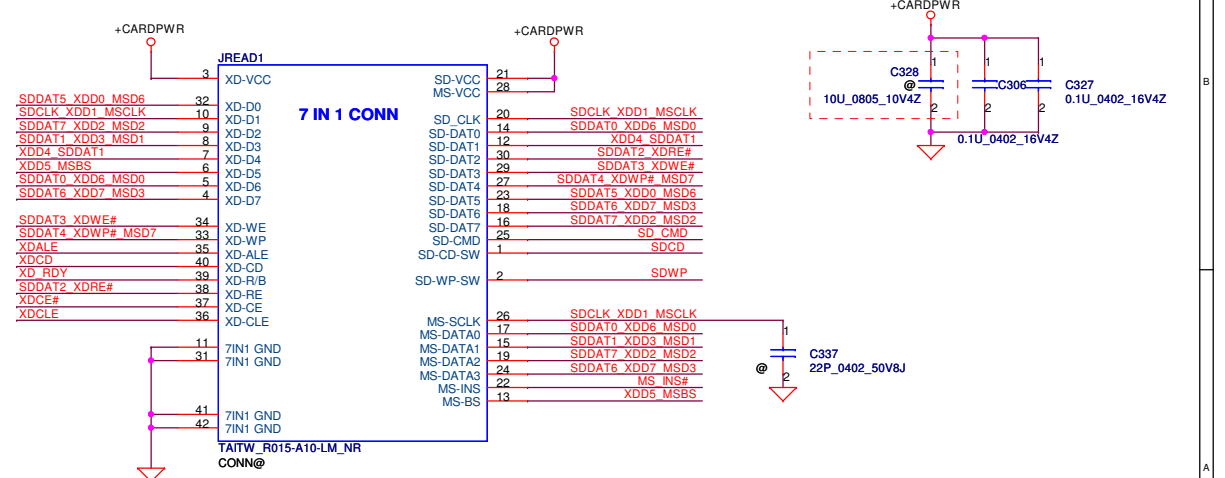
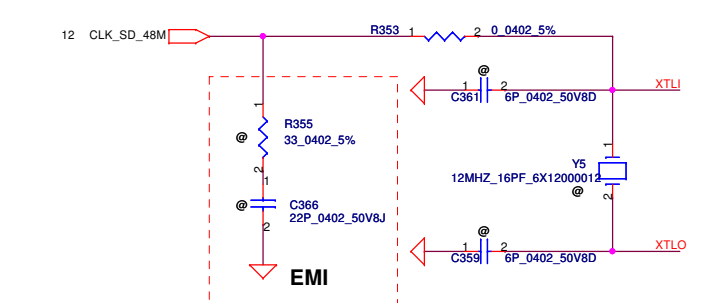
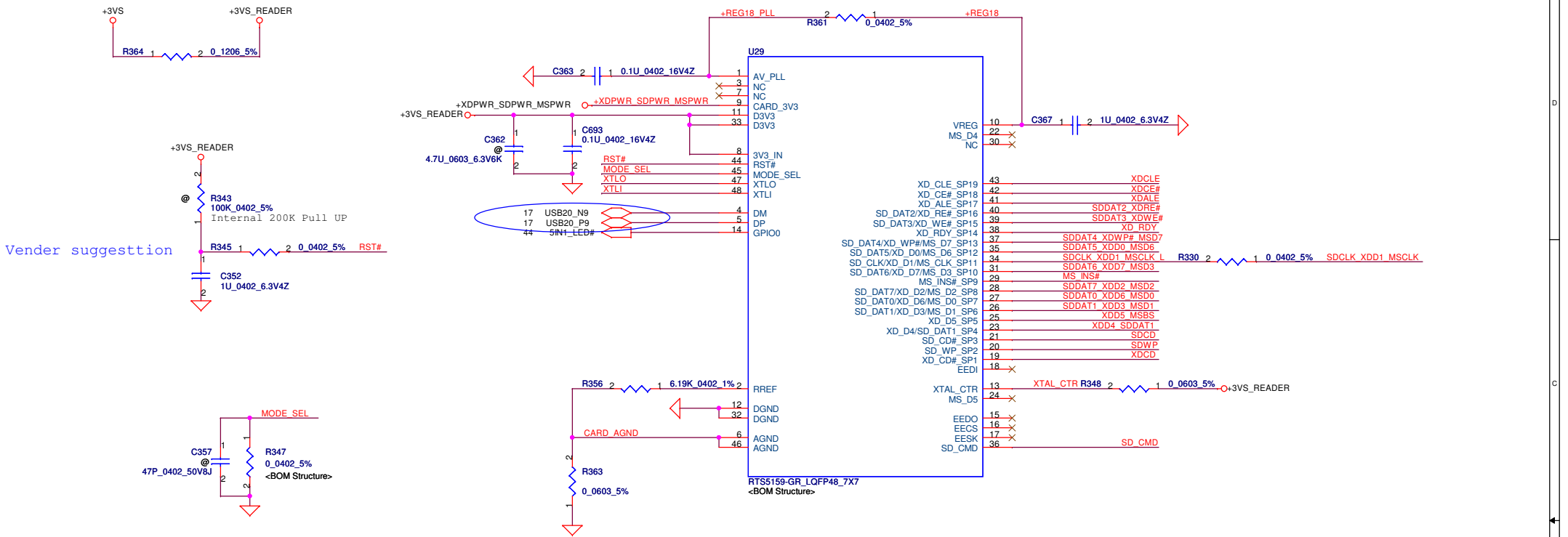
To USB/B Connector



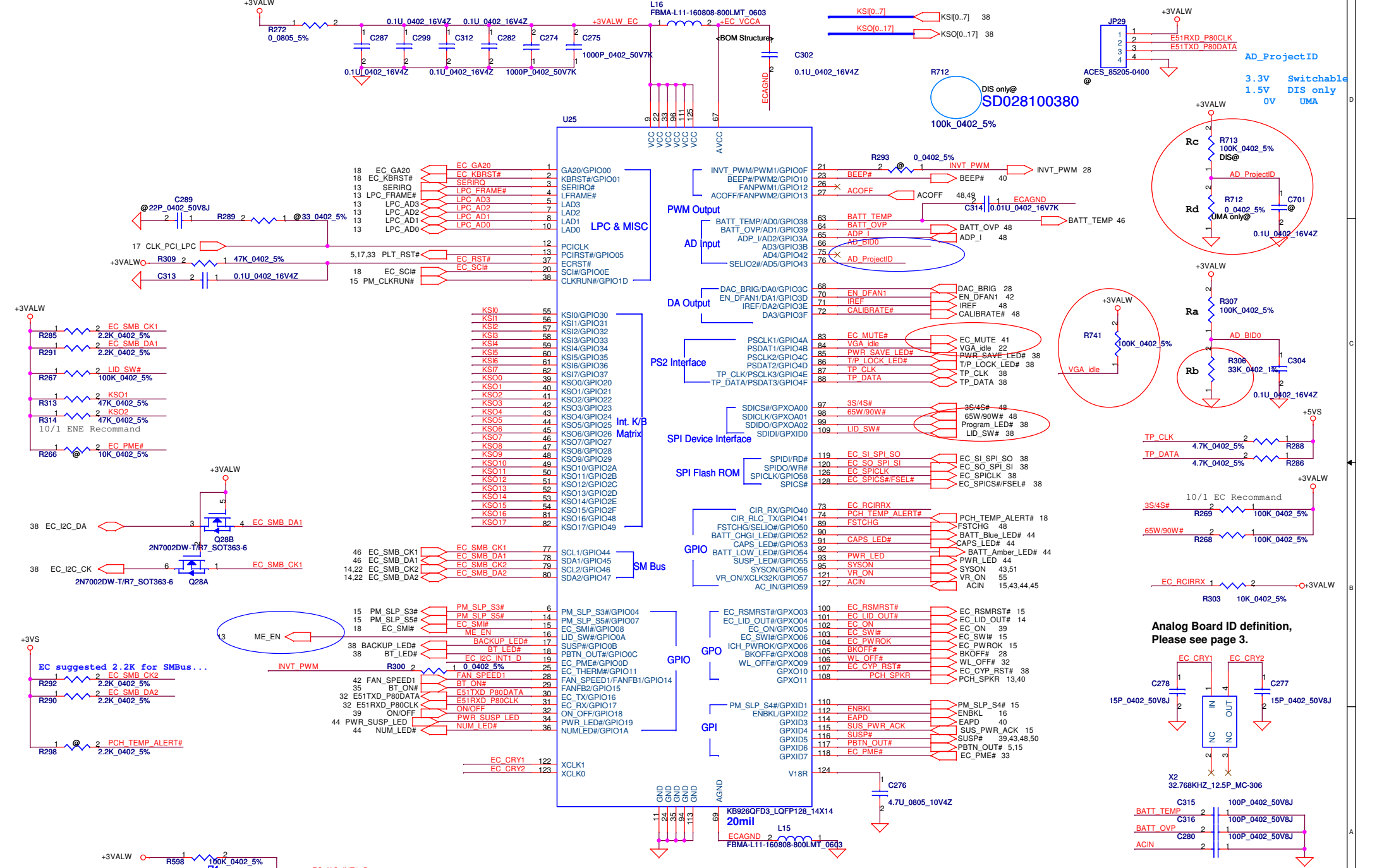
USB CONN.



Security Classification	Compal Secret Data		Title	
Issued Date	2009/5/12	Deciphered Date	2009/12/31	NEW CARD & eSATA Connector
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File No.	Document Number	Rev		
8102B	NALGO M/B LA-5681P Schematic	1.0		
Date:	Friday, October 23, 2009	Sheet	35	of 60



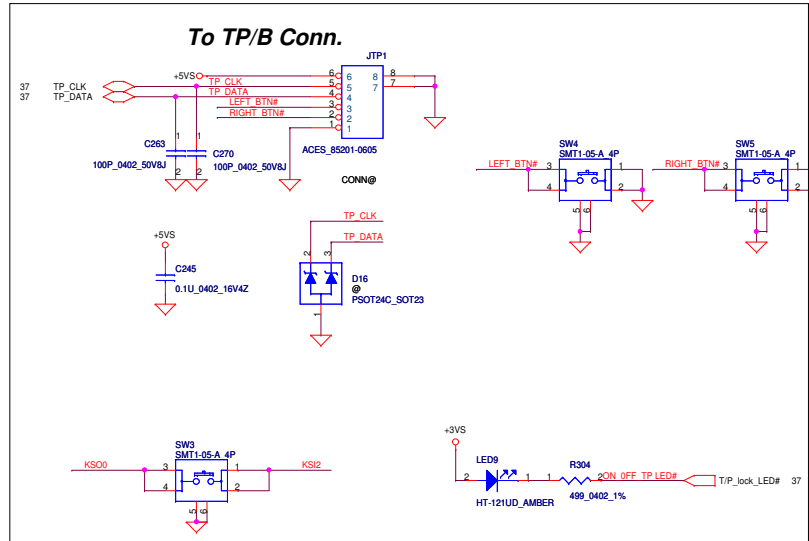
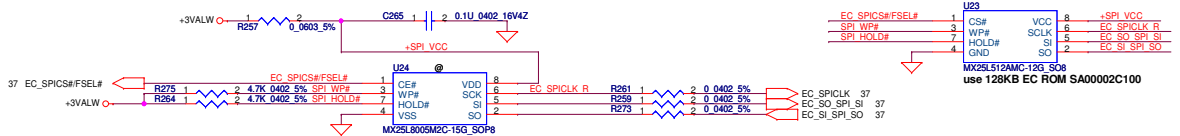
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2009/08/10	Title	
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Size	Document Number	Customer		Rev	
	NALG0 M/B LA-5681P Schematic	Friday, October 23, 2009		1.0	
Date:	Friday, October 23, 2009	Sheet	36	of 60	



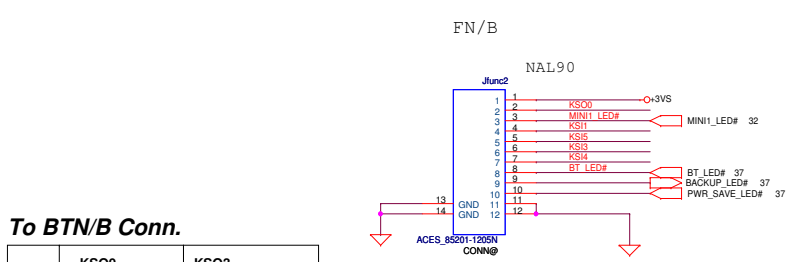
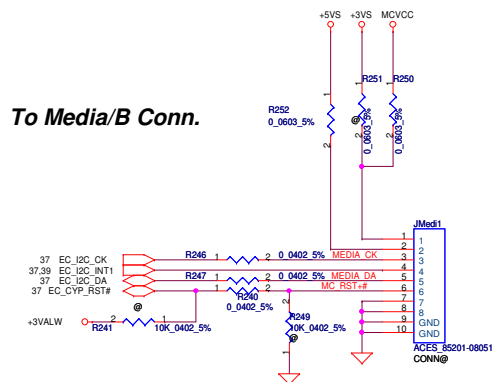
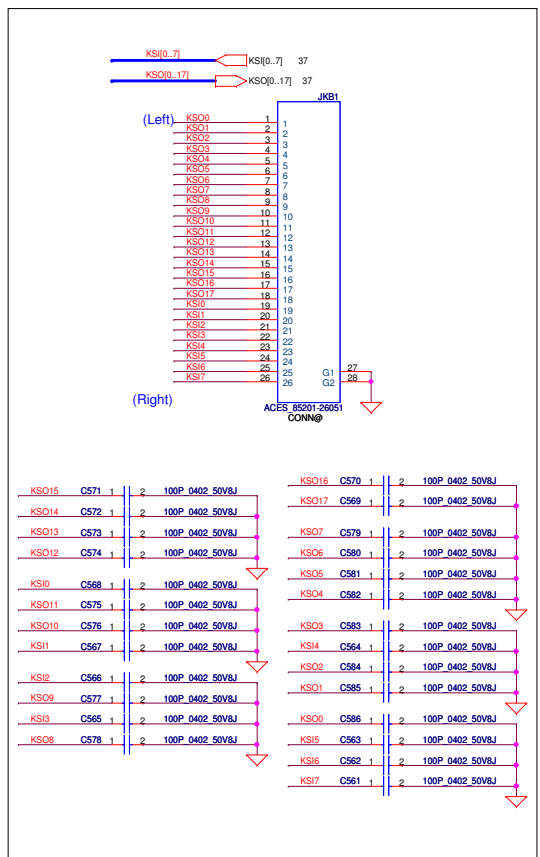
AD_ProjectID
3.3V Switchable
1.5V DIS only
0V UMA

Analog Board ID definition,
Please see page 3.

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B				1.0	
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ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

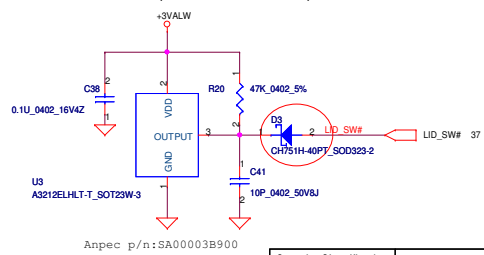


To BTN/B Conn.

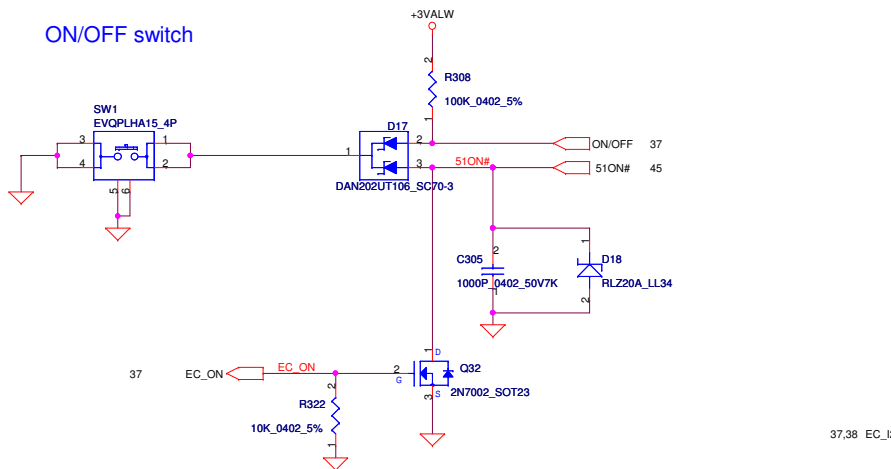
	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

Lid Switch

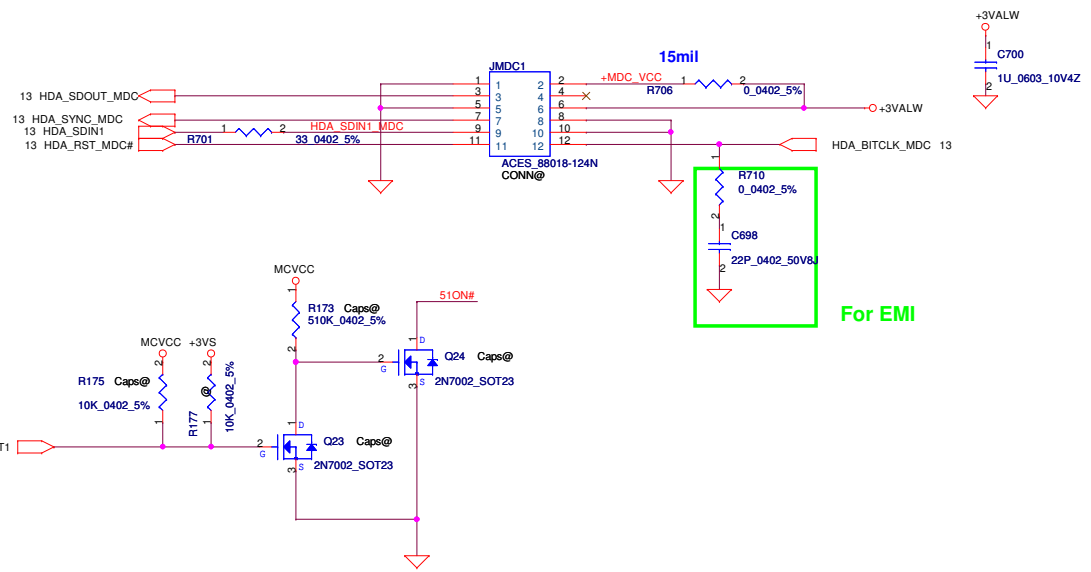
(Hall Effect Switch)



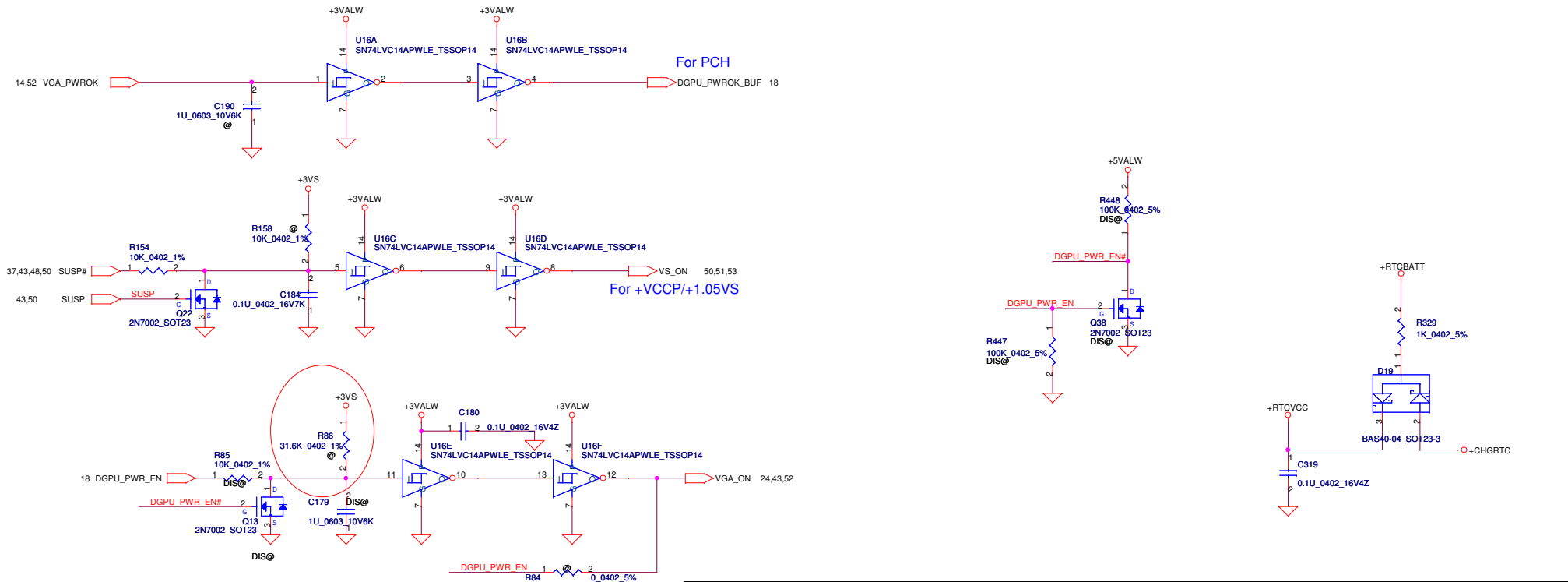
Power Button



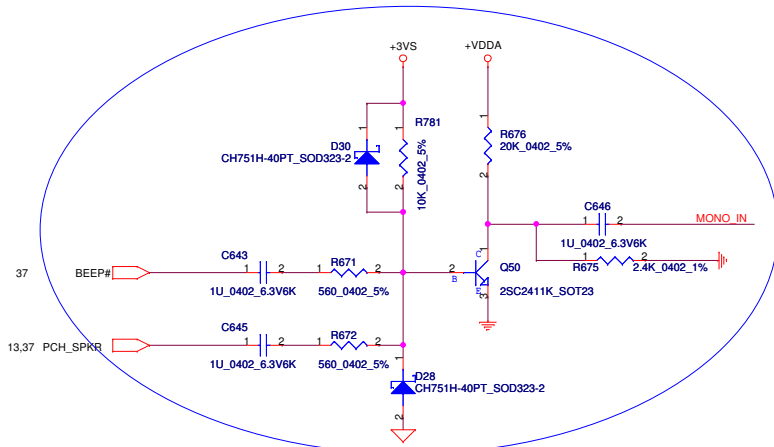
HDA MDC Conn.



Power ON Circuit



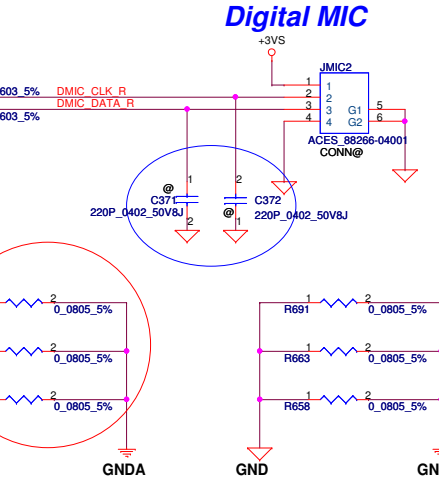
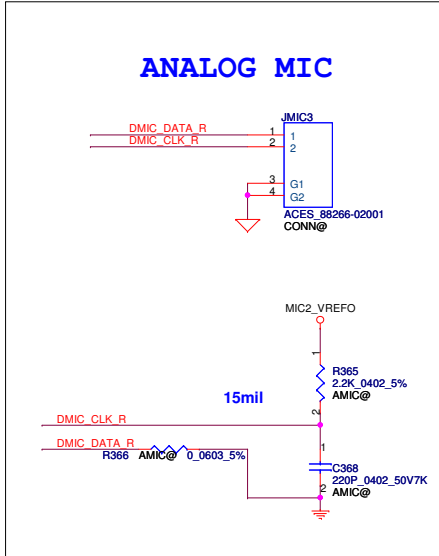
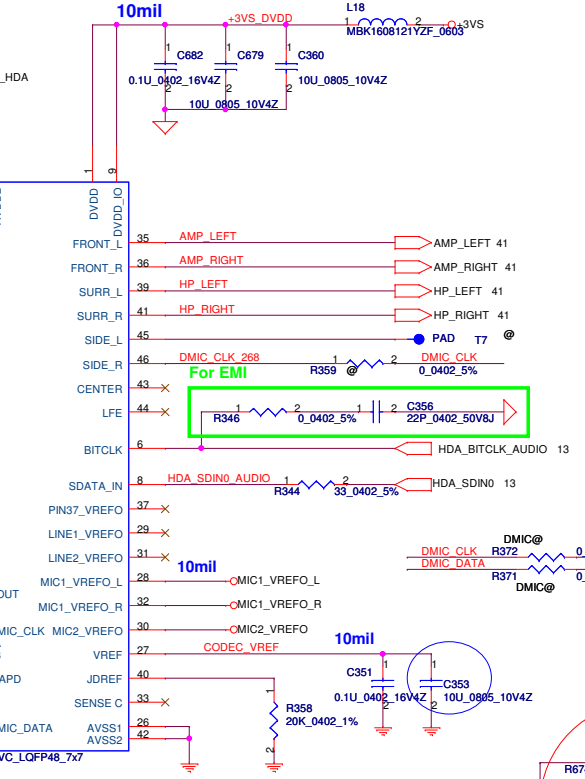
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Issued Date	2009/5/12	Deciphered Date	2009/12/31	Title	
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BOM Option

ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@

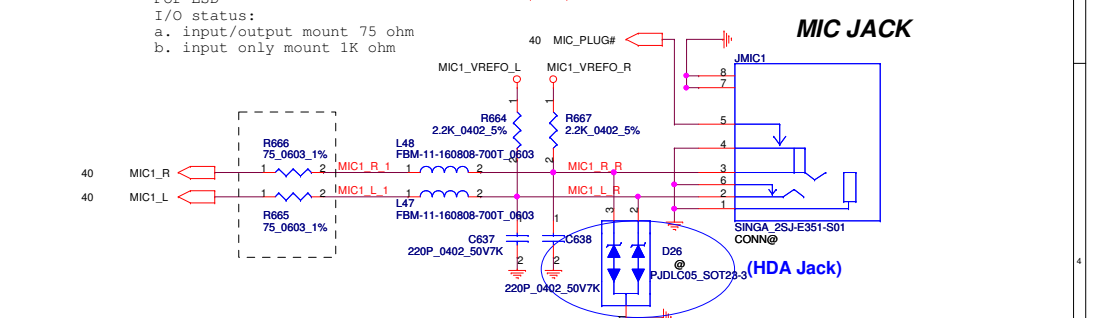
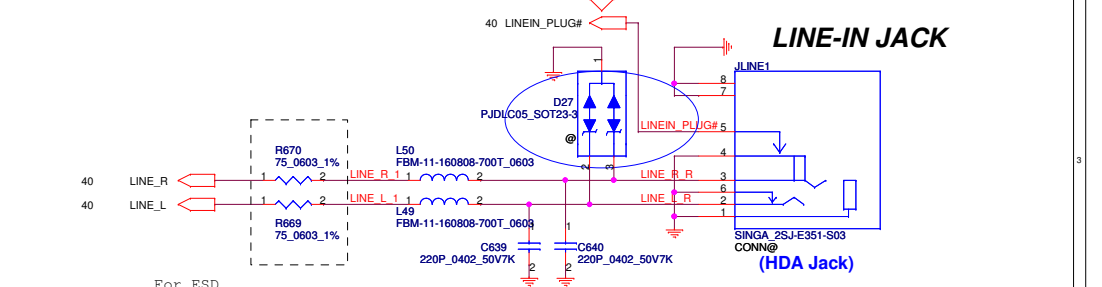
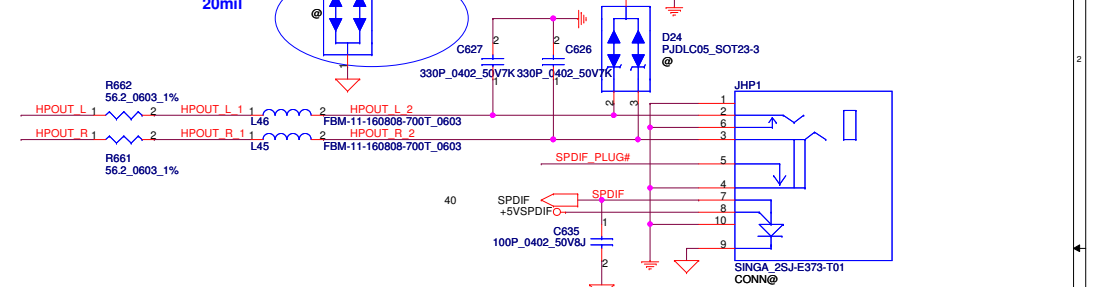
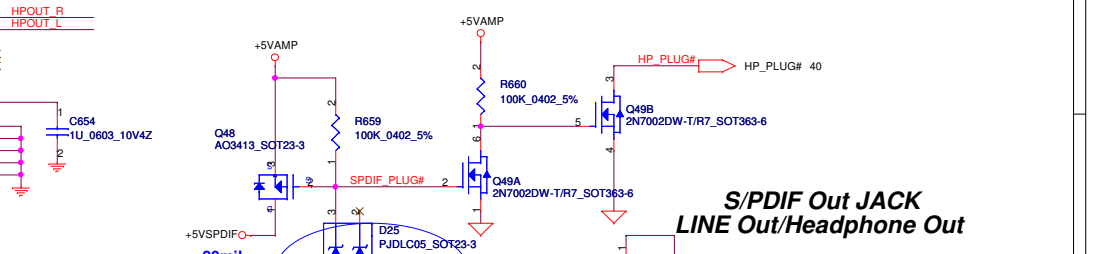
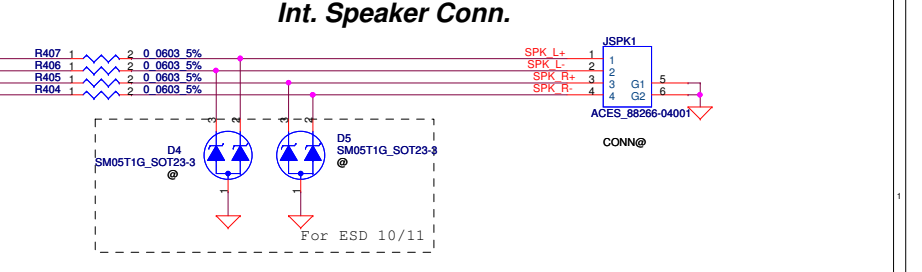
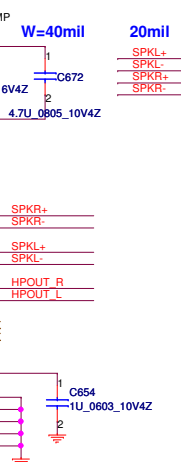
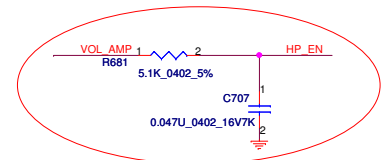
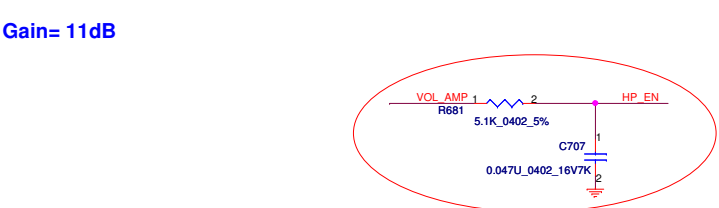
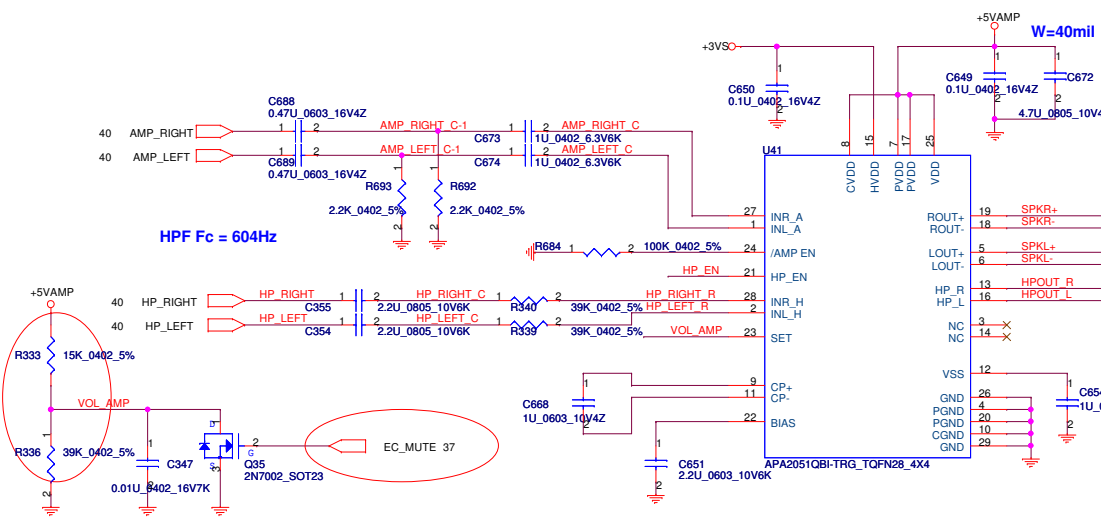
HD Audio Codec



Place close to Codec

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

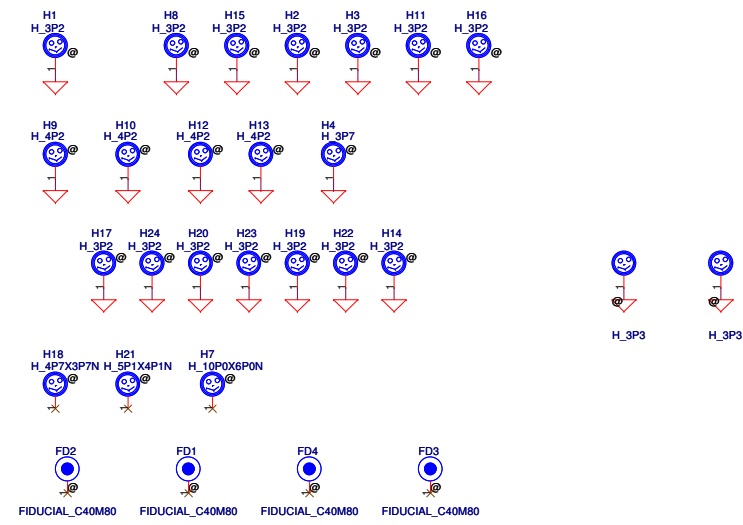
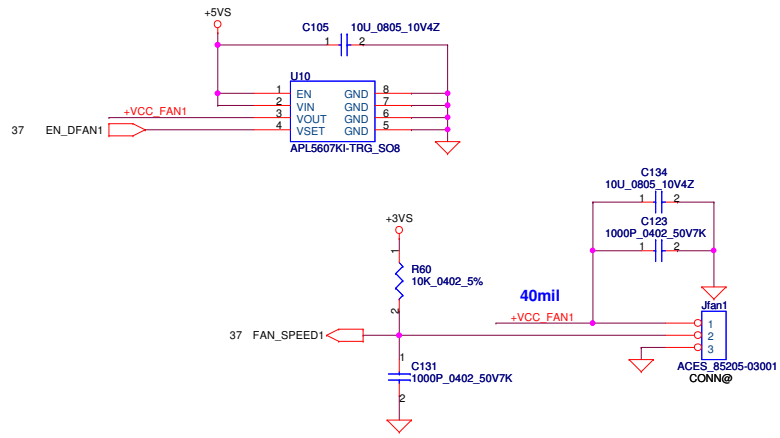
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Issued Date	2009/5/12	Deciphered Date	2009/12/31	HD Audio Codec ALC888S-VC
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For ESD
I/O status:
a. input/output mount 75 ohm
b. input only mount 1K ohm

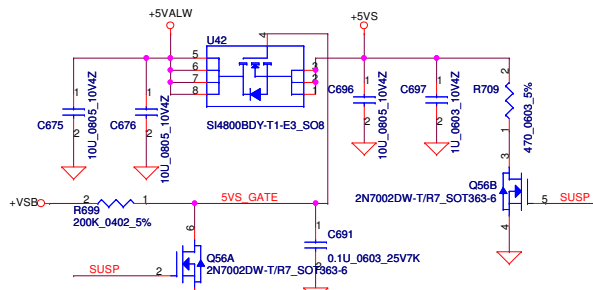
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/5/12	Deciphered Date	2009/12/31	Title
				Amplifier & Audio Jack
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Date: Friday, October 23, 2009		Sheet 41 of 60		Rev 1.0

FAN1 Conn

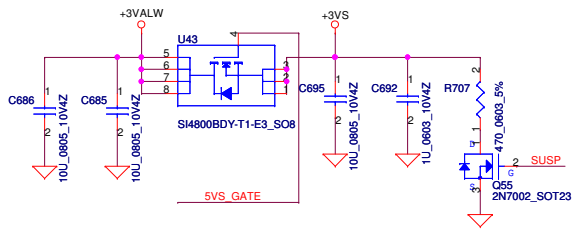


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				NALG0 M/B LA-5681P Schematic
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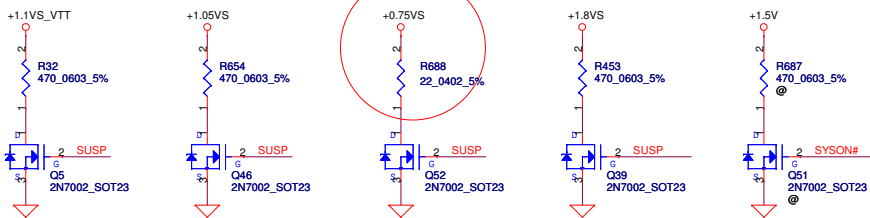
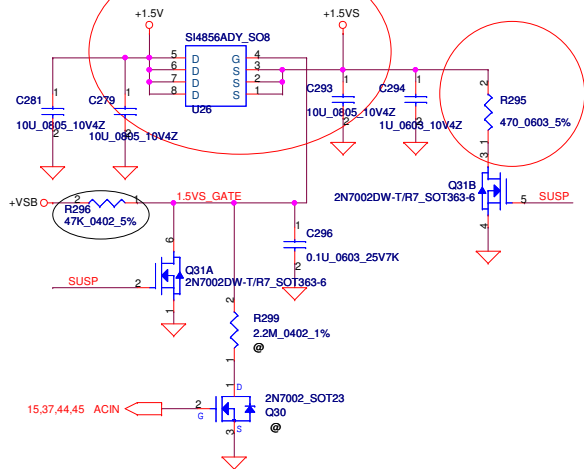
+5VALW TO +5VS



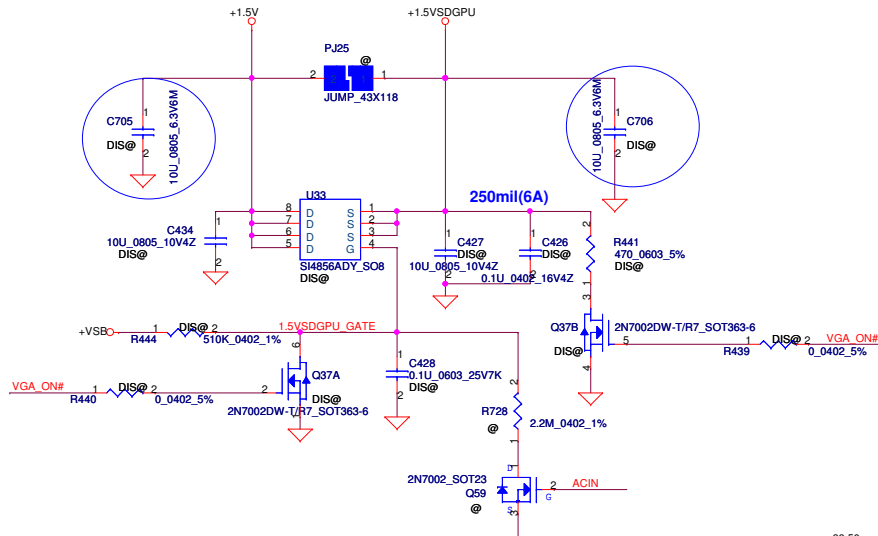
+3VALW TO +3VS



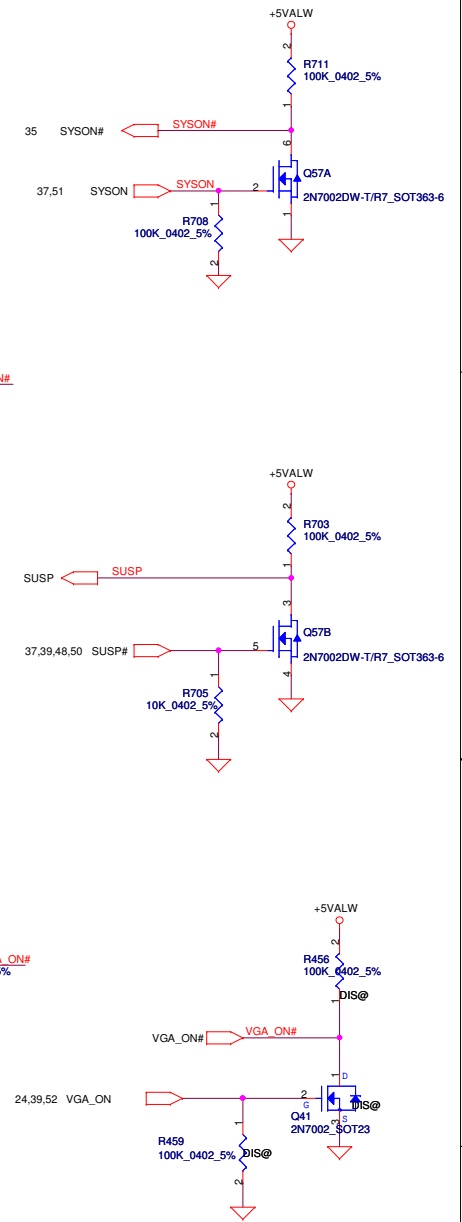
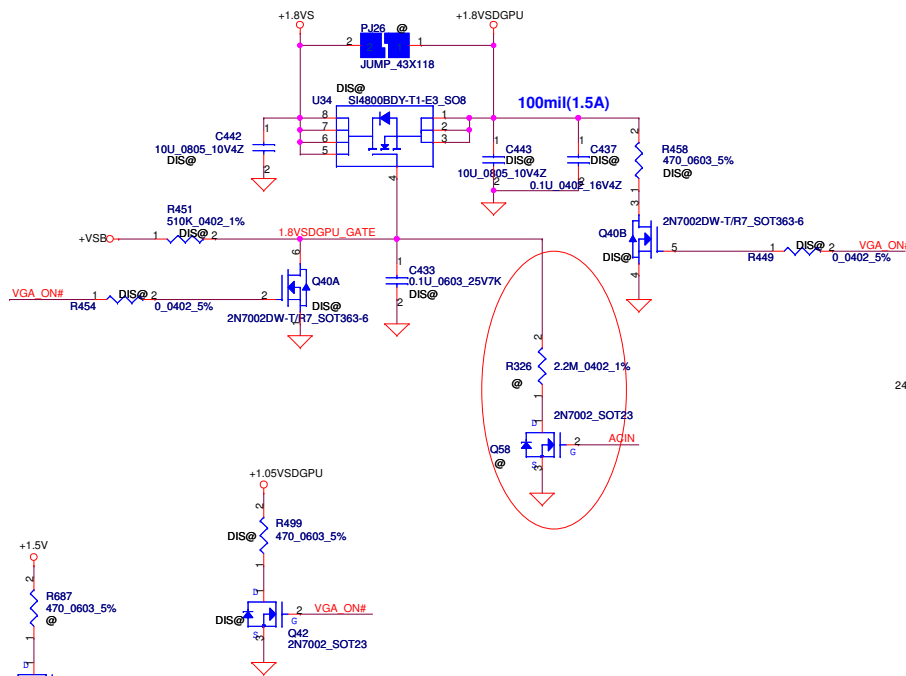
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU Transfer

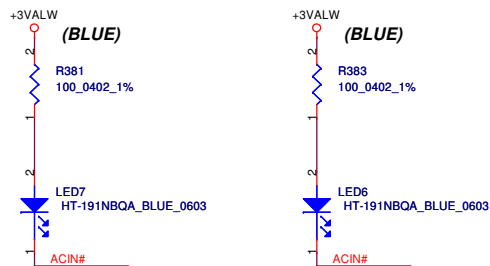


+1.8VS to +1.8VSDGPU Transfer

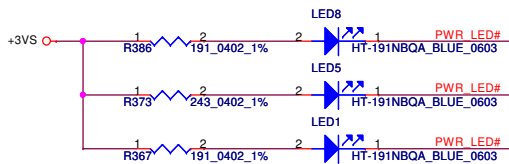


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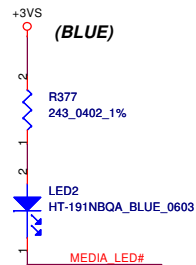
Enlightener LED



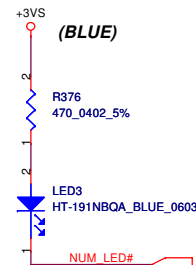
ON/OFF LED LEFT



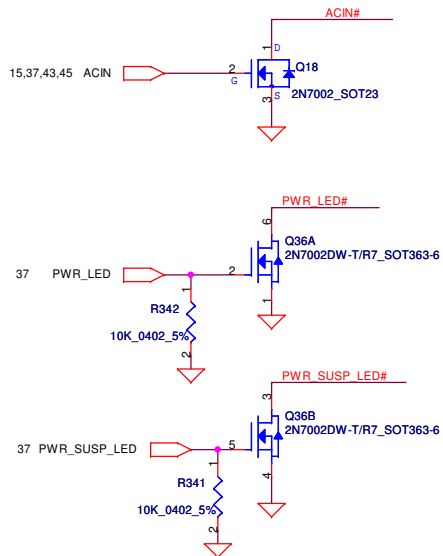
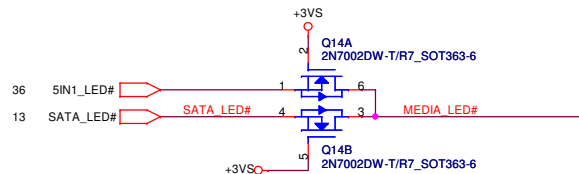
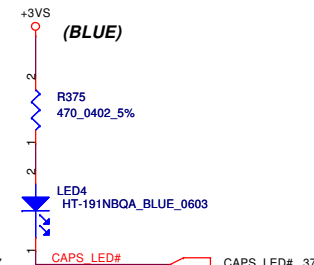
MEDIA_LED



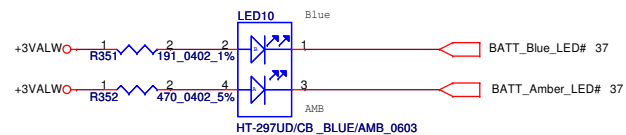
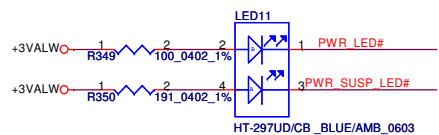
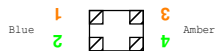
NUM_LED



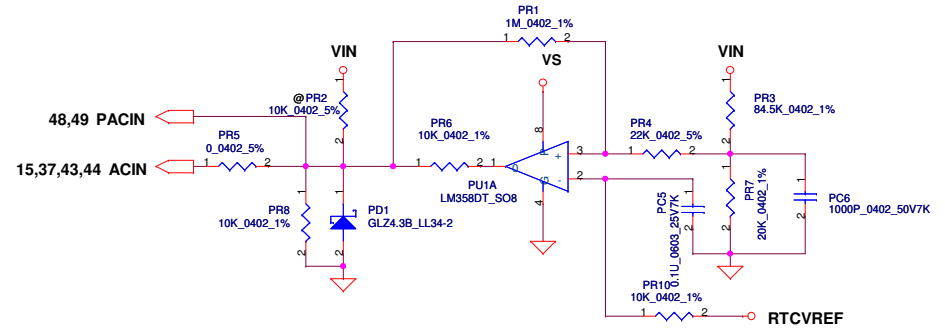
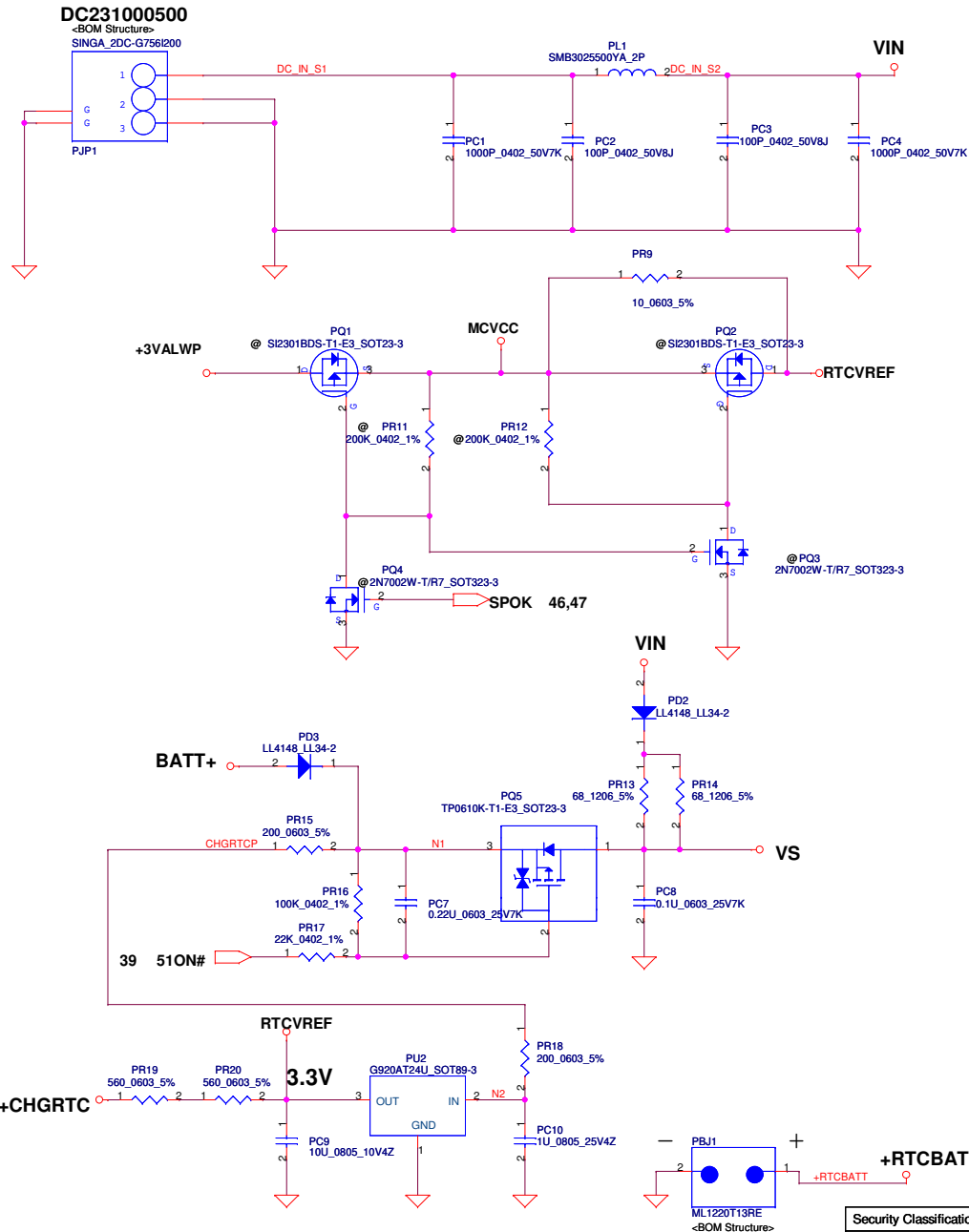
CAPS_LED



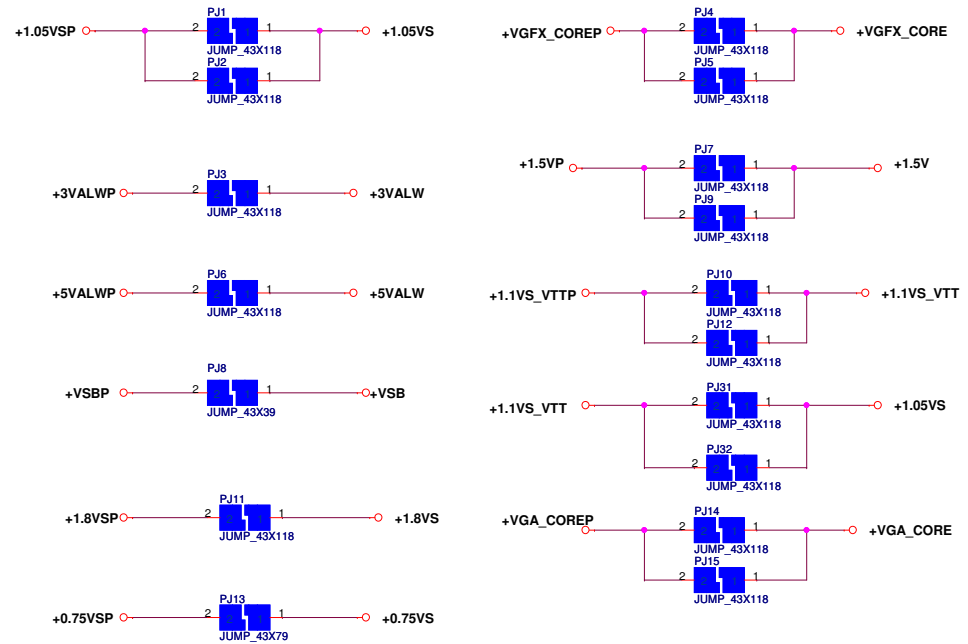
Compal Footprint



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				PWR/B	
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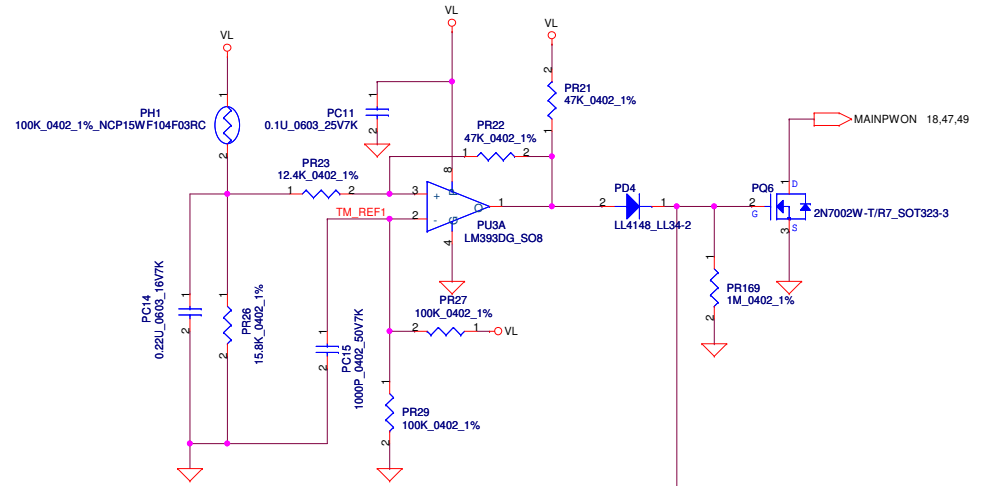
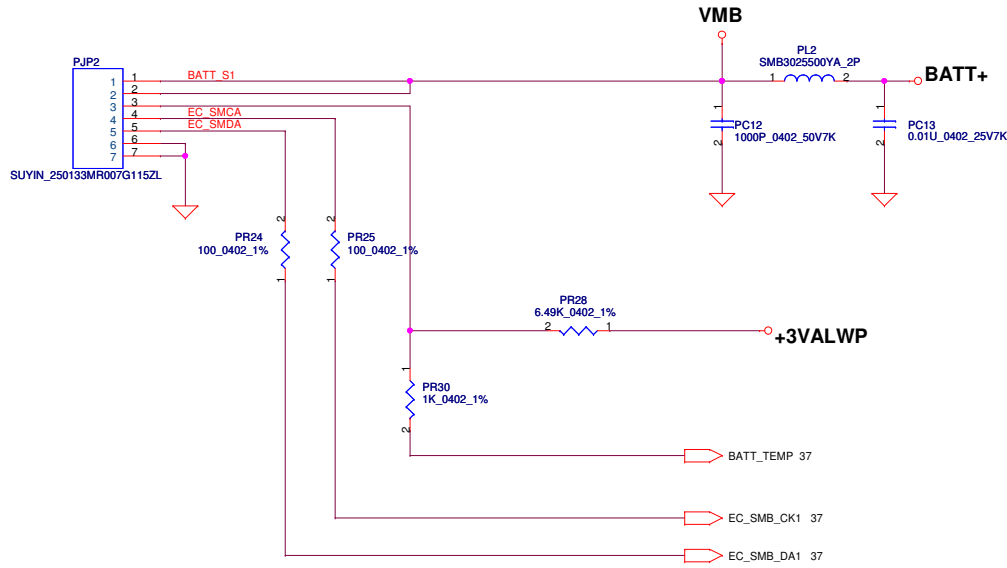


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



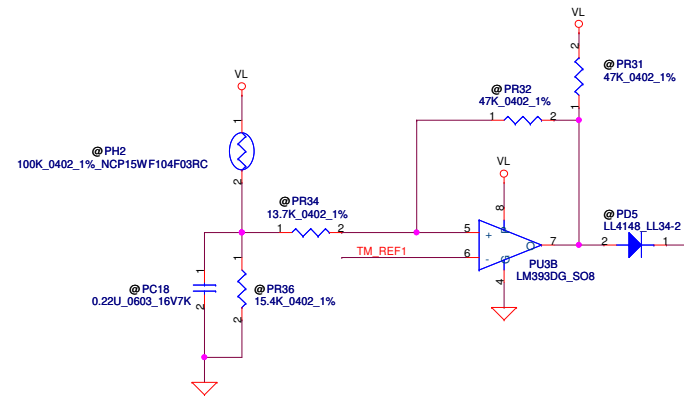
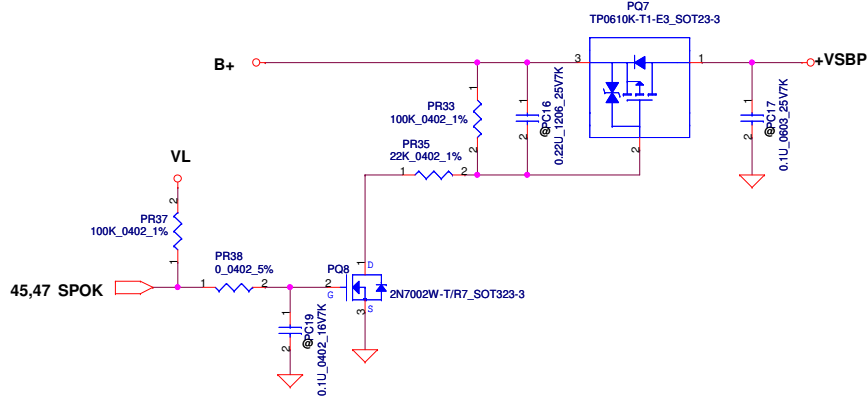
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

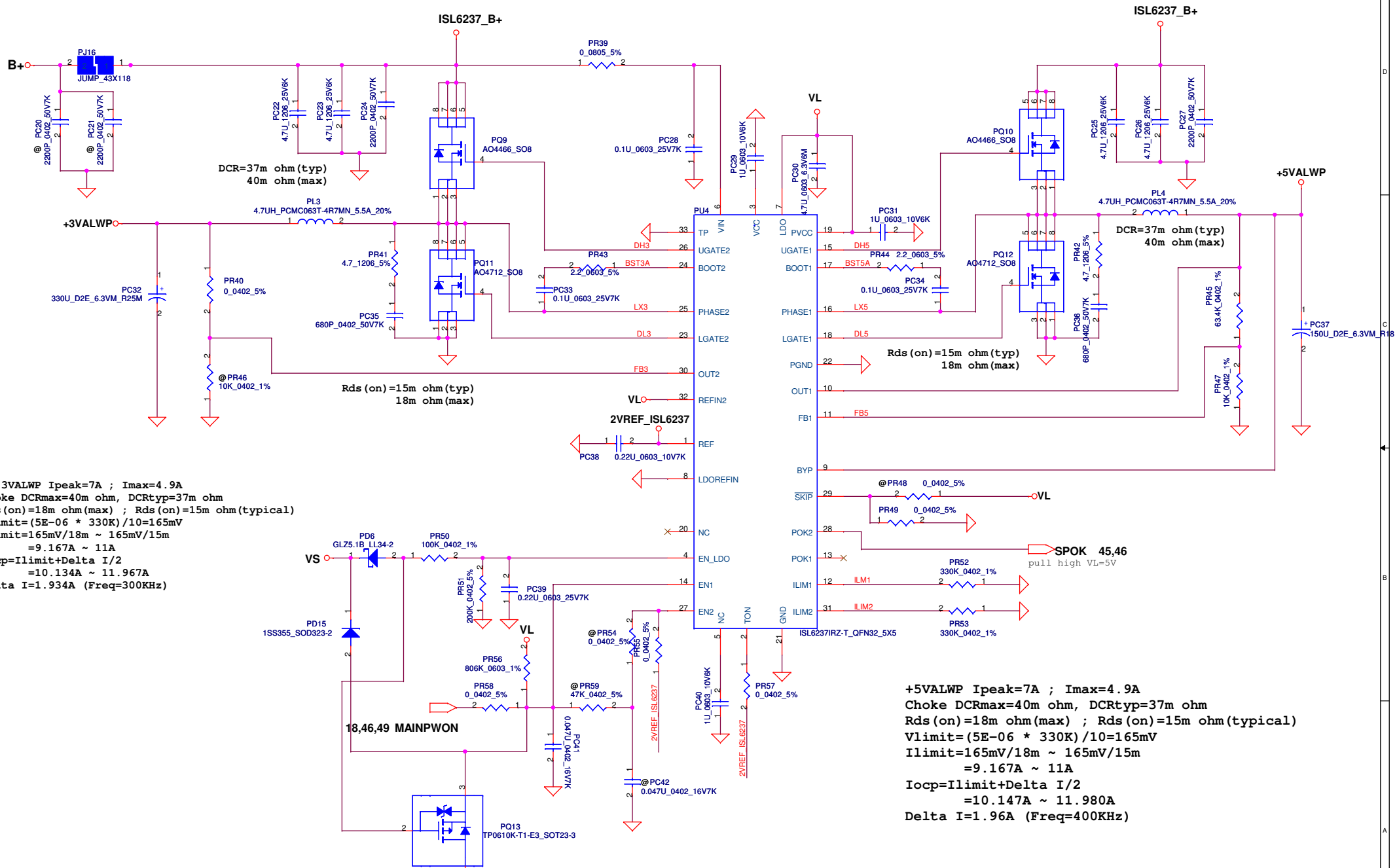


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C



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+3.3VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

18,46,49 MAINPWON

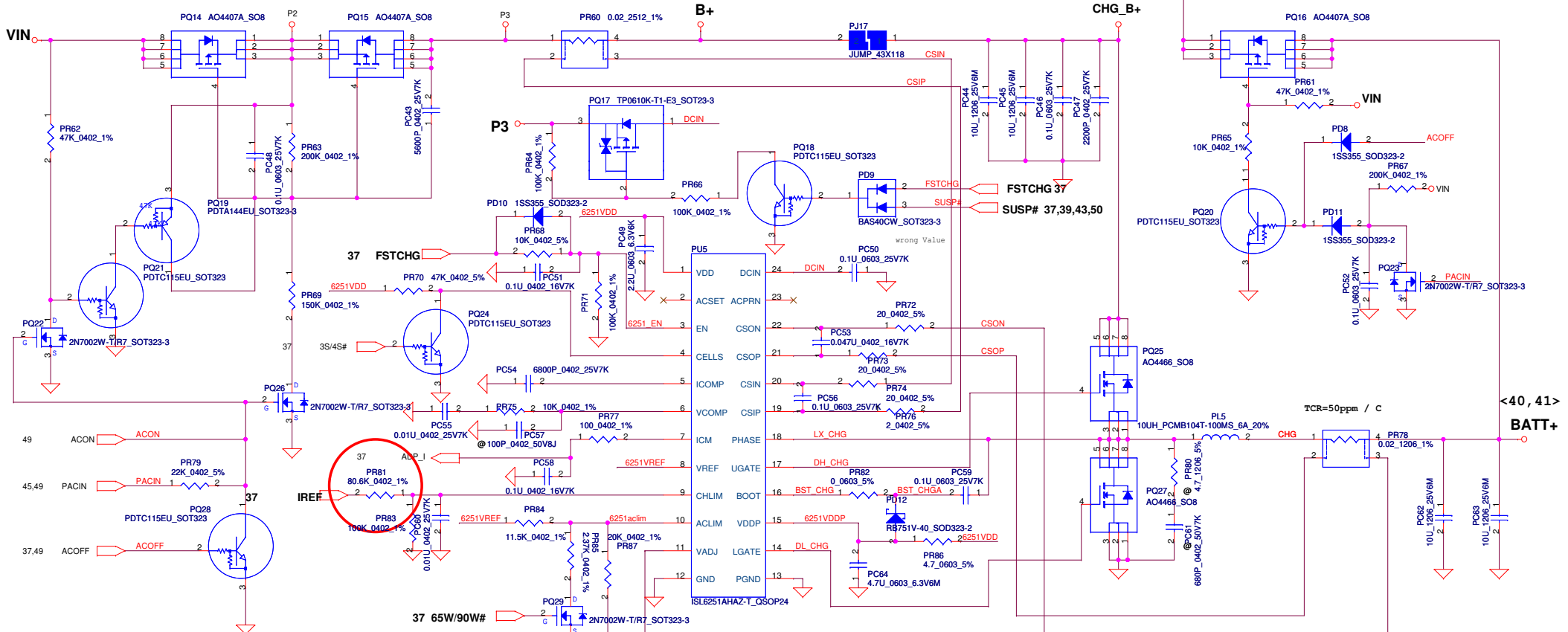
+5VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

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Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
 CP = 85%*Iada ; CP = 2.91A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

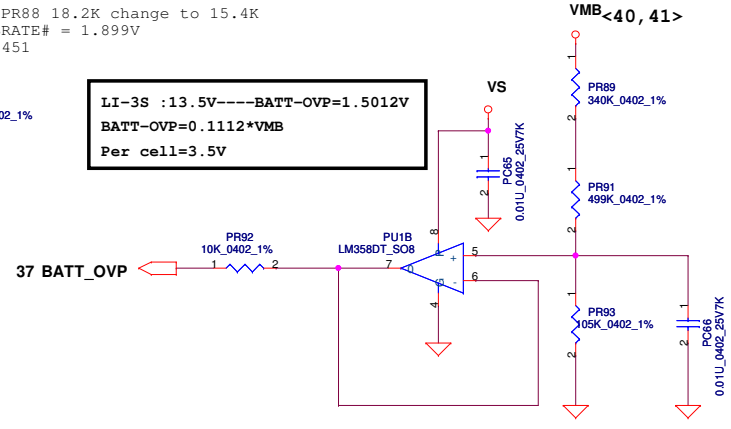
$V_{cell} = (0.175 * V_{adj}) + 3.99$

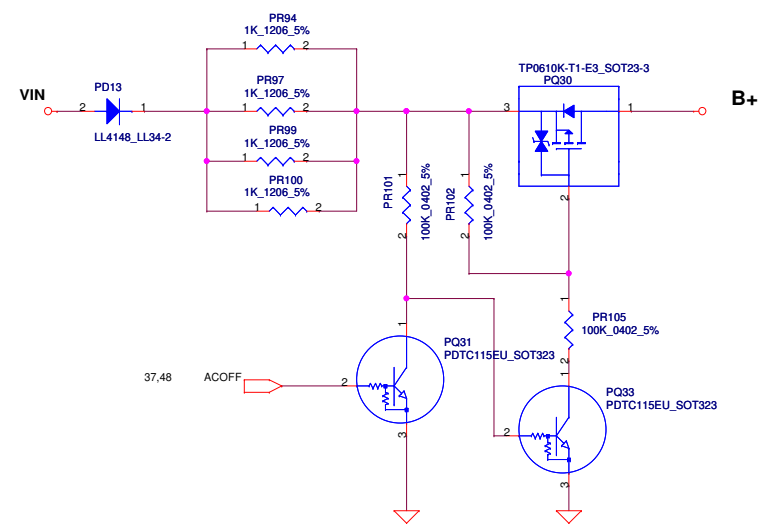
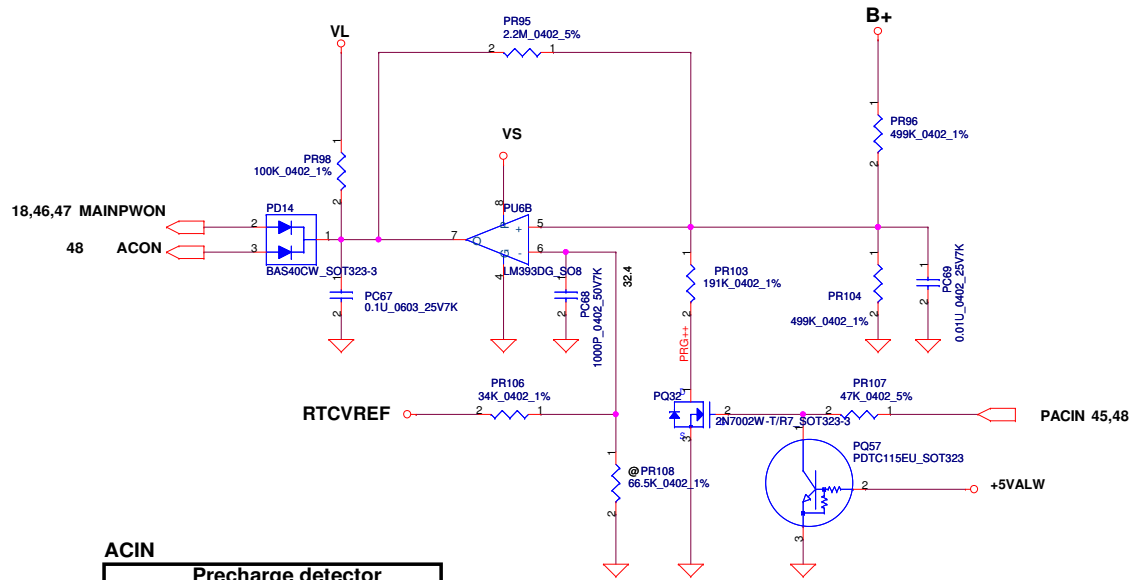
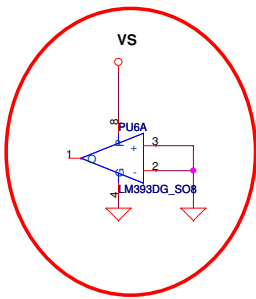
CALIBRATE#	Pre Cell
3.3V	4.35V
1.899V	4.20V

0826 PR88 18.2K change to 15.4K
 CALIBRATE# = 1.899V
 Kv=9.451

LI-3S : 13.5V --- BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V





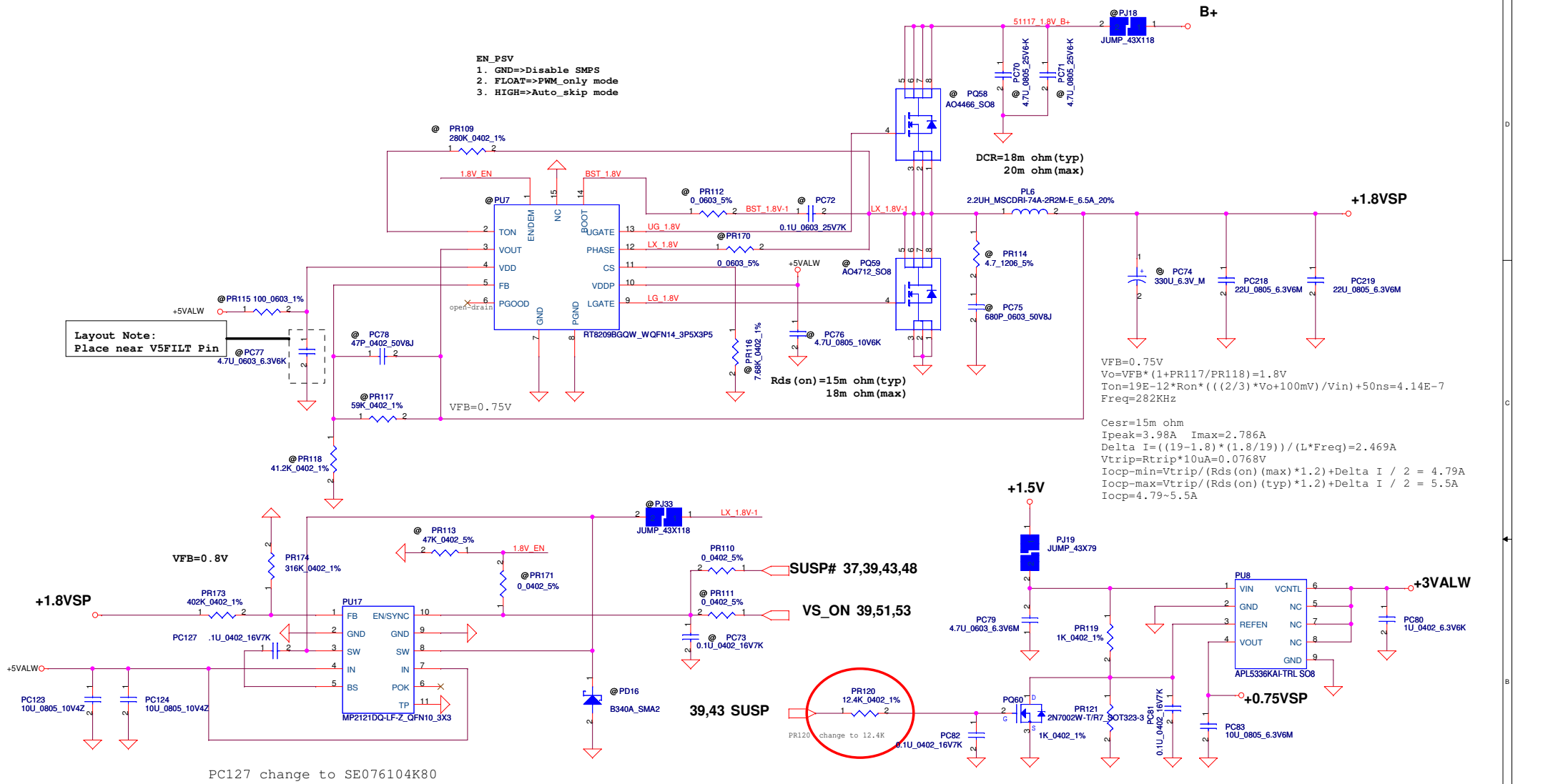
ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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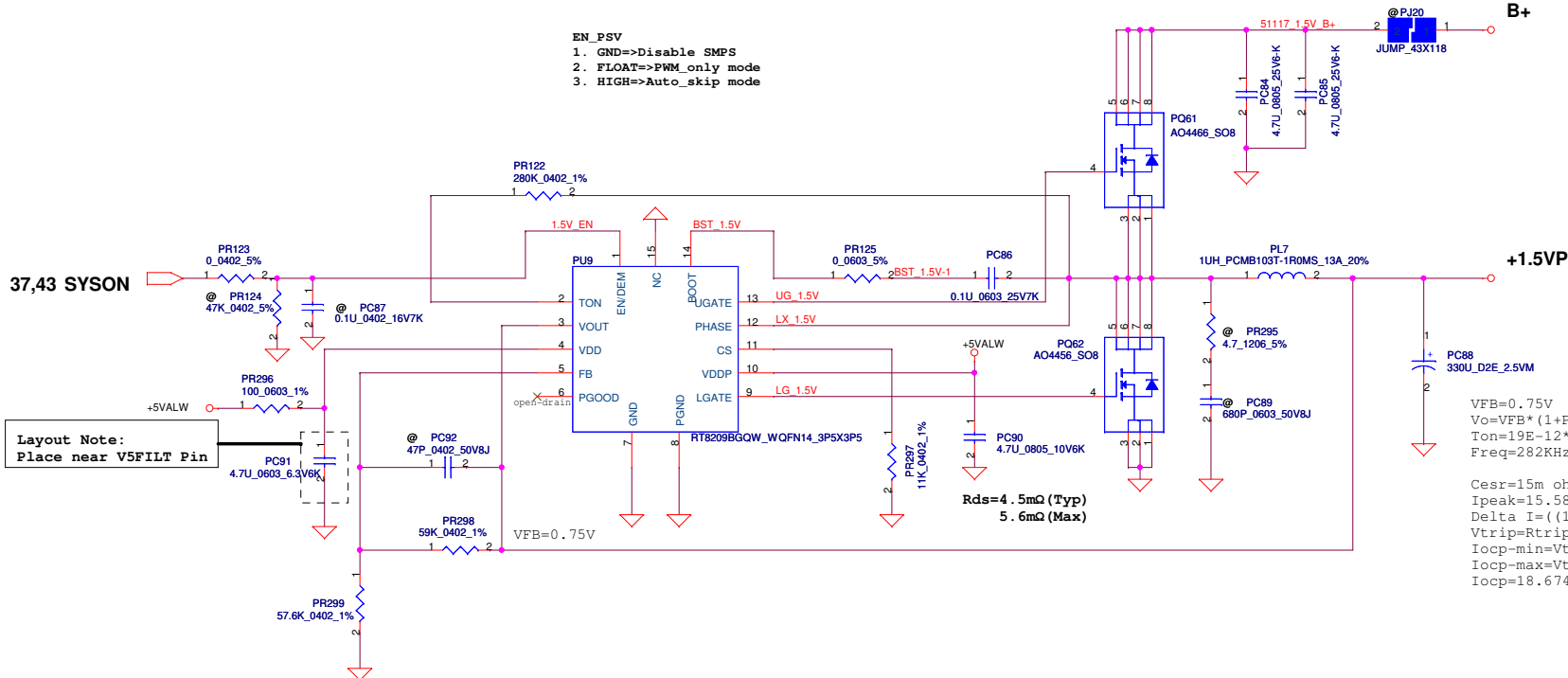


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EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

37,43 SYSON

Layout Note:
 Place near V5FILT Pin

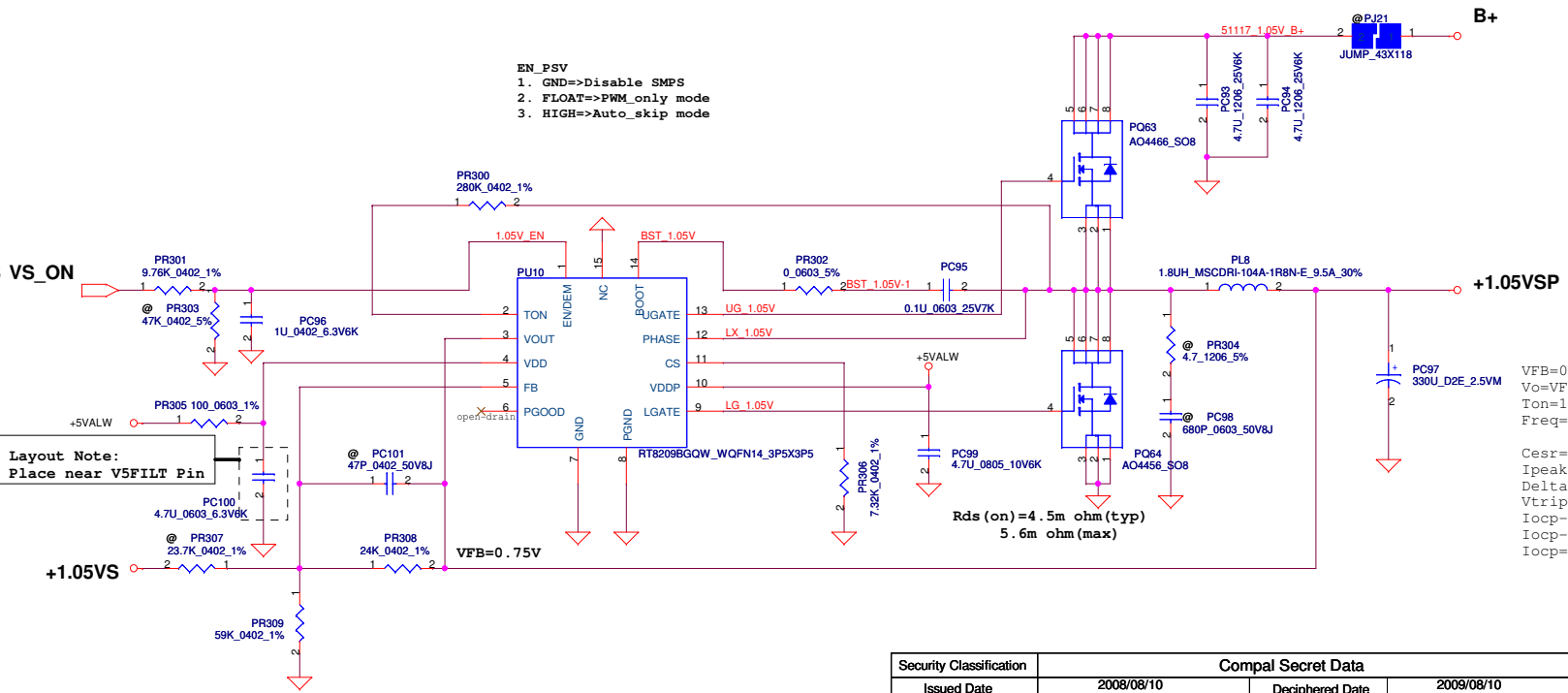


VFB=0.75V
 $V_o = VFB * (1 + PR298 / PR299) = 1.52V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / Vin + 50ns = 3.8E-7$
 Freq=282KHz (min) , 300KHz (typ)
 Cesr=15m ohm
 Ipeak=15.58A Imax=10.906A
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Freq) = 4.61A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.11V$
 $I_{ocp_min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 18.674A$
 $I_{ocp_max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 22.675A$
 $I_{ocp} = 18.674 \sim 22.675A$

EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

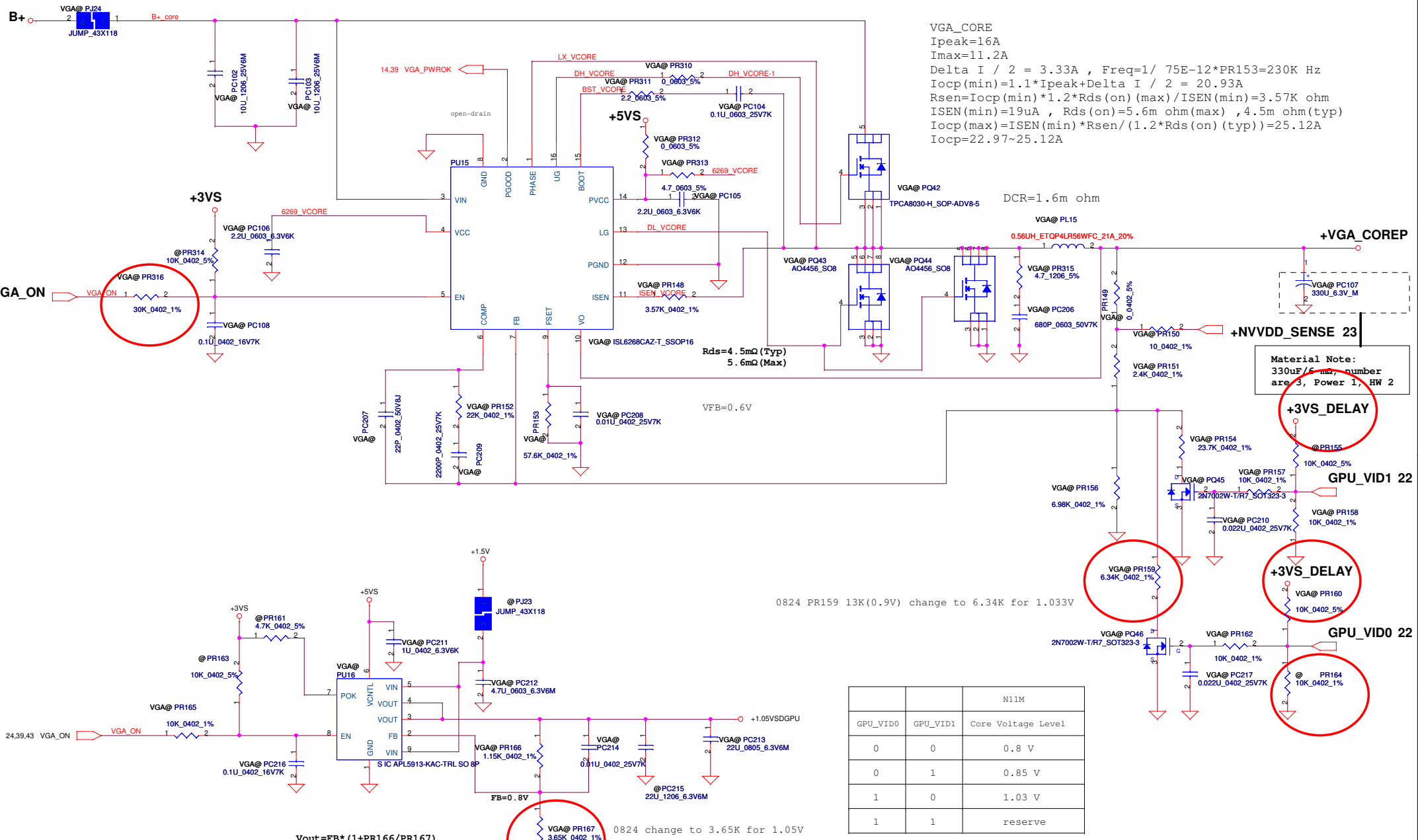
53 VS_ON

Layout Note:
 Place near V5FILT Pin



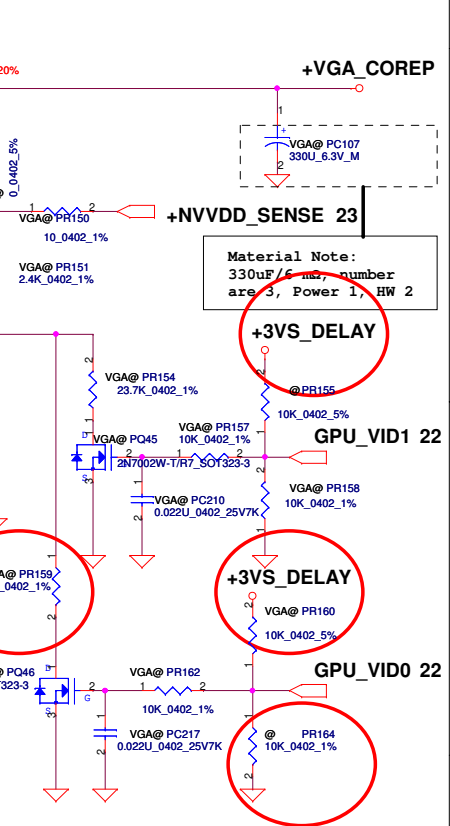
VFB=0.75V
 $V_o = VFB * (1 + PR308 / PR309) = 1.05V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / Vin + 50ns = 2.74E-07$
 Freq=282KHz , 300KHz (typ)
 Cesr=15m ohm
 Ipeak=10.9A Imax=7.63A
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Freq) = 1.837A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.0732V$
 $I_{ocp_min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 11.81A$
 $I_{ocp_max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 14.47A$
 $I_{ocp} = 11.81 \sim 14.47A$

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				1.5VP / 1.05VSP	
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		NALGO		0.1	
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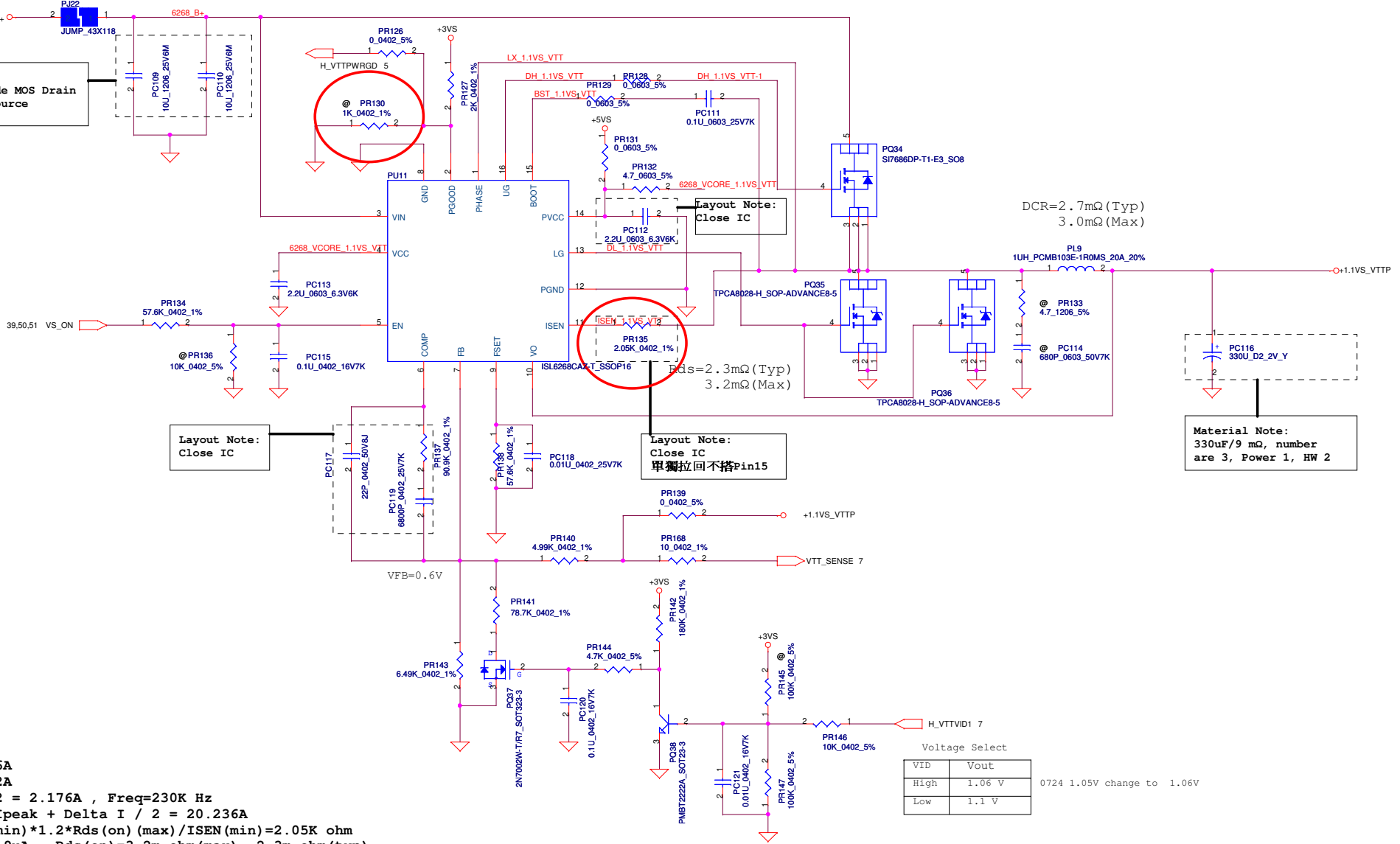


VGA_CORE
 Ipeak=16A
 Imax=11.2A
 $\Delta I / 2 = 3.33A$, Freq=1/75E-12*PR153=230K Hz
 $I_{ocp(min)} = 1.1 * I_{peak} + \Delta I / 2 = 20.93A$
 $R_{sen} = I_{ocp(min)} * 1.2 * R_{ds(on)(max)} / I_{SEN(min)} = 3.57K \text{ ohm}$
 $I_{SEN(min)} = 19\mu A$, $R_{ds(on)} = 5.6m \text{ ohm(max)}$, $4.5m \text{ ohm(typ)}$
 $I_{ocp(max)} = I_{SEN(min)} * R_{sen} / (1.2 * R_{ds(on)(typ)}) = 25.12A$
 $I_{ocp} = 22.97 \sim 25.12A$

Material Note:
 330uF/6.3V, number
 are 3, Power 1, HW 2



Layout Note:
Place near high-side MOS Drain
and low-side MOS Source



+1.1VS_VTT
 $I_{peak} = 18.06A$
 $I_{max} = 12.642A$
 $\Delta I / 2 = 2.176A$, Freq=230K Hz
 $I_{ocp(min)} = I_{peak} + \Delta I / 2 = 20.236A$
 $R_{sen} = I_{ocp(min)} * 1.2 * R_{ds(on)}(max) / I_{SEN(min)} = 2.05K \text{ ohm}$
 $I_{SEN(min)} = 19\mu A$, $R_{ds(on)} = 3.2m \text{ ohm}(max)$, $2.3m \text{ ohm}(typ)$
 $I_{ocp(max)} = I_{SEN(min)} * R_{sen} / (1.2 * R_{ds(on)}(typ)) = 28.225A$
 $I_{ocp} = 20.236 \sim 28.225A$

Layout Note:
Close IC

Layout Note:
Close IC
單獨拉回不搭Pin15

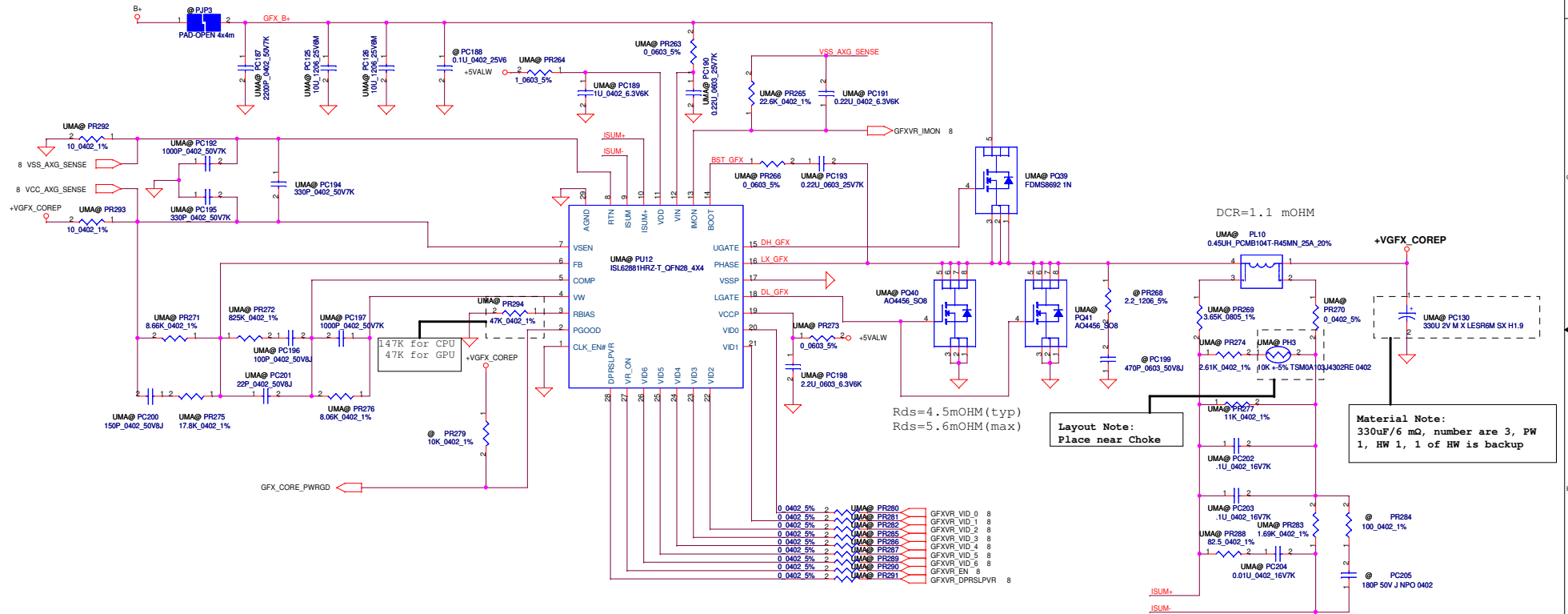
Material Note:
330uF/9 mΩ, number
are 3, Power 1, HW 2

Voltage Select	
VID	Vout
High	1.06 V
Low	1.1 V

0724 1.05V change to 1.06V

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Intel Aiburndale CPU(Integrate Graphics) I_{max}=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k\ ohm$
 $Rsum=PR269=3.65k\ ohm$
 $LL=2*Rdroop*G1*DCR/Ri=6.96m\ V/A$
 where $Rdroop=PR271=8.66k\ ohm$, $Ri=PR283=1.69k\ ohm$
 $Iocp=OCP\ Threshold*Rdroop/LL=24.89A$

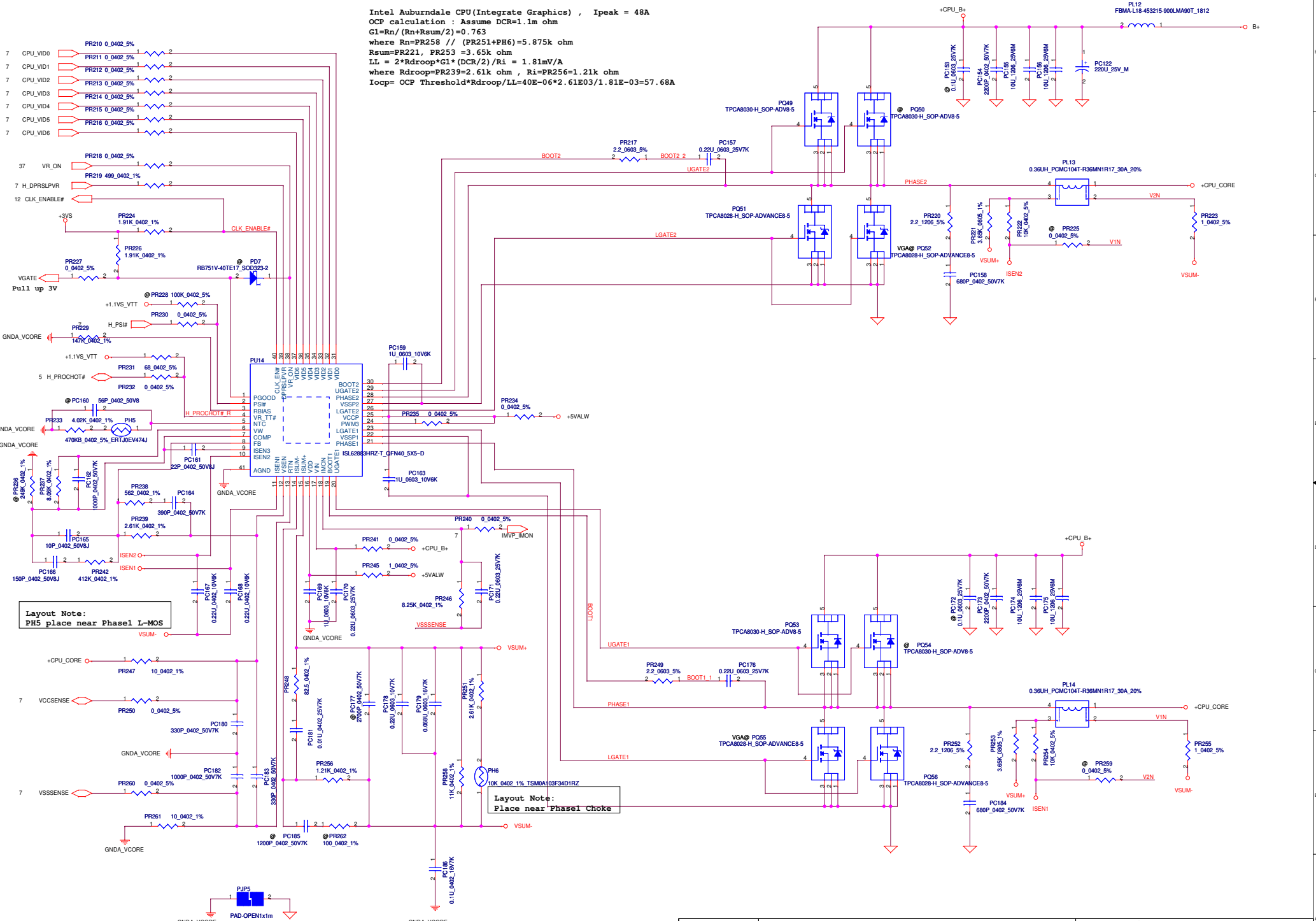


Layout Note:
Place near Choke

Material Note:
330uF/6 mΩ, number are 3, PW 1, HW 1, 1 of HW is backup

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum/2)=0.763$
 where $Rn=PR258 // (PR251+PH6)=5.875k\ ohm$
 $Rsum=PR221, PR253 =3.65k\ ohm$
 $LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A$
 where $Rdroop=PR239=2.61k\ ohm$, $Ri=PR256=1.21k\ ohm$
 $Iocp= OCP\ Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A$



Layout Note:
 PH5 place near Phase L-MOS

Layout Note:
 Place near Phase Choke

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Title	+CPU_CORE			
Size	Document Number	Rev		1
C	NALGO			0.1
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify charger circuit	design change	0.1	48	Change PR60 to SD000001F00 (0.02_2512_1%) Change PR115 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/06/23	EVT
2	Modify 1.8V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	50	Change PC77 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603) Change PR296 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/07/21	DVT
3	Modify 1.5V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Change PC91 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603) Change PR305 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/07/21	DVT
4	Modify 1.05V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Change PC100 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603) Change PR149 to SD028000080 (S RES 1/16W 0 +-5% 0402)	09/07/21	DVT
5	Modify VGA_COREP circuit	design change	0.1	52	Change PR150 to SD034100A80 (S RES 1/16W 10 +-1% 0402) Change PR139 to SD028000080 (S RES 1/16W 0 +-5% 0402)	09/06/23	EVT
6	Modify +1.1VS_VTTP circuit	design change	0.1	53	Change PR168 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
7	Modify OTP circuit	Link right component	0.1	46	Add PH1 to SL210031F00 (S THERM_ 100K +-1% TH11-4H104FT 0603)	09/06/25	EVT
8	Modify 5V/3V circuit	Delete component	0.1	47	Delete PC42 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/06/25	EVT
9	Modify 1.1VSDGPU circuit	design change	0.1	52	Change PU16, PR165, PR166, PR167, PC211, PC212, PC213, PC214, PC215, PC216 BOM structure to VGA@	09/06/26	EVT
10	Modify charger circuit	design change	0.1	48	Change PR78 to SD012200D80 (S RES 1/2W 0.02 +-1% 1206) Change PR151 to SD034240180 (S RES 1/16W 2.4K +-1% 0402)	09/06/26	EVT
11	Modify VGA_COREP circuit	design change (Voltage Level)	0.1	52	Change PR156 to SD000002680 (S RES 1/16W 6.98K +-1% 0402) Change PR154 to SD034237280 (S RES 1/16W 23.7K +-1% 0402)	09/06/30	EVT
12	Modify VGA_COREP circuit	design change (Voltage Level)	0.1	52	Change PR159 to SD034130280 (S RES 1/16W 13K +-1% 0402) Change PQ6 to SB000006800 (S TR 2N7002W T/R7 1N SOT-323)	09/06/30	EVT
13	Modify OTP circuit	design change	0.2	46	Add PR169 to SD034100480 (S RES 1/16W 1M +-1% 0402)	09/07/13	DVT
14	Modify 1.5VP circuit	design change	0.2	51	Change PL7 to SH000009U00 (S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A)	09/07/20	DVT
15	Modify VGA_COREP circuit	design change	0.2	52	Change PR153 to SD034576280 (S RES 1/16W 57.6K +-1% 0402) Change PQ35 to SB000006L00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
16	Modify +1.1VS_VTTP circuit	design change	0.2	53	Change PQ36 to SB000006L00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
17	Modify VGA_COREP circuit	design change	0.2	52	Change PC107 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)	09/07/20	DVT
18	Modify 1.8V circuit	design change	0.2	50	Change PC74 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU) and BOM structure to @	09/07/20	DVT
19	Modify CPU circuit	design change	0.2	55	Change PR226 to SD000009080 (S RES 1/16W 1.91K +-1% 0402)	09/07/20	DVT
20	Modify +1.1VS_VTTP circuit	design change	0.2	53	Change PC116 to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	09/07/21	DVT
21	Modify CPU circuit	design change	0.2	55	Change PC179 to SE026683K80 (S CER CAP .068U 16V K X7R 0603) Change PC53 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/07/22	DVT
22	Modify charger circuit	design change	0.2	48	Change PC64 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT
23	Modify 1.1VSDGPU circuit	design change	0.2	52	Change PC212 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Modify GFX_COREP circuit	design change	0.2	54	Change PC189 to SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	09/07/22	DVT
25	Modify 1.8V circuit	design change	0.2	50	Add PR170 to SD013000080 (S RES 1/10W 0 +-5% 0603)and BOM structure to @ Change PR109, PR117, PC72, PQ58, PQ59 BOM structure to @	09/07/28	DVT
26	Modify 1.8V circuit	design change	0.2	50	Add PUI7 to SA00003KL00(S IC MP2212DQ-LF-Z QFN 10P PWM) Add PD16 to SC500001I80(S SCH DIO B340A SMA VISHAY) BOM structure to @ Add PR173 to SD034402380(S RES 1/16W 402K +-1% 0402)	09/07/28	DVT
27	Modify 1.8V circuit	design change	0.2	50	Add PR174 to SD034316380(S RES 1/16W 316K +-1% 0402) Add PR171 to SD028000080(S RES 1/16W 0 +-5% 0402)BOM structure to @ Add PR113 to SD028470280(S RES 1/16W 47K +-5% 0402)	09/07/28	DVT
28	Modify 1.8V circuit	design change	0.2	50	Add PC123, PC124 to SE053106Z80(S CER CAP 10U 10V Z Y5V 0805) Add PC127 to SE076103K80(S CER CAP .01U 16V K X7R 0402) Add PC218, PC219 to SE000000I10(S CER CAP 22UF 6.3V M X5R 0805 H1.25)	09/07/28	DVT
29	Modify 1.8V circuit	design change	0.2	50	Add PR41, PR42 to SD001470B80(S RES 1/4W 4.7 +-5% 1206)	09/07/28	DVT
30	Modify 5V/3V circuit	add snubber(PR42 PC36), (PR41 PC35) add boost PR43, PR44	0.2	47	Add PC35, PC36 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR43, PR44 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
31	Modify VGA_COREP circuit	add snubber(PR315 PC206) add boost PR311	0.2	52	Add PR311 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)and BOM structure to V6A@ Change PR315 PC206 BOM structure to V6A@	09/07/28	DVT
32	Modify CPU circuit	add snubber(PR220 PC158), (PR252 PC184) add boost PR217, PR249	0.2	55	Add PR220, PR252 to SD011220B80(S RES 1/4W 2.2 +-5% 1206) Add PC158, PC184 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR217, PR249 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
33	Modify +1.1VS_VTTP circuit	design change	0.2	53	Change PR141 to SD034787280(S RES 1/16W 78.7K +-1% 0402) Change PR143 to SD034649180(S RES 1/16W 6.49K +-1% 0402)	09/07/28	DVT
34	Modify OTP circuit	design change	0.2	46	Change PH1 to SL200000U00(S THERM_100K +-1% TSMOB104F4251RZ 0402) Change PH2 to SL200000U00(S THERM_100K +-1% TSMOB104F4251RZ 0402)	09/07/28	DVT
35	Modify +1.1VS_VTTP circuit	design change (OCP)	0.2	53	Change PR135 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/07/29	DVT
36	Modify GFX_COREP circuit	design change	0.2	54	Change PH3 to SL200000Y00(10K +-5% TSM0A103J4302RE 0402)	09/07/29	DVT
37	Modify CPU circuit	design change	0.2	55	Change PH6 to SL200000W00(10K +-1% TSM0A103F34D1RZ 0402)	09/07/29	DVT
38	Modify 1.5V circuit	Change to 3mm height choke for thermal issue	0.2	51	Change PL7 to SH00000AB00(S COIL 1UH +-20% PCMB103T-1R0MS 13A)	09/08/06	DVT
39	Modify VGA_COREP circuit	design change (GS sample define 1.03V, +1.05VSDGPU Vo=1.05V)	0.3	52	Change PR159 to SD034634180(S RES 1/16W 6.34K +-1% 0402) Change PR167 to SD034365180(S RES 1/16W 3.65K +-1% 0402)	09/08/24	PVT
40	Modify 1.8V circuit	design change	0.3	50	Change PC127 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	09/08/24	PVT
41	Modify charger circuit	design change	0.3	48	Change PR88 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR81 to SD034154380(S RES 1/16W 154K +-1% 0402)	09/08/26	PVT
42	Modify VGA_COREP circuit	design change	0.3	52	Change PR160 BOM structure to V6A@ VID pull high voltage change to +3VS_DELAY	09/09/03	PVT
43	Modify +1.1VS_VTTP circuit	design change	0.3	53	Change PR130 BOM structure to @	09/09/03	PVT
44	Modify 0.75V circuit	design change	0.3	50	Change PR120 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/09/11	PVT
45	Modify VGA_COREP circuit	design change	0.3	52	Change PR316 to SD034300280(S RES 1/16W 30K +-1% 0402) Change PR164 BOM structure to @	09/09/11	PVT
46	Modify +1.1VS_VTTP circuit	design change	0.3	53	Change PR135 to SD034205180(S RES 1/16W 2.05K +-1% 0402)		

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
47	Modify OTP circuit	design change	0.3	46	Change PR23 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402) Change PR26 to SD034158280(S RES 1/16W 15.8K +-1% 0402)	09/09/14	PVT
48	Modify 1.8V circuit	design change	0.3	50	Change PL6 to SH000009Q00(S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A)	09/09/16	PVT
49	Modify 5V/3V circuit	design change	0.3	47	Change PU4 to SA00001TN00(S IC ISL6237IRZ-T QFN 32P)	09/09/16	PVT
50	Modify 0.75V circuit	design change	0.3	50	Change PR120 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)	09/10/08	PVT
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				4	R72 bom structure	7/23	0.2
2				5	reserve R735	7/23	0.2
3				8	rename CPU VDDQ from +1.5V to +1.5V_CPU	7/23	0.2
4				8	R146 BOM structure	7/23	0.2
5				11	reserve S3 power consumptiosn circuit	7/23	0.2
6				12	change Y1 Y4 Y6 footprint	7/23	0.2
7				13	add ME_EN# from EC to PCH	7/23	0.2
8				14	pop Y6,C254,C255 , and project ID pin	7/23	0.2
9				17	change USB port 8 to port 1 , port 2 to port 8	7/23	0.2
10				18	GPIO35 pin(VGa presetnt) modfiy	7/23	0.2
11				19	R605 and R628 BOM structure modify	7/23	0.2
12				22	add VGA thermal sensor from EC to VGA	7/23	0.2
13				23	pop R479,del R491	7/23	0.2
14				29	L29~L34 change from 0805 to 0603	7/23	0.2
15				30	Q45,Q47 gate voltage change from +3VS to +3VS_delay	7/23	0.2
16				37	change R306 to 8.2K, add D29, rename EC_MUTE	7/23	0.2
17				38	Jfun1 pin3 change form KSO1 to KSO3	7/23	0.2
18				39	del SW2	7/23	0.2
19				41	change R333, R336 to 39k,15k, add R681,C707	7/23	0.2
20				43	reserve Q58,Q59,R728,R326, change U26,R688	7/23	0.2
21				24	reserve C710	7/23	0.2
22				28	reserve U44,U45	7/23	0.2
23				19	update L7,L8,L10,L11 footprint	7/23	0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				30	pop R248, R271,R265	7/23	0.2
2				7	pop C165, del C170	7/23	0.2
3				18	unpop R532, R86	7/23	0.2
4				5	add R472 and C713	8/31	0.3
5				11	add C714	8/31	0.3
6				12	add C715	8/31	0.3
7				17	USB20 port 6 change to USB20 port 9	8/31	0.3
8				24	3VS_delay related circuit	8/31	0.3
9				30	del R236,C257 , pop R254,C268 in all sku	8/31	0.3
10				33	unpop R3 , U1, pop R6 , change R306 to 18K	8/31	0.3
11				37	ME_EN change from U25,75 to U25.16	8/31	0.3
12				29	pop Q6,Q7 in all sku	8/31	0.3
13				29	change L29~L34 footprint	8/31	0.3
14				41	del D25,D26,D27	8/31	0.3
15				43	update C705,C706 BOM structure	8/31	0.3
16				14	unpop R112	8/31	0.3
17				7	change C165 p/n	8/31	0.3
18				40	pop C353	9/10	0.3
19					change R157,R527,R570,R575,R582,R634,R239,R64 to 0 ohm		0.3
20				5	add R746,R747	9/10	0.3
21				12	U27 clk gen change to siligo	9/10	0.3
22				40	del C371,C372	9/10	0.3
23				3	Modify BOM Config add S3@ on all SKU	10/20	1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				14	Change R209,C254,C255,Y6 BOM config to UMA@	10/20	1.0
2				19	Added C257	10/20	1.0
3				22	Change N11 to A2 (P/N SA00003HZ10)	10/20	1.0
4				22	Added R748 and R749 as I2C pull high resistor.	10/20	1.0
5				22	Pop R36,R37 as DIS@	10/20	1.0
6				28	Change Q11,Q19 BOM config to SG@	10/20	1.0
7				28	Change R502,R484 BOM config to DIS only@	10/20	1.0
8				37	Change R306 to 33k(Board ID)	10/20	1.0
9				38	Change LED9 PN to SC5191UD00	10/20	1.0
10				43	Change R296 to 47K,R295 to 470	10/20	1.0
11				44	Change LED Resistors:	10/20	1.0
12					R373 to 243,R381 and R383 to 100,R377 to 243,		
13					R375 and R376 to 470,R349 to 100,R350 to 191		
14					R304 to 499		1.0
15				17	Change C256 to 22u	10/22	
16				18	ADD R750 10K pull hig resistor	10/22	1.0
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