

Compal Confidential

NCWGO/H0 Schematics Document

AMD S1g1 / RS780MN/ SB710

2009 / 05 / 19

LA-5481

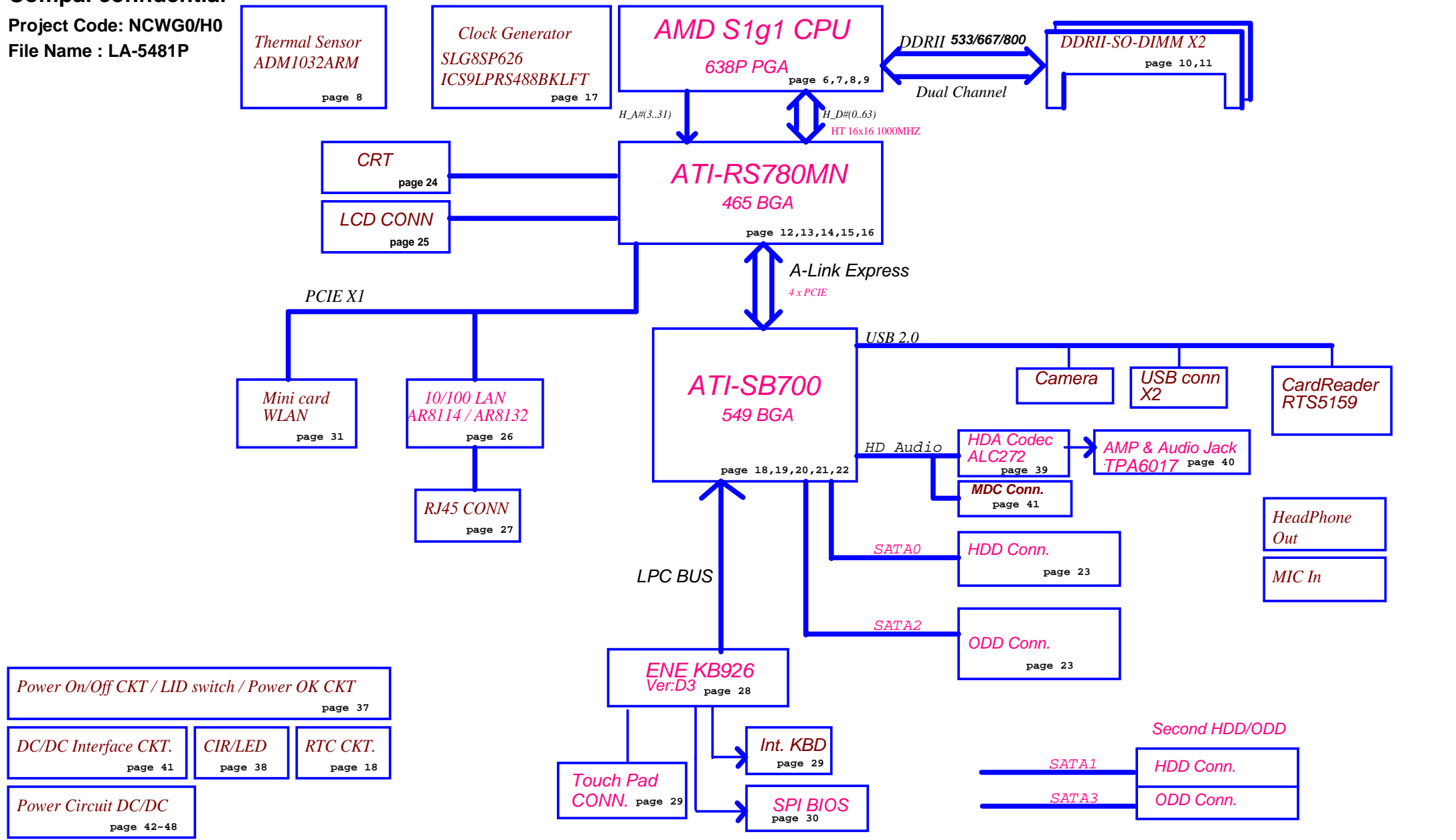
Rev:0.2

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				Date	Wednesday, May 20, 2009	Sheet 1 of 47

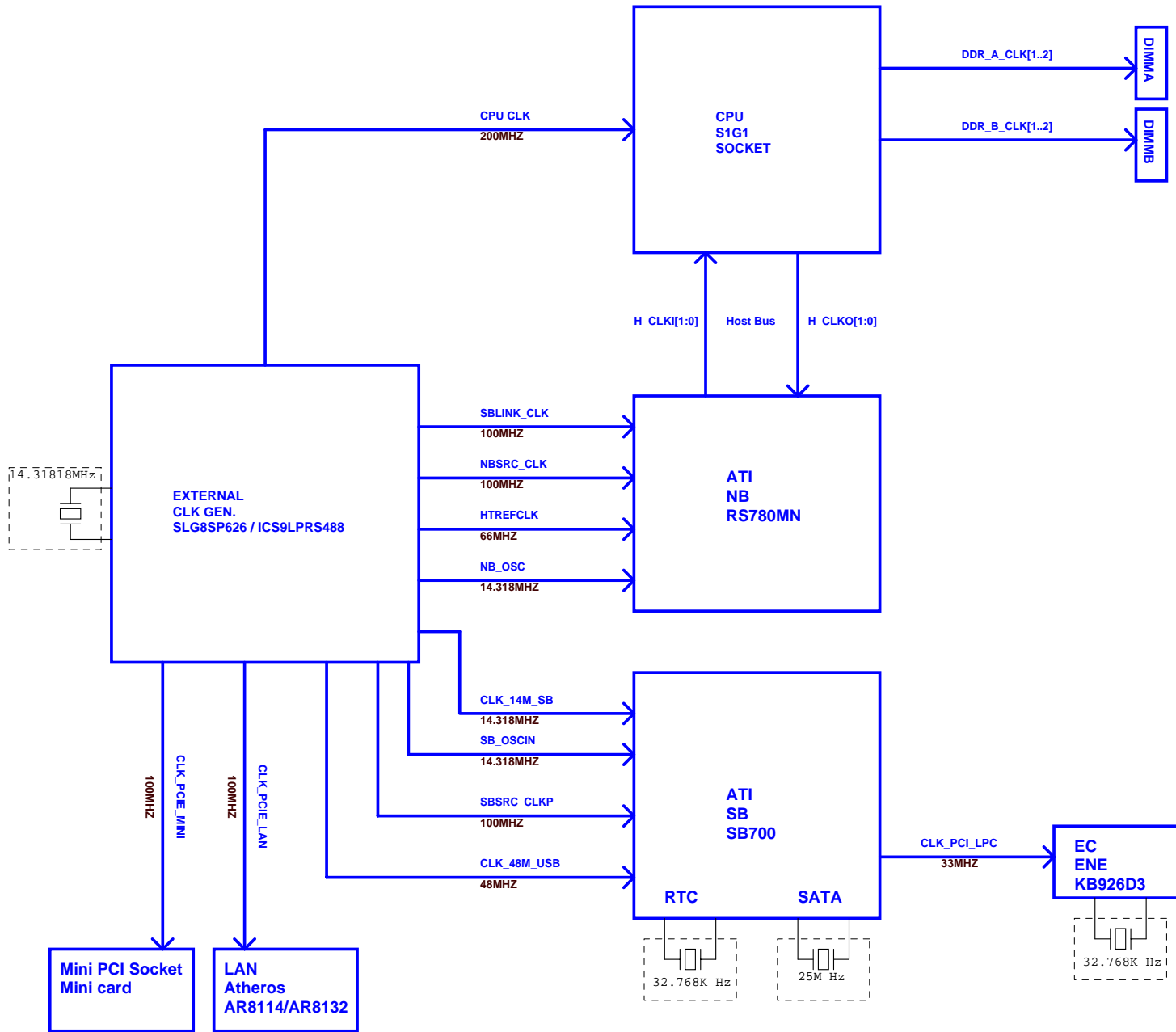
Compal confidential

Project Code: NCWG0/H0

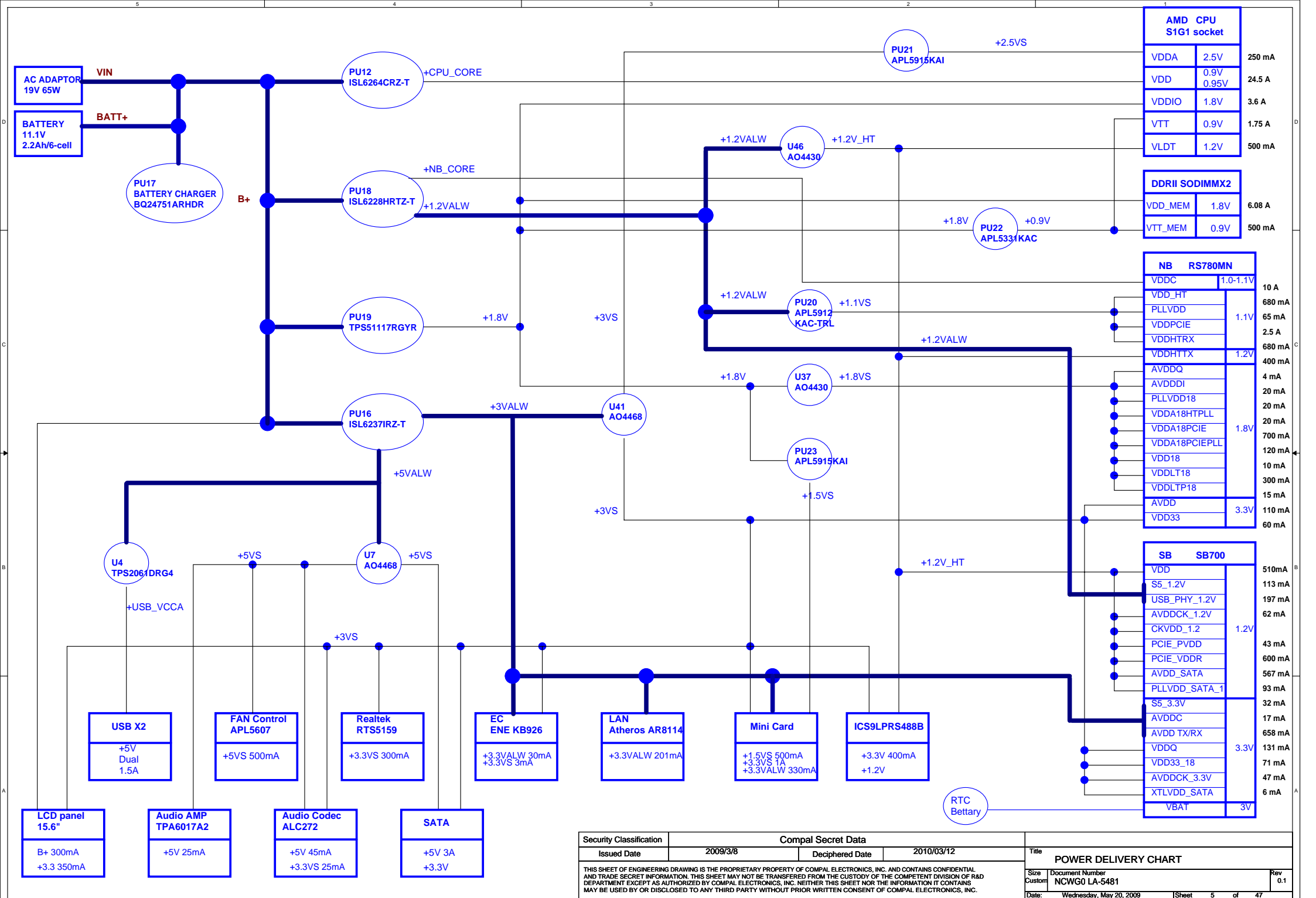
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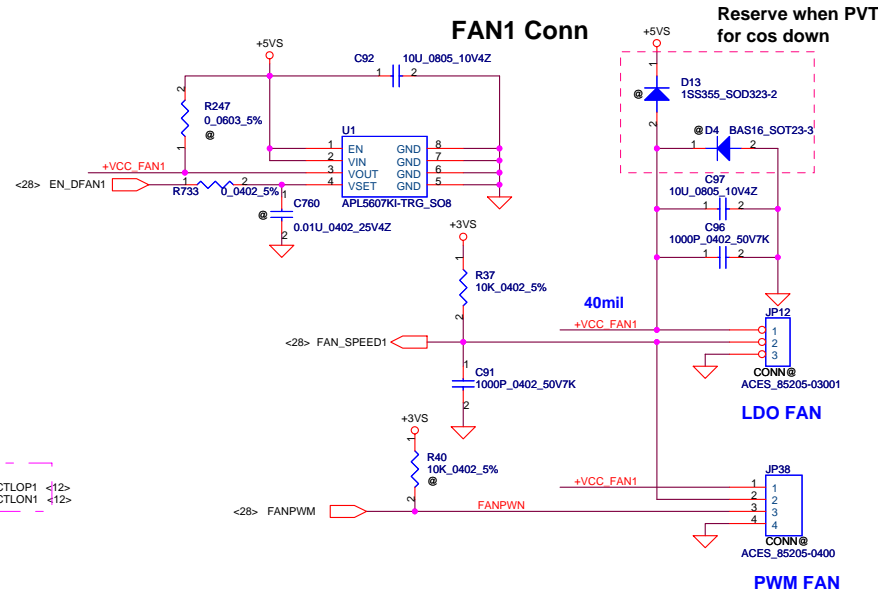
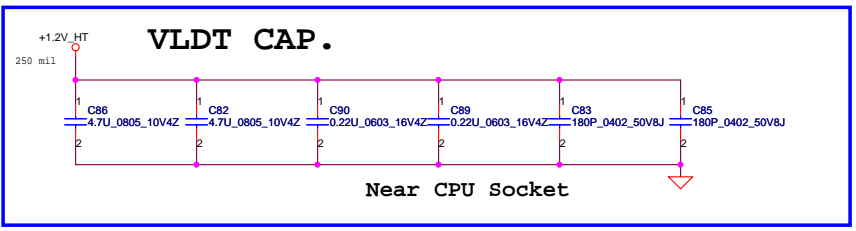
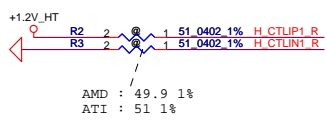
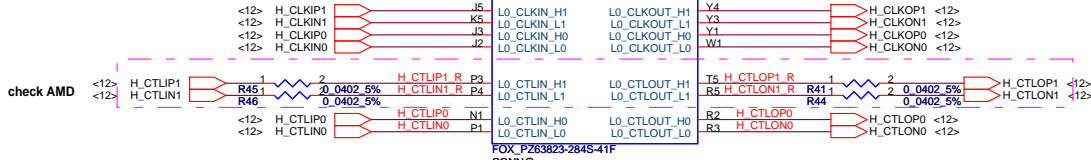
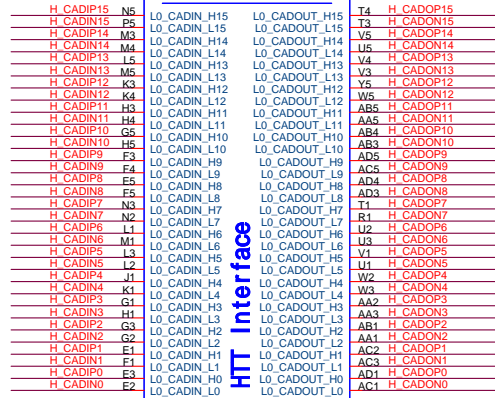
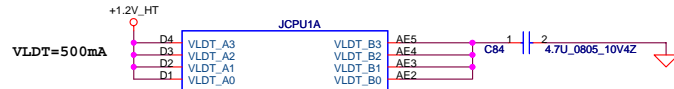
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				Date:	Wednesday, May 20, 2009
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				Date:	Wednesday, May 20, 2009
				Sheet	4 of 47
				Rev	0.1

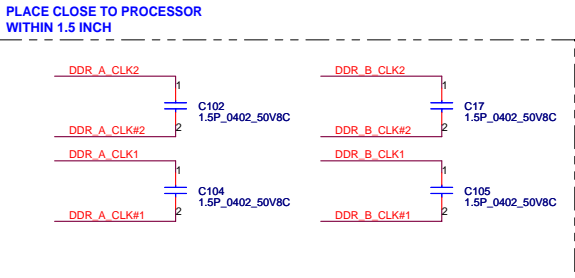
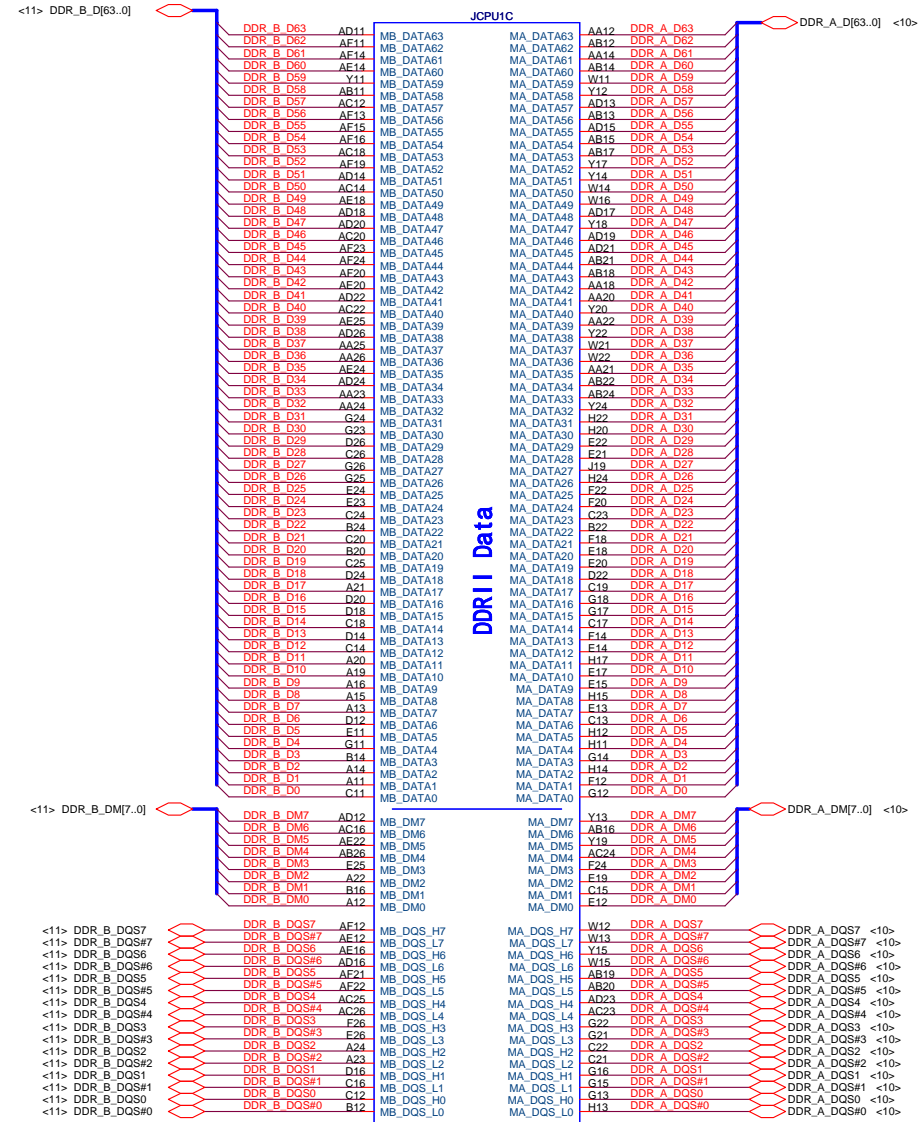
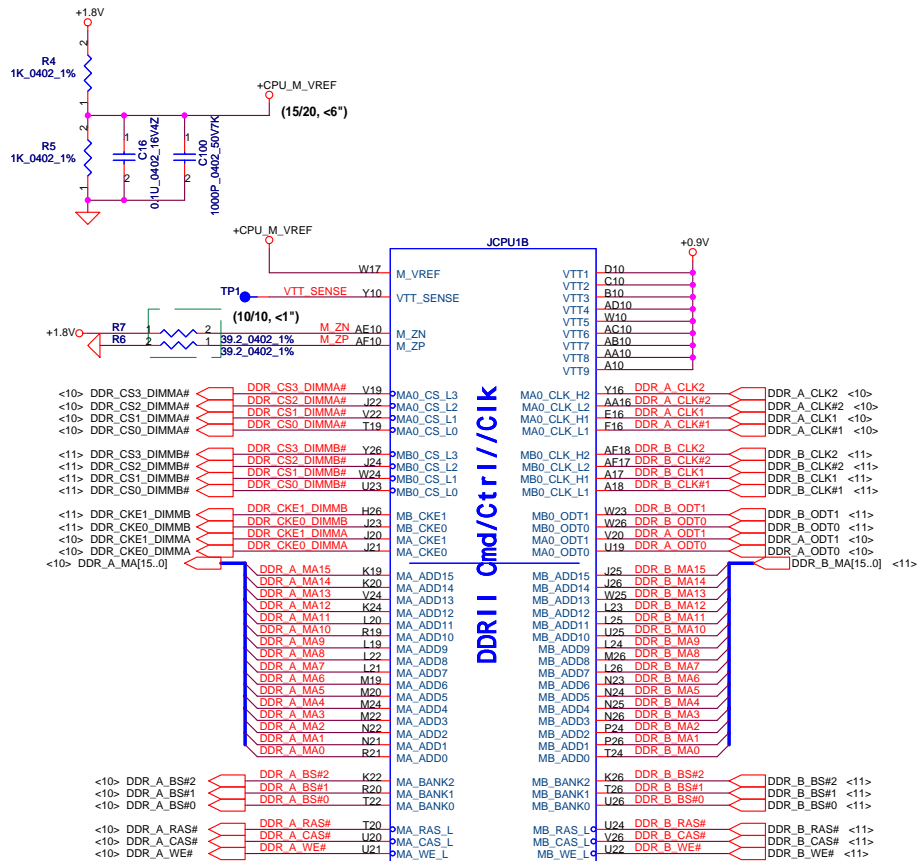


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Customer	Document Number	Date	Sheet	of	47
NCWGO LA-5481	Wednesday, May 20, 2009	5	47		

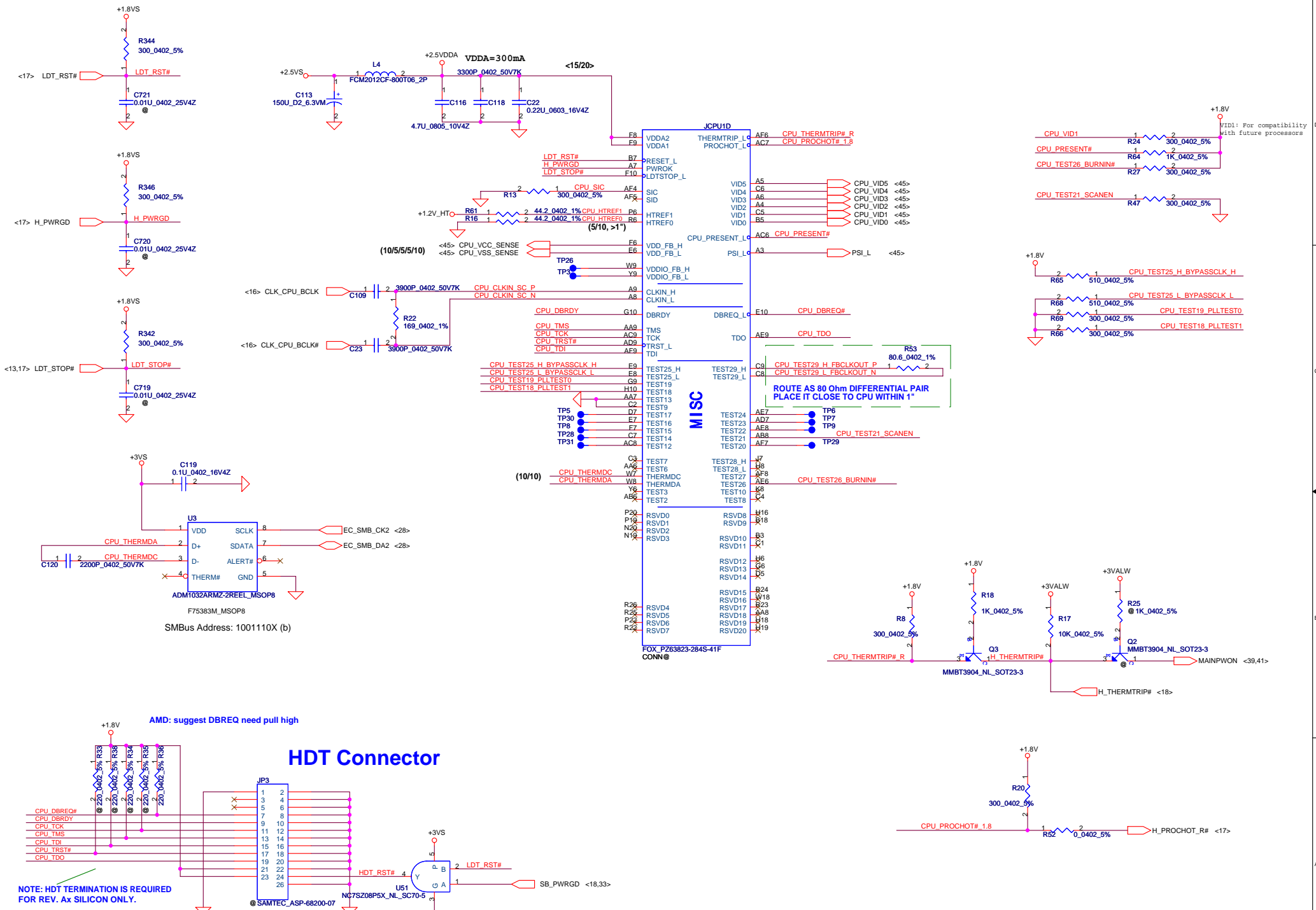


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				Customer	NCWGO LA-5481
				Date:	Wednesday, May 20, 2009
				Sheet	6 of 46
				Rev	0.1

Processor DDR2 Memory Interface

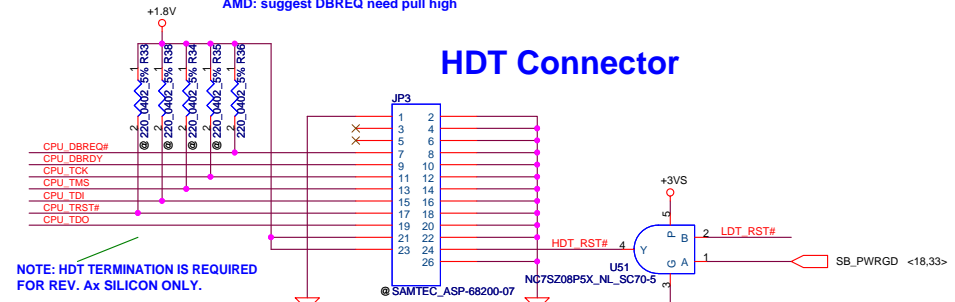


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		Date: Wednesday, May 20, 2009		Rev 0.1
		Sheet 7 of 46		



AMD: suggest DBREQ need pull high

HDT Connector

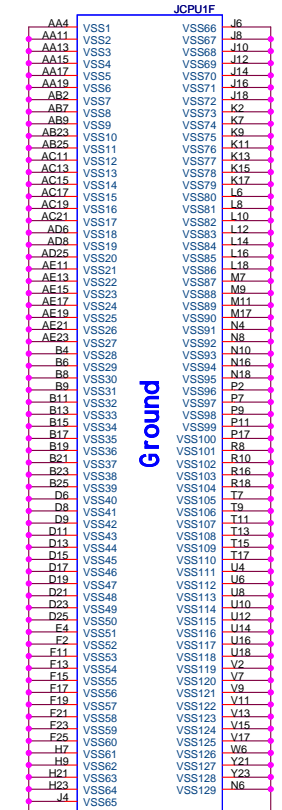
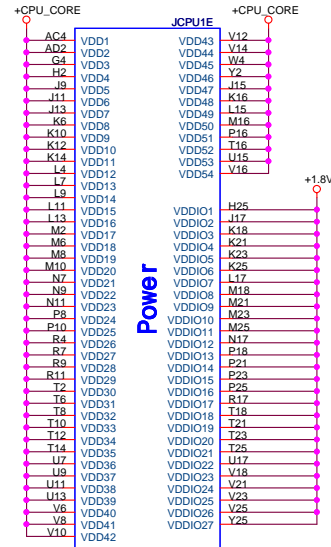
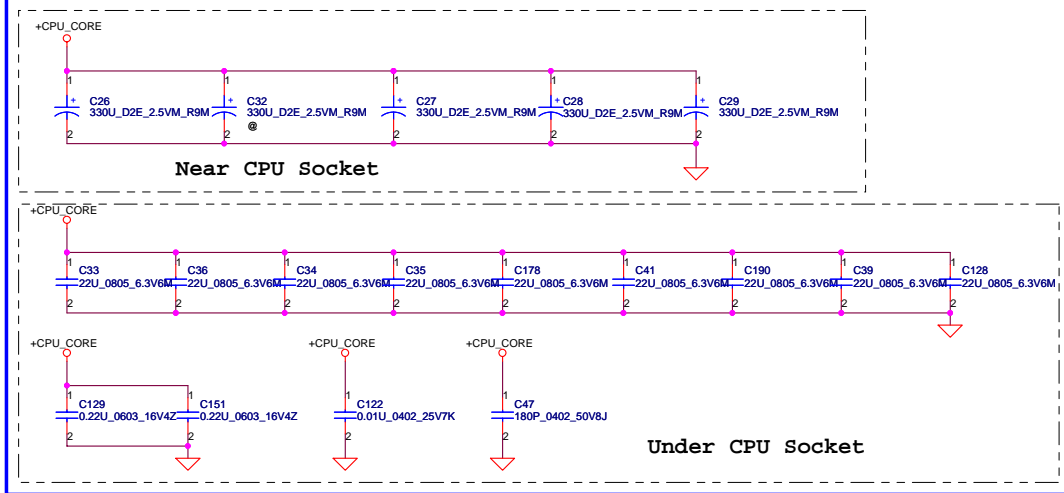


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Size	Document Number	Rev	
Custort	NCWG0 LA-5481	0.1	
Date:	Wednesday, May 20, 2009	Sheet	8 of 46

Compal Electronics, Inc.

Sig1 CTRL

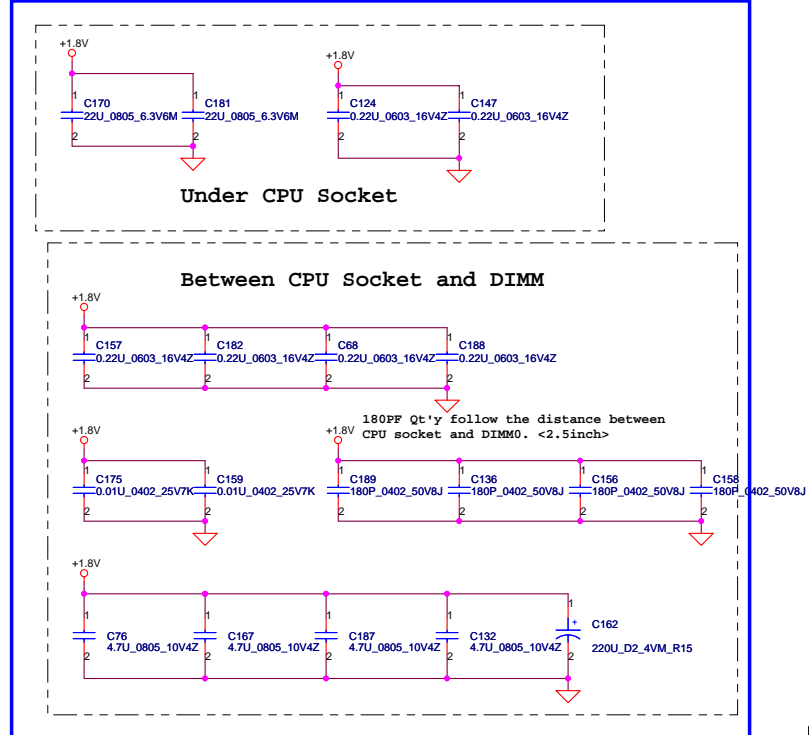
VDD(+CPU_CORE) decoupling.



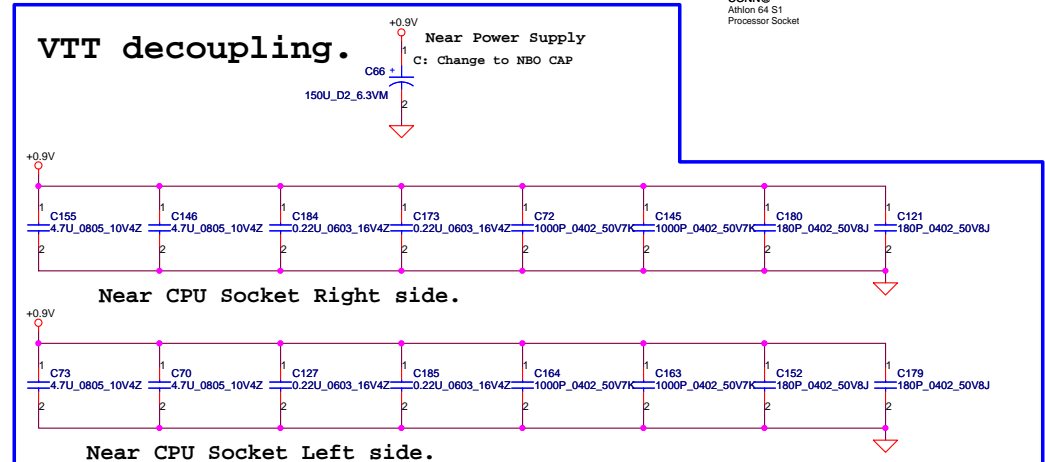
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CONN@
Arlton 64 S1
Processor Socket

FOX_PZ63823-284S-41F
CONN@
Arlton 64 S1
Processor Socket

VDDIO decoupling.



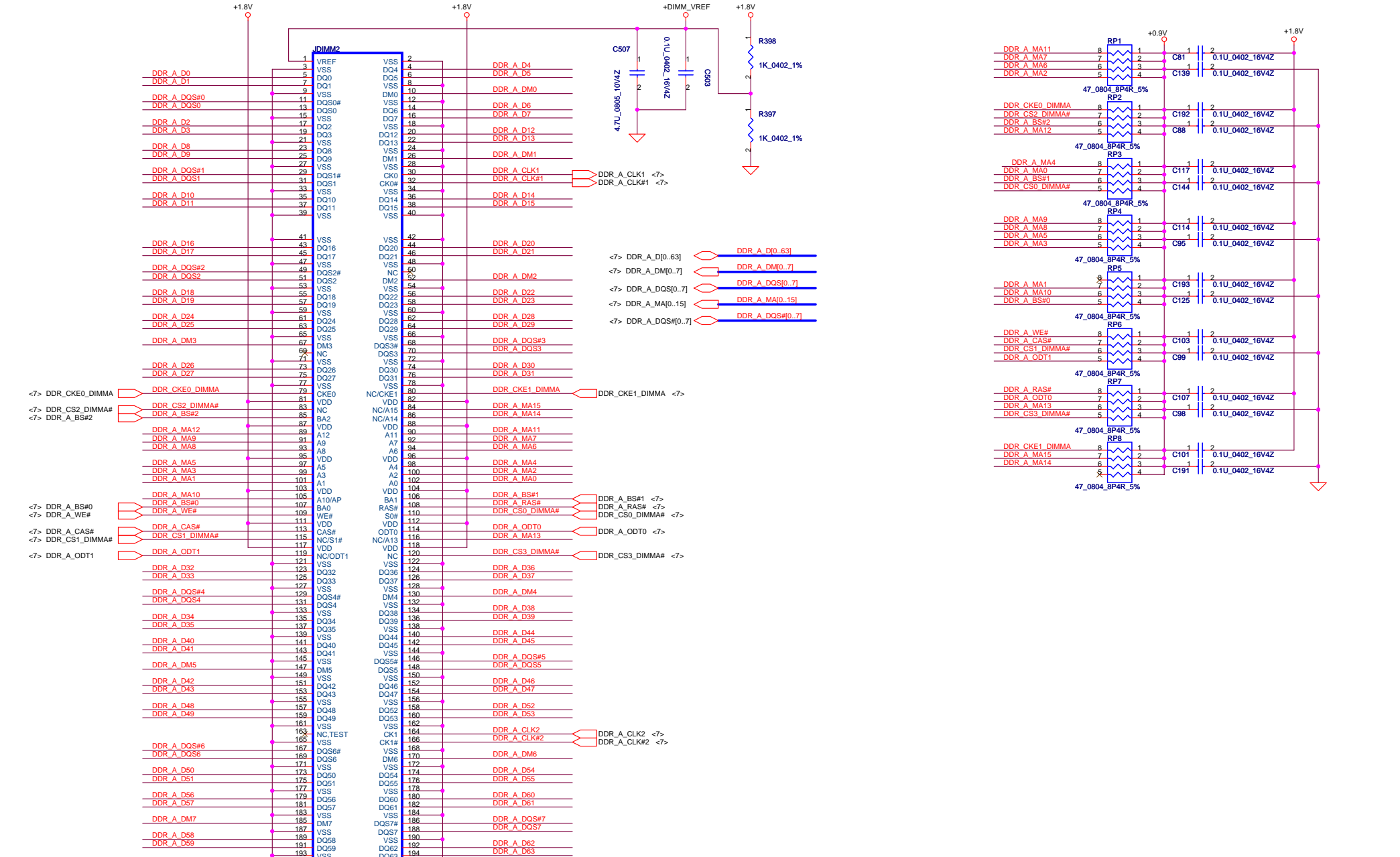
VTT decoupling.



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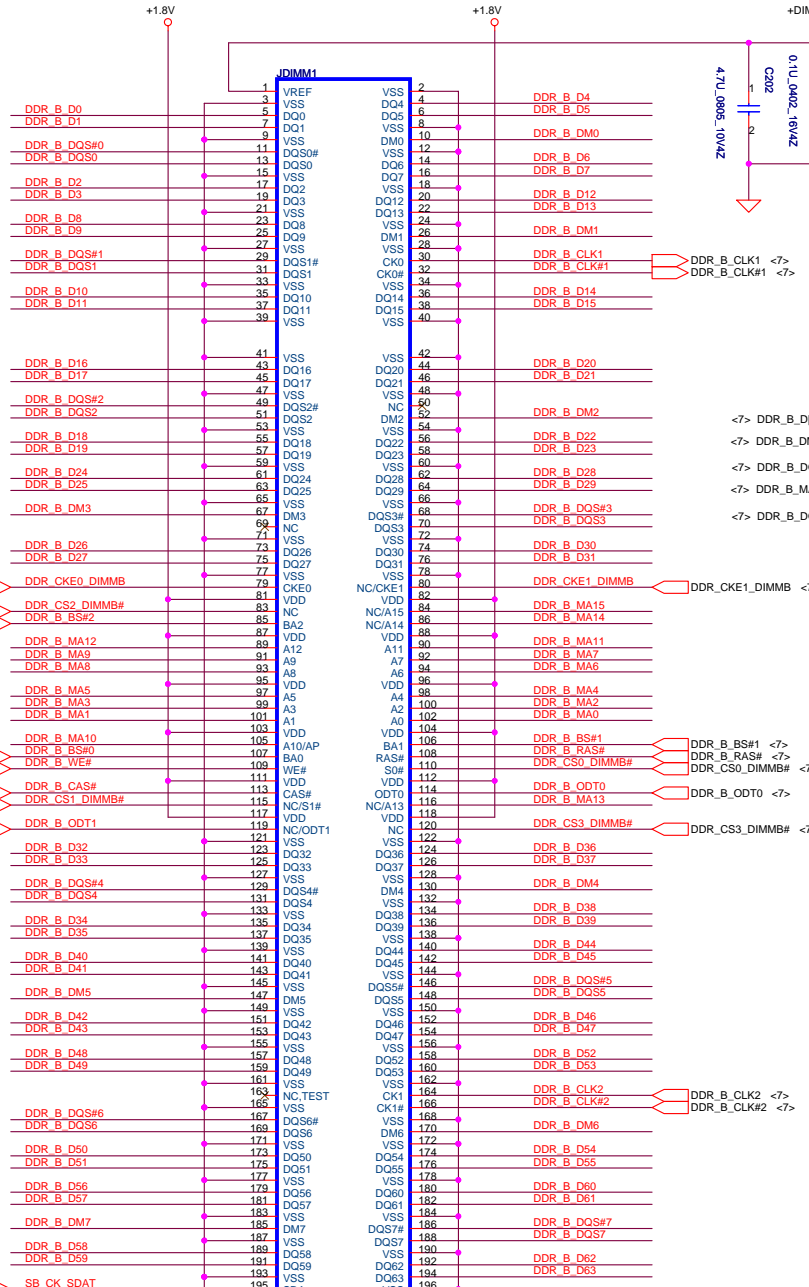
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S1g1 PWR & GND		Size	Document Number
		Custort	NCWG0 LA-5481
Date:	Wednesday, May 20, 2009	Sheet	9 of 46

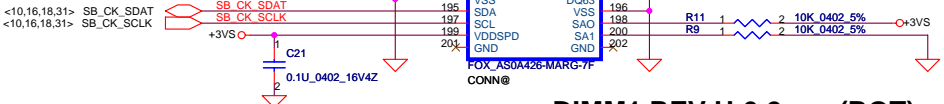
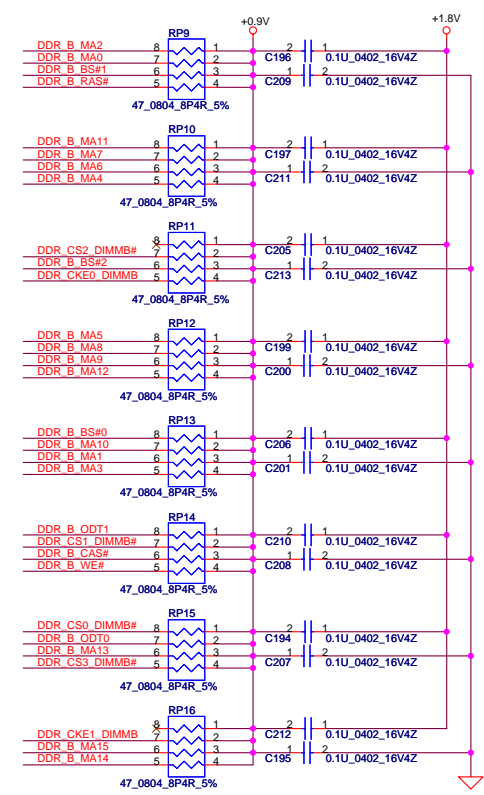


DIMM2 REV H:5.2mm (BOT)

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				NCWG0 LA-5481	0.1	
				Date: Wednesday, May 20, 2009	Sheet 10 of 46	

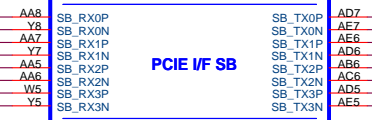
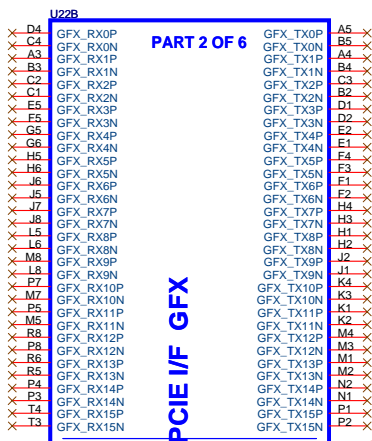


- <?> DDR_B_D[0..63] **DDR_B D[0..63]**
- <?> DDR_B_DM[0..7] **DDR_B DM[0..7]**
- <?> DDR_B_DQS[0..7] **DDR_B DQS[0..7]**
- <?> DDR_B_MA[0..15] **DDR_B MA[0..15]**
- <?> DDR_B_DQS#[0..7] **DDR_B DQS#[0..7]**



DIMM1 REV H:9.2mm (BOT)

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				Date:	Wednesday, May 20, 2009	Sheet 11 of 46



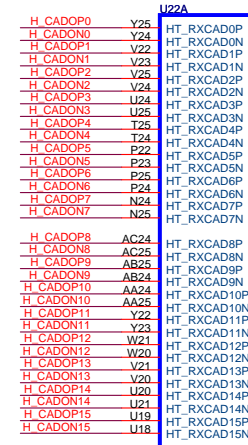
RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

Check SW Routing
AN_RS780MN1. Only suggest pair0-3 can use for power save.

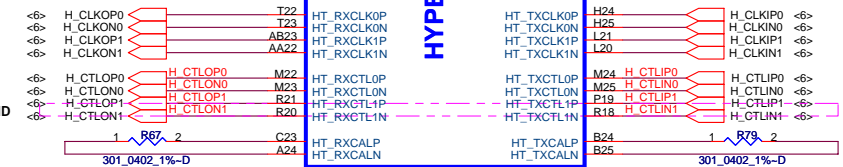
WAN
LAN



HYPER TRANSPORT CPU I/F

HT Link
When tune trace length, must keep 1:4 on self-trace

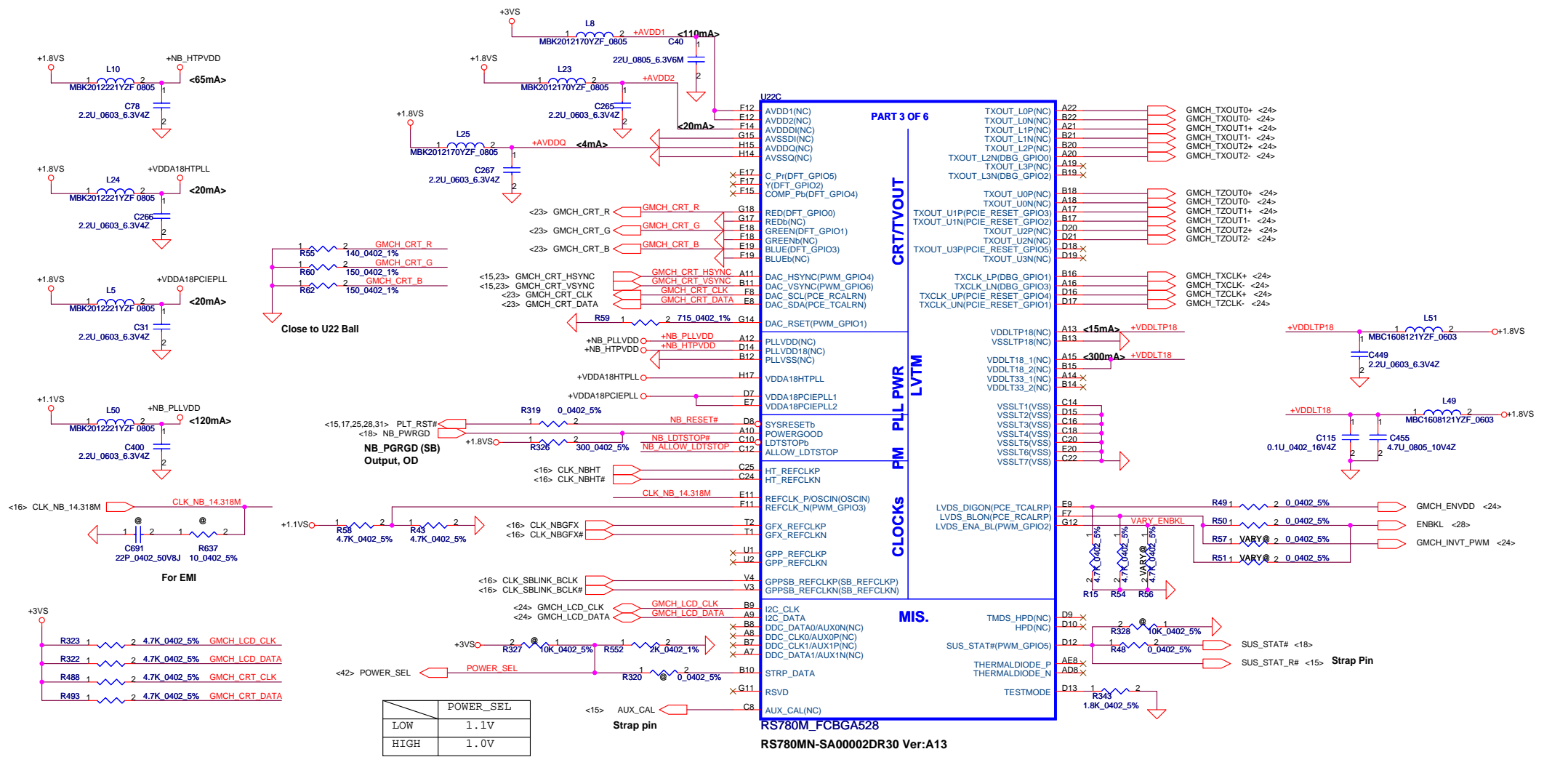
Check AMD



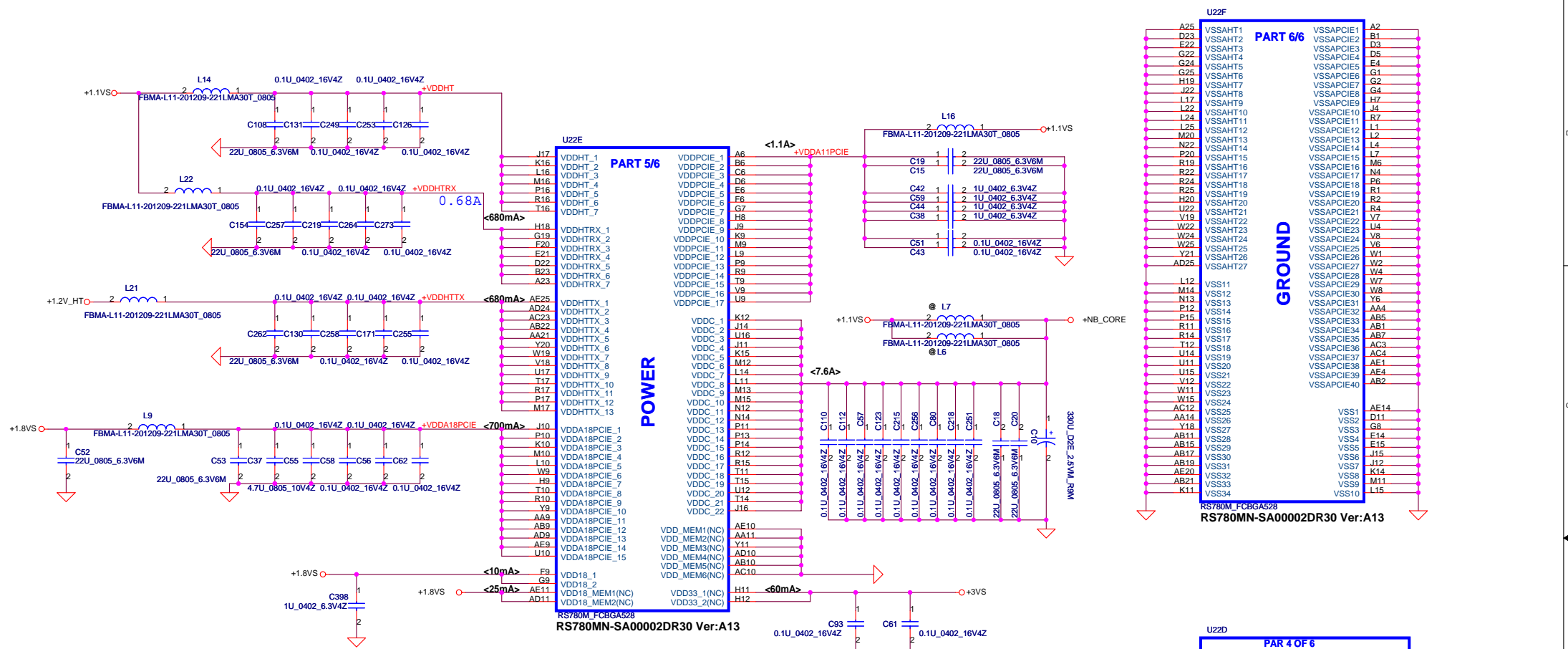
Place within 1" layout 4/8

Place within 1" layout 4/8

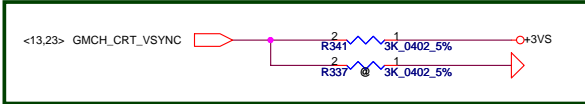
Security Classification		Compal Secret Data		Title	
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				Customer	NCWGO LA-5481
				Date:	Wednesday, May 20, 2009
				Sheet	12 of 47
				Rev	0.1



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Custom	NCWGO LA-5481	0.1			
Date:	Wednesday, May 20, 2009	Sheet	13	of	47

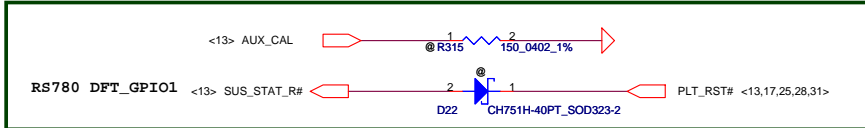


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Date:	Wednesday, May 20, 2009	Sheet	14	of 47	



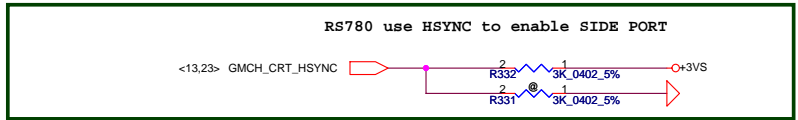
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



DFT_GPIO1:LOAD_EEPROM_STRAPS

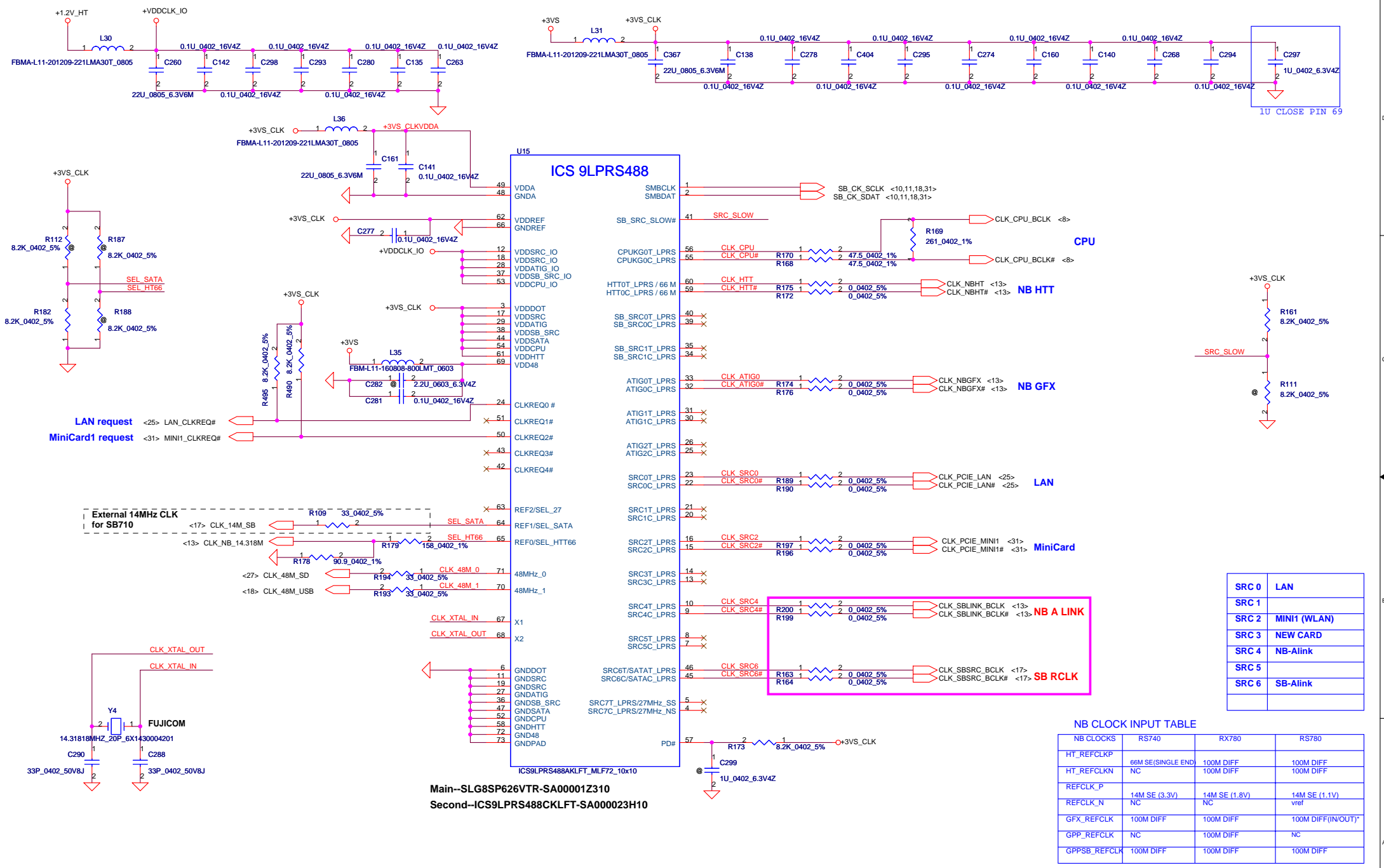
Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0. Enable (RS780)
 1 : Disable(RS780)

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				Date:	Wednesday, May 20, 2009
				Sheet	15 of 47
				Rev	0.1



Main-SLG8SP626VTR-SA00001Z310
 Second-ICS9LPRS488CKLFT-SA000023H10

SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

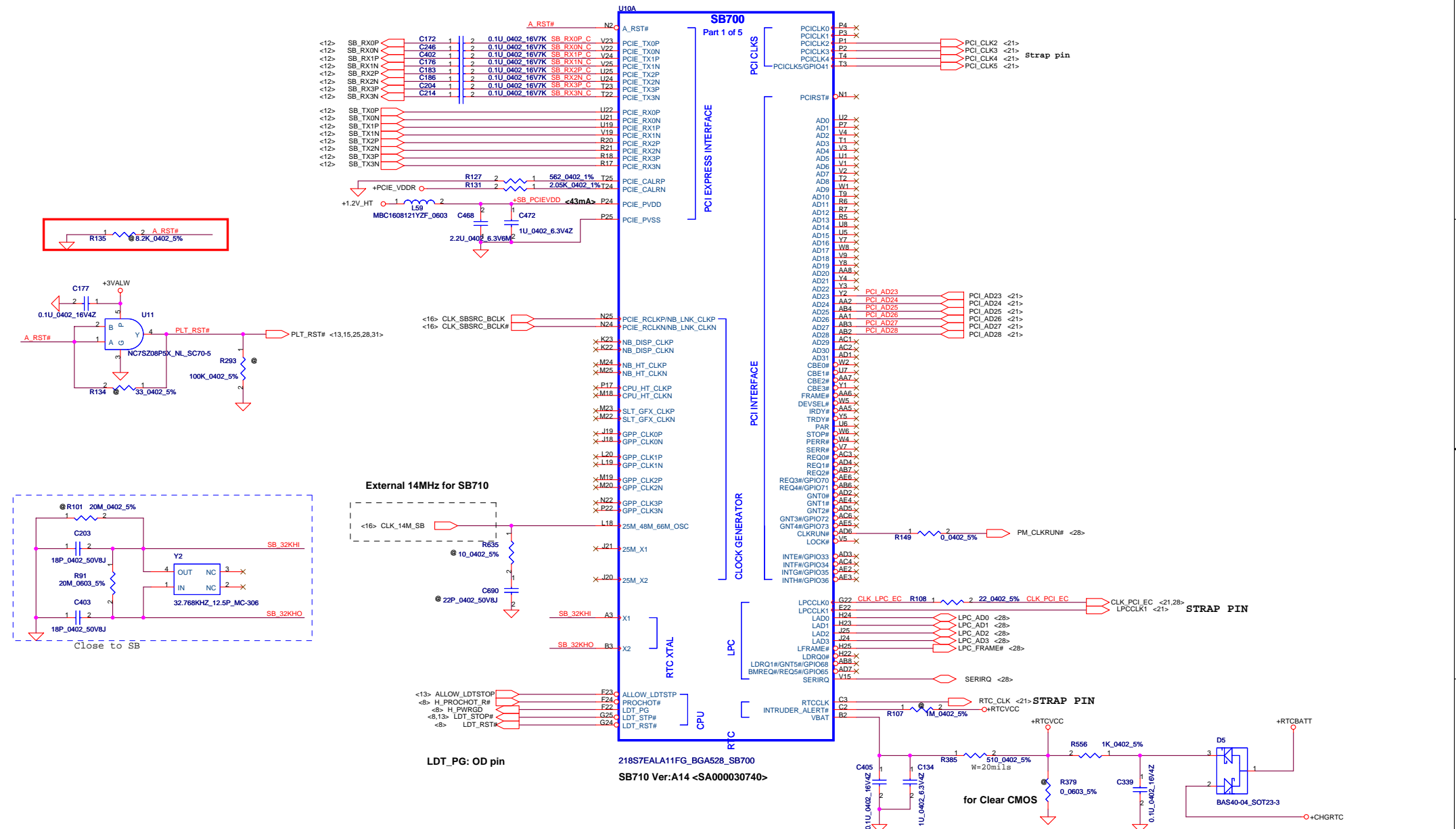
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P			
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

SEL_27M	1	configure as 27M and 27M_SS output
No used	0	configure as SRC_7 output

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Custom	NCWGO LA-5481	0.1			
Date:	Wednesday, May 20, 2009	Sheet	16	of 47	



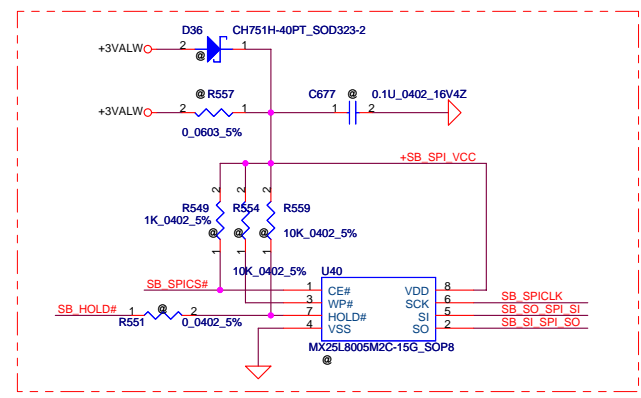
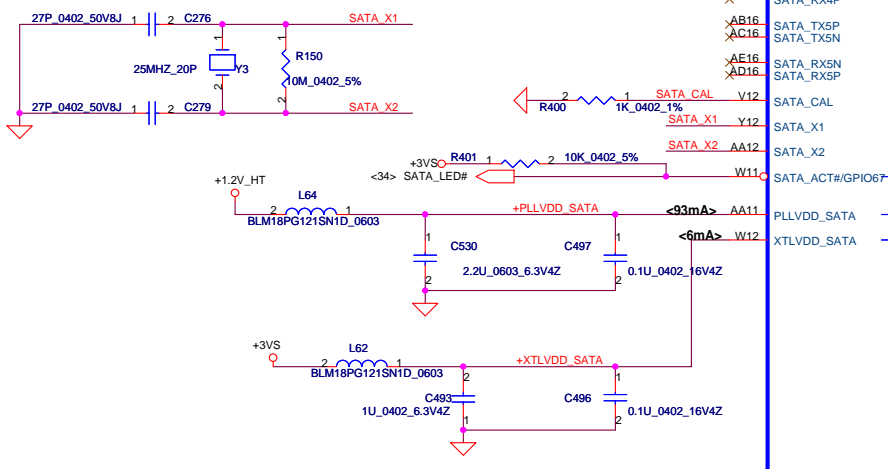
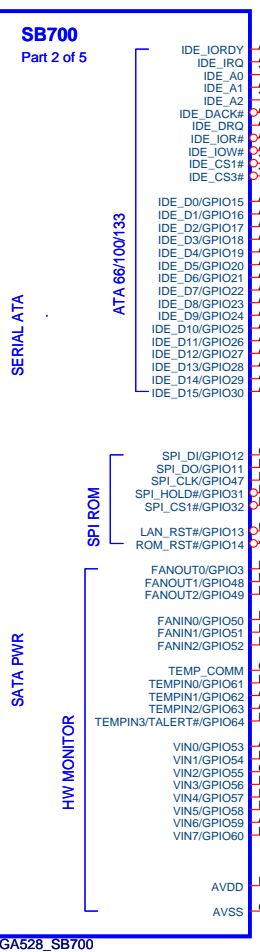
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			Sheet 17 of 47

Rev 0.1

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

Main HDD
2nd HDD
Main ODD
2nd ODD

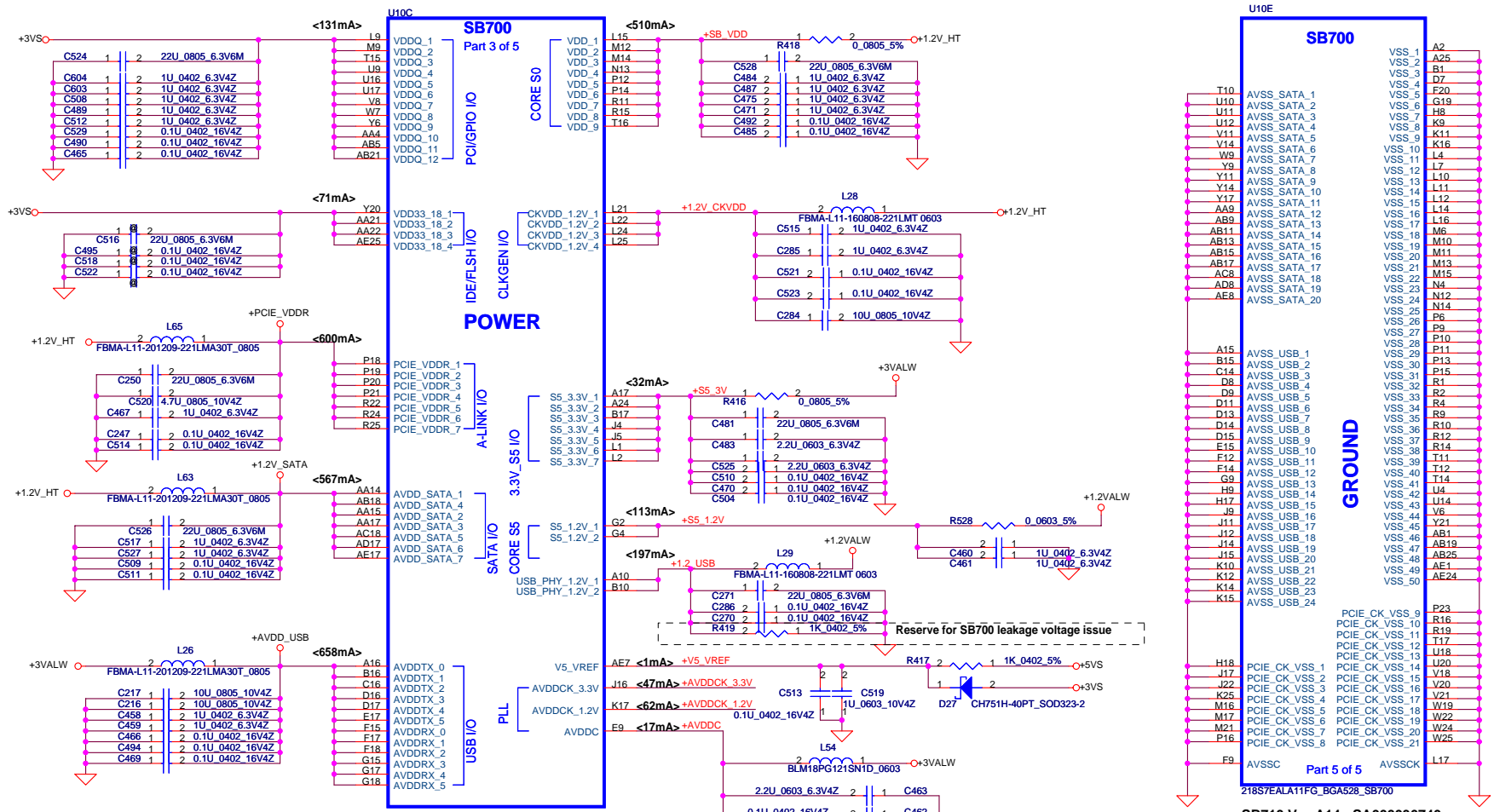
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- <22> SATA_STX_DRX_N0
- <22> SATA_DTX_C_SRX_N0
- <22> SATA_DTX_C_SRX_P0
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- <22> SATA_STX_DRX_N1
- <22> SATA_DTX_C_SRX_N1
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- <22> SATA_STX_DRX_N2
- <22> SATA_DTX_C_SRX_N2
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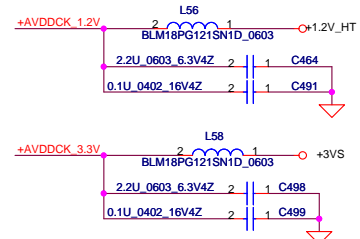
for ACIN level issue

218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12

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218S7EAL11FG_BGA528_SB700
SB710 Ver:A14 <SA000030740>

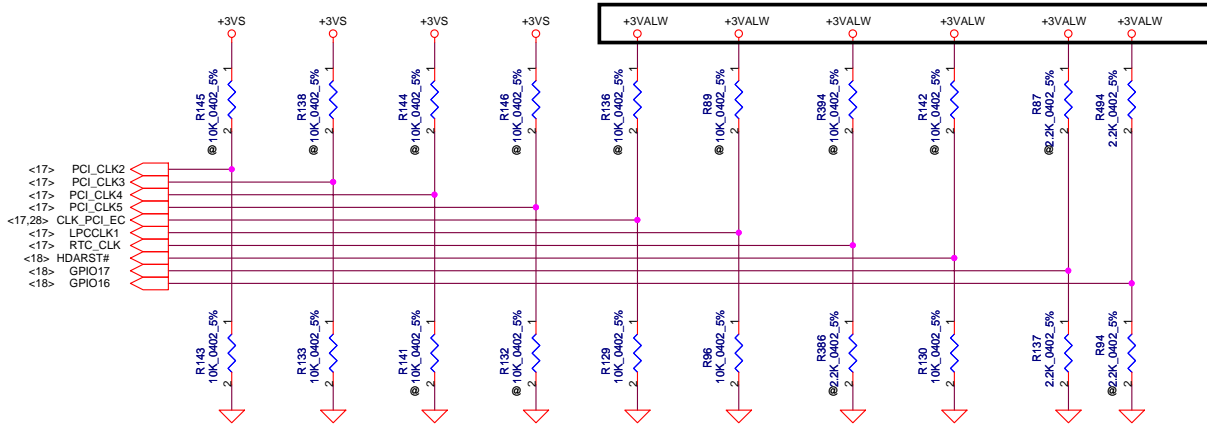


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Size	Document Number	Rev			
Customr	NCWG0 LA-5481	0.1			
Date:	Wednesday, May 20, 2009	Sheet	20	of 47	

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	

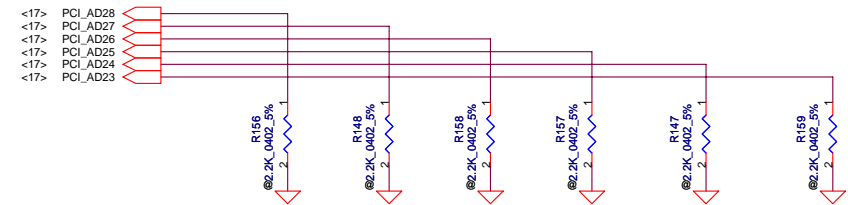


DEBUG STRAPS

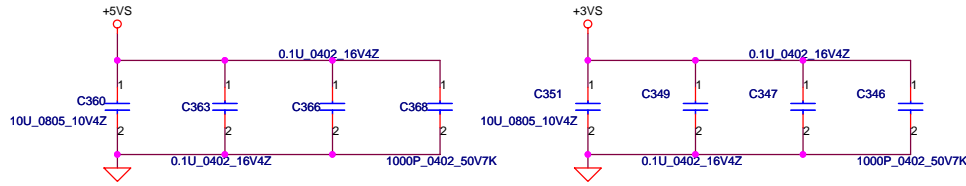
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

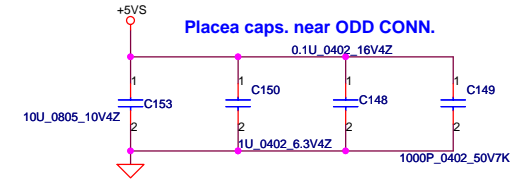
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



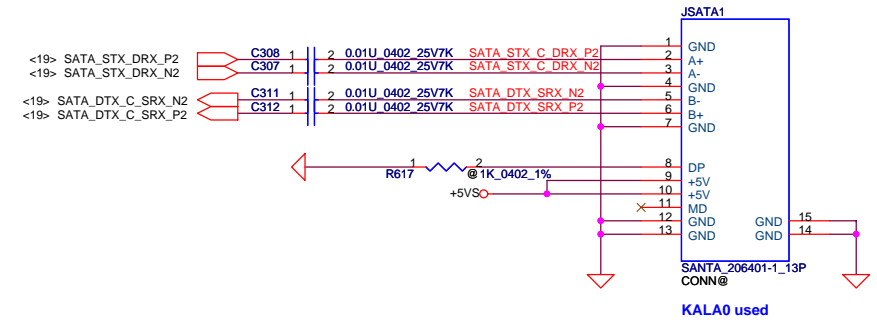
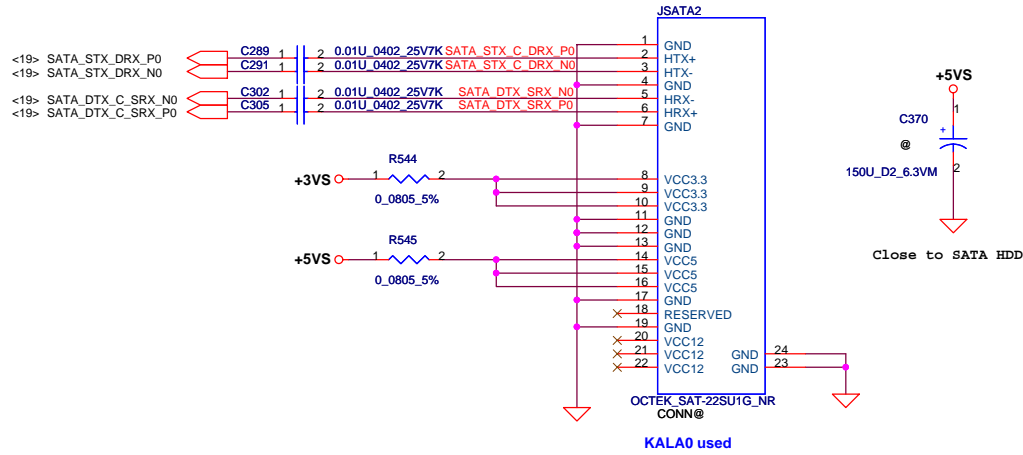
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Issued Date	2005/03/08	Deciphered Date	2010/03/12	Title	
				SB700-STRAPS	
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Date:	Wednesday, May 20, 2009	Sheet	21	of	47



SATA HDD CONN

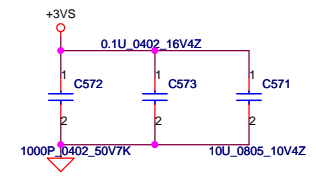
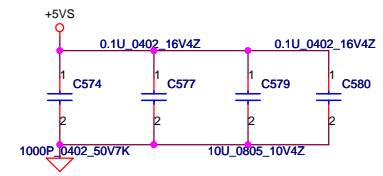
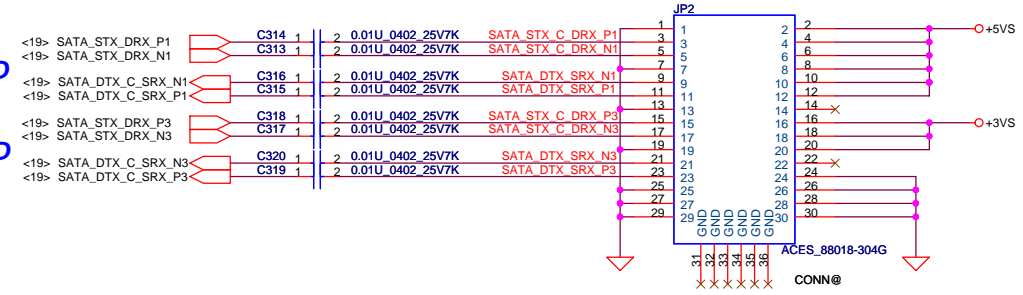


SATA ODD CONN



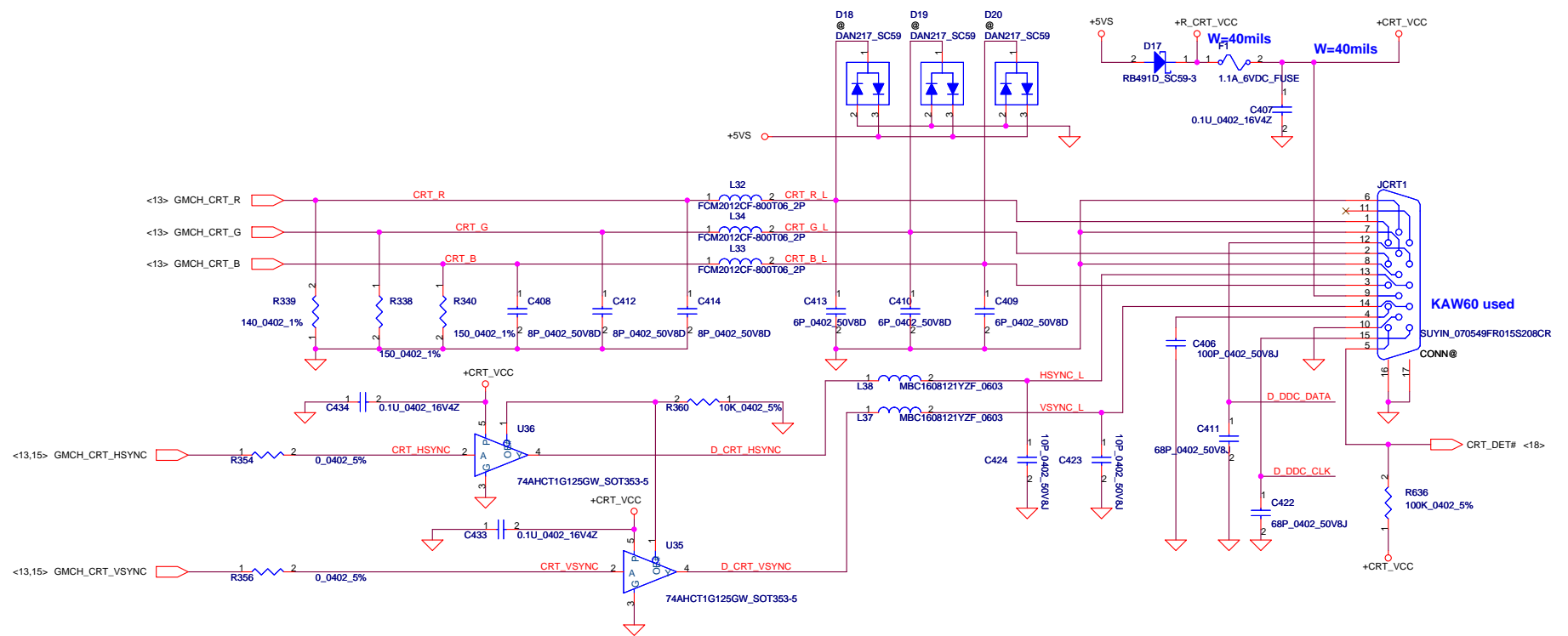
Second HDD

Second ODD

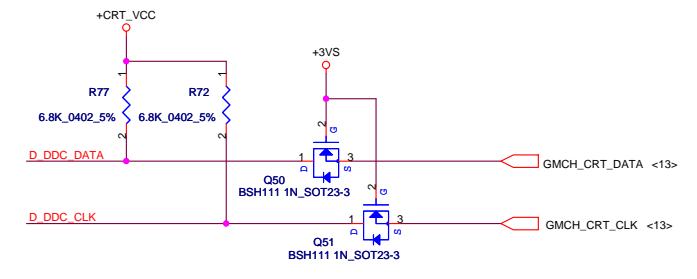


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2005/03/08		2010/03/12		Size B	
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				NCWG0 LA-5481	
				Rev 0.1	
				Date: Wednesday, May 20, 2009	
				Sheet 22 of 47	

CRT Connector

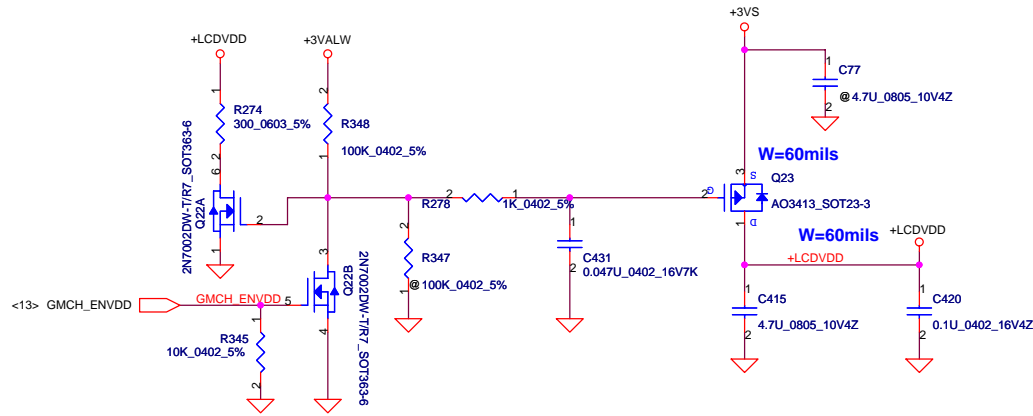


Close to Conn side

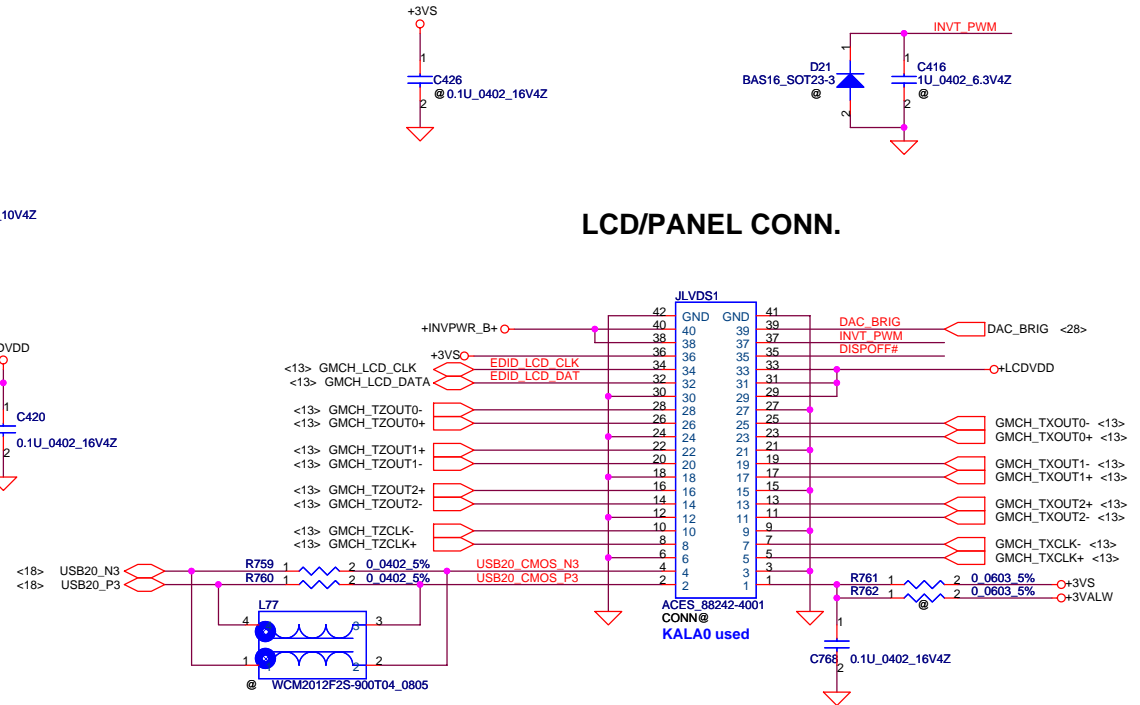


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				NCWGO LA-5481	Rev 0.1
				Date: Wednesday, May 20, 2009	Sheet 23 of 47

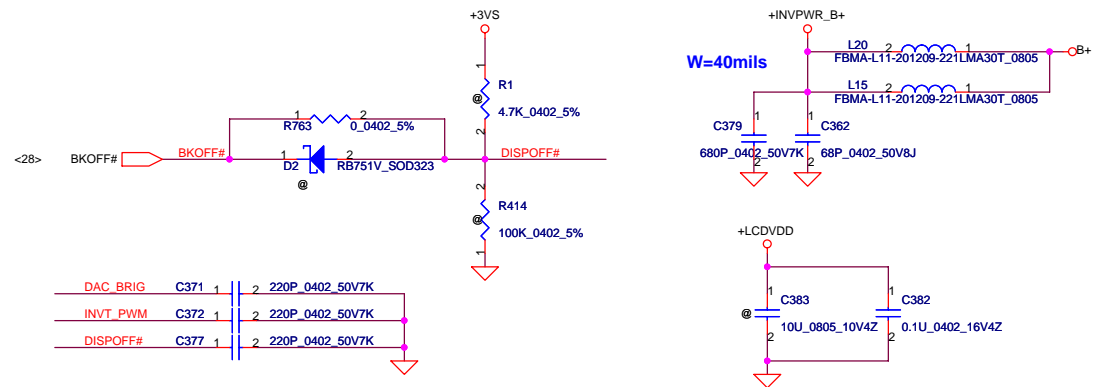
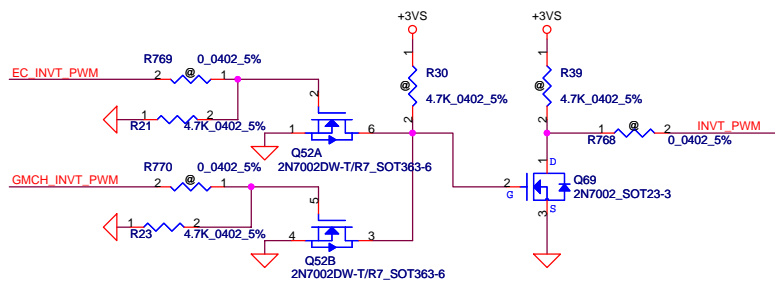
LCD POWER CIRCUIT



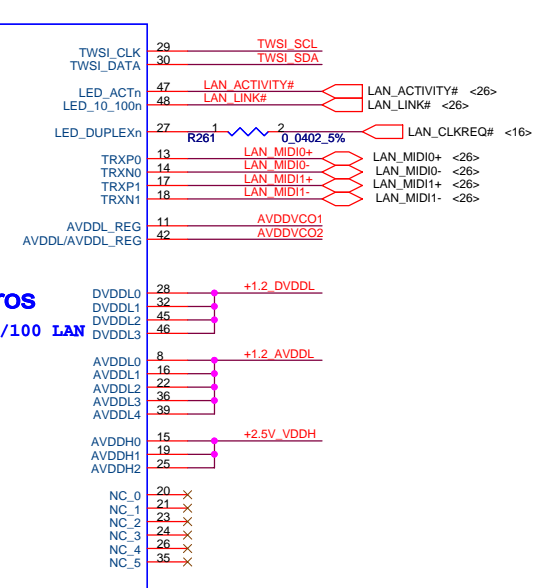
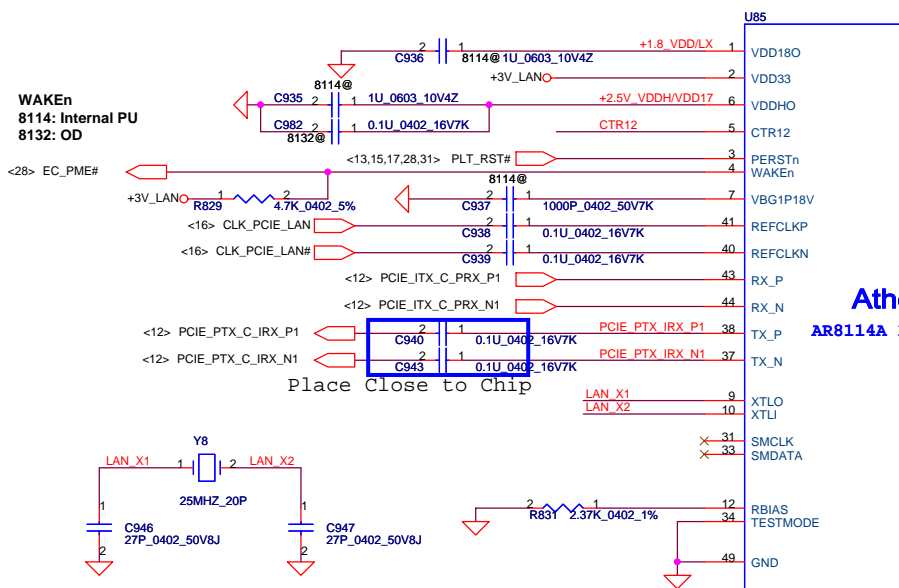
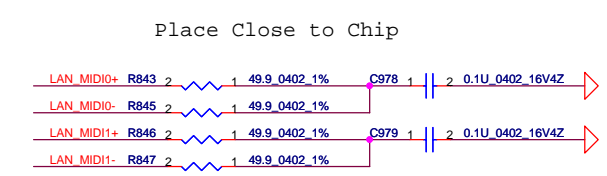
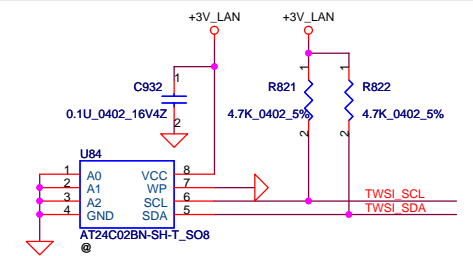
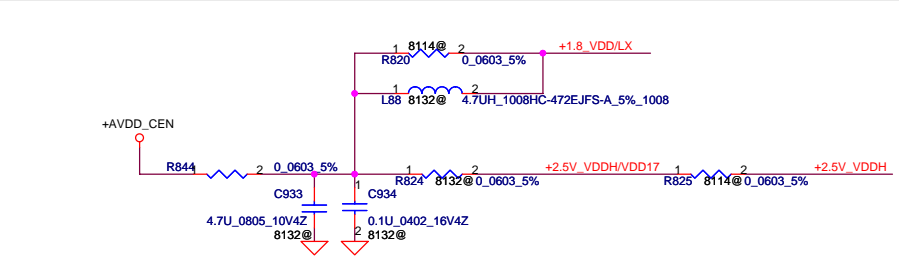
LCD/PANEL CONN.



VARYBRIGHT FUNCTION

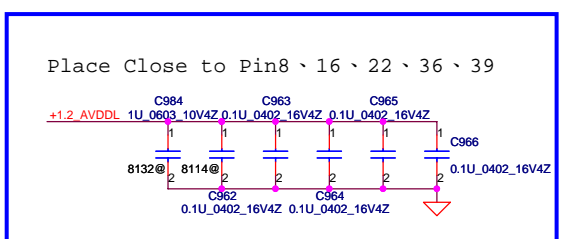
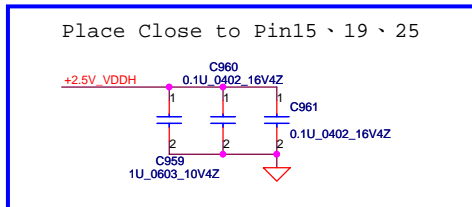
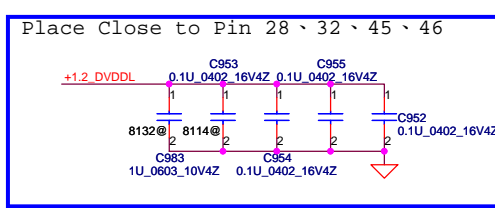
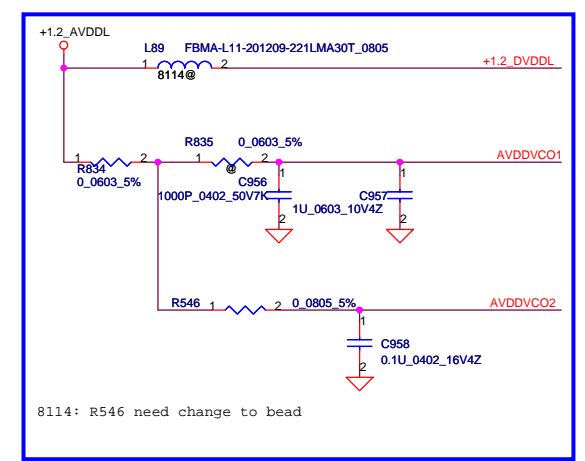
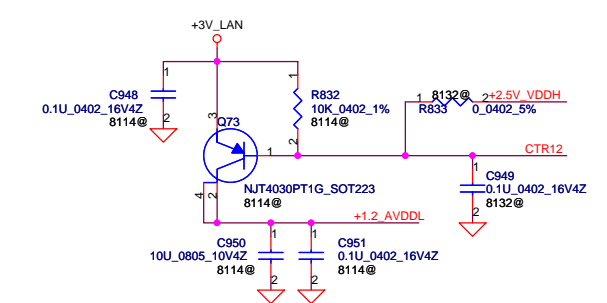
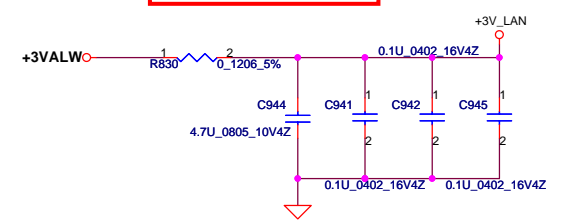


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Custom	NCWG0 LA-5481	0.1	
Date:	Wednesday, May 20, 2009	Sheet	24 of 47

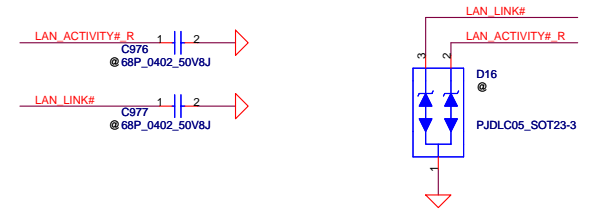
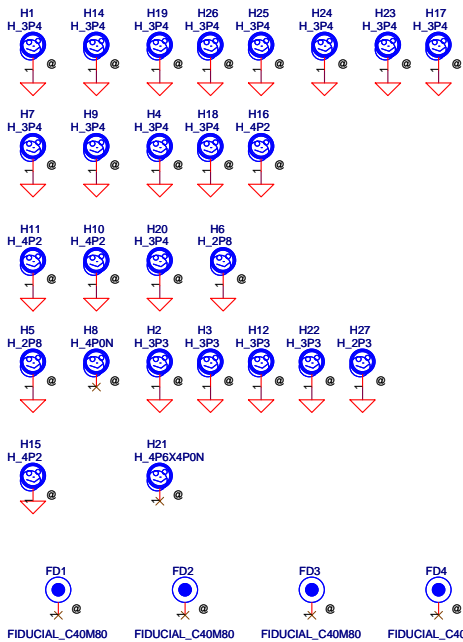
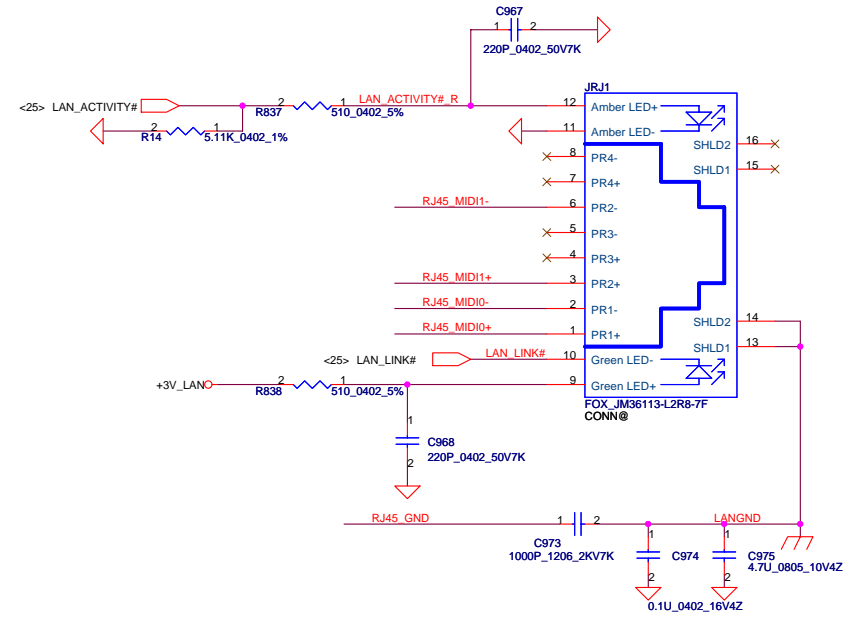
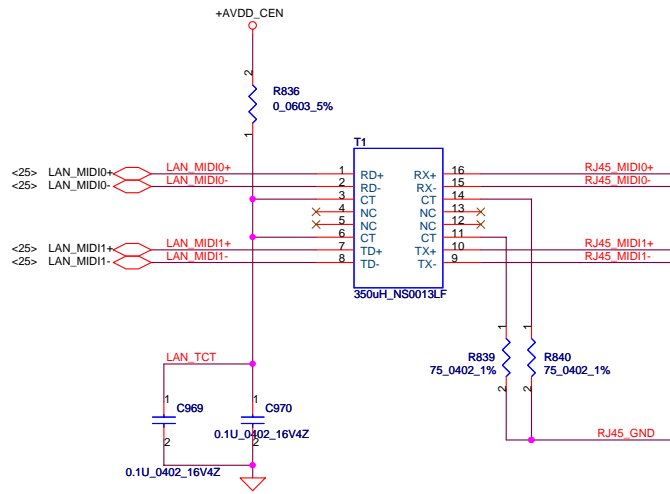


change to AR8132L-AL1E

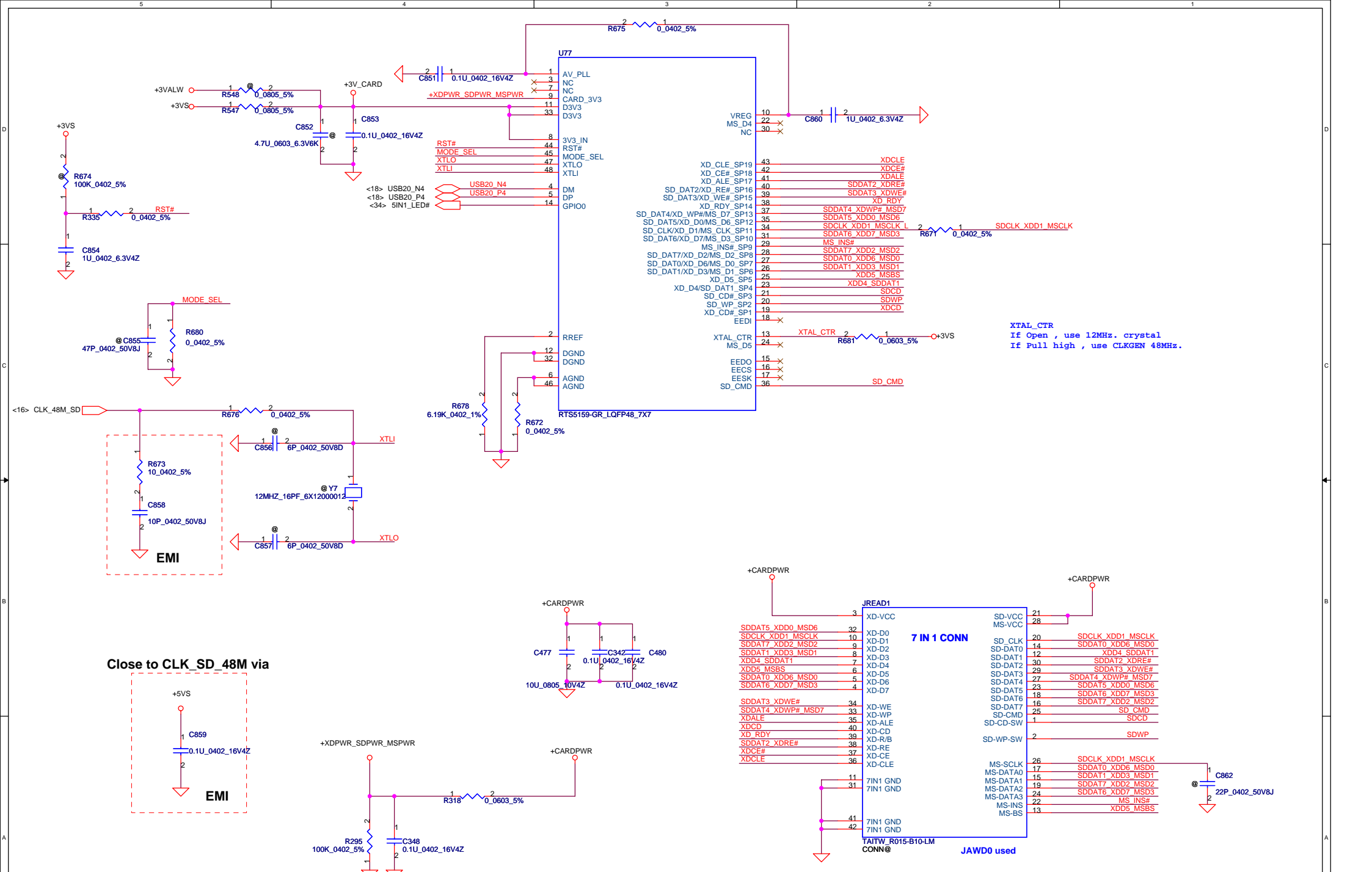
Layout Notice : Close to chip



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	NCWGO LA-5481	Wednesday, May 20, 2009		25	0.1
				Sheet	of 47

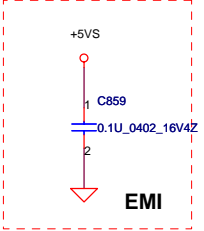


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Date:	Wednesday, May 20, 2009	Sheet	26	of	47
Rev	0.1				

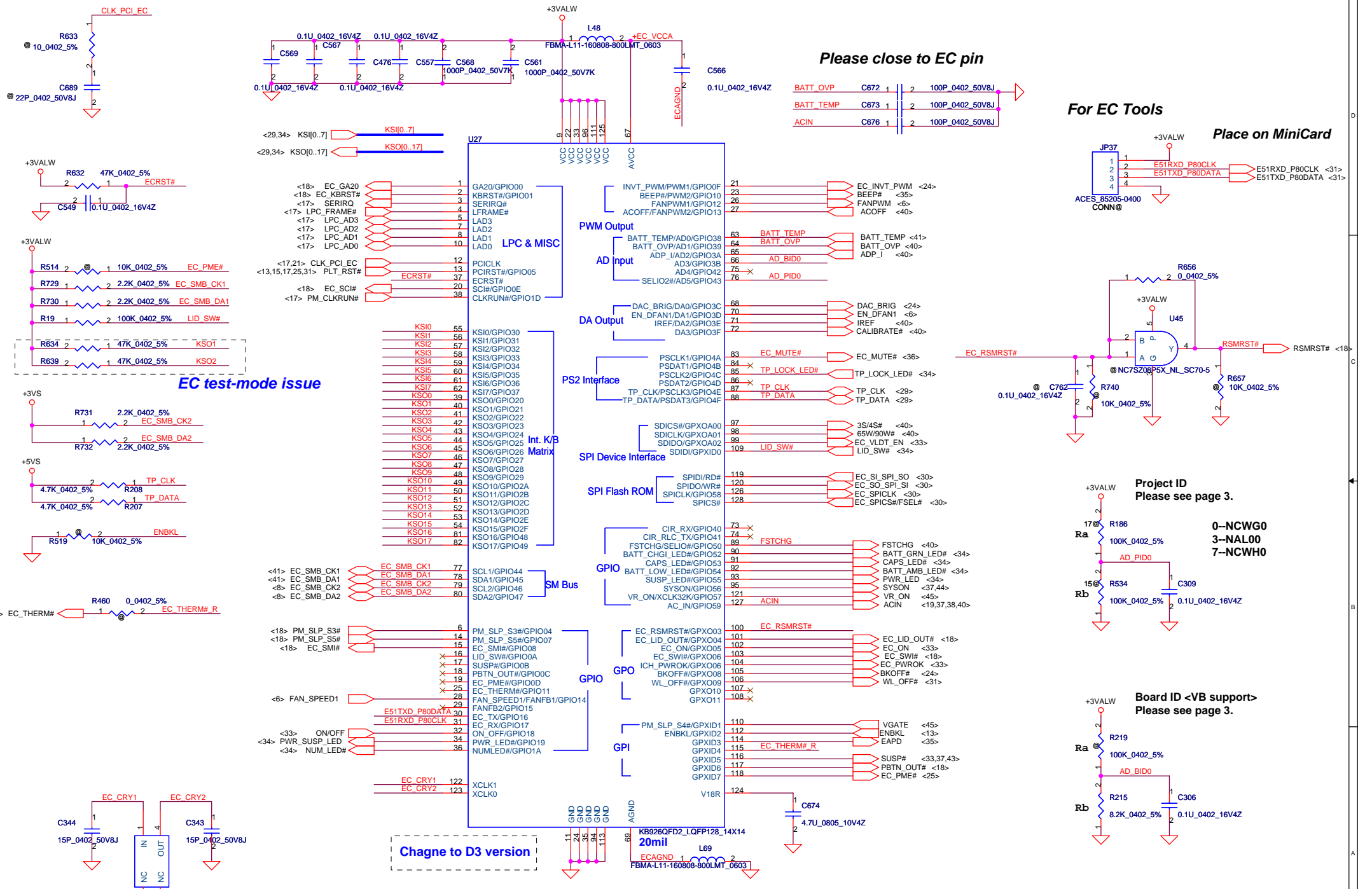


XTAL_CTR
 If Open, use 12MHz. crystal
 If Pull high, use CLKGEN 48MHz.

Close to CLK_SD 48M via

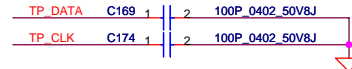
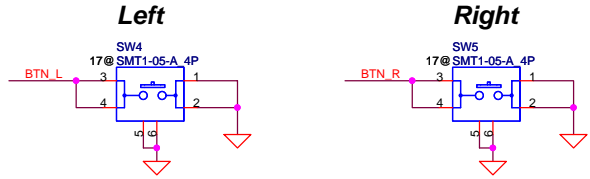


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				B	NCWG0 LA-5481
				Date:	Wednesday, May 20, 2009
				Sheet	27 of 47
				Rev	0.1

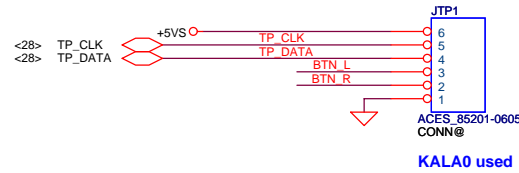


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Size	Document Number			Rev	
Custpm	NCWG0 LA-5481			0.1	
Date:	Wednesday, May 20, 2009	Sheet	28	of 47	

For 17"

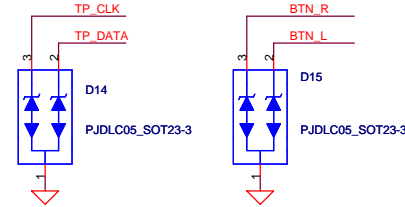
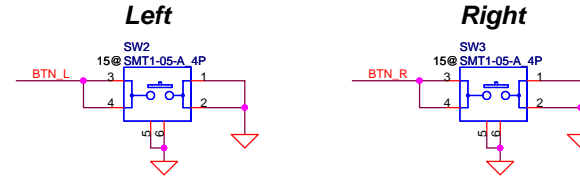


To TP/B Conn.



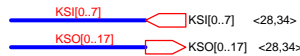
KALA0 used

For 15"

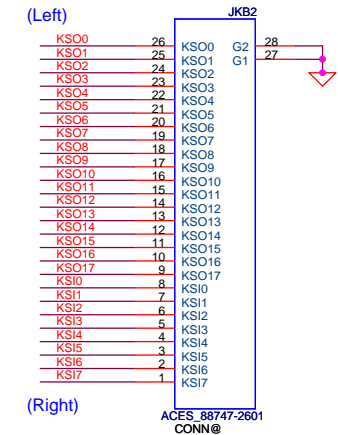
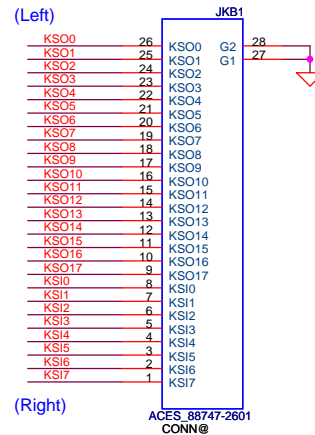
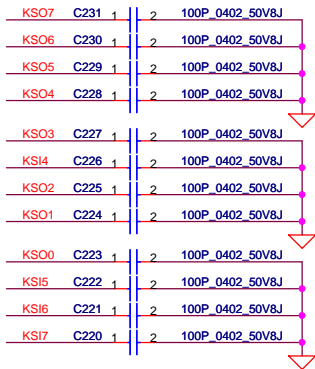
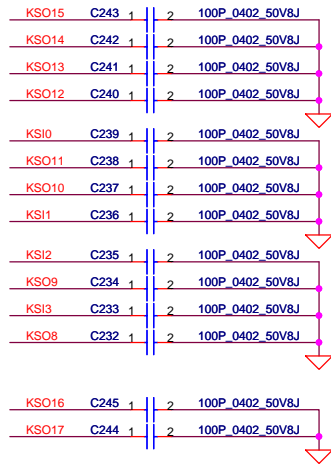


Change to SCA00000200

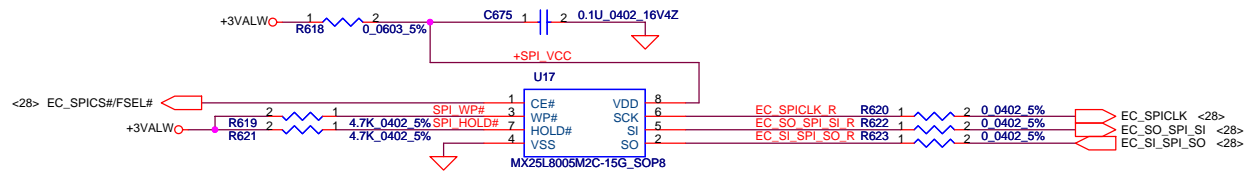
INT_KBD Conn.



KB1 for 15"
KB2 for 17"

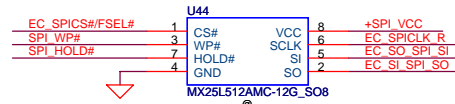
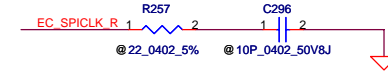


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			Size Custom	Document Number
Date:			Wednesday, May 20, 2009	Sheet 29 of 47
			NCWG0 LA-5481	0.1



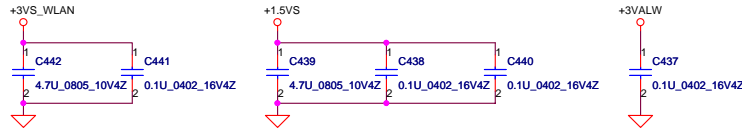
SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

ONLY MXIC used in this project (66MHz)

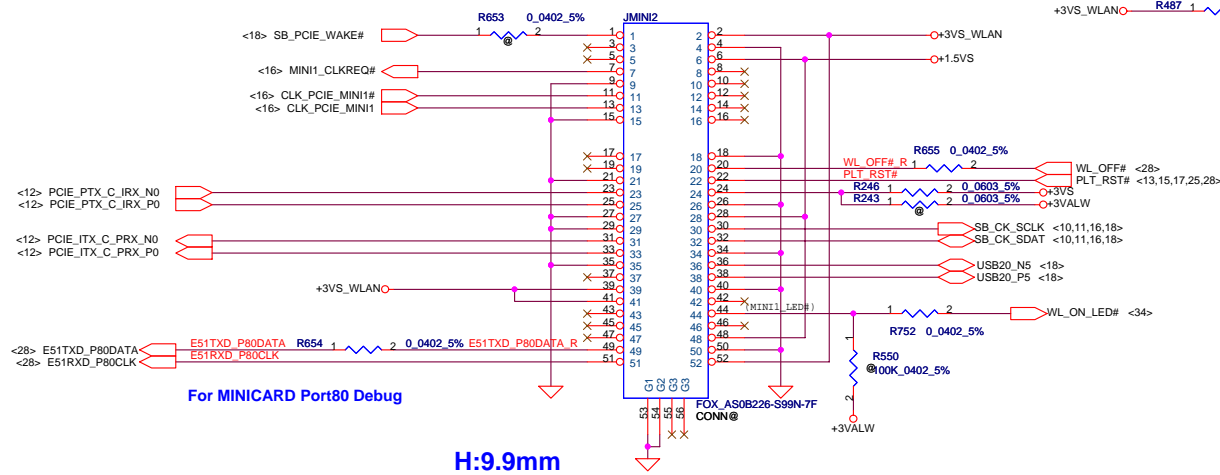


Reserved for BIOS simulator.
 Footprint S08
SPI ROM Footprint 150mil

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				NCWG0 LA-5481
				Rev 0.1
Date:		Wednesday, May 20, 2009	Sheet	30 of 47



For Wireless LAN



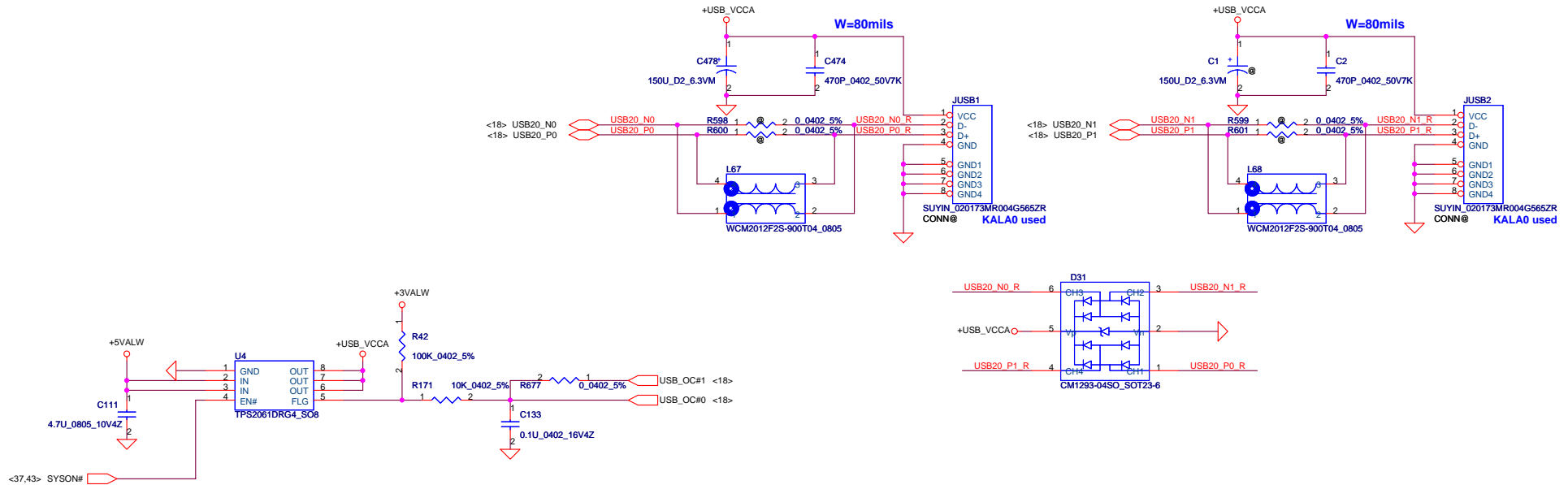
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For MINICARD Port80 Debug

H:9.9mm

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				NCWG0 LA-5481		0.1
				Date:	Wednesday, May 20, 2009	Sheet 31 of 47

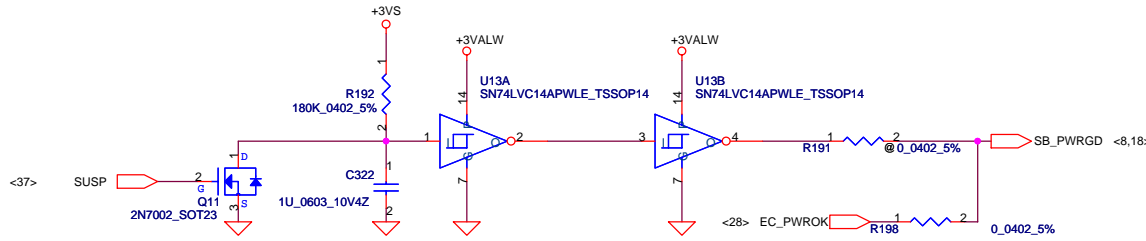
USB CONN. 1 & 2



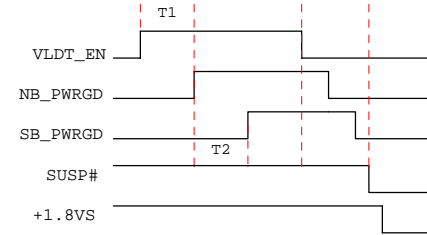
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2010/03/12	Title	
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				NCWG0 LA-5481	
				Date:	Wednesday, May 20, 2009
				Sheet	32 of 47
				Rev	0.1

Power ON Circuit

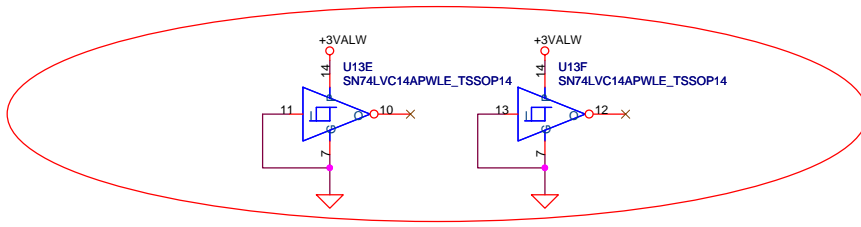
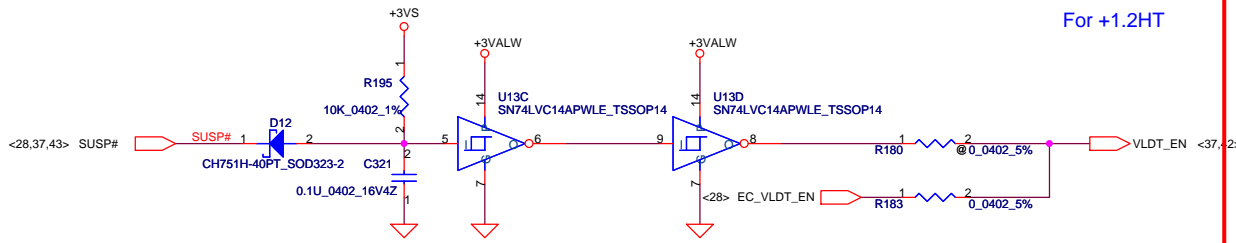
For South Bridge



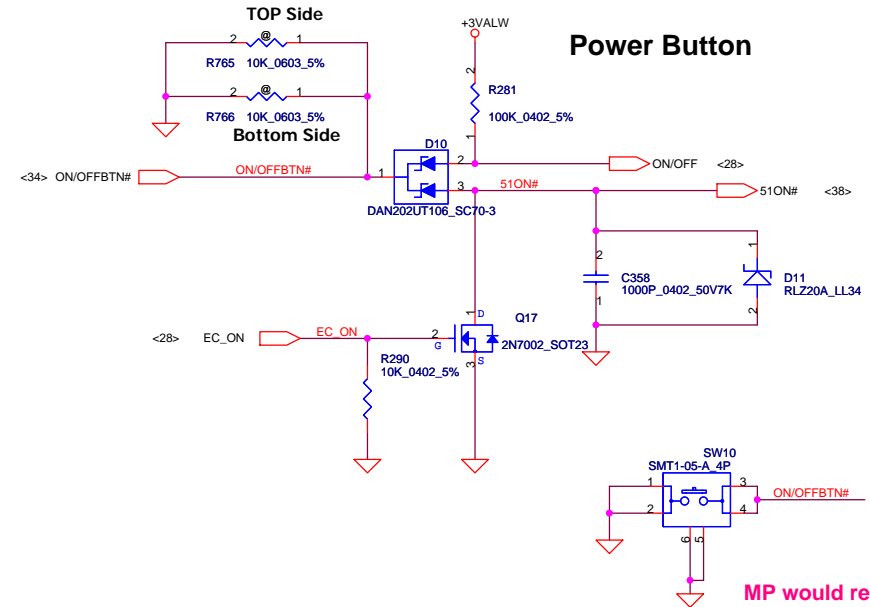
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



For +1.2HT

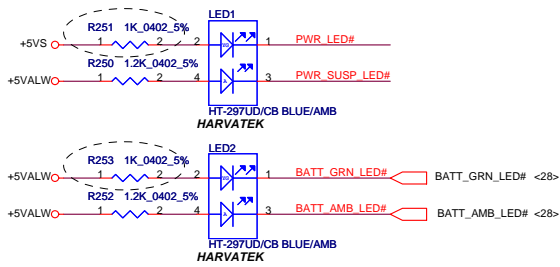
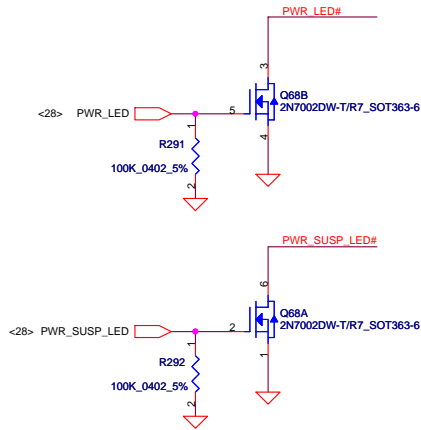


Power Button

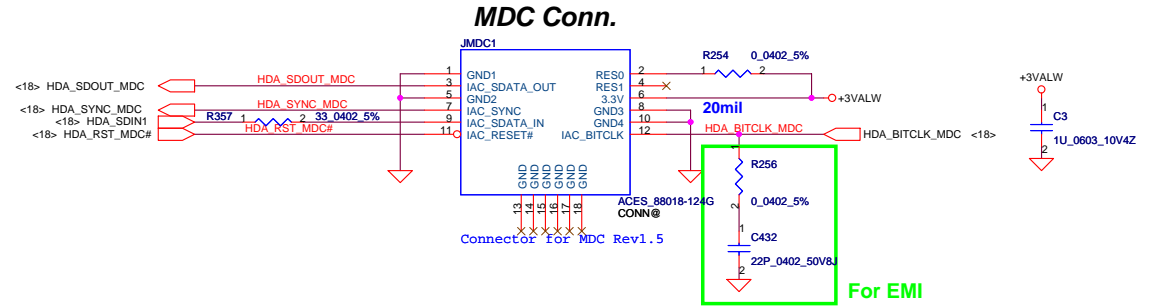


MP would remove

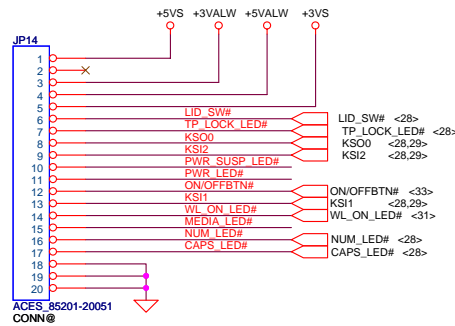
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2010/03/12	PWR_OK/ PWR BTN	
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Size B	Document Number	Date		Sheet	Rev
	NCWG0 LA-5481	Wednesday, May 20, 2009		33 of 47	0.1



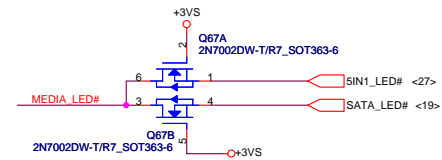
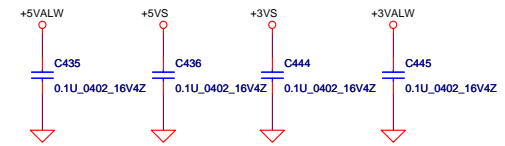
BLUE/AMB LED



To PWR LED/B

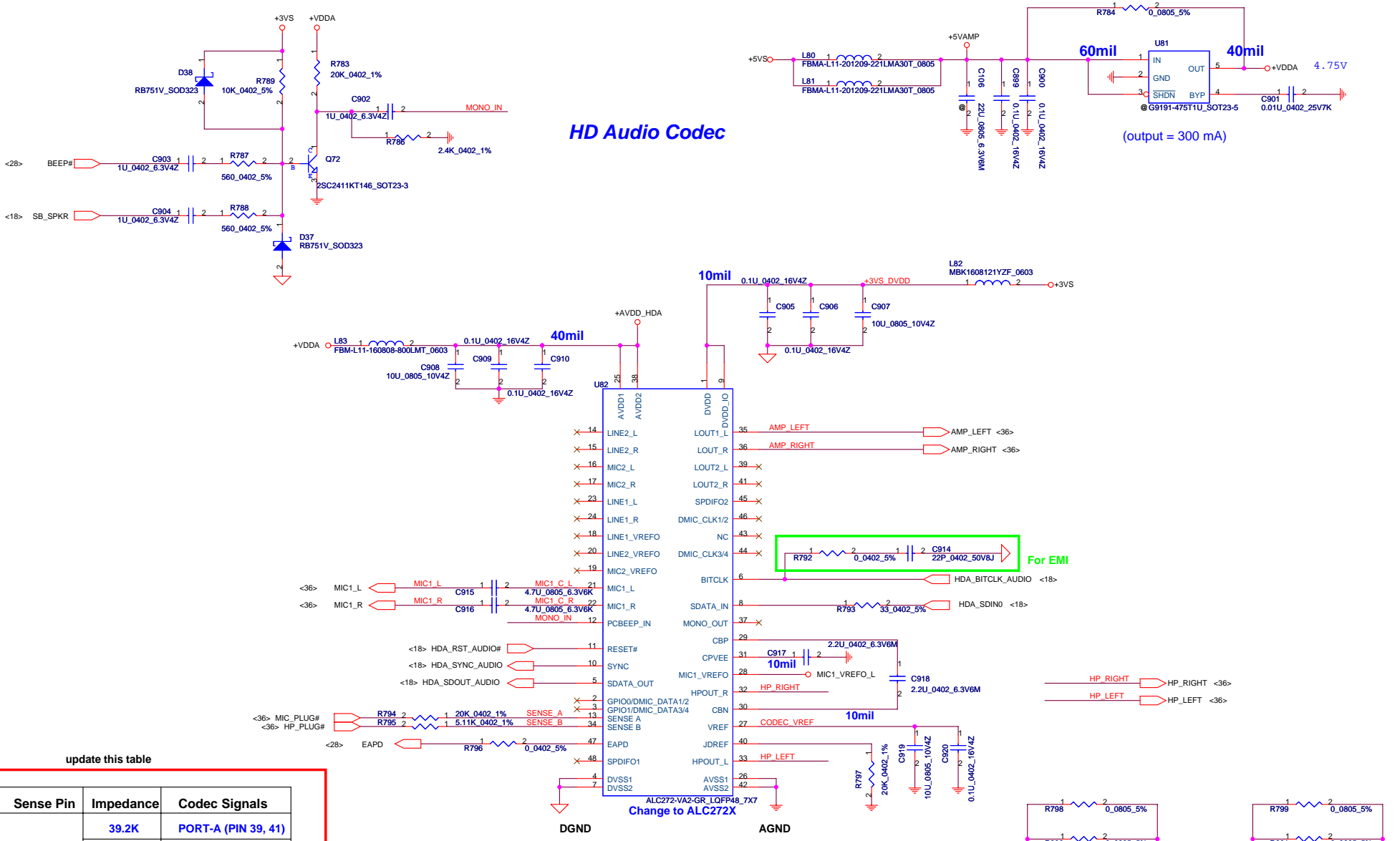


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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Size B	Document Number			Rev	
	NCWG0 LA-5481			0.1	
Date:	Wednesday, May 20, 2009	Sheet	34	of	47

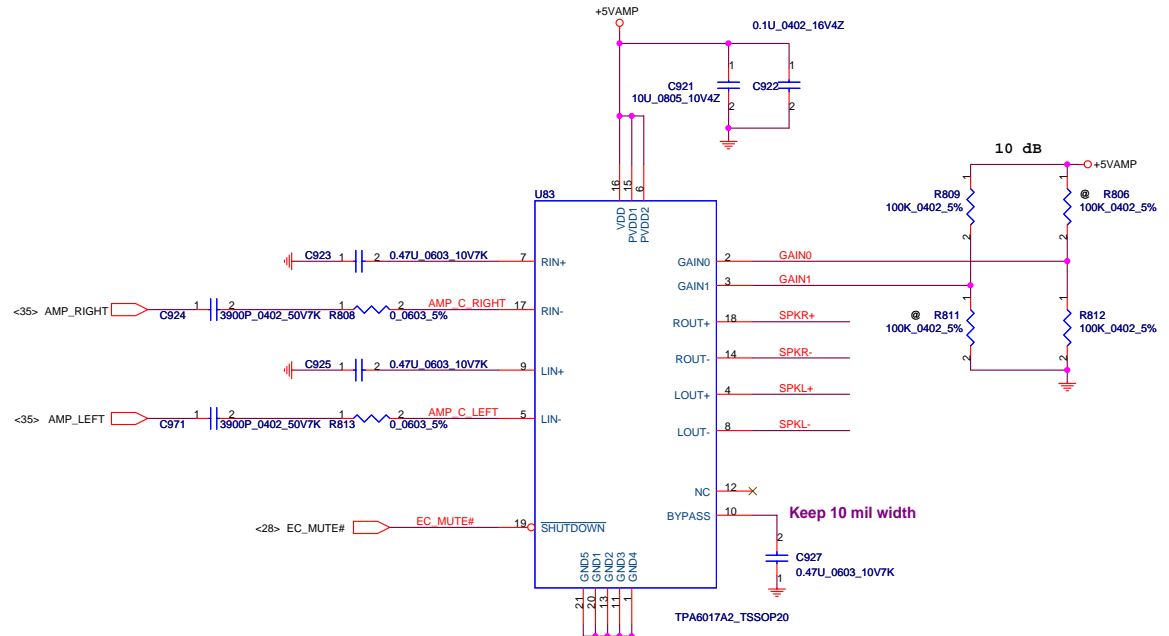
HD Audio Codec



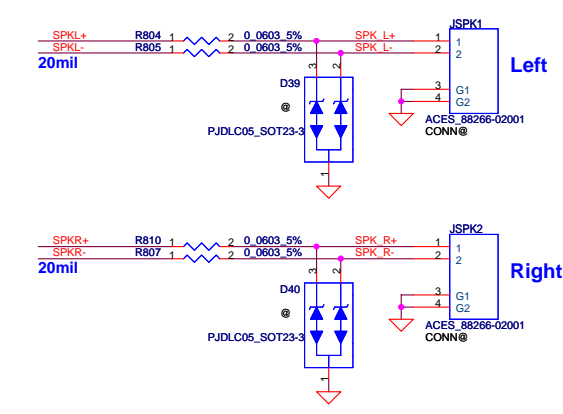
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

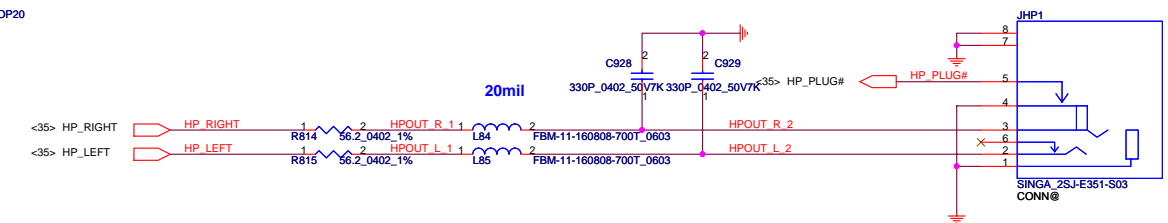
Security Classification		Compal Secret Data		Title	
Issued Date	2007/09/20	Deciphered Date	2010/03/12	HDA Codec ALC268	
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Date:	Wednesday, May 20, 2009	Sheet	35 of 47	Rev	0.1



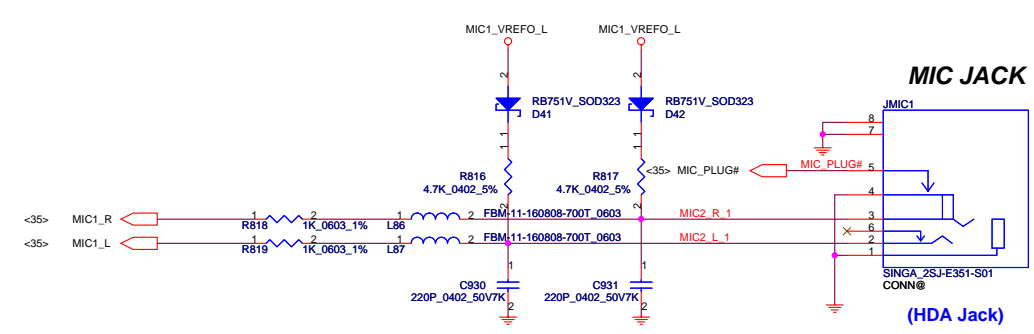
Int. Speaker Conn.



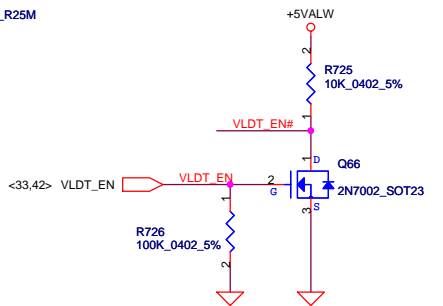
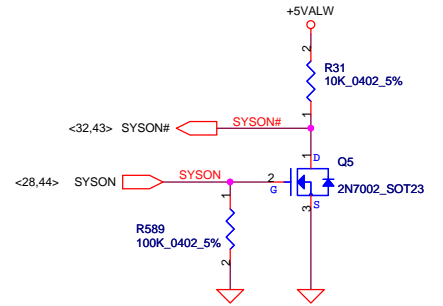
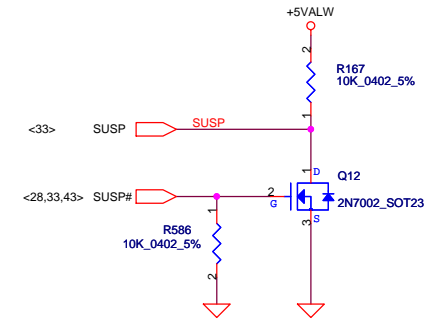
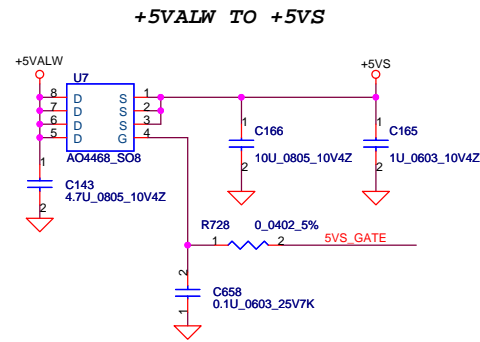
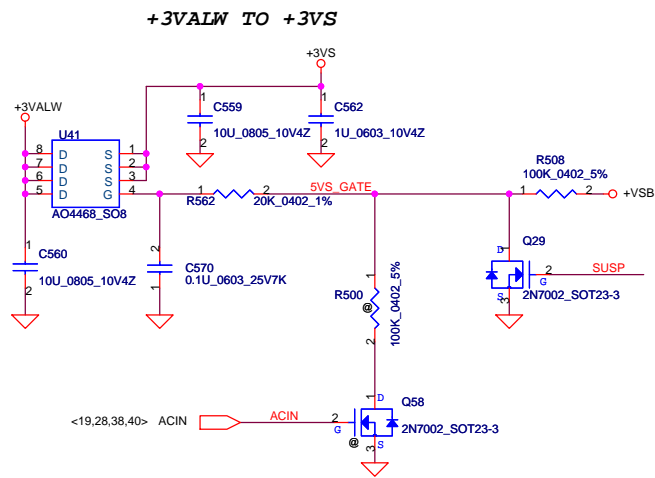
LINE Out/Headphone Out



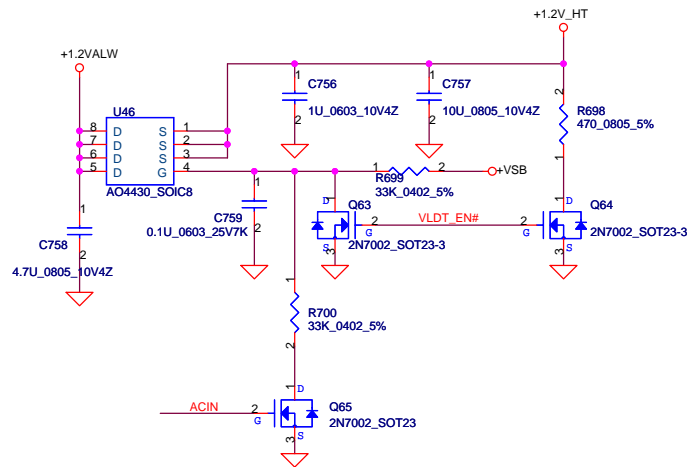
MIC JACK



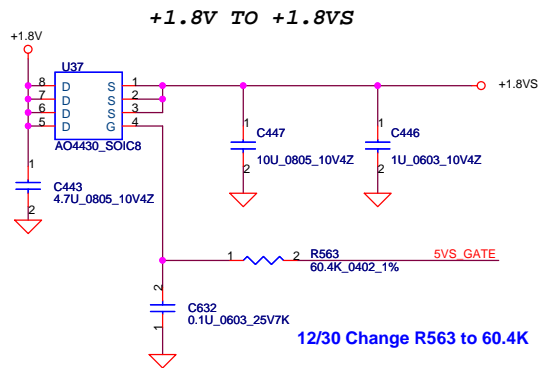
Security Classification		Compal Secret Data		Title	
Issued Date	2007/09/20	Deciphered Date	2010/03/12	Amplifier & Audio Jack	
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				NCWG0 LA-5481	Rev 0.1
				Date: Wednesday, May 20, 2009	Sheet 36 of 47



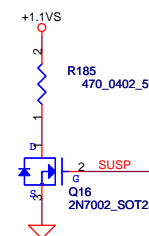
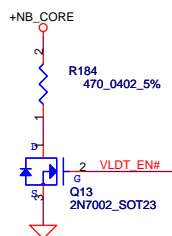
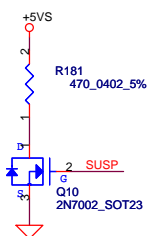
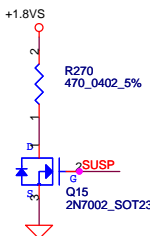
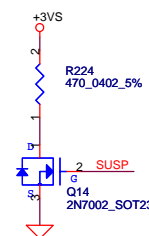
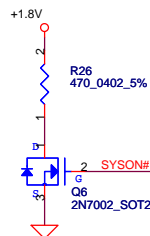
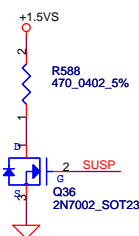
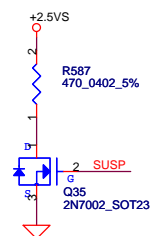
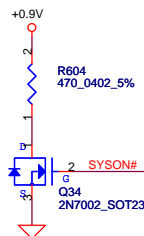
+1.2VALW TO +1.2V_HT



For PWR request

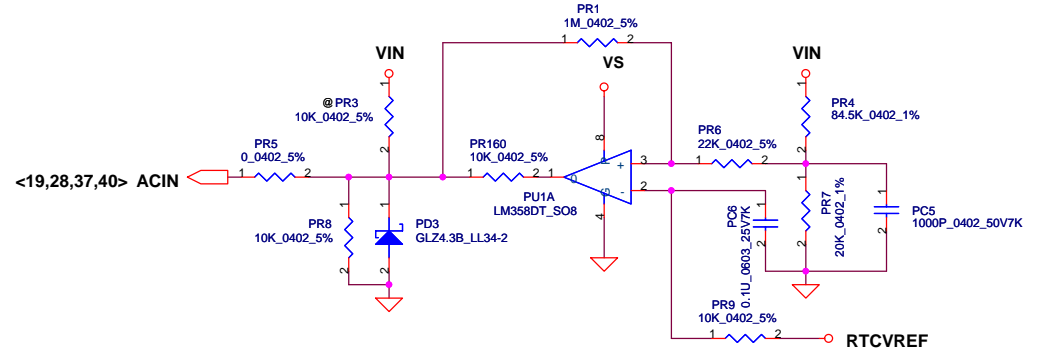
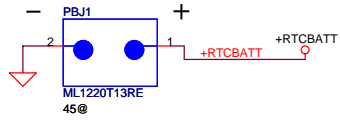
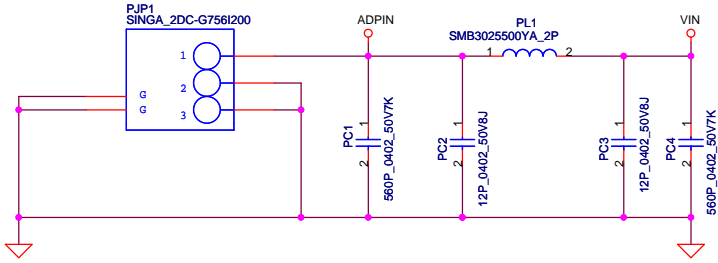


12/30 Change R563 to 60.4K

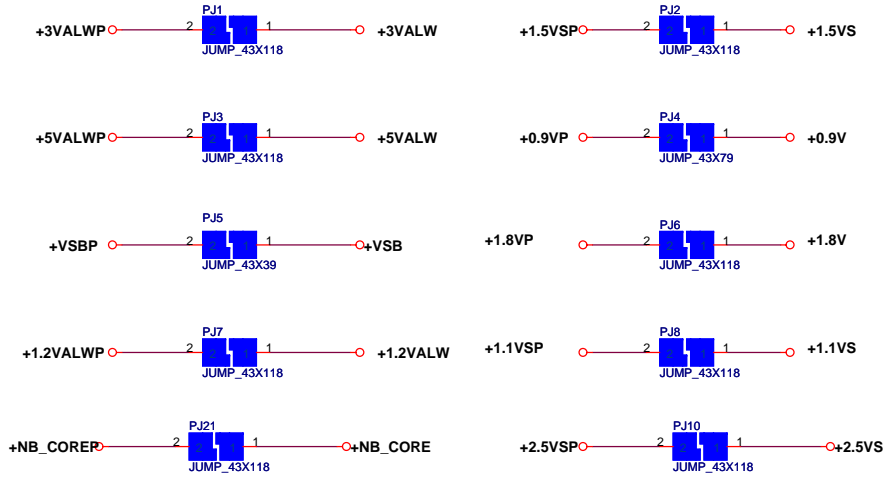
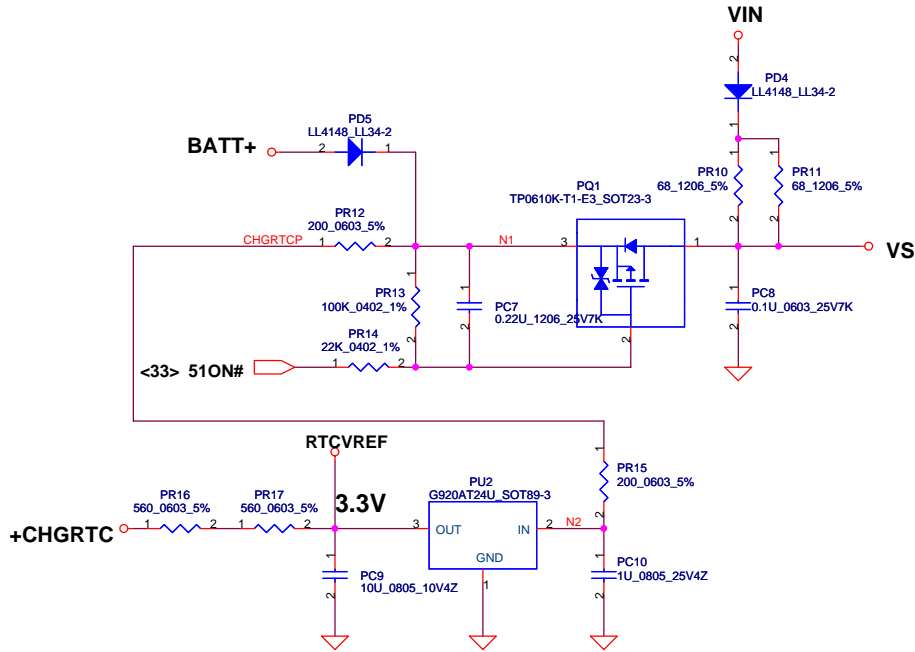


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Issued Date	2005/03/08	Deciphered Date	2010/03/12	DC INTERFACE	
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Size	Document Number			Rev	
B	NCWG0 LA-5481			0.1	
Date:	Wednesday, May 20, 2009	Sheet	37	of	47

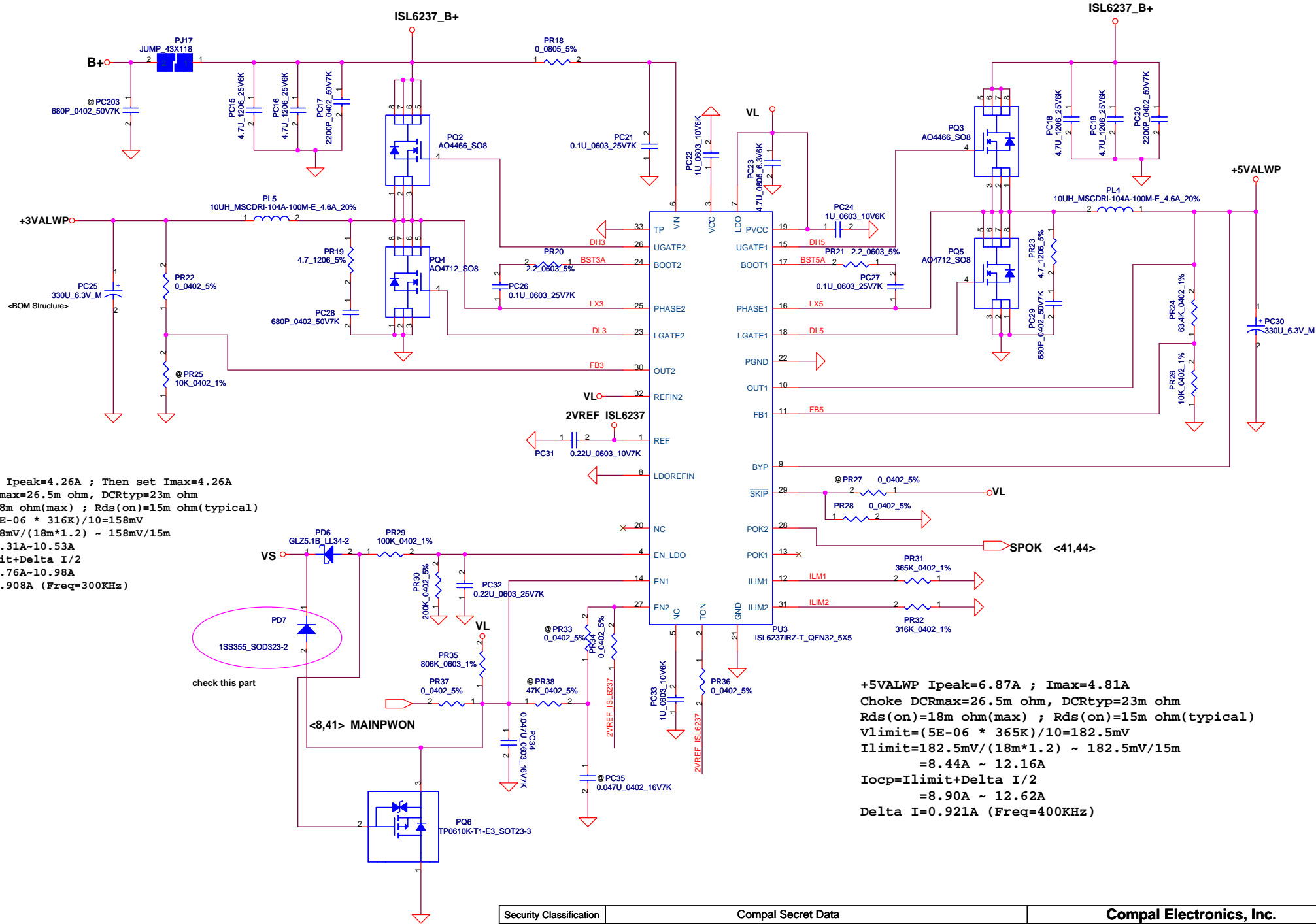
DC231000500



Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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				Size B	Document Number	Rev
Date: Wednesday, May 20, 2009				Sheet	38	of 47



+3.3VALWP Ipeak=4.26A ; Then set I_{max}=4.26A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 316K)/10=158mV
 I_{limit}=158mV/(18m*1.2) ~ 158mV/15m
 =7.31A~10.53A
 I_{ocp}=I_{limit}+Delta I/2
 =7.76A~10.98A
 Delta I=0.908A (Freq=300KHz)

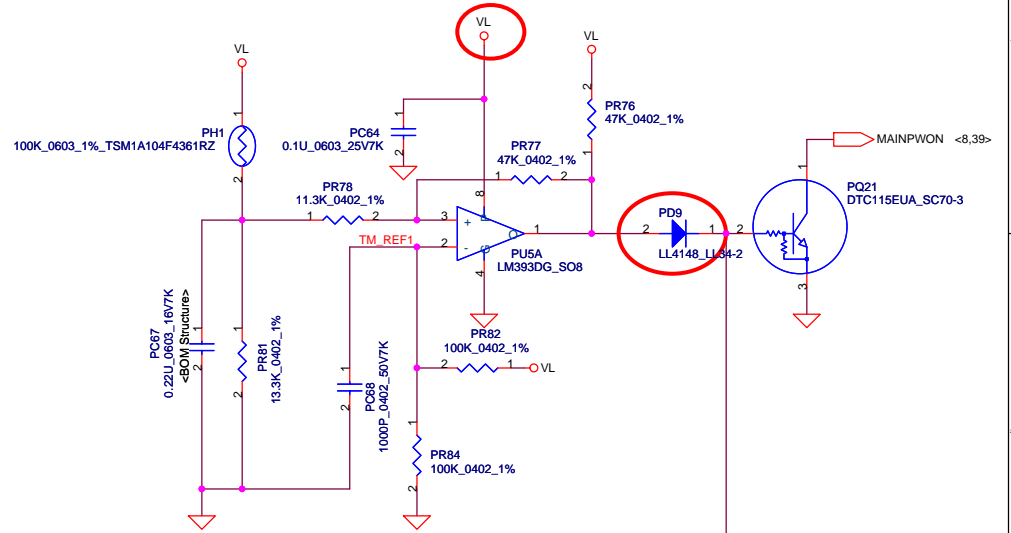
check this part
 1SS355_SOD323-2

<8,41> MAINPWON

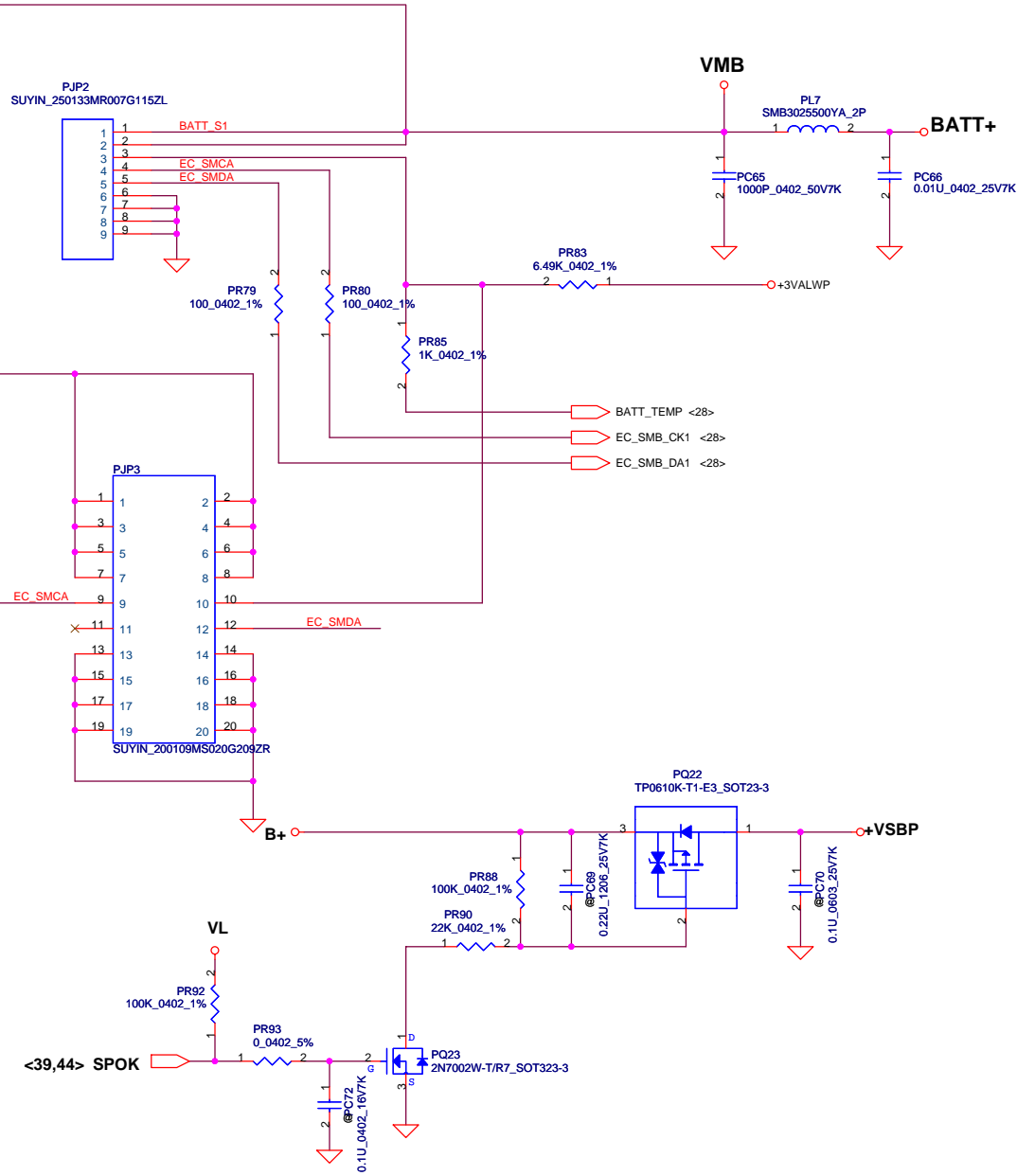
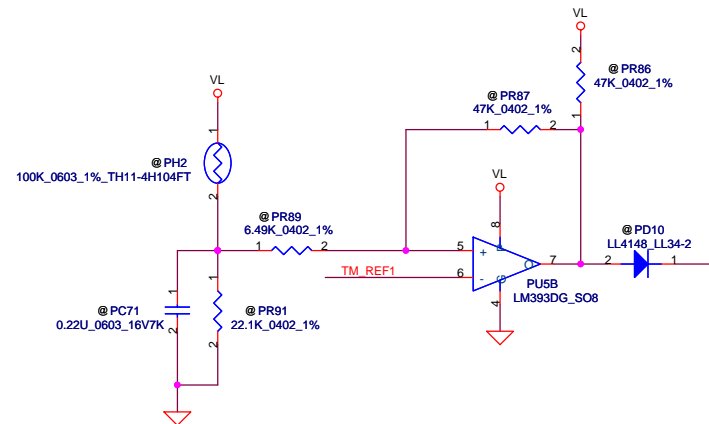
+5VALWP Ipeak=6.87A ; I_{max}=4.81A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 365K)/10=182.5mV
 I_{limit}=182.5mV/(18m*1.2) ~ 182.5mV/15m
 =8.44A ~ 12.16A
 I_{ocp}=I_{limit}+Delta I/2
 =8.90A ~ 12.62A
 Delta I=0.921A (Freq=400KHz)

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				Custom	NCWG0
				Date:	Wednesday, May 20, 2009
				Sheet	39 of 47
				Rev	0.1

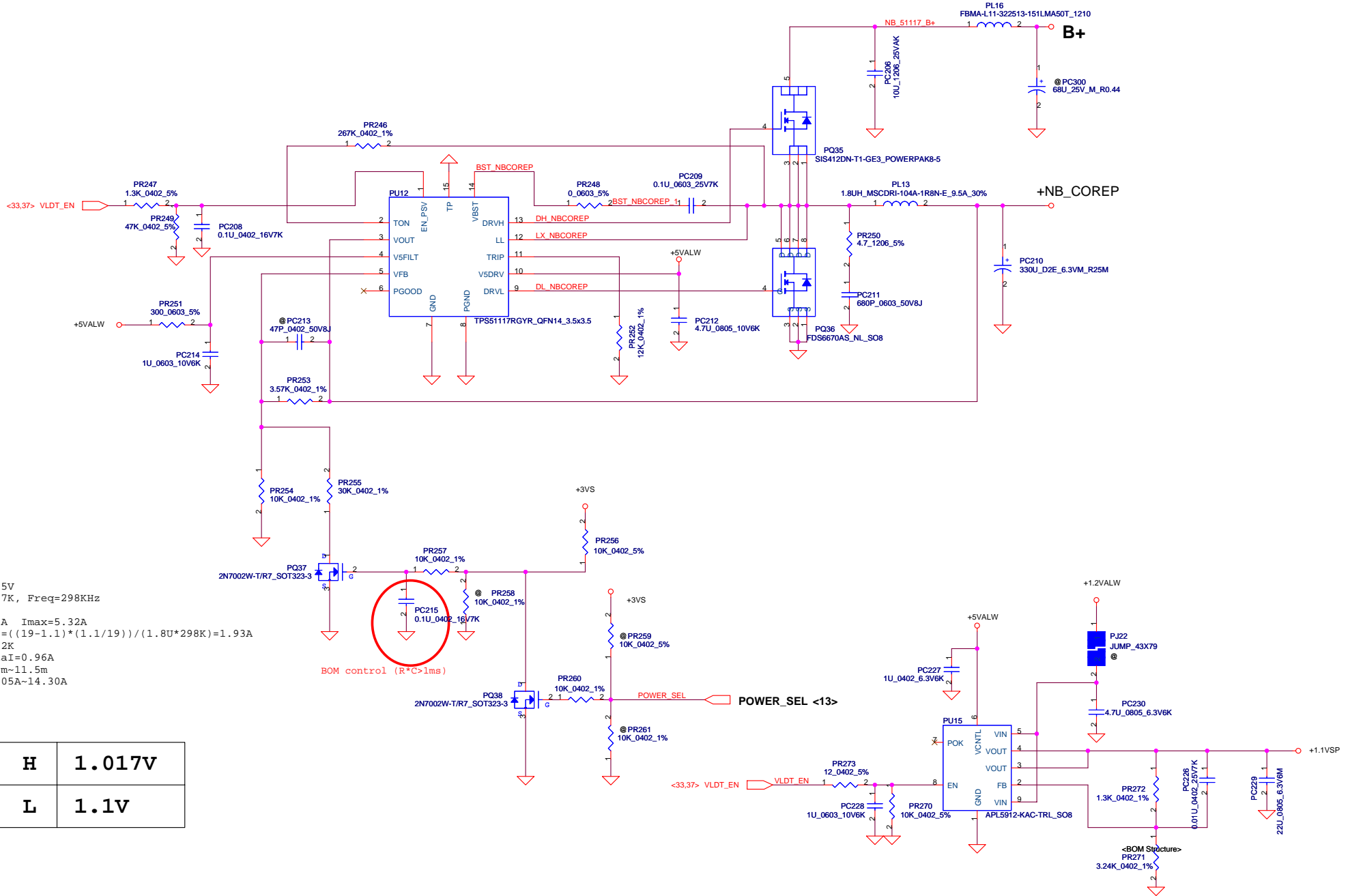
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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Size B	Document Number	NCWGO		Rev	0.1
Date:	Wednesday, May 20, 2009	Sheet	41	of	47

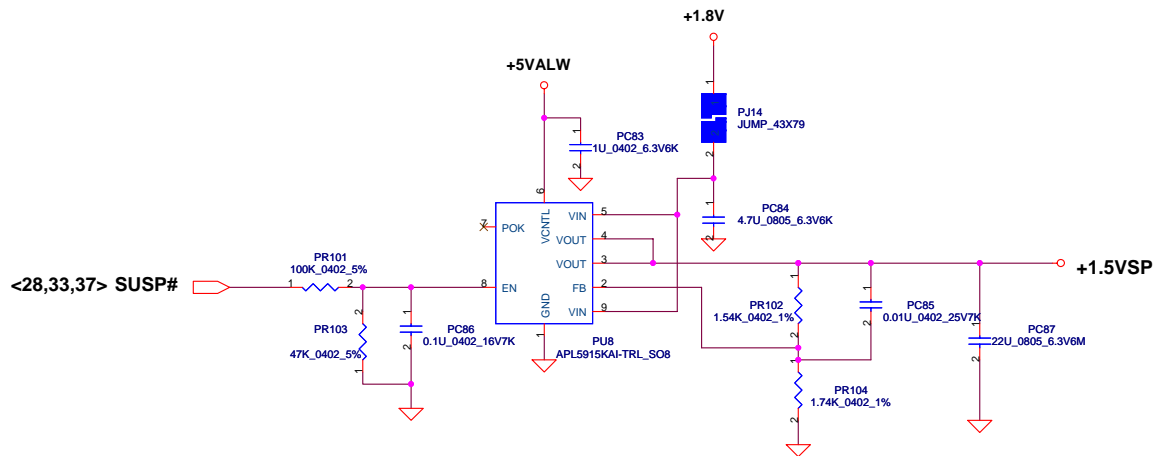
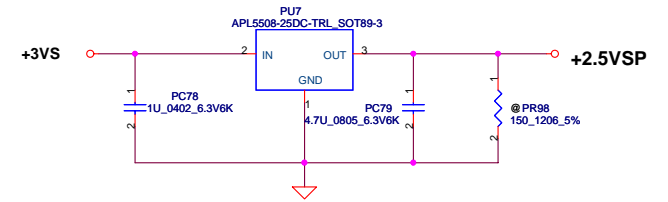
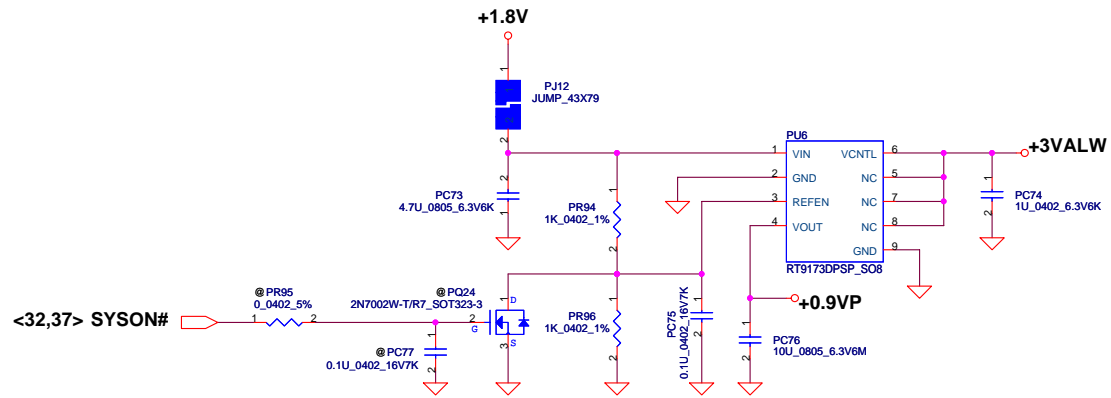


VFB=0.75V
 Rton=267K, Freq=298KHz
 Ipeak=7A Imax=5.32A
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$
 Rtrip=12K
 $1/2\Delta I = 0.96A$
 Rdson=9m~11.5m
 Iocp=9.05A~14.30A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

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				NCWGO	Rev 0.1
				Date: Wednesday, May 20, 2009	Sheet 42 of 47



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Date	Wednesday, May 20, 2009	Sheet	43 of 47	

<28,37> SYSON

VFB=0.75V
Vo=VFB*(1+PR111/PR112)=0.75*(1+14K/10K)=1.8V
Rton=267K=>Fsw=297KHz

Cout ESR=15m ohm
Ipeak=11.96A, Imax=8.372A
Delta I=((19-1.8)*(1.8/19))/(L*Fsw)
((19-1.8)*(1.8/19))/(1.8u*297000)=3.048A
=>1/2DeltaI=1.524A

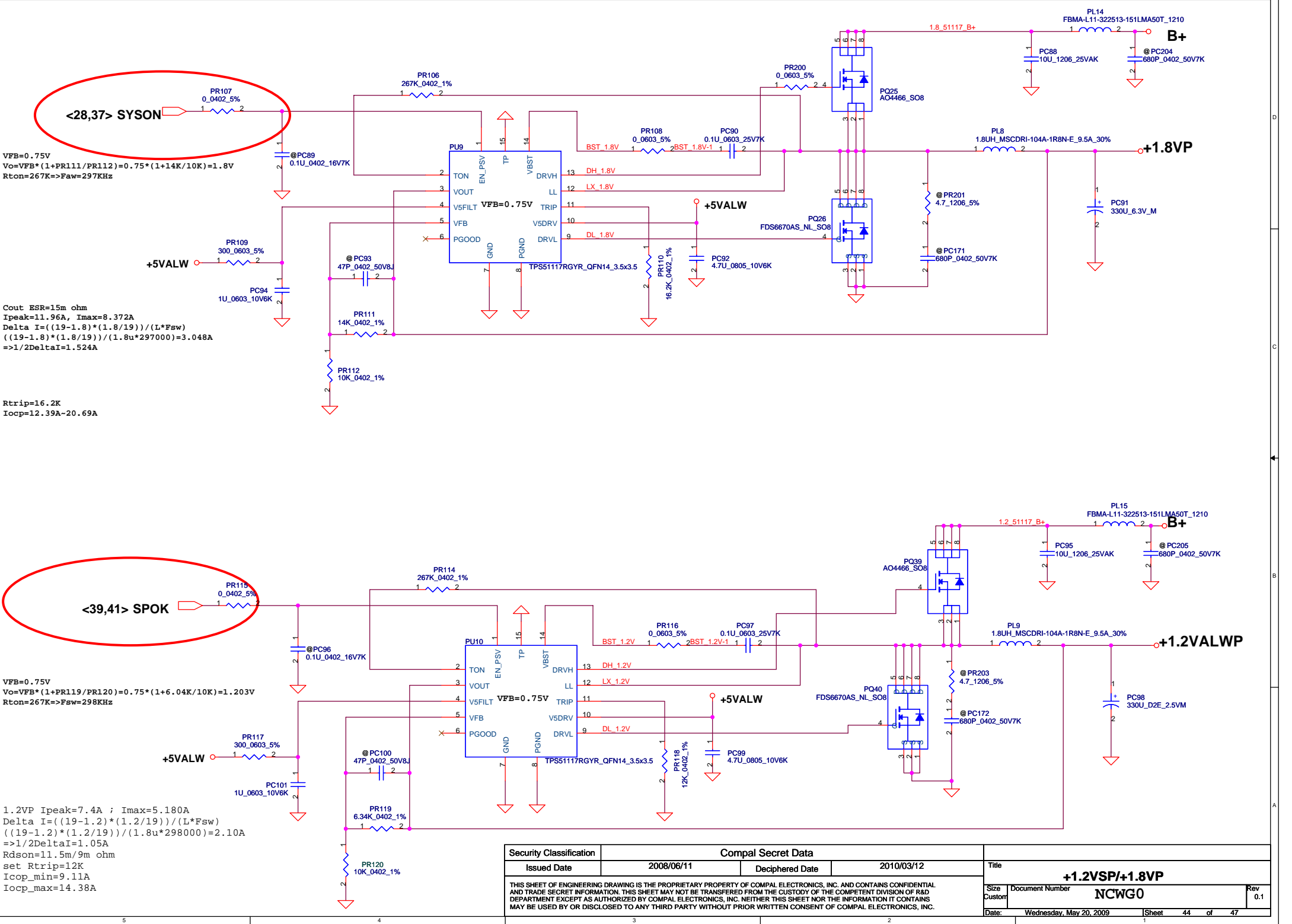
Rtrip=16.2K
Iocp=12.39A-20.69A

<39,41> SPOK

VFB=0.75V
Vo=VFB*(1+PR119/PR120)=0.75*(1+6.04K/10K)=1.203V
Rton=267K=>Fsw=298KHz

1.2VP Ipeak=7.4A ; Imax=5.180A
Delta I=((19-1.2)*(1.2/19))/(L*Fsw)
((19-1.2)*(1.2/19))/(1.8u*298000)=2.10A
=>1/2DeltaI=1.05A
Rdson=11.5m/9m ohm
set Rtrip=12K
Icop_min=9.11A
Icop_max=14.38A

Security Classification		Compal Secret Data		Title	
Issued Date	2008/06/11	Deciphered Date	2010/03/12	+1.2VSP/+1.8VP	
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Date:	Wednesday, May 20, 2009	Sheet	44	of	47
Rev	0.1				



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
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Security Classification		Compal Secret Data		Title	
Issued Date	2008/06/11	Deciphered Date	2010/03/12	PIR(PWR)	
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				Date: Wednesday, May 20, 2009	Rev 0.1
				Sheet 46 of 46	

Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
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Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2010/03/12	PIR-HW & Option Component	
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				Sheet 47 of 47	

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