

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

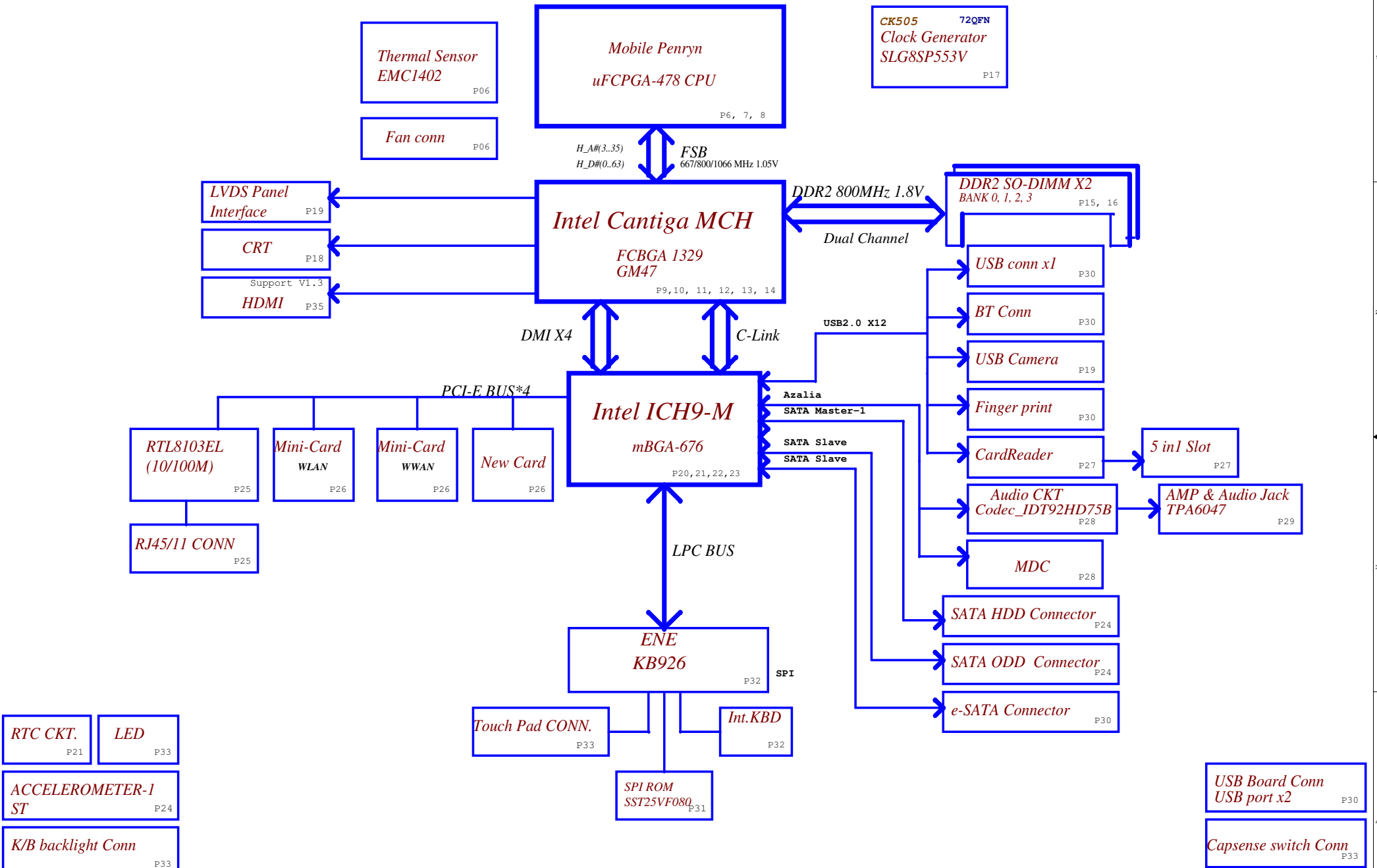
2009-02-16

REV:1.0



Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet	
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Montevina Consumer UMA



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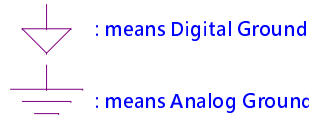
Block Diagram

Voltage Rails

○ MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +2.5VS +1.8V
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note:



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

USB-0	Right side(with eSATA)
USB-1	Left side
USB-2	Left side
USB-3	Cardreader
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

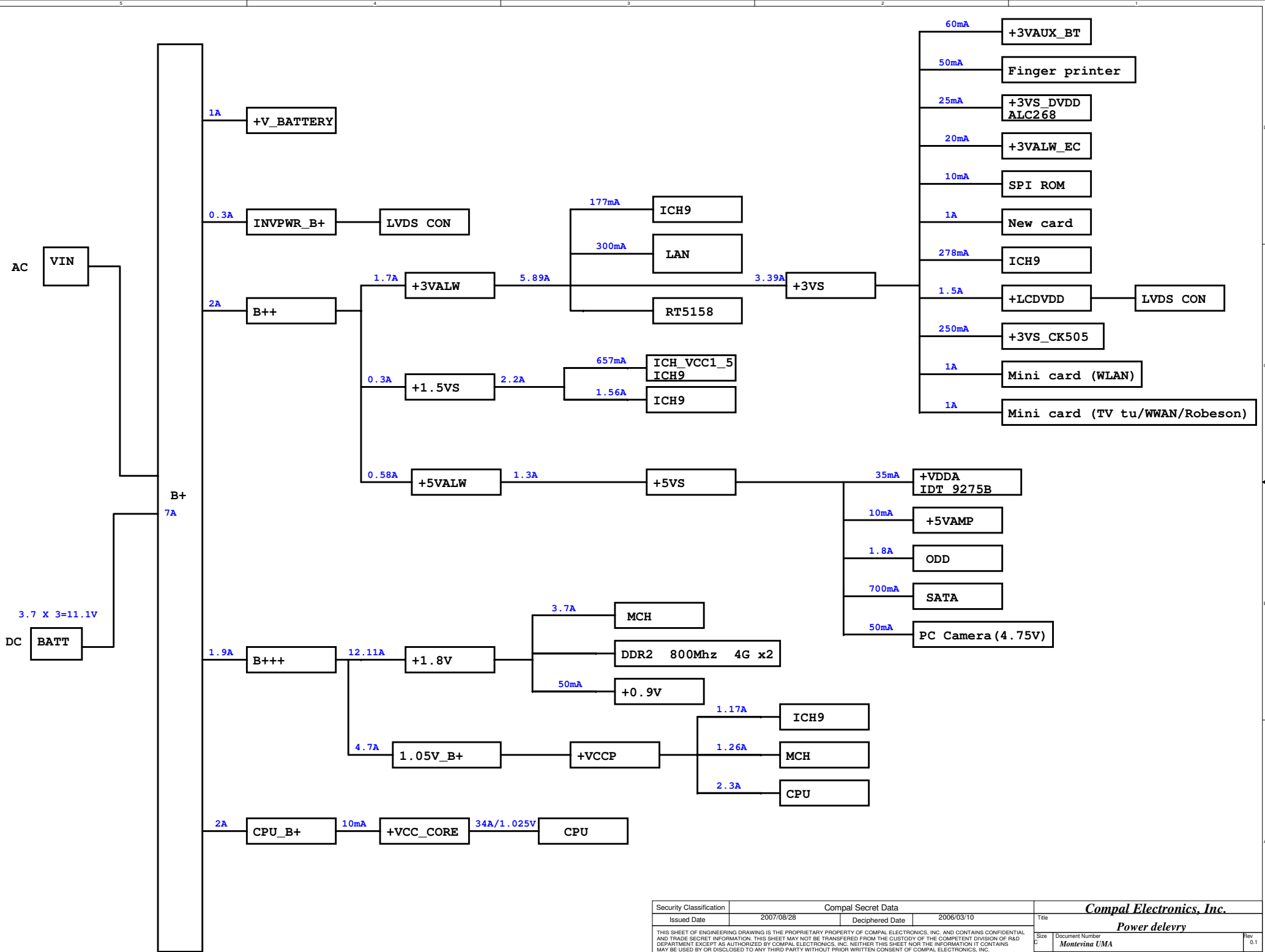
PCIe-1	WWAN
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	New Card

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10 10 0 0 0
DDR SO-DIMM 1	A4	10 10 0 1 0
CLOCK GENERATOR (EXT.)	D2	11 0 1 0 1 0

SMBUS Control Table

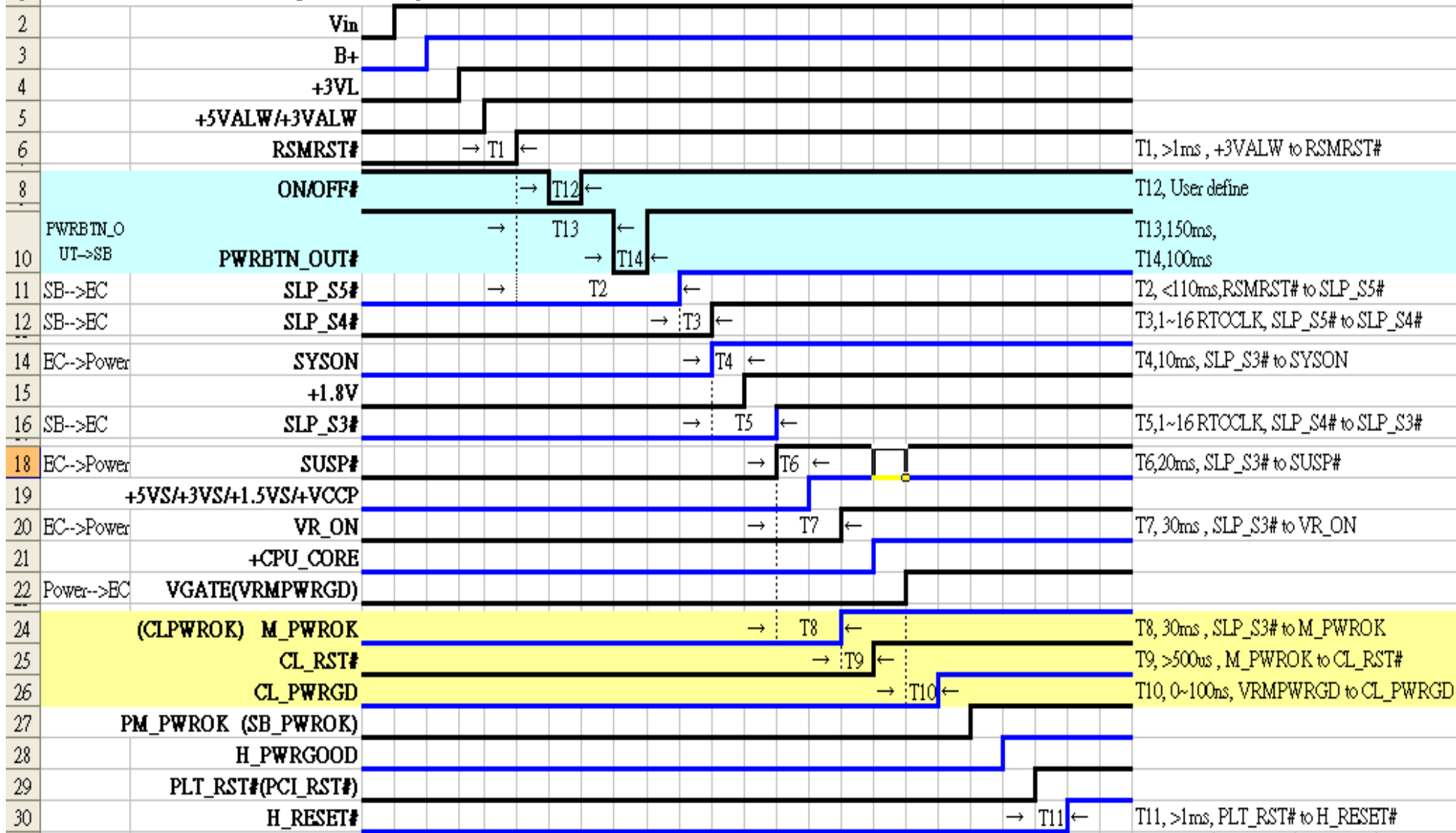
	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

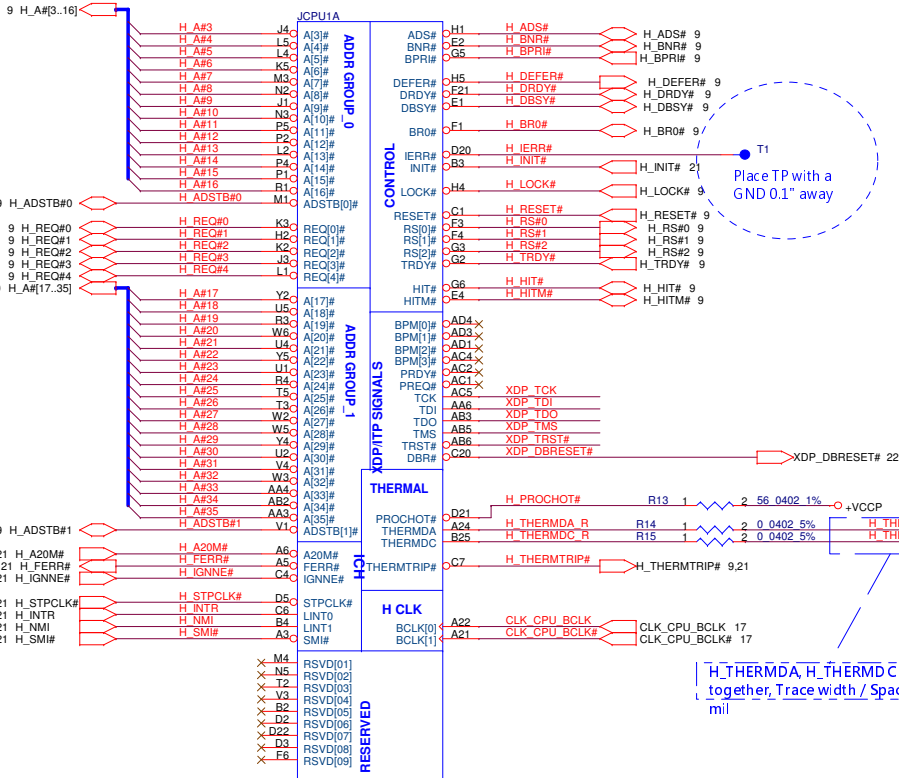


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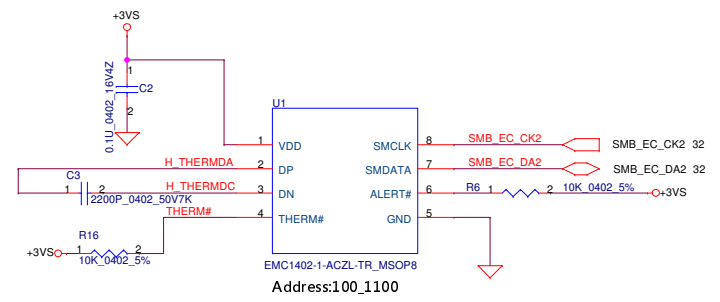
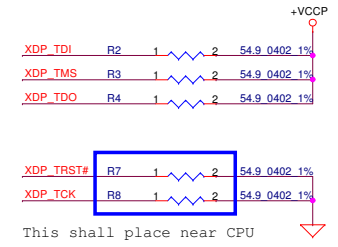
JAL50 power sequence AC mode

96.09.03.

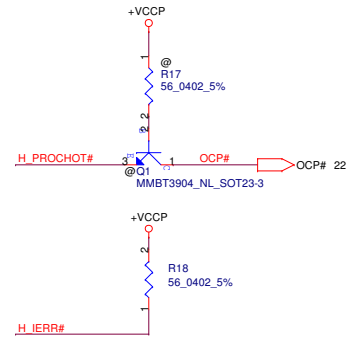
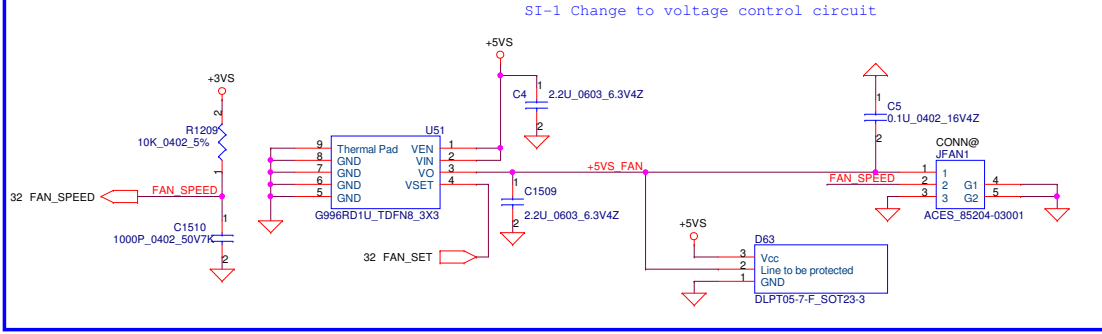




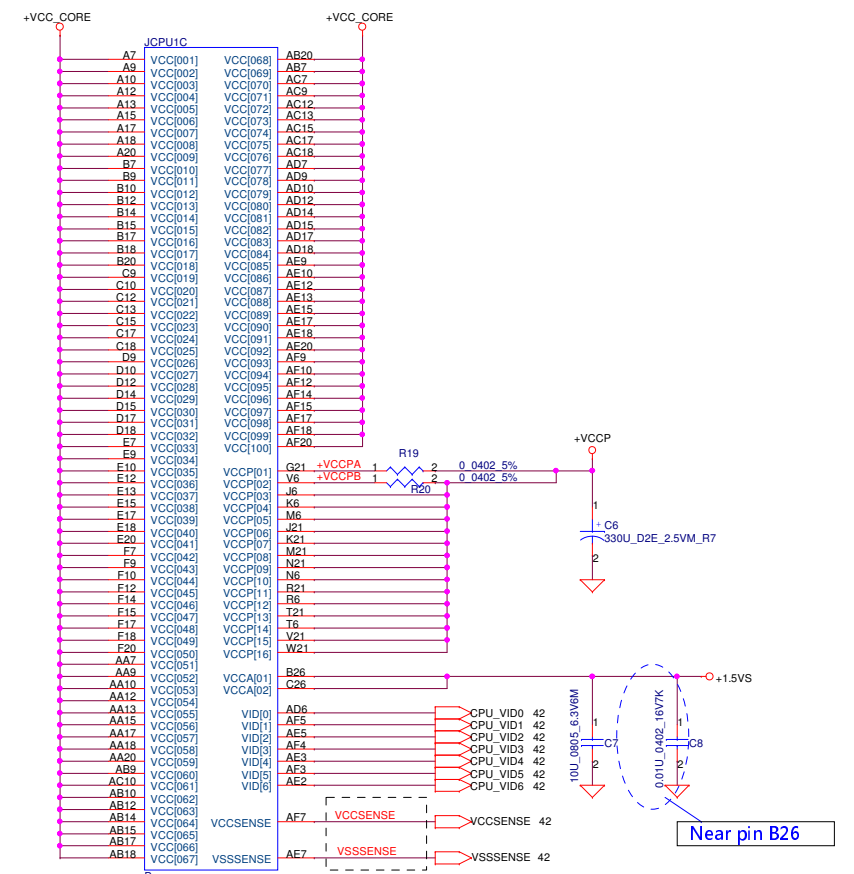
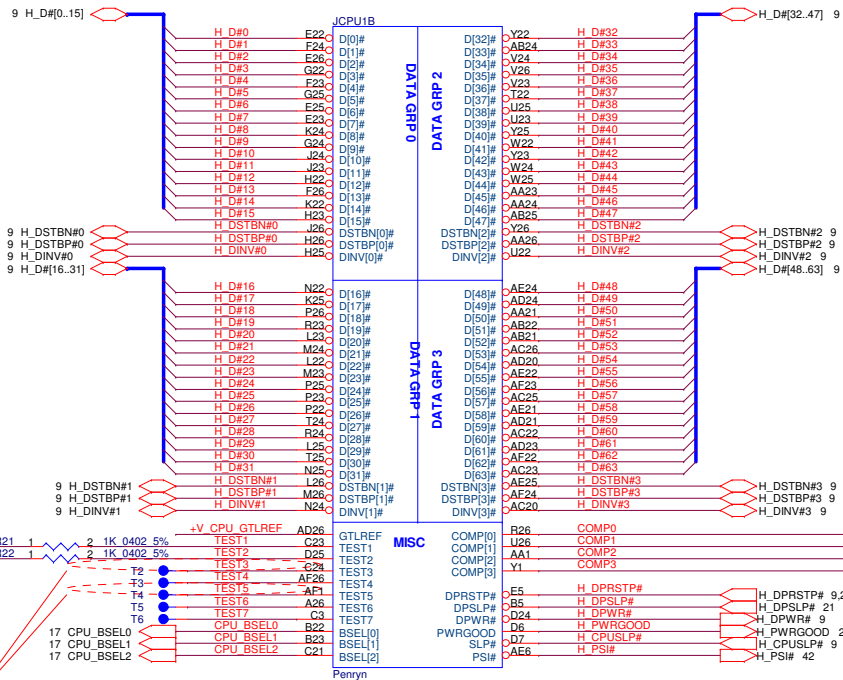
ITP-XDP Connector



Fan Control circuit



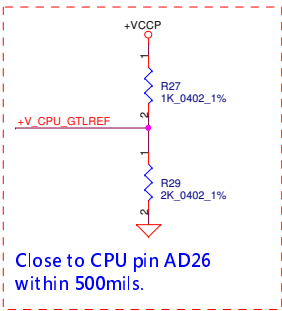
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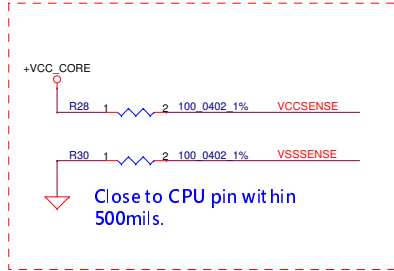
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

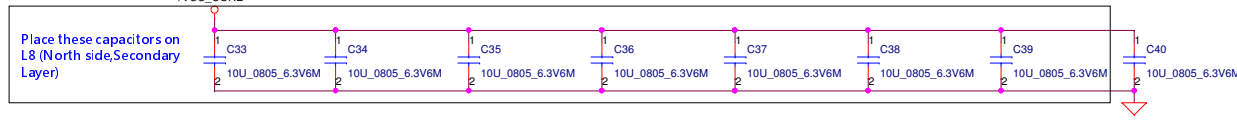
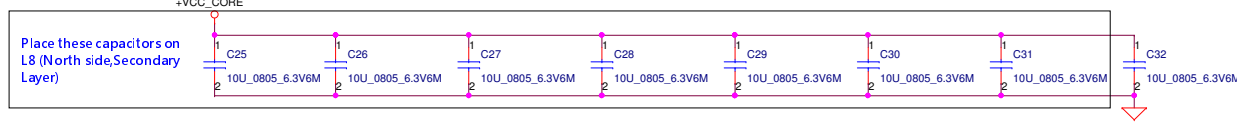
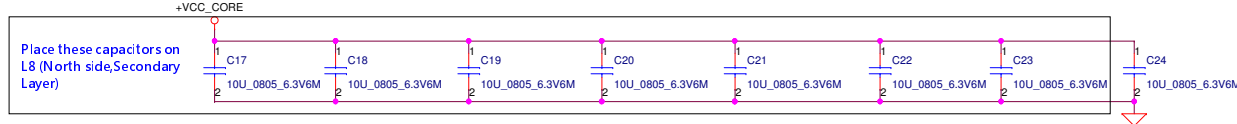
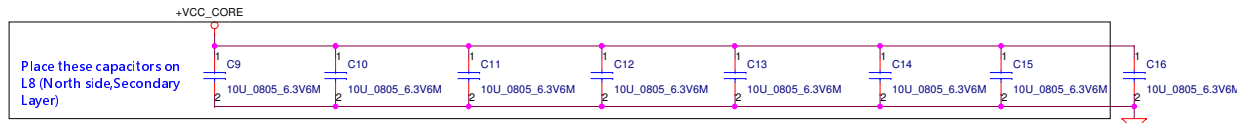
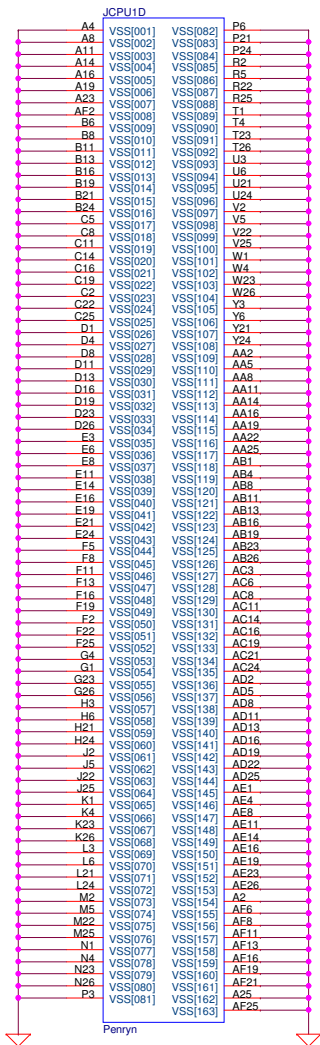
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



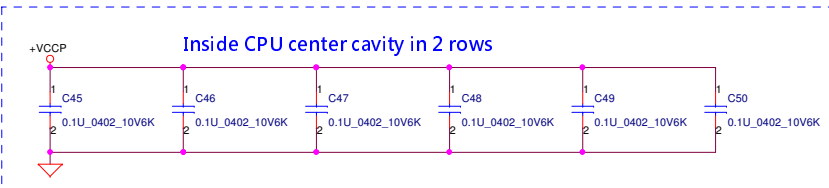
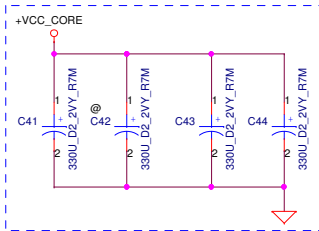
Length match within 25 mils. The trace width/space/other is 20/7/25.



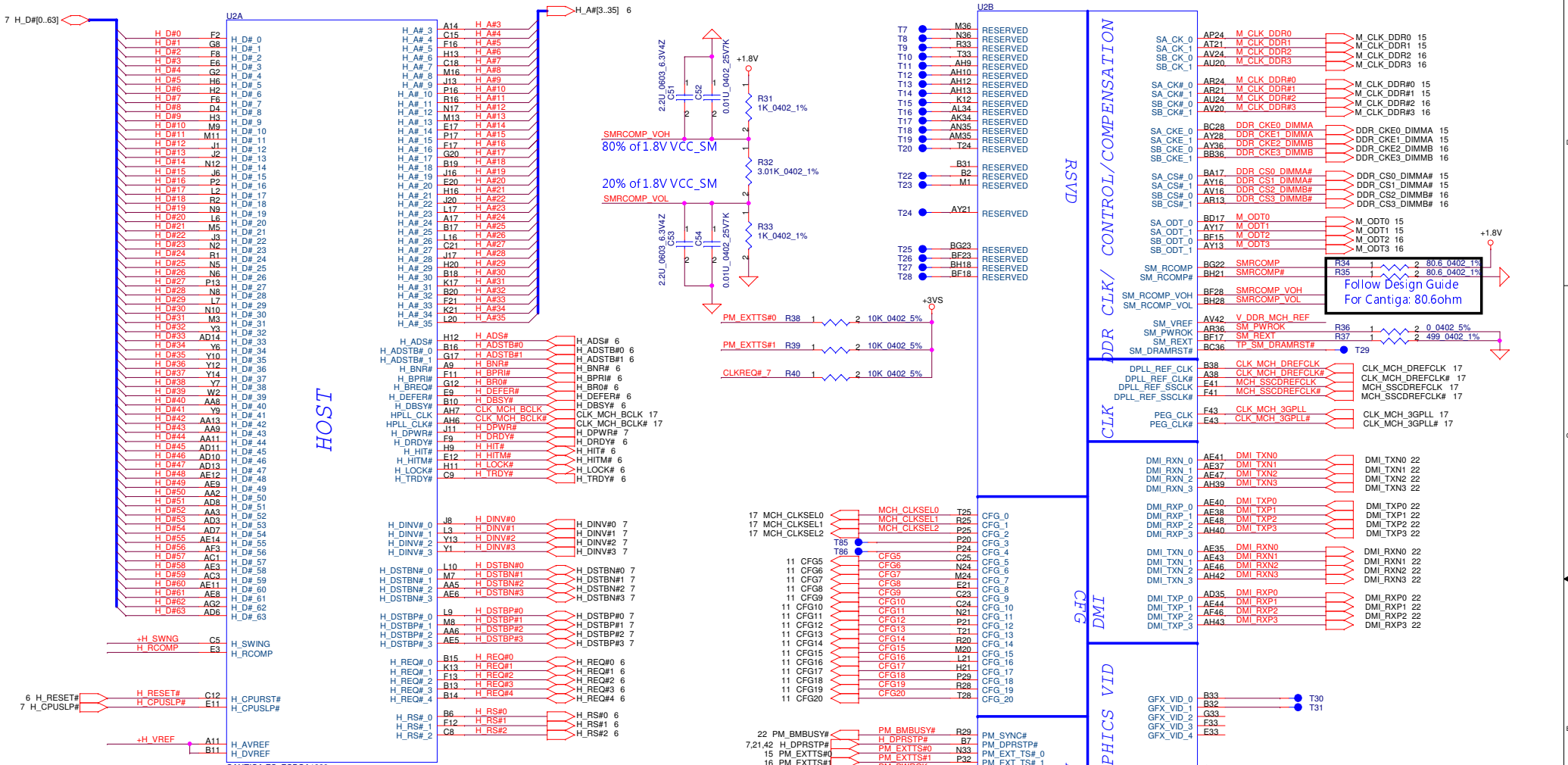


Mid Frequency Decoupling

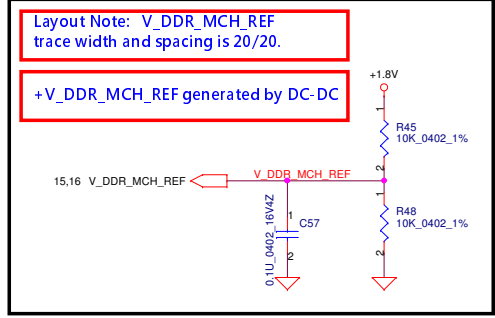
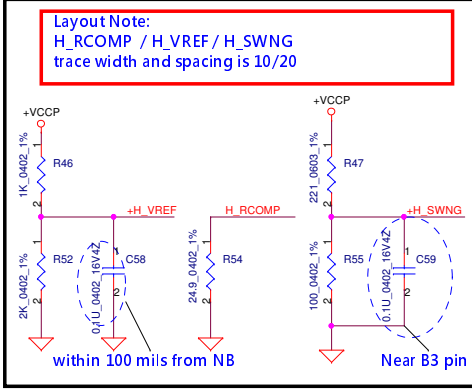
Near CPU CORE regulator
 ESR <= 1.5m ohm
 Capacitor > 1980uF



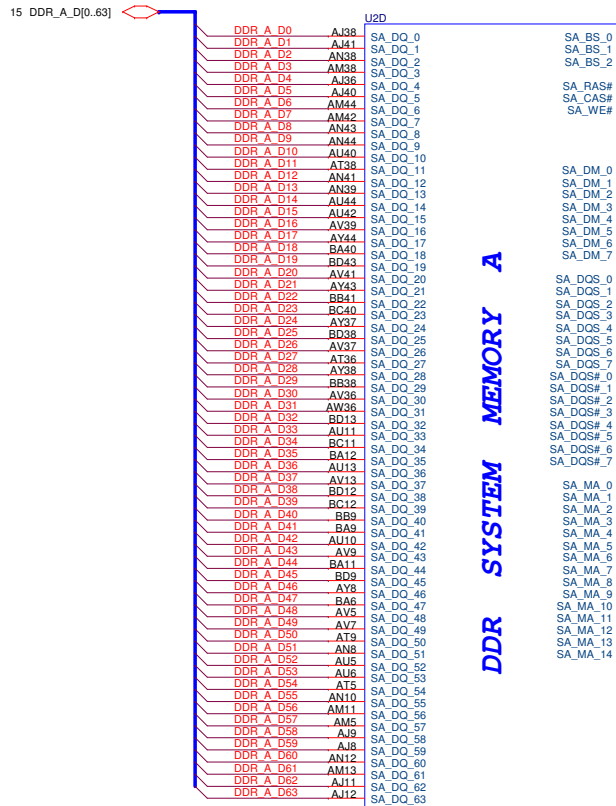
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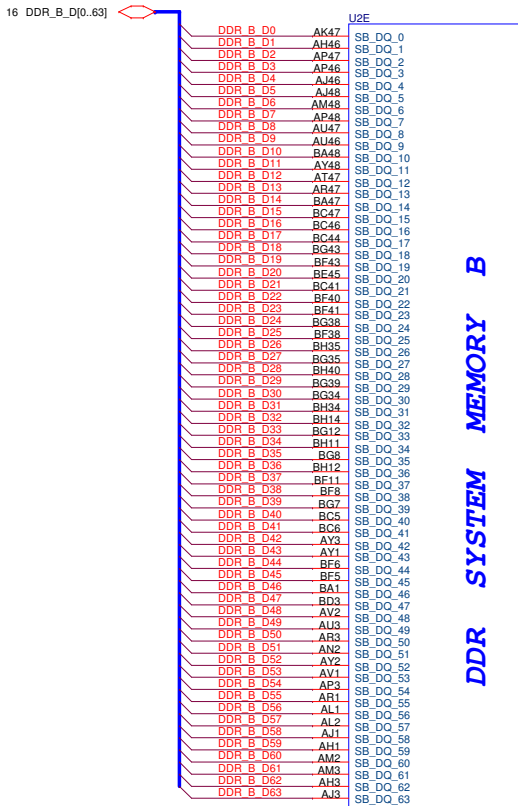
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



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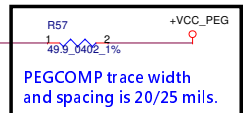
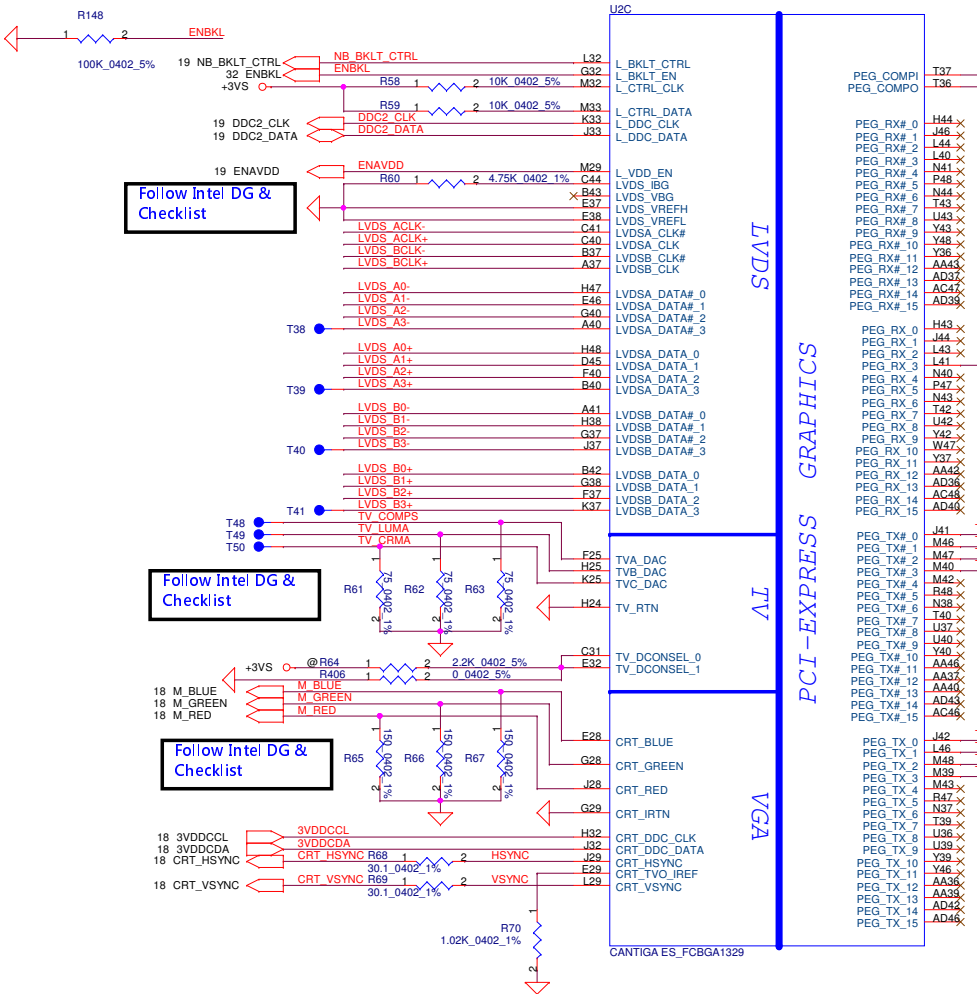


CANTIGA ES_FCBGA1329



CANTIGA ES_FCBGA1329

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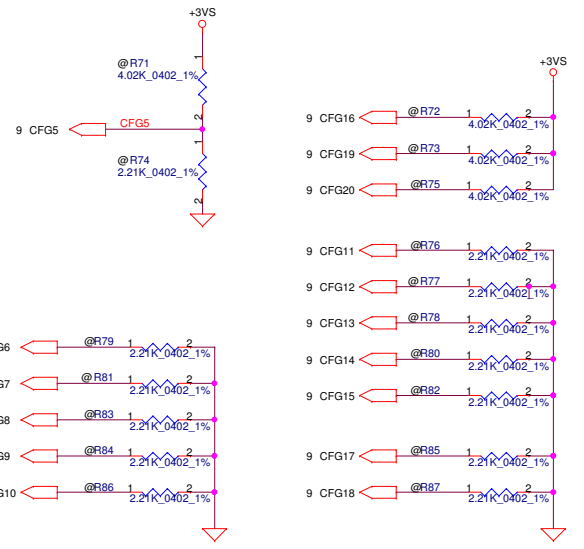
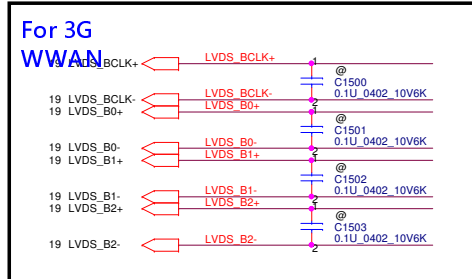
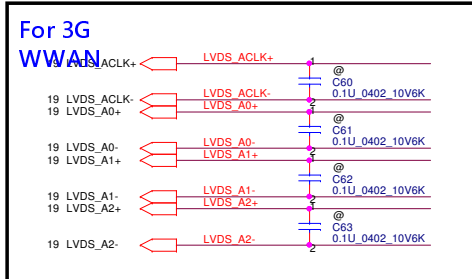
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 001 = 600MHz 010 = 800MHz 011 = 1000MHz
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 1 = DMI x *
CFG6	0 = The iTPM Host Interface is enabled 1 = The iTPM Host Interface is disabled
CFG7 (Intel Management Engine Crypto strap)	0 = iTPM chip set with no confidentiality 1 = iTPM chip set with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Disabled 1 = Enabled *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode 10 = All Z Mode 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operating 1 = Both PCIe/SDVO are operating simultaneously *

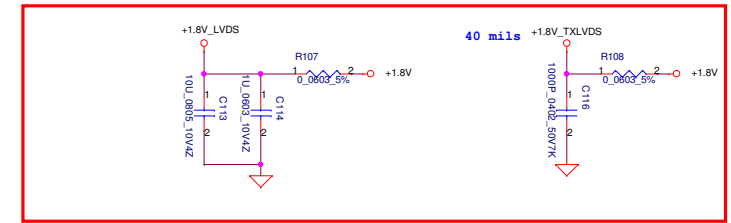
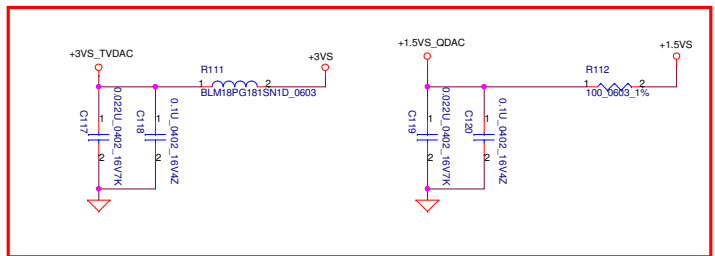
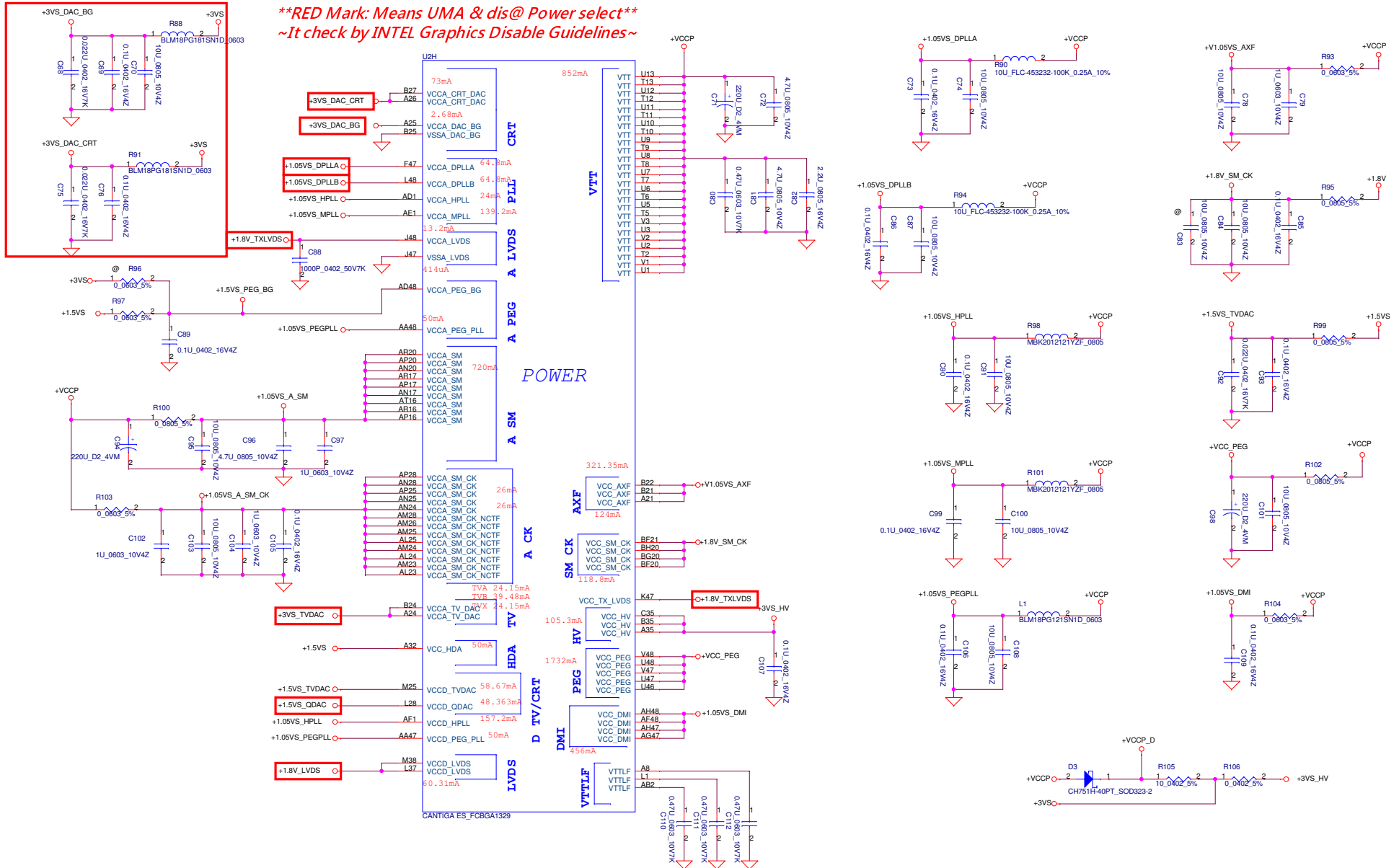
Follow Intel DG & Checklist

Follow Intel DG & Checklist

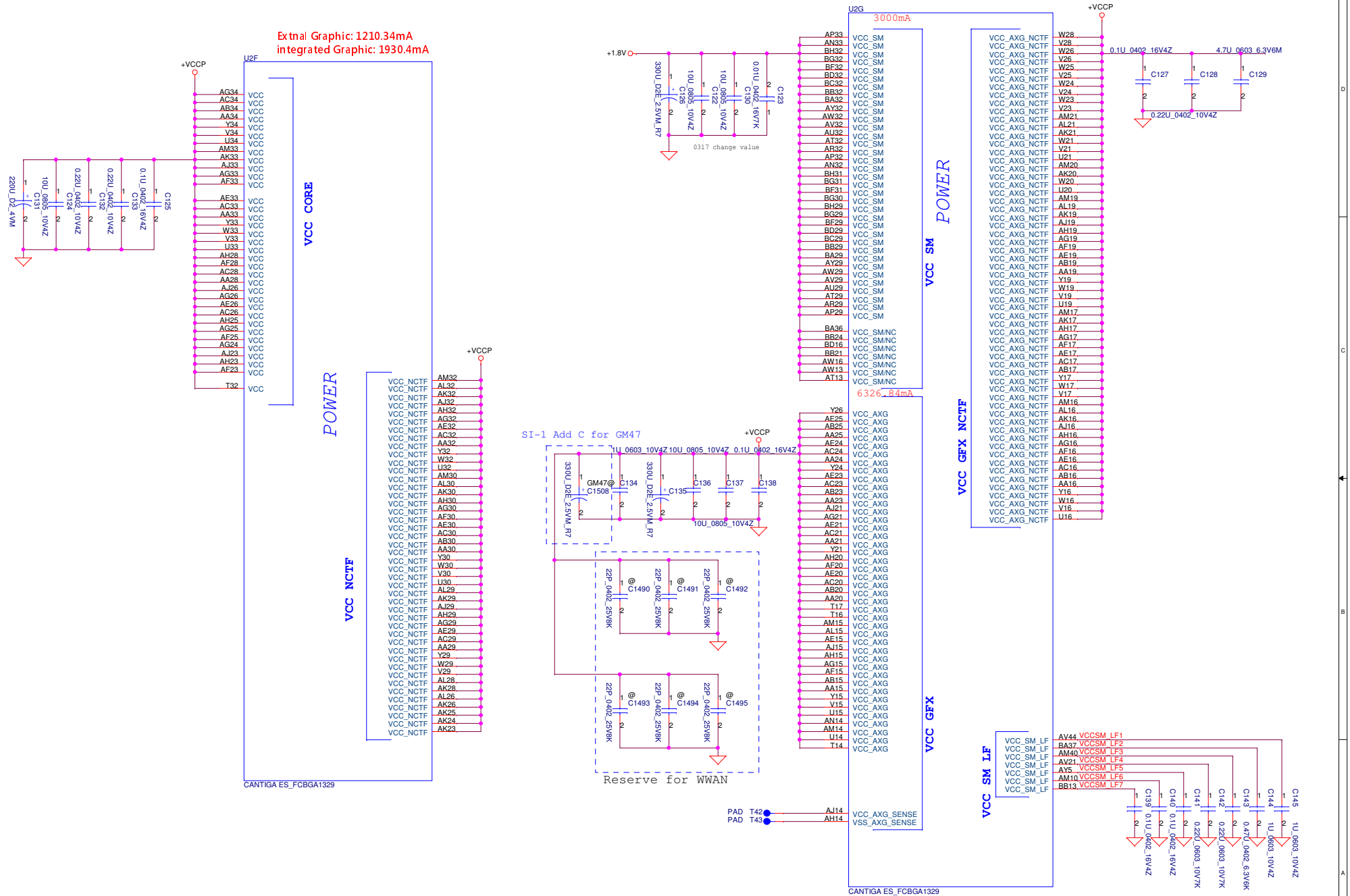
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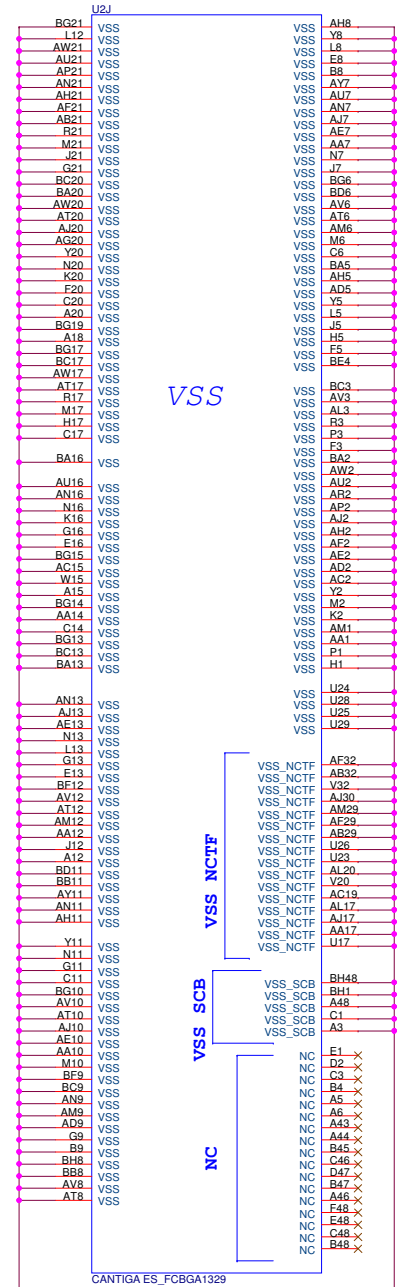
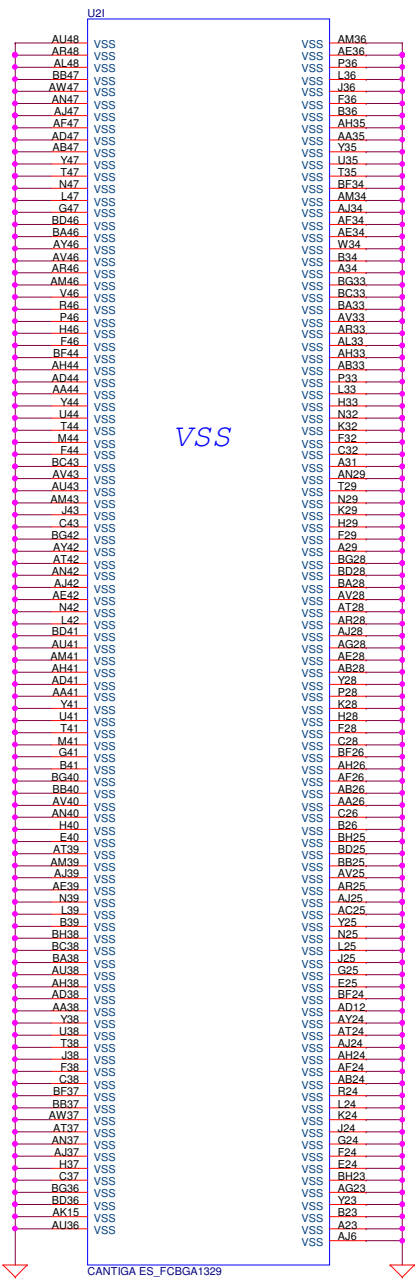
****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable Guidelines~



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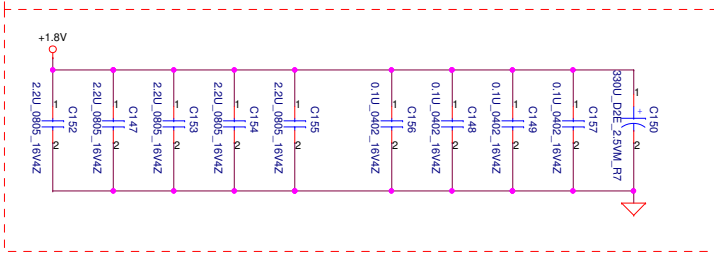
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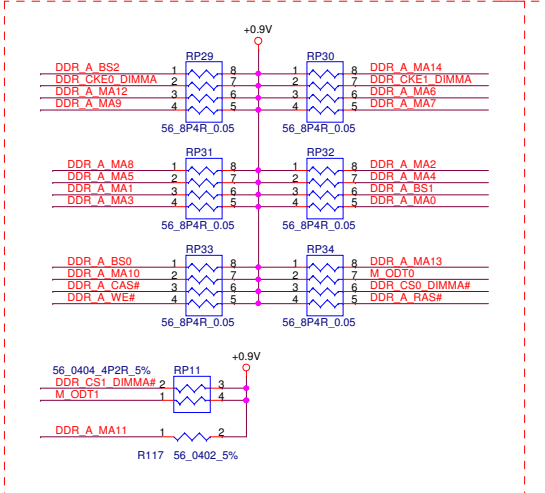
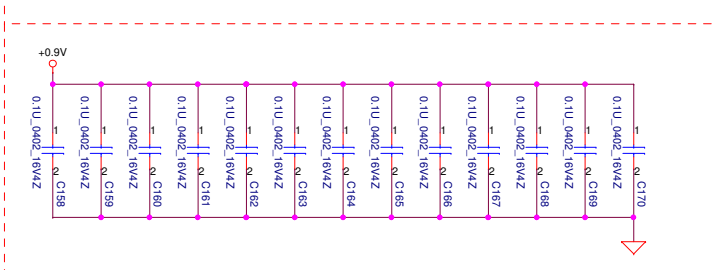
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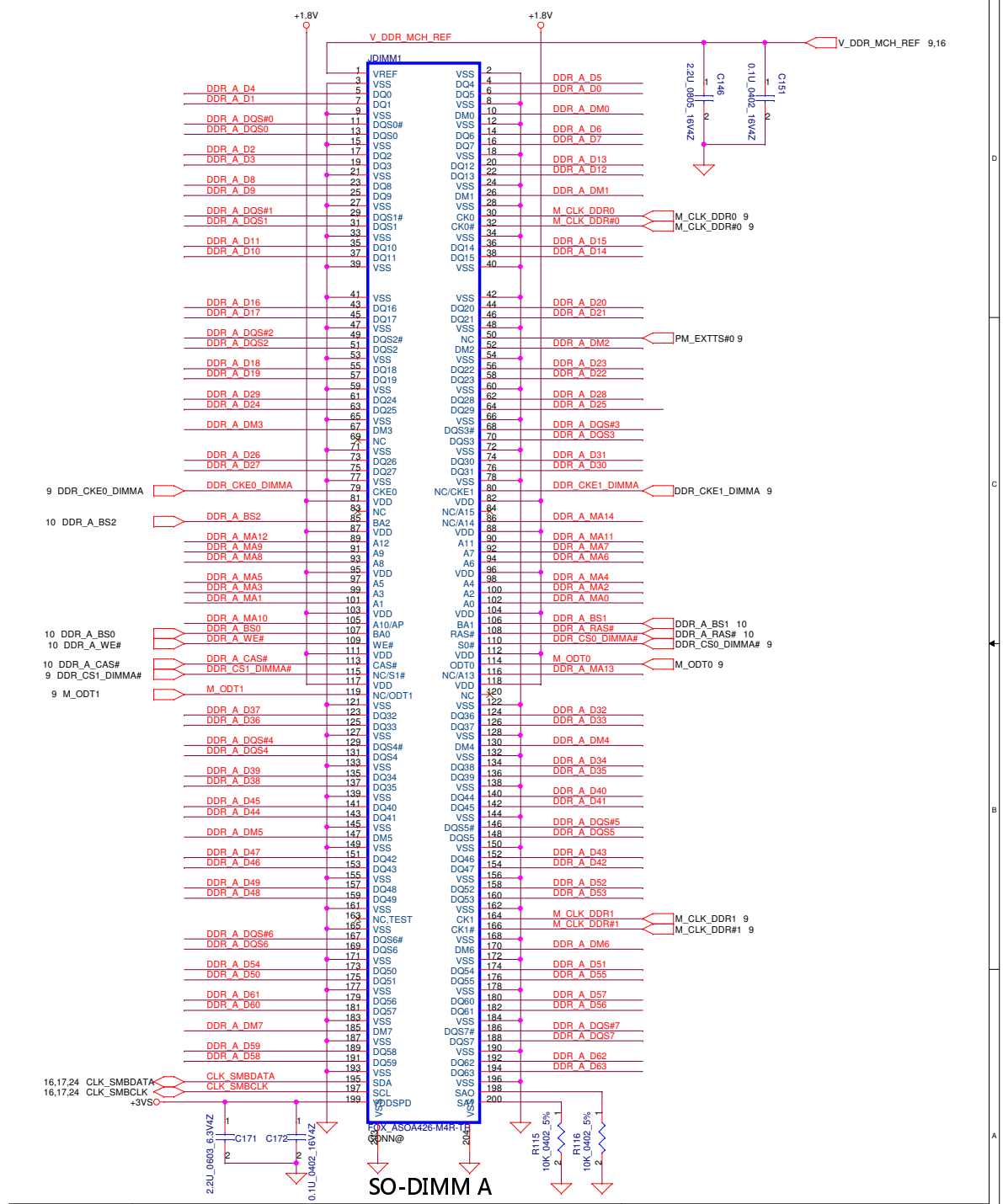
Layout Note:
Place near JP3



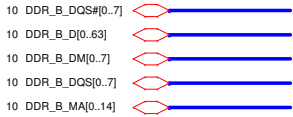
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5



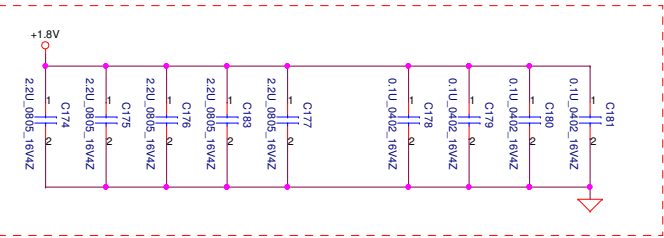
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



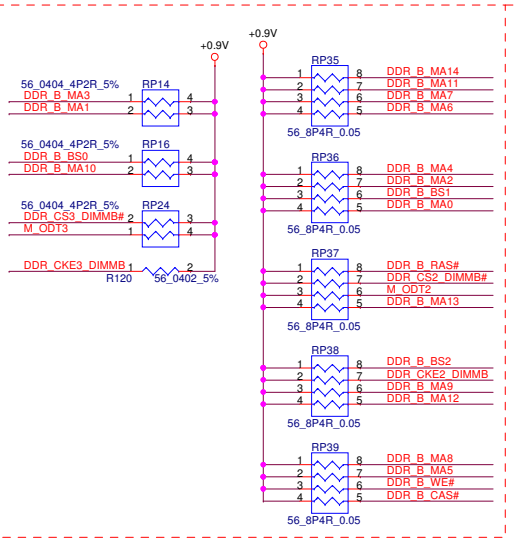
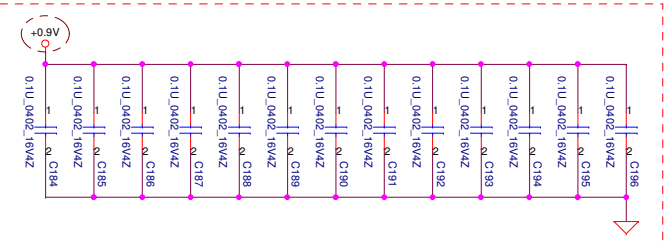
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Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5

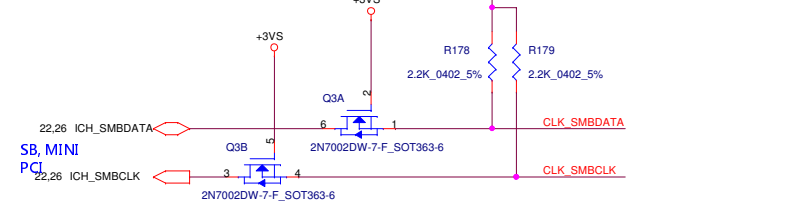
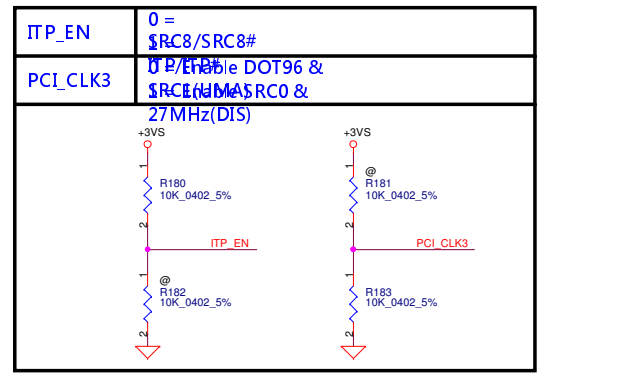
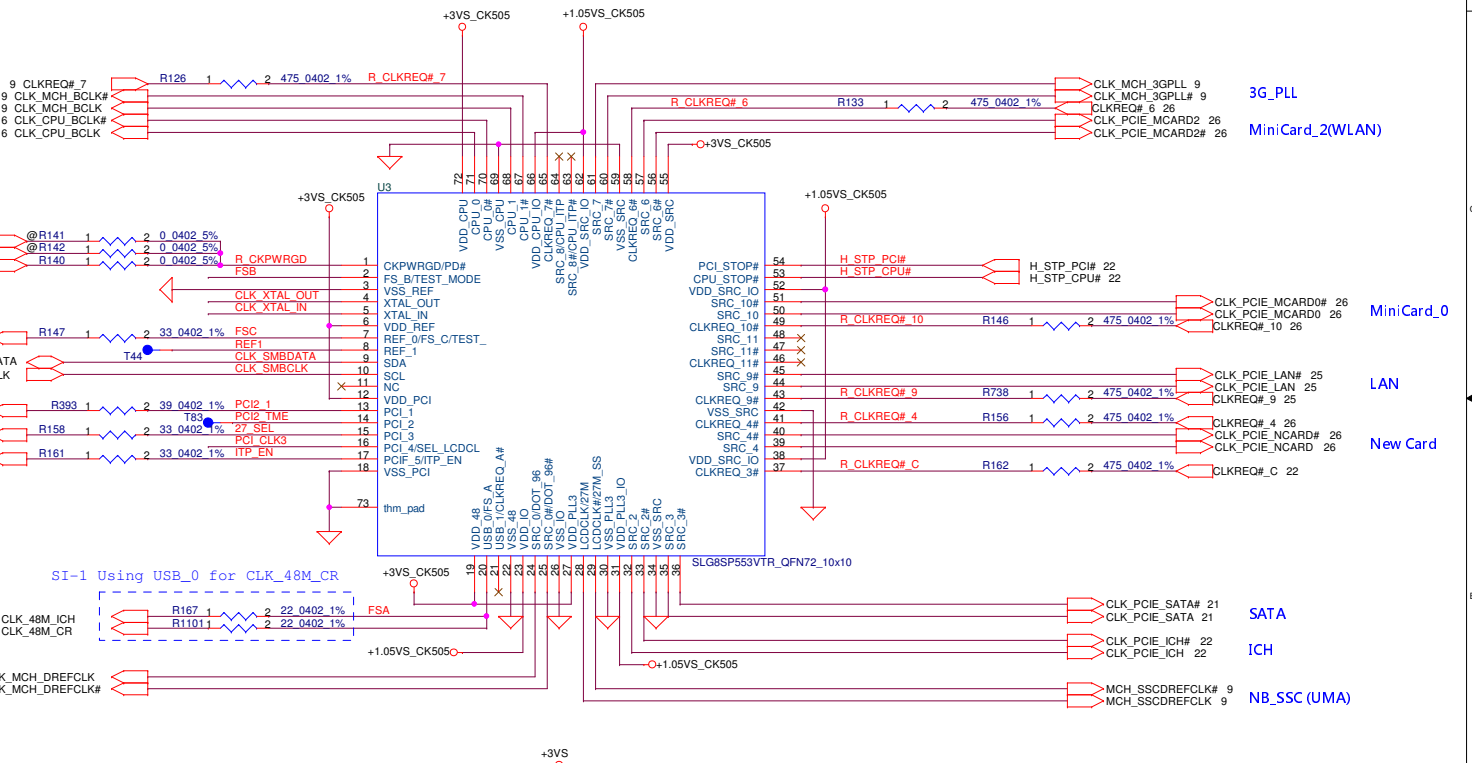
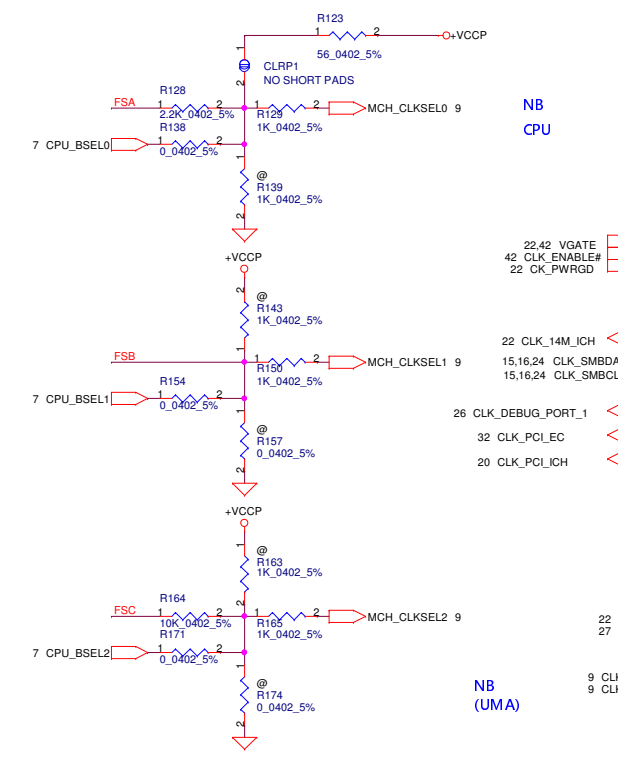
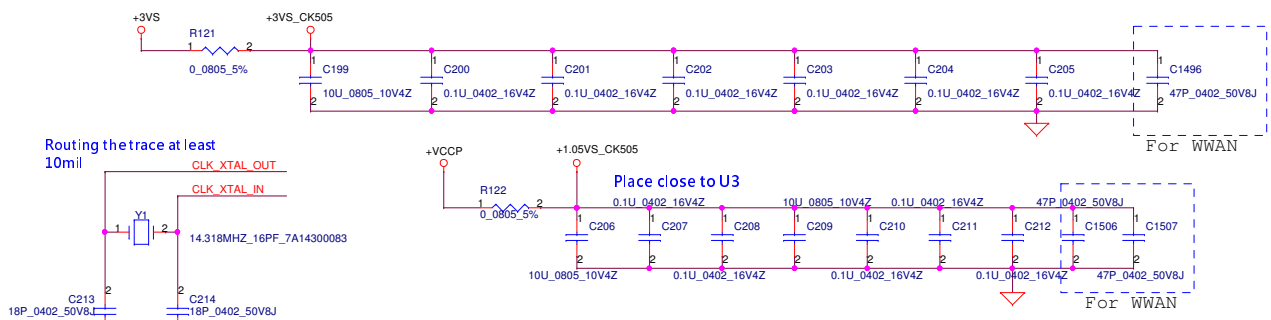


Layout Note:
Place these resistor closely JP3, all trace length Max = 1.5"



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Date	Wednesday, February 18, 2009	Sheet	16	of	46

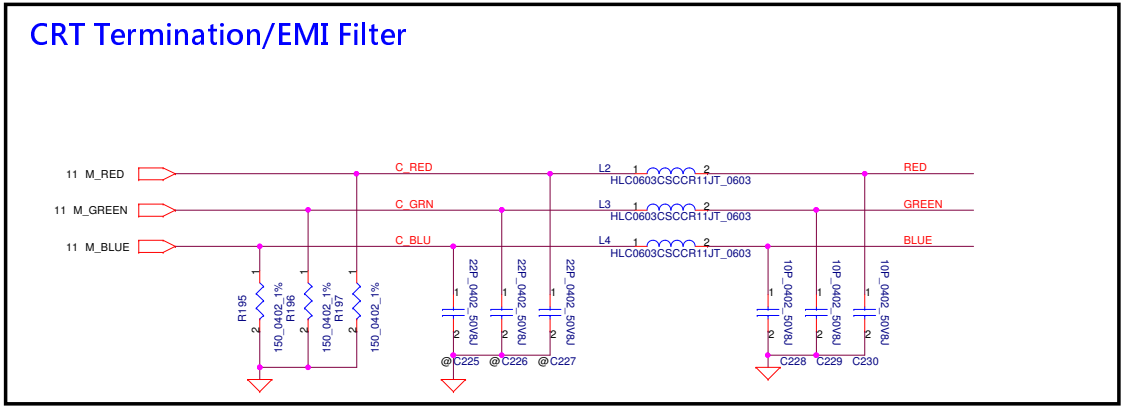
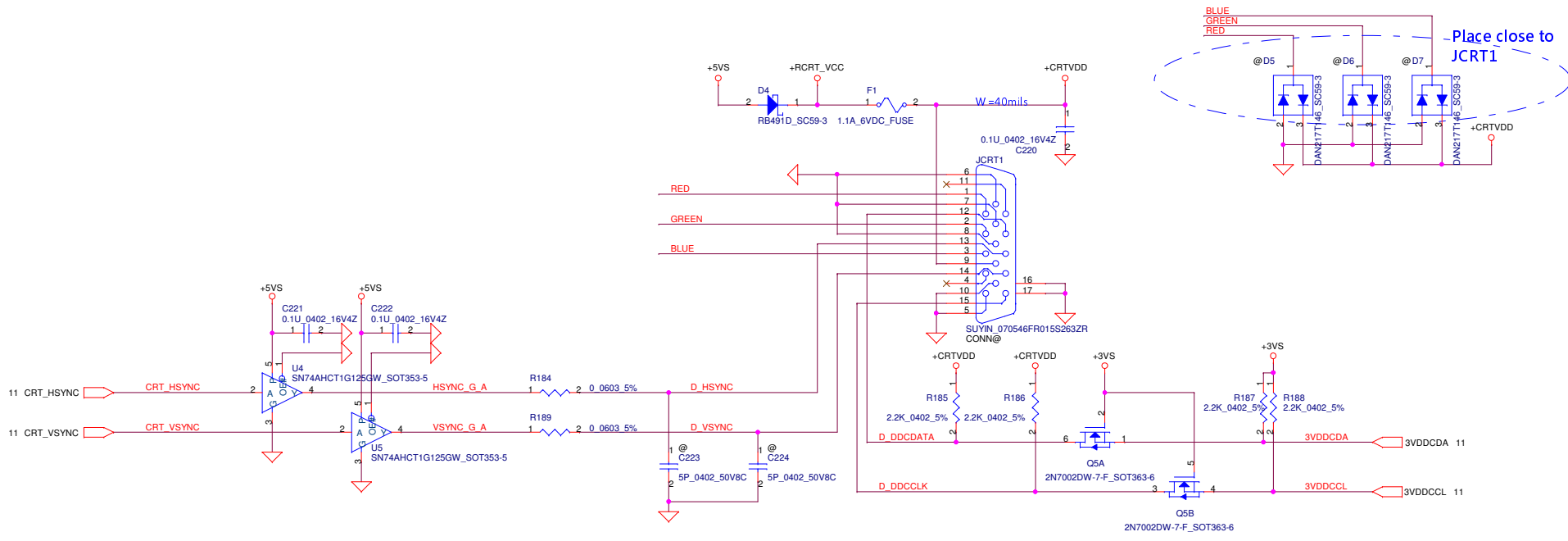
FSC	FSA	FSE	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



EMI			
@C1482	2	1	CLK 48M_CR
5P_0402_50V8C	2	1	CLK 48M_ICH
5P_0402_50V8C	2	1	CLK 14M_ICH
C216	2	1	CLK PCI_ICH
12P_0402_50V8J	2	1	CLK PCI_EC
@C217	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK PCI_EC
@C218	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK PCI_EC
@C219	2	1	CLK DEBUG_PORT_1

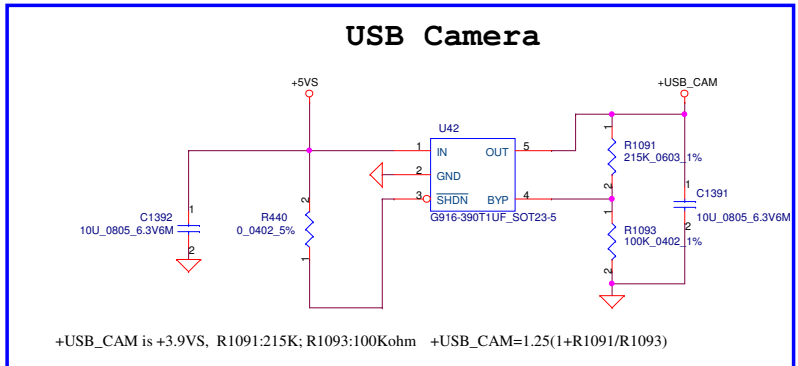
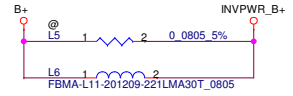
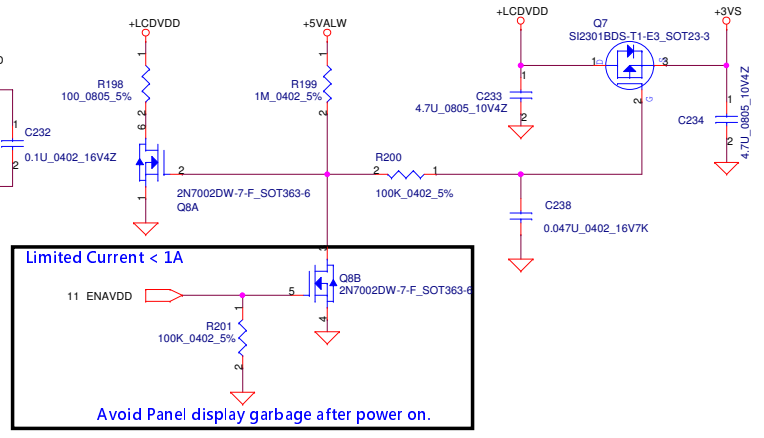
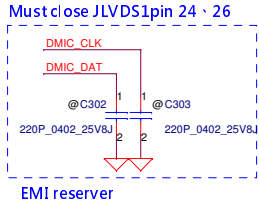
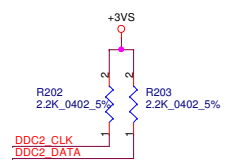
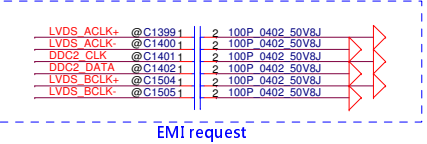
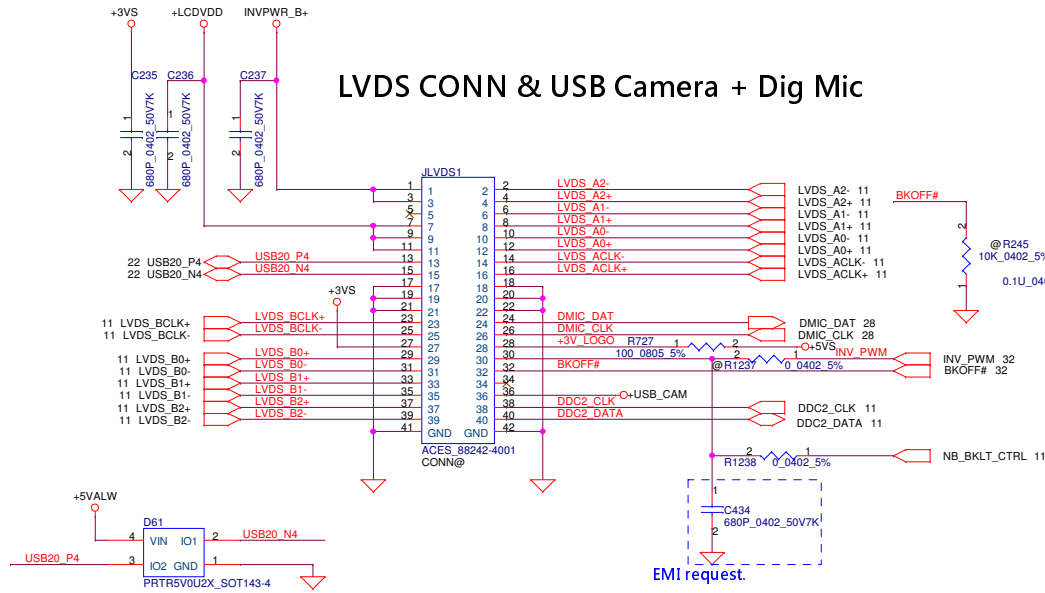
Install C217,C218,C219 for WWAN noise

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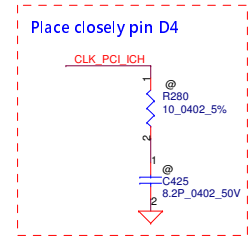
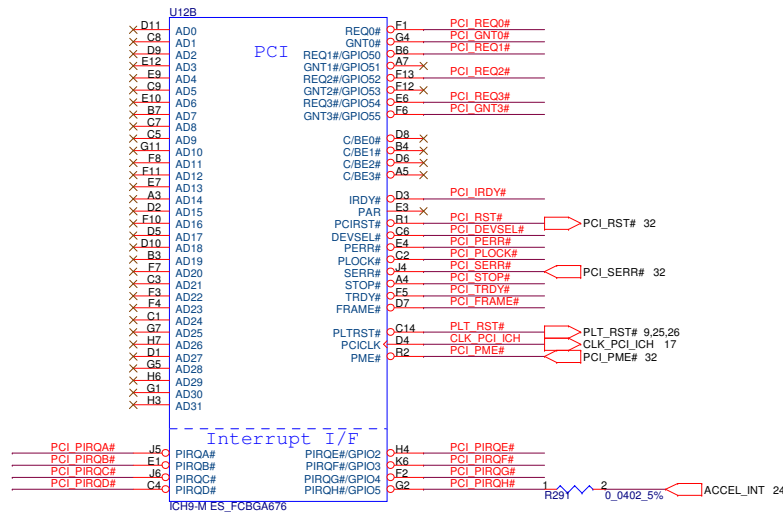
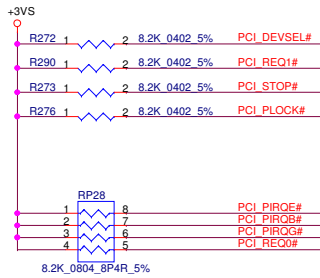
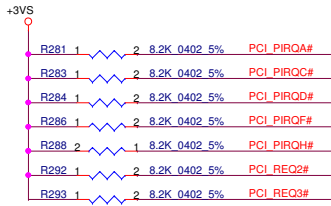
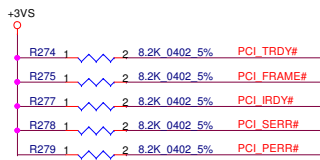


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				Montevina UMA
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LVDS CONN & USB Camera + Dig Mic

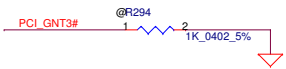


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				Montevina UMA	0.1
Date: Wednesday, February 18, 2009				Sheet	19 of 46



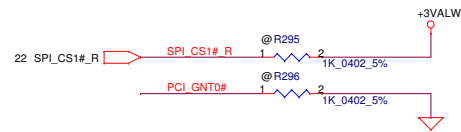
A16 swap override Strap

PCI_GNT3# Low= A16 swap override Enable
 High= Default*

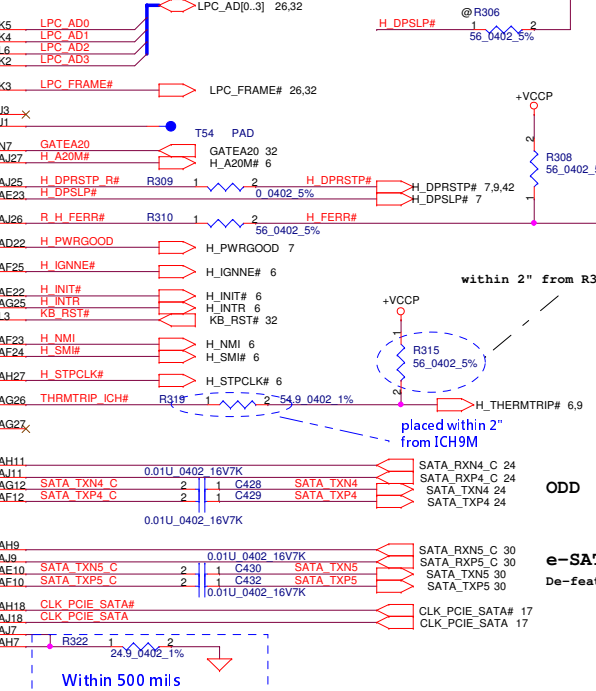
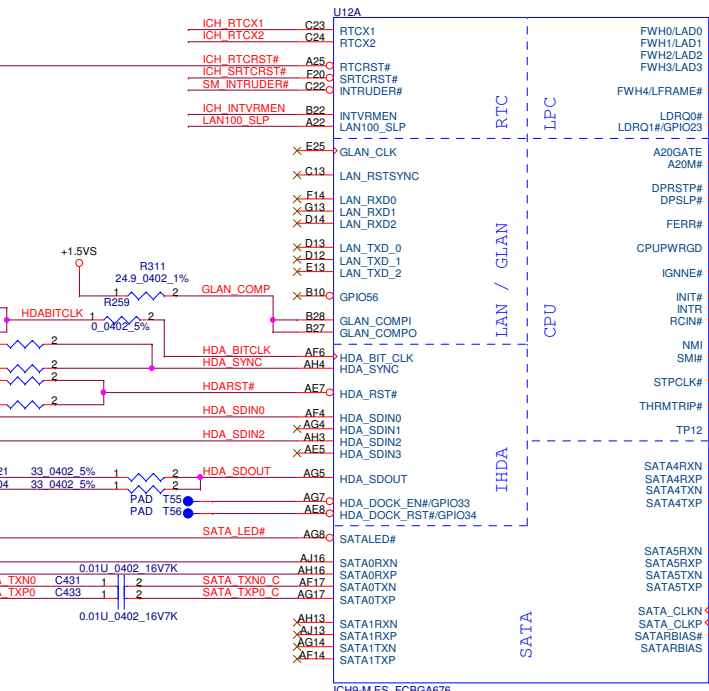
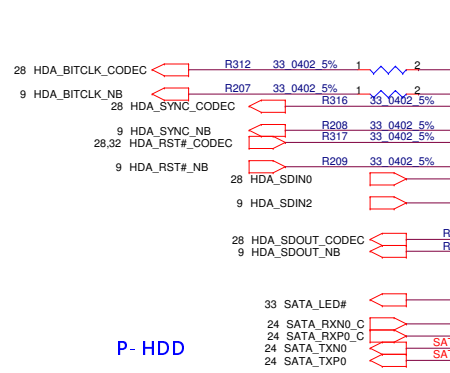
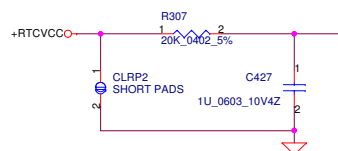
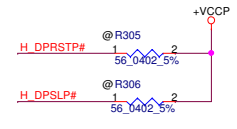
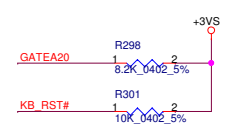
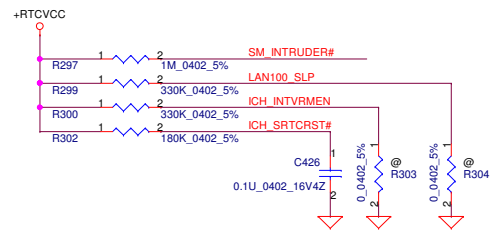


Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



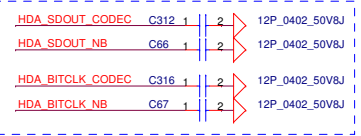
ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



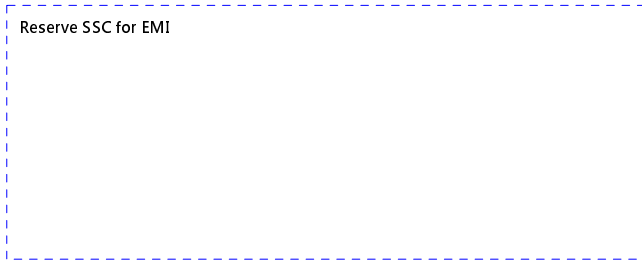
P-HDD

e-SATA
De-feature disable

Add 12p on HDA_SDOUT and HDA_SDOU
Add 12p on HDA_BITCLK_CODE and HDA_BITCLK_NB



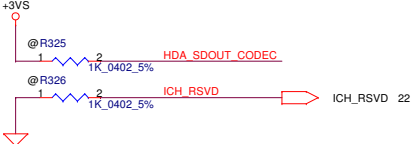
SI-1 Remove SSC



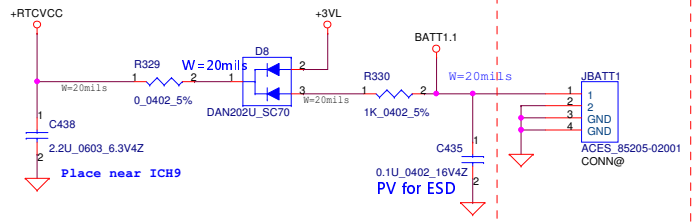
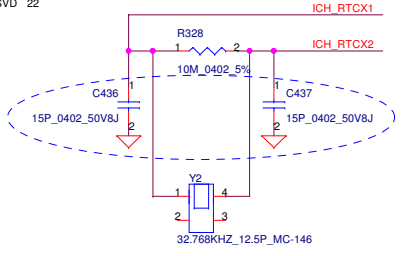
Reserve cap on HDA_BITCLK for WWAN noise issue

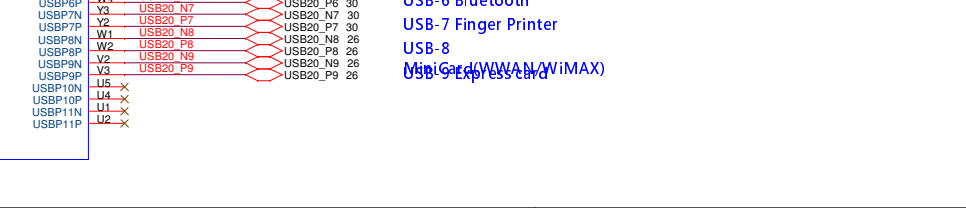
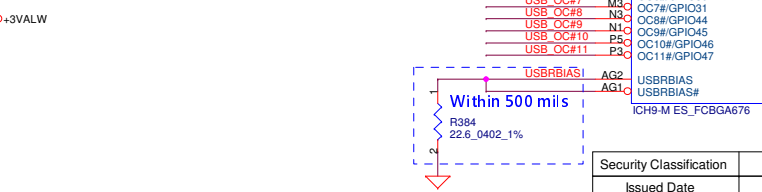
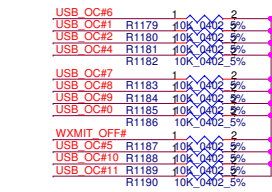
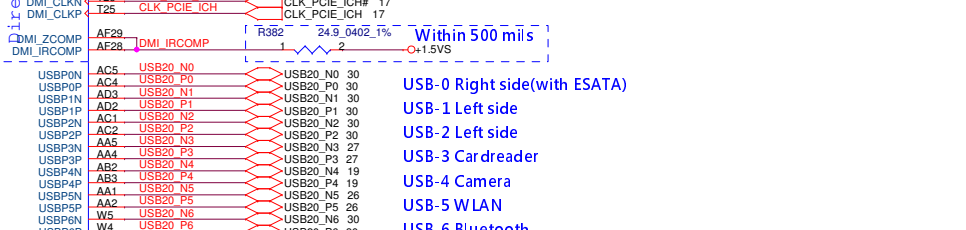
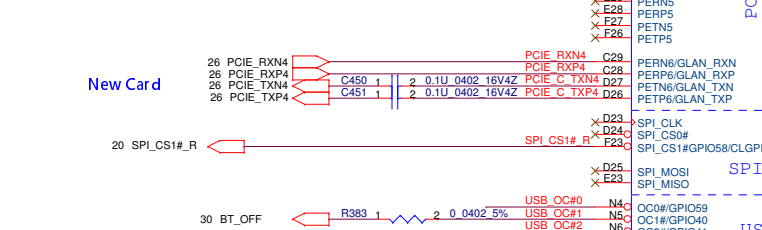
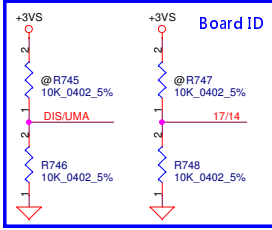
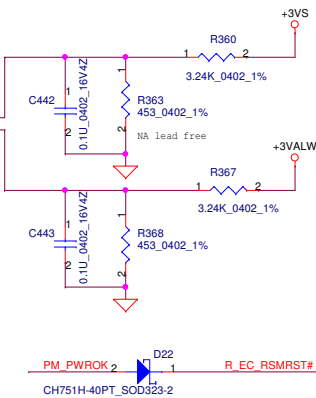
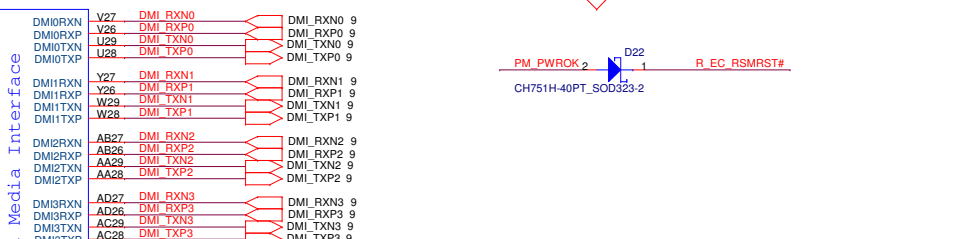
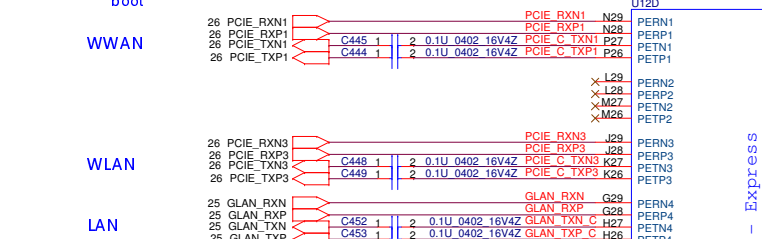
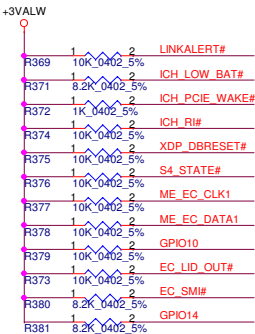
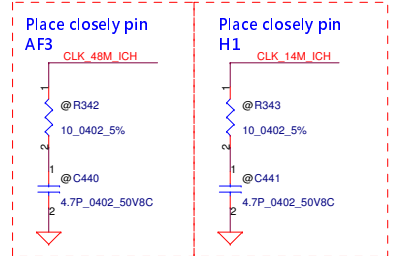
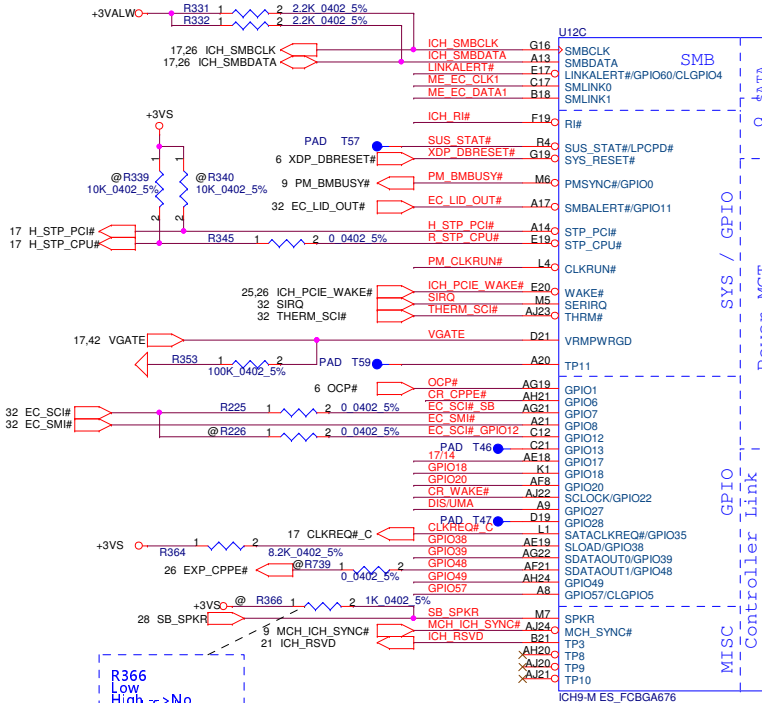
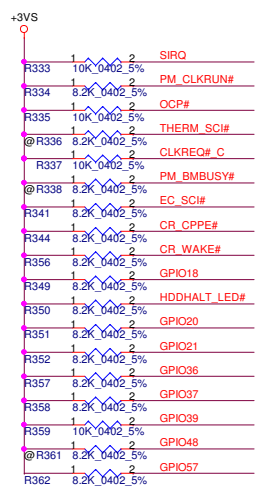


XOR CHAIN ENTRANCE STRAP:RSVD

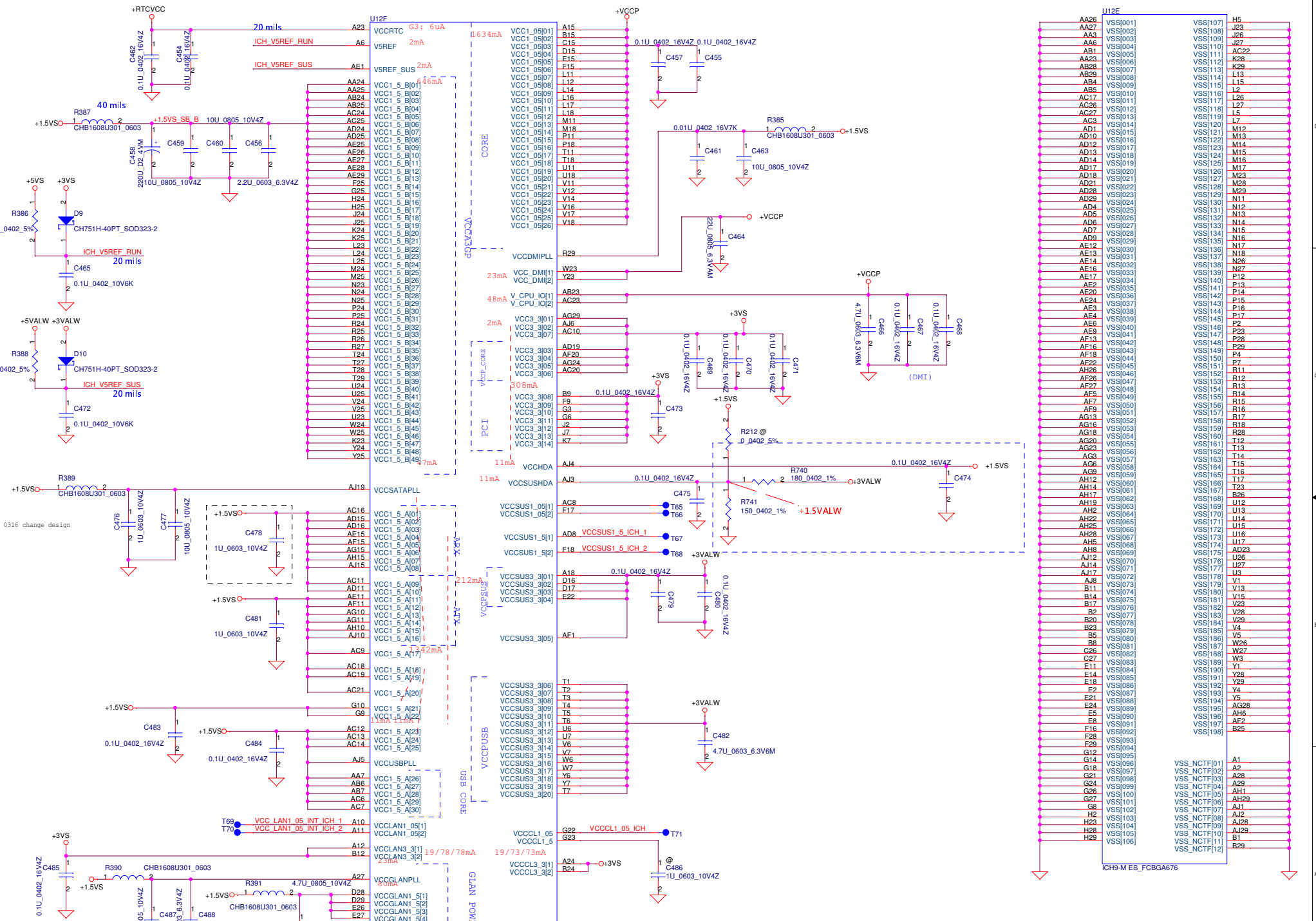


ICH_RSVD	HDA_SDOU_CODEC
0	0
0	1
1	0
1	1





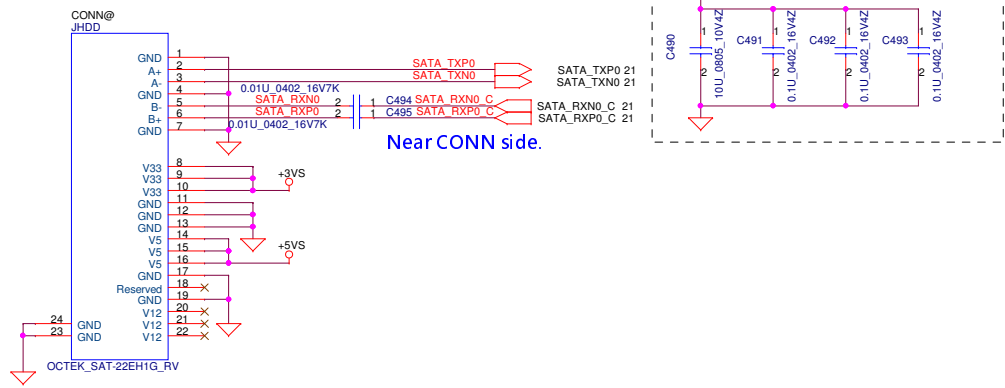
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Date	Wednesday, February 18, 2009	Sheet	22	of 46



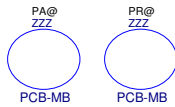
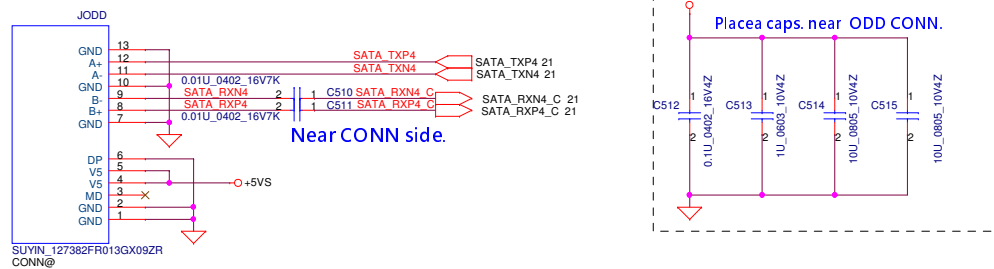
Pin	Signal	Value
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AA3	VSS[002]	J23
AA6	VSS[003]	J26
AA7	VSS[004]	J27
AA8	VSS[005]	ACC22
AA23	VSS[006]	K28
AB28	VSS[007]	K29
AB29	VSS[008]	L13
AB5	VSS[009]	L15
AB6	VSS[010]	L2
AC17	VSS[011]	L26
AC26	VSS[012]	L27
AC27	VSS[013]	L5
AC3	VSS[014]	L7
AD1	VSS[015]	L12
AD10	VSS[016]	M13
AD12	VSS[017]	M14
AD13	VSS[018]	M15
AD14	VSS[019]	M16
AD17	VSS[020]	M17
AD18	VSS[021]	M23
AD28	VSS[022]	M28
AD29	VSS[023]	M29
AD3	VSS[024]	N11
AD4	VSS[025]	N12
AD5	VSS[026]	N13
AD6	VSS[027]	N14
AD7	VSS[028]	N15
AD9	VSS[029]	N16
AE12	VSS[030]	N17
AE13	VSS[031]	N18
AE14	VSS[032]	N26
AE16	VSS[033]	N27
AE17	VSS[034]	P12
AE2	VSS[035]	P13
AE20	VSS[036]	P14
AE24	VSS[037]	P15
AE3	VSS[038]	P16
AE4	VSS[039]	P17
AE6	VSS[040]	P2
AE9	VSS[041]	P23
AE10	VSS[042]	P28
AE16	VSS[043]	P29
AF18	VSS[044]	P4
AF22	VSS[045]	P7
AG2	VSS[046]	R11
AG24	VSS[047]	R13
AG25	VSS[048]	R14
AG26	VSS[049]	R15
AG27	VSS[050]	R16
AG13	VSS[051]	R17
AG16	VSS[052]	R18
AG18	VSS[053]	R28
AG20	VSS[054]	T12
AG23	VSS[055]	T13
AG3	VSS[056]	T14
AG6	VSS[057]	T15
AH12	VSS[058]	T16
AH17	VSS[059]	T17
AH14	VSS[060]	T23
AH19	VSS[061]	T28
AH2	VSS[062]	B26
AH22	VSS[063]	U12
AH25	VSS[064]	U13
AH28	VSS[065]	U14
AH3	VSS[066]	U15
AH8	VSS[067]	U16
AH5	VSS[068]	U17
AH8	VSS[069]	AD23
AJ12	VSS[070]	U26
AJ14	VSS[071]	U27
AJ17	VSS[072]	U9
B11	VSS[073]	V1
B14	VSS[074]	V13
B1	VSS[075]	V15
B2	VSS[076]	V28
B20	VSS[077]	V29
B23	VSS[078]	V4
B5	VSS[079]	V5
B8	VSS[080]	W26
C26	VSS[081]	W27
E11	VSS[082]	W3
E14	VSS[083]	Y1
E18	VSS[084]	Y28
E21	VSS[085]	Y2
E22	VSS[086]	Y3
E2	VSS[087]	Y4
E21	VSS[088]	Y5
E24	VSS[089]	AG28
E5	VSS[090]	AH6
E8	VSS[091]	AF2
F18	VSS[092]	B25
F29	VSS[093]	A1
G12	VSS[094]	A2
G14	VSS[095]	A28
G18	VSS[096]	A29
G21	VSS[097]	AH1
G24	VSS[098]	AH2
G26	VSS[099]	AH3
G27	VSS[100]	AH4
G8	VSS[101]	AJ1
H2	VSS[102]	AJ2
H23	VSS[103]	AJ28
H28	VSS[104]	BJ29
H23	VSS[105]	BJ
H23	VSS[106]	B29
VSS_NCTF[01]		A1
VSS_NCTF[02]		A2
VSS_NCTF[03]		A28
VSS_NCTF[04]		A29
VSS_NCTF[05]		AH1
VSS_NCTF[06]		AH2
VSS_NCTF[07]		AH3
VSS_NCTF[08]		AH4
VSS_NCTF[09]		AJ1
VSS_NCTF[10]		AJ2
VSS_NCTF[11]		BJ29
VSS_NCTF[12]		B29

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				Montevina UMA	
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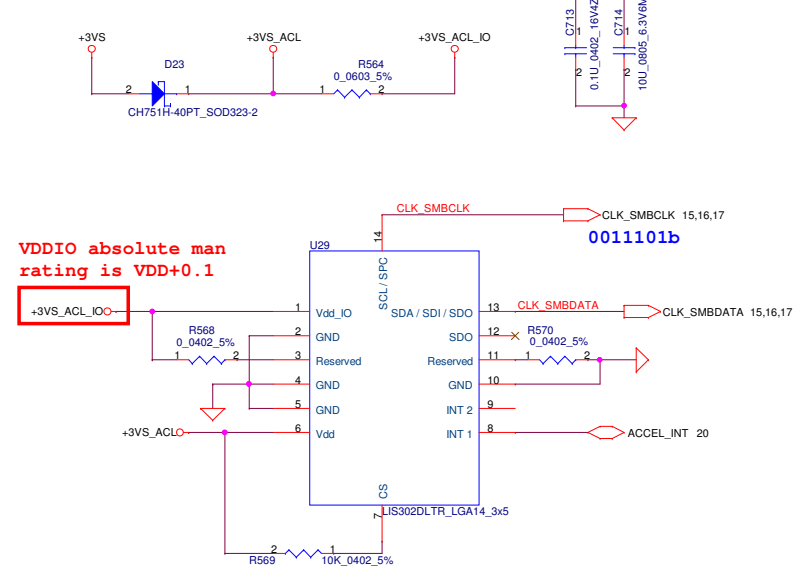
HDD Connector



CD-ROM Connector



ACCELEROMETER (ST)

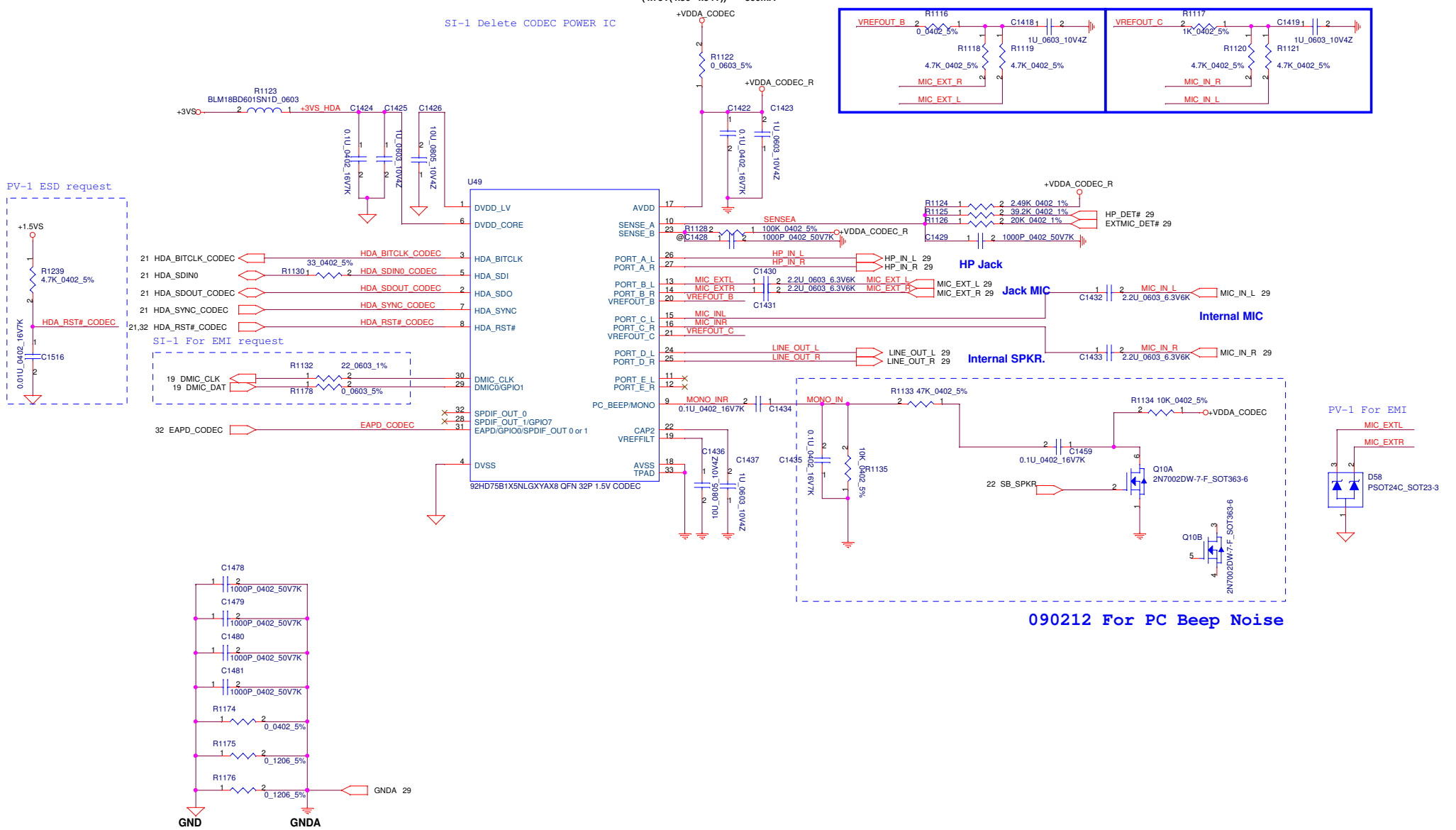


Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	HDD & CDROM	
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CODEC POWER

(4.75V(4.56-4.94V)) 300mA

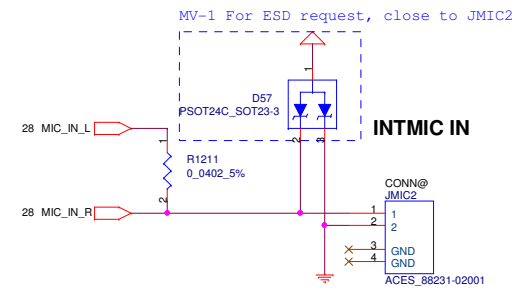
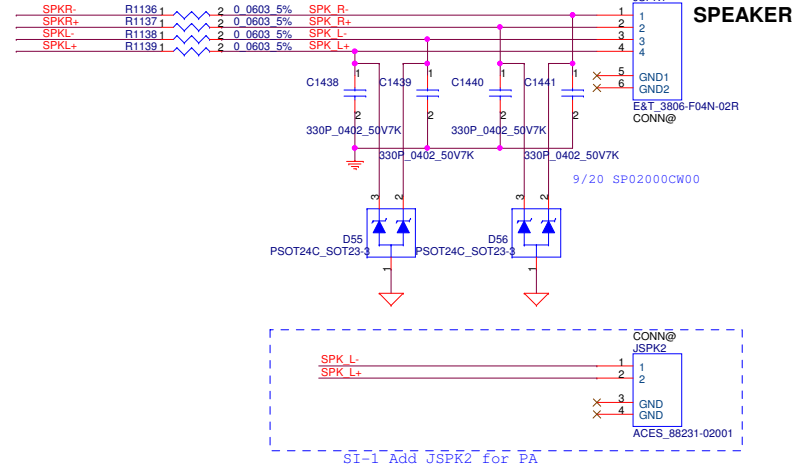
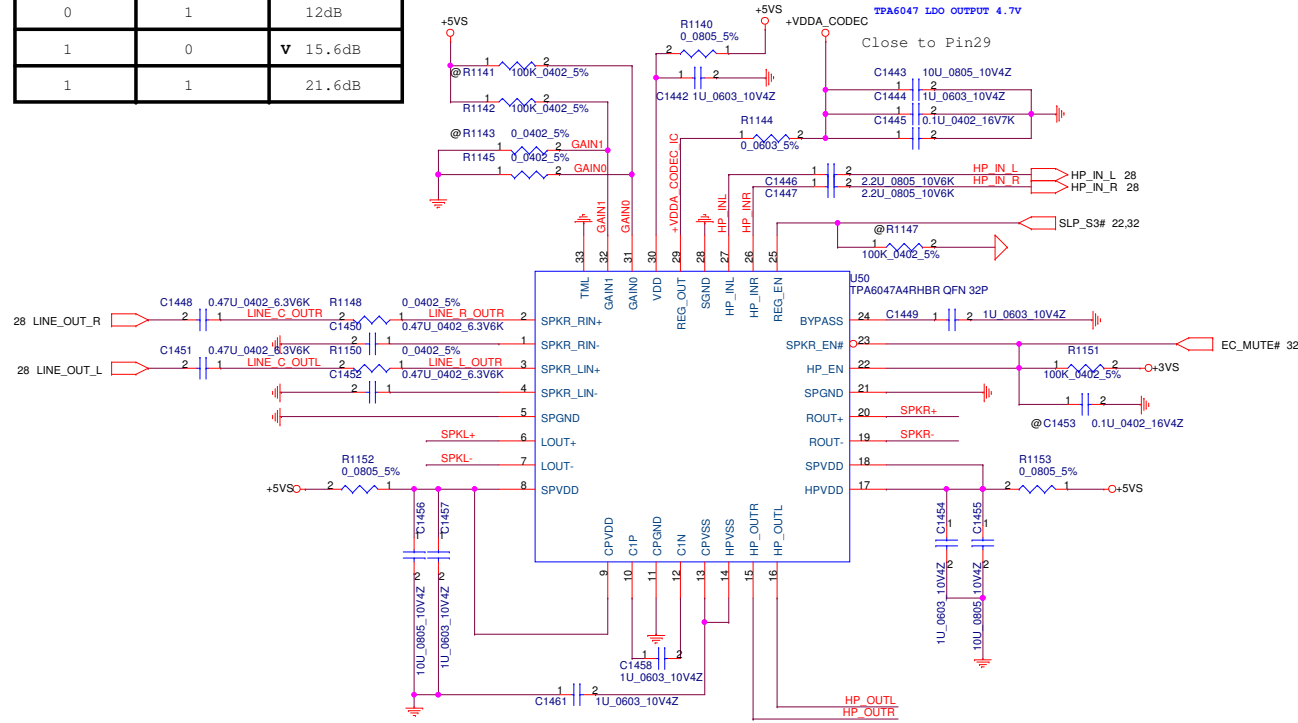
SI-1 Delete CODEC POWER IC



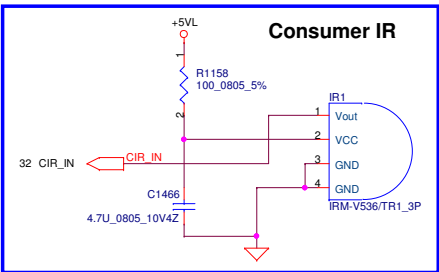
Security Classification	Compal Secret Data		Title	Codec_IDT9275B
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Rev
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			Montevina UMA	
			Date: Wednesday, February 18, 2009	Sheet 28 of 46

AMP. FOR INTERNAL SPEAKER

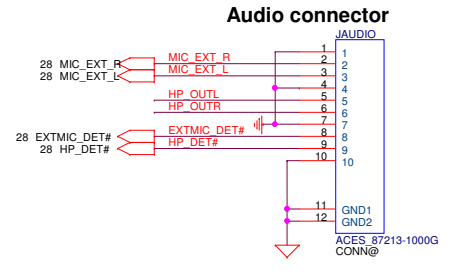
GAIN1	GAIN0	Av (inv)
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0	1	12dB
1	0	V 15.6dB
1	1	21.6dB



SI-1 Change IR1 to SCR00000E00

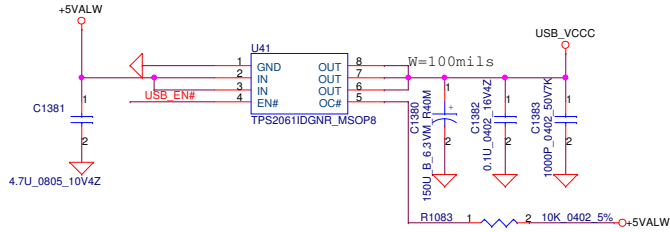


SI-1 Add Audio board connector

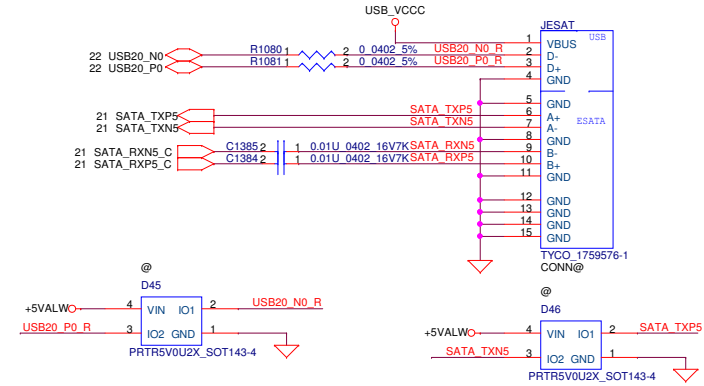


Security Classification	Compal Secret Data		Title
Issued Date	2007/08/28	Deciphered Date	2006/07/26
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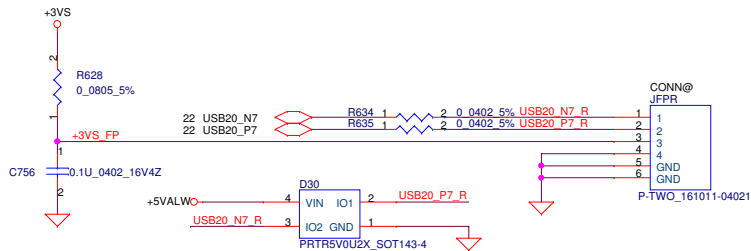
Right side USB Power Switch



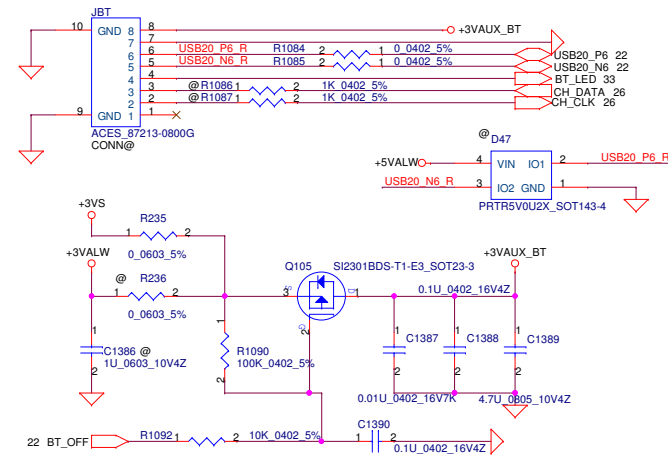
Right side eSATA/USB combination Connector



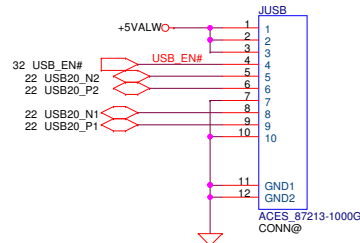
Finger printer



BT Connector

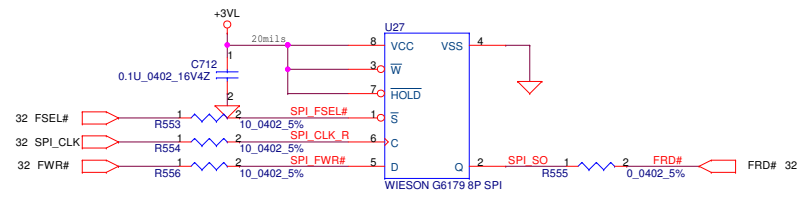


USB cable connector for Right side

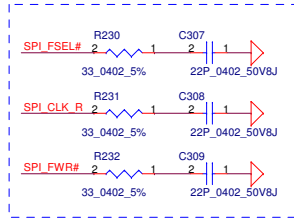


Security Classification	Compal Secret Data			Title
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc. USB, BT, eSATA
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SPI ROM

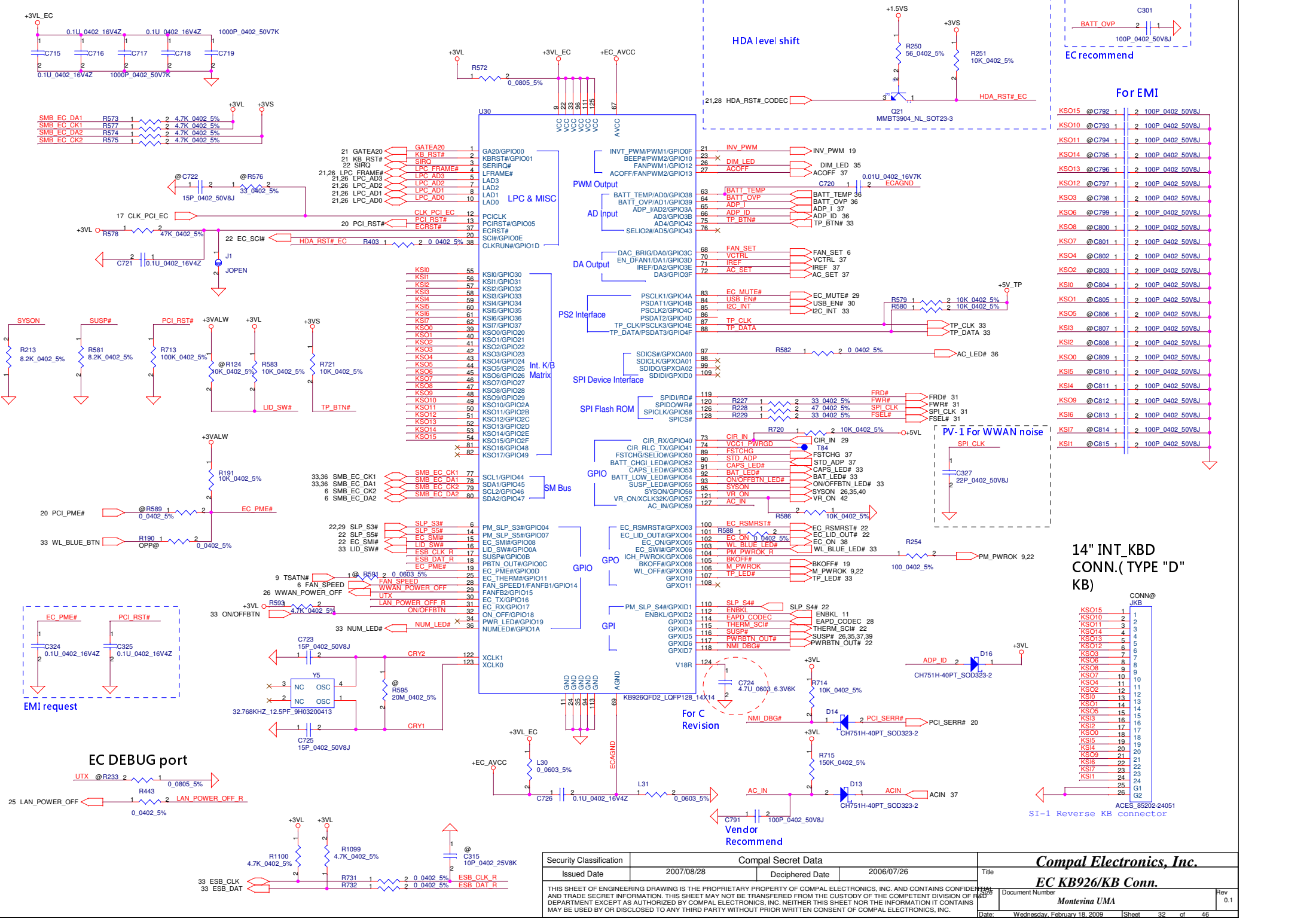


SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



EMI request

Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	BIOS ROM	
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For EMI

KS015 @C792	1	2	100P_0402_50V8J
KS010 @C793	1	2	100P_0402_50V8J
KS011 @C794	1	2	100P_0402_50V8J
KS014 @C795	1	2	100P_0402_50V8J
KS013 @C796	1	2	100P_0402_50V8J
KS012 @C797	1	2	100P_0402_50V8J
KS03 @C798	1	2	100P_0402_50V8J
KS06 @C799	1	2	100P_0402_50V8J
KS08 @C800	1	2	100P_0402_50V8J
KS07 @C801	1	2	100P_0402_50V8J
KS04 @C802	1	2	100P_0402_50V8J
KS02 @C803	1	2	100P_0402_50V8J
KS10 @C804	1	2	100P_0402_50V8J
KS01 @C805	1	2	100P_0402_50V8J
KS05 @C806	1	2	100P_0402_50V8J
KS13 @C807	1	2	100P_0402_50V8J
KS12 @C808	1	2	100P_0402_50V8J
KS00 @C809	1	2	100P_0402_50V8J
KS15 @C810	1	2	100P_0402_50V8J
KS14 @C811	1	2	100P_0402_50V8J
KS09 @C812	1	2	100P_0402_50V8J
KS16 @C813	1	2	100P_0402_50V8J
KS17 @C814	1	2	100P_0402_50V8J
KS11 @C815	1	2	100P_0402_50V8J

14" INT_KBD CONN.(TYPE "D" KB)

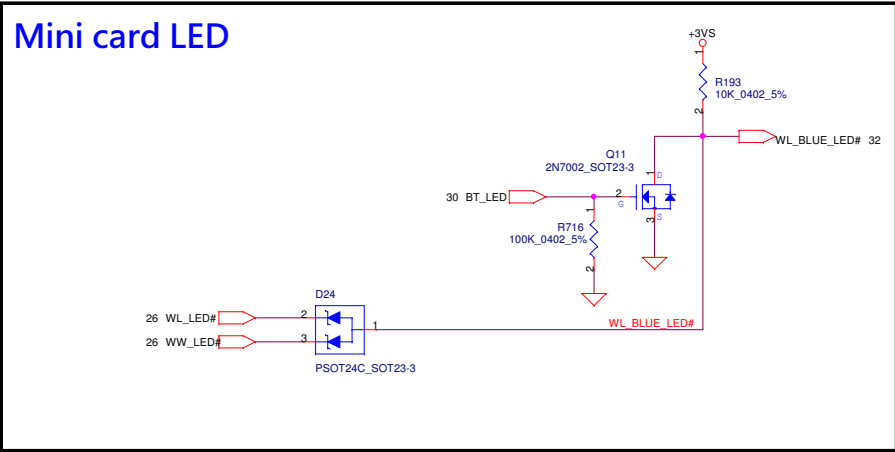
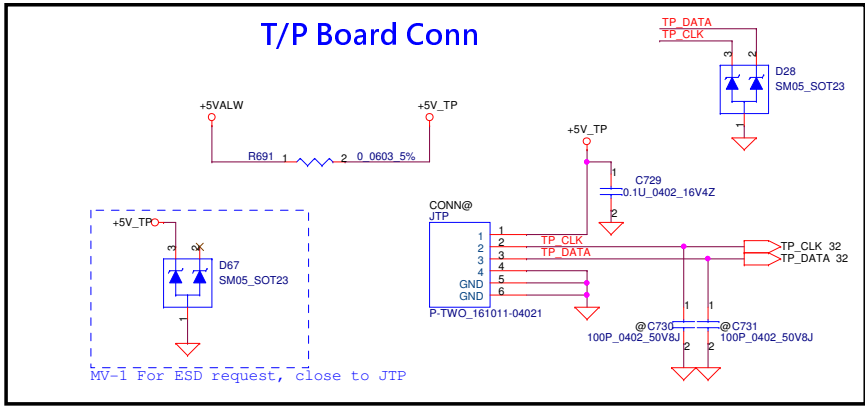
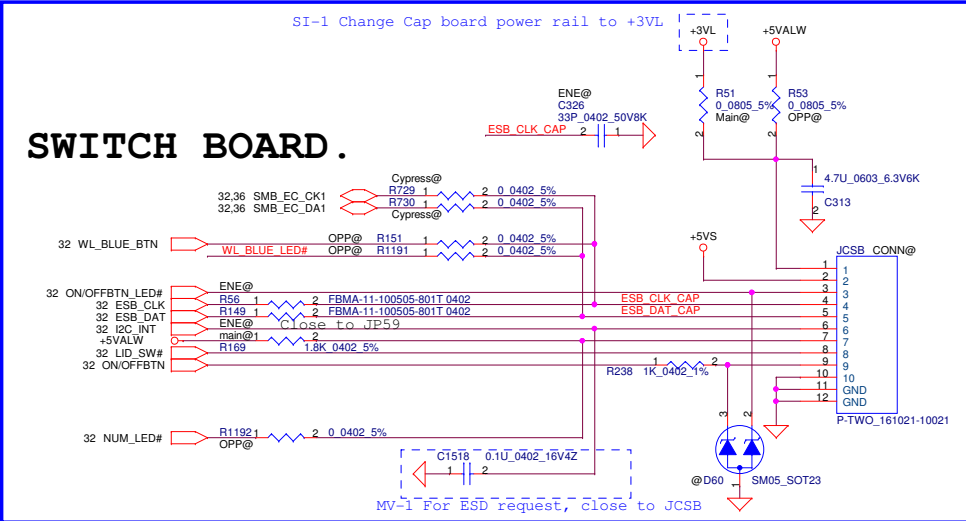
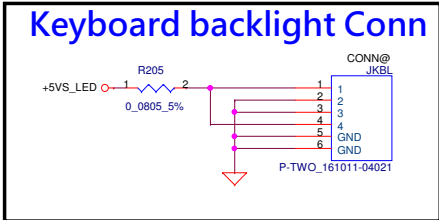
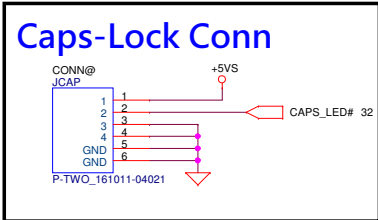
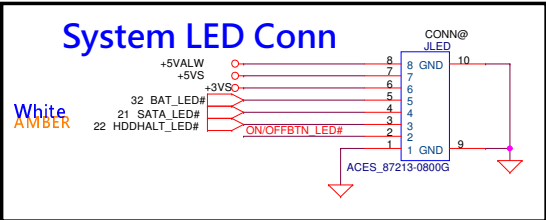
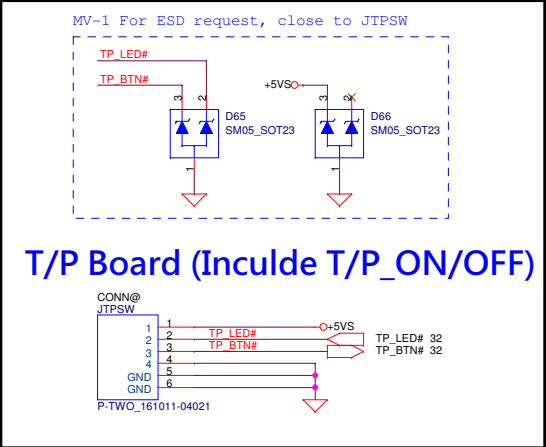
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KS01	2
KS011	3
KS014	4
KS013	5
KS012	6
KS06	7
KS08	8
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KS05	11
KS10	12
KS01	13
KS01	14
KS05	15
KS16	16
KS12	17
KS15	18
KS15	19
KS14	20
KS09	21
KS16	22
KS17	23
KS11	24
KS11	25
G1	26
G2	26

ACES_B5202-24051

Security Classification	Compal Secret Data		
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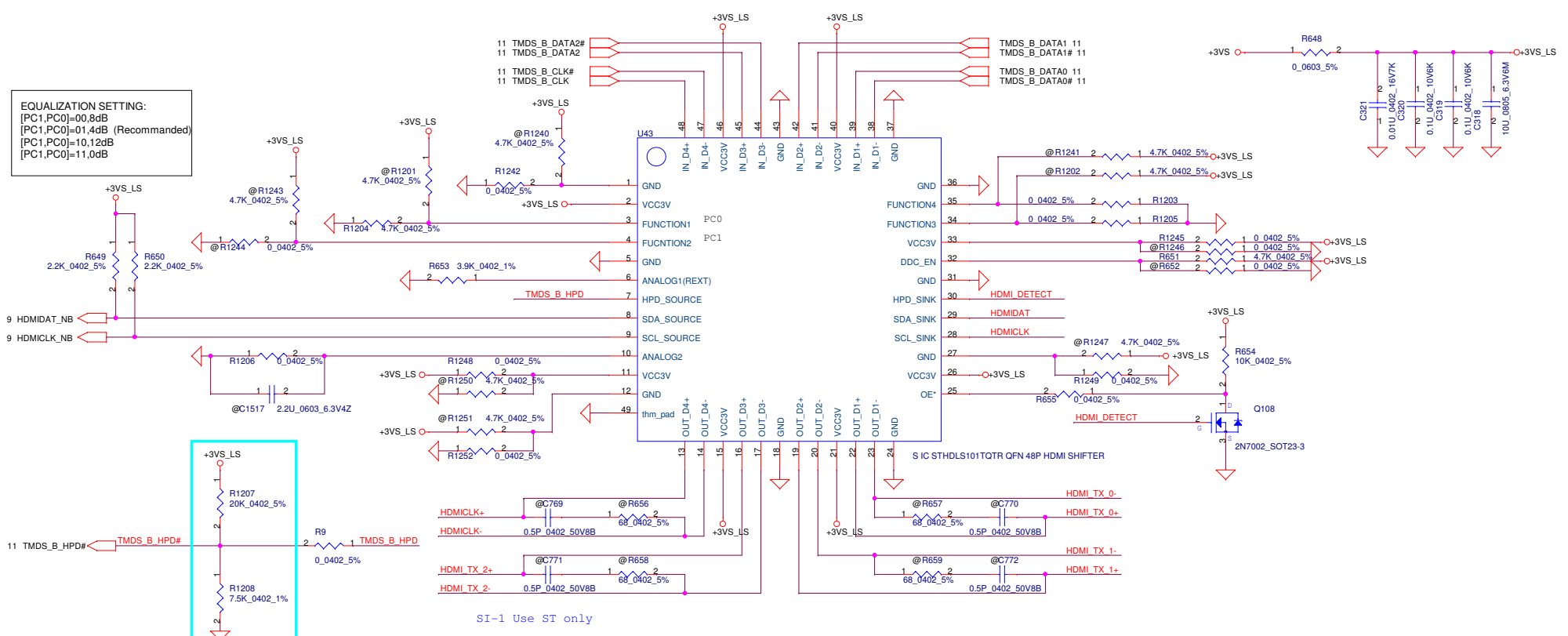
Compal Electronics, Inc.	
EC KB926/KB Conn.	
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Date	Wednesday, February 18, 2009
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SI-1 Delete SW2



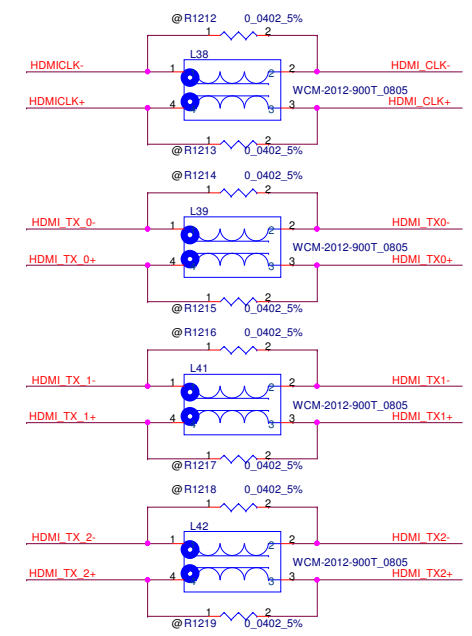
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	KBD, ON/OFF, SW, CIR	
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EQUALIZATION SETTING:
 [PC1,PC0]=00,8dB
 [PC1,PC0]=01,4dB (Recommended)
 [PC1,PC0]=10,12dB
 [PC1,PC0]=11,0dB

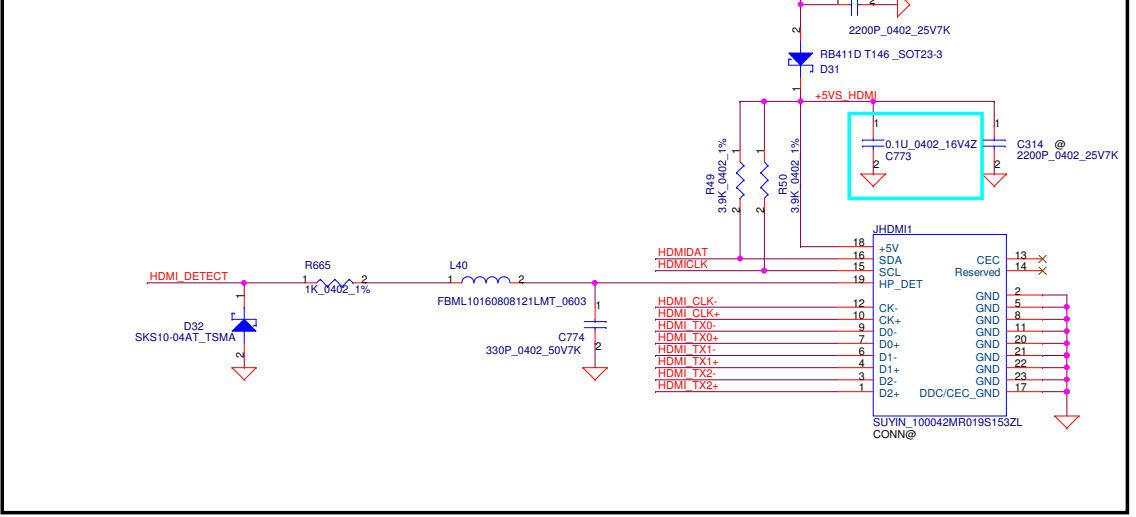


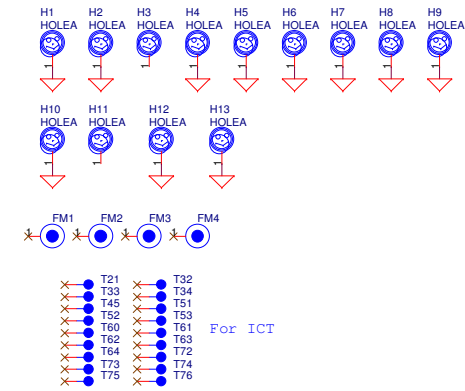
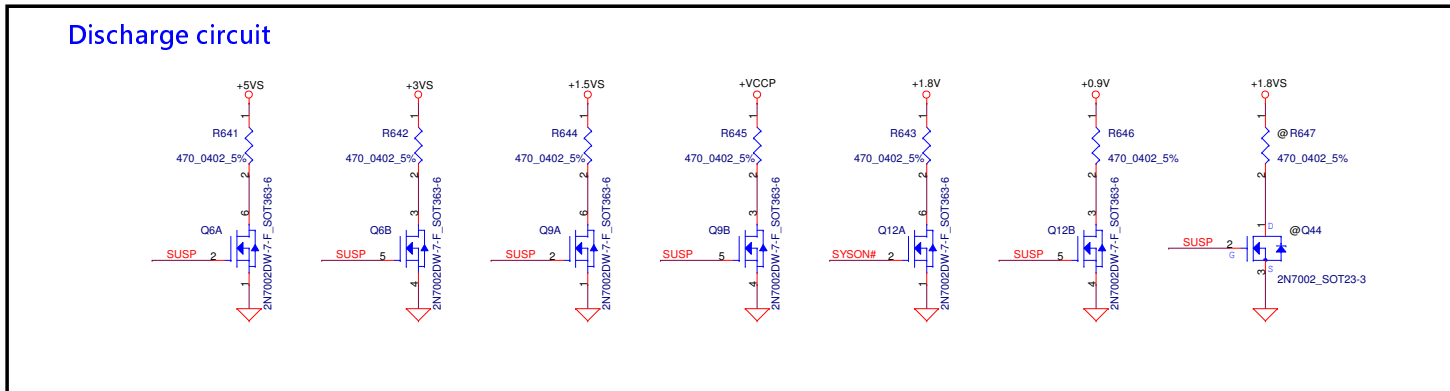
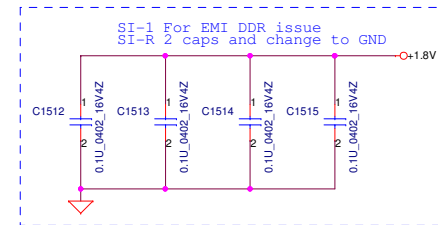
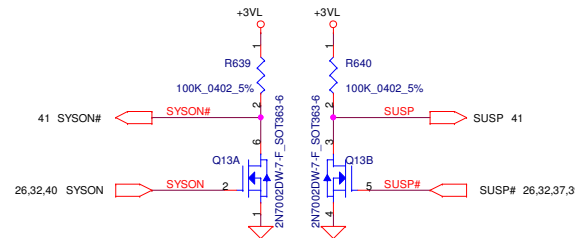
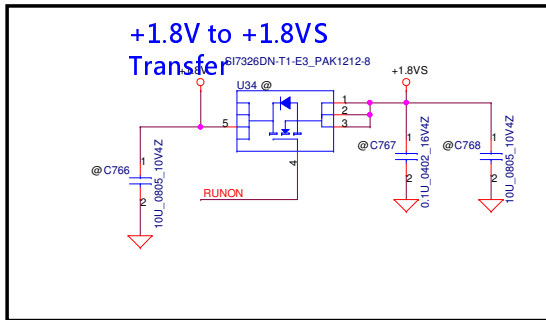
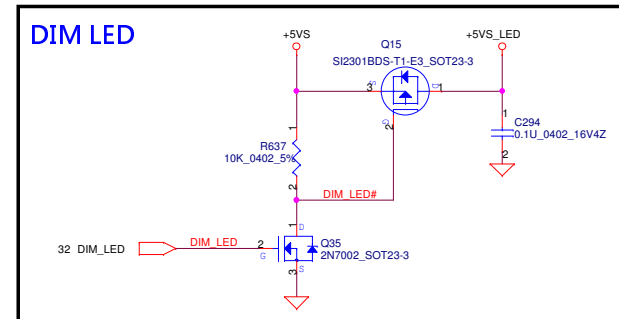
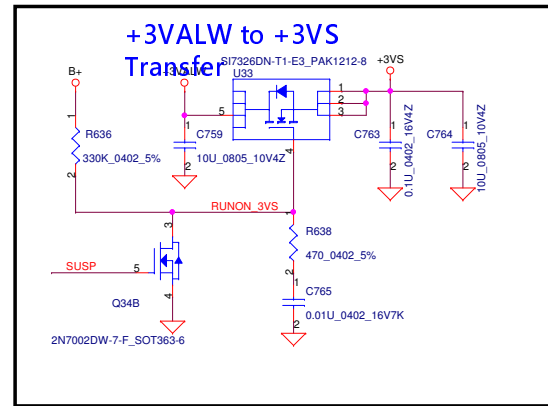
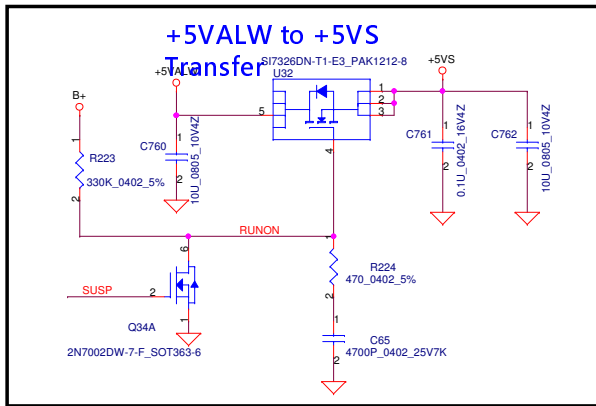
To option use ST or Parade

	ST	Parade 81011	Parade 8171
R1240	X	X	X
R1242	0 ohm	0 ohm	4.7K ohm
R1201	X	4.7K ohm	X
R1204	4.7K ohm	X	4.7K ohm
R1243	X	X	4.7K ohm
R1244	X	X	X
R653	3.9K ohm	499 ohm	499 ohm
R1206	0 ohm	X	X
C1517	X	X	2.2uF
R1248	0 ohm	0 ohm	X
R1250	X	X	4.7K ohm
R1251	X	X	4.7K ohm
R1252	0 ohm	0 ohm	X
R1247	X	X	4.7K ohm
R1249	0 ohm	0 ohm	X
R1245	0 ohm	0 ohm	X
R1246	X	X	4.7K ohm
R1203	0 ohm	X	4.7K ohm
R1241	X	X	X
R1205	0 ohm	X	X
R1202	X	X	4.7K ohm
C773	0.1uF	1uF	1uF
R1207	V	X	X
R1208	V	X	X

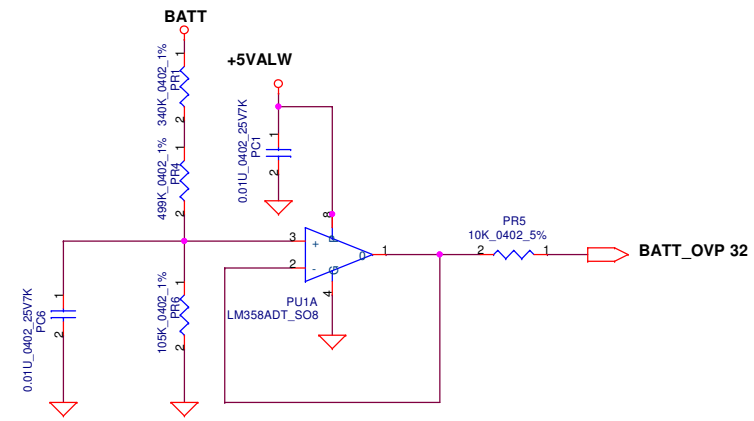
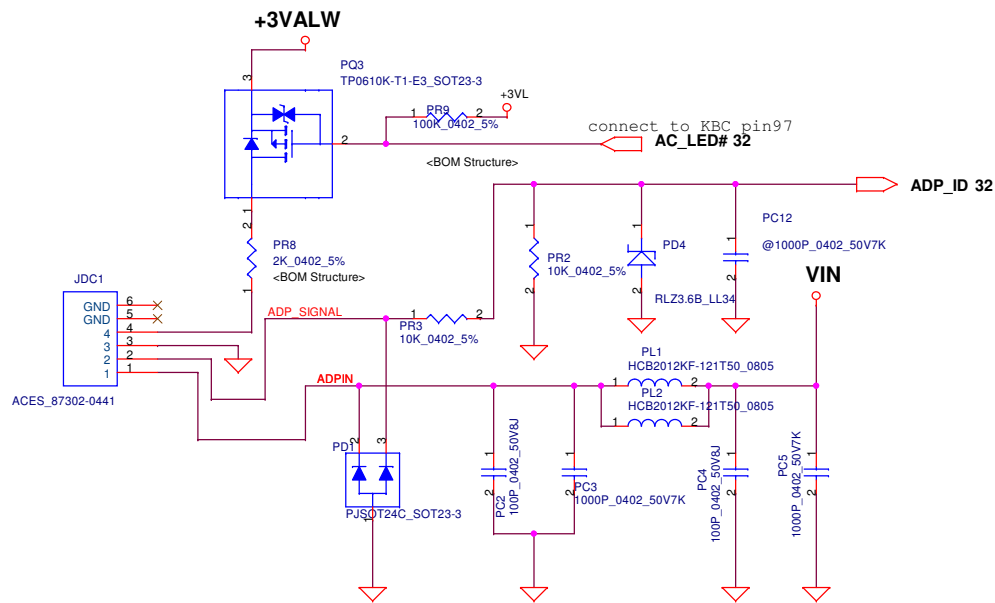


HDMI Connector

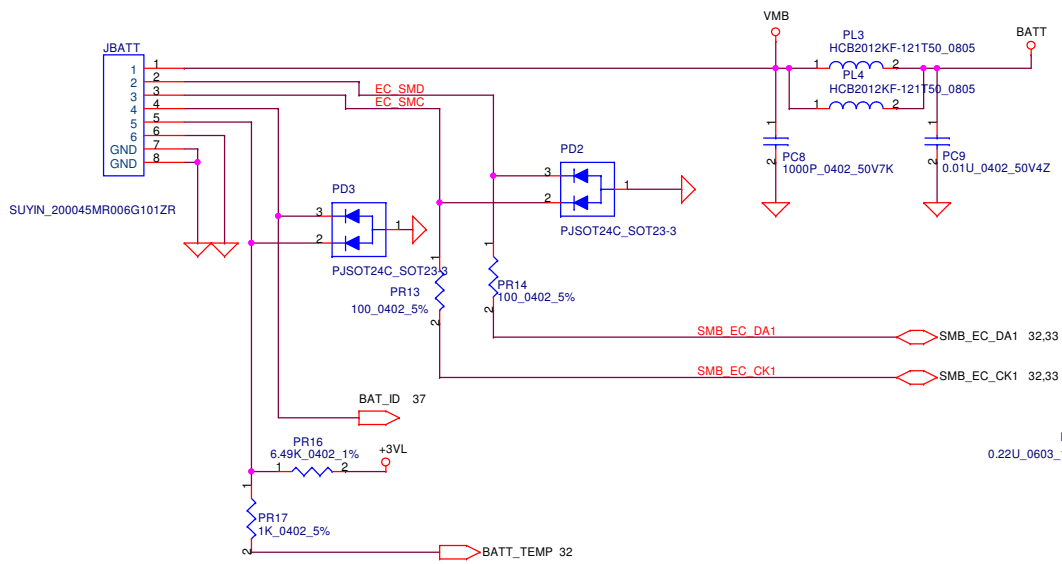
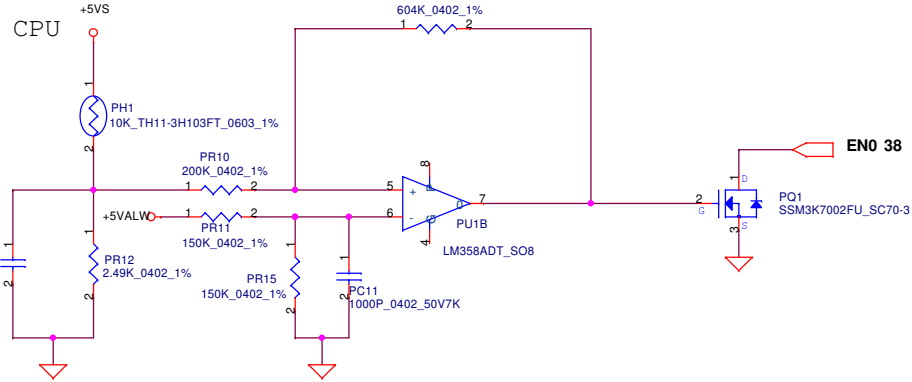




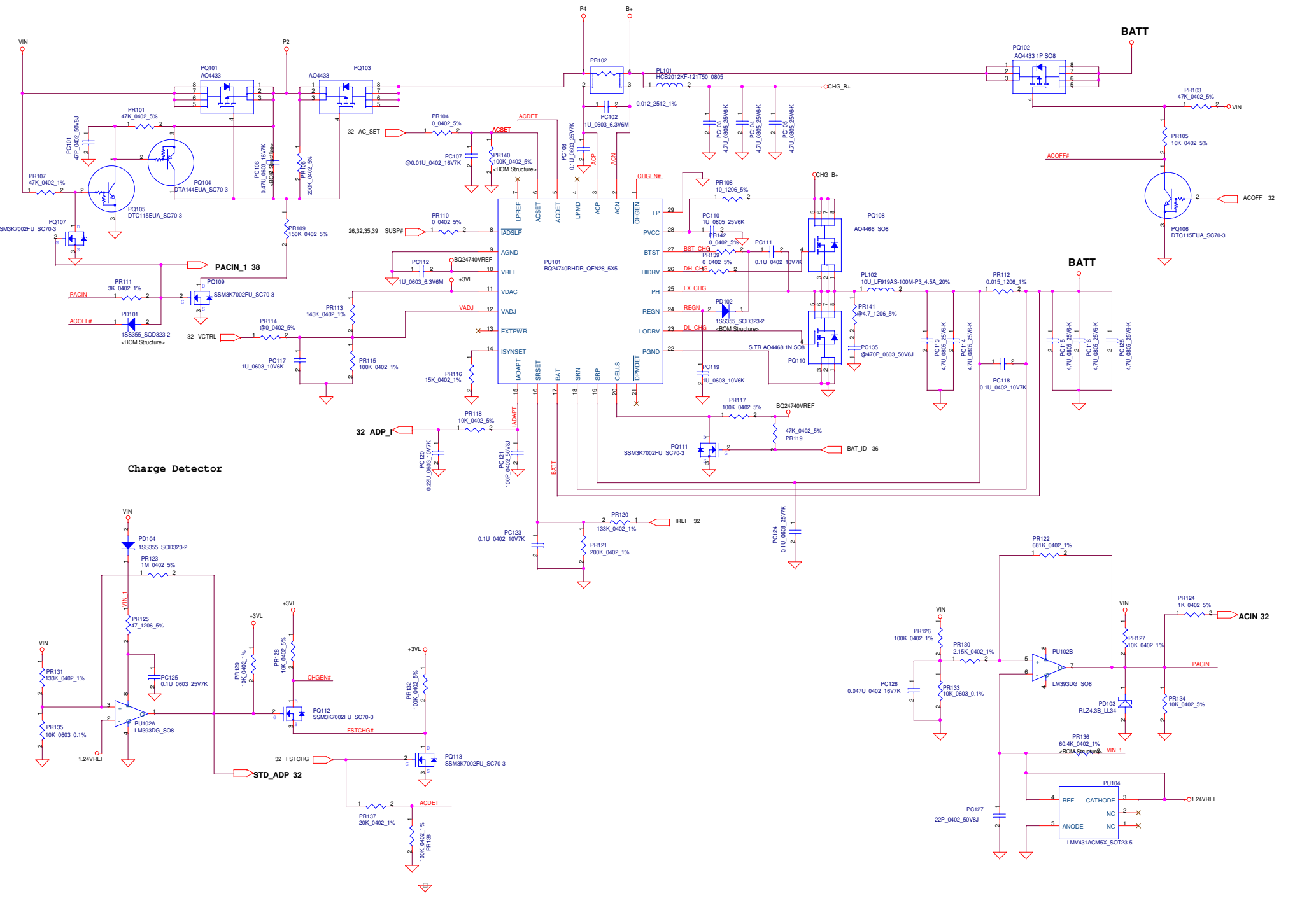
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	DC/DC Interface	
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				Montevina UMA	0.1
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PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C

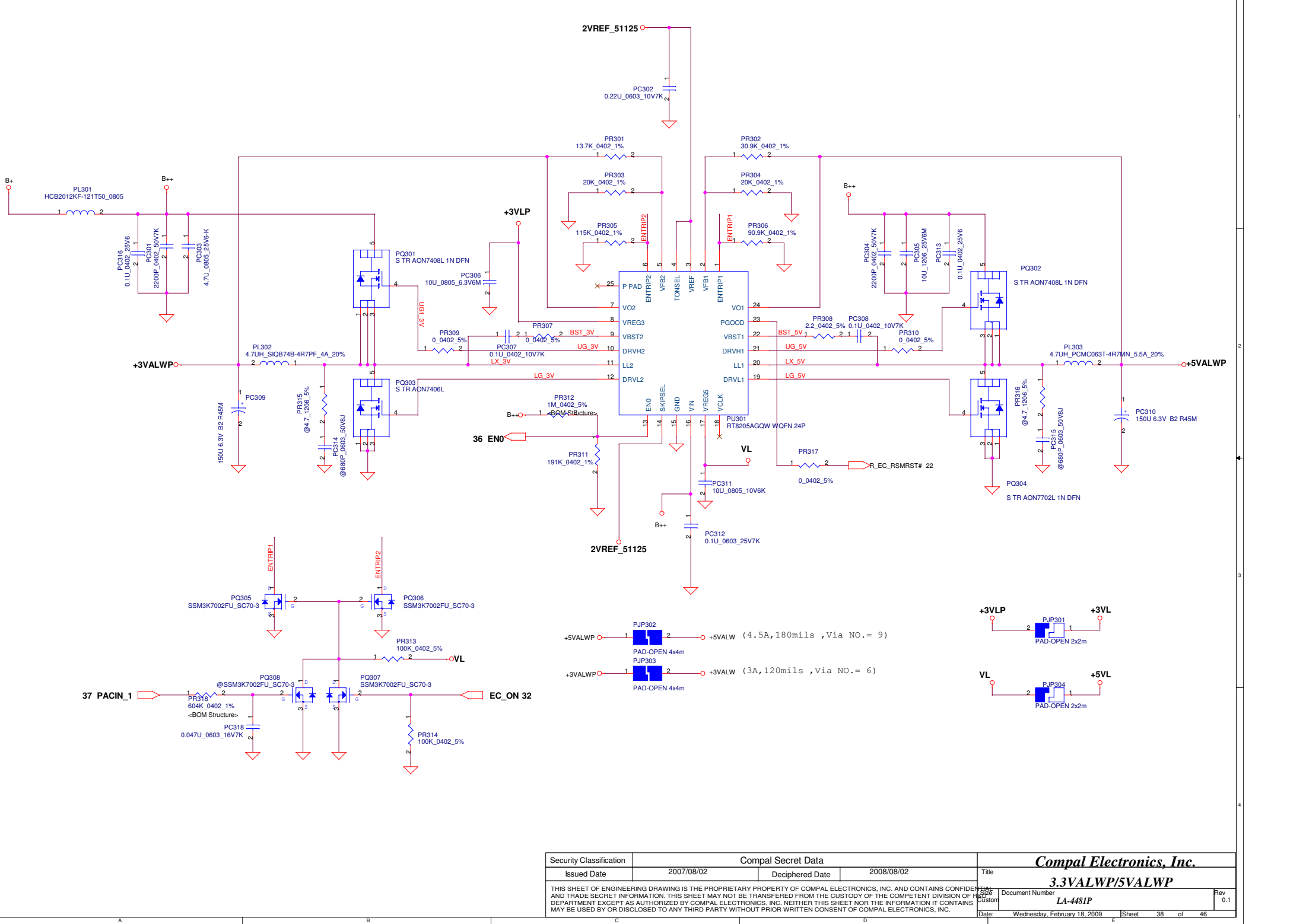


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Issued Date	2007/05/29	Deciphered Date	2008/05/29	DC Connector/CPU_OTP	
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				Montevina Consumer Discrete	
				Rev	0.1
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Charge Detector

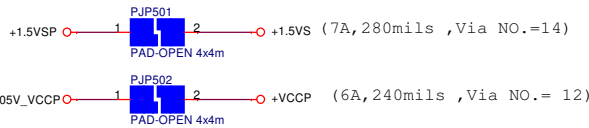
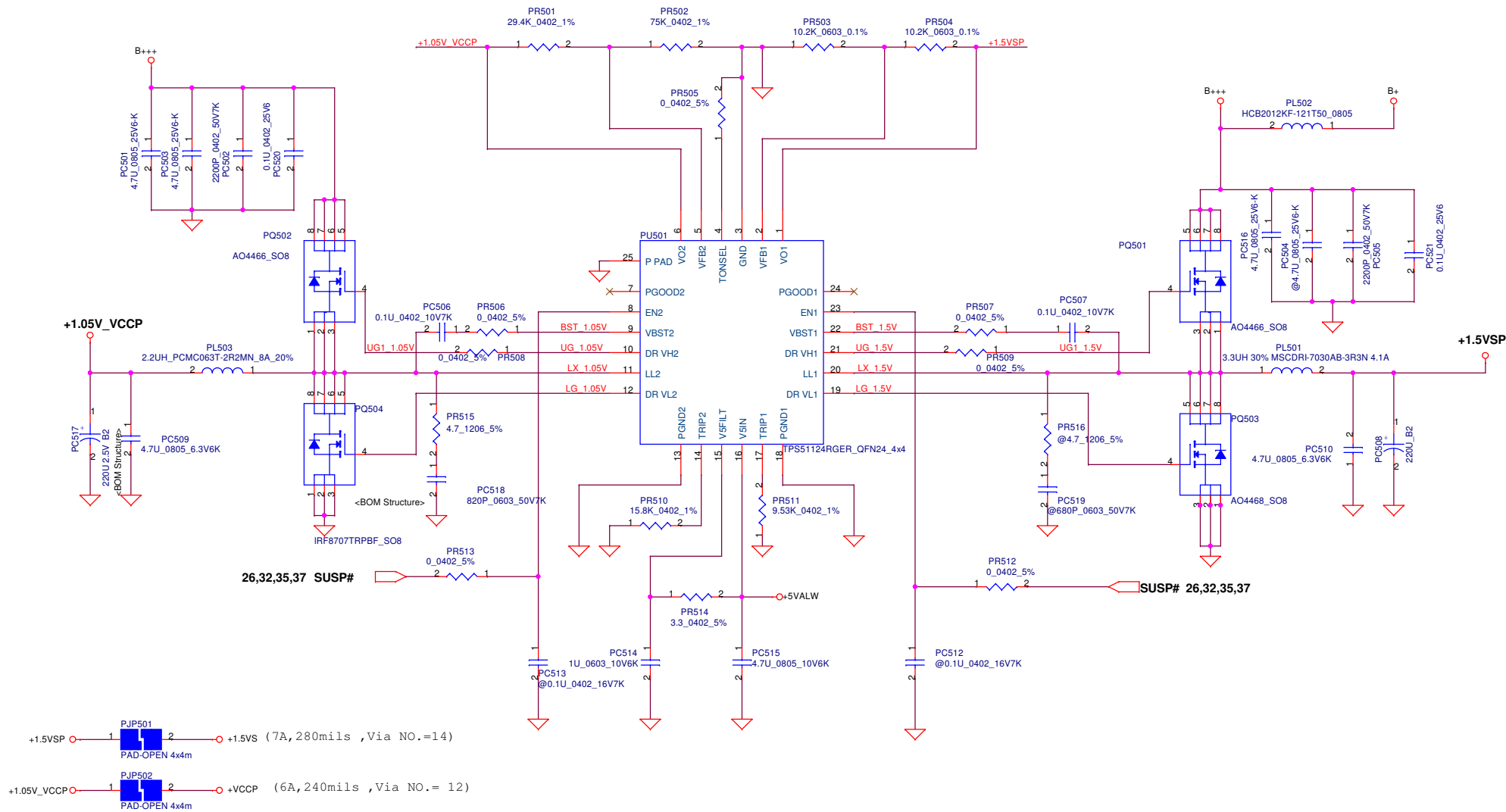
Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger	
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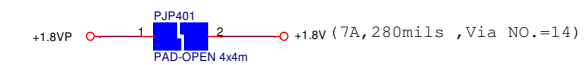
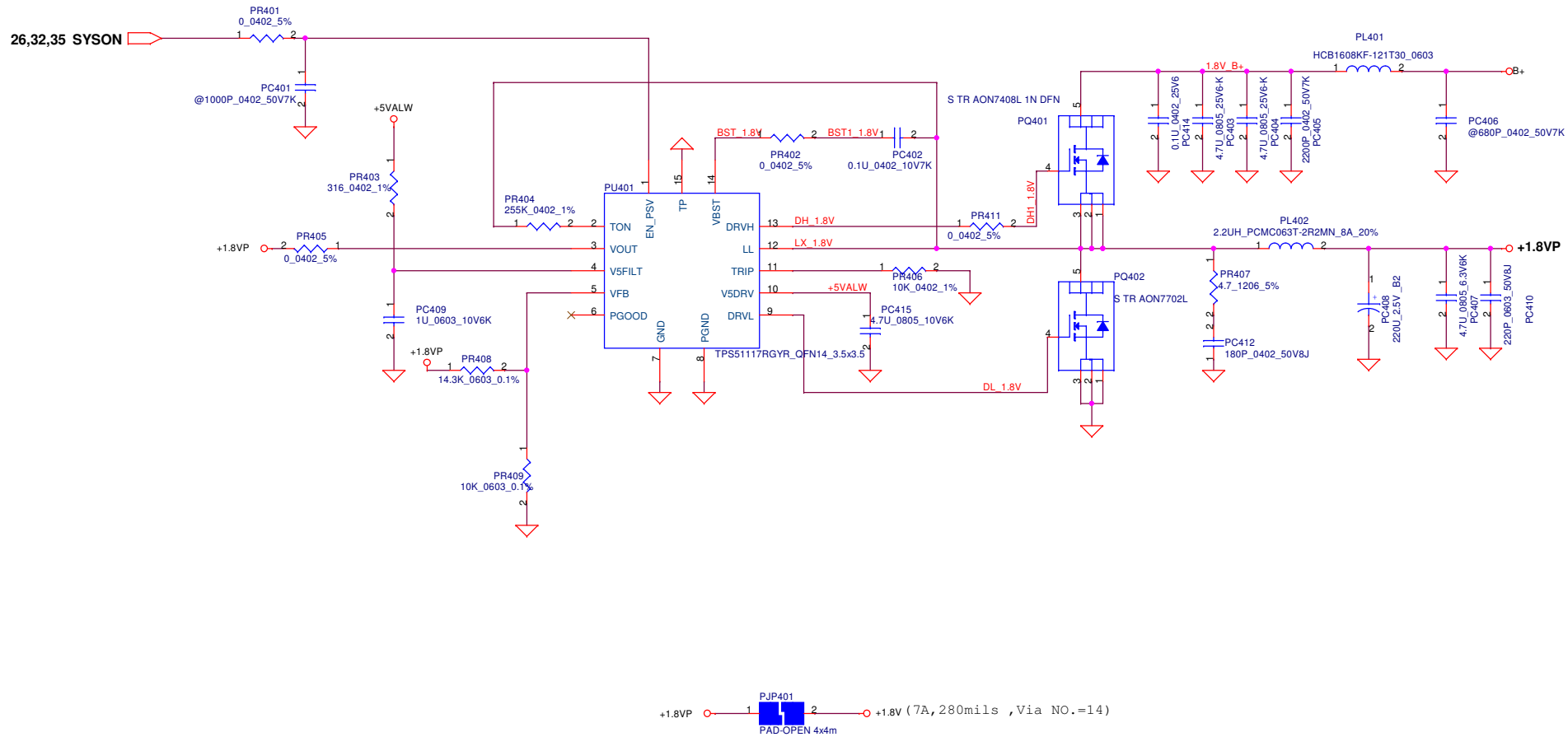
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Issued Date	2007/08/02	Deciphered Date	2008/08/02
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Compal Electronics, Inc.		
3.3VALWP/5VALWP		
Document Number	LA-448IP	
Date	Wednesday, February 18, 2009	Sheet 38 of 46

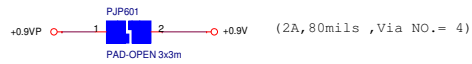
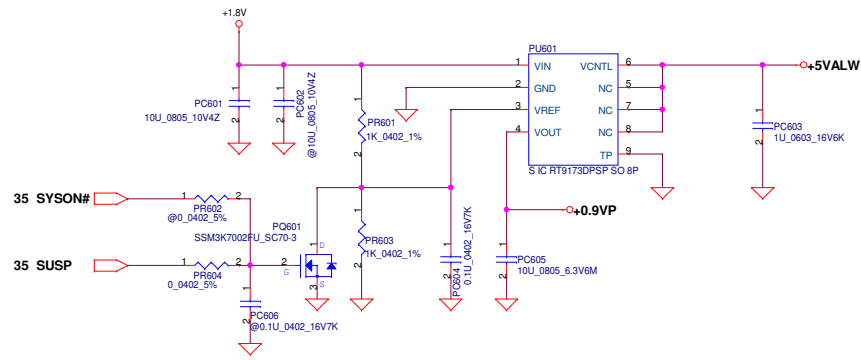
Rev 0.1



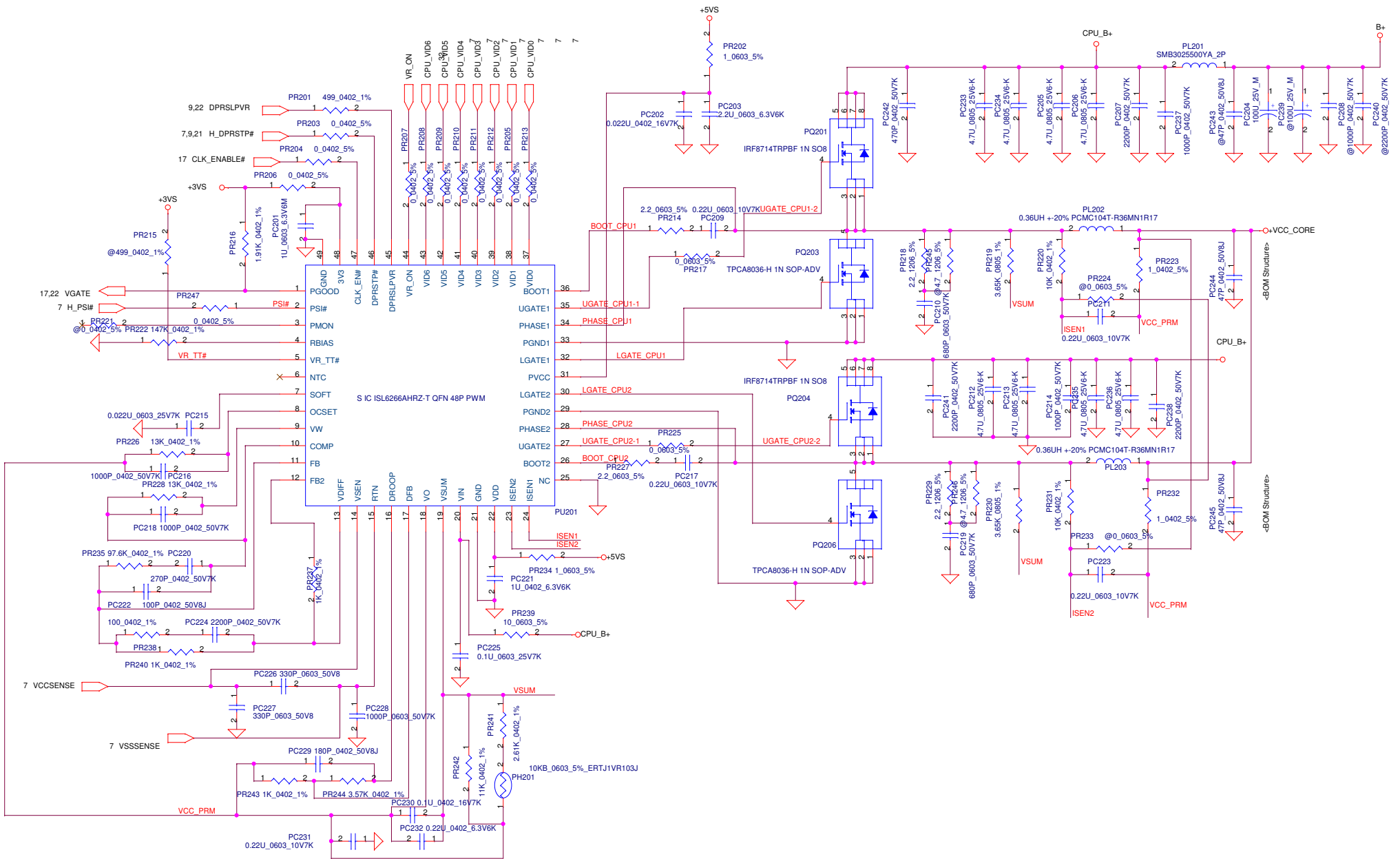
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Issued Date	2007/05/29	Deciphered Date	2008/05/29		
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Issued Date	2007/05/29	Deciphered Date	2008/05/29		
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	26	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	SMT issue	29	Change IR1 to SCR00000E00	2008/10/08	SI-1
4	Add Audio board	29	Add JAUDIO for audio board	2008/10/08	SI-1
5	SW2 is for DB1 debug	33	Delete SW2	2008/10/08	SI-1
6	Cap board issue	33	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Support GM47	13	Add C1503 for GM47	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D63	2008/10/08	SI-1
9	Delete HDA SSC	21	Remove U8 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	26	Add R1225 -- R1236	2008/10/08	SI-1
11	PA/PR CardReader LED	27	D54 for PA, D64 for PR	2008/10/08	SI-1
12	EMI request	28	Change R1132 to bead	2008/10/08	SI-1
13	Use audio board	29	Add audio board connector, change NIC to 2pin and add SPK connector	2008/10/08	SI-1
14	Change JFPR to 6 pin connector	30	Add Q109, C1518, R1210	2008/10/08	SI-1
15	EMI request	35	Add C1512 -- C1517	2008/10/08	SI-1
16	Change JFPR to 4 pin connector	30	Delete Q109, C1518, R1210	2008/11/21	SI-R
17	Delete resistor for Debug card	26	Delete R1220-R1224	2008/11/21	SI-R
18	EMI request	35	Delete C1516,C1517 and connect to GND	2008/11/21	SI-R
19	For Intel DPST	19	Add R1237,R1238	2008/11/25	SI-R
20	EMI and WWAN request	17 28	Install C217, C218, C219, C435, C312, C316, C66, C67, C1478, C1479, C1480, C1481, D58, C1516, R1239, C327	2008/12/18	PV-1
21	Audio board connector	29	Change pin define	2008/12/18	PV-1
22	ST and Parade level shift	34	Add R for Parade	2008/12/18	PV-1
23	ESD request	33	Add C1518,D65,D66,D67	2008/1/19	MV-1
24	ESD/ EMI request	17 38 32	C217-C219, D5-D7, D45-D47, D20, C792-C815 no stuff	2008/2/13	MV-1
25	AUDIO issue	29	C1446, C1447 change to 0805 size	2008/2/13	MV-1
26	PC Beep issue	28	change to analog GND and add separate diode	2008/2/13	MV-1
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28					

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