

Compal confidential

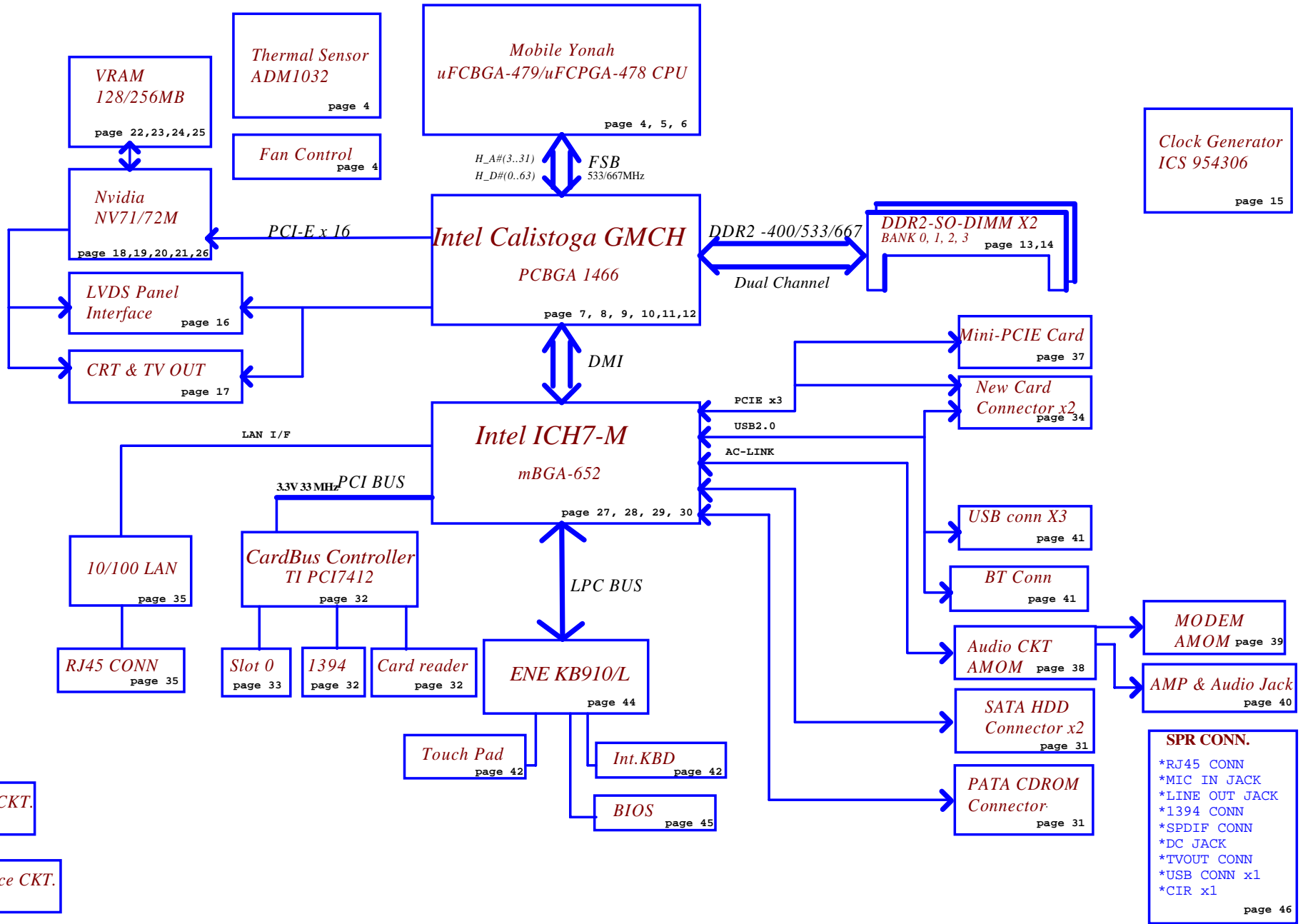
Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2005-12-15

REV:1.0

Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>		
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Size Document Number Custom <i>LA-2841</i>		
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RTC CKT.
page 29

Power On/Off CKT.
page 42

DC/DC Interface CKT.
page 47

Power Circuit DC/DC
page 48-56

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				Block Diagram	

Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
s0	○	○	○	○
s1	○	○	○	○
s3	○	○	○	✗
s5 s4/AC	○	○	✗	✗
s5 s4/ Battery only	○	✗	✗	✗
s5 s4/AC & Battery don't exist	✗	✗	✗	✗

○ MEANS ON
✗ MEANS OFF

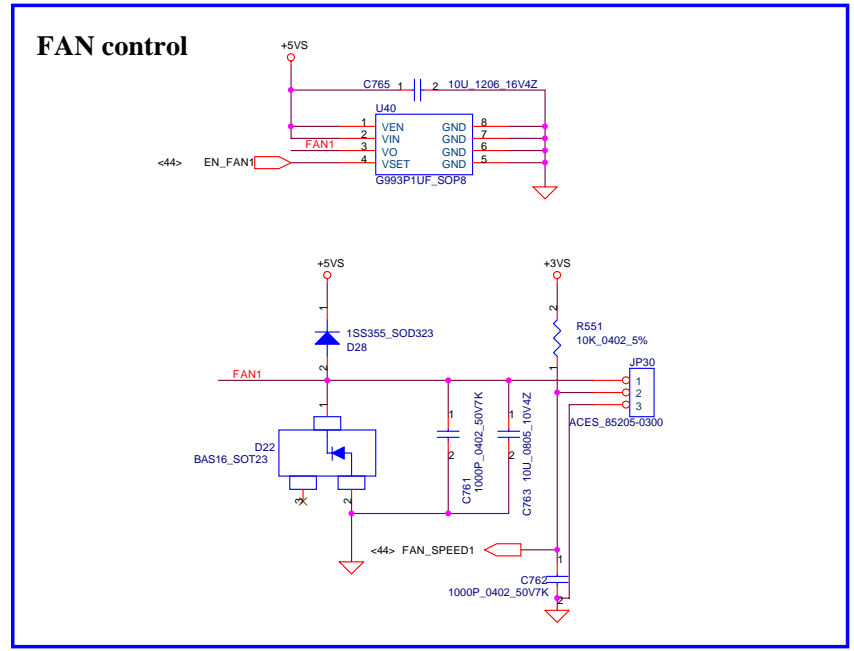
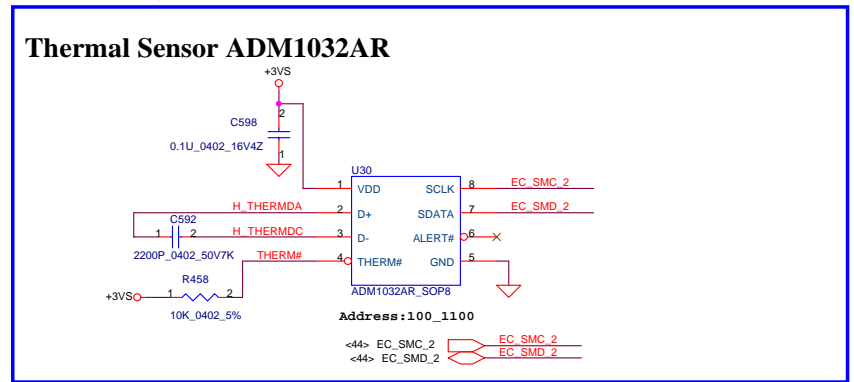
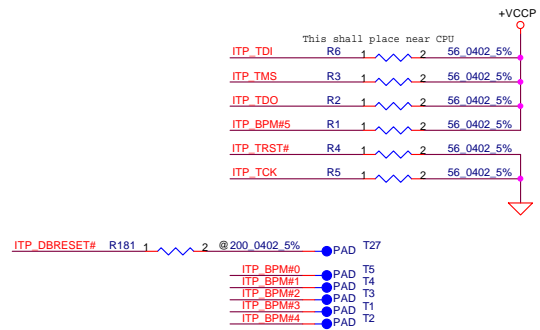
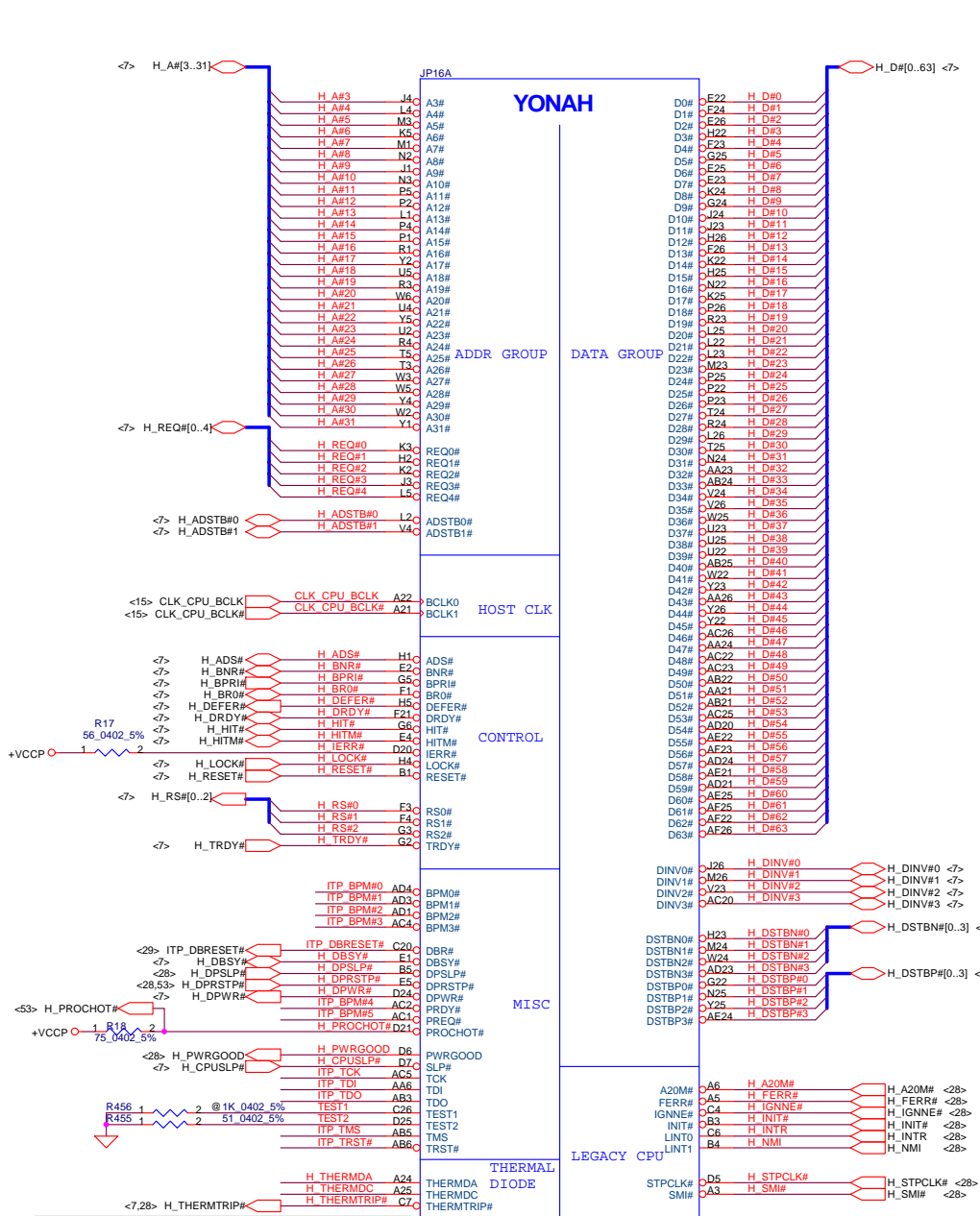
PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

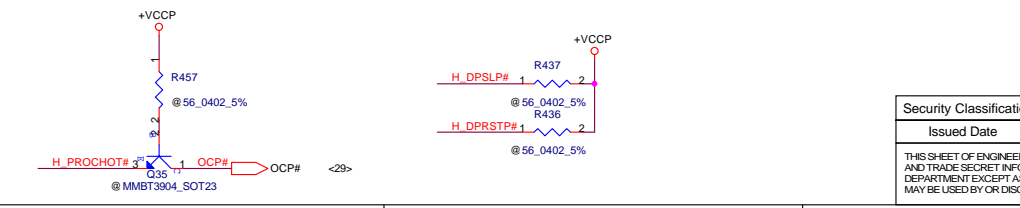
Load BOM check item

- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number
- 3.VRAM part number and Page26 RAM_CFG[0:3]/PCI_DEVID[0:3] modify check
- 4.For NV73 R510/R75/R533/R168 change to 499ohm
- 5.U33 NV7x part number

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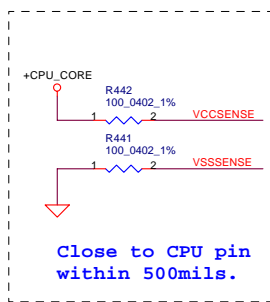
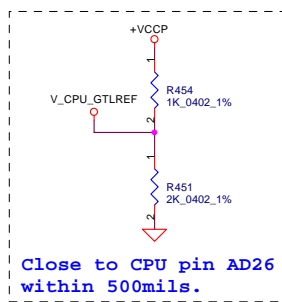
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



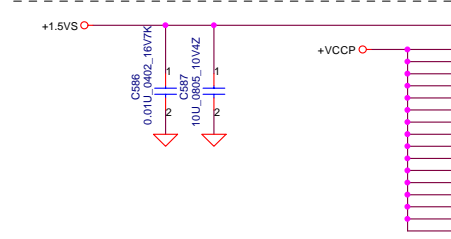
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Compal Electronics, Inc.		
Title Yonah CPU in mFCPGA479		
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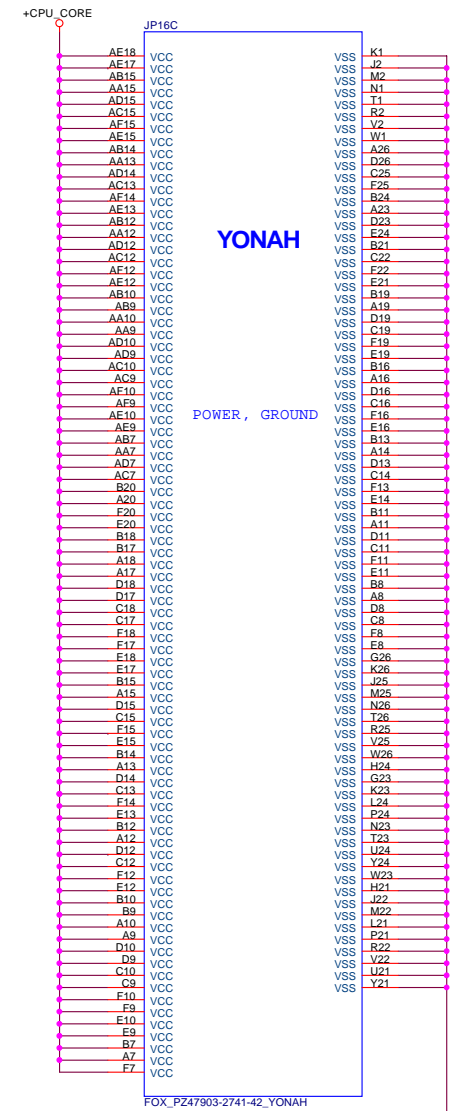
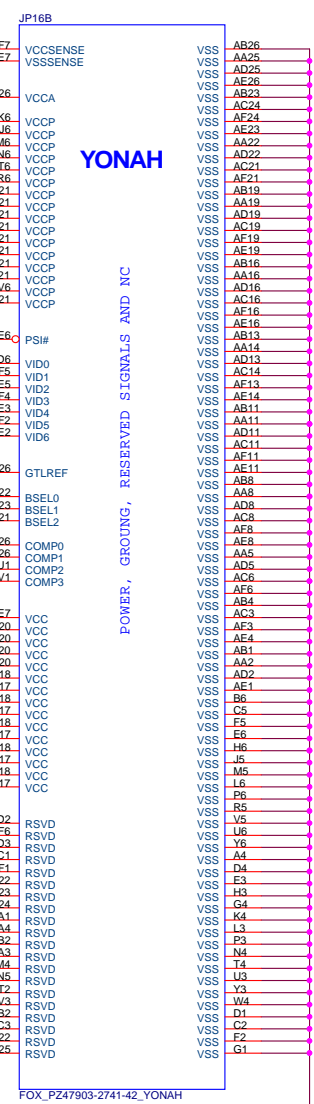
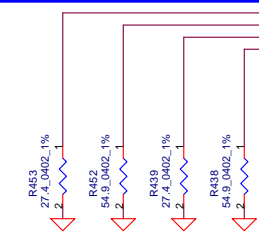


Length match within 25 mils
The trace width 18 mils space
7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

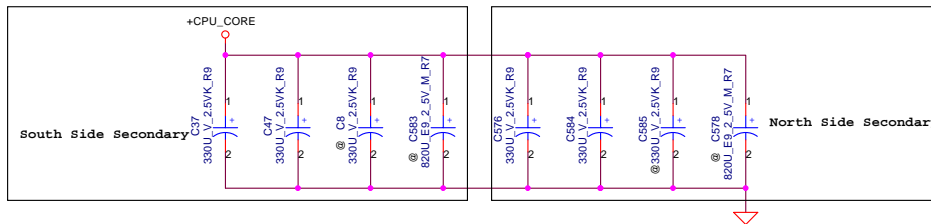
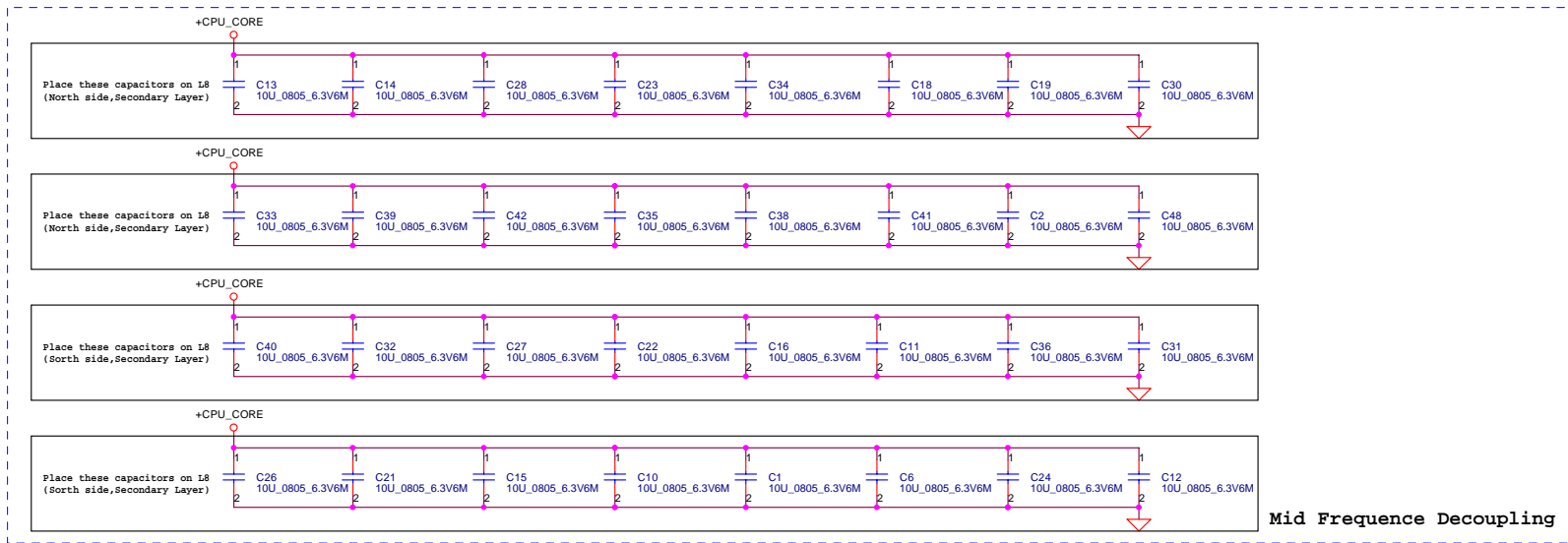
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



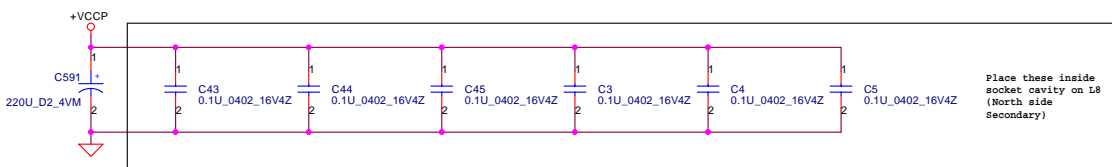
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LA-2841 <td>1A-2841 <td>1.0</td> </td>		1A-2841 <td>1.0</td>	1.0
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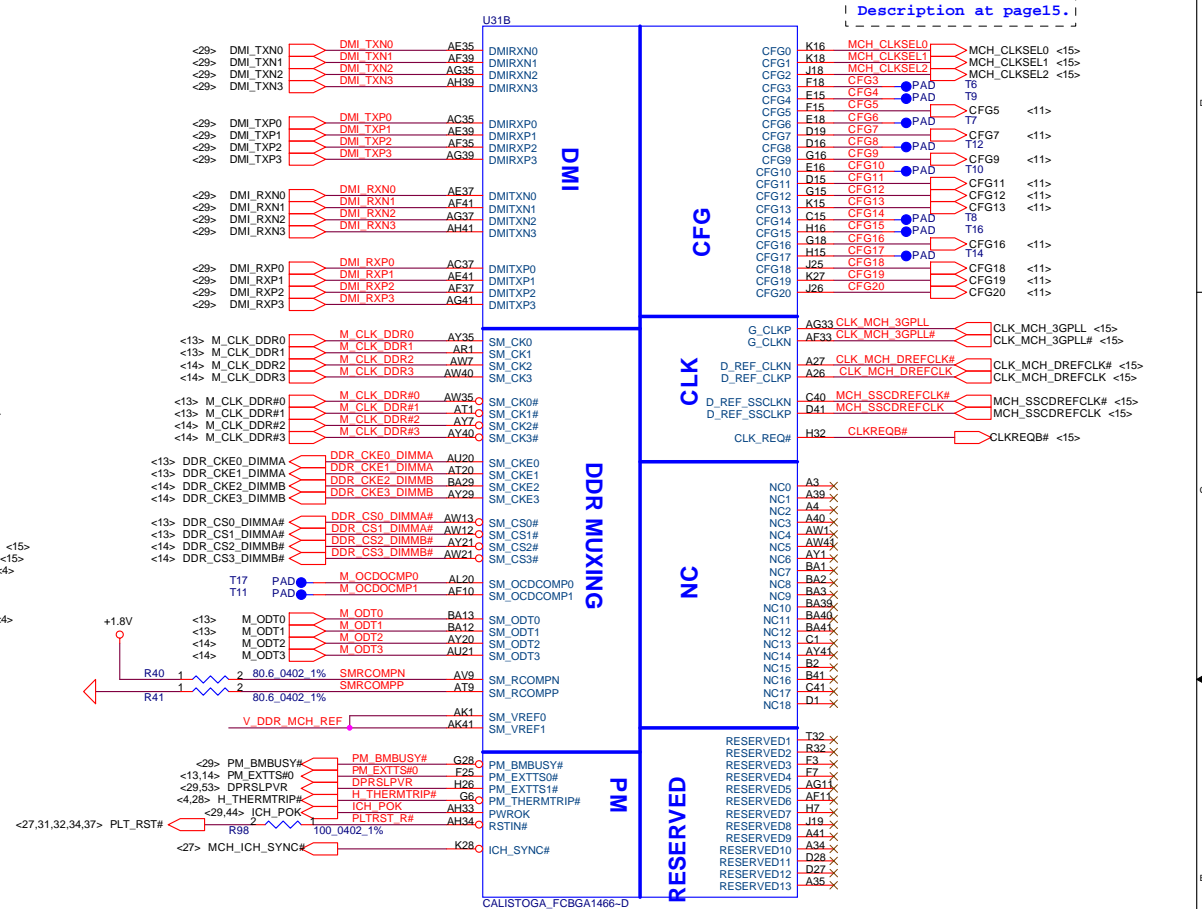
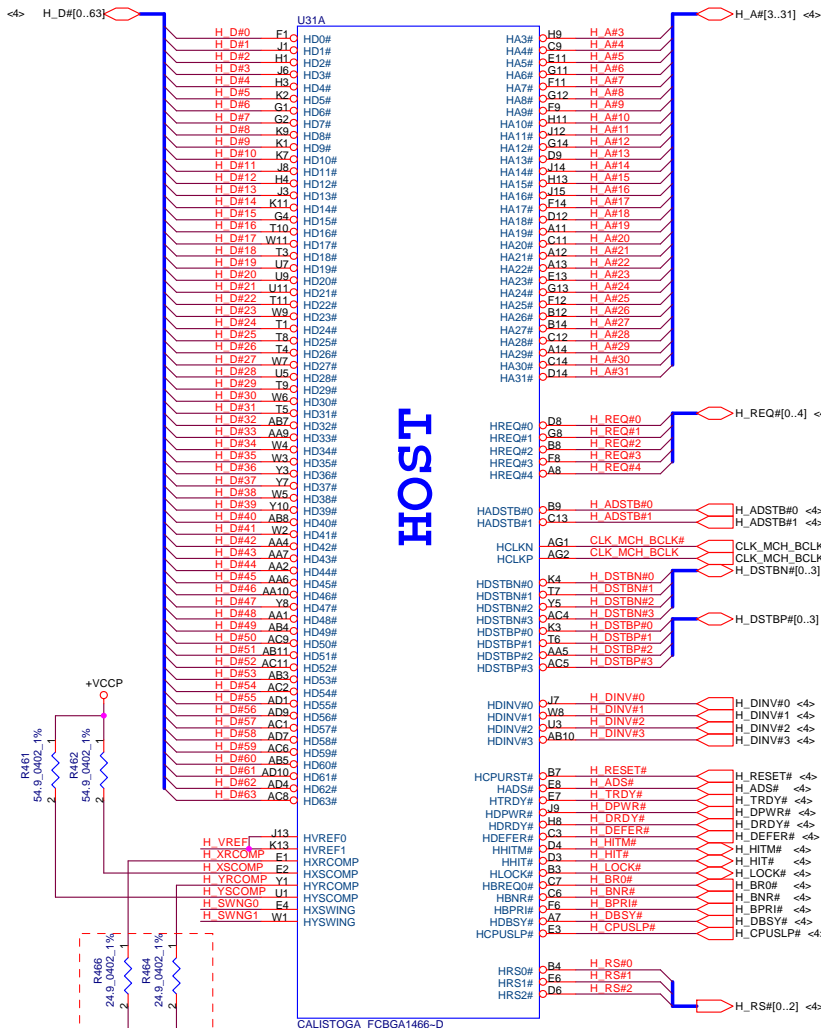


ESR <= 1.5m ohm
Capacitor > 1980uF



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Description at page 15.

HOST

DMI

CFG

CLK

DDR MUXING

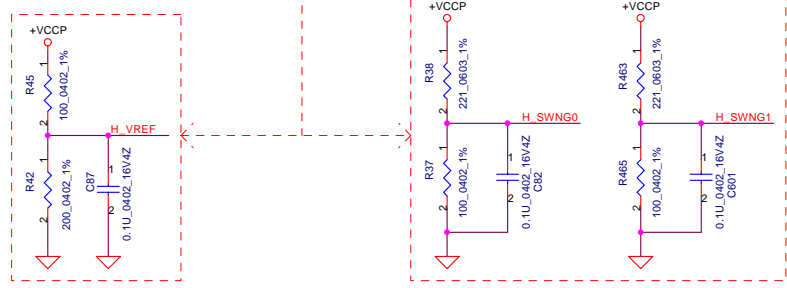
NC

PM

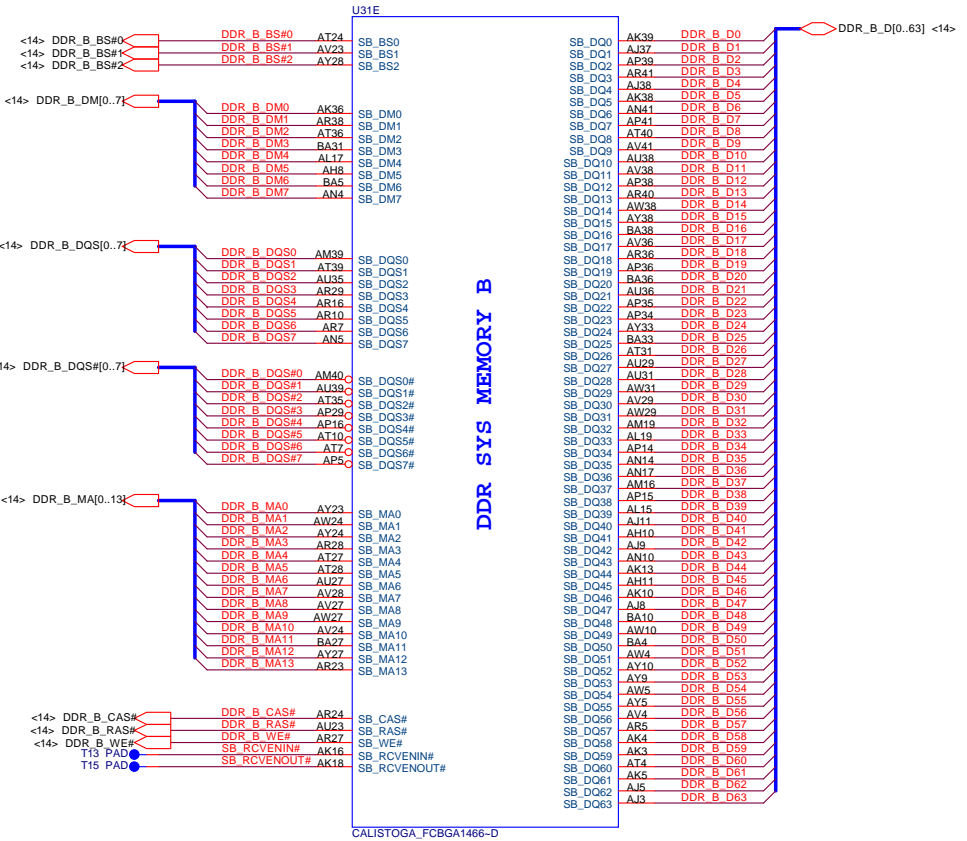
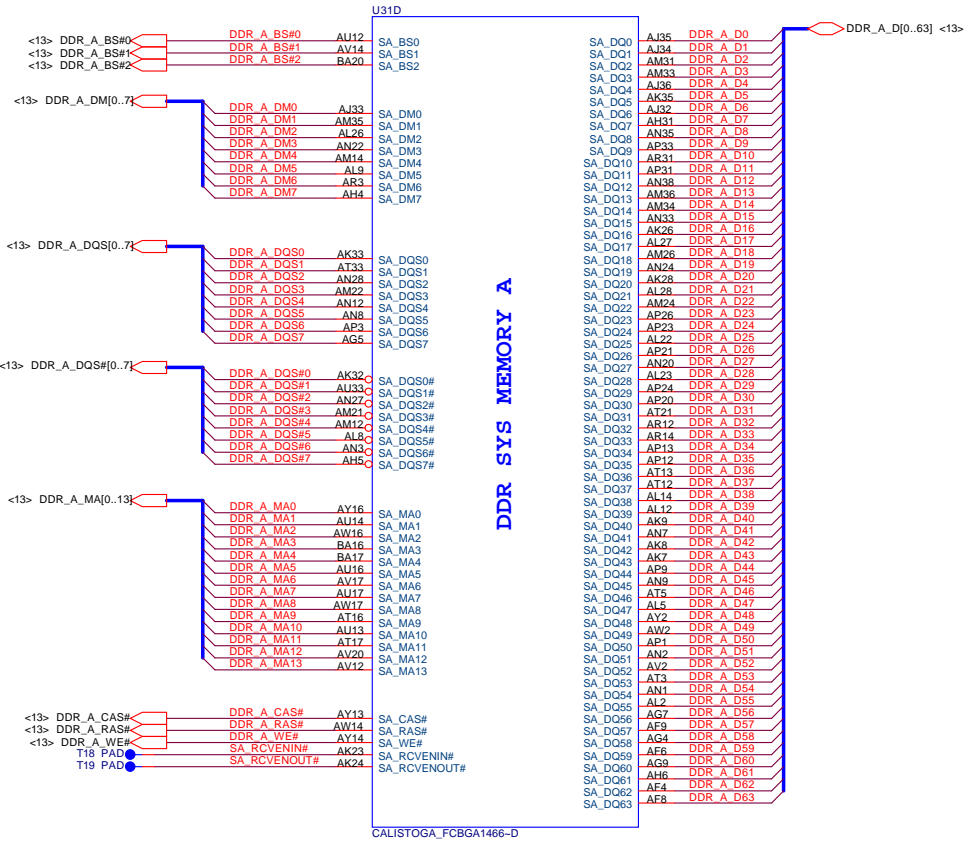
RESERVED

Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.



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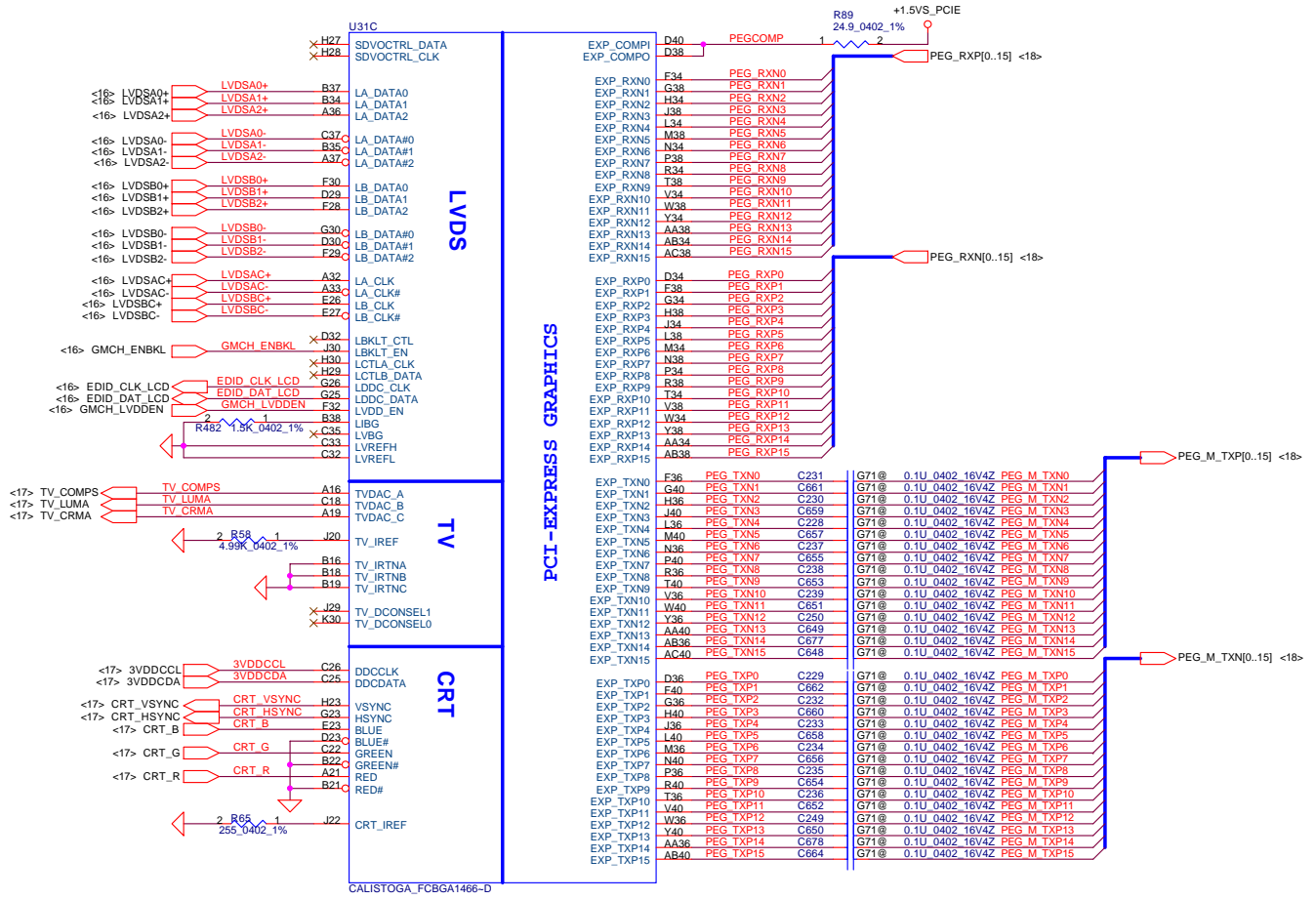
DDR SYS MEMORY A

DDR SYS MEMORY B

CALISTOGA_FCBGA1466-D

CALISTOGA_FCBGA1466-D

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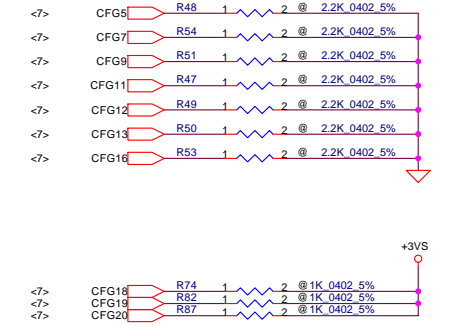
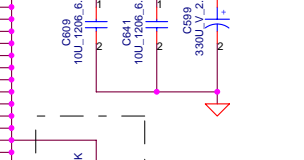
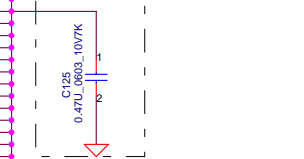
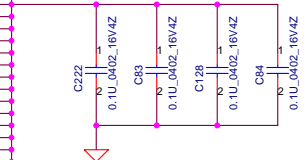
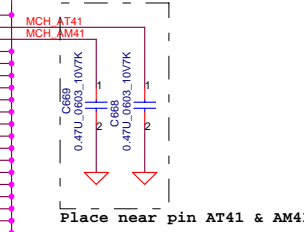
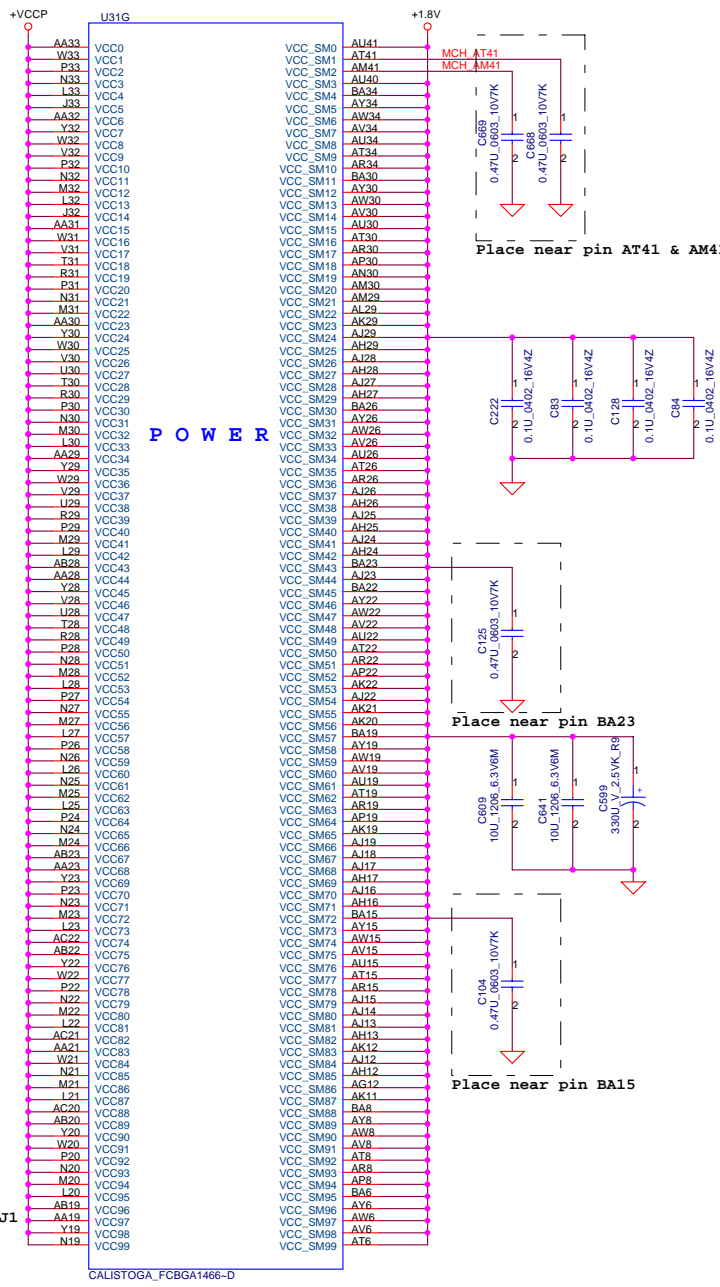
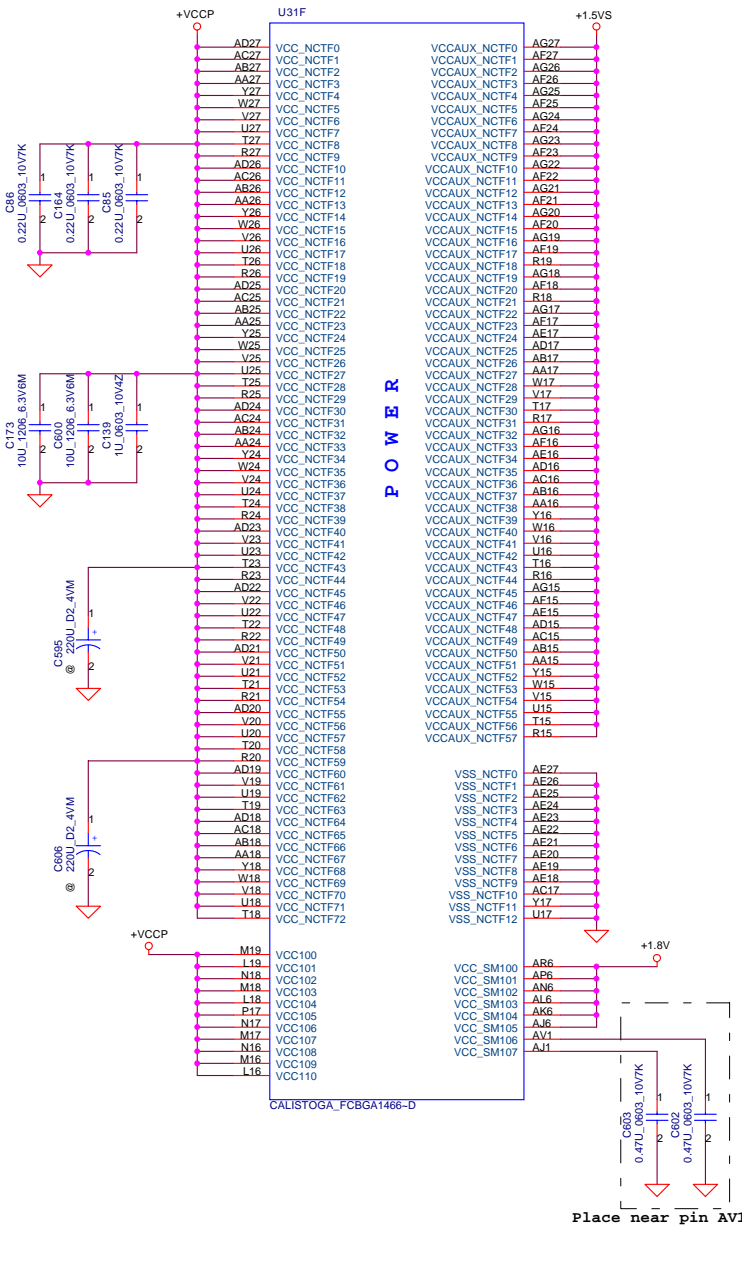
CALISTOGA_FCBGA1466-D

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Strap Pin Table

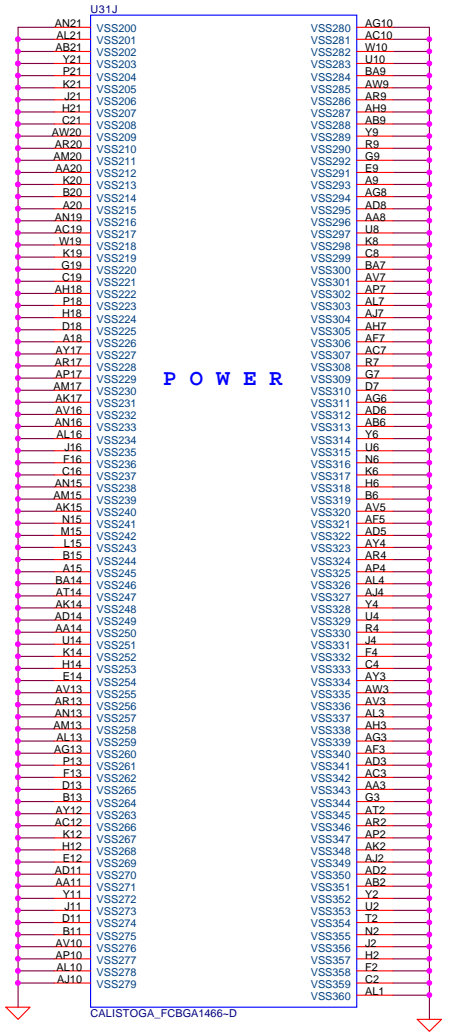
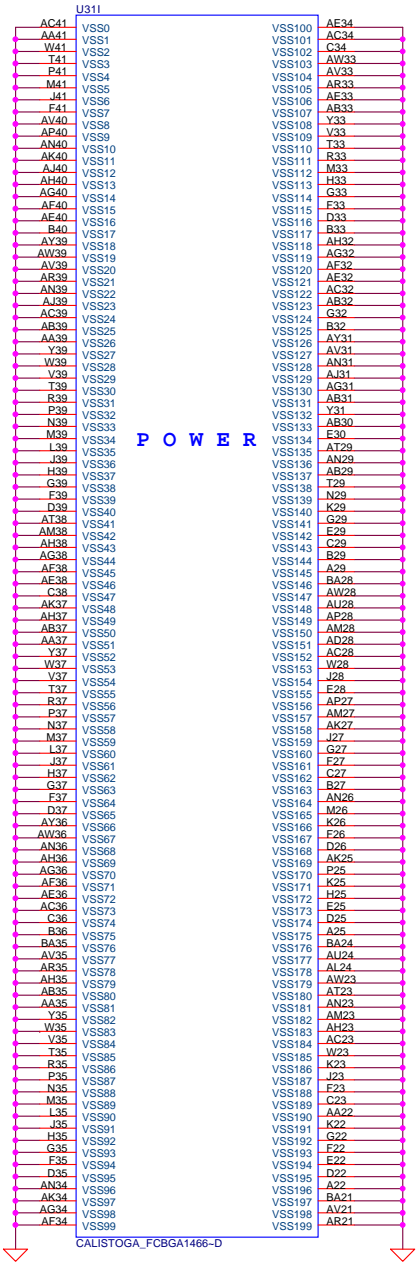
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG6	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

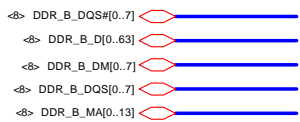


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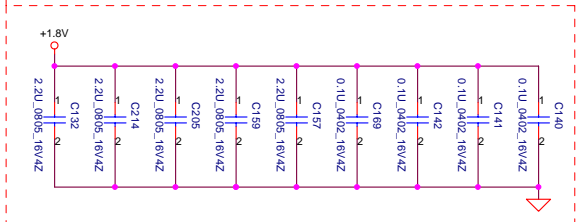
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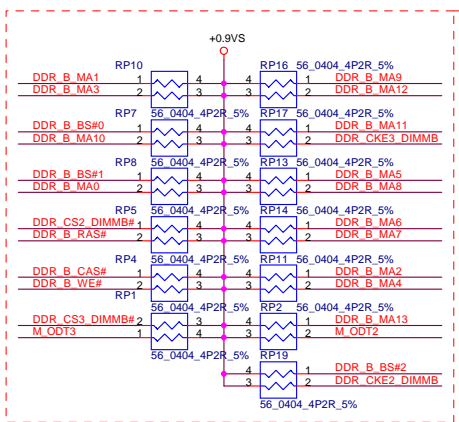
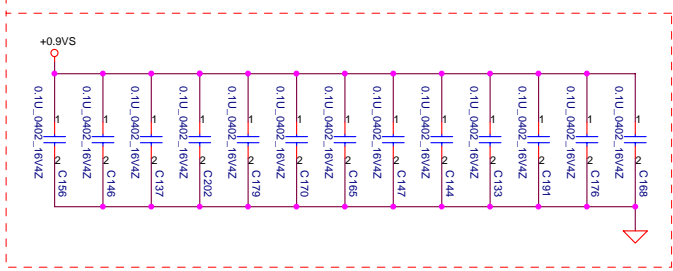
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Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



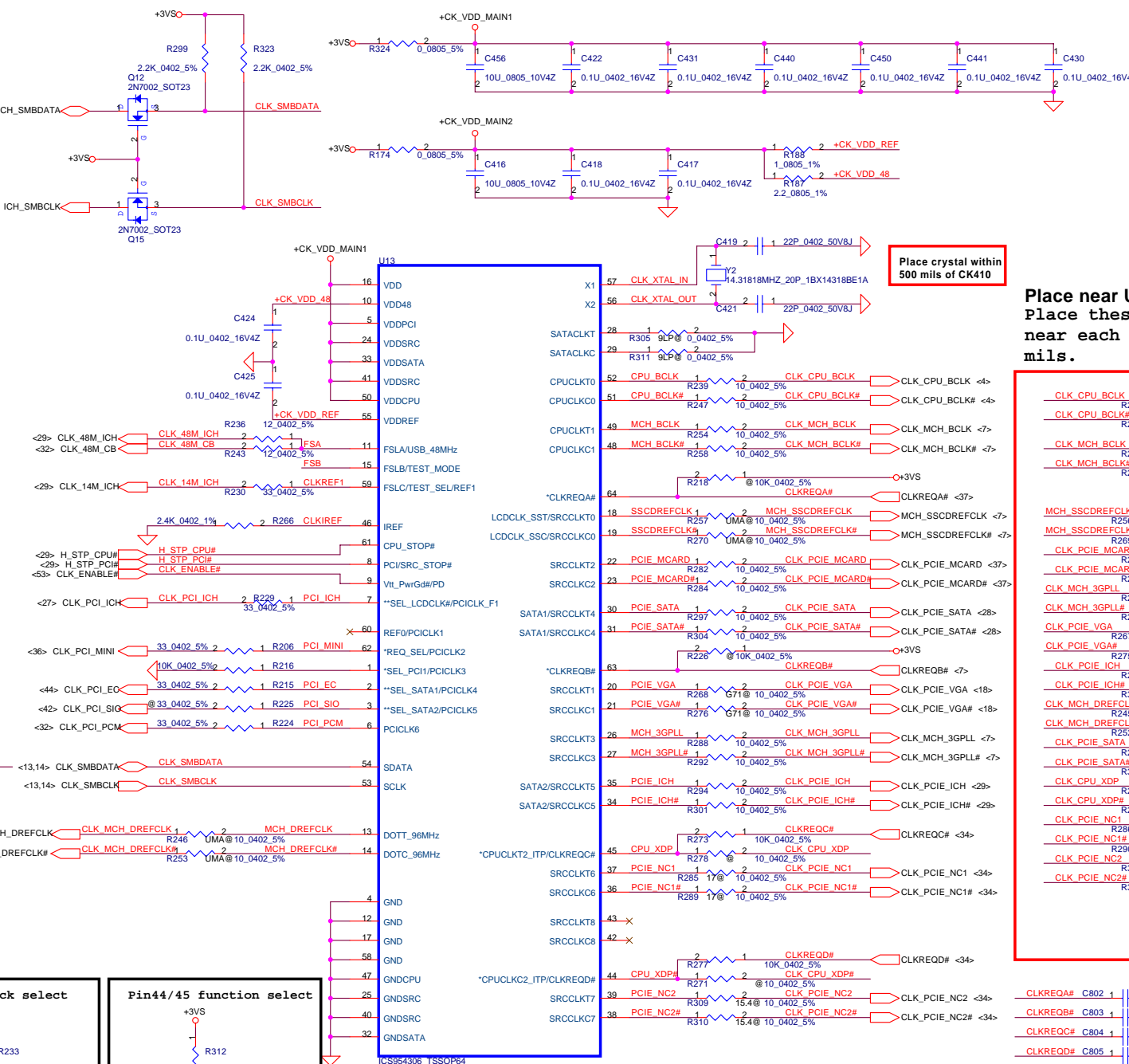
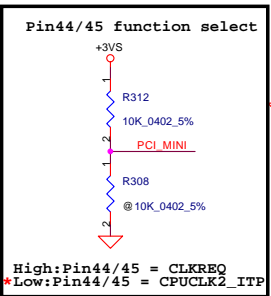
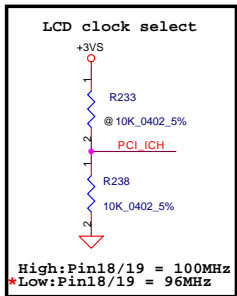
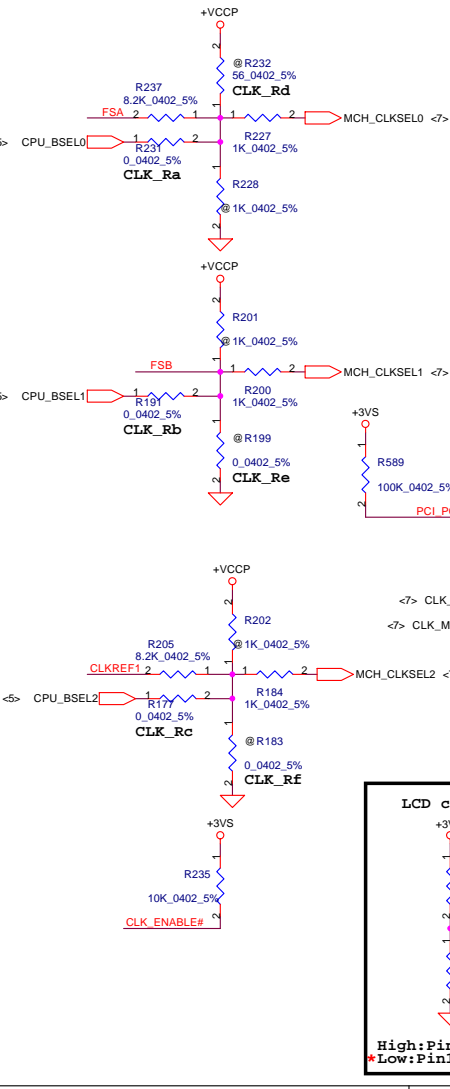
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

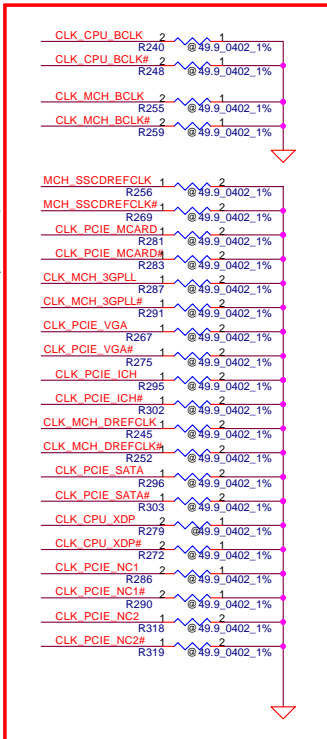
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
*(Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
	533MHz	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



Place crystal within 500 mils of CK410

Place near U54
Place these components near each pin within 40 mils.

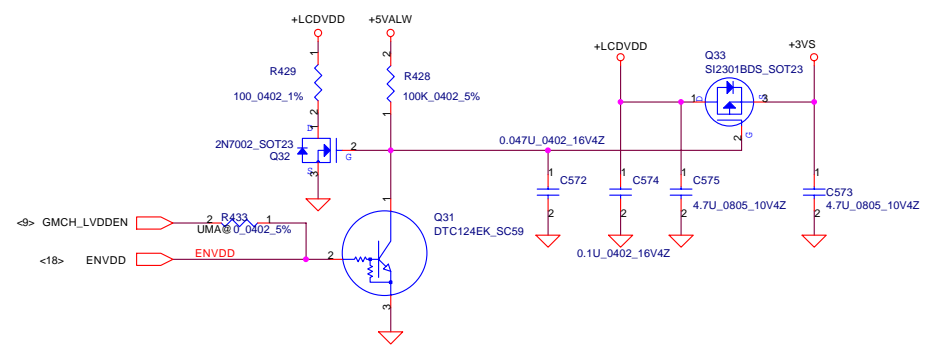
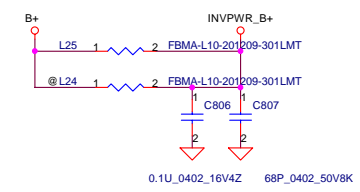
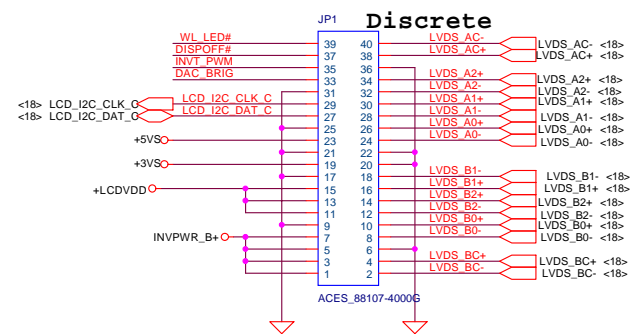
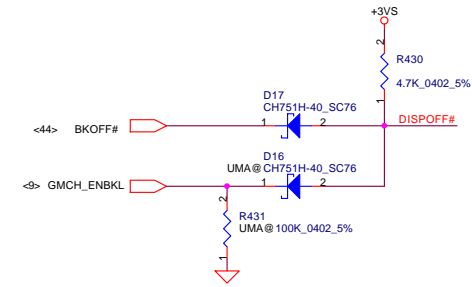
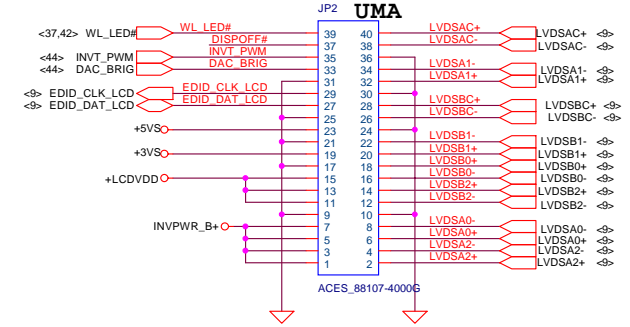
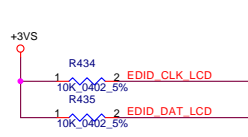


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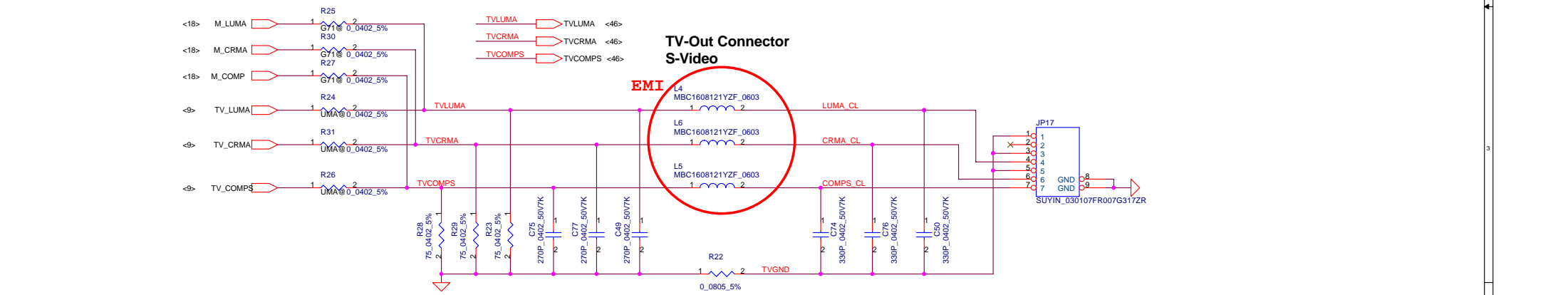
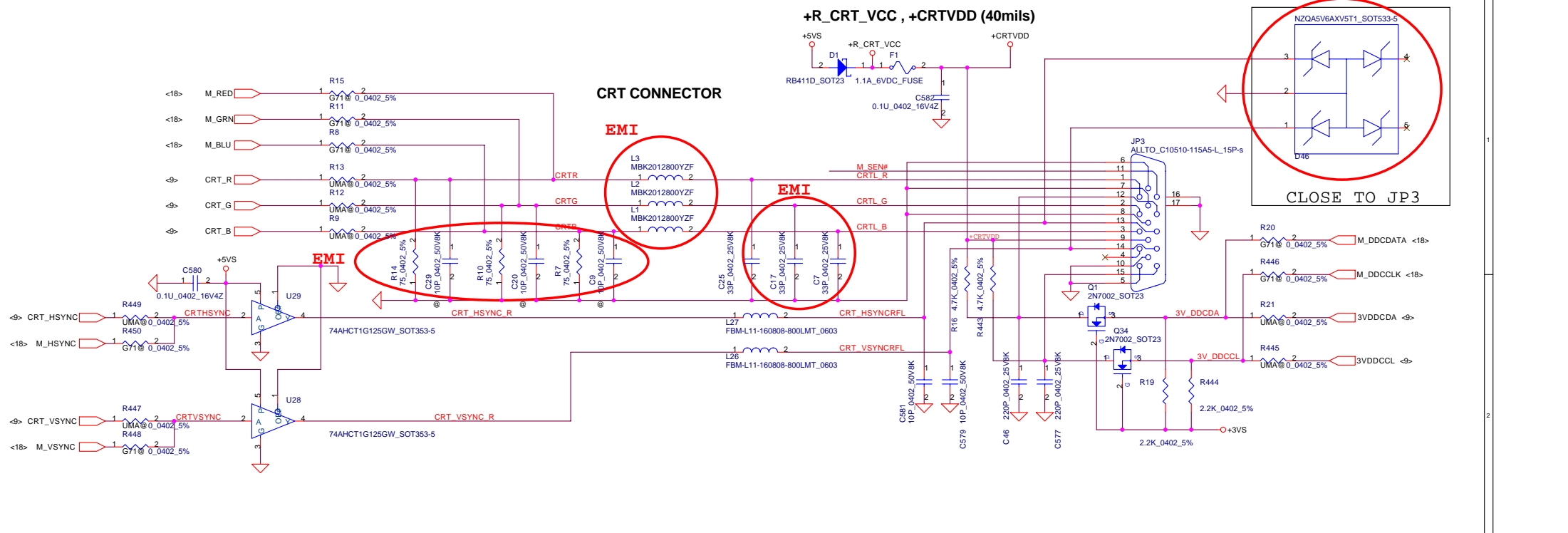
Compal Electronics, Inc.		
Clock generator		
Size	Document Number	Rev
	LA-284I	1.0
Date:	Thursday, December 15, 2005	Sheet 15 of 60

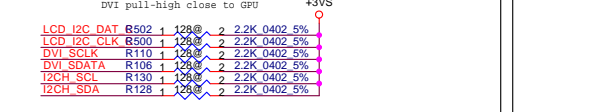
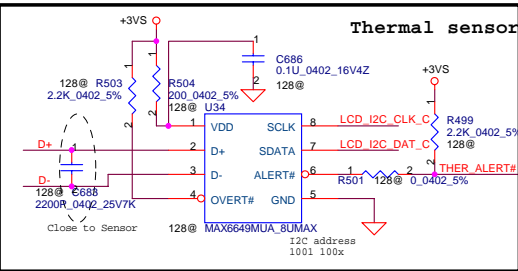
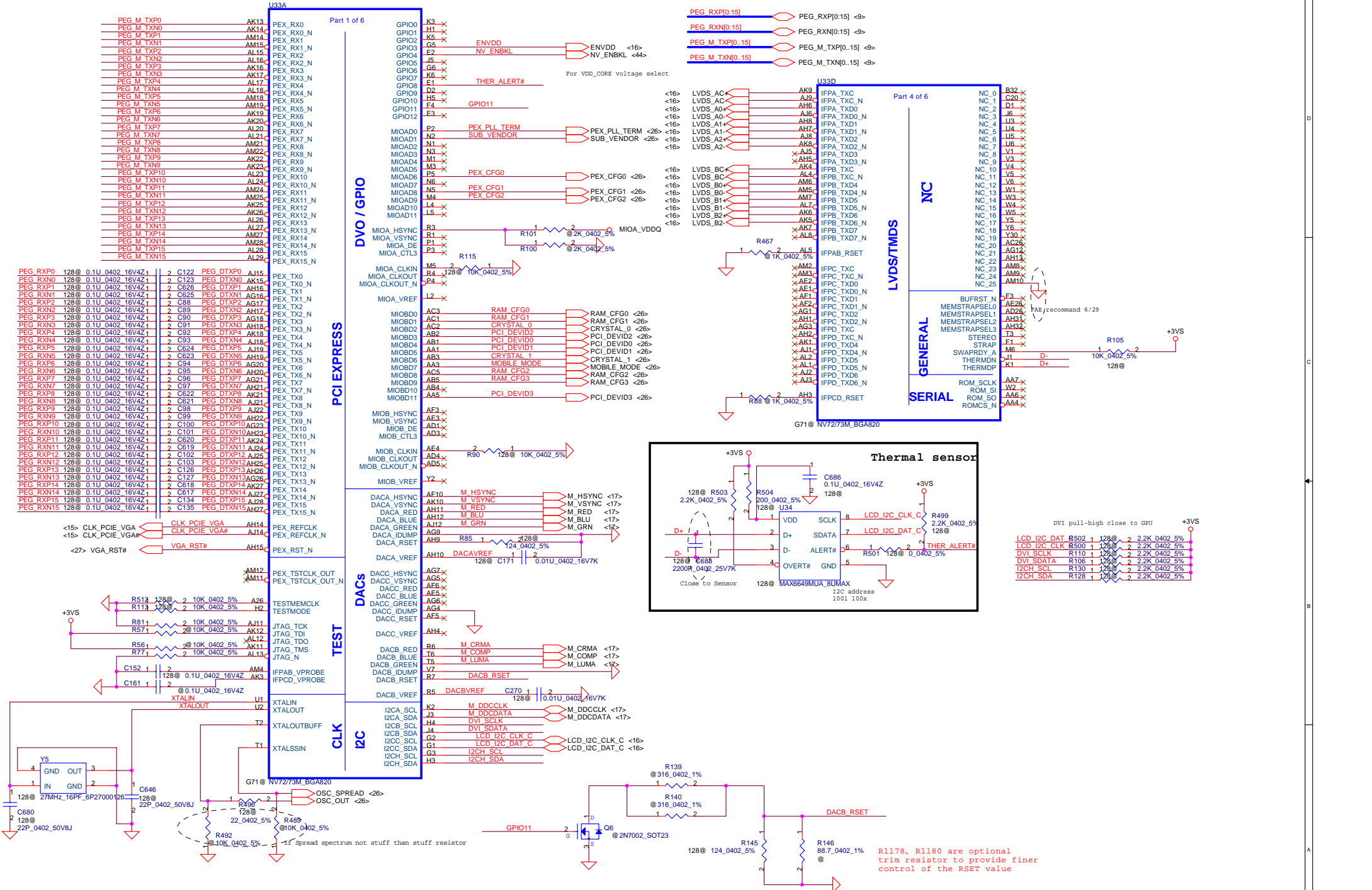
LCD Panel & inverter Connector



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Issued Date	2005/03/10	Deciphered Date
		2006/03/10
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Compal Electronics, Inc.		
Title	LVDS Connector	
Size	Document Number	Rev
Custom	LA-2841	1.0
Date:	Thursday, December 15, 2005	Sheet 16 of 60

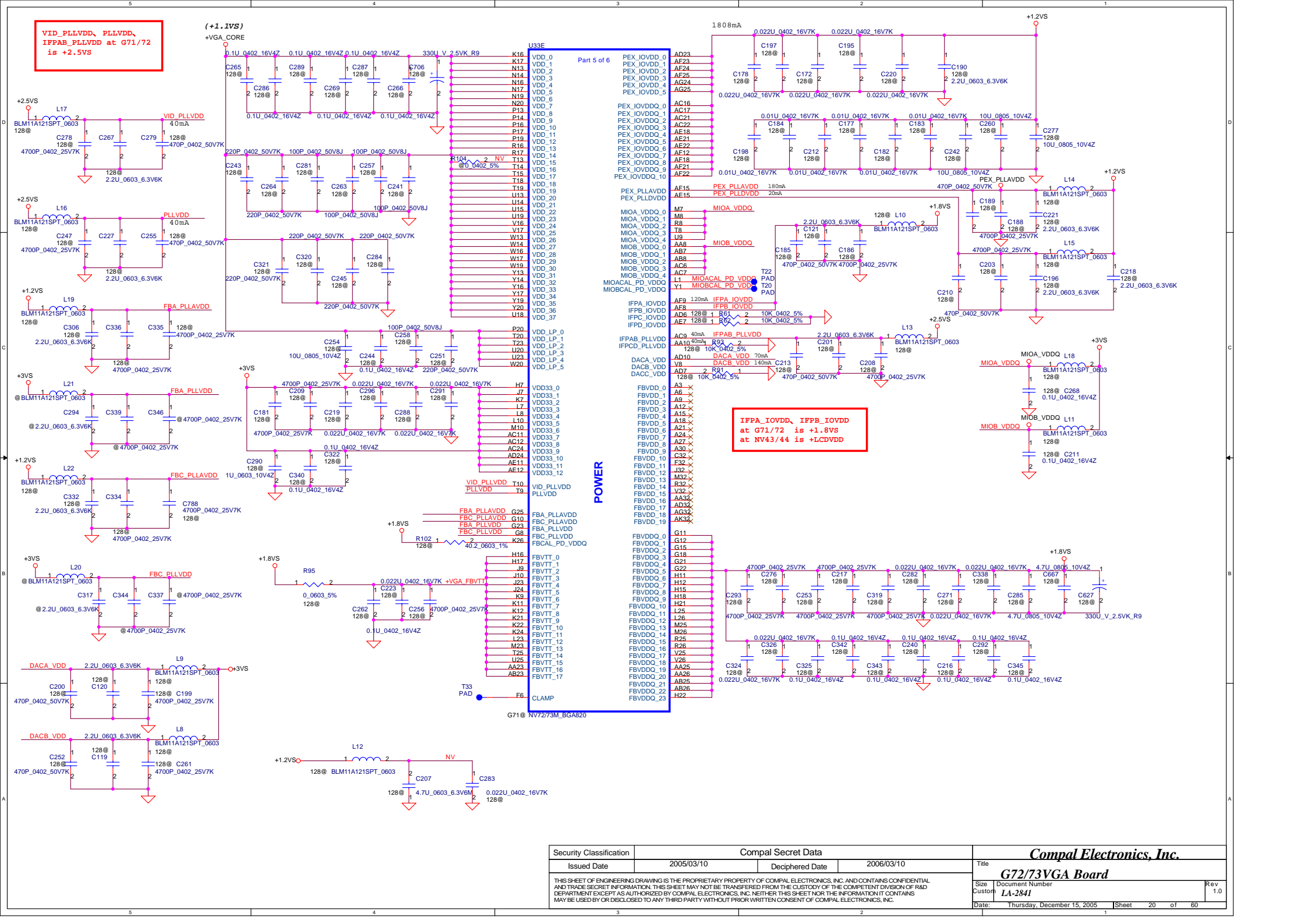




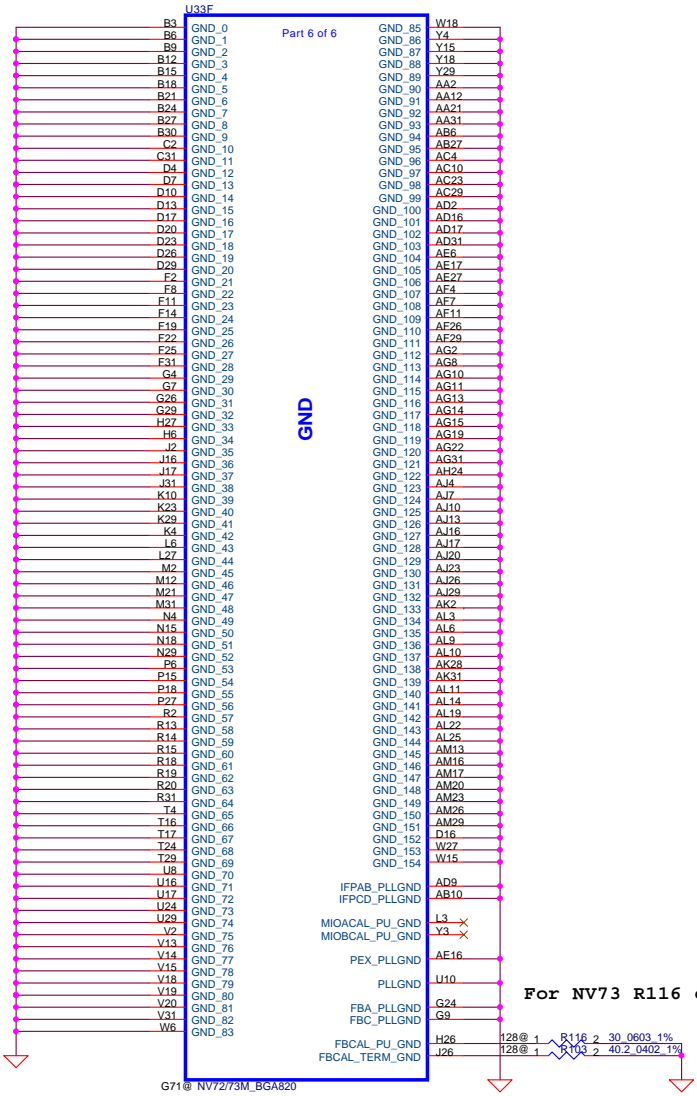
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	G72/73VGA Board
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Size	Document Number	Rev	1.0	
Custom	LA-2841	Date:	Thursday, December 15, 2005	Sheet 18 of 60

VID_PLLVDD, PLLVDD, IFPAB_PLLVDD at G71/72 is +2.5VS

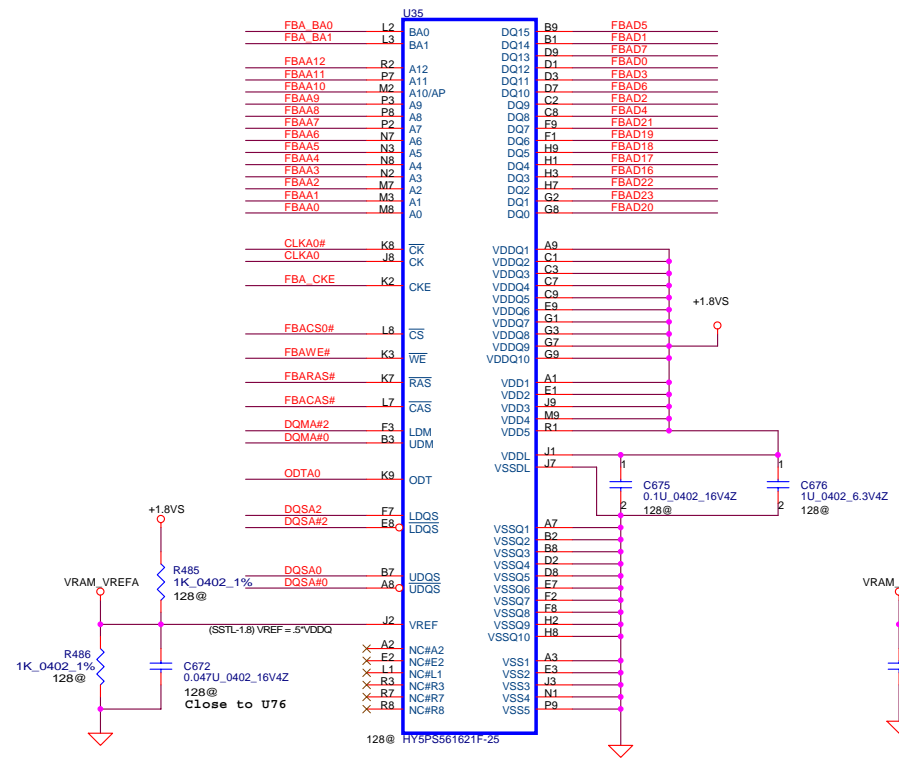
IFPPA_IOVDD, IFPPB_IOVDD at G71/72 is +1.8VS at NV43/44 is +LCDVDD



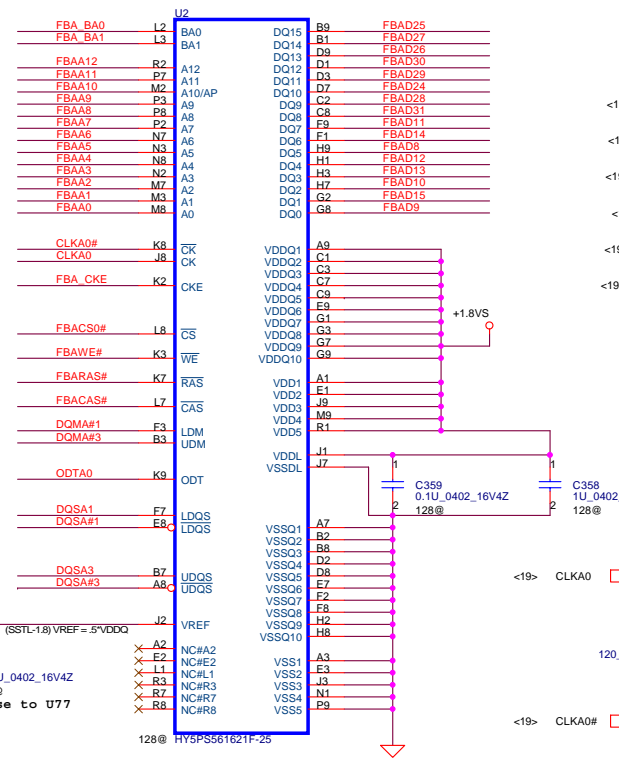
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
				G72/73VGA Board	
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				Custom	LA-2841
				Date:	Thursday, December 15, 2005
				Sheet	20 of 60
				Rev	1.0



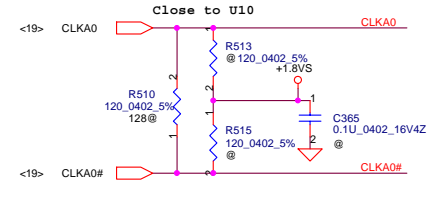
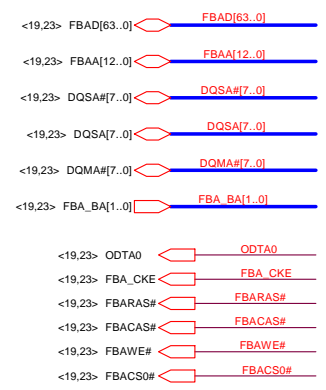
Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	G72/73VGA Board	
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				Date:	Thursday, December 15, 2005
				Sheet	21 of 60
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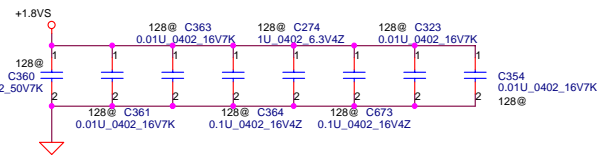
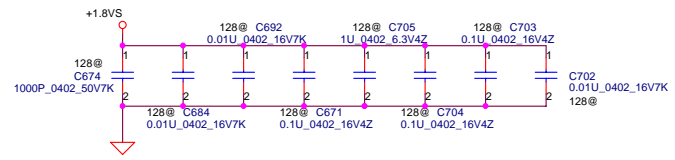
DDR2 BGA MEMORY



DDR2 BGA MEMORY

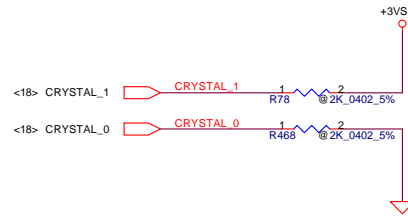


For NV73 R510 change to 481_0402_1%(SD0000CA80)

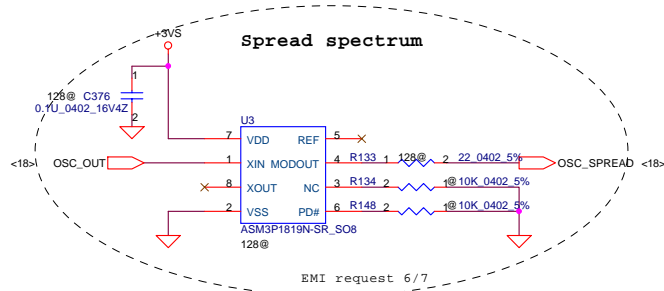
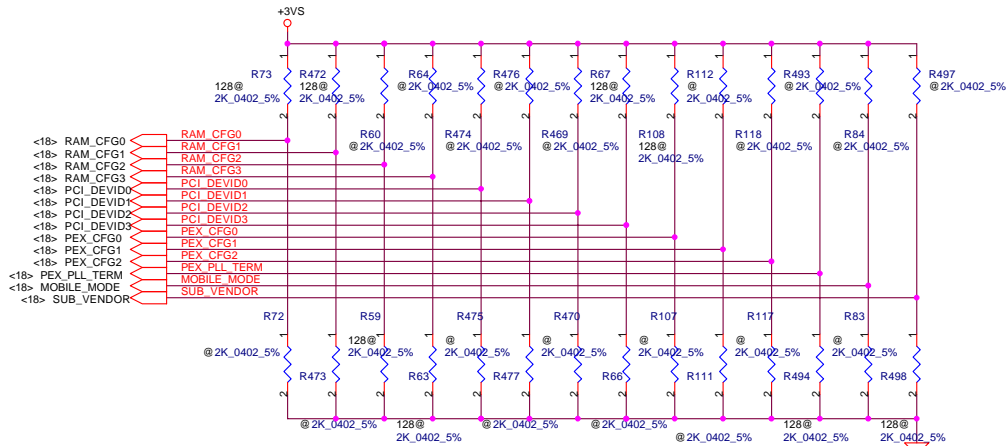


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Issued Date	2005/03/10	Deciphered Date
		2006/03/10
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Compal Electronics, Inc.		
Title	G72/73VGA Board	
Size	Document Number	Rev
Custom	LA-2841	1.0
Date:	Thursday, December 15, 2005	Sheet 22 of 60



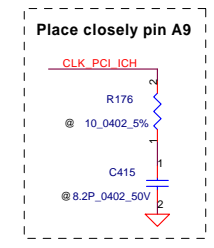
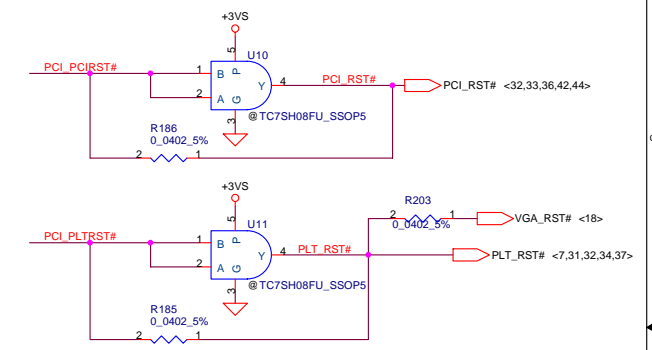
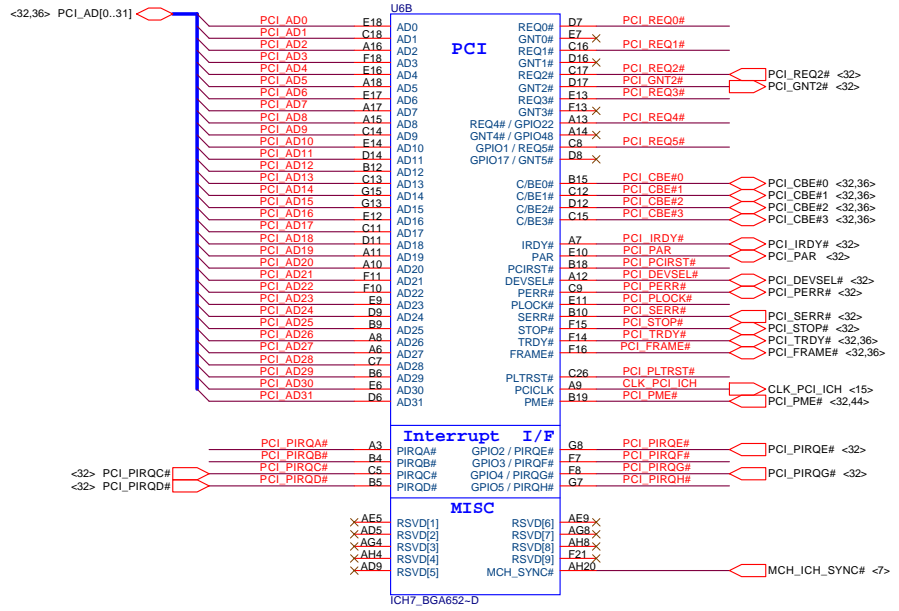
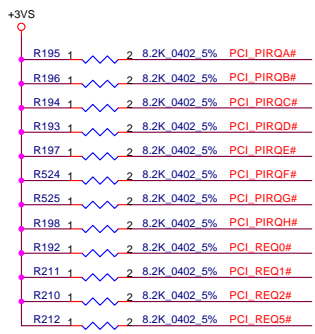
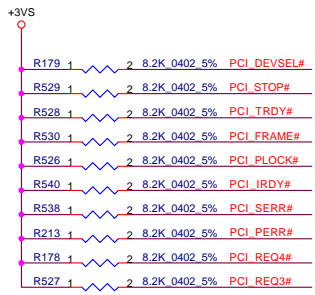
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CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Overridden	001	
RAM_CFG[3:0]		16Mx16 (1.8V or 2.5V)Hynix X 4pcs	0011	
		16Mx16 (1.8V or 2.5V)Infineon X 4pcs	0010	
		16Mx16 (1.8V or 2.5V)Samsung X 4pcs	0001	
		16Mx16 (1.8V or 2.5V)Hynix X 8pcs	1011	
		16Mx16 (1.8V or 2.5V)Infineon X 8pcs	1010	
		16Mx16 (1.8V or 2.5V)Samsung X 8pcs	1001	
PCI_DEVID[3:0]	R01 VTPD[5:3]	NV72M	1000	
	MIOA_HSYNC	NV73M	1000	



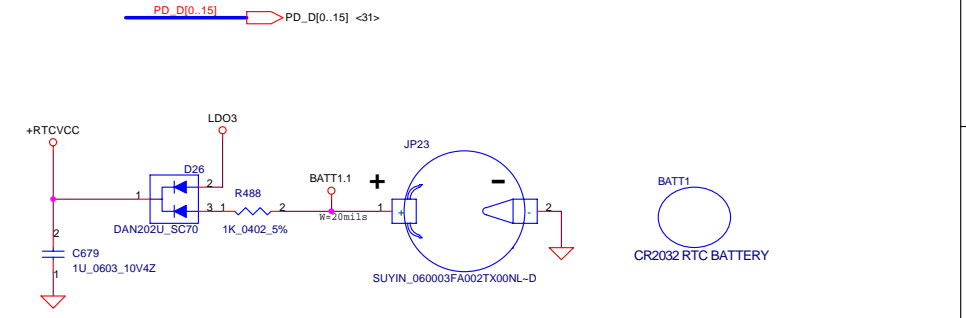
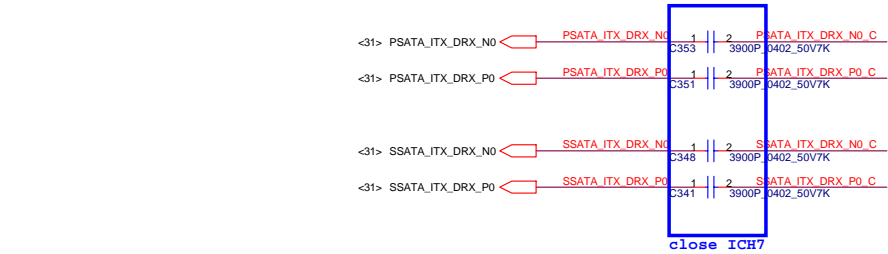
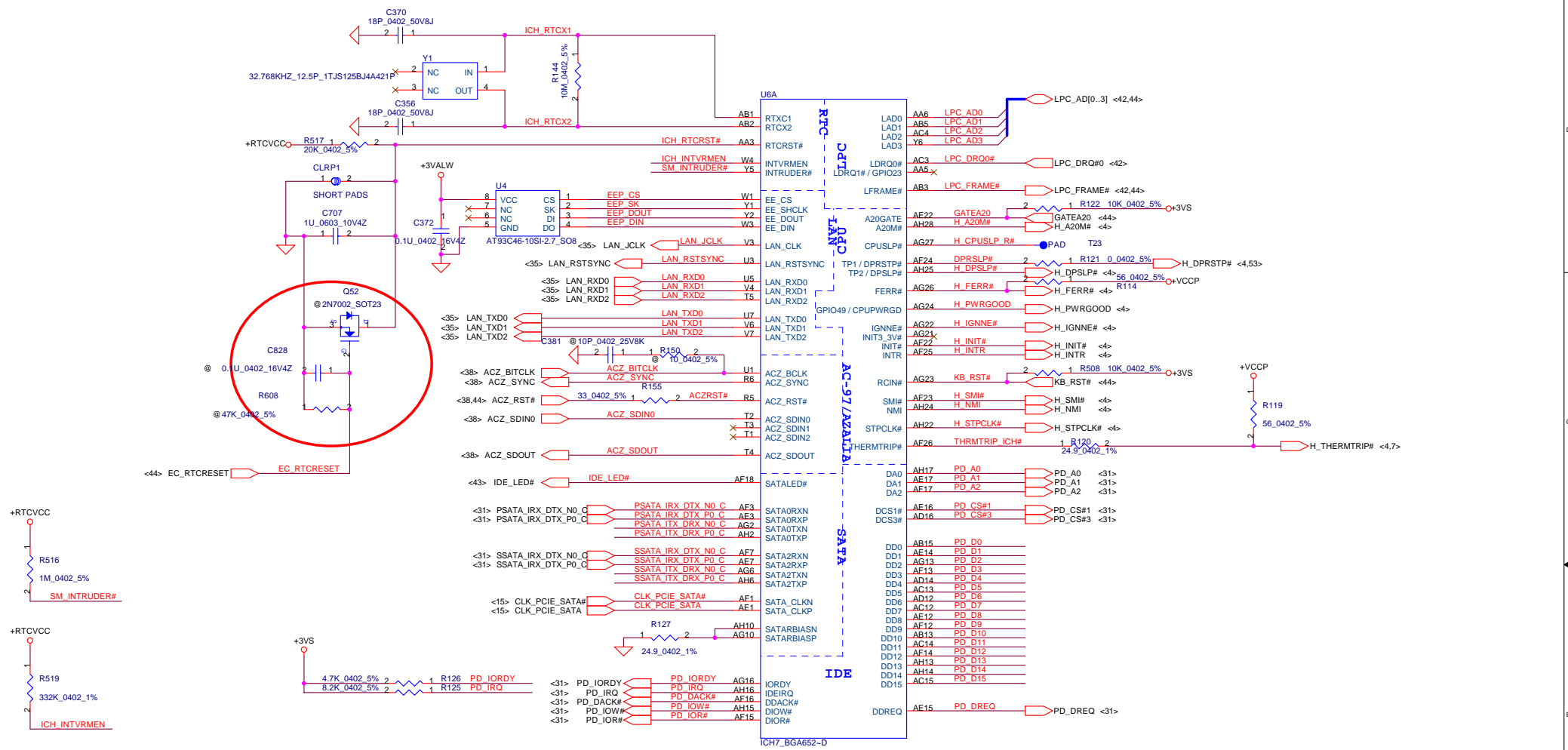
Security Classification	Compal Secret Data	
Issued Date	2005/03/01	Deciphered Date
		2006/03/01

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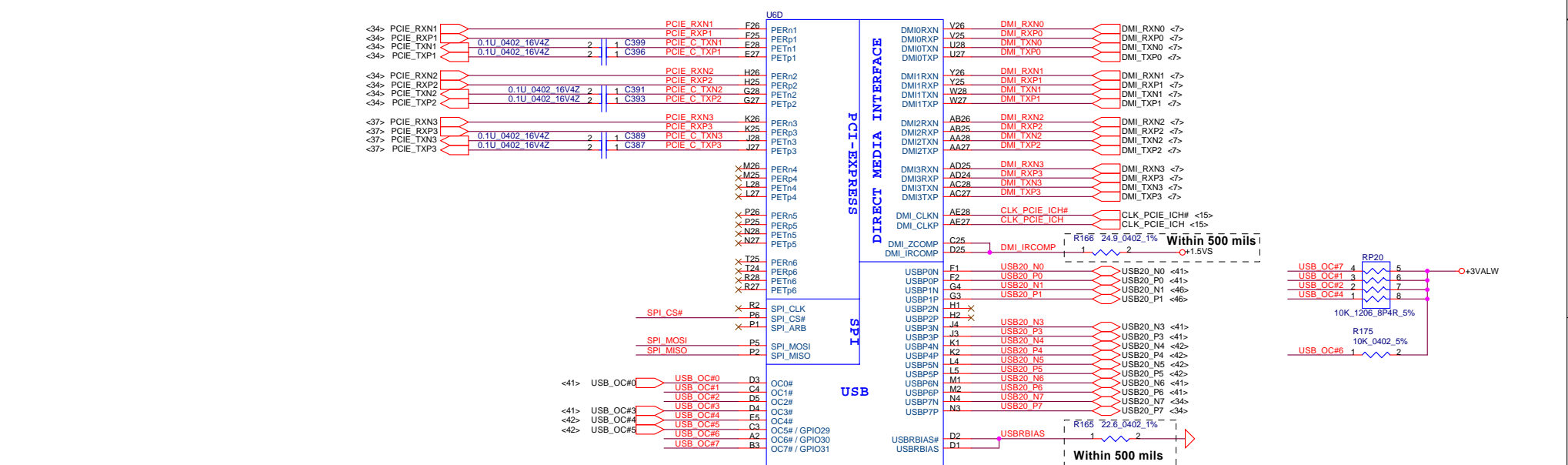
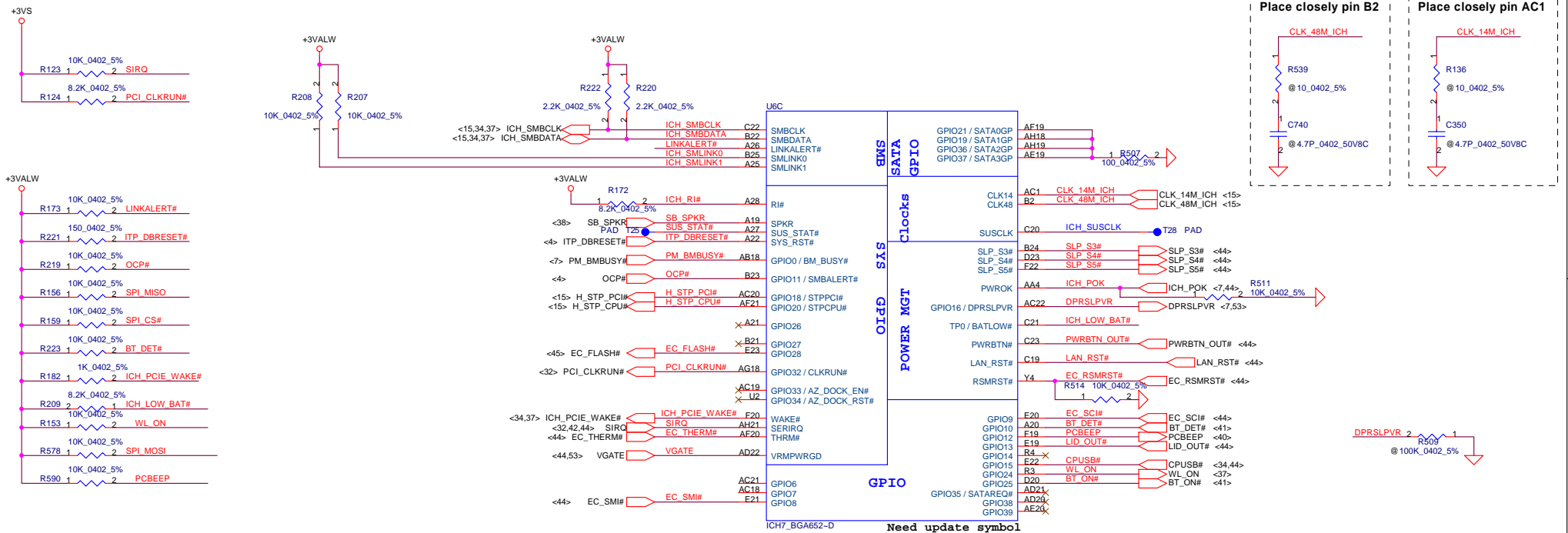
Title		
Compal Electronics, Inc.		
G71/72 VGA Board		
Size	Document Number	Rev
Custom	LA-2841	1.0
Date:	Thursday, December 15, 2005	Sheet 26 of 60



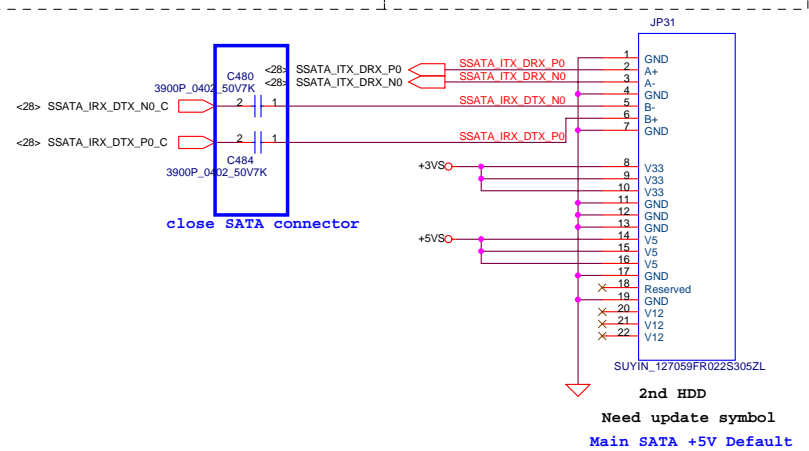
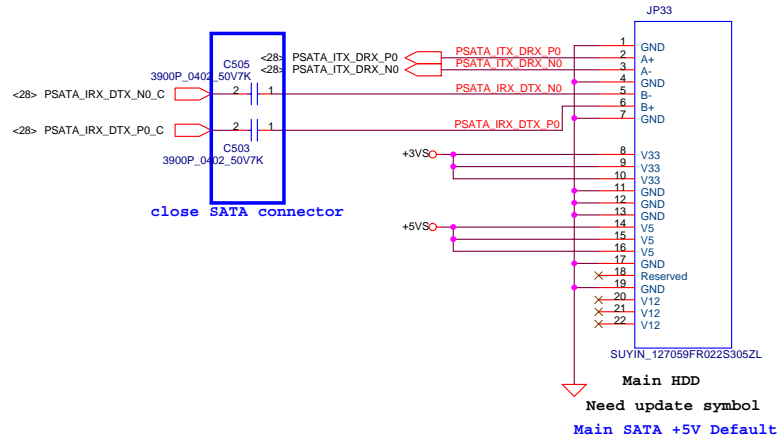
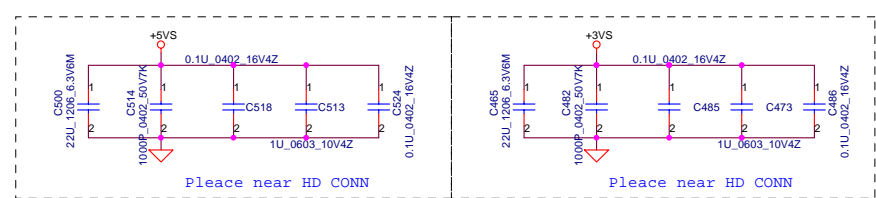
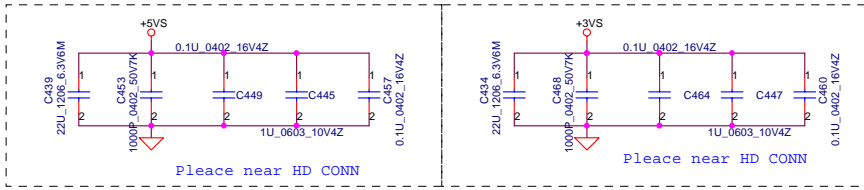
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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Date:	Thursday, December 15, 2005	Sheet	27 of 60	Rev 1.0



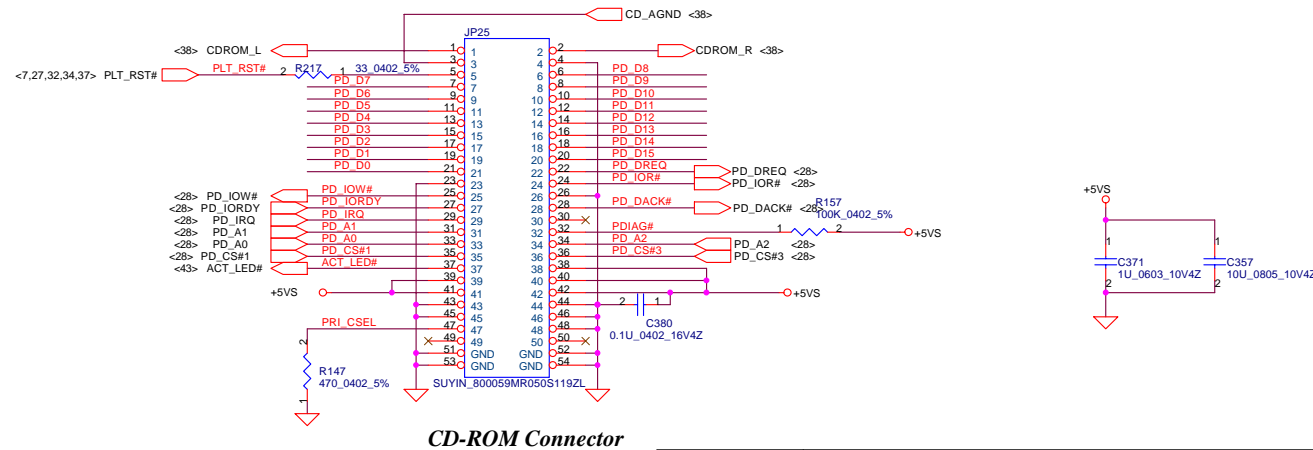
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Size	Document Number
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				Date:	Thursday, December 15, 2005
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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Size	Document Number	Rev		
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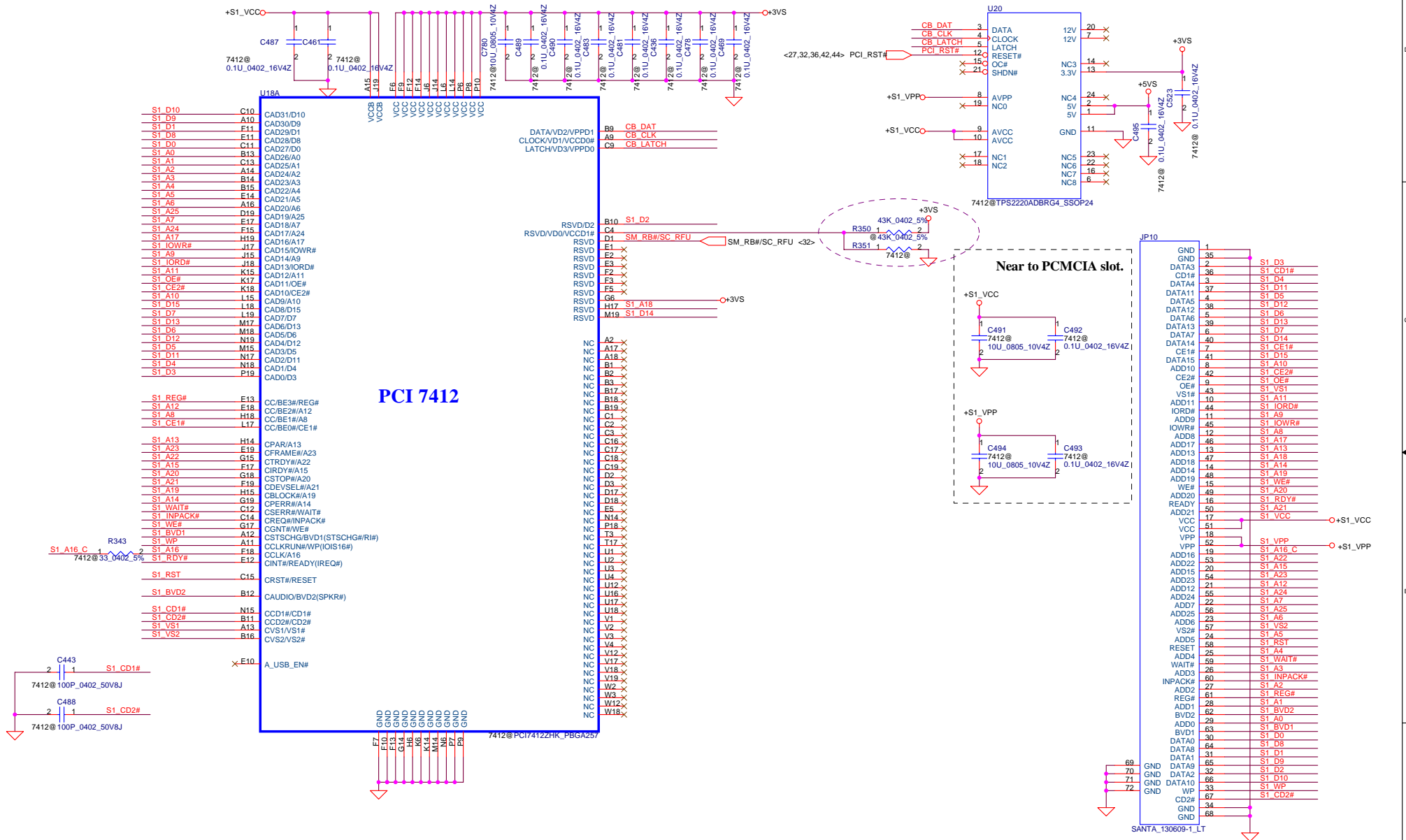
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CD-ROM Connector

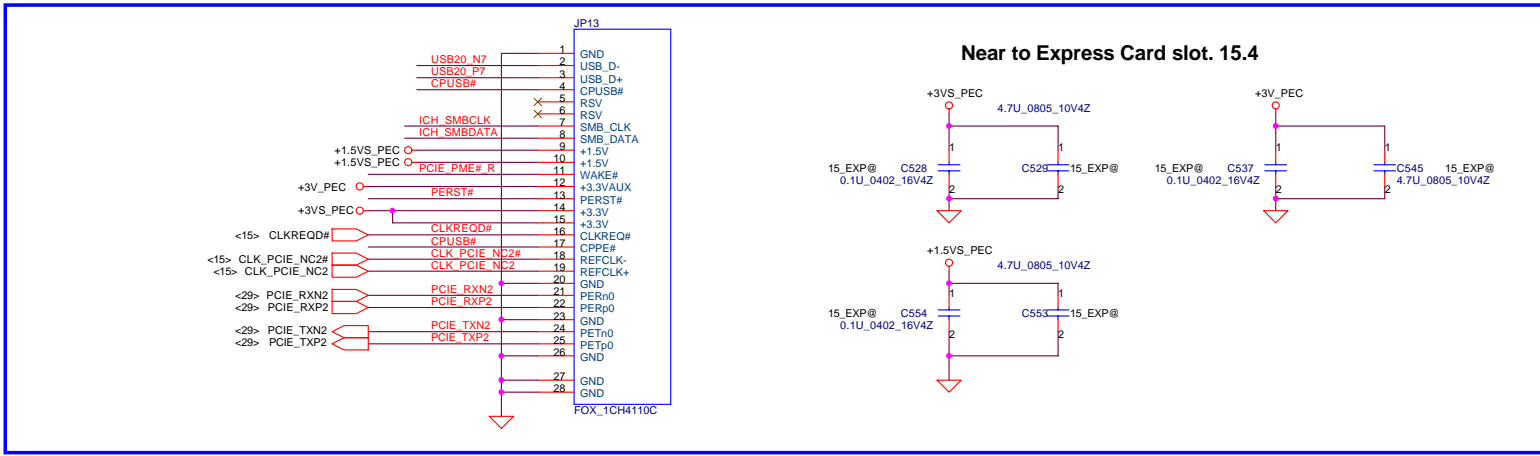
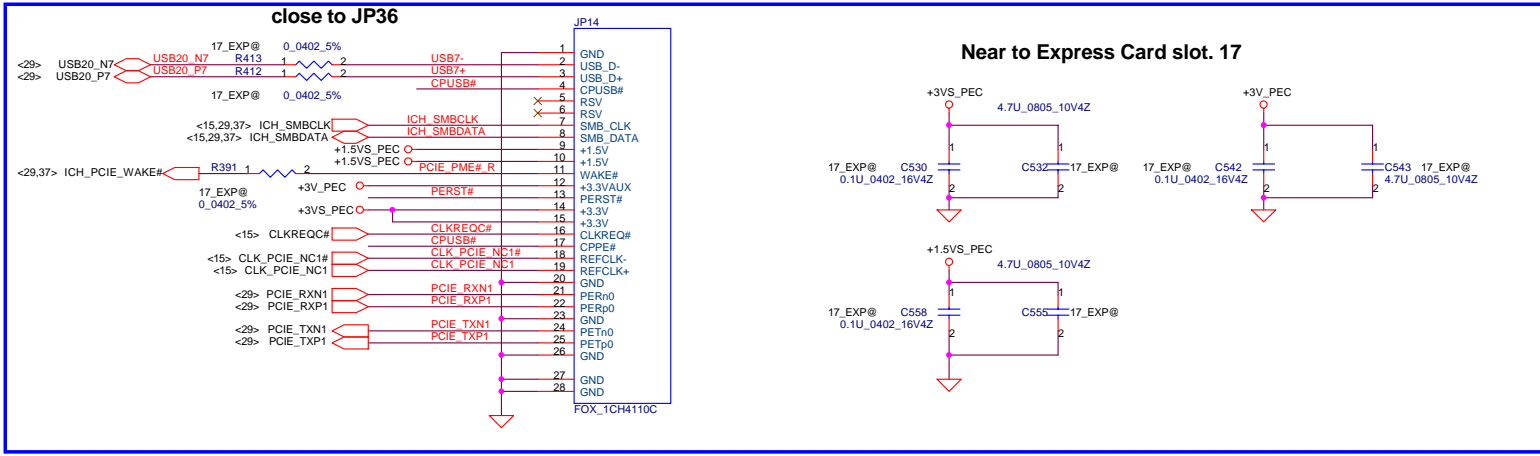
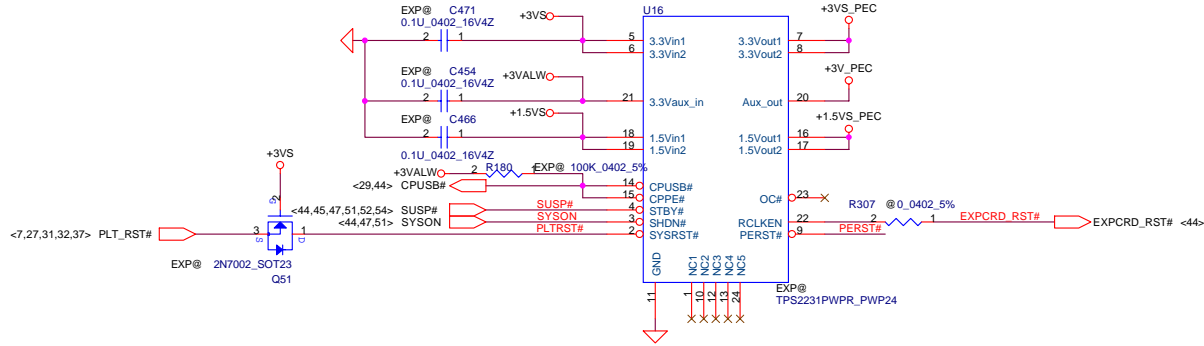
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	HDD & CDROM	
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				Custom	LA-2841
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CardBus Power Switch



Security Classification	Compal Secret Data		Title	PCI7412	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Size	Document Number
				Custom	LA-2841
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			Sheet	33	of 60
			Rev	1.0	

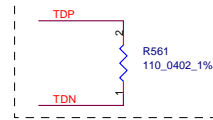
Express Card Power Switch



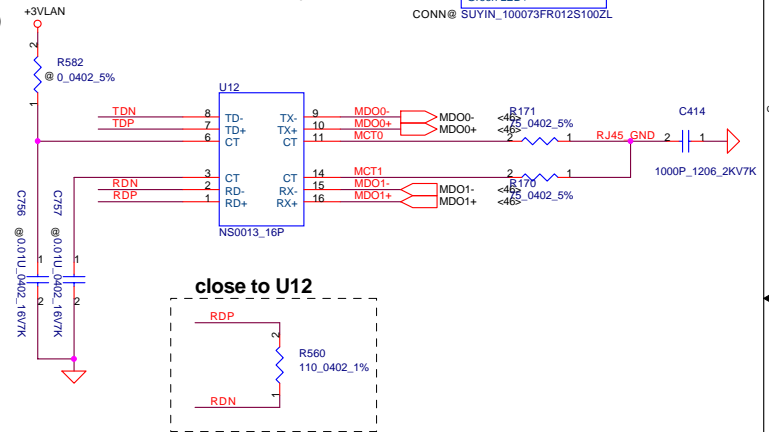
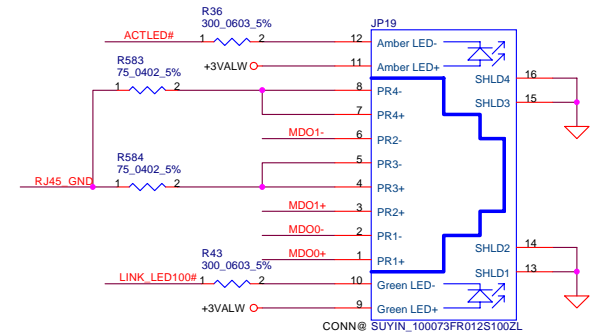
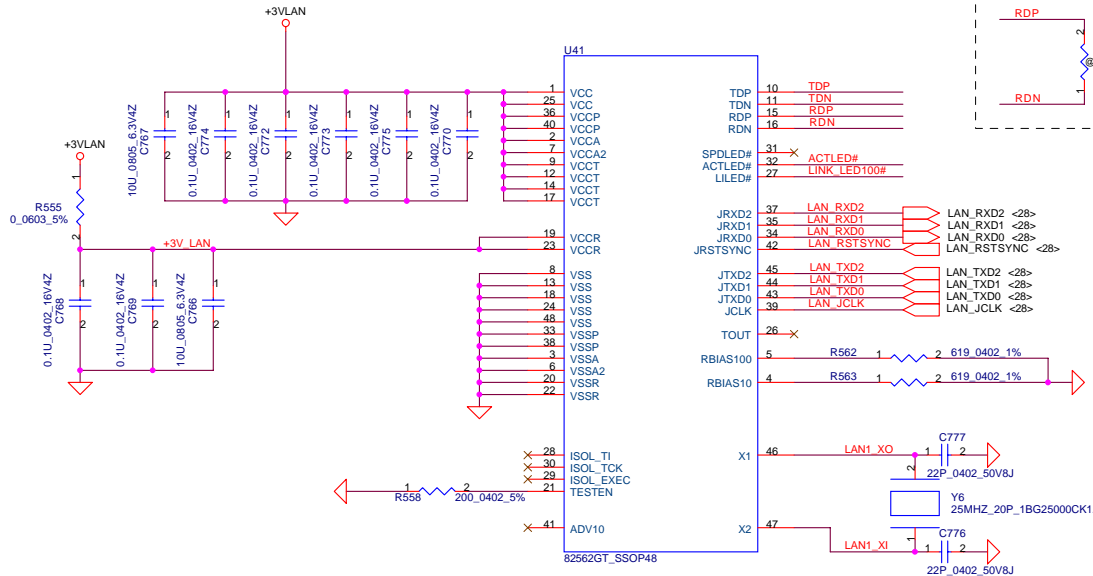
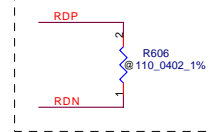
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Express Card	
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Date:	Thursday, December 15, 2005	Sheet	34	of	60



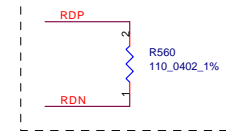
close to U41chip(Intel rule)



close to U41chip(Intel rule)



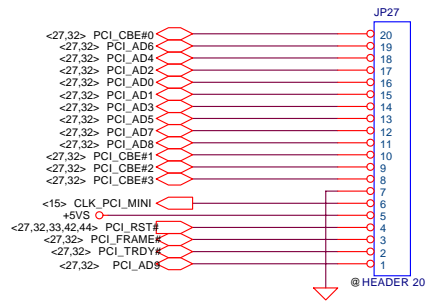
close to U12



Security Classification		Compal Secret Data	
Issued Date	2005/03/10	Deciphered Date	2006/03/10
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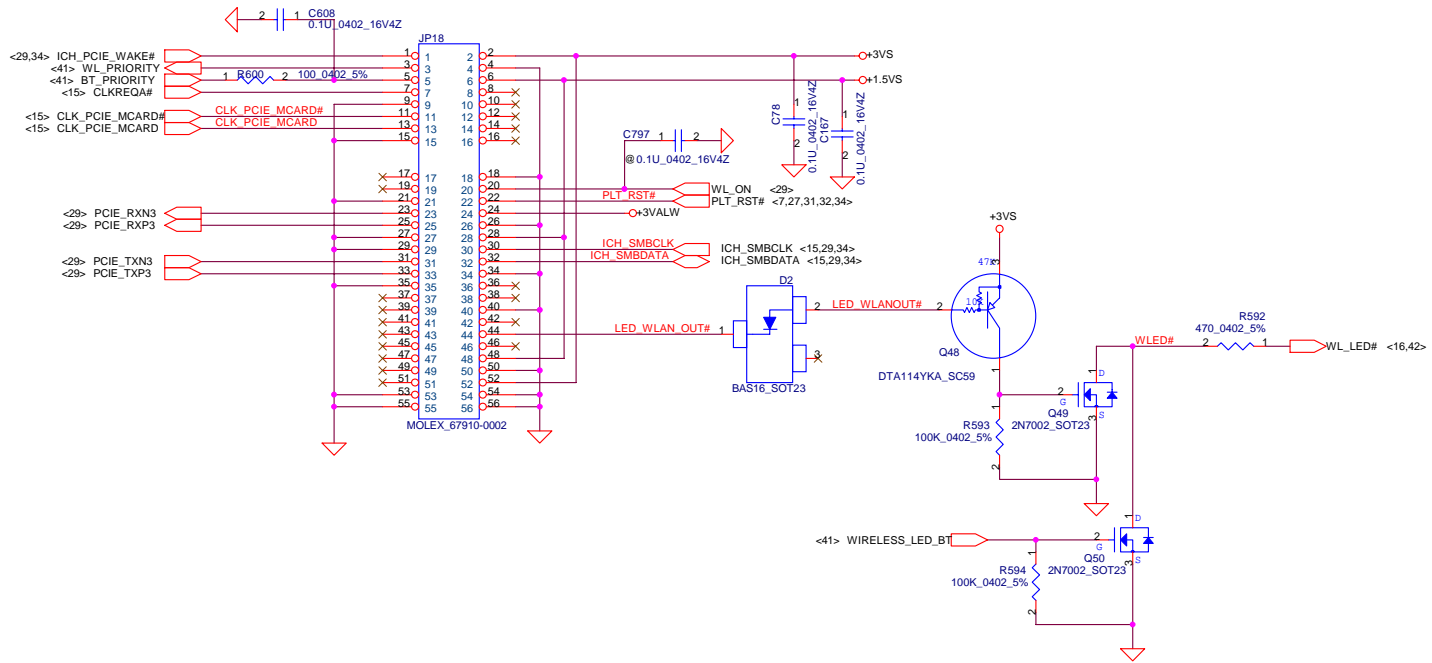
Compal Electronics, Inc.			
Title 82562EZ LAN			
Size	Document Number	Rev	
Custom	LA-2841	1.0	
Date:	Thursday, December 15, 2005	Sheet	35 of 60

Port 80 Debug Card Connector

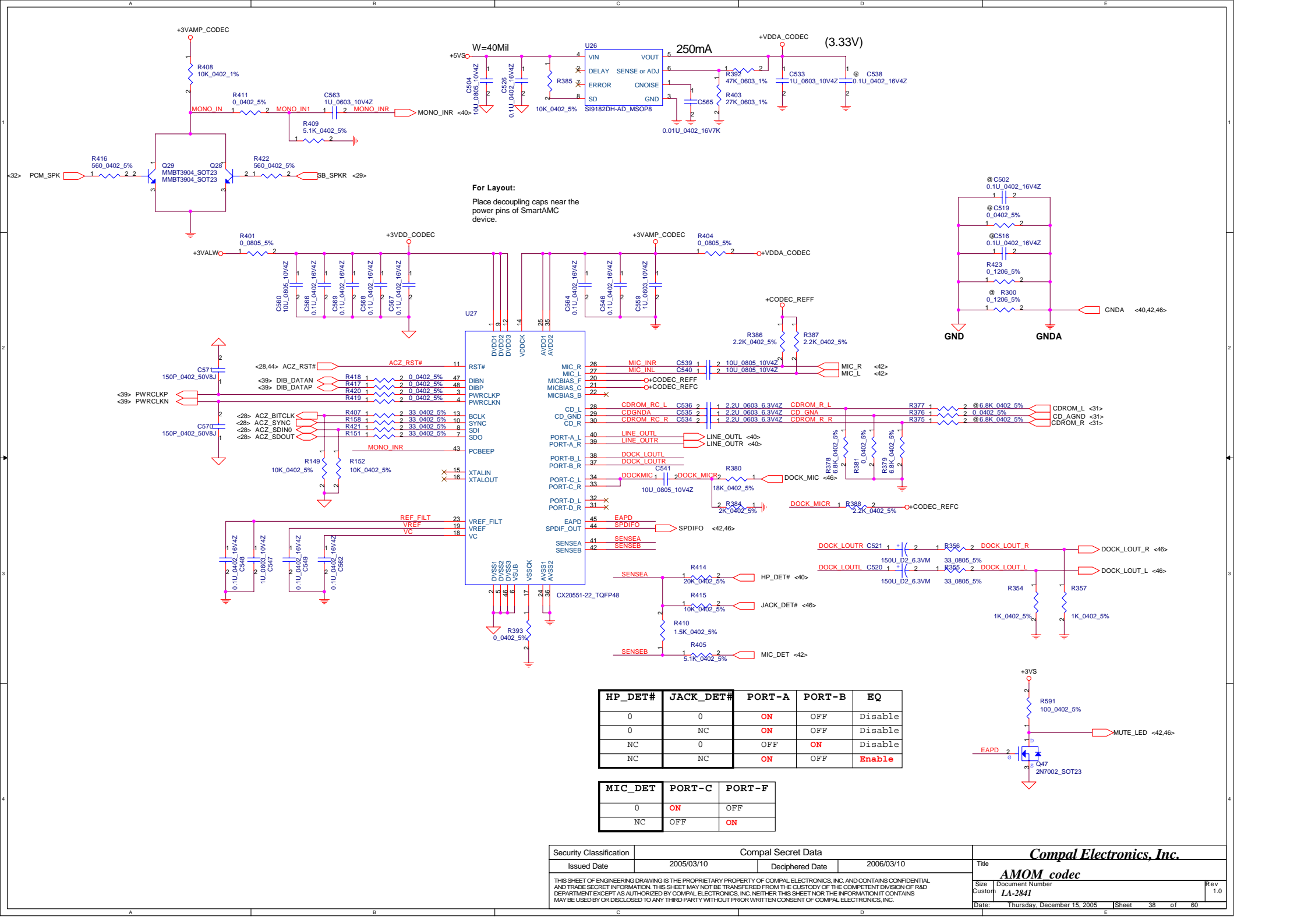


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Debug port	
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				Date:	Thursday, December 15, 2005
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Mini-Express Card(Slot 1-WLAN)



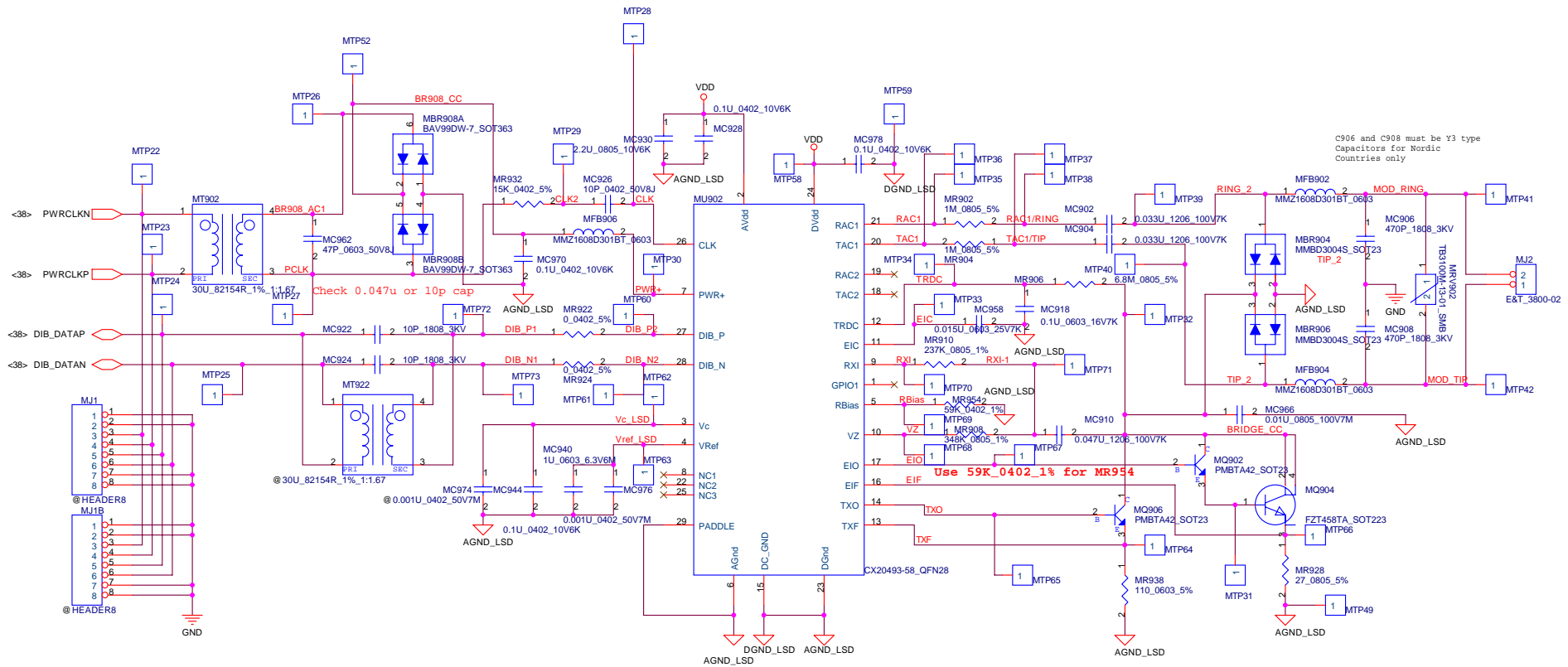
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Mini Card
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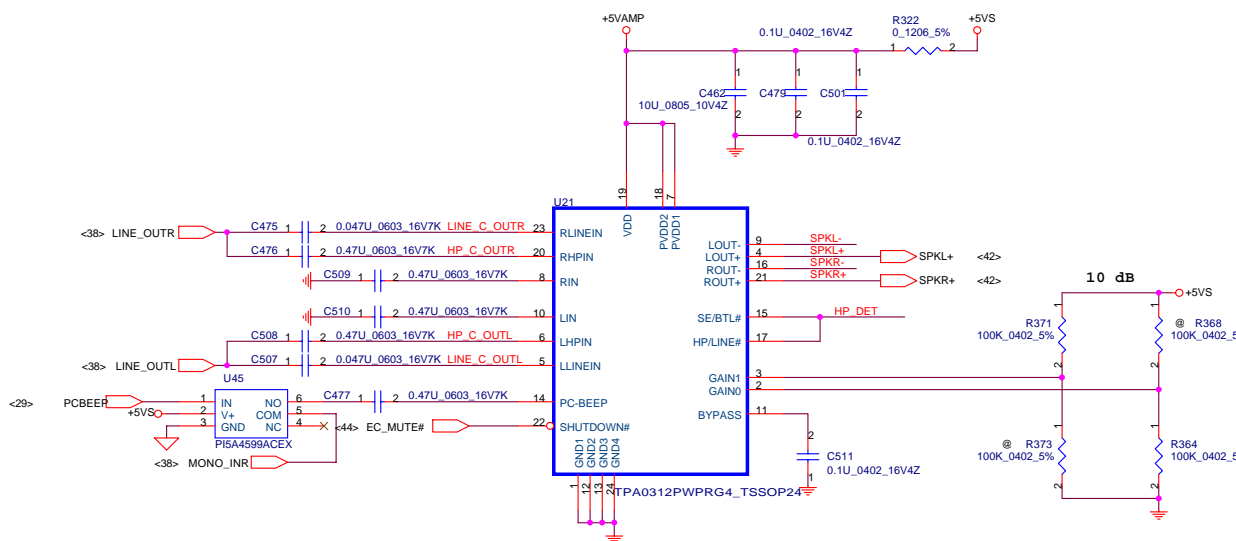
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

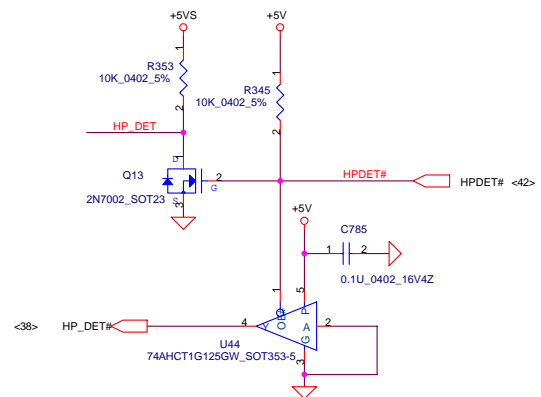
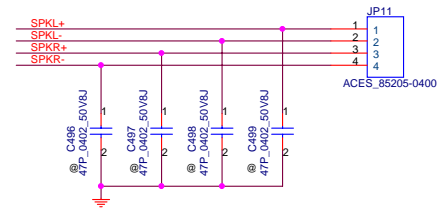


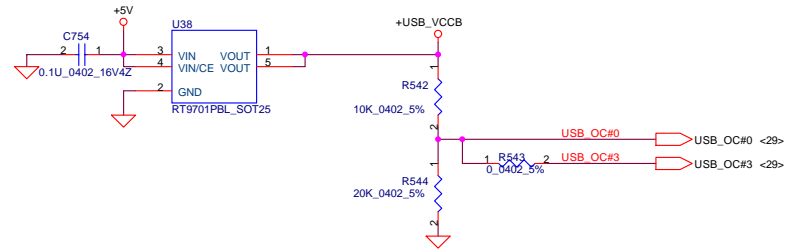
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				Rev: 1.0
				Sheet 39 of 60



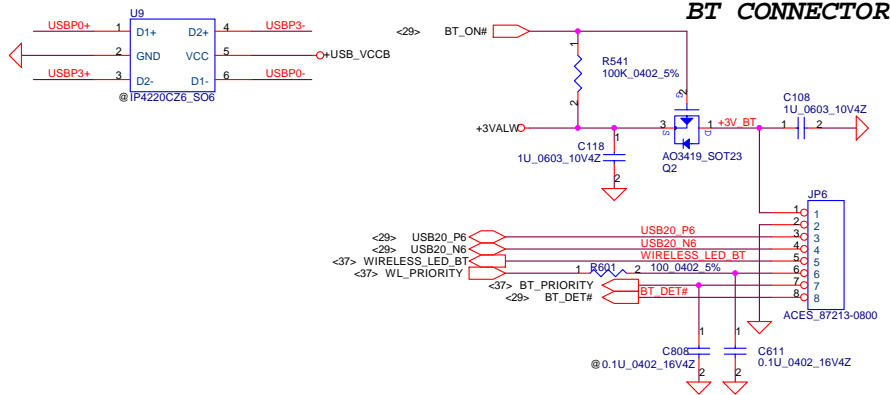
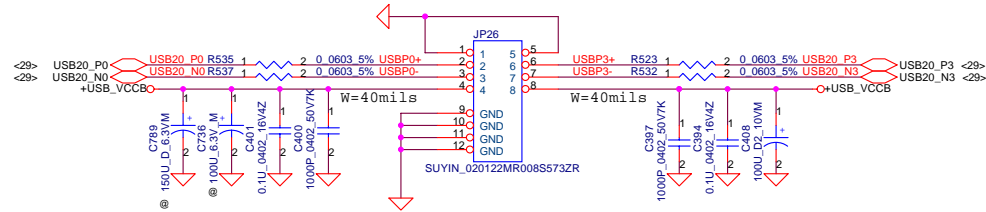
HEADPHONE OUT/LINE OUT

Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av (inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



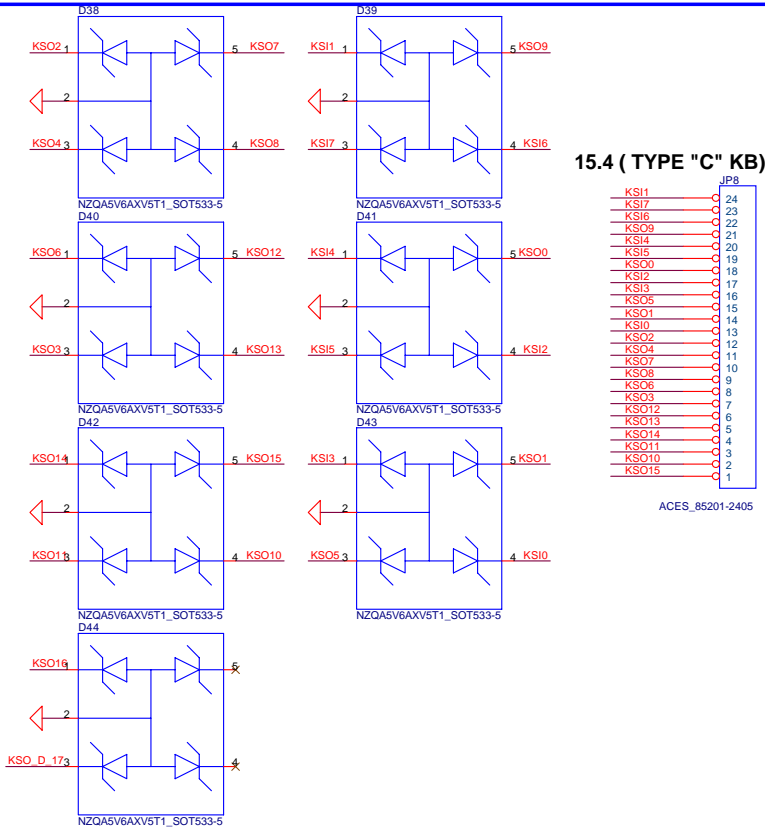
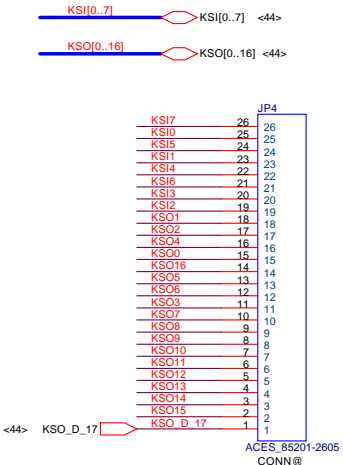


USB CONNECTOR (Left side)



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				Rev 1.0

INT_KBD CONN.(TYPE "D" KB)

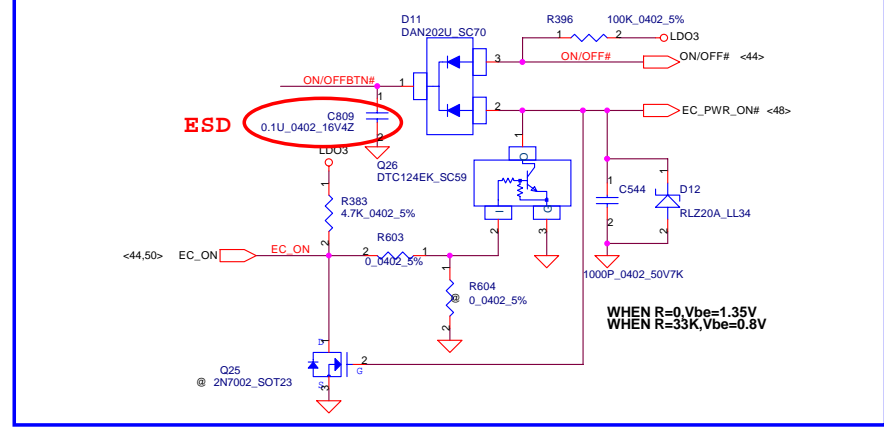


15.4 (TYPE "C" KB)

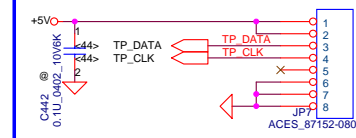
- KS11 23
- KS17 24
- KS16 23
- KSO9 21
- KS14 20
- KSO0 19
- KS12 17
- KS13 16
- KS03 15
- KSO1 14
- KSO2 12
- KS04 13
- KSO7 11
- KSO8 10
- KSO6 8
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- KS10 4
- KSO15 3
- KSO14 2
- KSO11 1

ACES_85201-2405

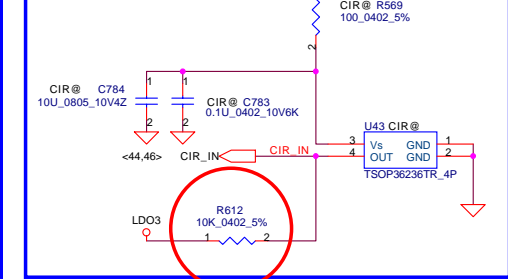
Power BTN



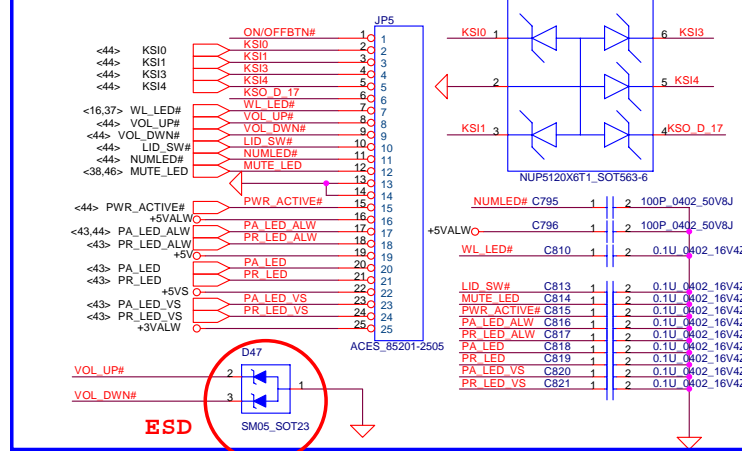
TP to MB CONN(15.4)



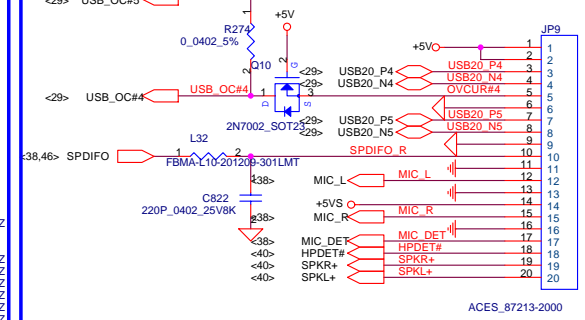
Consumer IR



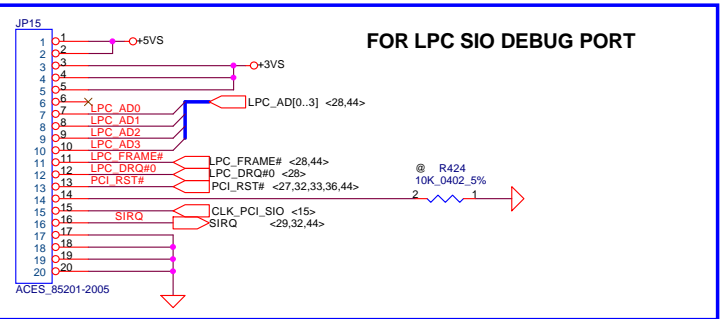
Switch board conn



Audio board conn



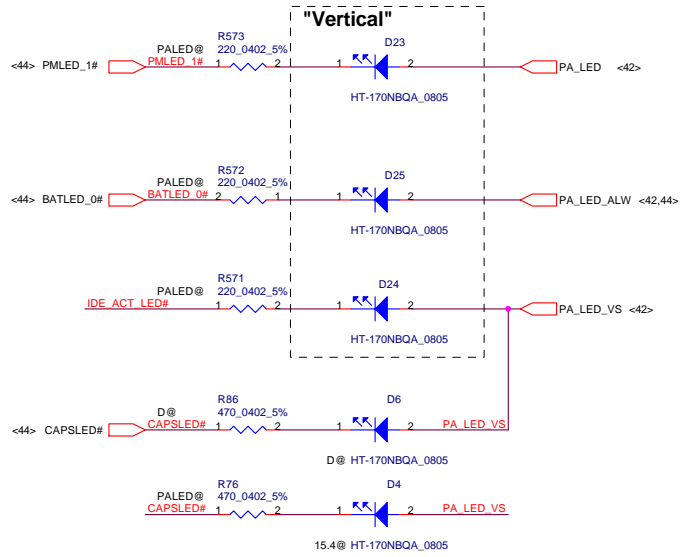
FOR LPC SIO DEBUG PORT



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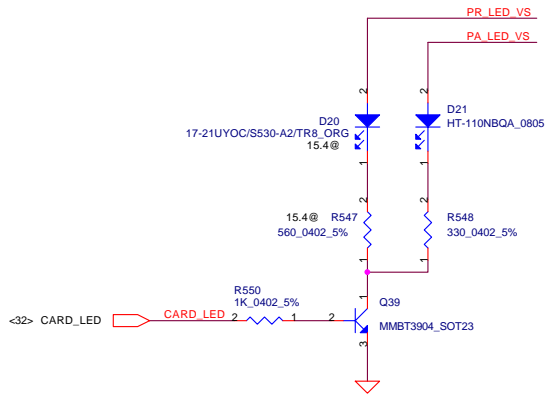
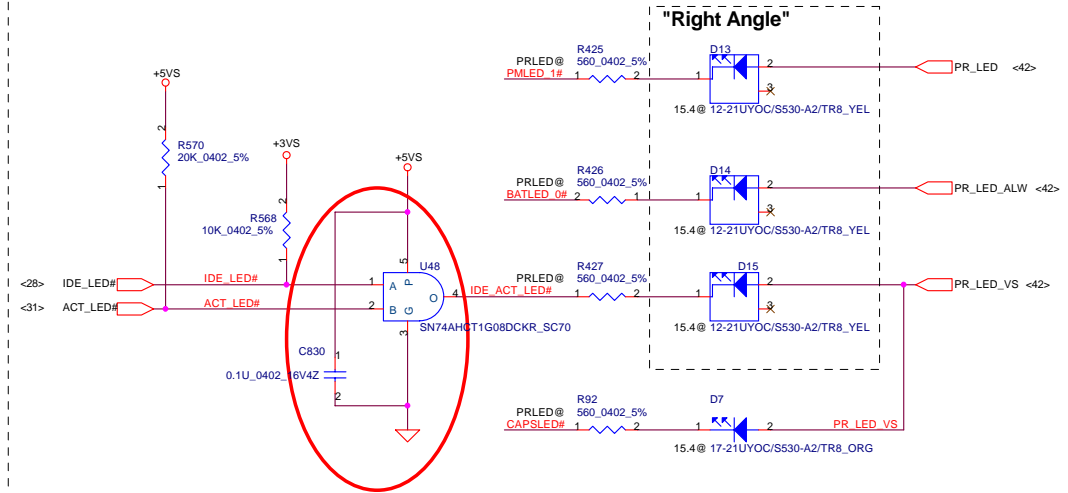
For PA

FOR POWER BUTTON BACKLIGHT SYSTEM POWER





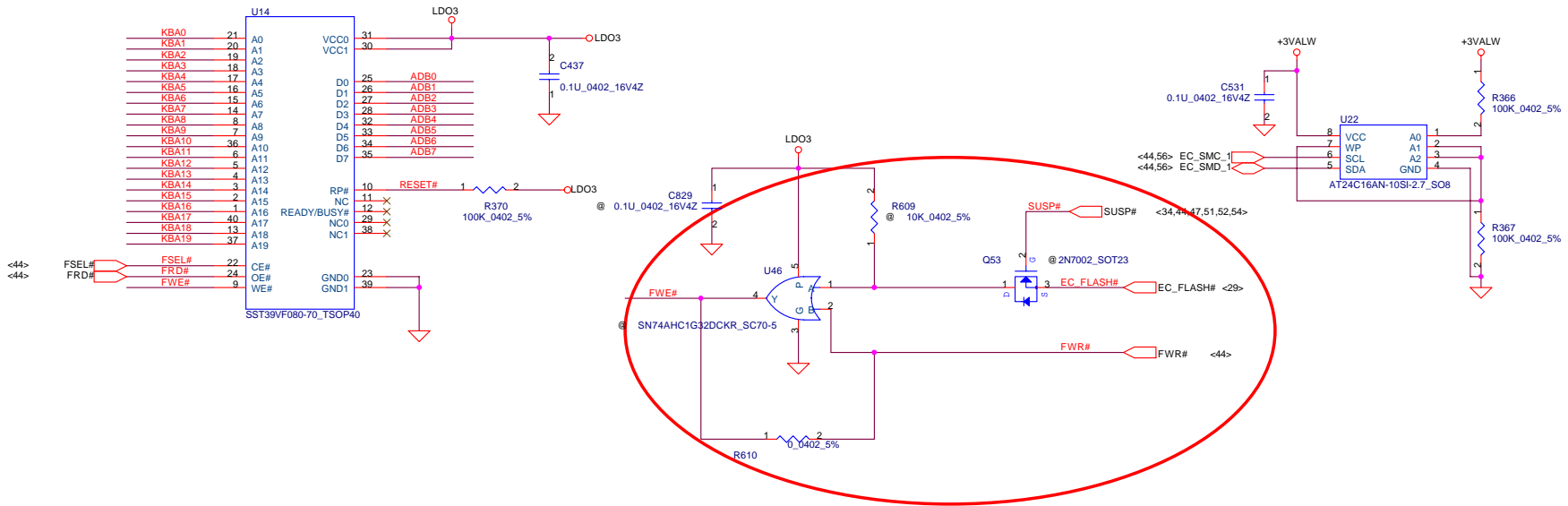
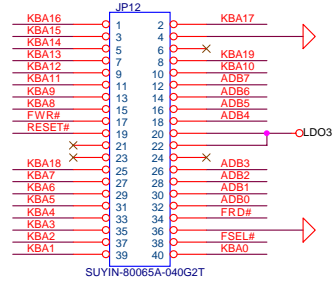
For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER

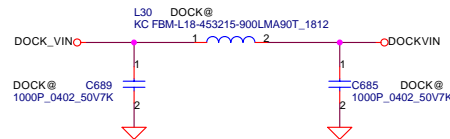


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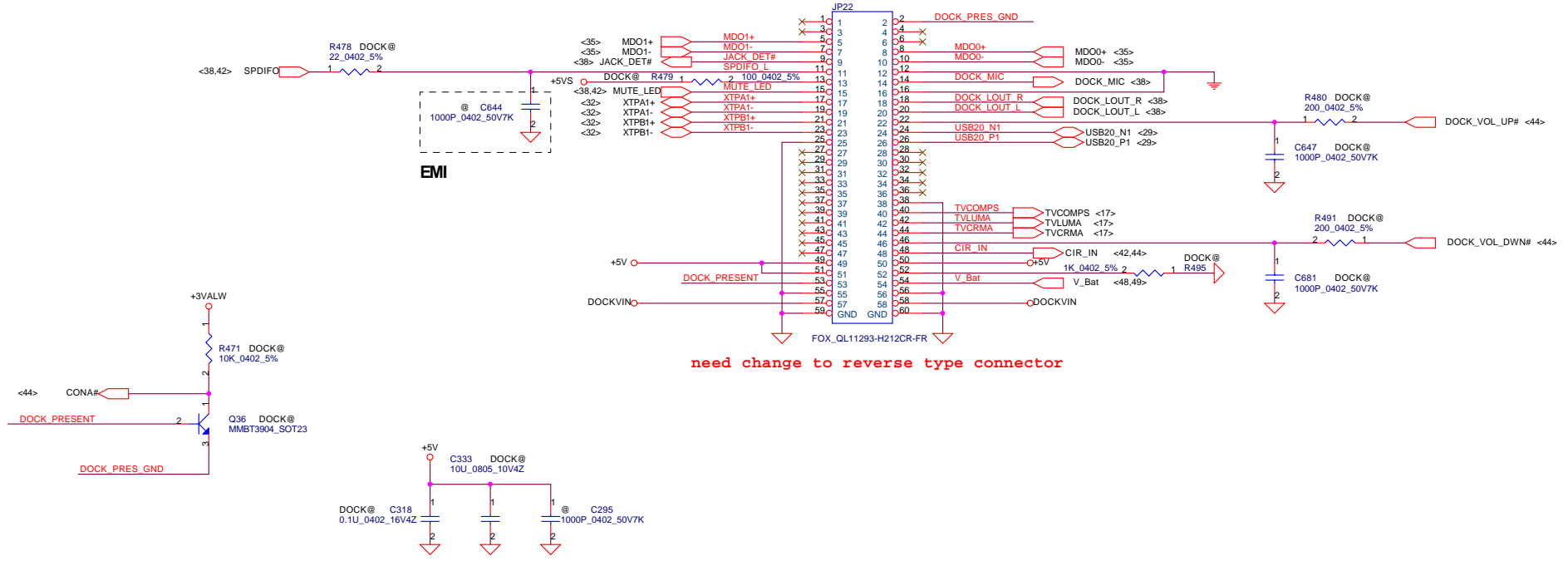
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 <44> KBA[0..19]  KBA[0..19]



Security Classification		Compal Secret Data		Compal Electronics, Inc. BIOS & EC I/O Port	
Issued Date	2005/03/10	Deciphered Date	2006/03/10		
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				Date: Thursday, December 15, 2005	Sheet 45 of 60
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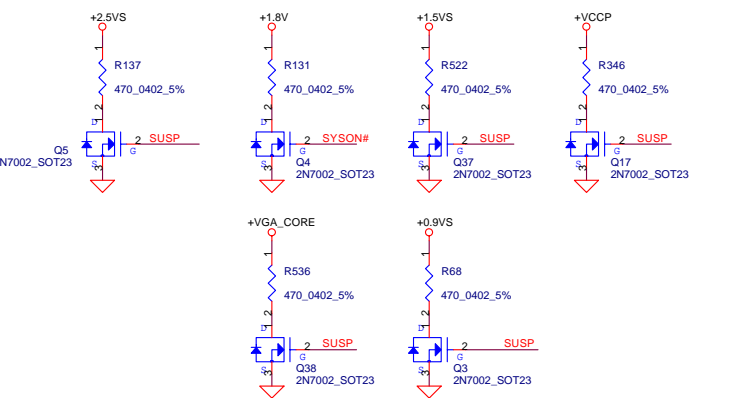
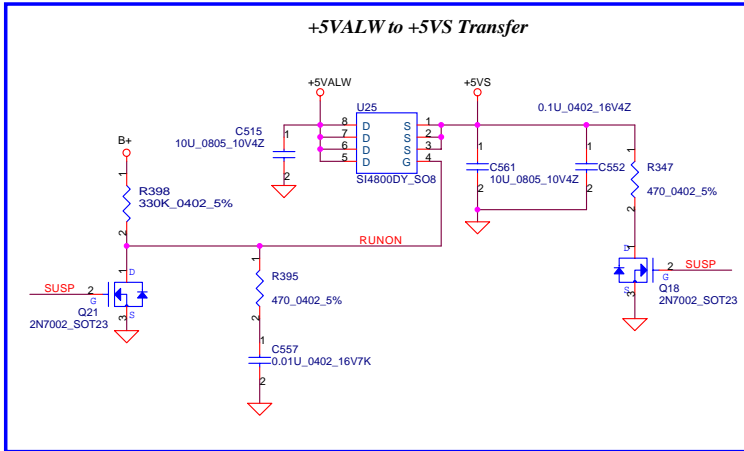
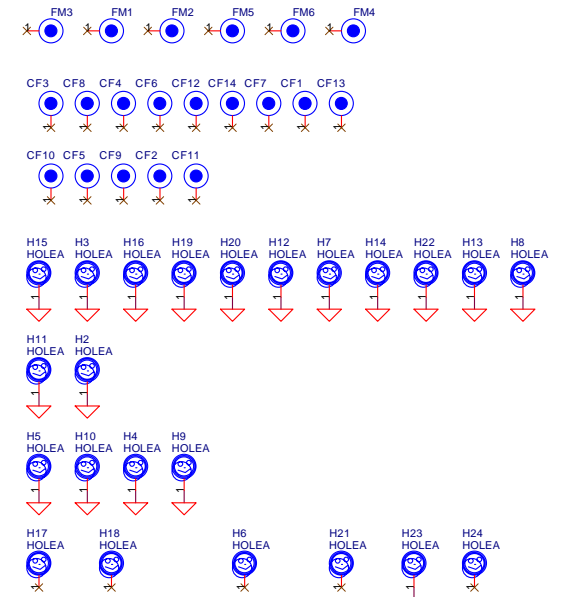
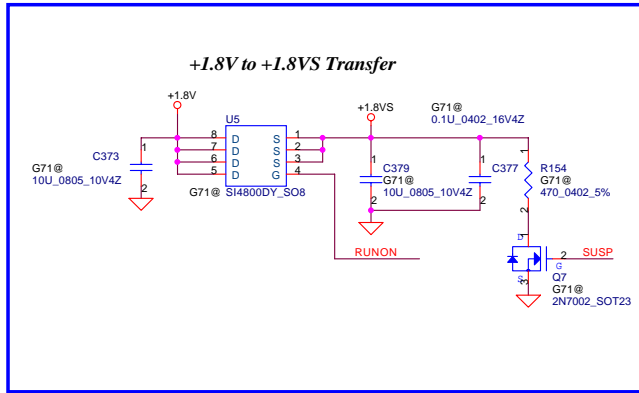
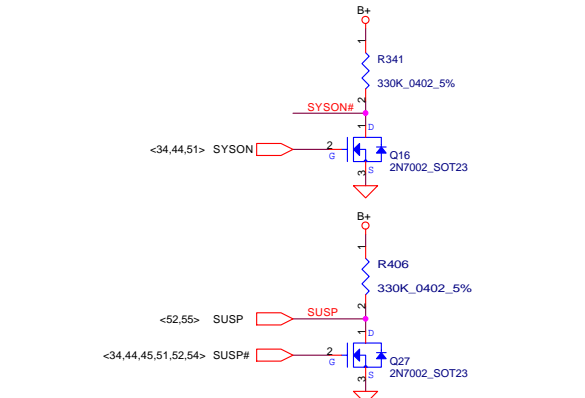
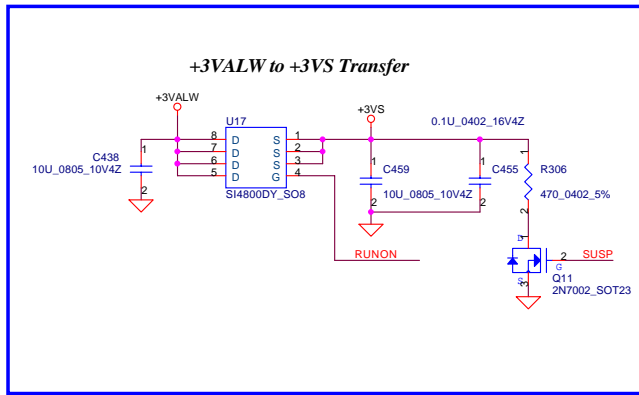
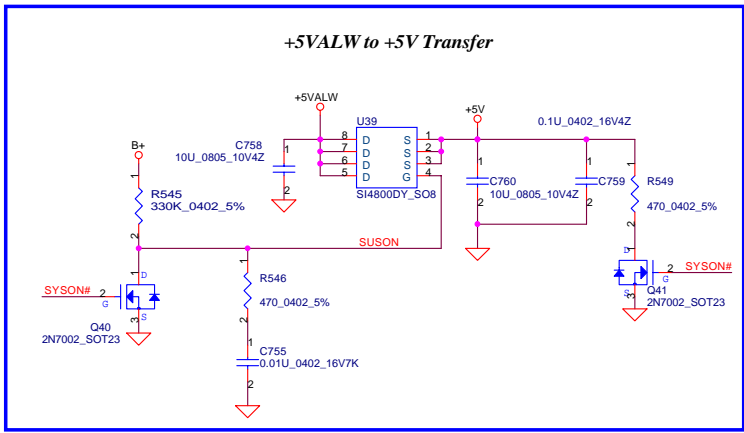


Tampa 2



need change to reverse type connector

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Issued Date	2005/03/10	Deciphered Date	2006/03/10	DC/DC Circuit
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Vin Detector : Titan

18.234	17.841	17.449
17.597	17.210	16.813

Vin Detector : Altima

14.698	14.285	13.879
13.818	13.411	13.000

**Titan: PR5= 22K; PR6= 19.6K
Altima: PR5= 47K; PR6= 27K**

**Titan: PR21= 200K
Altima: PR21= 300K**

ACIN: Titan

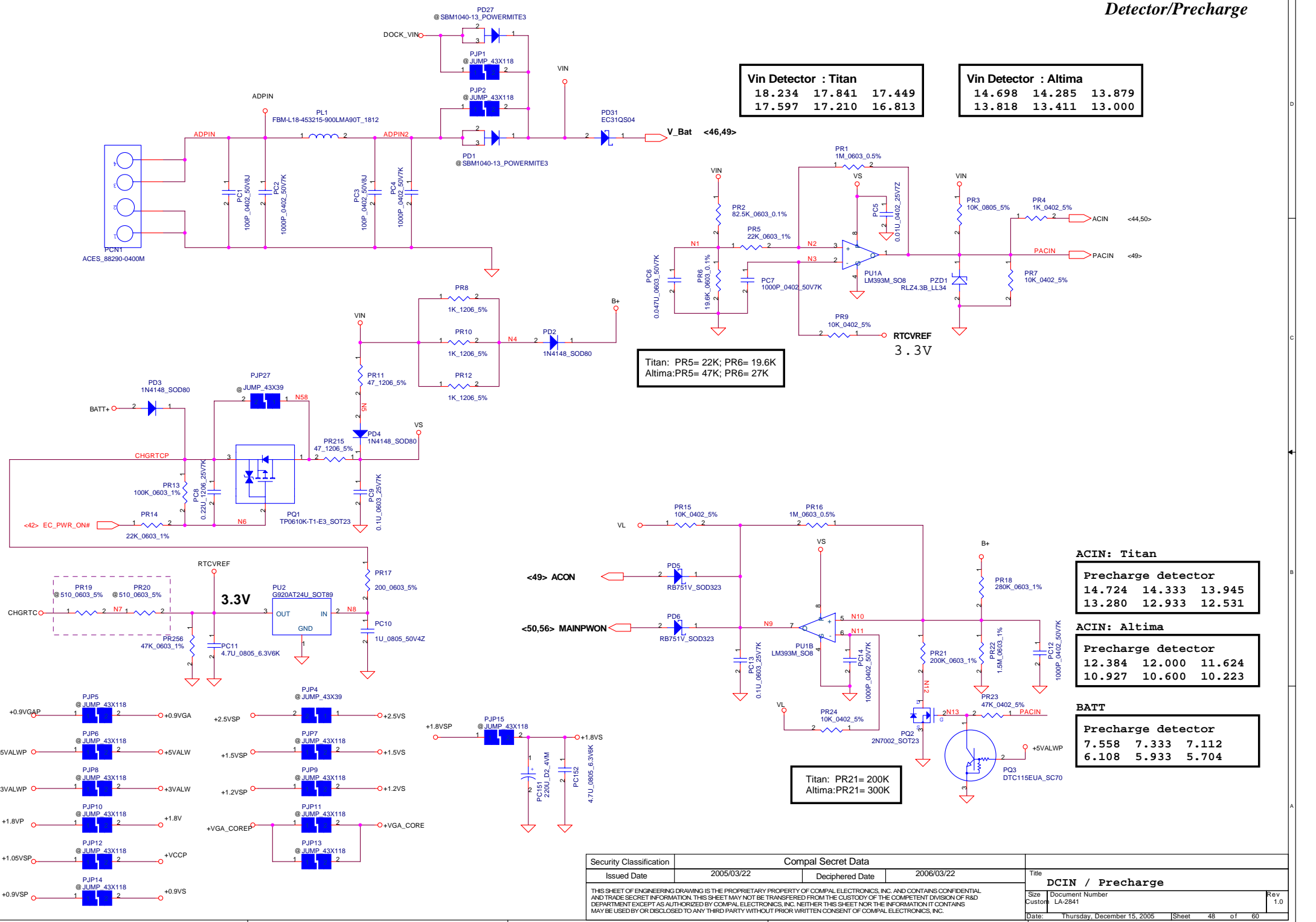
Precharge detector	14.724	14.333	13.945
	12.280	12.933	12.531

ACIN: Altima

Precharge detector	12.384	12.000	11.624
	10.927	10.600	10.223

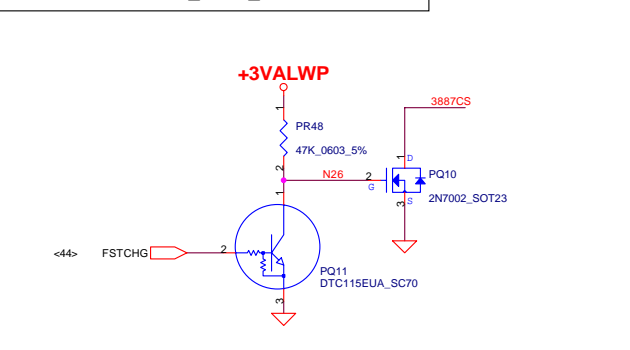
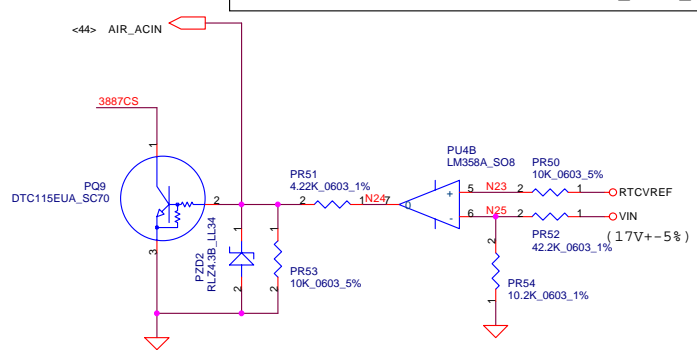
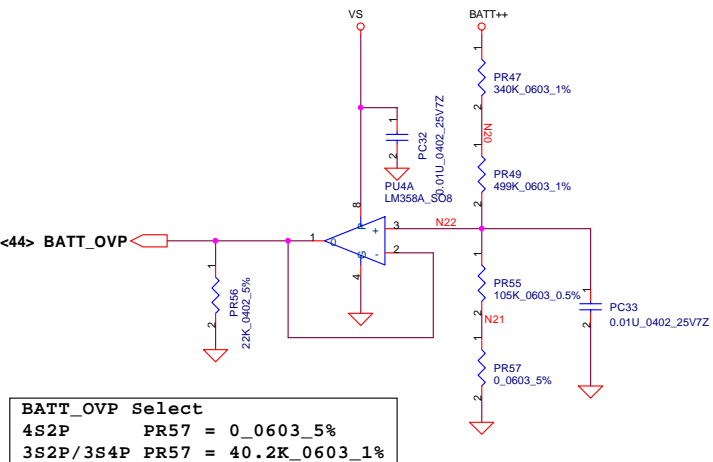
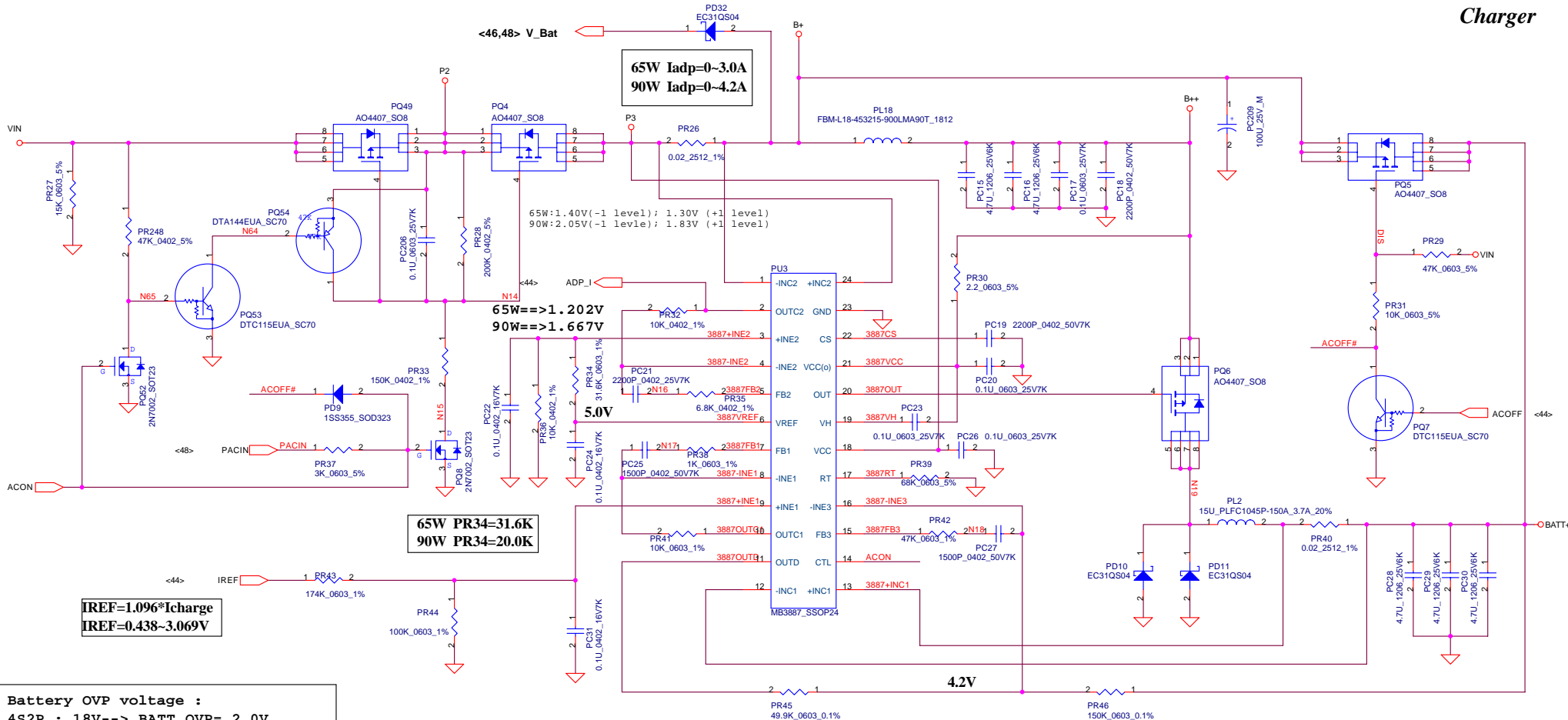
BATT

Precharge detector	7.558	7.333	7.112
	6.108	5.933	5.704



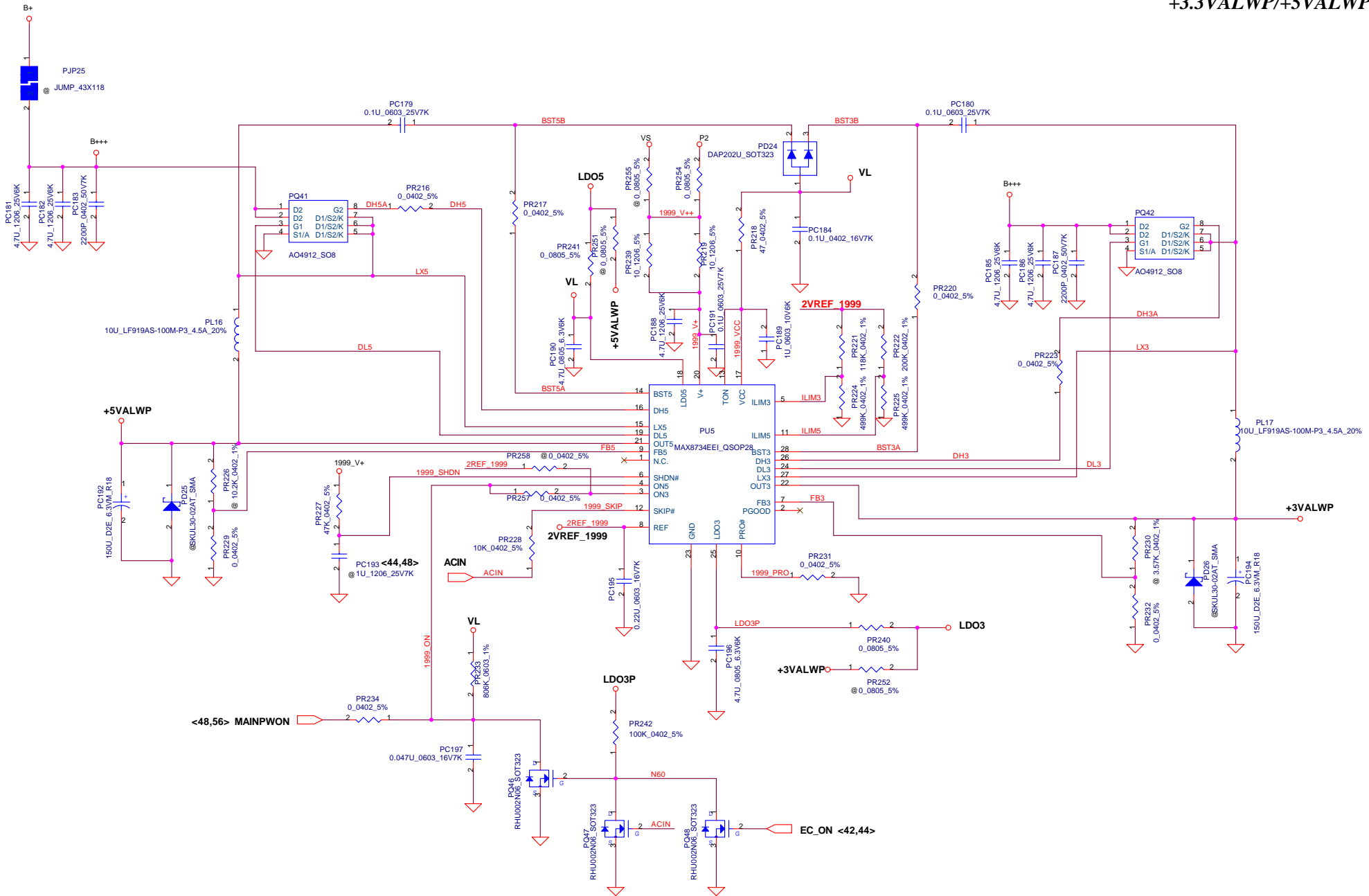
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Charger



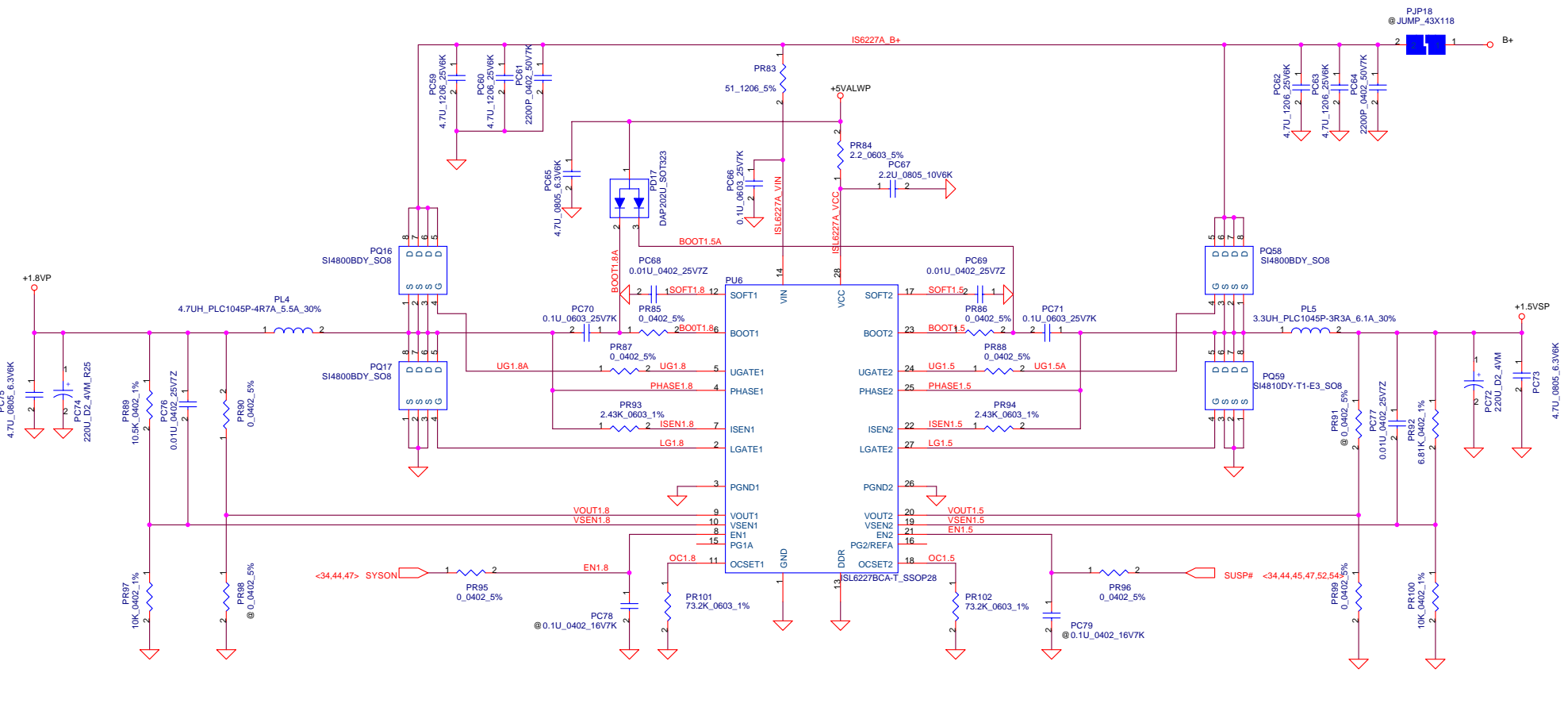
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+3.3VALWP/+5VALWP

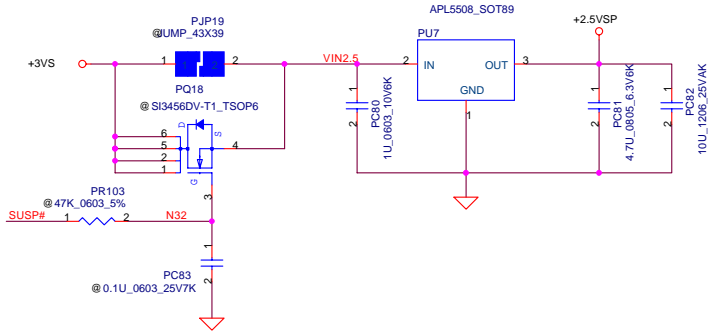


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Size	Document Number	Rev		
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+1.8VP/+1.5VALWP/+2.5VS

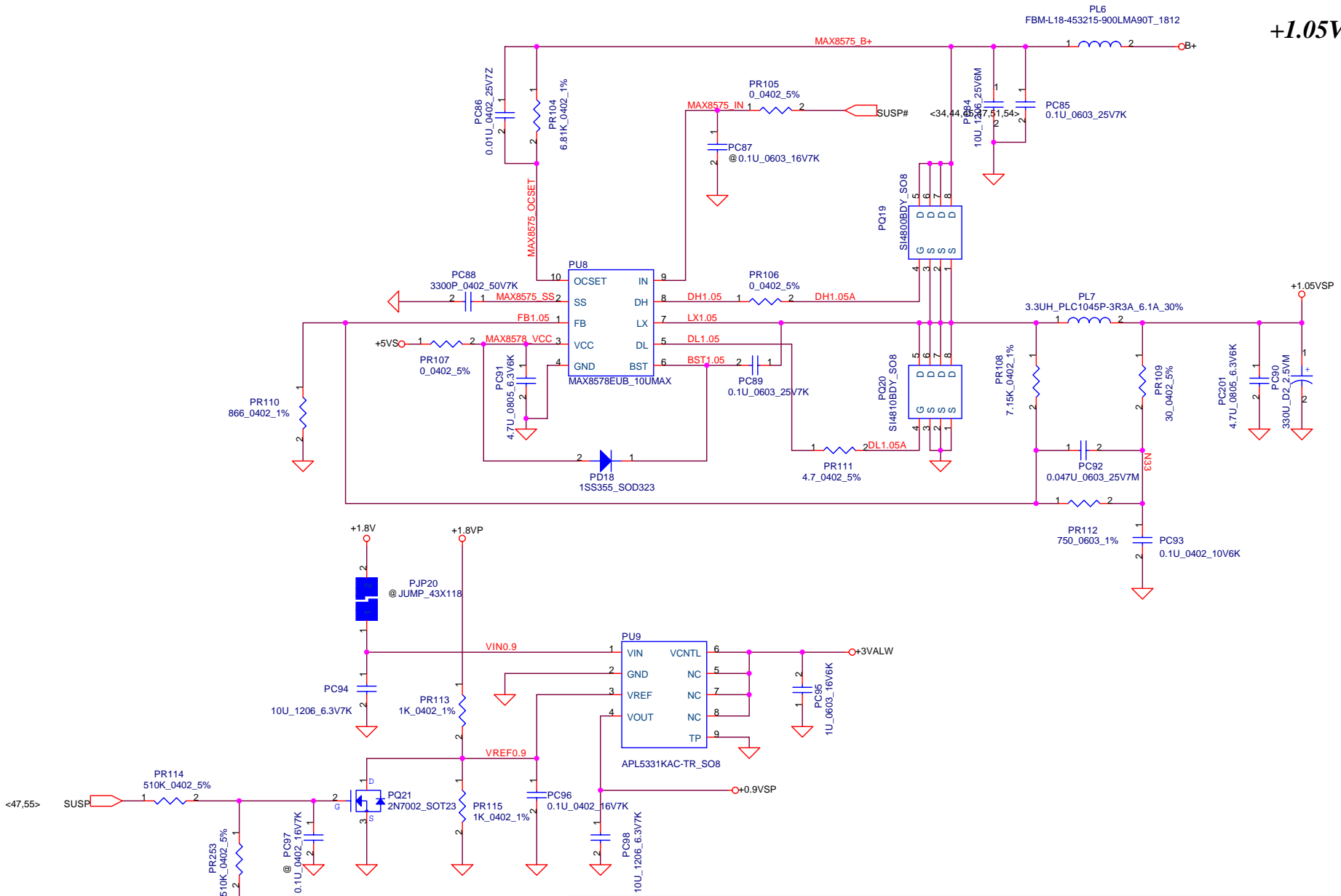


(400mA, 40mils, Via NO. = 1)

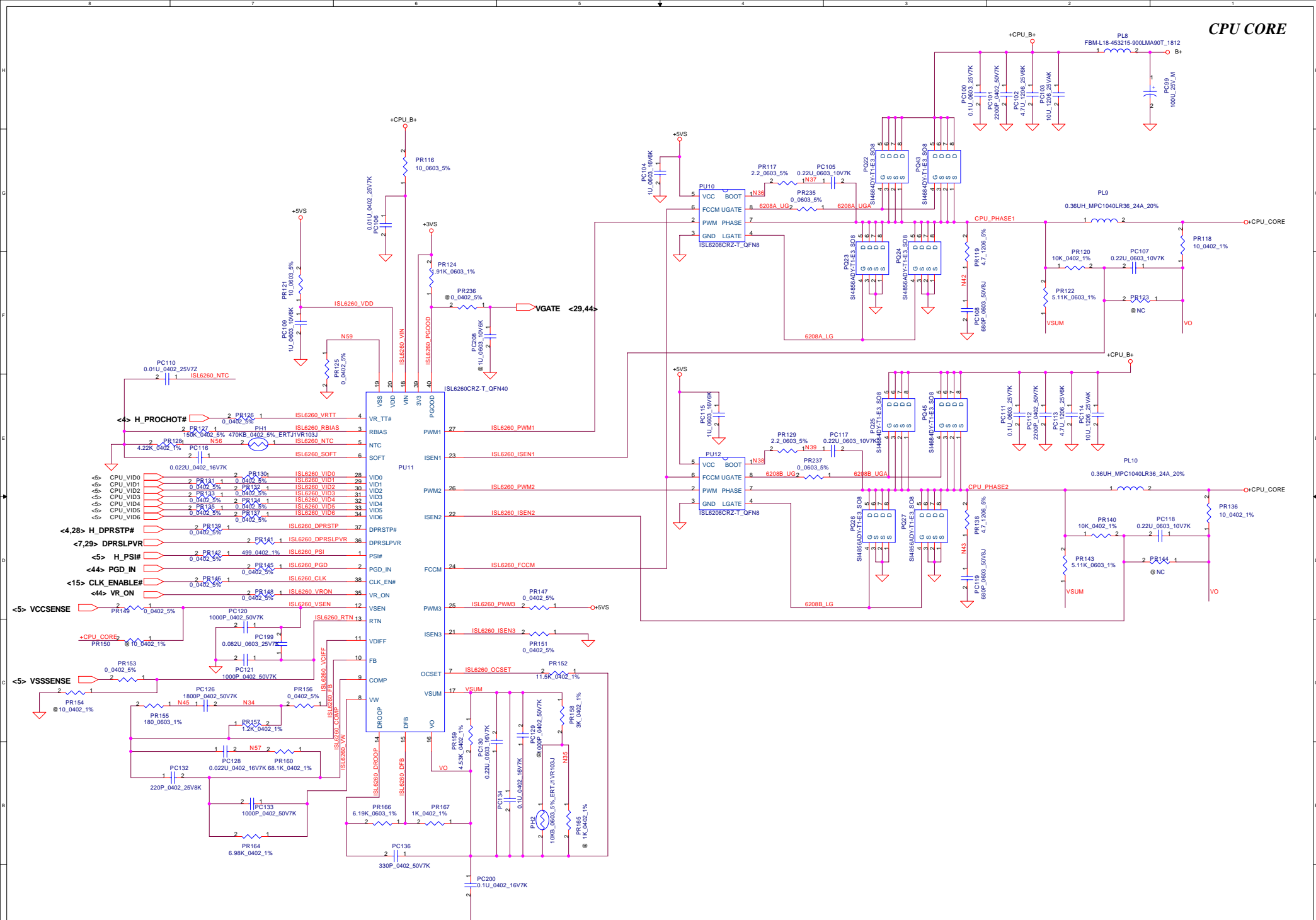


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Date:	Thursday, December 15, 2005	Sheet	51	of 60

+1.05V_VCCPP/+0.9VSP

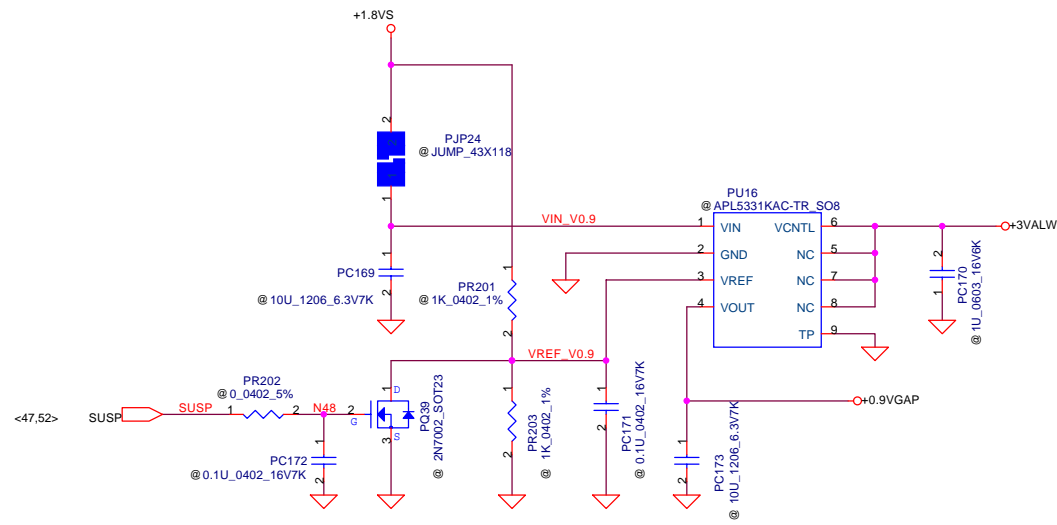
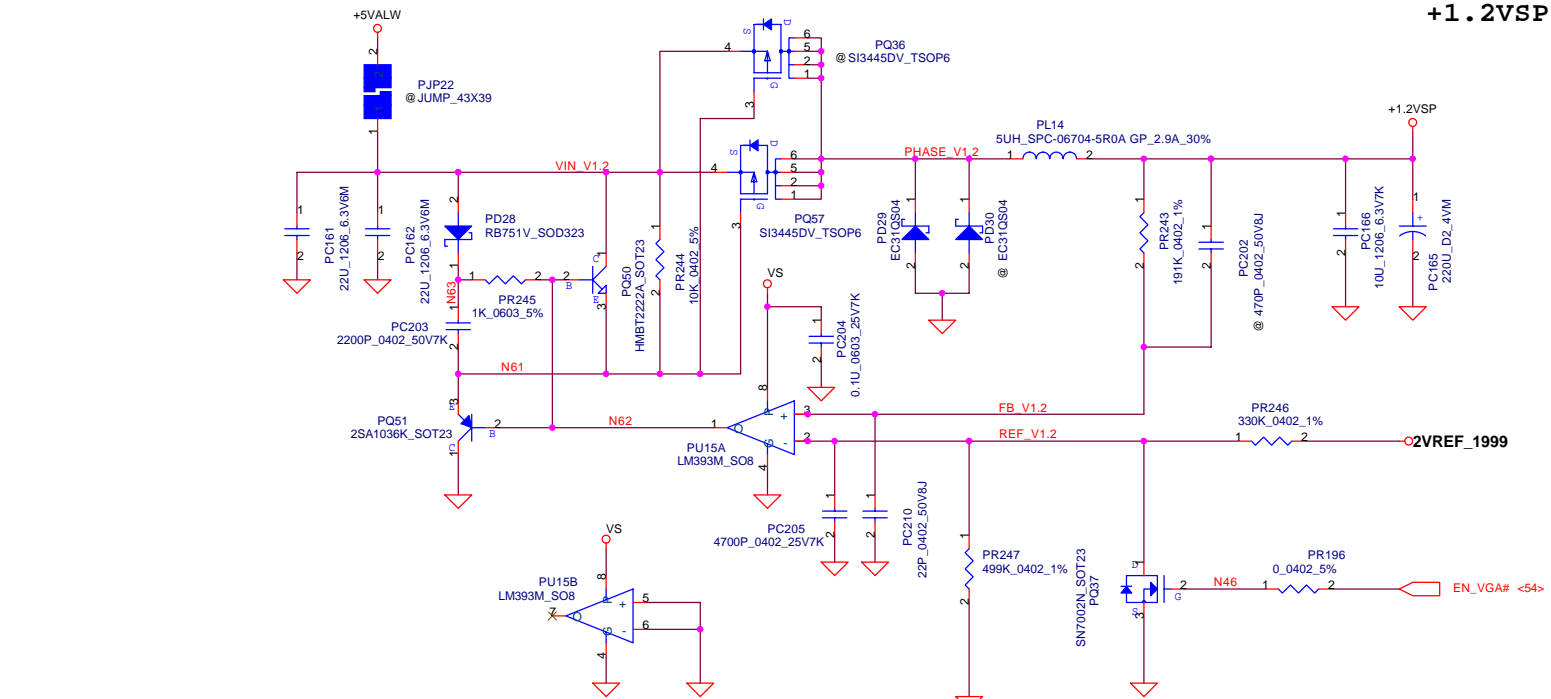


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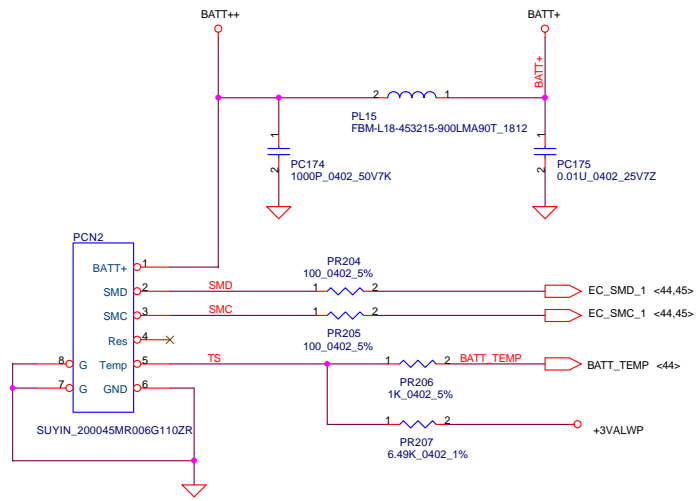
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+1.2VSP/+0.9VSP



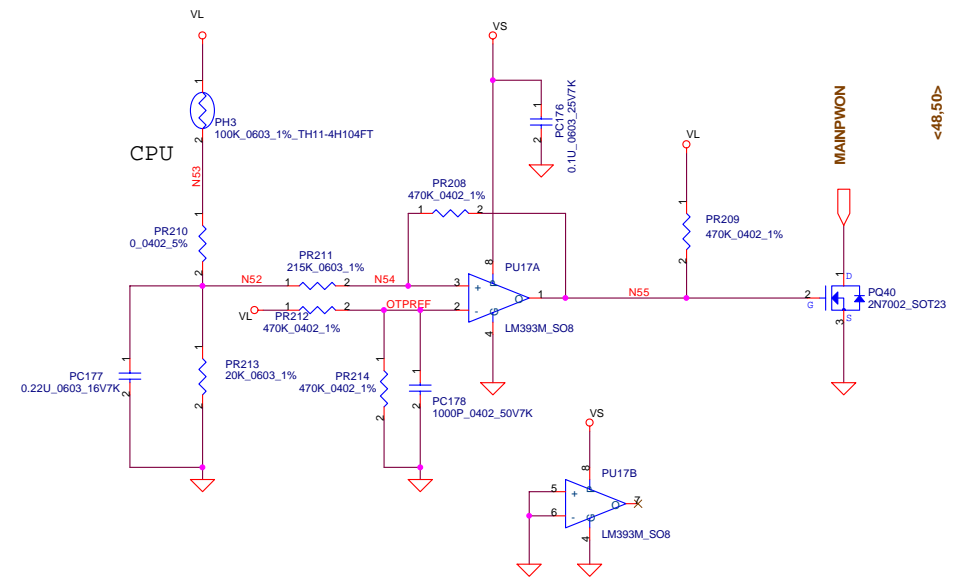
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Battery Connect/OTP



PJPB1 battery connector
SMART
Battery:
1.BATT+
2.SMBD
3.SMBC
4.Res
5.Temp
6.GND

PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



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Version change list (P.I.R. List)

Item	Modify list	Reason for change	Rev.	PG#	Modify by
1	Add R579 and R580 for EC PA/PR detec	EC team request	Rev0.2	P44	6/6 '05
2	BOM del C591 220U_D2 for +VCCP bypass capacitance	Cost down	Rev0.2	P6	6/6 '05
3	U44 pin5 change from +5VAMP to +5V	Design modify	Rev0.2	P40	6/6 '05
4	U44 pin3 change from GMDA to GND	Design modify	Rev0.2	P40	6/6 '05
5	JF21 50pin contact to U31_F25pin	support system memory throttling	Rev0.2	P13	6/6 '05
6	JF24 50pin contact to U31_H26pin	support system memory throttling	Rev0.2	P14	6/6 '05
7	Add D26	Add RTC Battery life	Rev0.2	P28	6/6 '05
8	BOM del R51	Change NB strap pin CFG9 to Normal Operation	Rev0.2	P11	6/6 '05
9	Change R562 from 649K_0402 to 649_0402_1%	BOM error fix LAN can't link	Rev0.2	P35	6/6 '05
10	Change R558 from 3.3K_0402 to 200_0402_5%	BOM error fix LAN can't link	Rev0.2	P35	6/6 '05
11	U24 contact to CPUSB#	Reserve new card detect input	Rev0.2	P44	6/6 '05
12	BOM del R307	no need EC control new card reset	Rev0.2	P44	6/6 '05
13	Add R582 @0_0402	Reserve	Rev0.2	P35	6/6 '05
14	Cancel U12 pin3 contact to +3VLAN	Design modify for LAN function fix LAN can't link	Rev0.2	P35	6/6 '05
15	IFPAB_PLLVDD_PLLVDD_VID_PLLVDD change from 3.3V to 2.5V	G72 G73 power modify	Rev0.2	P20	6/6 '05
16	PEX_CFG 0-2 change from 100 to 001	Overridden CFG modify	Rev0.2	P26	6/6 '05
17	Add JF34 for mini-PCIe Card	ME update	Rev0.2	P37	6/6 '05
18	Del BOM R359,R349,R361,D9,D10,Q23	For TI 7412 modify request	Rev0.2	P32	6/7 '05
19	Change MSBS_SDCMD_SMWE_FIXED# to MSBS_SDCMD_SMWE#	For TI 7412 modify request	Rev0.2	P32	6/7 '05
20	Change SDCLK_SMRE_FIXED# to SDCLK_SMRE#	For TI 7412 modify request	Rev0.2	P32	6/7 '05
21	Change SDWP#_SMCE_FIXED# to SDWP#_SMCE#	For TI 7412 modify request	Rev0.2	P32	6/7 '05
22	Change SM_RB_FIXED# to SM_RB#	For TI 7412 modify request	Rev0.2	P32	6/7 '05
23	Change R554,R556,R557,R559 from 10K to 2.2K	For TI 7412 modify request	Rev0.2	P32	6/7 '05
24	Del R369,Q20,Q9,C446,Jp29,JOPEN1,JOPEN2	Cancel TV tuner function	Rev0.2	P41	6/7 '05
25	Change LINK_LED100# contact to U41 pin27	Customer request for LAN link LED state	Rev0.2	P35	6/8 '05
26	Add R583,R584 75 ohm contact to JP19 and RJ45_GND	LAN modify	Rev0.2	P35	6/8 '05
27	Swap DQSA0-7/DQSA#0-7 and DQSC0-7/DQSC#0-7	Schematic error modify	Rev0.2	P19	6/8 '05
28	Add R585 LID_SW# 10K pull-high reserve	LID_SW# floating	Rev0.2	P44	6/13 '05
29	U6 pin D23 SLP_S4# contact to U24 pin35	EC need detect SLP_S4# for S4 state	Rev0.2	P44	6/13 '05
30	BOM update add R388	D0CK_MFCR need pull-high to +CODEC_REFC	Rev0.2	P38	6/13 '05
31	Change WL_PRIORITY contact to JP18 pin3 and BT_PRIORITY contact to JP18 pin5	pin define swap	Rev0.2	P37	6/14 '05
32	BOM add R587,R588,R589,R590 0 ohm	for NV72 CLK swap pin rework	Rev0.2	P19	6/14 '05
33	JF17 footprint update	DB1 footprint error, fix can't TV-out	Rev0.2	P17	6/14 '05
34	Del R587,R588,R589,R590 0 ohm	for NV72 chipset modify	Rev0.3	P19	6/17 '05
35	Add R586,R587	UMA or Discrete PCB detect	Rev0.3	P44	6/27 '05
36	Change R145,R146 from 88.7k to 88.7 ohm	BOM error	Rev0.3	P18	6/28 '05
37	Change C419,C421 form 33F to 22P_0402	improve TV out quality.	Rev0.3	P15	6/28 '05
38	Add R588	TI recommend(it can avoid the small noise form this SPKROUT pin)	Rev0.3	P32	6/30 '05
39	JF26 footprint update	ME change new USB connector	Rev0.3	P41	6/30 '05
40	JF3 footprint update	ME change new CRT connector	Rev0.3	P17	
41	Add R589	Dual layout for 9LP306 and SLG8LP462.	Rev0.3	P15	7/05 '05
42	BOM add C591 220U_D2 for +VCCP bypass capacitance	change 220U location with C595	Rev0.3	P06	7/06 '05
43	BOM del C595 220U_D2 for +VCCP bypass capacitance	For cost down	Rev0.3	P11	7/06 '05
44	U24(EC) pin9I add AC2_RS# input	fix into xp codec out popo noise	Rev0.3	P44	7/06 '05
45	Add C790,C791,C792,C793,C794,C795,C796 I00P_0402	For EMI	Rev0.3	P42	7/06 '05
46	Add R590,Q46	Switch PCBEEP path	Rev0.3	P29,40	7/07 '05
47	Add C797 reserve	For EMI	Rev0.3	P37	7/07 '05
48	Change R94,R141 to @ and change R96,R142 form @ to 120@	For NVMDIA change request	Rev0.3	P19	7/08 '05
49	Change R139,Q6 to @ and change R145 form 87_0402 to 124_0402, R84 from 130_0402 change to 124_0402	For NVMDIA change request	Rev0.3	P18	7/08 '05
50	Add screw h0Id H23, H24	ME drawing modify	Rev0.3	P47	7/08 '05
51	R36 pin1 change contact to ACTLED#,R43 pin1 change contact to LINK_LED100#	change LAN LED state, Amber LED indicates activity, Green LED indicates the link is present	Rev0.3	P35	7/09 '05
52	Add R591 10k_0402 and Q47	fix mute LED power on turn on	Rev0.3	P38	7/11 '05
53	BOM del R383 4.7K pull-high	EC program this pin as push-pull output	Rev0.3	P42	7/13 '05

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Version change list (P.I.R. List)

Item	Modify list	Reason for change	Rev.	PG#	Modify by
54	BOM del R101,C161,R467,R88	nvidia recommend	Rev0.3	P18	7/13 '05
55	BOM del R78,R468,R111,R117,R63,R475,R477	nvidia recommend	Rev0.3	P26	7/13 '05
56	BOM del R108,add R112	nvidia recommend(change to PEK_CFG[2..0]=0x010b)	Rev0.3	P26	7/18 '05
57	BOM add C599	add 220u cap for 1.8V power decoupling	Rev0.4	P11	8/18 '05
58	BOM add R455	add 51_0402 resistor for intel Yonah B0 sightings update	Rev0.4	P04	8/18 '05
59	add Q46,Q49,Q50,R593,R594	modify WLED control circuit for OTS:0I64892 issue	Rev0.4	P37	8/22 '05
60	del D3	modify WLED control circuit for OTS:0I64892 issue	Rev0.4	P41	8/22 '05
61	del R440,R432,Q30	modify WLED control circuit for OTS:0I64892 issue	Rev0.4	P16	8/22 '05
62	add R592	add R592 150 ohm for WLED# current limit	Rev0.4	P37	8/22 '05
63	JP9 Pin 14 contact to +5VS	change SPDIF LED power from +5V to +5VS	Rev0.4	P42	8/22 '05
64	add Q51	prevent TP82231 pin2 +3VALW leakage to +3VS	Rev0.4	P34	8/29 '05
65	JP5 Pin 25 contact to +3VALW	switch board need +3VALW provide lie switch power	Rev0.4	P42	8/23 '05
66	BOM change R554/R557/R556 to 100K, change R559 to 22K	TI 7412 pull-high recommend	Rev0.4	P32	8/23 '05
67	JP3 change new part	change CRT conn from top side to bottom side for DPX request	Rev0.4	P17	8/24 '05
68	del C764,R552,R553, Add D28,change U40 to G993 fan control	Fan control circuit change to G993	Rev0.4	P04	8/24 '05
69	BOM del R47	intel WW31 document update	Rev0.4	P11	8/29 '05
70	add R595/R596/R597/R598/R599	SD card signal add 33 ohm damping resistor	Rev0.4	P32	8/30 '05
71	add R817/R77 10K_0402	NV72 AL chip recommend UTAG_TCK pull-high and UTAG_N pull-down	Rev0.4	P18	8/29 '05
72	del clock generators difference clock 49.9ohm termination	ICS9LP306 clock generators update	Rev0.4	P15	8/29 '05
73	change clock generators difference clock 33ohm damping to 100ohm	ICS9LP306 clock generators update	Rev0.4	P15	8/29 '05
74	change R266 from 475 ohm to 2.4K ohm	ICS9LP306 clock generators update	Rev0.4	P15	8/29 '05
75	add D297/D30/D31/D32/D33/D34/D35/D36	SD card signal add diode for voltage clamp	Rev0.4	P32	8/30 '05
76	move C8/C11/C10/C3/C4/C5/C2/C13/C14/C34/C35/C1 for layout	ME update limit area for CPU	Rev0.4	P06	8/30 '05
77	change R591 from 10K ohm to 100 ohm	fix OTS:I63350 Calgary's mute LED can't display	Rev0.4	P38	8/30 '05
78	JP34 pin50 change contact from PM_EXTT5#1 to PM_EXTT5#0	intel WW31 document update	Rev0.4	P14	8/30 '05
79	U31 pin86 change contact from PM_EXTT5#1 to DPRSLPVR	intel WW31 document update	Rev0.4	P07	8/30 '05
80	D26 pin2 change contact from +3VALW to LD03	add RTC battery life	Rev0.4	P28	8/30 '05
81	BOM change R562 from 649 ohm to 619 ohm and change U12 to new part	LAN performance modify	Rev0.4	P35	8/30 '05
82	add R600 100 ohm and DEL C608 @	HP recommend	Rev0.4	P37	8/30 '05
83	add R601 100 ohm	HP recommend	Rev0.4	P41	8/30 '05
84	Reserve C810-C821 0.1u cap	For EMI	Rev0.4	P42	8/30 '05
85	add L32 and C822 on SPDIF signal	For EMI	Rev0.4	P42	8/30 '05
86	add C802 /C803 /C804 /C805 1000P for CLKREQA#/CLKREQB#/CLKREQC#/CLKREQD#	For EMI	Rev0.4	P15	8/30 '05
87	U40 pin5,6,7,8 contact to GND	schematic update for SI2 fan can't full trun on issue	Rev0.5	P04	10/26 '05
88	change C599 from 220u to 330u	steady the 1.8V	Rev0.5	P11	10/26 '05
89	add R103 40.2ohm	nvidia recommend	Rev0.5	P21	10/28 '05
90	change R510,R75,R533,R168 from 120ohm to 499ohm for NV73 only	nvidia recommend	Rev0.5	P22-25	10/26 '05
91	straps table PEK_CFG[2:0] from 010 to 001 and PCI_DeVID[3:0] NV73M from 1010 to 1011	nvidia recommend	Rev0.5	P26	10/26 '05
92	add C825 15p_0402 for MSCLK_SDCLK_SMBLW# signal	For EMI	Rev0.5	P32	10/26 '05
93	add C823 1000P_0402 for +VCC_SD	For EMI	Rev0.5	P32	10/26 '05
94	add C824 1000P_0402 for +VCC_SM_XD	For EMI	Rev0.5	P32	10/26 '05
95	add C826 1000P_0402 for JP32 pin4	For EMI	Rev0.5	P32	10/26 '05
96	change PCM_SPK pull down R588 from 43K to 10K	TI recommend	Rev0.5	P32	10/26 '05
97	D29,D30,D31,D32 pin1 contact to +VCC_MS	schematic update for SI2 MS card can't work issue	Rev0.5	P32	10/26 '05
98	add R607 22ohm and @ C827 10P	Reserve	Rev0.5	P32	10/26 '05
99	U18 pin06 contact to +3VS	TI recommend	Rev0.5	P33	10/26 '05
100	add @ R606 110ohm	Reserve	Rev0.5	P35	10/26 '05
101	change Q46 to U45 analog switch	design change	Rev0.5	P40	10/26 '05
102	change U38 pin3,4 form +5VALW to +5V	design change	Rev0.5	P41	10/26 '05
103	change Q2 from A03413 to A03419		Rev0.5	P41	10/26 '05
104	add D38-D45 for KB ESD solution	For ESD request	Rev0.5	P42	10/26 '05
105	AIR_ACIN change contact to U24 pin81 and add R605 for BID define, add D37.	design change	Rev0.5	P44	10/26 '05

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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Solve the oscillate of +3VALWP when plug adapter.	48	Change PC11 from 10U_0805_10V to 0.1U_0603_25V.	2005.06.01	
2	Adjust VGA power rail sequence.	54	Add PQ55, PQ56 and PR249	2005.06.21	
3	To protect PQ21, because SUSP change to 18.5V from 5V.	52	Add PR253 and change PR114 to 510K_0402_5%.	2005.08.10	
4	To save S5 power consumption.	50,48	Add PR254, PR13, PR14, PQ1 and PC8. Reserve PR255.	2005.08.15	
5	To solve EMI issue.	53,49	Add PR117,PR129,PR119,PR138,PC108 and PC119. Change PJP16 to PL18 and PR30 from 0_0402 to 2.2_0603.	2005.08.15	
6	To speed up CP mode response.	49	Change PR32 to 10K; PR35 to 6.8K and PC21 to 2200P.	2005.08.23	
7	Reserve capacitor to reduce noise.	49	Reserve PC209.	2005.08.27	
8	To speed up C4 return to C0. follow Intel recommend.	53	Change PR141 from 0_0402_5% to 499_0402_1%.	2005.08.29	
9	To pull up +1.8V power plan to 1.846V.	51	Change PR89 from 10.2K to 10.5K.	2005.10.01	
10	To filter high frequency from AirCard.	55	Add PC210 22P_0402_50V.	2005.11.25	

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