

# Compal confidential

## Schematics Document

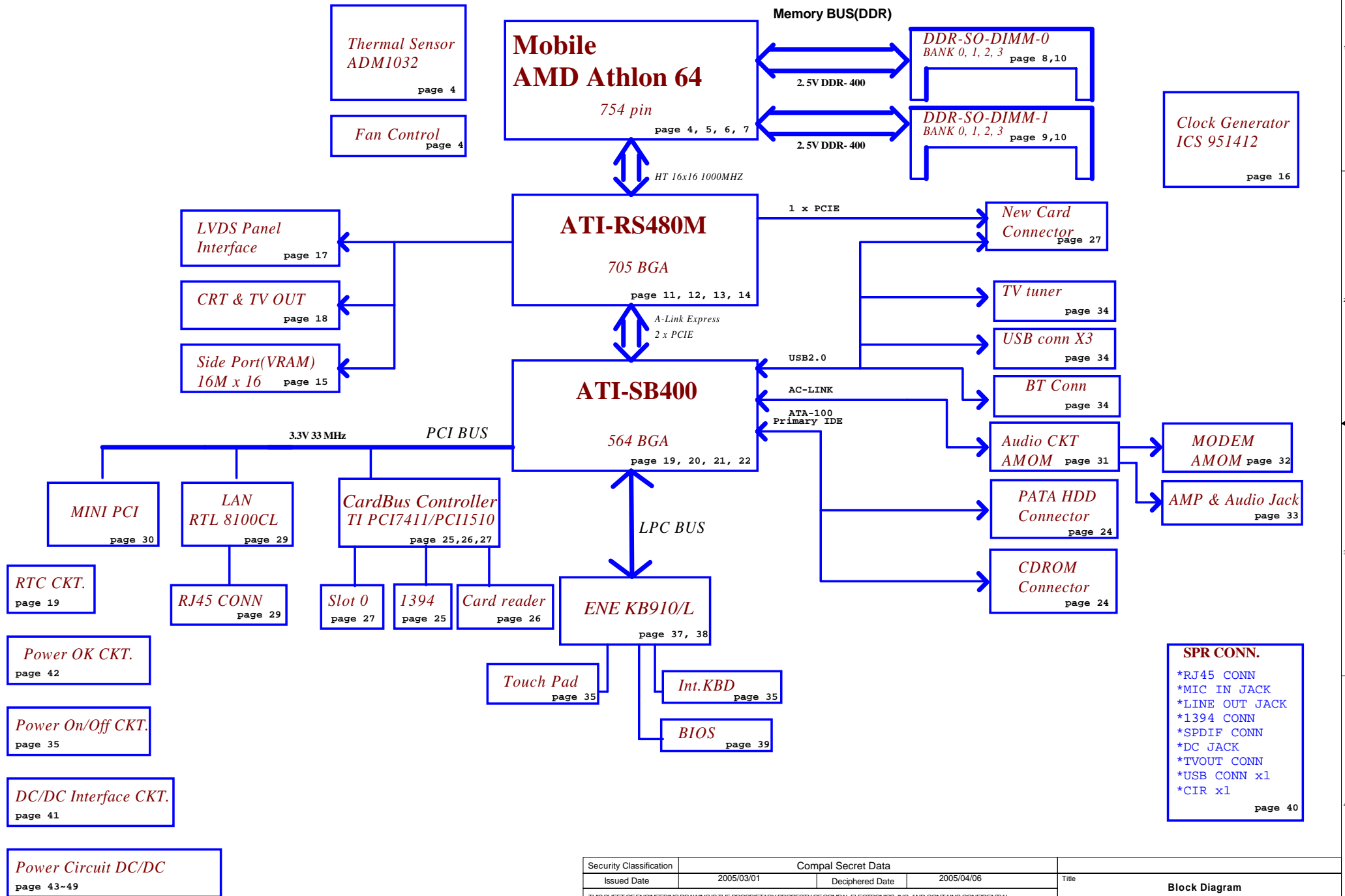
### AMD K8 with ATI RS480M+ATI SB400

2005-08-29

REV:0.8



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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Cover Page		
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Block Diagram	
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## Voltage Rails

power plane State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
s0	O	O	O
s1	O	O	O
s3	O	O	X
s5 s4/AC	O	X	X
s5 s4/AC don't exist	X	X	X

O MEANS ON

X MEANS OFF

## PCI Devices

INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

EXTERNAL	IDSEL #	REQ/GNT #	PIRQ
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS & 1394	AD20	2	E,H

## BOM STATUS :

VRAM@ ,VRAMIC@, SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17\_EXP@ ,15\_EXO@,CIR@ ,D@, C@, 15.4@, DOCK@, WL\_LED@

45@ ( for 45 level RTC battery )

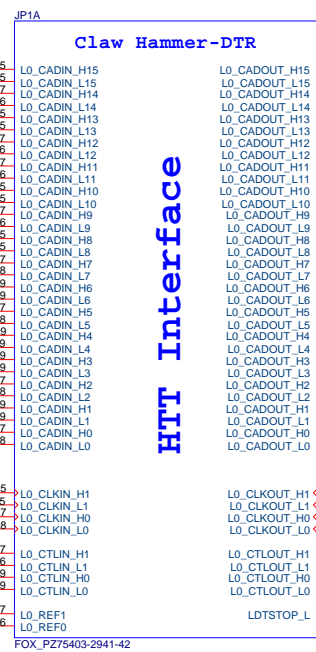
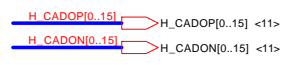
HAL10 17"      VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17\_EXP@ ,CIR@ ,D@ ,DOCK@,WL\_LED@

HAL20 FF 15.4"      VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,15\_EXP@ ,CIR@ ,C@ ,DOCK@,WL\_LED@, 15.4@(LED)

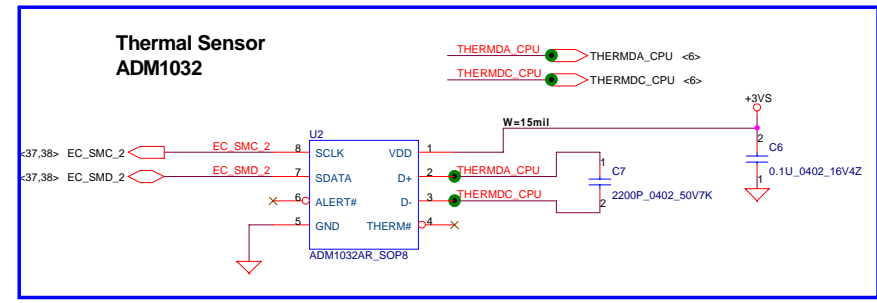
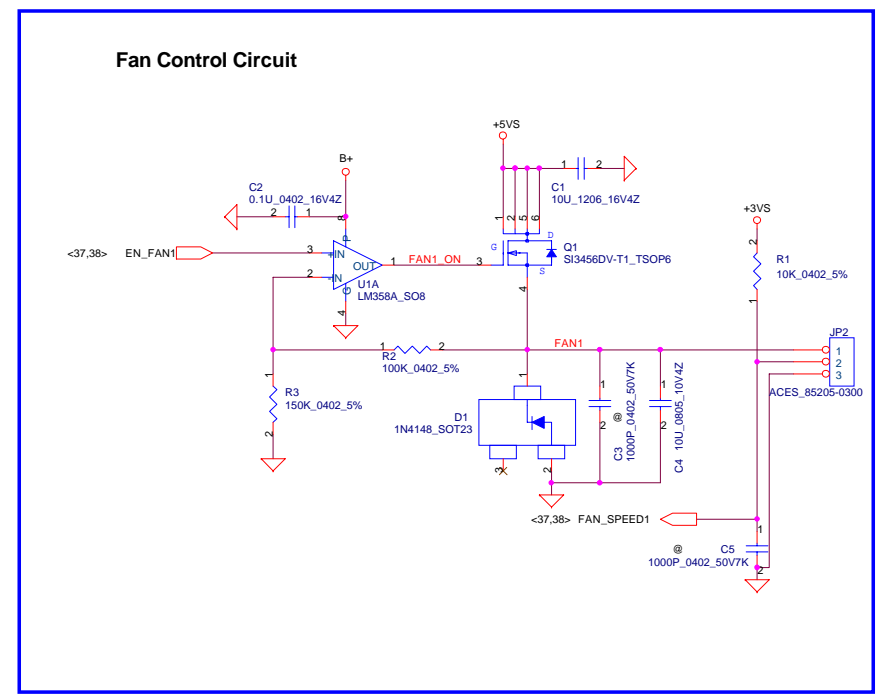
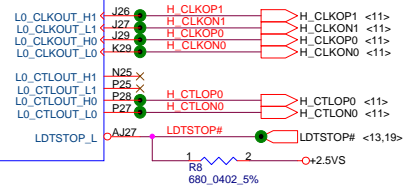
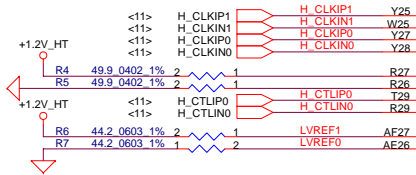
HAL20 DF 15.4"      EXP@, C@ ,DOCK@ ,15.4@(LED), CIR@, WLAN@, 15\_EXP@

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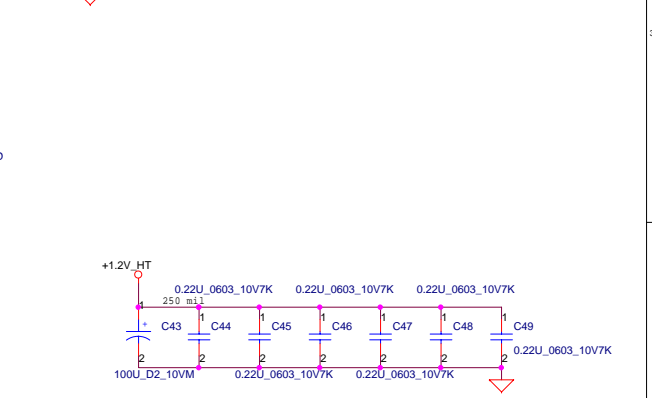
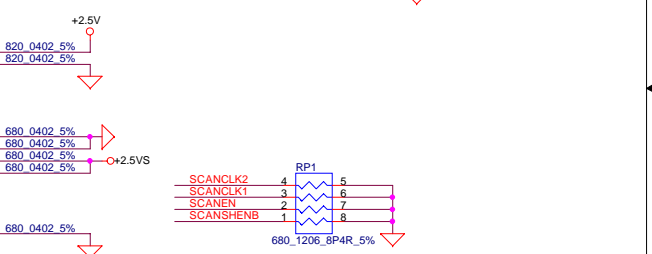
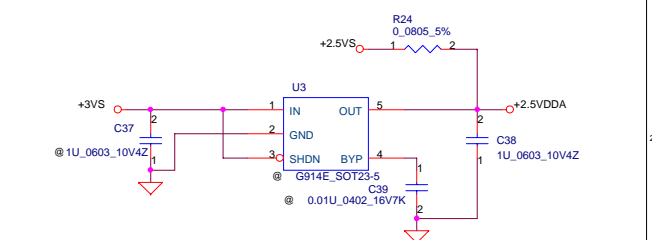
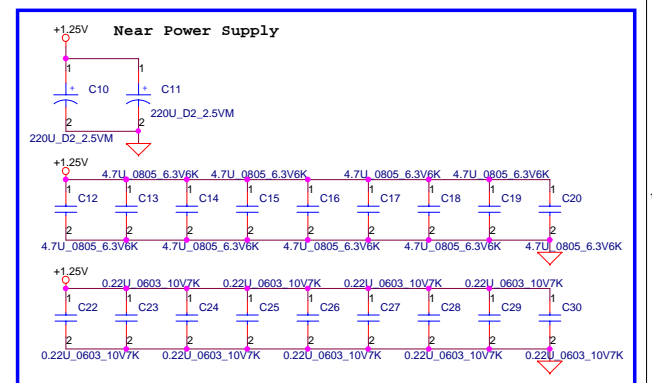
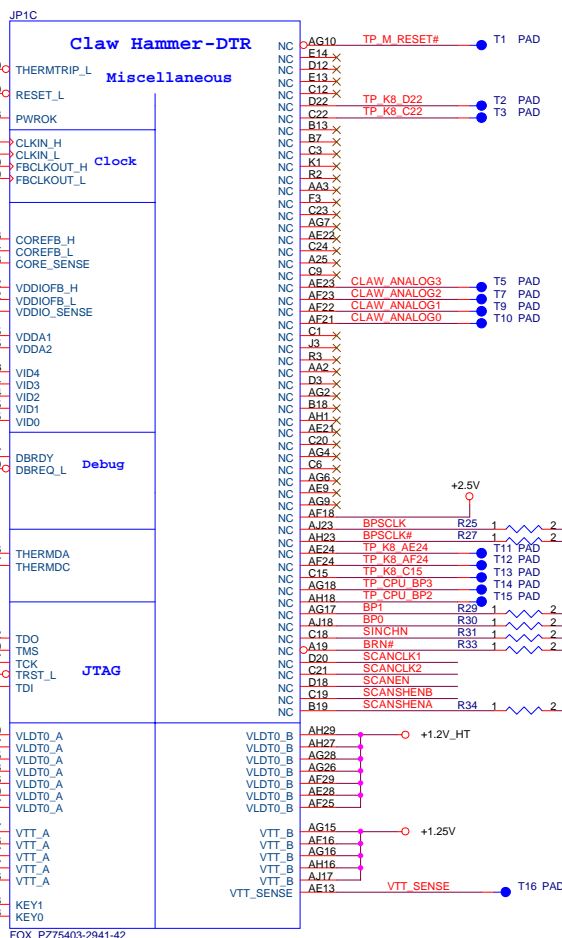
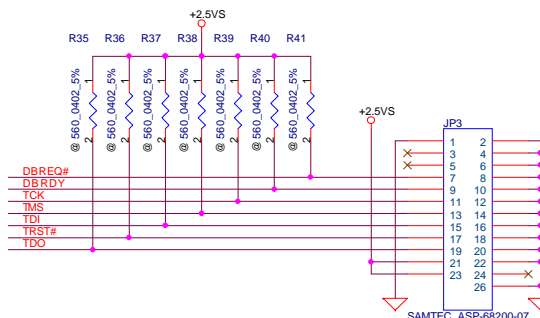
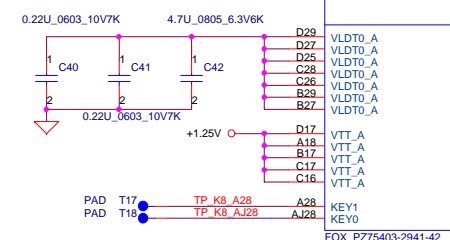
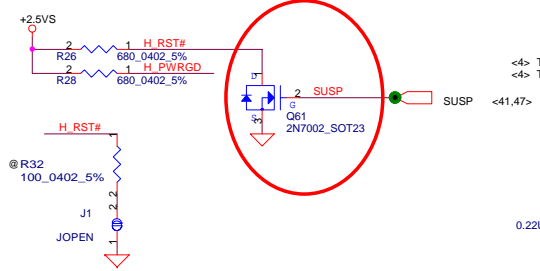
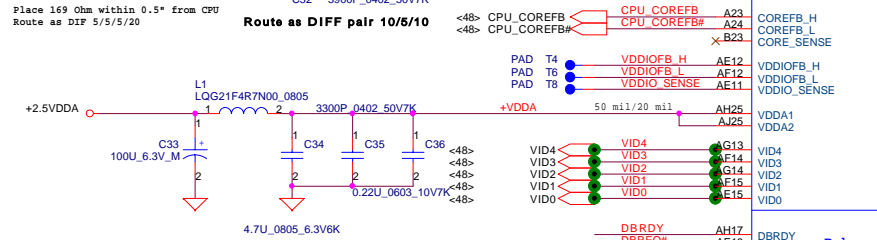
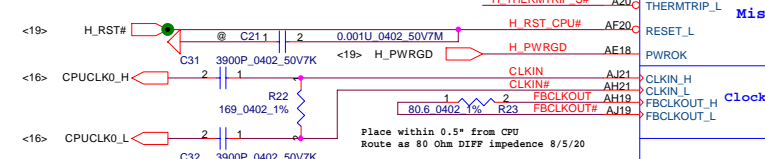
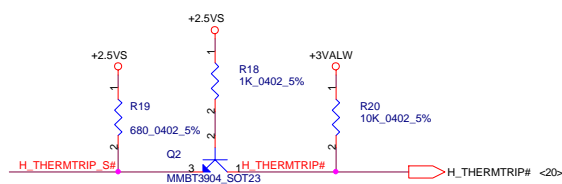


**HTT Interface**

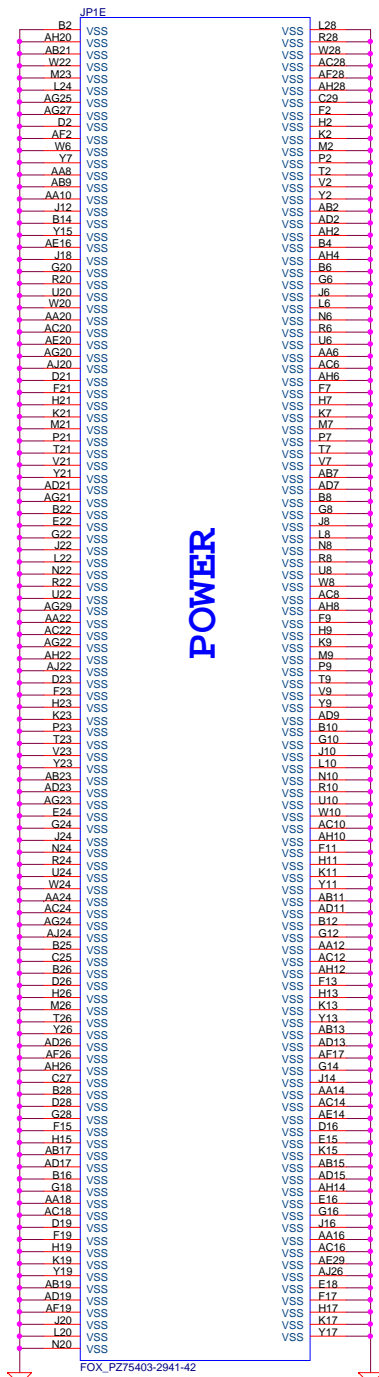


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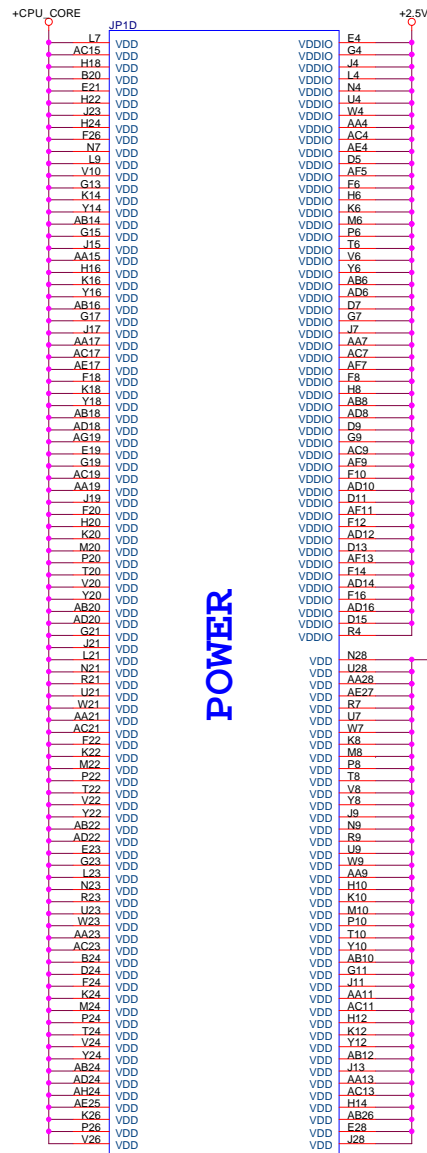




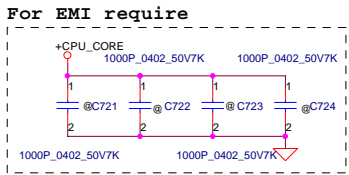
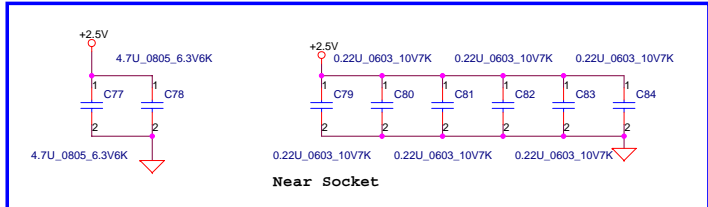
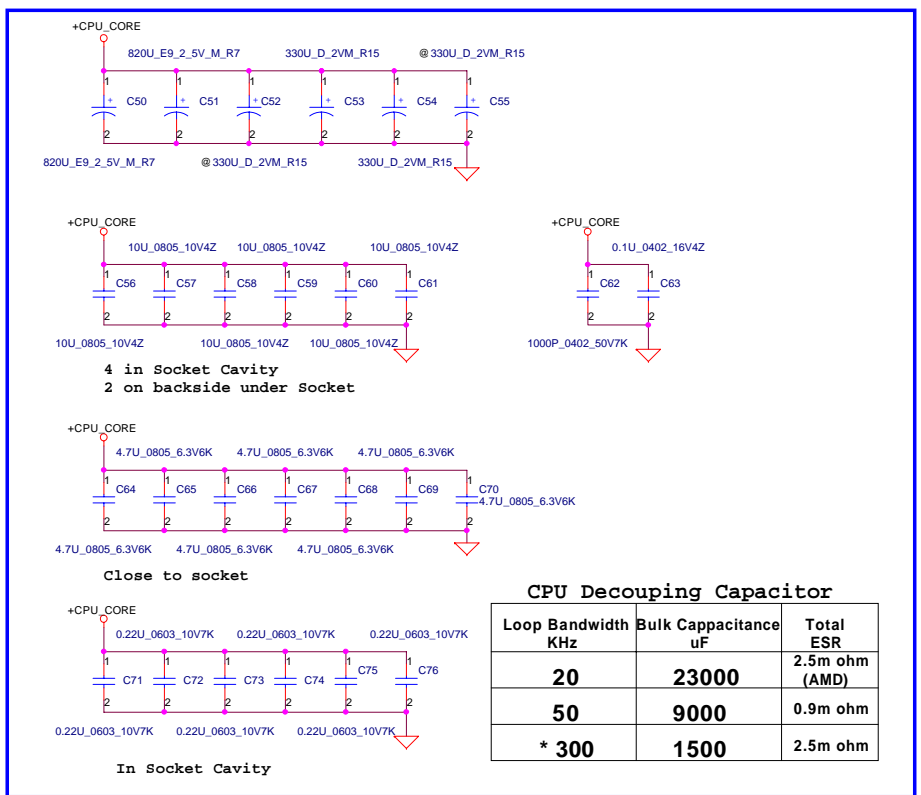
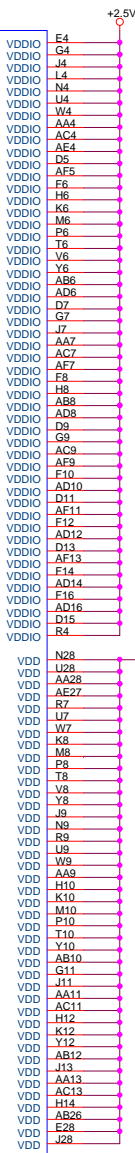
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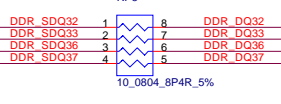
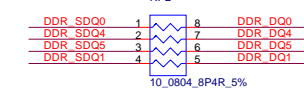
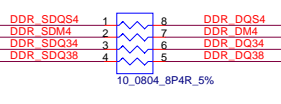
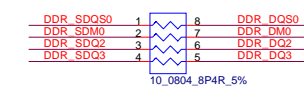
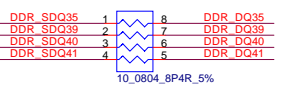
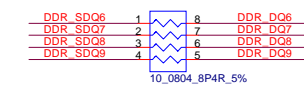
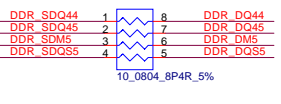
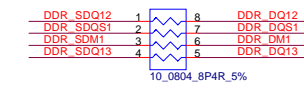
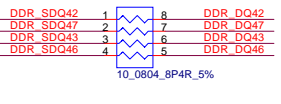
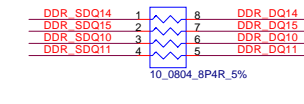
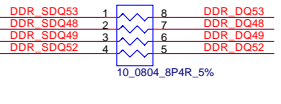
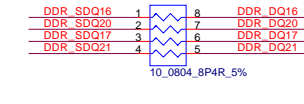
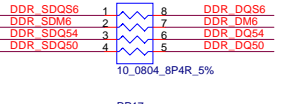
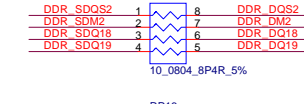
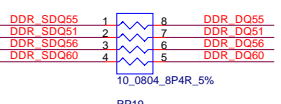
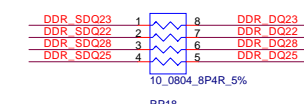
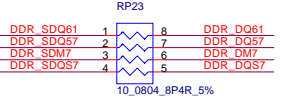
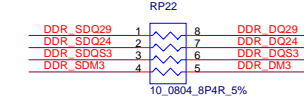
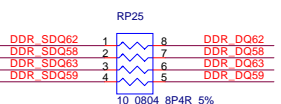
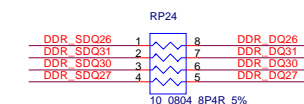
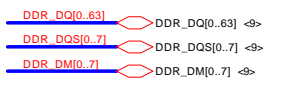
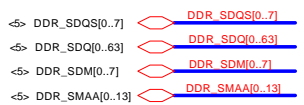
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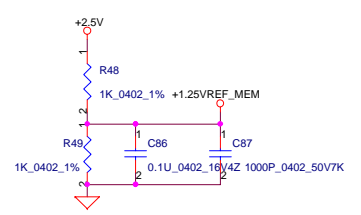
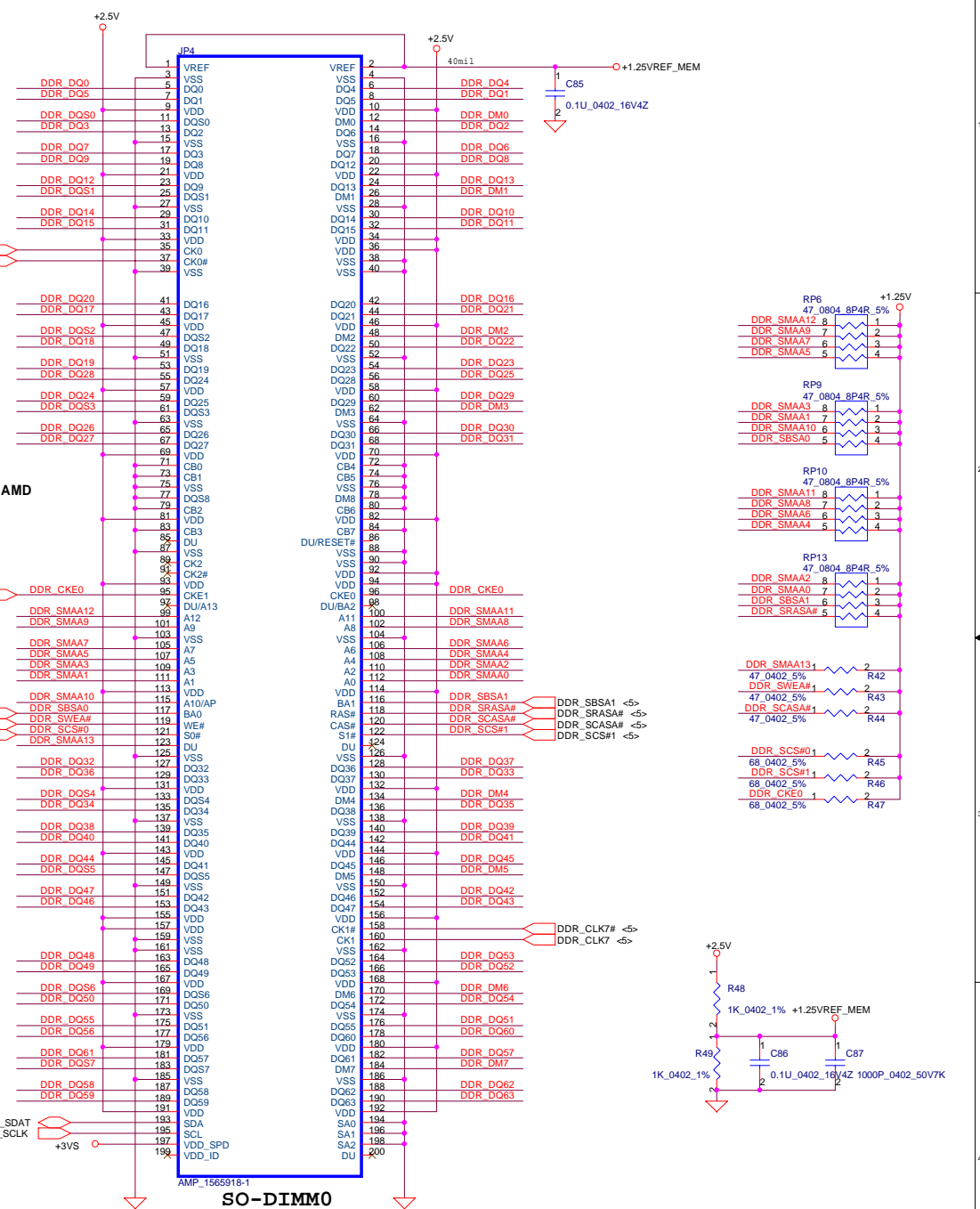


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Note:  
DDR\_SMAA13 Recommend for AMD

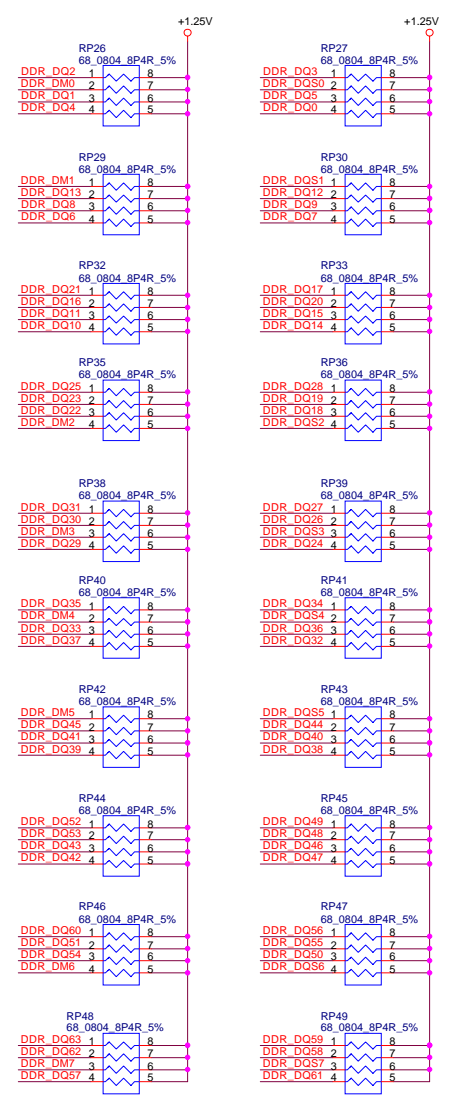
Layout note  
Place these resistors  
close to DIMM0,  
all trace length<500 mil



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<8> DDR\_DQS[0..7]       **DDR DQS[0..7]**  
 <8> DDR\_DQ[0..63]       **DDR DQ[0..63]**  
 <8> DDR\_DM[0..7]       **DDR DM[0..7]**  
 <5> DDR\_SMAB[0..13]    **DDR SMAB[0..13]**

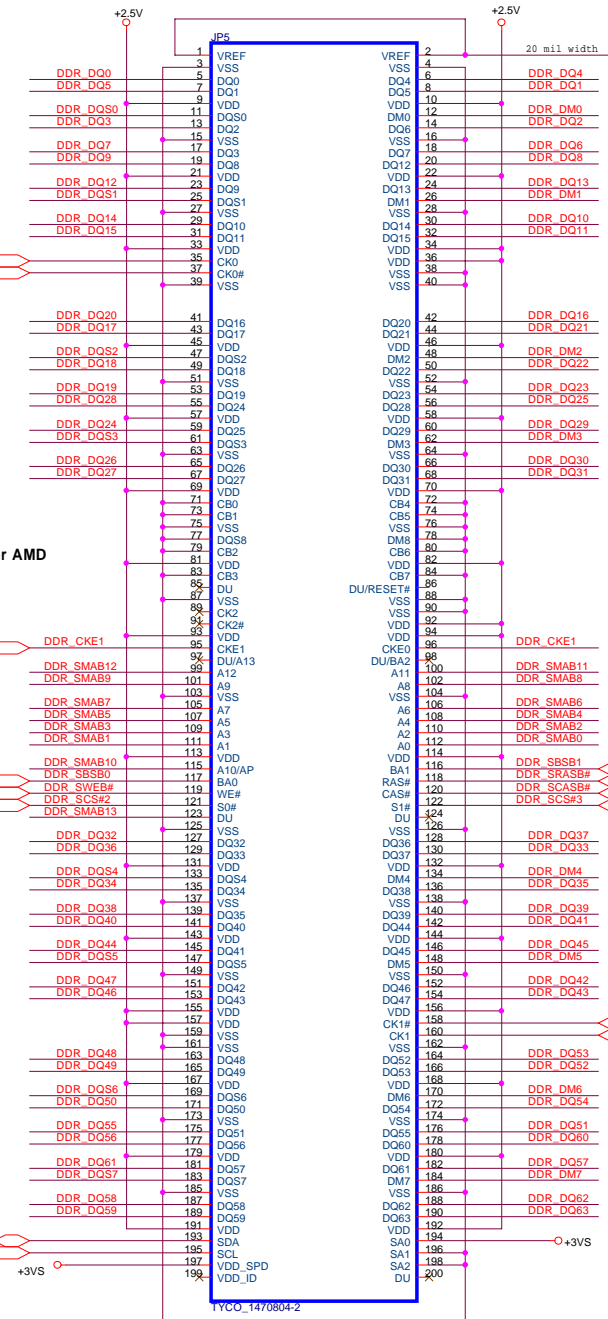


**Note:**  
DDR\_SMAA13 Recommend for AMD

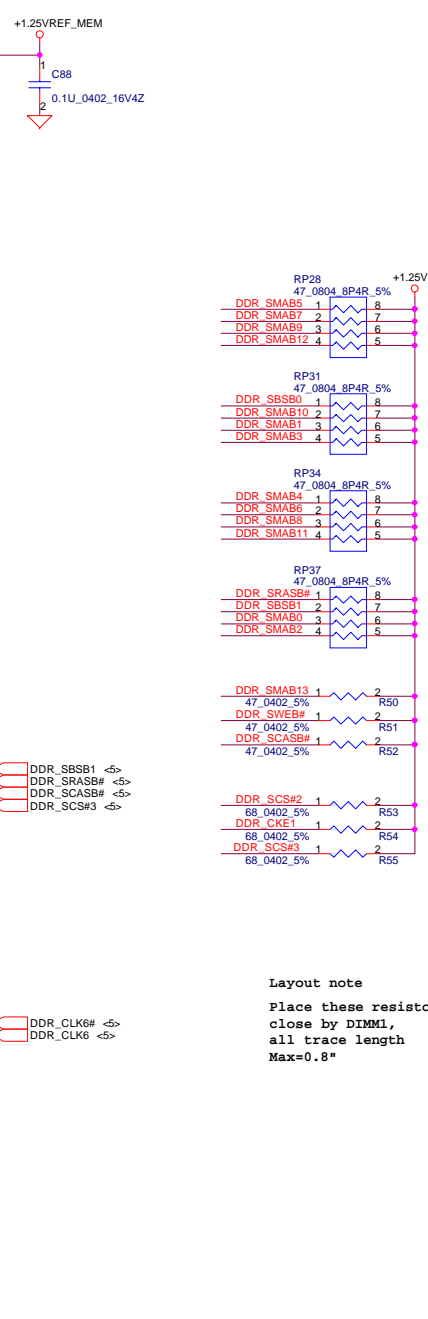
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 <5> DDR\_SBSB0       **DDR\_SBSB0**  
 <5> DDR\_SWEB#       **DDR\_SWEB#**  
 <5> DDR\_SCS#2       **DDR\_SCS#2**

**Layout note**  
Place these resistor closely DIMM1, all trace length<=800mil

<8,16,20,28> SB\_SDAT       **SB\_SDAT**  
 <8,16,20,28> SB\_SCLK       **SB\_SCLK**



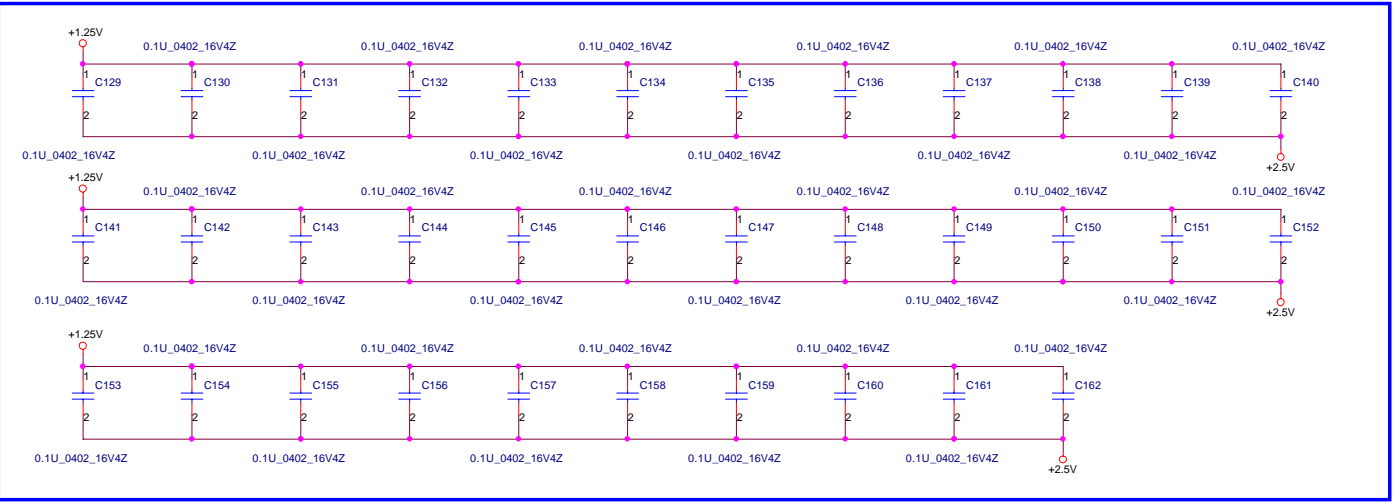
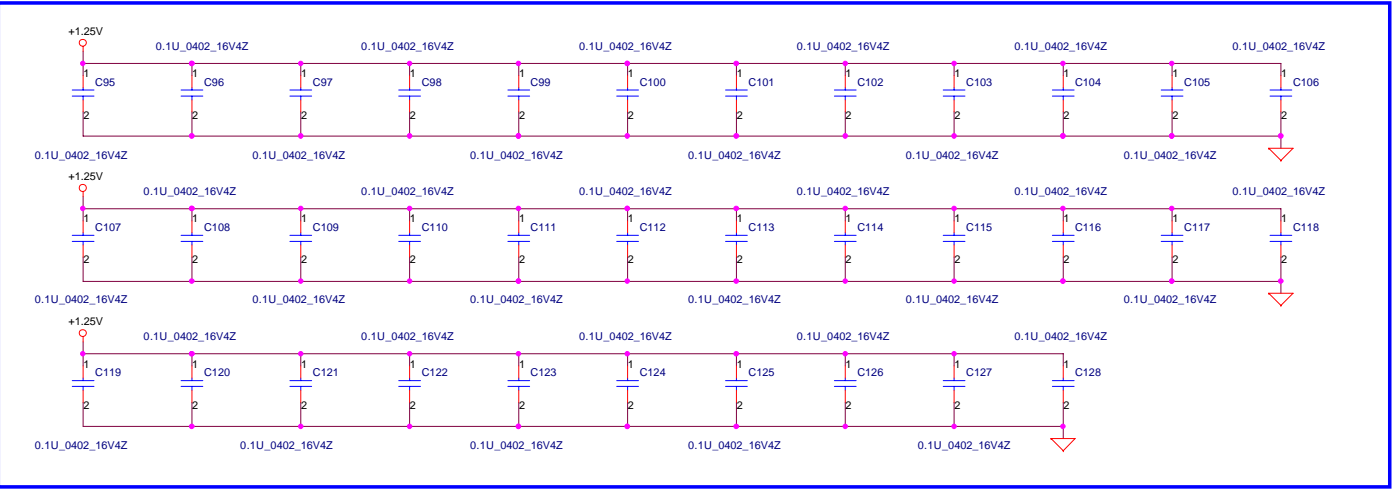
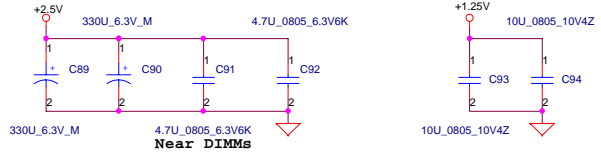
**DIMM1**



**Layout note**  
Place these resistor close by DIMM1, all trace length Max=0.8"

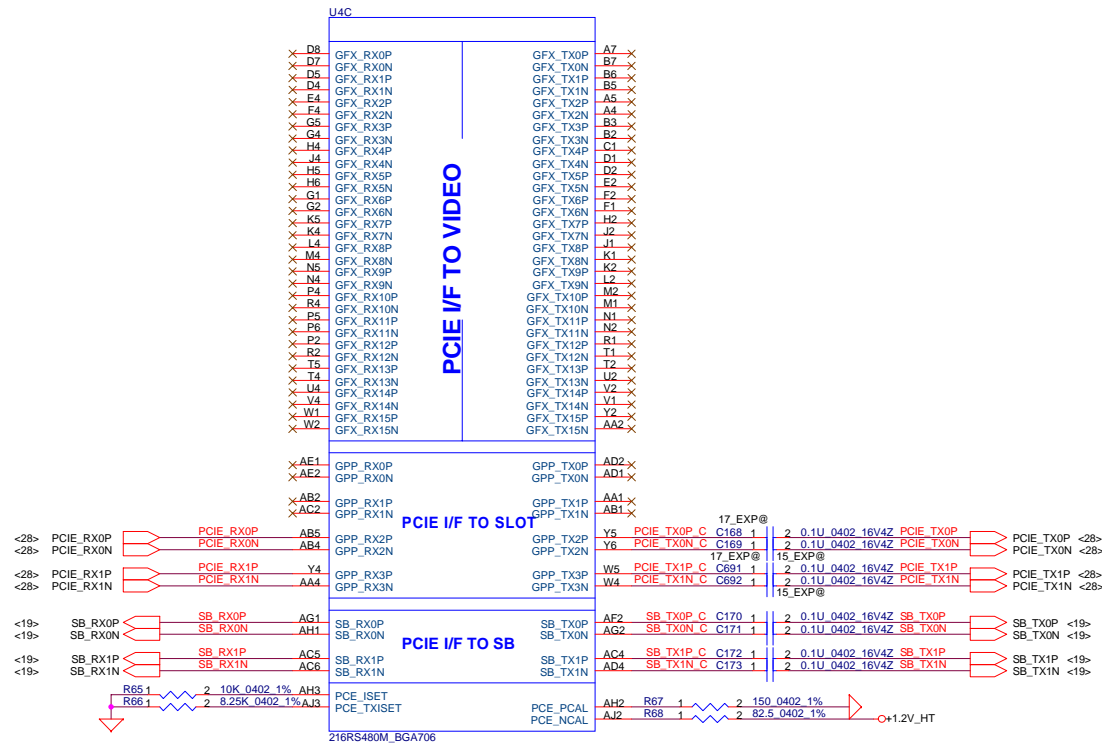
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**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25V



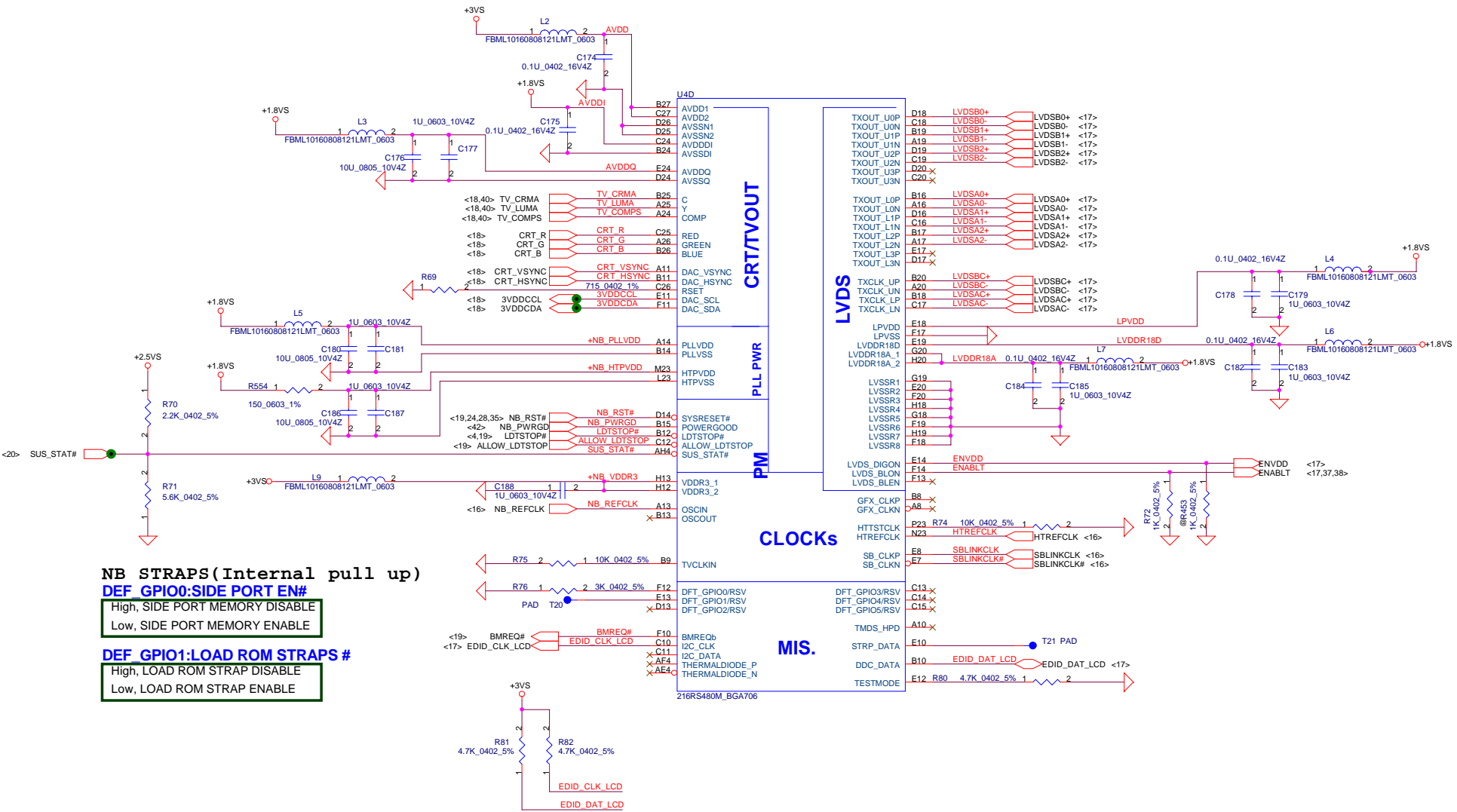
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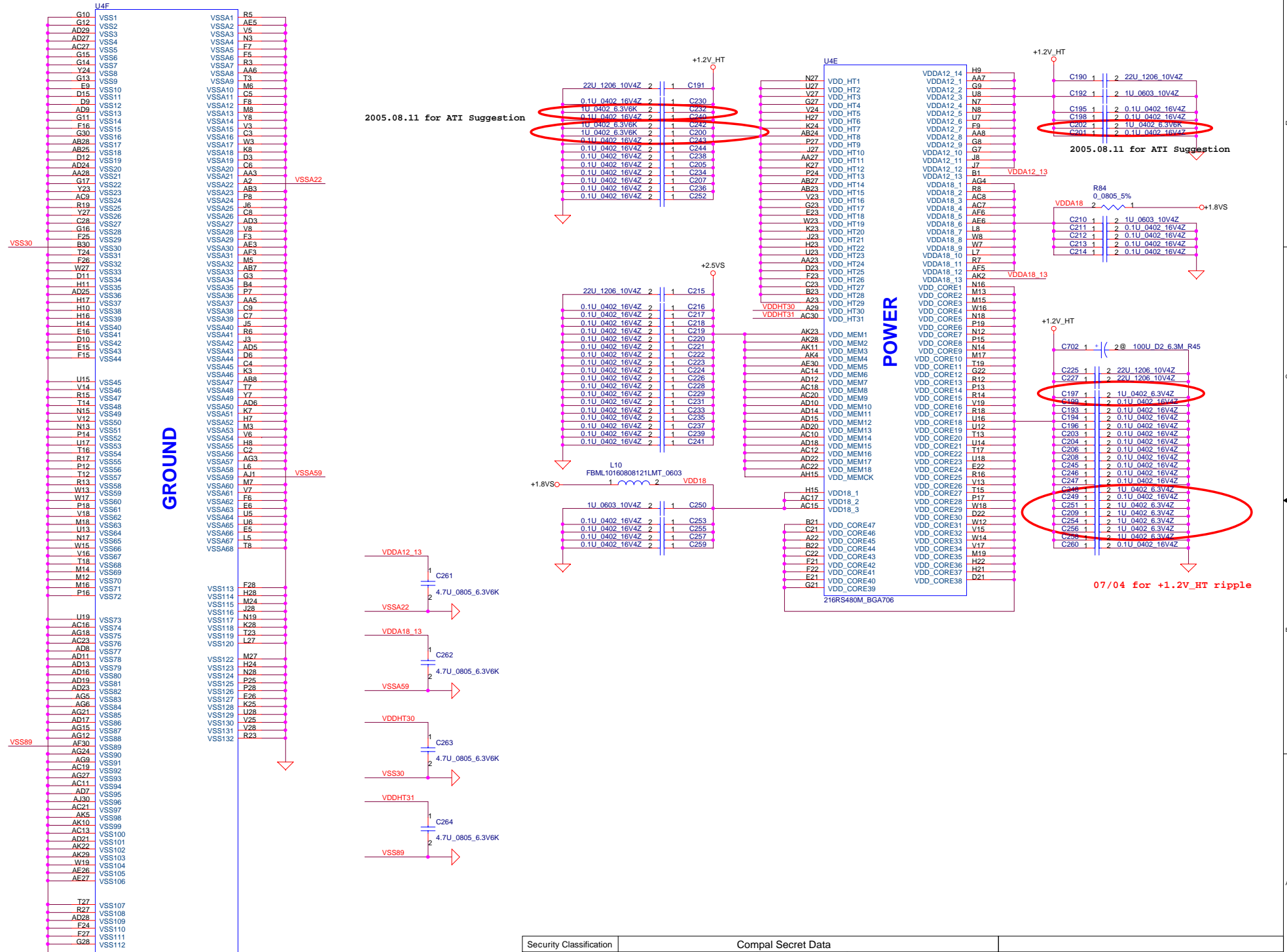


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**AVDD , AVDDI , AVDDQ , +NB\_PLLVDD , +NB\_HTPVDD  
+NB\_VDDR3 , LPVDD , LVDDR18D , LVDDR18A (20mils)**



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Date:	Tuesday, August 30, 2005	Sheet	13	of 53



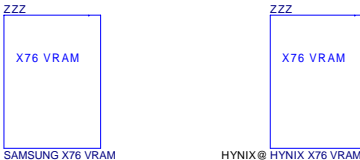
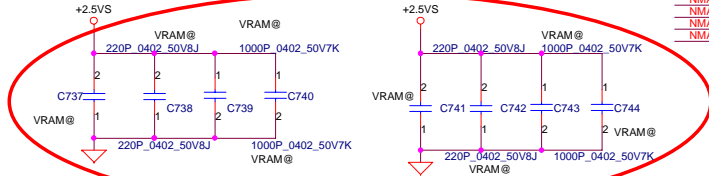
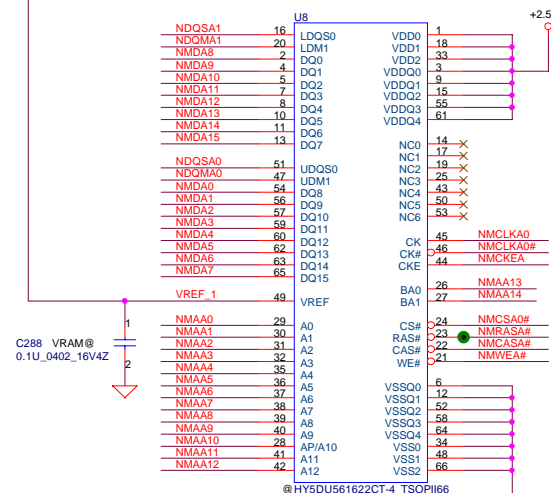
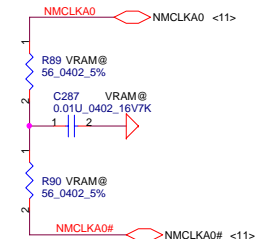
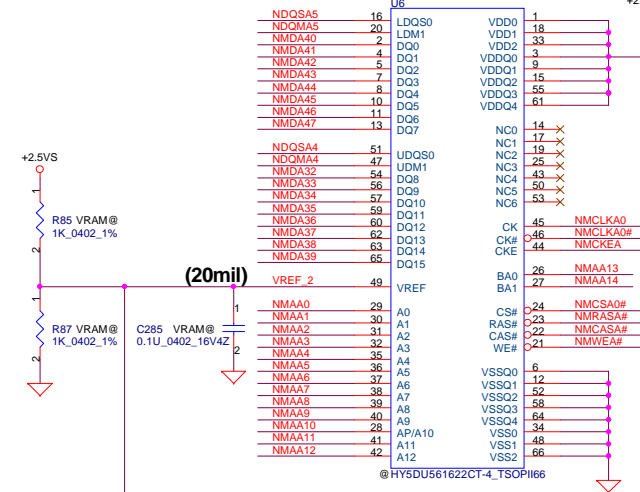
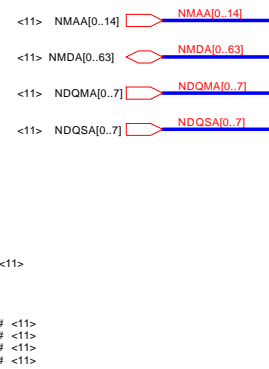
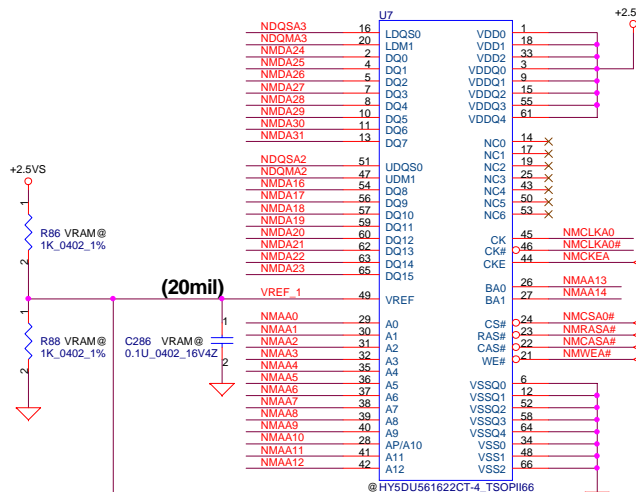
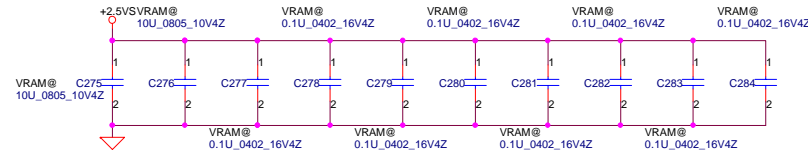
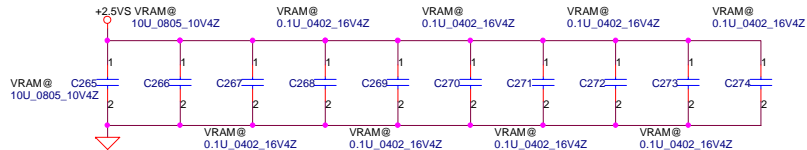
2005.08.11 for ATI Suggestion

2005.08.11 for ATI Suggestion

POWER

07/04 for +1.2V\_HT ripple

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	RS480M Power/GND	
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Date	Tuesday, August 30, 2005	Sheet	14	of	53



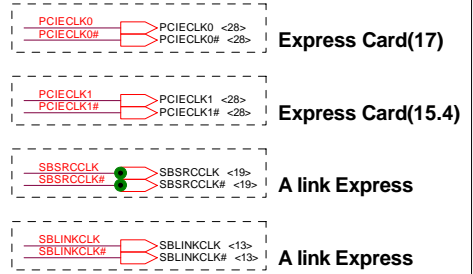
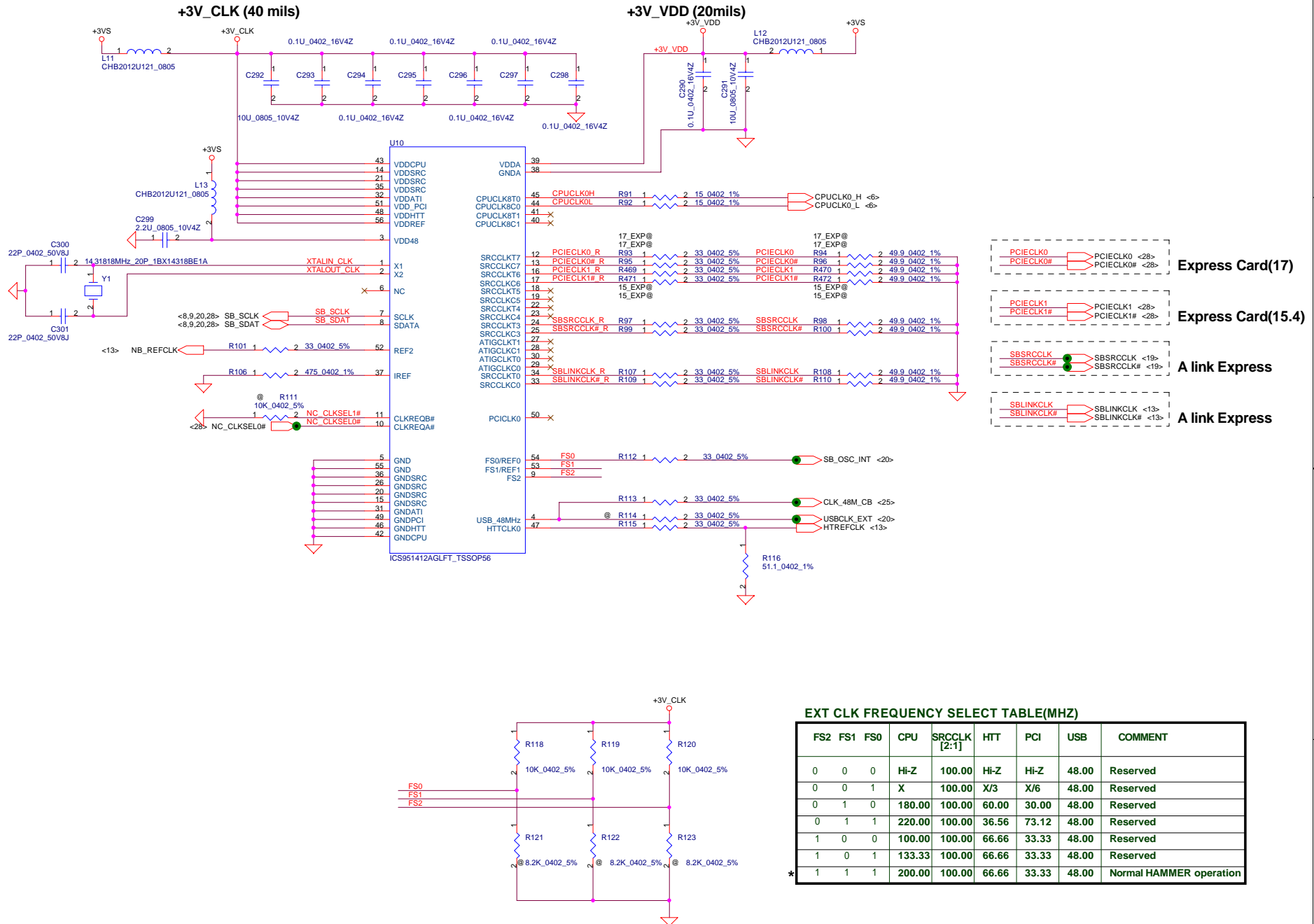
07/04 For EMI

Security Classification	Compal Secret Data	
Issued Date	2005/03/01	Deciphered Date
		2005/04/06

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Title		VGA DDR	
Size	Document Number	Rev	0.8
Custom	LA-2771	Date	Tuesday, August 30, 2005
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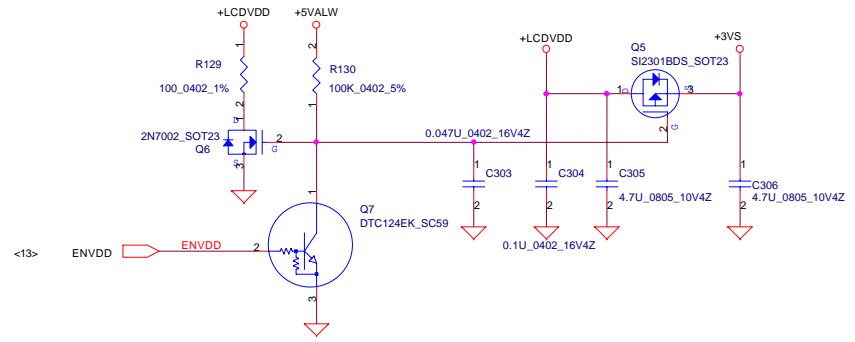
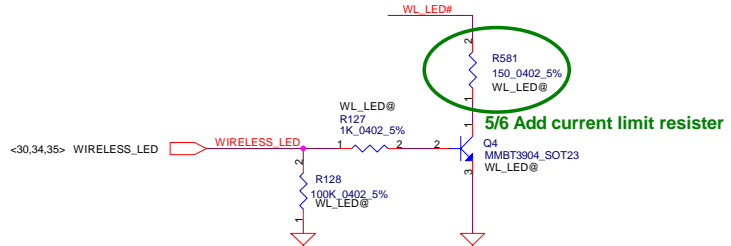
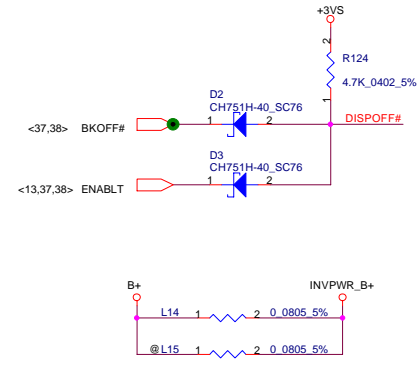
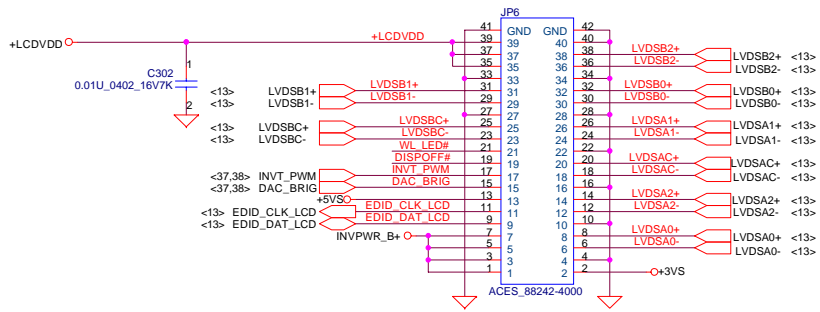


EXT CLK FREQUENCY SELECT TABLE(MHZ)

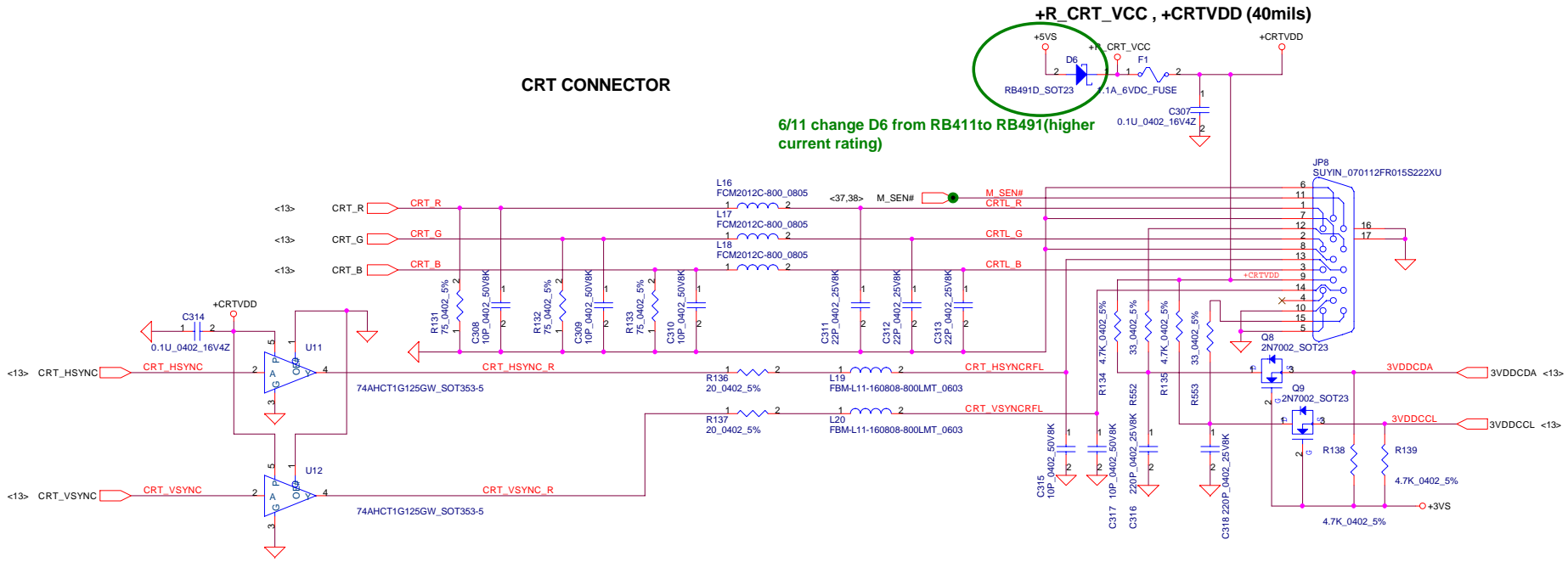
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation



### LCD Panel & inverter Connector

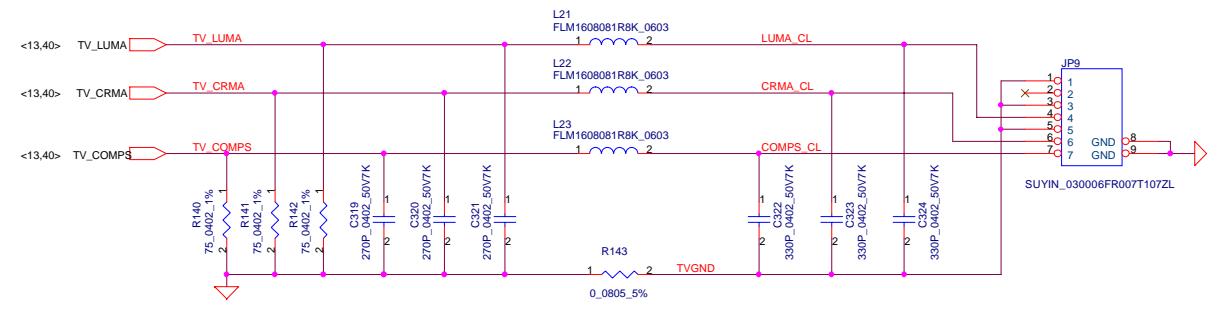


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	LVDS Panel Interface	
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Date: Tuesday, August 30, 2005				Sheet	17 of 53



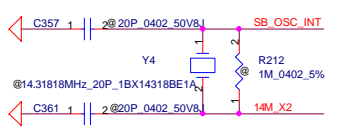
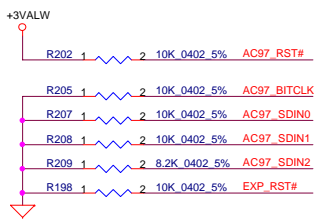
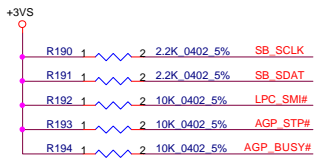
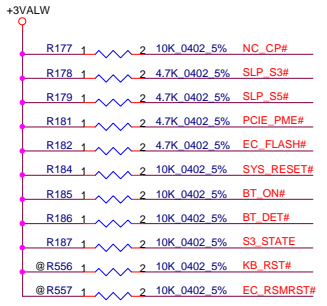
6/11 change D6 from RB411 to RB491 (higher current rating)

### TV-Out Connector S-Video

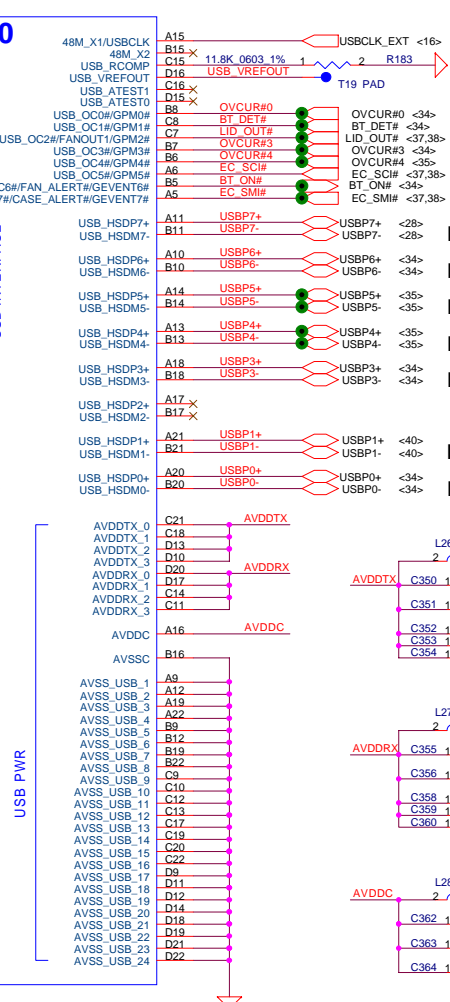
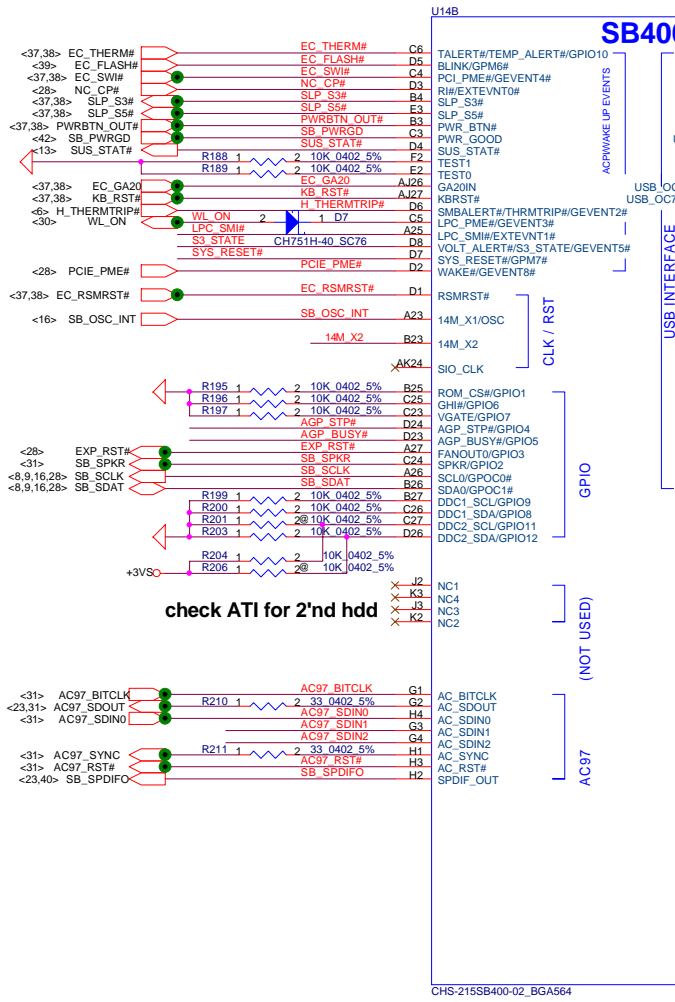


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	CRT Connector & TV-OUT CONN	
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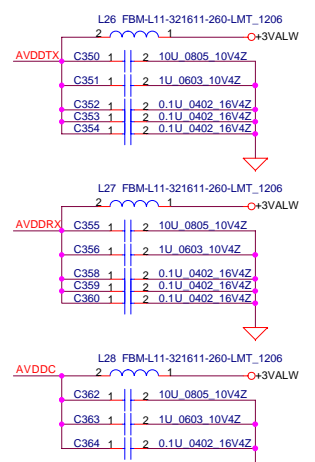




	GPI012	GPI011
* HYNIX 128MB	0	1
SAMSUNG 128MB	1	1
No VRAM	0	0
Reserved	1	0

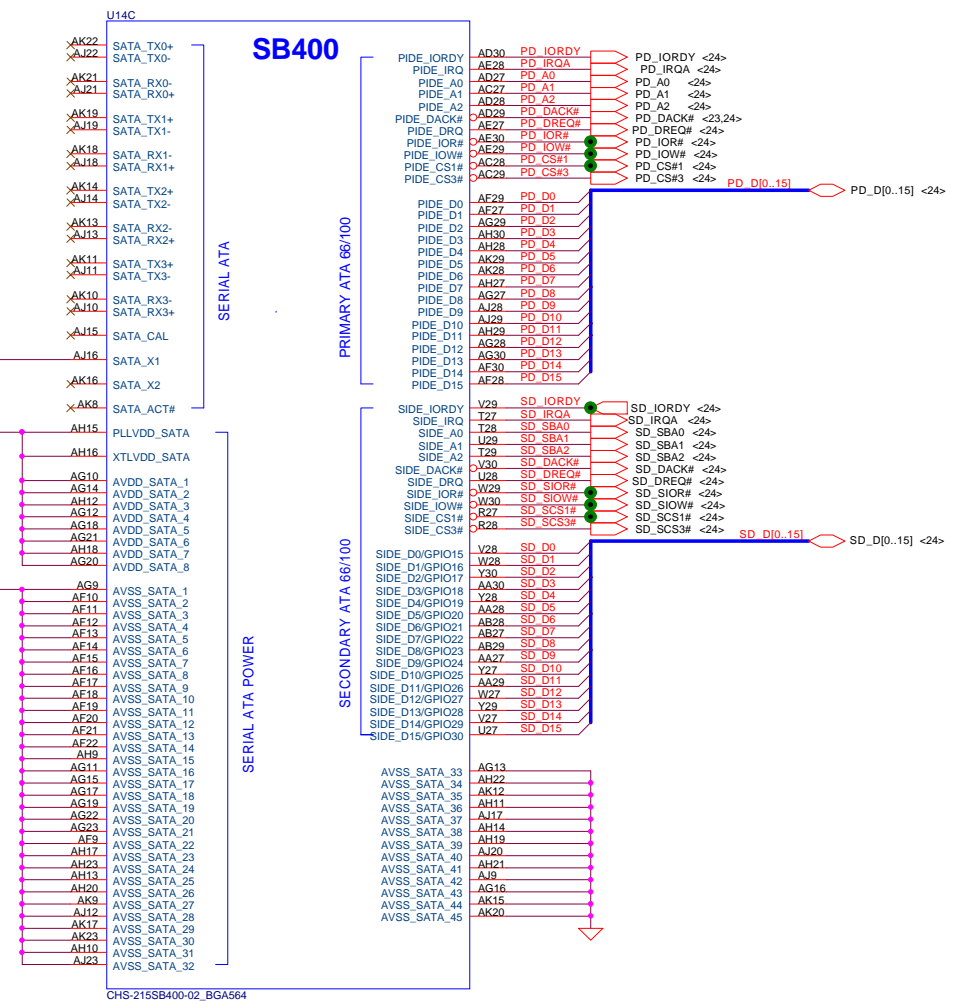


- Express Card 15.4
- Bluetooth
- Right side USB
- Right side USB
- Left side USB
- Docking
- Left side USB

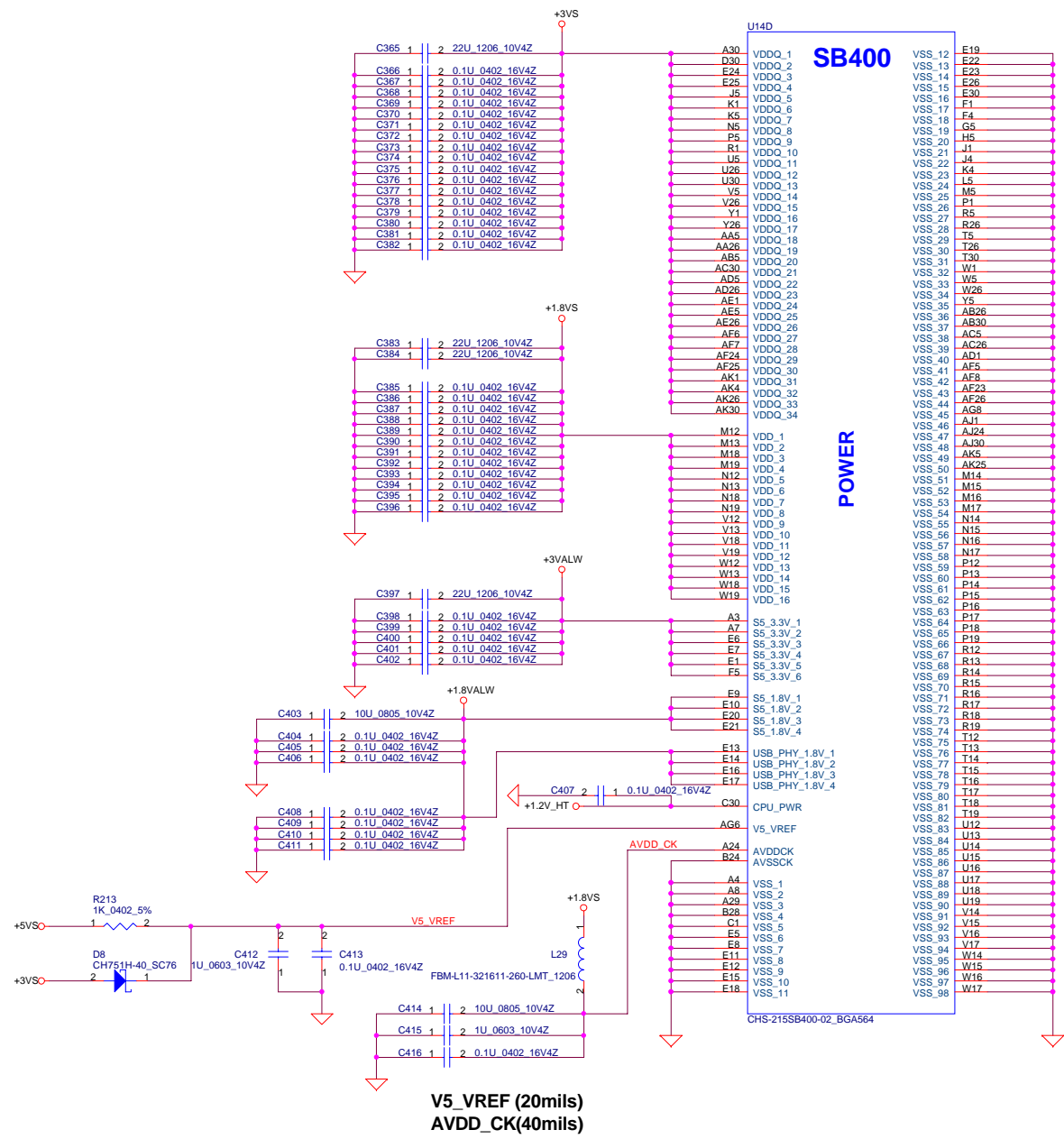


AVDDC (20mils)  
AVDDTX, AVDDRX (40mils)

Security Classification	Compal Secret Data			Title
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-USB/ACPI/AC97/GPIO
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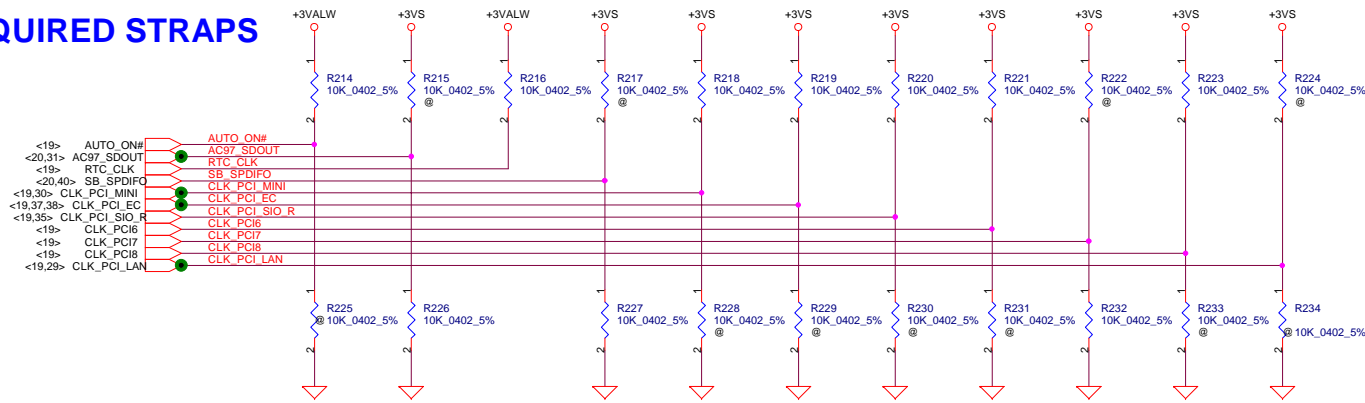
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-IDE/SATA	
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**V5\_VREF (20mils)  
AVDD\_CK(40mils)**

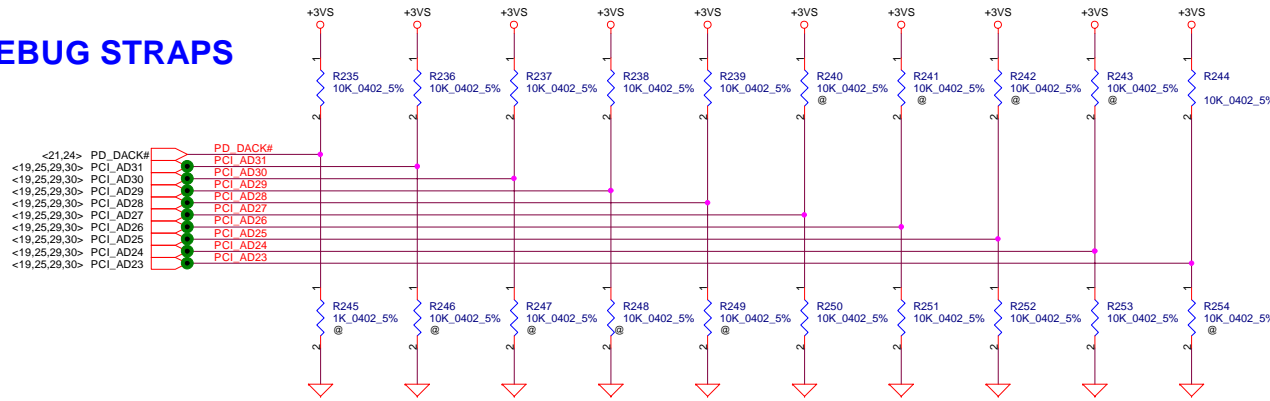
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	<b>SB400-Power/GND</b>
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# REQUIRED STRAPS



	AUTO_ON#	AC97_SDOUT	RTC_CLK	SB_SPDIF0	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	CLK_PCI8
<b>PULL HIGH</b>	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	PCIE_CM_SET LOW DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712 )	SIO 48MHz DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	PCIE_CM_SET High	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM DEFAULT	

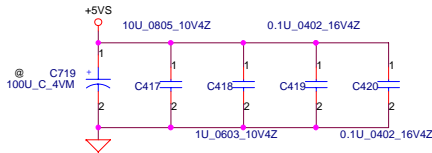
# DEBUG STRAPS



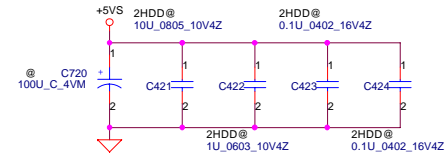
	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
<b>PULL LOW</b>	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Hardware Trap	
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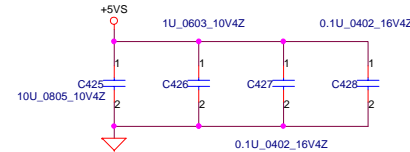
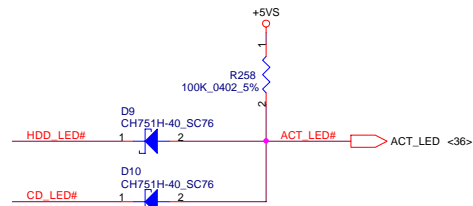
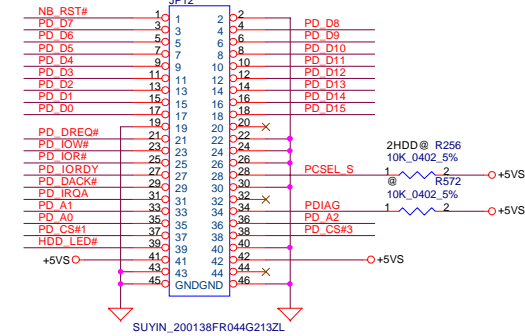
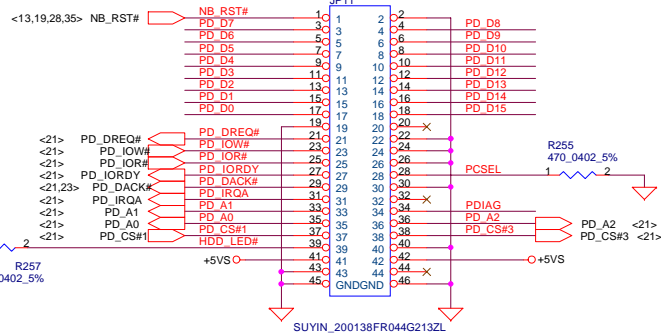
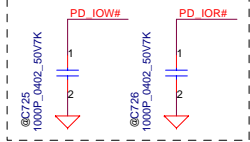
### Main HDD



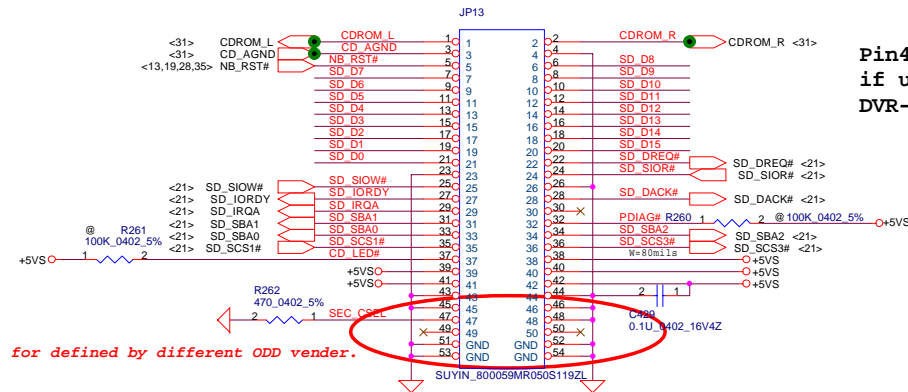
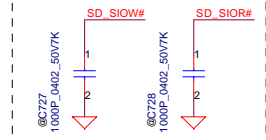
### Second HDD



### EMI



### EMI

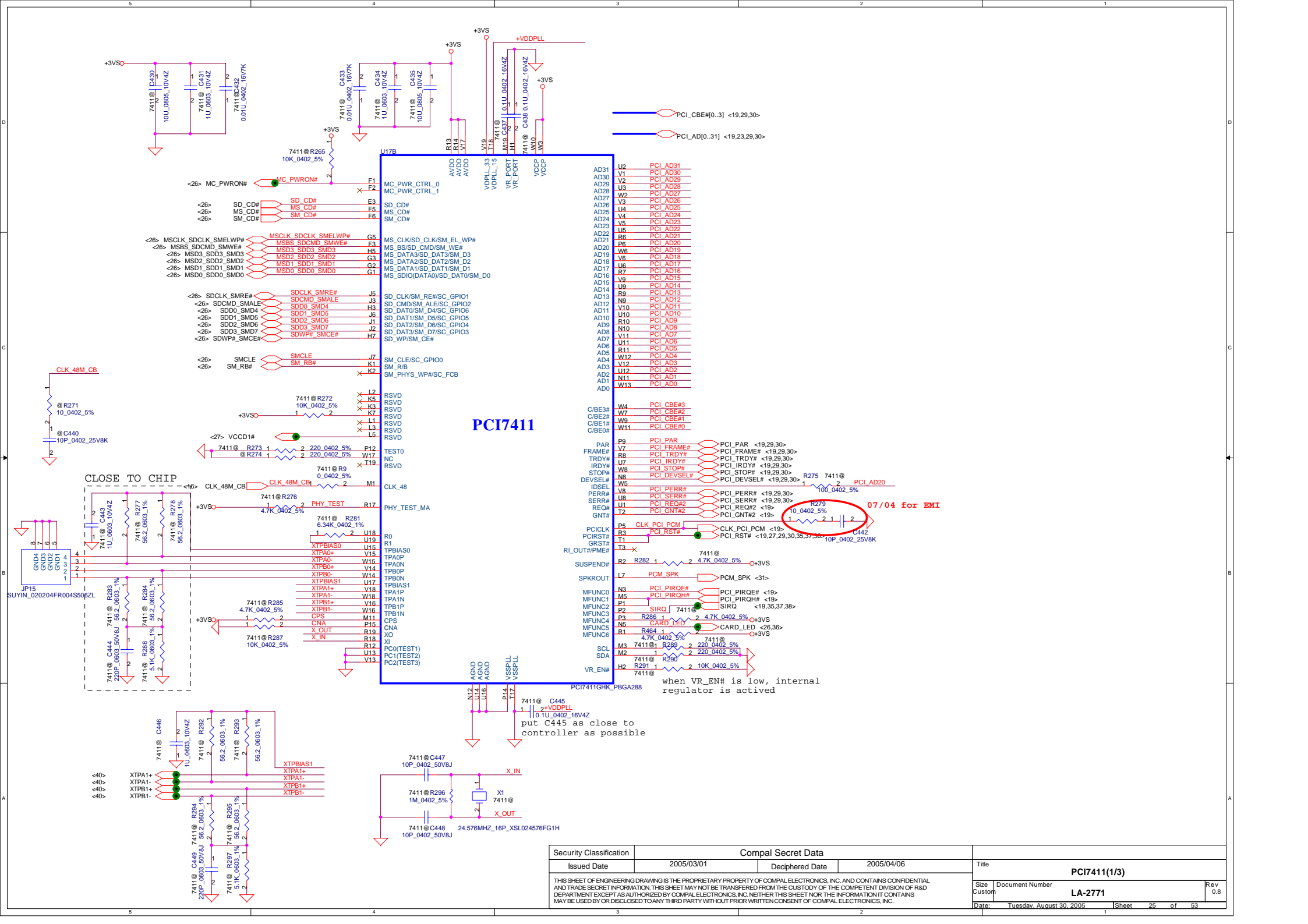


Pin4 of CD\_ROM connector is NC if use Pioneer ODD(DVD Dual DVR-K12TBC/DVR-K13TBC)

07/11 for defined by different ODD vender.

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	HDD/CDROM	
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**PCI7411**

PCI\_CBE#[0..3] <19,29,30>  
 PCI\_AD#[0..31] <19,23,29,30>

- AD31 U12 PCI\_AD31
- AD30 U11 PCI\_AD30
- AD29 U2 PCI\_AD29
- AD28 U3 PCI\_AD28
- AD27 U2 PCI\_AD27
- AD26 U4 PCI\_AD26
- AD24 U4 PCI\_AD24
- AD23 U5 PCI\_AD23
- AD22 U6 PCI\_AD22
- AD21 U8 PCI\_AD21
- AD20 U6 PCI\_AD20
- AD19 U6 PCI\_AD19
- AD18 U6 PCI\_AD18
- AD17 U6 PCI\_AD17
- AD16 U7 PCI\_AD16
- AD15 U9 PCI\_AD15
- AD14 U9 PCI\_AD14
- AD13 U9 PCI\_AD13
- AD12 U9 PCI\_AD12
- AD11 U10 PCI\_AD11
- AD10 U10 PCI\_AD10
- AD9 U10 PCI\_AD9
- AD8 U10 PCI\_AD8
- AD7 U11 PCI\_AD7
- AD6 U11 PCI\_AD6
- AD5 U11 PCI\_AD5
- AD4 U12 PCI\_AD4
- AD3 U12 PCI\_AD3
- AD2 U12 PCI\_AD2
- AD1 U11 PCI\_AD1
- AD0 U13 PCI\_AD0

- C/BE3# U7 PCI\_CBE#3
- C/BE2# U9 PCI\_CBE#2
- C/BE1# U9 PCI\_CBE#1
- C/BE0# U11 PCI\_CBE#0

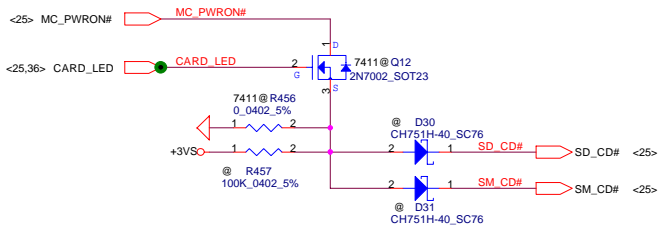
- PAR P9 PCI\_PAR <19,29,30>
- FRAME# U7 PCI\_FRAME# <19,29,30>
- TRDY# U8 PCI\_TRDY# <19,29,30>
- IRDY# U7 PCI\_IRDY# <19,29,30>
- STOP# U8 PCI\_STOP# <19,29,30>
- DEVSEL# U8 PCI\_DEVSEL# <19,29,30>
- PERR# U8 PCI\_PERR# <19,29,30>
- SERR# U8 PCI\_SERR# <19,29,30>
- REQ# U11 PCI\_REQ# <19,29,30>
- GNT# U2 PCI\_GNT# <19,29,30>
- CLK PCI\_PCM U5 CLK\_PCI\_PCM <19,29,30>
- RST# U3 PCI\_RST# <19,29,30,35,37,38>

- PCICLK U5 PCI\_PERR# <19,29,30>
- PCIRST# U3 PCI\_SERR# <19,29,30>
- GRST# U11 PCI\_REQ# <19,29,30>
- T3# X PCI\_GNT# <19,29,30>
- SUSPEND# R2 R282 1 2 4.7K 0.402 5% <3V>
- SPKROUT L7 PCM\_SPK <31>
- MFUNC0 N3 PCI\_PIRQ# <19,29,30>
- MFUNC1 M5 PCI\_PIRQ# <19,29,30>
- MFUNC2 P2 SIRO 7411# SIRO <19,35,37,38>
- MFUNC3 P3 R286 1 2 4.7K 0.402 5% <3V>
- MFUNC4 N5 CARD\_LED <26,36>
- MFUNC6 R1 R464 1 2 4.7K 0.402 5% <3V>
- SCL M3 7411@1 R280 2 220 0.402 5%
- SDA M2 7411@ R290 2 220 0.402 5%
- VR\_EN# H2 R291 1 2 10K 0.402 5%

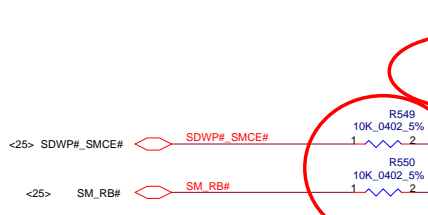
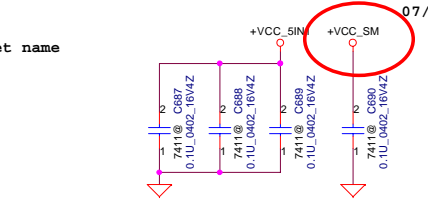
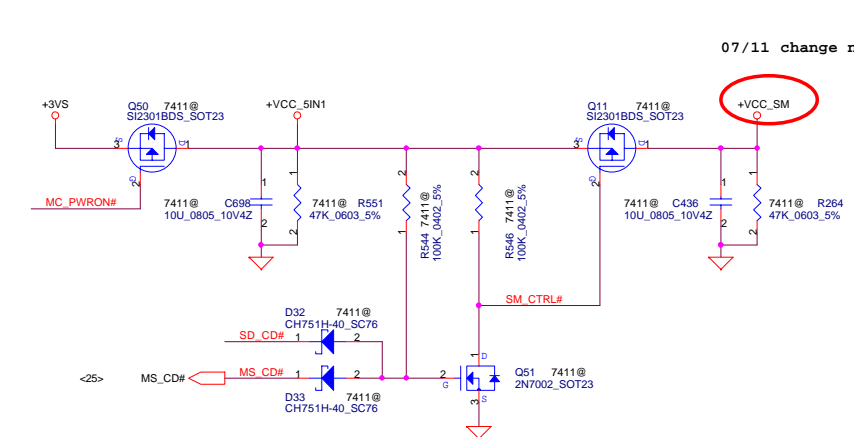
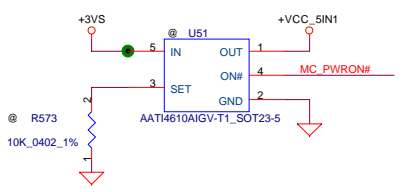
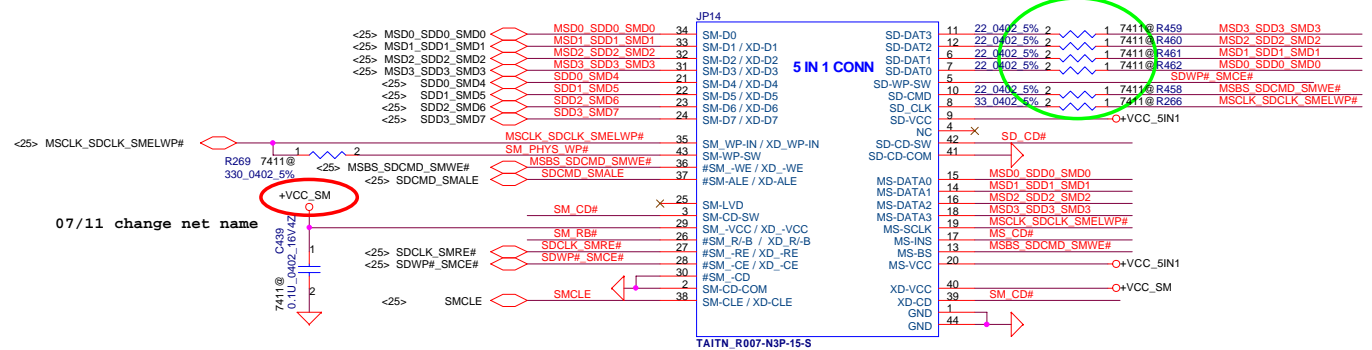
when VR\_EN# is low, internal regulator is activated

put C445 as close to controller as possible

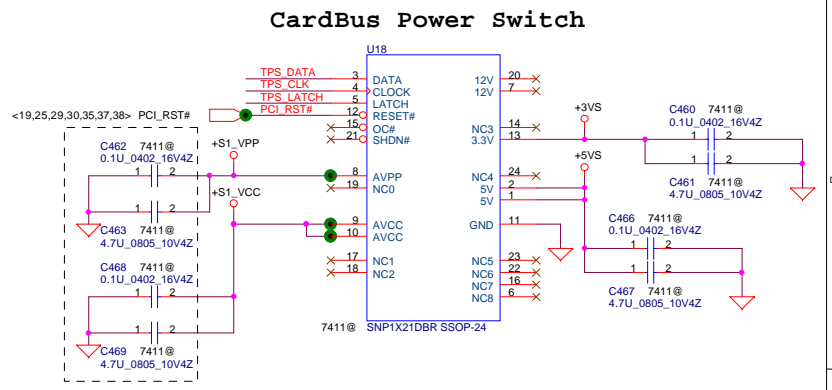
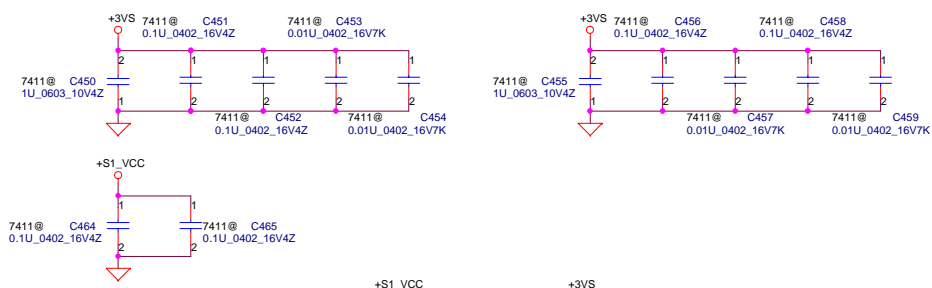
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	PCI7411(1/3)	
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Size	Document Number	Rev			
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Date	Tuesday, August 30, 2005	Sheet	25	of	53



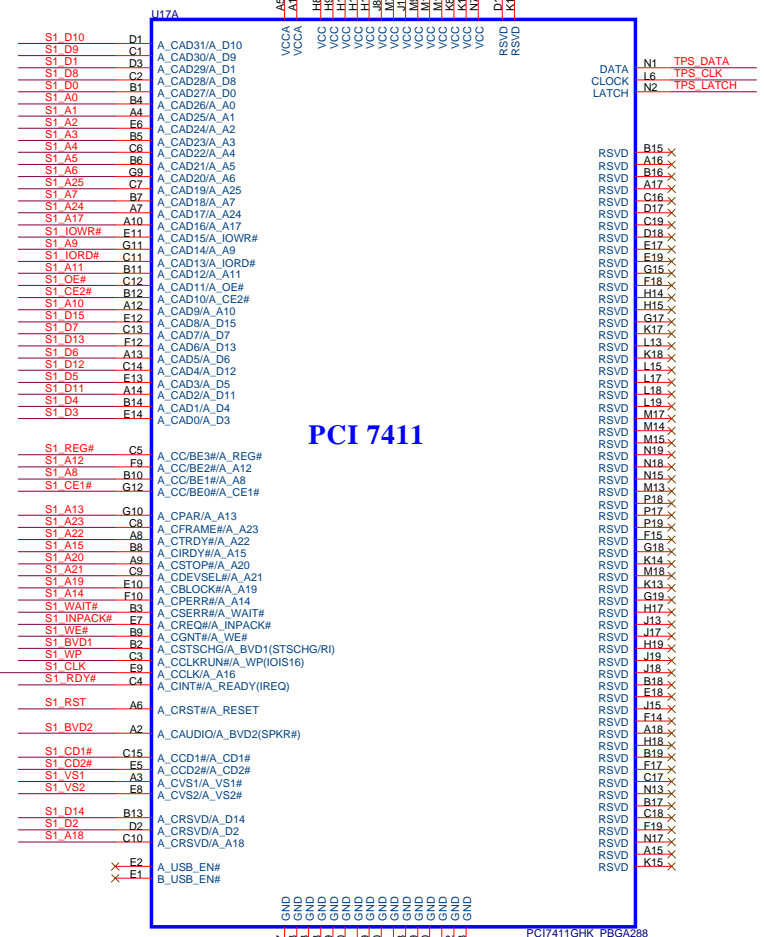
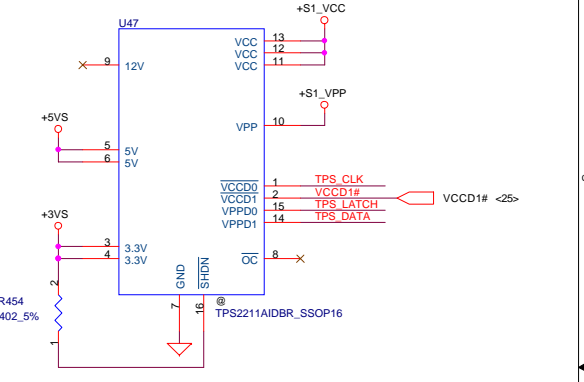
8/23 Relocate Damping resistor to solve Sandisk Card issue



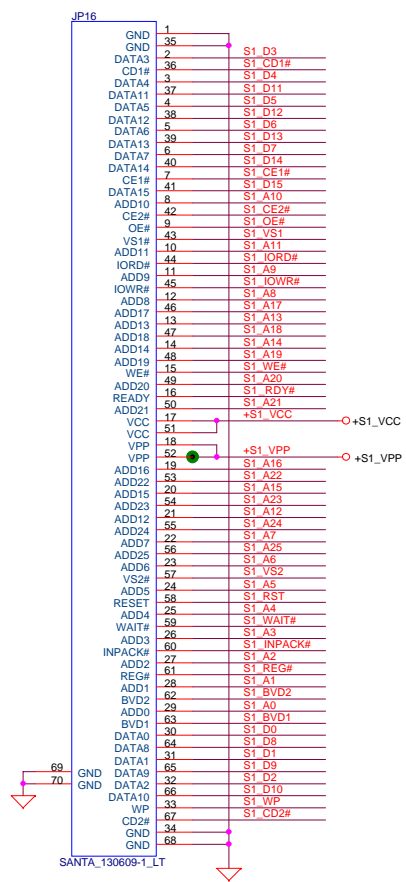
Security Classification	Compal Secret Data			Title	PCI7411(2/3)		
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Size	Document Number	Rev	
				Custom	LA-2771	0.8	
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close to card bus conn



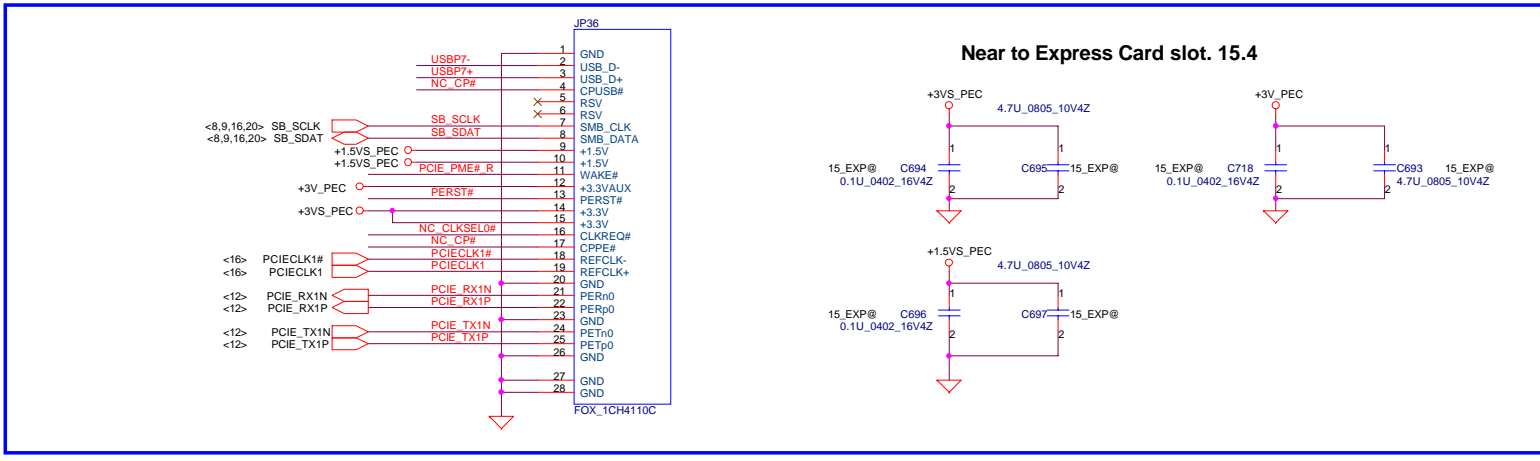
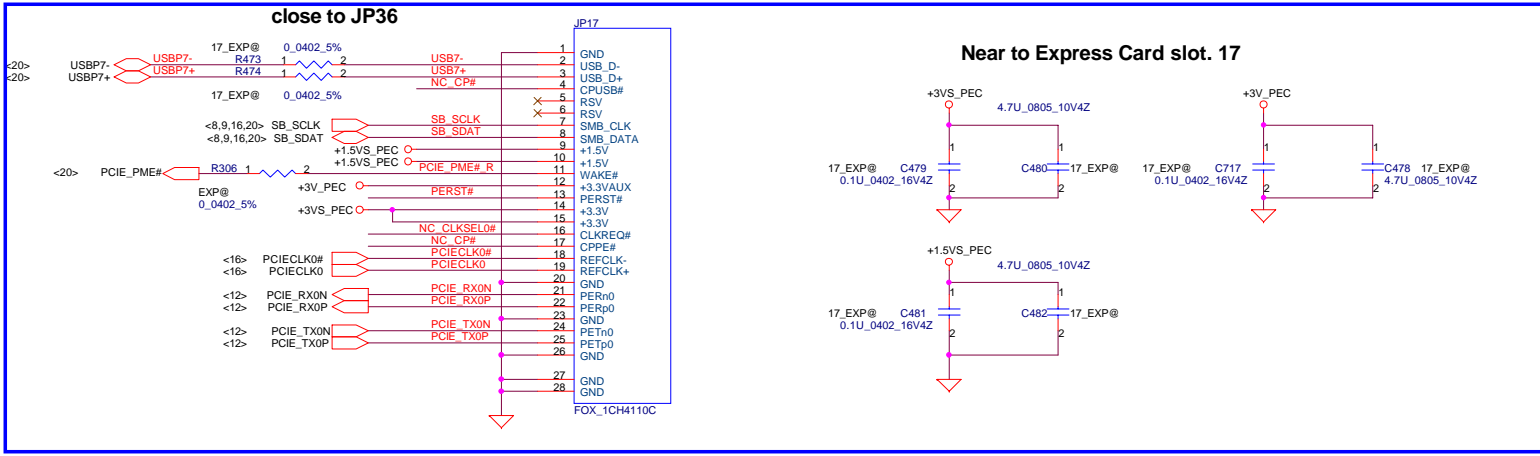
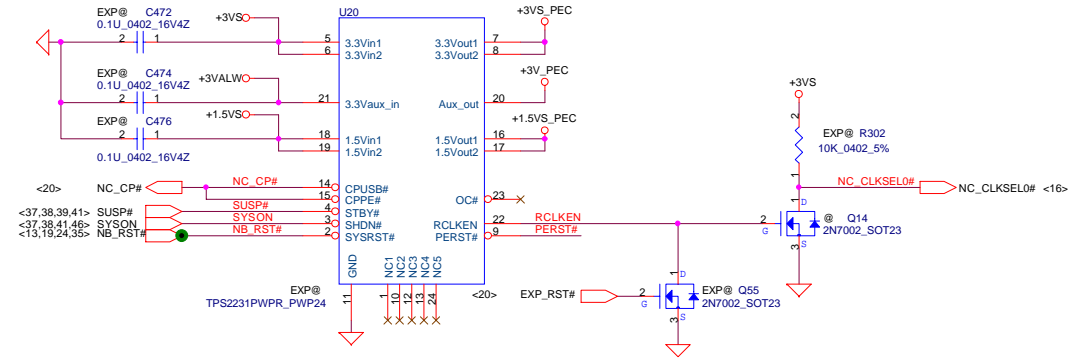
PCI 7411



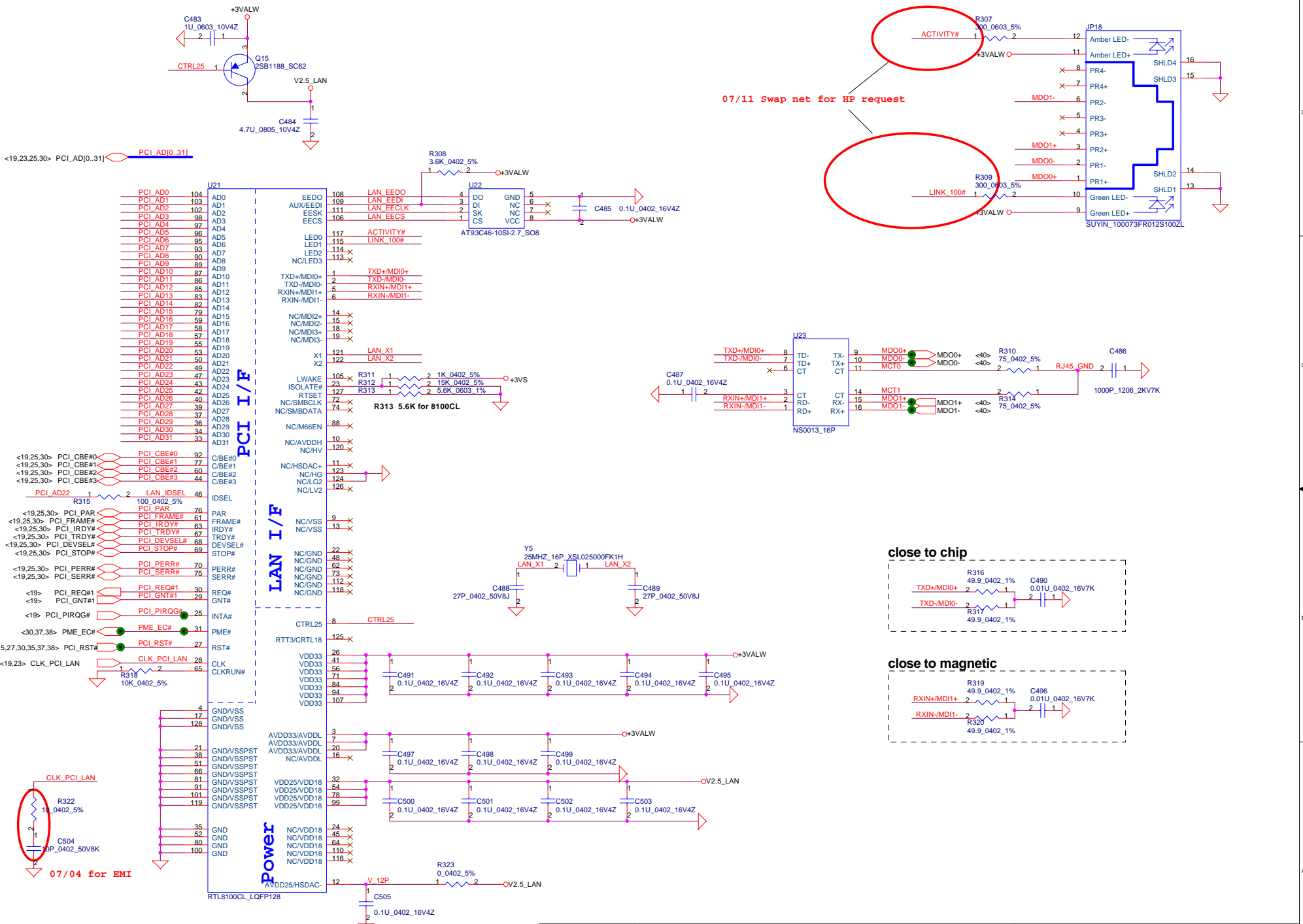
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Issued Date	2005/03/01	Deciphered Date	2005/04/06
			PCI7411(3/3)
Size	Document Number	Rev	
Custom	LA-2771	0.8	
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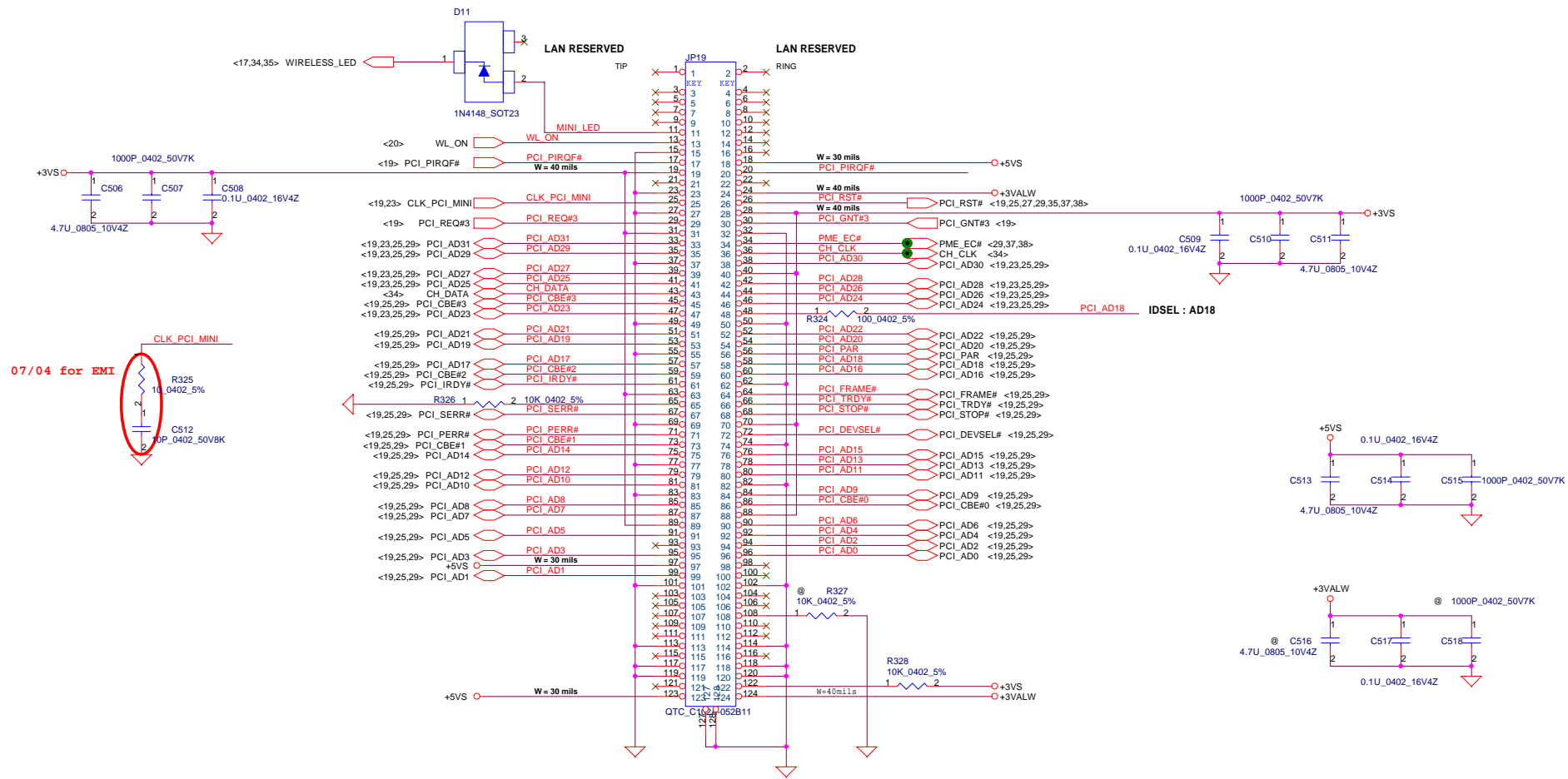
# Express Card Power Switch



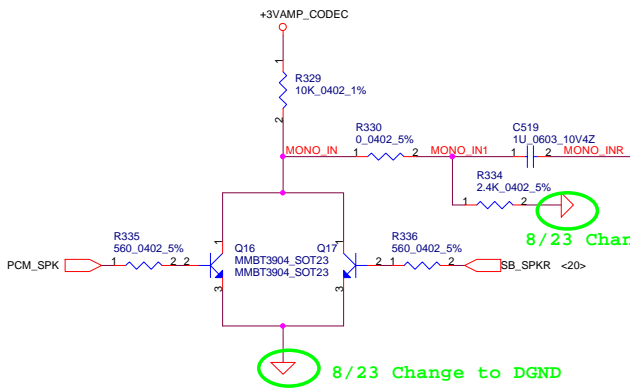
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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Express Card	
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Customer	Document Number		LA-2771	0.8	
Date	Tuesday, August 30, 2005	Sheet	28	of	53



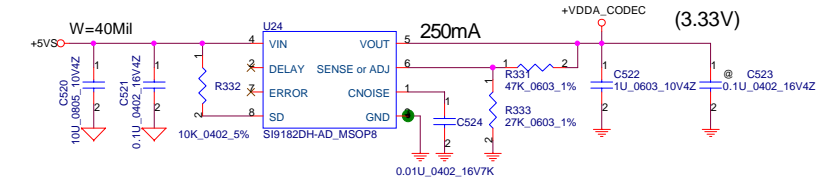
Security Classification	Compal Secret Data		Title	LAN-8100CL	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Size	Document Number
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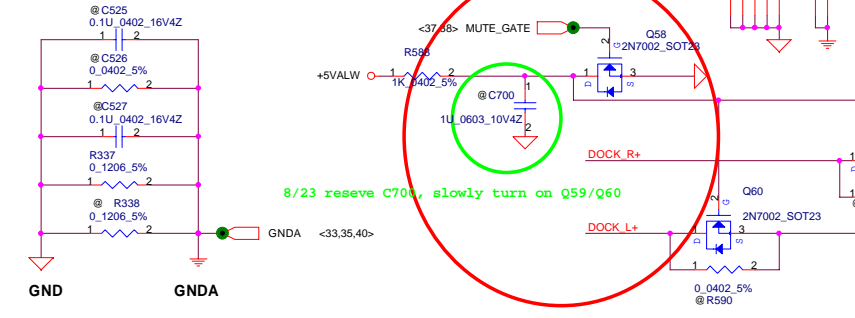
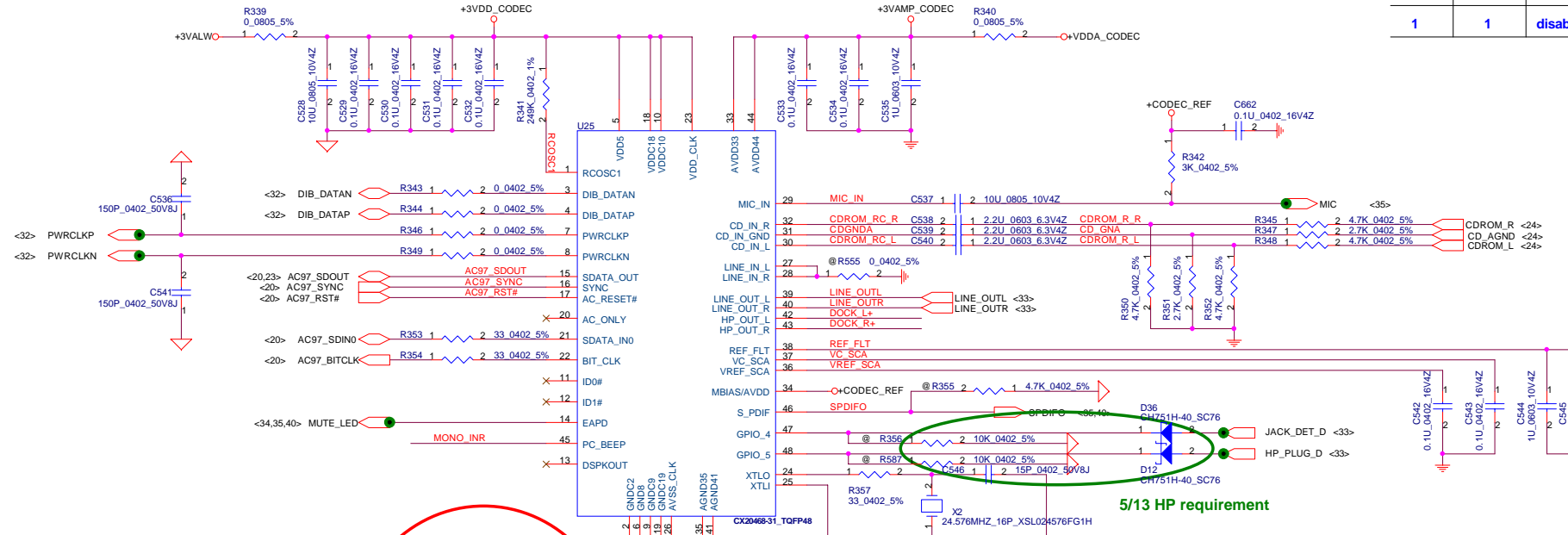
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Issued Date	2005/03/01	Deciphered Date	2005/04/06
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For Layout:  
Place decoupling caps near the power pins near the SmartAMC device.



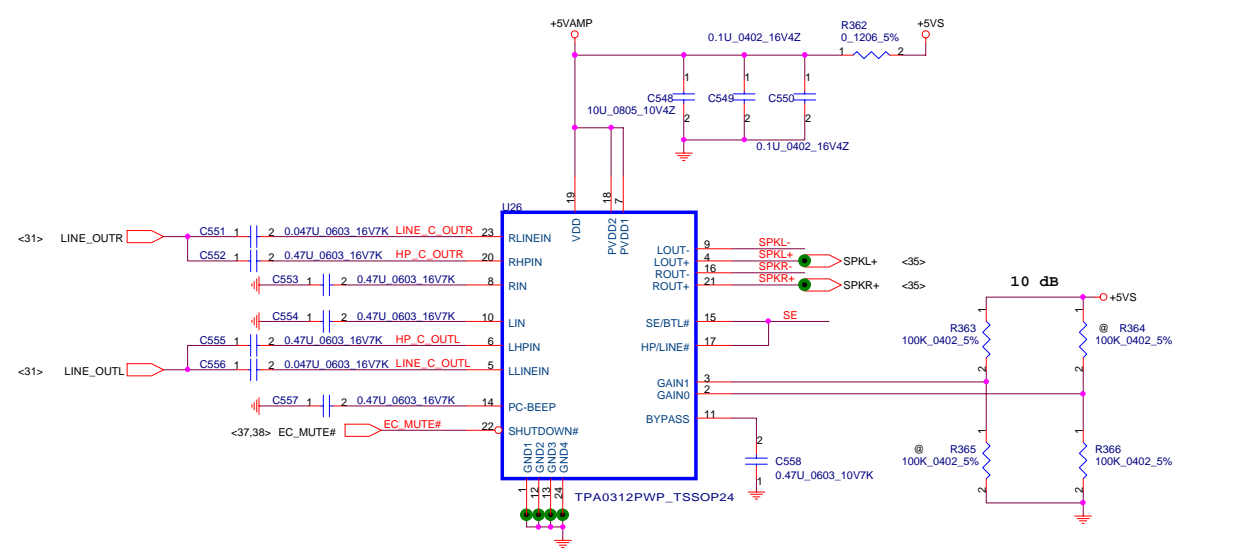
GPIO4	GPIO5	
0	0	disable HP-out
0	1	disable EQ/HP-out(sys HP only)
1	0	enable HP-out
1	1	disable EQ/HP-Out(sys HP only)



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			Rev: 0.8 Sheet 31 of 53

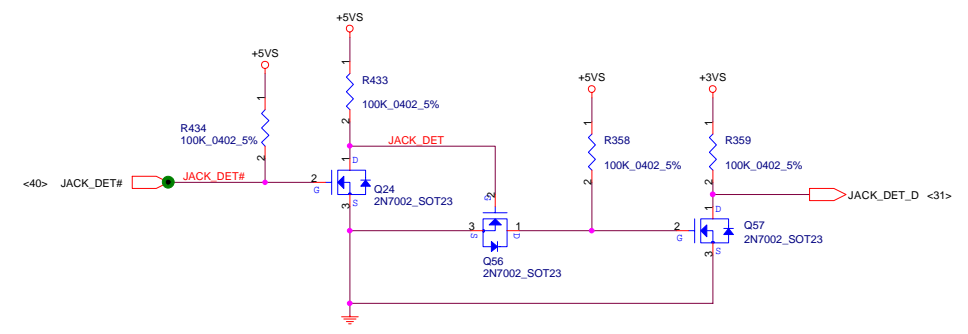
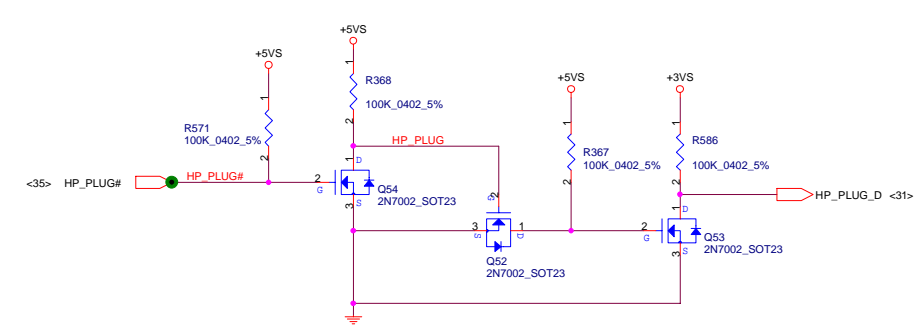
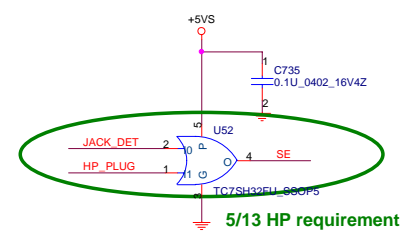
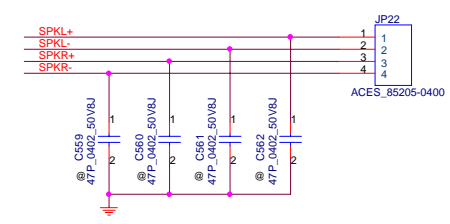
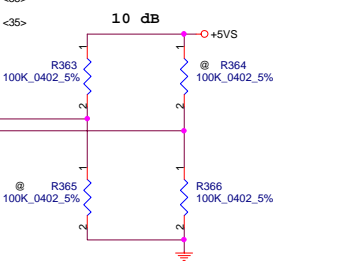




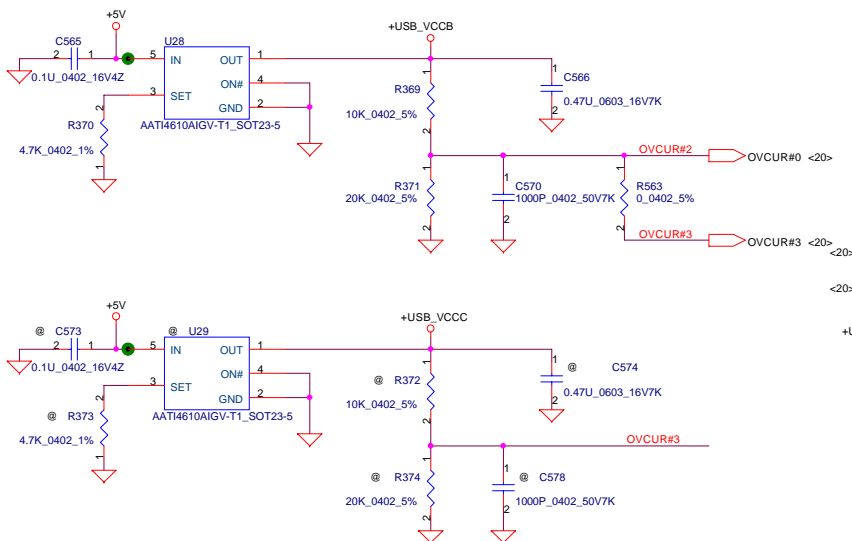


HEADPHONE OUT/LINE OUT

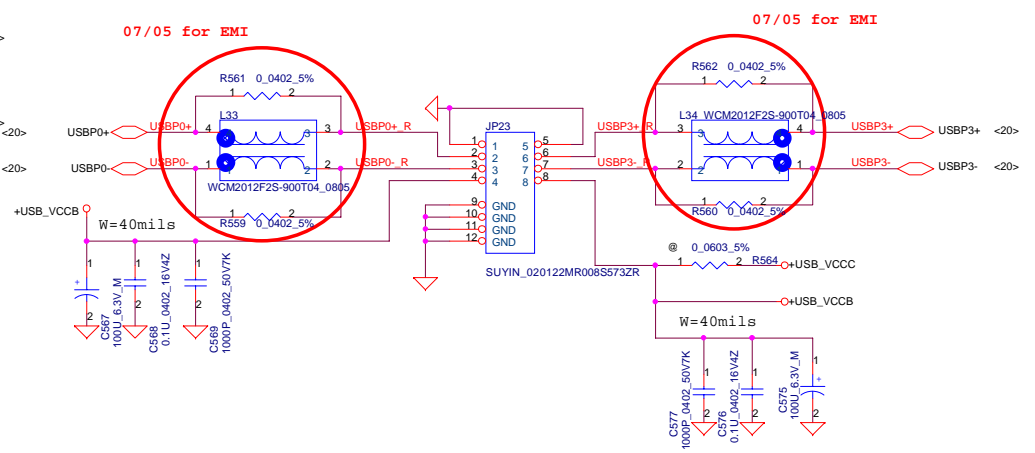
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



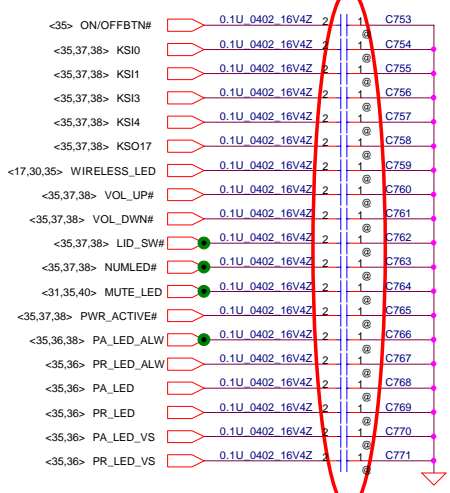
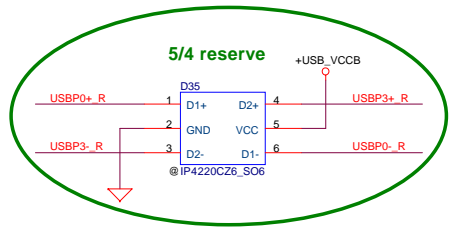
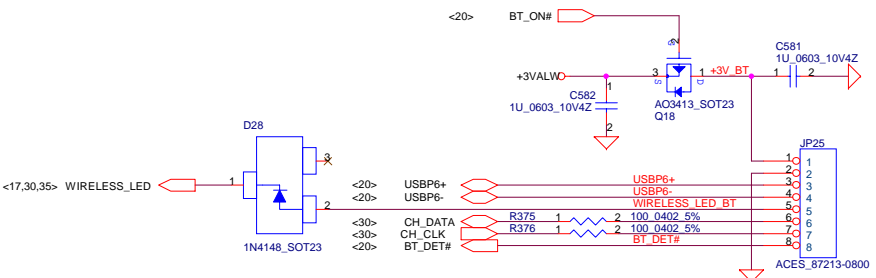
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	AMP & Audio jack	
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### USB CONNECTOR 0/3 (Left side)



### BT CONNECTOR



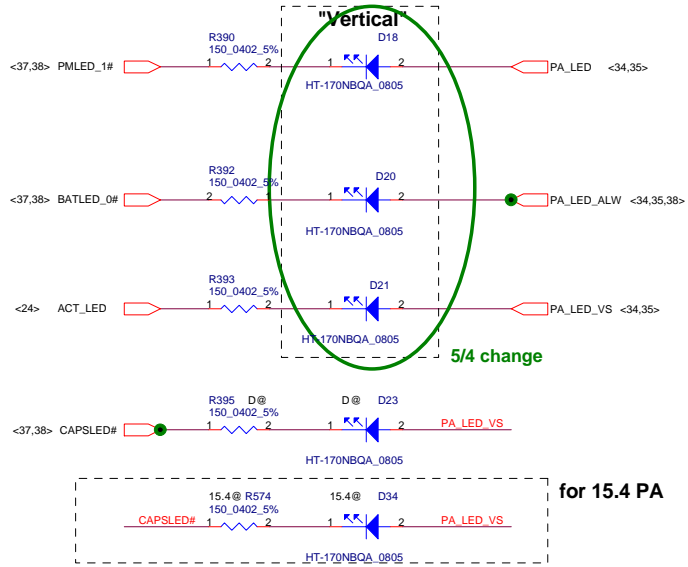
2005.08.11 for EMI solution

Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Bluetooth & USB CONN
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Date: Tuesday, August 30, 2005			Sheet 34 of 53	Rev 0.8 Document Number LA-2771



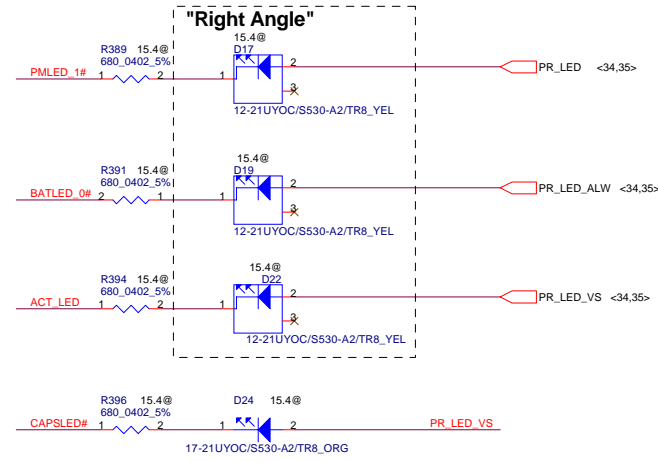
For PA

FOR POWER BUTTON BACKLIGHT SYSTEM POWER

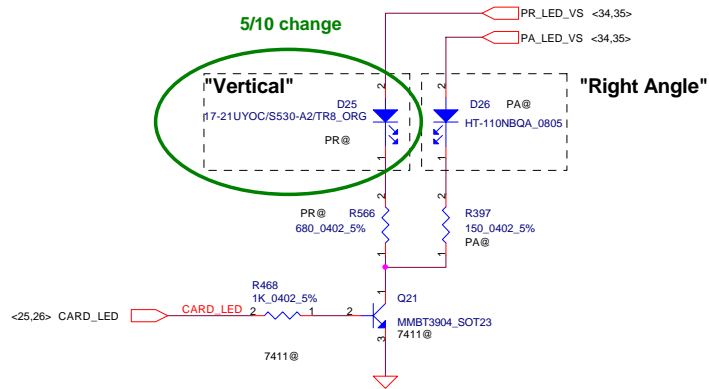


For PR

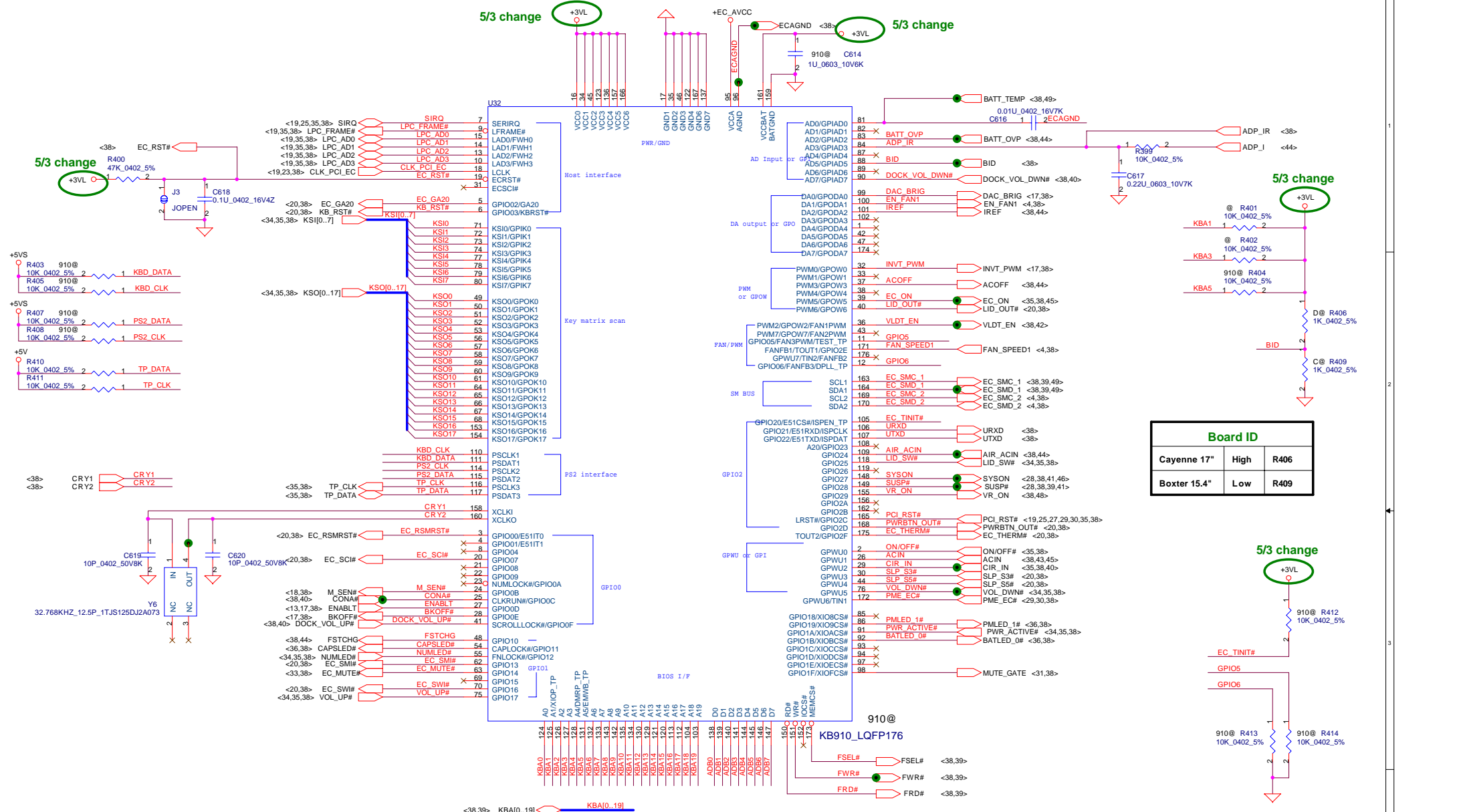
FOR POWER BUTTON BACKLIGHT SYSTEM POWER



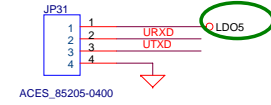
5/10 change



Security Classification	Compal Secret Data			Title		
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**EC DEBUG port** 6/27 change

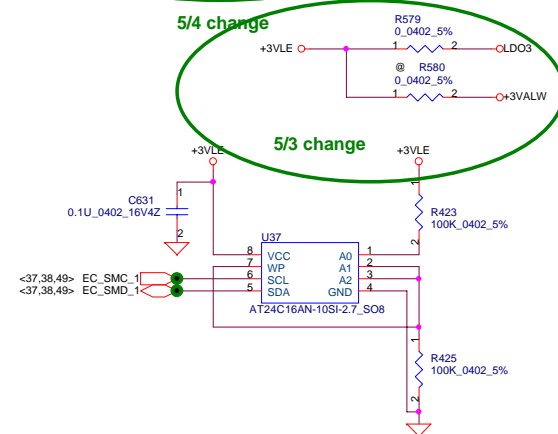
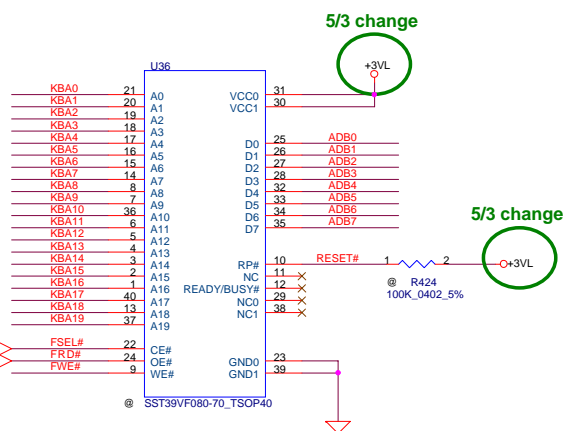
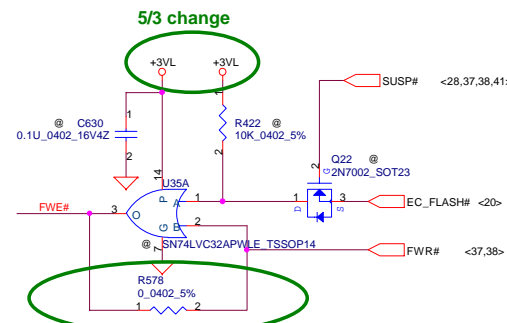
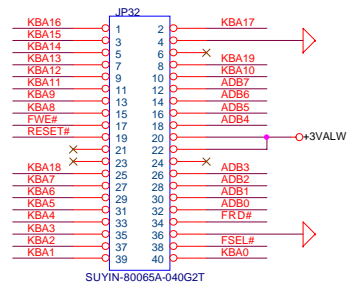
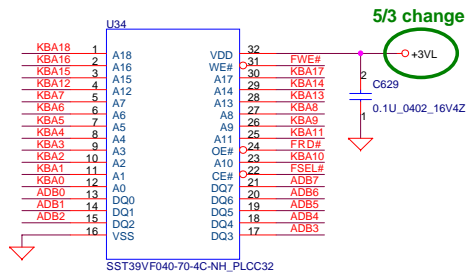


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EC KB910			
Size	Document Number	Rev	
Custom	LA-2771	0.8	
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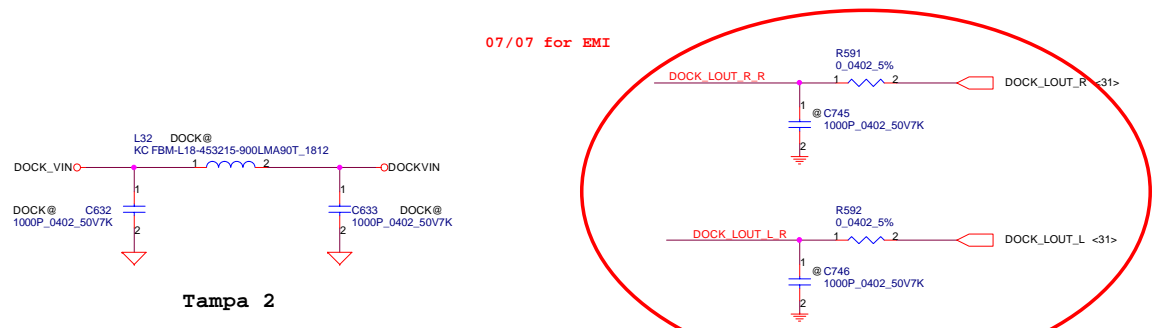
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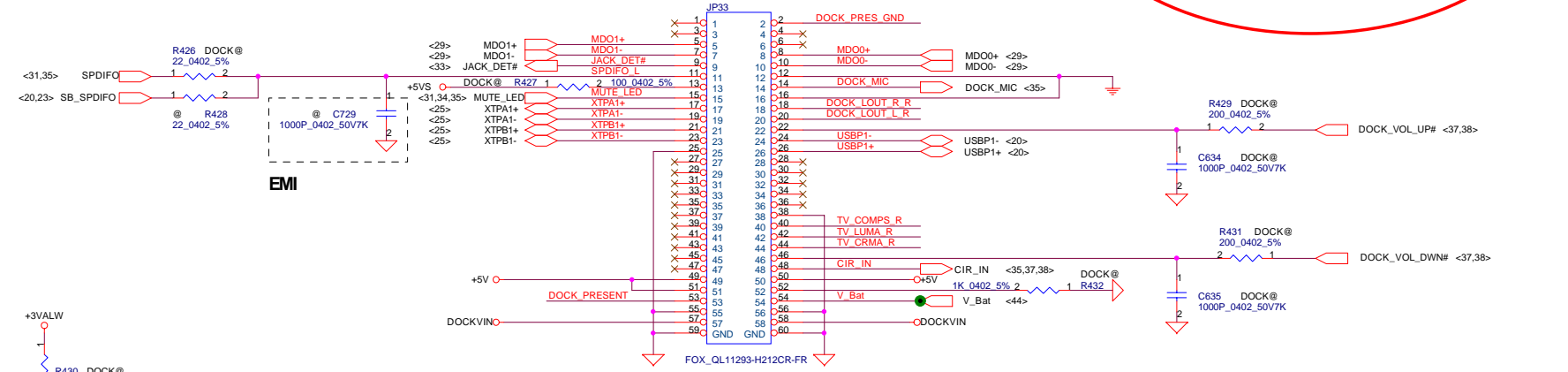
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 <37,38> KBA[0..19]  KBA[0..19]



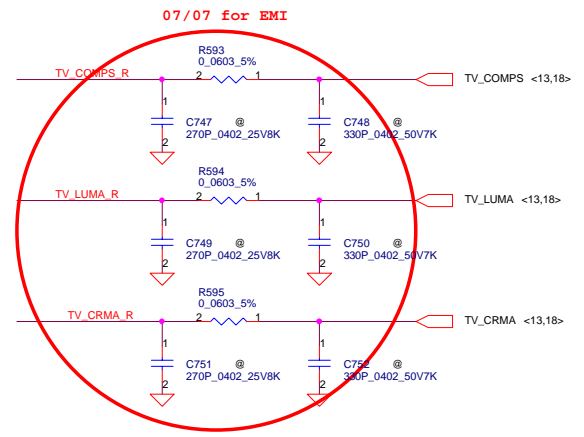
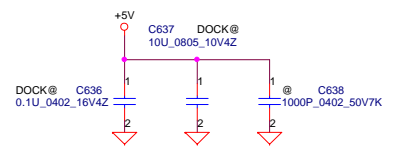
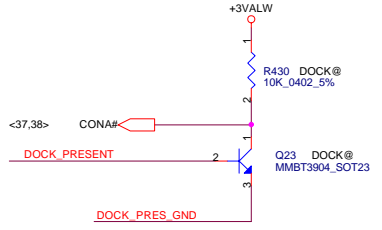
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Tampa 2

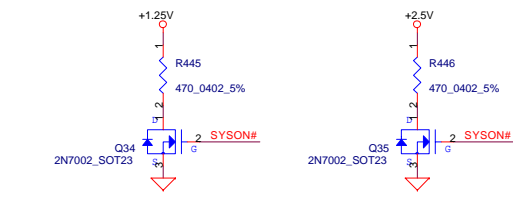
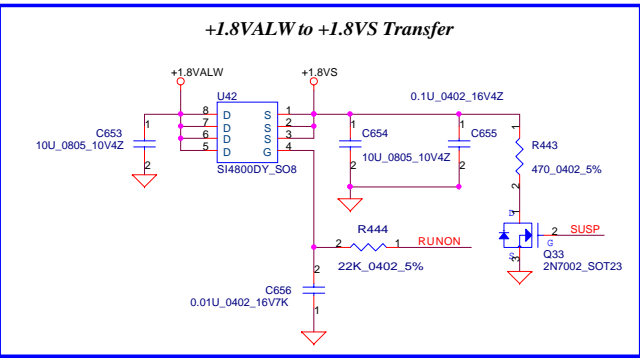
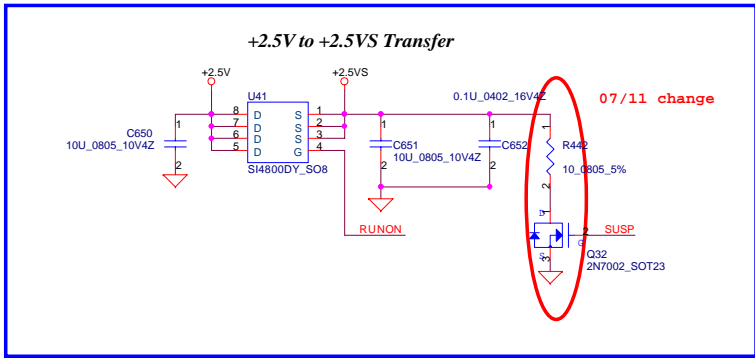
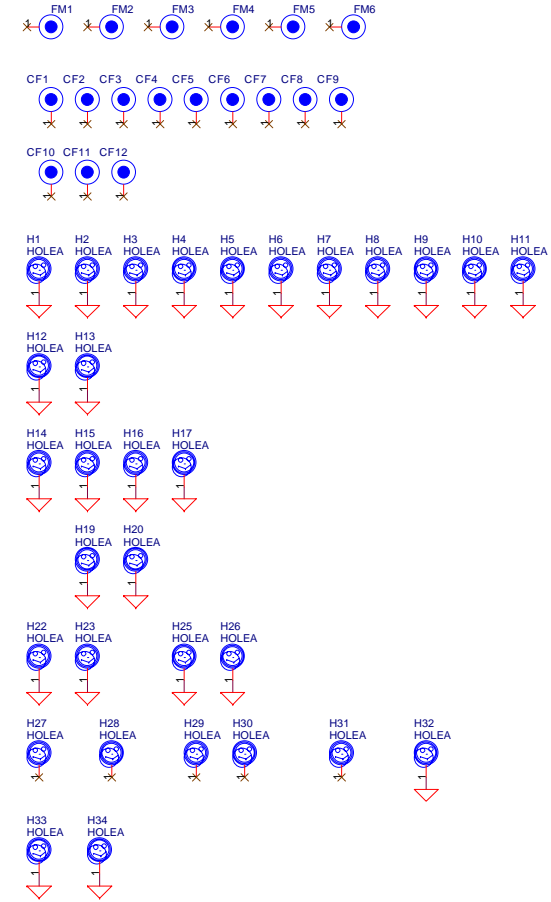
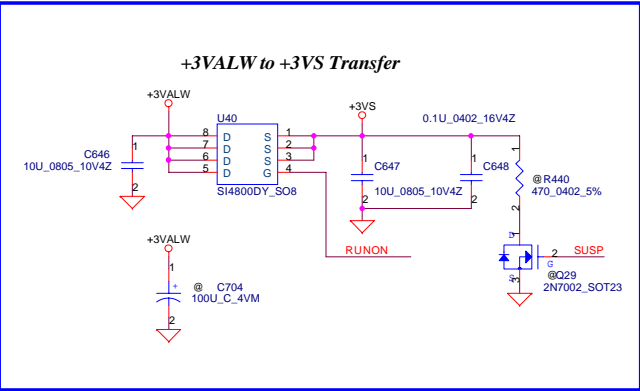
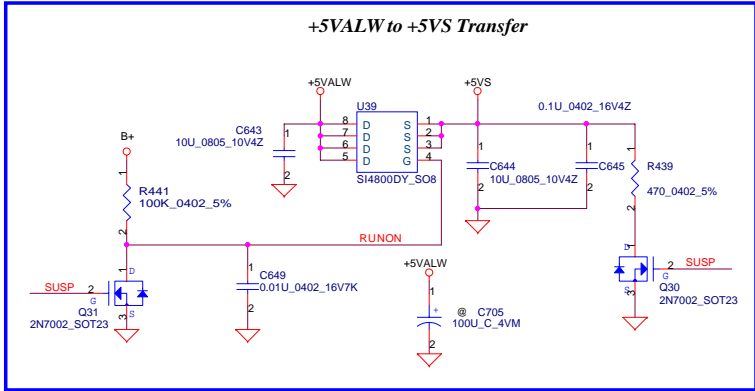
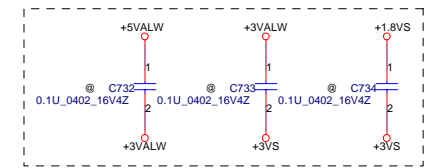
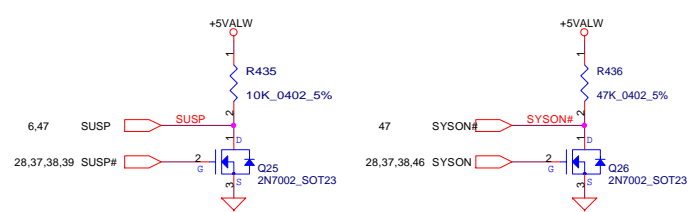
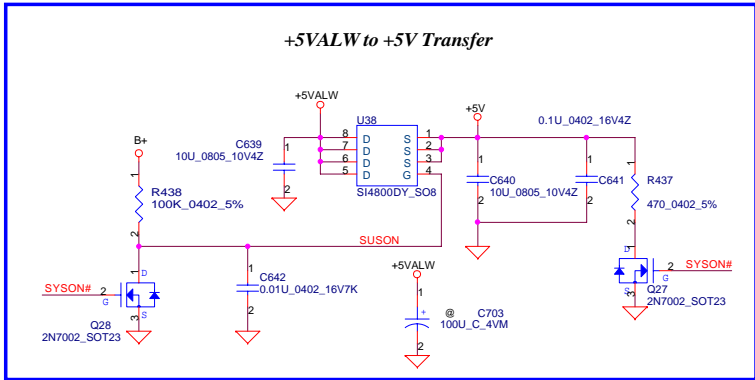


EMI

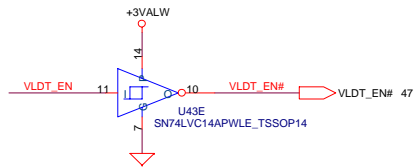
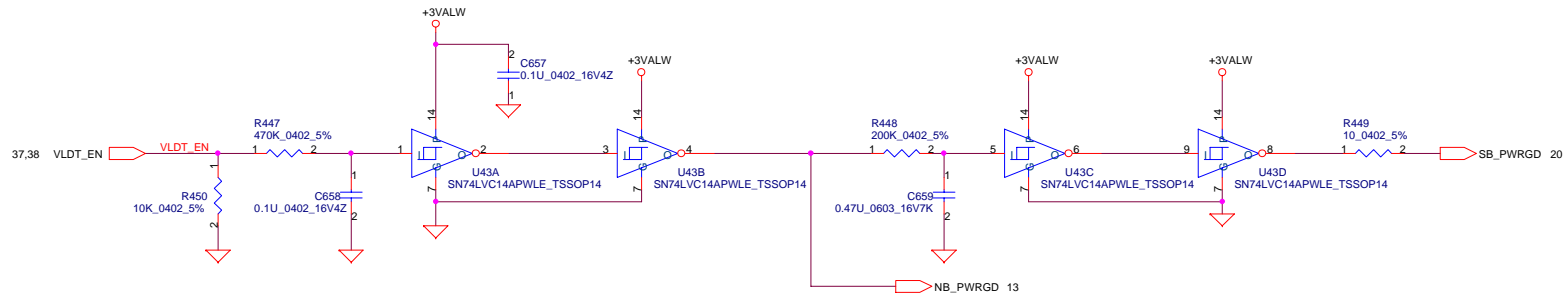


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				Custom	LA-2771
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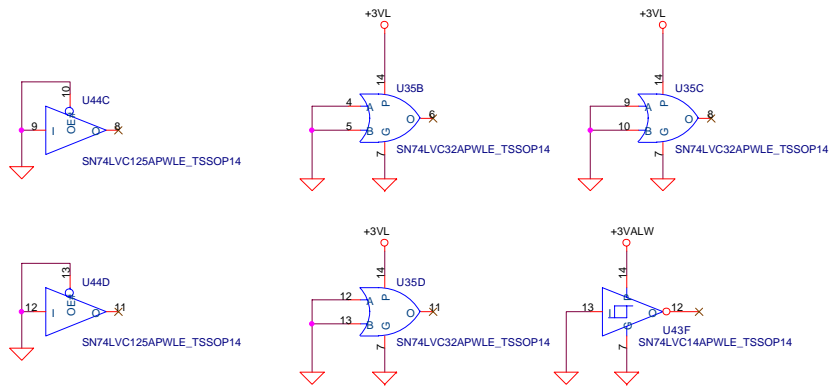
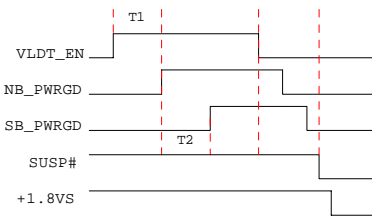




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note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,  
SUSP# goes to low after SB\_PWRGD goes to low for power  
down.



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				Date	Tuesday, August 30, 2005	Sheet

# Detector

**Vin Detector : Cayenne**

18.234	17.841	17.449
17.597	17.210	16.813

**Vin Detector : Boxster**

14.352	13.950	13.555
13.818	13.411	13.000

8/29 Change to 0.022uF for AC Off issue

**Cayenne : PR5=22K; PR6=19.6K**

**Boxster : PR5=47K; PR6=27K**

<44> ACON

**ACIN : Cayenne**

**Precharge detector**

14.805	14.333	13.872
13.355	12.933	12.465

**ACIN : Boxster**

**Precharge detector**

12.384	12.000	11.624
10.927	10.600	10.223

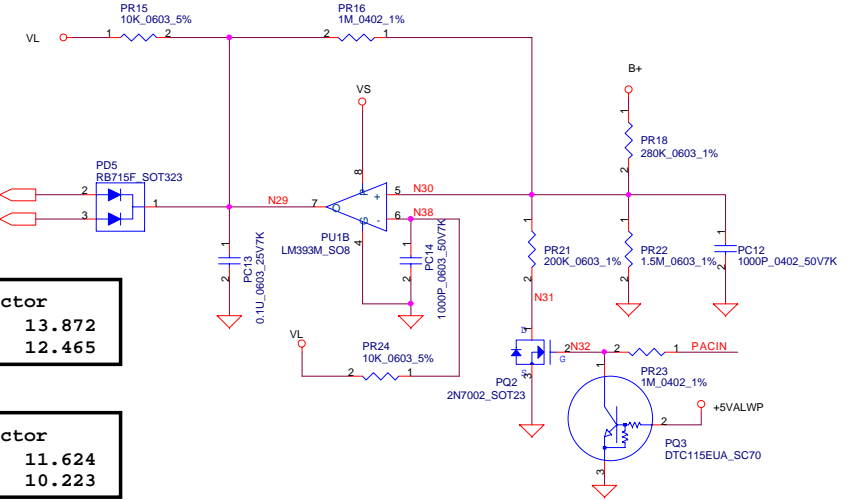
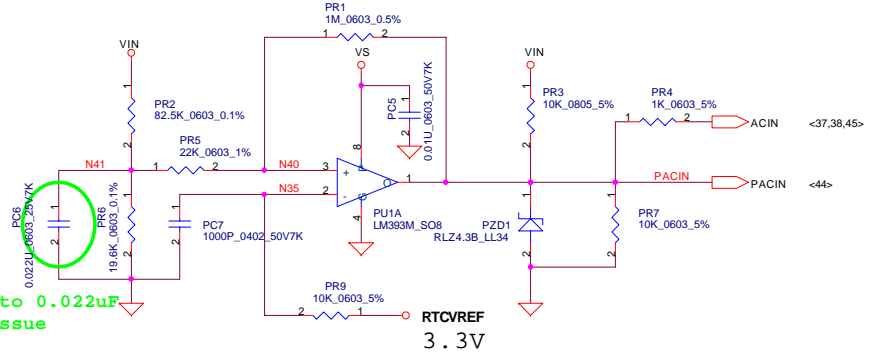
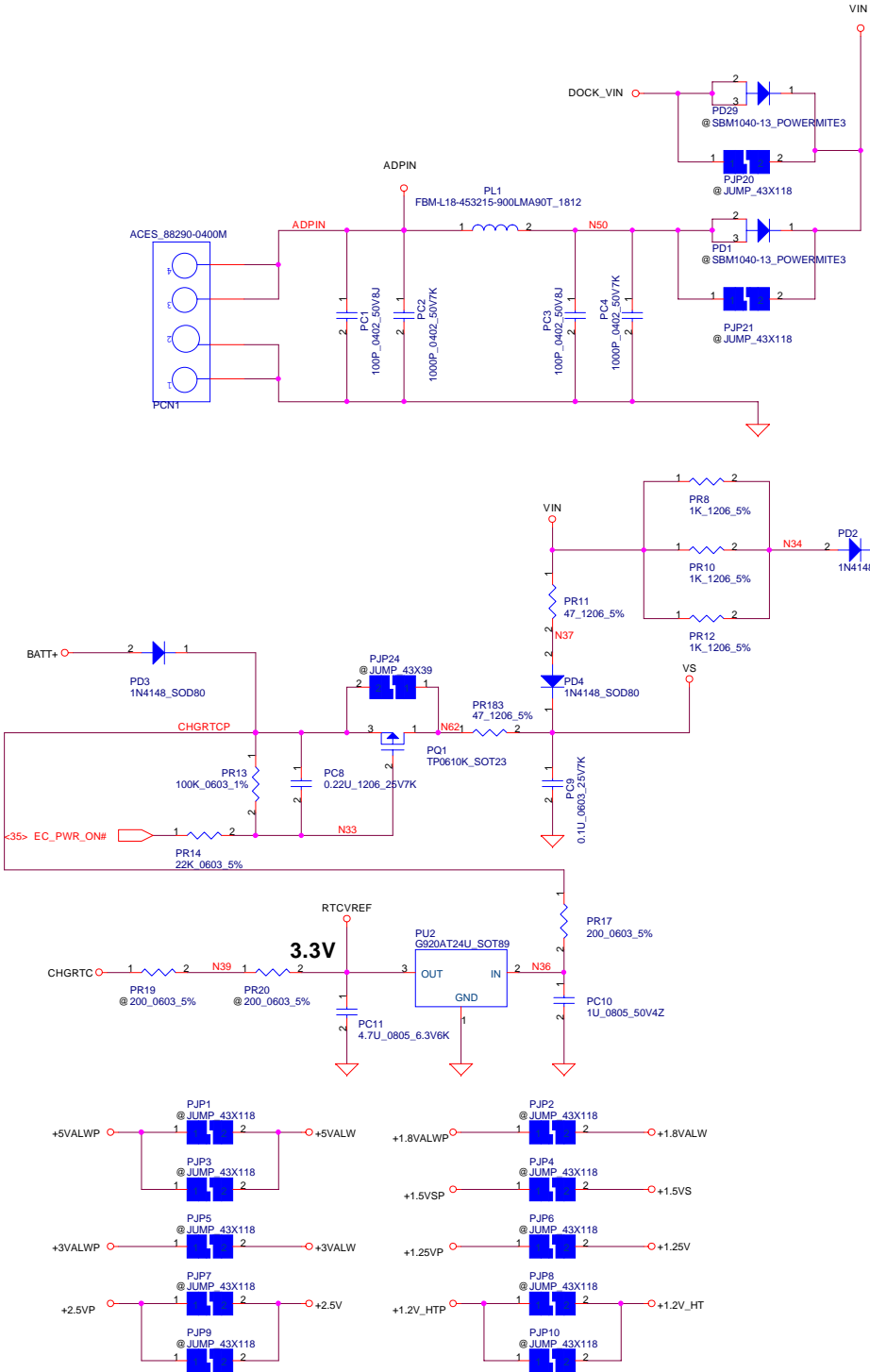
**BATT**

**Detector**

7.558	7.333	7.112
6.108	5.933	5.704

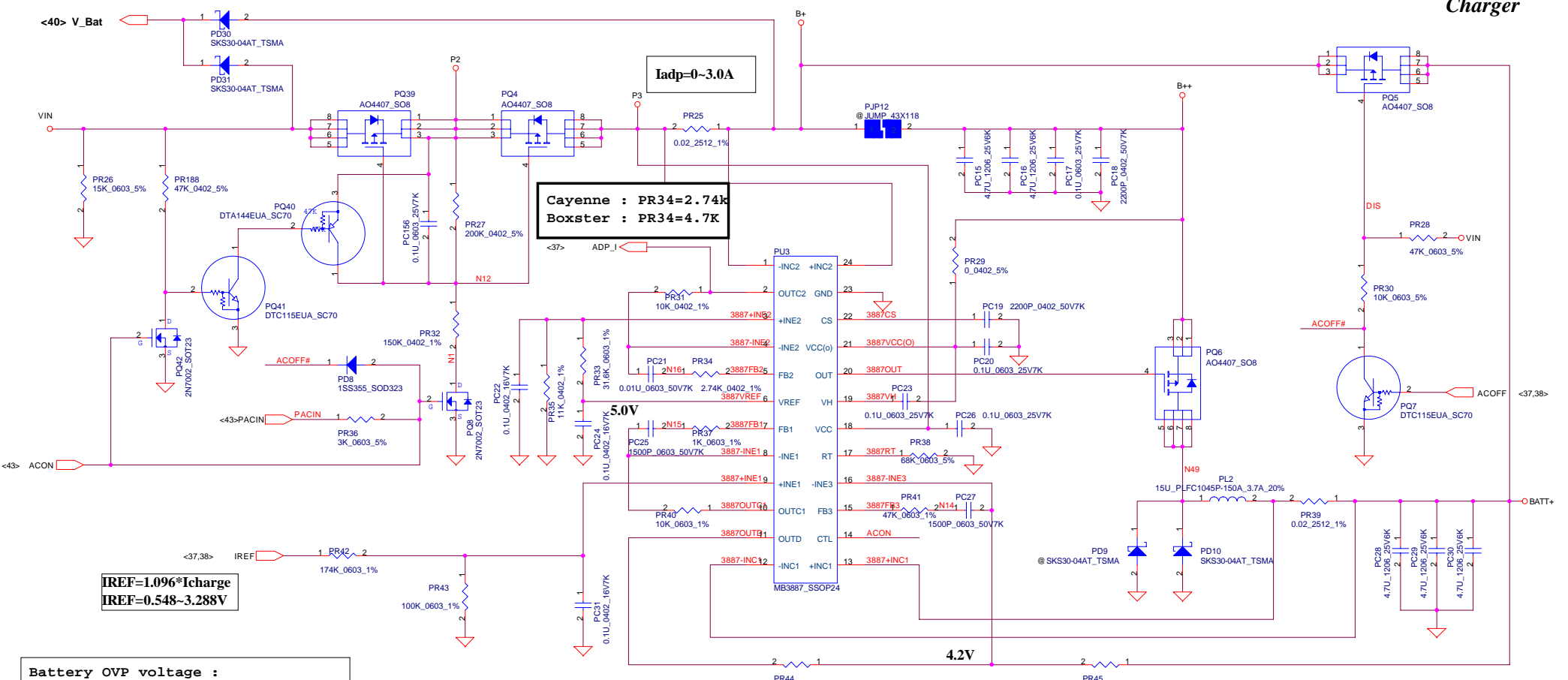
**Cayenne : PR21=200K**

**Boxster : PR21=300K**



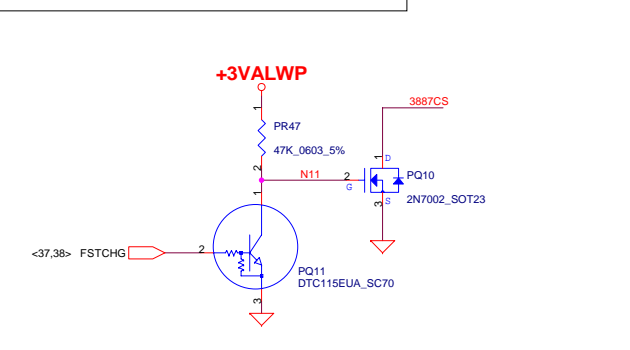
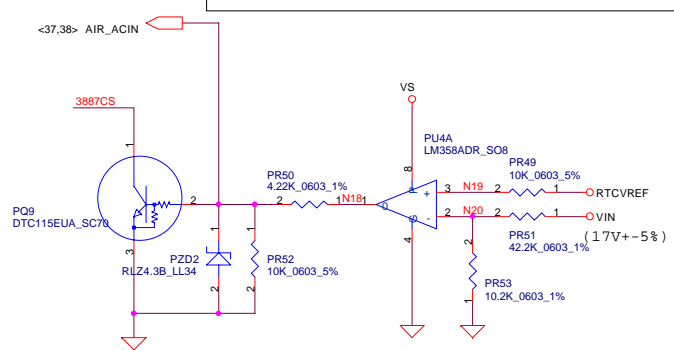
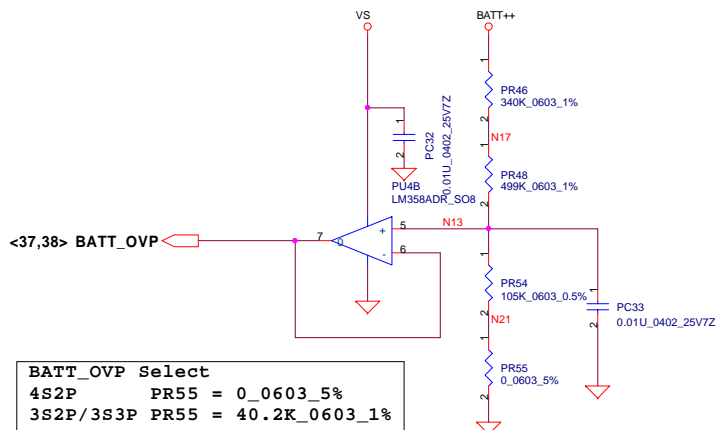
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# Charger



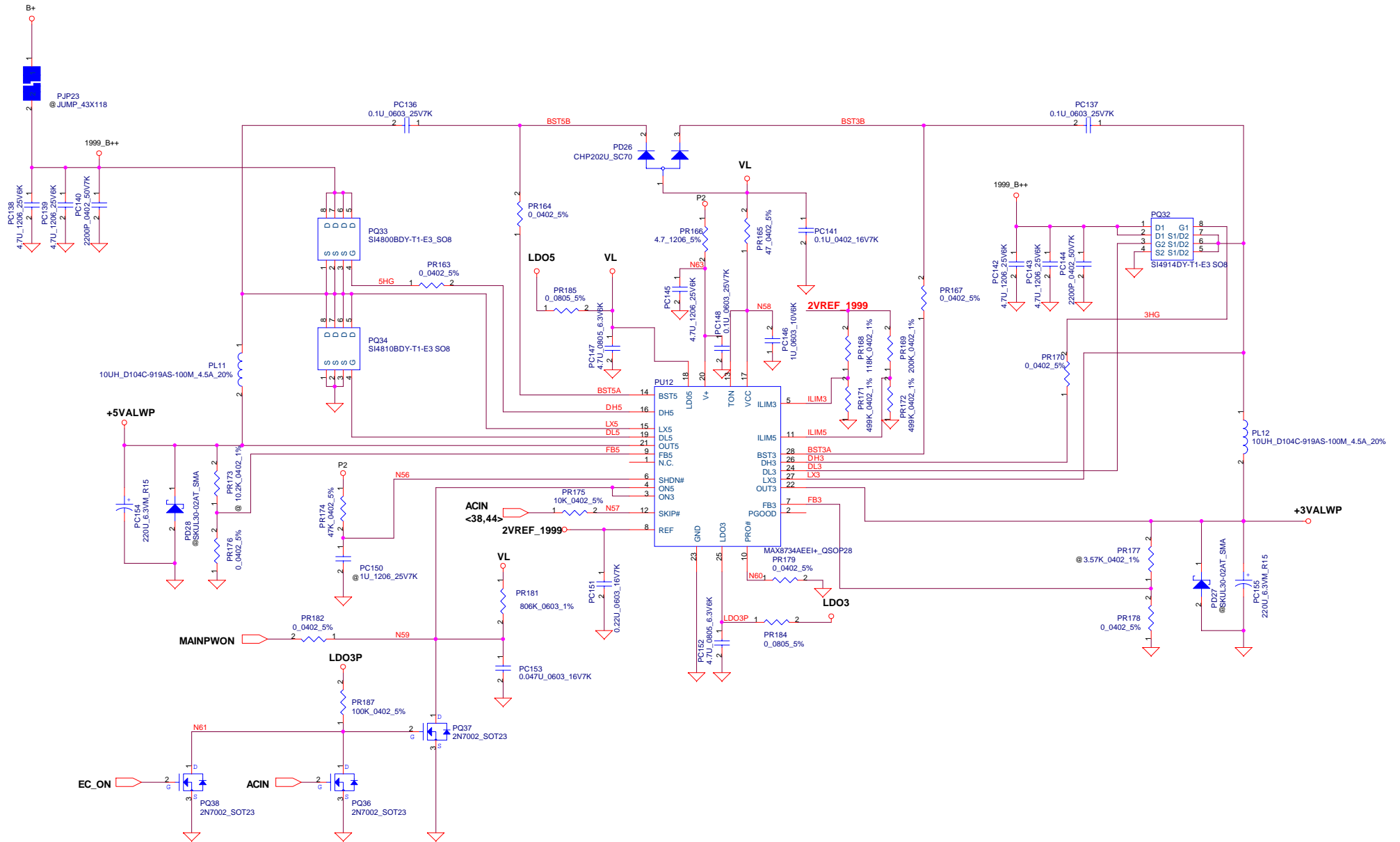
**Battery OVP voltage :**  
4S2P : 18V--> BATT\_OVP= 2.0V  
(BAT\_OVP=0.1112\*V<sub>MB</sub>)  
3S2P/3S3P : 13.5V--> BATT\_OVP= 2.0V  
(BAT\_OVP=0.14753 \*BATT+)

**CC=0.4~3.0A**  
**BATT\_Charge Voltage Select**  
4S2P CV=16.8V PR44 = 49.9K\_0603\_0.1% PR45=150K\_0603\_0.1%  
3S2P/3S3P CV=12.6V PR44 = 150K\_0603\_0.1% PR45=300K\_0603\_0.1%



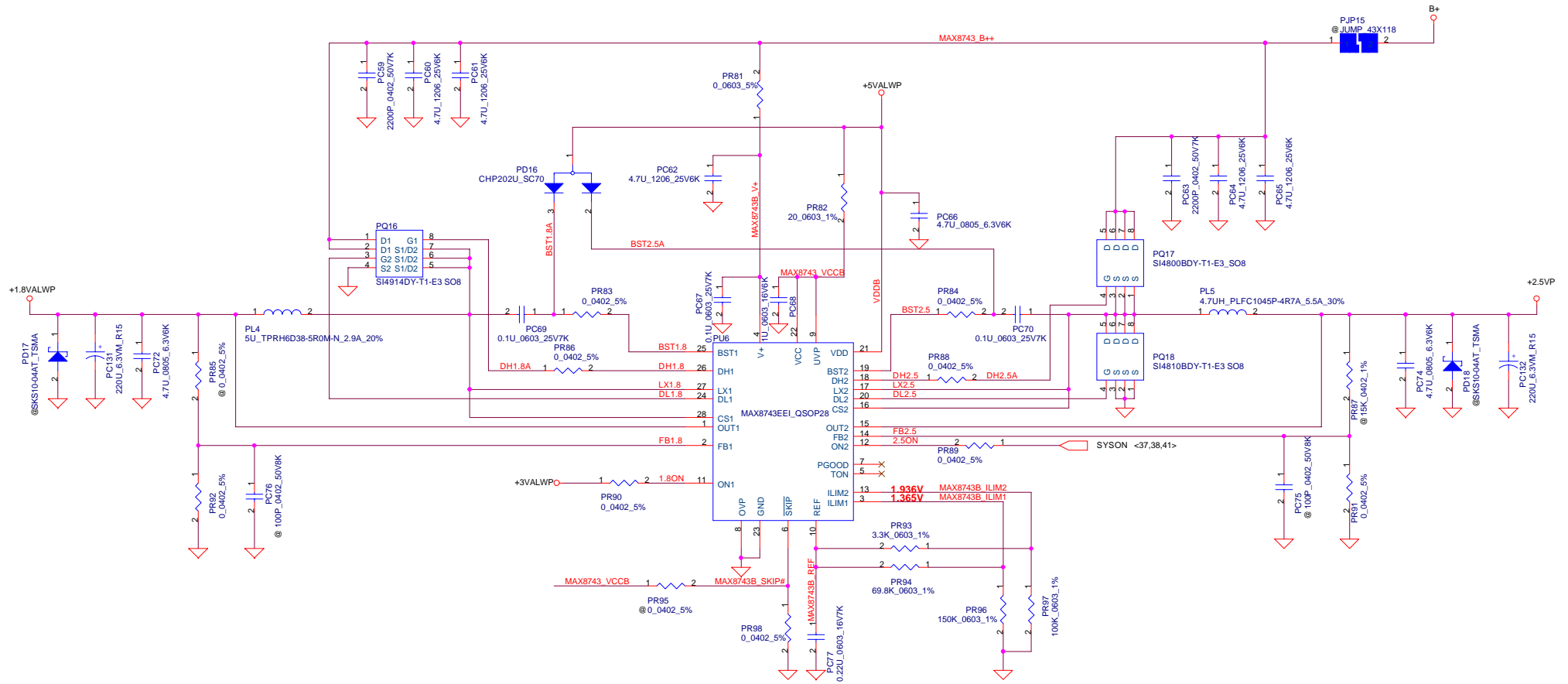
Security Classification	Compal Secret Data			Title	<b>Charger</b>	
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# +3VALWP/+5VALWP



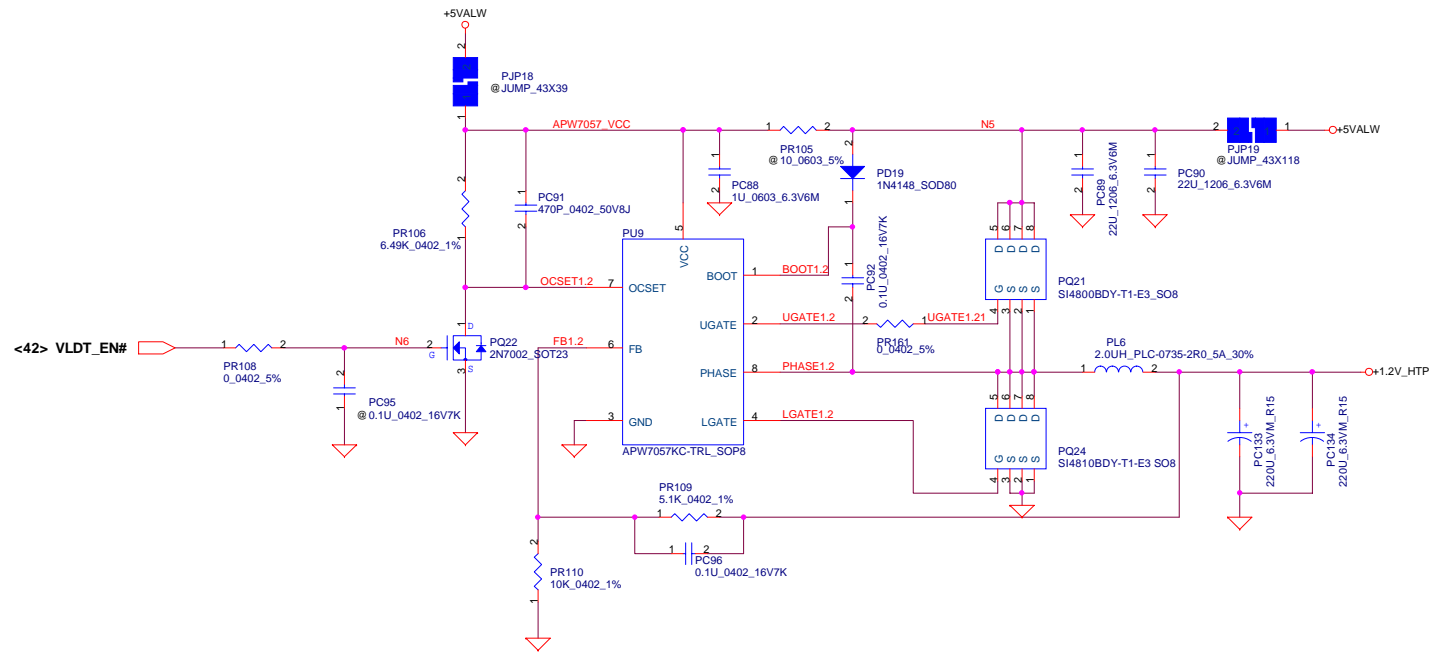
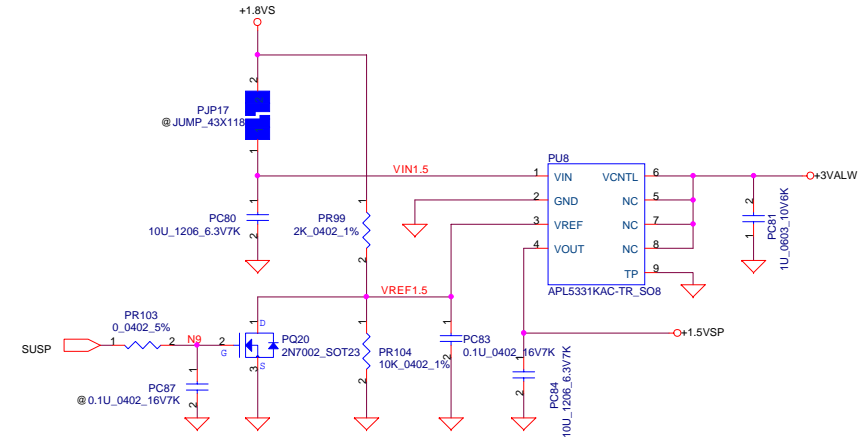
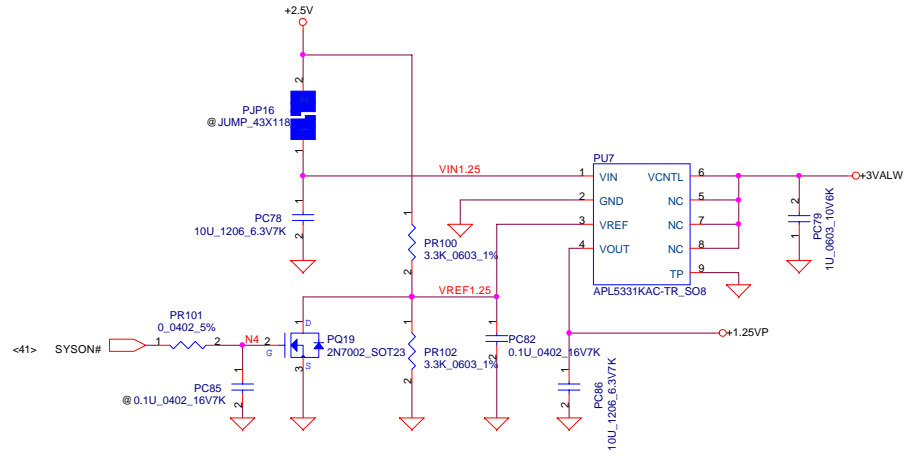
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Title			<b>+ 3VALWP / + 5VALWP</b>	
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**+1.8VALWP/+2.5VP**

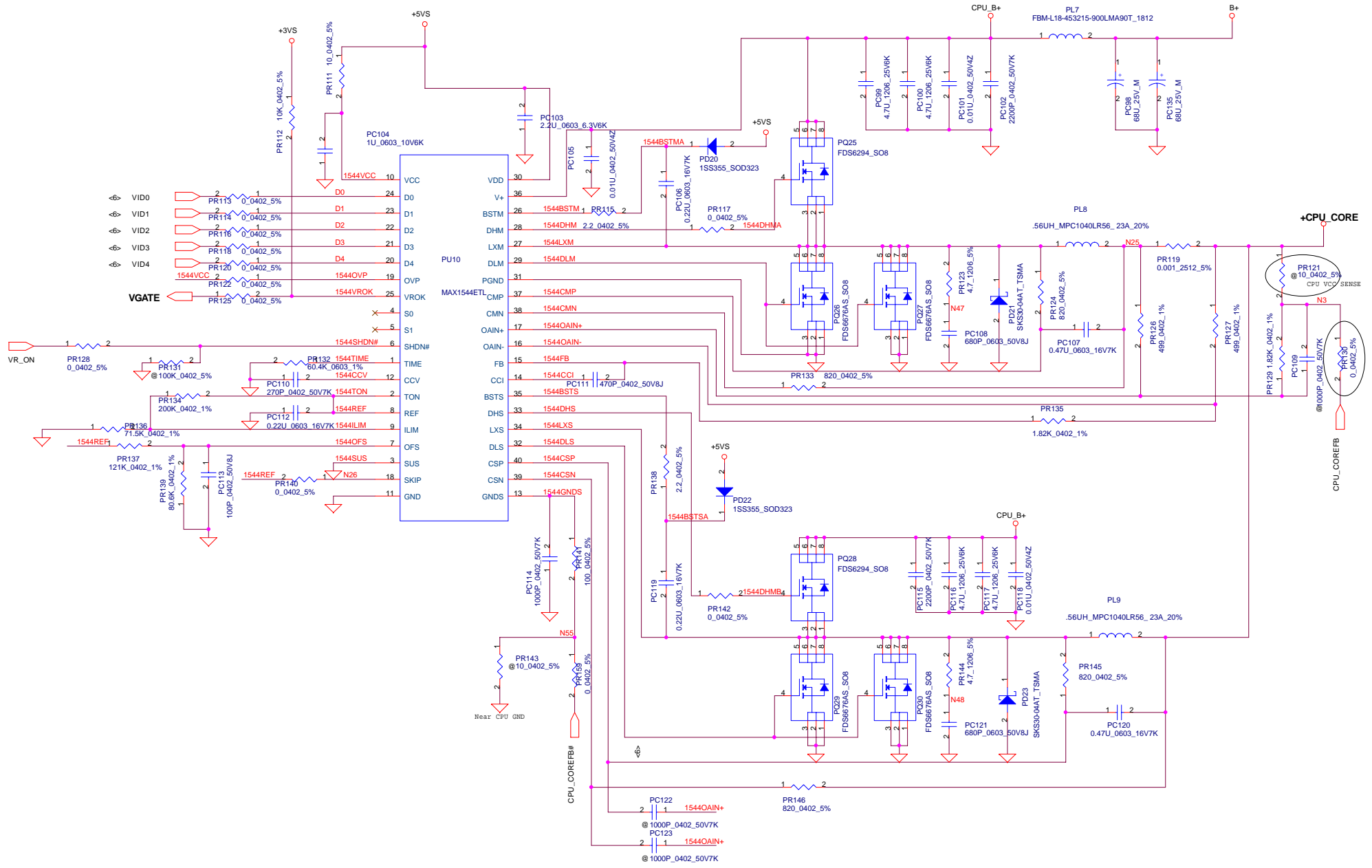


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**+1.2V\_HTP/+1.5VSP/+1.25VP**



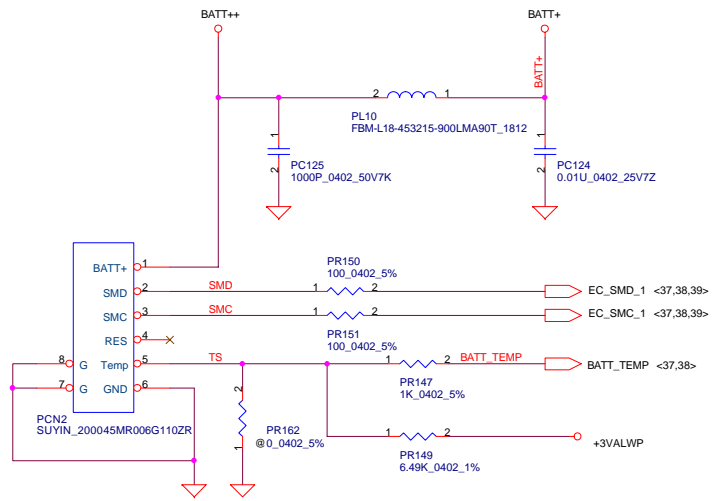
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Title	<b>+1.2VSP/+1.5VP/+1.25VSP</b>		
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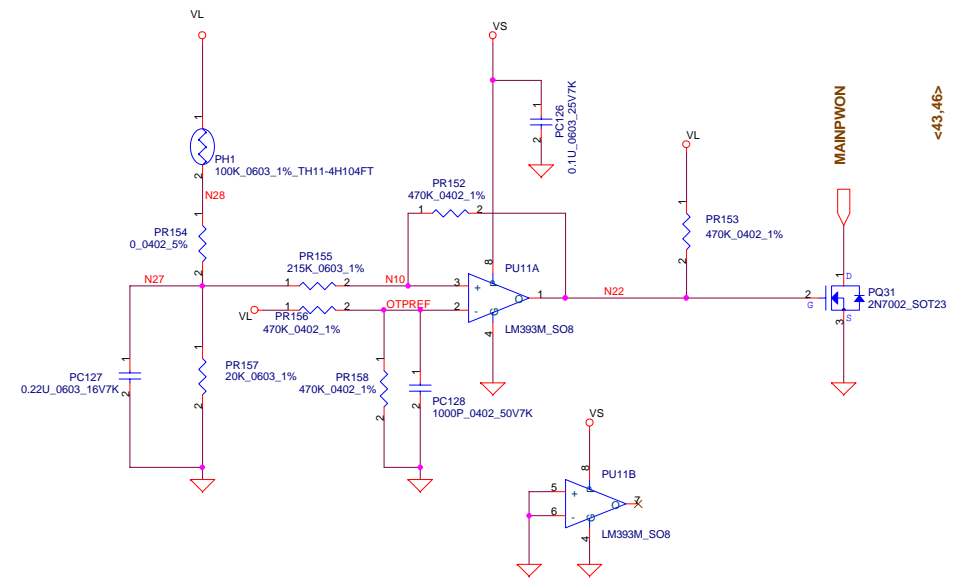
# Battery Connect/OTP



**PJPB1 battery connector**  
**SMART Battery:**  
**1. BATT +**  
**2. SMD**  
**3. SMC**  
**4. Res**  
**5. Temp**  
**6. GND**

CPU

**PH1 under CPU bottom side :**  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 50 +-3 degree C



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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Add the functionality to turn on the system on from Off and S4 with the consumer IR.	45	Change 3/5VALWP regulator from MAX1902 to MAX1999	2005.04.08	
2	Change PCN1 from SP020022200 to SP020024800.	49	Change PCN1 from SP02000A000 to DC040001P00.	2005.04.08	
3	Because EMI test fail	48	Change CPU_CORE HI-SIDE MOS from AO4408 to FDS6294, LOW-SIDE from AO4410 to FDS6676AS	2005.05.18	
4	Because V_bat to Calgary havn a leakage current, cause precharge can't finisn.	44	Add PD30 and PD31 to supply the V_bat power.	2005.06.09	
5	Add air-adapter detector	44	Add PU4 to detector air-adapter in.	2005.07.02	
6	Adjust the MB3887 CC to CP response cause the adapter OCP.	44	Change the PR31 from 100k_0402_1% to 10k_0402_1% Change the PR34 from 10k_0402_1% to 2.74k_0402_1% Change the PC21 from 4700p_0603_50V to 0.01u_0603_50v	2005.07.29	

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Title		
PWR PIR		
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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2005.04.18> 1		HP Jack + SPDIF change type	31 , 33	Del : U27 , C563 , C564 Add: Q52 , Q53 , Q54 , Q56 , Q57 , R571 , C730 , C731 , R567 , R569 , R568 , R570	0.2
2		Support CIR wake up from battery mode	4 , 37 , 38 , 41 , 35	12VALW change to B+ +3VALW change to LDO3 , +5VALW change to LDO5	0.2
3		for Marvell express card Rest timing	20 , 28	Add: Q55	0.2
4		for some HDD's LED always on	24	Del: D29 , R259 , Q10	0.2
5		for card bus can't work	27	S1_VCC and S1_VPP change to +S1_VCC and +S1_VPP	0.2
6		For nissan common design	35	JP28 and JP29 pin swap	0.2
7		For keyboard issue	37	Del: D27	0.2
<2005.04.27> 1		wake up from LAN	38	Add: R575(Pull UP PME_EC#)	0.3
2		For VOL_UP,DOWN function issue	38	POP: R418,R419,R420,R421	0.3
<2005.05.3> 1		For CIR wake up	38	Add: R576, R577 to option	0.3
<2005.05.4> 1		EC 910L include portion circuit	39	Add: R578 , Del:C630 , R422 , Q22 , U35A	0.3
2		ME change LED type	36	D18,D20,D21 from right angle change to vertical type	0.3
<2005.05.6> 1		Add wireless LED current limit resistor	17	Add: R581 current limit resistor	0.3
<2005.05.9> 1		TP conn pin reverse	35	Pin swap	
<2005.05.10> 1		ME change LED type	36	D25 from right angle change to vertical type	
2		HP requirement from 75 ohm change to 33 ohm	33	R567 , R569 from 75 ohm change to 33 ohm	
3		For nissan common design	35	Add: R582 , R583	
<2005.05.11> 1		For 2 way and 4 way touch pad	36	Add: R584 , R585	
<2005.06.10>		update JP23 dual USB connector to reverse type			0.4
		DFX modification for Rev0.4 MB			
		Change MR954, MC928, MR924, MR922, MR932, MC944, MC970, MC976, MC978, MC926 to correct pad size with Compal layout rule			
		update USB connector to reverse type			
		Change D6 form RB411 to RB491			

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2005.06.27>	1	For clear H_RST# glitch	41	Add Q61	0.5
<2005.07.04>	1	For +1.8VS EMI	11	Change R61, R84 value from 0 ohm to 120 ohm	0.5
	2	For +1.2V_HT power ripple	14	Change C197, C209, C254, C248, C251, C256, C258 value from 0.1U 16V4Z 0402 to 1U 6.3V4Z 0402	0.5
	3	For +2.5VS EMI	15	Add C737, C738, C741, C742 220P 50V8J 0402	0.5
	4	For +2.5VS EMI	15	Add C739, C740, C743, C744 1000P 50V7K 0402	0.5
	5	For Mini-PCI_CLK EMI	30	Mount R325 and C512	
	6	For CardBus chip PCI_CLK EMI	25	mount R279 and C442	0.5
	7	For LAN chip PCI_CLK EMI	29	Mount R322 and C504	0.5
	8	For EC K/B chip PCI_CLK EMI	30	Mount R415 and C628	
<2005.07.05>	1	For USB EMI	34	Add L33, L34	
	2	For USB EMI	34	change R561,R559,R562,R560 size from 0603 to 0402	
<2005.07.07>	1	For dock Docking audio noise	31	Add Q58, R589, Q60, R590, Q59, R589	
	2	For Dock_LOUTR/L EMI	40	Add R591, C745, R592, C746	
	3	For Docking TV_out signals EMI	40	Add R593, C747, R594, C748,C749, C750, R595, C751, C752	
<2005.07.11>	1	For accelerate +2.5VS discharge speed	40	change R442 size and value from 470_0402 to 10_0805	
	2	For LAN lamp	29	Swap Activity and Link Lamp	
<2005.07.25>	1	For SanDisk SD 256M card could not work issue	25	delete U48 Quick switch reserve schematics	
	2	For SanDisk SD 256M card could not work issue	25	Delete R463, R465, R466, R476, R268	
	3	For SanDisk SD 256M card could not work issue	26	Delete R270, R267, R547, R548	
	4	For SanDisk SD 256M card could not work issue	26	Mount R550 and R549	
<2005.07.28>	1	For lower power consumption	38	Add and un-mount R596	
	2	For CRT Assy	18	change CRT footprint	

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