

Compal confidential

Schematics Document

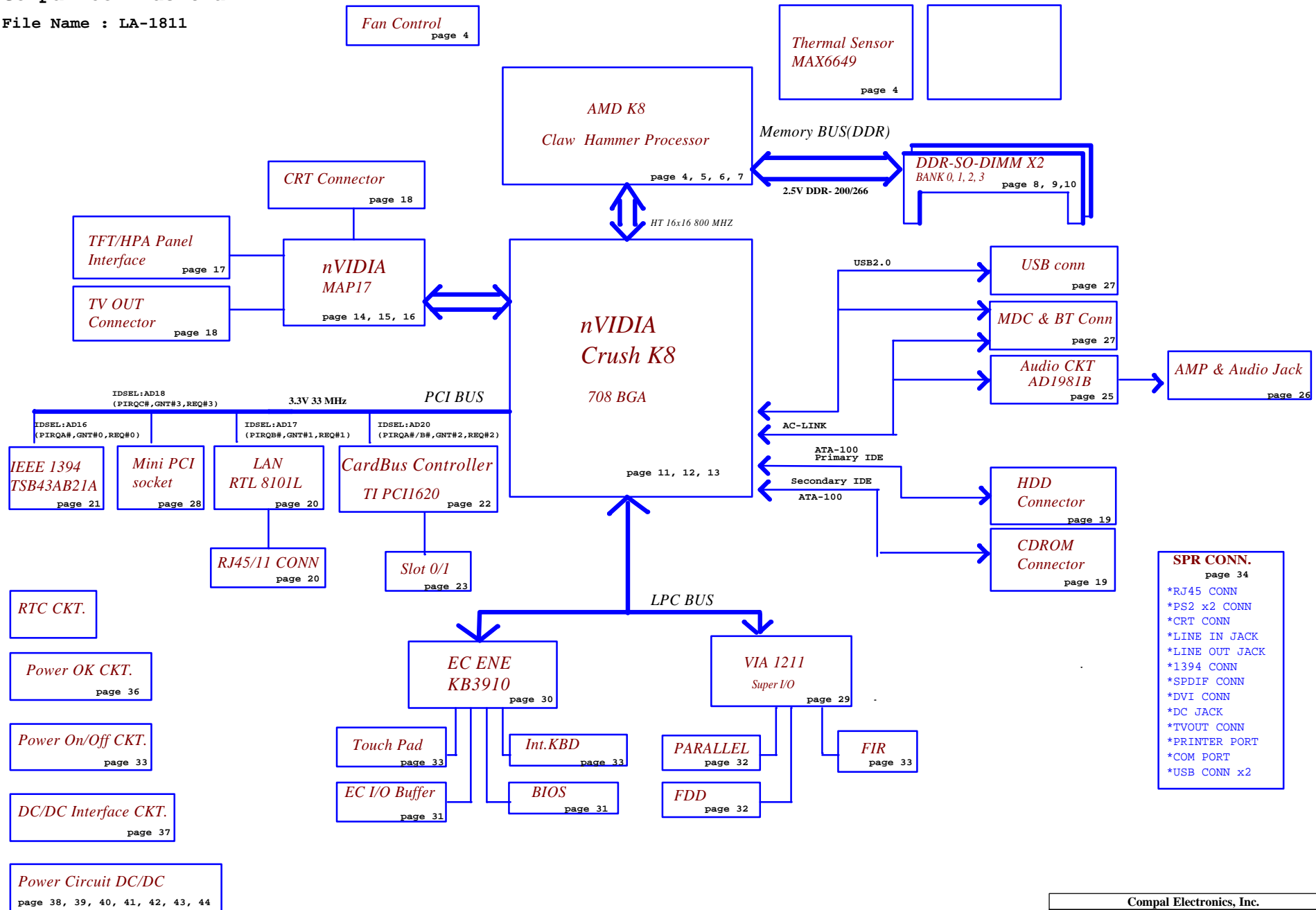
ClawHammer AMD K8 with nVIDIA Chrush K8

2003-10-15

REV:0.5

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Cover Sheet		
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Block Diagram		
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Voltage Rails

power plane \ State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	O	O	O
S1	O	O	O
S3	O	O	X
S5 S4/AC	O	X	X
S5 S4/AC don't exist	X	X	X

O MEANS ON
X MEANS OFF

PCI Devices

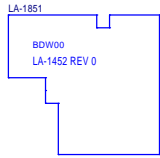
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
INTERNAL				
USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F
EXTERNAL				
VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

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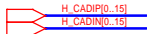
Notes List

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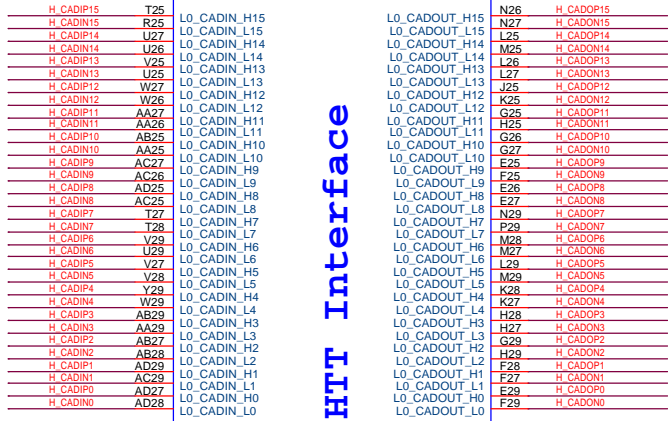
<11> H_CADIP[0..15]
<11> H_CADIN[0..15]



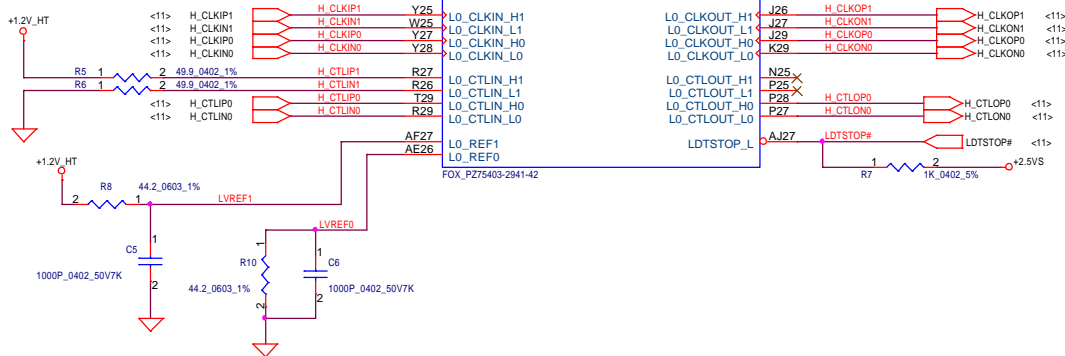
<11>

U1A

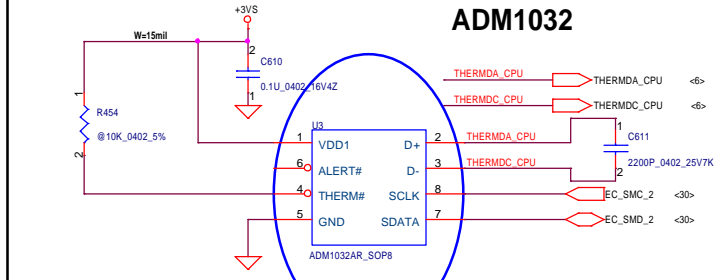
Claw Hammer-DTR



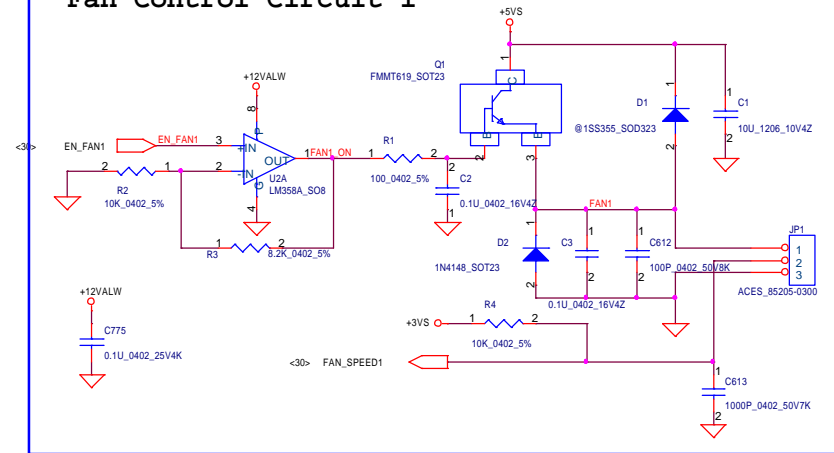
HTT Interface



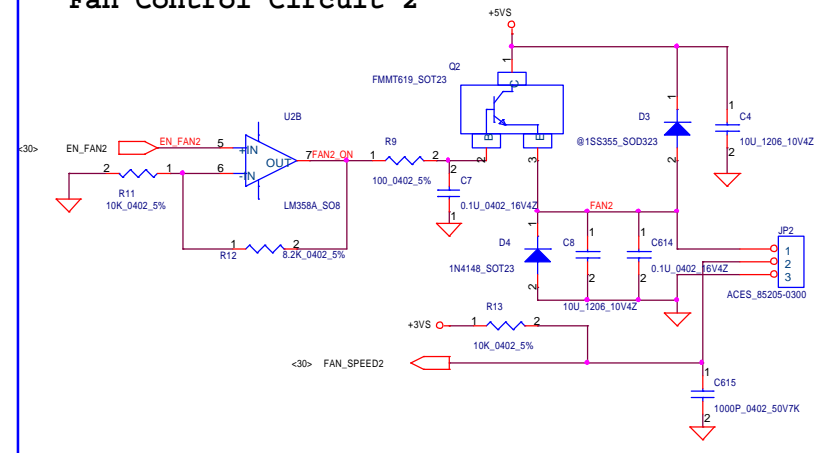
Thermal Sensor ADM1032



Fan Control Circuit 1



Fan Control Circuit 2

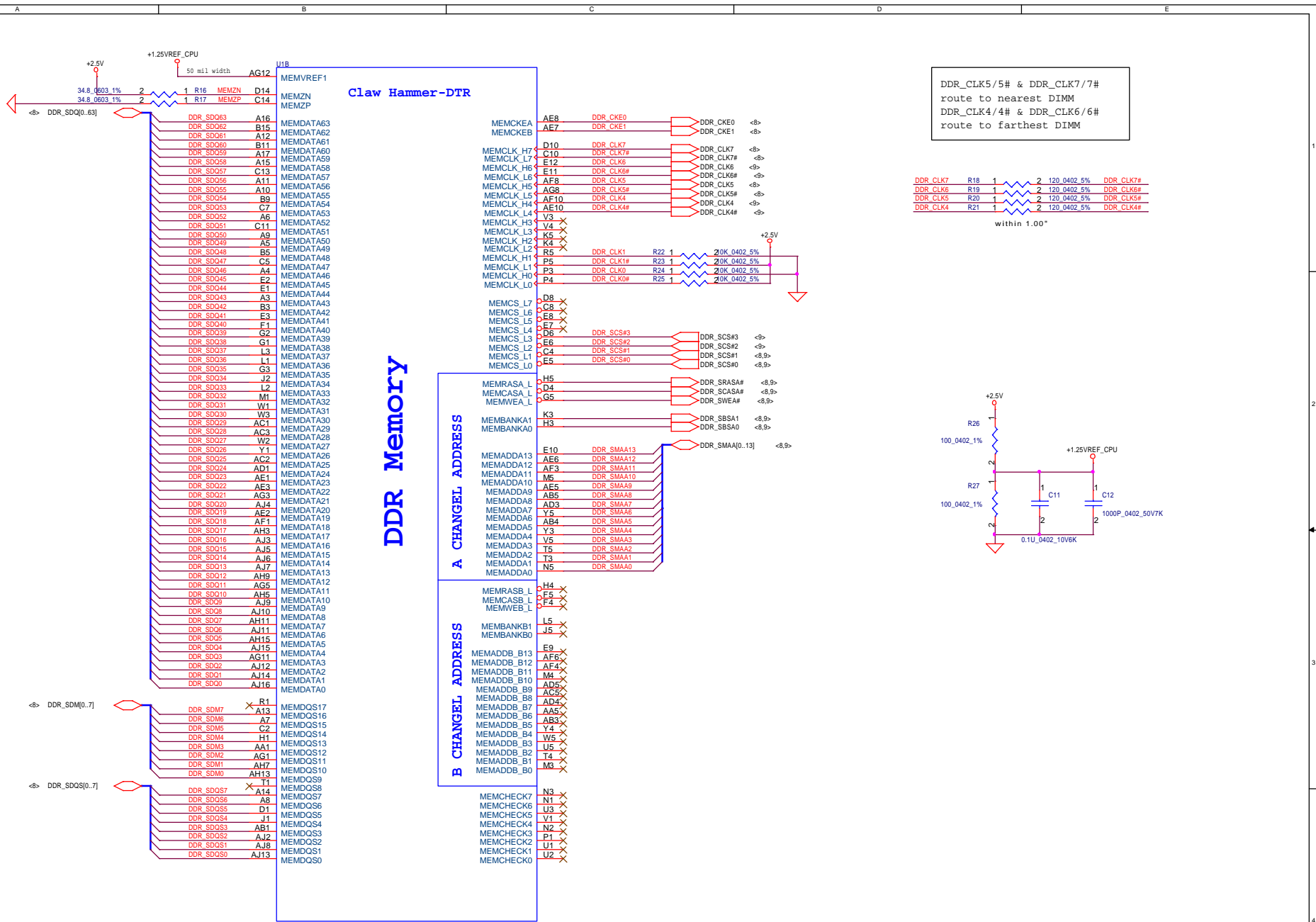


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Claw Hammer CPU (Host Bus)

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Claw Hammer-DTR

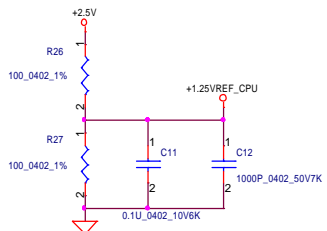
DDR Memory

A CHANGE ADDRESS

B CHANGE ADDRESS

DDR_CLK5/5# & DDR_CLK7/7#
route to nearest DIMM
DDR_CLK4/4# & DDR_CLK6/6#
route to farthest DIMM

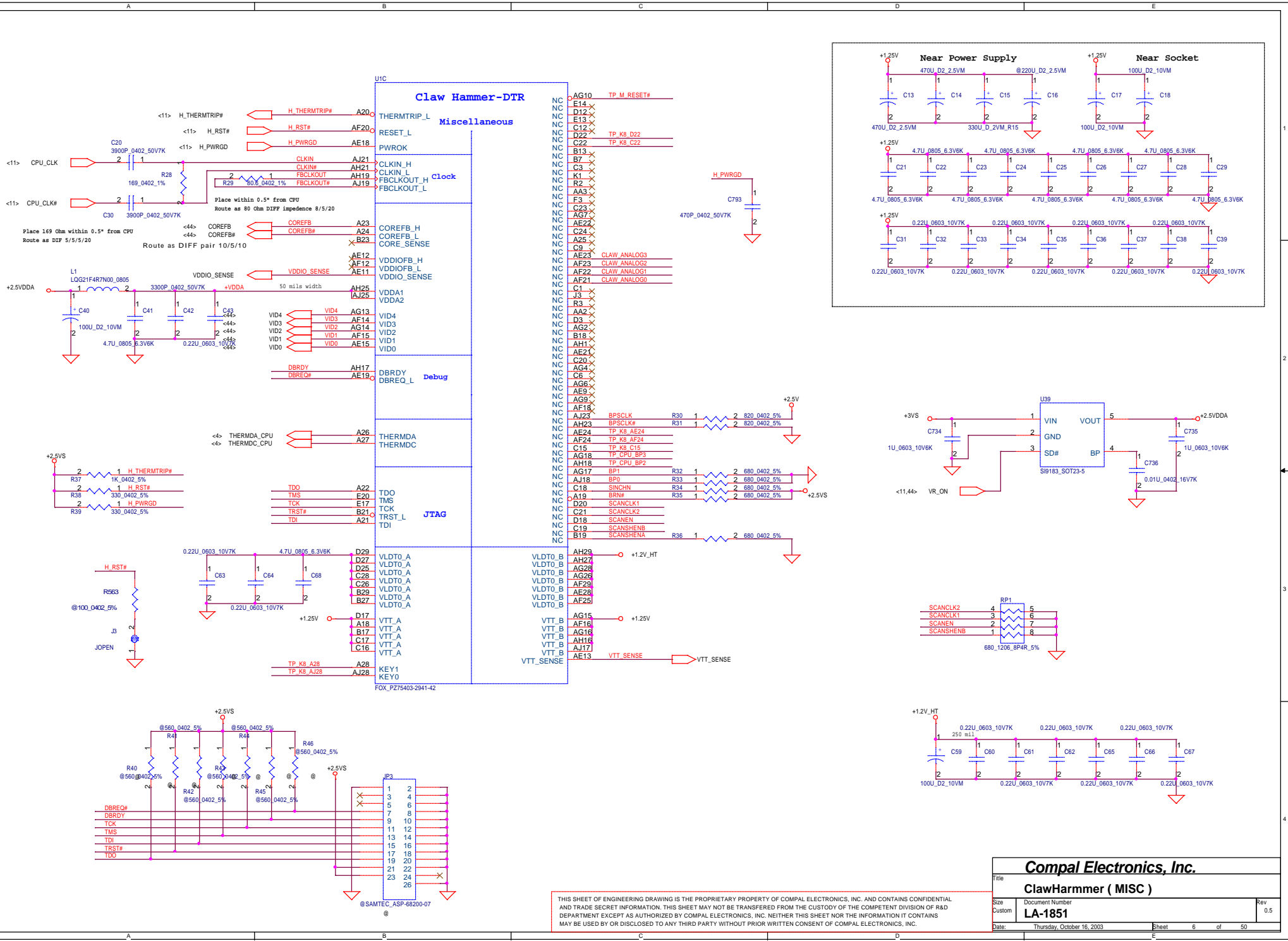
DDR_CLK7 R18 1 2 120 0402 5% DDR_CLK7#
DDR_CLK6 R19 1 2 120 0402 5% DDR_CLK6#
DDR_CLK5 R20 1 2 120 0402 5% DDR_CLK5#
DDR_CLK4 R21 1 2 120 0402 5% DDR_CLK4#
within 1.00"



FOX_P275403-2941-42

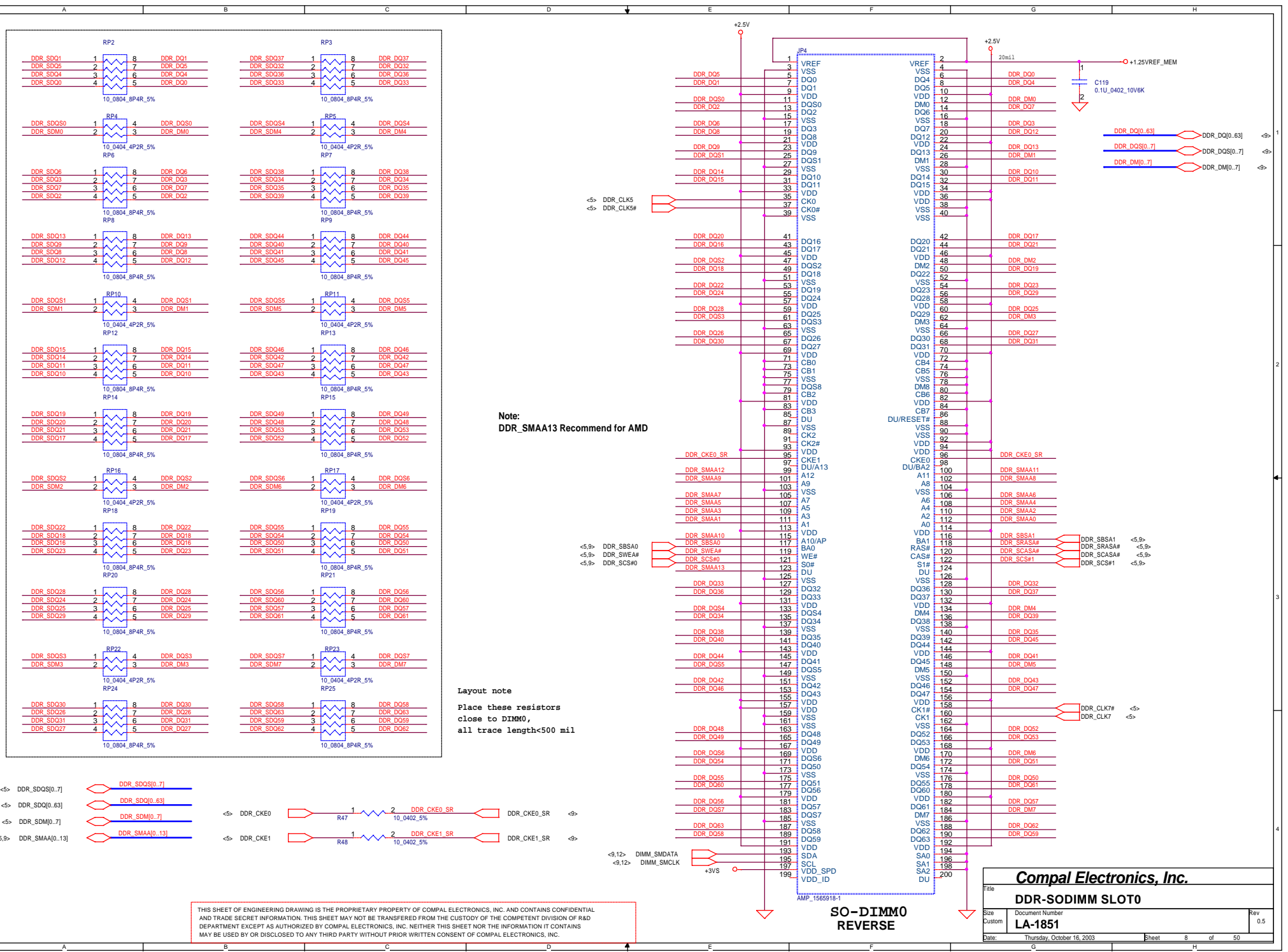
Compal Electronics, Inc.		
Claw Hammer (MEMORY BUS)		
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ClawHammer (MISC)		
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<-> DDR_CLK5
<-> DDR_CLK#

<-> DDR_SBSA0
<-> DDR_SWEAR
<-> DDR_SCS#0

<-> DDR_CKE0
<-> DDR_CKE1

<-> DIMM_SMDATA
<-> DIMM_SMCLK

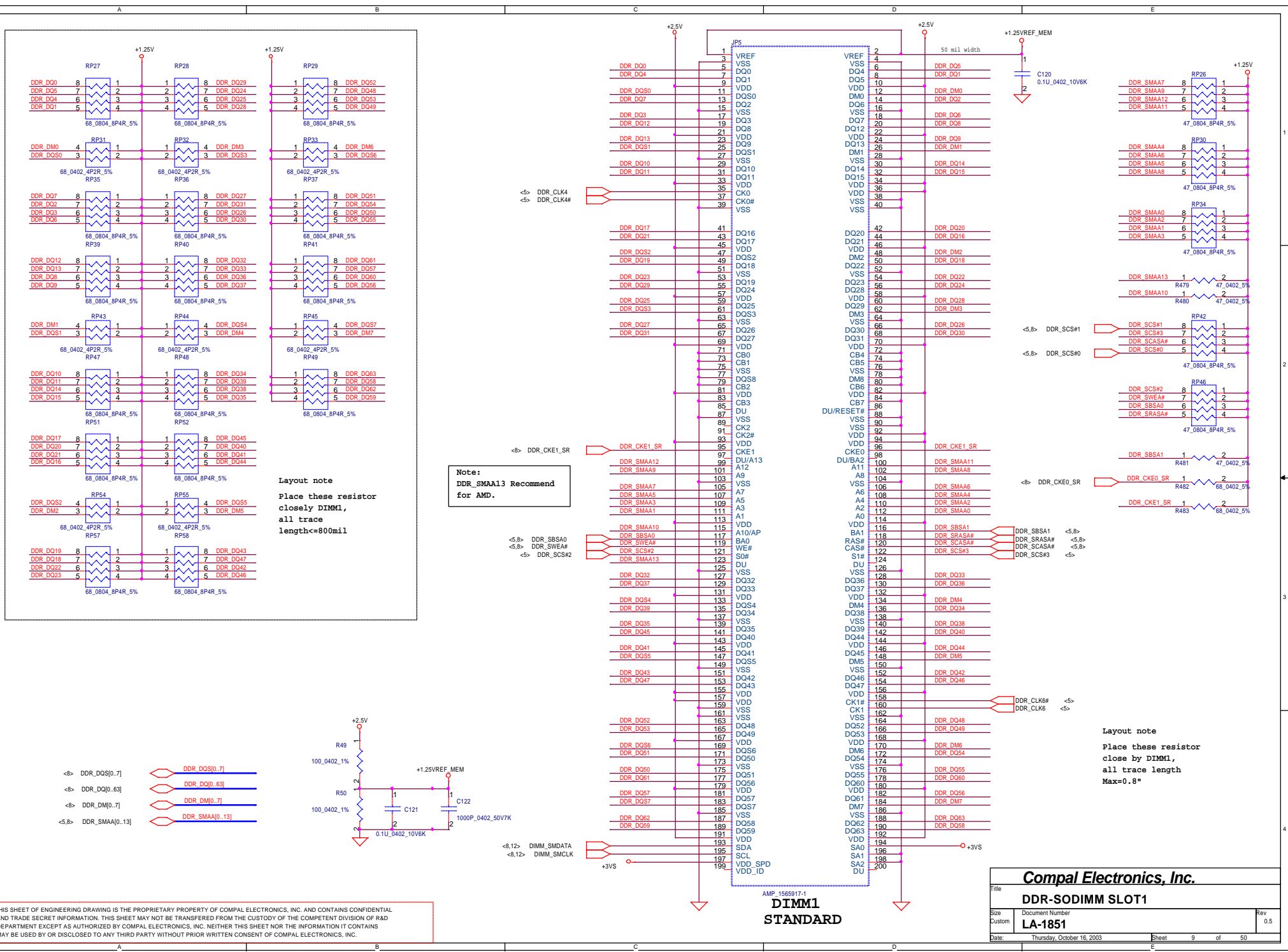
Note:
DDR_SMAA13 Recommend for AMD

Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

Compal Electronics, Inc.		
DDR-SODIMM SLOT0		
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SO-DIMM0
REVERSE



Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

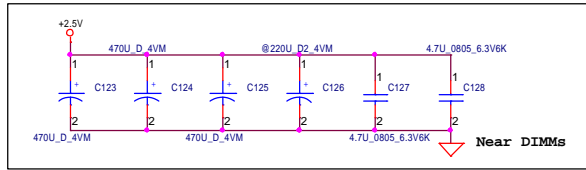
Note:
DDR SMAA13 Recommend
for AMD.

Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

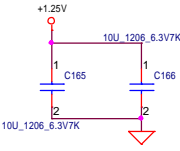
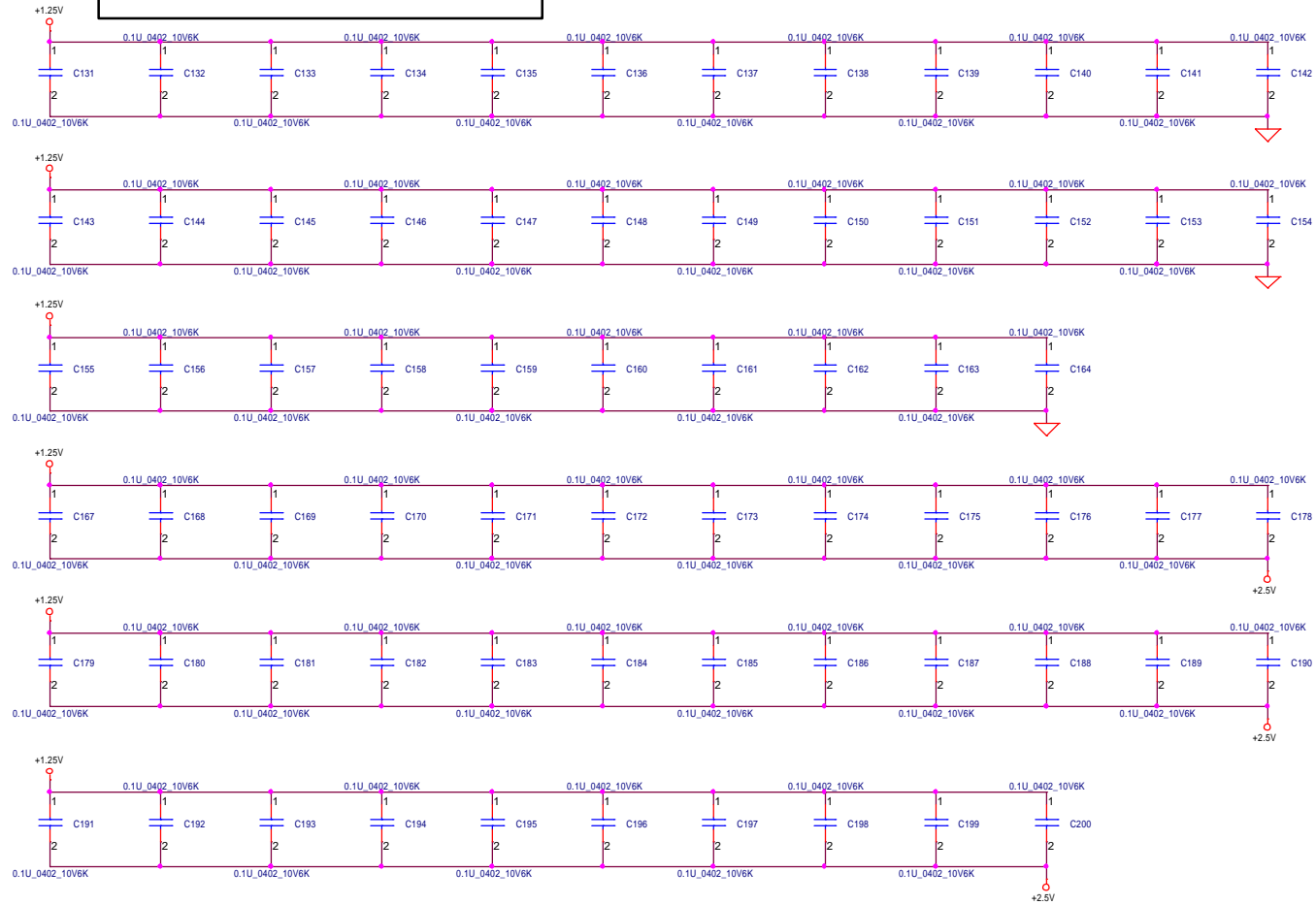
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DDR-SODIMM SLOT1		
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AMP 1565917-1
DIMM1
STANDARD

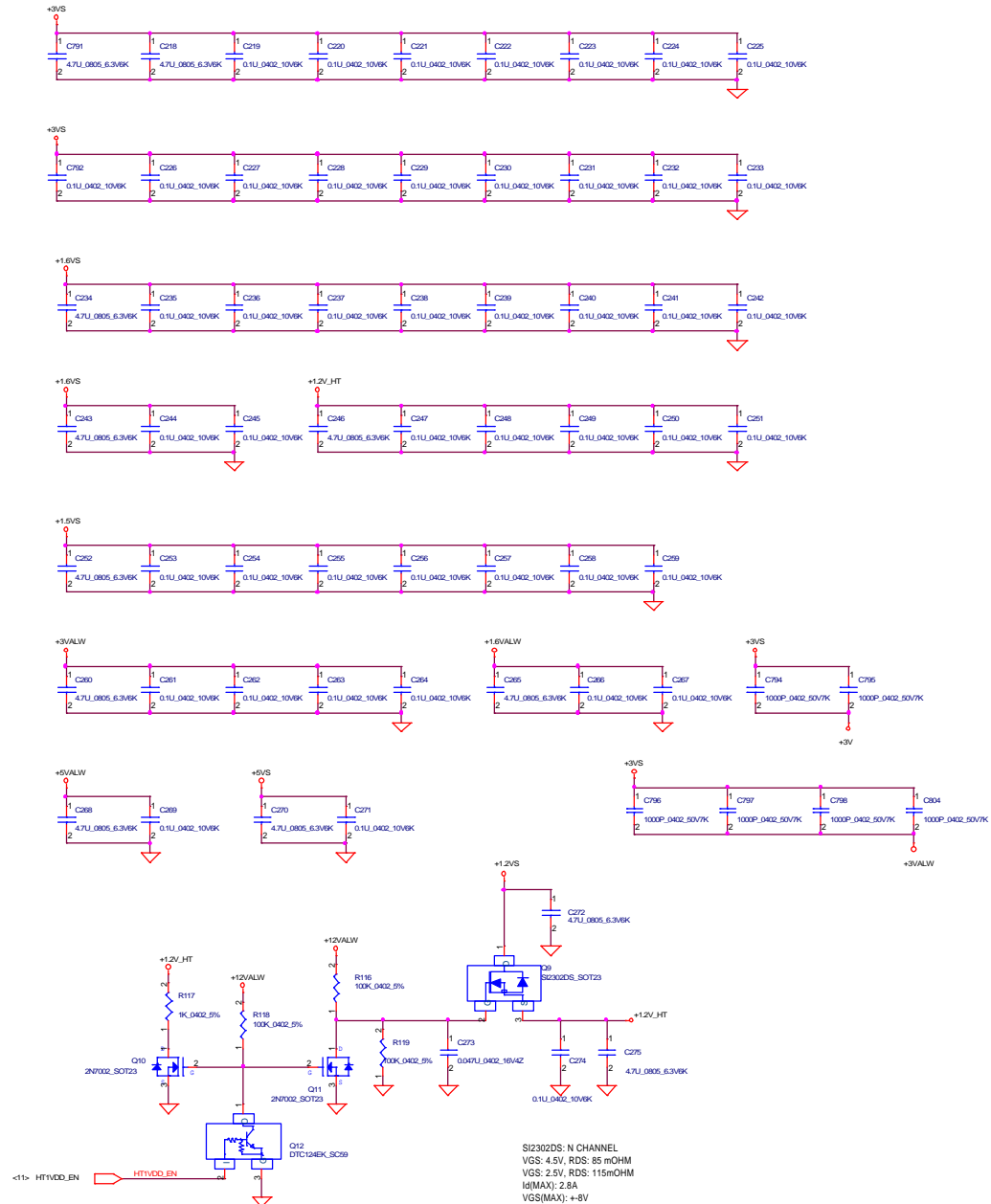
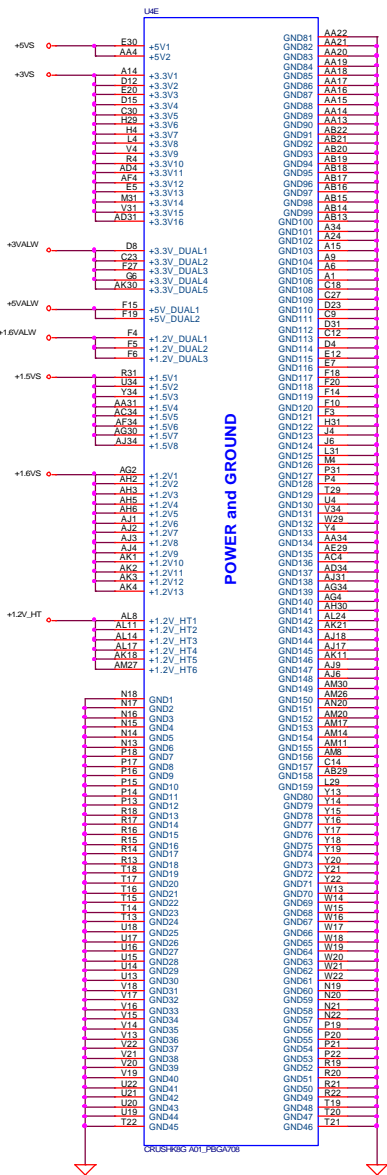


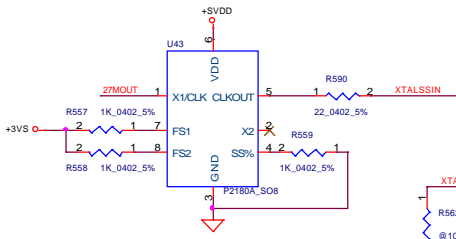
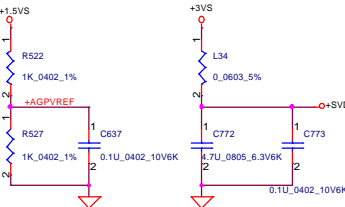
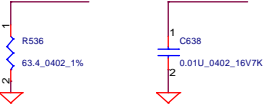
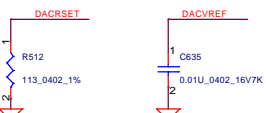
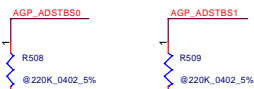
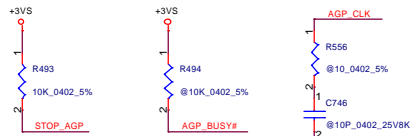
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



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Compal Electronics, Inc.		
DDR SODIMM Decoupling		
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SST Ratio selection table for W180

Modulation setting	SST Ratio
0	1.25%
1	3.75%

- AGP_AD0 AD00
- AGP_AD1 AD01
- AGP_AD2 AD02
- AGP_AD3 AD03
- AGP_AD4 AD04
- AGP_AD5 AC30
- AGP_AD6 AF28
- AGP_AD7 AC29
- AGP_AD8 AH30
- AGP_AD9 AC28
- AGP_AD10 AH29
- AGP_AD11 AE28
- AGP_AD12 A180
- AGP_AD13 AC28
- AGP_AD14 AC30
- AGP_AD15 AC27
- AGP_AD16 AH23
- AGP_AD17 A124
- AGP_AD18 AH22
- AGP_AD19 AK24
- AGP_AD20 AH21
- AGP_AD21 AF22
- AGP_AD22 AH20
- AGP_AD23 AK22
- AGP_AD24 AC21
- AGP_AD25 A119
- AGP_AD26 AG18
- AGP_AD27 AK19
- AGP_AD28 AH19
- AGP_AD29 A118
- AGP_AD30 AF19
- AGP_AD31 AK18

- PCICBE#0 AH28
- PCICBE#1 A127
- PCICBE#2 AK25
- PCICBE#3 AF21
- AH11 PCIRST#
- AH12 PCIGNT#
- AH13 PCIRCS#
- AH14 PCIFRAME#
- AH15 PCIRDY#
- AH16 PCITRDY#
- AH17 PCICBEVSEL#
- AH18 PCISTOP#
- AH19 PCIPAR
- AH20 PCINTA#
- AH21 PCICLK
- AG15 AGPRBF#
- AG16 AGPVB#
- AG17 AGPP#
- AG18 AGPBUSY#
- AG19 STOP_AGP
- AG20 AGP_VREF
- AG21 AGP_VREF

- AG15 AGPSB#0
- AG16 AGPSB#1
- AG17 AGPSB#2
- AG18 AGPSB#3
- AG19 AGPSB#4
- AG20 AGPSB#5
- AG21 AGPSB#6
- AG22 AGPSB#7
- AG23 AGPADSTB#1
- AG24 AGPADSTB#0
- AG25 AGPADSTB#0
- AG26 AGP_ST0
- AG27 AGP_ST1
- AG28 AGP_ST2
- AG29 CRT_R
- AG30 CRT_G
- AG31 CRT_B
- AG32 CRT_HSYNC
- AG33 CRT_VSYNC
- AG34 DACRSET
- AG35 DACVREF
- AG36 TV_CRMA
- AG37 TV_LUMA
- AG38 TV_COMPS
- AG39 DACZREST
- AG40 DACZVREF
- AG41 DACZVREF

- AG21 AGPADSTB#1
- AG22 AGPADSTB#0
- AG23 AGPADSTB#0
- AG24 AGP_ST0
- AG25 AGP_ST1
- AG26 AGP_ST2
- AG27 CRT_R
- AG28 CRT_G
- AG29 CRT_B
- AG30 CRT_HSYNC
- AG31 CRT_VSYNC
- AG32 DACRSET
- AG33 DACVREF
- AG34 TV_CRMA
- AG35 TV_LUMA
- AG36 TV_COMPS
- AG37 DACZREST
- AG38 DACZVREF
- AG39 DACZVREF

- AG39 DACZREST
- AG40 DACZVREF
- AG41 DACZVREF
- AG42 TV_CRMA
- AG43 TV_LUMA
- AG44 TV_COMPS
- AG45 DAC2HSYNC
- AG46 DAC2VSYNC
- AG47 DAC2REST
- AG48 DAC2VREF
- AG49 TV_CRMA
- AG50 TV_LUMA
- AG51 TV_COMPS
- AG52 DAC2HSYNC
- AG53 DAC2VSYNC
- AG54 DAC2REST
- AG55 DAC2VREF

- AG56 XTALIN
- AG57 XTALOUT
- AG58 XTALSSIN
- AG59 XTALSSIN
- AG60 XTALSSIN
- AG61 XTALSSIN
- AG62 XTALSSIN
- AG63 XTALSSIN
- AG64 XTALSSIN
- AG65 XTALSSIN
- AG66 XTALSSIN
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- AG95 XTALSSIN
- AG96 XTALSSIN
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- AG99 XTALSSIN
- AG100 XTALSSIN

GPIO/VIP Interface

PCI/AGP BUS Interface

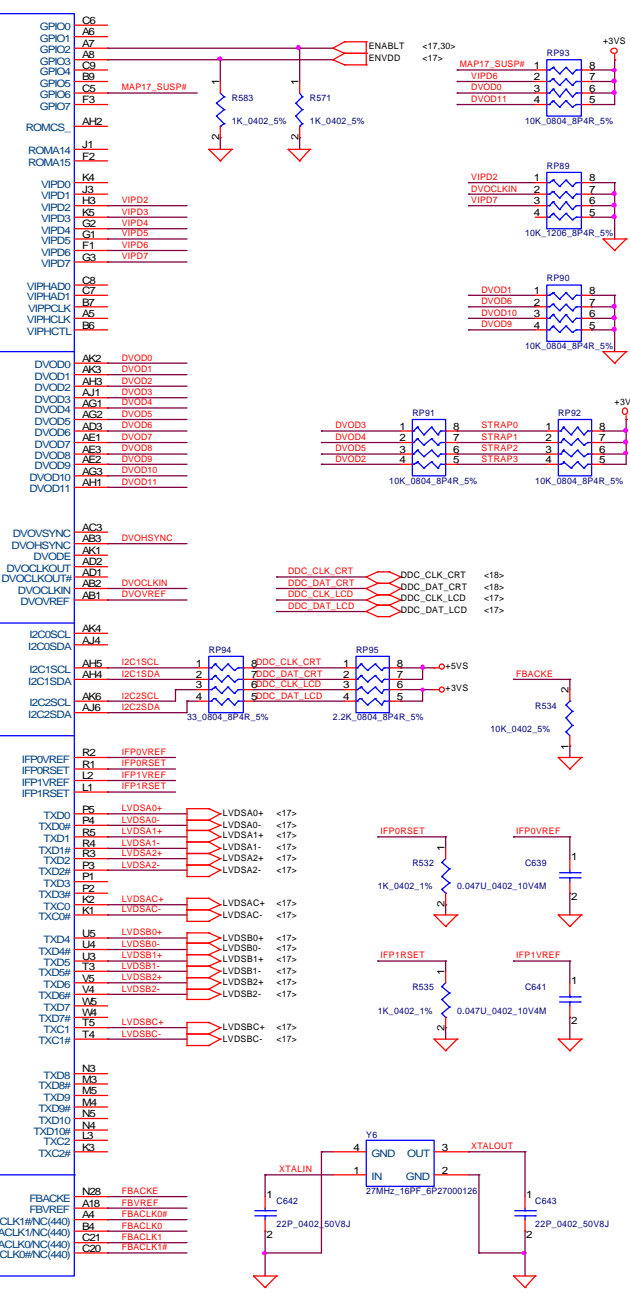
I2C

LVDS/TMDS

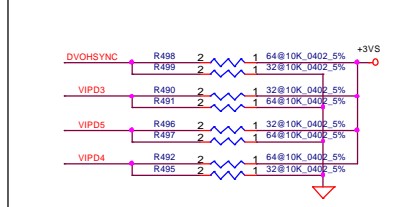
DAC

CLOCK

SDRAM

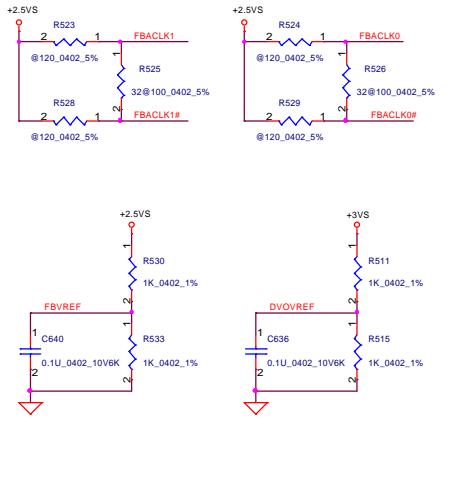


DVOHSYNC	VIPD3	VIPD5	VIPD4	DEVICE
1	1	0	1	MAP17-116 (16MB)
0	1	1	0	* MAP17-232 (32MB)
1	0	0	1	MAP17-464 (64MB)



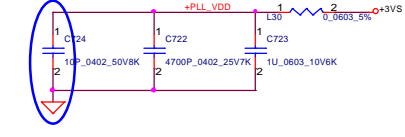
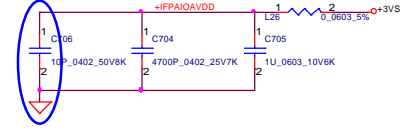
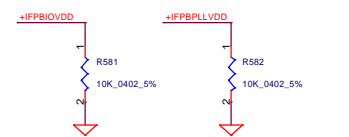
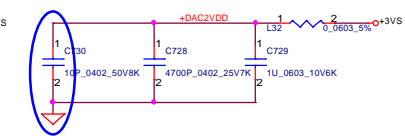
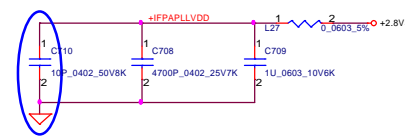
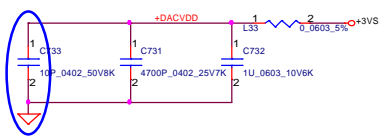
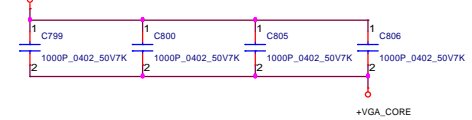
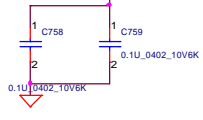
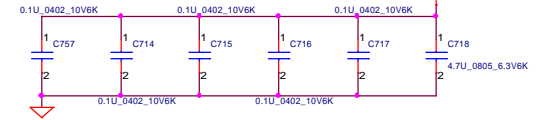
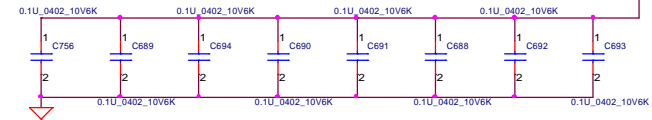
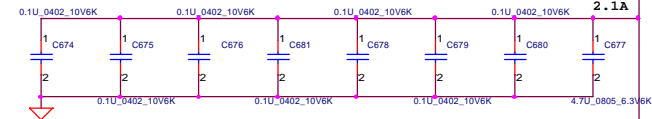
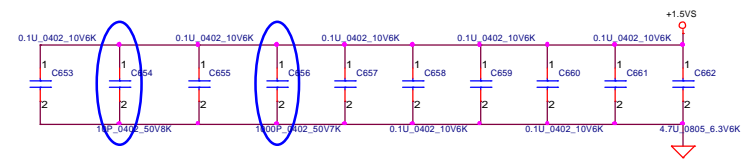
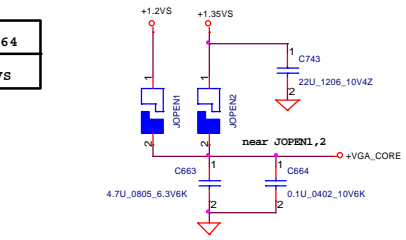
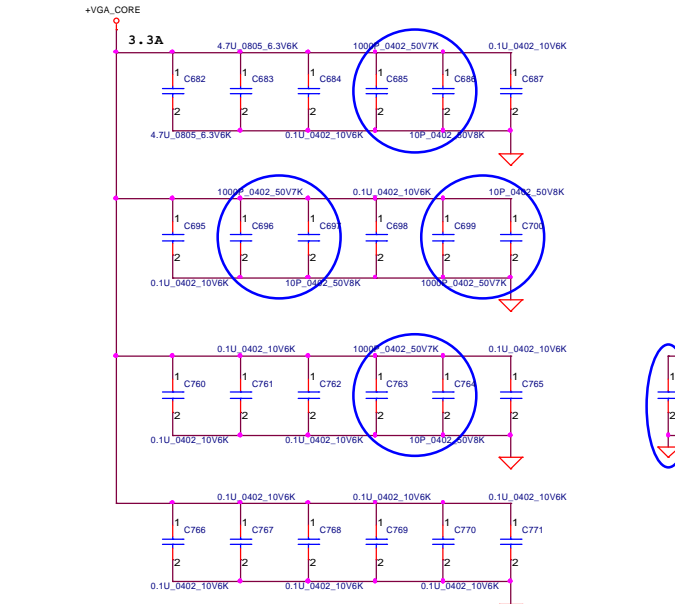
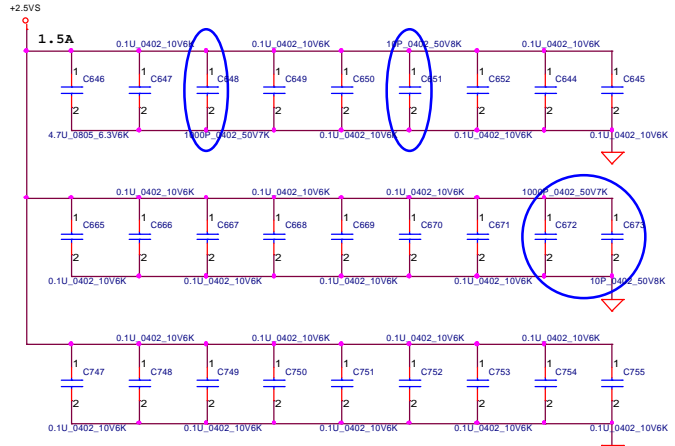
CRYSTAL

DVOD8	DVOD7	TVMODE
0	0	SECAM
0	1	* NTSC
1	0	PAL
1	1	VGA



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	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS



Compal Electronics, Inc.

MAP17 Power (2/3)

LA-1851

Thursday, October 16, 2003

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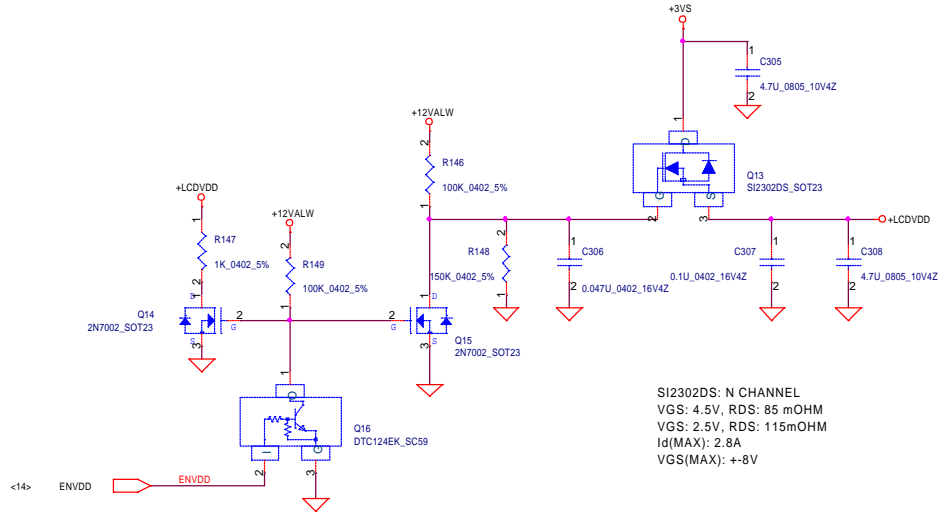
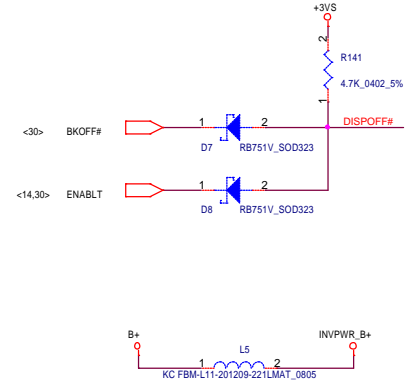
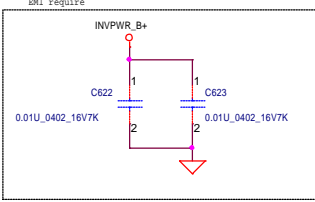
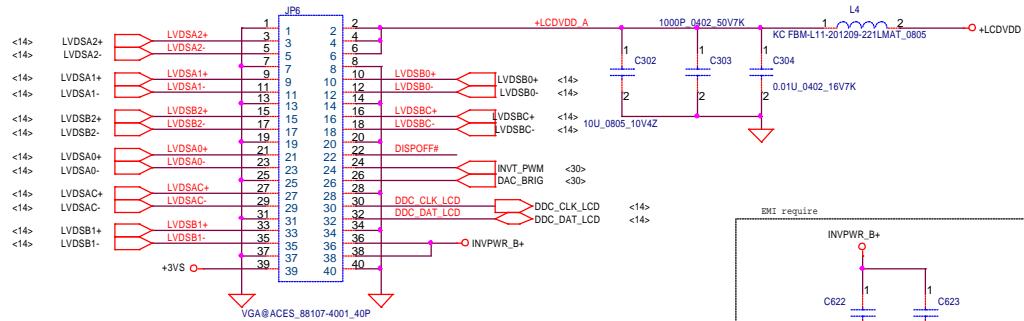
U38D		
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L10	GND/NO PIN(440)	M17
M10	GND/NO PIN(440)	N17
N10	GND/NO PIN(440)	P17
R10	GND/NO PIN(440)	T17
T10	GND/NO PIN(440)	U17
U10	GND/NO PIN(440)	V17
V10	GND/NO PIN(440)	W17
W10	GND/NO PIN(440)	Y17
Y10	GND/NO PIN(440)	AA17
AA10	GND/NO PIN(440)	K18
K11	GND/NO PIN(440)	L18
L11	GND/NO PIN(440)	M18
M11	GND/NO PIN(440)	N18
N11	GND/NO PIN(440)	P18
P11	GND/NO PIN(440)	R18
R11	GND/NO PIN(440)	T18
T11	GND/NO PIN(440)	U18
U11	GND/NO PIN(440)	V18
V11	GND/NO PIN(440)	W18
W11	GND/NO PIN(440)	Y18
Y11	GND/NO PIN(440)	AA18
AA11	GND/NO PIN(440)	K19
K12	GND/NO PIN(440)	L19
L12	GND/NO PIN(440)	M19
M12	GND/NO PIN(440)	N19
N12	GND/NO PIN(440)	P19
P12	GND/NO PIN(440)	T19
R12	GND/NO PIN(440)	U19
T12	GND/NO PIN(440)	V19
U12	GND/NO PIN(440)	W19
V12	GND/NO PIN(440)	Y19
W12	GND/NO PIN(440)	AA19
Y12	GND/NO PIN(440)	K20
AA12	GND/NO PIN(440)	L20
K13	GND/NO PIN(440)	M20
L13	GND/NO PIN(440)	N20
M13	GND/NO PIN(440)	P20
N13	GND/NO PIN(440)	T20
P13	GND/NO PIN(440)	U20
R13	GND/NO PIN(440)	V20
T13	GND/NO PIN(440)	W20
U13	GND/NO PIN(440)	Y20
V13	GND/NO PIN(440)	AA20
W13	GND/NO PIN(440)	K21
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P14	GND/NO PIN(440)	V21
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AA16	GND/NO PIN(440)	GND
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AB7	GND/NO PIN(440)	GND
AD7	GND	GND
AE7	GND	GND
B8	GND	GND
E9	GND	GND
Q9	GND	GND
AD9	GND	GND
AF9	GND	GND
B11	GND	GND
E11	GND	GND
G11	GND	GND
AD11	GND	GND
AE11	GND	GND
AJ11	GND	GND
AH12	GND	GND
BH4	GND	GND
E14	GND	GND
G14	GND	GND
AD14	GND	GND
AE14	GND	GND
AJ14	GND	GND
Y7	GND	GND
E17	GND	GND
G17	GND	GND
B17	GND	GND

SA000040300(0304231100)

U38C		
A1	NC	C30
B1	NC	V26
C1	NC	V28
D1	NC	V27
E1	NC	A27
F1	NC	B27
G1	NC	C27
H1	NC	D27
J1	NC	K27
K1	NC	M27
L1	NC	N27
M1	NC	R27
N1	NC	T27
P1	NC	U27
Q1	NC	V27
R1	NC	W27
S1	NC	Y27
T1	NC	AA28
U1	NC	B28
V1	NC	E28
W1	NC	H28
X1	NC	L28
Y1	NC	M28
AA1	NC	P28
AB1	NC	T28
AC1	NC	U28
AD1	NC	V28
AE1	NC	Y28
AF1	NC	AA29
AG1	NC	AB29
AH1	NC	C29
AI1	NC	D29
AJ1	NC	F29
AK1	NC	G29
AL1	NC	J29
AM1	NC	K29
AN1	NC	M29
AO1	NC	N29
AP1	NC	T29
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AS1	NC	Y29
AT1	NC	F28
AU1	NC	K28
AV1	NC	AA26
AW1	NC	R26
AX1	NC	V29
AY1	NC	AA29
AZ1	NC	AB29
BA1	NC	B13
BB1	NC	T30
BC1	NC	P30
BD1	NC	R30
BE1	NC	T30
BF1	NC	U30
BG1	NC	Y30
BH1	NC	AA30
BI1	NC	AB30
BJ1	NC	D13
BK1	NC	V28
BL1	NC	AA27
BM1	NC	D28
BN1	NC	C11
BO1	NC	B10
BP1	NC	A24
BQ1	NC	E3
BR1	NC	D3
BS1	NC	B12
BT1	NC	C12
BU1	NC	J30
BV1	NC	K30
BW1	NC	AH13
BX1	NC	A19
BY1	NC	M30
BZ1	NC	V30
CA1	NC	AH14
CB1	NC	D12
CC1	NC	C30
CD1	NC	L7
CE1	NC	U7
CF1	NC	W1
CG1	NC	AA8
CH1	NC	DAC2GND
CI1	NC	DAC3GND
CJ1	NC	IFF1PLL3GND
CK1	NC	IFF110GND
CL1	NC	IFF1PLL1GND
CM1	NC	IFF1PLL2GND
CN1	NC	IFF1PLL4GND
CO1	NC	IFF1PLL5GND
CP1	NC	IFF1PLL6GND
CQ1	NC	IFF1PLL7GND
CR1	NC	IFF1PLL8GND
CS1	NC	IFF1PLL9GND
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CU1	NC	IFF1PLL11GND
CV1	NC	IFF1PLL12GND
CW1	NC	IFF1PLL13GND
CX1	NC	IFF1PLL14GND
CY1	NC	IFF1PLL15GND
CZ1	NC	IFF1PLL16GND
DA1	NC	IFF1PLL17GND
DB1	NC	IFF1PLL18GND
DC1	NC	IFF1PLL19GND
DD1	NC	IFF1PLL20GND
DE1	NC	IFF1PLL21GND
DF1	NC	IFF1PLL22GND
DG1	NC	IFF1PLL23GND
DH1	NC	IFF1PLL24GND
DI1	NC	IFF1PLL25GND
DJ1	NC	IFF1PLL26GND
DK1	NC	IFF1PLL27GND
DL1	NC	IFF1PLL28GND
DM1	NC	IFF1PLL29GND
DN1	NC	IFF1PLL30GND
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DP1	NC	IFF1PLL32GND
DQ1	NC	IFF1PLL33GND
DR1	NC	IFF1PLL34GND
DS1	NC	IFF1PLL35GND
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ED1	NC	IFF1PLL46GND
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KF1	NC	IFF1PLL216GND
KG1	NC	IFF1PLL217GND
KH1	NC	IFF1PLL218GND
KI1	NC	IFF1PLL219GND
KJ1	NC	IFF1PLL220GND
KA1	NC	IFF1PLL221G

LCD Panel Connector

The cap.'s colsely to LCD CONN.

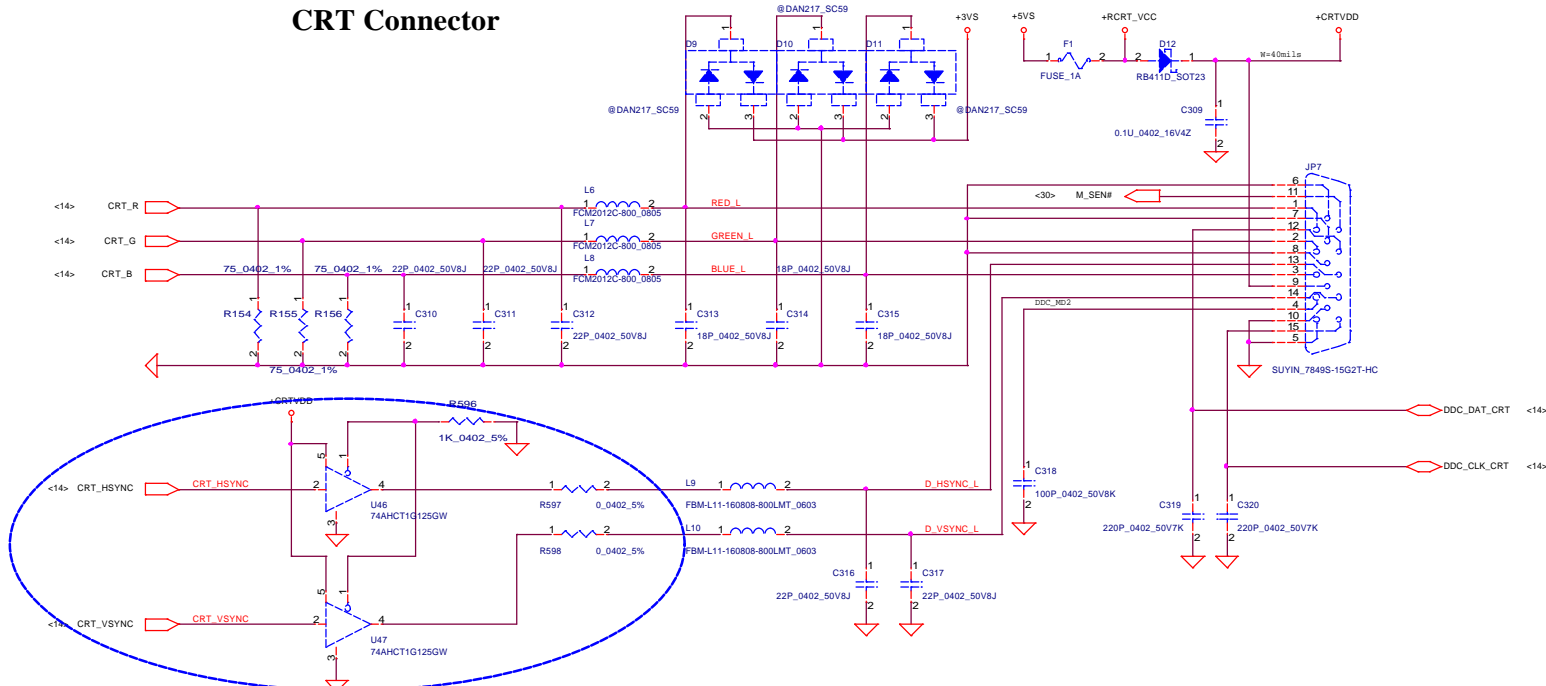


SI2302DS: N CHANNEL
 VGS: 4.5V, RDS: 85 mOHM
 VGS: 2.5V, RDS: 115mOHM
 Id(MAX): 2.8A
 VGS(MAX): +-8V

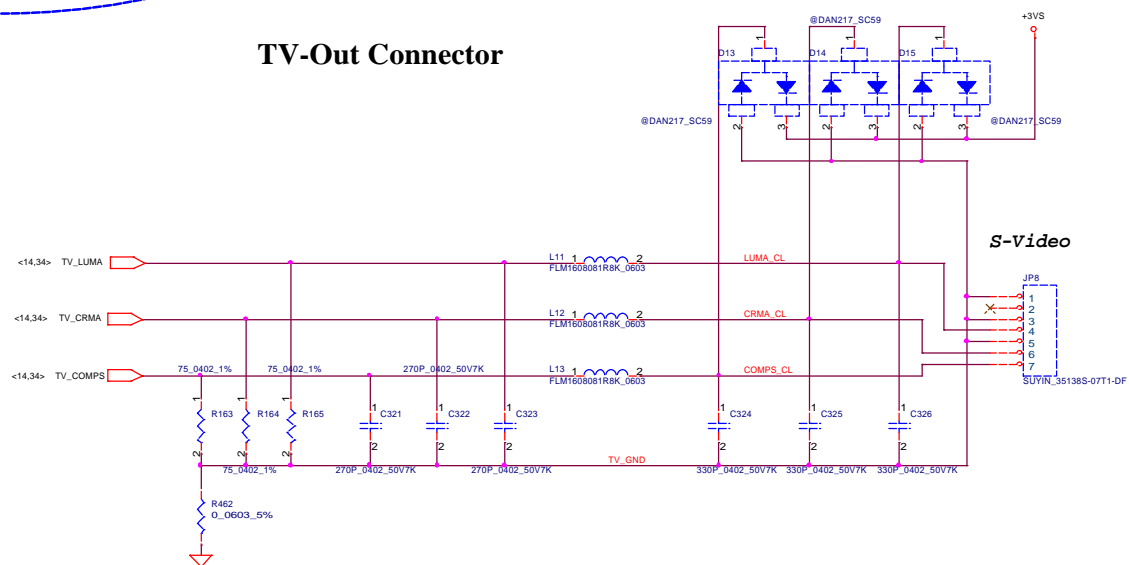
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Compal Electronics, Inc.		
Title		
LVDS Connector		
Size	Document Number	Rev
LA-1851		0.5
Date:	Thursday, October 16, 2003	Sheet 17 of 50

CRT Connector



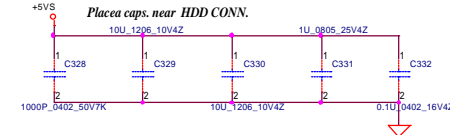
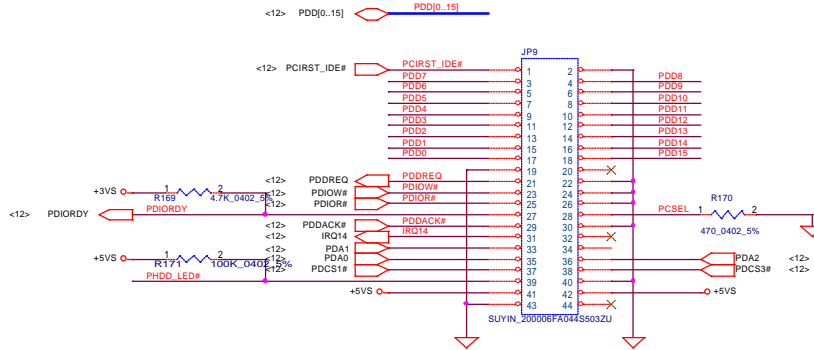
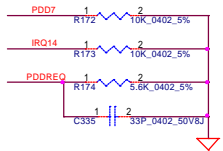
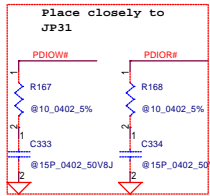
TV-Out Connector



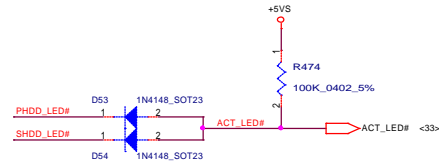
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Compal Electronics, Inc.		
CRT & TVout Connector		
Doc No	Document Number	Rev
	LA-1851	0.5
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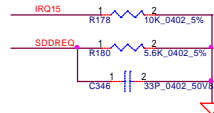
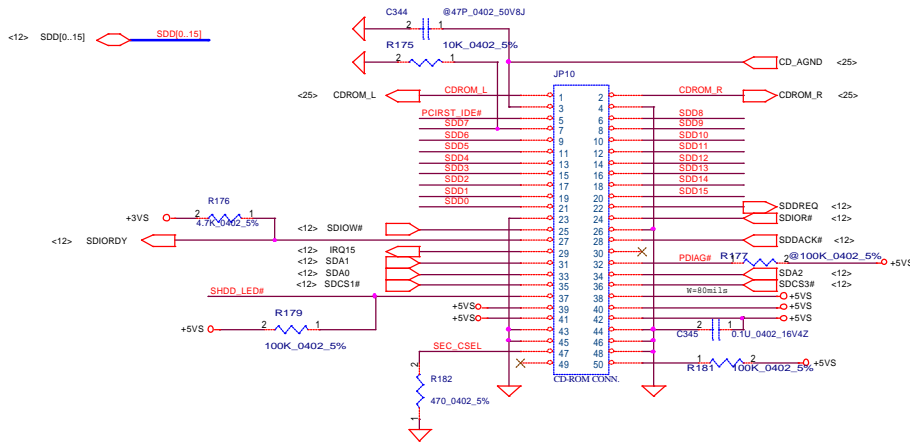
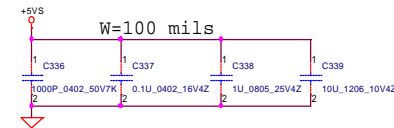
HDD Connector



CD-ROM Connector



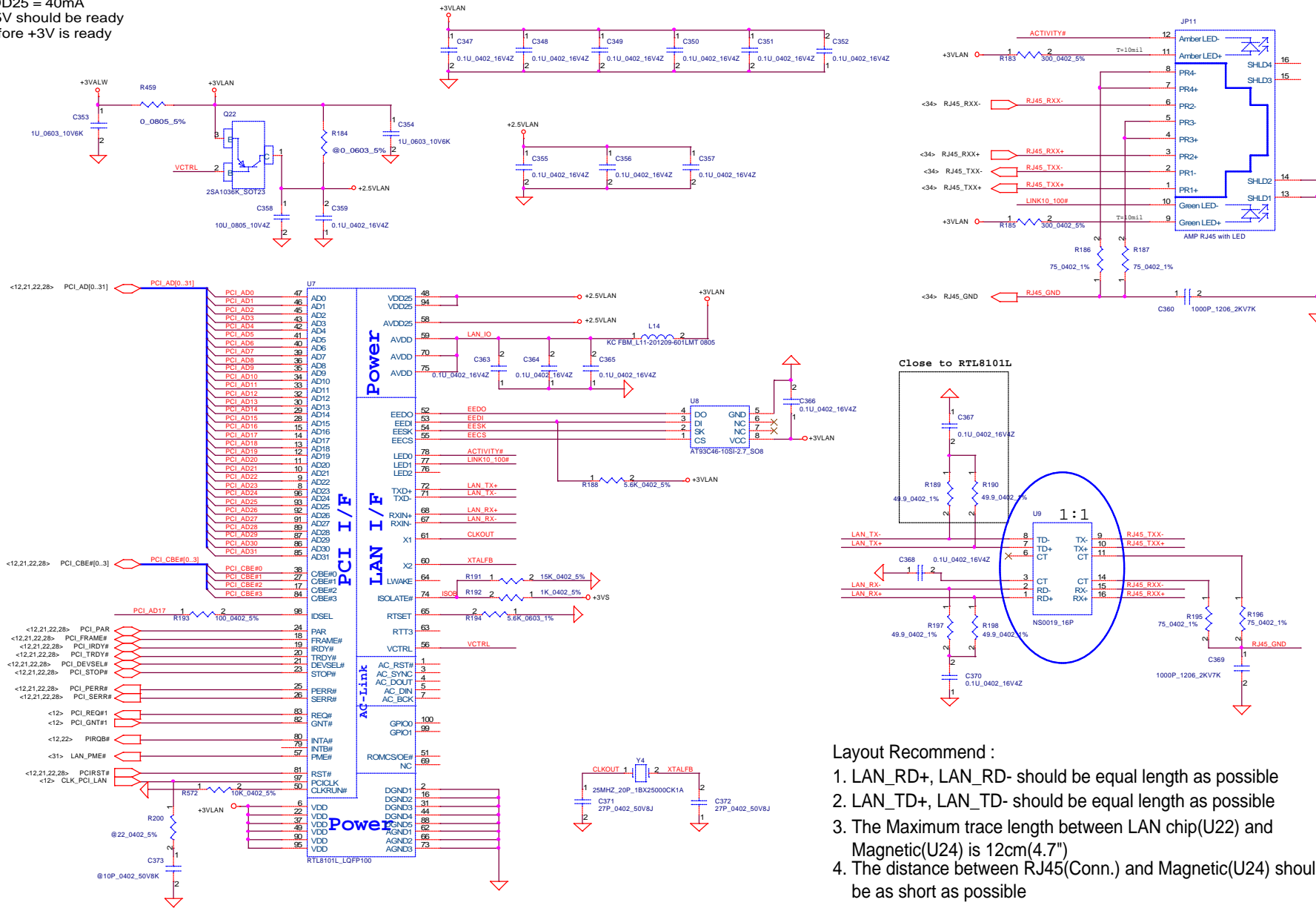
Place caps. near CDROM CONN.



Compal Electronics, Inc.		
IDE/FDD/CD-ROM Module		
Size	Document Number	Rev
Custom	LA-1851	0.5
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Note : I_{max} for VDD25 = 40mA
 2.5V should be ready before +3V is ready



Layout Recommend :

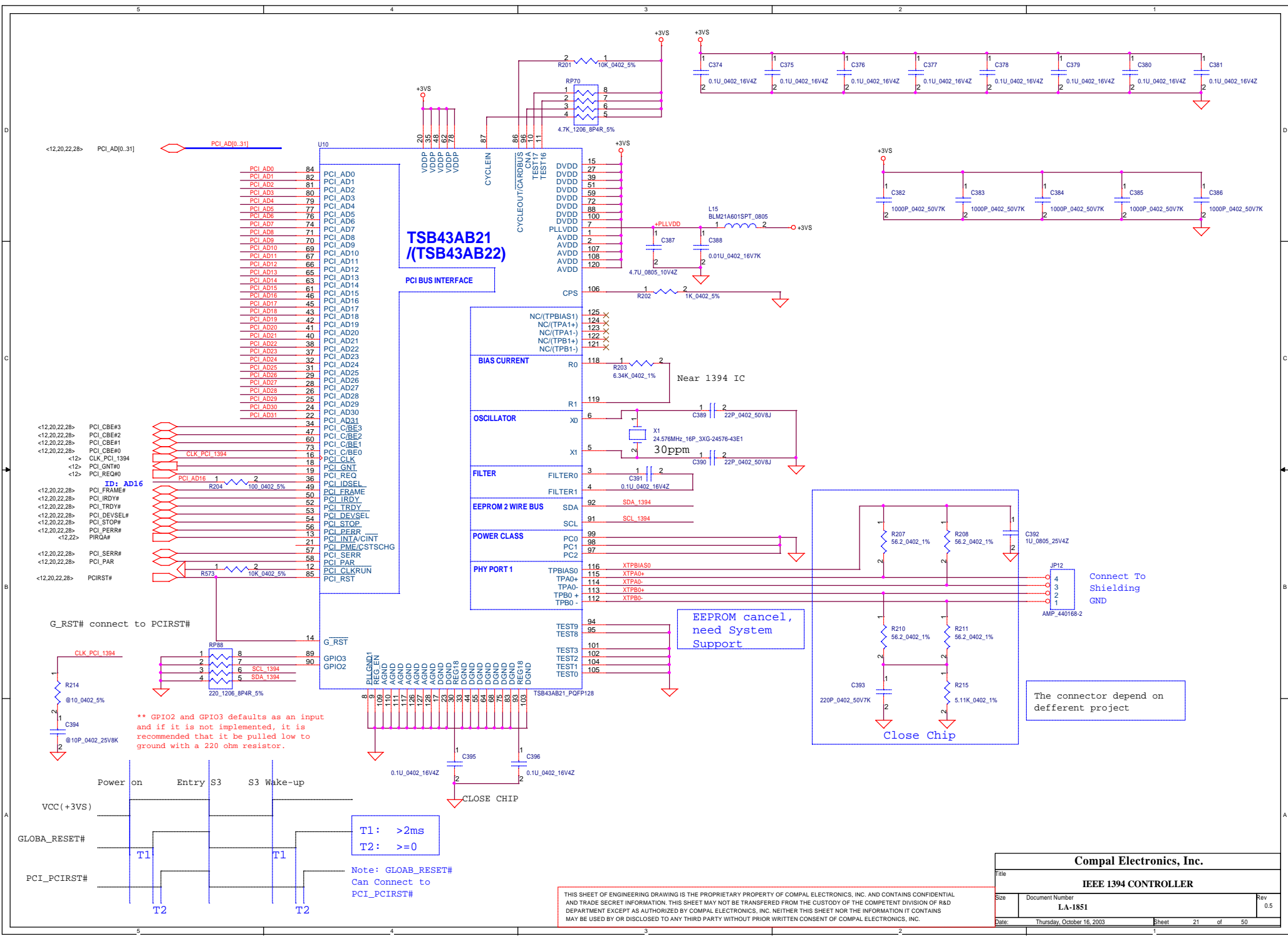
1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

Compal Electronics, Inc.

LAN RealTech8100BL

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Title		LAN RealTech8100BL	
Doc No	Document Number	LA-1851	
Date	Thursday, October 16, 2003	Sheet	20 of 50
Rev	0.5		

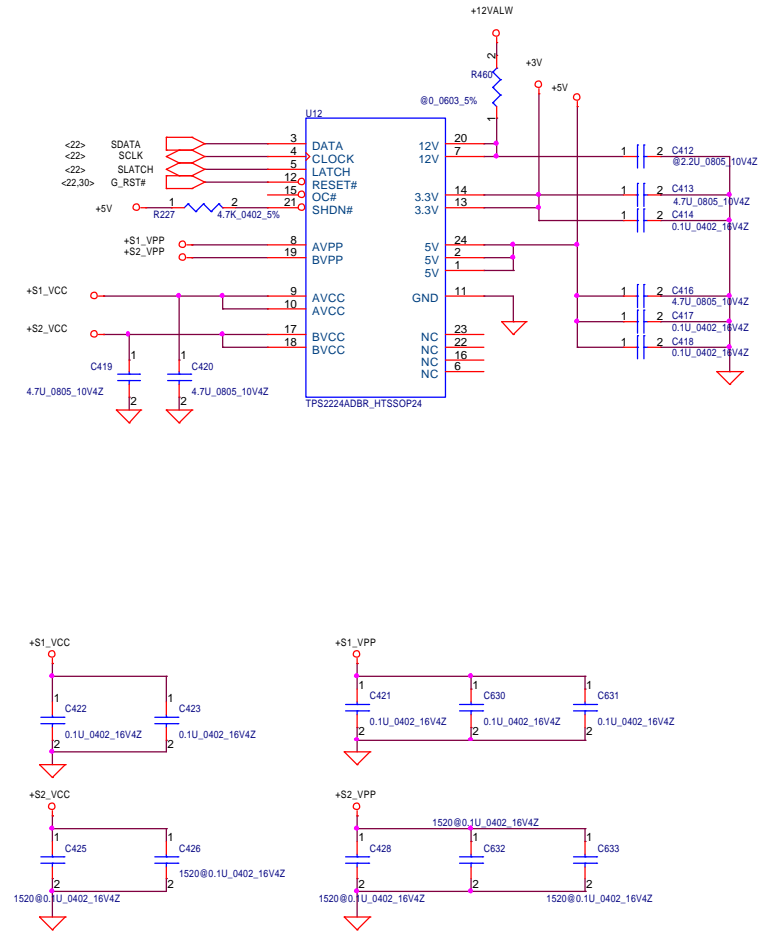
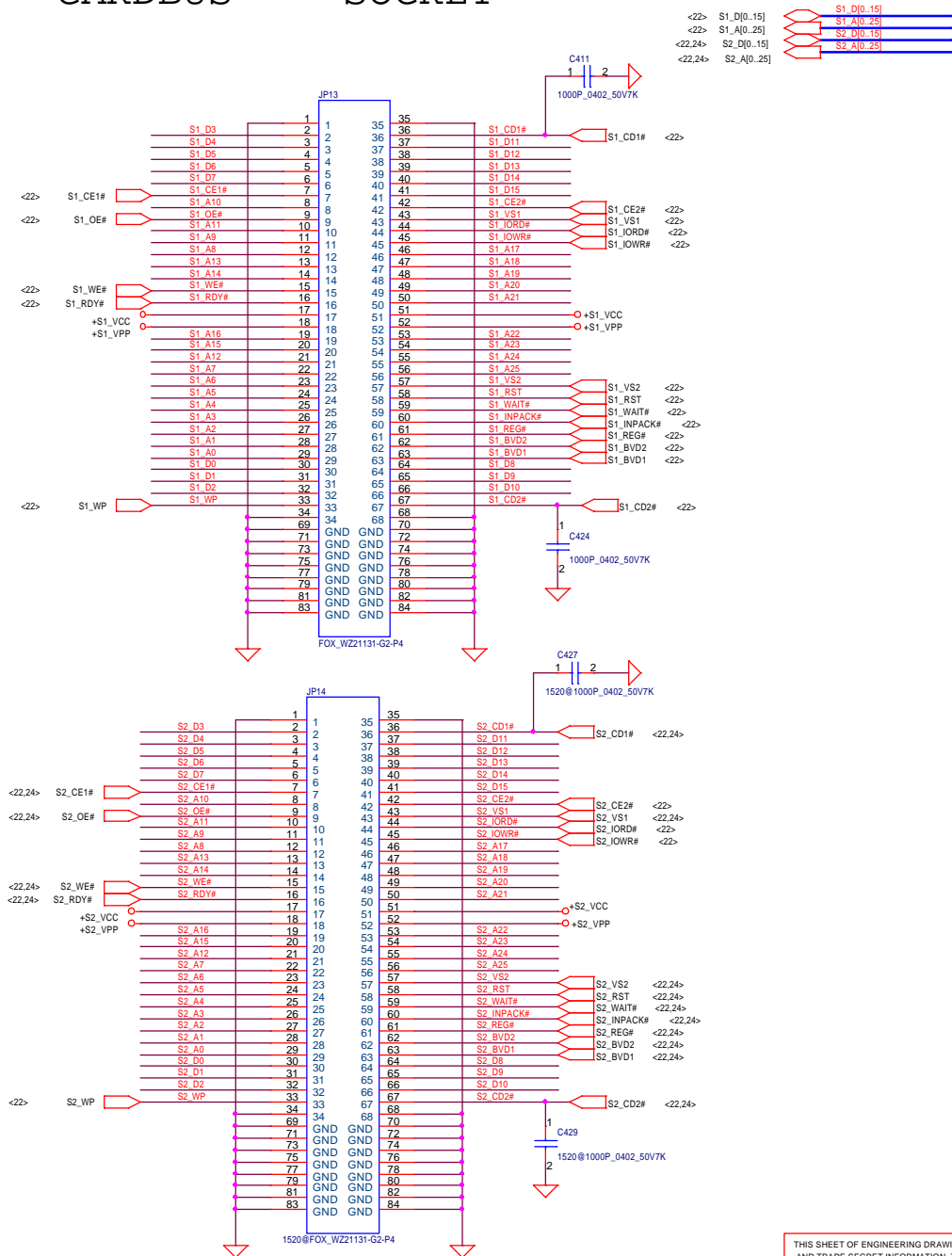


Compal Electronics, Inc.		
Title IEEE 1394 CONTROLLER		
Size	Document Number LA-1851	Rev 0.5
Date	Thursday, October 16, 2003	Sheet 21 of 50

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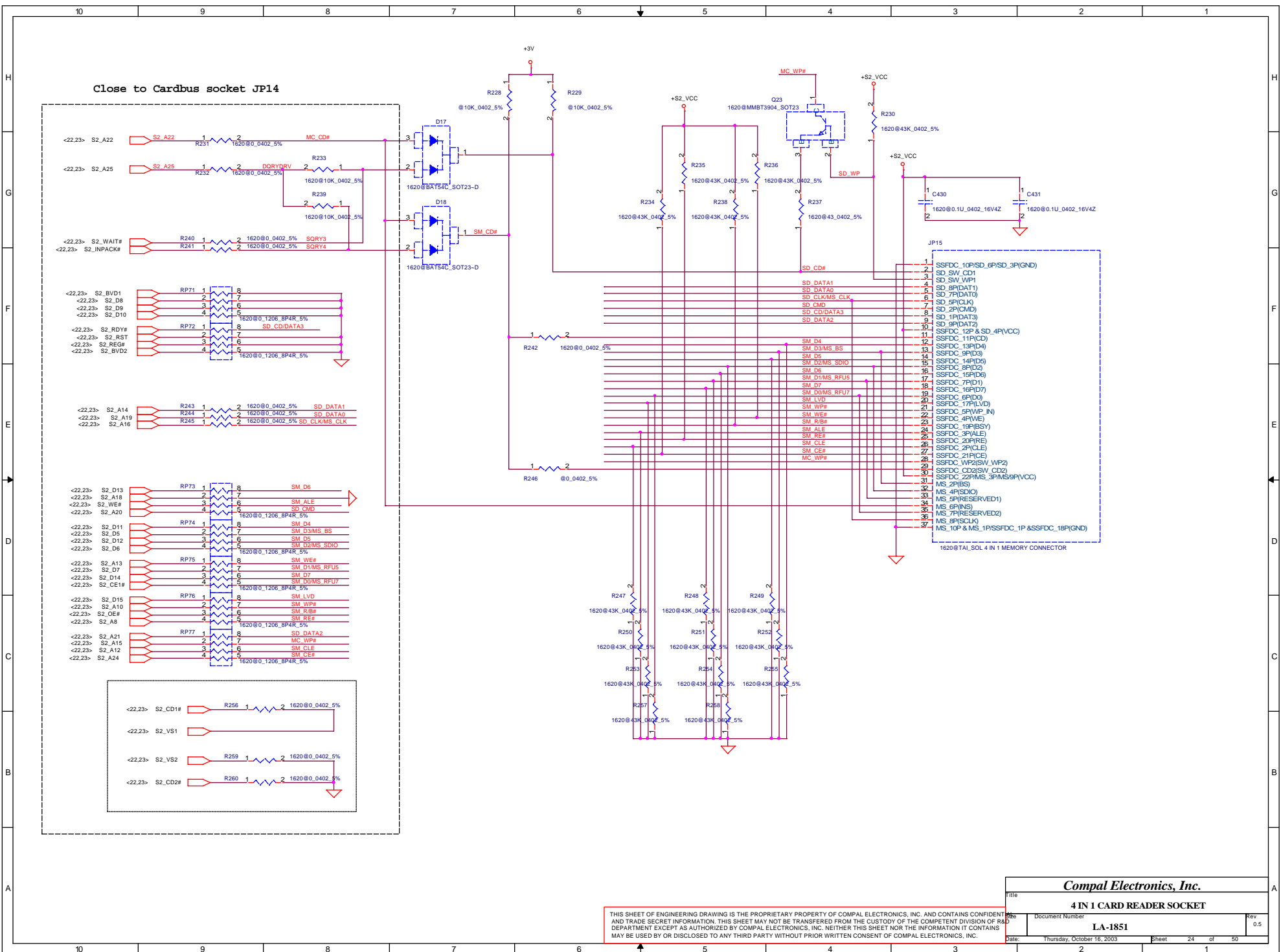
PCMCIA POWER CTRL.

CARDBUS SOCKET

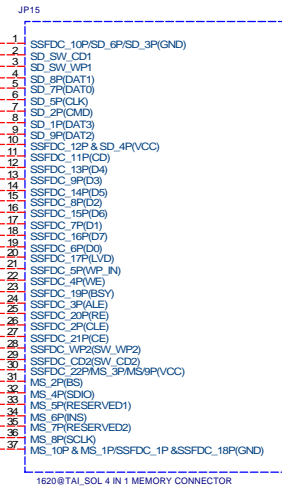
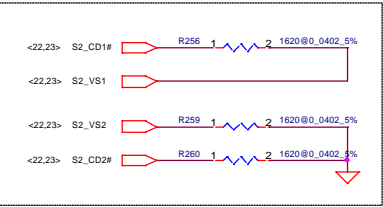
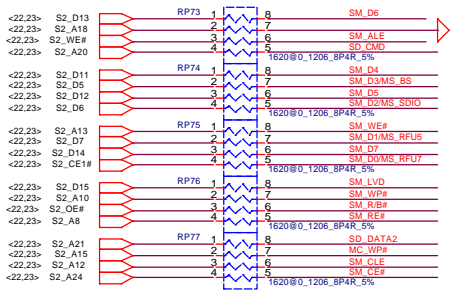
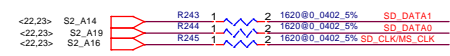
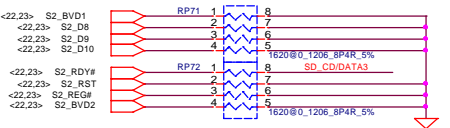
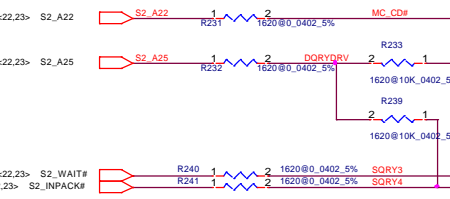


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Compal Electronics, Inc.		
File	CARD BUS SOCKET	
Size	Document Number	Rev
	LA-1851	0.5
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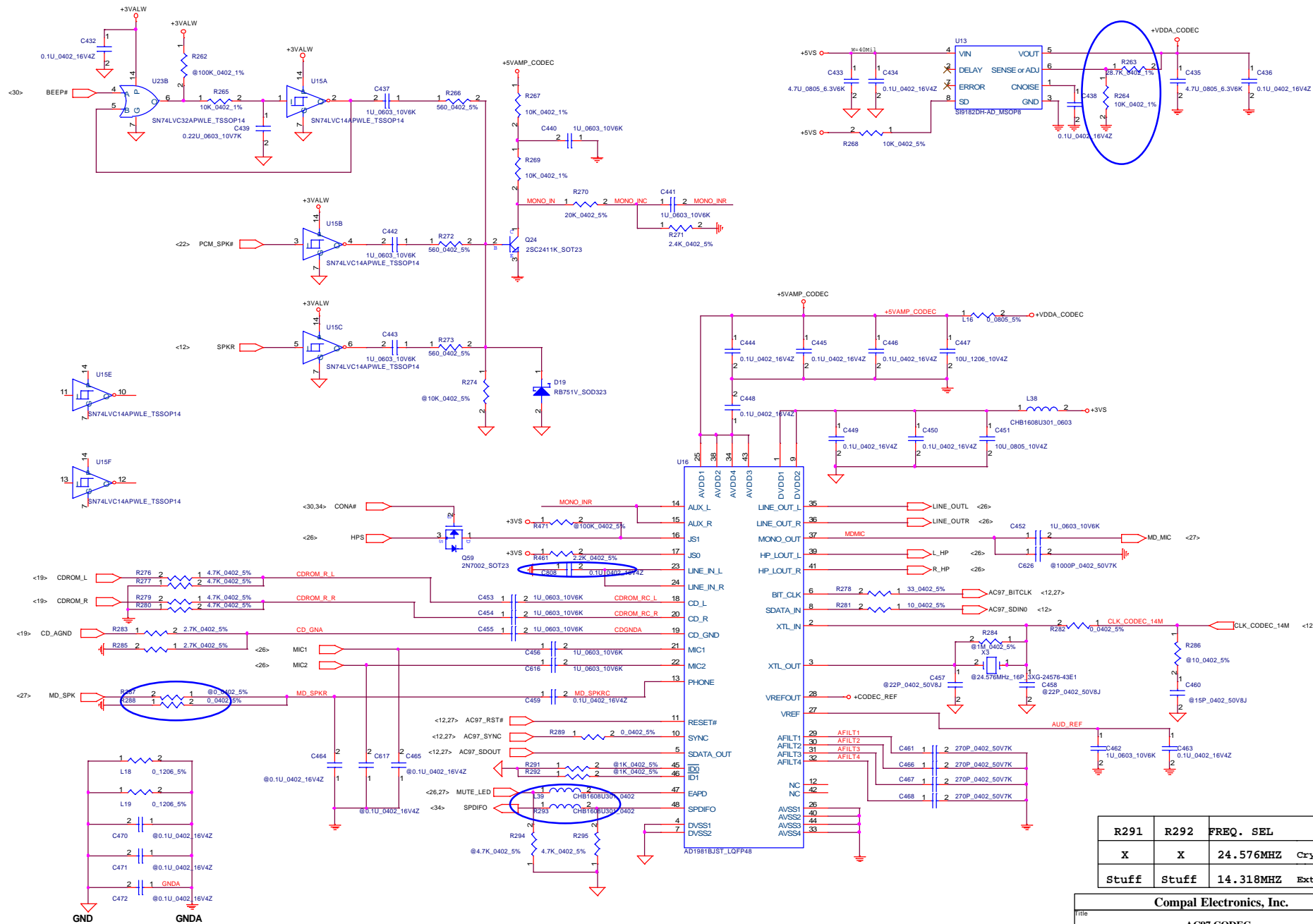


Close to Cardbus socket JP14



Compal Electronics, Inc.	
4 IN 1 CARD READER SOCKET	
File	Document Number
LA-1851	
Date: Thursday, October 16, 2003	Sheet 24 of 50
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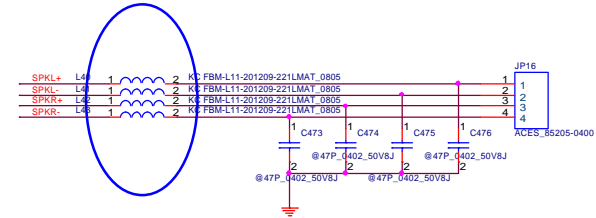
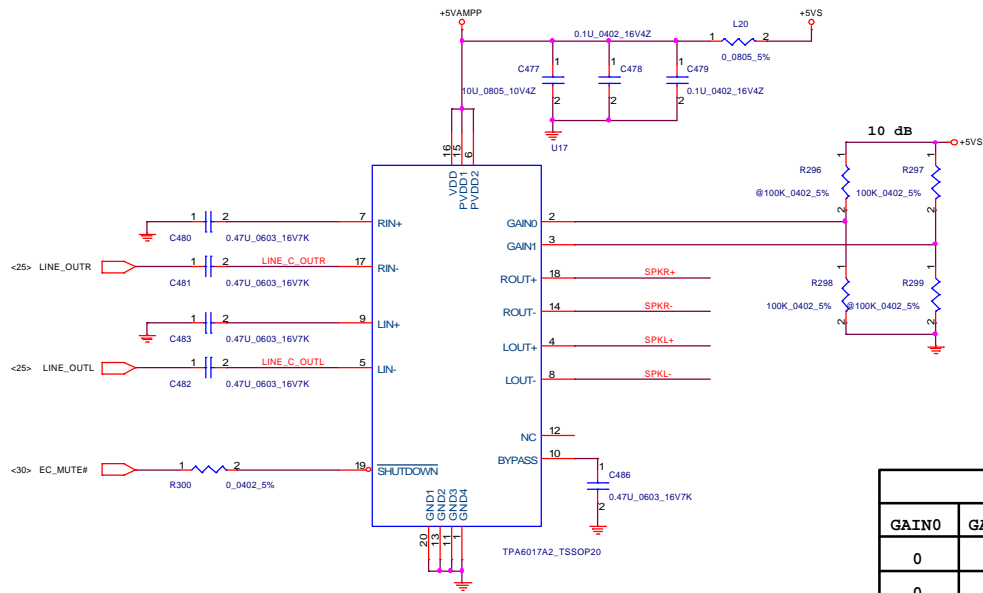
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R291	R292	FREQ. SEL	
X	X	24.576MHZ	Crystal
Stuff	Stuff	14.318MHZ	External

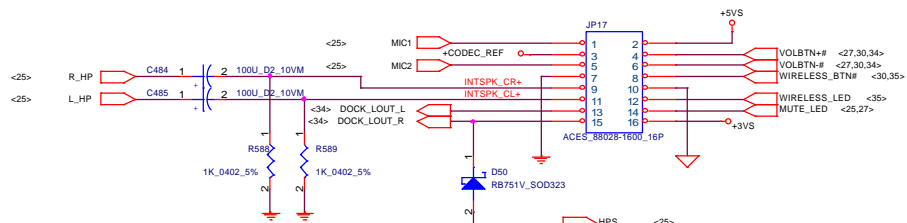
Compal Electronics, Inc.			
AC97 CODEC			
Title	Document Number	Rev	
	LA-1851	0.5	
Date	Thursday, October 16, 2003	Sheet	25 of 50

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Gain Settings		
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

AUDIO CONNECTOR



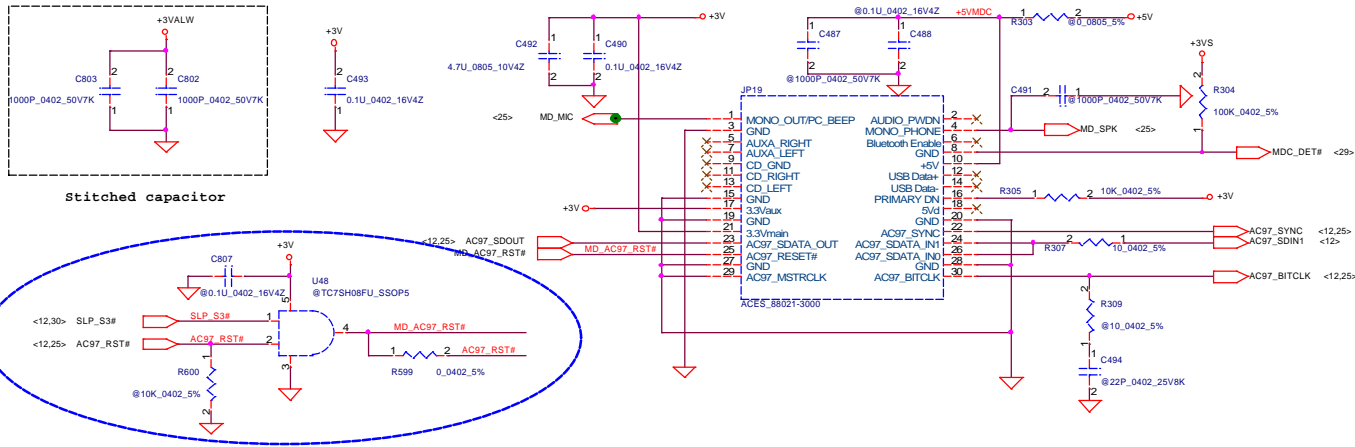
Compal Electronics, Inc.

AMP & Audio Jack

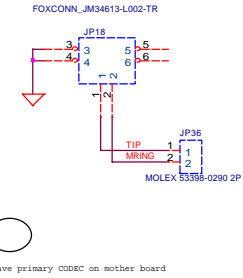
Title		Document Number		Rev
		LA-1851		0.5
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MDC Conn.

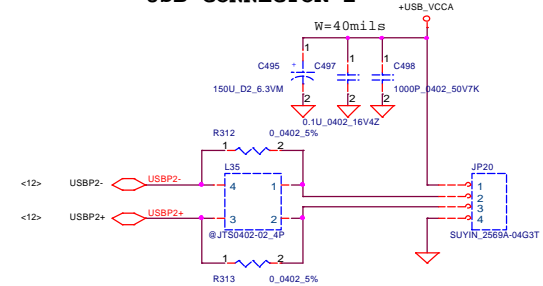


RJ11 CONN.

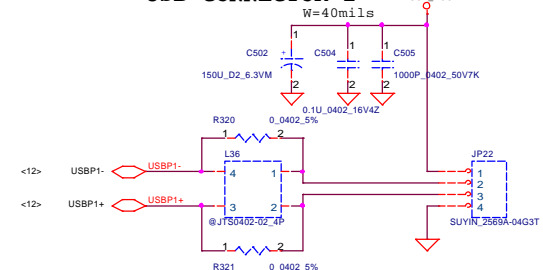


0: Have primary CODEC on mother board

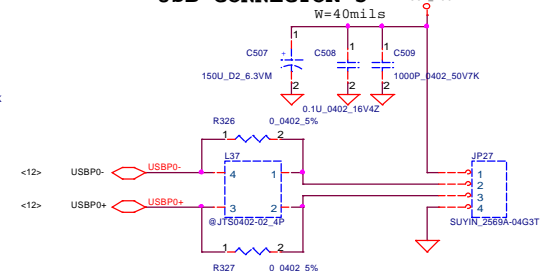
USB CONNECTOR 1



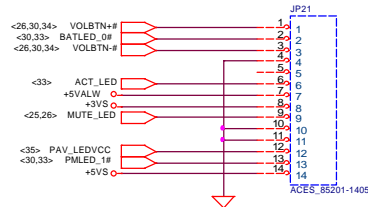
USB CONNECTOR 2



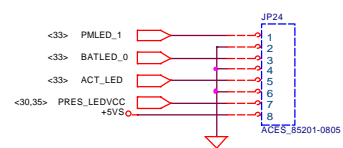
USB CONNECTOR 3



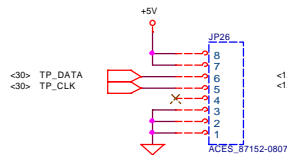
Front Board CONNECTOR Pavilion only



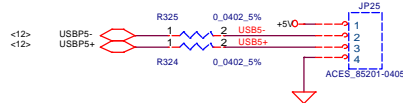
Front Board CONNECTOR PRESARIO only



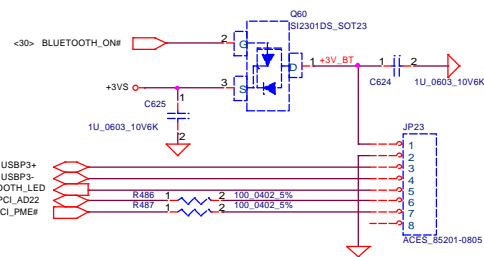
TP CONNECTOR



USB KEY

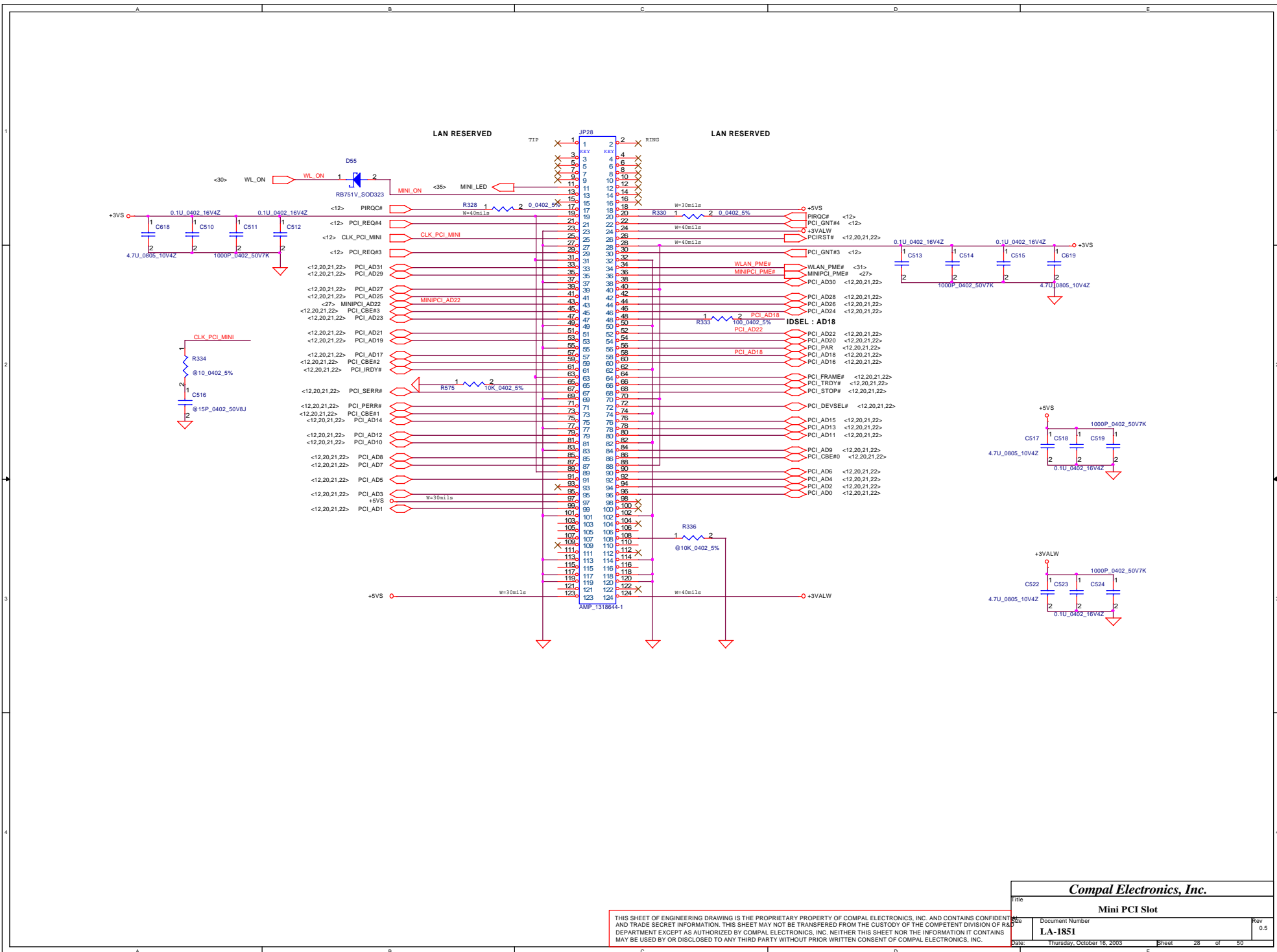


BT CONNECTOR



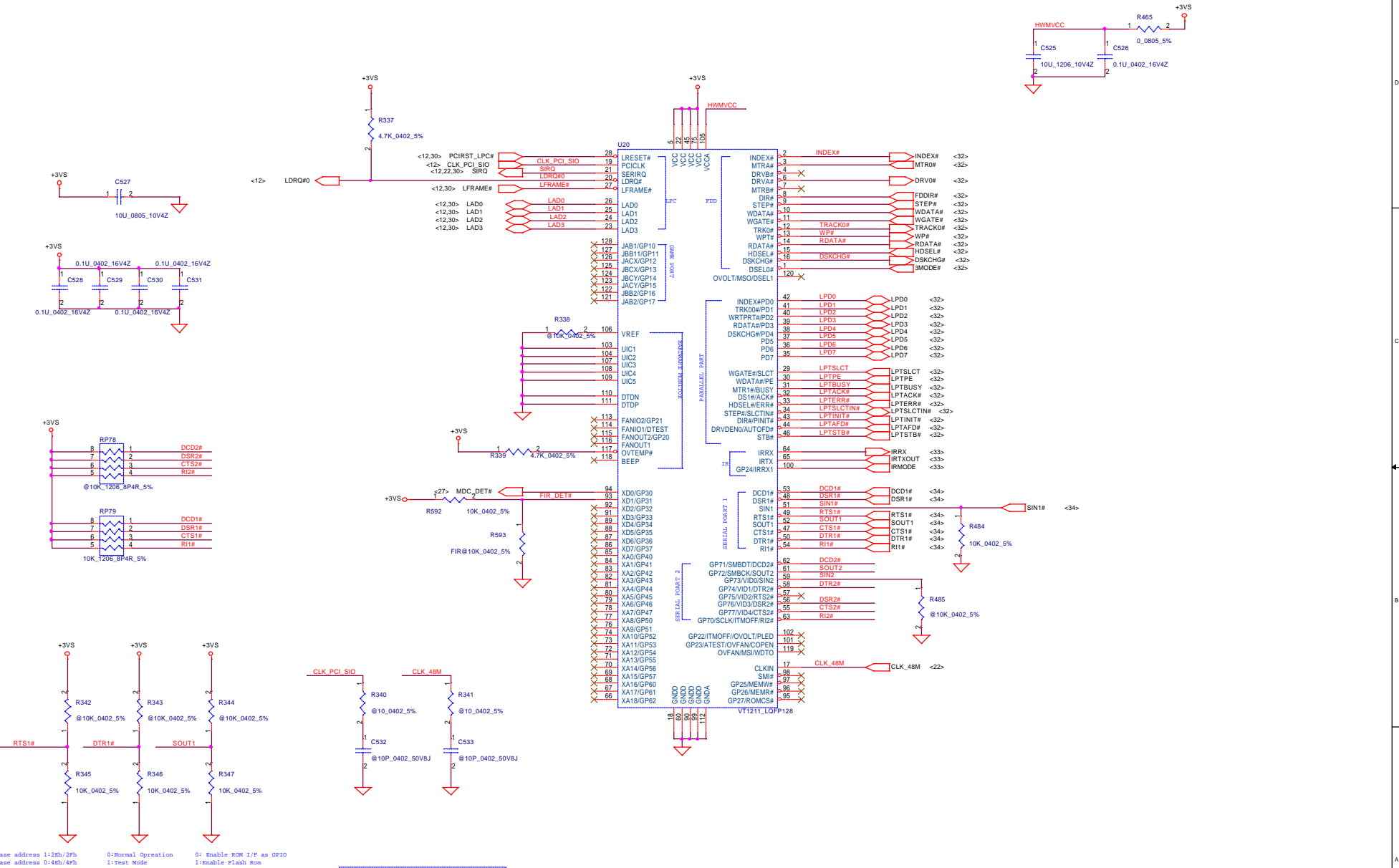
Compal Electronics, Inc.		
MDC , Bluetooth & USB CONN.		
File	Document Number	Rev
	LA-1851	0.5
Date	Friday, October 17, 2003	Sheet 27 of 50

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Compal Electronics, Inc.		
Mini PCI Slot		
Doc No	Document Number	Rev
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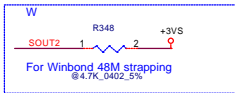


Base address 1:2Kh/3Ph
 Base address 0:4Kh/4Ph

0:Normal operation
 1:Test Mode

0: Enable ROM I/P as GP10
 1:Enable Flash Rom

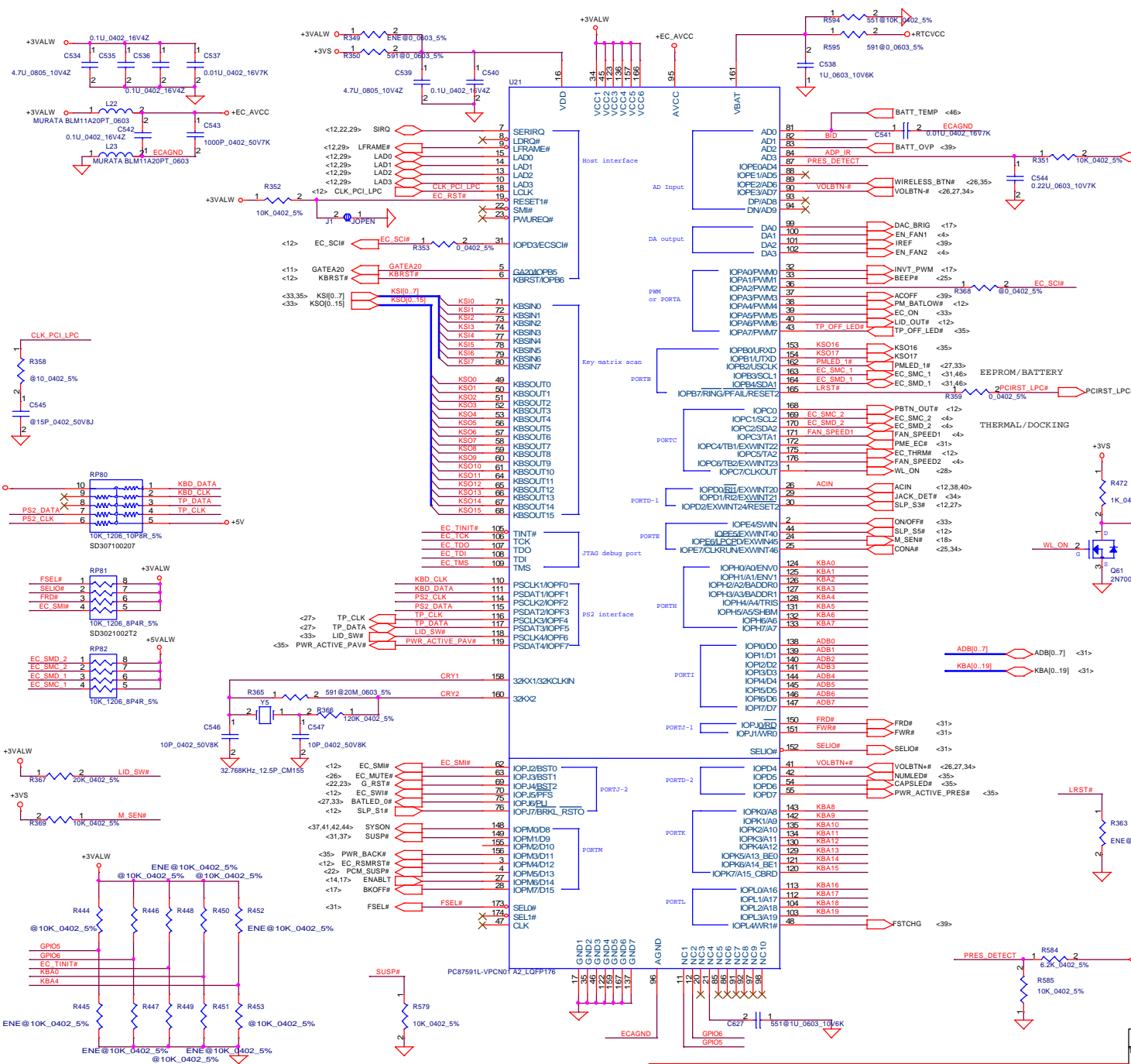
Super I/O strapping for VT1211



For Winbond 48M strapping @4.7K_0402_5%

Compal Electronics, Inc.		
Title LPC SUPER I/O VIA VT1211		
Size	Document Number	Rev
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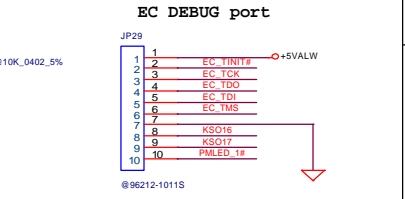
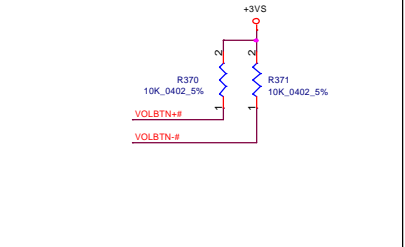
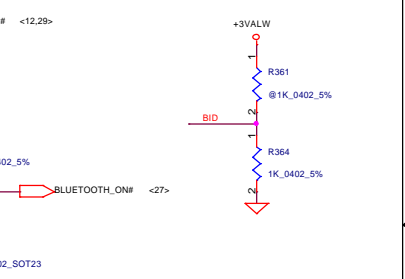
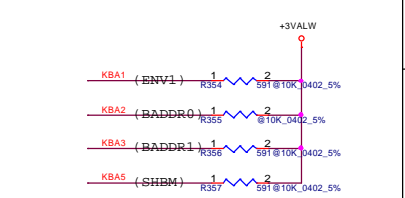
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I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL+1)
1 1	Reserved	

	ENVO	ENV1	TRIS
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

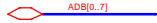
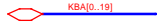
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



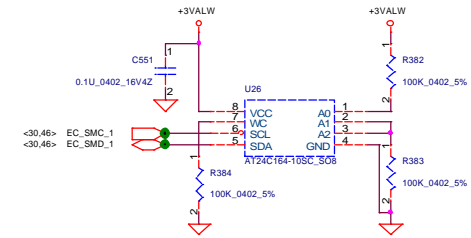
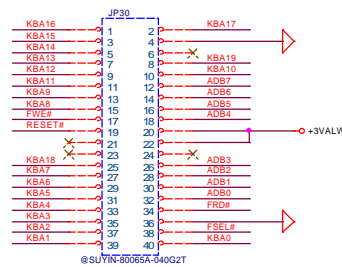
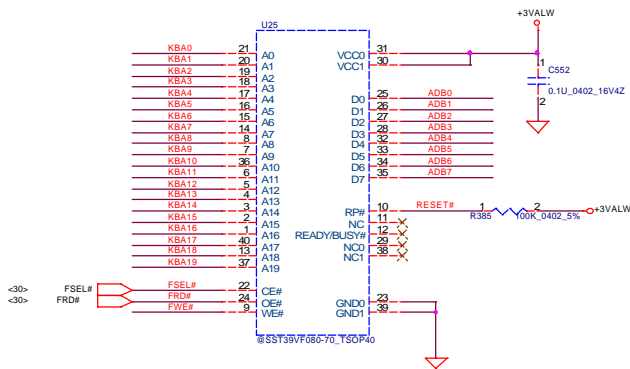
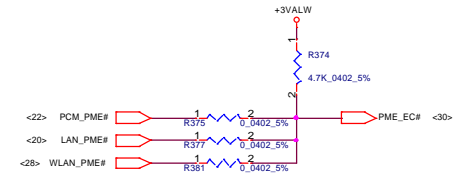
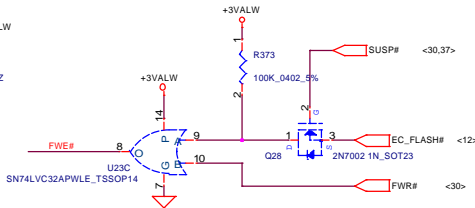
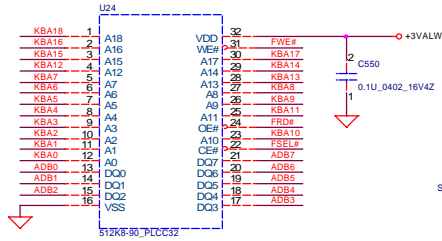
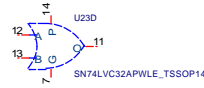
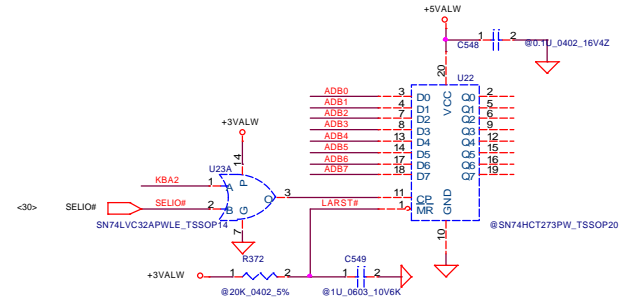
EC DEBUG port		
JP29	Signal	Value
1	EC_TINIT#	+5VALW
2	EC_TCK	
3	EC_TDO	
4	EC_TDI	
5	EC_TMS	
6	EC_TMS	
7		
8	KSD16	
9	KSD17	
10	PMLED_1#	

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INPUT

<30> ADB[0..7]  ADB[0..7]
 <30> KBA[0..19]  KBA[0..19]

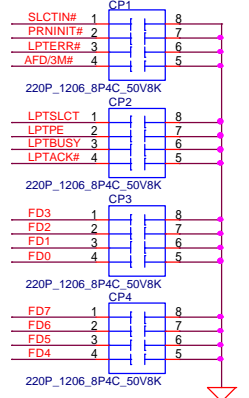
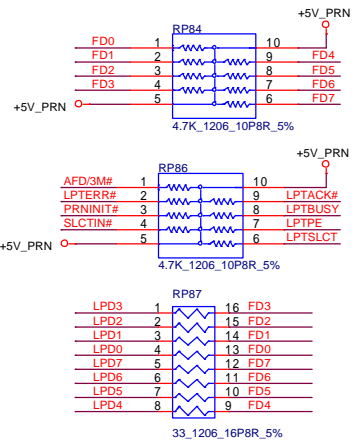
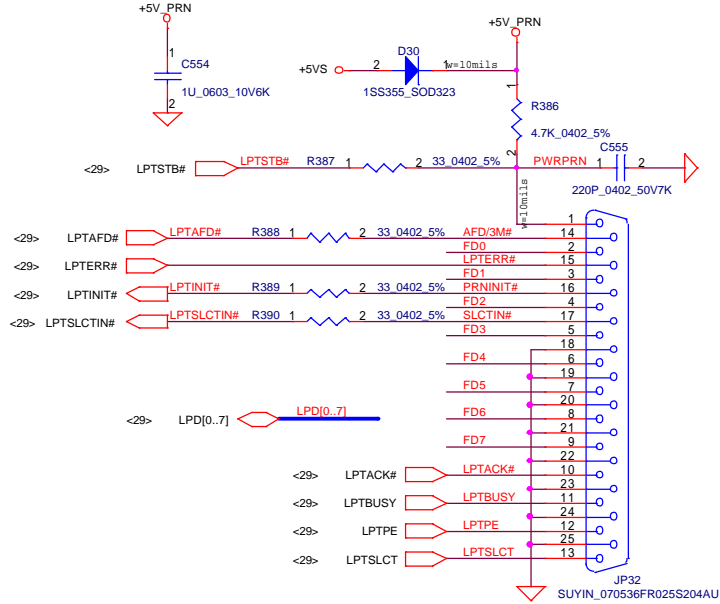
OUTPUT



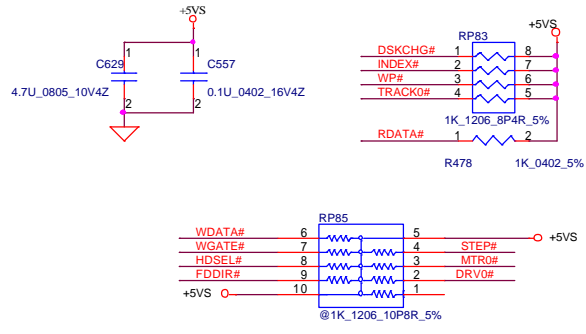
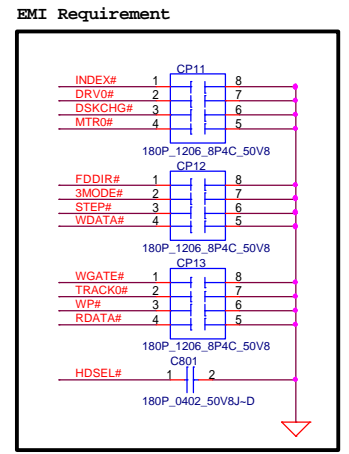
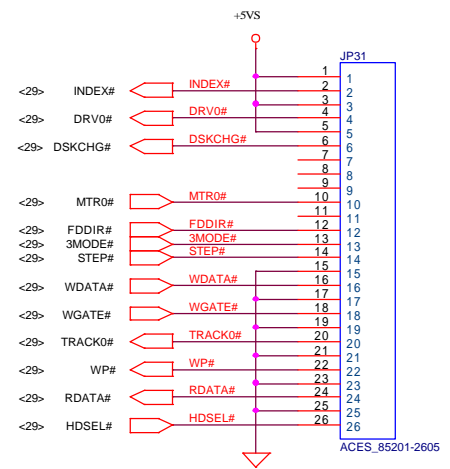
Compal Electronics, Inc.		
BIOS & EC I/O Port		
Part Number	Document Number	Rev
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Parallel Port



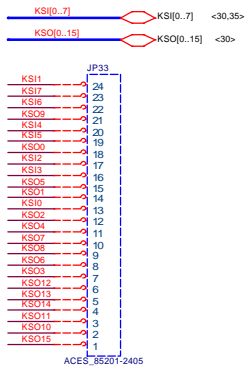
FDD CONN.



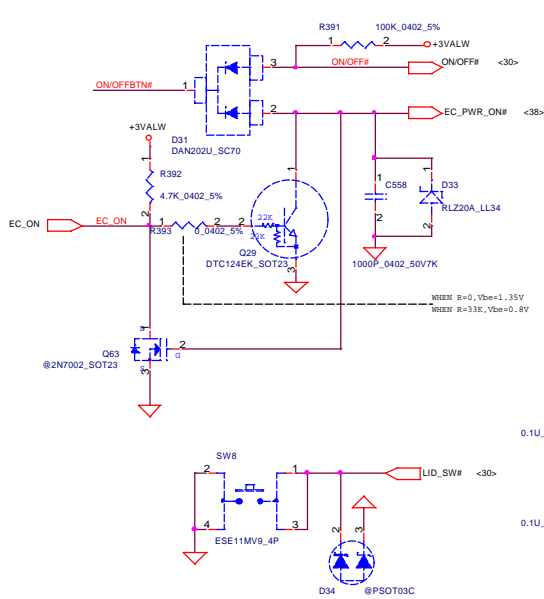
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Title		
Parallel port & FDD Connector		
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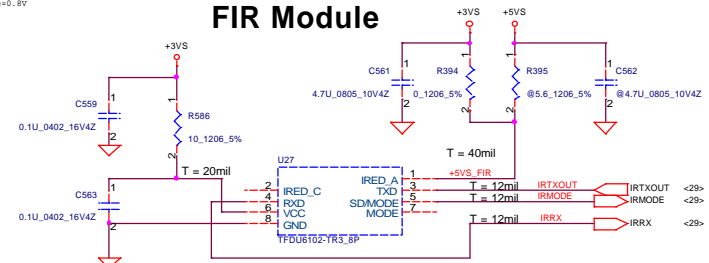
INT_KBD CONN.



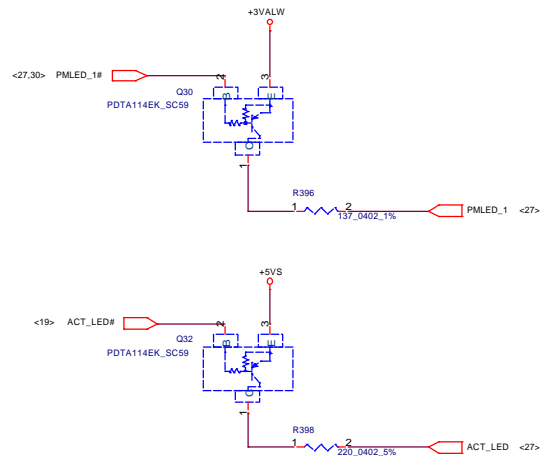
Power BTN



FIR Module

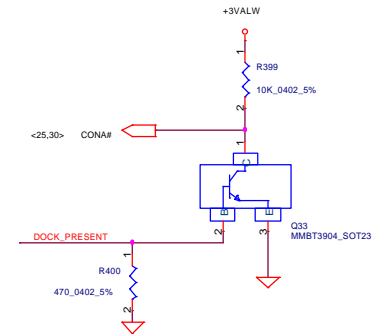
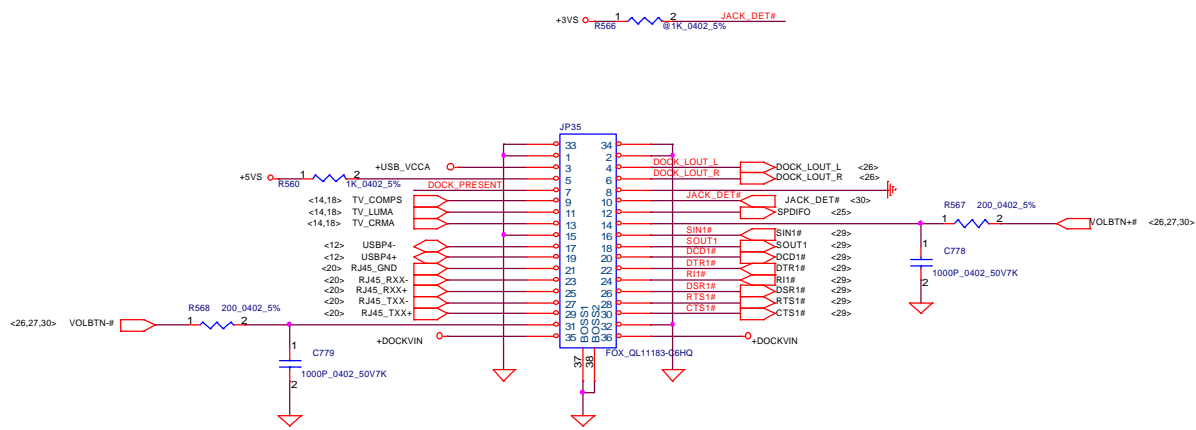


Touch Pad & Status LED Conn.

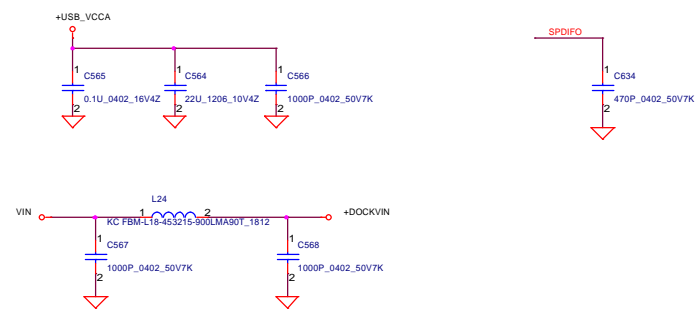
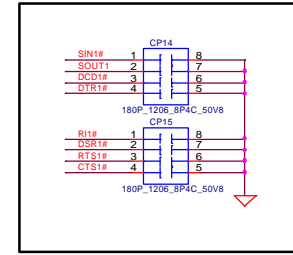


Compal Electronics, Inc.		
KBD,ON/OFF,T/P,LED & FIR		
Doc#	Document Number	Rev
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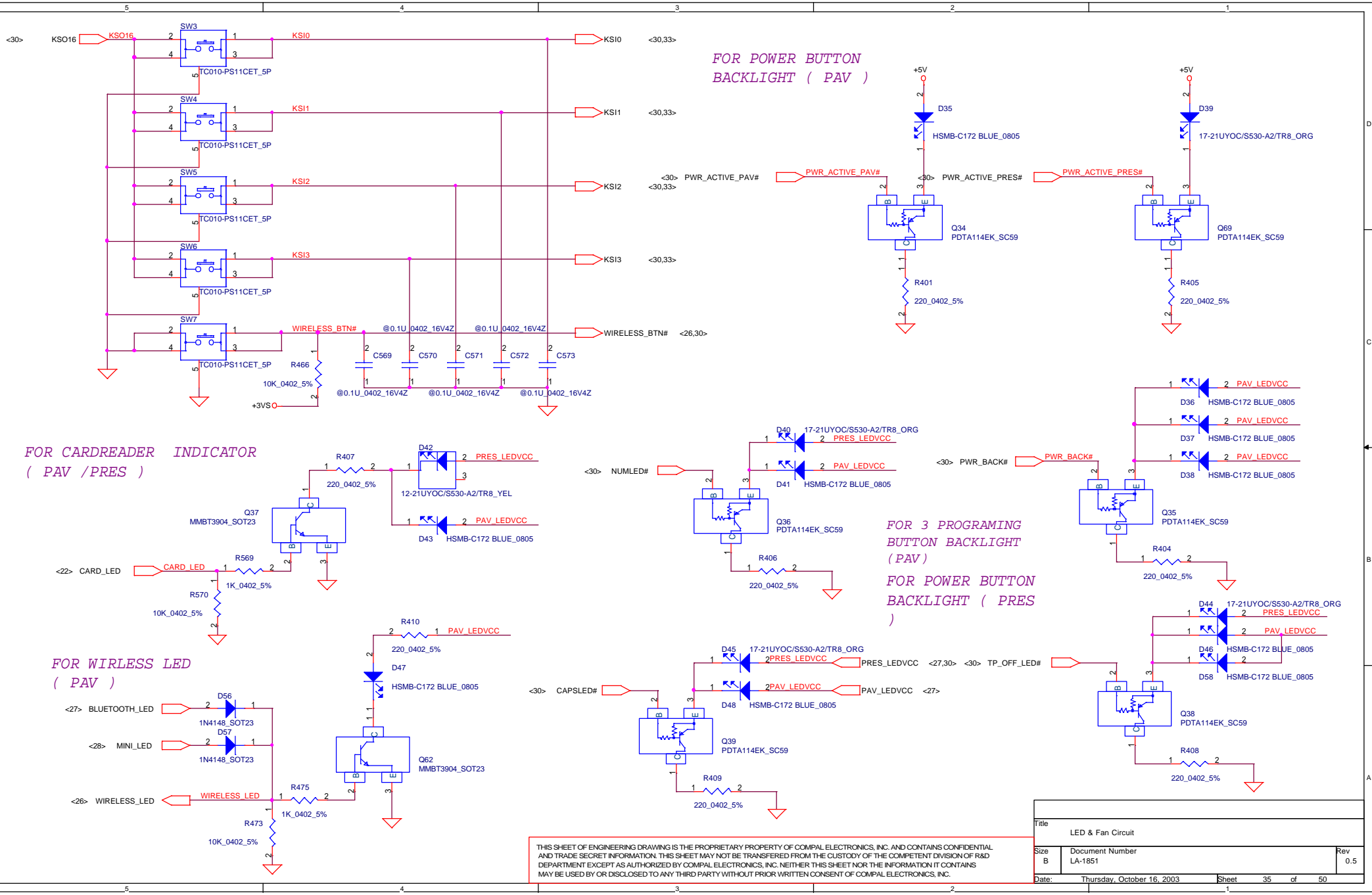


EMI Requirement



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Compal Electronics, Inc.		
SPR Connector		
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FOR POWER BUTTON
BACKLIGHT (PAV)

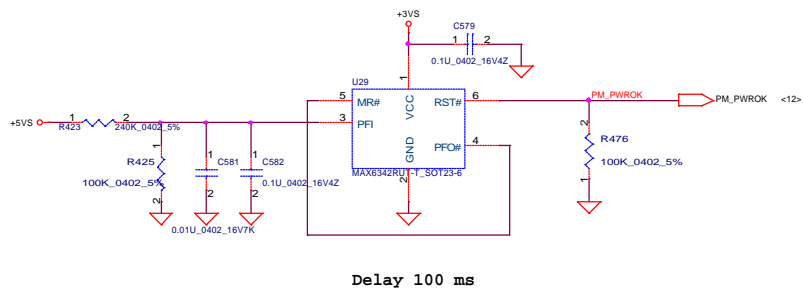
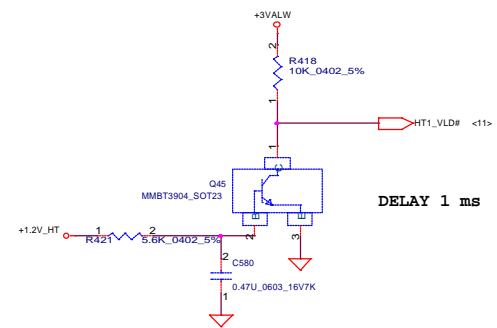
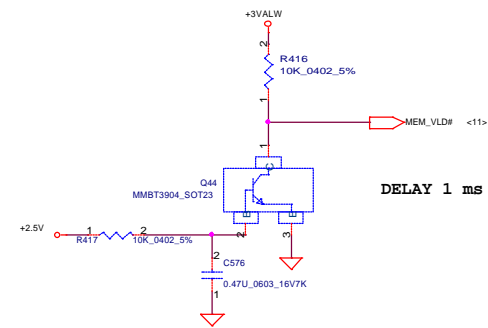
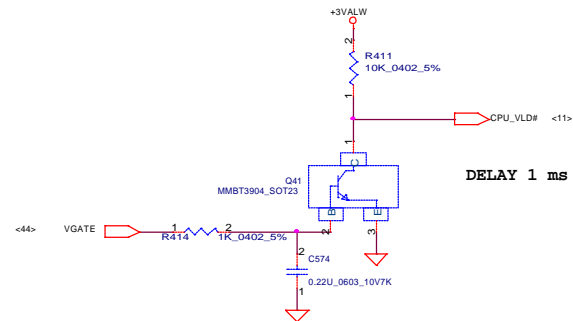
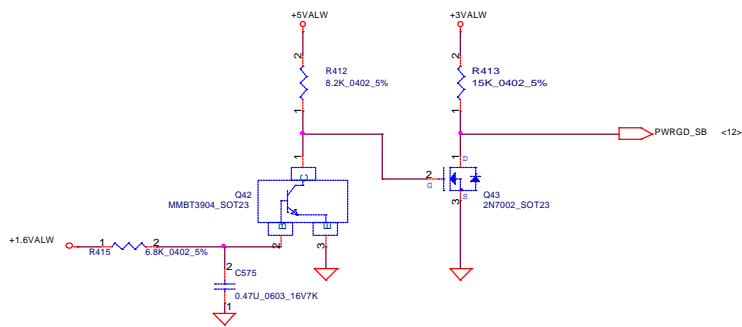
FOR CARDREADER INDICATOR
(PAV /PRES)

FOR 3 PROGRAMING
BUTTON BACKLIGHT
(PAV)
FOR POWER BUTTON
BACKLIGHT (PRES)

FOR WIRLESS LED
(PAV)

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Title		
LED & Fan Circuit		
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Delay 100 ms

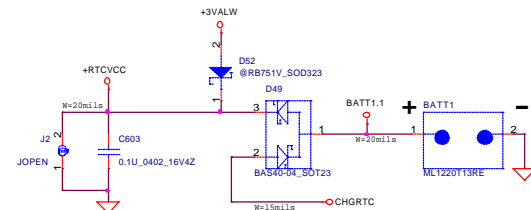
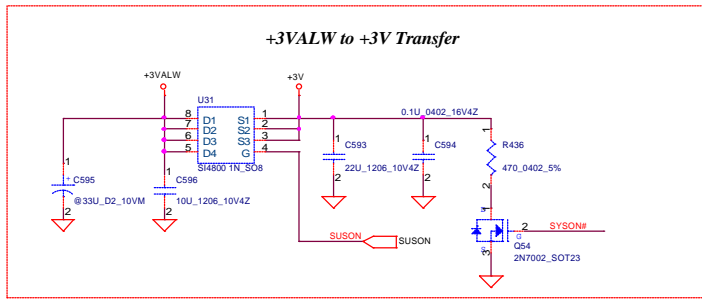
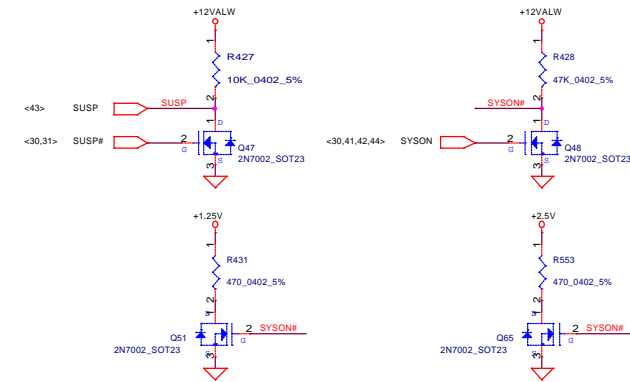
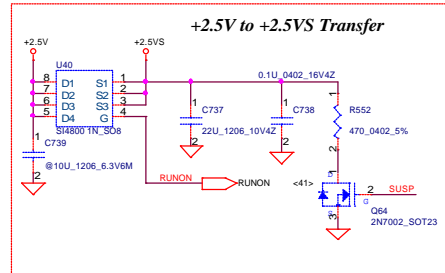
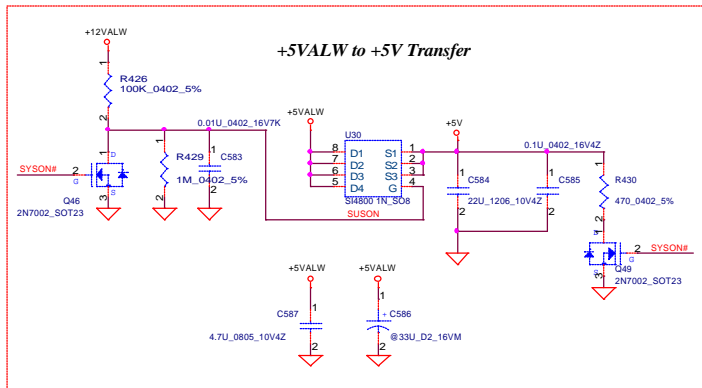
DELAY 1 ms

DELAY 1 ms

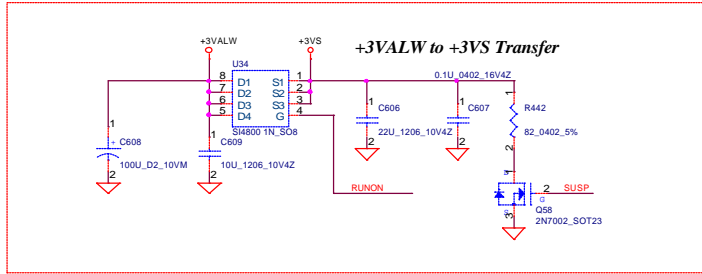
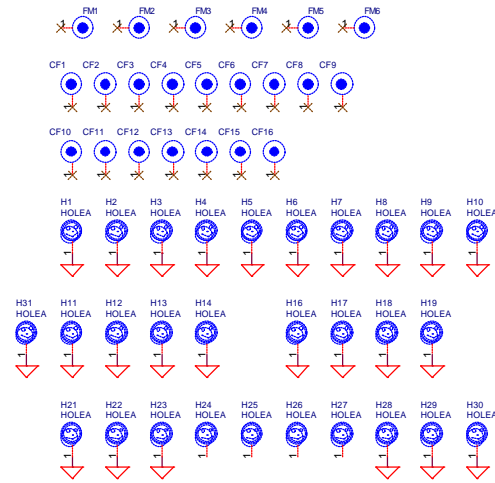
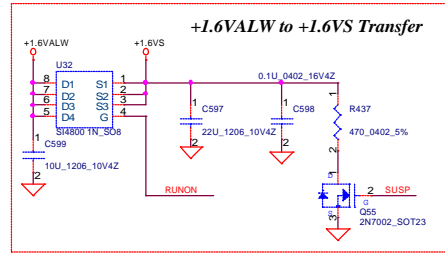
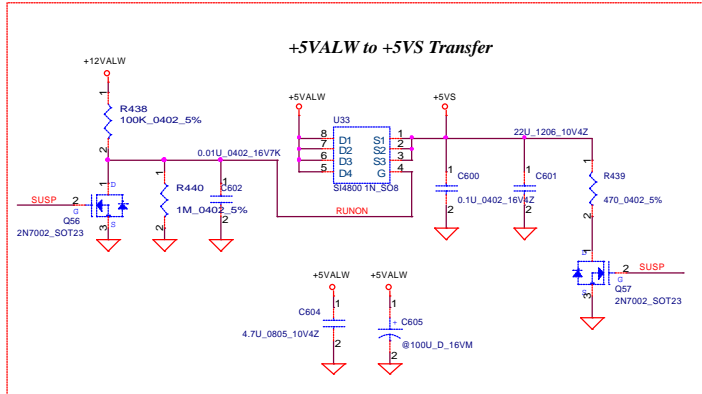
DELAY 1 ms

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Compal Electronics, Inc.	
Power OK/Reset Conn. & MUTE Switch	
File	Document Number
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For customer request
,they don't wanna
charge RTC

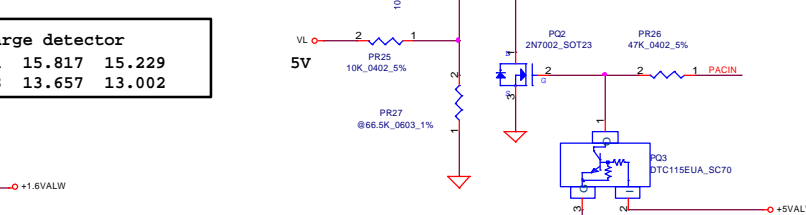
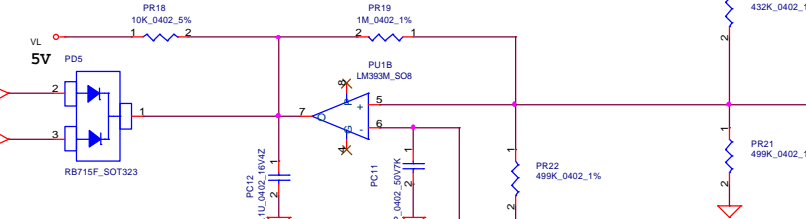
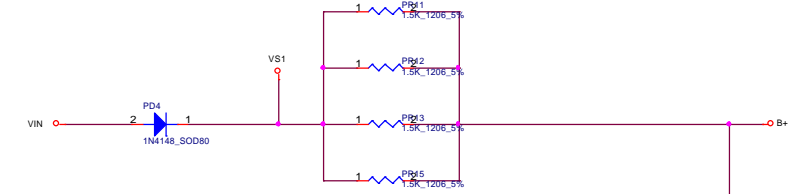
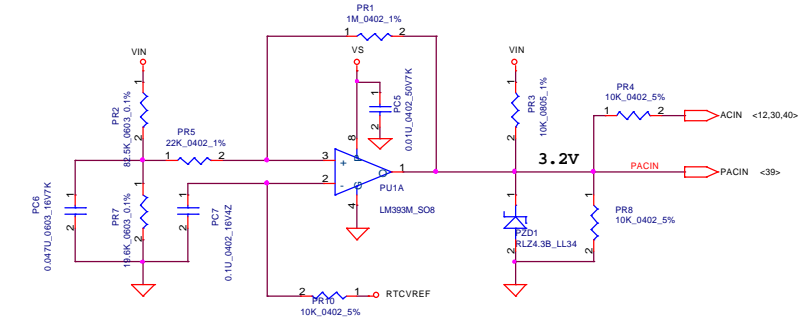


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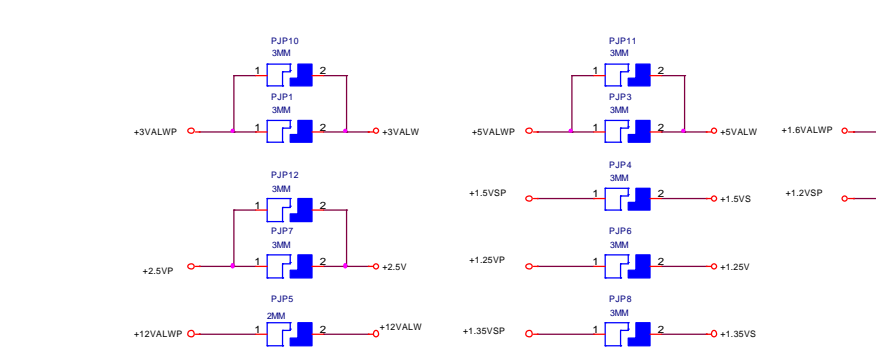
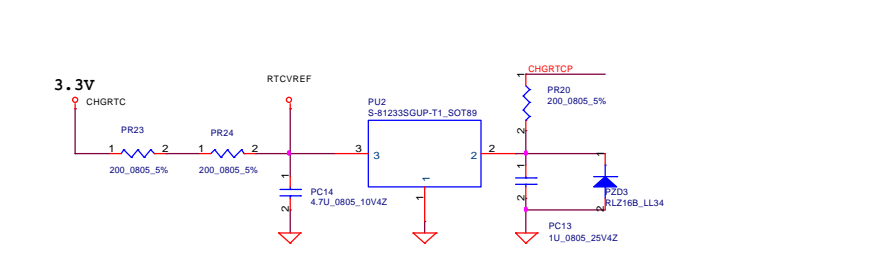
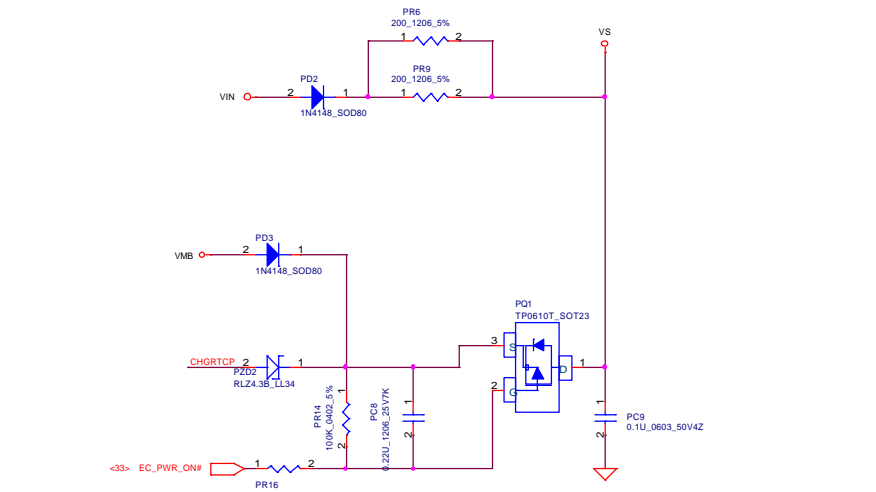
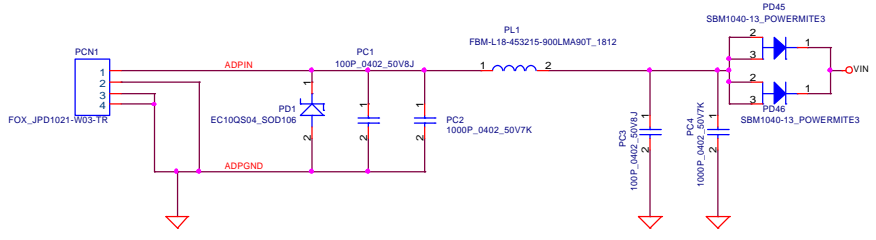
Compal Electronics, Inc.			
DC/DC Circuit			
File	Document Number	Rev	
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Detector

VIN detector
 17.945 17.343 16.757
 17.372 16.782 16.207



ACIN
 Precharge detector
 16.421 15.817 15.229
 14.108 13.657 13.002



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Compal Electronics, Inc.		
Title	Detector	
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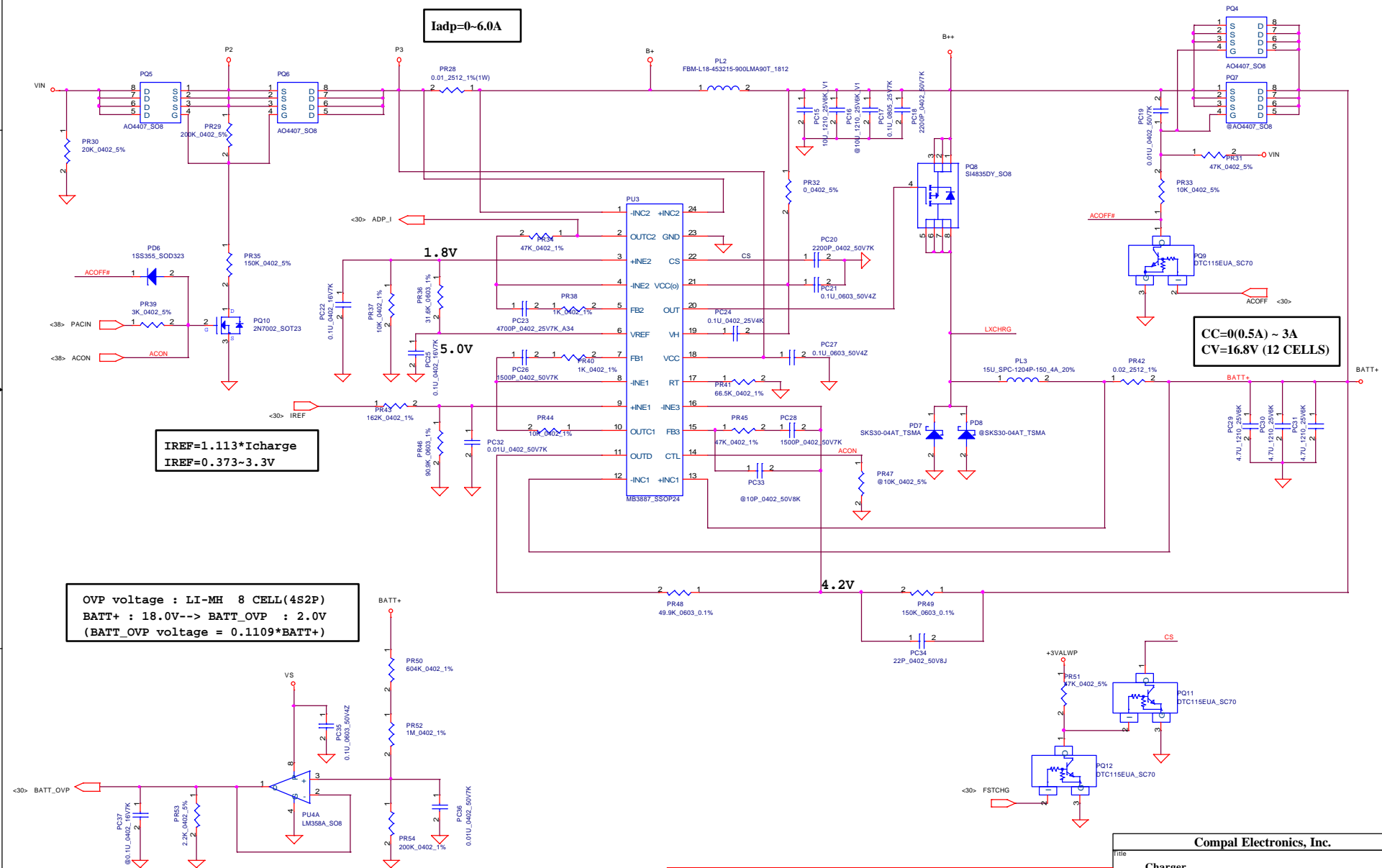
Charger

I_{adp}=0-6.0A

**CC=0(0.5A) ~ 3A
CV=16.8V (12 CELLS)**

**I_{REF}=1.113*I_{charge}
I_{REF}=0.373~3.3V**

**OVP voltage : LI-MH 8 CELL(4S2P)
BATT+ : 18.0V--> BATT_OVP : 2.0V
(BATT_OVP voltage = 0.1109*BATT+)**



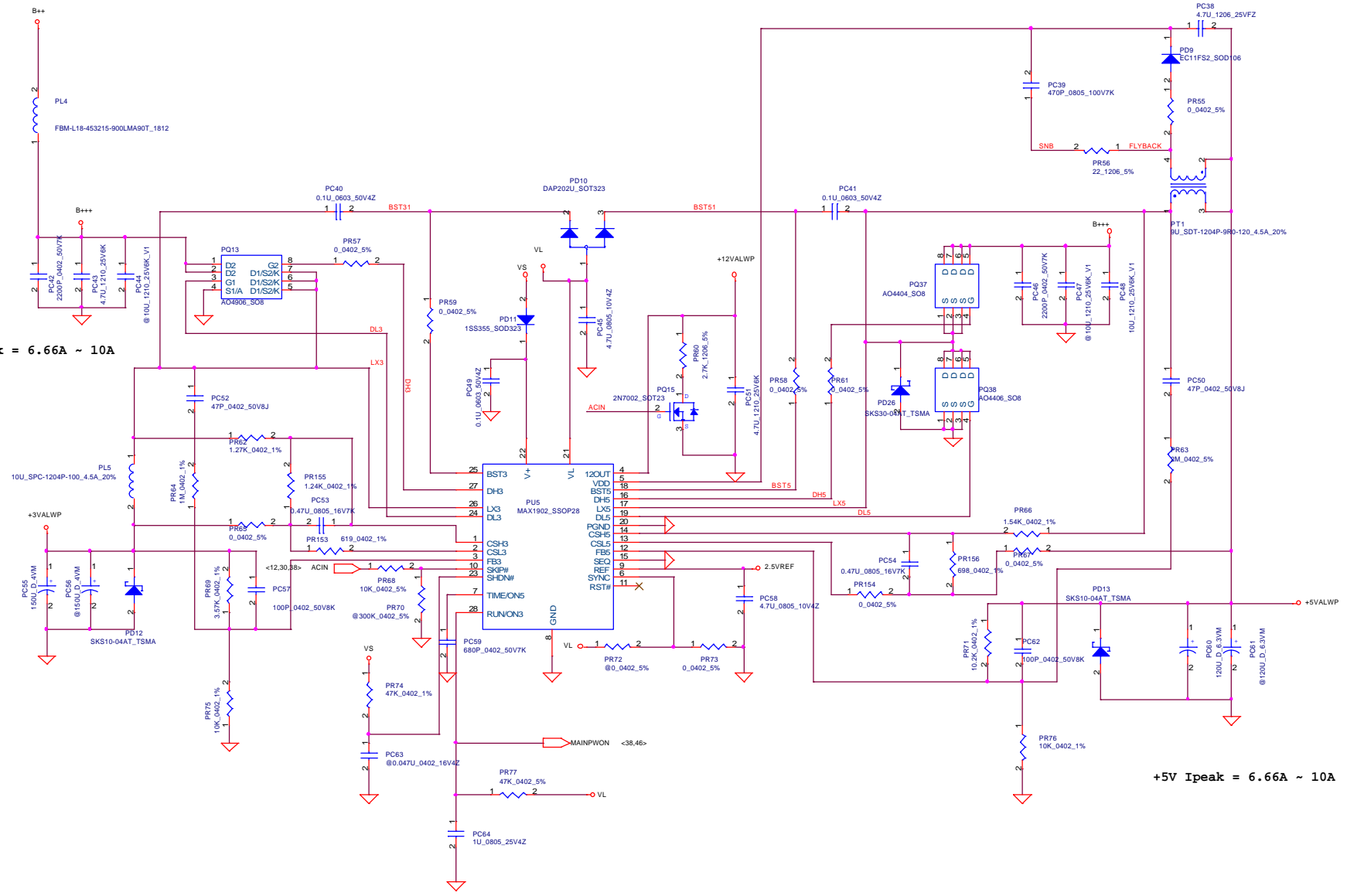
Compal Electronics, Inc.		
Charger		
File	Document Number	Rev
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+3.3V/+5V/+12V

+3.3V Ipeak = 6.66A ~ 10A

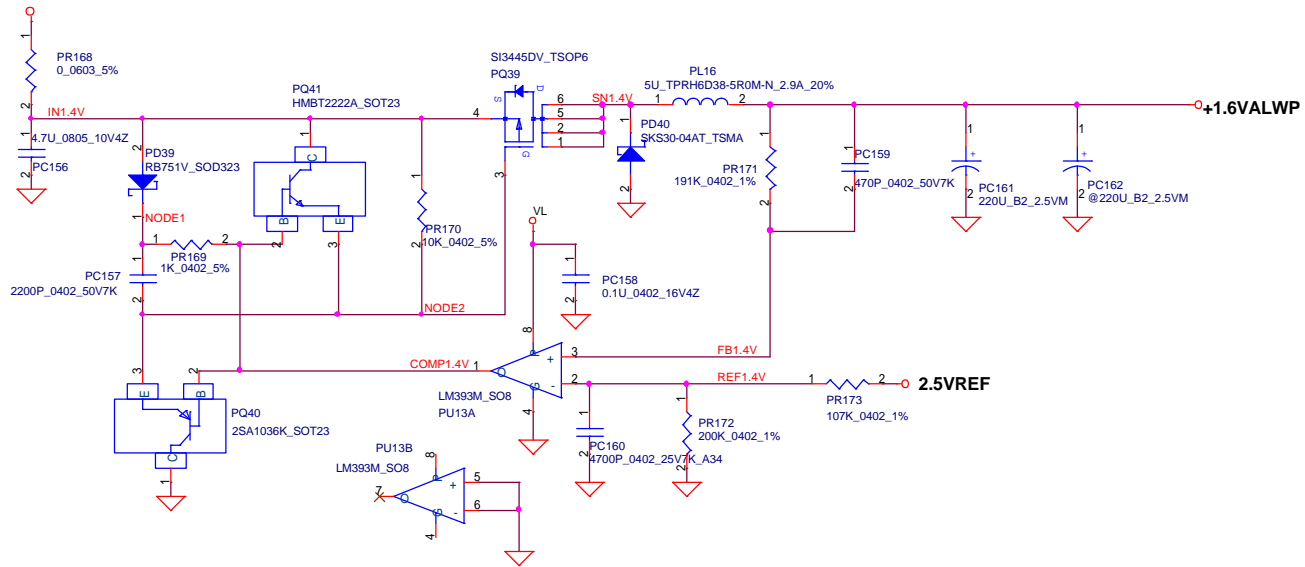
+5V Ipeak = 6.66A ~ 10A



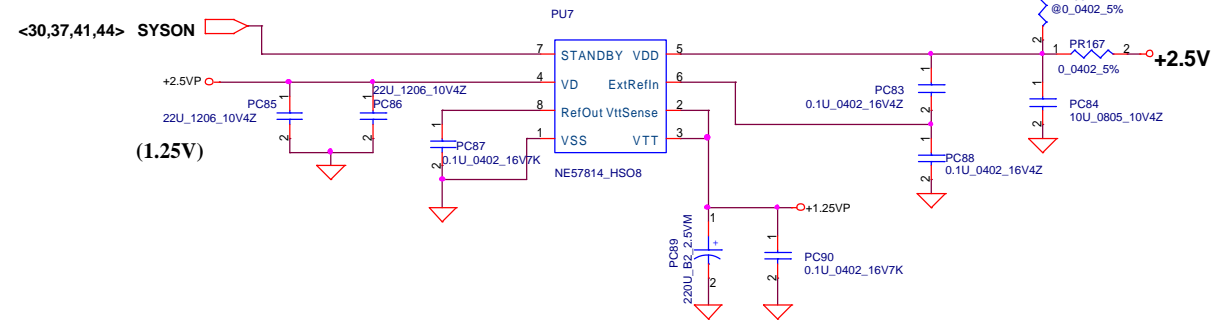
Compal Electronics, Inc.	
Title	3.3V / 5V / 12V
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B	LA-1851
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+5VALWP

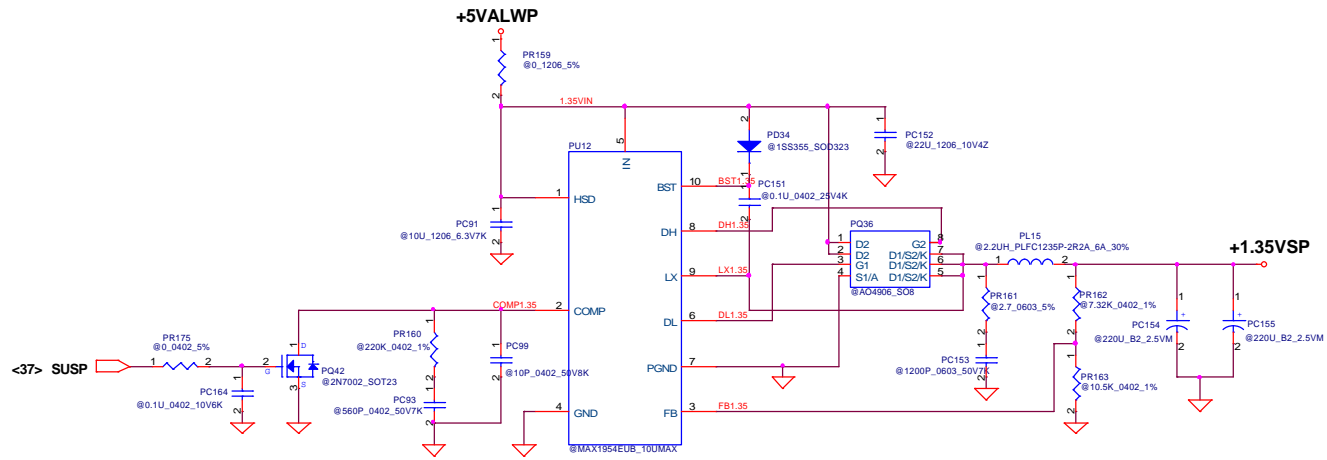
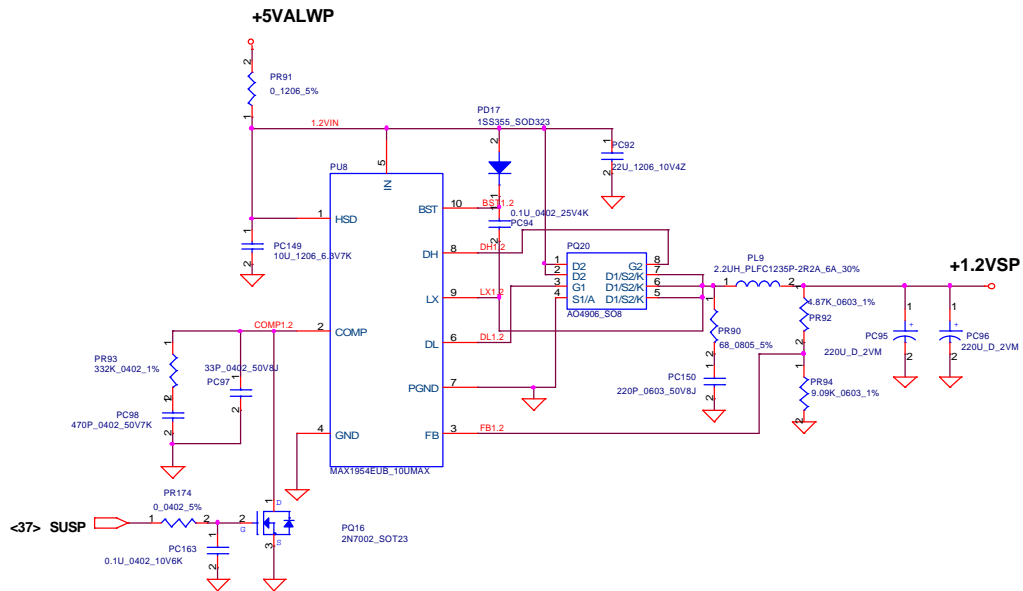


+2.5VP



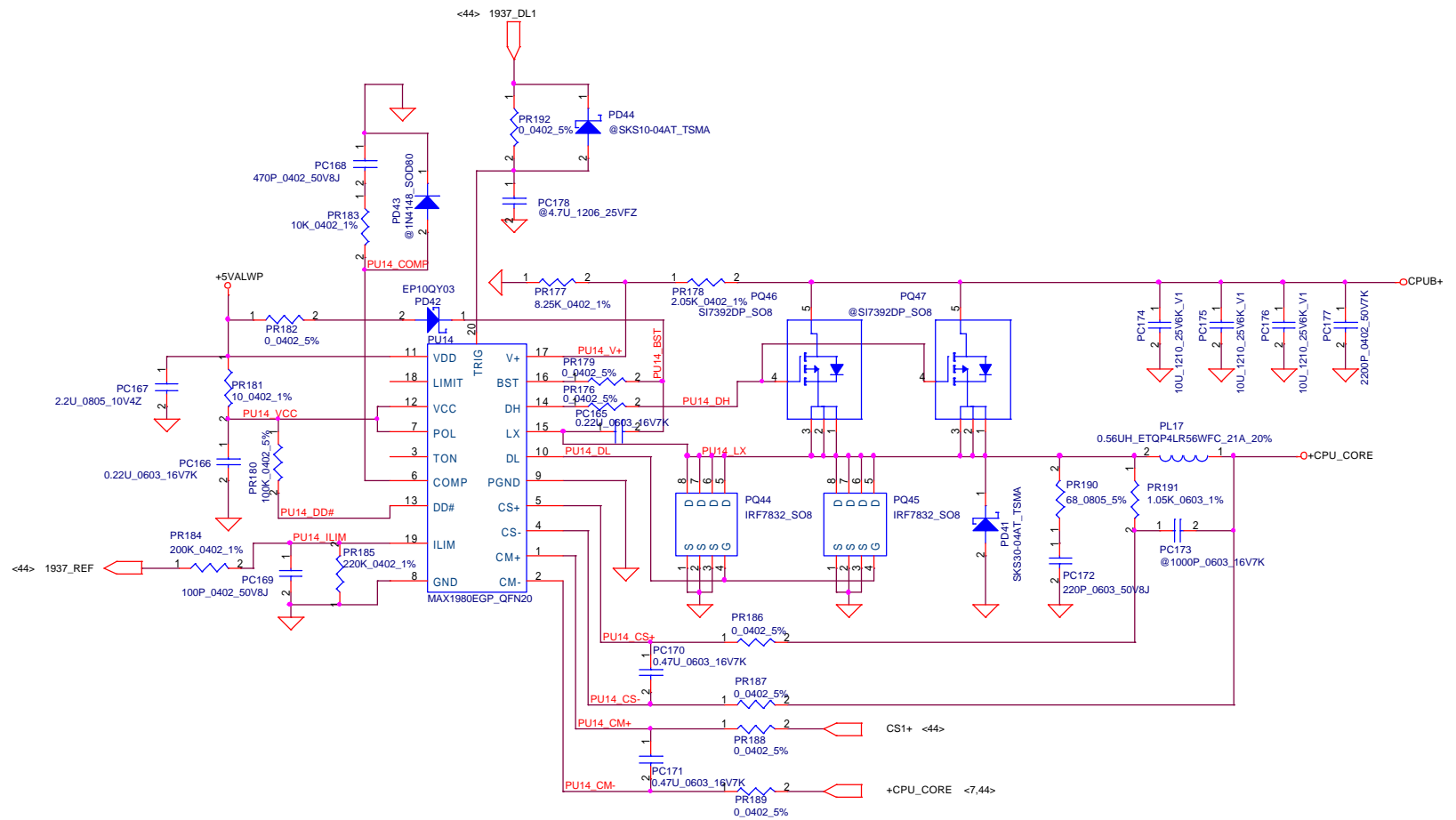
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COMPAL ELECTRONICS, INC		
Title		
+1.6VALWP & +1.25VP		
Size B	Document Number LA-1581	Rev 0.5
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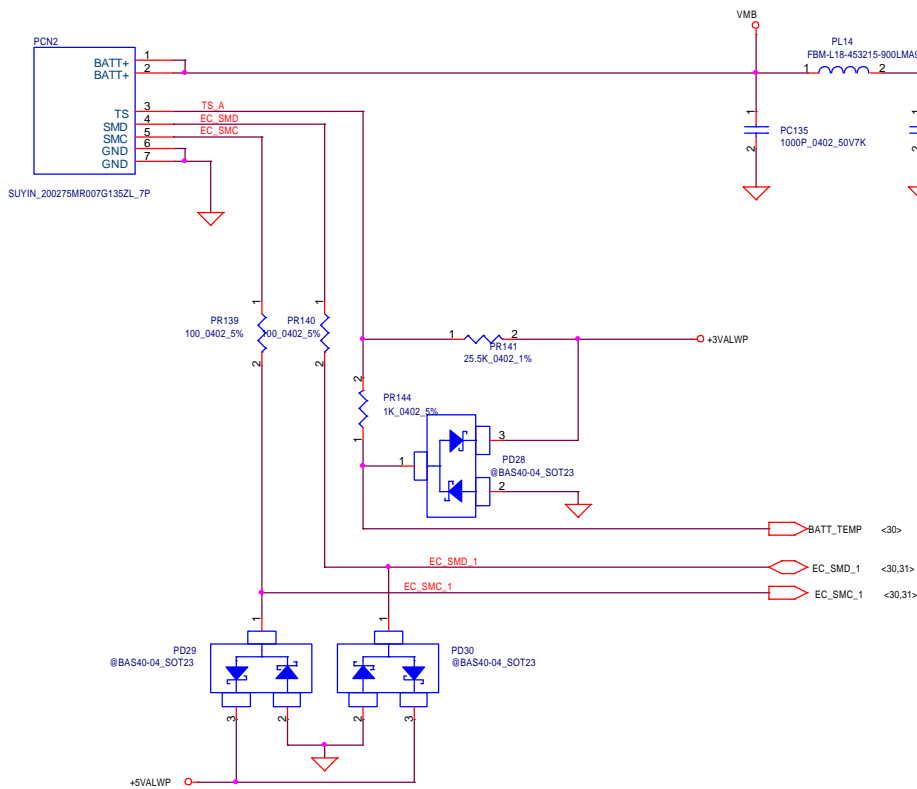
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COMPAL ELECTRONICS, INC		
File		
1.25V / VGA_CORE		
Doc	Document Number	Rev
	LA-1851	0.5
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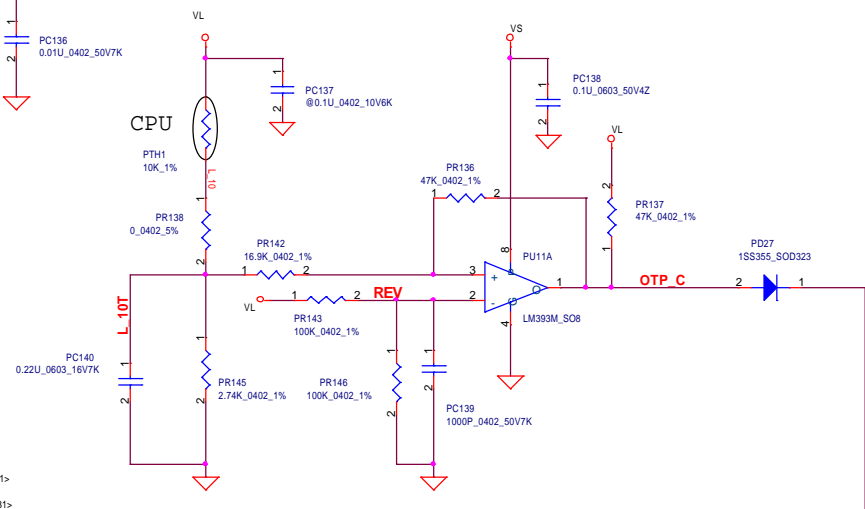


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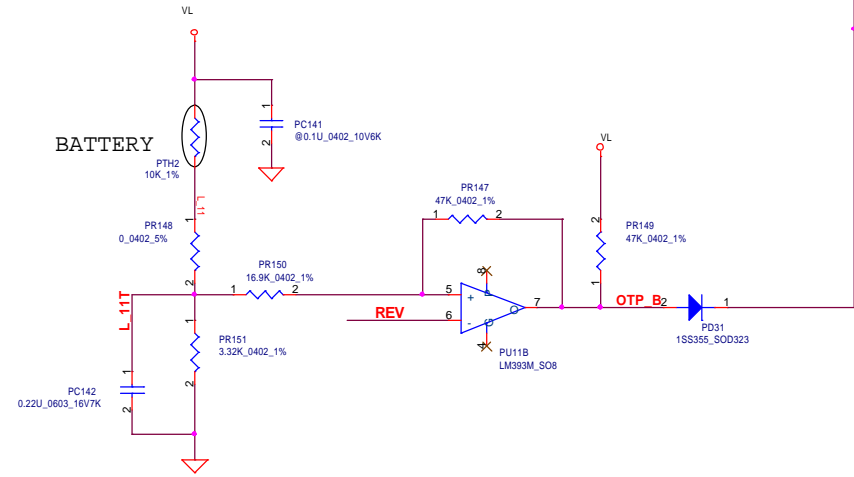
COMPAL ELECTRONICS, INC		
Title		
+CPU_CORE(2)		
Size	Document Number	Rev
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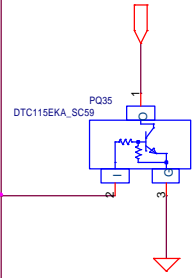
PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 84 +-3 degree C
 Recovery at 45 +-3 degree C



<38,40> MAINPWON



COMPAL ELECTRONICS, INC		
Title		
BATTERY CONN / OTP/1.8V		
Size	Document Number	Rev
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POWER PIR LIST

PHASE	page	Reason for change	Modify list
DB2	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvement noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202

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COMPAL ELECTRONICS, INC		
Title		
PIR		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Fixed USB 1.1 rising/falling time error	P12	Delete C785, C786, C787, C788, C789, & C790	0.3
2		Fixed TV-out no display	P14	Swap TV_CRMA and TV_COMPS	0.3
3		Prevent PCI1620 latched up	P22	Reserve G_RST# to pin U37.C11	0.3
4		Design change (solve for HR60 audio issue)	P26	Move two load resistors from sub-board to M/B and swap JP17.2 and JP17.3	0.3
5		Supported wake up from TP	P27	Change TP connector JP26's power pin from +5VS to +5V	0.3
6		EMI required (solve for 48 MHz noise from FDD connector)	P32	Add CP11, CP12, CP13, and C801	0.3
7		Design change (TFDU6102 design guide)	P33	Delete C560 and C562 & add R586 Change C561 from 10uf to 4.7uf	0.3
8		EMI required (solve for 48 MHz noise from serial port)	P34	Add CP14, and CP15	0.3
9		ID required (for Pavillion)	P35	Add D58	0.3
10		EMI required	P25	Add L38, and L39	0.3
11		Add bypass cap. to solve for AC97 link cross a split plane	P27	Add C802, C803, C804, C805, and C806	0.3
12		Design change (reserve space for power placement and no need too many caps.)	P07	Delete C75, and C88	0.3
13		RealTech 8101L design guide	P20	Change R194 to 5.6K +/- 1%	0.3
14		Solve for SPDIF no output	P34	Delete C634	0.3
15		CPU_CLK is current drive from CK8. So, delete damping resistors.	P11	Change R69, and R70 from 15 ohm to 0 ohm	0.3
16		Solve for burst frequency error	P14	Change C642, and C643 from 18 pF to 22 pF	0.3
17		Solve for chrominance and burst level	P18	Change L11, L12, and L13 to 1.8uH	0.3

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P.I.R HISTORY

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 - 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop S19182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNC average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module (16 chips)	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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Compal Electronics, Inc.	
P.I.R HISTORY	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		TI recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5

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