

888Z4.5 / LA-1302 Mother Board Rev : 0.5 for Layout

Intel (Northwood) with Intel 845M+ICH3

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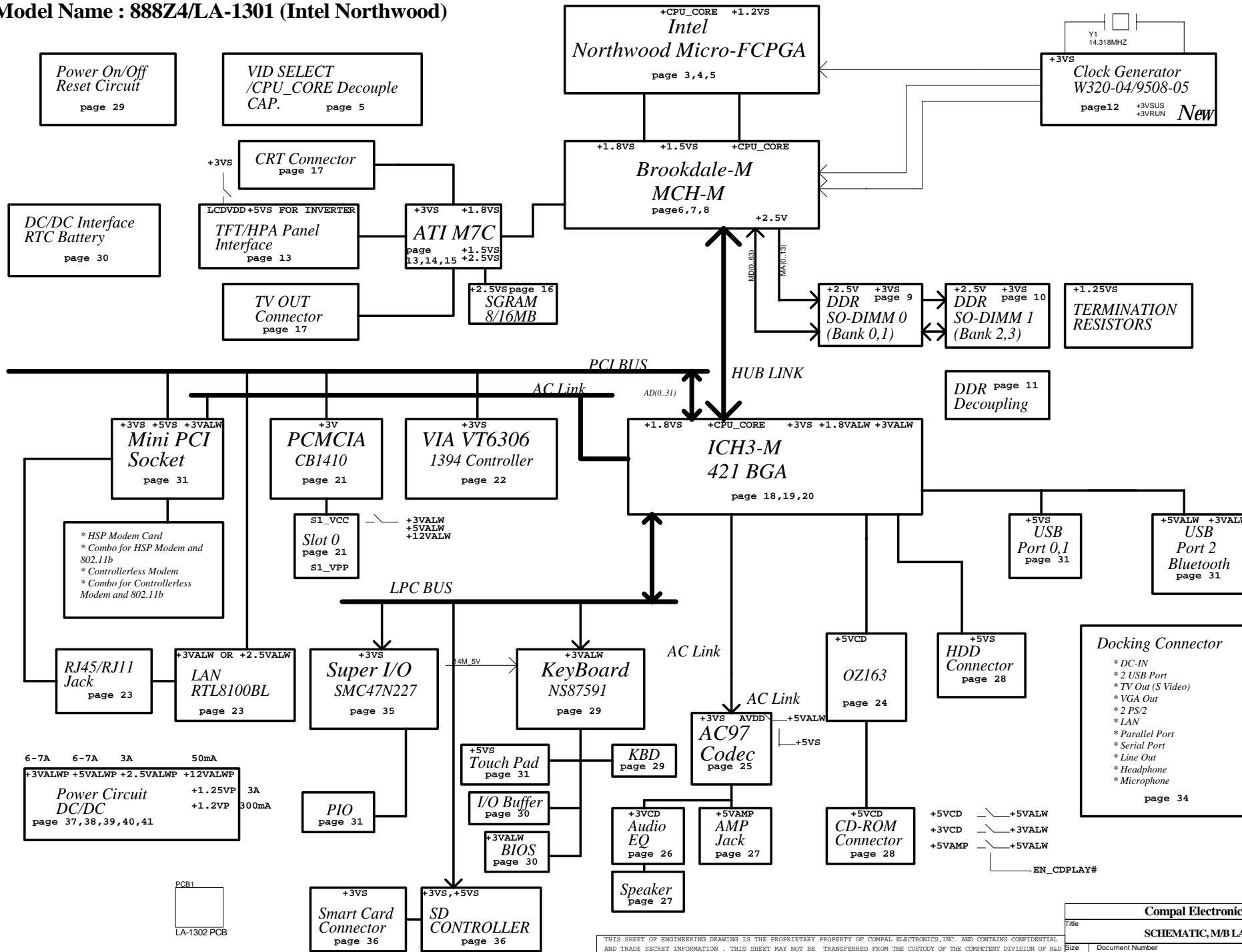
stencil not open:

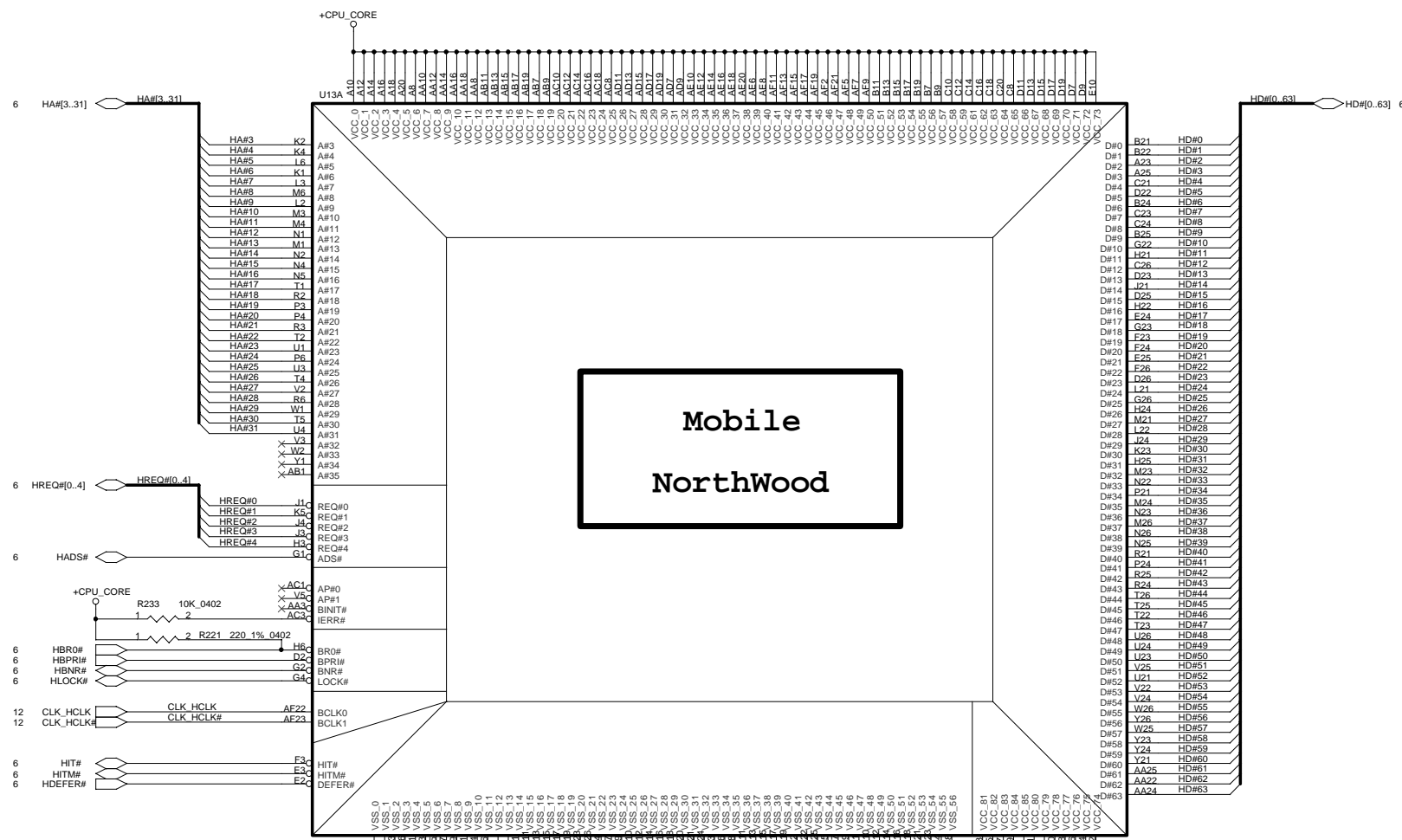
- J1
- U24
- PJP2
- PJP4
- C715
- C716
- PC155
- C72
- C94

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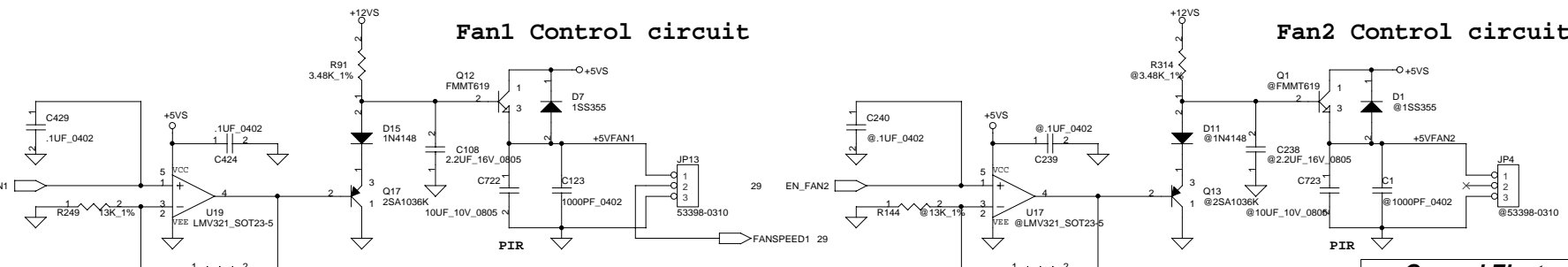
Model Name : 888Z4/LA-1301 (Intel Northwood)





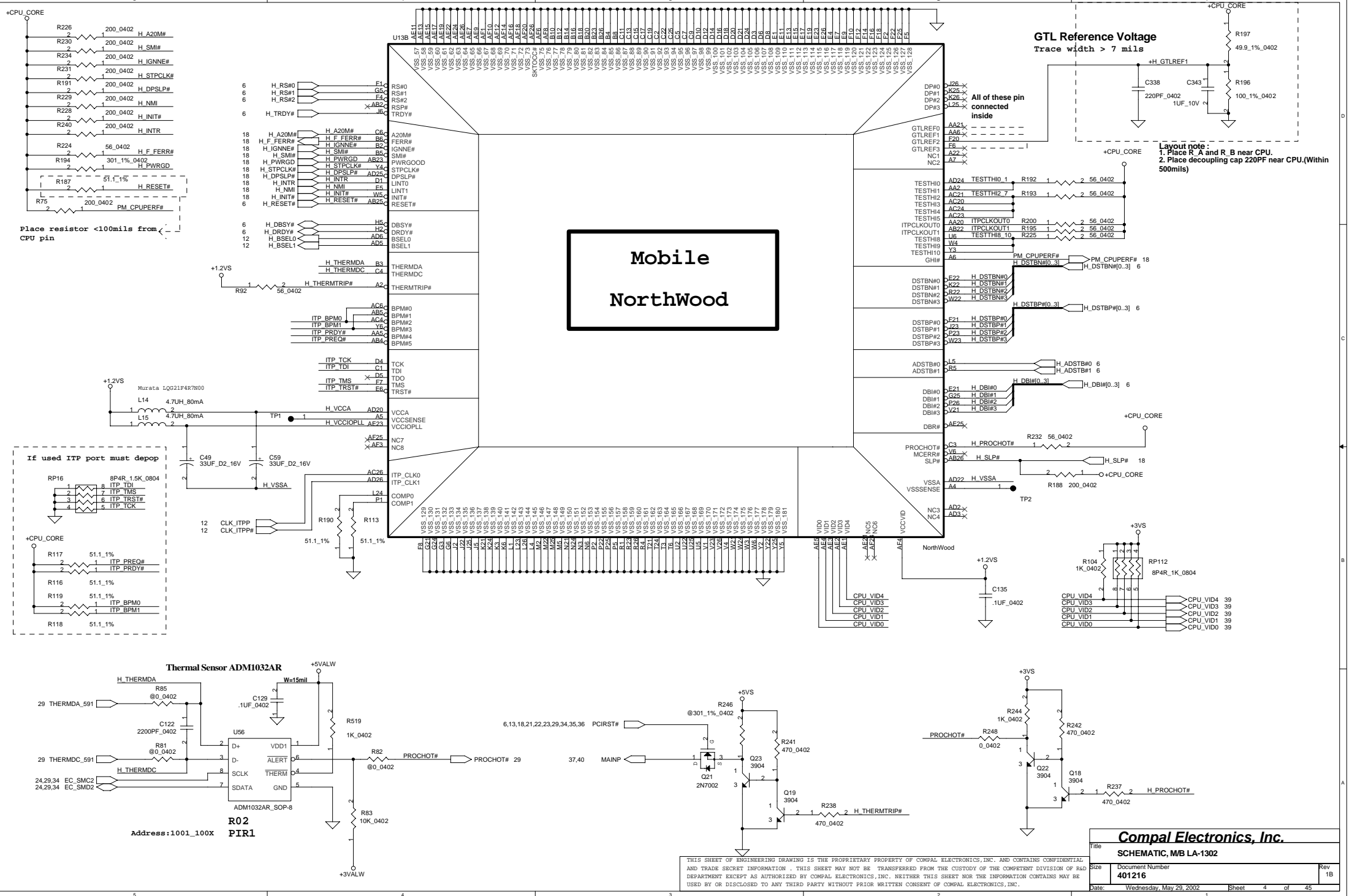
Fan1 Control circuit

Fan2 Control circuit

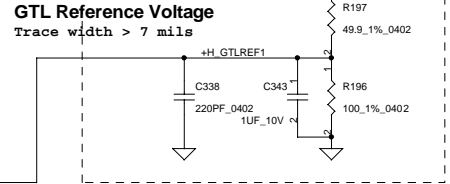


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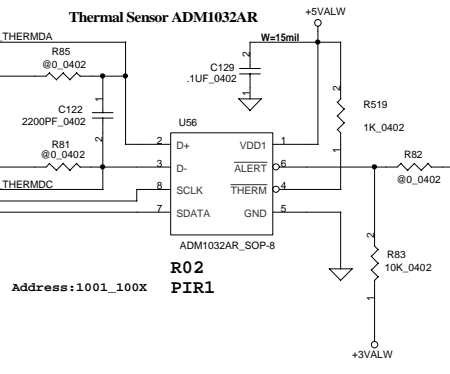
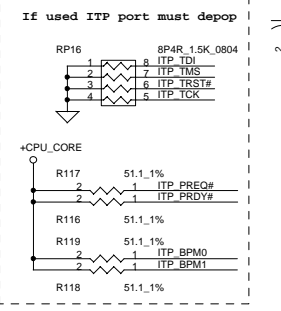


**Mobile
NorthWood**



Layout note:
1. Place R_A and R_B near CPU.
2. Place decoupling cap 220PF near CPU. (Within 500mils)

Place resistor <100mils from CPU pin



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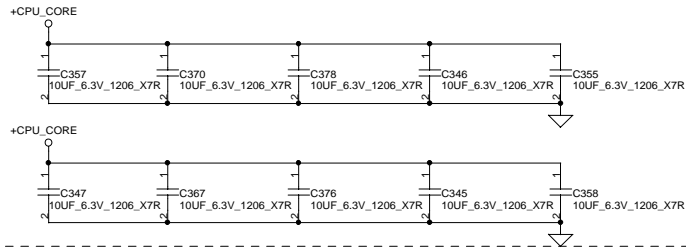
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Layout note :
 Place close to CPU. Use 2-3 vias per PAD.
 Place .22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

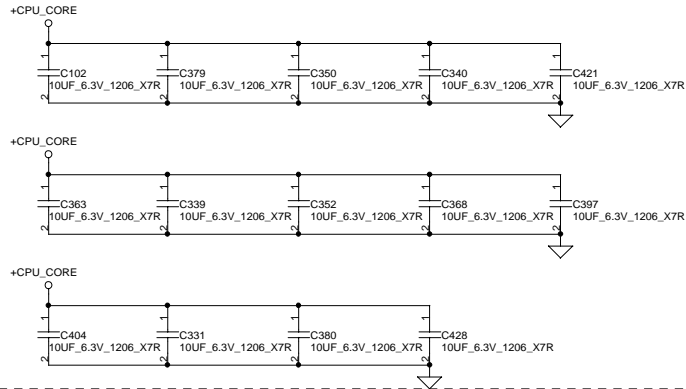
Layout note :
 Place close to CPU power and ground pin as possible (<1inch)

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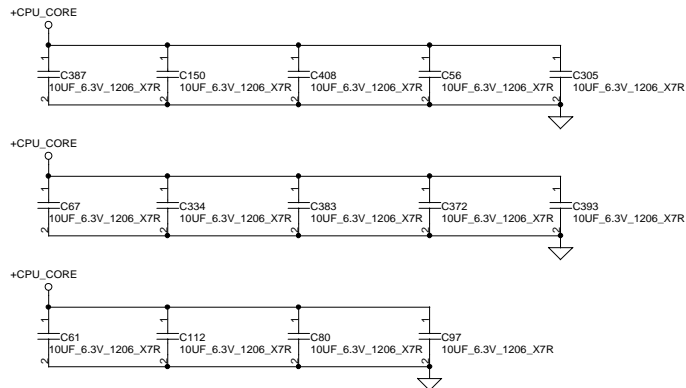
Please place these cap in the socket cavity area



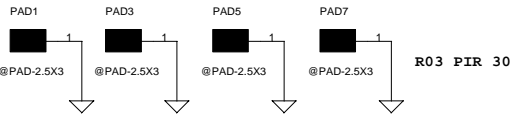
Please place these cap on the socket north side



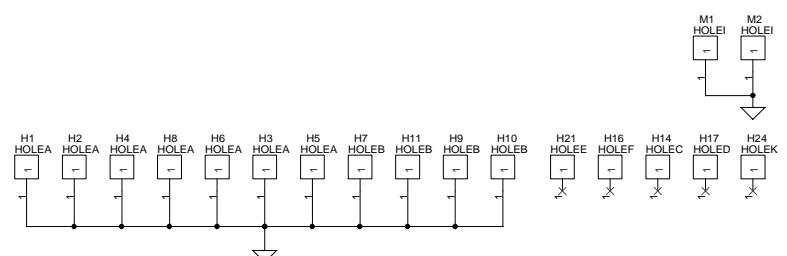
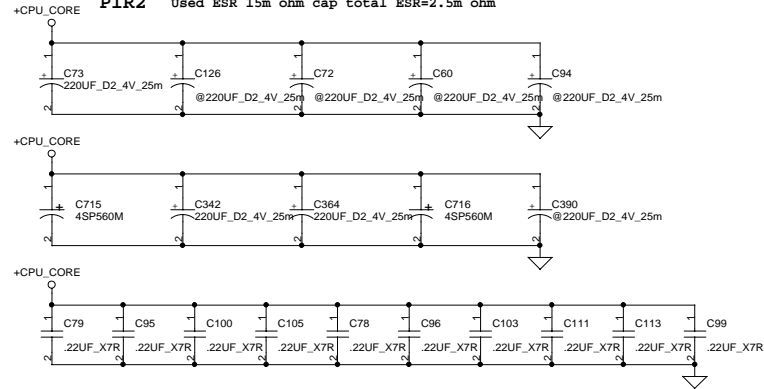
Please place these cap on the socket south side



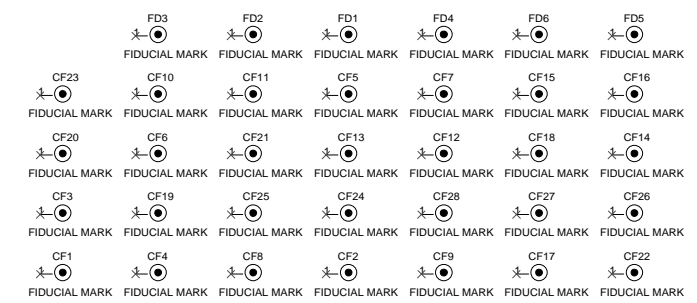
EMI Clip PAD for CPU



R02 PIR2 Used ESR 15m ohm cap total ESR=2.5m ohm



Fiducial Mark

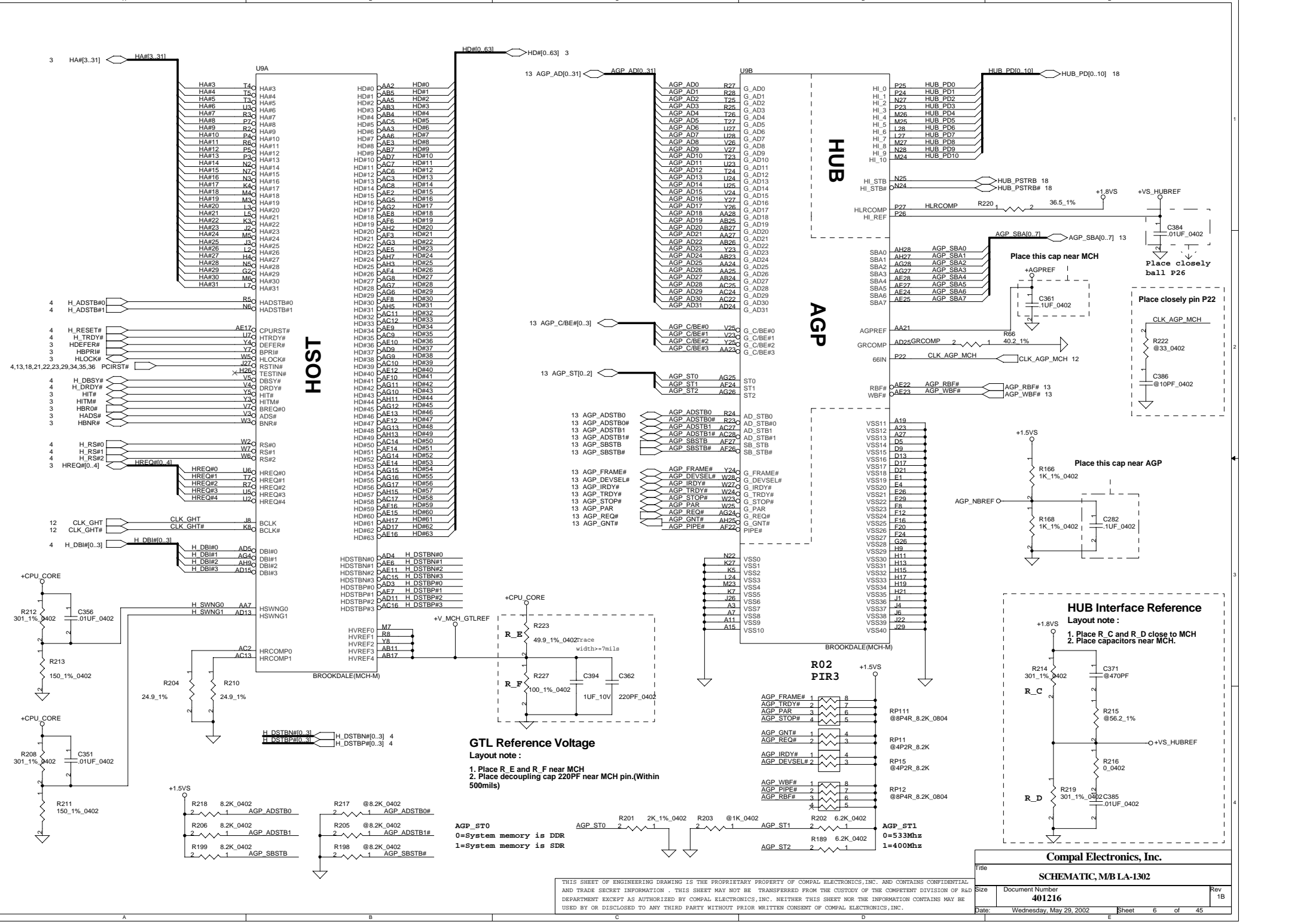


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HOST

HUB

AGP

GTL Reference Voltage

Layout note :
 1. Place R_E and R_F near MCH
 2. Place decoupling cap 220PF near MCH pin. (Within 500mils)

HUB Interface Reference

Layout note :
 1. Place R_C and R_D close to MCH
 2. Place capacitors near MCH.

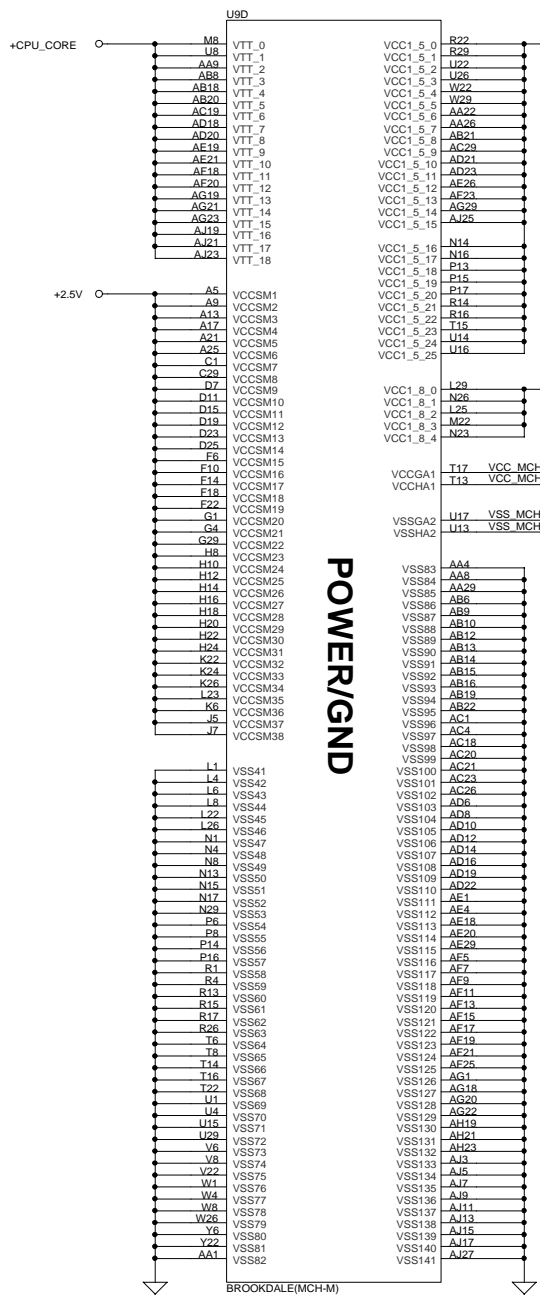
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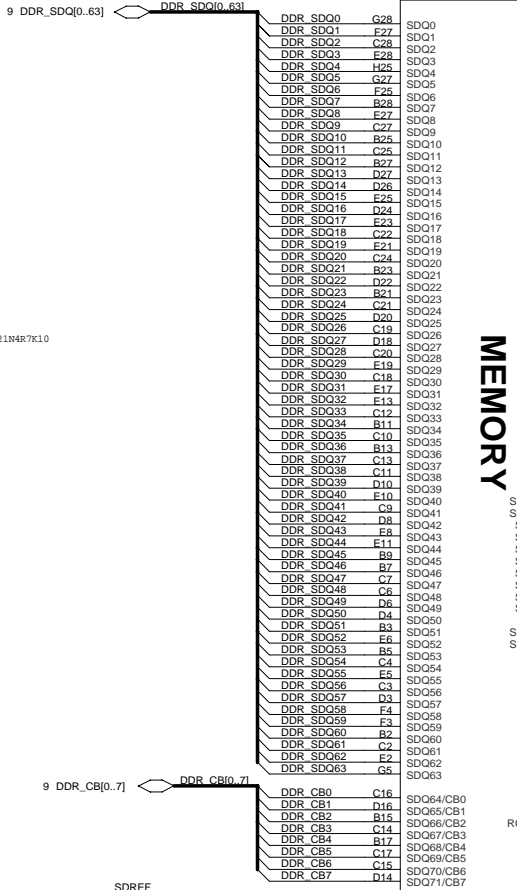
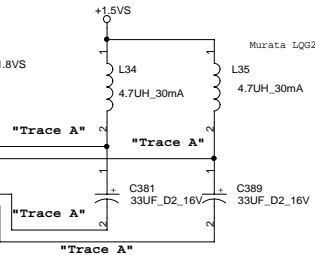
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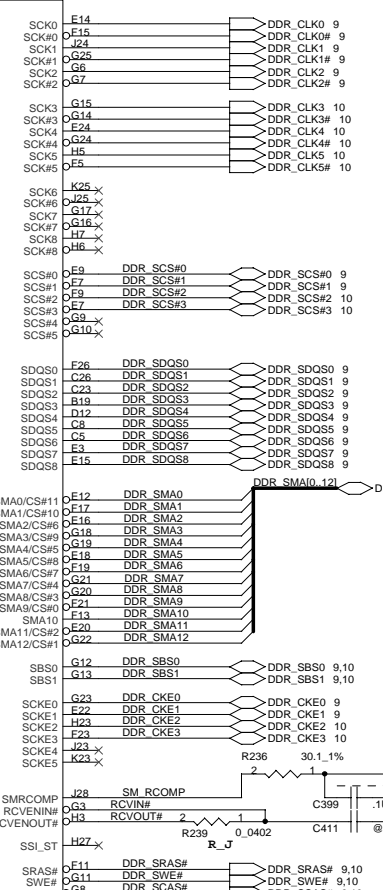


POWER/GND

Layout note :
Trace width 5mil ; Spacing 10mil
Trace A to ball U13/T13 or U17/T7 =1.5" Max



MEMORY



Layout note
Place R620 closely pinJ28

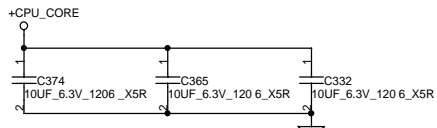
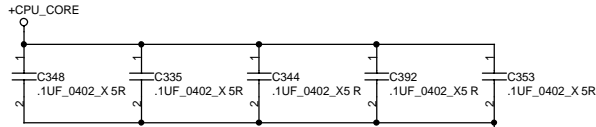
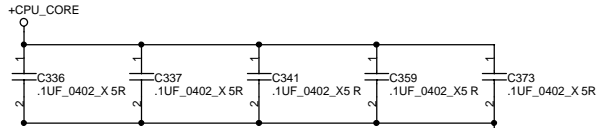
Layout note
Place R_J closely Ball H3<40mil, Ball H3 to G3 trace must routing 1"

Layout note
Please closely pinJ21 and J9

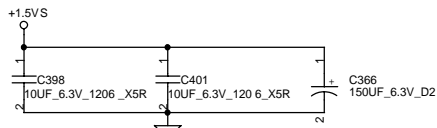
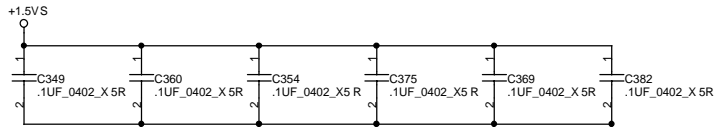
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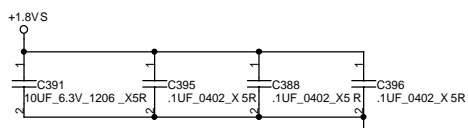
Layout note : Processor system bus
 Distribute as close as possible
 to MCH Processor Quadrant.(between VTTFBS and VSS pin)



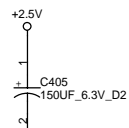
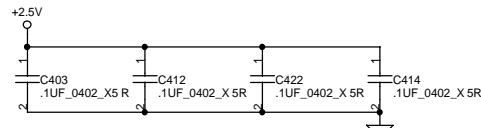
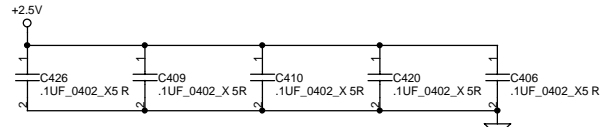
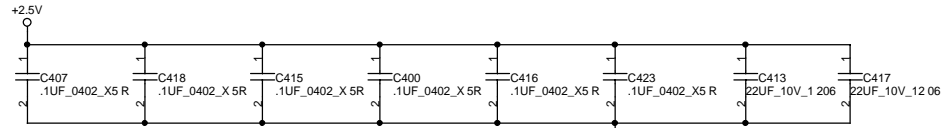
Layout note : AGP / CORE
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCAGP/VCCCORE
 and VSS pin)



Layout note : Hub-Link
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCHL and VSS pin)



Layout note : DDR Memory interface
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCSM and VSS pin)



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Layout note
Place these resistor closely DIMM0, all trace length<750mil

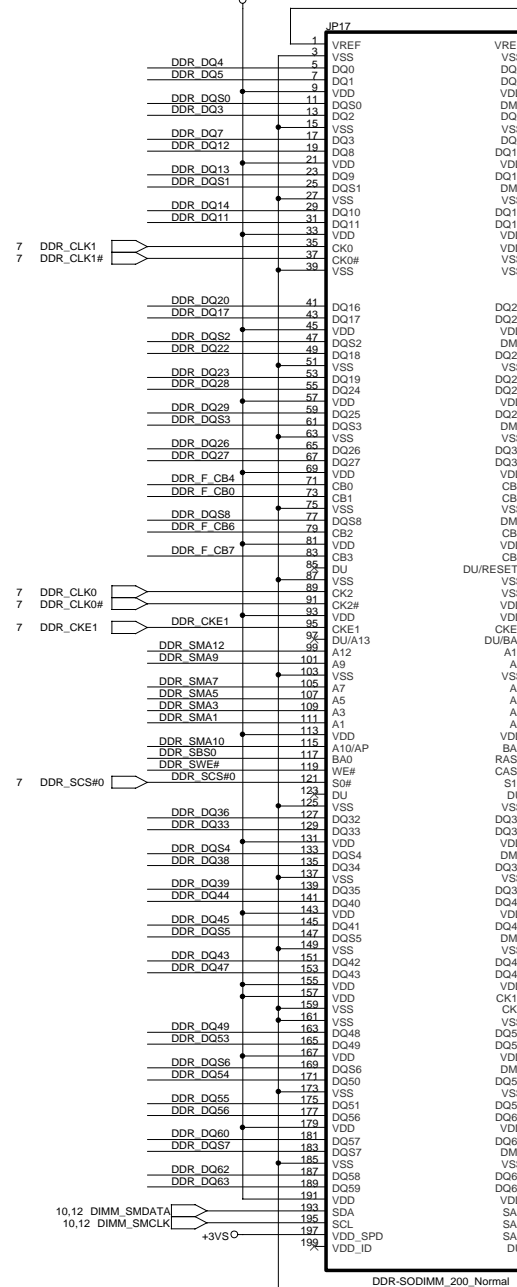
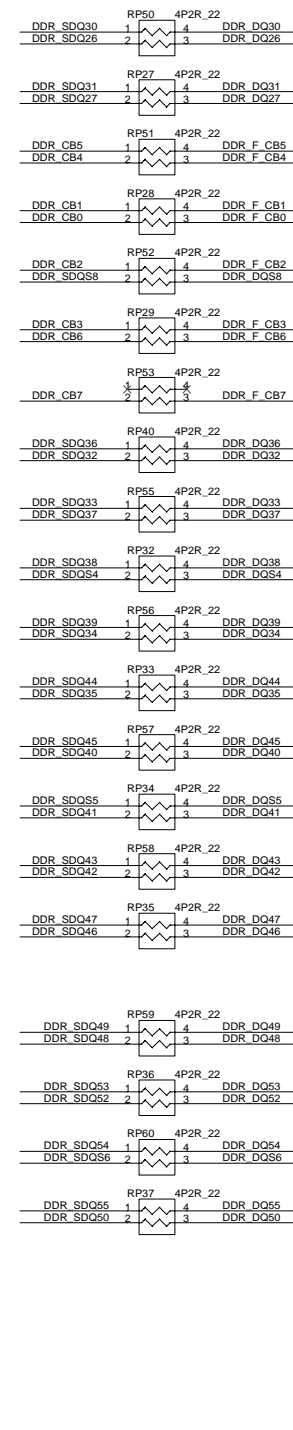
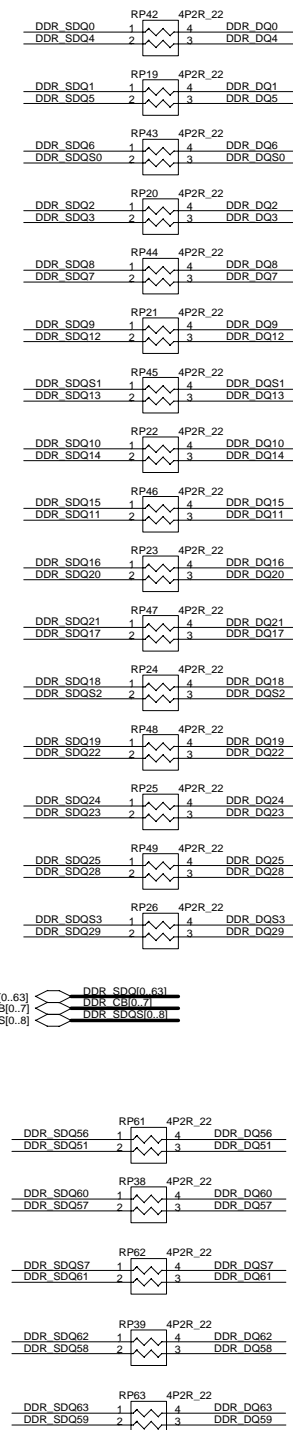
7 DDR_SQ[0..63] DDR_SQ[0..63]
7 DDR_CB[0..7] DDR_CB[0..7]
7 DDR_SQ[8..8] DDR_SQ[8..8]

7 DDR_SQ[56] DDR_SQ[56]
7 DDR_SQ[57] DDR_SQ[57]

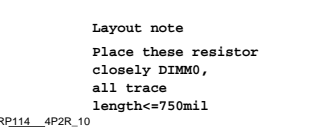
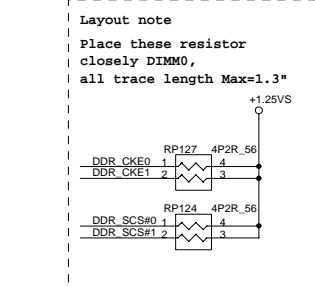
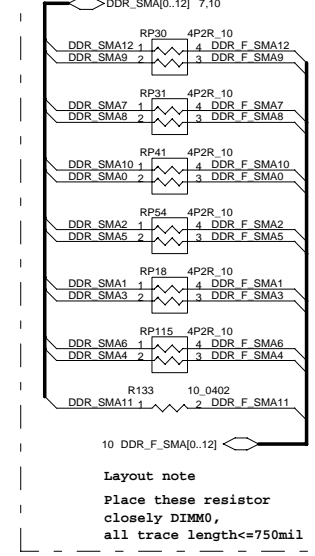
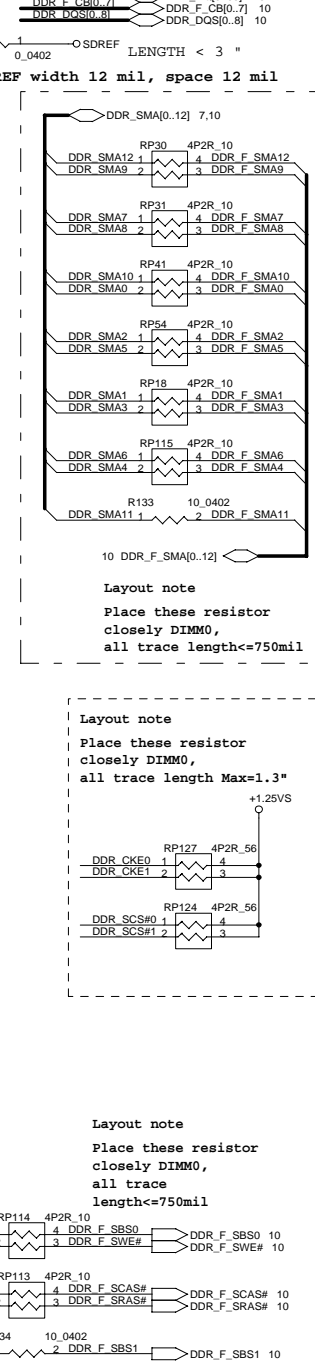
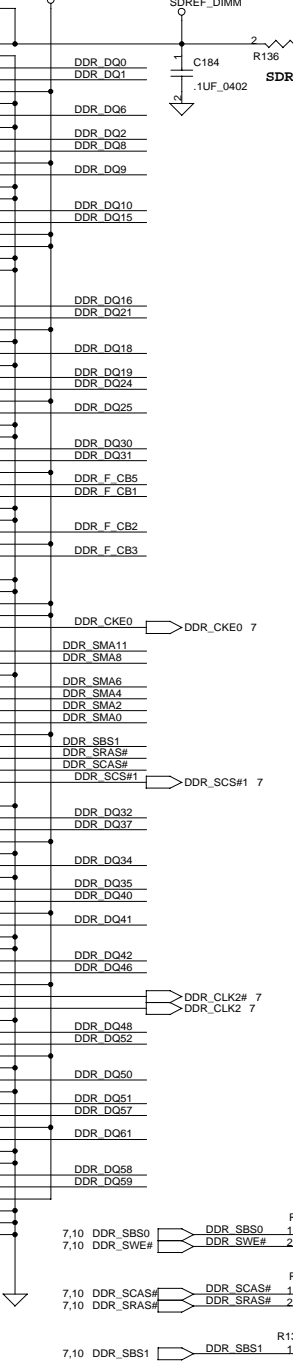
7 DDR_SQ[61] DDR_SQ[61]
7 DDR_SQ[62] DDR_SQ[62]

7 DDR_SQ[63] DDR_SQ[63]
7 DDR_SQ[64] DDR_SQ[64]

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7 DDR_SQ[66] DDR_SQ[66]

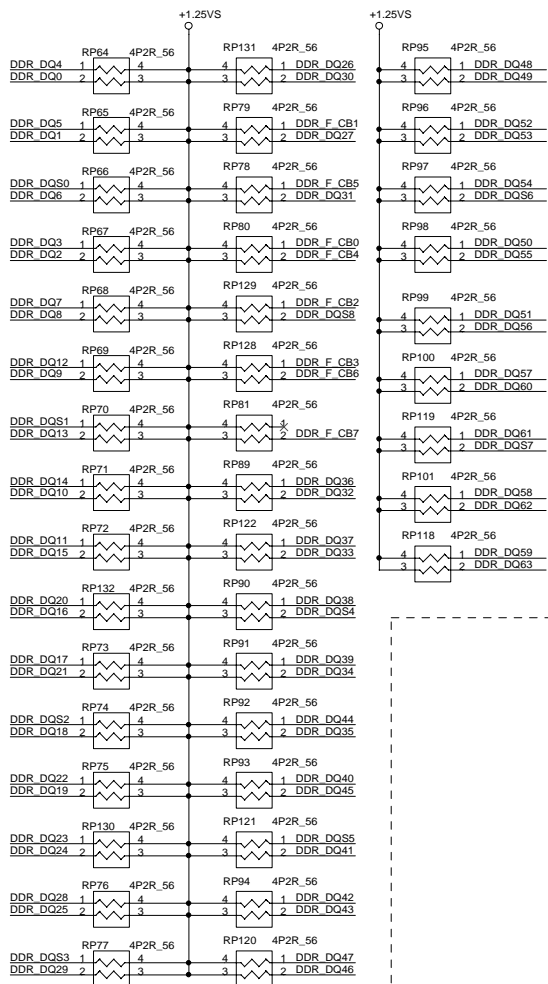


DIMM0
top side

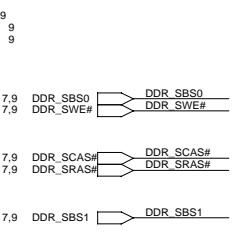
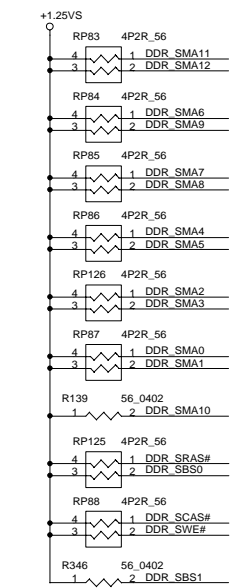
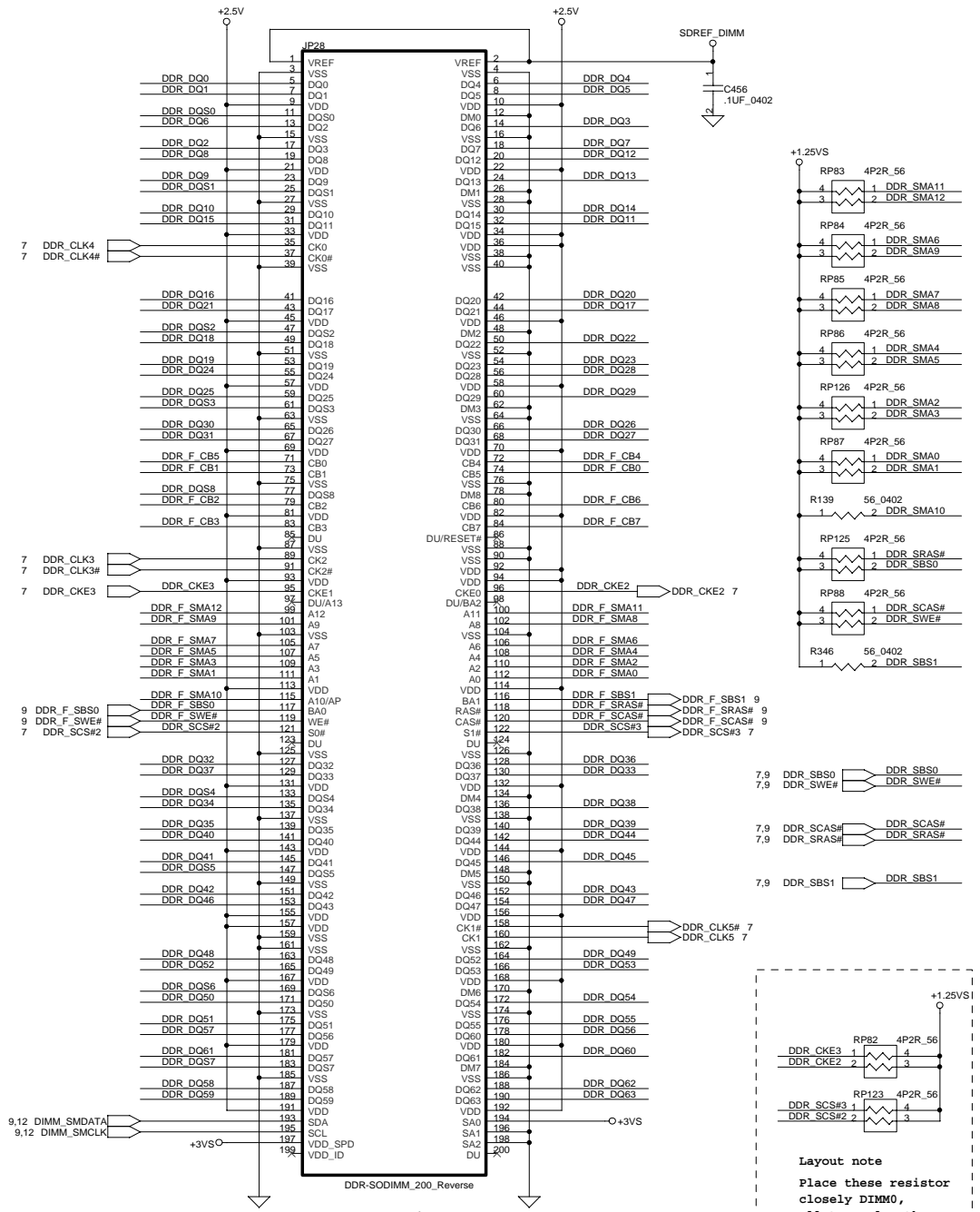
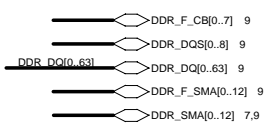


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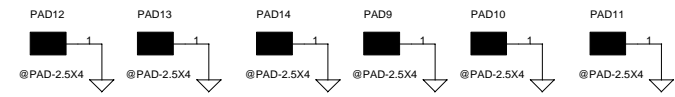


Layout note
Place these resistor closely DIMM1, all trace length<=800mil



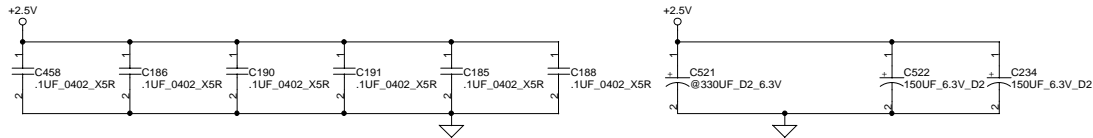
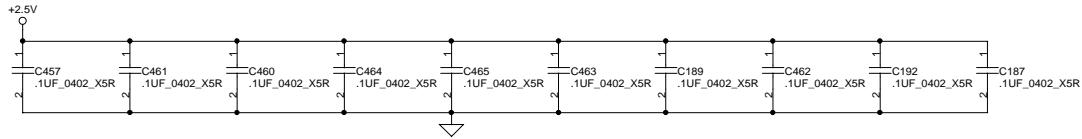
Layout note
Place these resistor closely DIMM0, all trace length Max=1.3"

EMI Clip PAD for Memory Door

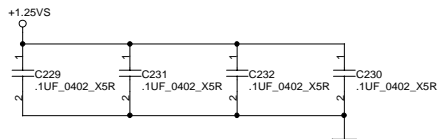
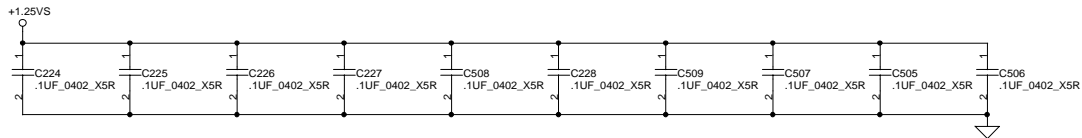
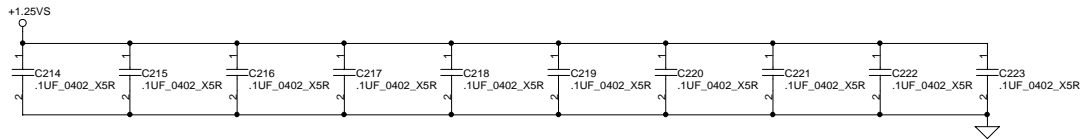
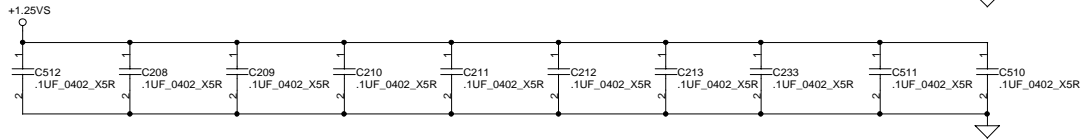
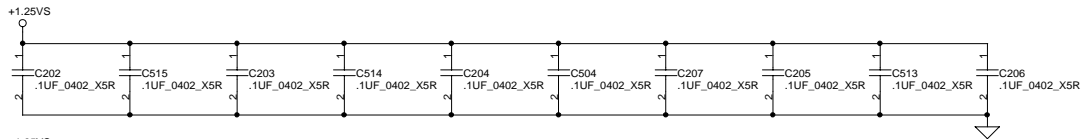
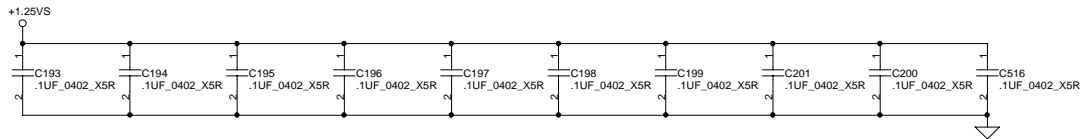


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Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



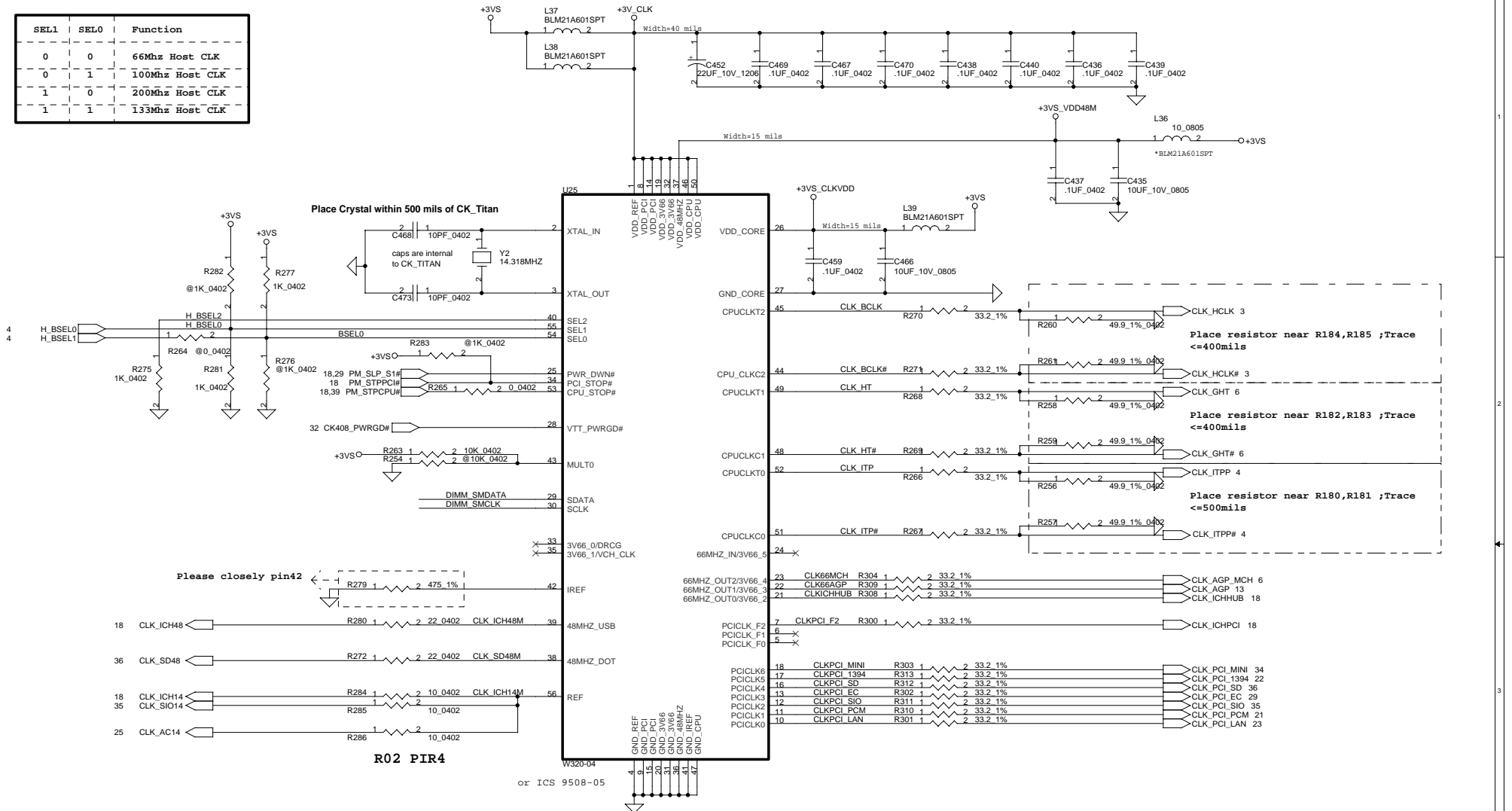
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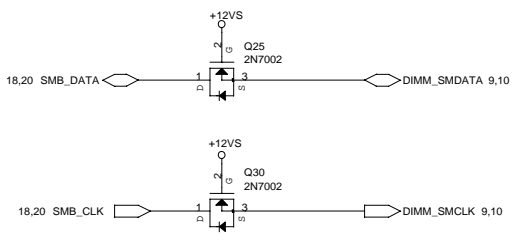
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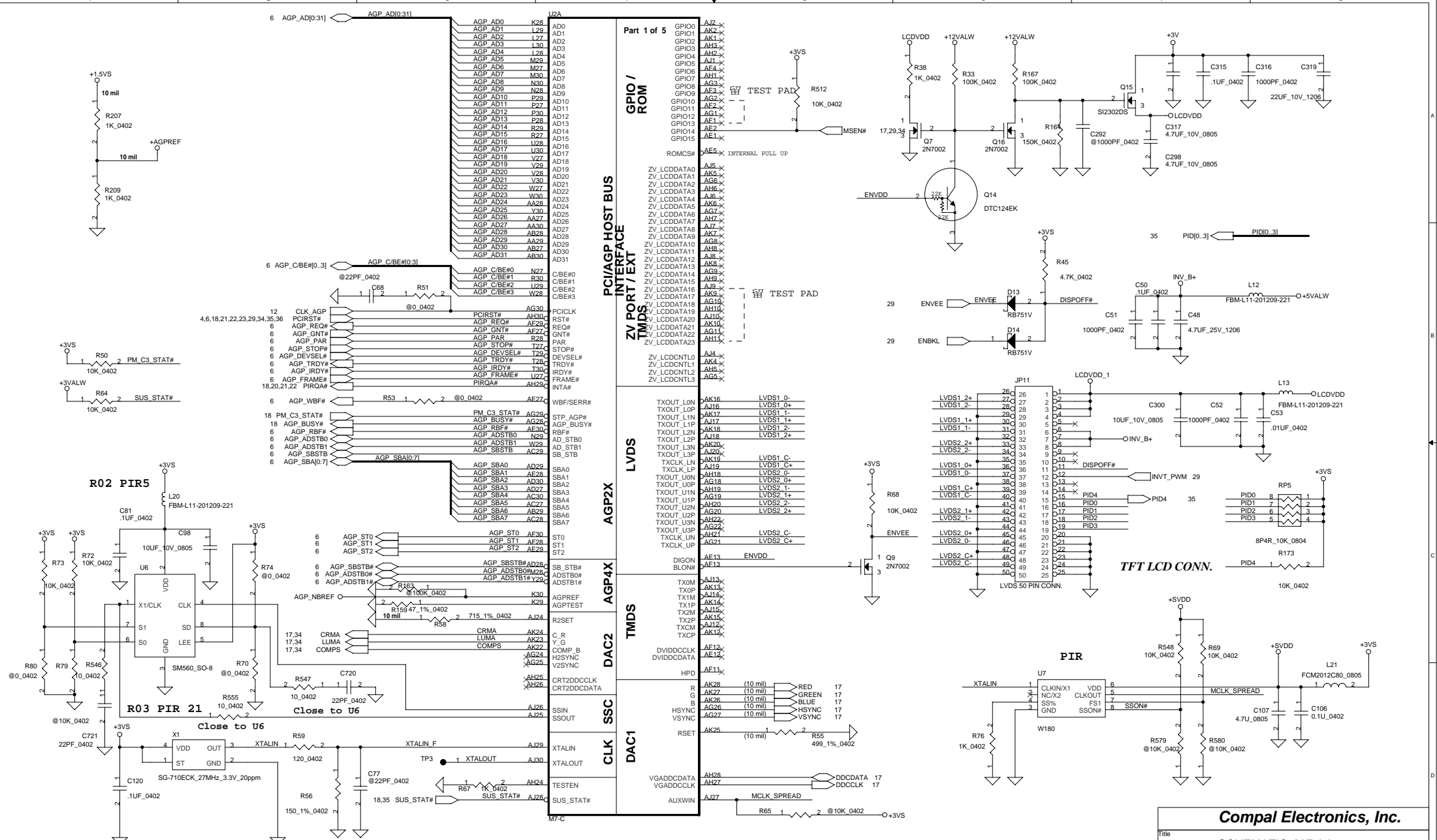
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SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



Note:
CPU_CLK[2:0] needs to be running in C3, C4.





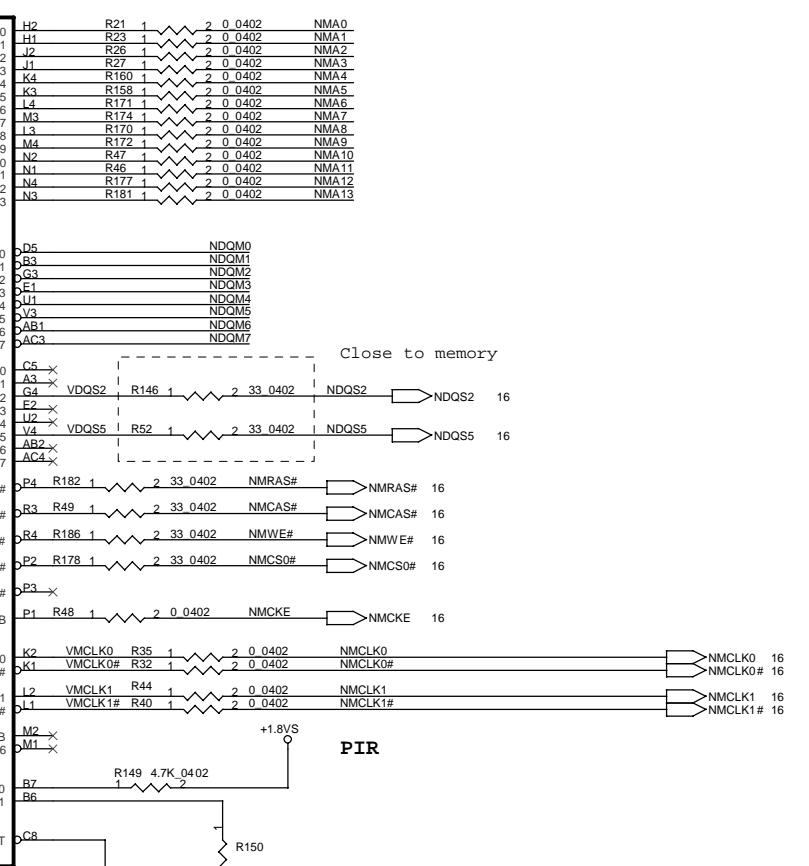
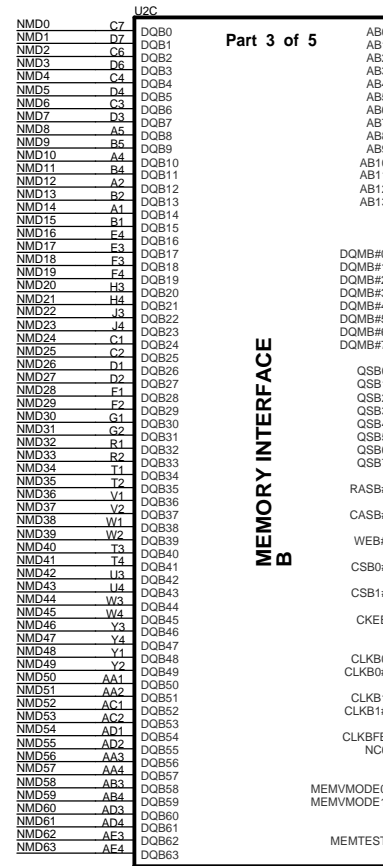
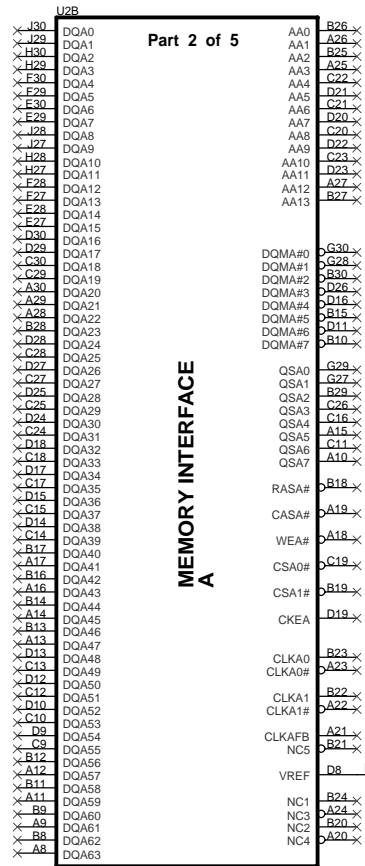
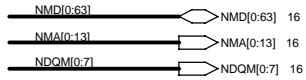
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Divider circuit for 1.8Vdc XTALIN from 3.3Vdc OSC out



MEMORY INTERFACE

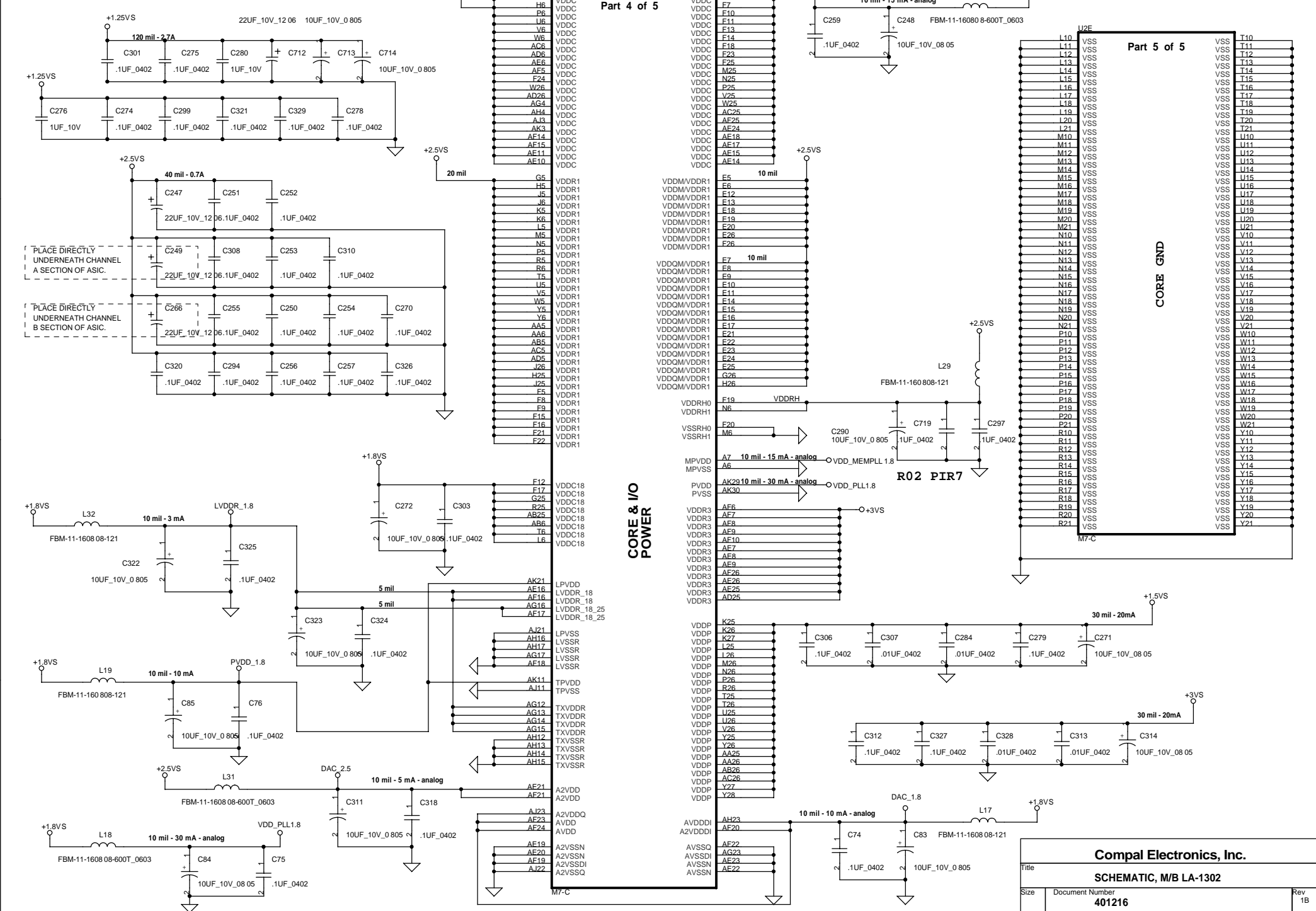


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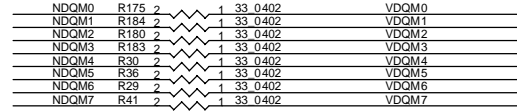
POWER INTERFACE



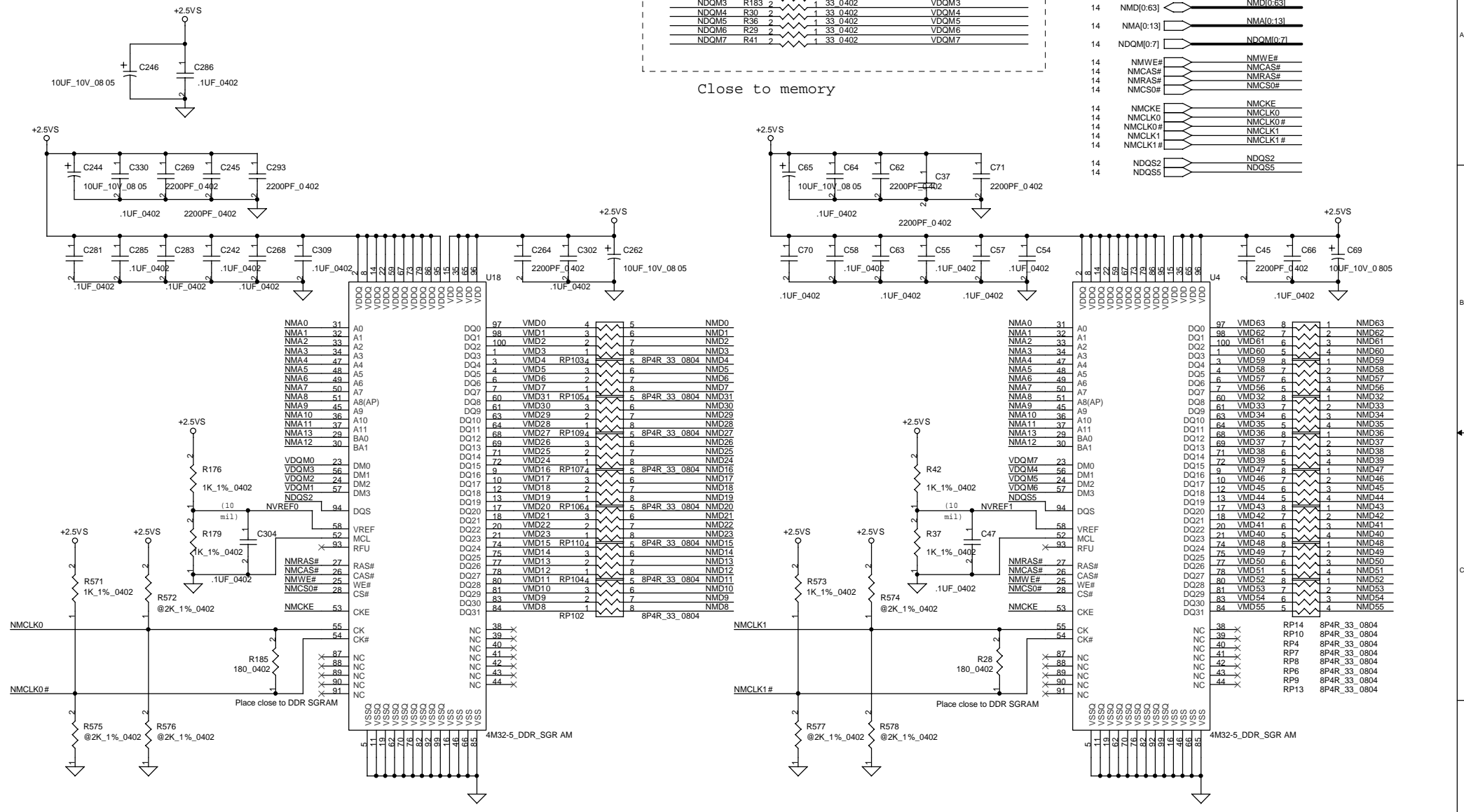
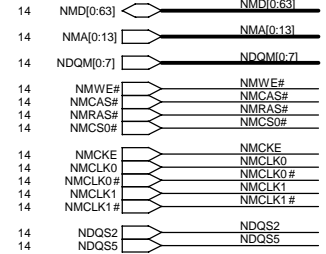
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NOTE : MA11 CONNECTION REQUIRED FOR 4Mx32 DDR SGRAM ONLY

DDR SGRAM



Close to memory



NOTE : Resistors of NDQS0 and NDQS4 closed to the 94 pin of every DDR SGRAM

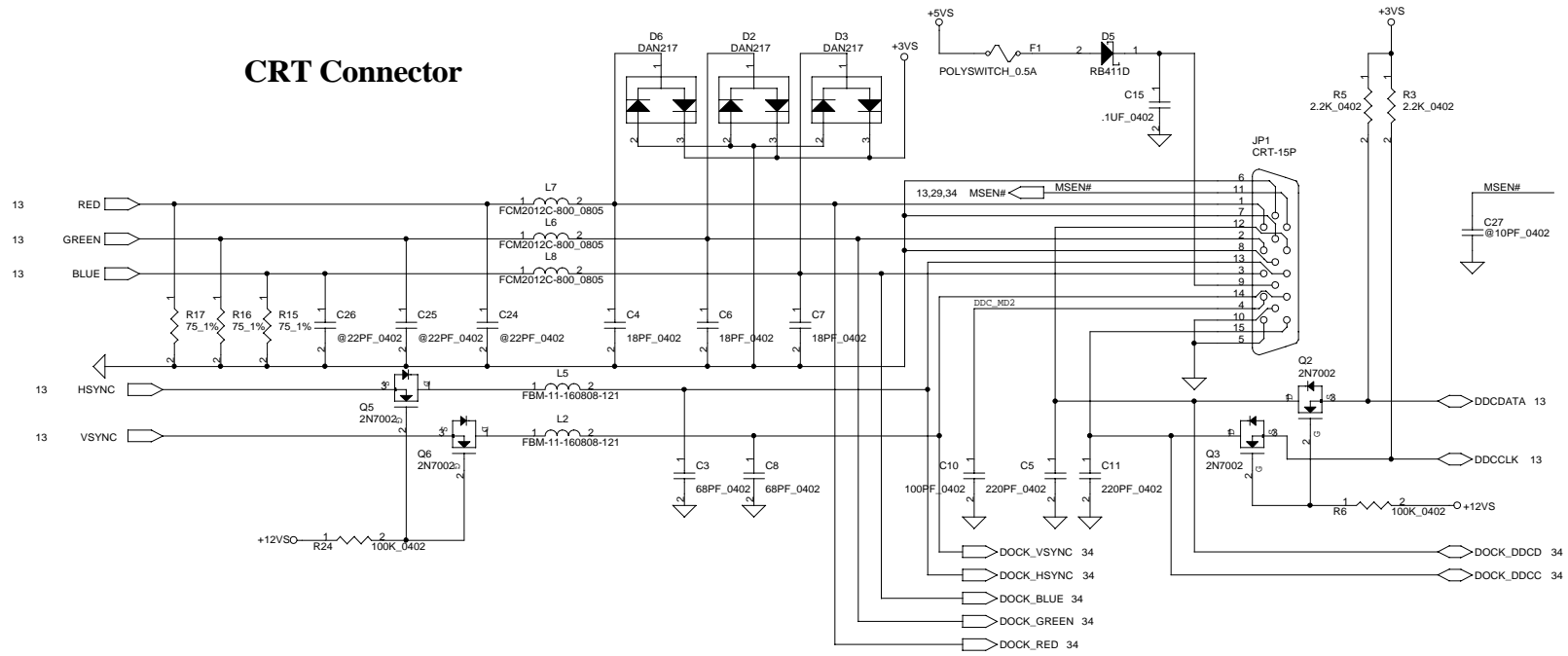
16/32MB DDR 2/4MX32 SGRAM

16MB 64 BIT INTERFACE WITH TWO PIECES 2MX32
32MB 64 BIT INTERFACE WITH TWO PIECES 4MX32

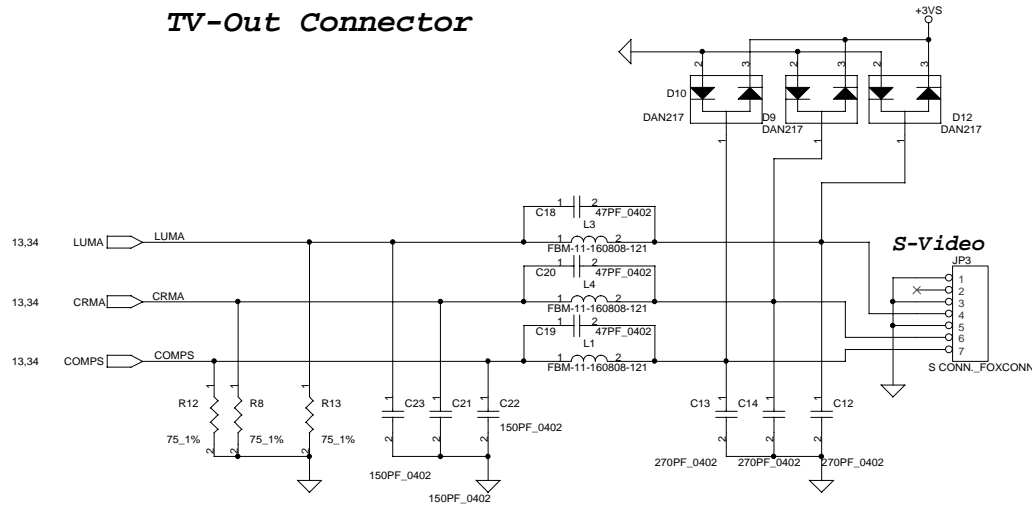
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CRT Connector



TV-Out Connector

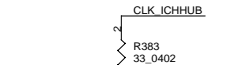
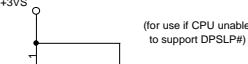
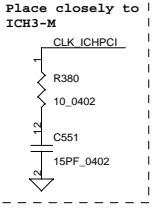
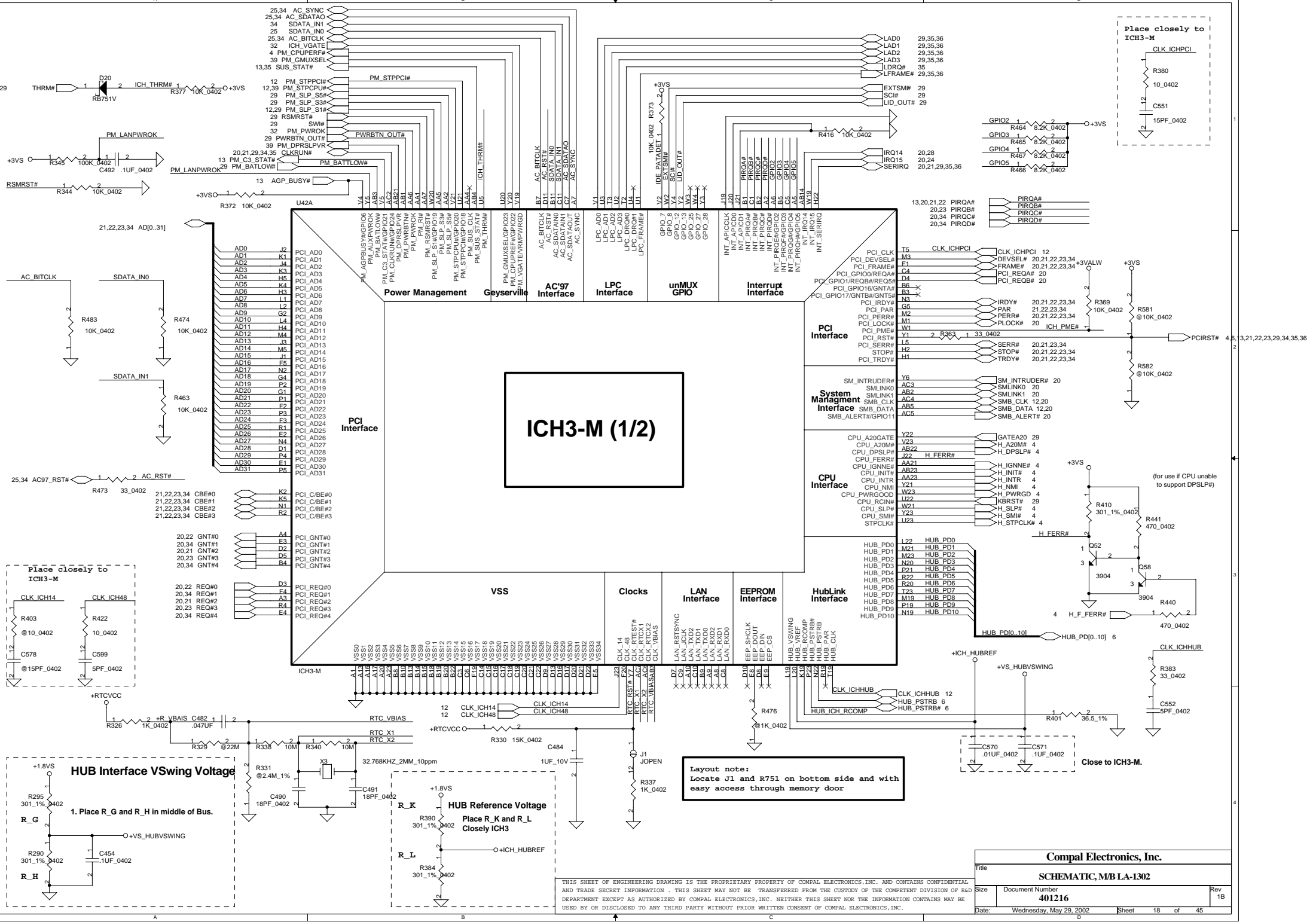


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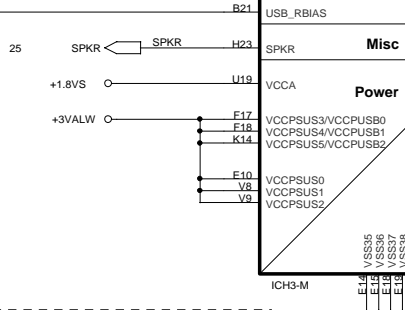
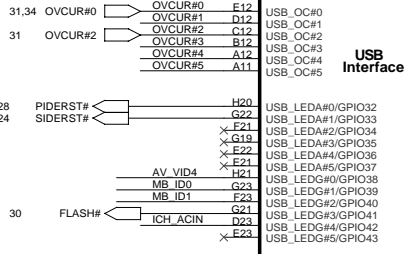
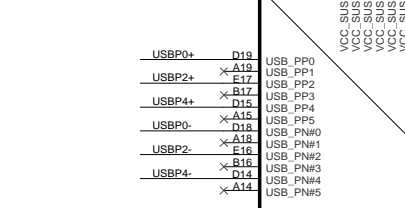
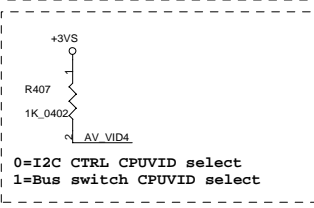
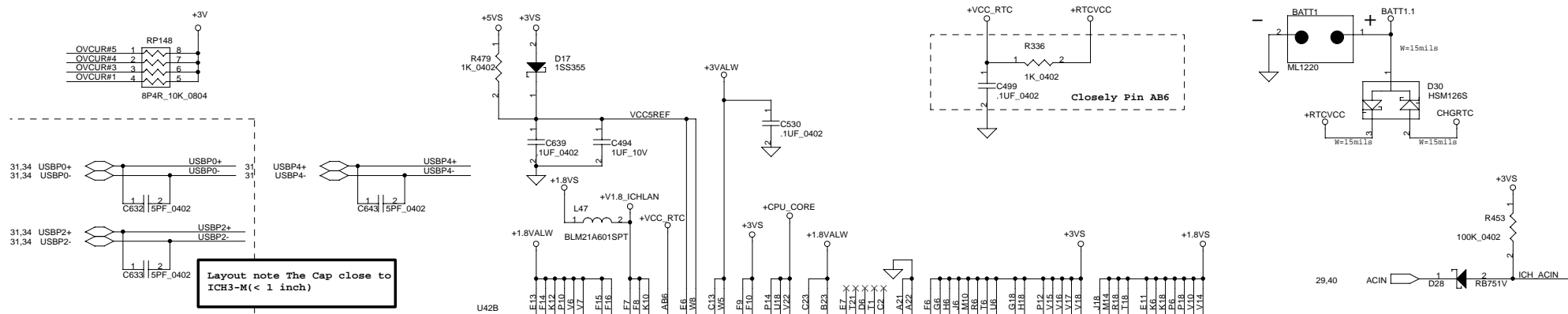
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Layout note:
Locate J1 and R751 on bottom side and with easy access through memory door

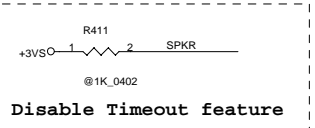
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Note:
 R376=22.6_1% for B0(QB63 part)
 R376=18.2_1% for B0(QB62 & SL5LF part)

MB_ID0	MB_ID1
SST	0
PT	1
ST	0
QT	1



ICH3-M (2/2)

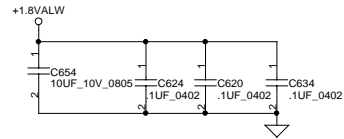
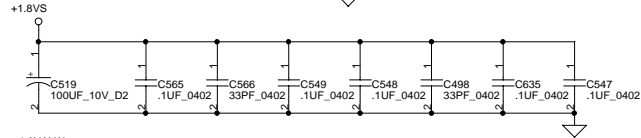
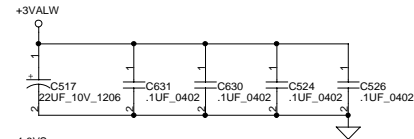
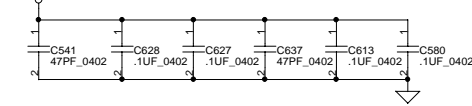
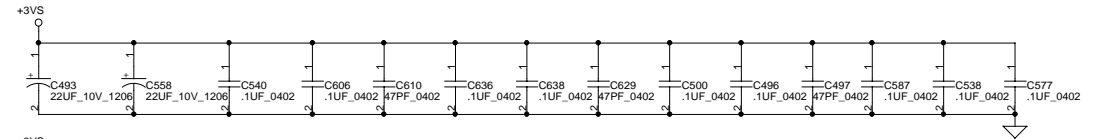
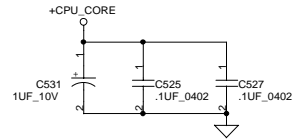
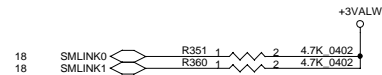
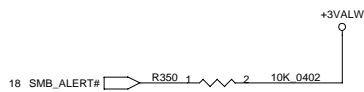
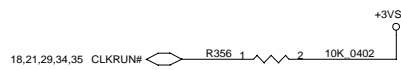
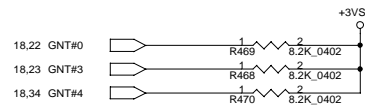
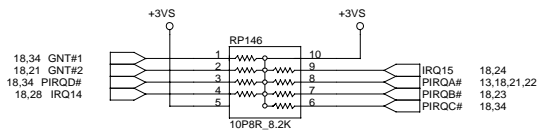
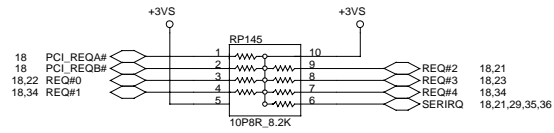
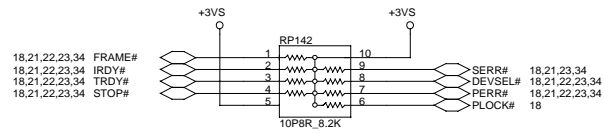
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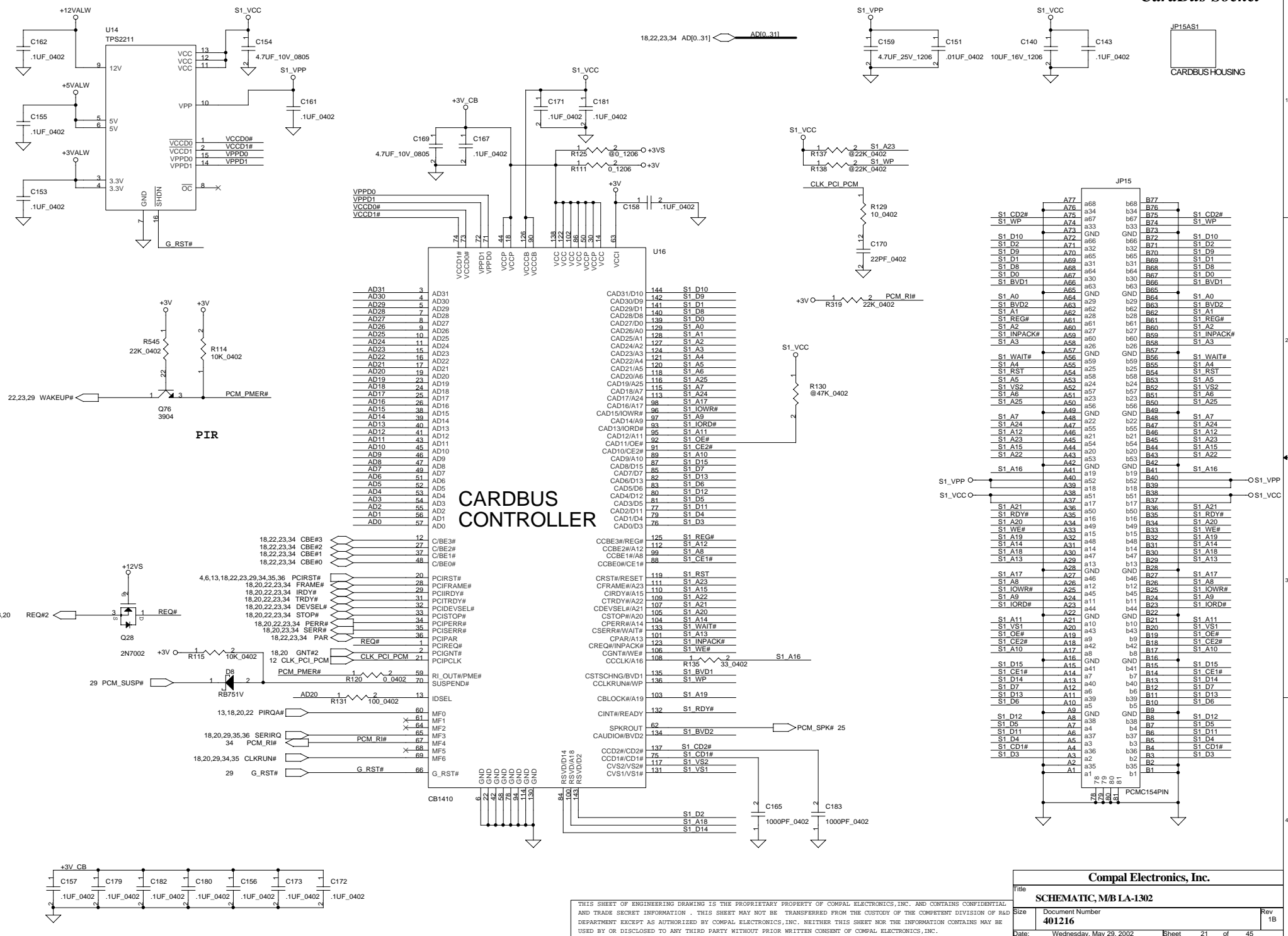
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CardBus Socket



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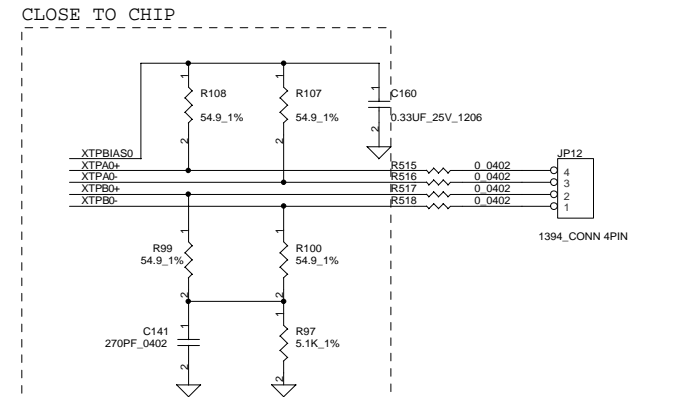
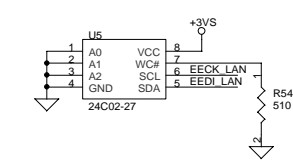
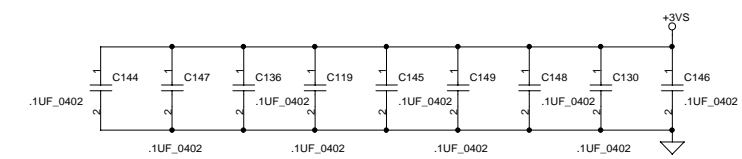
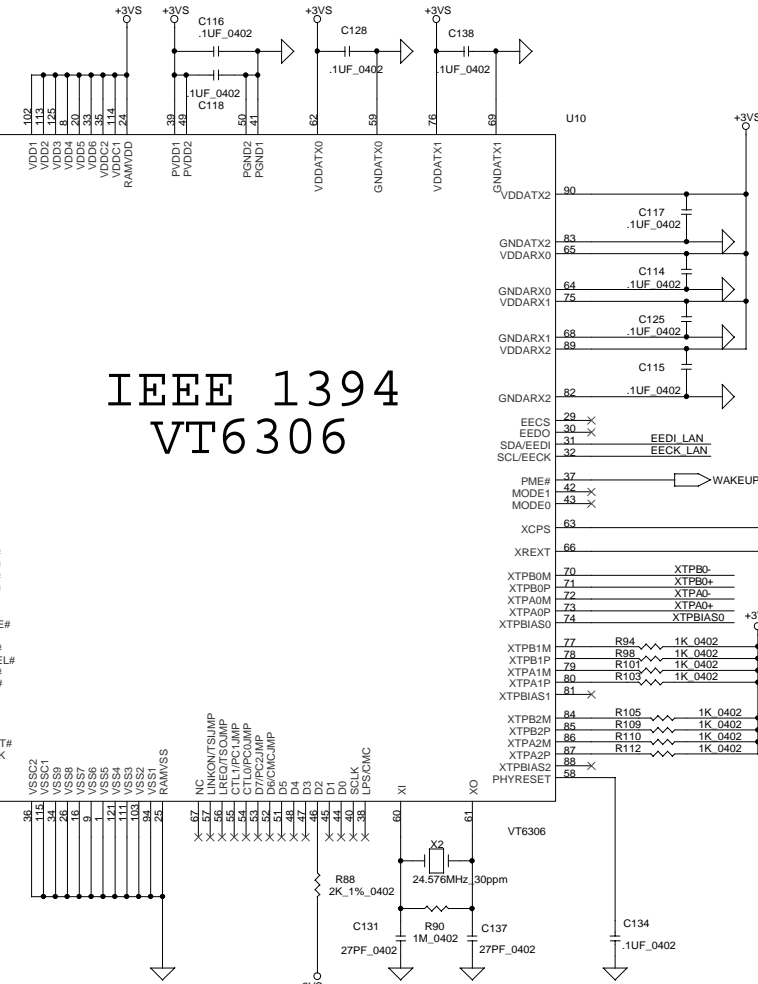
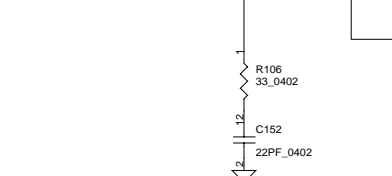
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18,21,23,34 AD[0..31] AD[0..31]

AD0	28	AD0
AD1	27	AD1
AD2	23	AD2
AD3	22	AD3
AD4	21	AD4
AD5	19	AD5
AD6	18	AD6
AD7	17	AD7
AD8	14	AD8
AD9	13	AD9
AD10	12	AD10
AD11	11	AD11
AD12	10	AD12
AD13	7	AD13
AD14	6	AD14
AD15	5	AD15
AD16	120	AD16
AD17	119	AD17
AD18	118	AD18
AD19	117	AD19
AD20	116	AD20
AD21	112	AD21
AD22	110	AD22
AD23	109	AD23
AD24	106	AD24
AD25	105	AD25
AD26	104	AD26
AD27	101	AD27
AD28	100	AD28
AD29	99	AD29
AD30	98	AD30
AD31	97	AD31

IEEE 1394 VT6306

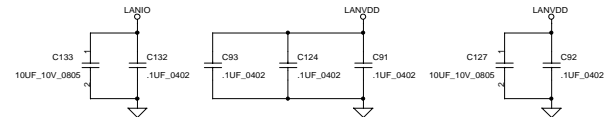
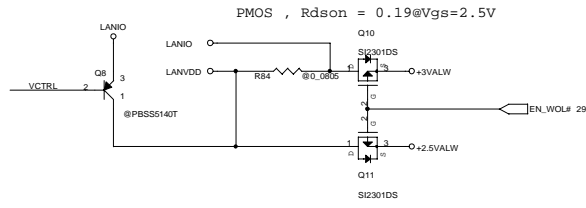
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18,21,23,34 CBE#3	107	CBE#3
18,20,21,23,34 FRAME#	108	FRAME#
18,20,21,23,34 IRDY#	123	IRDY#
18,20,21,23,34 TRDY#	126	TRDY#
18,20,21,23,34 DEVSEL#	127	DEVSEL#
18,20,21,23,34 STOP#	128	STOP#
18,20,21,23,34 PER#	2	PER#
18,21,23,34 PAR	3	PAR
18,20 REQ#	96	REQ#
18,20 GNT#	95	GNT#
13,18,20,21 PIRQ#	91	INTA#
12 CLK_PCI_1394	92	PCIRST#
	93	PCICLK



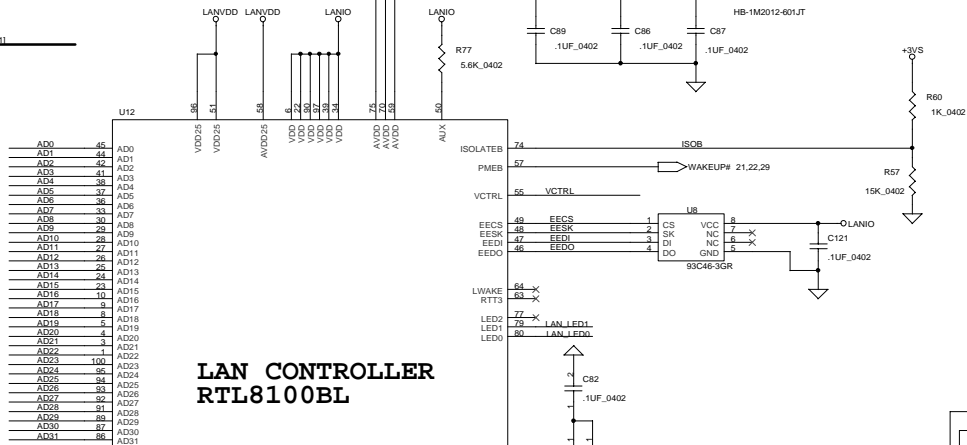
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LAN Realtek RTL8100



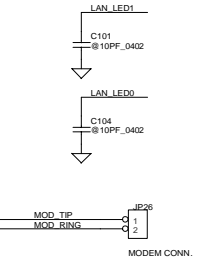
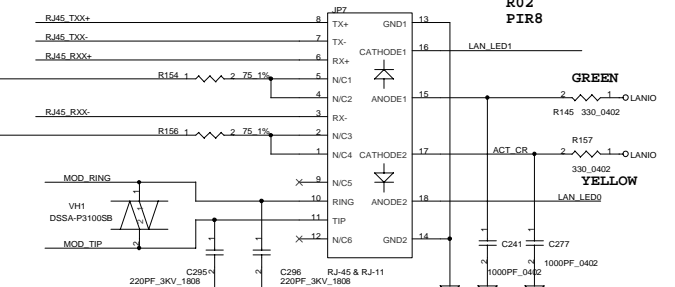
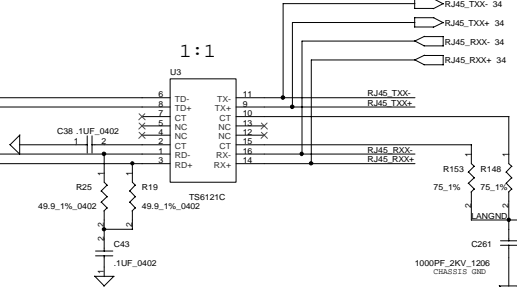
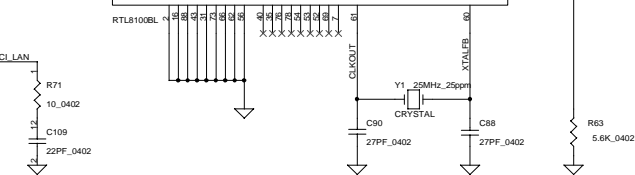
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18.21,22,34 CBE#2
18.21,22,34 CBE#3

18.20,21,22,34 FRAME#
18.20,21,22,34 IRDY#
18.20,21,22,34 TRDY#
18.20,21,22,34 DEVSEL#
18.20,21,22,34 STOP#
18.20,21,22,34 PERR#
18.20,21,24 SERR#
18.21,22,34 PARK#
18.20 REQ#3
18.20 GNT#3
18.20 PIRCB#
18.20 PCIRST#

12 CLK_PCI_LAN



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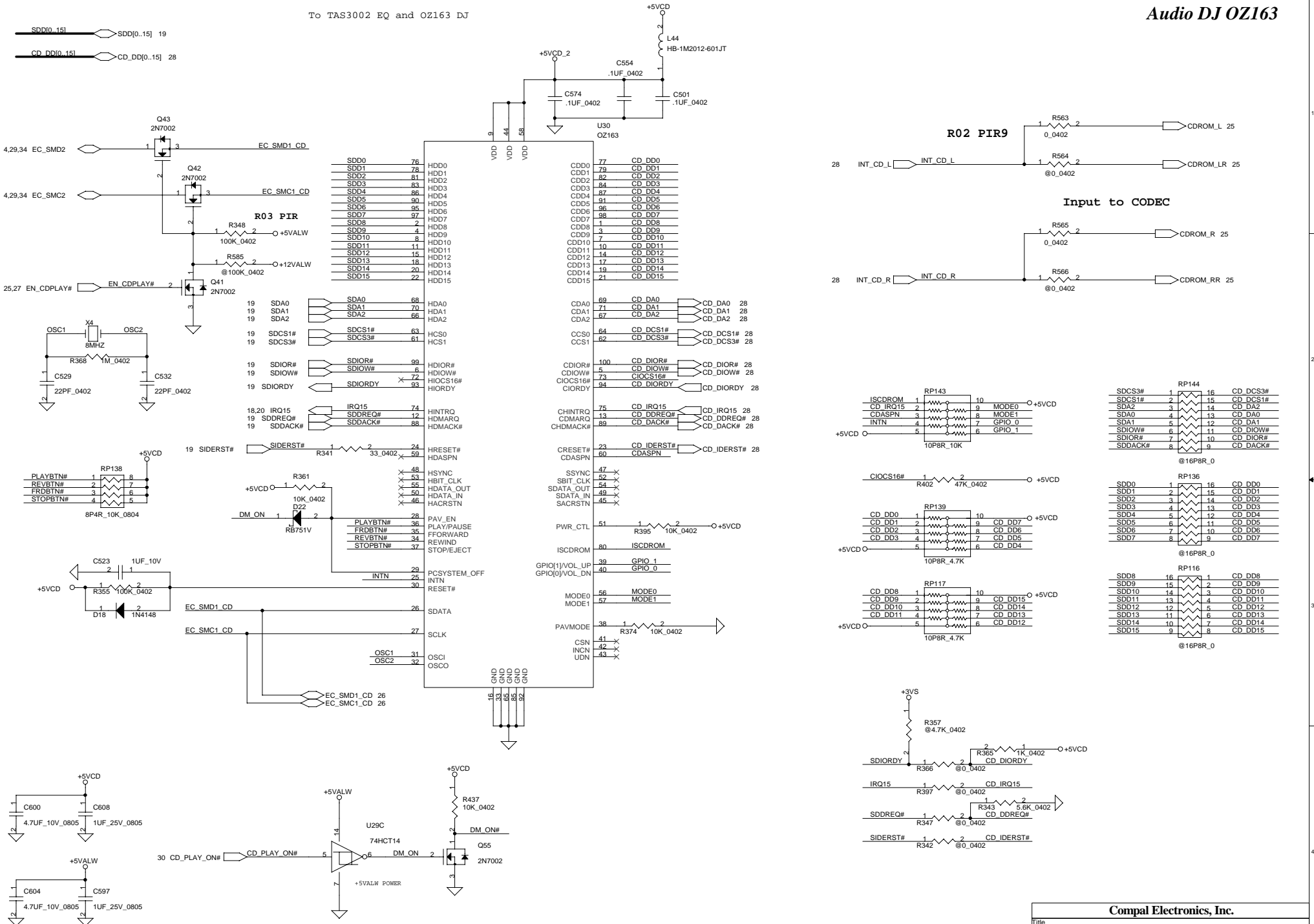
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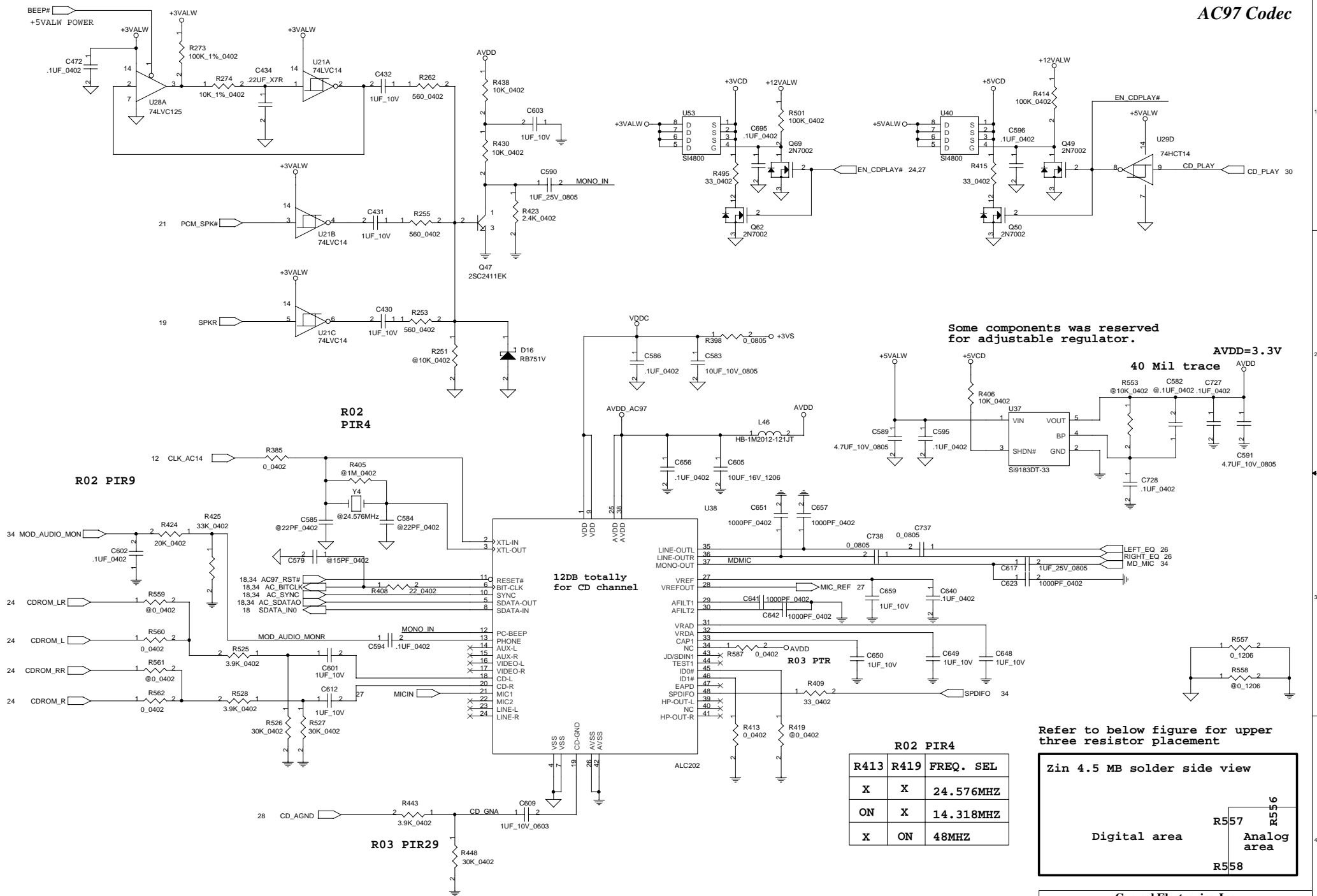
To TAS3002 EQ and OZ163 DJ

Audio DJ OZ163



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Some components was reserved for adjustable regulator.

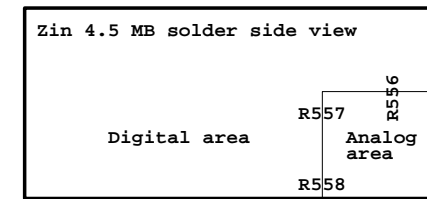
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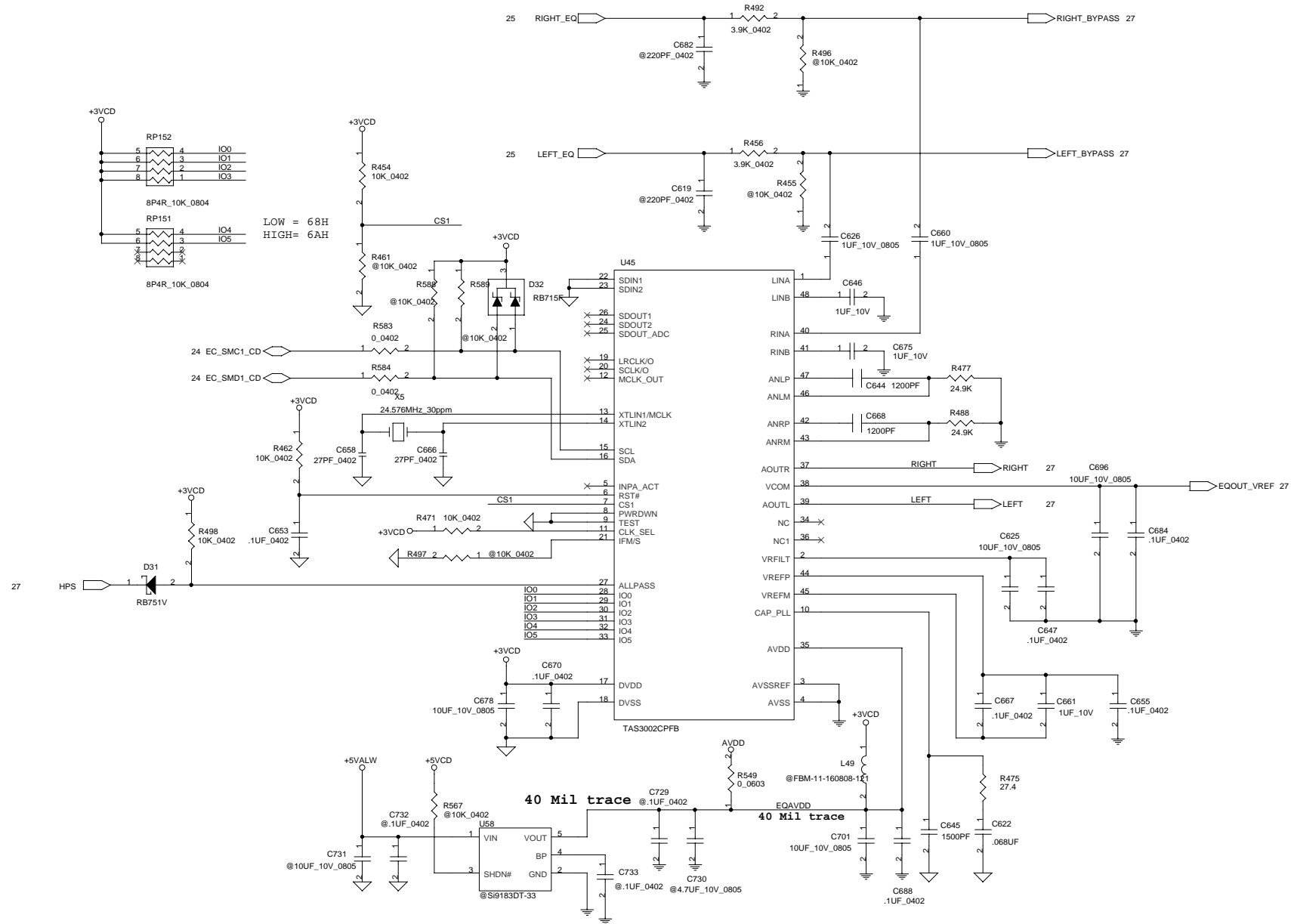
40 Mil trace

R02 PIR4

R413	R419	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ

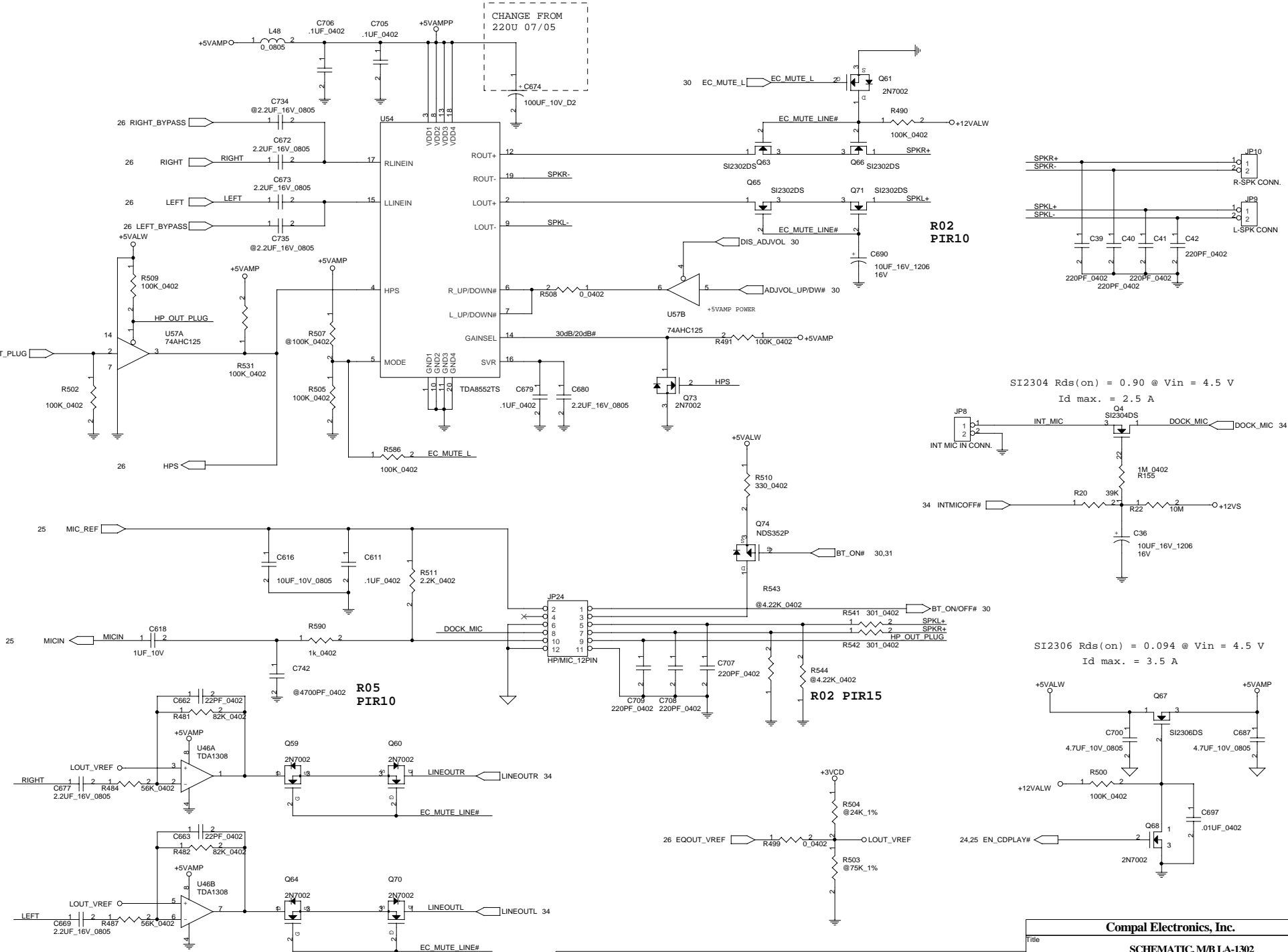
Refer to below figure for upper three resistor placement





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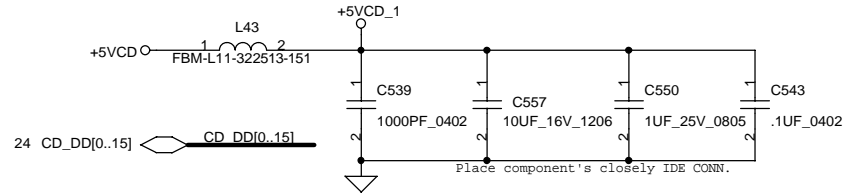
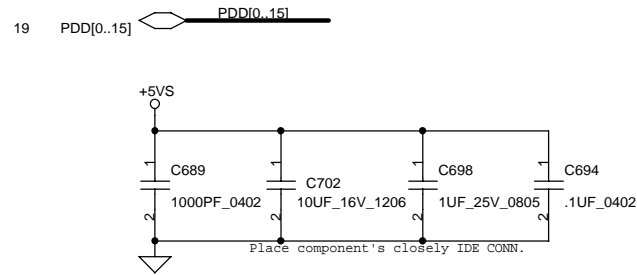
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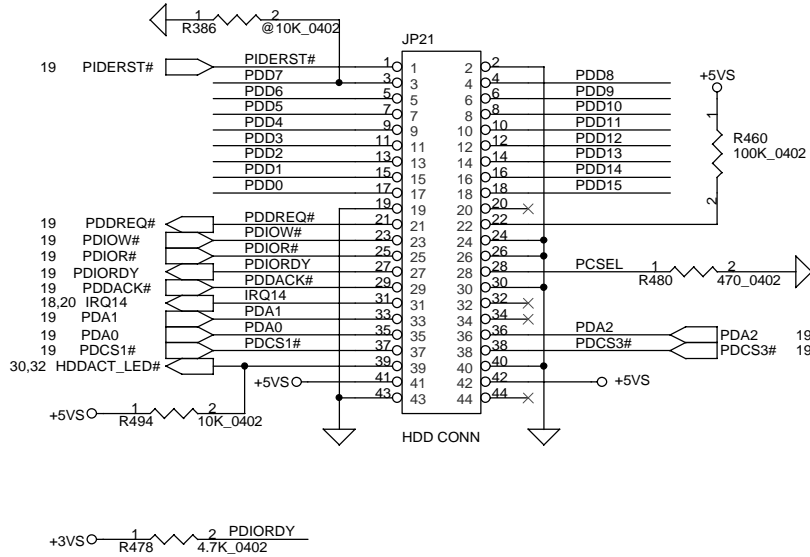
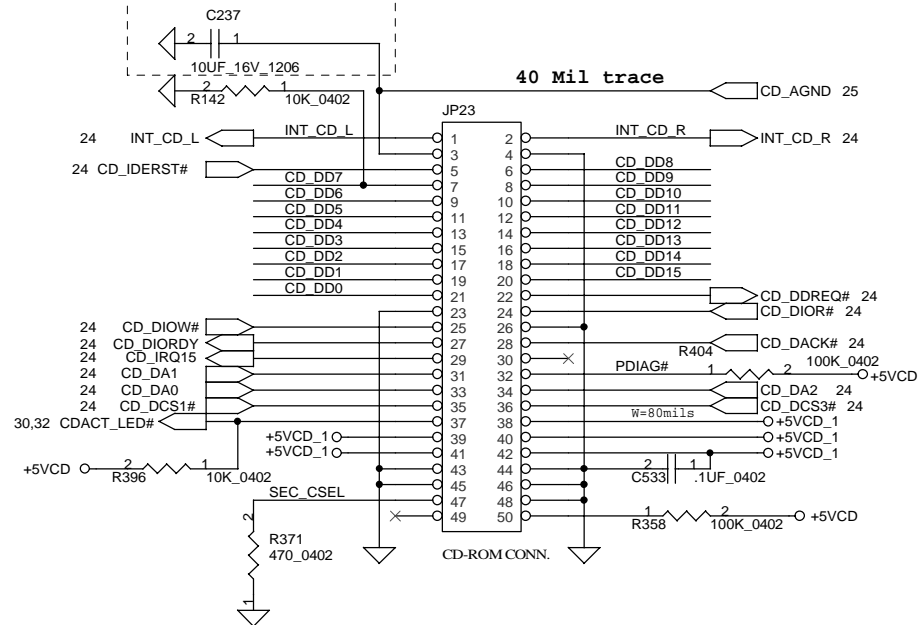
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HDD/CD-ROM Module



R03 PIR16



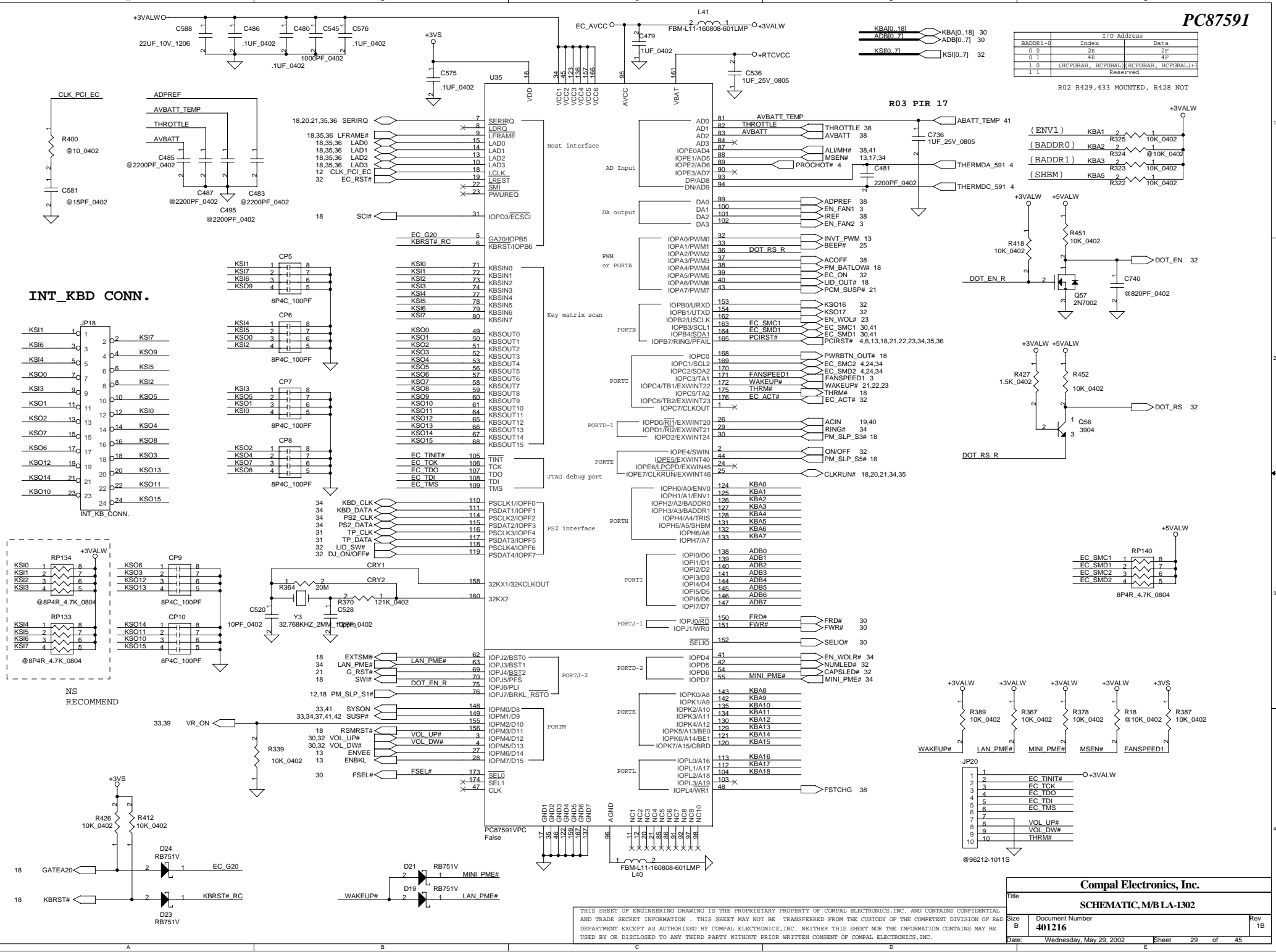
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I/O Address		
BADDR1-d	Index	Data
0 0	2E	2F
0 1	4E	4F
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1 1	Reserved	

R02 R429, 433 MOUNTED, R428 NOT

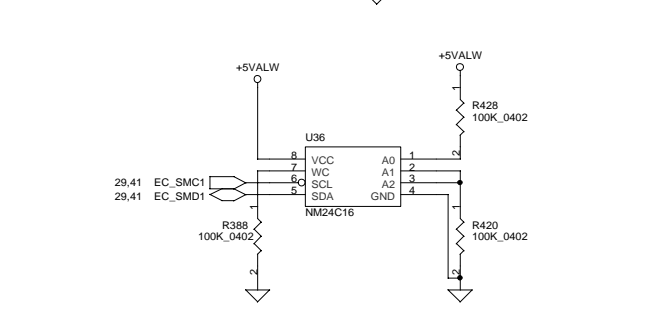
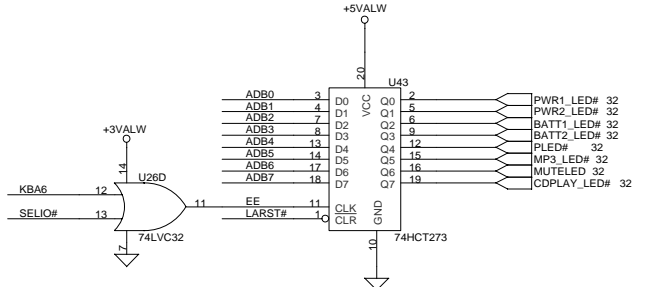
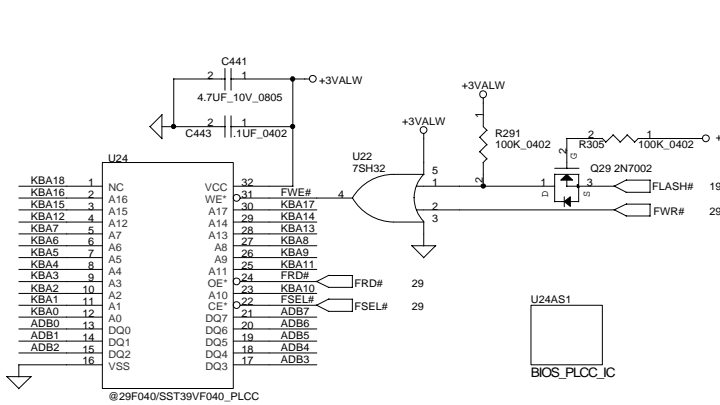
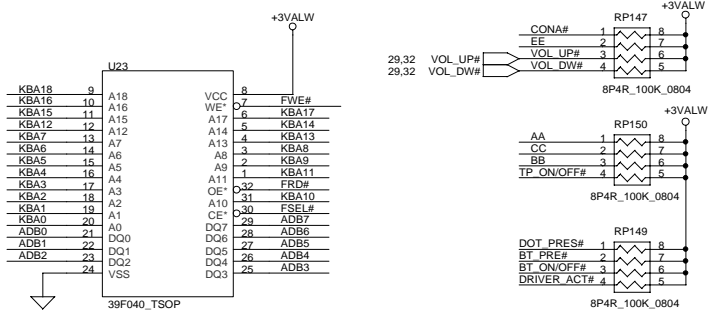
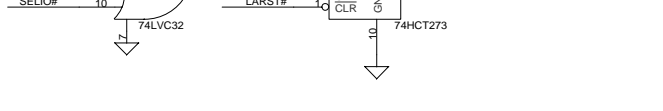
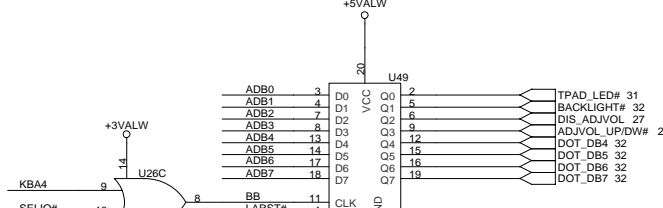
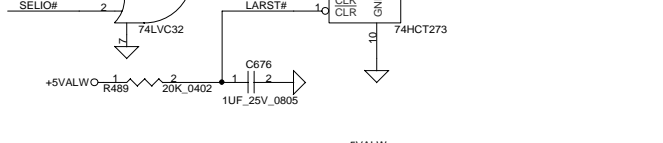
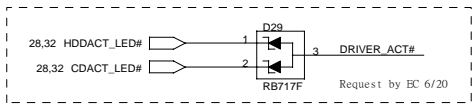
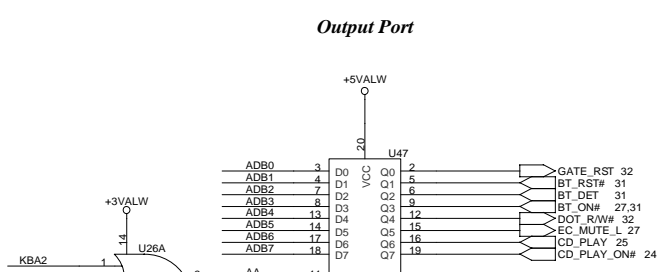
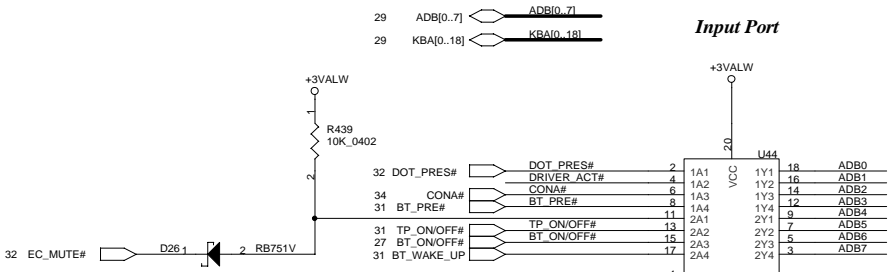


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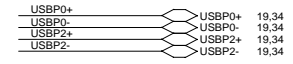
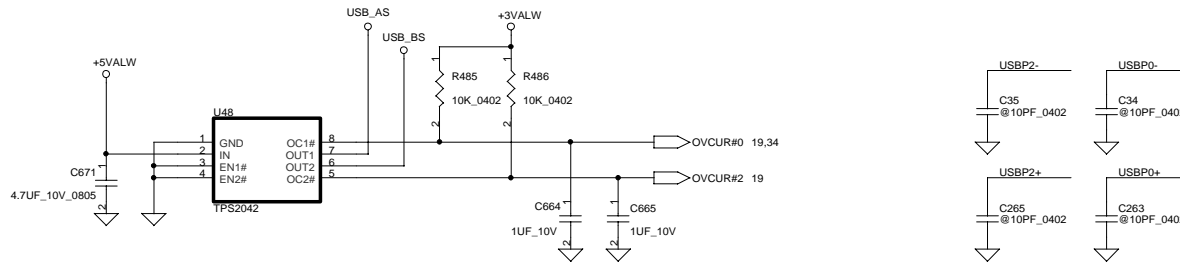
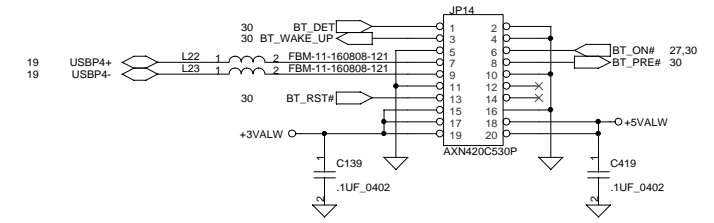
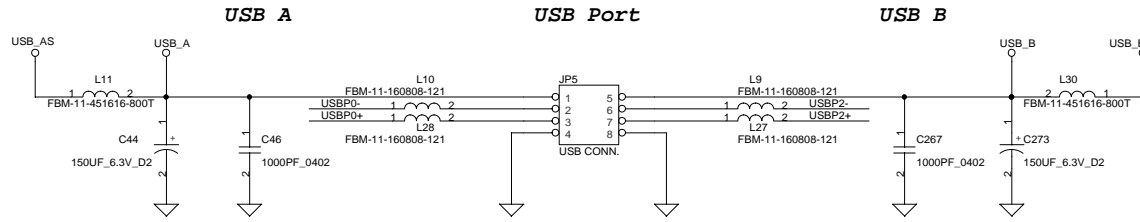


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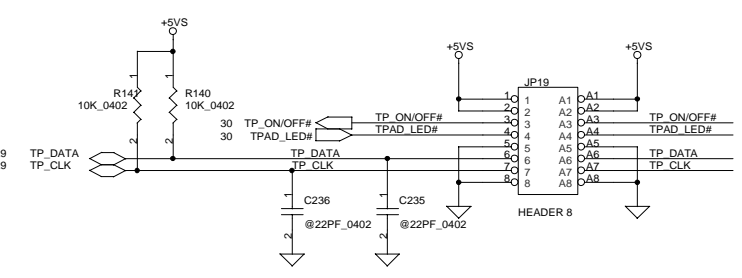
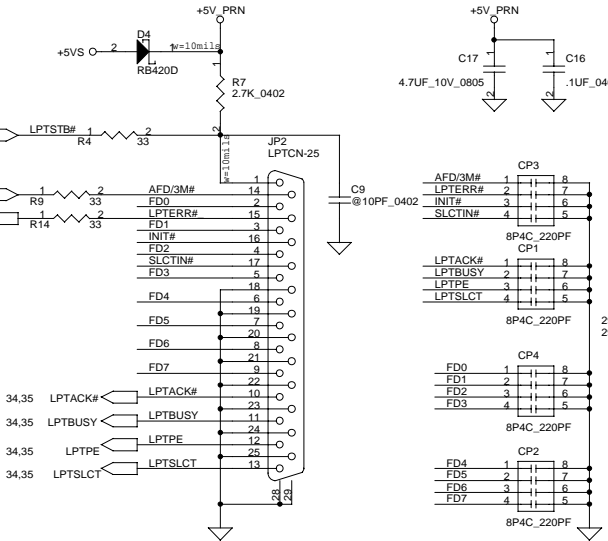
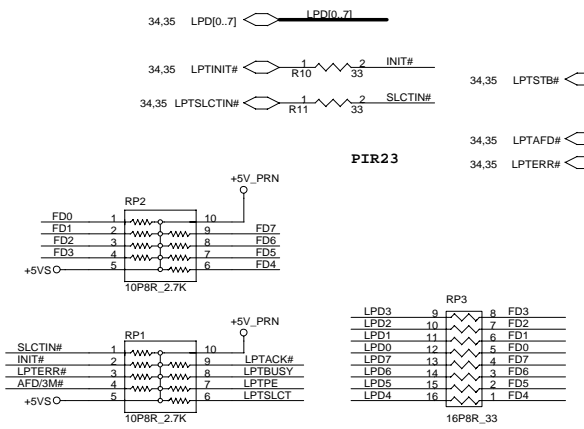
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Printer Port/USB

Bluetooth Connector



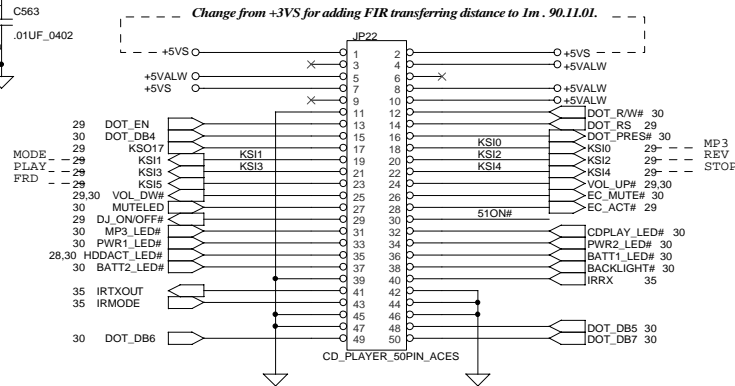
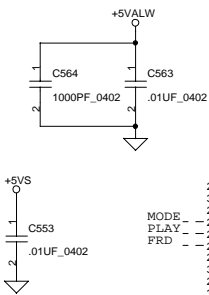
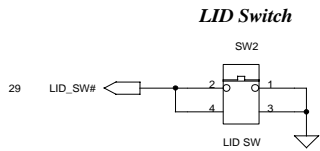
Parallel Port



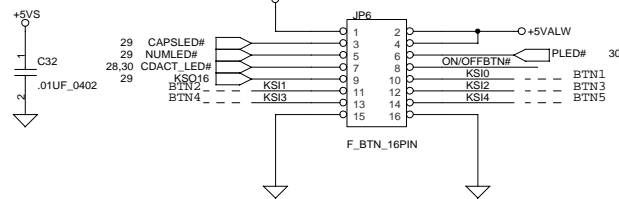
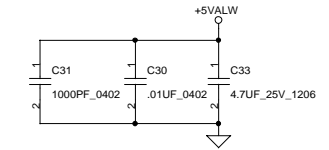
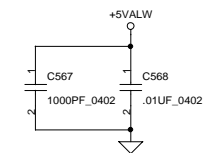
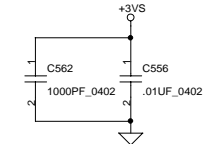
Compal Electronics, Inc.

SCHMATIC, M/B LA-1302

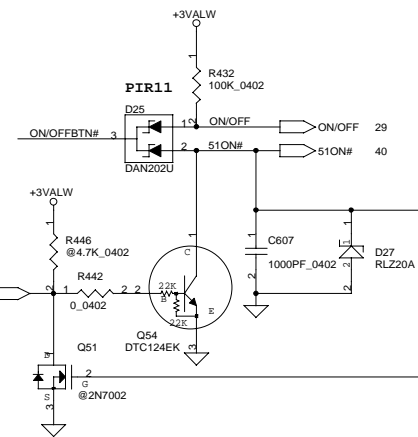
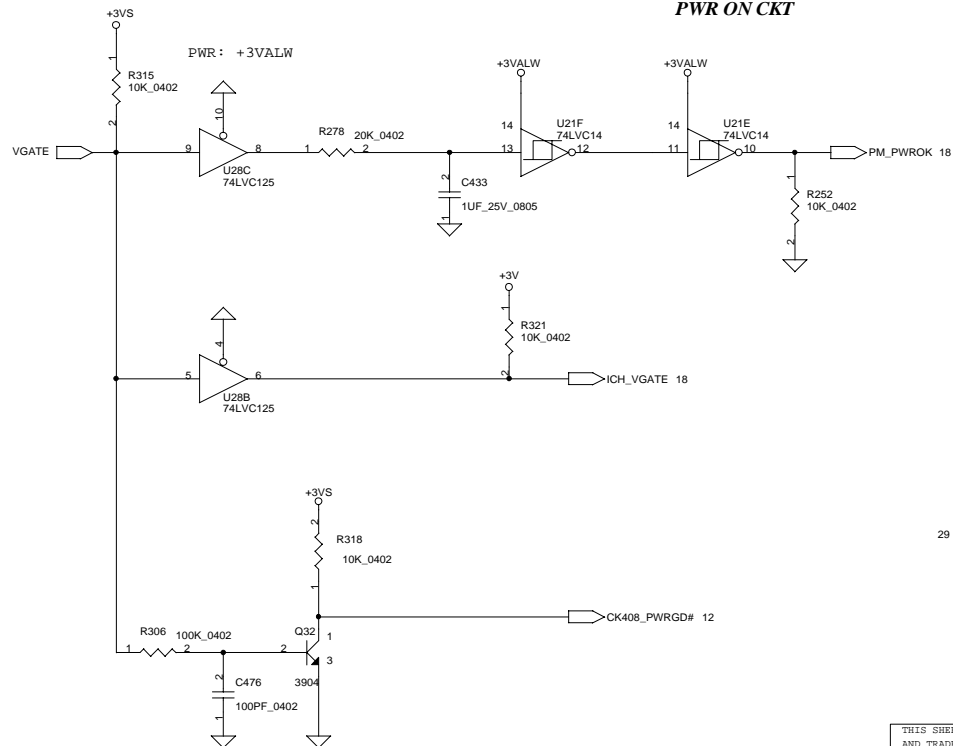
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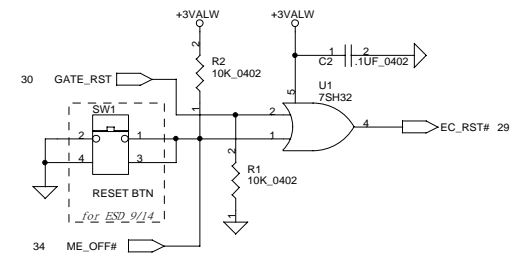
Dot Matrix LCD/FIR



PWR ON CKT



M/E OFF Button

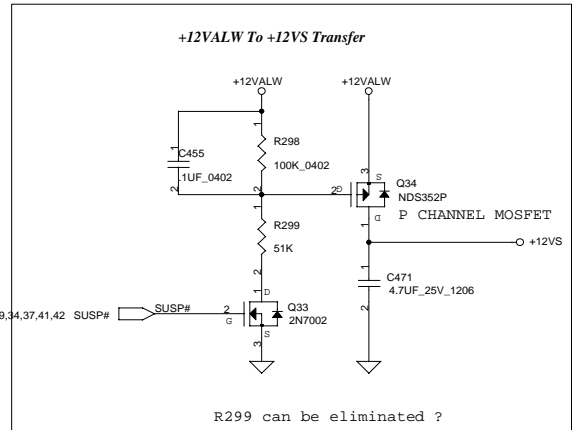
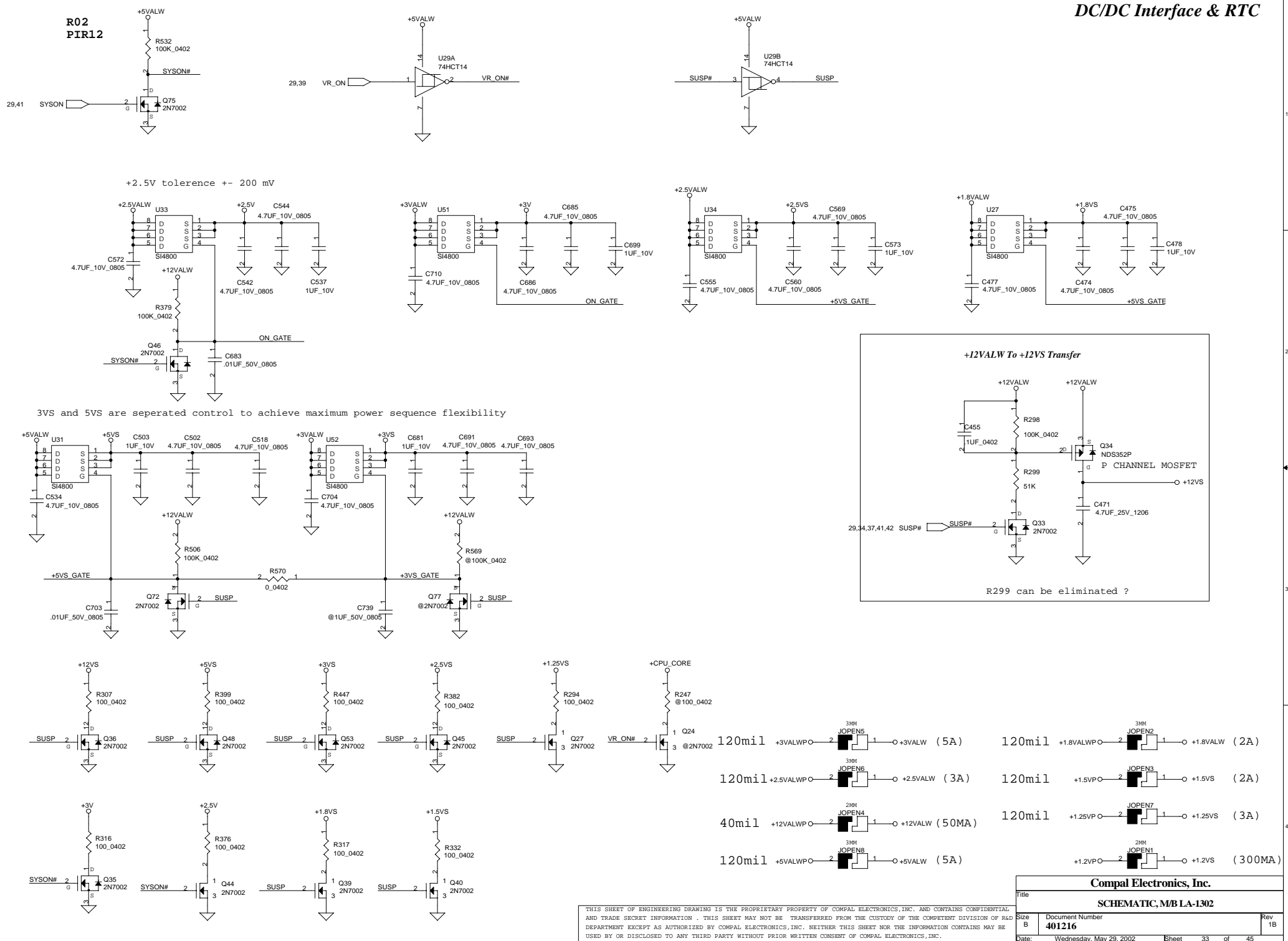


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DC/DC Interface & RTC

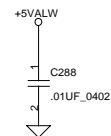
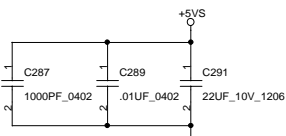
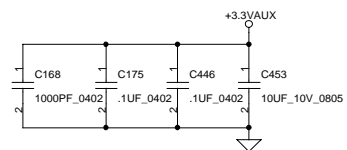
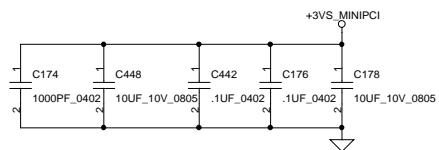
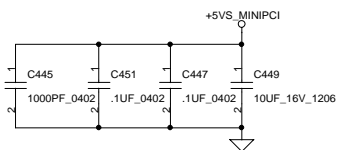
R02
PIR12



120mil	+3VALWPO	JOPEN5	33M	1	+3VALW (5A)	120mil	+1.8VALWPO	JOPEN2	33M	1	+1.8VALW (2A)
120mil	+2.5VALWPO	JOPEN6	33M	1	+2.5VALW (3A)	120mil	+1.5VPO	JOPEN3	33M	1	+1.5VS (2A)
40mil	+12VALWPO	JOPEN4	23M	1	+12VALW (50MA)	120mil	+1.25VPO	JOPEN7	33M	1	+1.25VS (3A)
120mil	+5VALWPO	JOPEN8	33M	1	+5VALW (5A)	120mil	+1.2VPO	JOPEN1	33M	1	+1.2VS (300MA)

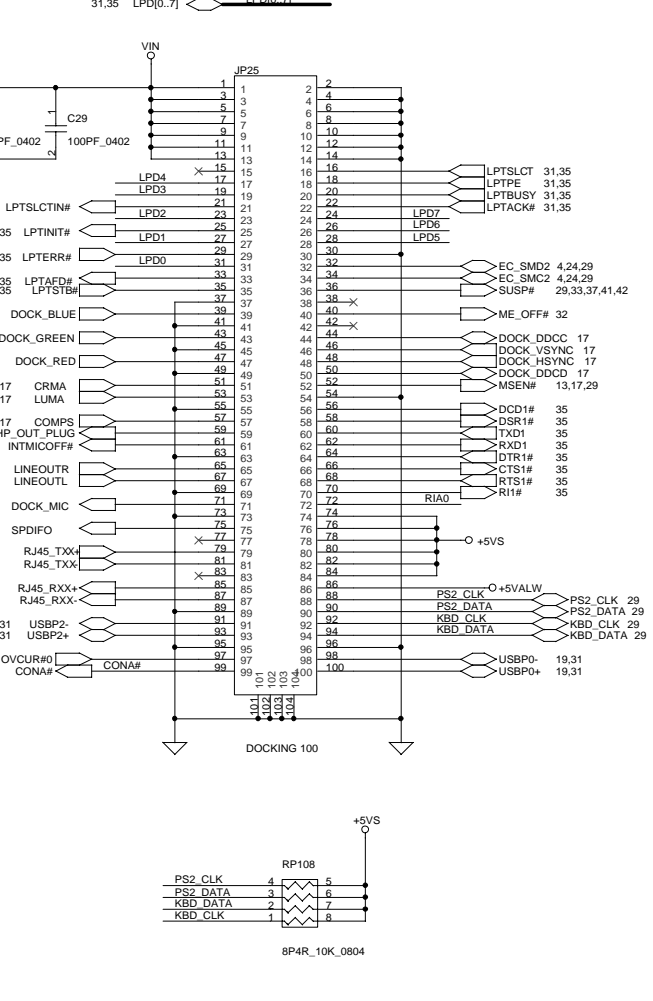
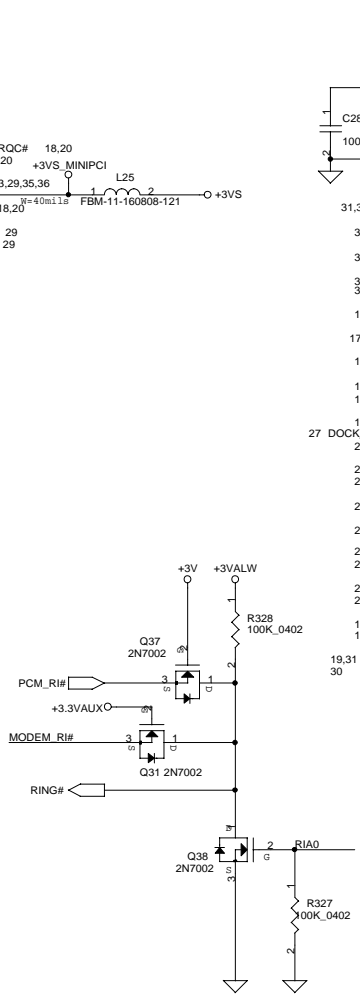
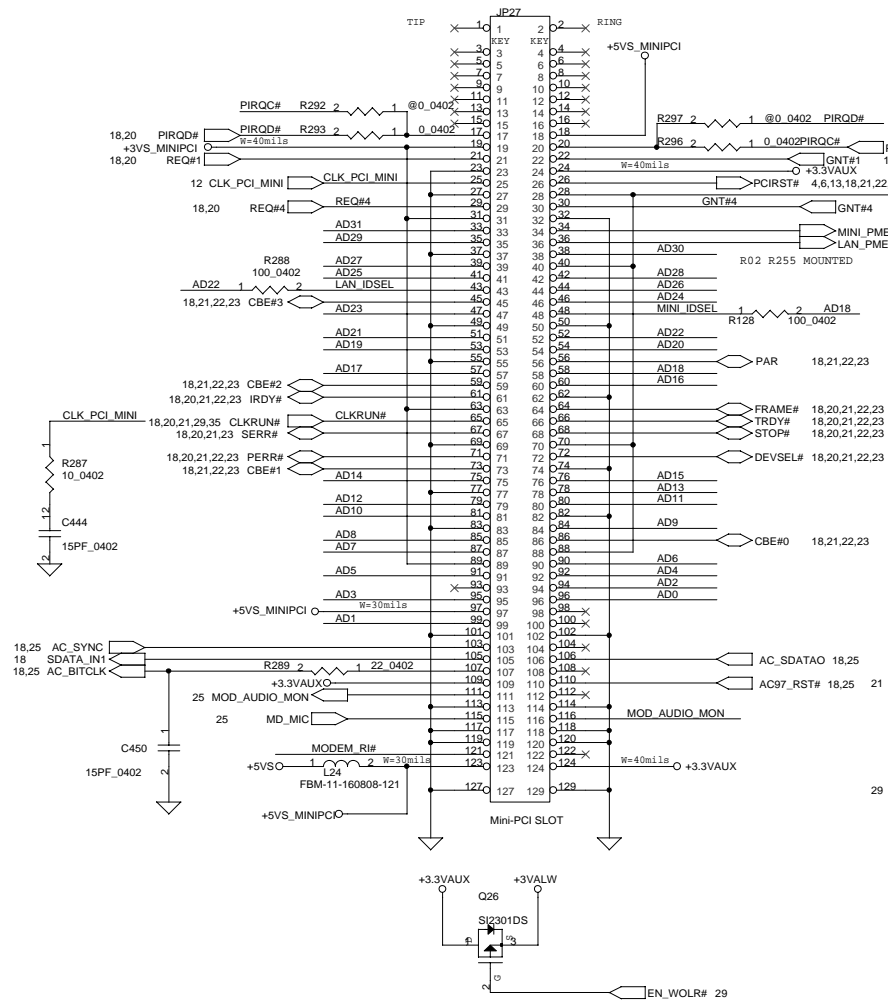
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AD[0..31] AD[0..31] 18,21,22,23

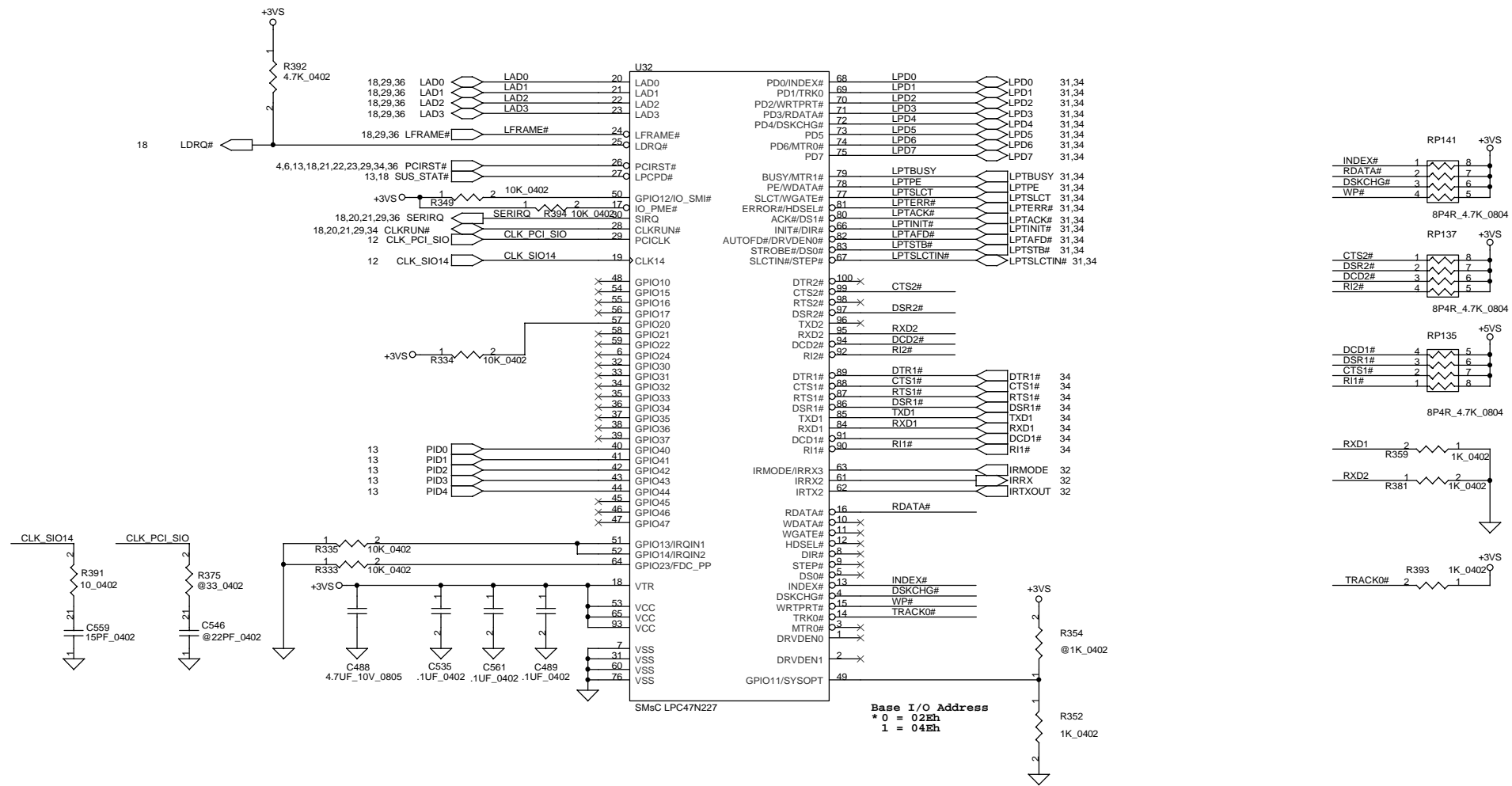
31,35 LPD[0..7] LPD[0..7]



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SUPER I/O SMC FDC47N227



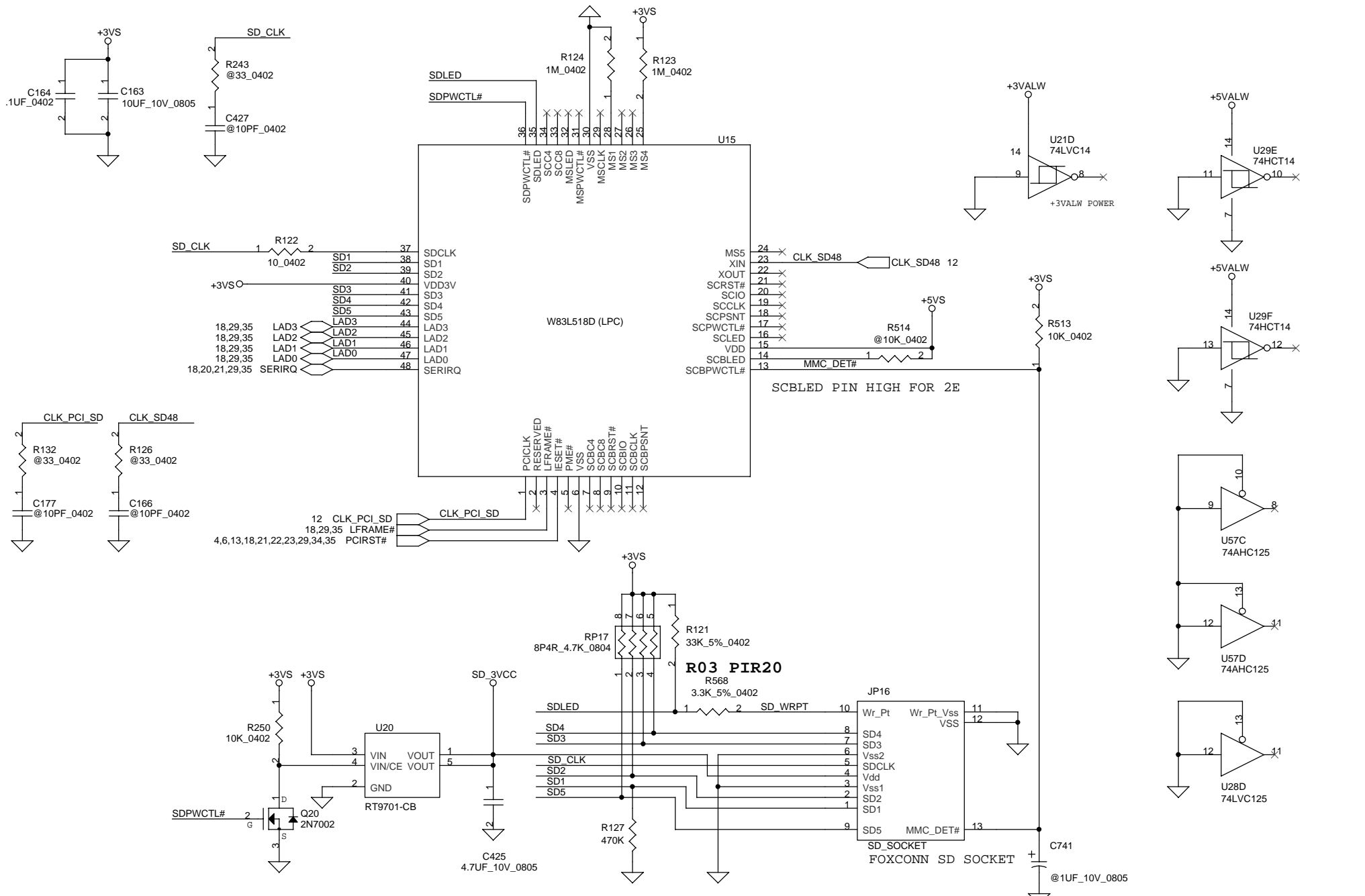
Base I/O Address
 * 0 = 02Eh
 * 1 = 04Eh

Compal Electronics, Inc.

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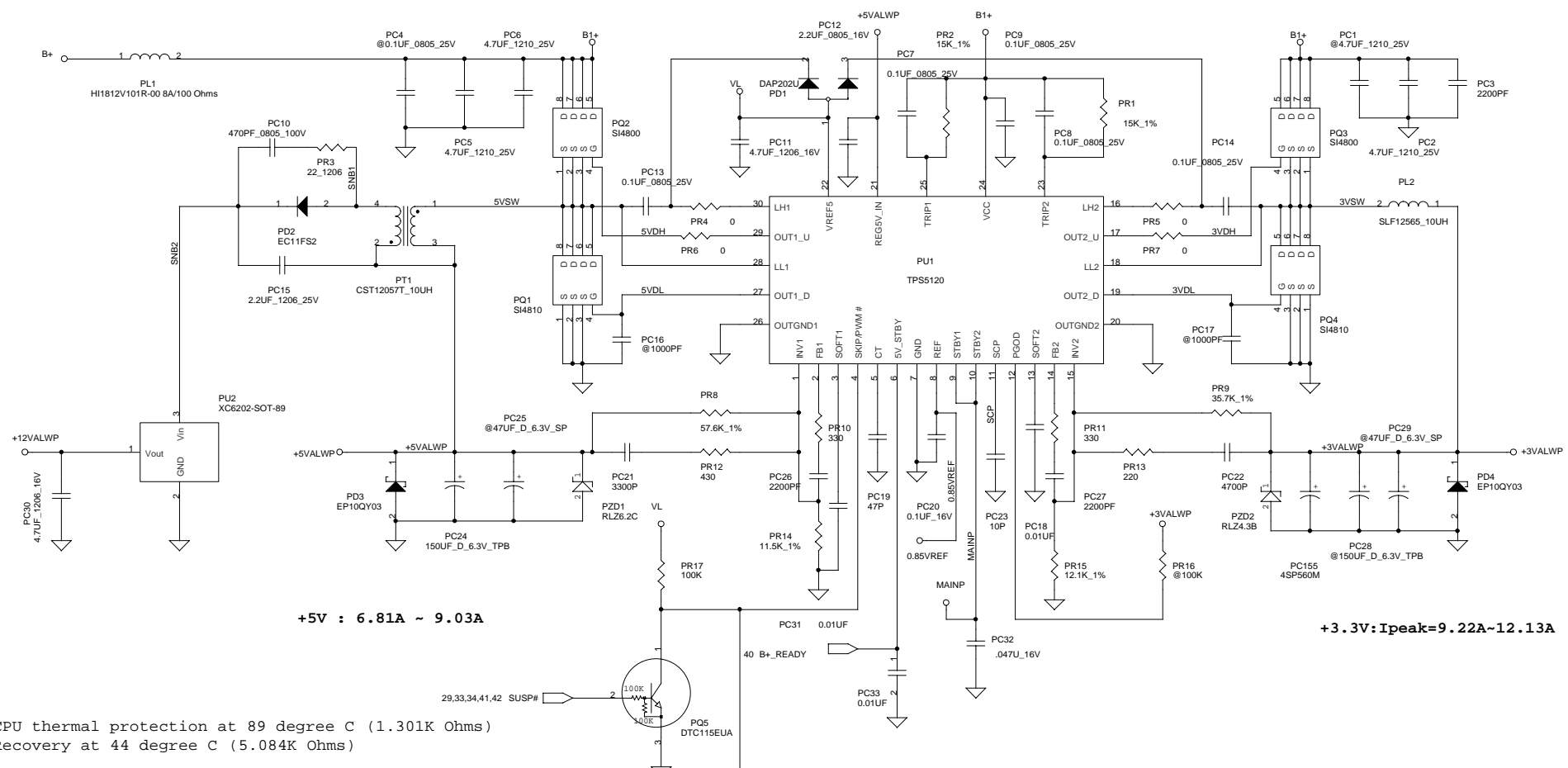
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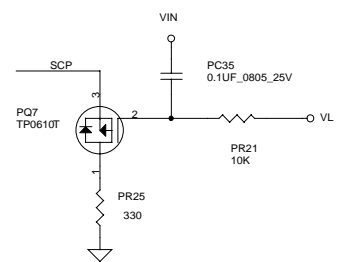
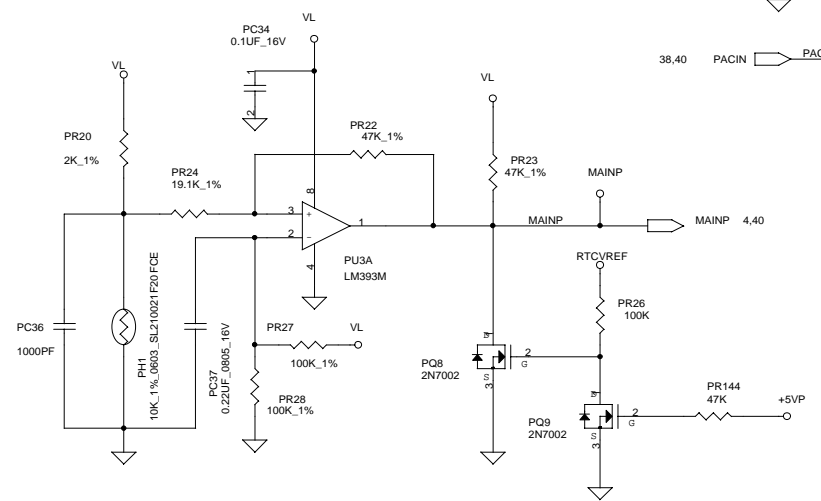


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CPU thermal protection at 89 degree C (1.301K Ohms)
 Recovery at 44 degree C (5.084K Ohms)

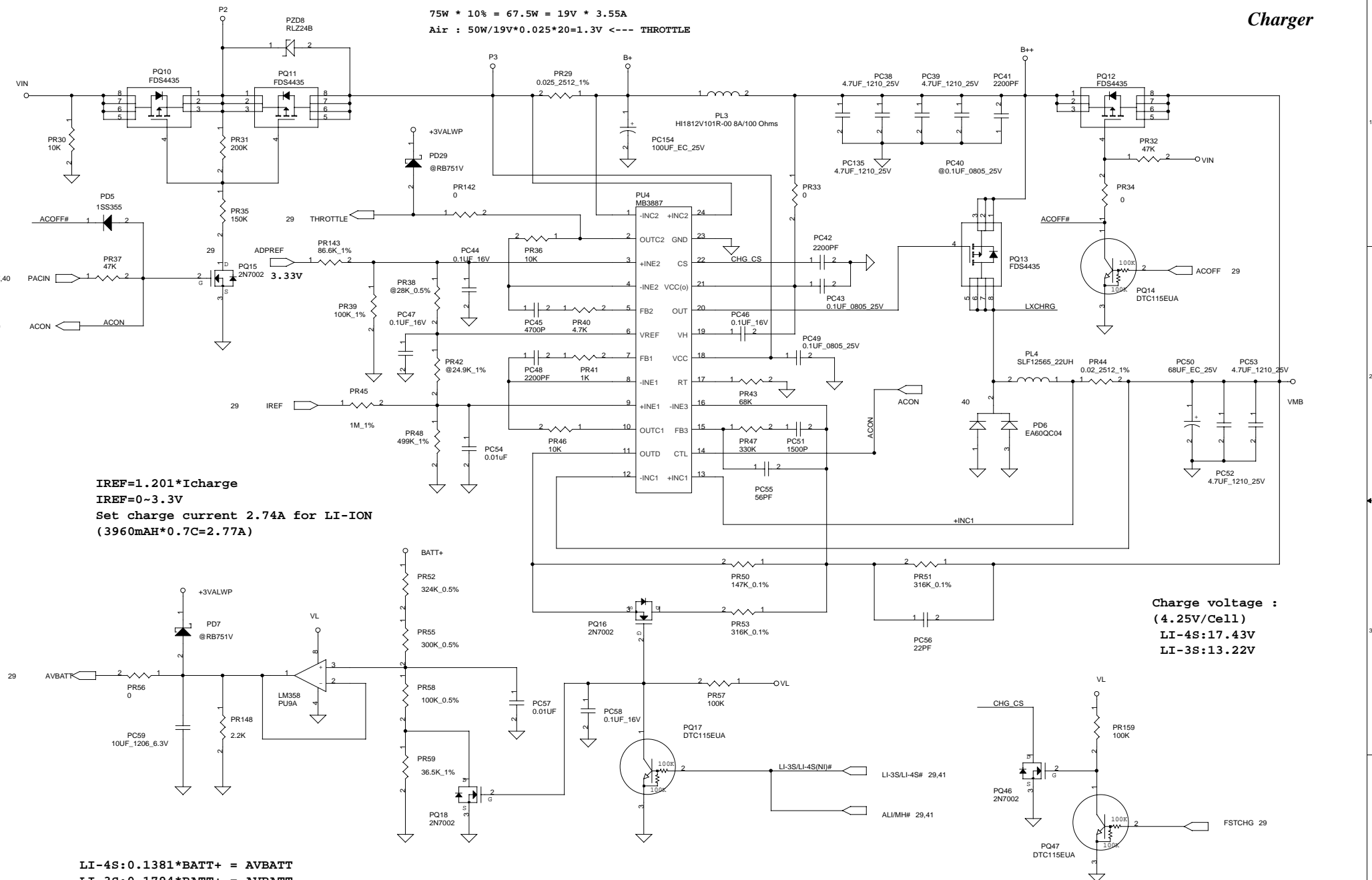


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Charger

75W * 10% = 67.5W = 19V * 3.55A
 Air : 50W/19V*0.025*20=1.3V <--- THROTTLE



IREF=1.201*Icharge
IREF=0~3.3V
 Set charge current 2.74A for LI-ION
 (3960mAh*0.7C=2.77A)

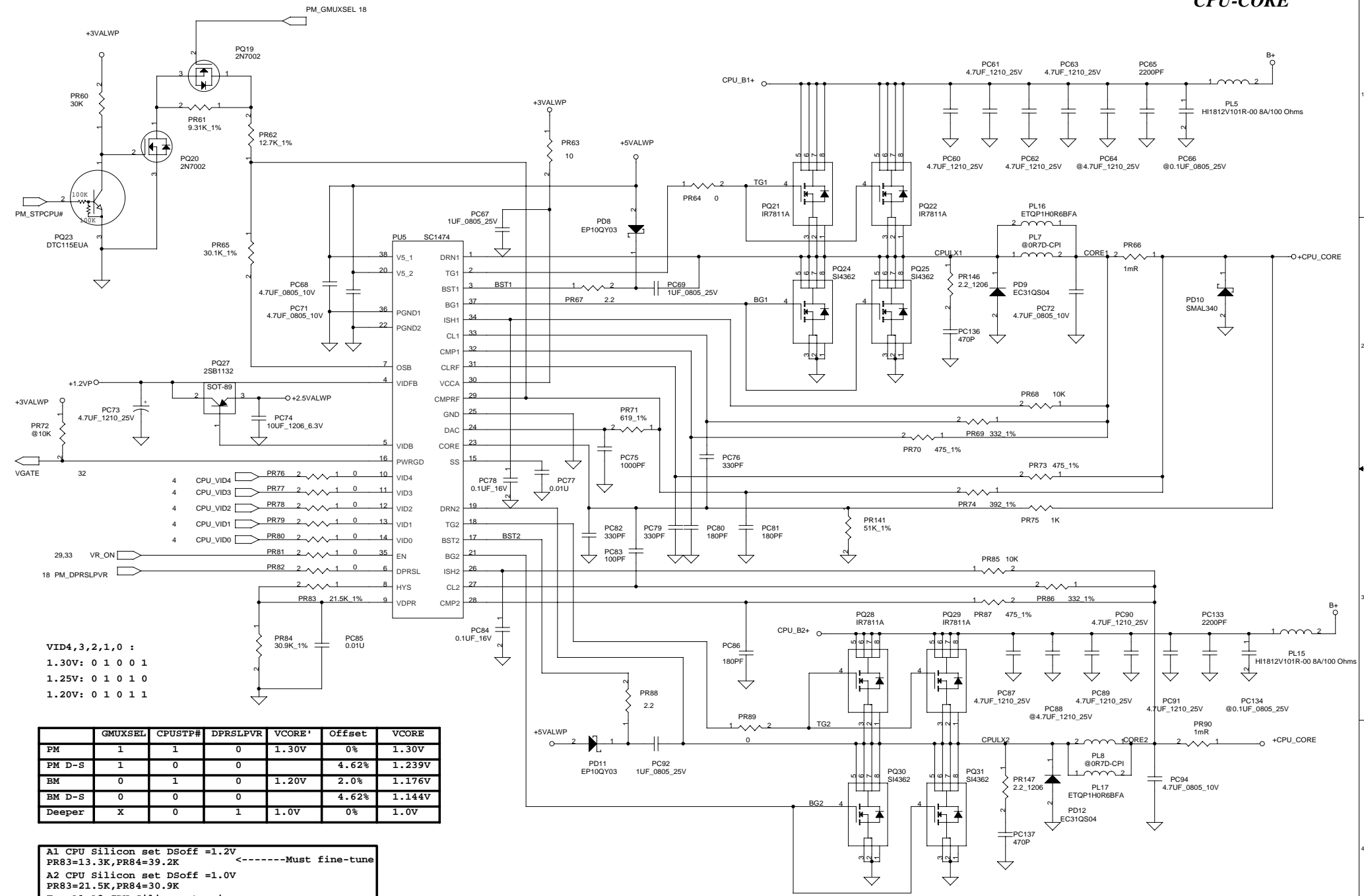
Charge voltage :
(4.25V/Cell)
LI-4S:17.43V
LI-3S:13.22V

LI-4S:0.1381*BATT+ = AVBATT
LI-3S:0.1794*BATT+ = AVBATT

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CPU-CORE



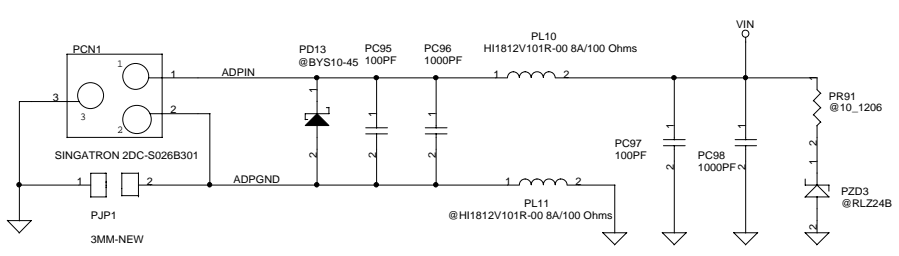
VID4,3,2,1,0 :
 1.30V: 0 1 0 0 1
 1.25V: 0 1 0 1 0
 1.20V: 0 1 0 1 1

	GMUXSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

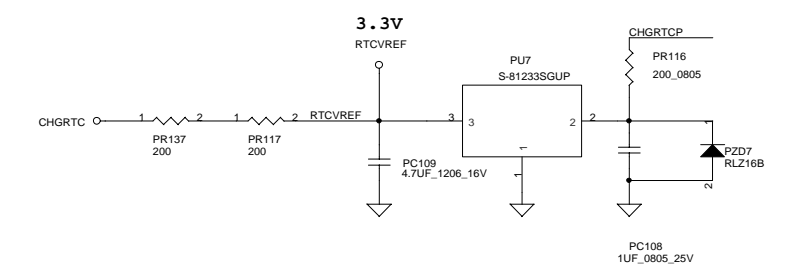
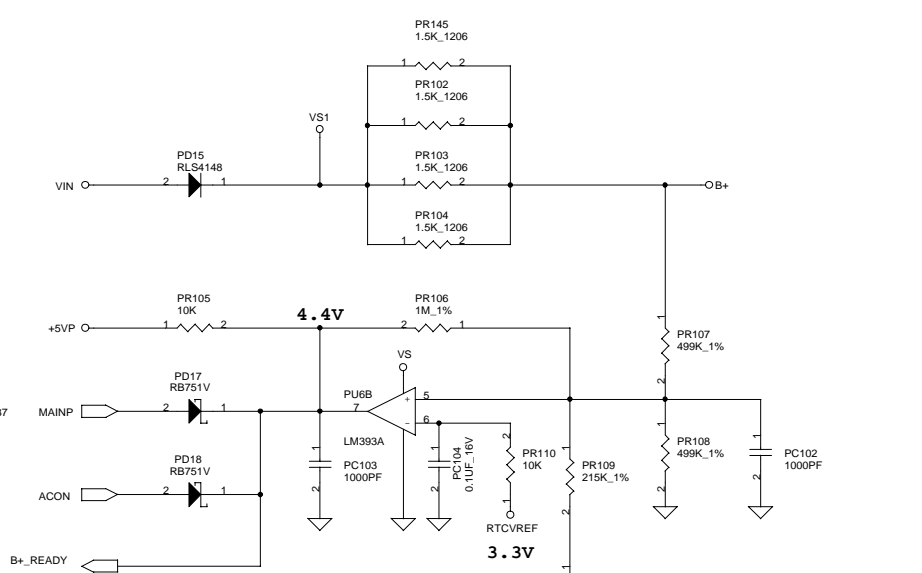
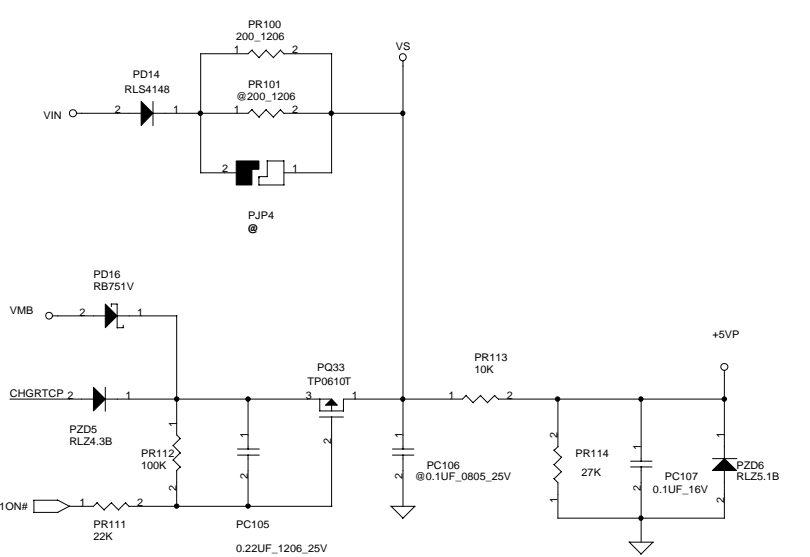
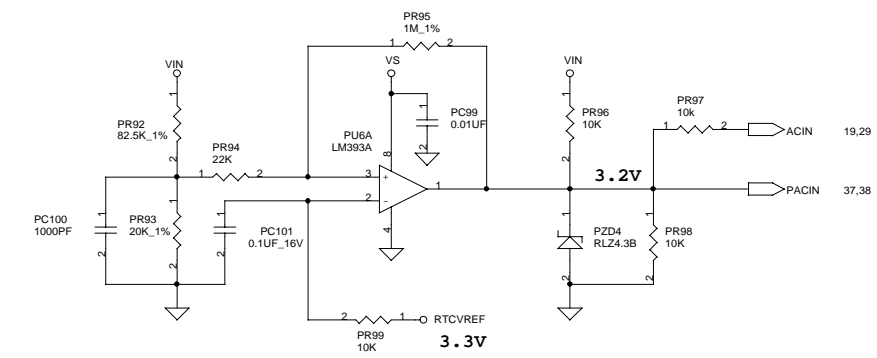
A1 CPU Silicon set Dsoff =1.2V
 PR83=13.3K,PR84=39.2K <-----Must fine-tune
 A2 CPU Silicon set Dsoff =1.0V
 PR83=21.5K,PR84=30.9K
 For A1,A2 CPU Silicon stepping
 PQ19 is nopop, PR61=0, PR62=13K and PR65 is nopop
 For B0 CPU Silicon stepping
 PQ19 is pop, PR61=9.31K,PR62=12.7K and PR65=30.1K

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VIN detector		
16.90	17.55	18.22
16.46	17.08	17.72



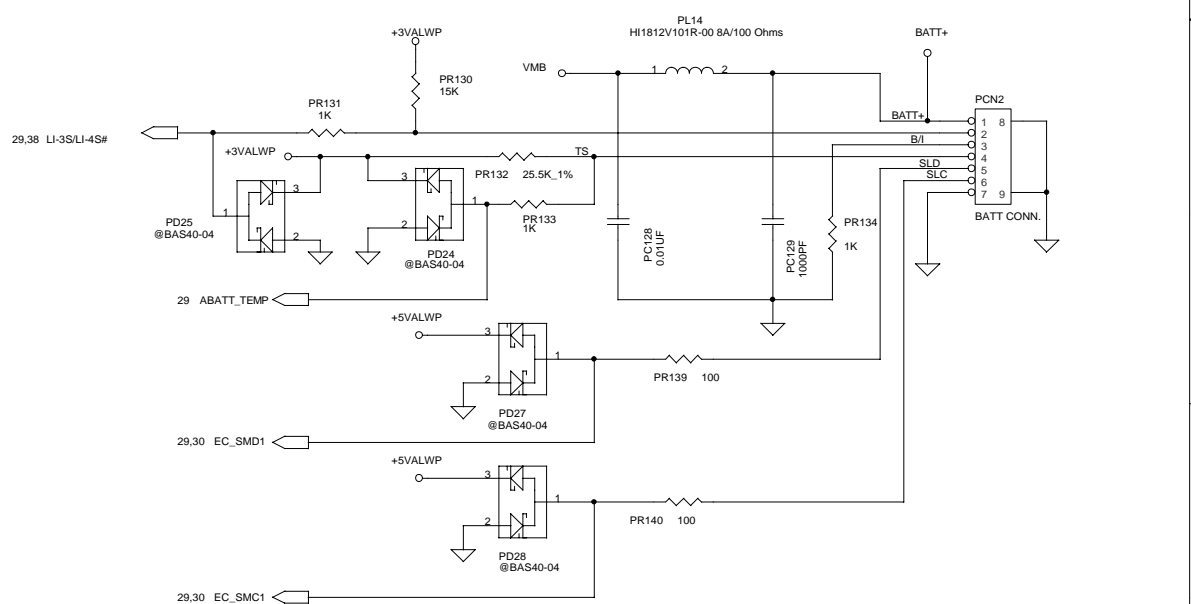
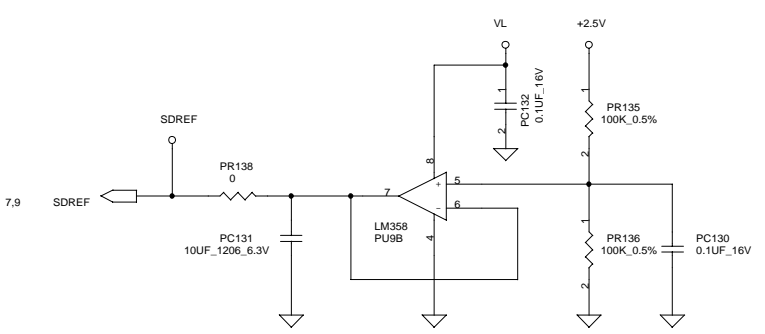
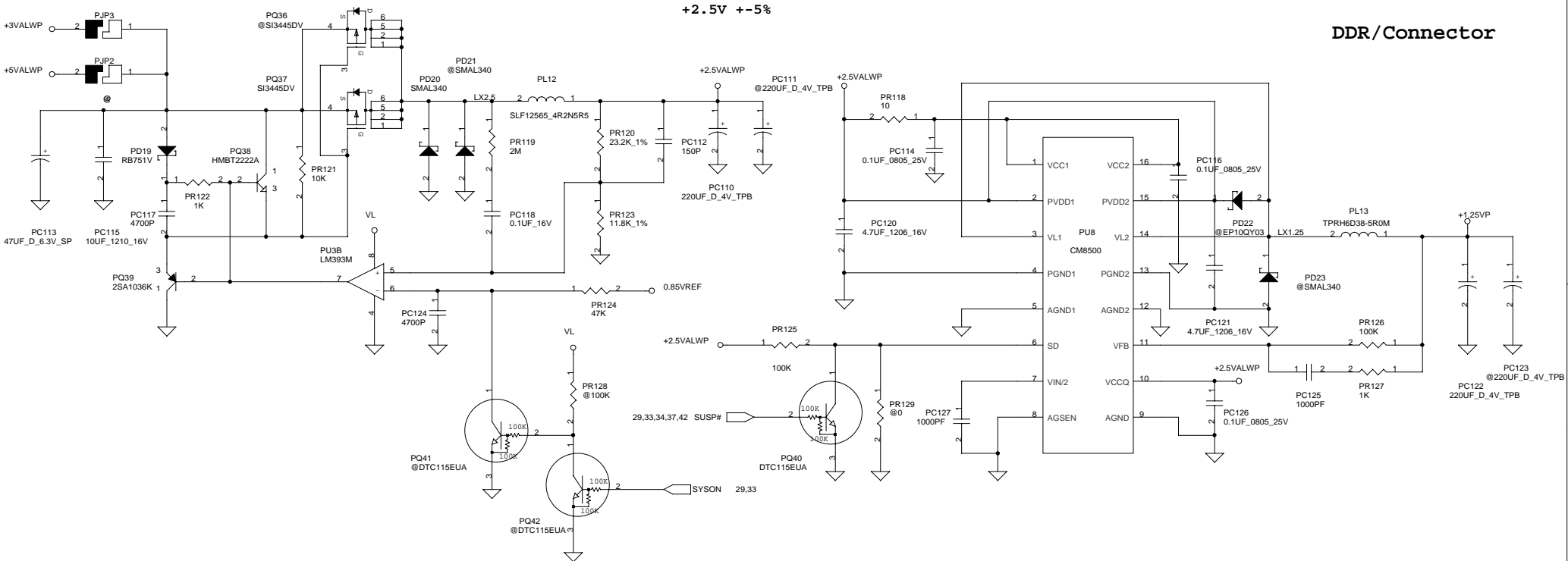
Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

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DDR/Connector

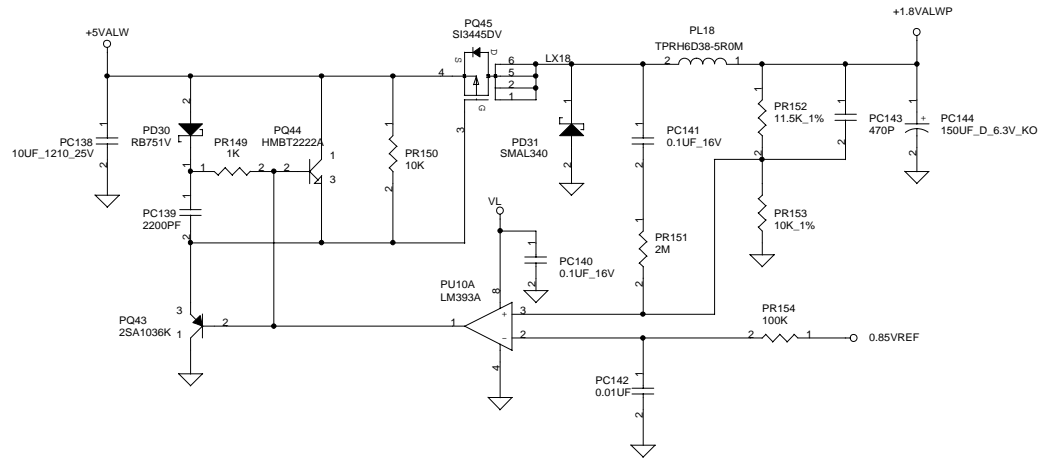
+2.5V +-5%



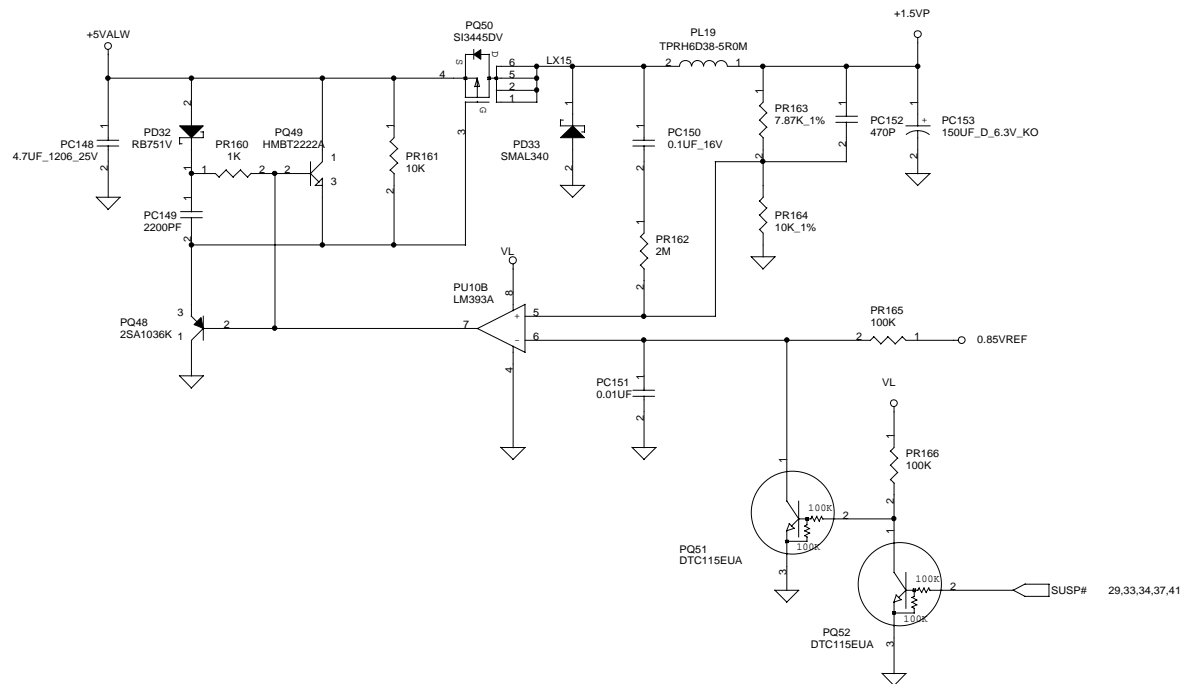
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+1.8V+-5%



+1.5V+-5%



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Voltage Rails

Power Plane	Description	S1	S3	S5	FUNCTION	RELATED POWER NET NAME
VIN	Adapter power supply (19V)	N/A	N/A	N/A	Pullhigh,Switch,DOCKING,VL,AC IN.	VIN1
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	Pullhigh,Switch,B1+,PWR MB3878,PWR MAX1718.	B++,B1+,CPU_B1+,CPU_B2+
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	Pullhigh,Switch,NB,CPU.	
+2.5VALW	2.5V always on power rail	ON	ON	ON*	Pullhigh,Switch,NB,DDR SODIMM.	LANVDD
+2.5V	2.5V power rail	ON	ON	OFF	Pullhigh,Switch,NB,DDR SODIMM.	
+2.5VS	2.5V switched power rail	ON	OFF	OFF	Pullhigh,Switch,NB,CLK Buffer,SB,LANVDD.	+VCCCHK,+VCCMCK,+VCCMDLL,+2.5VRGBPLL,+2.5VRGBDAC,+2.5VSBRAM +SB_PLLVDD
+3VALW	3.3V always on power rail	ON	ON	ON*	Pullhigh,Switch,PCMCIA Switch,LAN,CMOS,KBD CTRL, SMBus,BIOS,BlueTooth, USB	+3VCD(+3VCD_A), LANIO, +3.3VAUX
+3V	3.3V power rail	ON	ON	OFF	Pullhigh,Switch,SB,PCMCIA CTRL,CMOS,PANEL.	LCDVDD,+3V_CB
+3VS	3.3V switched power rail	ON	OFF	OFF	Pullhigh,DJ,Switch,LOGIC,KBD,SIO,LAN,1394,	VDDC,+3VS_MINIPCI,LCDVDD(LCDVDD_1),TV_DVDD,LVDS_PLLVCC(LVDS_VCC)
+5VALW	5V always on power rail	ON	ON	ON*	Pullhigh,Docking,DJ,Switch,BT,LOGIC,AVDD(Audio),Thermal,FAN.	+5VCD(+5VCD_1,+5VCD_2),AVDD(AVDD_AC97),S1_VCC,+5VAMP,INV_B+
+5V	5V power rail	ON	ON	OFF	Pullhigh,Switch.	
+5VS	5V switched power rail	ON	OFF	OFF	Pullhigh,Docking,MiniPCI,+5VALW, USB,T/P,LPT,DJ,HDD,TV,CRT,Inverter,Switch,VID.	+5VFAN1,+5VFAN2,CRTVDD,+5V_PRN,+5VS_MINIPCI,USB_AS(USB_A), USB_BS(USB_B),TV_VDD,TV_AVDD
+12VALW	12V always on power rail	ON	ON	ON*	PC CARD,Pullhigh,Switch,MOS	
+12VS	12V switched power rail	ON	OFF	OFF	Switch,Power MOS.	
+RTCVCC	RTC power	ON	ON	ON	RTC Power.	
+1.25VS	1.25V switched power rail	ON	OFF	OFF	Pullhigh,DDR termination.	1.25VP
+1.2VS	1.2V switched power rail	ON	OFF	OFF	CPU	1.2VP,+H_VCCA,+HVCCIOPLL

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
LAN	AD17	3	PIRQB
CardBus	AD20	2	PIRQA
Mini-PCI	AD18	4	PIRQD
Mini-PCI LAN	AD22	1	PIRQC
IEEE-1394 Controller	AD16	0	PIRQA
AGP VGA			PIRQA

VGA LCD PANEL ID LIST

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM	1010 000X b

EC SM Bus2 address

Device	Address
AD1032	1001 100X b
OZ163	0011 0100 b
Docking	0011 011X b
EQ TAS3002	0110 011X b

ICH3-M SM Bus address

Device	Address
SODIMM	1010 000X b
Clock Gen	1101 001x b

P.S:Default Resistor & Capacitor's package are 0603.
Default 8P4R package is 0402.

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PIR listing :

PAGE 4	PIR1	CHANGE THERMAL SENSOR FROM MAX6654 TO ADM1032	DEL U11, R78, R86; ADD U56, R519
PAGE 5	PIR2	COST DOWN CPU CAPS	DEL C110, C377 ADD DIP 560UF_4V_14m C715, C716; C72, C97, C126 NOT ON
PAGE 6	PIR3	REMOVE AGP_BUS PULLUPS	RP111, RP11, RP12, RP15 NOT ON
PAGE 12			CHANGE R284, R285 FROM 33 OHM TO 10 OHM
PAGE 24	PIR4	AUDIO CODEC CHANGED FROM ALC201 TO ALC202	ADD R286 10_0402; U41, C592, C615, C593, R459, R458, C621, R433, R417, C598, R449, R444
PAGE 25			NOT ON; CHANGE R450, R444 TO 0_0402, ADD R522, R523 0_0402
PAGE 13	PIR5	EMI REQUEST TO PULL HIGH ON MK1709	ADD R385 0_0402, RESERVE R405, C585, C584, Y4; ADD 20K_0402 R525, R528 33K_0402 R526, R527; ADD R413 0_0402, R524 10K_0402, Q75 PDTA114EK
PAGE 15	PIR7	DECREASE THE NOISE ON VDDRH	ADD A .1UF_0402 CAP C719
PAGE 23	PIR8	REMOVE LAN CHASIS GROUND PER EMI'S REQUEST	DEL C243
PAGE 27	PIR10	MOVE SPKR CAPS TO AUDIO BOARD FOR COST DOWN	C692, C711 NOT ON, ADD 0_0805 R531, R532
PAGE 26	PIR11	FOR AUDIO NOISE, ISOLATE LEFT_EQ , GET_EQ , CHANGE C237'S GND TO AGND	RESERVE R529, R530
PAGE 33	PIR12	+3V, +2.5V RISES AS AC_IN, USE 2N7002 AS INVERTER INSTEAD OF 7414	ADD Q75, R532
PAGE 27	PIR13	COST DOWN, USE 74AHC125 TO REPLACED 7SH32	ADD U57, DEL U56, U50
PAGE 25	PIR14	RESERVE A JUMPER FOR AGND TO DGND	
PAGE 27	PIR15	DECREASE EARPHONE'S VOLUME	ADD R541, 542, 543, 544
PAGE 28	PIR16	Add bead for CD ROM analog grounding option	Del C237 , add L50 , change bead connection from Analog to Digital ground
PAGE 29	PIR17	Add capacitor to filter out noise on AVBATT_TEMP to prevent shut_down bug	Add C736 1uF capacitor
PAGE 5	PIR18	EMI team agree to delete all EMI clip Still reserve four clip for backup	Del EMI clip PAD2,4,6,8
PAGE 36	PIR19	Add JAE SD/MMC socket as 2nd source	Add JP29
PAGE 36	PIR20	1.Chang R121 from 499 1% 0402 Resistor to 33K 5% 0402 resistor 2.Add R568 to prevent SDLED signal directly short with Ground while write protect tag enabled.	Change R121 Add R568 3.3K , 5% , 0402
PAGE 13	PIR21	Some additional RC on SPECTRUM IC was requested by EMI to reduce interference .	Add R547 -> 10 Ohm , R546 -> 10 Ohm , R555 -> 10 Ohm , C720 -> 22p , C721 -> 22p

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Item	Reason for change	PG#	Modify List	B.Ver#
1	For thermal teem request that thermal setting point changed from 96 to 90 degree C.	37	PR20 changed from 1.74k into 2k_1%_0603(SD014200101) PR24 changed from 21k into 19.1k_1%_0603(SD014191209)	B test BOM
2	+2.5VALWP is always power plane	41	PQ41,PQ42,PR128 should not be POP	B test BOM
3	For cost down issue	37	PC28,PC29 should not be POP PC155 should be POP (CB5600NM000)	B test BOM
4	Prevent PU4 leakage lock pre-charge circuit	38	PU4 pin14 changed from PACIN into ACON	B gerber
5				
6				

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