ZZZ1
DAZ

ZZZ2
12.1W_PCB_LA5191P
Part Number = DA80000EF10

ZZZ3
12.1W_PCB_LS5191P
Part Number = DA60000C410

ZZZ4
12.1W_PCB_LS5192P
Part Number = DA40000K110

ZZZ5
12.1W_PCB_LS5193P
Part Number = DA40000K010

ZZZ6
12.1W_PCB_LS5194P
Part Number = DA20000GH10

KIUE0

Schematics Document

Mobile Penryn PGA with Intel Cantiga_GM45+ICH9-M core logic

REV:1.0

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

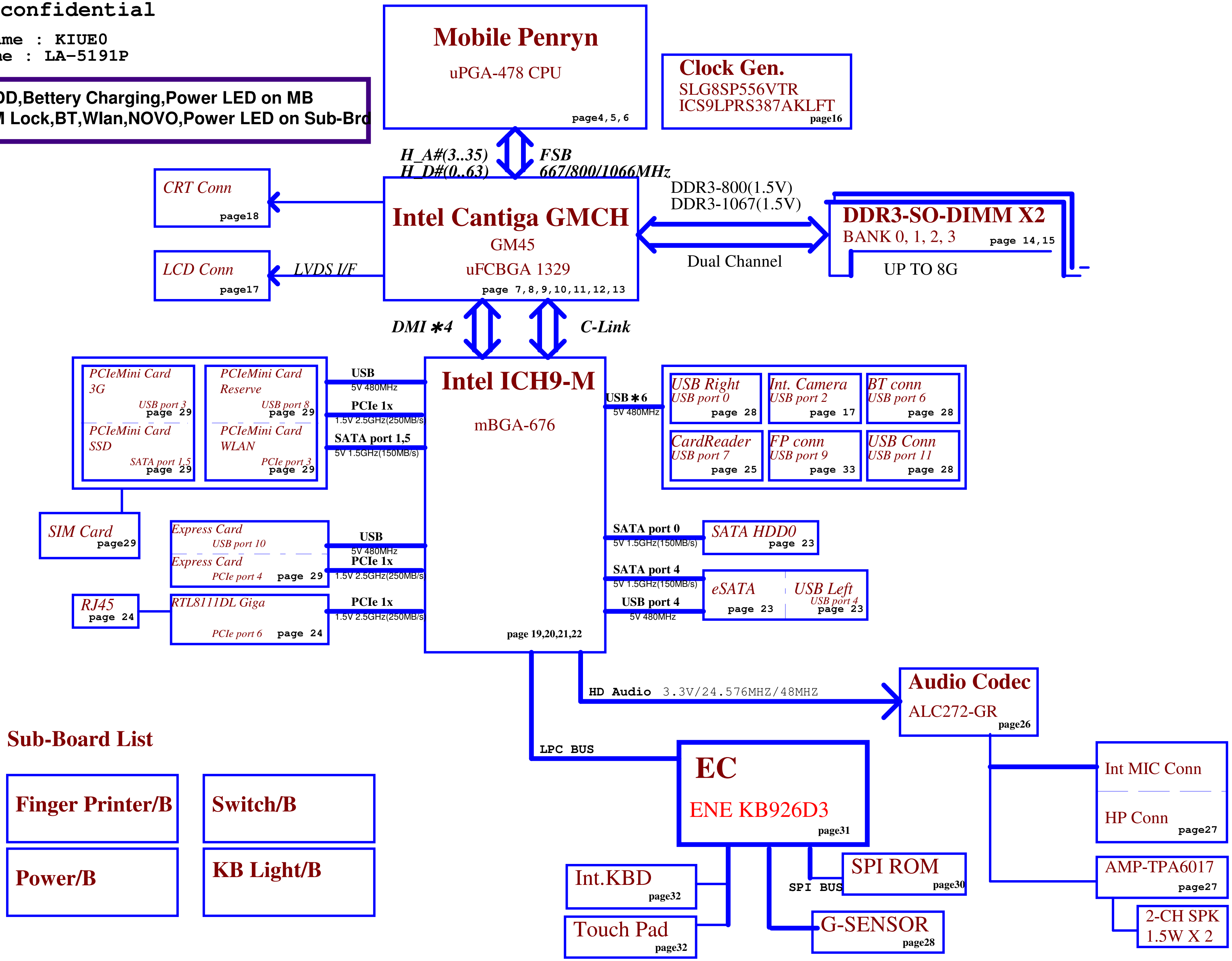
Compal Electronics,Ltd.

Title	Cover Sheet	
Size: Custom	Document Number: KIUE0_LA-5191P	Rev: 1.0
Date: Thursday, June 25, 2009	Sheet 1 of 43	

Compal confidential

Model Name : KIUE0
File Name : LA-5191P

TP Lock,HDD,Bettery Charging,Power LED on MB
CAPS ,NUM Lock,BT,Wlan,NOVO,Power LED on Sub-Brd



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2008/03/24	Deciphered Date	2008/04/	Title: MB Block Diagram
				Size: Custom; Document Number: KIUE0_LA-5191P; Rev 1.0
				Date: Wednesday, June 24, 2009; Sheet 2 of 43

Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
VL	3.3V always on power rail	ON	ON	ON	ON
~~+3V_SB~~	~~3.3V power rail for LAN~~	~~ON~~	~~ON~~	~~OFF~~	~~OFF~~
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
~~+3V_WLAN~~	~~3.3V power rail for LAN~~	~~ON~~	~~ON~~	~~OFF~~	~~OFF~~
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
~~+5VL~~	~~5V always on power rail~~	~~ON~~	~~ON~~	~~ON~~	~~ON~~
~~+5V_SB~~	~~5V power rail for SB~~	~~ON~~	~~ON~~	~~OFF~~	~~OFF~~
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
~~+GPU_CORE~~	~~Core voltage for VGA chip~~	~~ON~~	~~ON~~	~~OFF~~	~~OFF~~
+1.8VS	1.8V power rail for NB	ON	OFF	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	*HIGH*	*HIGH*	*HIGH*	*HIGH*		
S1(Power On Suspend)	*LOW*	*HIGH*	*HIGH*	*HIGH*		
S3 (Suspend to RAM)	*LOW*	*LOW*	*HIGH*	*HIGH*		
S4 (Suspend to Disk)	*LOW*	*LOW*	*LOW*	*HIGH*		
S5 (Soft OFF)	*LOW*	*LOW*	*LOW*	*LOW*		
G3	*LOW*	*LOW*	*LOW*	*LOW*		

BTO Option Table

Function	CRT	LAN	Finger printer	BLUE TOOTH	3G SIM slot	Mini card
description	(Q)	(C)	(F)	(B)	(3)	(D2)
explain						
BTO						

External PCI Devices

EC SM Bus1 address

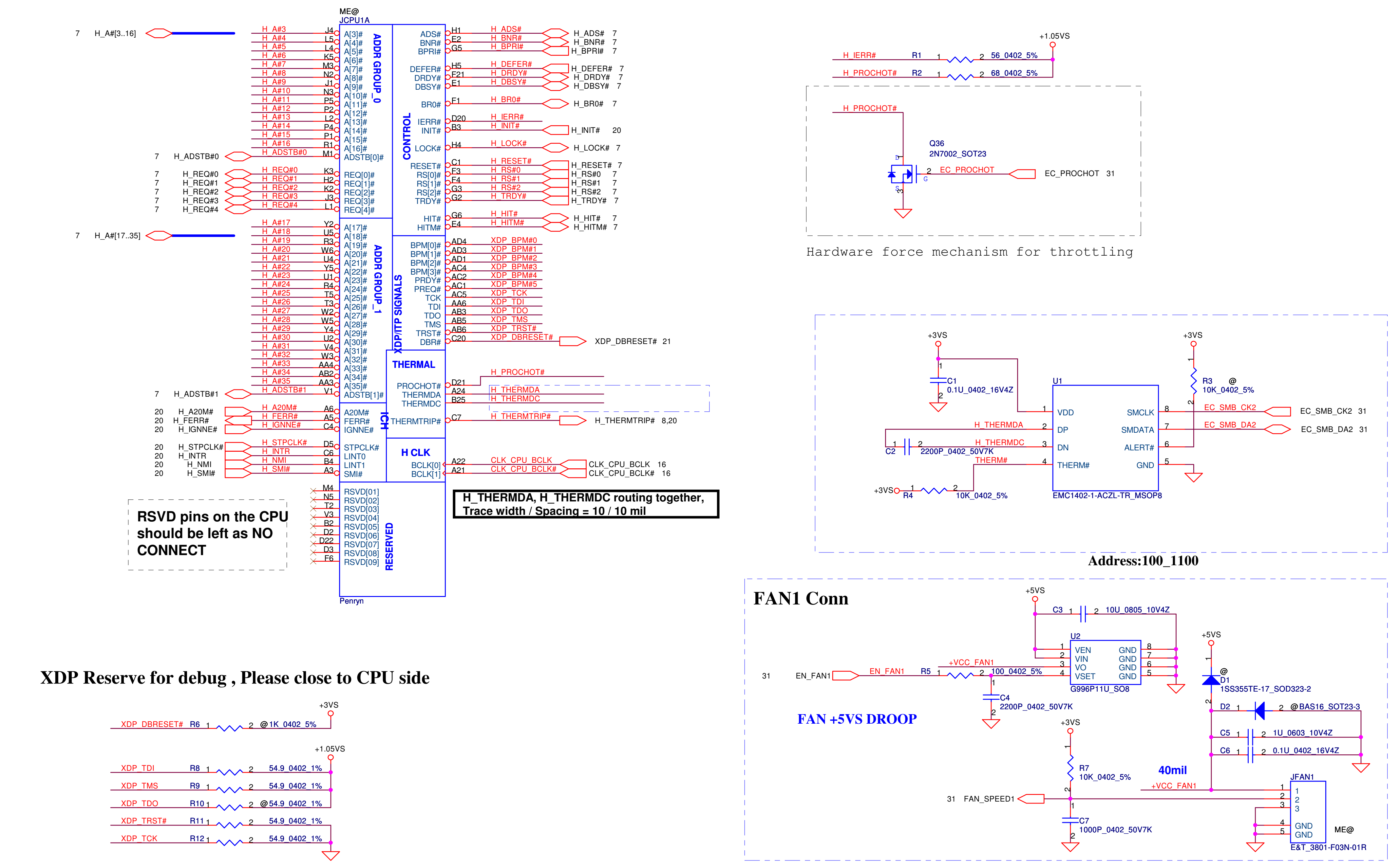
Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	Smart Battery	

EC SM Bus2 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	CPU THM Sen SMSC SMC1402	

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	
+3VS	DDR DIMM0	
+3VS	DDR DIMM1	
+3VS	Express	



Security Classification	Compal Secret Data			Compal Electronics,Ltd.
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title: Penryn(1/3)
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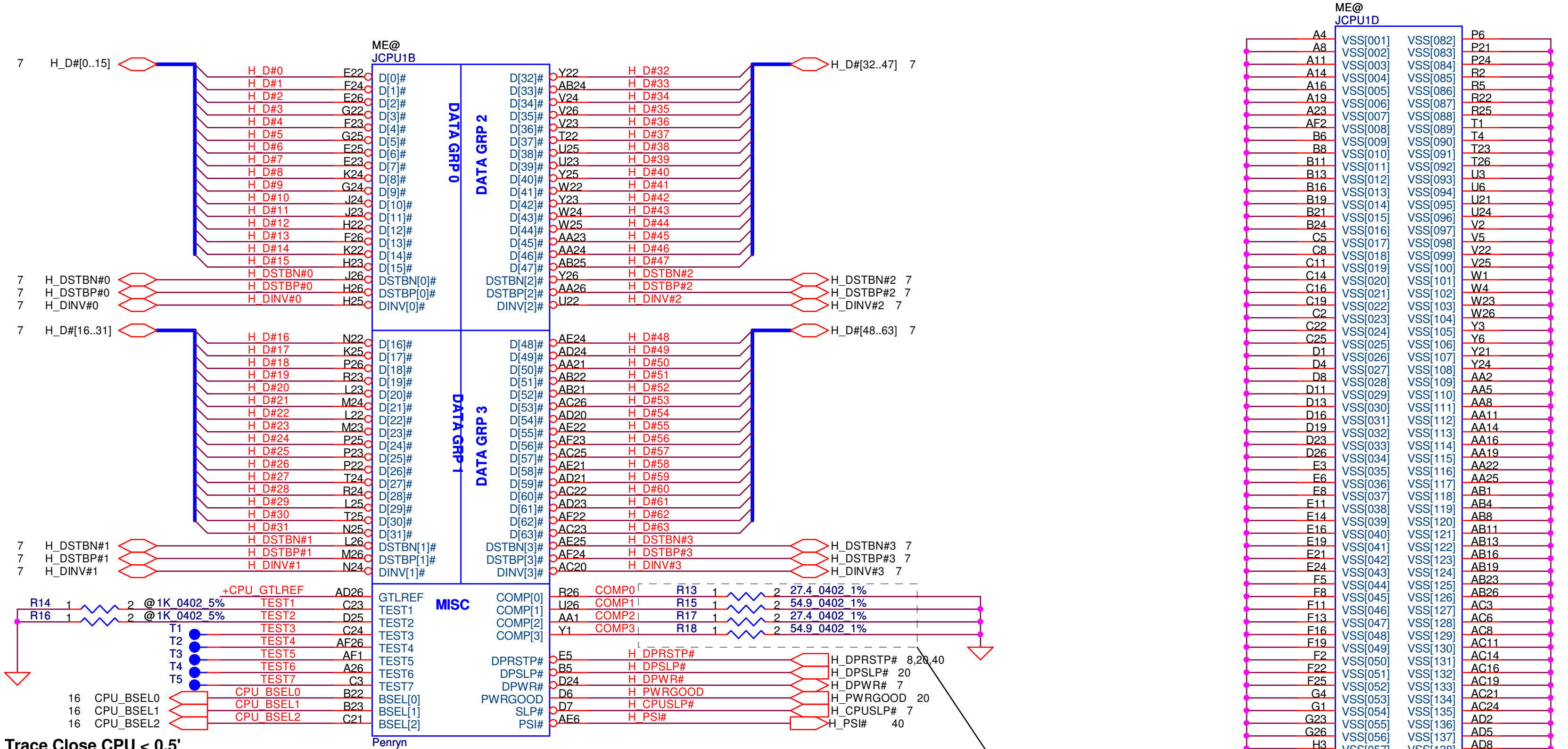
				Date: Wednesday, June 24, 2009; Sheet 4 of 43



Trace Close CPU < 0.5'

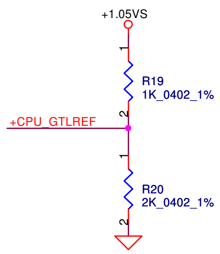
Width=4 mil ,
Spacing: 15mil
(55Ohm)

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

Layout note: Z0=55 ohm
0.5" max for GTLREF.



Close to CPU pin AD26 within 500mils.

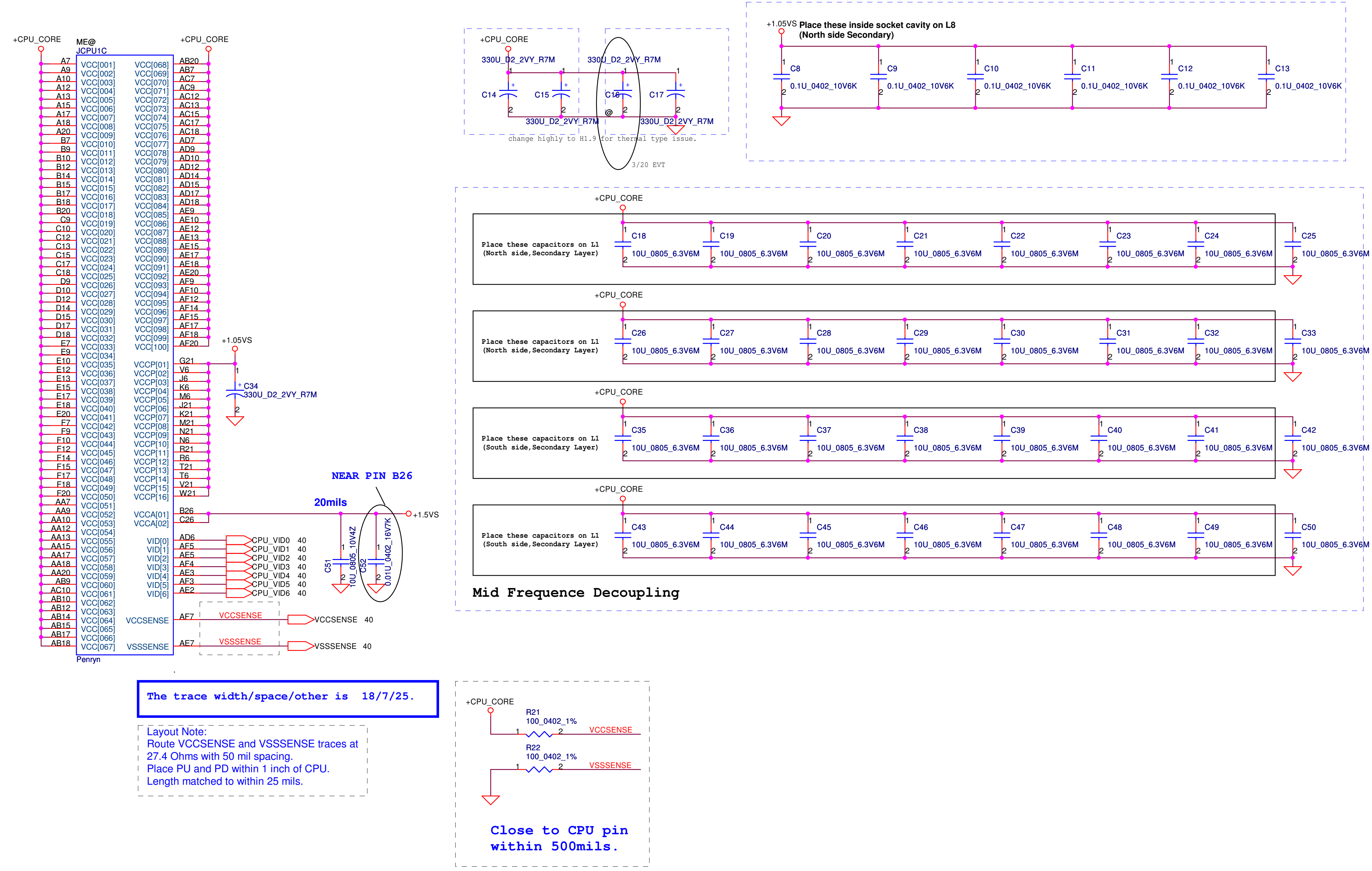
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Penryn (2/3)

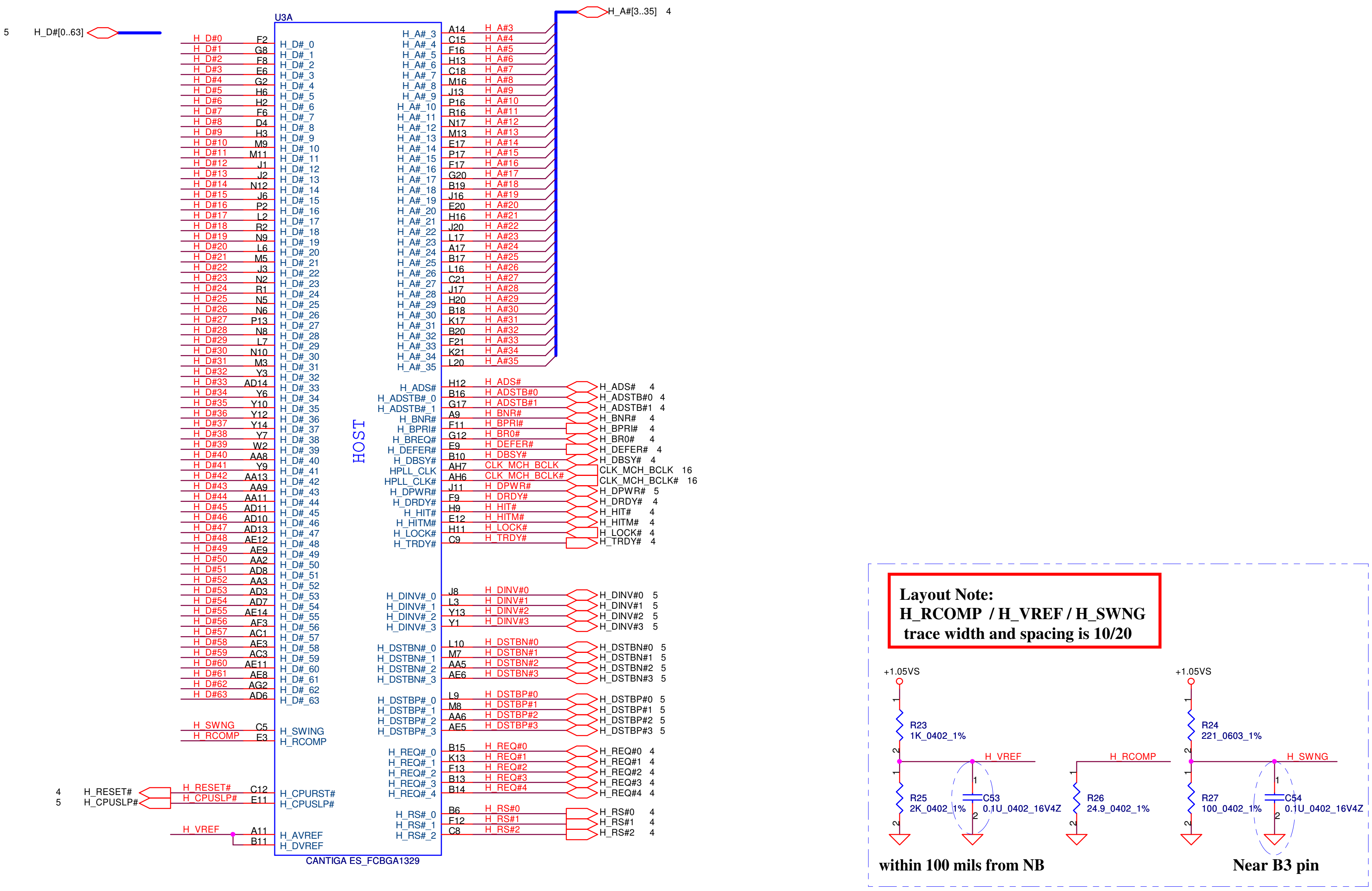
Size: B | Document Number: KIUE0_LA-5191P | Rev 1.0



The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title: Penryn (3/3)
				Size: Custom; Document Number: KIUE0_LA-5191P; Rev: 1.0
				Date: Wednesday, June 24, 2009; Sheet 6 of 43



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title: Cantiga GMCH(1/6)-GTL
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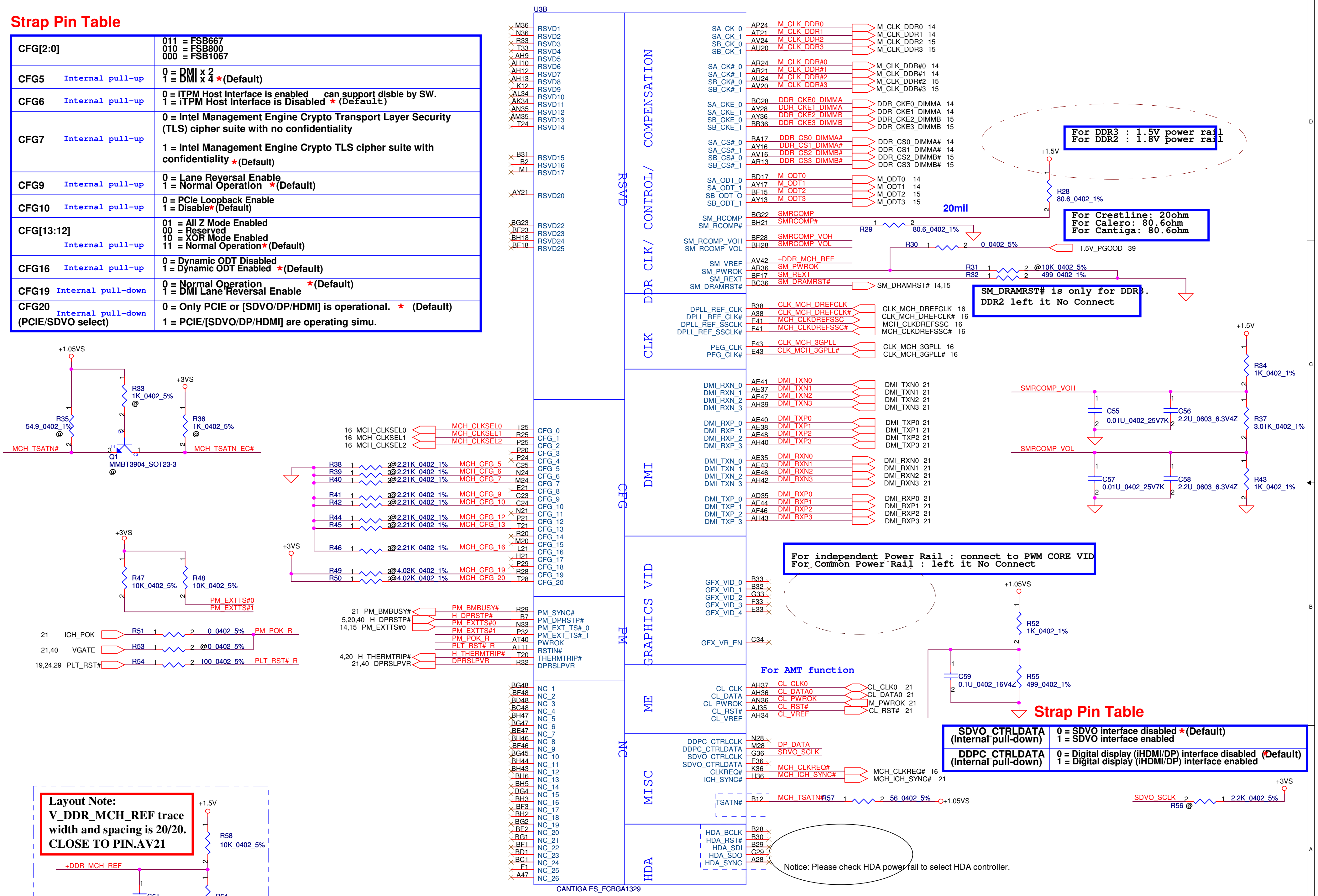
				Date: Wednesday, June 24, 2009; Sheet 7 of 43

Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 ★(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled ★ (Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality ★(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation ★(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable★(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation★(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled ★(Default)
CFG19	Internal pull-down	0 = Normal Operation ★(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. ★ (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.



For DDR3 : 1.5V power rail
For DDR2 : 1.8V power rail

For Crestline: 20ohm
For Calero: 80.6ohm
For Cantiga: 80.6ohm

SM_DRAMRST# is only for DDR3.
DDR2 left it No Connect

For independent Power Rail : connect to PWM CORE VID
For Common Power Rail : left it No Connect

For AMT function

Notice: Please check HDA power rail to select HDA controller.

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.
CLOSE TO PIN.AV21

Strap Pin Table

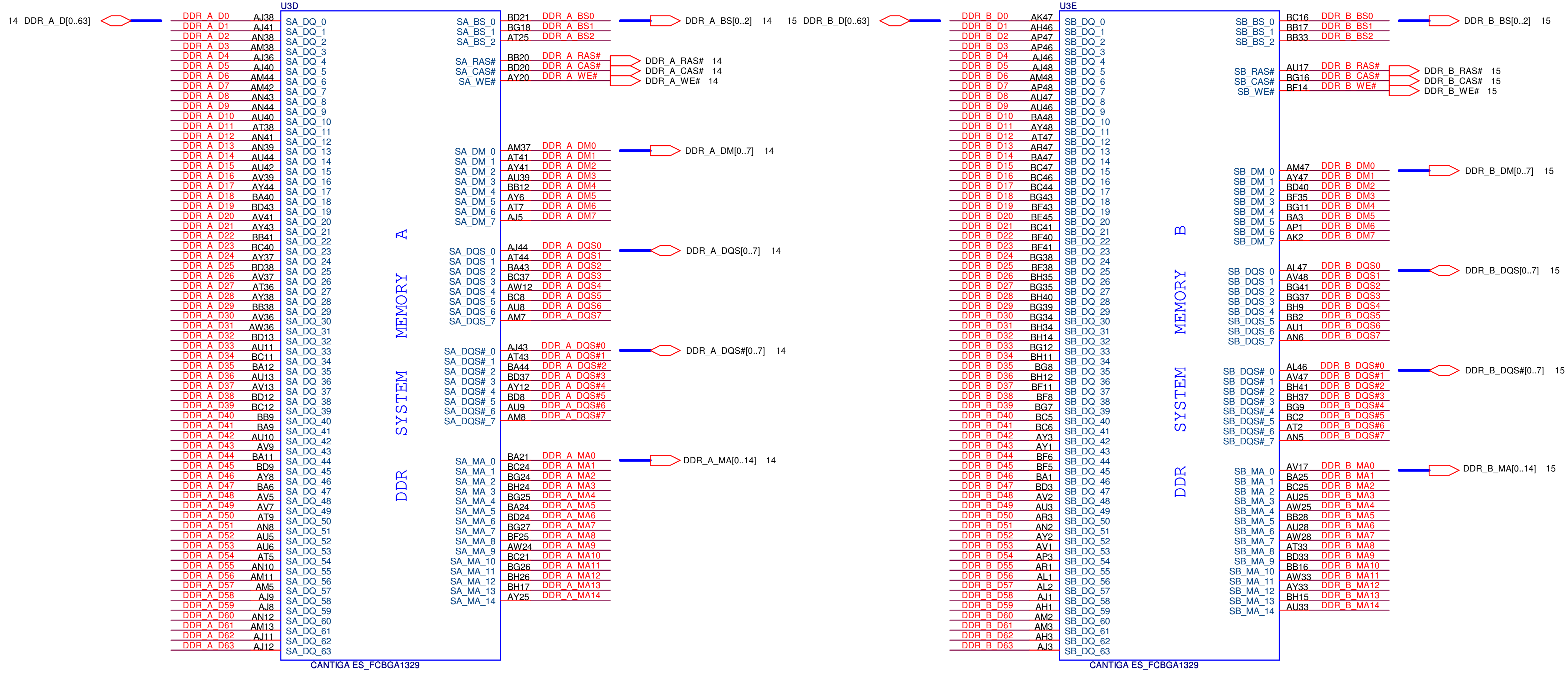
SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled ★(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled ★(Default) 1 = Digital display (iHDMI/DP) interface enabled

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: *Cantiga(2/7)-DMI/DDR/STRP*

Size: Custom | Document Number: KIUE0_LA-5191P | Rev 1.0



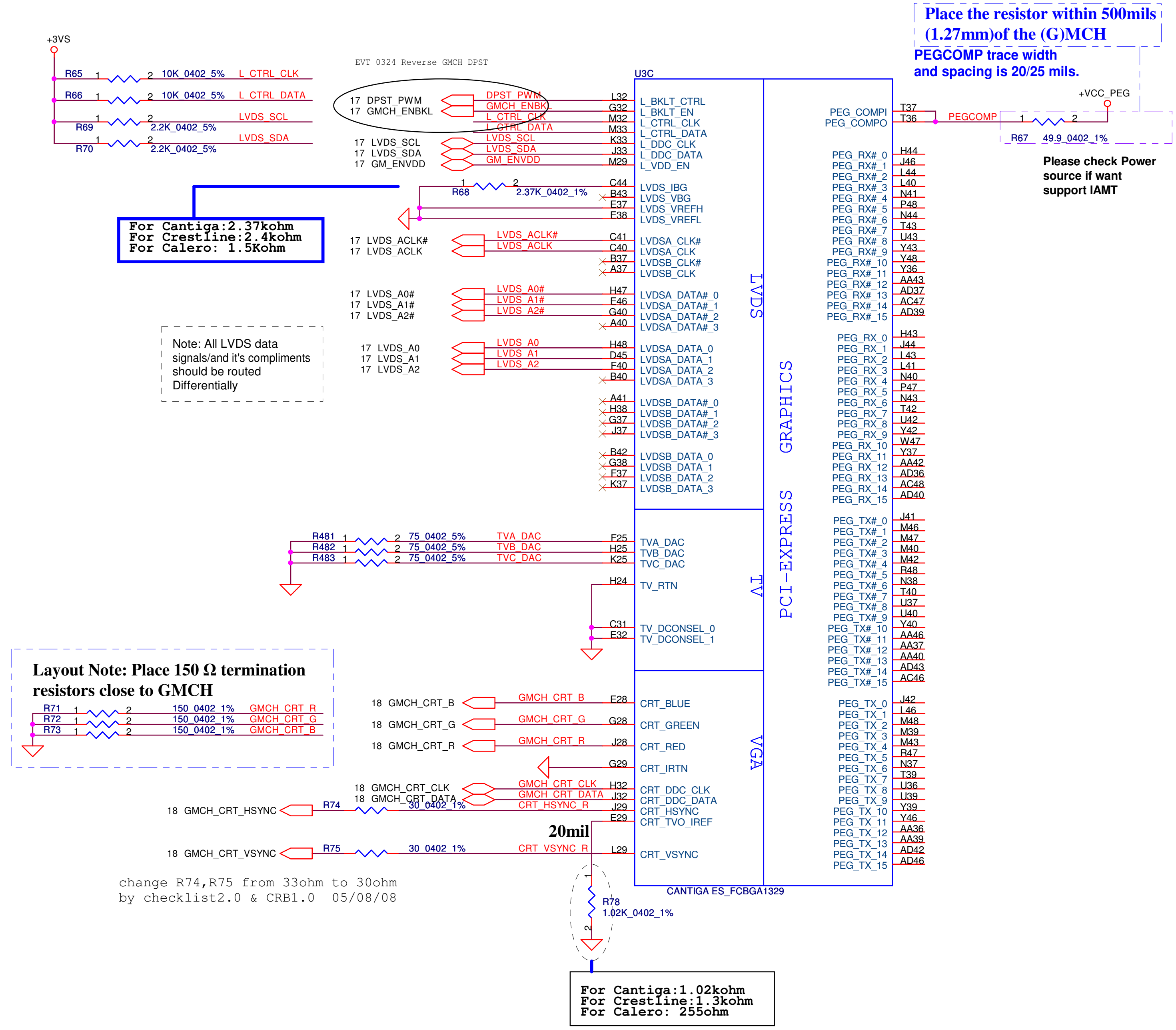
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009



Security Classification	Compal Secret Data			Compal Electronics,Ltd.
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title: Cantiga(3/6)-VGA/LVDS/TV
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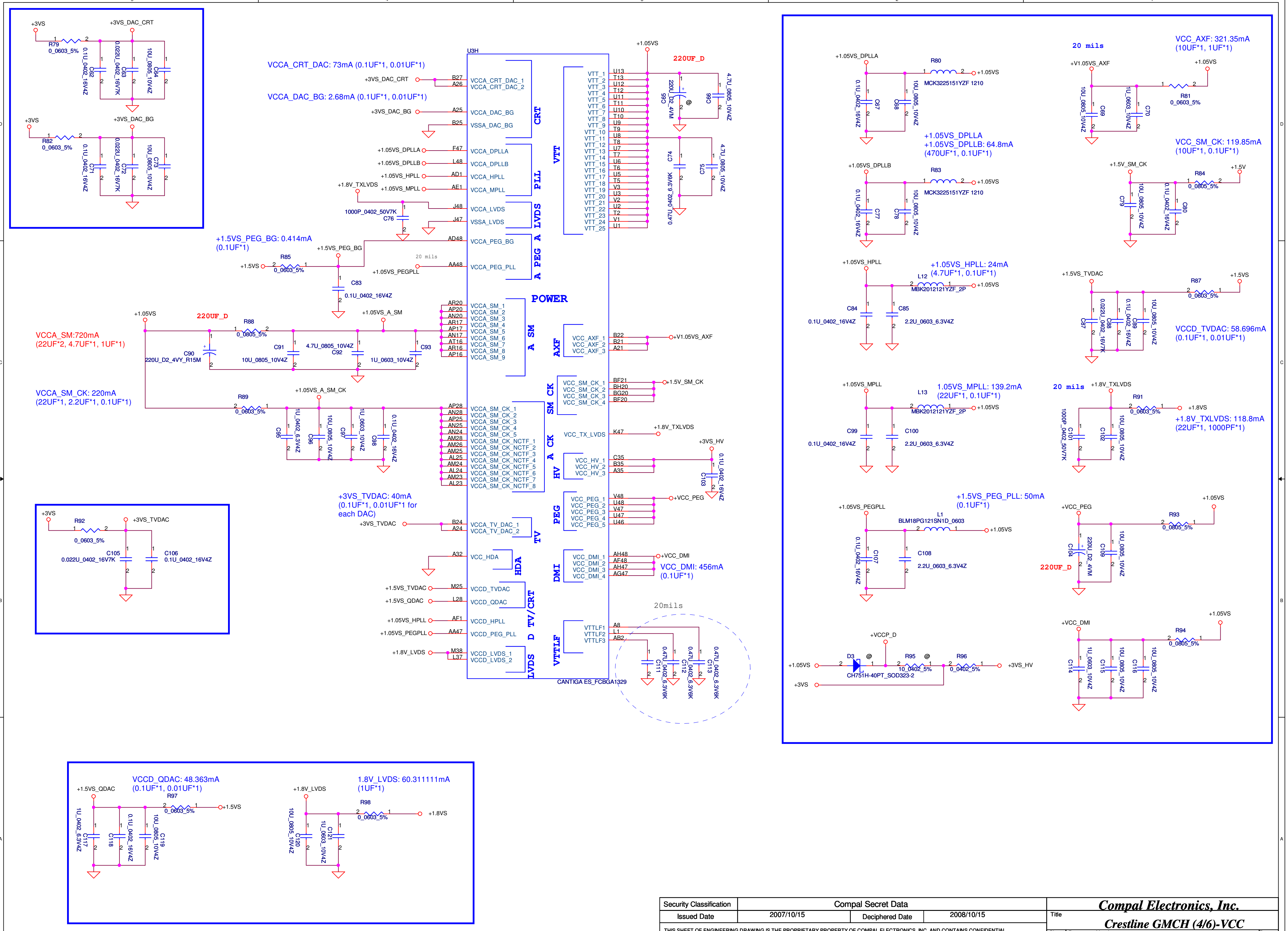
				Date: Wednesday, June 24, 2009; Sheet 10 of 43



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date 2008/10/15	Title: Crestline GMCH (4/6)-VCC
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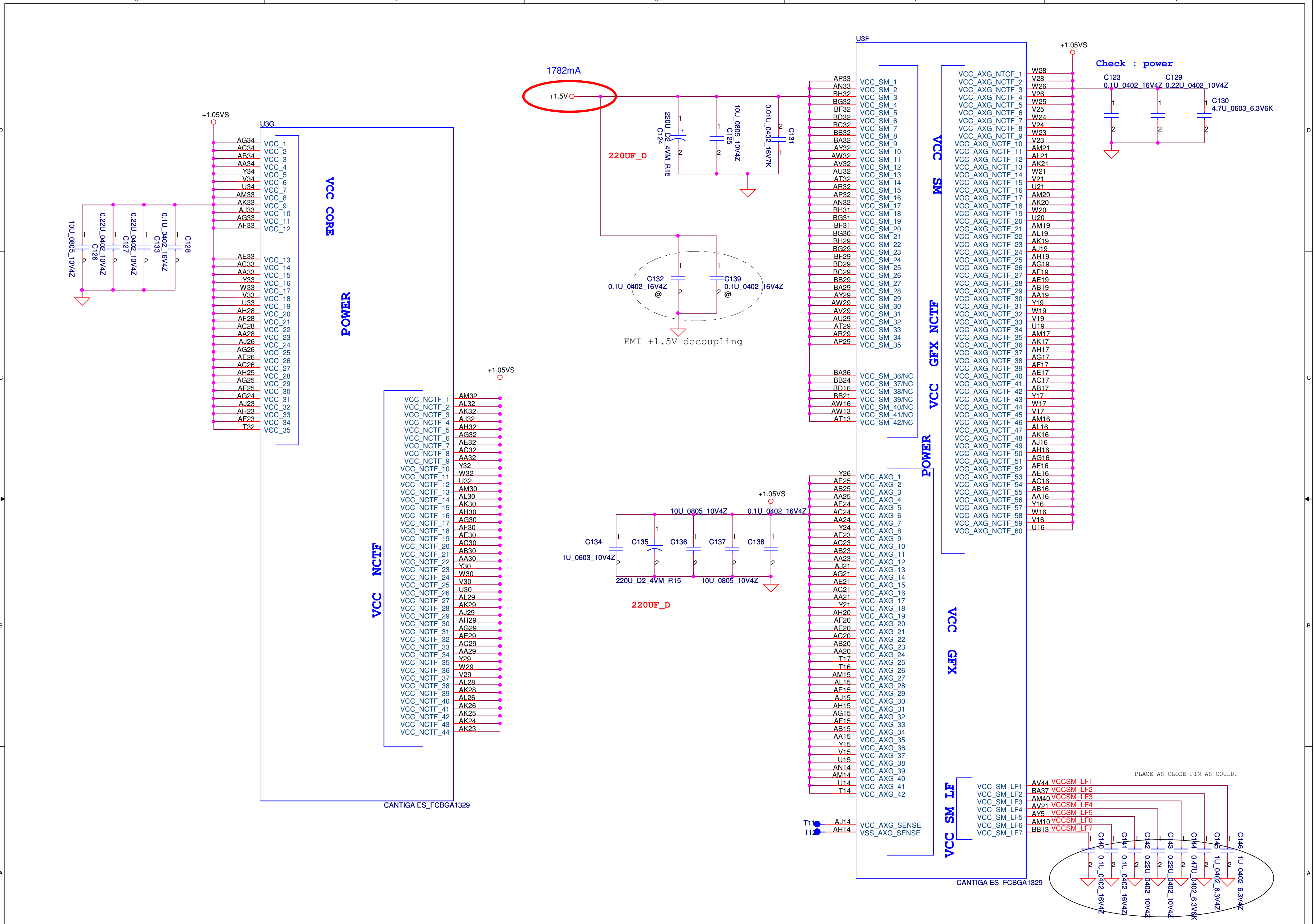
			Date: Wednesday, June 24, 2009; Sheet 11 of 43



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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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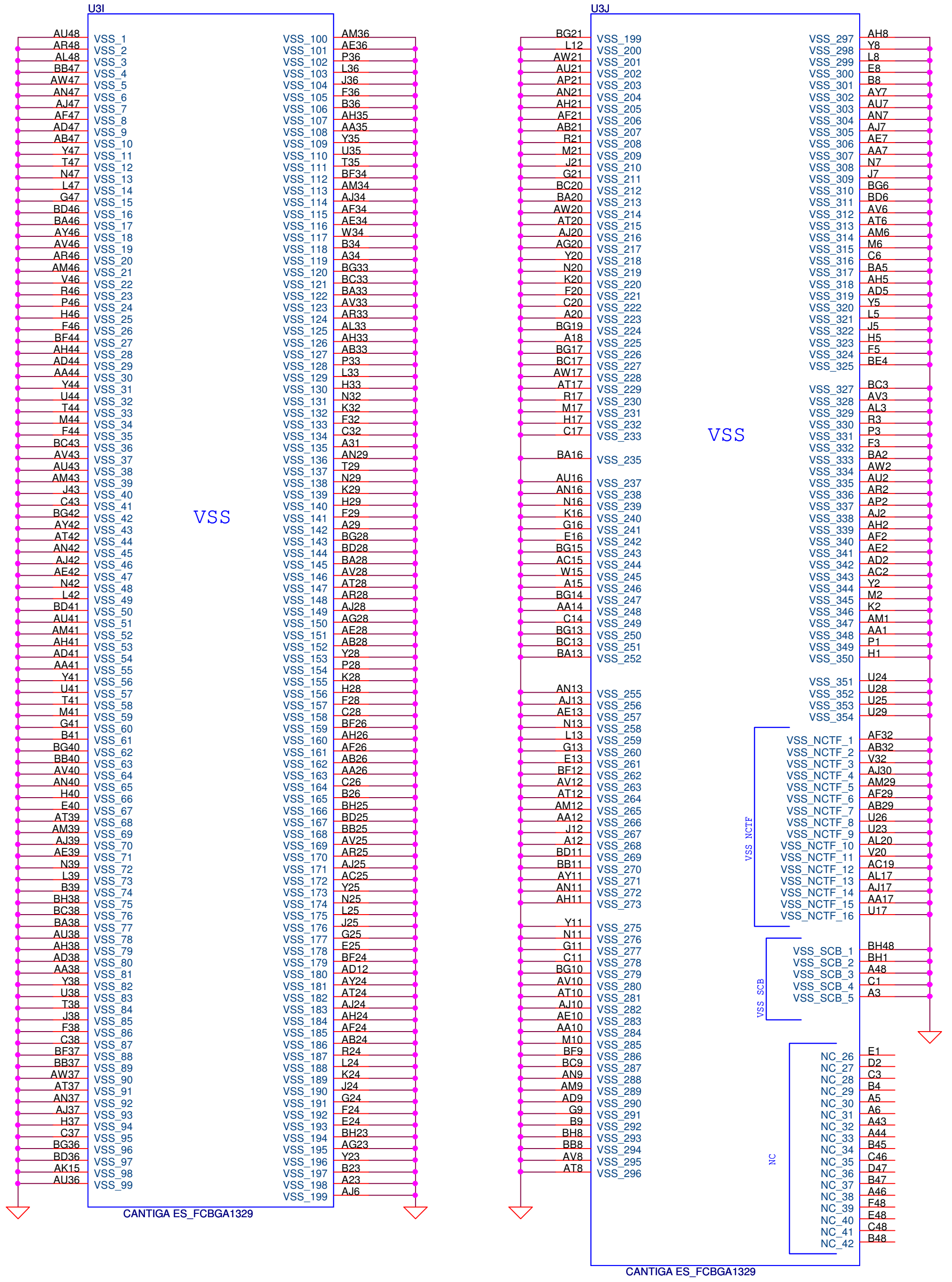
Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 12 of 43



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title: Cantiga GMCH (6/6)-GND
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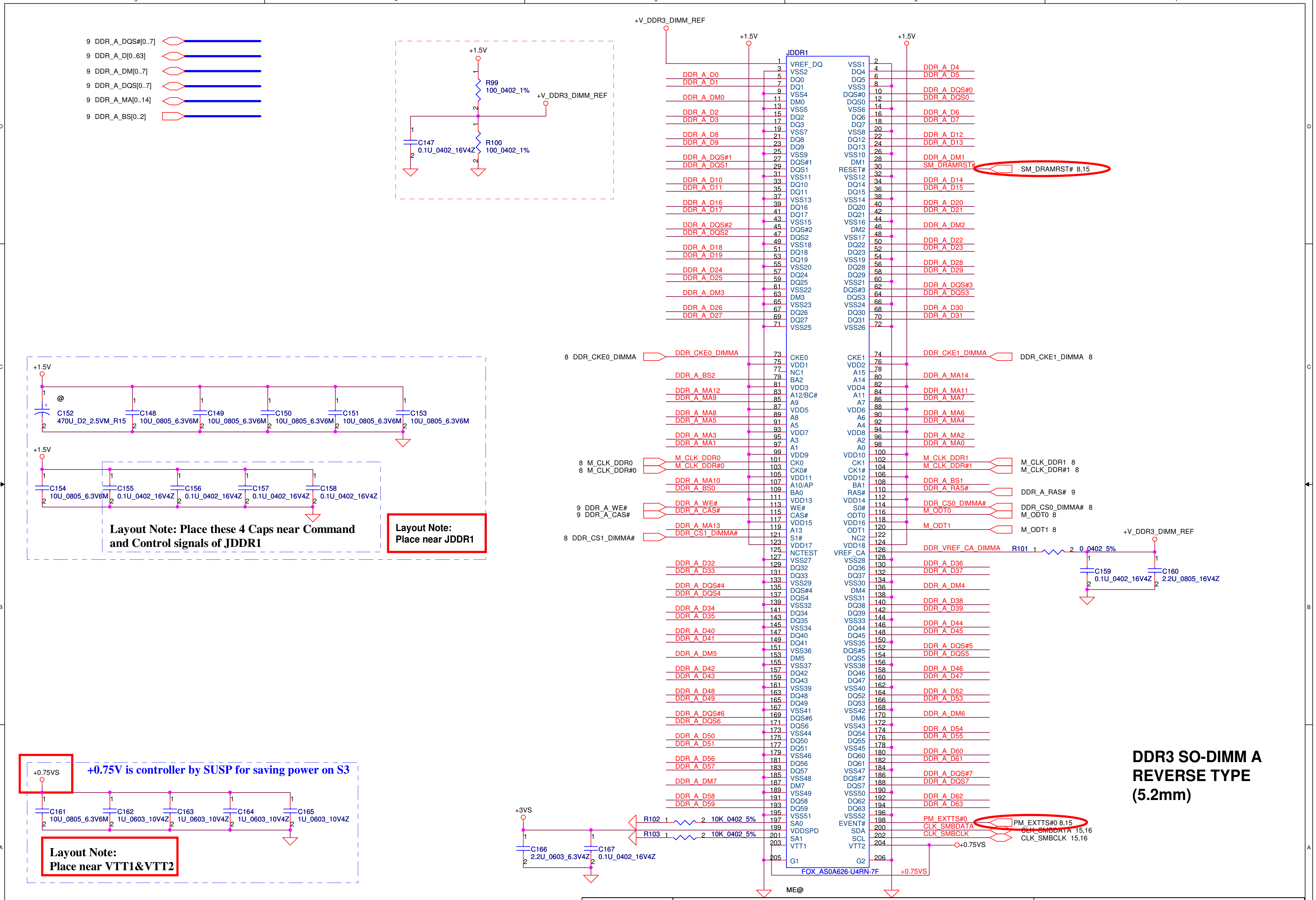
				Date: Wednesday, June 24, 2009; Sheet 13 of 43



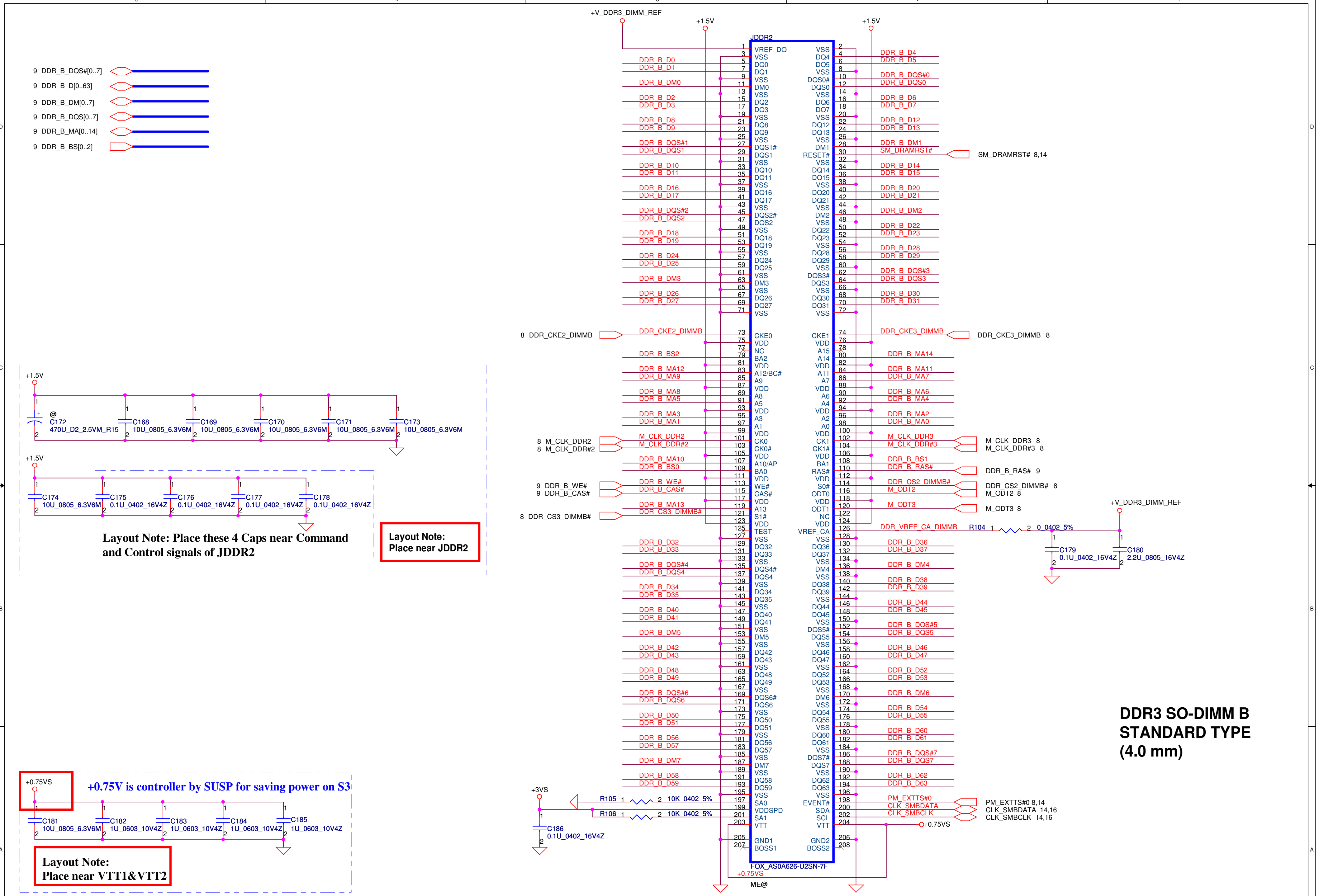
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 14 of 43



Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

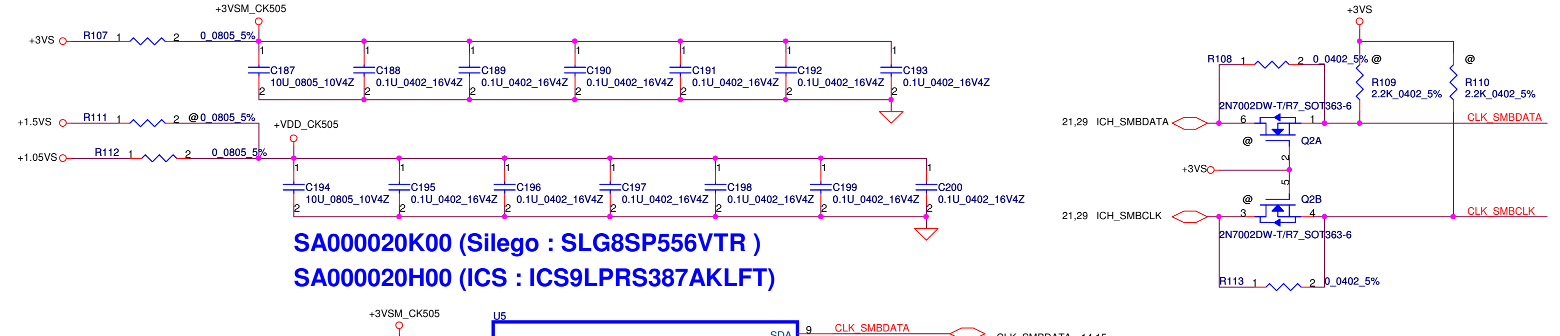
Compal Electronics, Inc.

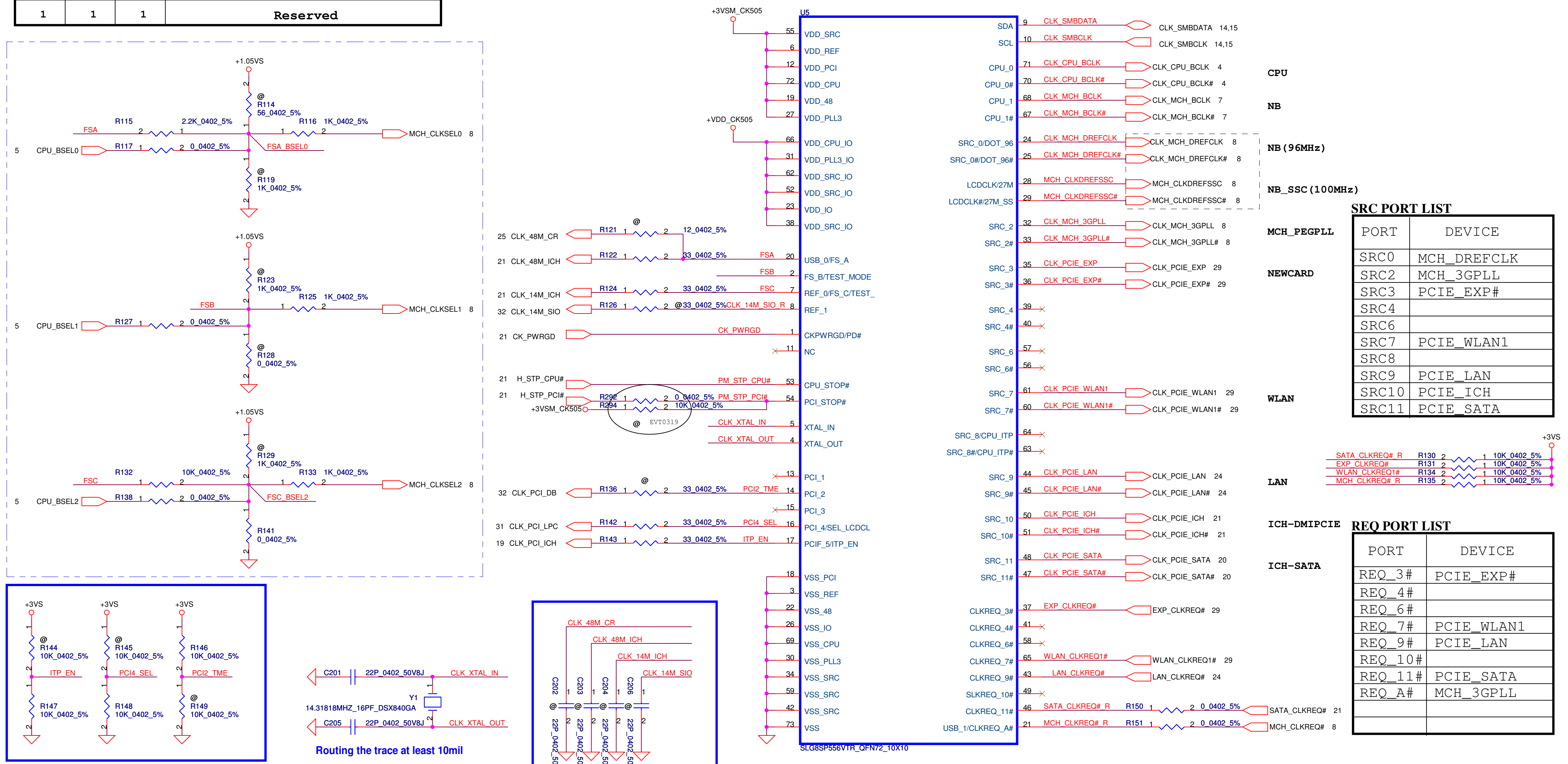
Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: KIUE0_LA-5191P | Rev 1.0

Date: Wednesday, June 24, 2009 |

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					





SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 =SRC8/SRC8#(100MHz); 1 = ITP/ITP#(266MHz)

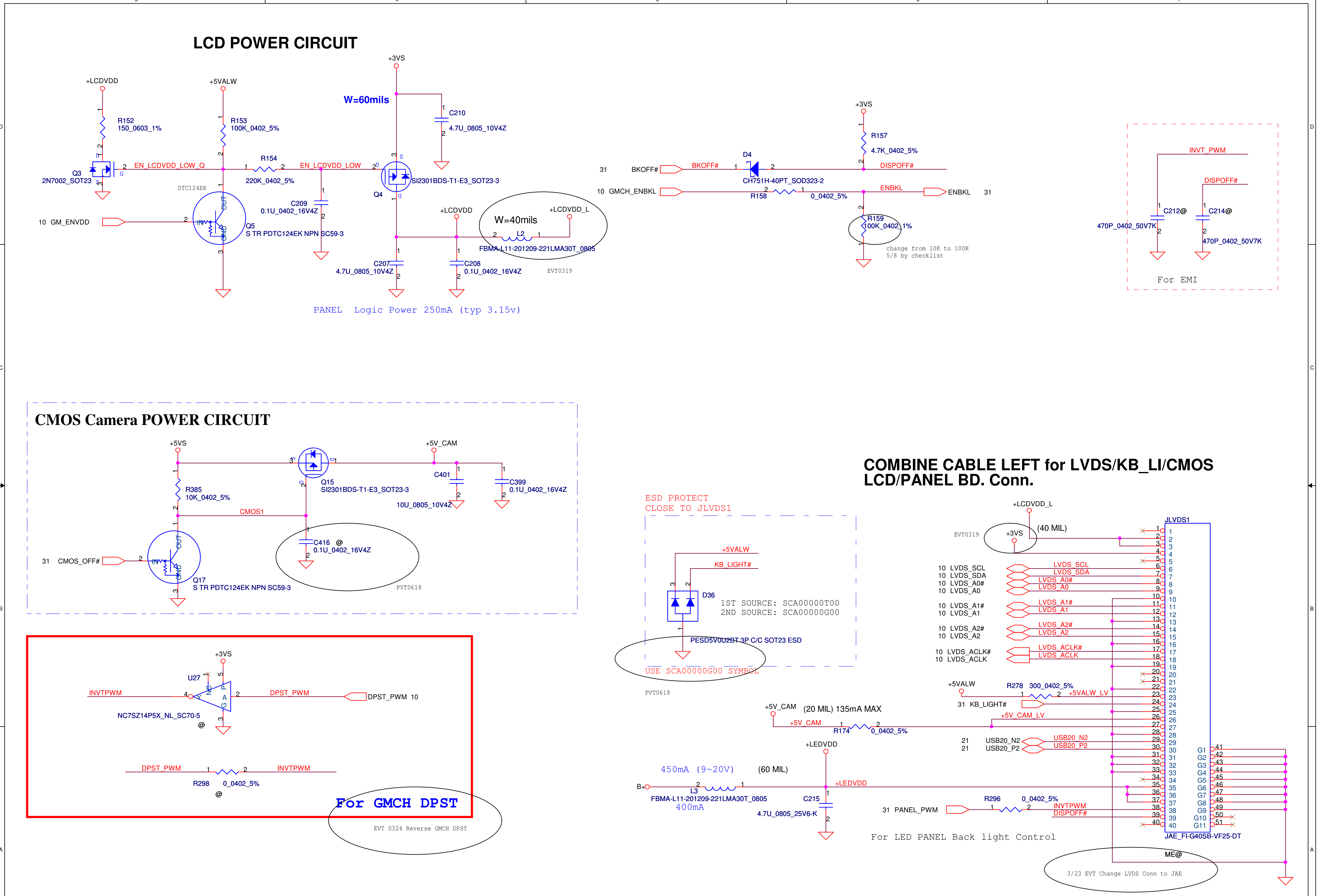
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#(UMA)
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS(DISCRETE)

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Clock Generator CK505**

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

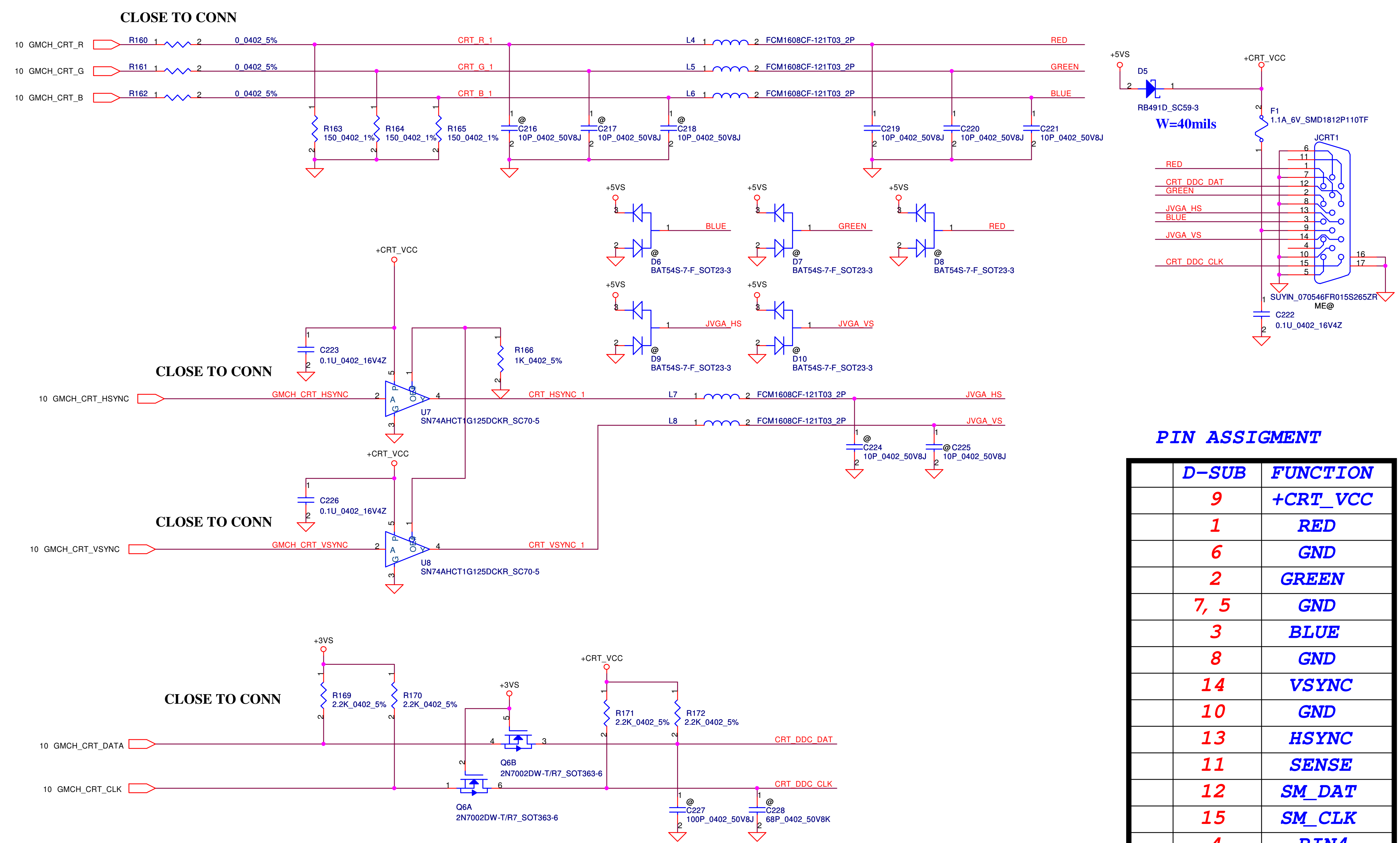
Compal Electronics, Inc.

Title: **LVDS & DVI Connector**

Size B | Document Number: KIUE0_LA-5191P | Rev 1.0

Date: Wednesday, June 24, 2009 | Sheet 17 of 43

CRT Connector

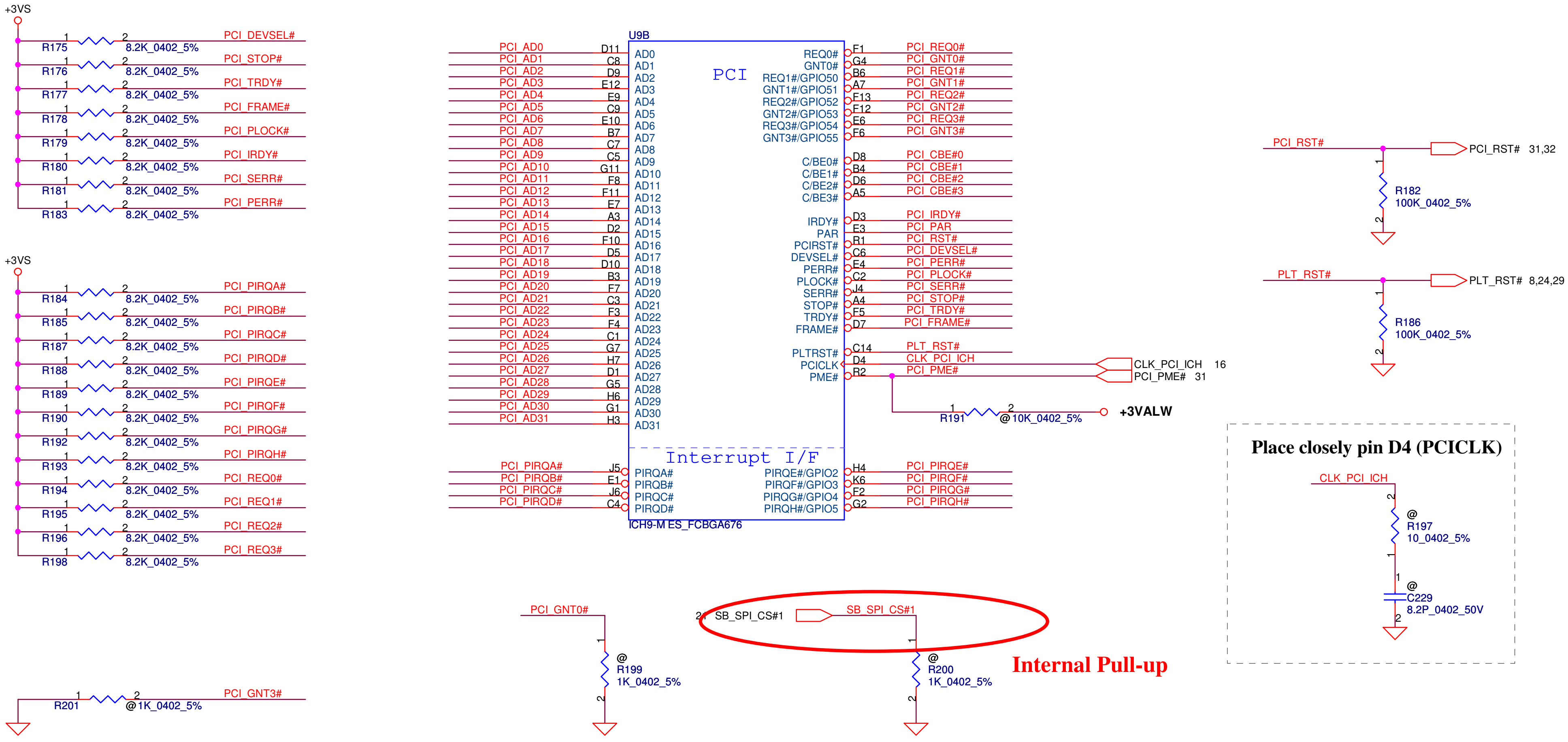


PIN ASSIGMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.
Title: CRT & TV-OUT Connector
Size: Custom | Document Number: KIUE0_LA-5191P | Rev 1.0
Date: Wednesday, June 24, 2009 | Sheet 18 of 43



A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap

PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

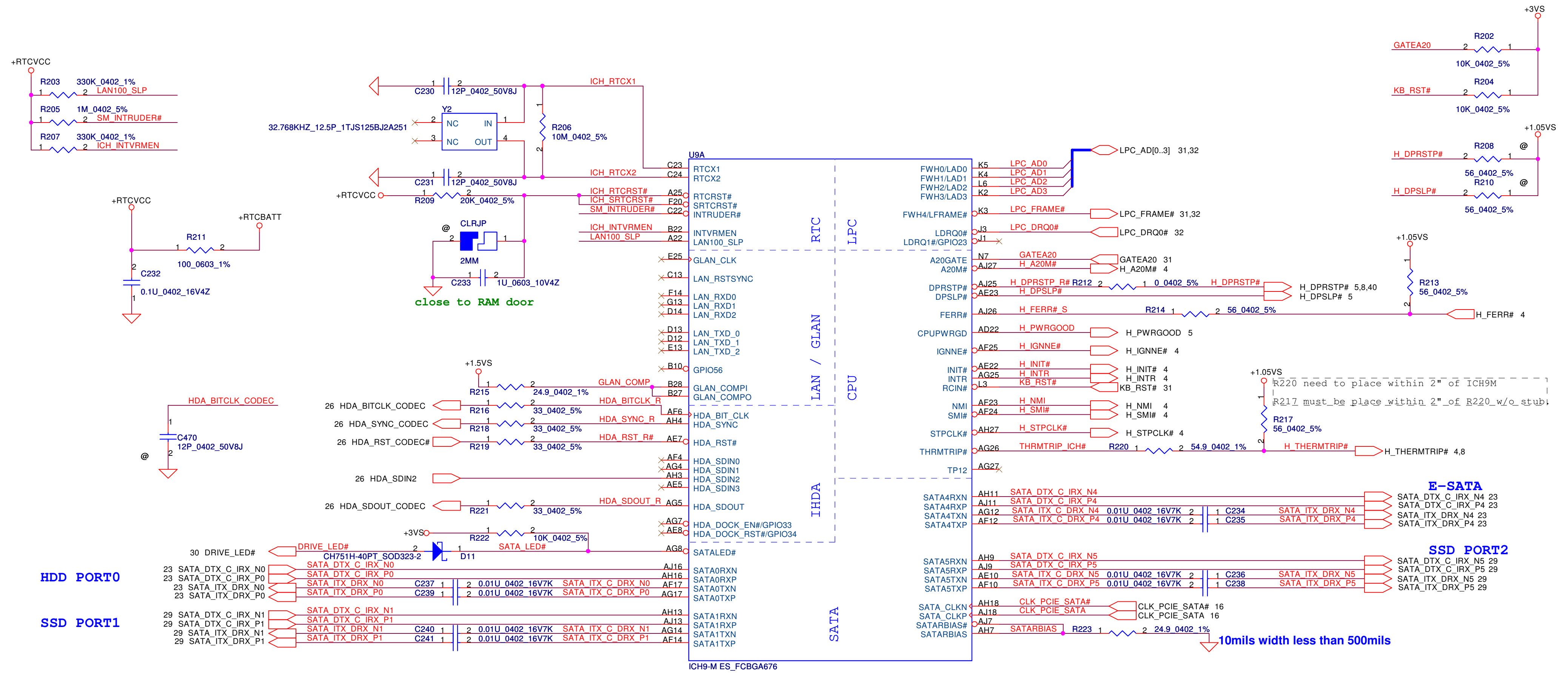
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

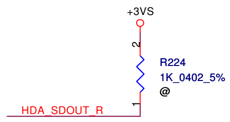
Title: **ICH9M(1/4)-PCI**

Size | Document Number: KIUE0_LA-5191P | Rev 1.0

Date: Wednesday, June 24, 2009 |



Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST

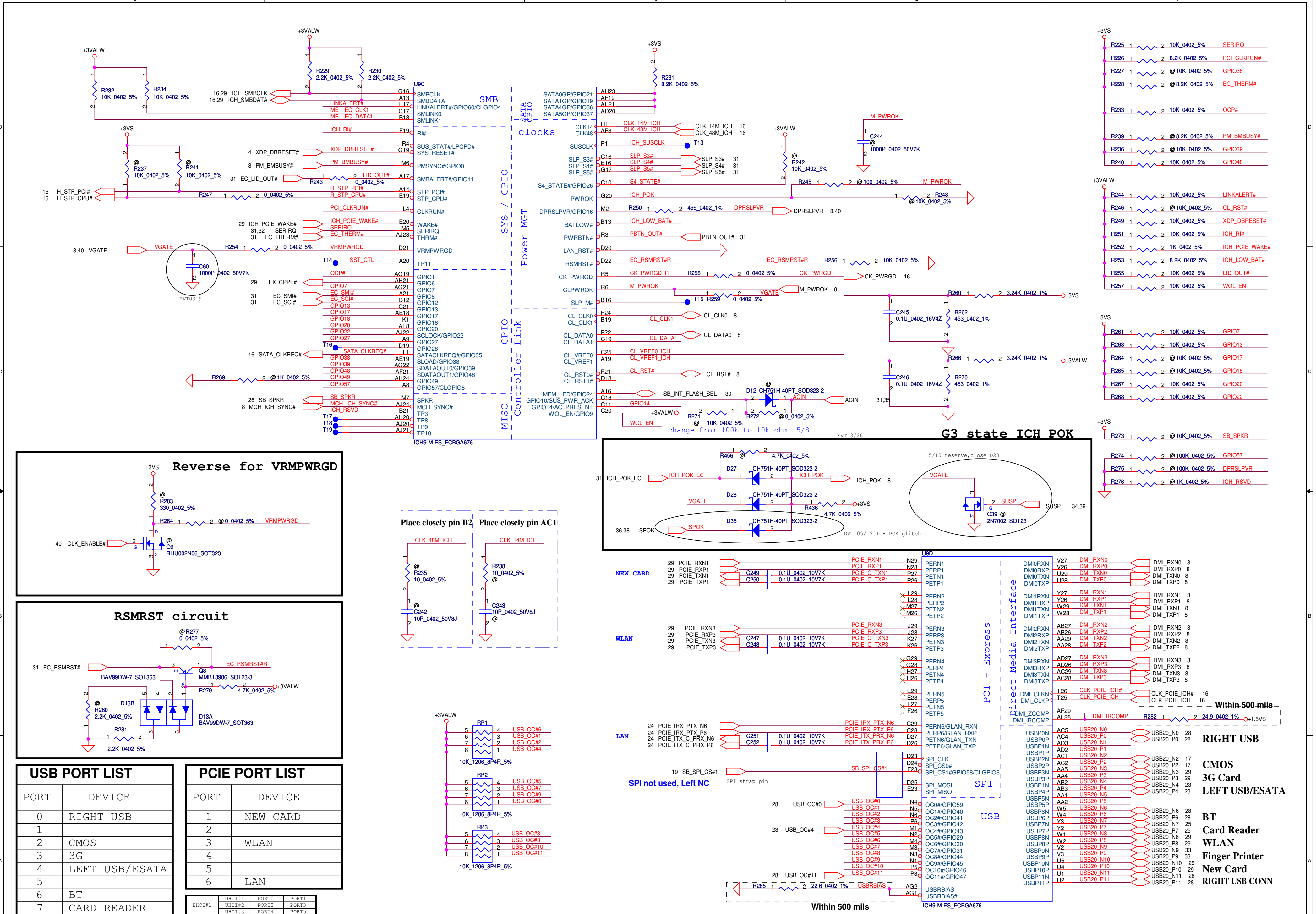
PORT	DEVICE
0	HDD
1	Mini-Card SSD PORT1
4	E-SATA
5	Mini-Card SSD PORT2

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0



USB PORT LIST

PORT	DEVICE
0	RIGHT USB
1	
2	CMOS
3	3G
4	LEFT USB/ESATA
5	
6	BT
7	CARD READER
8	WIRELESS
9	Finger Print
10	NEW CARD
11	RIGHT USB CONN

PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	
3	WLAN
4	
5	
6	LAN

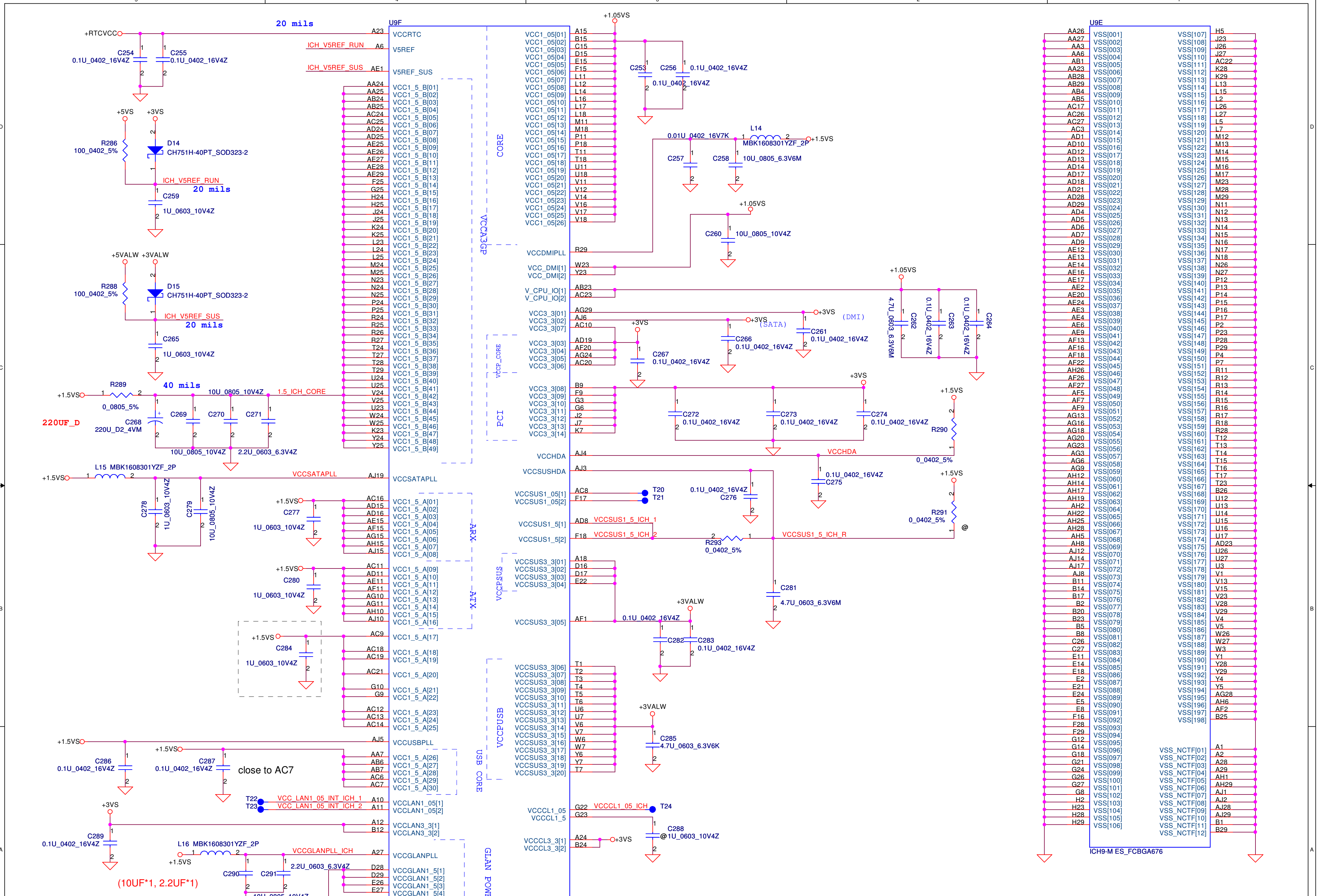
EHCI#1	UHCI#1	PORT0	PORT1
	UHCI#2	PORT2	PORT3
	UHCI#3	PORT4	PORT5
EHCI#2	UHCI#4	PORT6	PORT7
	UHCI#5	PORT8	PORT9
	UHCI#6	PORT10	PORT11

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size: C | Document Number: KIUE0_LA-5191P | Rev: 1.0



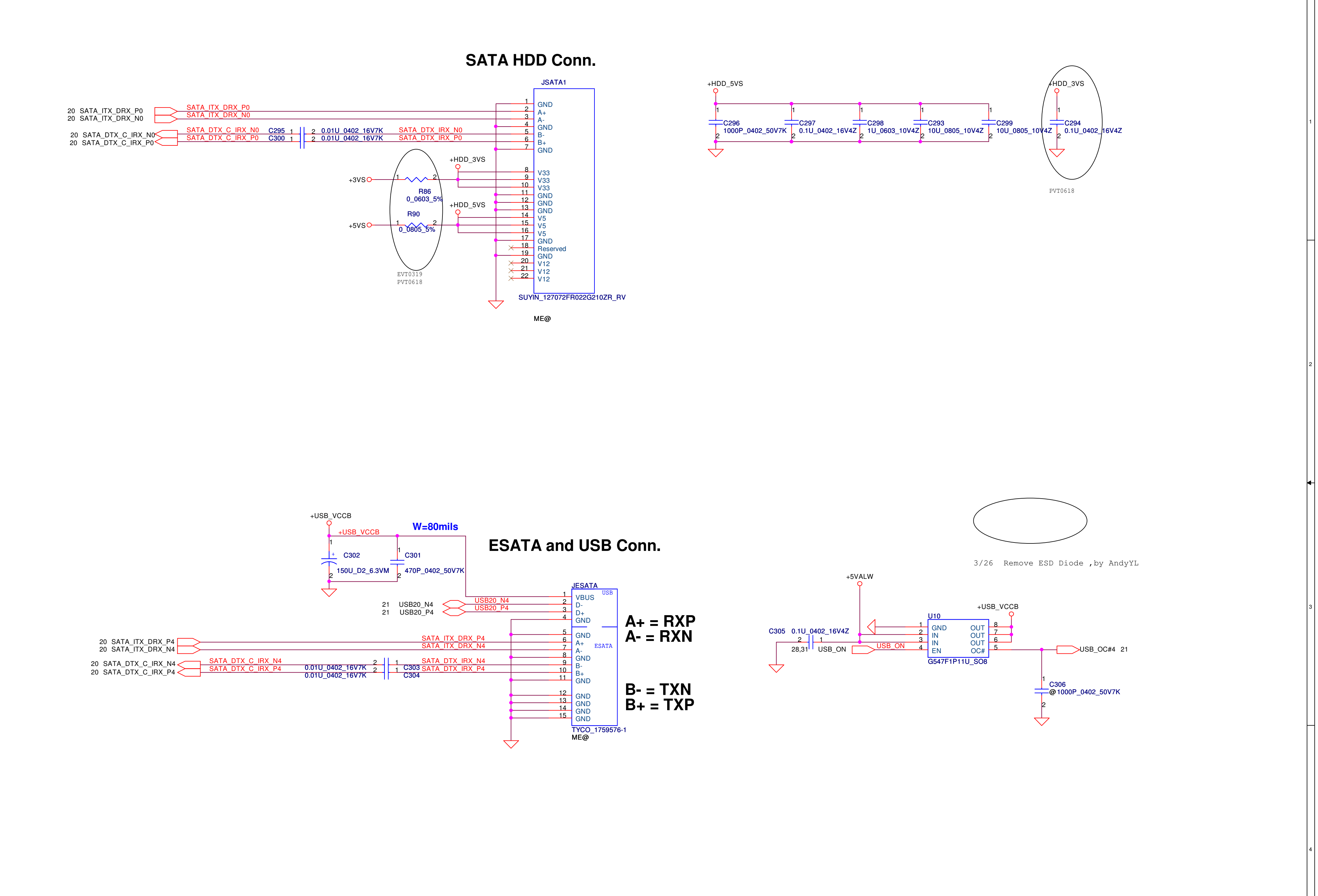
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **ICH9M(4/4)-POWER&GND**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 22 of 43



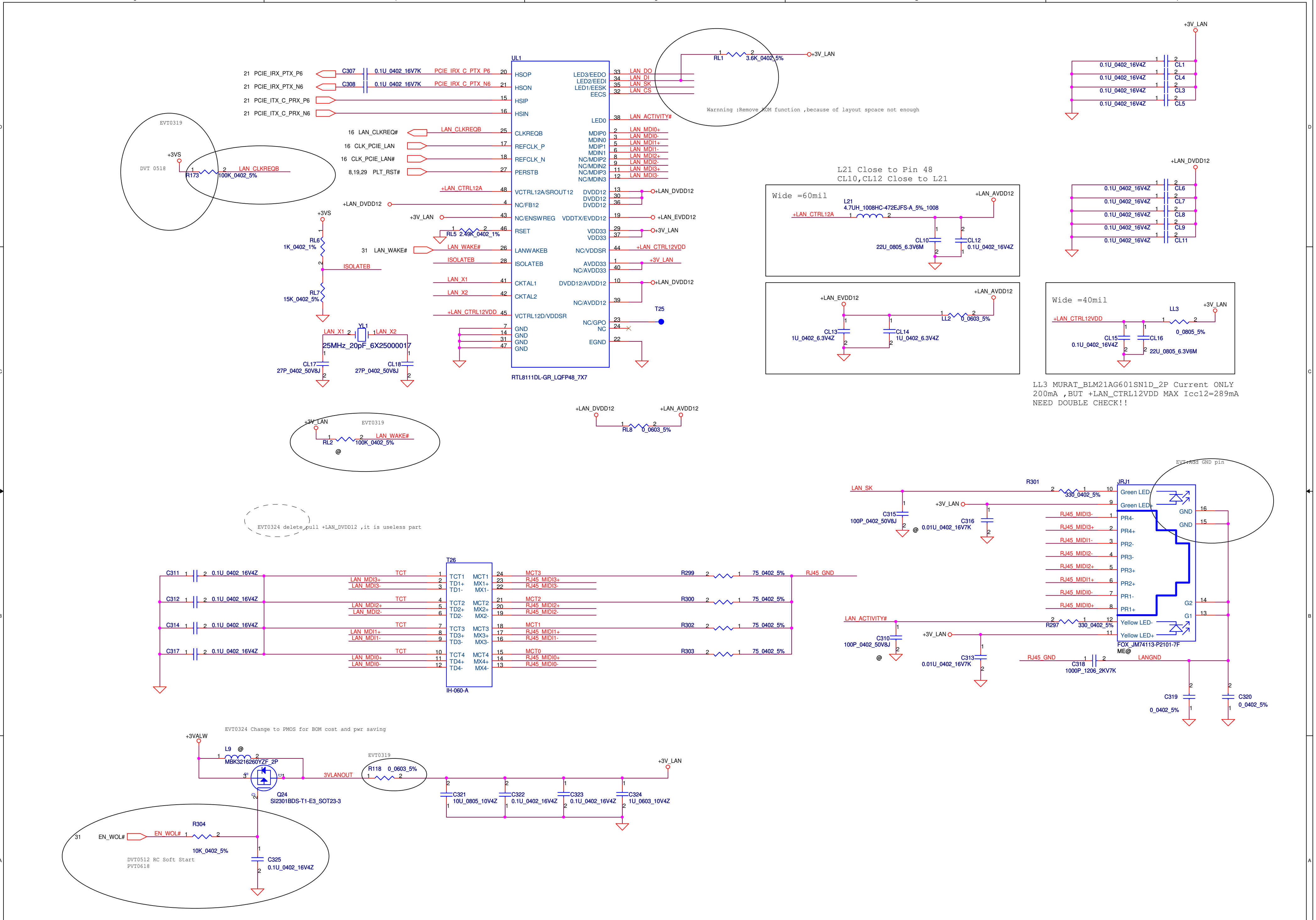
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **HDD & ODD Connector**

Size: B | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 |



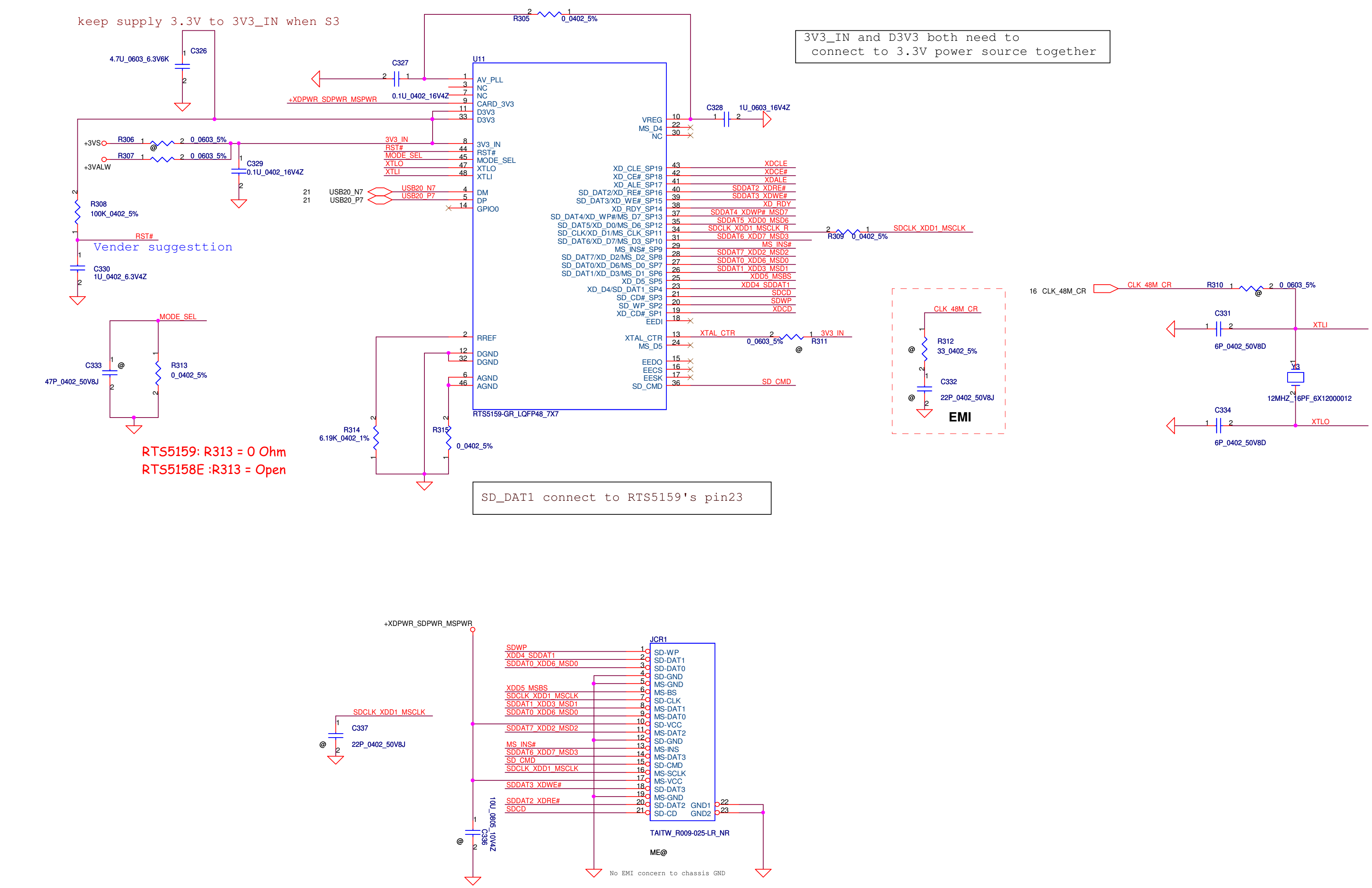
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **RTL8111DL-GR_LQFP48_7X7**

Size: C | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 24 of 43



Security Classification	Compal Secret Data			Compal Electronics,Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title: RTS5159-VCC-GRT CARD READER	
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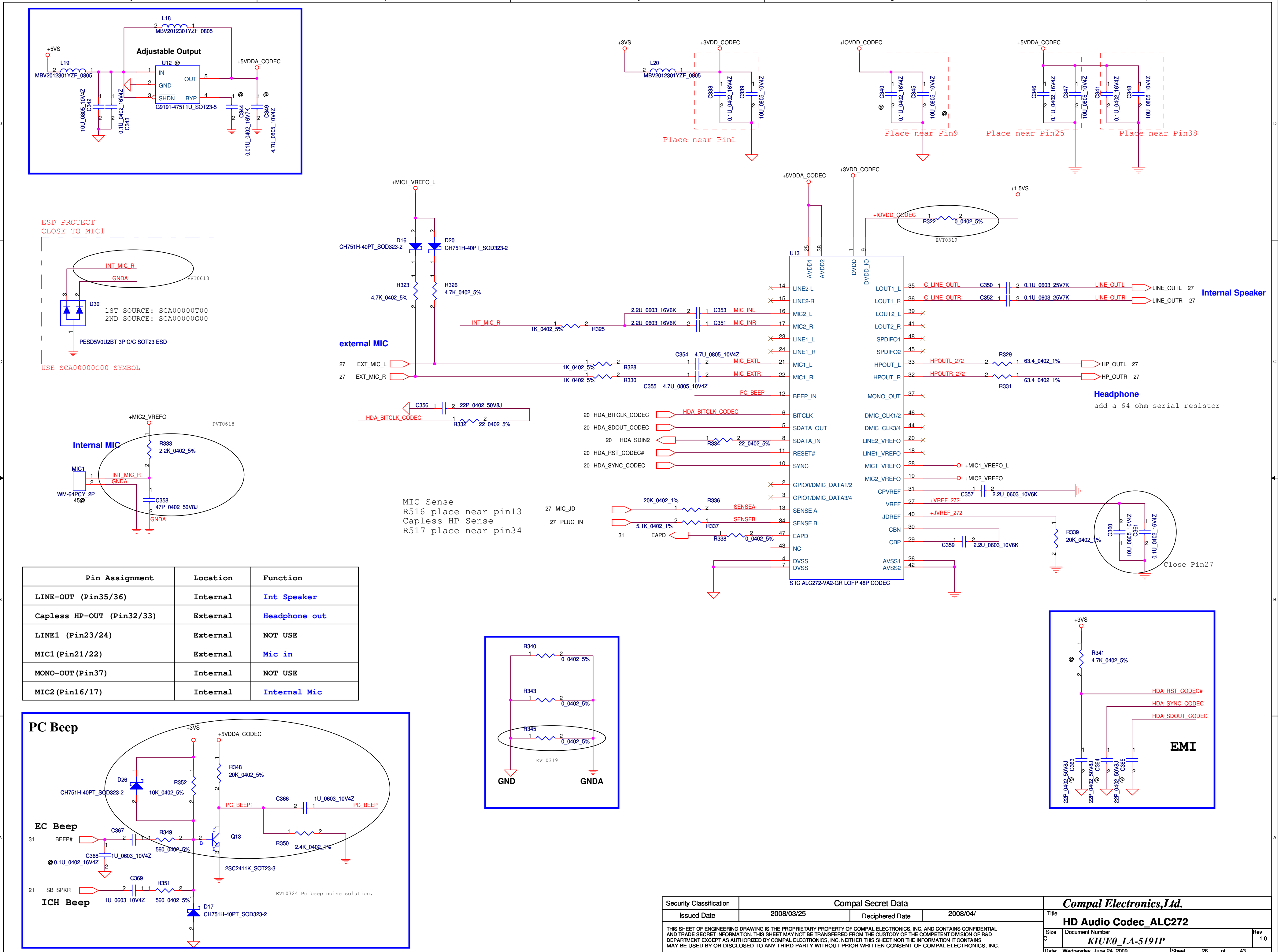
				Date: Wednesday, June 24, 2009	Sheet 25 of 43



Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	NOT USE
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	NOT USE
MIC2(Pin16/17)	Internal	Internal Mic

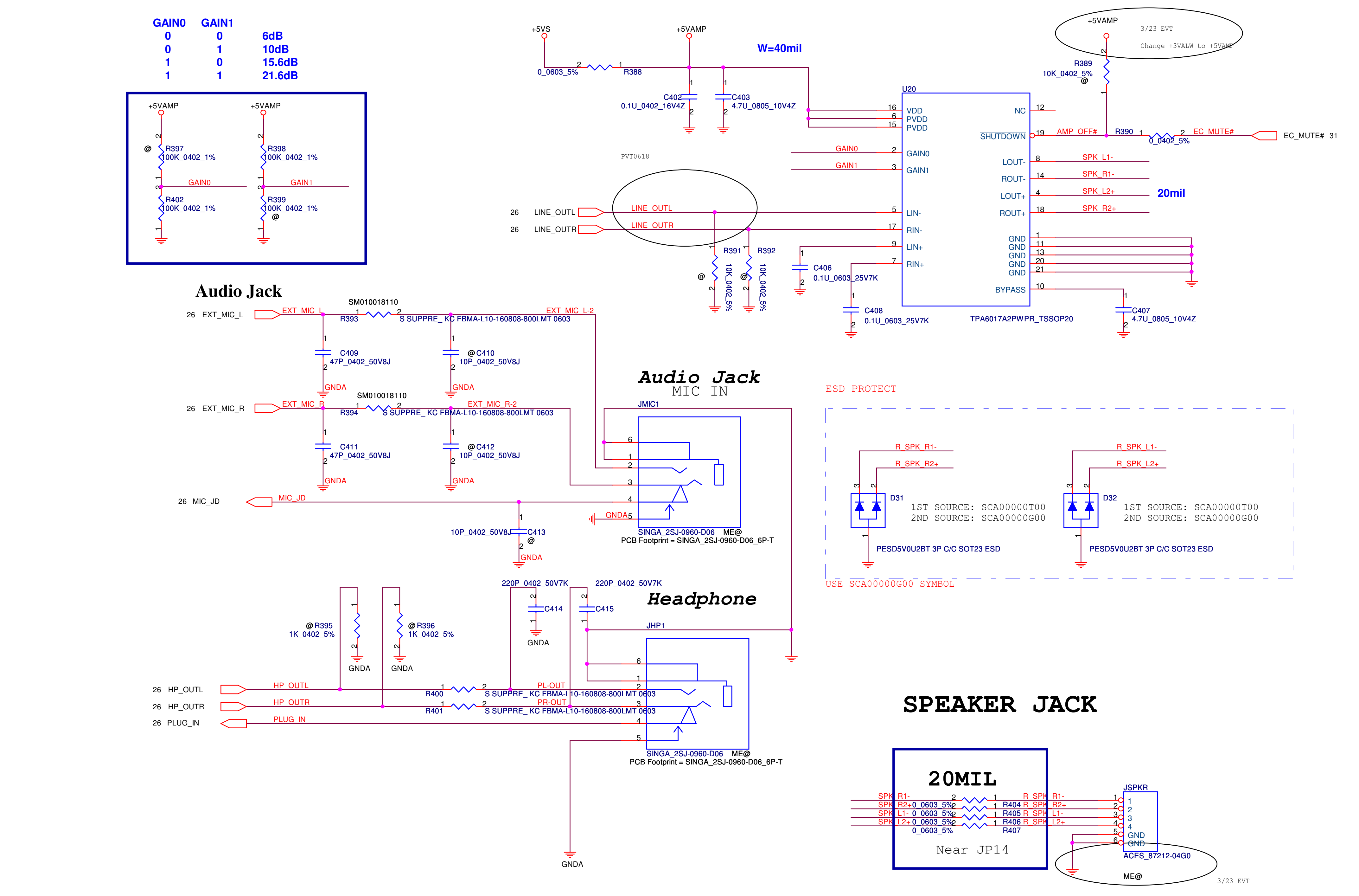
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC272

Size: C — Document Number: KIUE0_LA-5191P — Rev: 1.0

Date: Wednesday, June 24, 2009 — Sheet 26 of 43



Security Classification	Compal Secret Data		Compal Electronics,Ltd.
Issued Date	2008/03/25	Deciphered Date 2008/04/	Title: AMP,Audio speaker CONN
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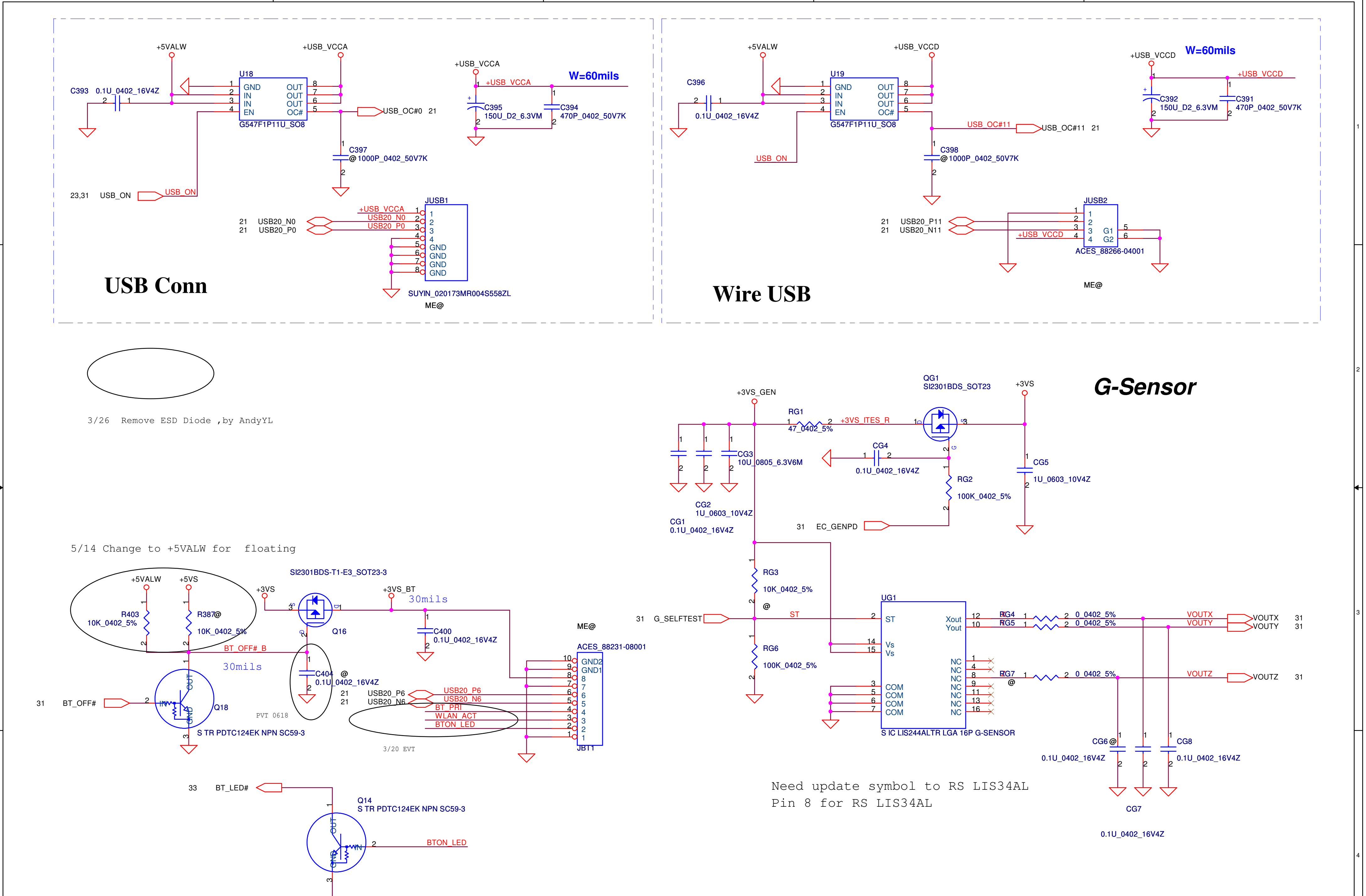
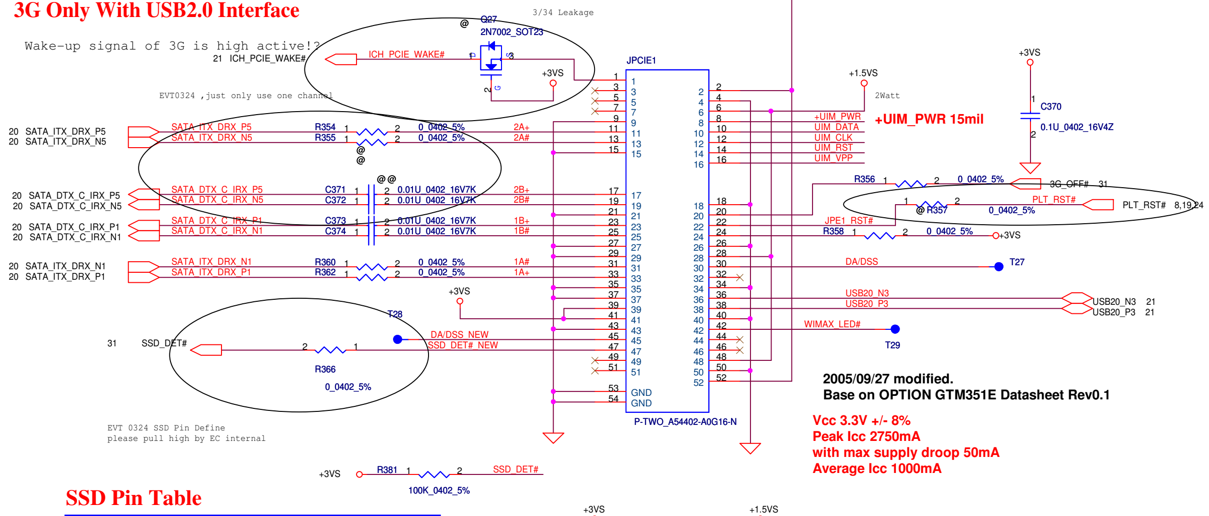
			Date: Wednesday, June 24, 2009; Sheet 27 of 43

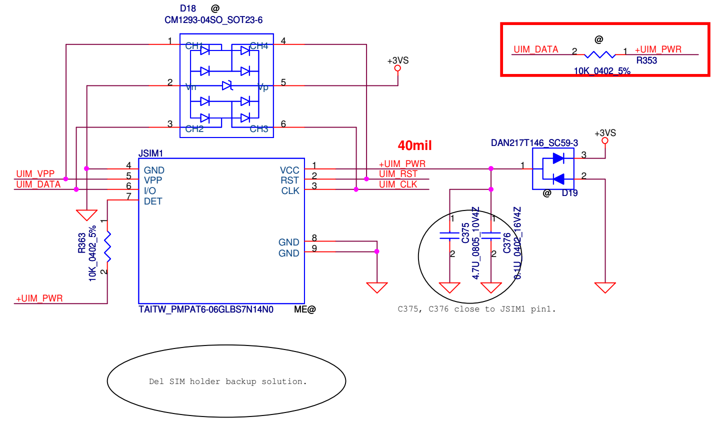


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title: USB/CMOS/BT/G-SENSOR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: KIUE0_LA-5191P; Rev: 1.0
				Date: Wednesday, June 24, 2009; Sheet 28 of 43

Mini-Express Card(Slot 3-WWAN 3G) 4.0 mm high

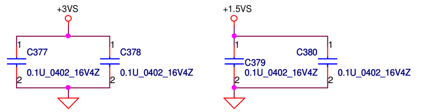
3G Only With USB2.0 Interface

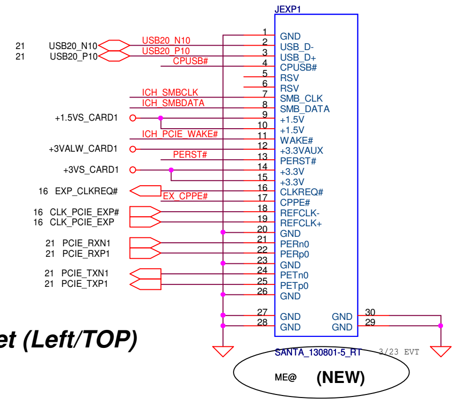




SSD Pin Table

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	DA/DSS
31	-A (port 1)
32	Presence Detection
33	+A (port 1)

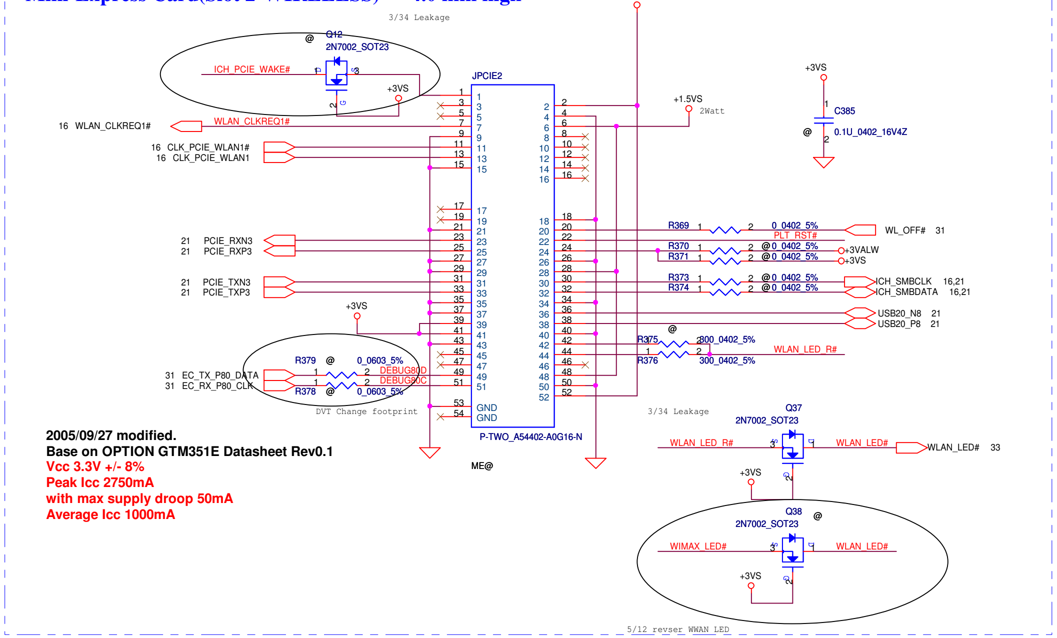




New Card 34mm Socket (Left/TOP)

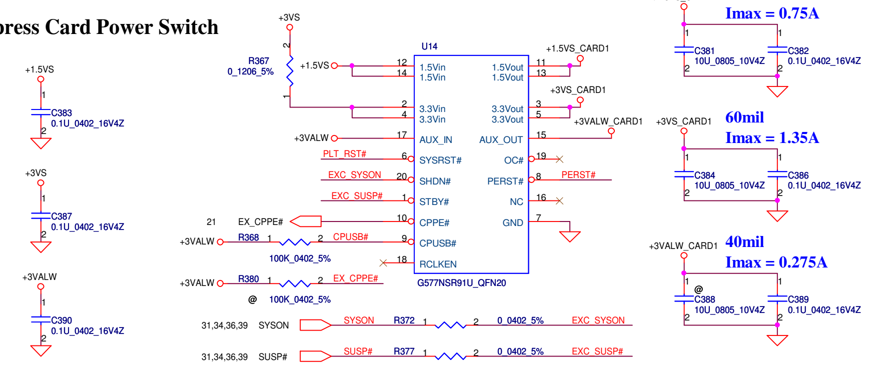
(NEW)

Mini-Express Card(Slot 2-WIRELESS) 4.0 mm high



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Express Card Power Switch



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

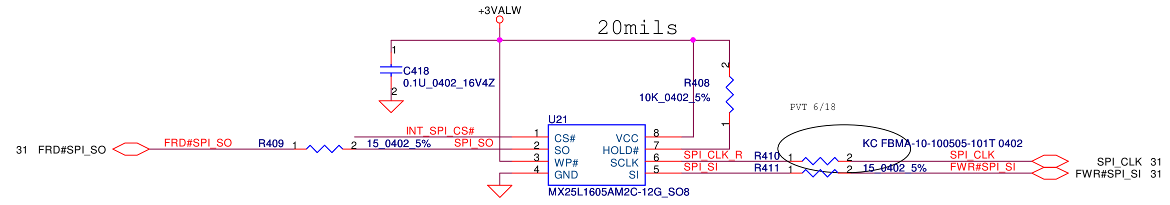
Compal Electronics, Inc.

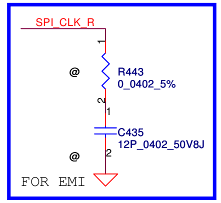
Title: Mini-Card/3G/TV /BT

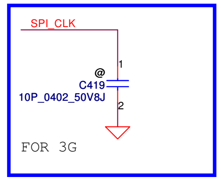
Size | Document Number: KIUE0_LA-5191P | Rev 1.0

Date: Thursday, June 25, 2009 | Sheet 29 of 43

FOR EC 16M SPI ROM

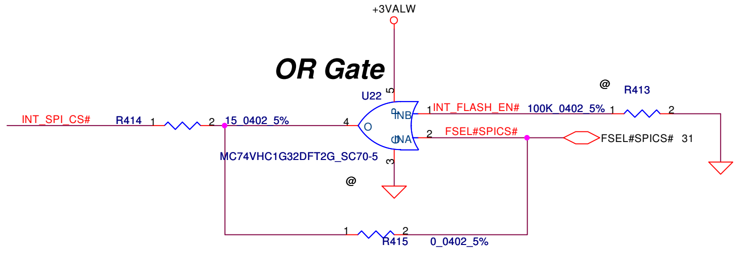




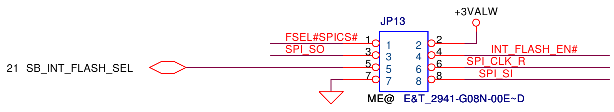


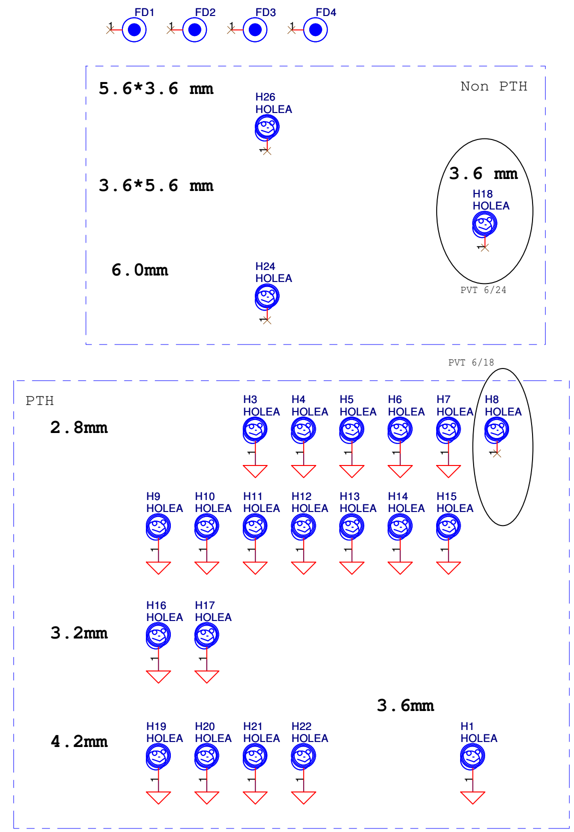
INPUT		OUTPUT Y
A	B	
L	L	L
H	L	H
L	H	H
H	H	H

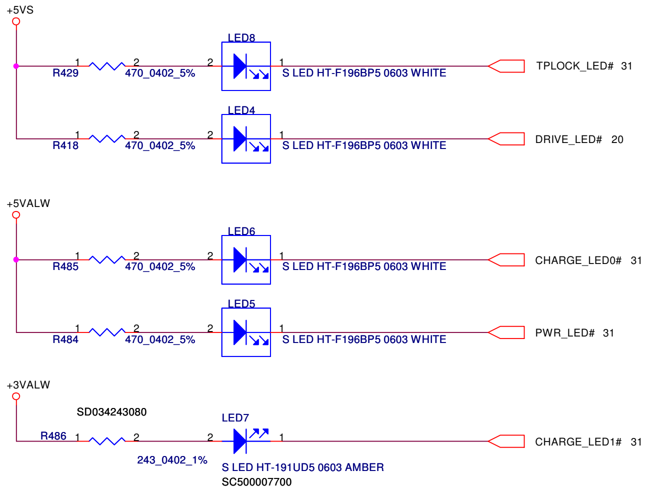
OR Gate



EVT 3/26 Close EC Pin







+5VLAW 470 ohm	typ	max
White LED(Vf)	2.8	3.15
current	4.6mA	3.9mA

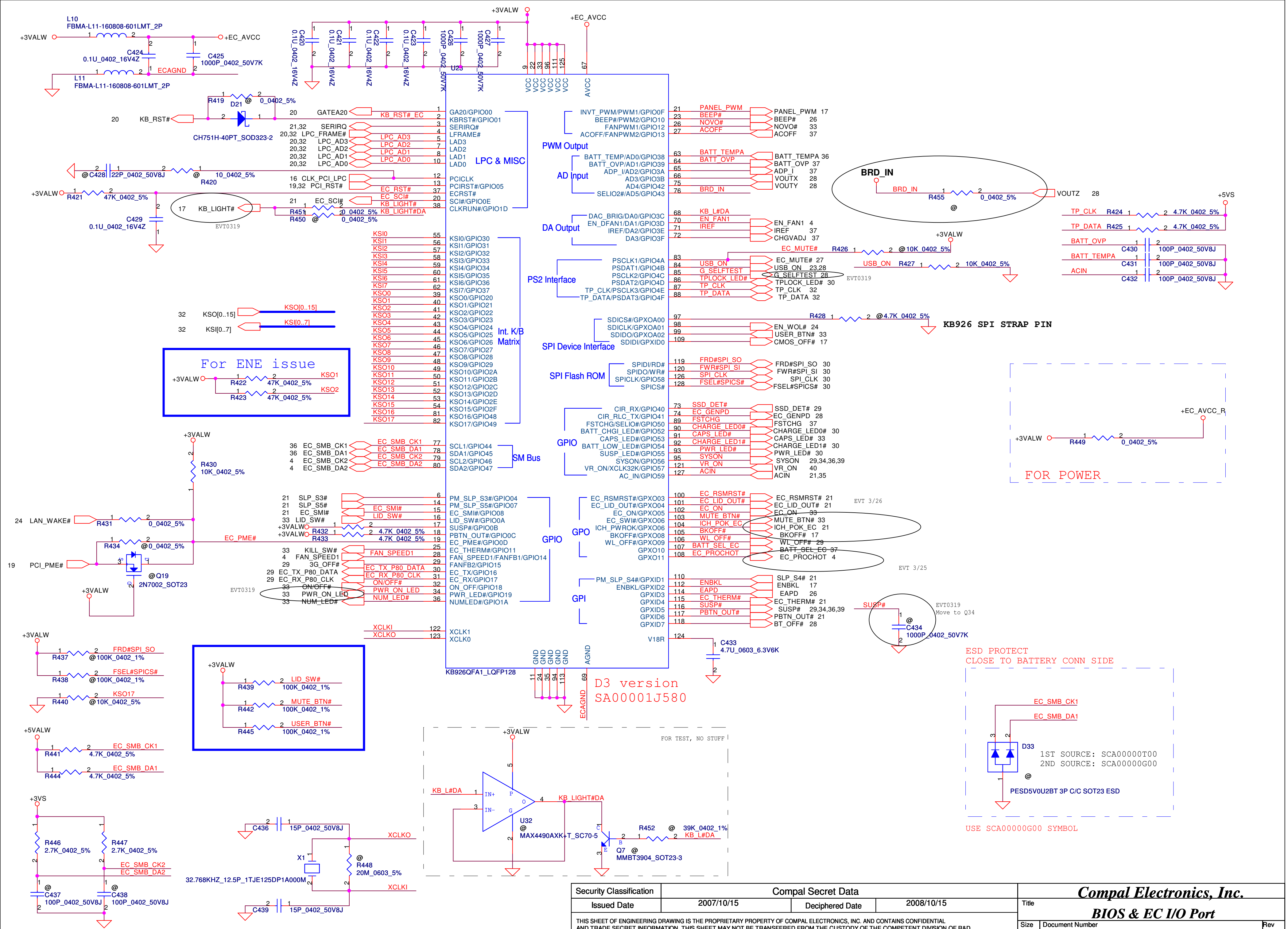
+3.3 VALW 243 ohm	typ	max
Amber LED(Vf)	1.9	2.4
current	5.7mA	3.7mA

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: *LED/EC SPI ROM*

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title: BIOS & EC I/O Port

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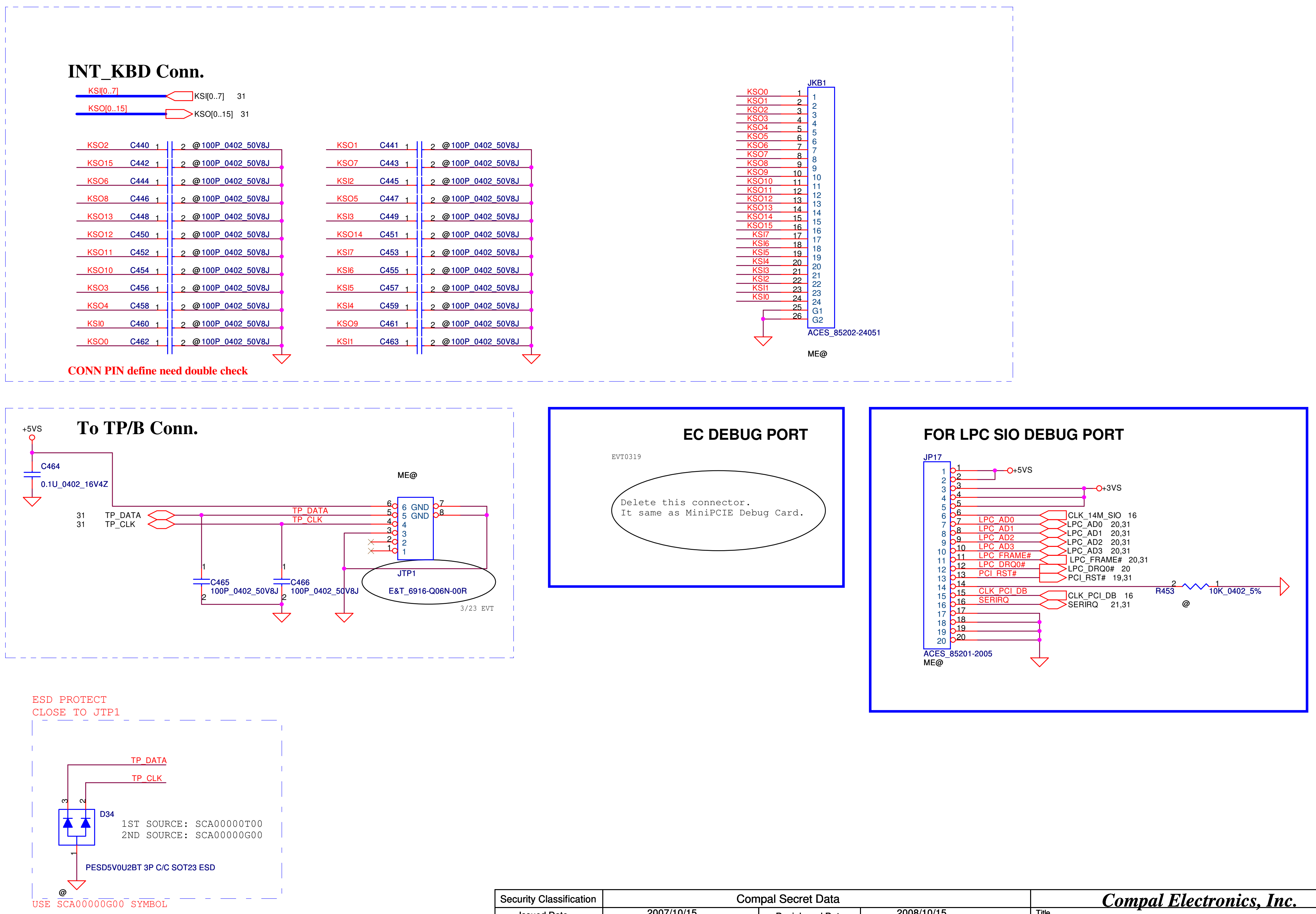
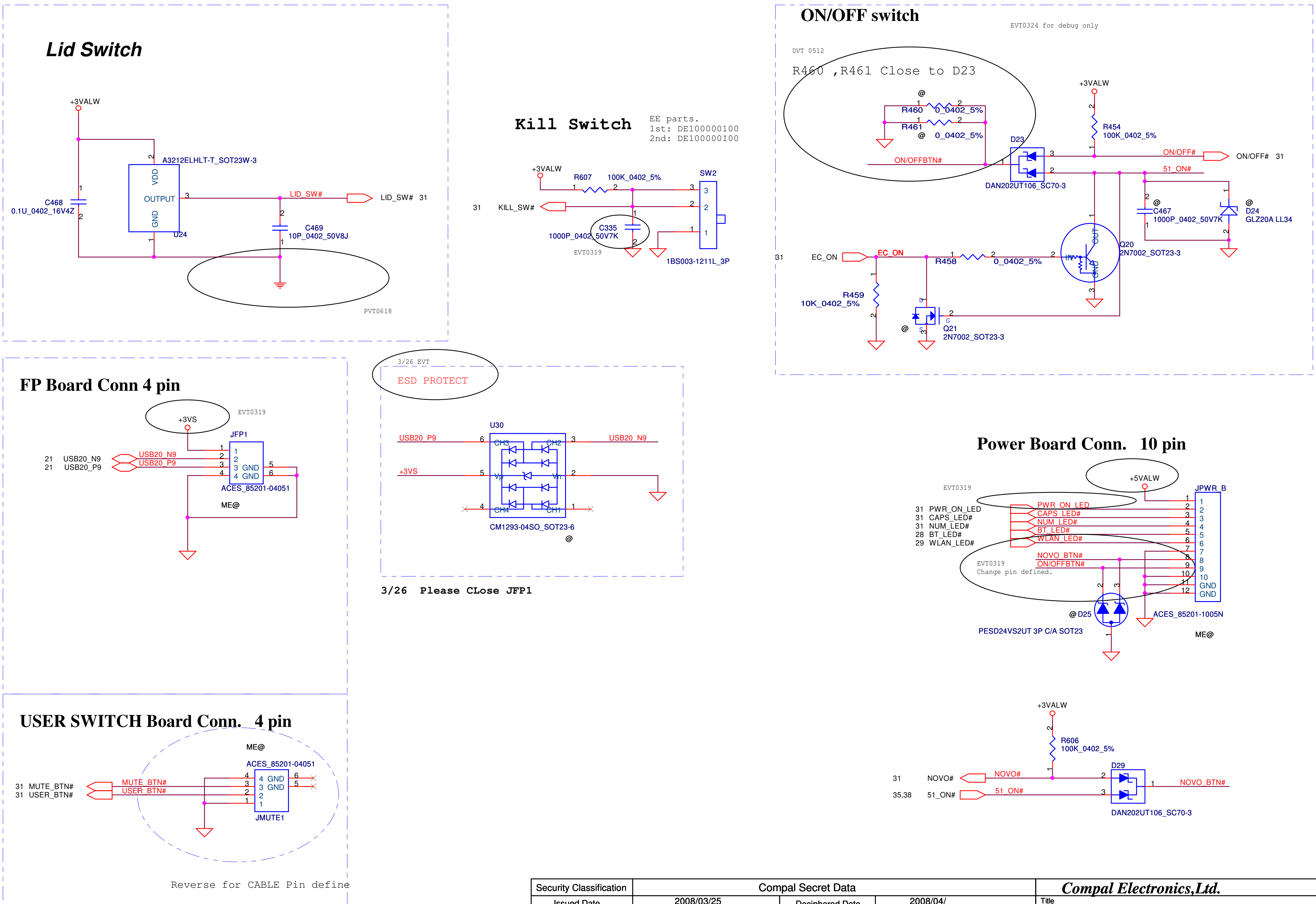
Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 31 of 43



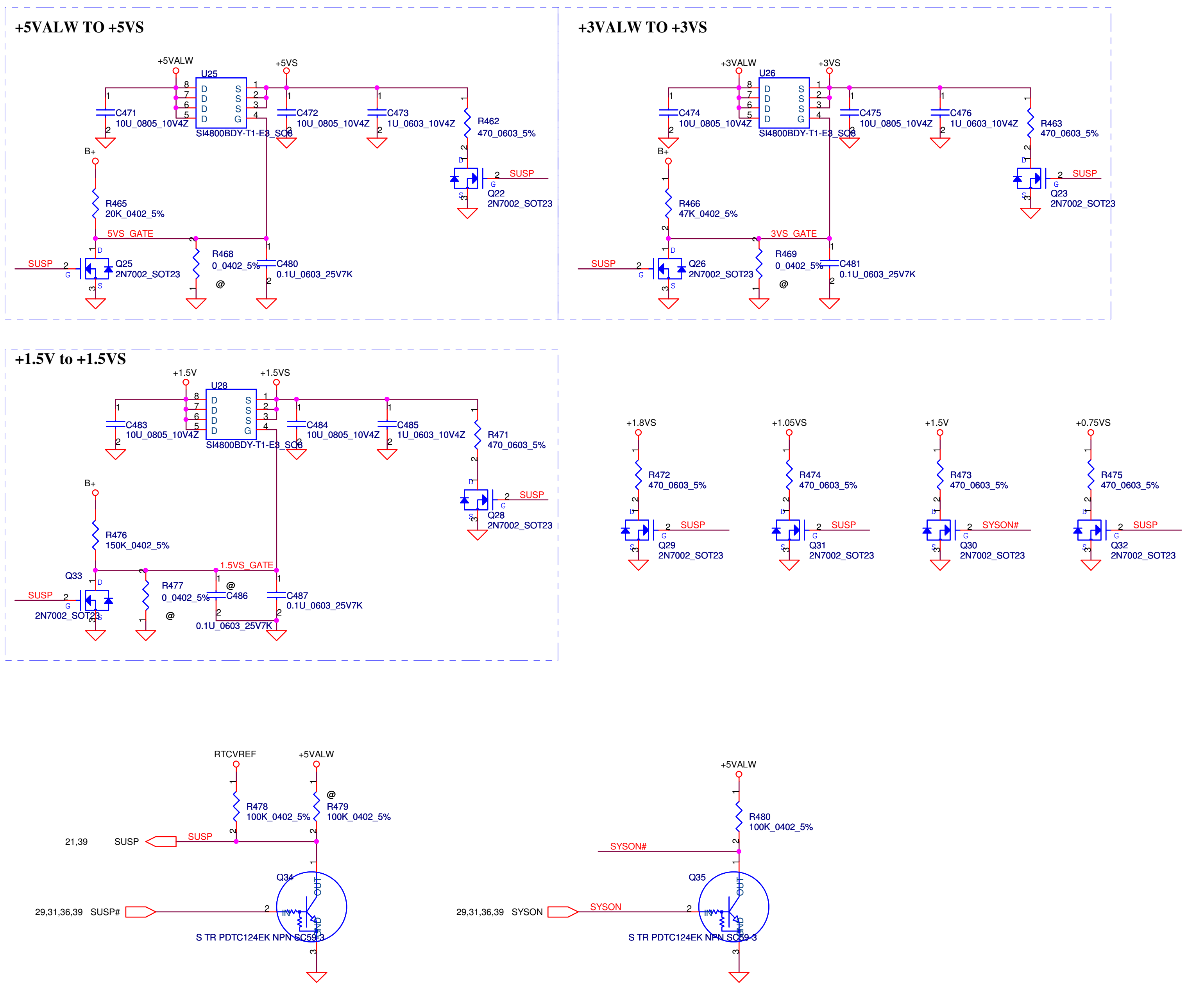
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title: KB /SW /LPC Debug Conn.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: B; Document Number: KIUE0_LA-5191P; Rev: 1.0
				Date: Wednesday, June 24, 2009; Sheet 32 of 43



Security Classification	Compal Secret Data			Compal Electronics,Ltd.
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title: Audio Jack & SW connector

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title: DC Interface	
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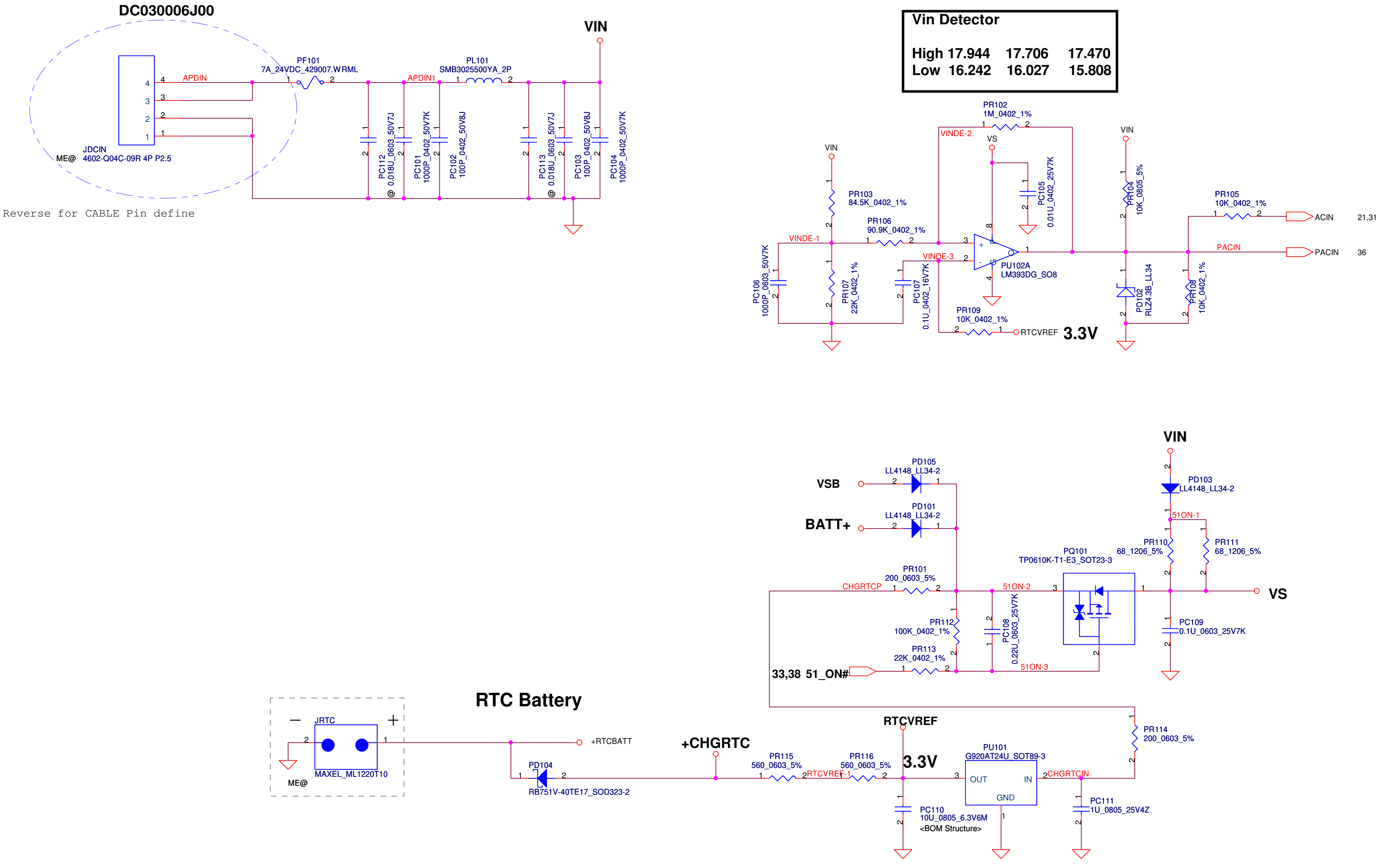
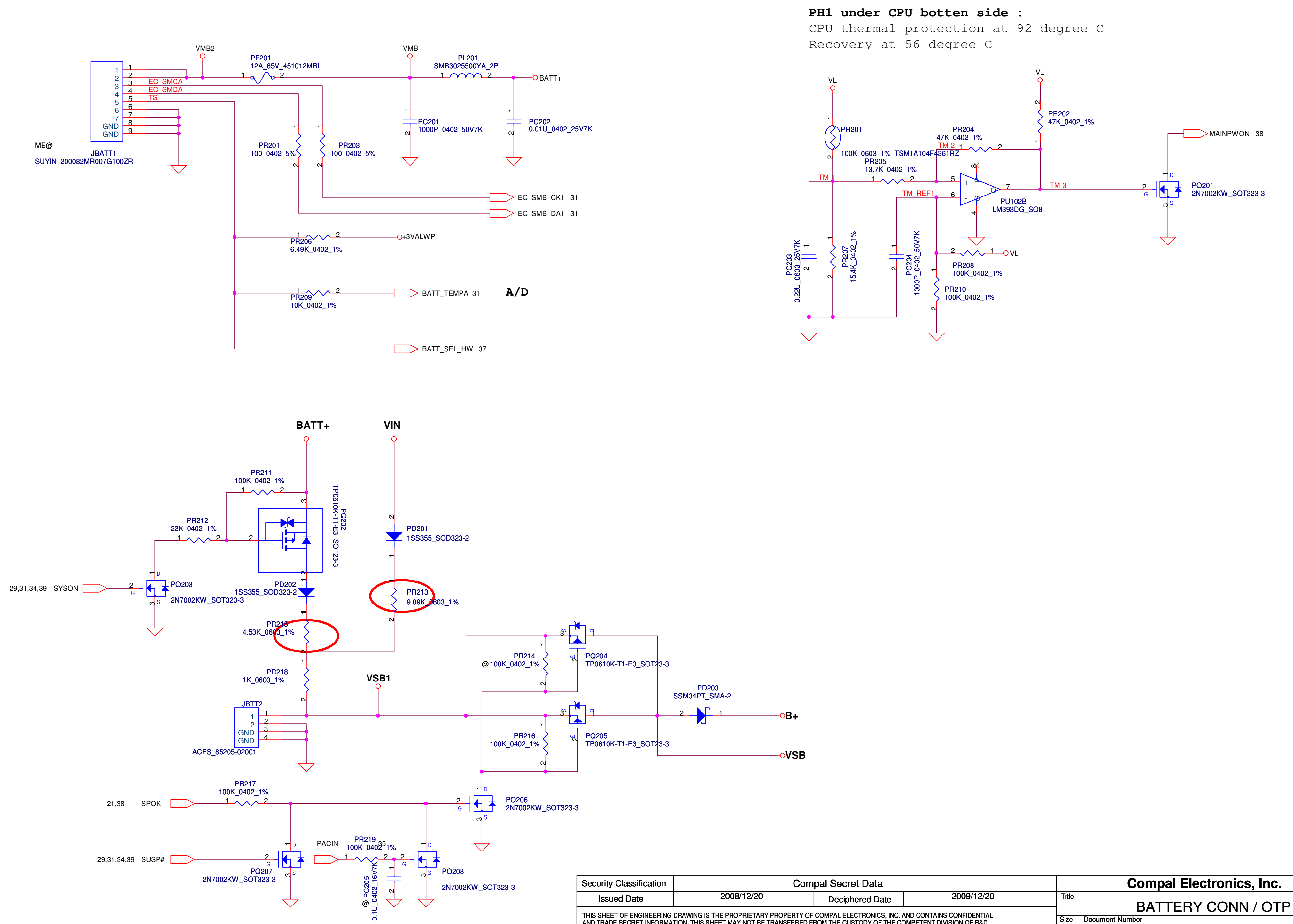
				Date: Wednesday, June 24, 2009	Sheet 34 of 43



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title: DCIN & DETECTOR
Size: Custom	Document Number			Rev 0.1
Date: Wednesday, June 24, 2009	Sheet 35 of 42			



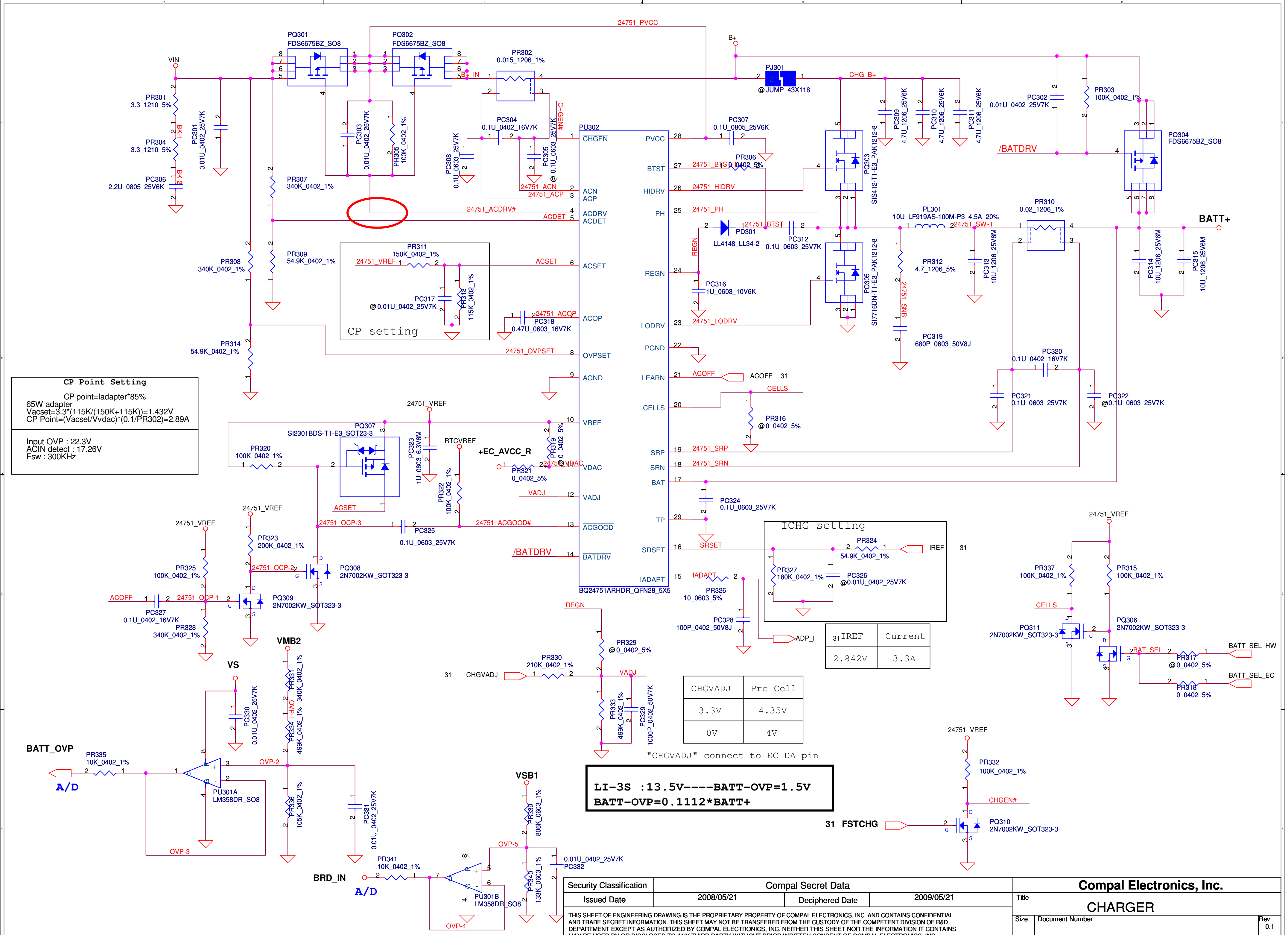
Security Classification	Compal Secret Data		
Issued Date	2008/12/20	Deciphered Date	2009/12/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number | Rev 0.1

Date: Wednesday, June 24, 2009 | Sheet 36 of 42



CP Point Setting

CP point=Iadapter*85%
65W adapter
Vacset=3.3*(115K/(150K+115K))=1.432V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.89A

Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz

IREF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

"CHGVADJ" connect to EC DA pin

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

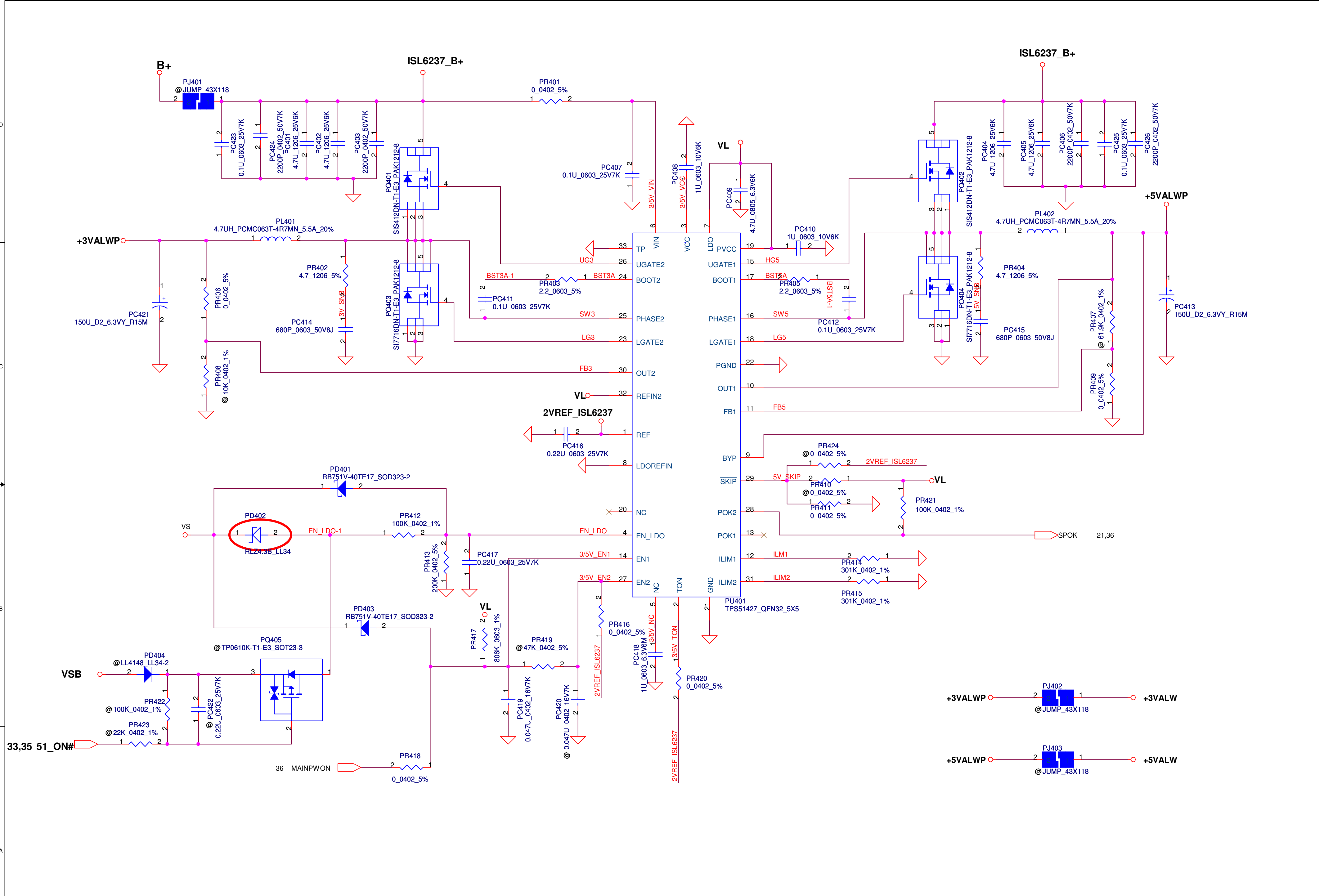
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 0.1

Date: Wednesday, June 24, 2009 | Sheet 37 of 42

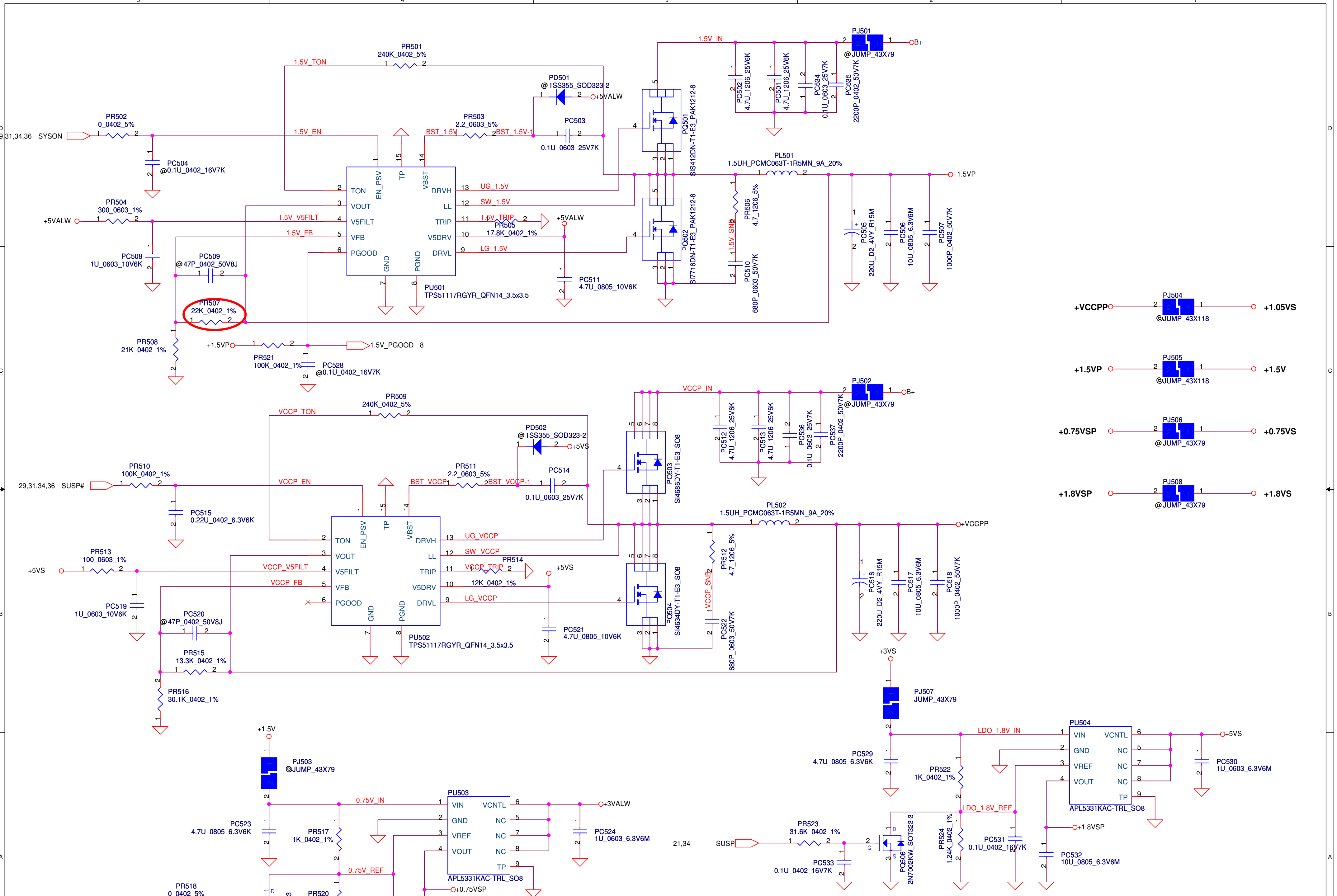


Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: **3VALW/5VALW**

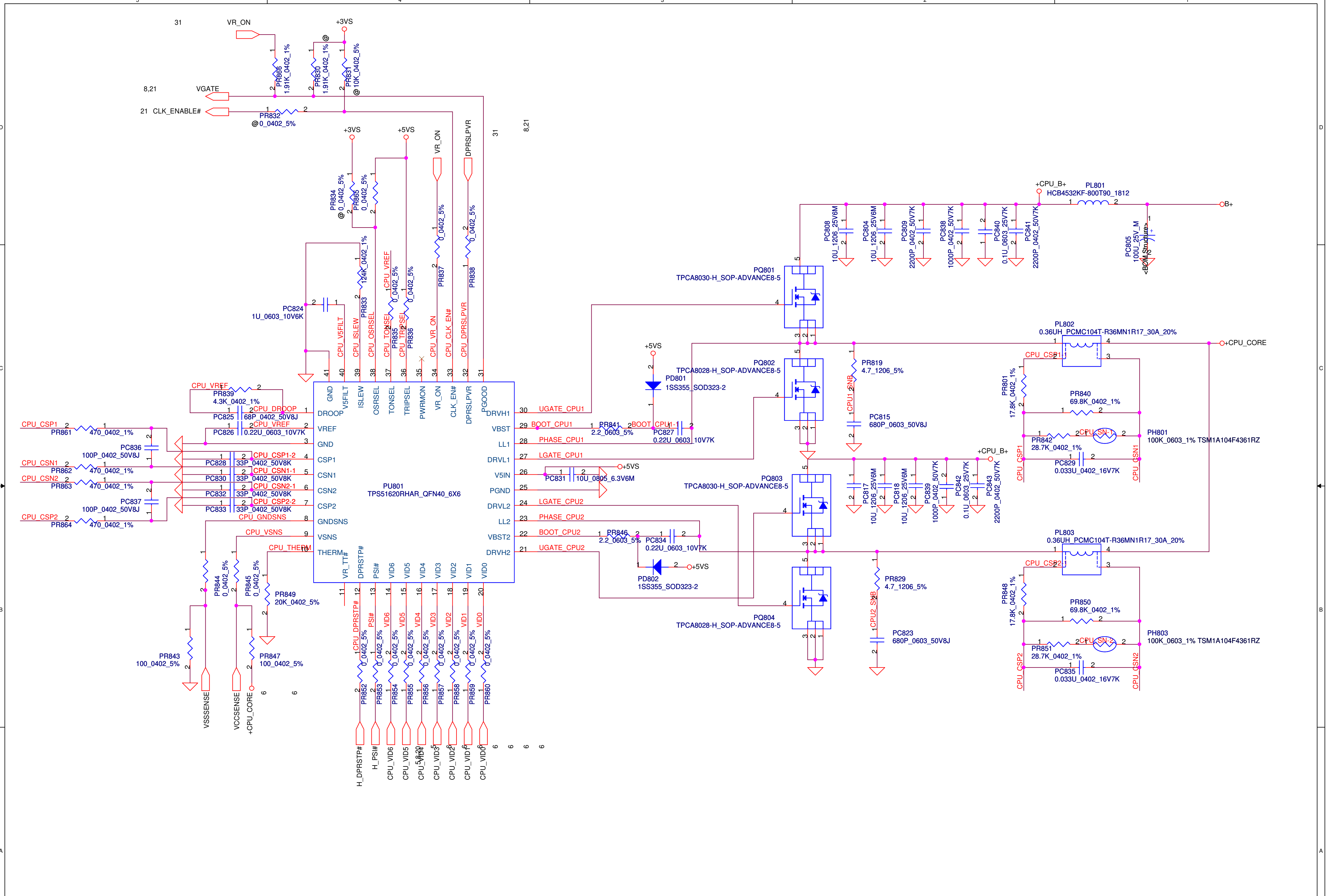
Size: Custom | Document Number | Rev: 0.1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/11/12	Deciphered Date 2008/11/12	Title: 1.5V / 0.9V / VCCP / 1.8V

Size | Document Number | Rev 0.1

Date: Wednesday, June 24, 2009 | Sheet 39 of 42



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.1

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change design	add bridge battery charge circuit		P.37	add PR215 and PR218 and change PR213 from 2K to 2.2K	2009.3.20	DVT
2	Change design	Change design		P.36	JDCIN turn off 180 degree	2009.3.20	DVT
3	Change design	Change design		P.37	change JBTT2 from lie to stand	2009.3.24	DVT
4	Change design	Change design		P.37	add PR219 and PC205	2009.3.25	DVT
5	Change design	Change design		P.39	change PR403 and PR405 from 0 to 2.2 ohm	2009.3.25	DVT
6	Change design	Change design		P.40	change PR503 and PR511 from 0 to 2.2 ohm	2009.3.25	DVT
7	Change design	Change design		P.41	change PR841 and PR846 from 0 to 2.2 ohm	2009.3.25	DVT
8	Change design	Change design		P.40	change PR514 from 15.4K to 12K ohm	2009.3.25	DVT
9	Change design	Change design		P.38	add PR339 PR340 PR341 and PC332	2009.5.5	PVT
10	Change design	Change design		P.41	change PR839 from 5.76K to 4.3K ohm	2009.5.15	PVT
11	Change design	Change design		P.40	change PR504 and PR513 from 422 to 300 ohm	2009.5.15	PVT
12	Change design	Change design		P.38	delect PR338	2009.6.18	Pre_MP
13	Change design	Modify bridge battery charge current		P.37	change PR213 from 2.2k to 9.09k and PR215 from 1.21k to 4.53k	2009.6.18	Pre_MP
14	Change design	Modify 1.5V output voltage		P.40	change PR507 from 21k to 22k	2009.6.18	Pre_MP
15	Change design	For bridge battery can work in S3		P.39	change PD402 from RLZ5.1B to RLZ4.3B	2009.6.18	Pre_MP
16							
17							
18							
19							
20							
21							

NO DATE PAGE MODIFICATION LIST PURPOSE

EVT modify 20090319

1. 03/19 P.17: Change EDID voltage to +3VS rail.
2. 03/19 P.23: HDD power +3VS +5VS add resistors for measure.
3. 03/19 P.24: LANREQB is low active. Don't need unnecessary circuit.
4. 03/19 P.24: Net LAN_WAKE# is double pull-up. del RL2.
5. 03/19 P.24: +3V_LAN add a resistor for measure.
6. 03/19 P.32: Del JP15. It same as MiniPCIE Debug Card.
7. 03/19 P.26: R322 add, R321 del. For HDA interface.
8. 03/19 P.33: Change Finger printer from Egis to Upek. Power rail is +3VS of Upek.
9. 03/19 P.16: Avoid glitch of H_STP_PCI#, pull-up PCI_STP# directly.
10. 03/19 P.29: For debug card issue. And add R378, R379, R295 100K.
11. 03/19 P.21: For Waveform add C60.
12. 03/19 P.26: For EMI R345.
13. 03/19 P.31: KB light change to pin38 GPIO1D.
14. 03/19 P.31: Add EC pin34 GPIO19 PWR_ON_LED to page.33 power board connector.
15. 03/19 P.31: Add EC pin85 GPIO4C G_SELFTEST to page.28 G-sensor ST pin.
16. 03/19 P.33: Add C335 for Kill-switch.
17. 03/19 P.33: Change JPWR_B conn Pin define

EVT modify 20090320

18. 03/20 P.6: C16 NC,for Pwr confirm
19. 03/20 P.28: Change JBT1 pin define for BT spec updated

EVT modify 20090323

20. 03/23 P.29: Change JEXP1 ;JLVDS1; JTP1 Conn by ME

EVT modify 20090324

21. 03/24 P.17: Reverse GMCH DPST function
22. 03/24 P.29: Reverse MINI CARD SATA Lane
23. 03/24 P.29: Change Pin Define for SSD
24. 03/24 P.29: Reveerse JPCIE1 PLT_RST#

EVT modify 20090325

25. 03/25 P.4 : Add thermal protection Circuit by lenvono
26. 03/25 P.21 : S0 to G3 state ,abnormal shudown
27. 03/25 P.21 : Change New CARD PCI-E port 4 to Port 1 for powr saving
28. 03/25 P.33 : ADD EMI&ESD solution
29. 03/25 P.24 : Delete Mac ROM Circuit ,Because of layout space not enough
30. 03/25 P.24 : Change Q24 to PMOS From NMOS,to saving bom cost
31. 03/25 P.26 : modify PC-BEEP circuit aviod Signal and Pwr noise

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Detect Bridge Bettery life	Can't detect Bridge bettery	0.3	31	ADD R455	5/5	DVT
2	Esay rework for PORT 80	Not easy debug with system builded	0.3	29	CHANGE R378,R379 SIZE From 0402 to 0603 (NC)	5/13	DVT
3	BT Pwer MOS Floating	BT Pwr MOS Floating	0.3	28	NC R387, ADD R403	5/13	DVT
4	WWAN Noise Solution	Reserve C470	0.3		ADD C470 (NC)	5/13	DVT
5	Material LT	LIS34ALTR LT more than 4 months	0.3	28	CHANGE UG1 From LIS34ALTR to LIS244ALTR	5/13	DVT
6	DFB Design	COST DOWN	0.3	17	DELETE R167,R168,R287,R361	5/13	DVT
7	WWLAN LED	Reverse WWAN LED SWITCH	0.3	29	ADD Q38 (NC)	5/13	DVT
8	ICH_POK Glitch	Glitch will cause abnormal Power sequence	0.3	21	ADD D35,Q39 (NC),R456 (NC)	5/13	DVT
9	EMI Solution	EMI issue	0.3	17	ADD D36	5/13	DVT
10	Soft Start circuit	OCP	0.3	24	ADD R304,C325 (NC),C122	5/13	DVT
11	Debug use only		0.3	33	DELETE J3,J4,SW1,ADD R460 (NC),R461(NC)	5/13	DVT
12	BOM Option	Reserve R121	0.3	16	CHANGE R122 From 12 Ohm to 33 Ohm	5/16	DVT
13	BOM Option	ALC272-GR EOL	0.3	20	CHANGE SA00002CI00 to SA00002CI10	5/25	DVT
14	BOM Option	DELETE ROHM MATERIAL FROM 1st BOM	0.3		CHANGE SBX01240010 to SB00000AG00	5/25	DVT
15	BOM Modify		1.0	23	CHANGE R90 SIZE From 0603 to 0805, DELETE R335,R342,R416	6/23	PVT
16	Stepping to V1.0	Update LA5191PR10 to Stepping to V1.0	1.0	01	Update DAZ P/N to V1.0 and ADD Sub-Bard P/N LS5191/LS5192/LS5193/LS5194	6/23	PVT
17	Soft START Circuit	OCP for LAN	1.0	24	Change R304 from 0 Ohm to 10K Ohm , Delete C122	6/23	PVT
18	Mic Pull high change		1.0	26	Change R333 From 4.7K Ohm to 2.2K Ohm	6/23	PVT
19	AUDIO LINE OUT CAP	Remove Duplicated Cap	1.0	27	DELETE C404,C405	6/23	PVT
20	EMI SOLUTION	SPI CLK	1.0	30	Change R410 From 15 Ohm to KC FBMA-10-100505-101T 0402	6/23	PVT
21	Soft START Circuit	OCP for Bluetooth	1.0	28	ADD C404 (NC)	6/23	PVT
21	Soft START Circuit	OCP for CAMERA	1.0	17	ADD C416 (NC)	6/23	PVT

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