

Model Name : AIVP1/AIVP2

File Name :

Compal Confidential

AIVP1/AIVP2 UMA M/B Schematics Document

Intel Bay Trail M

2015-01-15

REV: 0.2

14@
DA1 PCB

Part Number	Description
DA6001DH000	REV0.1 M/B

15@
DA2 PCB

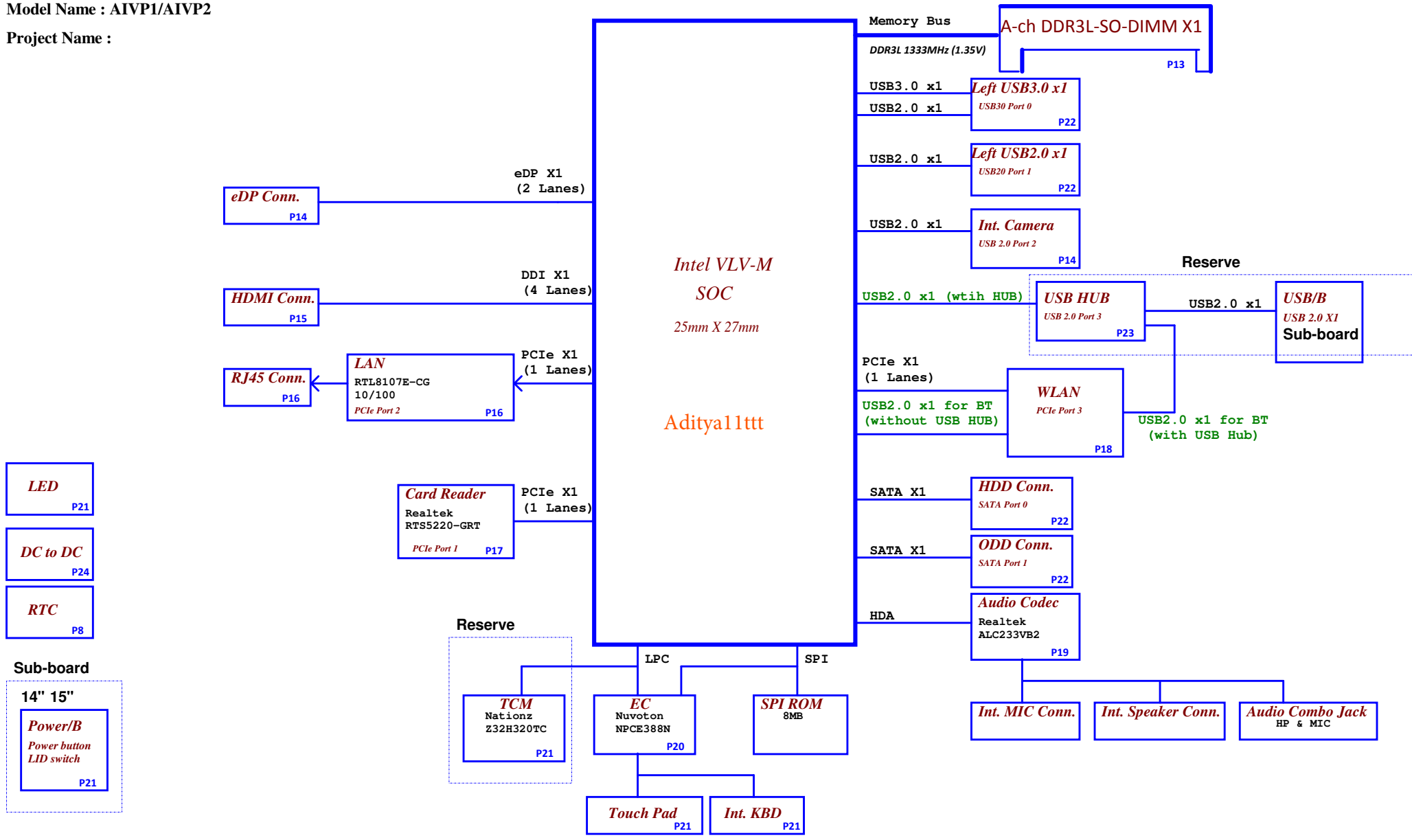
Part Number	Description
DA6001DH000	REV0.1 M/B

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/07	Deciphered Date	2015/11/07	Title
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Model Name : AIVP1/AIVP2

Project Name :



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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Title
				Block Diagram
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMI@
EMC requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
TCM requirement	TCM@
NTCM SKU	NTCM@
Camera requirement	CMOS@
ODD requirement	ODD@
USB HUB requirement	HUB@
Port 80(Debug Port)	DB@
Bluetooth requirment	BT@
14"	14@
15"	15@

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h

Aditya11ttt

43 level BOM table

43 Level	Description	BOM Structure

UC4
N3540@

UC4
N2940@

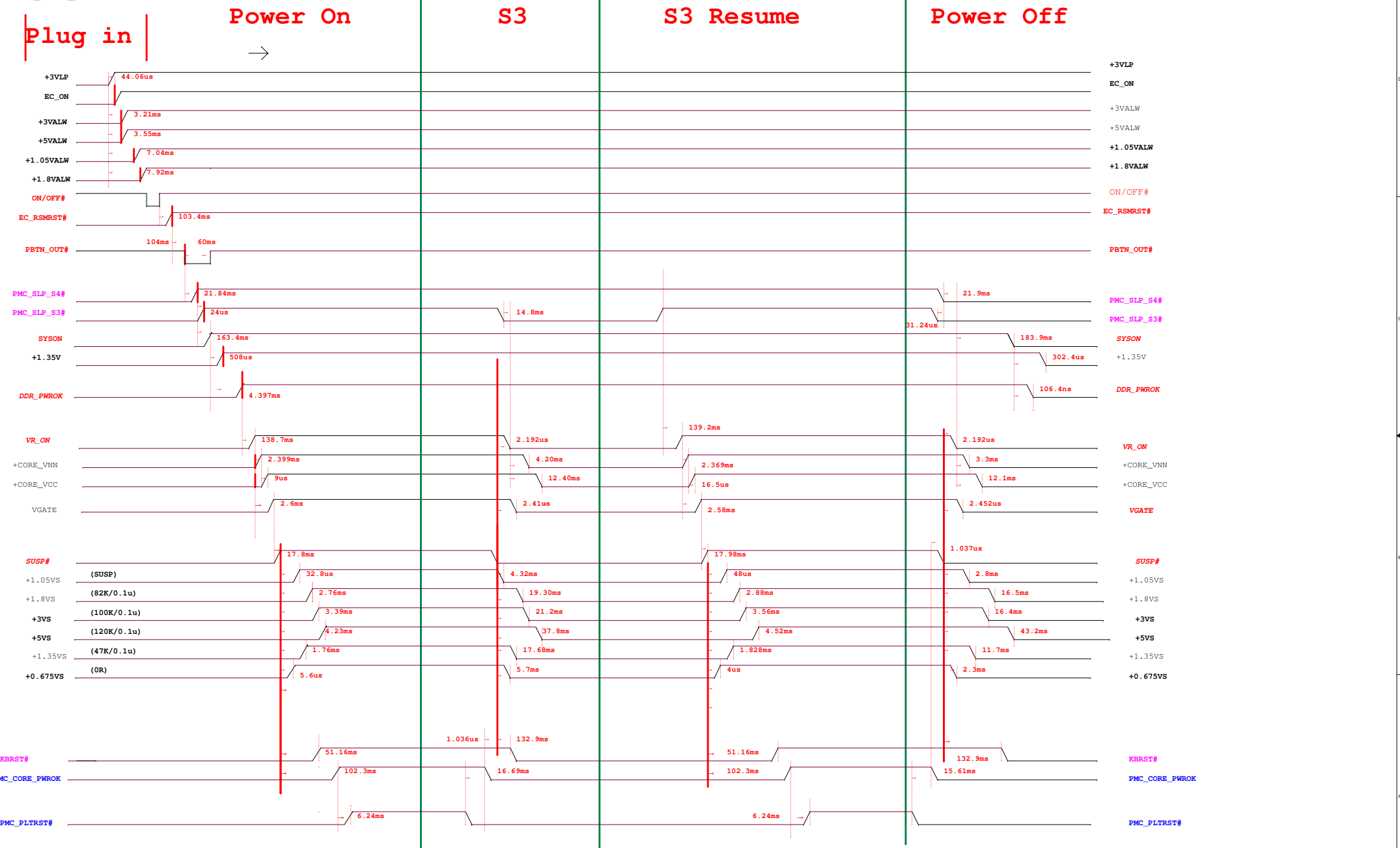
UC4
N2840@

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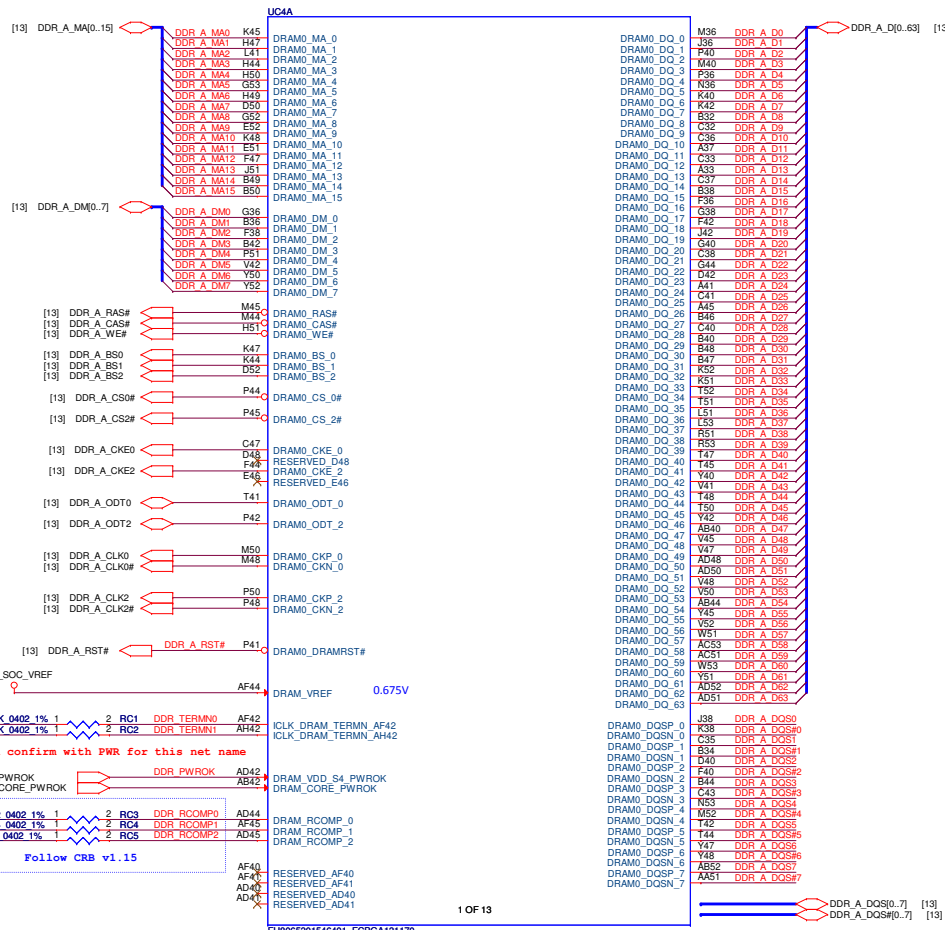
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S IC FH8065301903600 SR1YJ C0 2.16G C38! Part Number = SA00007ZJ30

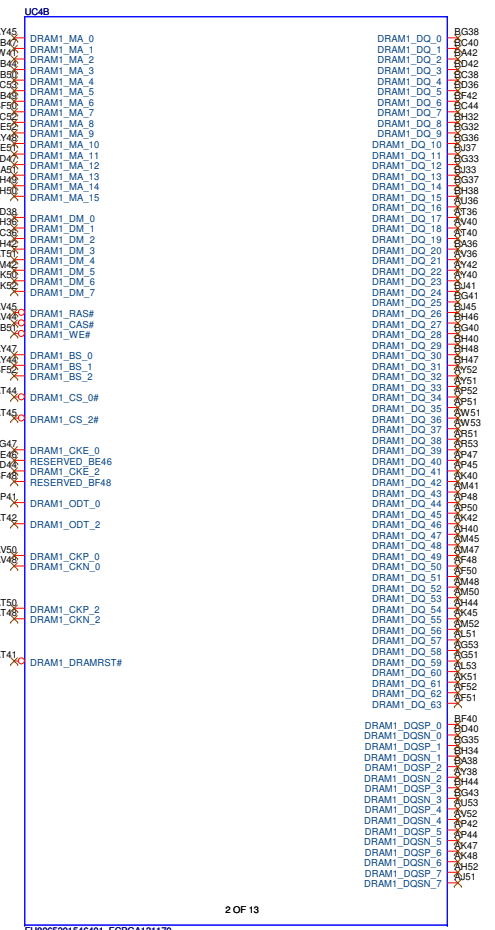
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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Title
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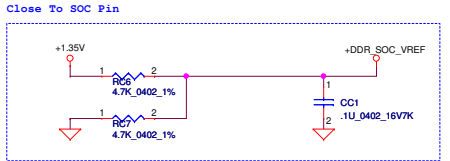
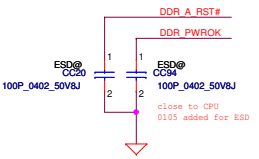
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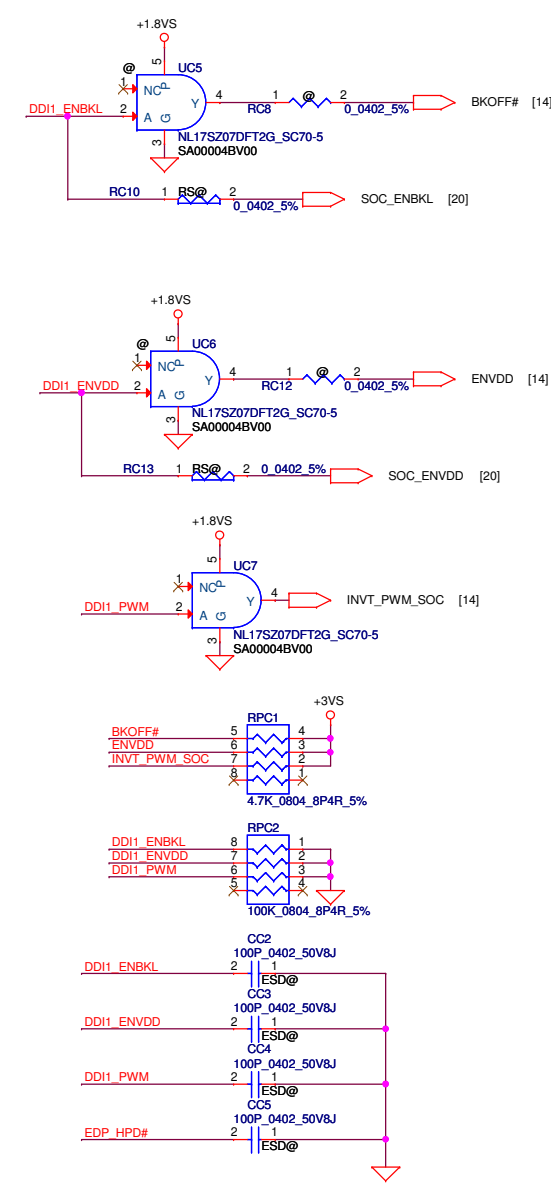
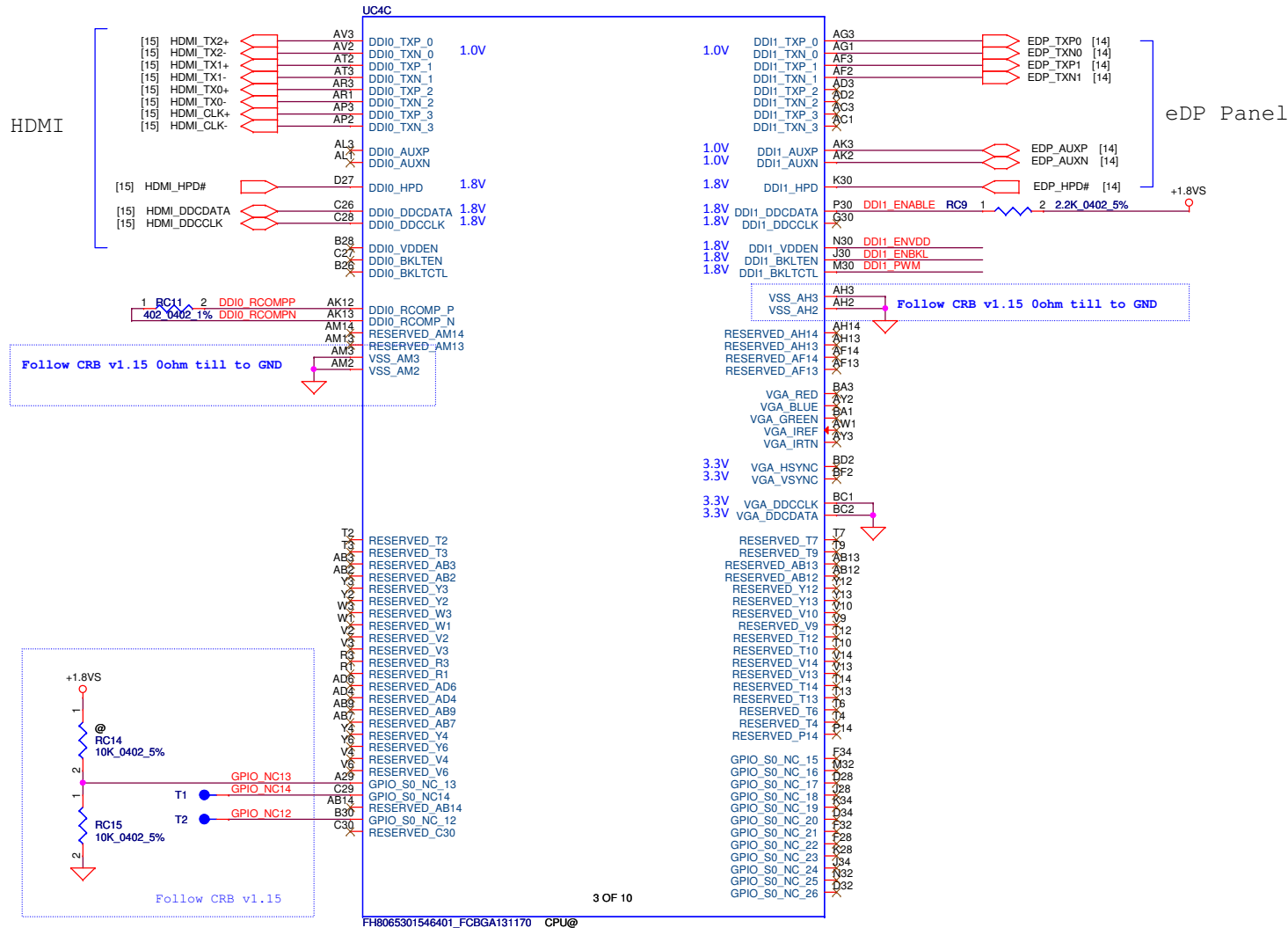
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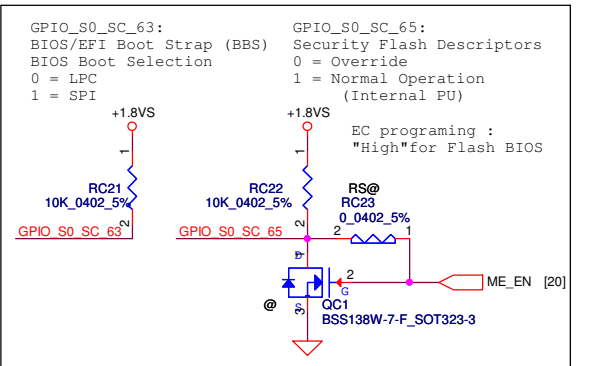
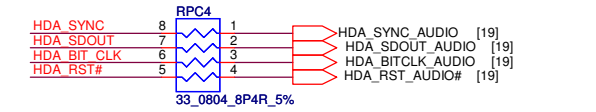
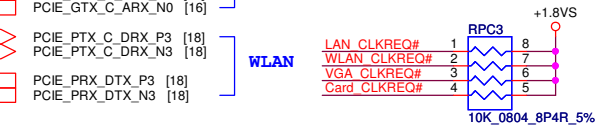
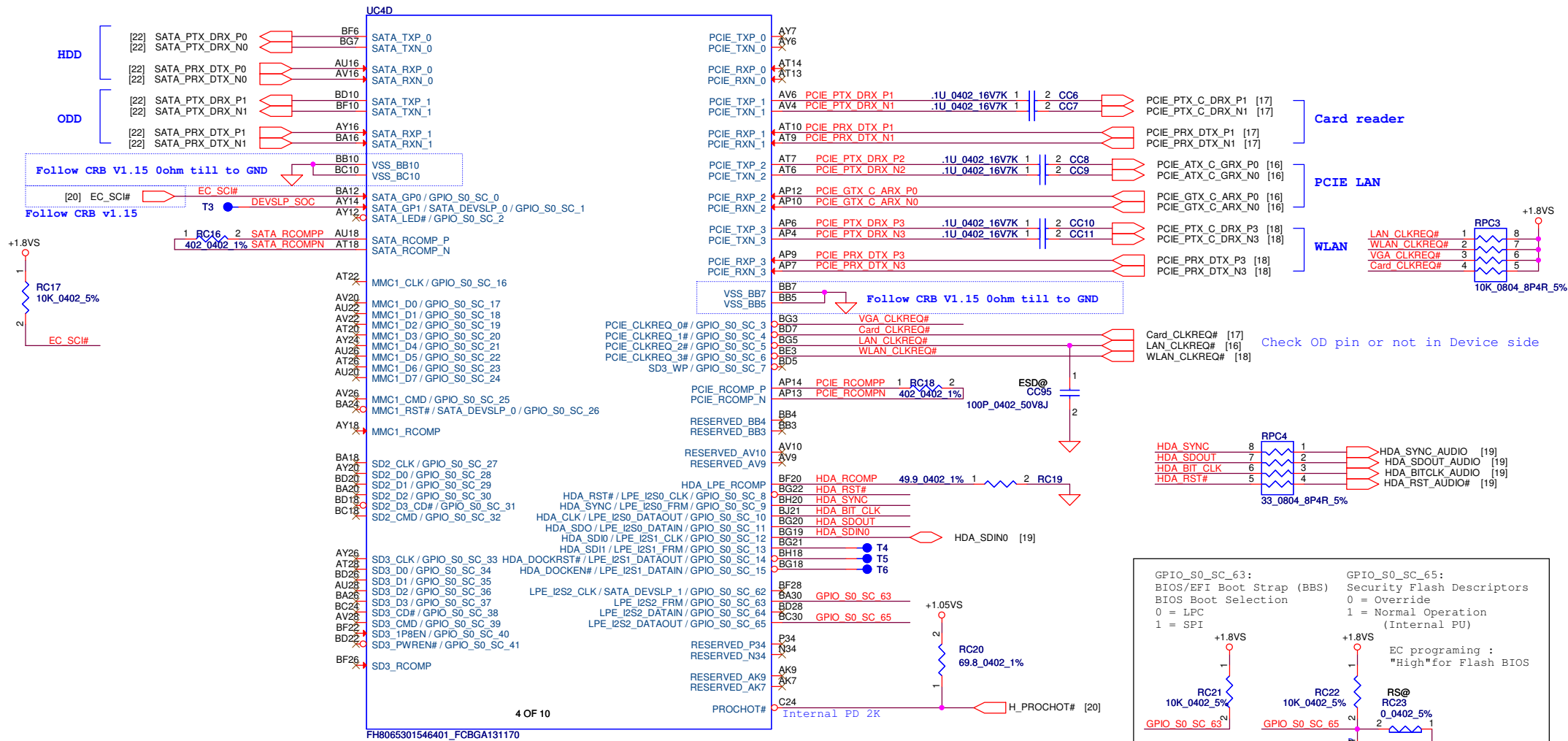
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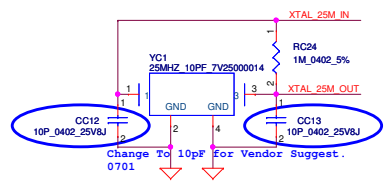
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Issued Date	2014/11/07	Deciphered Date	2015/11/07	VLV-M(1/8) Memory DDR3L
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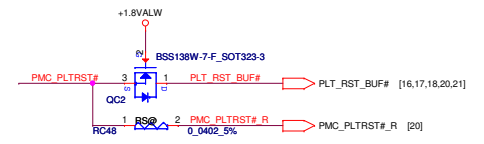
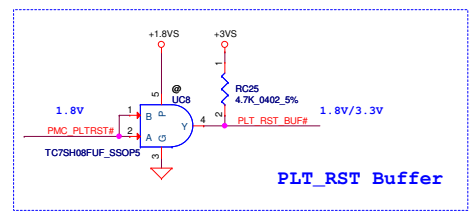
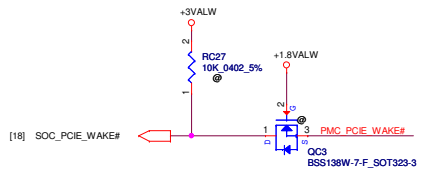
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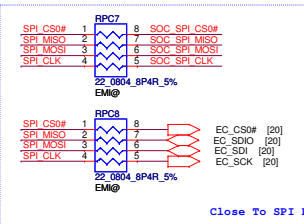
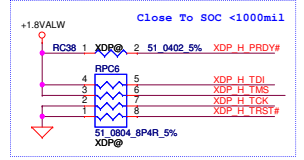
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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Compal Electronics, Inc. VLV-M(3/8) SATA/PCI-E/HDA	
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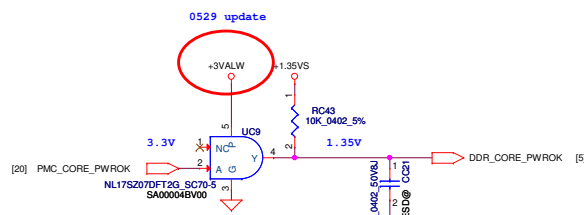
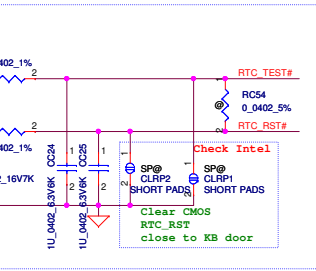
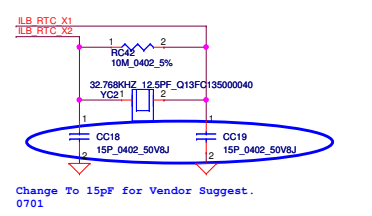
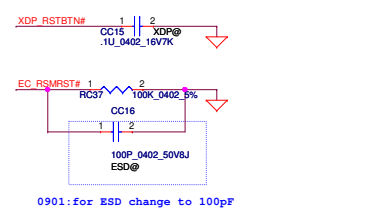
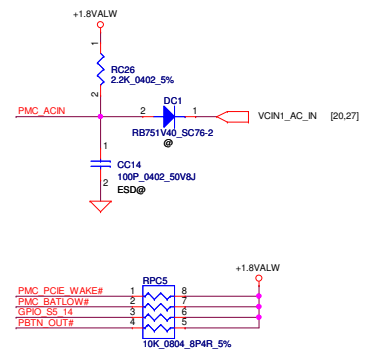
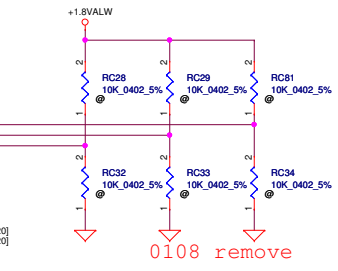
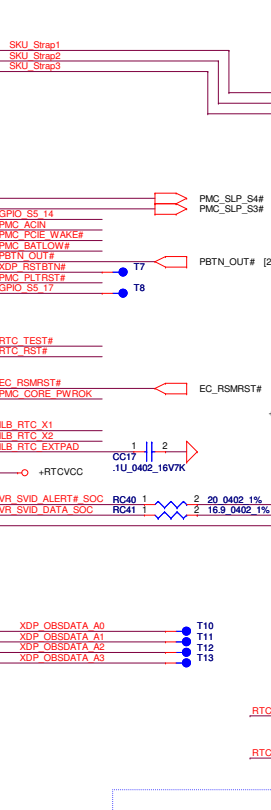
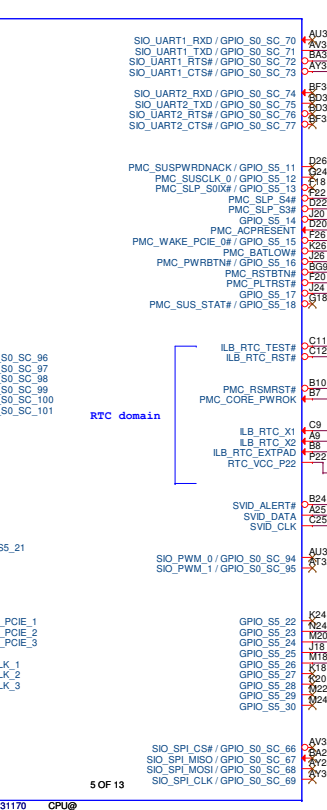
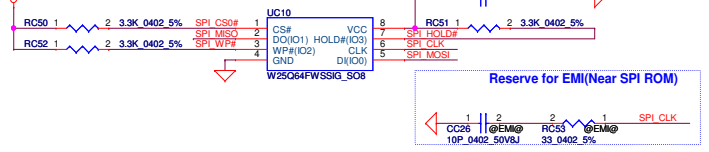
Check power rail



Card
LAN
WLAN



SPIROM (8MByte) 1.8V

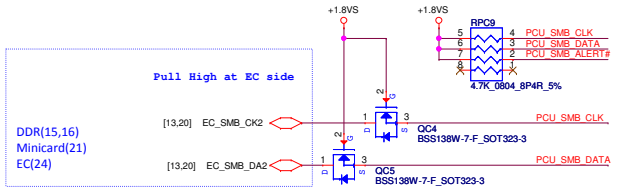
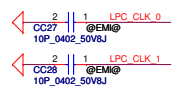
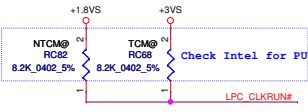


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				VLV-M(4/8) CLK/PMU/SPI/RTC
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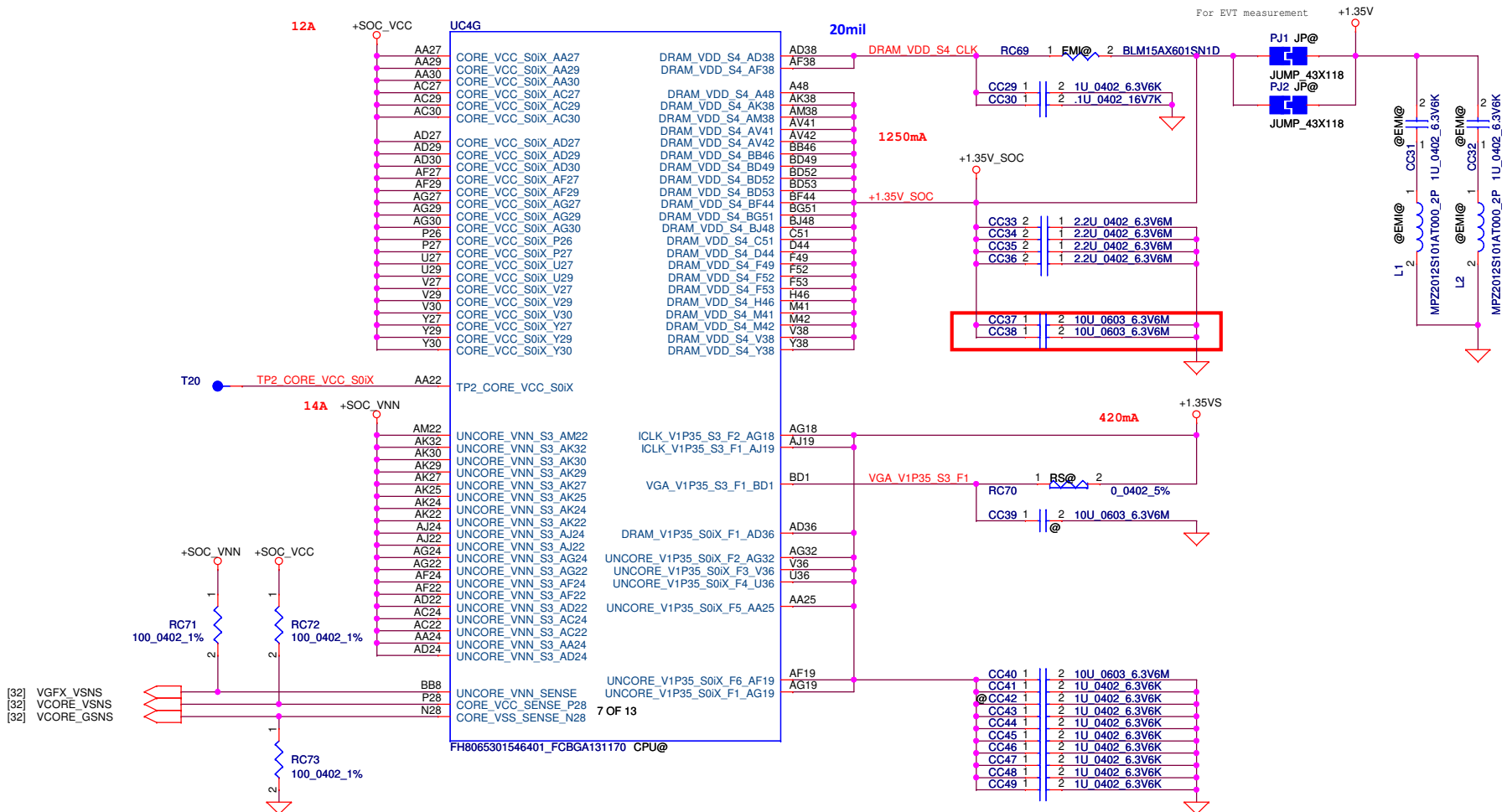


ILB_LPC_CLK_0 : Output of 25MHz, Need Check with EC

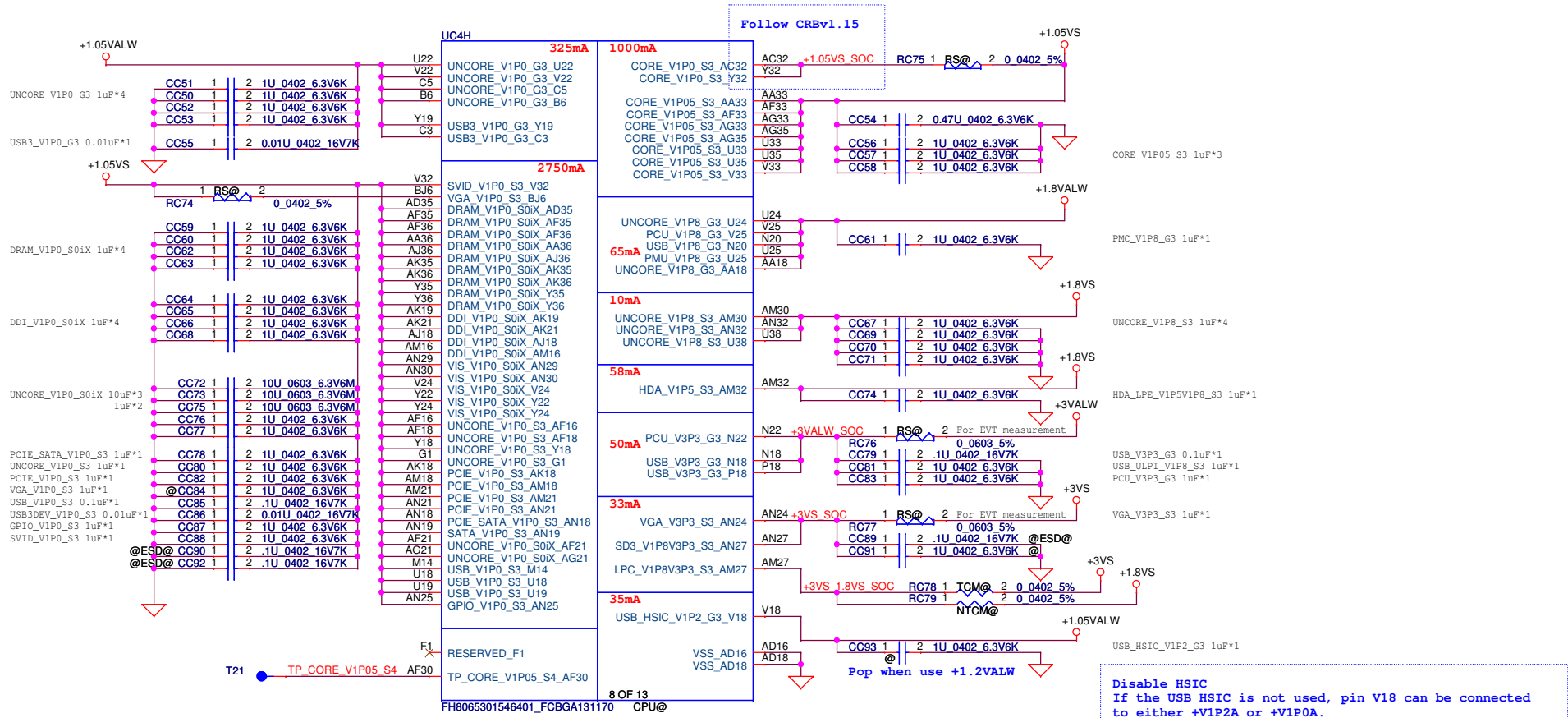
ILB_LPC_CLK_1 is for CLK_0 feedback.(Input) Set to Output for Normal Usage



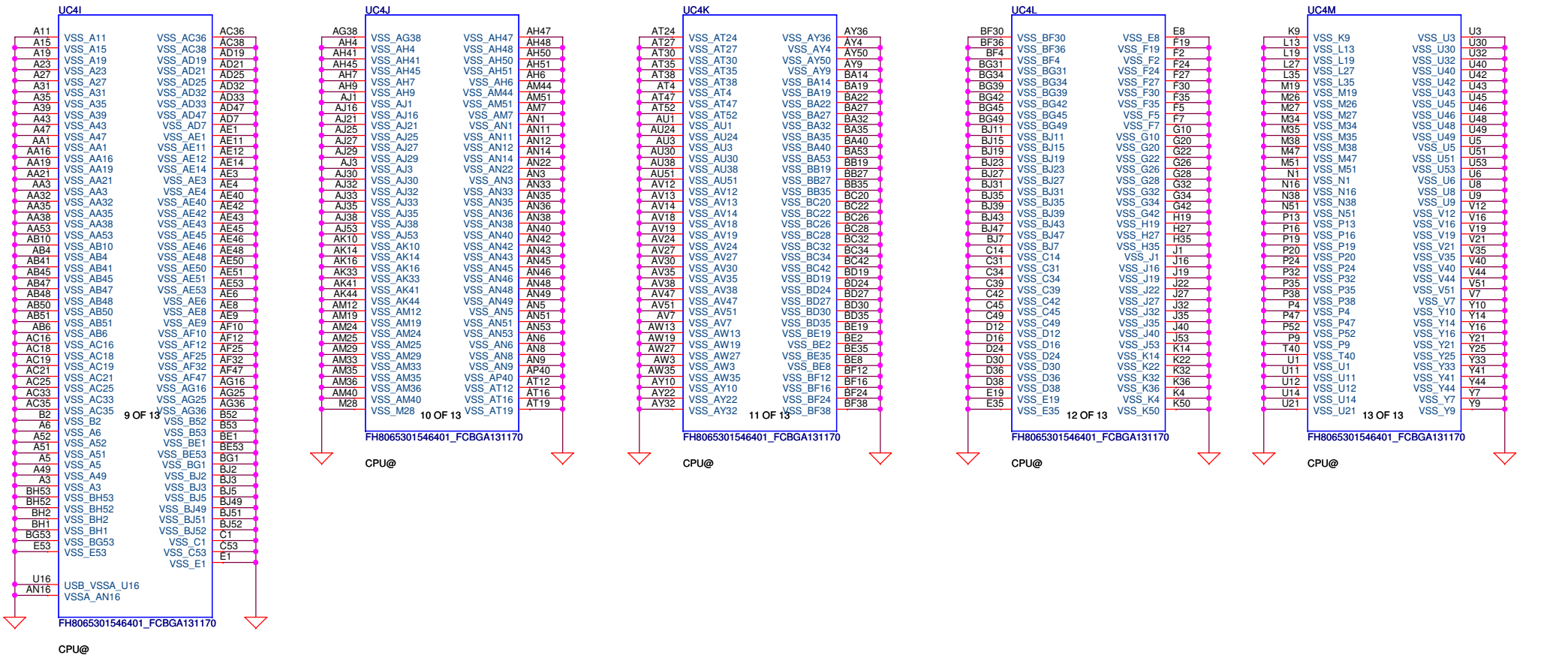
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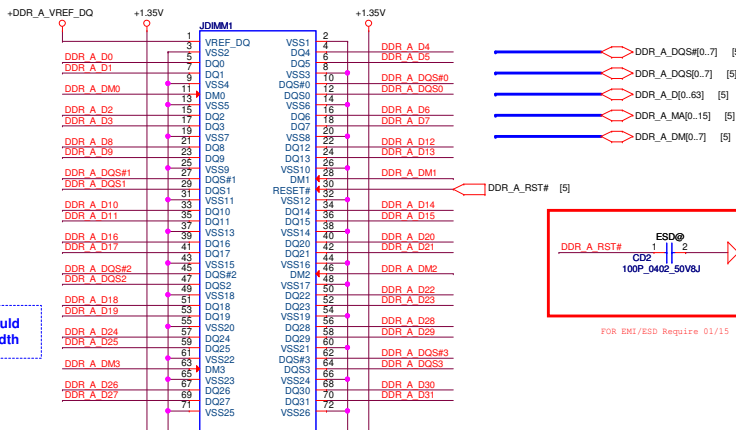
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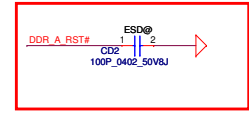
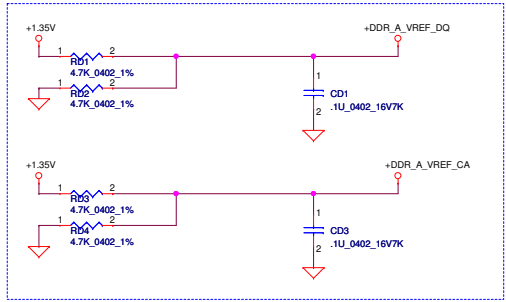
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				VLV-M(8/8) GND	
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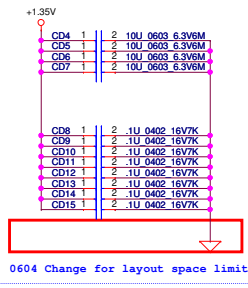
Signal voltage level = 0.675 V
 PLACE TWO 4.7K RESISTORS CLOSE TO
 DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
 Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.



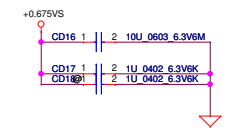
FOR EMI/ESD Require 01/15

Layout Note:
Place near JDIMM1

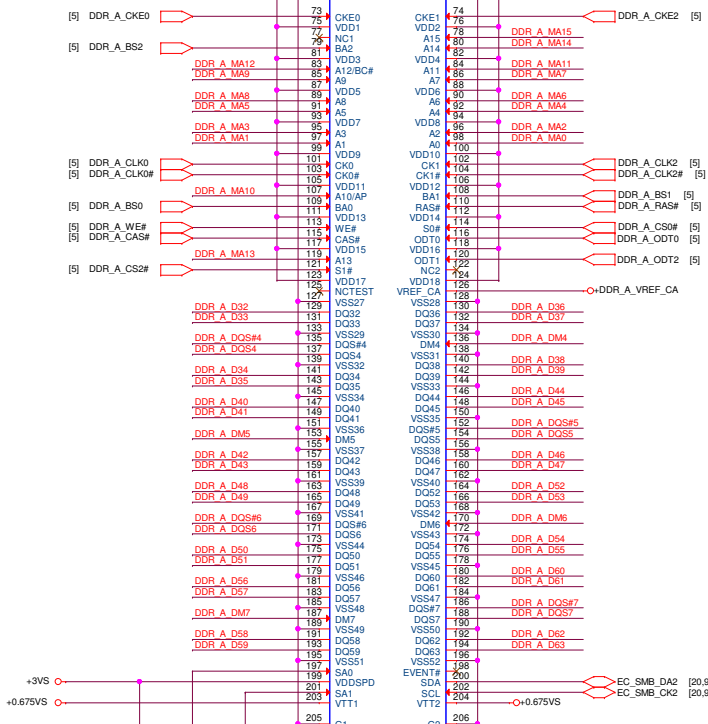
All VREF traces should have 10 mil trace width



0604 Change for layout space limit



Layout Note:
Place near JDIMM1.203,204

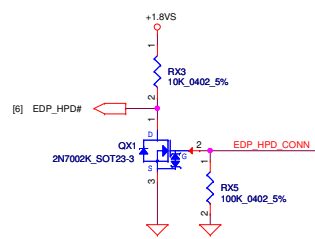
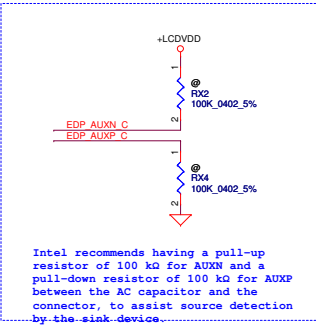
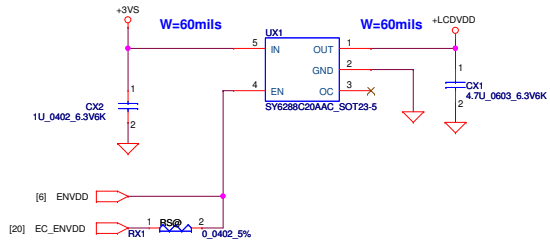


Channel A

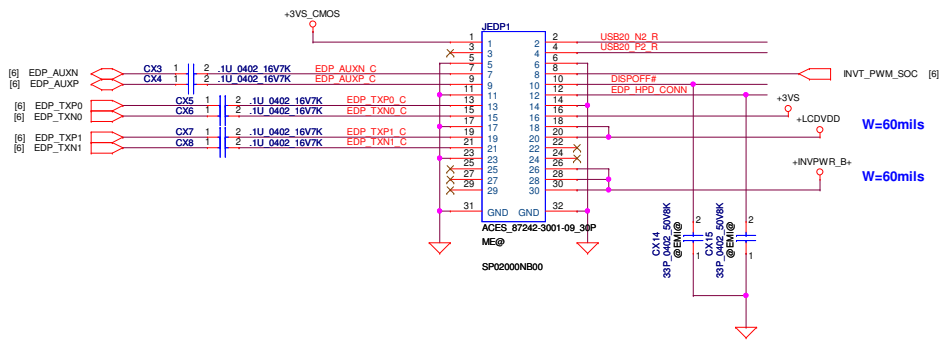
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 DIMM_1 STD H:4mm

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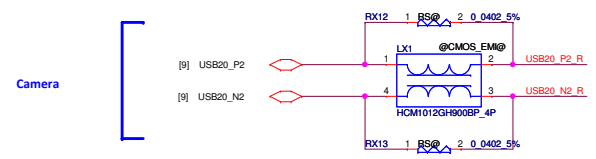
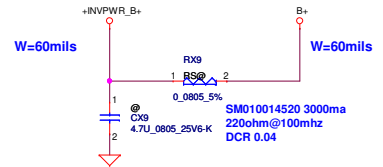
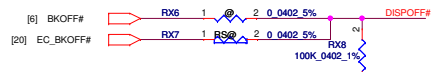
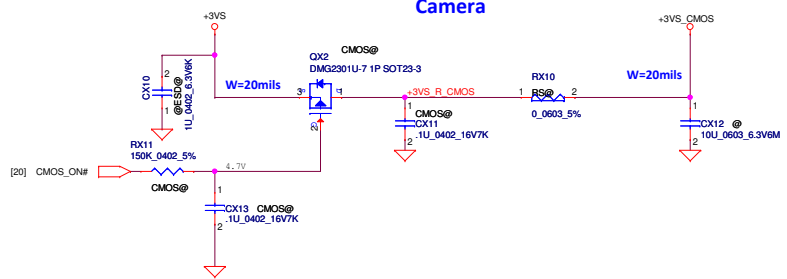
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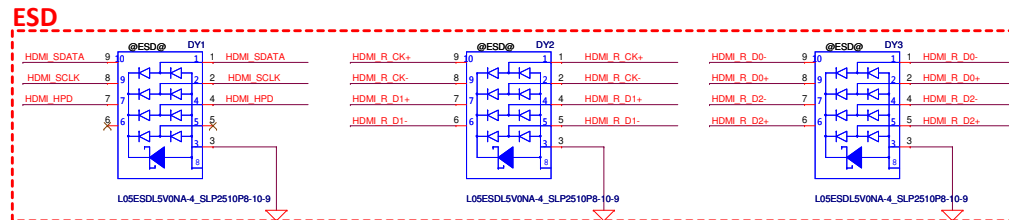
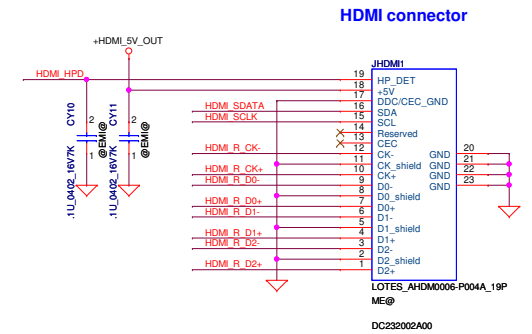
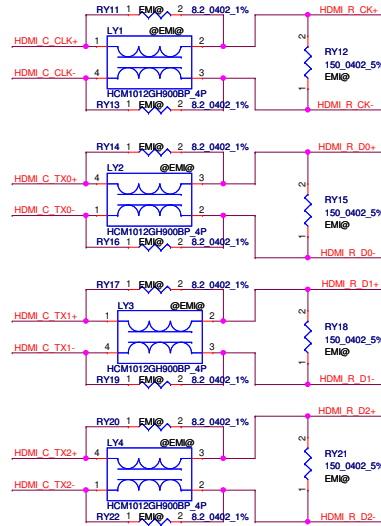
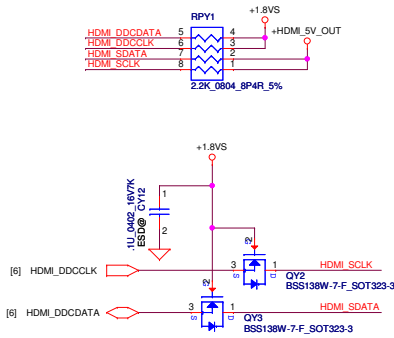
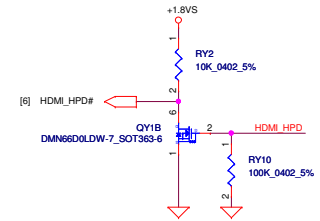
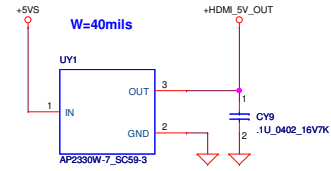
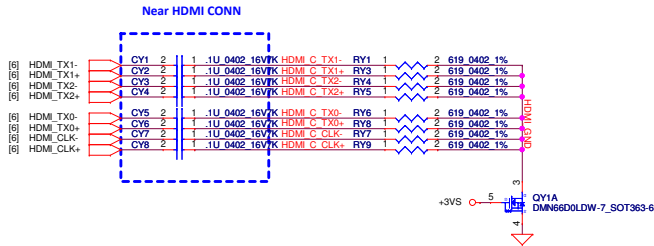
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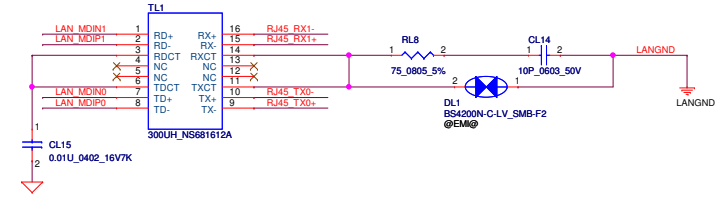
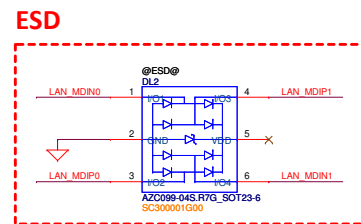
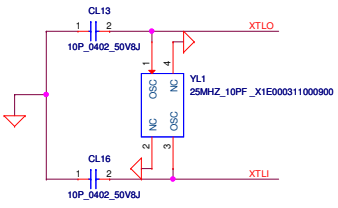
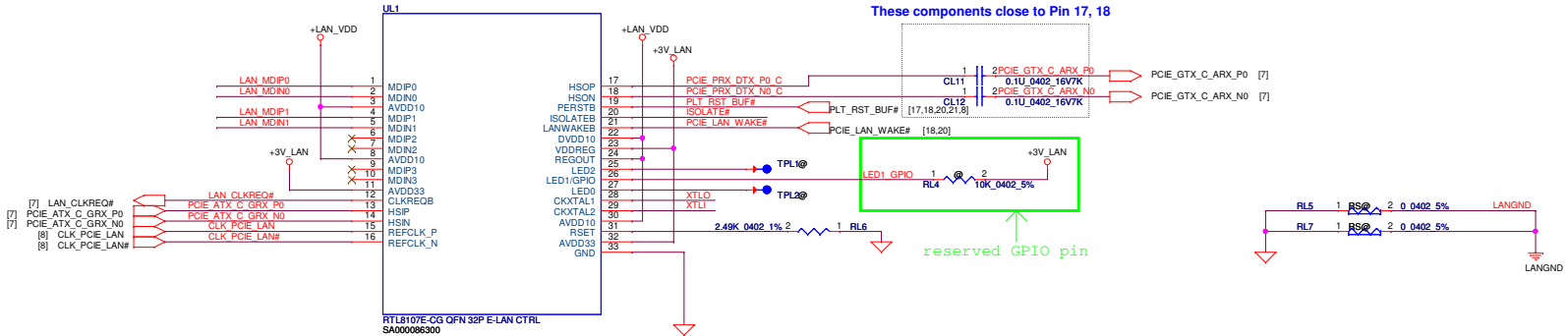
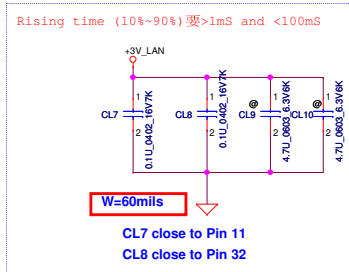
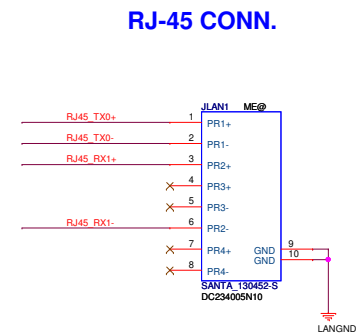
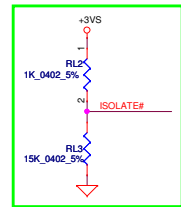
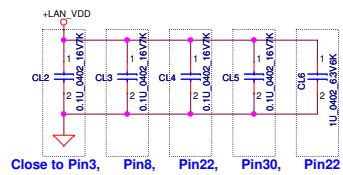
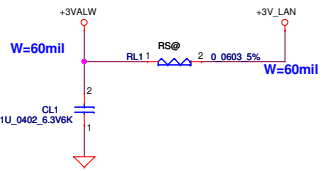
Camera



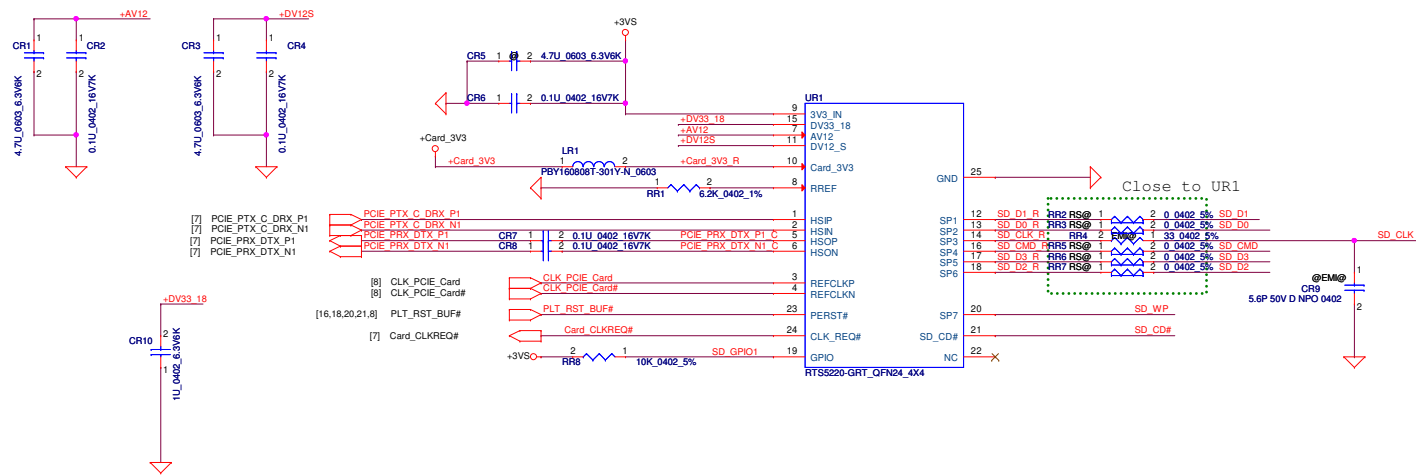
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc. eDP CONN.
Issued Date	2014/11/07	Deciphered Date		
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Document Number	LA-C771P		Rev	0.2
Date:	Wednesday, January 14, 2015		Sheet	14 of 34



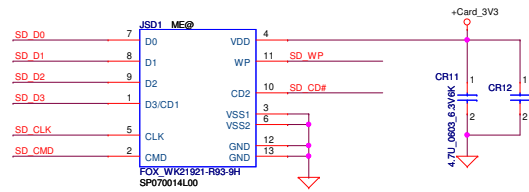
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Issued Date	2014/11/07	Deciphered Date	2015/11/07	HDMI CONN.
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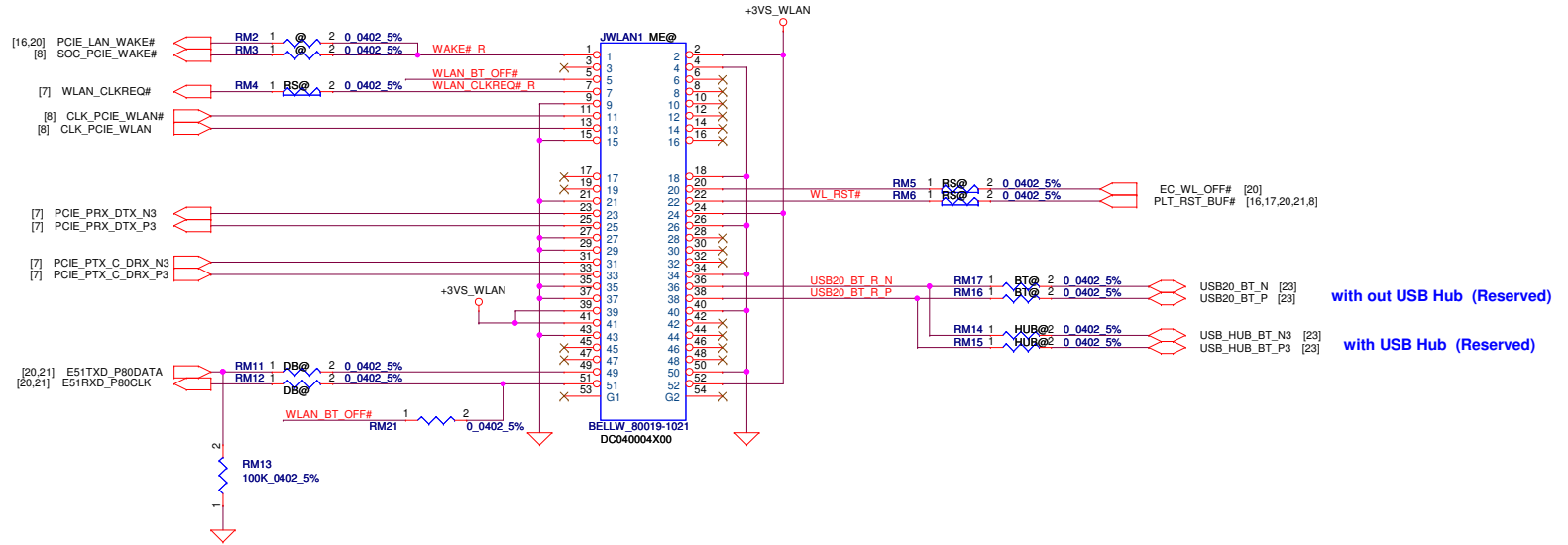
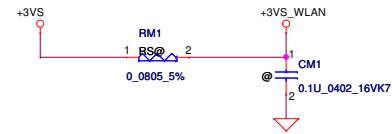
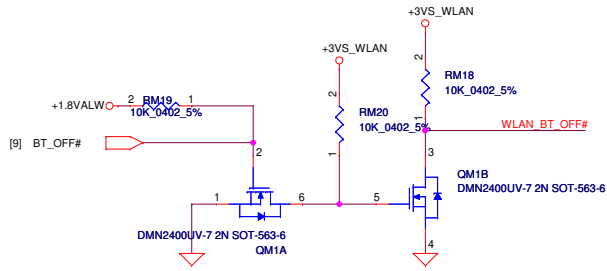
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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Title
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SD/SDXC

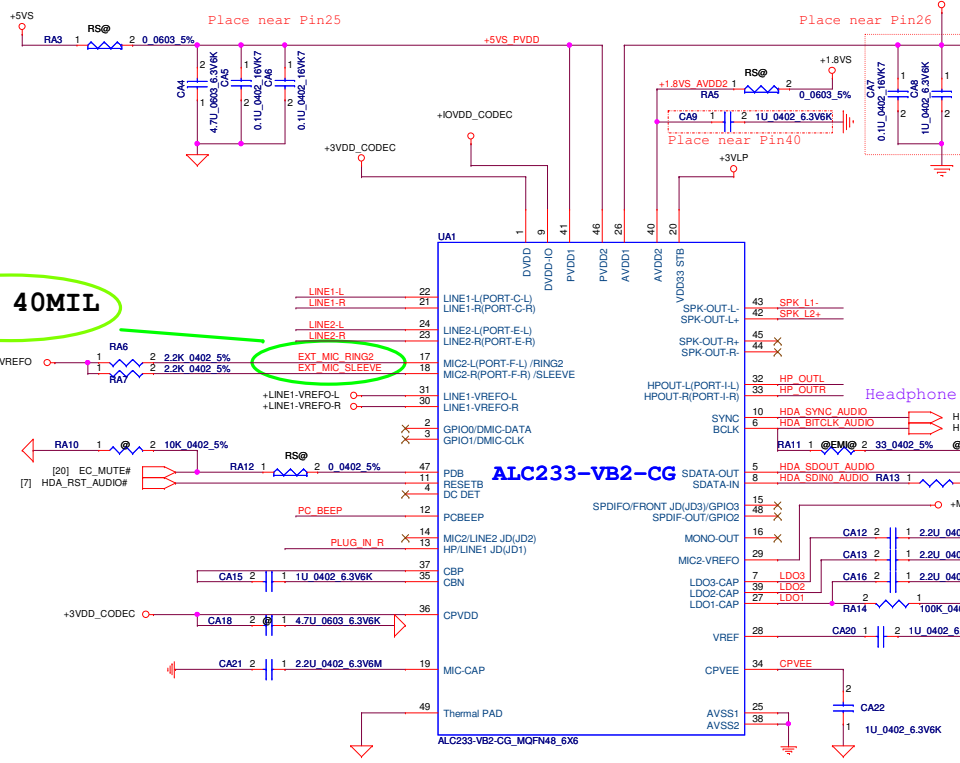


Security Classification	Compal Secret Data		Title Compal Electronics, Inc. Card Reader_RTS5220
Issued Date	2014/11/07	Deciphered Date	
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Date: Wednesday, January 14, 2015			Sheet 17 of 34

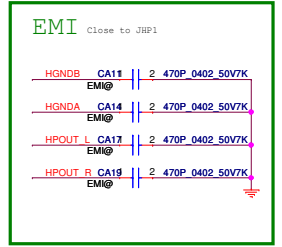
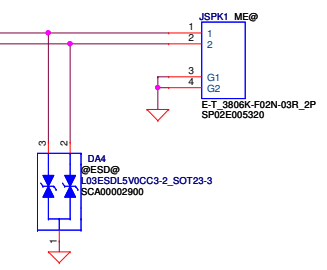
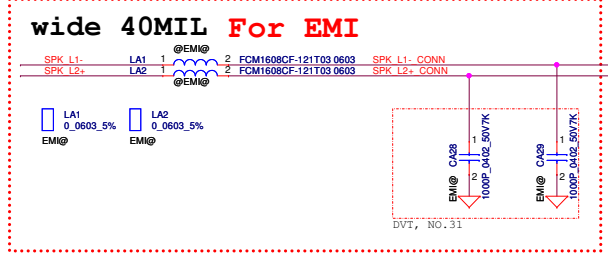
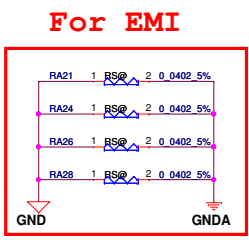
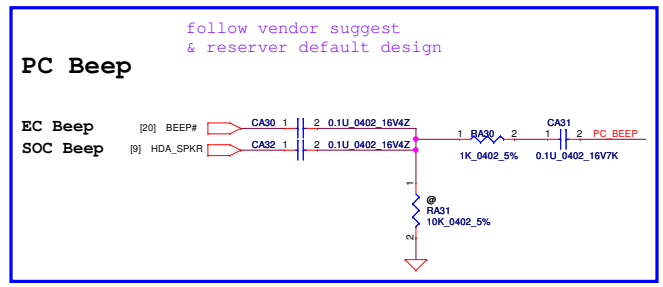
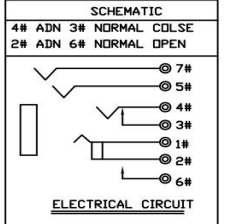
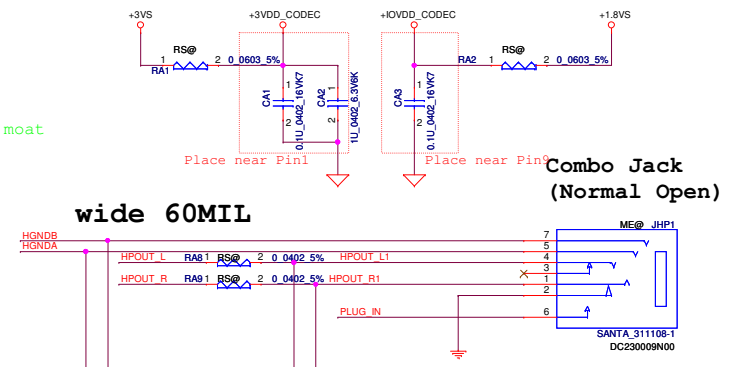


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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Title Mini Card-WLAN	
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600ohms @100MHz 2A
P/N: SM01000E200

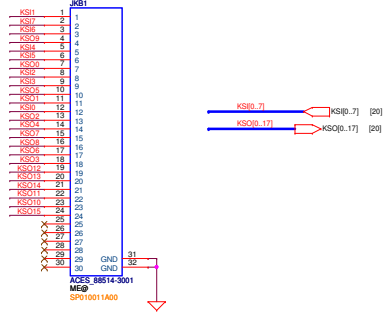


Place RA4 on AGND/DGND moat

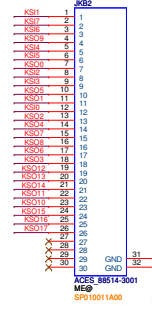


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Issued Date	2014/11/07	Deciphered Date	2015/11/07	Size	Document Number
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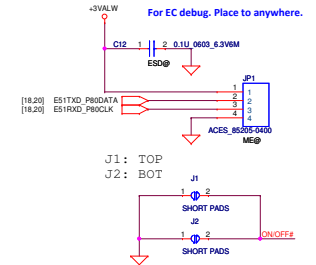
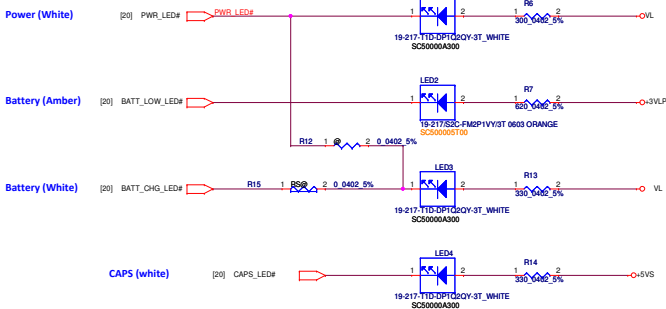
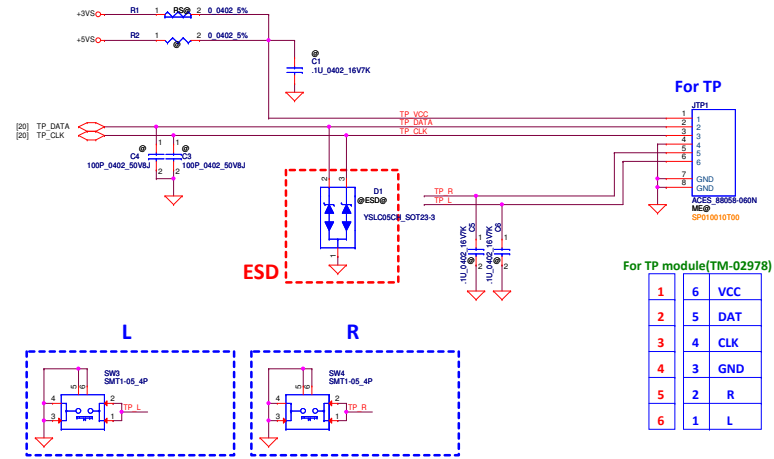
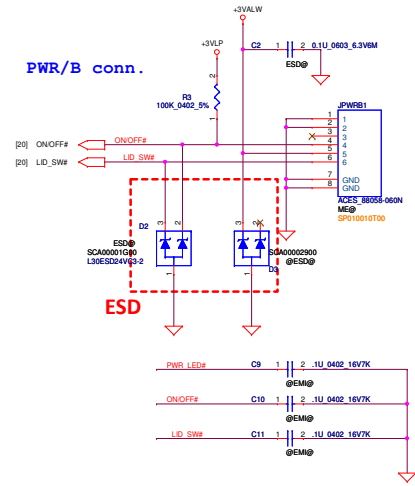
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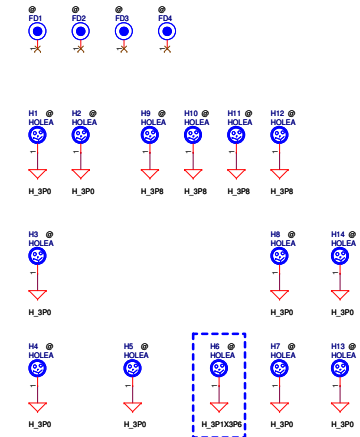
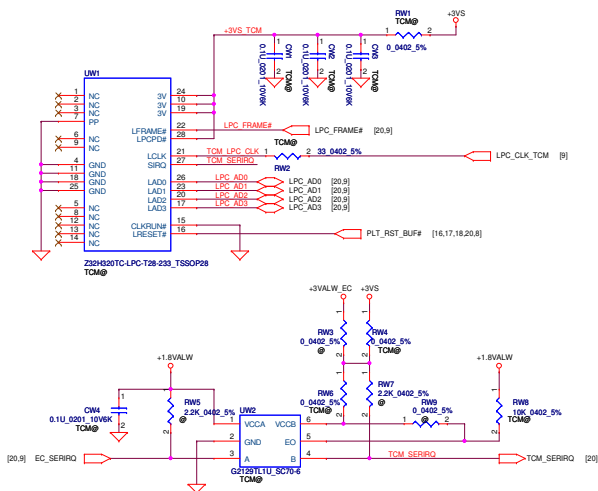
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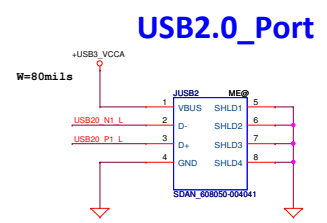
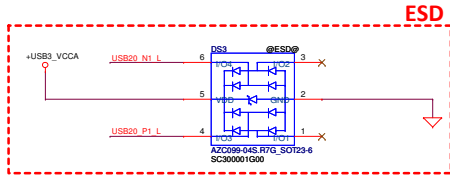
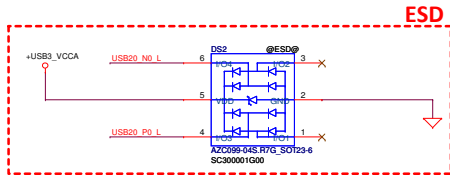
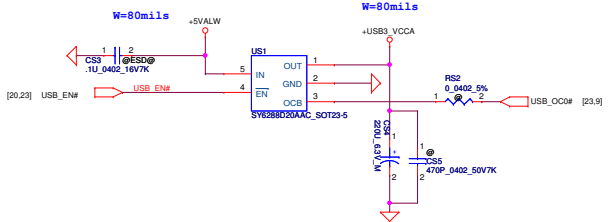
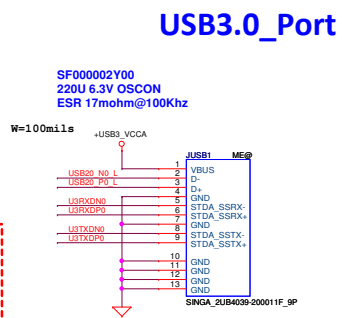
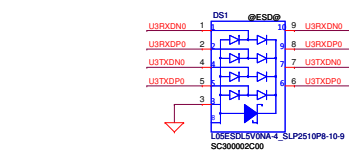
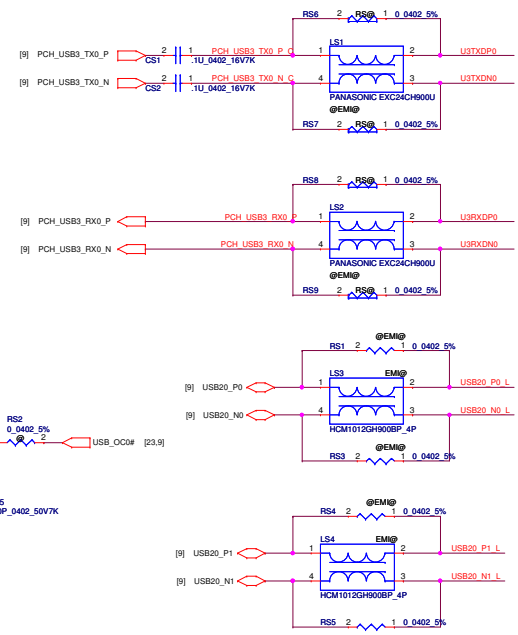
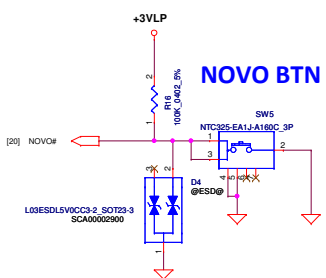
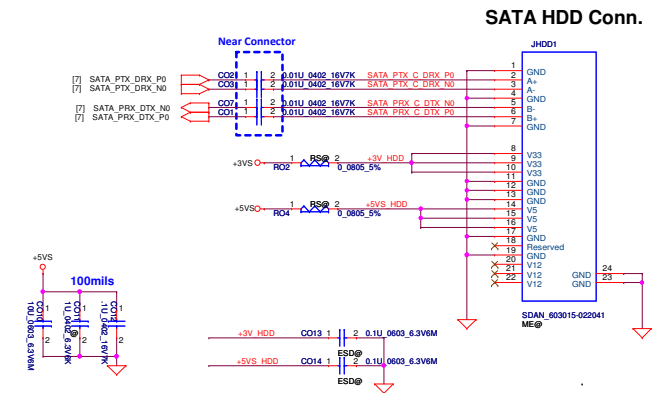
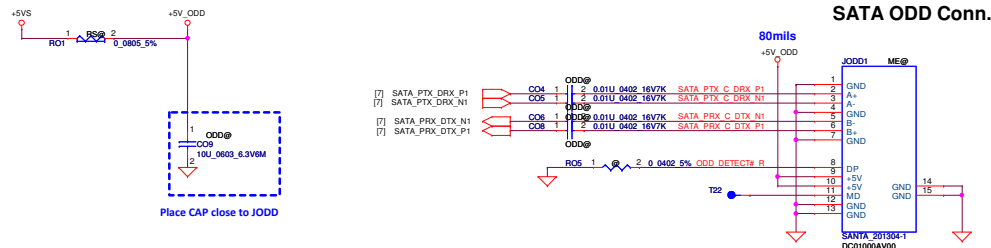


PWR/B conn.

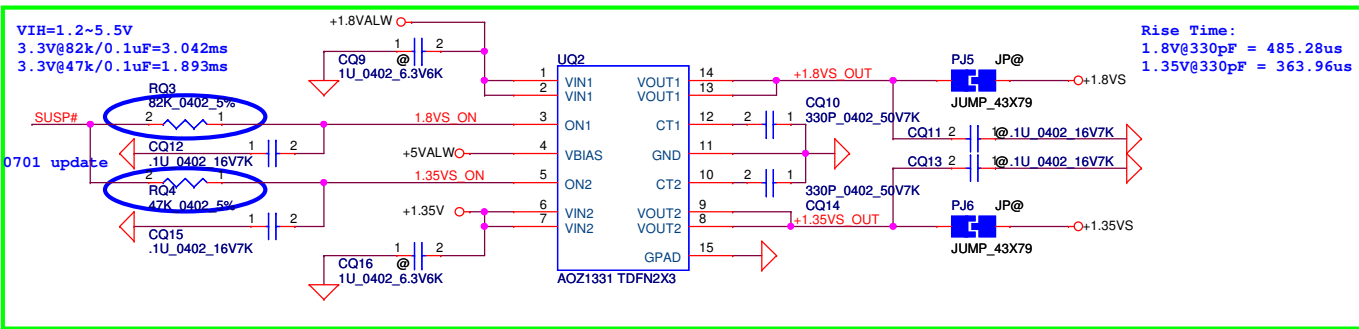
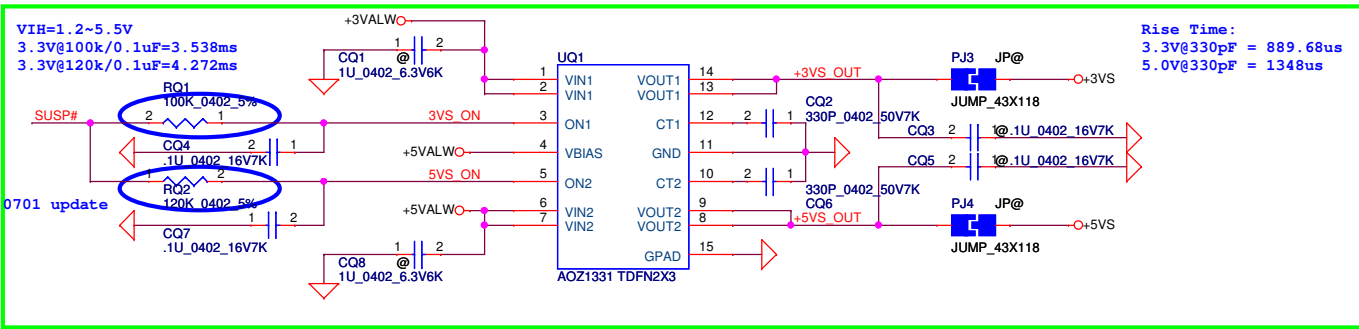


TCM (TPM)

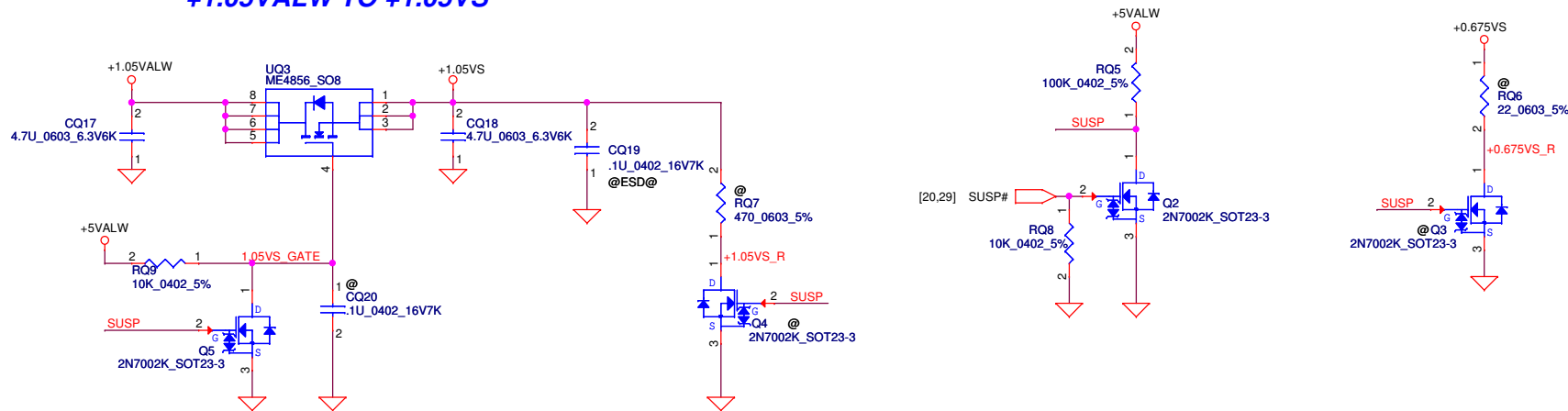




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Issued Date	2014/11/07	Deciphered Date	2015/11/07	HDD/ODD/USB
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Size	Document Number	LA-C771P		Rev
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+1.05VALW TO +1.05VS

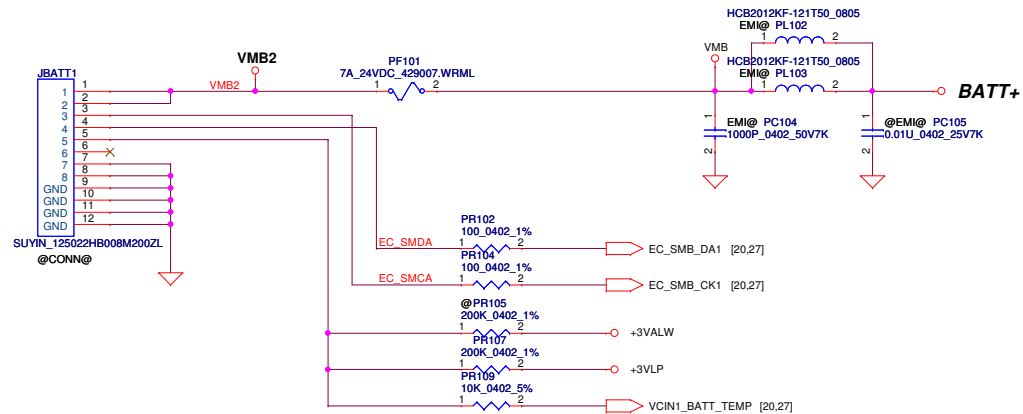
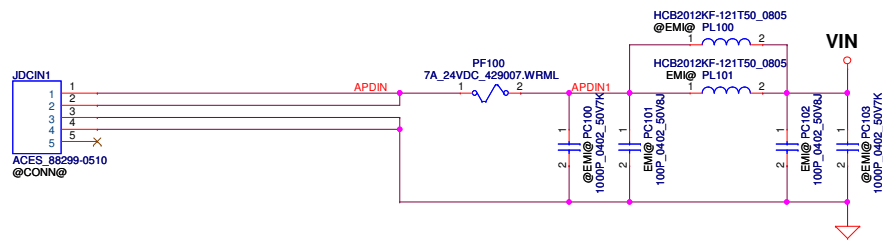


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Date:	Wednesday, January 14, 2015	Sheet	24 of 34	Rev 0.2
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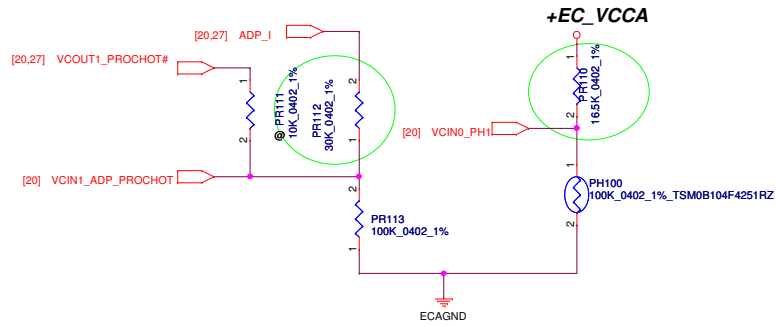
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	22	HW	2014/11/18	COMPAL	added NOVO BTN function	SW5, R16 connected to EC for NOVO function	0.1
2	18	HW	2014/11/19	COMPAL	reserver level shift for BT	Reserver QM1, RM18, Rm19and RM20 for BT level shift	0.1
3	9	HW	2014/11/19	COMPAL	added TCM, NTCM BOM option	added RC82 reserve for LPC_CLKRUN# PU 1.8VS	0.1
4	21	HW	2014/11/19	COMPAL	Move the hall sensor to power S/B	remove hall sensor circiut	0.1
5	8, 20	HW	2014/11/21	COMPAL	reserver EC clean CMOS	reserver QB1, RB31, RC83, and RC84	0.1
6	14	EMI	2014/11/24	COMPAL	for EMI request	reserver CX14 and CX15	0.1
7	20	HW	2014/11/25	COMPAL	EC vendor implement	Added NUVOTON_VIT RB32 PD	0.1
8	23	HW	2014/11/25	COMPAL	Reserve USB 2.0 HUB for external USB CONN	Added page 23 for USB 2.0 HUB	0.1
9	20	EC	2014/11/25	COMPAL	Change and remove EC pin define	PMC_SLP_S3# 97 pin -> 106 pin Remove PCIE_LAN_WAKE# 123 pin -> 19 pin BRDID EC_SLP_S4# 89 pin -> 123 pin EC_SW_OFF# VR_ON 121 pin -> 108 pin HDD_DETECT# SOC_ERVDD? 1 pin -> 121 pin EC_LID_OUT# EC_ERVDD? 76 pin -> 74 pin VDATE 16 pin -> 21 pin SOC_EMBKL 18 pin -> 97 pin	0.1
10	23	HW	2014/11/27	COMPAL	Change USB S/B from 2 port to lport	Change JSB1	0.1
11	22	EMC	2014/11/28	COMPAL	Reserve ESD diode	Reserve D4 and DA5	0.1
12	19	HW	2014/12/01	COMPAL	for Audio vendor review change	change RA27 form 4.7K to 2.2K	0.1
13	20	HW	2014/12/01	COMPAL	Reserver Smbus resistor from CPU to EC	Reserve RB16 and RB17	0.1
14	21	HW	2014/12/02	COMPAL	Change LED form green to white	Change LED1, LED2, and LED3 form SC590KGK020 to SC50000A300, and change R6 from 100 to 300 ohm	0.1
15	23	HW	2014/12/02	COMPAL	Reserve USB power switch for S/B on M/B side	Reserve US3, CS13, CS14, CS6 and RS20	0.1
16	18	HW	2014/12/03	COMPAL	For support BT funciton WLAN card	Add RM21 for support BT WLAN CARD, reserve RM11, RM12, RM13 for debug	0.1
17	21	HW	2014/12/22	COMPAL	JTP1 pin swap for Tp module imformation error	Swap JTP1 pin define	0.2
18	16, 22	EMI	2014/12/22	COMPAL	For EMI requested	Change DL1, LS1 and LS2 Bom structure from EMI@ to @EMI@ and chage R56, RS7, R58, and RS9 from @EMI@ to EMI@	0.2
19	23	HW	2014/12/22	COMPAL	BT function fail, pin connected error	Swap USB20_BT_P & USB20_BT_N	0.2
20	15	HW	2014/12/22	COMPAL	HDMI function fail, pin connected error	Swap HDMI_R_CK- & HDMI_R_CK+, HDMI_R_D1+ & HDMI_R_D1-	0.2
21	22, 23	HW	2014/12/24	COMPAL	ME Z-high interfere	Change CS4, CS14 from SF000006900 to SF000006R00	0.2
22		HW	2014/12/24	COMPAL	change o ohm to short pad	change RX9, RX10, RL1, RML, RA3, RA4, RA1, RA2, RA5, RB7, RB4, RC1, RC4, RC7, RC77, RC48, RC70, RC74, RC80 to short pad	0.2
23		EMI	2015/01/05	COMPAL	change o ohm to short pad for EMI requested	change RK12, RK13, RL5, RL7, RA21, RA24, RA26, RA28, RS6, RS7, RS8, RS9 to short pad	0.2
24	15	EMI	2015/01/05	COMPAL	change BOM structure	Change LY1, LY2, LY3 and LY4 BOM structure form EMI@ to @EMI@ Change RV12, RV15, RV18, and RV21 form @EMI@ to EMI@ Change RV11, RV13, RV14, RV16, RV17, RV19, RV20, RV22 form 0 ohm @EMI@ to 8.2 ohm EMI@	0.2
25	5, 7	ESD	2015/01/05	COMPAL	add ESD cap for ESD requested	Add CC20, CC94, CC95 and change CD2 form 0.1U to 100P for ESD	0.2
26	8	HW	2015/01/07	COMPAL	prevent the power leakage issue.	Chaneg RC29 and RC33 bom structure form 14@ to @	0.2
27	20	HW	2015/01/09	COMPAL	prevent the antenna effect	Add CB13, CB14 0.1u 0402	0.2
28	22	DFB	2015/01/10	COMPAL	add test point for DFB requested	Add T22 (JODD1.11)	0.2
29	21	HW	2015/01/14	COMPAL	add screw hole conneted to GND	add H13, H14 conneted to GND	0.2

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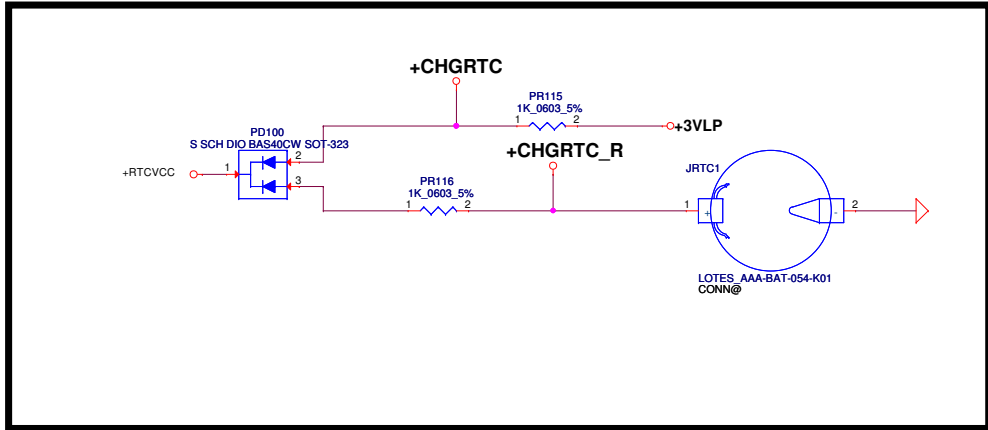


PH7 under CPU bottom side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C

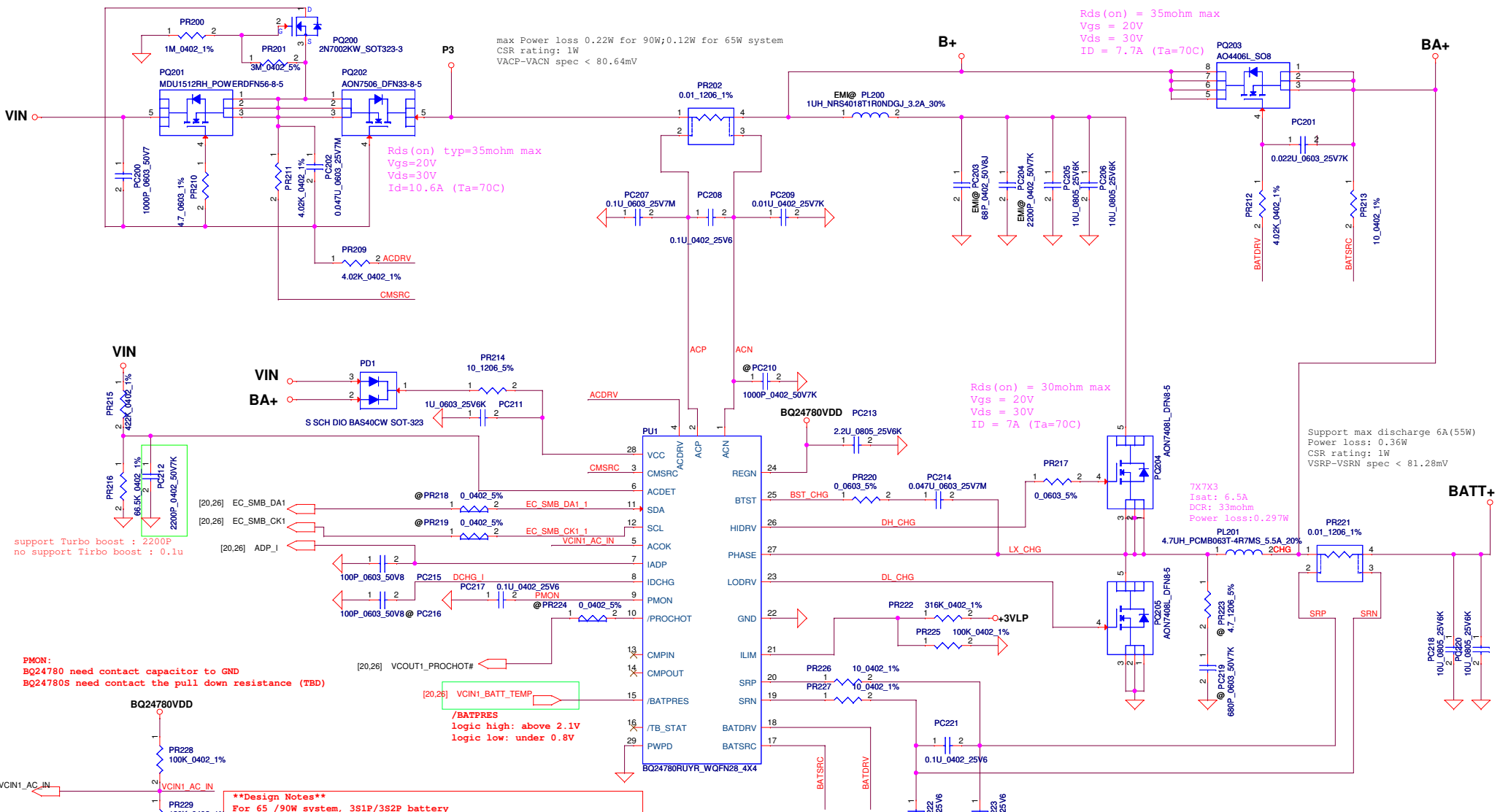


VCIN1 setting
Trigger point is 1.0V at 65W
Recovery point is 0.692V at 45W

RTC



	ADP_SET1	ADP_SET2
45W adapter	0	0
60W adapter	1	0
90W adapter	0	1
135W adapter	1	1



max Power loss 0.22W for 90W;0.12W for 65W system
 CSR rating: 1W
 VACP-VACN spec < 80.64mV

Rds(on) = 35mohm max
 Vgs = 20V
 Vds = 30V
 ID = 7.7A (Ta=70C)

Rds(on) typ=35mohm max
 Vgs=20V
 Vds=30V
 Id=10.6A (Ta=70C)

Rds(on) = 30mohm max
 Vgs = 20V
 Vds = 30V
 ID = 7A (Ta=70C)

Support max discharge 6A(55W)
 Power loss: 0.36W
 CSR rating: 1W
 VSRP-VSRN spec < 81.28mV

support Turbo boost : 2200P
 no support Tirbo boost : 0.1u

PMON:
 BQ24780 need contact capacitor to GND
 BQ24780S need contact the pull down resistance (TBD)

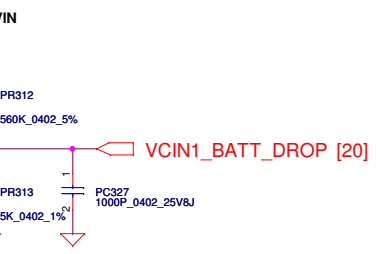
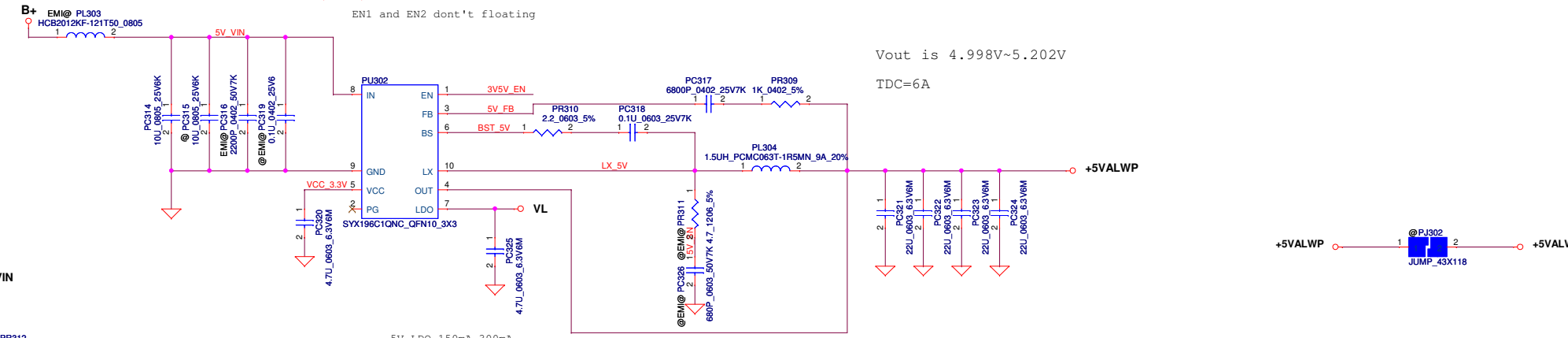
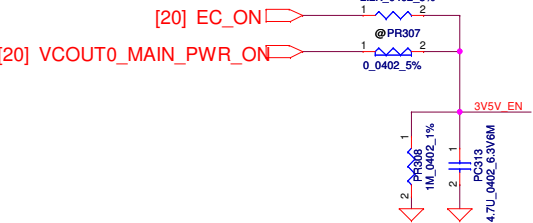
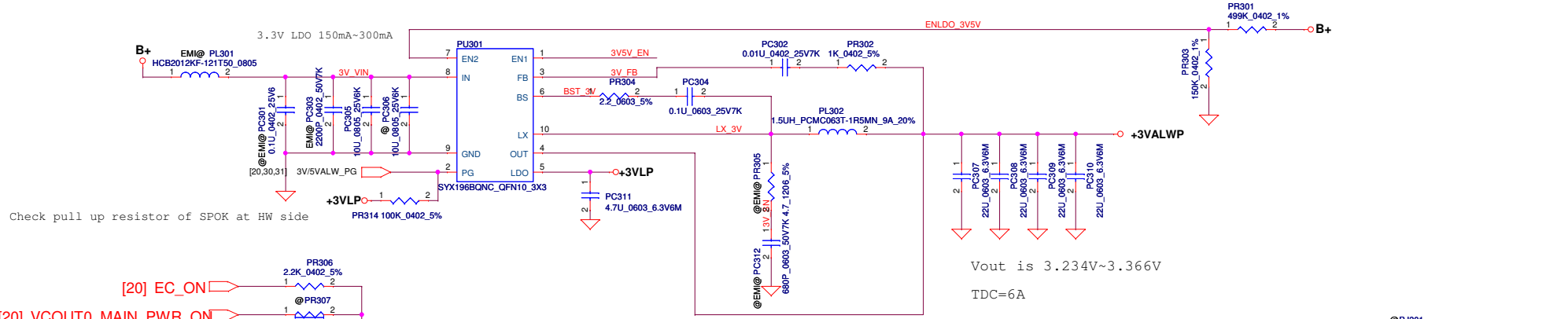
VCIN1_BATT_TEMP
 /BATPRES
 logic high: above 2.1V
 logic low: under 0.8V

****Design Notes****
 For 65 /90W system, 3S1P/3S2P battery
 Maximum Charging current 3A
 Maximum Battery discharge power 55W
 #Register Setting
 1. 0X12 bit2 set 1 (default 0) to enable turbo boost function
 2. Disable turbo when AC only
 #Circuit Design
 1. ILIM pull high voltage base on 3/5V enable control
 2. Use 7X7 choke and 3X3 H/L side MOSFET
 Charge current 3A
 Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)
 Power density : 0.61 (23X16)
 #Protect function
 1. ACOVP : VCC voltage > 24V
 2. Charger timeout : No communication within 175s(default)
 3. ACOC : 3.33 X Input current DAC setting (default:Disable)
 4. CHGOCP : based on charge current setting
 5. BATOVP : 103-106%
 6. BATLOWV : 2.6V
 7. TSHUT : 155C
 8. IFAULT HI : 750mV (default:Disable)
 9. IFAULT LOW : 230mV (default)

Module model information
 BQ24780_V1.mdd for dual layer

Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

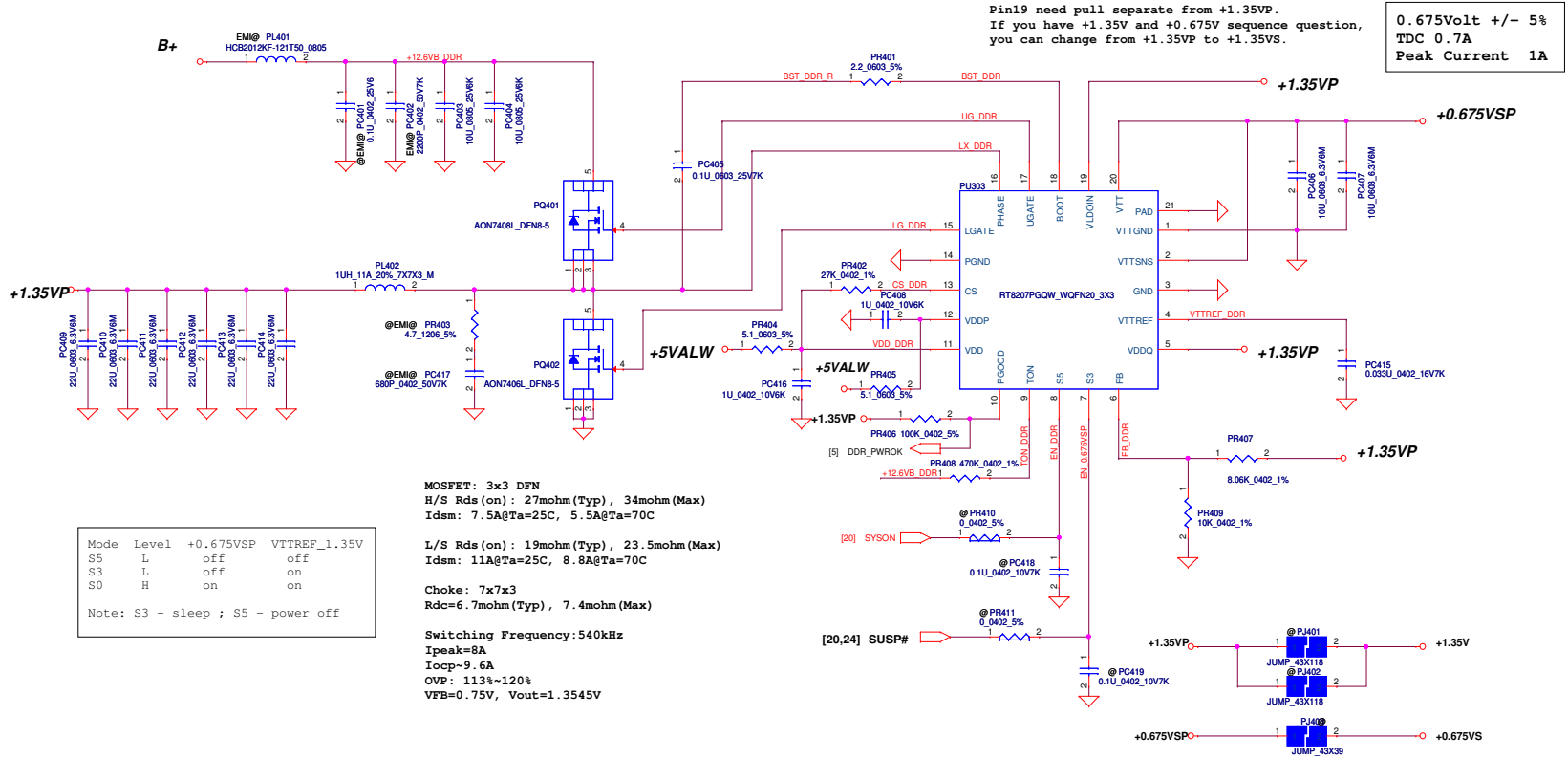
VILIM = 20*ILIM*Rsr
 ILIM = 3.3*100/(316+100)/20/0.01 = 3.966 A



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Bay Trail M LA-C771P +3VALW/+5VALW				Date: Thursday, January 15, 2015 Sheet 28 of 28

Module model information

RT8207P_V1.mdd For Single layer
RT8207P_V2.mdd For Dual layer



0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

MOSFET: 3x3 DFN
H/S Rds (on): 27mohm (Typ), 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

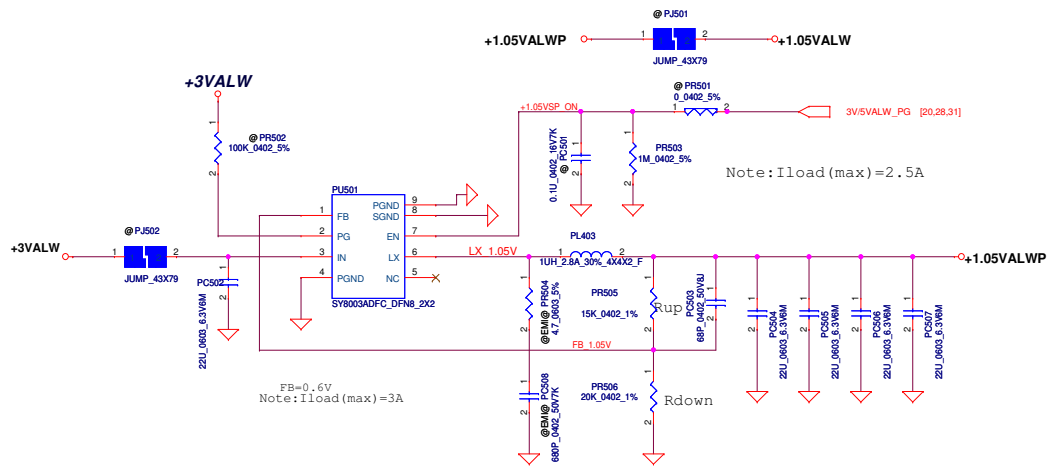
L/S Rds (on): 19mohm (Typ), 23.5mohm (Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

Choke: 7x7x3
Rdc=6.7mohm (Typ), 7.4mohm (Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

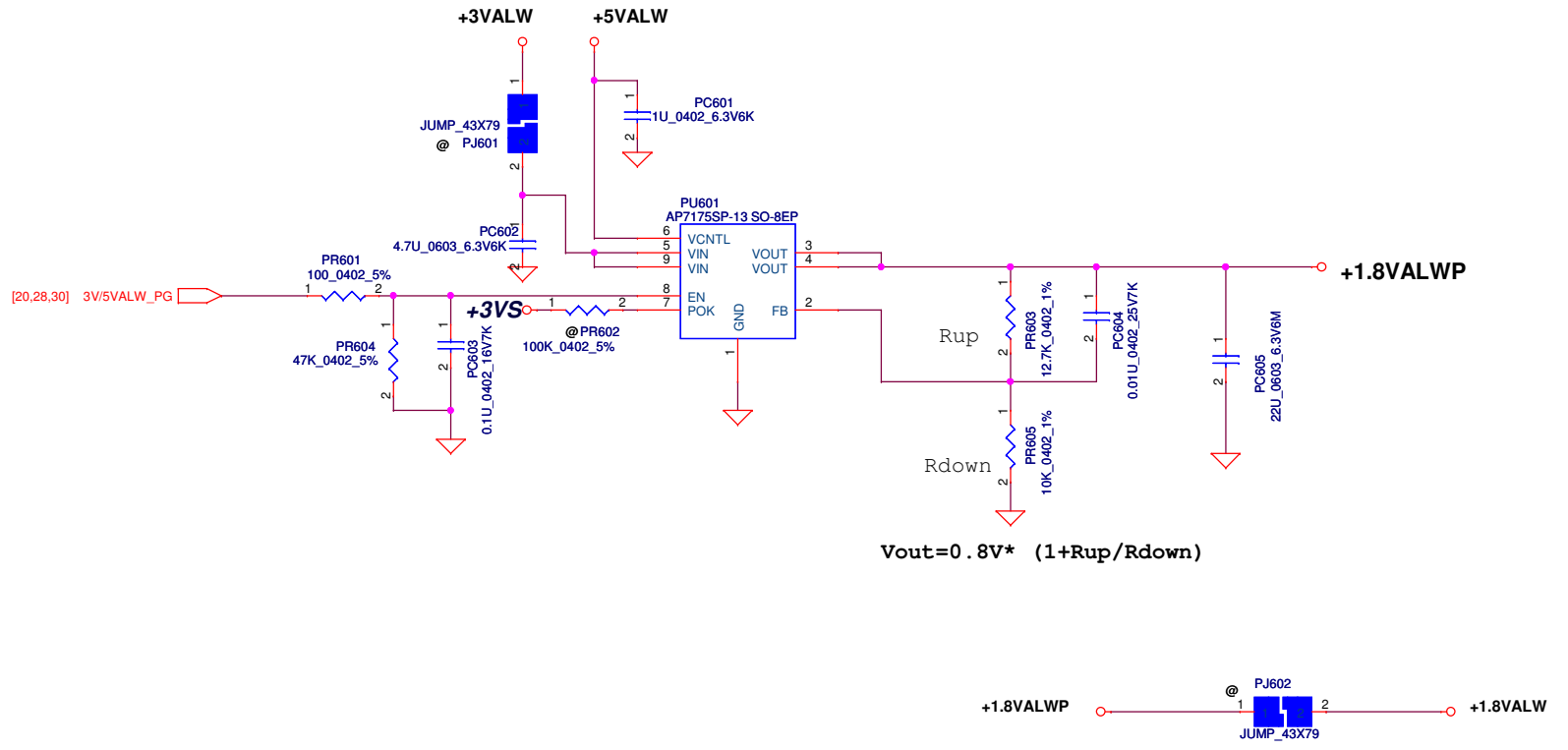
Note: S3 - sleep ; S5 - power off



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Module model information
 ISL95833-BTM_V1A.mdd for IC portion
 ISL95833-BTM_V1B.mdd for SW portion

Design for BT-M 4.5W CPU

PR15 and PR27
 27.4K ohm for 100 degree
 61.9K ohm for 110 degree

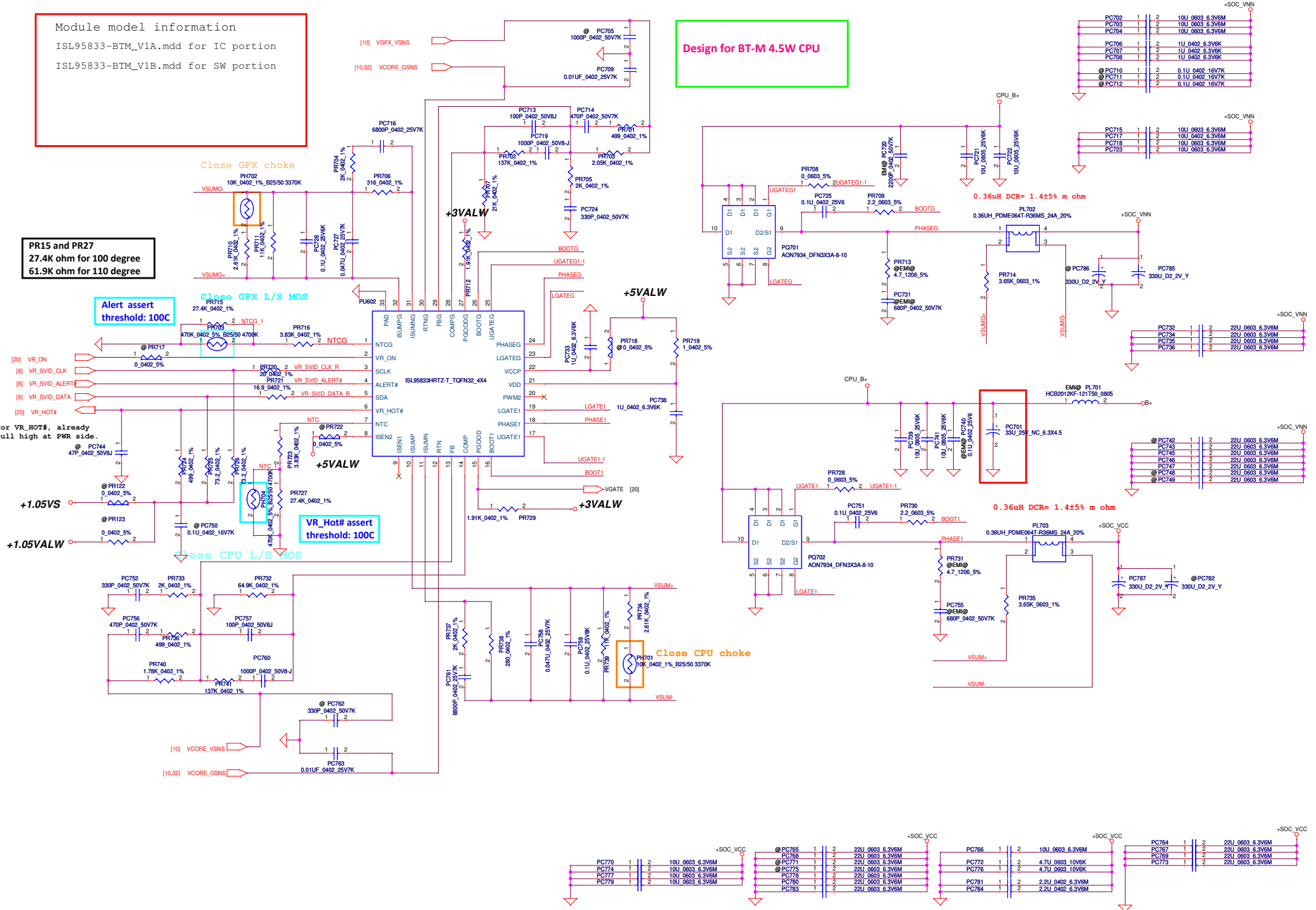
Alert assert
 threshold: 100C

Close GFX L/S MOS

VR_Hot# assert
 threshold: 100C

Close CPU L/S MOS

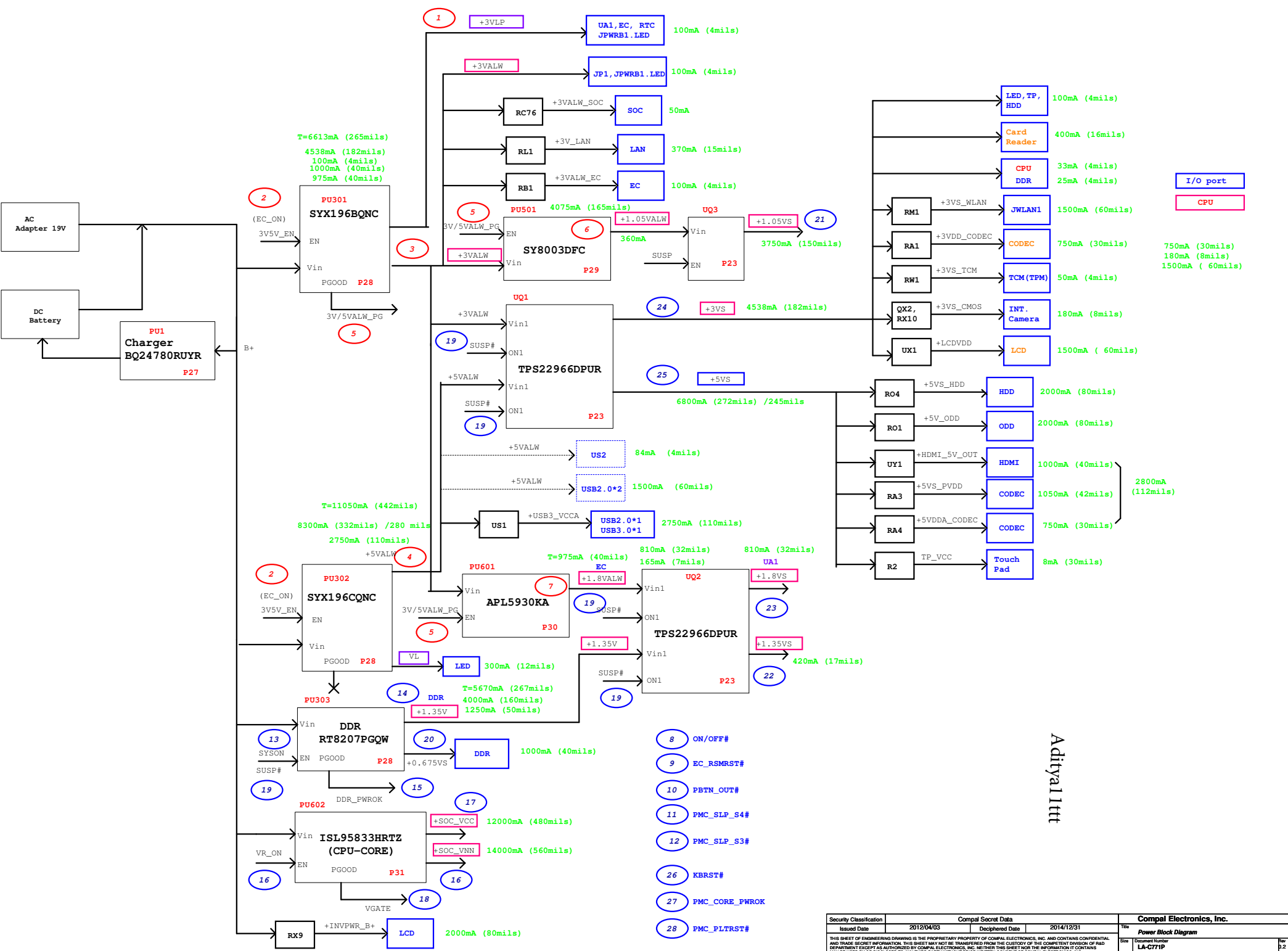
Close CPU choke



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	PR601_0_0402 change PR601_100_0402	31	HW 需求		SIT
2	修正PC207 fromluF to 0.1uF · 修正PC209 from 0.1u to 0.01uF	27	線路修正		SIT
3	pc203改EMI@上件	27	EMI 需求		SIT
4	inpop cap from PC785 to PC786	32	ME 需求		SIT
5	change PR410,PR411,PR501,PR218,PR219,PR224 to short pad	27,29,30	HW 需求		SIT
6	change PC715 · PC718 · PC723 · PC770 · PC774 · PC777 · PC779 From 0402 to 0603	32	線路修正		SIT
7					
8					
9					
10					
11					
12					
13					
14		33			
15		38			
16		38			
17		31			
18		31			
19		35			
20		35			
21		38			
22		35			
23		32		2014/4/4	SVT
		33			
		34			
24		38		2014/4/14	SVT
25		38		2014/4/14	SVT



I/O port
CPU

750mA (30mils)
180mA (8mils)
1500mA (60mils)

2800mA (112mils)

Aditya Iitit

- 8 ON/OFF#
- 9 EC_RSMRST#
- 10 PBTN_OUT#
- 11 PMC_SLP_S4#
- 12 PMC_SLP_S3#
- 26 KBRST#
- 27 PMC_CORE_PWROK
- 28 PMC_PLTRST#

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Power Block Diagram	
Doc No	LA-C71P	Doc Name	LA-C71P	Rev	0.2
Doc Date	Wednesday, January 14, 2015	Sheet	31	of 34	