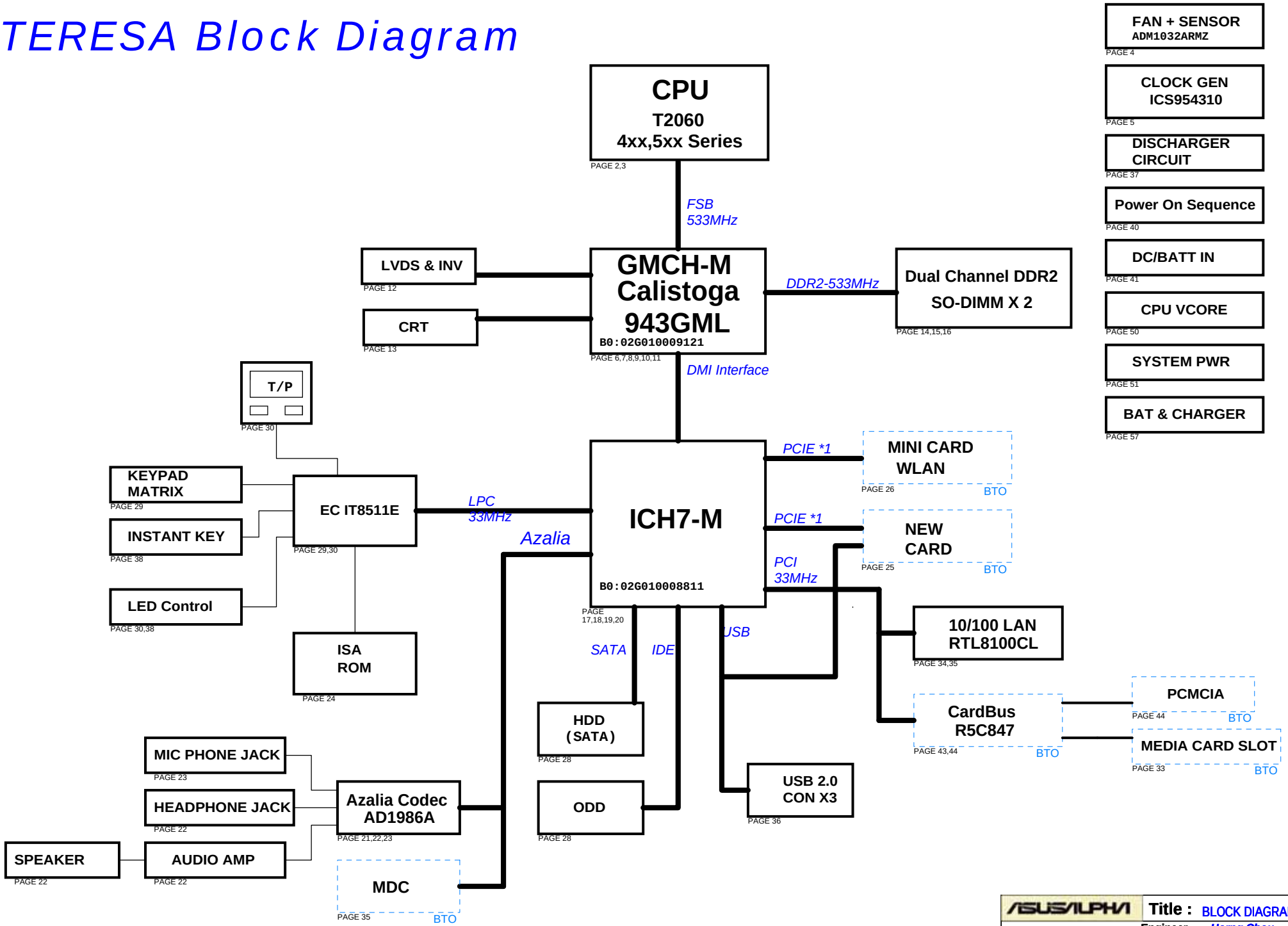
TERESA Block Diagram



ASUSALPHA

Title : BLOCK DIAGRAM

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 1 of 57

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

U201A

ADDR GROUP 0 / ADDR GROUP 1 / CONTROL / XDP/ITP SIGNALS / THERM / HCLK / RESERVED

H_ADSTB#0 H_ADSTB#1

H_A20M# H_FERR# H_IGNNE#

H_STPCLK# H_INTR H_NMI H_SMI#

H_ADS# H_BNR# H_BPRI# H_DEFER# H_DRDY# H_DBSY# H_BR0# H_IERR# H_INIT# H_LOCK# H_CPURST# H_RS#0 H_RS#1 H_RS#2 H_TRDY# H_HIT# H_HITM#

H_PREQ# H_TCK H_TDI H_TDO H_TMS H_TRST#

CPU_DBR# PROCHOT_S# CPU_THRM_DA CPU_THRM_DC PM_THRMTRIP# CLK_CPU_BCLK CLK_CPU_BCLK#

T202 T203 T204 TPC28T T201

R201 56Ohm R202 54.9Ohm @ R203 R204 R205 R206 R207 R208 56Ohm 56Ohm@

+VCCP_AGTL+ GND

U201B

DATA GRP 0 / DATA GRP 1 / DATA GRP 2 / DATA GRP 3 / MISC

H_D#[0..63] 6

H_DSTBN#0 H_DSTBP#0 H_DINV#0 H_DSTBN#1 H_DSTBP#1 H_DINV#1 H_DSTBN#2 H_DSTBP#2 H_DINV#2 H_DSTBN#3 H_DSTBP#3 H_DINV#3

GTL_REF TEST1 TEST2 CPU_BSEL0 CPU_BSEL1 CPU_BSEL2

H_COMP0 R210 27.4Ohm 1% H_COMP1 R211 54.9Ohm 1% H_COMP2 R212 27.4Ohm 1% H_COMP3 R215 54.9Ohm 1%

H_DPRSTP# H_DPSLP# H_DPWR# H_PWRGD H_CPUSLP# PM_PSI#

R209 1KOhm 1% R213 2KOhm 1% C201 0.1UF/10V @ @R214 1KOhm R216 51Ohm

<500 mil (55 Ohm) T/B trace 5 Space 25

For Celeron M

BCLK	FSB	BSEL2	BSEL1	BSEL0
133MHz	533MHz	L	L	H

(070122)Change CPU Socket into PN=12G011204796

(070122)Change CPU Socket into PN=12G011204796

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

+VCCP_AGTL+ +VCCP JP201 SHORT_PIN 2.5A

+VCCP 6,9,20,52
+VCCP_AGTL+ 3,5,6,9

29 H_PROCHOT_S# R217 56Ohm R218 56Ohm@ H_PWRGD

ASUSALPHA

Title : YONAH CPU (1)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

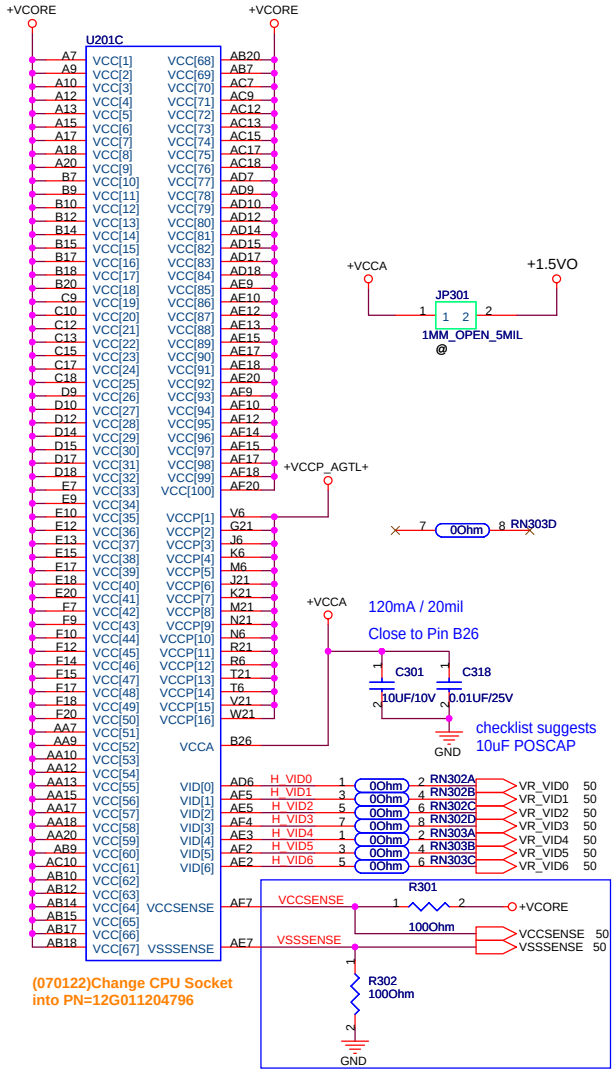
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 2 of 57

Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCC	1.0V	1.2V	1.3V
	C3	C2	C0
ICC	14.7A	16.5A	29Ah

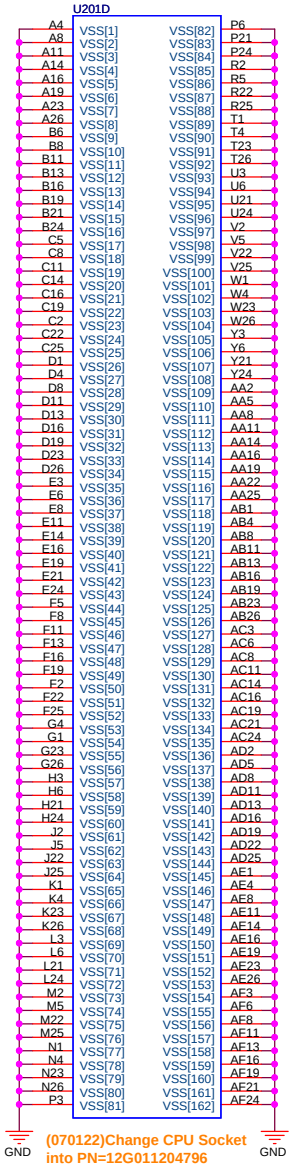
Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

Modity Table for Celeron M

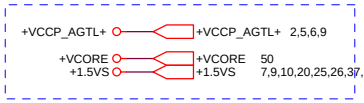


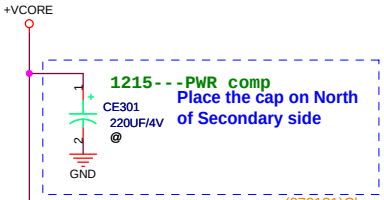
(070122)Change CPU Socket into PN=12G011204796

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



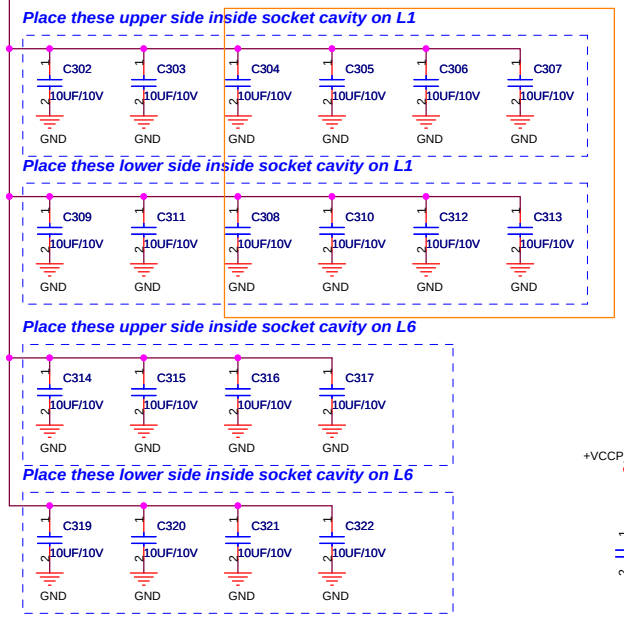
(070122)Change CPU Socket into PN=12G011204796



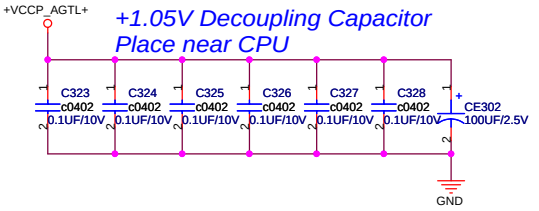


Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

(070131)Change 22UF into 10UF



(061228)Change into 10UF/10V PN:11G236322636360
C302,C303,C309,C311
C314,C315,C316,C317
C319,C320,C321,C322



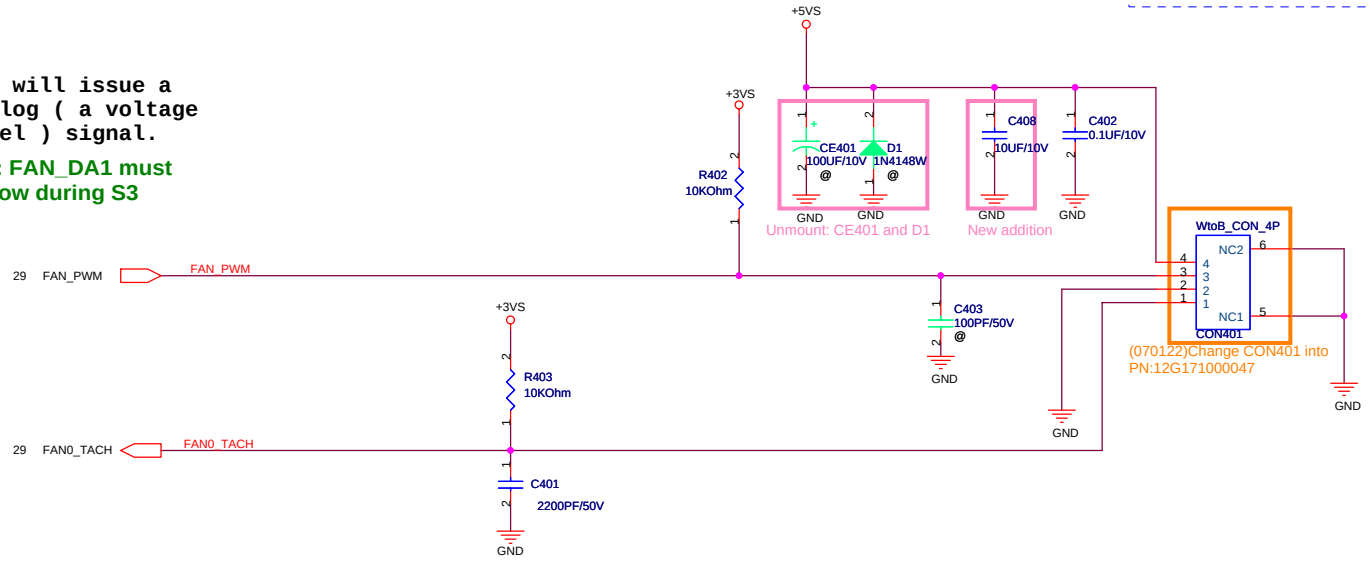
ASUSALPHA	Title :	Yonah CPU (2)	
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou	
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 3	of 57	

Fan Speed Control

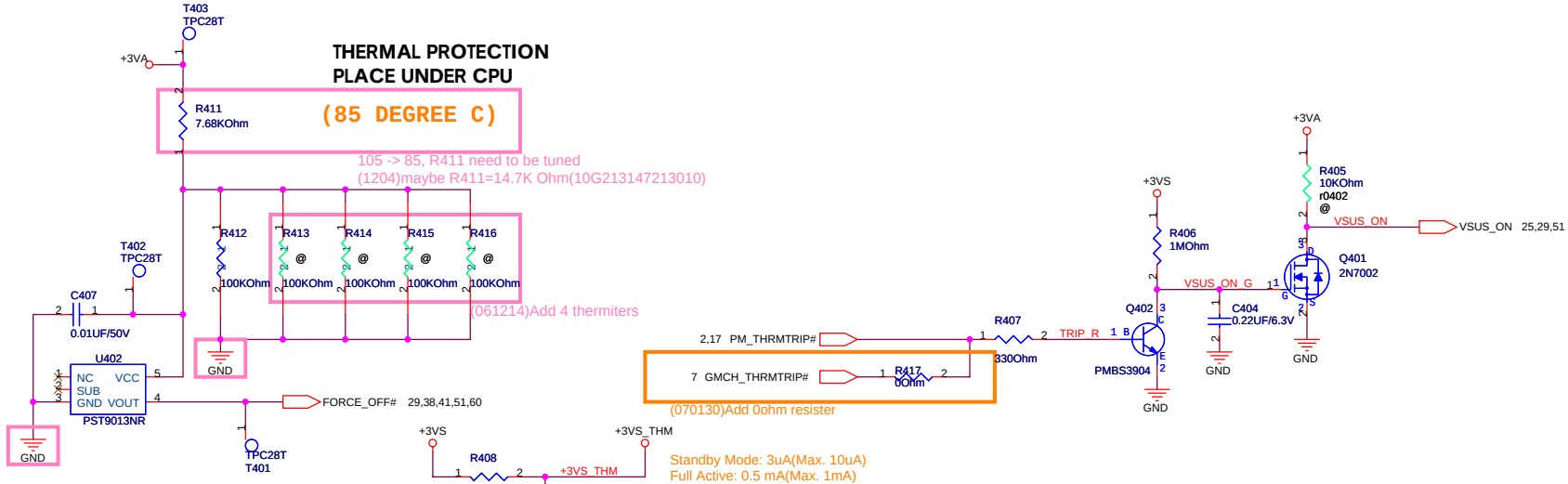
+5VS, +3VS, +3VA → +5VS 13,19,20,21,22,28,29,30,34,37,38,50,61; +3VS 5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61; +3VA 12,22,29,37,38,40,41,54,59,63

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



THERMAL PROTECTION PLACE UNDER CPU



Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSALPHA	Title : THER-SENSOR,FAN		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 4 of 57		

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

(070130)Change C516 from 27PF to 33PF

Delete CLK_ITPMPCI(connect to pin5)

internal pull high

Remove 0ohm

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

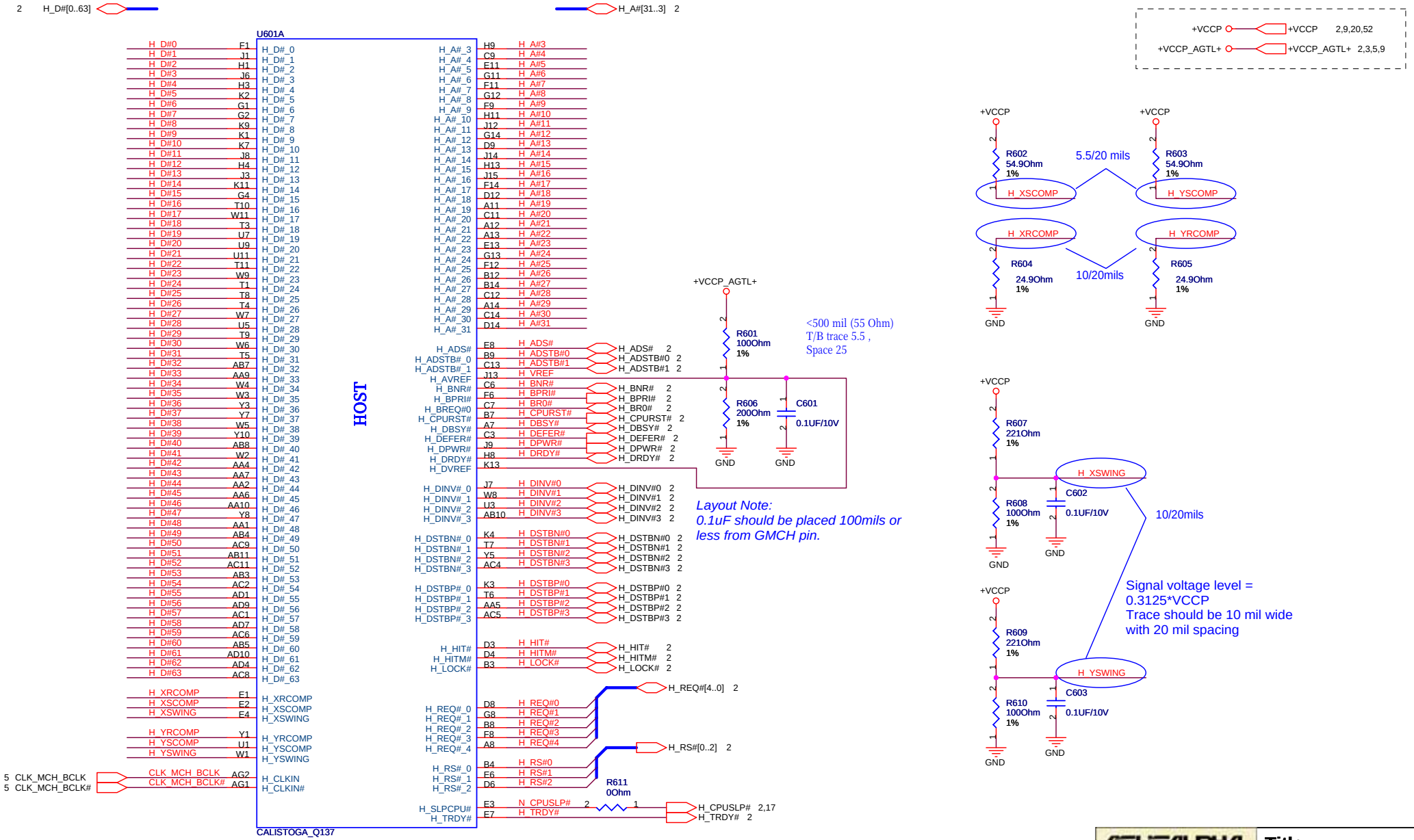
Realtek:Mount R519,Remove R550 R534

ICS954310CGLFT

Internal Pull-Up Resistor

Internal Pull-Down Resistor

ASUSALPHA	Title :	CLOCK GEN	
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou	
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 5 of 57		



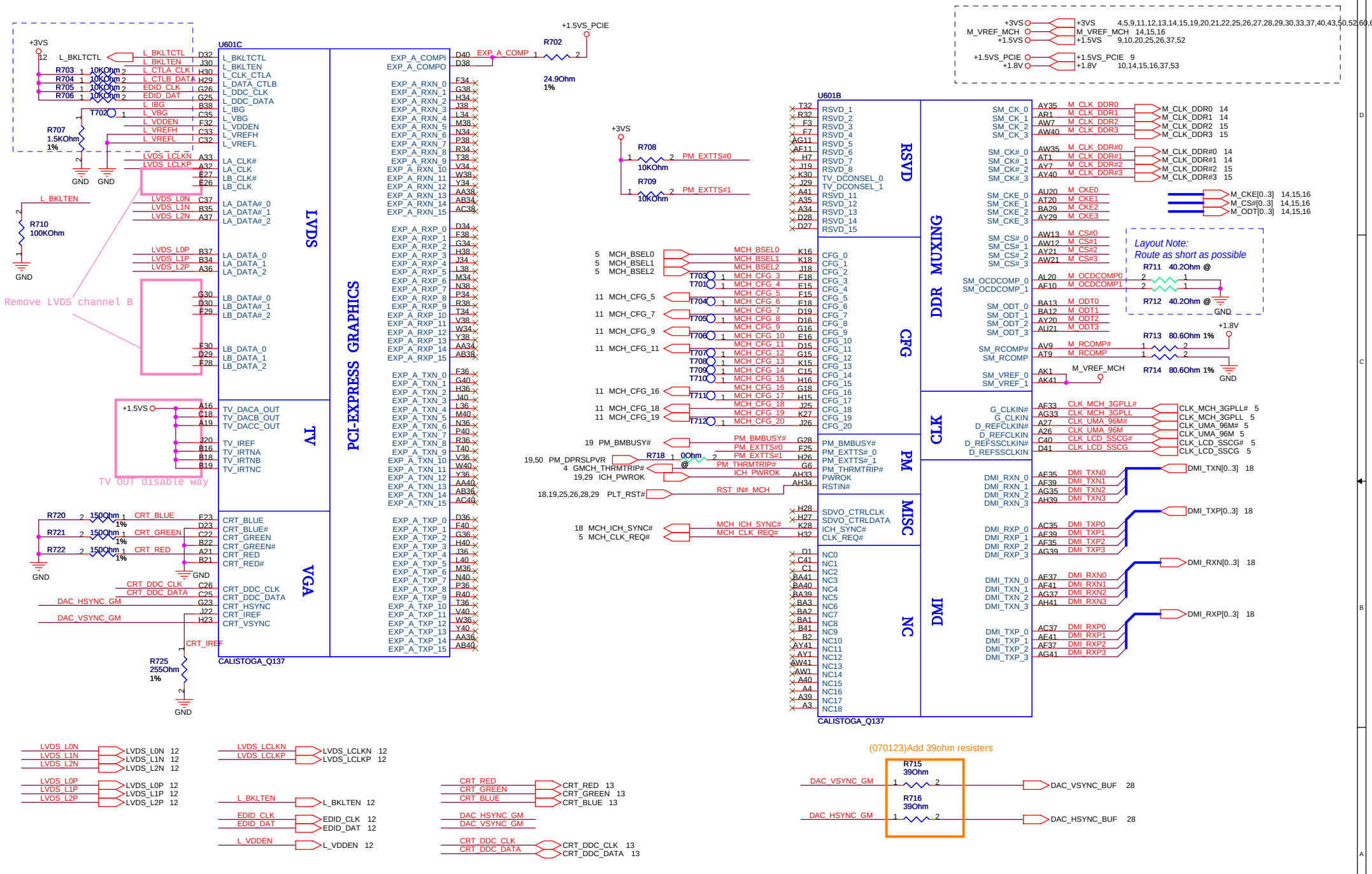
ASUSALPHA

Title : Calistoga GMCH (1)

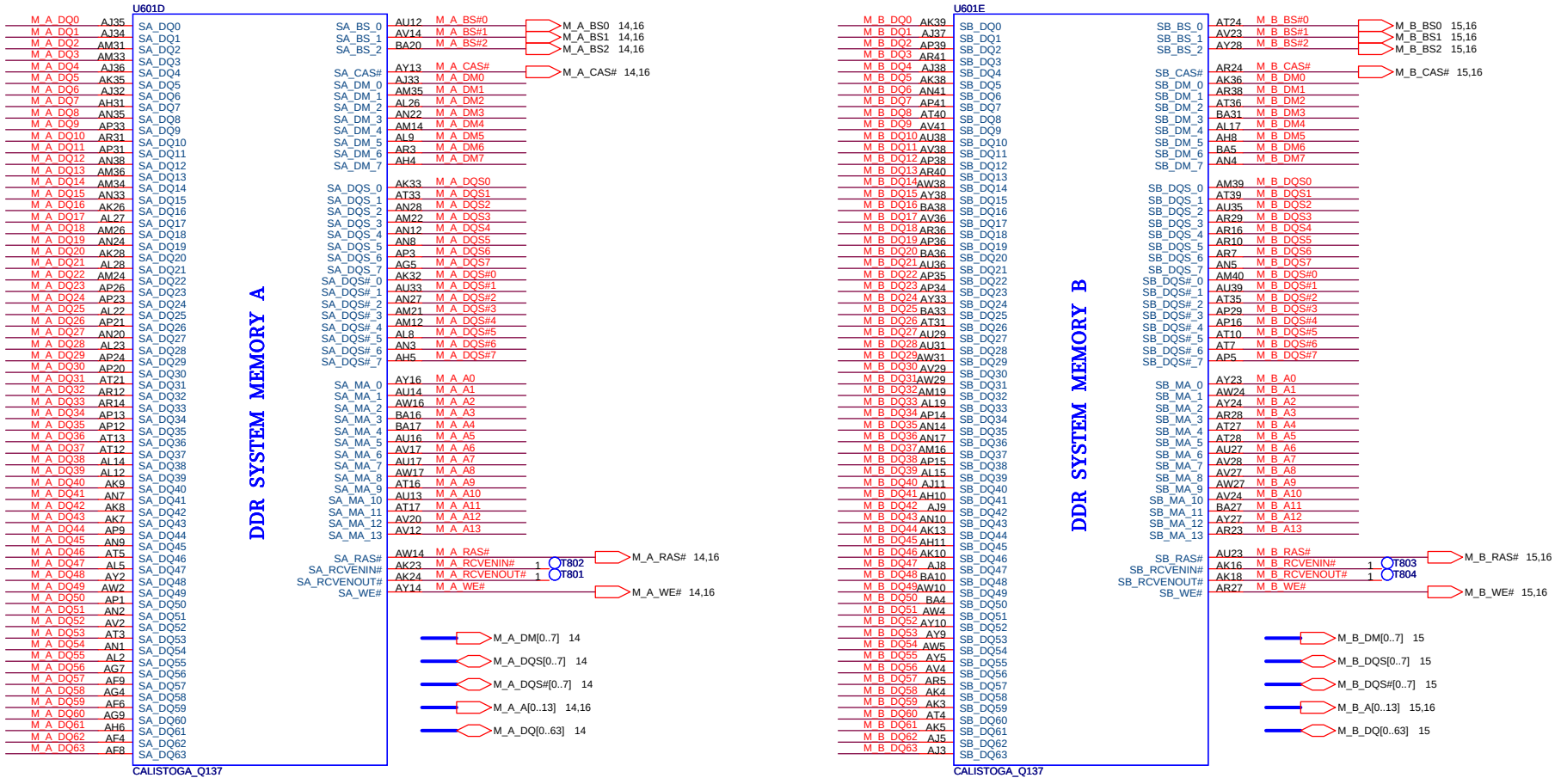
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 6 of 57



Title	Calistoga PCI-E (2)
Company	ASUSALPHATeK COMPUTER INC.
Engineer	Horng Chou
Size	Custom
Project Name	TERESA
Rev	1.1
Date	Monday, February 05, 2007
Sheet	7 of 57



ASUSALPHA

Title : Calistoga DDR2 (3)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 8 of 57

Layout Note:
Place filter components close to GMCH

Layout Note:
Caps should be on Top layer

+1.5VS_PCIE

VCC3G

+1.5VS_3GPLL

1500 mA

L902 120Ohm/100Mhz
CE902 150UF/4V @
C902 10UF/10V
C903 10UF/10V

L901 30Ohm/100Mhz
C904 0.1UF/10V
C905 10UF/10V
VCCA_3GPLL

+1.5VS_VCCAUX

L903 80Ohm/100Mhz
(070131)
220UF=>150UF
CE903 150UF/4V
C909 0.1UF/10V
VCCAUX
1900 mA

+1.5VS_DPLLA

L904 30Ohm/100Mhz
CE904 @ 470UF/2.5V
C912 0.1UF/10V
VCCA_DPLLA
50 mA

+1.5VS_DPLLB

L906 30Ohm/100Mhz
CE905 @ 470UF/2.5V
C918 0.1UF/10V
VCCA_DPLLB
50 mA

+1.5VS_HPLL

L907 120Ohm/100Mhz
C923 22UF/6.3V @
C924 0.1UF/10V
VCCA_HPLL
45 mA

+1.5VS_MPLL

L908 120Ohm/100Mhz
C927 22UF/6.3V @
C928 0.1UF/10V
VCCA_MPLL
45 mA

(070131)C923, C927:unmount

GMCH VCORE

+VCCP
+1.05VS
3500 mA
+VCCP_GMCH
JP902 SHORT_PIN @
JP901 SHORT_PIN @

+1.5VS
VCCD_LVDS 20 mA
Pin A28 B28 C28
C910 0.1UF/10V
C911 10UF/10V

+1.5VS
VCCD_TVDAC
Pin D21
C913 0.022UF/25V
C914 0.1UF/10V

24 mA

+1.5VS
VCCD_QTVDAC
H19 C28
C919 0.022UF/25V
C920 0.1UF/10V

Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
0.1uF caps in 1.5VS_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

+2.5VS

VCC_SYNC
Pin H22
C932 0.1UF/10V

VCCA_LVDS
Pin A38 10 mA
C933 0.01UF/25V
C934 0.1UF/10V

VCCA_3GBG
Pin G41 2 mA
C935 0.1UF/10V

VCCTX_LVDS 60 mA
Pin A30 B30 C30
C936 0.1UF/10V
C937 4.7UF/10V

R905 10Ohm
+VCCP_GMCH_R
D902 BAT54C
+VCCP_GMCH

70 mA

VCCA_CRTDAC
Pin E21 F21
+2.5VS_CRTDAC
L909 120Ohm/100Mhz
C901 0.022UF/25V
C946 0.1UF/10V

Layout Note:
These Caps should be within 250 mils of edge of GMCH

+3VS
VCC_HV 40 mA
Pin A23 B23 B25
C944 10UF/10V
C945 0.1UF/10V

U601H

H22	VCCSYNC	
C30	VCC_TXLVDS0	
B30	VCC_TXLVDS1	
A30	VCC_TXLVDS2	
AJ41	VCC3G0	
AB41	VCC3G1	
Y41	VCC3G2	
V41	VCC3G3	
R41	VCC3G4	
N41	VCC3G5	
L41	VCC3G6	
AC33	VCCA_3GPLL	
G41	VCCA_3GBG	
H41	VSSA_3GBG	
F21	VCCA_CRTDAC0	
E21	VCCA_CRTDAC1	
G21	VSSA_CRTDAC	
B26	VCCA_DPLLA	
C39	VCCA_DPLLB	
AF1	VCCA_HPLL	
A38	VCCA_LVDS	
B39	VSSA_LVDS	
AF2	VCCA_MPLL	
H20	VCCA_TVBG	
G20	VSSA_TVBG	
E19	VCCA_TVDACA0	
F19	VCCA_TVDACA1	
C20	VCCA_TVDACB0	
D20	VCCA_TVDACB1	
E20	VCCA_TVDACC0	
F20	VCCA_TVDACC1	
AH1	VCCD_HMPLL0	
AH2	VCCD_HMPLL1	
A28	VCCD_LVDS0	
B28	VCCD_LVDS1	
C28	VCCD_LVDS2	
D21	VCCD_TVDAC	
A23	VCC_HV0	
B23	VCC_HV1	
B25	VCC_HV2	
H19	VCCD_QTVDAC	
AK31	VCCAUX0	
AE31	VCCAUX1	
AE31	VCCAUX2	
AC31	VCCAUX3	
AL30	VCCAUX4	
AK30	VCCAUX5	
AJ30	VCCAUX6	
AH30	VCCAUX7	
AG30	VCCAUX8	
AF30	VCCAUX9	
AE30	VCCAUX10	
AD30	VCCAUX11	
AC30	VCCAUX12	
AG29	VCCAUX13	
AF29	VCCAUX14	
AE29	VCCAUX15	
AD29	VCCAUX16	
AC29	VCCAUX17	
AG28	VCCAUX18	
AE28	VCCAUX19	
AE28	VCCAUX20	
AH22	VCCAUX21	
AJ21	VCCAUX22	
AH21	VCCAUX23	
AJ20	VCCAUX24	
AH20	VCCAUX25	
AH19	VCCAUX26	
P19	VCCAUX27	
P16	VCCAUX28	
AH15	VCCAUX29	
P15	VCCAUX30	
AH14	VCCAUX31	
AG14	VCCAUX32	
AF14	VCCAUX33	
AE14	VCCAUX34	
Y14	VCCAUX35	
AF13	VCCAUX36	
AE13	VCCAUX37	
AF12	VCCAUX38	
AE12	VCCAUX39	
AD12	VCCAUX40	

CALISTOGA_Q137

TV OUT disable way

POWER

VTT_0	AC14
VTT_1	AB14
VTT_2	W14
VTT_3	Y14
VTT_4	T14
VTT_5	R14
VTT_6	P14
VTT_7	N14
VTT_8	M14
VTT_9	L14
VTT_10	AD13
VTT_11	AC13
VTT_12	AB13
VTT_13	AA13
VTT_14	Y13
VTT_15	W13
VTT_16	V13
VTT_17	U13
VTT_18	T13
VTT_19	R13
VTT_20	N13
VTT_21	M13
VTT_22	L13
VTT_23	AB12
VTT_24	AA12
VTT_25	Y12
VTT_26	W12
VTT_27	V12
VTT_28	U12
VTT_29	T12
VTT_30	R12
VTT_31	P12
VTT_32	N12
VTT_33	M12
VTT_34	L12
VTT_35	R11
VTT_36	P11
VTT_37	N11
VTT_38	M11
VTT_39	R10
VTT_40	P10
VTT_41	N10
VTT_42	M10
VTT_43	P9
VTT_44	N9
VTT_45	M9
VTT_46	R8
VTT_47	P8
VTT_48	N8
VTT_49	M8
VTT_50	P7
VTT_51	N7
VTT_52	M7
VTT_53	R6
VTT_54	P6
VTT_55	M6
VTT_56	A6
VTT_57	R5
VTT_58	P5
VTT_59	N5
VTT_60	M5
VTT_61	P4
VTT_62	N4
VTT_63	M4
VTT_64	R3
VTT_65	P3
VTT_66	N3
VTT_67	M3
VTT_68	R2
VTT_69	P2
VTT_70	M2
VTT_71	D2
VTT_72	AB1
VTT_73	R1
VTT_74	P1
VTT_75	N1
VTT_76	M1

VTTLF_CAP3
C929 0.47UF/16V

VTTLF_CAP2
VTTLF_CAP1
C938 0.47UF/16V
C939 0.22UF/6.3V

+VCCP_AGTL+
+VCCP_GMCH
+1.5VS_PCIE
+3VS
+2.5VS
+1.5VS

+VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH 10
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+2.5VS 37,54
+1.5VS 7,10,20,25,26,37,52

+VCCP_AGTL+

800 mA

C906 4.7UF/10V
C907 2.2UF/6.3V
C908 0.22UF/6.3V
CE901 100UF/2.5V

(070118)
change into 11G08D210791

Layout Note:
Place on the edge

Layout Note:
Place in cavity

Remove TV OUT Power

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS
+2.5VS should be placed within 200 mils of edge.

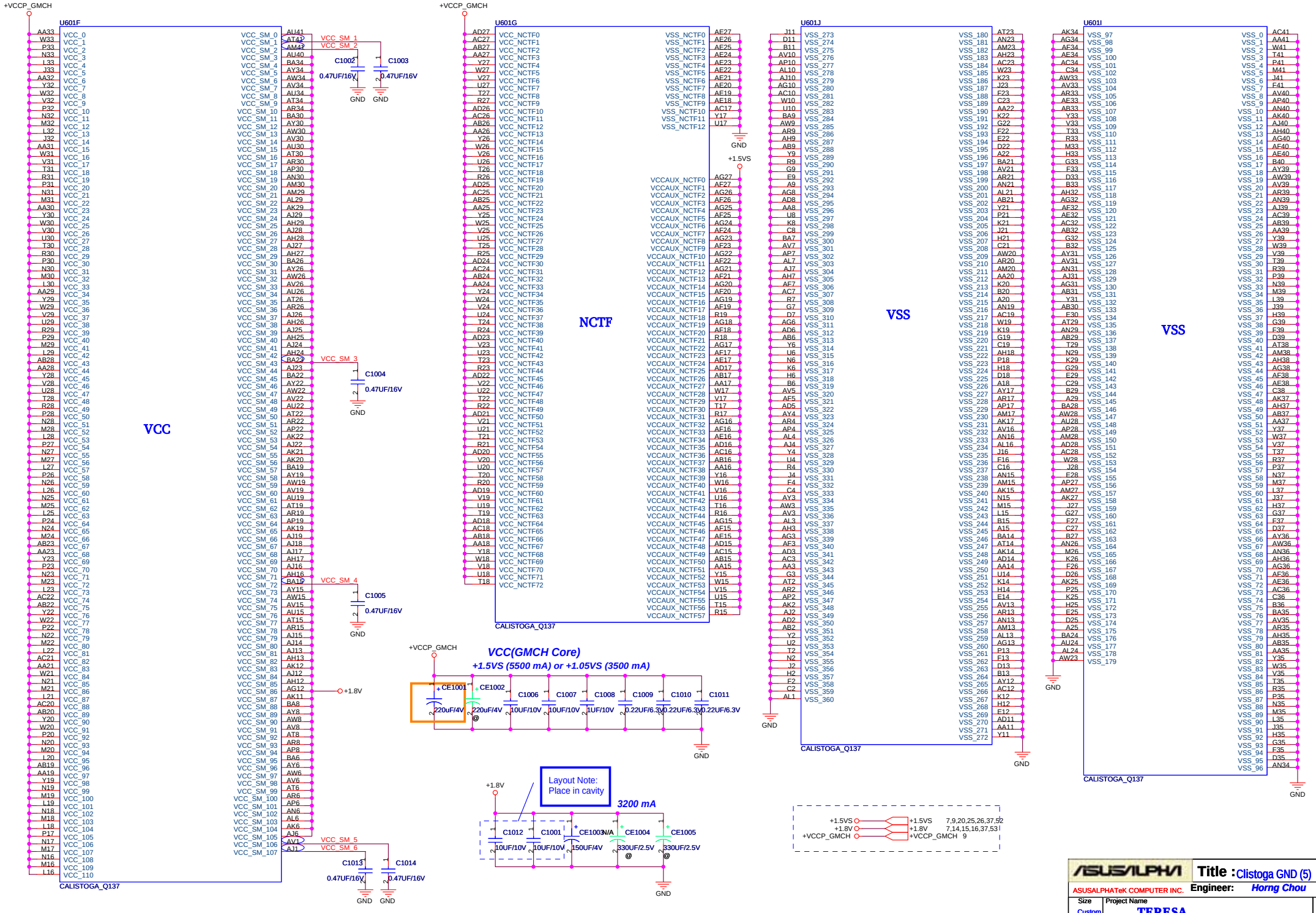
ASUSALPHA

Title : Calistoga Power (4)

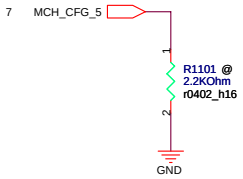
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

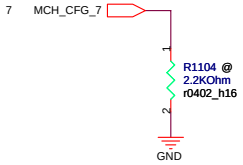
Date: Monday, February 05, 2007 Sheet 9 of 57



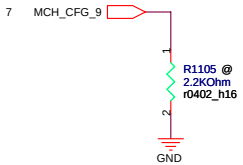
ASUSALPHATeK COMPUTER INC.	Title : Clistoga GND (5)	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 10 of 57	



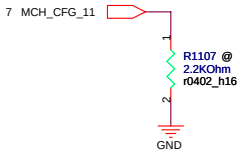
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



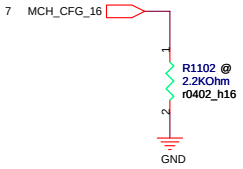
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



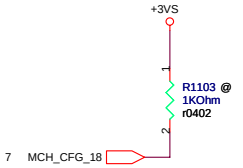
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



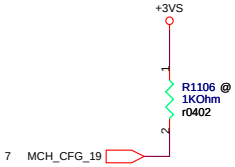
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

(061215)Remove +2.5VS power supply

ASUSALPHA

Title : Calistoga Strapping

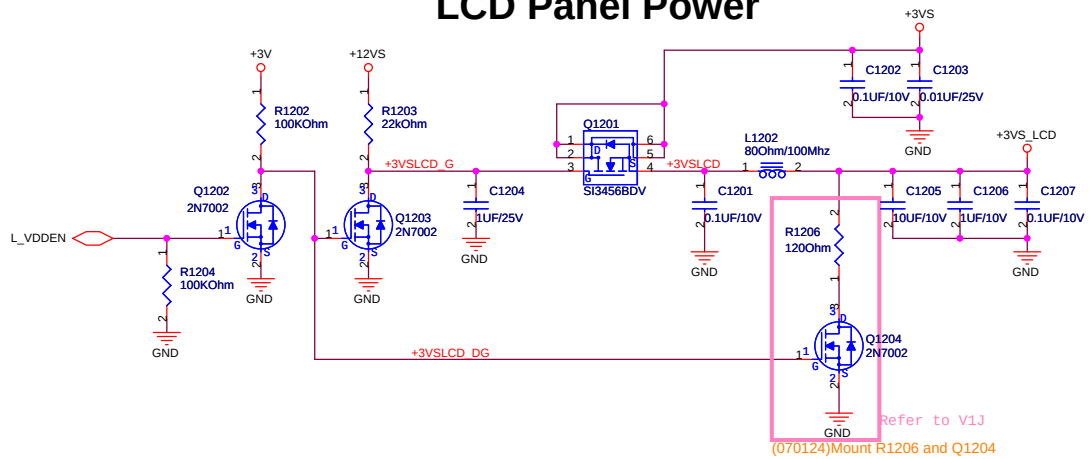
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Monday, February 05, 2007 Sheet 11 of 57

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



Refer to V1J
(070124)Mount R1206 and Q1204

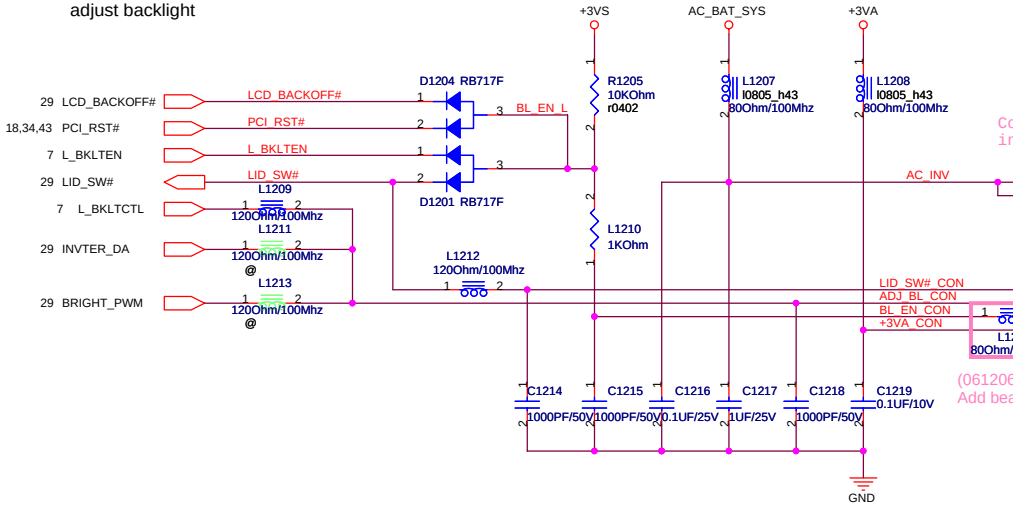
Remove CMOS Camera(USB4)

LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel



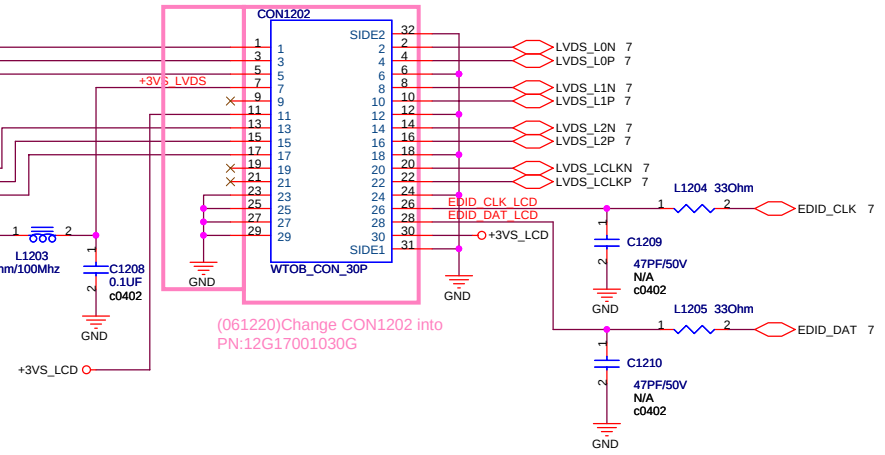
Combine Inverter interface into LVDS interface

(061206,EMI)
Add bead

LCD LVDS & INVERTER Interface

Delete LVDS channel B

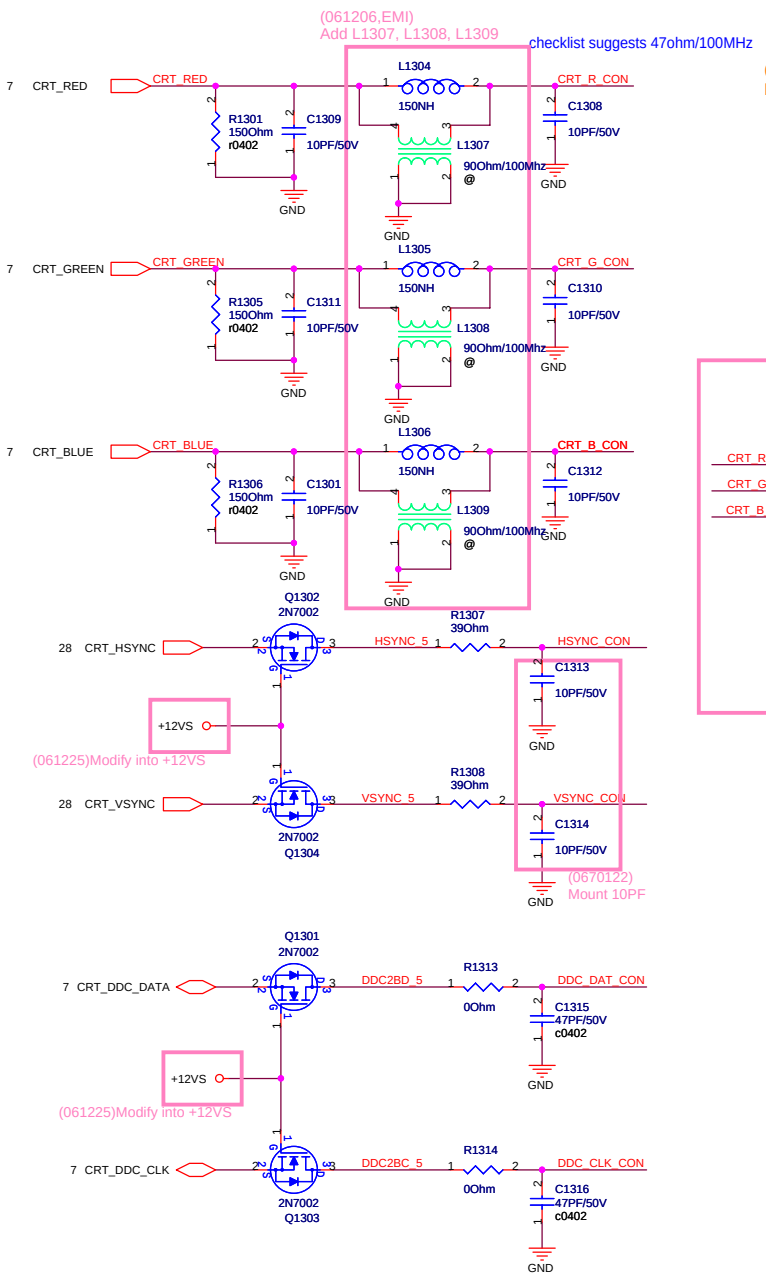
Rearrange pin location(061201)

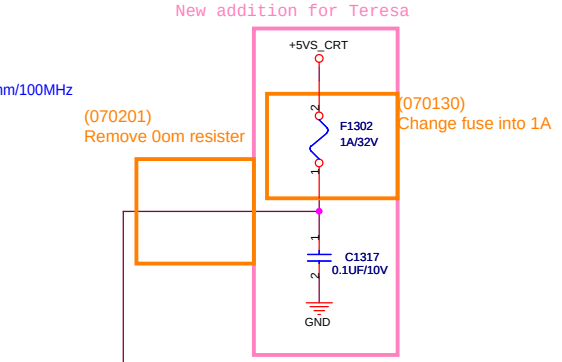


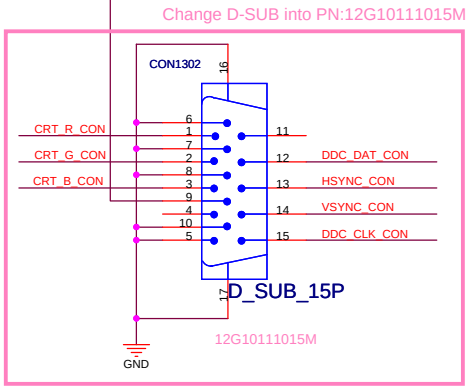
(061220)Change CON1202 into PN:12G17001030G

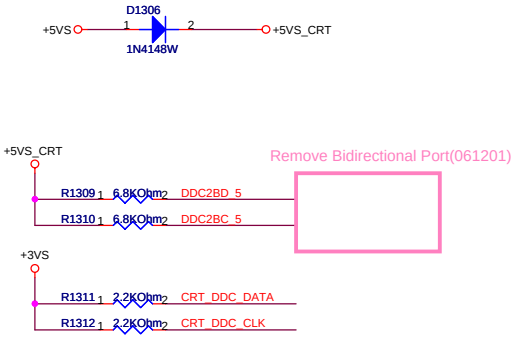
ASUSALPHA	Title : LVDS & INVERTER	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 12 of 57	

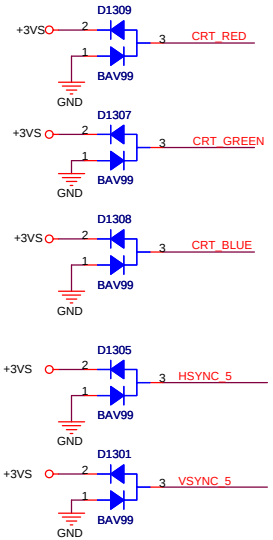
CRT OUT











ASUSALPHA	Title : CRT & TV OUT		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 13 of 57		

(061221)Change CON1401 into PN:12G02502200R

(061221)Change CON1401 into PN:12G02502200R

Layout Note: Place these Caps near SO DIMM 0

M_CLK_DDR0
C1406
PLACE NEAR SO-DIMM_1
10PF/50V
@
M_CLK_DDR#0

M_CLK_DDR1
C1408
PLACE NEAR SO-DIMM_1
10PF/50V
@
M_CLK_DDR#1

SMBus Slave Address:A0H

CON1401A

8,16 M_A_A[0..13]	M_A_A0	102	A0	DQ0	5 M_A_DQ0
	M_A_A1	101	A1	DQ1	7 M_A_DQ4
	M_A_A2	100	A2	DQ2	17 M_A_DQ2
	M_A_A3	99	A3	DQ3	19 M_A_DQ3
	M_A_A4	98	A4	DQ4	4 M_A_DQ1
	M_A_A5	97	A5	DQ5	6 M_A_DQ6
	M_A_A6	94	A6	DQ6	14 M_A_DQ5
	M_A_A7	92	A7	DQ7	16 M_A_DQ7
	M_A_A8	93	A8	DQ8	23 M_A_DQ12
	M_A_A9	91	A9	DQ9	25 M_A_DQ8
	M_A_A10	105	A10/AP	DQ10	35 M_A_DQ9
	M_A_A11	90	A11	DQ11	37 M_A_DQ10
	M_A_A12	89	A12	DQ12	20 M_A_DQ13
	M_A_A13	116	A13	DQ13	22 M_A_DQ14
		86	A14	DQ14	36 M_A_DQ11
		84	A15	DQ15	38 M_A_DQ15
8,16 M_A_BS2		85	A16_BA2	DQ16	43 M_A_DQ16
				DQ17	45 M_A_DQ17
8,16 M_A_BS0		107	BA0	DQ18	55 M_A_DQ18
8,16 M_A_BS1		106	BA1	DQ19	57 M_A_DQ19
7,16 M_CS#0		110	S0#	DQ20	44 M_A_DQ20
7,16 M_CS#1		115	S1#	DQ21	46 M_A_DQ21
7 M_CLK_DDR0		30	CK0	DQ22	56 M_A_DQ22
7 M_CLK_DDR#0		32	CK0#	DQ23	58 M_A_DQ23
7 M_CLK_DDR1		164	CK1	DQ24	61 M_A_DQ24
7 M_CLK_DDR#1		166	CK1#	DQ25	63 M_A_DQ25
7,16 M_CKE0		79	CKE0	DQ26	73 M_A_DQ26
7,16 M_CKE1		80	CKE1	DQ27	75 M_A_DQ27
8,16 M_A_CAS#		113	CAS#	DQ28	62 M_A_DQ28
8,16 M_A_RAS#		108	RAS#	DQ29	64 M_A_DQ29
8,16 M_A_WE#		109	WE#	DQ30	74 M_A_DQ30
		198	SA0	DQ31	76 M_A_DQ31
5,15,19,25,26 SMB_CLK_S		200	SA1	DQ32	123 M_A_DQ37
5,15,19,25,26 SMB_DAT_S		197	SCL	DQ33	125 M_A_DQ36
		195	SDA	DQ34	135 M_A_DQ34
				DQ35	137 M_A_DQ35
7,16 M_ODT0		114	ODT0	DQ36	124 M_A_DQ33
7,16 M_ODT1		119	ODT1	DQ37	126 M_A_DQ32
8 M_A_DM[0..7]				DQ38	134 M_A_DQ38
	M_A_DM0	10	DM0	DQ39	136 M_A_DQ39
	M_A_DM1	26	DM1	DQ40	141 M_A_DQ40
	M_A_DM2	52	DM2	DQ41	143 M_A_DQ41
	M_A_DM3	67	DM3	DQ42	151 M_A_DQ42
	M_A_DM4	130	DM4	DQ43	153 M_A_DQ43
	M_A_DM5	147	DM5	DQ44	140 M_A_DQ45
	M_A_DM6	170	DM6	DQ45	142 M_A_DQ44
	M_A_DM7	185	DM7	DQ46	152 M_A_DQ46
				DQ47	154 M_A_DQ47
8 M_A_DQS[0..7]	M_A_DQS0	13	DQS0	DQ48	157 M_A_DQ48
	M_A_DQS1	31	DQS1	DQ49	159 M_A_DQ49
	M_A_DQS2	51	DQS2	DQ50	173 M_A_DQ50
	M_A_DQS3	70	DQS3	DQ51	175 M_A_DQ54
	M_A_DQS4	131	DQS4	DQ52	158 M_A_DQ52
	M_A_DQS5	148	DQS5	DQ53	160 M_A_DQ53
	M_A_DQS6	169	DQS6	DQ54	174 M_A_DQ51
	M_A_DQS7	188	DQS7	DQ55	176 M_A_DQ55
8 M_A_DQS#[0..7]	M_A_DQS#0	11	DQS#0	DQ56	179 M_A_DQ60
	M_A_DQS#1	29	DQS#1	DQ57	181 M_A_DQ56
	M_A_DQS#2	49	DQS#2	DQ58	189 M_A_DQ57
	M_A_DQS#3	68	DQS#3	DQ59	191 M_A_DQ58
	M_A_DQS#4	129	DQS#4	DQ60	180 M_A_DQ61
	M_A_DQS#5	146	DQS#5	DQ61	182 M_A_DQ63
	M_A_DQS#6	167	DQS#6	DQ62	192 M_A_DQ62
	M_A_DQS#7	186	DQS#7	DQ63	194 M_A_DQ59

DDR_DIMM_200P

M_A_DQ[0..63] 8

SWAP SWAP SWAP SWAP SWAP

GND

CON1401B

	VDD1	VSS16	18
	VDD2	VSS17	24
	VDD3	VSS18	41
	VDD4	VSS19	53
	VDD5	VSS20	42
	VDD6	VSS21	54
	VDD7	VSS22	59
	VDD8	VSS23	65
	VDD9	VSS24	60
	VDD10	VSS25	66
	VDD11	VSS26	127
	VDD12	VSS27	139
		VSS28	128
	VDDSPD	VSS29	145
		VSS30	165
	NC1	VSS31	171
	NC2	VSS32	172
	NC3	VSS33	177
	NC4	VSS34	187
	NCTEST	VSS35	178
		VSS36	190
	VREF	VSS37	9
		VSS38	21
	GND0	VSS39	33
	GND1	VSS40	155
		VSS41	34
	NP_NC1	VSS42	132
	NP_NC2	VSS43	144
		VSS44	156
	VSS1	VSS45	168
	VSS2	VSS46	2
	VSS3	VSS47	3
	VSS4	VSS48	15
	VSS5	VSS49	27
	VSS6	VSS50	39
	VSS7	VSS51	149
	VSS8	VSS52	161
	VSS9	VSS53	28
	VSS10	VSS54	40
	VSS11	VSS55	138
	VSS12	VSS56	150
	VSS13	VSS57	162
	VSS14		
	VSS15		

DDR_DIMM_200P

+1.8V
C1402 0.1UF/16V
C1403 0.1UF/16V
C1404 0.1UF/16V
C1405 0.1UF/16V
GND

+3VS
C1407 0.1UF/16V
GND

M_VREF_MCH
C1409 2.2UF/6.3V
C1410 0.1UF/16V
GND GND

VREF -> 10/10 mils

+1.8V
CE1401 150UF/4V @
CE1402 150UF/4V @
GND GND

+1.8V
C1411 1UF/6.3V
C1412 1UF/6.3V
C1401 1UF/6.3V
C1413 1UF/6.3V
C1414 1UF/6.3V
GND

+1.8V

Layout Note: Place these Caps near SO DIMM 0

C1419 2.2UF/6.3V
C1420 2.2UF/6.3V
C1421 2.2UF/6.3V
C1422 2.2UF/6.3V
C1423 2.2UF/6.3V
GND GND GND GND GND

SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

ASUSALPHA	Title : DDR2 SO-DIMM0	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 14 of 57	

SMBus Slave Address:A4H

M_CLK_DDR2
C1507 PLACE NEAR SO-DIMM_0
10PF/50V
@
M_CLK_DDR#2

M_CLK_DDR3
C1509 PLACE NEAR SO-DIMM_0
10PF/50V
@
M_CLK_DDR#3

+3VS
R1501
10KOhm
GND

8,16 M_B_A[0..13]
8 M_B_DQ[0..63]
M_B_DQ[0..63]
8,16 M_B_BS2
8,16 M_B_BS0
8,16 M_B_BS1
7,16 M_CS#2
7,16 M_CS#3
7 M_CLK_DDR3
7 M_CLK_DDR#3
7 M_CLK_DDR2
7 M_CLK_DDR#2
7,16 M_CKE2
7,16 M_CKE3
8,16 M_B_CAS#
8,16 M_B_RAS#
8,16 M_B_WE#
+3VS_SET
5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S
7,16 M_ODT2
7,16 M_ODT3
8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

(061227)Update PCB footprint
PN:12G025032008

CON1501A

M_B_A0	102	A0	DQ0	5	M_B_DQ5
M_B_A1	101	A1	DQ1	7	M_B_DQ0
M_B_A2	100	A2	DQ2	17	M_B_DQ7
M_B_A3	99	A3	DQ3	19	M_B_DQ3
M_B_A4	98	A4	DQ4	4	M_B_DQ4
M_B_A5	97	A5	DQ5	6	M_B_DQ1
M_B_A6	94	A6	DQ6	14	M_B_DQ6
M_B_A7	92	A7	DQ7	16	M_B_DQ2
M_B_A8	93	A8	DQ8	23	M_B_DQ8
M_B_A9	91	A9	DQ9	25	M_B_DQ9
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ10
M_B_A11	90	A11	DQ11	37	M_B_DQ11
M_B_A12	89	A12	DQ12	20	M_B_DQ12
M_B_A13	116	A13	DQ13	22	M_B_DQ13
	86	A14	DQ14	36	M_B_DQ14
	84	A15	DQ15	38	M_B_DQ15
	85	A16_BA2	DQ16	43	M_B_DQ16
			DQ17	45	M_B_DQ17
	107	BA0	DQ18	55	M_B_DQ18
	106	BA1	DQ19	57	M_B_DQ19
	110	S0#	DQ20	44	M_B_DQ20
	115	S1#	DQ21	46	M_B_DQ21
	30	CK0	DQ22	56	M_B_DQ22
	32	CK0#	DQ23	58	M_B_DQ23
	164	CK1	DQ24	61	M_B_DQ24
	166	CK1#	DQ25	63	M_B_DQ25
	79	CKE0	DQ26	73	M_B_DQ26
	80	CKE1	DQ27	75	M_B_DQ27
	113	CAS#	DQ28	62	M_B_DQ28
	108	RAS#	DQ29	64	M_B_DQ29
	109	WE#	DQ30	74	M_B_DQ30
	198	SA0	DQ31	76	M_B_DQ31
	200	SA1	DQ32	123	M_B_DQ36
	197	SCL	DQ33	125	M_B_DQ32
	195	SDA	DQ34	135	M_B_DQ34
			DQ35	137	M_B_DQ35
	114	ODT0	DQ36	124	M_B_DQ33
	119	ODT1	DQ37	126	M_B_DQ37
			DQ38	134	M_B_DQ38
M_B_DM0	10	DM0	DQ39	136	M_B_DQ39
M_B_DM1	26	DM1	DQ40	141	M_B_DQ49
M_B_DM2	52	DM2	DQ41	143	M_B_DQ53
M_B_DM3	67	DM3	DQ42	151	M_B_DQ54
M_B_DM4	130	DM4	DQ43	153	M_B_DQ55
M_B_DM6	147	DM5	DQ44	140	M_B_DQ48
M_B_DM7	170	DM6	DQ45	142	M_B_DQ52
M_B_DM5	185	DM7	DQ46	152	M_B_DQ51
			DQ47	154	M_B_DQ50
M_B_DQS0	13	DQS0	DQ48	157	M_B_DQ62
M_B_DQS1	31	DQS1	DQ49	159	M_B_DQ57
M_B_DQS2	51	DQS2	DQ50	173	M_B_DQ59
M_B_DQS3	70	DQS3	DQ51	175	M_B_DQ58
M_B_DQS4	131	DQS4	DQ52	158	M_B_DQ56
M_B_DQS6	148	DQS5	DQ53	160	M_B_DQ60
M_B_DQS7	169	DQS6	DQ54	174	M_B_DQ61
M_B_DQS5	188	DQS7	DQ55	176	M_B_DQ63
M_B_DQS#0	11	DQS#0	DQ56	179	M_B_DQ42
M_B_DQS#1	29	DQS#1	DQ57	181	M_B_DQ47
M_B_DQS#2	49	DQS#2	DQ58	189	M_B_DQ40
M_B_DQS#3	68	DQS#3	DQ59	191	M_B_DQ45
M_B_DQS#4	129	DQS#4	DQ60	180	M_B_DQ43
M_B_DQS#6	146	DQS#5	DQ61	182	M_B_DQ46
M_B_DQS#7	167	DQS#6	DQ62	192	M_B_DQ41
M_B_DQS#5	186	DQS#7	DQ63	194	M_B_DQ44

SWAP
SWAP
SWAP

DDR_DIMM_200P

Address reference +1.8V, add four 0.1uF decoupling CAP.

(061227)Update PCB footprint
PN:12G025032008

CON1501B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR_DIMM_200P

+1.8V
C1502 0.1UF/16V c0402
C1503 0.1UF/16V c0402
C1504 0.1UF/16V c0402
C1505 0.1UF/16V c0402
GND

+3VS
C1506 0.1UF/16V
GND

M_VREF_MCH
VREF -> 10/10 mils
C1508 1UF/6.3V
C1501 0.1UF/16V
GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V
C1510 0.1UF/16V
C1511 0.1UF/16V
C1512 0.1UF/16V
C1513 0.1UF/16V
GND

Layout Note: Place these Caps near SO DIMM 0

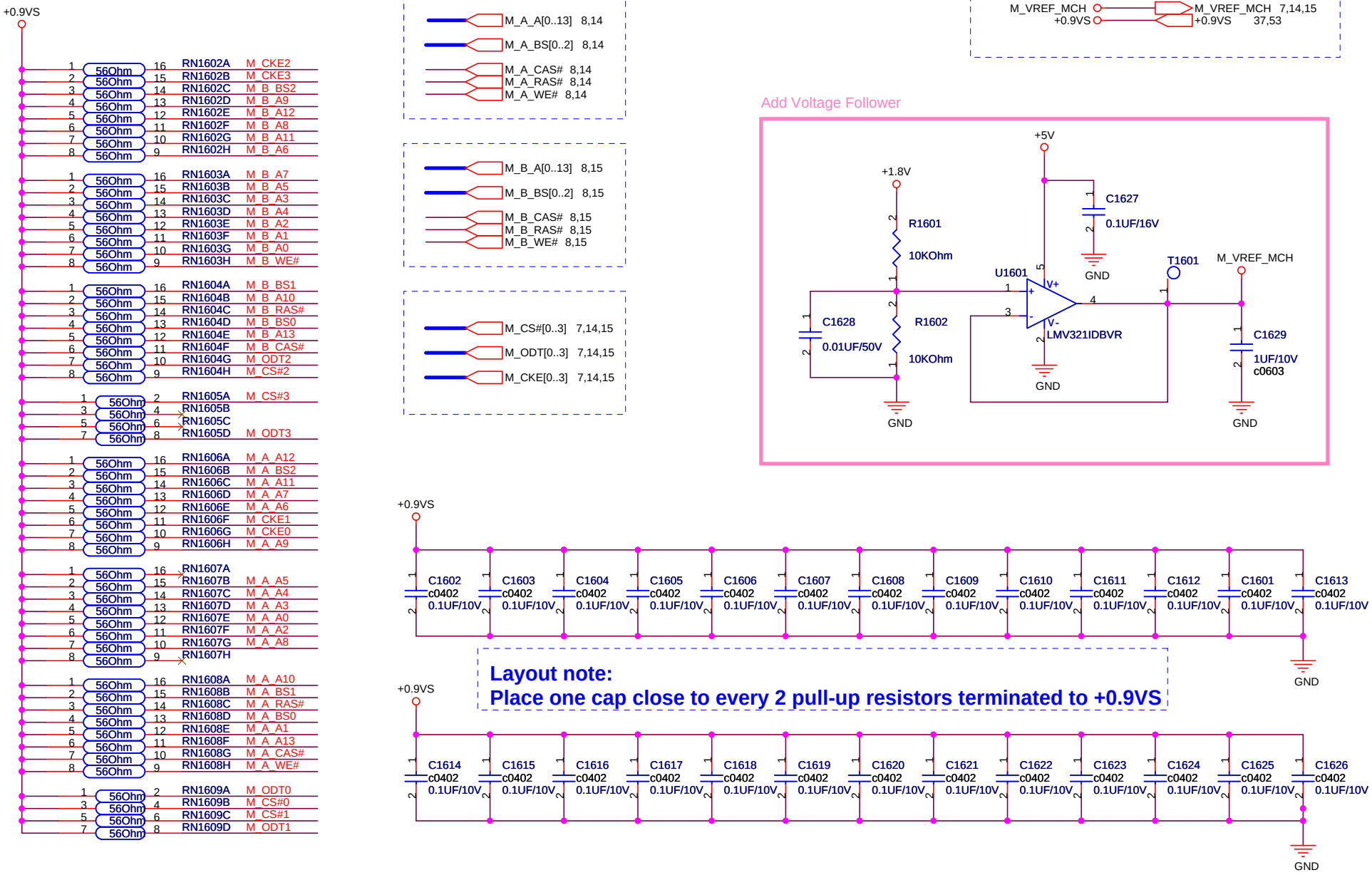
+1.8V
C1514 0.1UF/16V c0402
C1515 0.1UF/16V c0402
C1516 0.1UF/16V c0402
C1517 0.1UF/16V c0402
GND

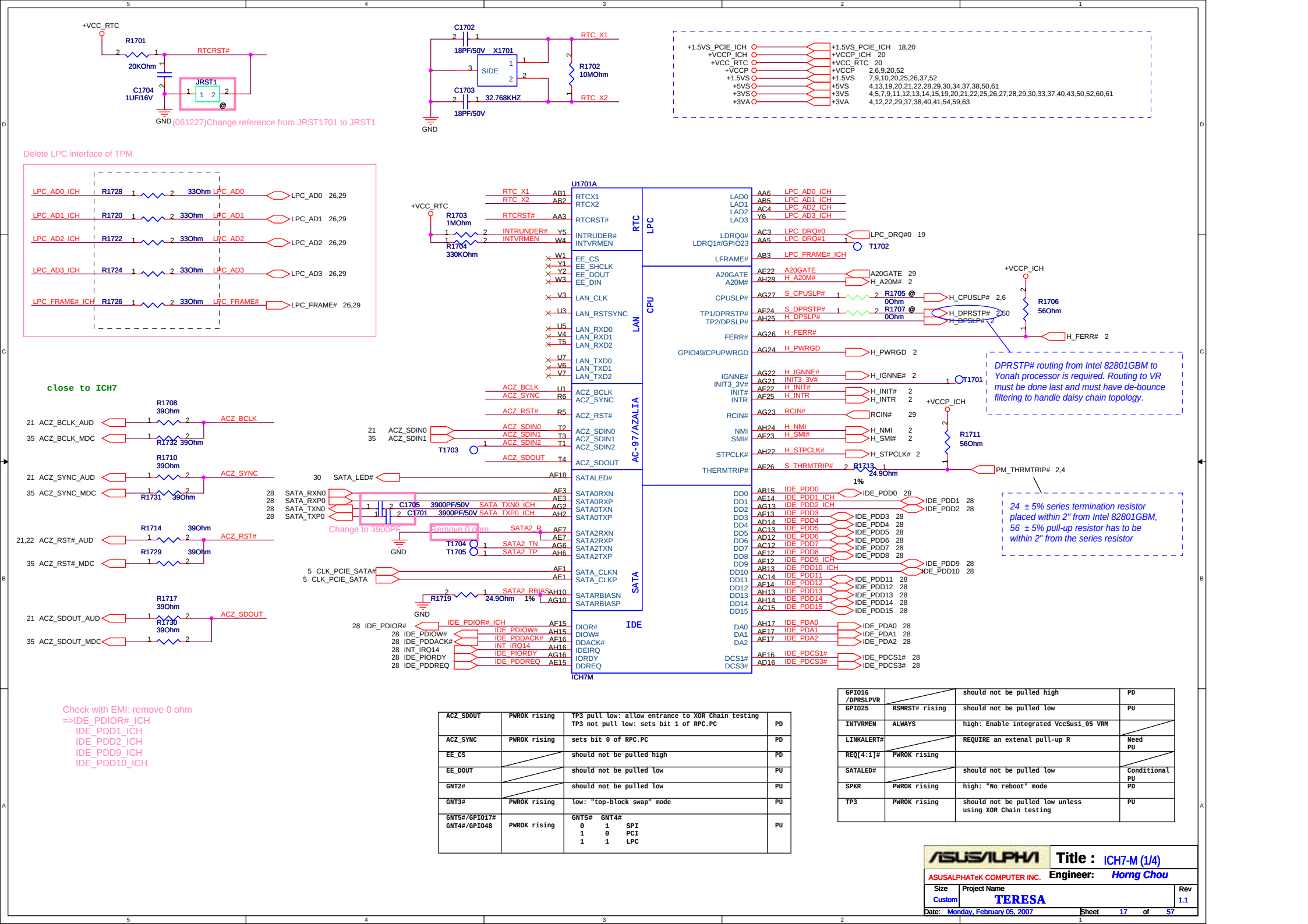
Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V
C1518 2.2UF/6.3V
C1519 2.2UF/6.3V
C1520 2.2UF/6.3V
C1521 2.2UF/6.3V
C1522 2.2UF/6.3V
GND

Layout Note: Place these CAPs near the GMCH

ASUSALPHA	Title : DDR2 SO-DIMM1	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 15 of 57	


+0.9VS
RN1602A M_CKE2
RN1602B M_CKE3
RN1602C M_B_BS2
RN1602D M_B_A9
RN1602E M_B_A12
RN1602F M_B_A8
RN1602G M_B_A11
RN1602H M_B_A6
RN1603A M_B_A7
RN1603B M_B_A5
RN1603C M_B_A3
RN1603D M_B_A4
RN1603E M_B_A2
RN1603F M_B_A1
RN1603G M_B_A0
RN1603H M_B_WE#
RN1604A M_B_BS1
RN1604B M_B_A10
RN1604C M_B_RAS#
RN1604D M_B_BS0
RN1604E M_B_A13
RN1604F M_B_CAS#
RN1604G M_ODT2
RN1604H M_CS#2
RN1605A M_CS#3
RN1605B
RN1605C
RN1605D M_ODT3
RN1606A M_A_A12
RN1606B M_A_BS2
RN1606C M_A_A11
RN1606D M_A_A7
RN1606E M_A_A6
RN1606F M_CKE1
RN1606G M_CKE0
RN1606H M_A_A9
RN1607A
RN1607B M_A_A5
RN1607C M_A_A4
RN1607D M_A_A3
RN1607E M_A_A0
RN1607F M_A_A2
RN1607G M_A_A8
RN1607H
RN1608A M_A_A10
RN1608B M_A_BS1
RN1608C M_A_RAS#
RN1608D M_A_BS0
RN1608E M_A_A1
RN1608F M_A_A13
RN1608G M_A_CAS#
RN1608H M_A_WE#
RN1609A M_ODT0
RN1609B M_CS#0
RN1609C M_CS#1
RN1609D M_ODT1
56Ohm
M_A_A[0..13] 8,14
M_A_BS[0..2] 8,14
M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14
M_B_A[0..13] 8,15
M_B_BS[0..2] 8,15
M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15
M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15
M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53
Add Voltage Follower
+5V
+1.8V
R1601
10KOhm
C1627
0.1UF/16V
GND
T1601
M_VREF_MCH
U1601
V+
V-
LMV321IDBVR
C1628
0.01UF/50V
R1602
10KOhm
C1629
1UF/10V
c0603
GND
C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1601 C1613
c0402
0.1UF/10V
C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624 C1625 C1626
Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS
ASUSALPHA
Title : DDR2 TERM
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Monday, February 05, 2007
Sheet 16 of 57



ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUSALPHA
Title : ICH7-M (1/4)
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size: Custom
Project Name: TERESA
Rev: 1.1
Date: Monday, February 05, 2007
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PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

(061215)Add AND gates

0ohm replace AND gates

(061204)CRT H/VSYNC buffer circuit move to page-28

Modify USB Device table

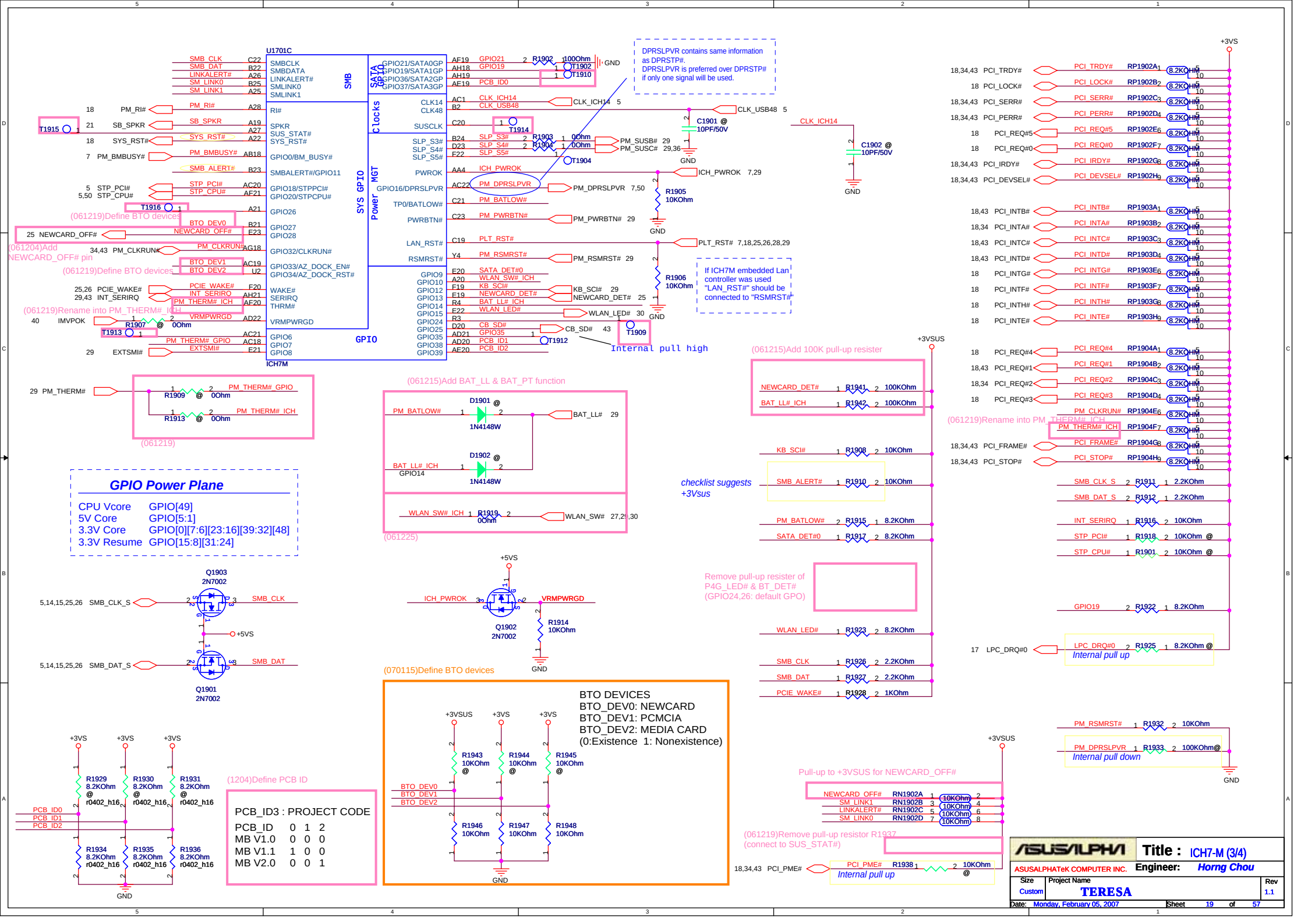
USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

Add test points

ASUSALPHATeK COMPUTER INC.	Title : ICH7-M (2/4)	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 18 of 57	


U1701C
ICH7M
SMB
SYS GPIO
Power MGT
Clocks
SATA GP
GPIO
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
SB_SPKR
SYS_RST#
PM_BMBUSY#
SMB_ALERT#
STP_PCI#
STP_CPU#
BTO_DEV0
NEWCARD_OFF#
PM_CLKRUN#
BTO_DEV1
BTO_DEV2
PCIE_WAKE#
INT_SERIRQ
PM_THERM# ICH
VRMPWRGD
EXTSMI#
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMBALERT#/GPIO11
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
CLK_ICH14
CLK_USB48
ICH_PWROK
PM_DPRSLPVR
PM_BATLOW#
PM_PWRBTN#
PLT_RST#
PM_RSMRST#
SATA_DET#0
WLAN_SW# ICH
KB_SCI#
NEWCARD_DET#
BAT_LL# ICH
WLAN_LED#
CB_SD#
PCB_ID1
PCB_ID2
GPIO1
GPIO19
PCB_ID0
R1902 100Ohm
T1902
T1910
T1914
R1903 0Ohm
R1904 0Ohm
T1904
R1905 10KOhm
R1906 10KOhm
T1909
T1912
C1901 @ 10PF/50V
C1902 @ 10PF/50V
GND
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
Internal pull high
(061219)Define BTO devices
(061204)Add NEWCARD_OFF# pin
(061219)Rename into PM_THERM#_ICH
R1907 @ 0Ohm
T1913
PM_THERM# R1909 @ 0Ohm
PM_THERM# R1913 @ 0Ohm
(061219)
(061215)Add BAT_LL & BAT_PT function
D1901 @ 1N4148W
D1902 @ 1N4148W
WLAN_SW# ICH R1919 0Ohm
(061225)
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
Q1903 2N7002
Q1901 2N7002
Q1902 2N7002
R1914 10KOhm
(070115)Define BTO devices
BTO DEVICES
BTO_DEV0: NEWCARD
BTO_DEV1: PCMCIA
BTO_DEV2: MEDIA CARD
(0:Existence 1: Nonexistence)
R1943 10KOhm @
R1944 10KOhm @
R1945 10KOhm @
R1946 10KOhm
R1947 10KOhm
R1948 10KOhm
(061215)Add 100K pull-up resister
NEWCARD_DET# R1941 100KOhm
BAT_LL# ICH R1942 100KOhm
checklist suggests +3Vsus
KB_SCI# R1908 10KOhm
SMB_ALERT# R1910 10KOhm
PM_BATLOW# R1915 8.2KOhm
SATA_DET#0 R1917 8.2KOhm
Remove pull-up resister of P4G_LED# & BT_DET# (GPIO24,26: default GPO)
WLAN_LED# R1923 8.2KOhm
SMB_CLK R1926 2.2KOhm
SMB_DAT R1927 2.2KOhm
PCIE_WAKE# R1928 1KOhm
(061219)Rename into PM_THERM#_ICH
SMB_CLK_S R1911 2.2KOhm
SMB_DAT_S R1912 2.2KOhm
INT_SERIRQ R1916 10KOhm
STP_PCI# R1918 10KOhm @
STP_CPU# R1901 10KOhm @
GPIO19 R1922 8.2KOhm
LPC_DRQ#0 R1925 8.2KOhm @
Internal pull up
PM_RSMRST# R1932 10KOhm
PM_DPRSLPVR R1933 100KOhm@
Internal pull down
Pull-up to +3VSUS for NEWCARD_OFF#
RN1902A RN1902B RN1902C RN1902D 10KOhm
(061219)Remove pull-up resistor R1937 (connect to SUS_STAT#)
PCI_PME# R1938 10KOhm @
Internal pull up
R1929 8.2KOhm @ r0402_h16
R1930 8.2KOhm @ r0402_h16
R1931 8.2KOhm @ r0402_h16
R1934 8.2KOhm r0402_h16
R1935 8.2KOhm r0402_h16
R1936 8.2KOhm r0402_h16
(1204)Define PCB ID
PCB_ID3 : PROJECT CODE
PCB_ID 0 1 2
MB V1.0 0 0 0
MB V1.1 1 0 0
MB V2.0 0 0 1
PCI_TRDY# RP1902A1
PCI_LOCK# RP1902B2
PCI_SERR# RP1902C3
PCI_PERR# RP1902D4
PCI_REQ#5 RP1902E6
PCI_REQ#0 RP1902F7
PCI_IRDY# RP1902G8
PCI_DEVSEL# RP1902H9
PCI_INTB# RP1903A1
PCI_INTA# RP1903B2
PCI_INTC# RP1903C3
PCI_INTD# RP1903D4
PCI_INTG# RP1903E6
PCI_INTF# RP1903F7
PCI_INTH# RP1903G8
PCI_INTE# RP1903H9
PCI_REQ#4 RP1904A1
PCI_REQ#1 RP1904B2
PCI_REQ#2 RP1904C3
PCI_REQ#3 RP1904D4
PM_CLKRUN# RP1904E6
PM_THERM# ICH RP1904F7
PCI_FRAME# RP1904G8
PCI_STOP# RP1904H9
8.2KOhm
ASUSALPHA
Title : ICH7-M (3/4)
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Monday, February 05, 2007
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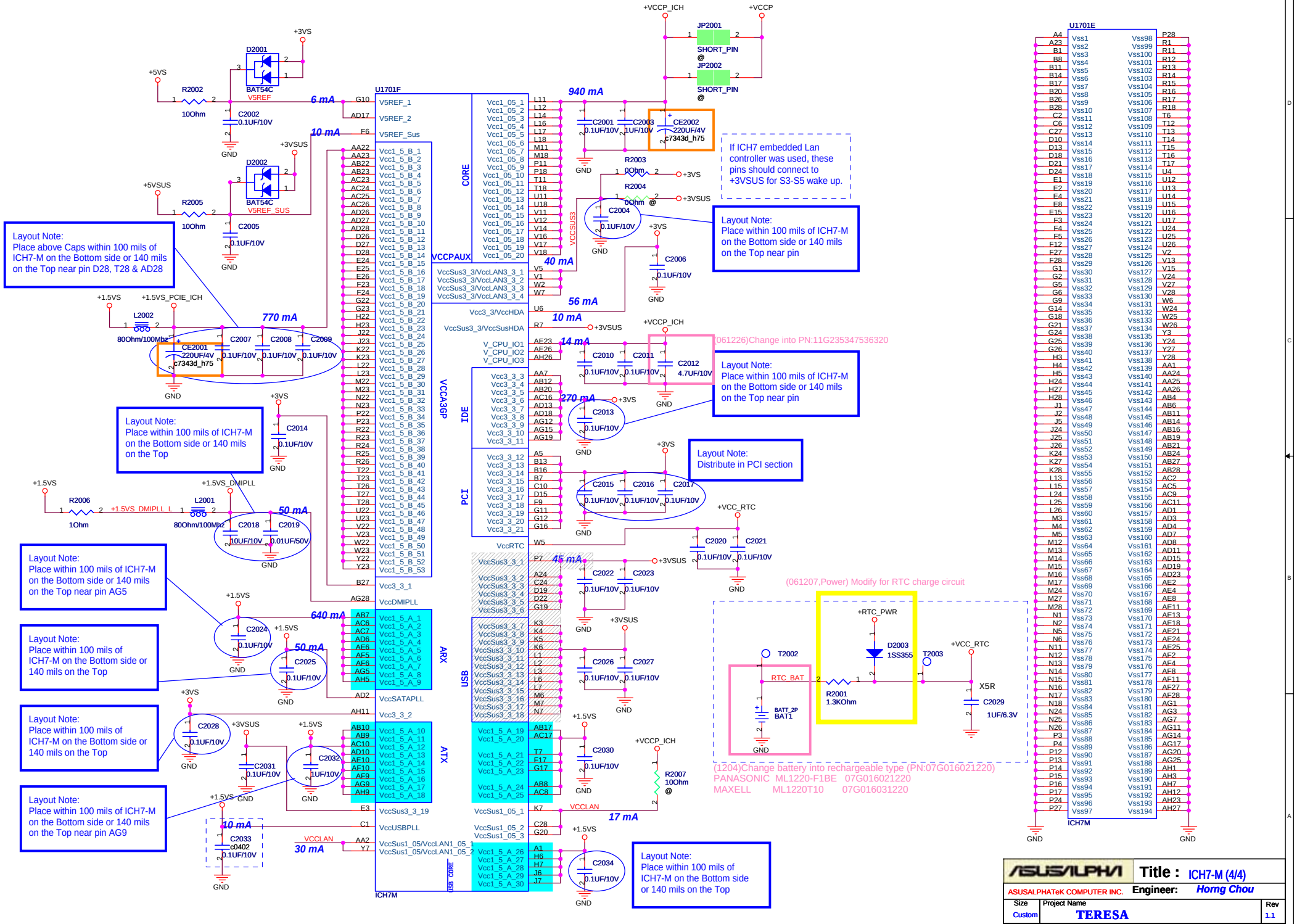
U1701F
ICH7M
U1701E
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ATX
Layout Note: Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note: Distribute in PCI section
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
(061226)Change into PN:11G235347536320
(061207,Power) Modify for RTC charge circuit
(1204)Change battery into rechargeable type (PN:07G016021220)
PANASONIC ML1220-F1BE 07G016021220
MAXELL ML1220T10 07G016031220
940 mA
56 mA
10 mA
14 mA
270 mA
770 mA
6 mA
10 mA
50 mA
640 mA
50 mA
45 mA
17 mA
10 mA
30 mA
Title : ICH7-M (4/4)
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size: Custom
Project Name: TERESA
Rev: 1.1
Date: Monday, February 05, 2007
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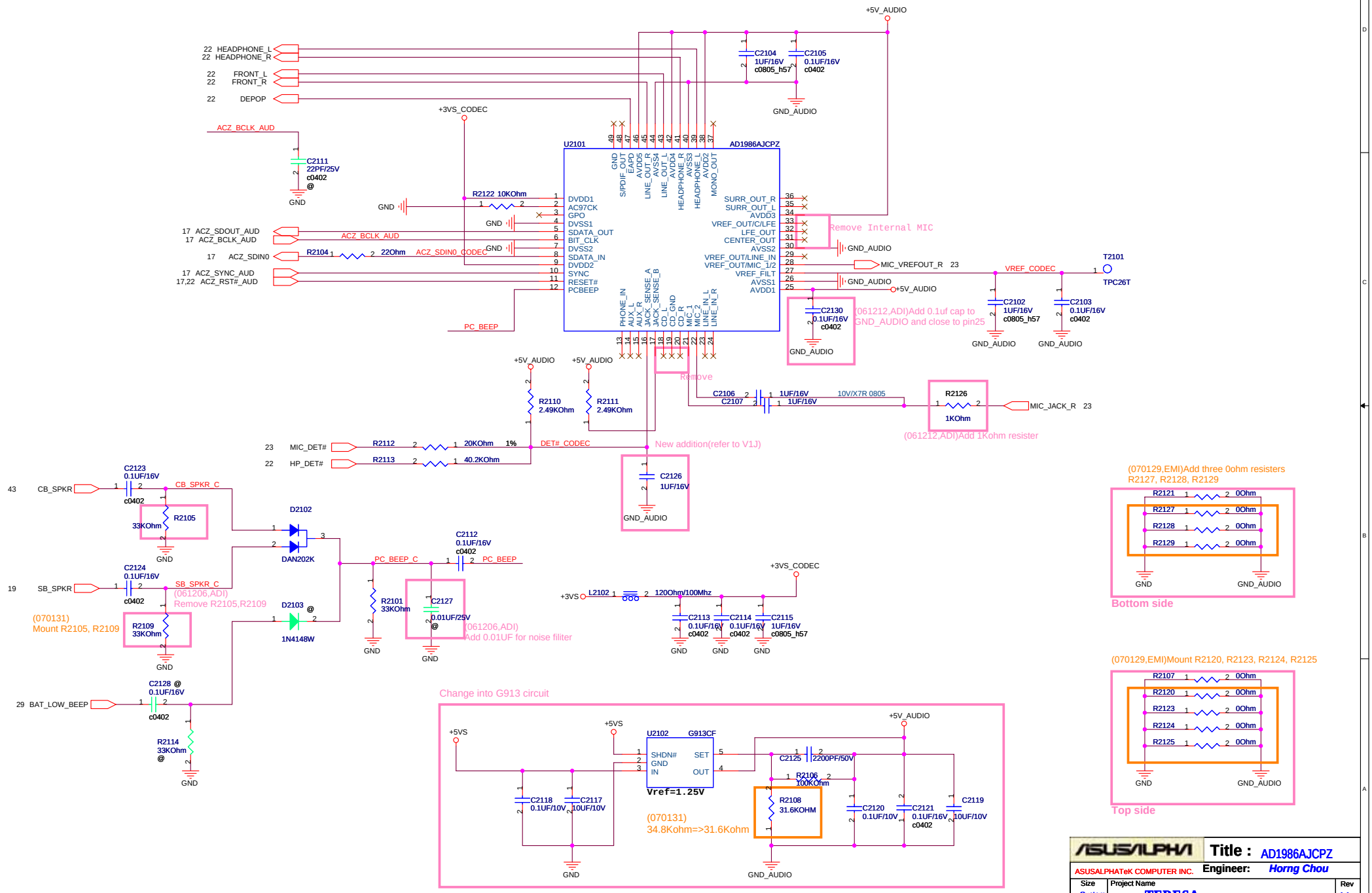


ASUSALPHATeK COMPUTER INC.	Title : AD1986AJCPZ	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 21 of 57	

(070126) Change R2201, R2202, R2203, R2204 into 27k ohm

Remove Woofer circuit

(070110)modify JACK_IN circuit

HP JACK

(061212,ADI) Placing Q2203, Q2205 on the other side of CE2202, CE2201

(070130,EMI)Add 4 Varistors(D2202~D2205)

(070117) change into 12G17100004F

(070117)Change Phone Jack into PN:12G14000106M

100PF/50V use 11G2330101043 11---change

Change for Layout

(061213,ADI)GND_JACK connect to GND_AUDIO directly

(061206,EMI) Add one 0ohm resister

(070129,EMI)Change 0ohm resisters into beads

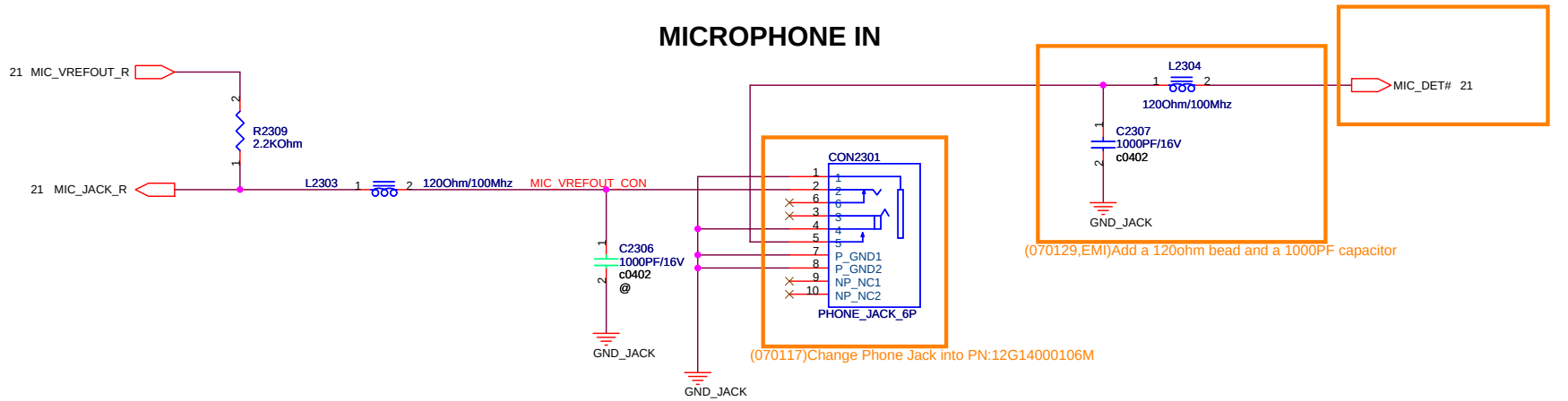
To Internal Speaker Connector

Title :	AUDIO AMP
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou
Size: Custom	Project Name: TERESA
Rev: 1.1	
Date: Monday, February 05, 2007	Sheet 22 of 57

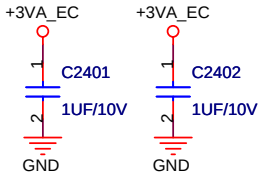
Remove Internal MIC pre-Amplifier

(070110)modify MIC_DET# circuit

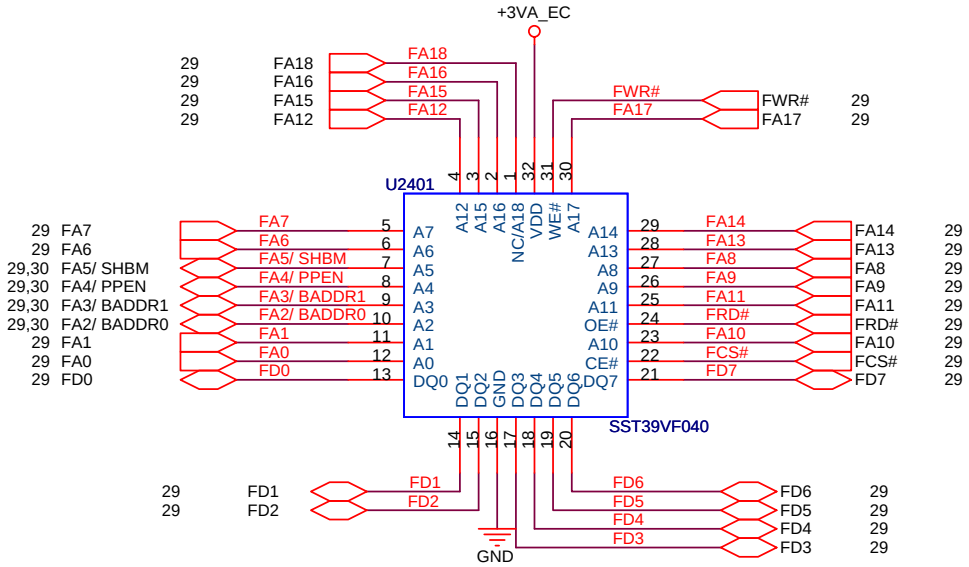
MICROPHONE IN



ASUSALPHA	Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 23 of 57	



ISA ROM

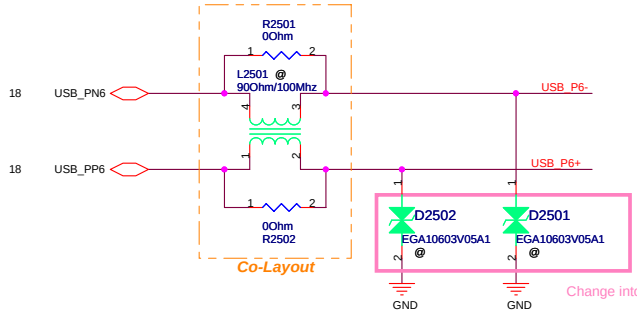


ASUSALPHA	Title : ISA ROM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 24 of 57	

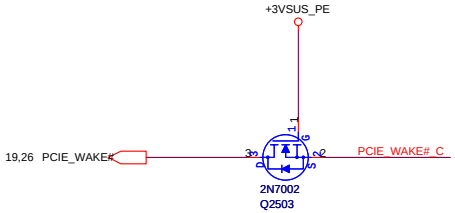
NewCard Header

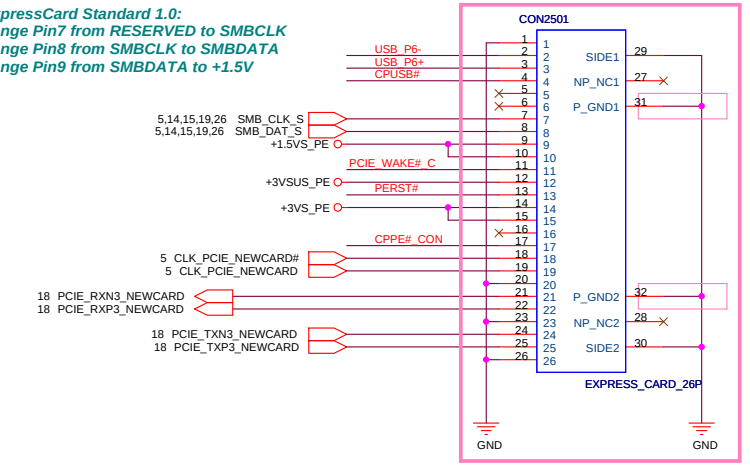
(061227)Change
Schematic Part=>EXPRESS_CARD_26P_6HOLD_SA
PCB Footprint=>nb_exp_card_26p_6hd_sa_lf2
PN=12G161300269

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



Change into PN:07G001122010

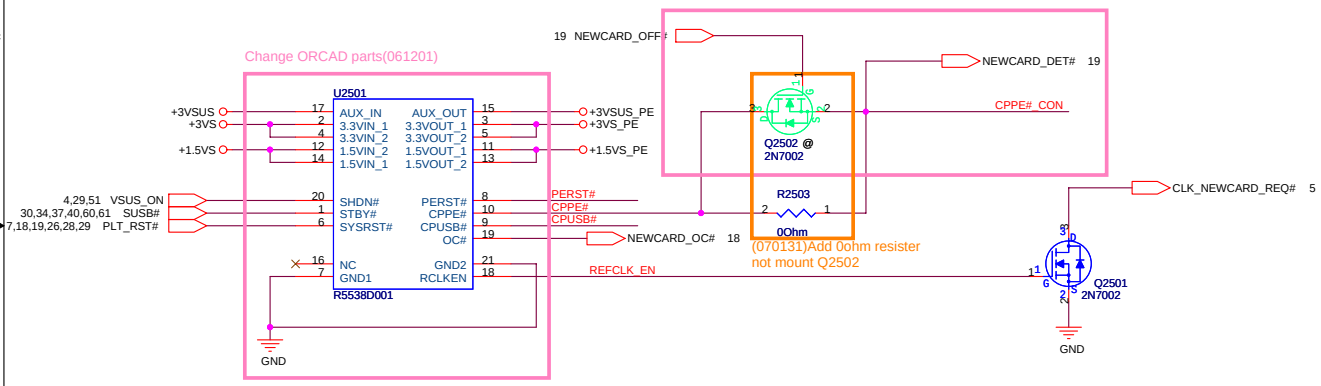




(061214)NewCard Ejector was combined into Header

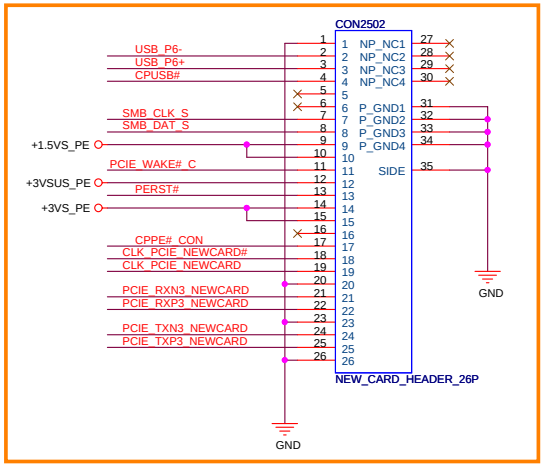
Refer to V1J(061201)

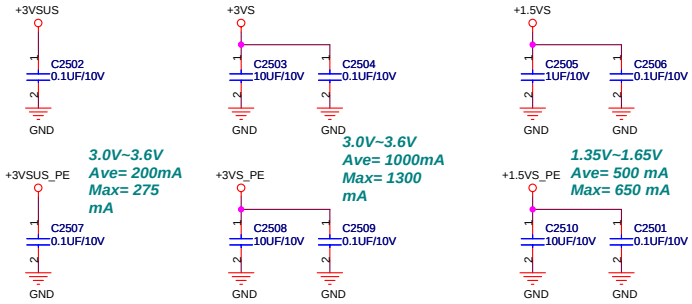
Change ORCAD parts(061201)



(070131)Add 0ohm resister
not mount Q2502

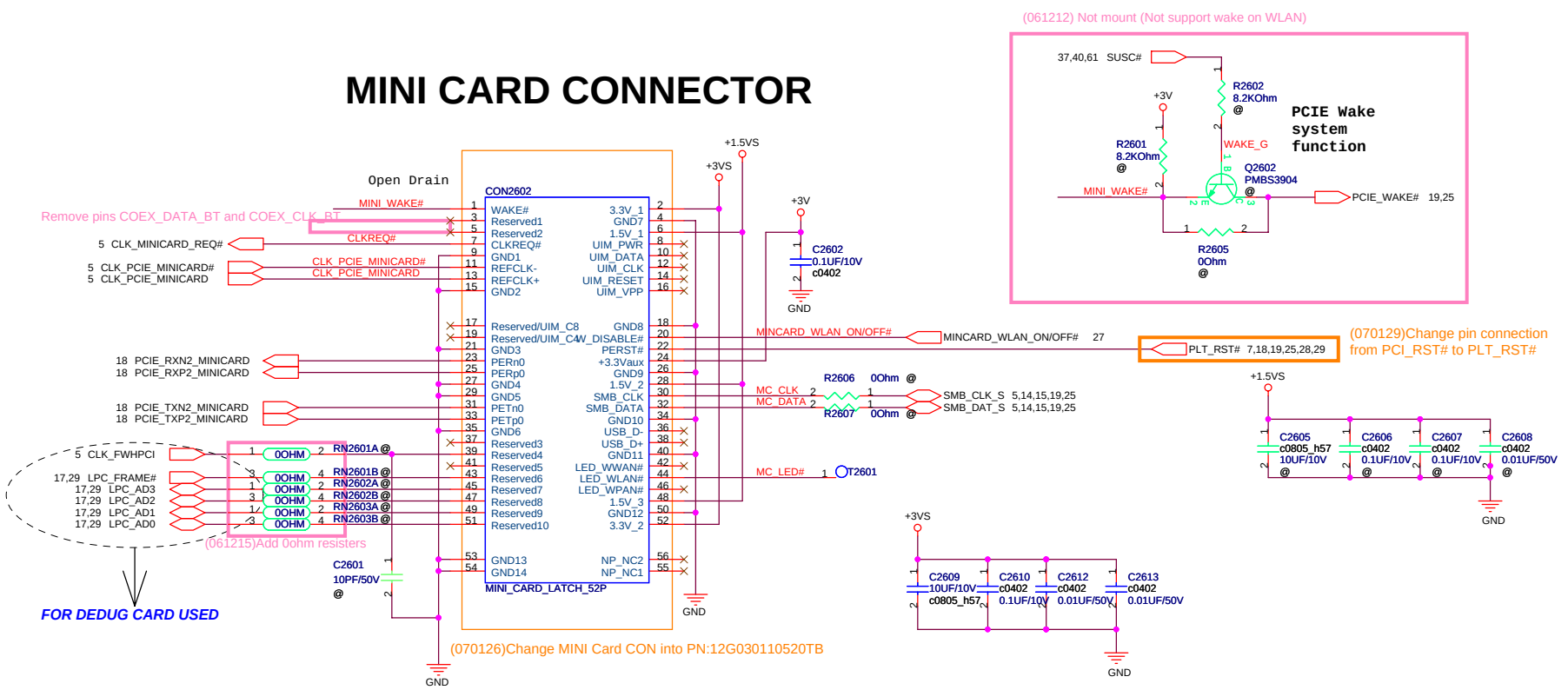
(070201)Add CON2502 in other to colayout with CON2501





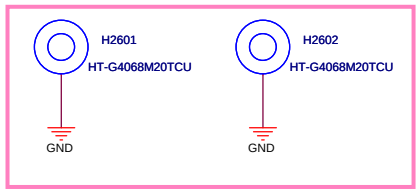
ASUSALPHA	Title : NEWCARD	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 25 of 57	

MINI CARD CONNECTOR



Check O/D output or push pull

Instead of Mini-PCIE latch connecter.For cost down.



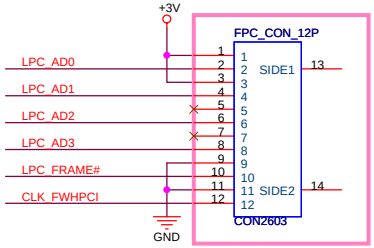
(070201)Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

Debug Card CON

(061206)Change Debug CON into PN:12G18340120E



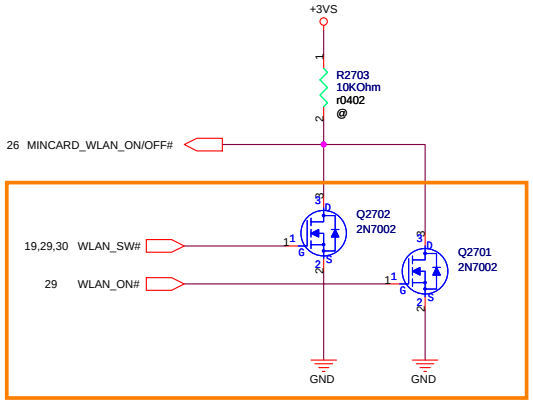
Title :	MINI PCIEX/DEBUG CON
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou
Size: Custom	Project Name: TERESA
Rev	1.1
Date: Monday, February 05, 2007	Sheet 26 of 57

For Bluetooth

Deltete Bluetooth CON

For Side SW

WLAN ON/OFF Control

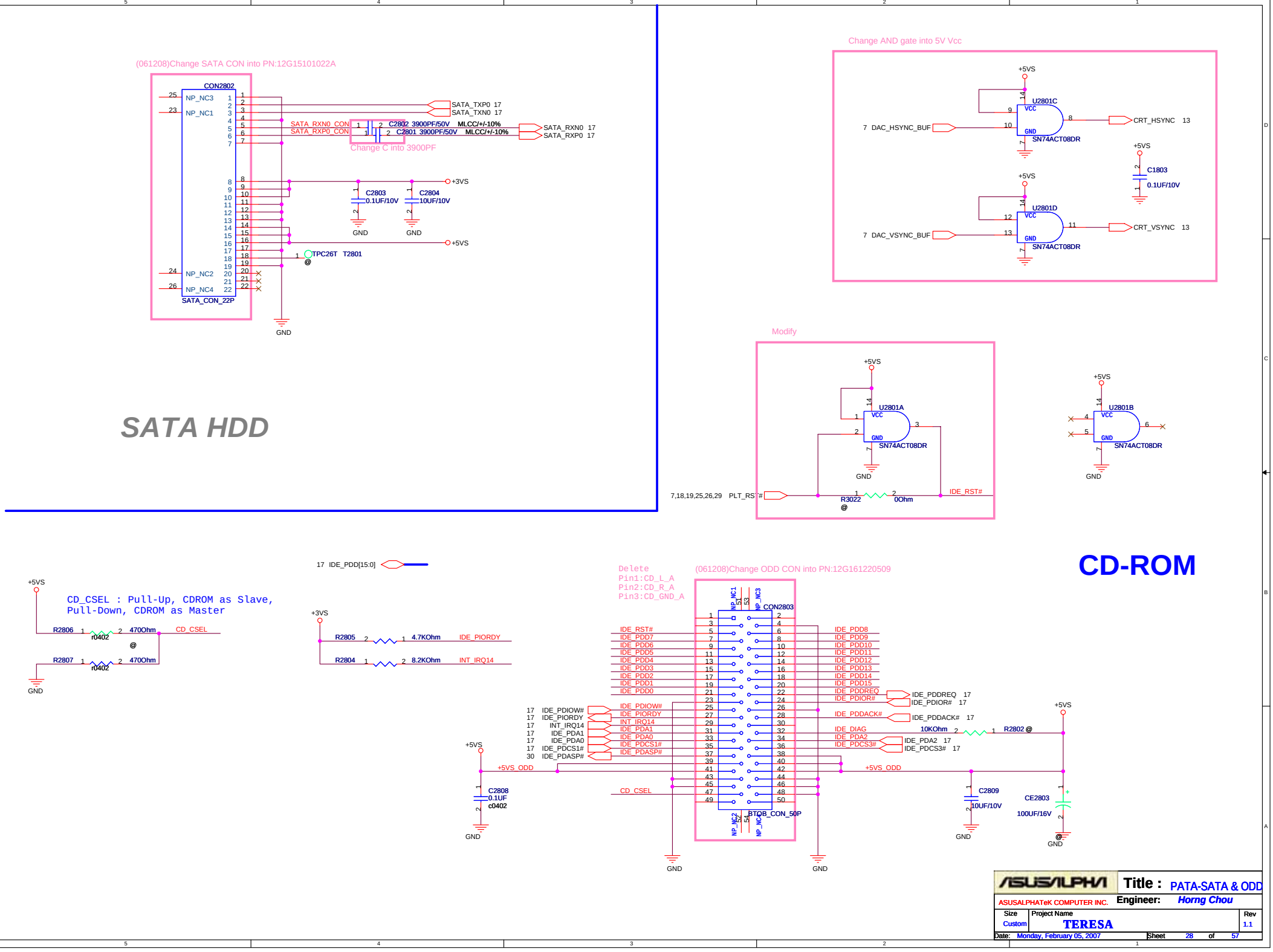


(070202)Modify WLAN on/off circuit

Deltete BT ON/OFF Control

Deltete FR Switch

ASUSALPHA	Title : WLAN CONTROL	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 27 of 57	


(061208)Change SATA CON into PN:12G15101022A
CON2802
NP_NC3
NP_NC1
NP_NC2
NP_NC4
SATA_CON_22P
SATA_TXP0 17
SATA_TXN0 17
SATA_RXN0_CON
SATA_RXP0_CON
C2802 3900PF/50V MLCC/+/-10%
C2801 3900PF/50V MLCC/+/-10%
Change C into 3900PF
SATA_RXN0 17
SATA_RXP0 17
C2803 0.1UF/10V
C2804 10UF/10V
+3VS
+5VS
GND
TPC26T T2801
SATA HDD
Change AND gate into 5V Vcc
U2801C
U2801D
SN74ACT08DR
7 DAC_HSYNC_BUF
CRT_HSYNC 13
7 DAC_VSYNC_BUF
CRT_VSYNC 13
C1803 0.1UF/10V
Modify
U2801A
U2801B
7,18,19,25,26,29 PLT_RST#
R3022 0Ohm
IDE_RST#
CD-ROM
17 IDE_PDD[15:0]
CD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master
R2806 r0402 470Ohm
R2807 r0402 470Ohm
R2805 4.7KOhm IDE_PIORDY
R2804 8.2KOhm INT_IRQ14
Delete
Pin1:CD_L_A
Pin2:CD_R_A
Pin3:CD_GND_A
(061208)Change ODD CON into PN:12G161220509
CON2803
BTOB_CON_50P
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDREQ
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
IDE_DIAG
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDASP#
10KOhm
R2802 @
+5VS_ODD
C2808 0.1UF c0402
C2809 10UF/10V
CE2803 100UF/16V
Title : PATA-SATA & ODD
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Monday, February 05, 2007
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TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

U2901 IT8511TE

Follow Z94 Keyboard

CON2901 FPC_CON_28P

to Battery

to Thermal

(061222)Remove netname pin 1 pin 47 pin 171

(061215)Add CHG_FULL_LED#_EC pin

Delete pull-up resisters: DJ_SW#, BT_ON#

Remove MARATHON# & DISTP#, but need to be pulled up

(061214)Remove PWRLMT#

(061222)Change pin48,148 netname

watchdog

Option1:
Mount R2926, R2918, C2917, D2904
Not mount C2910, C2912, U2902
Option 2:
Mount C2910, C2912, U2902
Not mount R2926, R2918, C2917, D2904

(070131)change into 1%

(070131)change into 10%

Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms

(070202)Connect to +3VSUS

close to EC

Cload=12.5PF

(061219)New addition

(061215)Add BAT_PT# pin and pull-up to +3VA_EC

(061215)Add ID pin

(061222)Add pin86 netname

Add test point

Layout Note: Close to Switch

(0611222) Modify into input port

(0611213)Keyboard pin definition is the same as F3 series PN=12G182402806

Title :	EC IT8511TE
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou
Size: Custom	Project Name: TERESA
Rev:	1.1
Date: Monday, February 05, 2007	Sheet 29 of 57

EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

+3VA_EC
R3002 @ 10KOhm r0402
FA2/ BADDR0
FA2/ BADDR0 24,29
R3006 10KOhm r0402
GND

+3VA_EC
R3003 10KOhm r0402
FA3/ BADDR1
FA3/ BADDR1 24,29
R3007 @ 10KOhm r0402
GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory

+3VA_EC
R3010 10KOhm r0402
FA5/ SHBM
FA5/ SHBM 24,29
R3013 @ 10KOhm r0402
GND

+3VA_EC
R3001 @ 10KOhm r0402
FA4/ PPEN
FA4/ PPEN 24,29
R3014 10KOhm r0402
GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

EC ADC

Battery

BAT
16.8V
R3004 @ 18KOhm r0402_h16
BAT0_R_AD
R3005 @ 1KOhm
R3008 @ 3.92KOhm
GND
+3VACC
D3002 @ 1N4148W
D3003 @ 1N4148W
C3002 @ 0.1UF/10V c0402
BAT0_AD 29

Adaptor

A/D_DOCK_IN
19V
R3009 @ 20KOhm
AC_R_AD
R3012 @ 3.74KOhm
GND
+3VACC
D3001 @ 1N4148W
R3011 @ 1KOhm
D3004 @ 1N4148W
C3003 @ 0.1UF/10V c0402
AC_AD 29
3V
2.99V

LED Board Interface

(070131,EMI)New addition for EMI
Connect to LED Board FFC
D3009 @ 0603-050E101NP-LF
GND
+5VSUS
+5V
(061219)New addition for EMI
C3008 0.01UF/25V
C3007 0.1UF/10V
GND
HDD_LED#
802_LED#_R
CHG_LED#_R
PWR_LED#_R
SUSPEND_LED#
R3024 0Ohm
R3025 0Ohm
R3026 0Ohm
R3027 0Ohm
R3028 0Ohm
R3029 0Ohm
R3030 0Ohm
CON3001
SIDE2
SIDE1
FPC_CON_12P
+5VS
+5VS_TP
L3002 80Ohm/100Mhz
C3006 0.1UF/10V
19,27,29 WLAN_SW#
WLAN_SW#
CHG_FULL_LED#
R3031 0Ohm
R3032 0Ohm
Change LED CON into PN:12G18340120E

Touchpad Board Interface

Connect to Touchpad Board FFC
+5VS_TP
29 TPAD_DAT
29 TPAD_CLK
C3009 0.1UF/10V
C3011 100PF/50V
C3012 100PF/50V
GNDGND
CON3002
SIDE2
SIDE1
FPC_CON_6P
(061215)Change TP CON into PN:12G18340060D
(070129,EMI)add two 100PF capacitors

HDD LED

+3VS
+5VS
R3019 10KOhm
R3020 10KOhm @
D3005
DAP202K @
D3008
1N4148W
17 SATA_LED#
28 IDE_PDASP#
HDD_LED#
(061212)Modify HDD LED circuit

(061201)Modify Charge & Power circuit

CHARGE LED

+5VSUS
R3015 10KOhm
CHG_LED#_R
ORANGE
T3001
Q3003 2N7002
Q3001 2N7002
29 CHG_LED_UP#
GND

Solution 1
+3VSUS
D3007 @ 1N4148W
R3021 @ 1MOhm
U3001 SN74AUP1G08DCKR @
C3010 1UF/16V @
Q3006 2N7002 @
Q3011 2N7002 @
29,57 CHG_EN#
29,59 ACIN_OC#
29,59 BAT_IN_OC#
GND

Solution 2
R3023 10KOhm
+5VSUS
29 CHG_FULL_LED#_EC
Q3007 2N7002
GND

CHG_FULL_LED#
GREEN
Q3005 2N7002
GND

POWER LED

25,34,37,40,60,61 SUSB#
+5V
D3006 1N4148W
R3017 10KOhm
PWR_LED#_R
GREEN
Q3008 2N7002
Q3002 2N7002
29 PWR_LED_UP#
GND

SUSPEND_LED#
ORANGE
Q3010 2N7002
GND

(061212)Modify charge full circuit : solution1 & solution2

WLAN LED

+5VS
R3016 10KOhm
802_LED#_R
Q3009 2N7002
Q3004 2N7002
Remove 0ohm
Remove RF_LED pin
19 WLAN_LED#
GND

ASUSALPHATeK COMPUTER INC.
Title : EC IT8511/LED&TP CON.
Engineer: Horng Chou
Size: Custom
Project Name: TERESA
Rev: 1.1
Date: Monday, February 05, 2007
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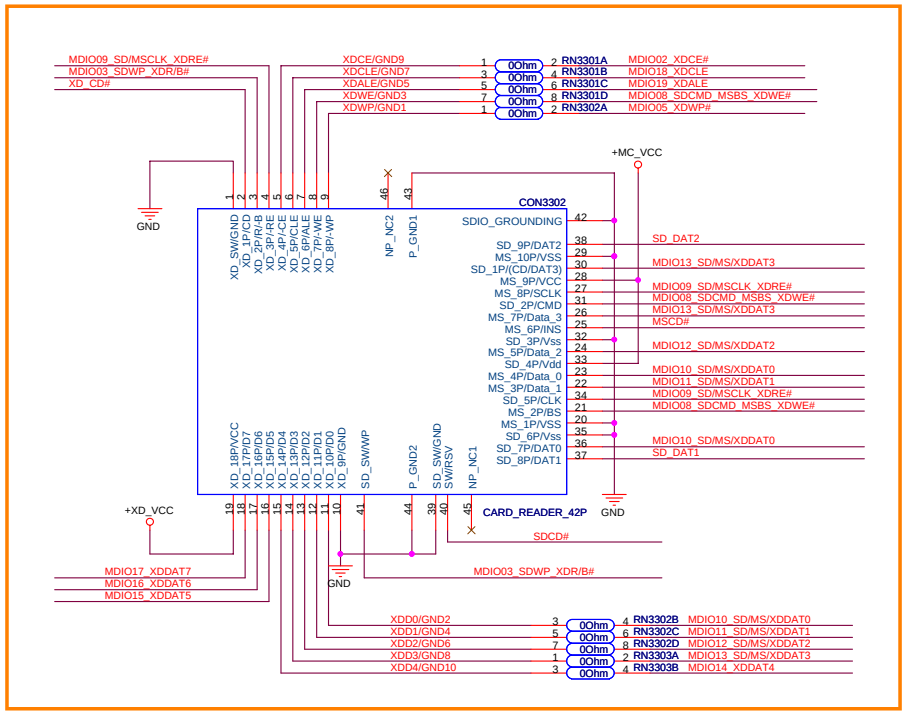
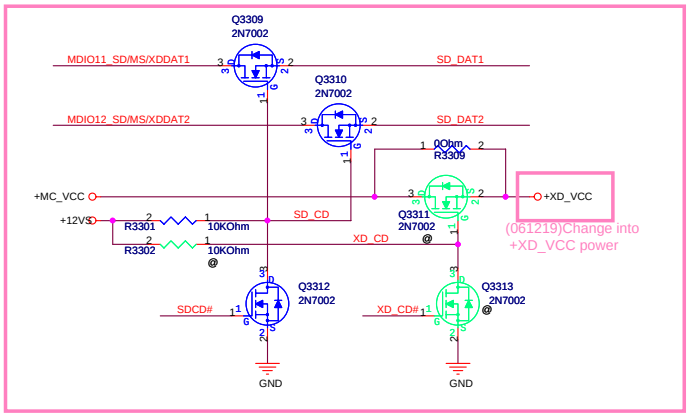
MEDIA CARD SLOT

(070124)Add Media Card CON for colayout

(070130)Add RN3301, RN3302, RN3303



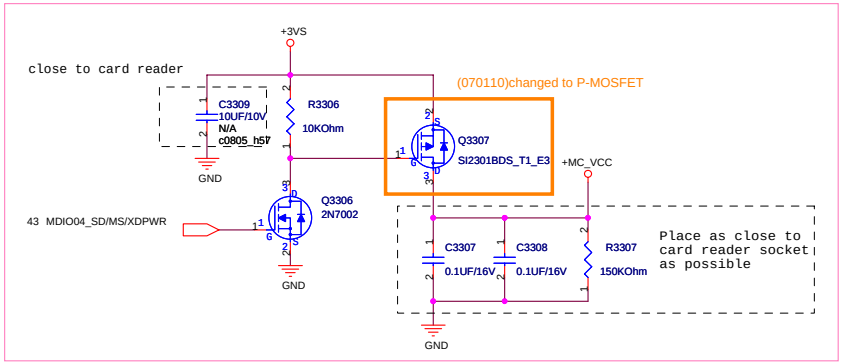
Solve-MS Duo Adaptor short problem / XD short problem



Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Change circuit from AAT4610A to SI2301

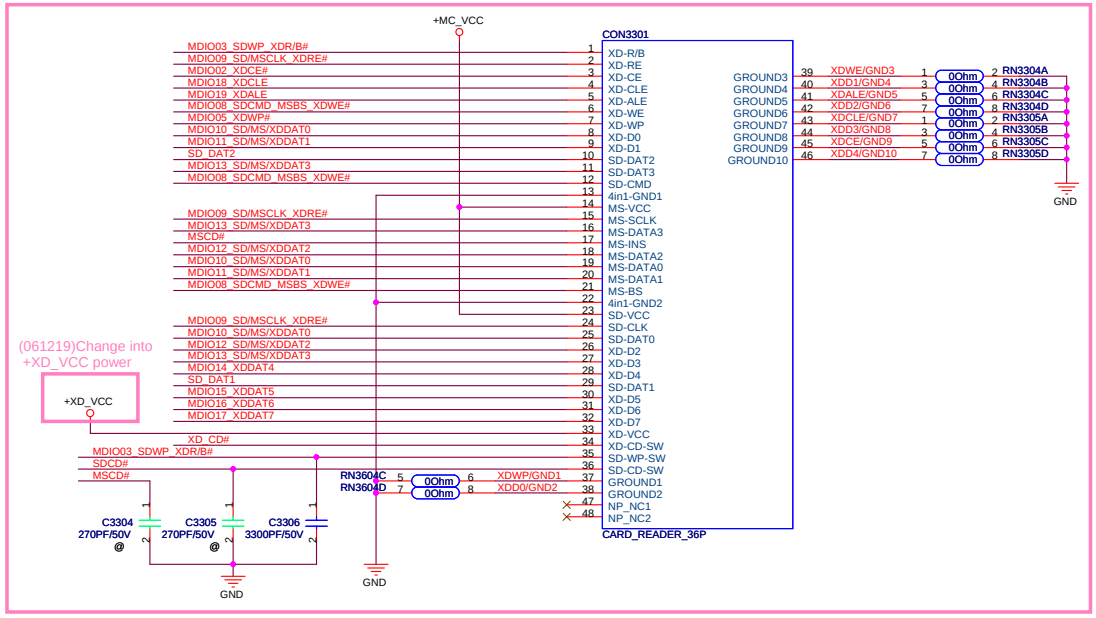


MEDIA CARD SLOT

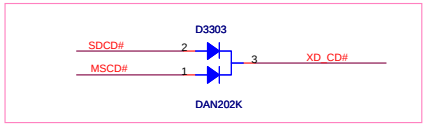
(061208)Change CON3301 into PN:12G340003601

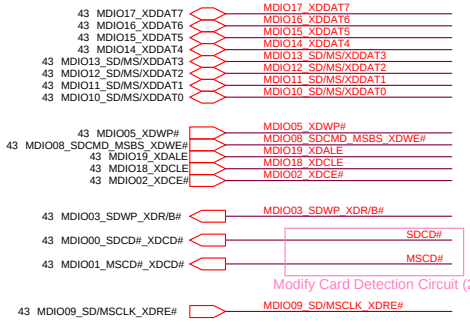
(061225)Change schematic part & PCB Footprint

(070130)Add RN3303, RN3304, RN3305



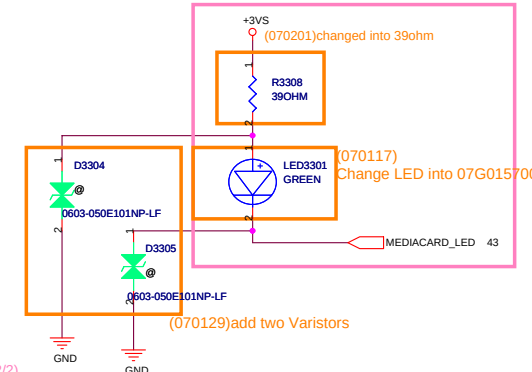
Modify Card Detection Circuit (1/2)





Modify Card Detection Circuit (2/2)

(161219)Change reference into R3308&LED3301



ASUSALPHA	Title : MEDIA CARD SLOT		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 33 of 57		

Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3

R3412 0Ohm @ — GND
(061207,REALTEK)Connect 0ohm to GND

PCI_AD[0..31] 18,43

18,43 PCI_C/BE#0 — PCI_C/BE#0

+3VSUS, DVDD

PCI_C/BE#1 — PCI_C/BE#1 18,43
PCI_PAR — PCI_PAR 18,43
PCI_SERR# — PCI_SERR# 18,19,43
PCI_PERR# — PCI_PERR# 18,19,43
PCI_STOP# — PCI_STOP# 18,19,43
PCI_DEVSEL# — PCI_DEVSEL# 18,19,43
PCI_TRDY# — PCI_TRDY# 18,19,43
CLKRUN — PM_CLKRUN# 19,43

R3402 @ 0Ohm r0402

U3401 RTL8100CL

PCI_IRDY# — PCI_IRDY# 18,19,43
PCI_FRAME# — PCI_FRAME# 18,19,43
PCI_C/BE#2 — PCI_C/BE#2 18,43
PCI_C/BE#3 — PCI_C/BE#3 18,43

R3407 33Ohm — PCI_AD23

R3408 need close to LAN chip
R3408 5.6KOhm 1% — LAN_RSET

XTAL1, XTAL2

L_TDP, L_TDN, L_RDP, L_RDN, CTRL25

C3405 0.1UF/10V c0402

PCI_INTA# 18,19
PCI_RST# 12,18,43
CLK_LAN_PCI 5

PCI_PME# 18,19,43
PCI_REQ#2 18,19
PCI_GNT#2 18

C3408 @ 10PF/50V c0402

R3410 1KOhm 1% — +5VS
R3409 0Ohm @
R3411 15KOhm 1%

25,30,37,40,60,61 SUSB# — SUSB#

(061207,REALTEK)Add voltage divider

Layout Note:
L_TDP, L_TDN termination resistors should be near chip

C3402 0.01UF/25V c0402
LAN_T_T — R3403 49.9Ohm 1% r0402 — L_TDP
R3404 49.9Ohm 1% r0402 — L_TDN

C3403 0.01UF/25V c0402
LAN_T_R — R3405 49.9Ohm 1% r0402 — L_RDP
R3401 49.9Ohm 1% r0402 — L_RDN

Layout Note:
L_RDP, L_RDN termination resistors should be near transformer

R3406 3.6KOhm r0402_h16

U3402 AT93C46
EECS, EESK, EEDI/AUX, EEDO

C3404 0.1UF/10V c0402

(061207)Change to PN:07G010Q12500

X3401 25Mhz
C3406 30PF/50V
C3407 30PF/50V

(070131)change into 30PF

Q3401 MW772M3L 07G003231011
CTRL25

Change trace wide into 30mil
30 mil

C3417 10UF/10V c0805_h57
C3418 c0402 0.1UF/10V
C3419 c0402 0.1UF/10V
C3420 c0402 0.1UF/10V
C3421 c0402 0.1UF/10V

(061207,REALTEK)Recommend change to 22UF

L3401 120Ohm/100Mhz
20 mil

C3414 c0402 0.1UF/10V
C3415 c0402 0.1UF/10V
C3416 c0402 0.1UF/10V

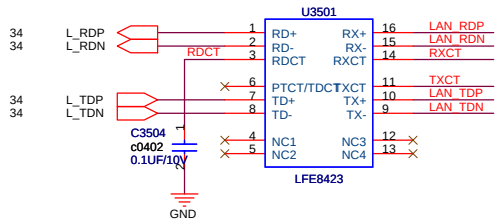
C3409 c0402 0.1UF/10V
30 mil
C3410 10UF/10V c0805_h57
C3401 c0402 0.1UF/10V
C3411 c0402 0.1UF/10V
C3412 c0402 0.1UF/10V
C3413 c0402 0.1UF/10V

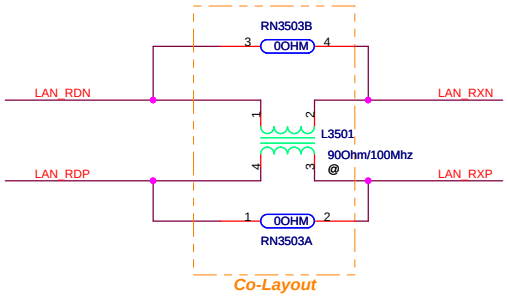
(061207,REALTEK)Remove capacitors

ASUSALPHA
Title : LAN_RTL8100CL
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou
Size: Custom | Project Name: TERESA | Rev: 1.1
Date: Monday, February 05, 2007 | Sheet 34 of 57

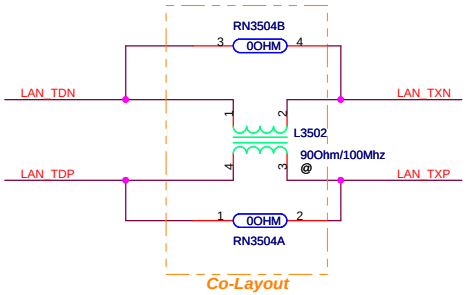
LAN PORT

TRANSFORMER 10/100MB

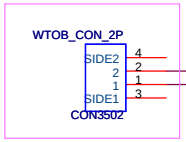




Co-Layout



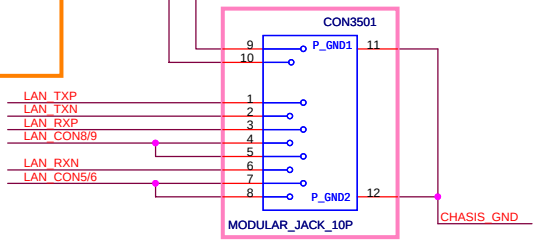
Co-Layout



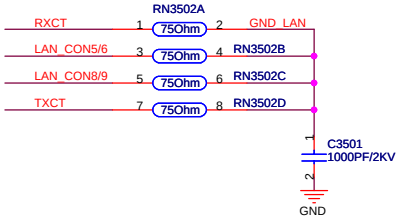
(061214)Change CON3502 into PN:12G17000002B

(070131)place C3502, C3503 on the other side of L3503, L3504

RJ11&RJ45



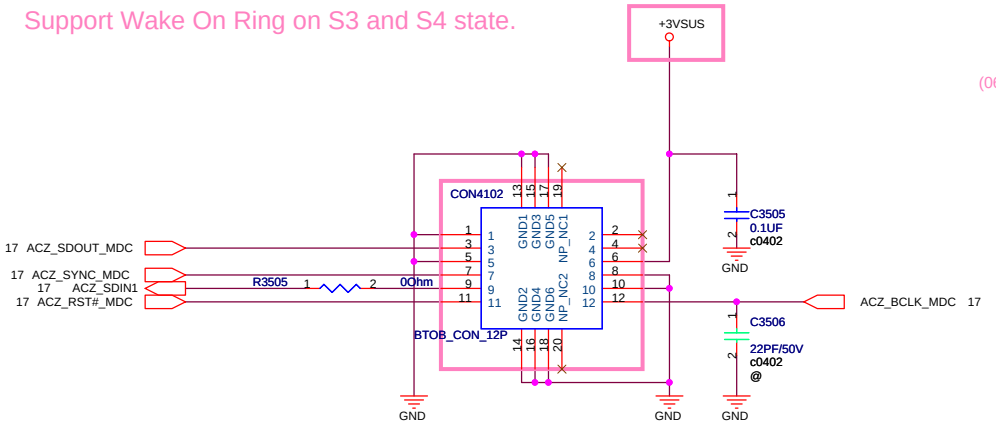
(061214)Change RJ11&RJ45 into PN:12G142011109



MDC CONNECTOR

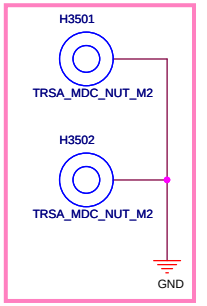
Support Wake On Ring on S3 and S4 state.

Change power from +3V to +3VSUS



B:MDC NUT

(061219)Change MDC NUT into PN:13G021054000



(061214)Change MDC CON into PN:12G16020012D

ASUSALPHA	Title : RJ45/RJ11/MDC	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
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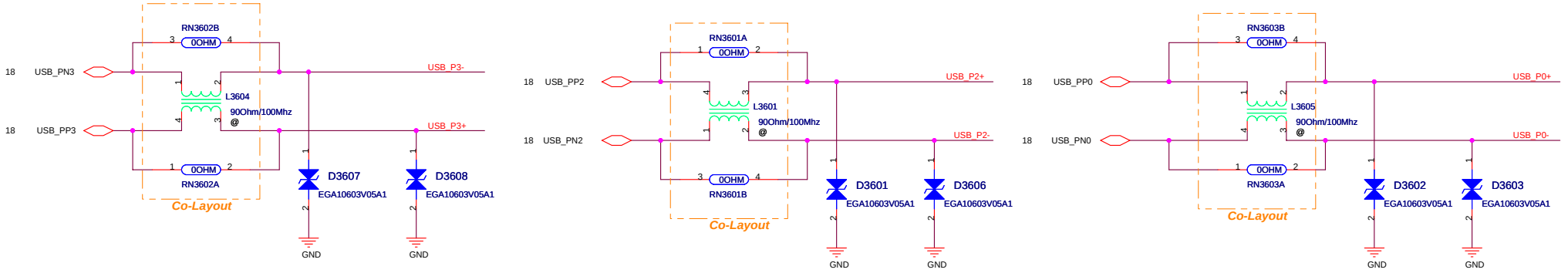
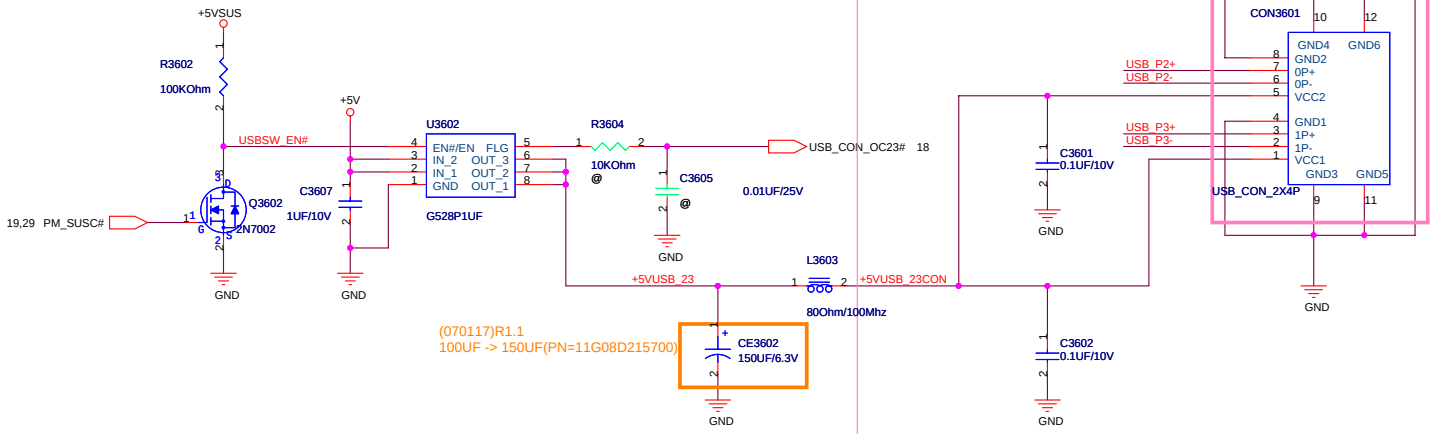


Delete N-MOSFET PMN45EN

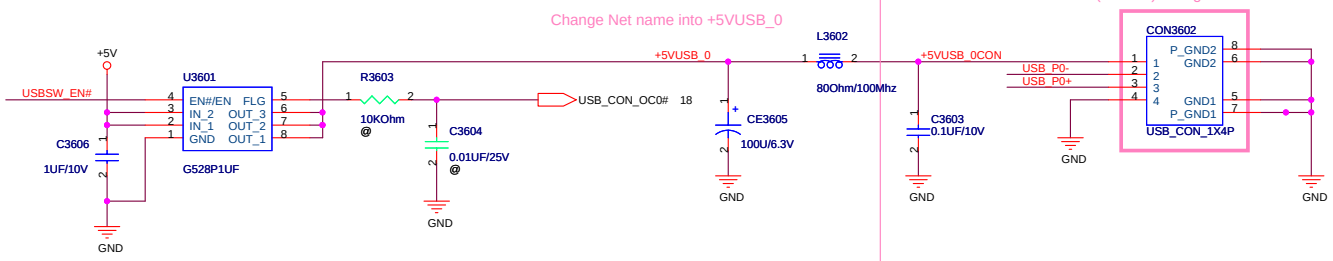
Add USB Switch

(061211)Change USB CON into PN:12G13111108F

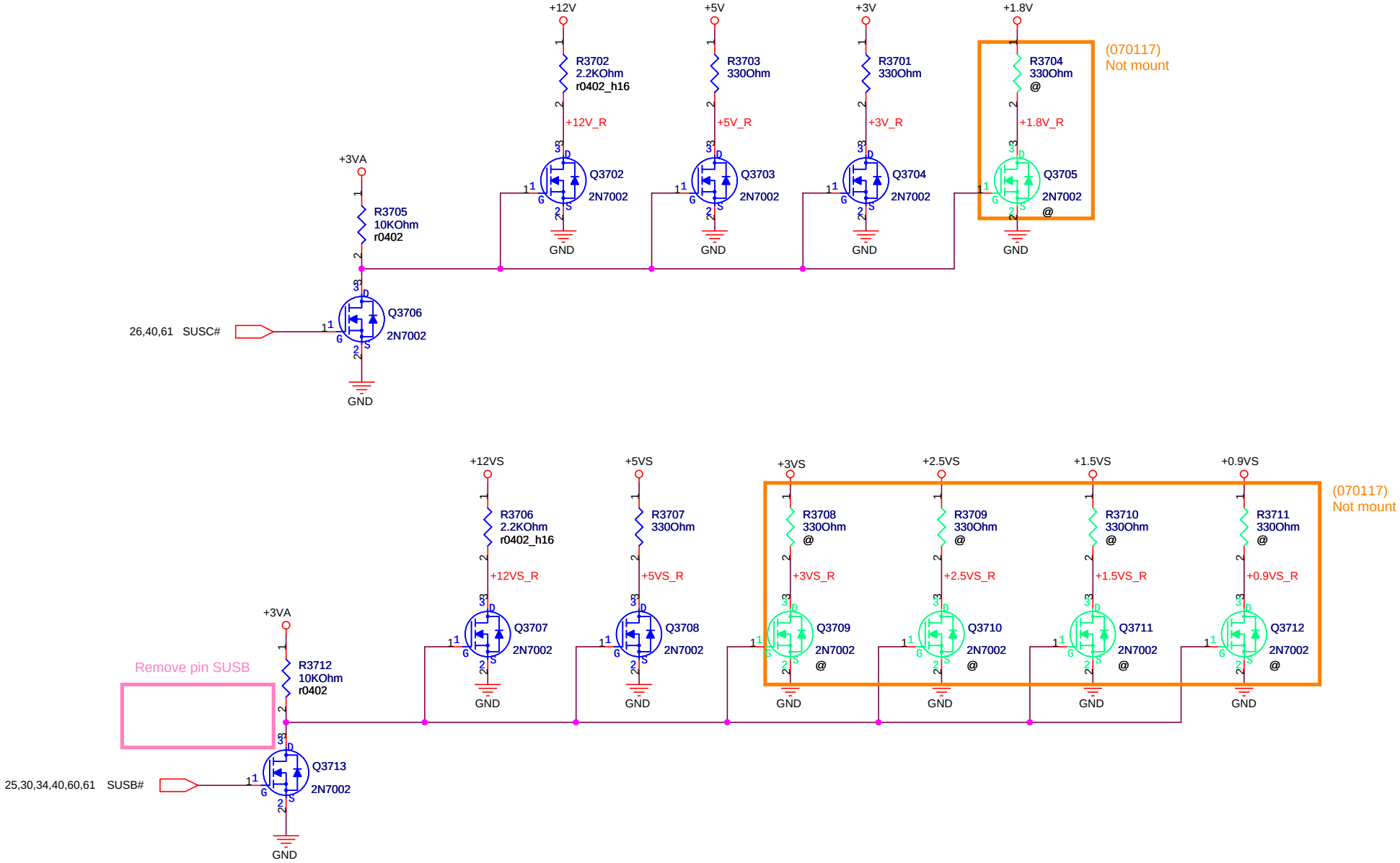


Change Net name into +5VUSB_0

(061206)Change USB CON into PN:12G131030043



ASUSALPHA	Title : USB CONN x3		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 36 of 57		



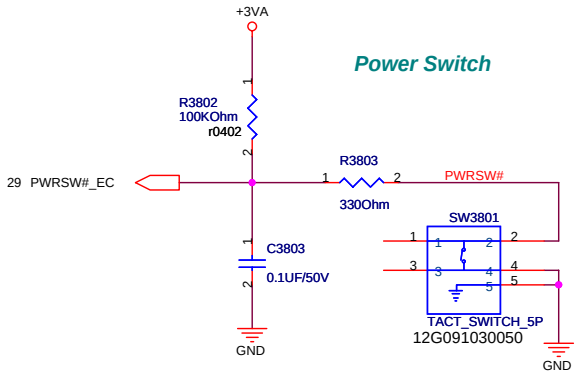
ASUSALPHA	Title : Discharge Circuit	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 37 of 57	

Main Board SW & LED

Delete RF/Touchpad and Power4 Gear SWITCH

Power LED move to daughter board

Power Switch

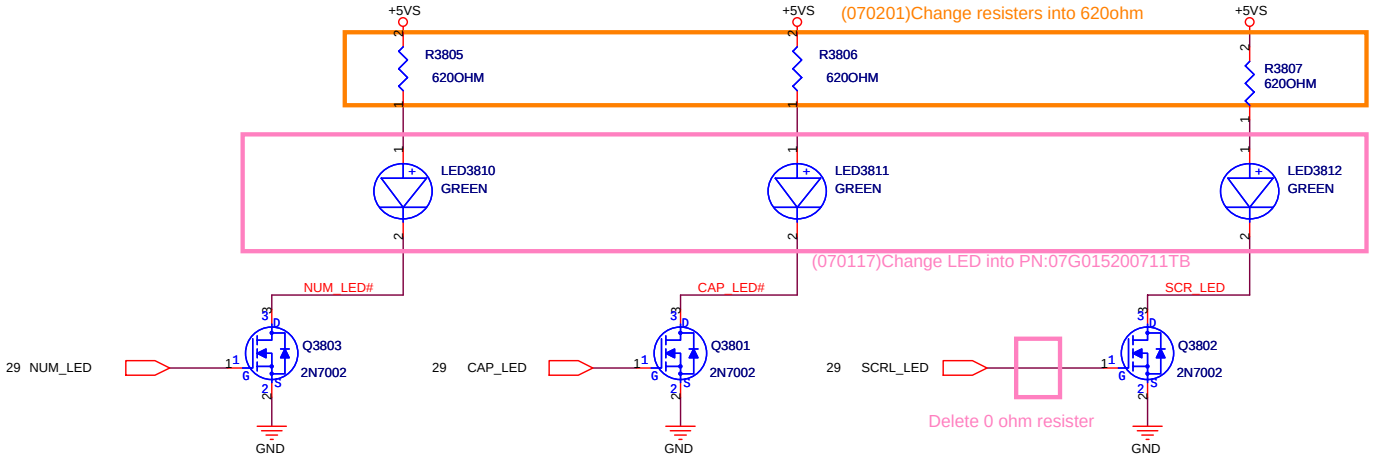


Delete RF LED and Power4 Gear LED

NUMBER LOCK LED

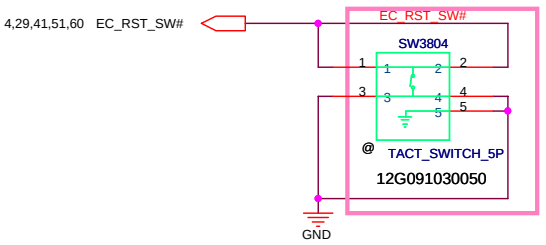
CAPS LOCK LED

SCROLL LOCK LED

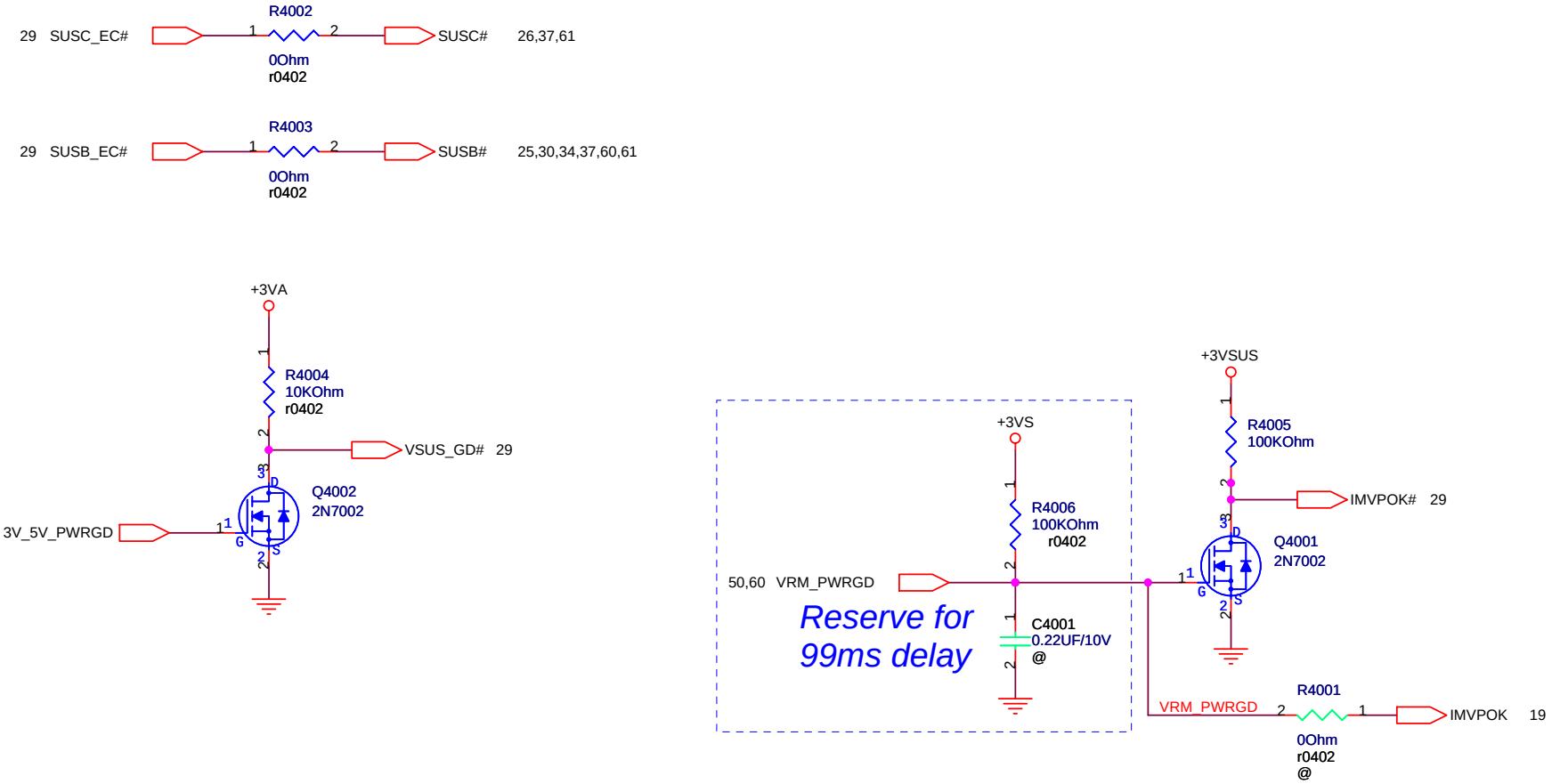


Reset Switch

SW does not mount

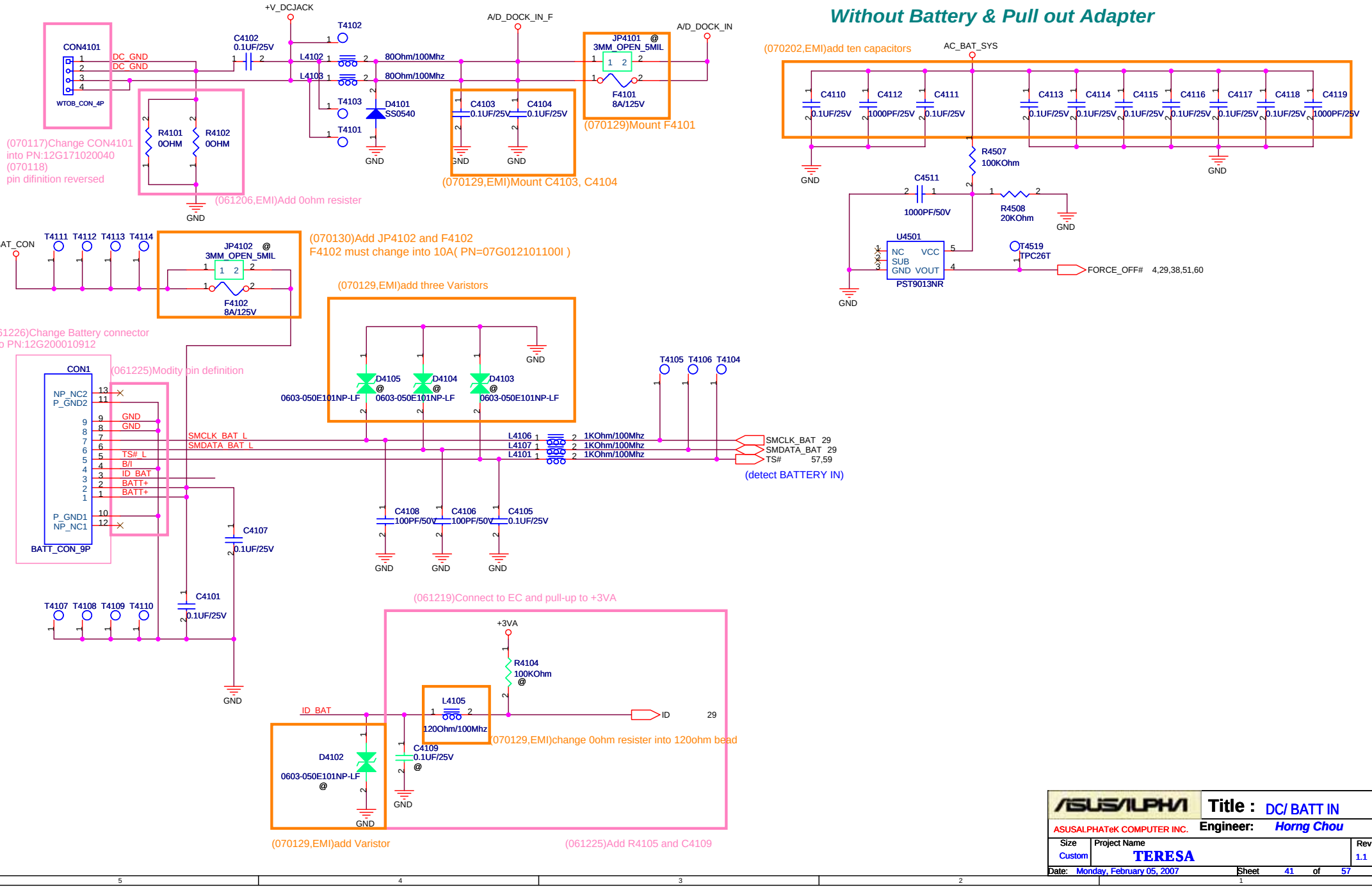


ASUSALPHA	Title : SW/LED	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 38 of 57	

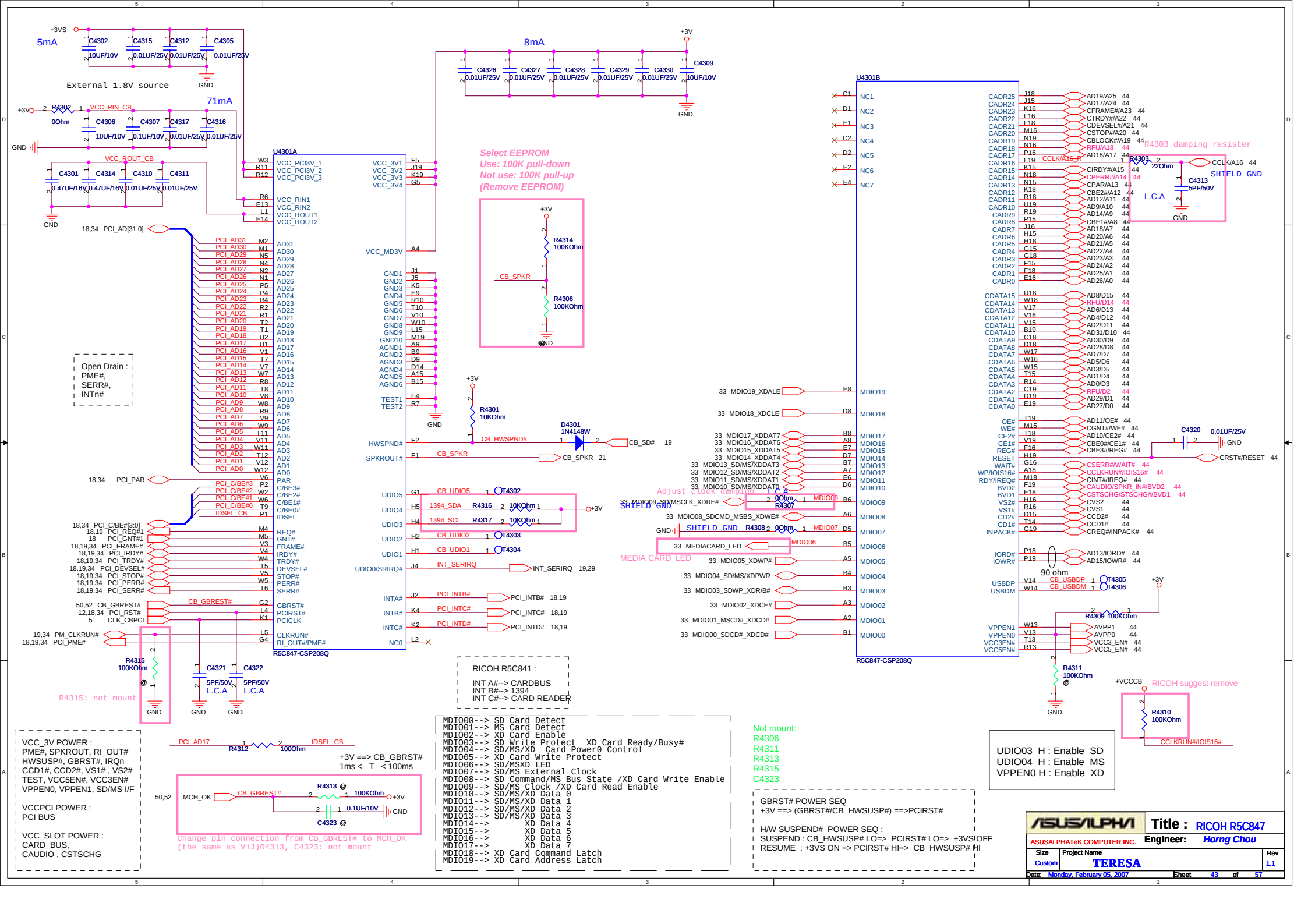


ASUSALPHA	Title : POWER-ON SEQ.	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 40 of 57	

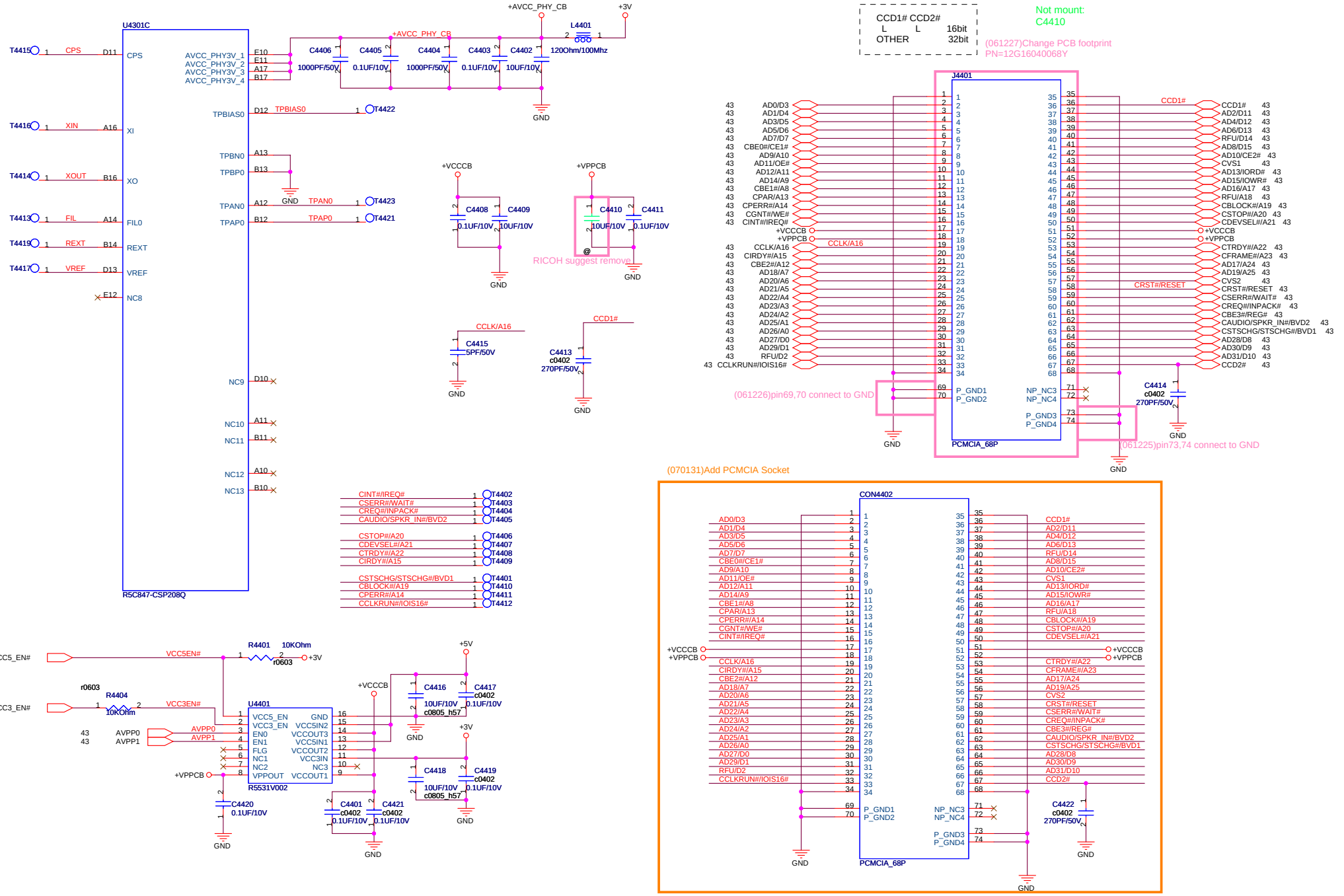
DC Power Jack



ASUSALPHA	Title : DC/ BATT IN	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 41 of 57	


5mA
8mA
71mA
External 1.8V source
U4301A
R5C847-CSP208Q
U4301B
R5C847-CSP208Q
Select EEPROM
Use: 100K pull-down
Not use: 100K pull-up
(Remove EEPROM)
Open Drain : PME#, SERR#, INTn#
R4303 damping resister
SHIELD GND
L.C.A
Adjust clock damping
MEDIA CARD_LED
90 ohm
RICOH suggest remove
R4315: not mount
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
Not mount:
R4306
R4311
R4313
R4315
C4323
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
Change pin connection from CB_GBREST# to MCH_OK
(the same as V1J)R4313, C4323: not mount
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
Title : RICOH R5C847
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Project Name: TERESA
Size: Custom
Rev: 1.1
Date: Monday, February 05, 2007
Sheet 43 of 57

PCMCIA SOCKET



CCD1# CCD2#
L L 16bit
OTHER 32bit

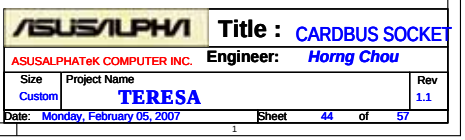
Not mount:
C4410

(061227)Change PCB footprint
PN=12G16040068Y

(061226)pin69,70 connect to GND

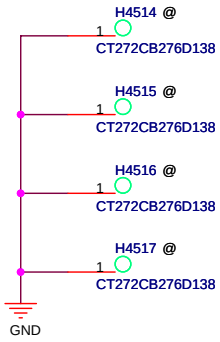
(061225)pin73,74 connect to GND

(070131)Add PCMCIA Socket



A:CPU BKT

PN:s01756



B:MDC NUT

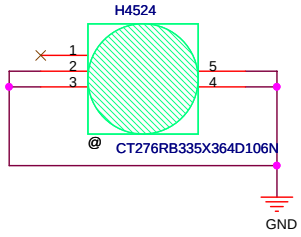
MDC NUT put on page35 (H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on page26(H2601, H2602)

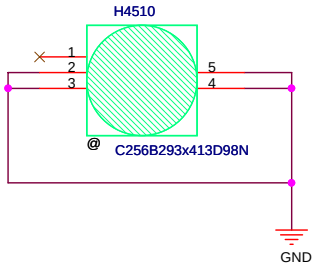
C:TOP TO BTM

PN:S01912



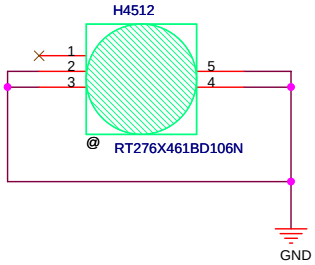
D:FIX MB

PN:s01769



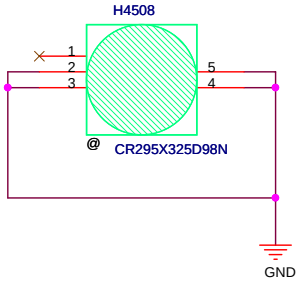
E:TOP TO BTM

PN:S01911



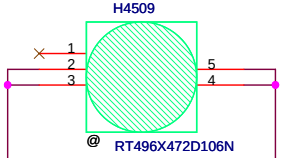
G:FIX MB

PN:s01783



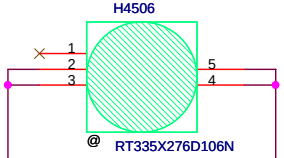
H:SYS BOSS

PN:S01914



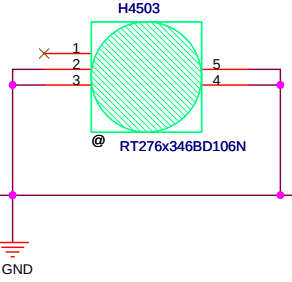
I:MB TO IO BKT

PN:S01913



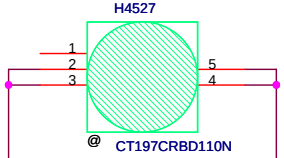
J:SYS BOSS

PN:S01915



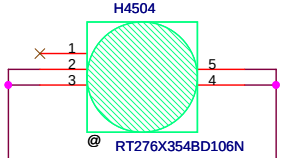
K:MB TO IO BKT

PN:S01705



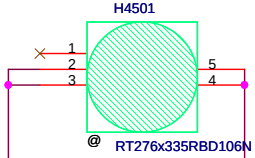
L:TOP TO BTM

PN:S01916



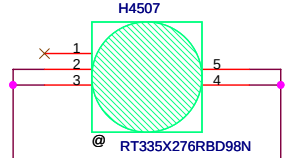
M:SYS BOSS

PN:s01917



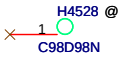
N:TOP TO BTM

PN:S01851



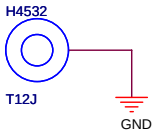
O:ALIGNMENT HOLE

PN:temp_5262_gh15



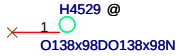
T:NB SINK NUT

PN:13GNJ510M170-1



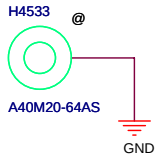
P:ALIGNMENT HOLE

PN:s01724



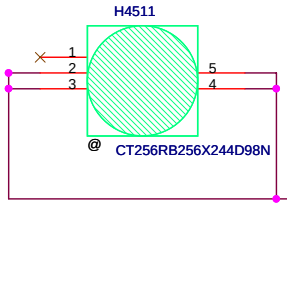
EMI NUT

for LVDS cable
PN:13G021029050



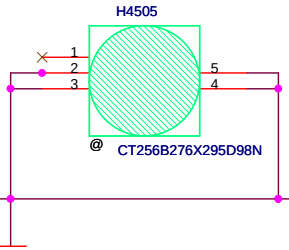
U:TOP TO BTM

PN:S01854



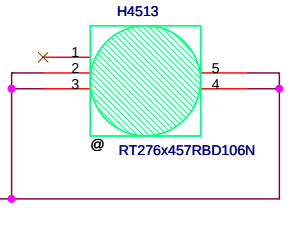
V:TOP TO BTM

PN:S01857



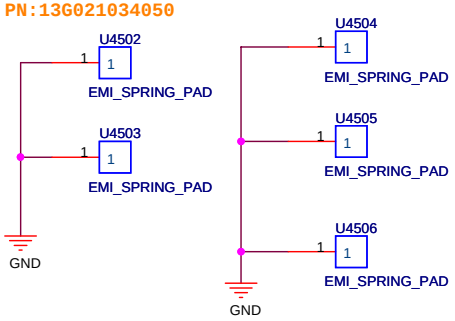
W:TOP TO BTM

PN:S01918



EMI SPRING

PN:13G021034050



ASUSALPHA	Title : SCREW HOLE	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 45 of 57	

R1.0 to R1.1

Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.

R1.1 to R1.2

Page	Action

R1.2 to R2.0

Page	Action	Reason

ASUSALPHA

Title : HISTORY

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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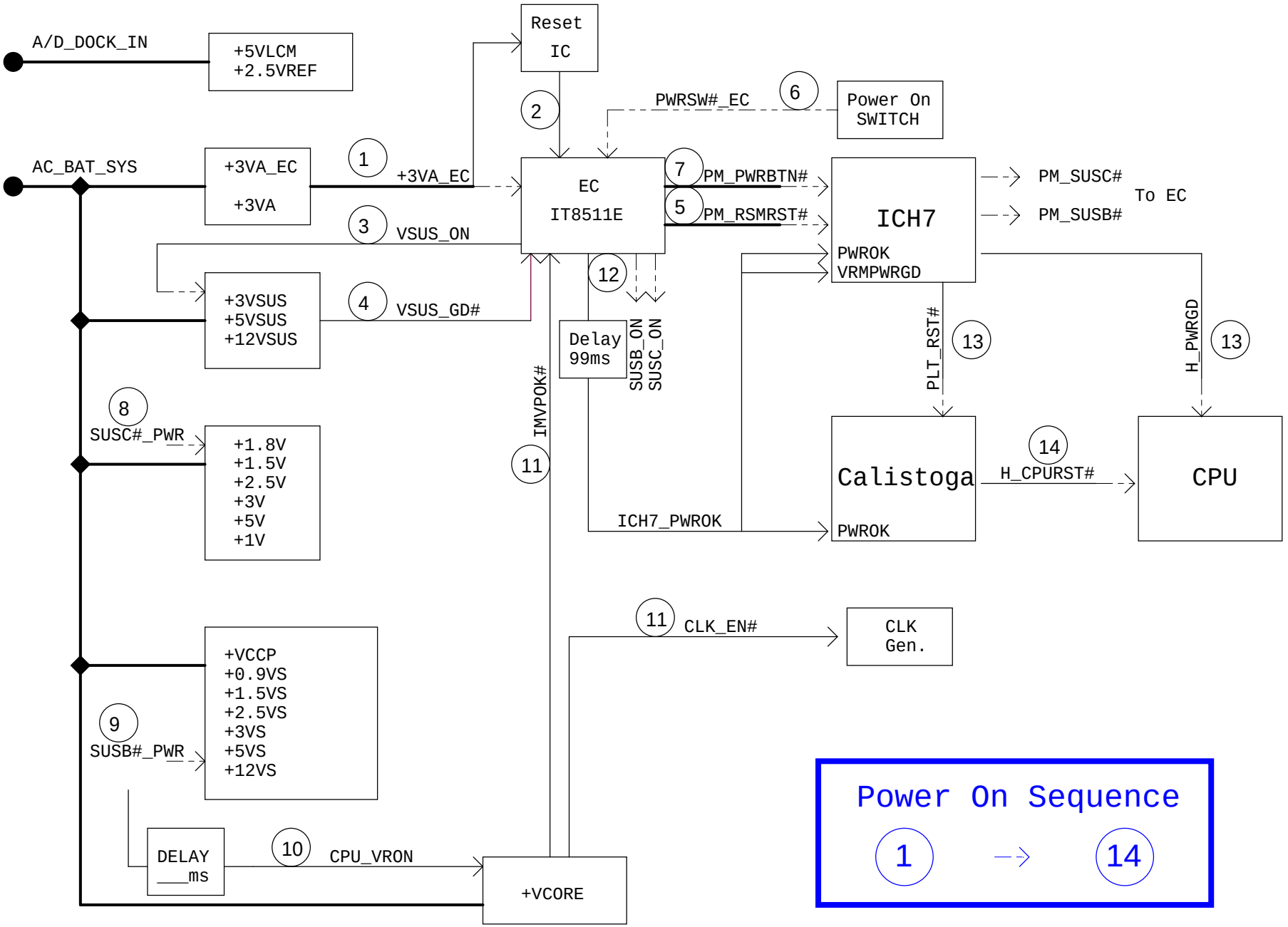

ASUSALPHA	Title : FLOWCHART	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 47 of 57	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12F
Pink: different from T12F

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ASUSALPHA

Title : GPIO Setting

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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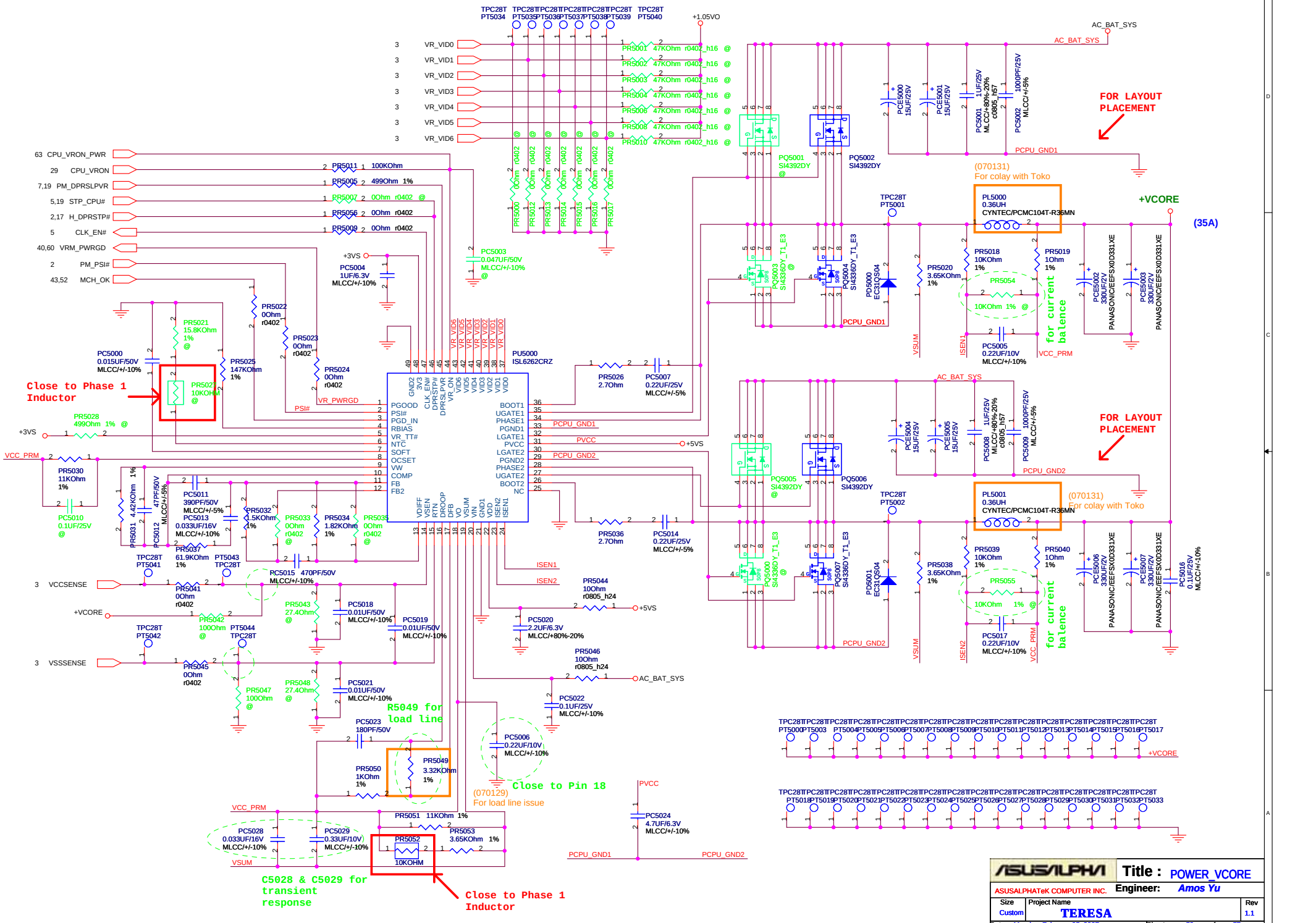
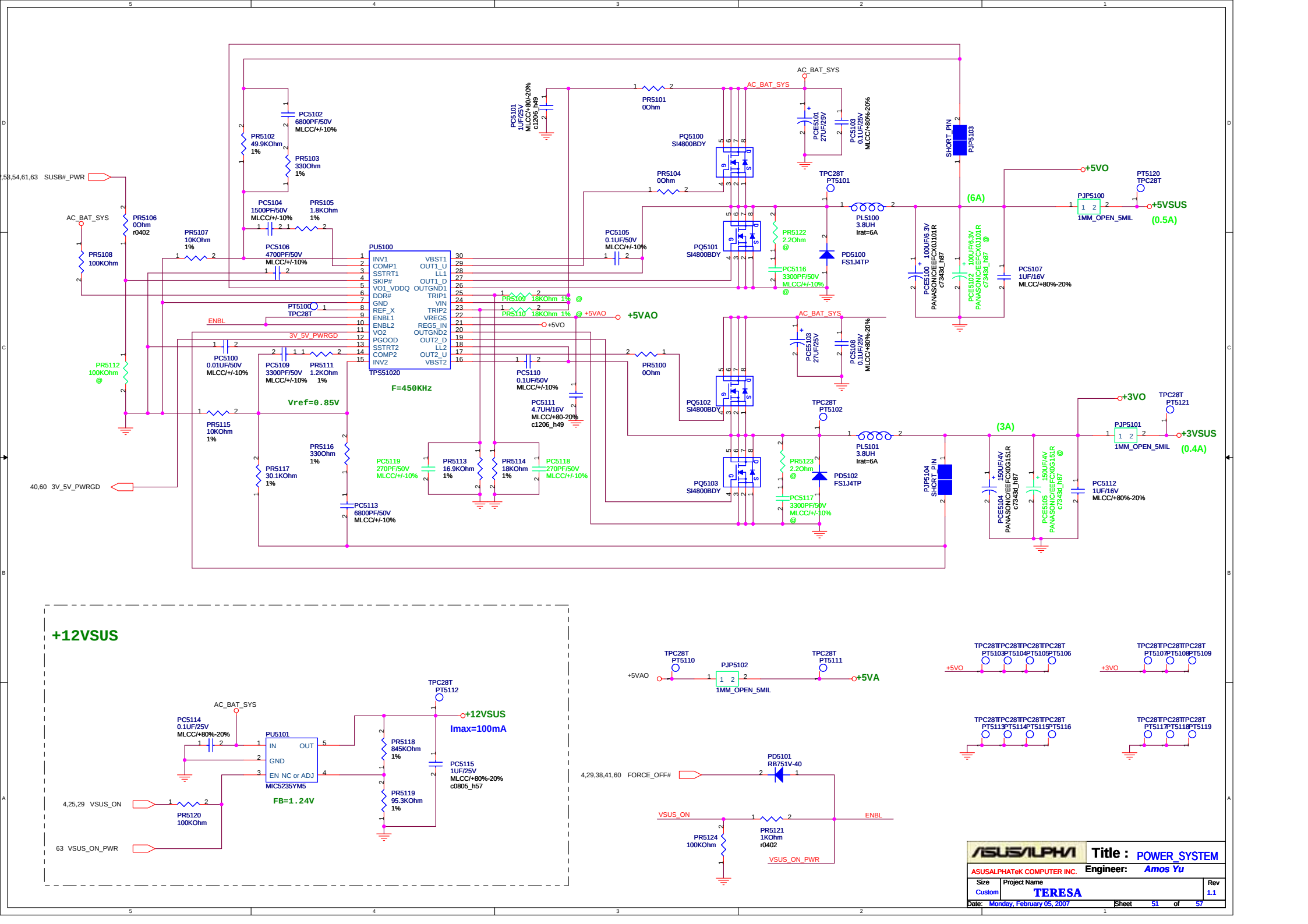
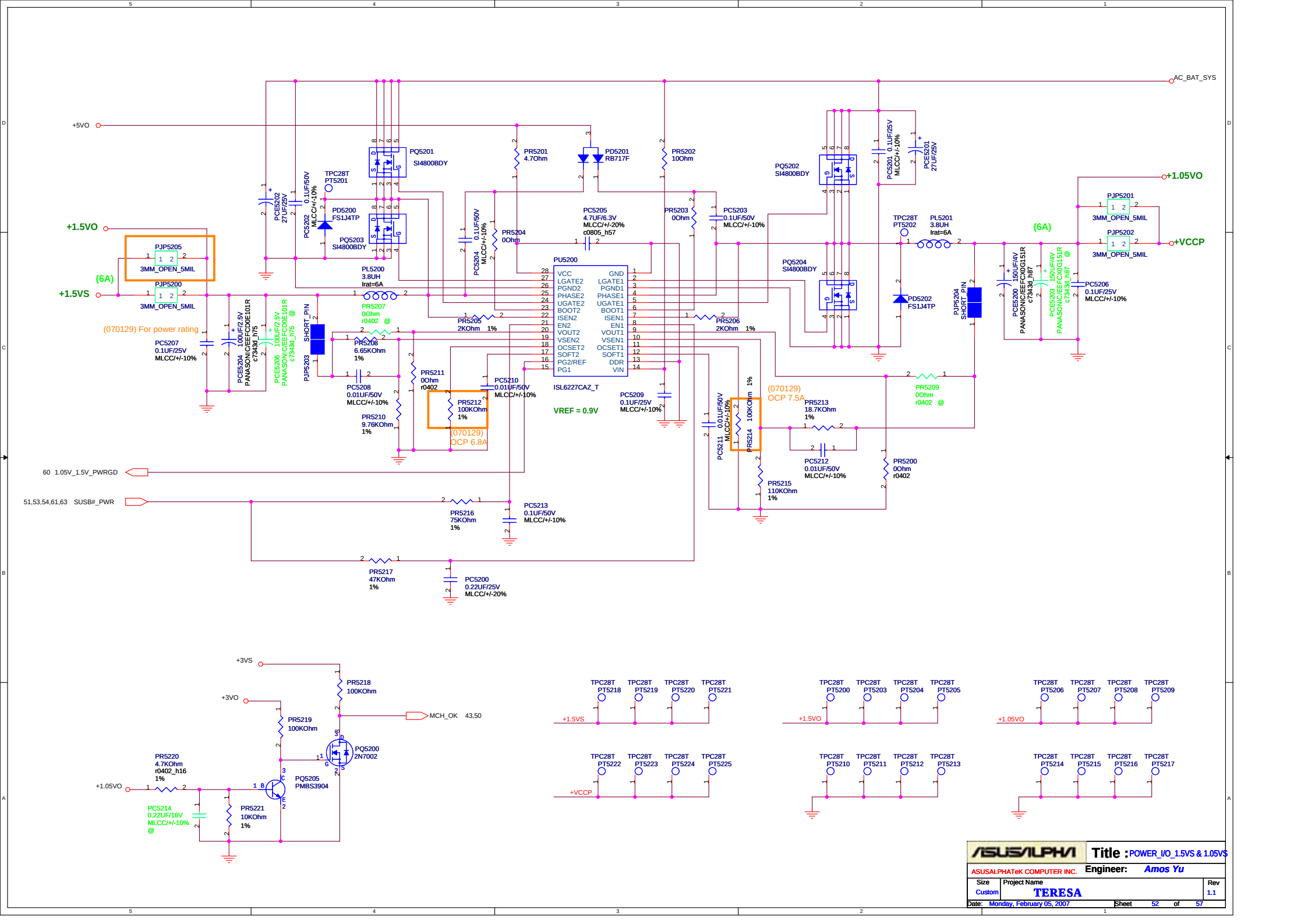
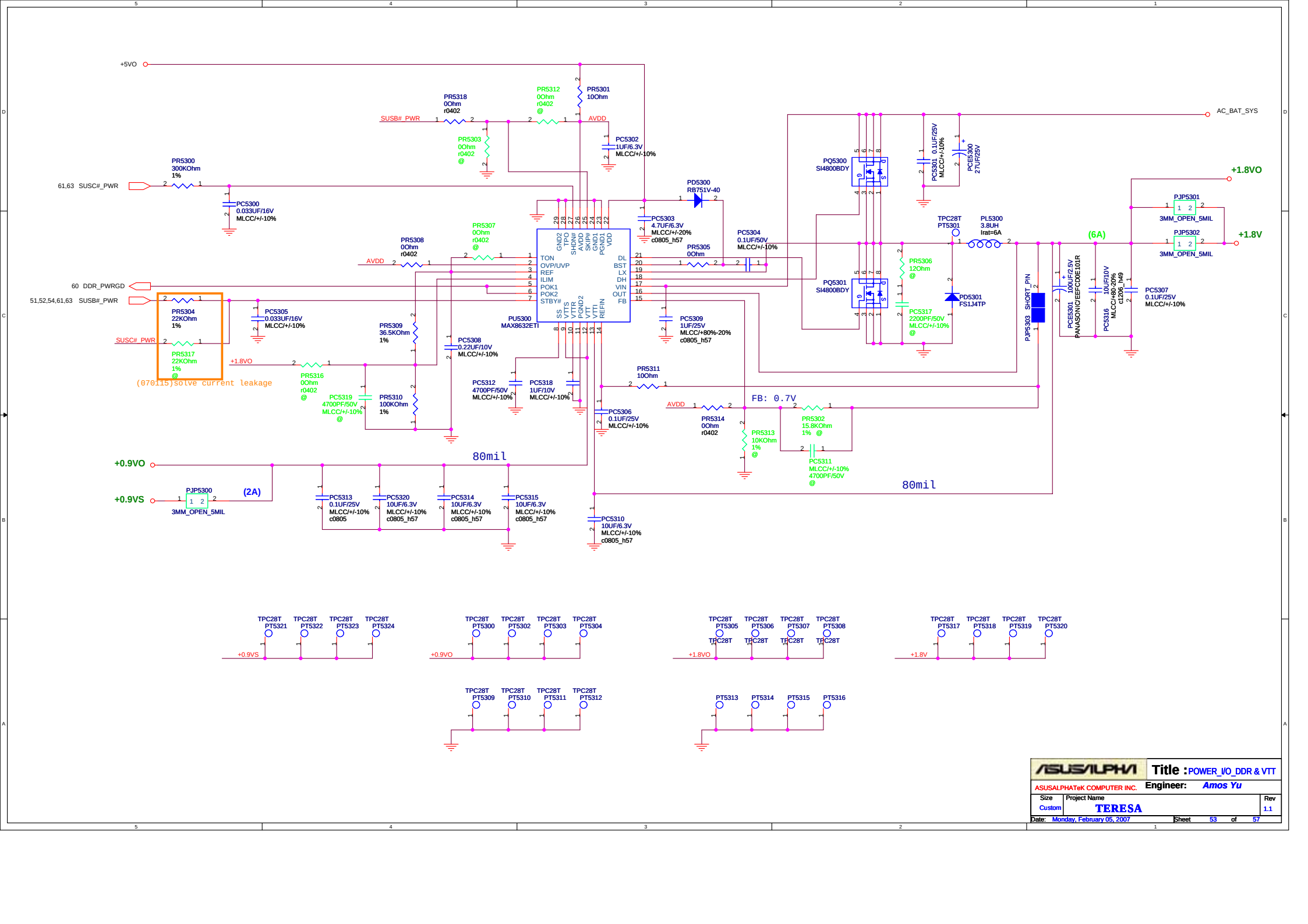

Close to Phase 1 Inductor
Close to Phase 1 Inductor
Close to Pin 18
R5049 for load line
C5028 & C5029 for transient response
FOR LAYOUT PLACEMENT
FOR LAYOUT PLACEMENT
for current balence
for current balence
(070131) For colay with Toko
(070131) For colay with Toko
(070129) For load line issue
+VCORE
(35A)
PU5000 ISL6262CRZ
Title : POWER_VCORE
ASUSALPHATeK COMPUTER INC.
Engineer: Amos Yu
Project Name TERESA
Rev 1.1
Date: Monday, February 05, 2007
Sheet 50 of 57


+12VSUS
Imax=100mA
FB=1.24V
MIC5235YM5
PU5101
PU5100
TPS51020
F=450KHz
Vref=0.85V
SUSB#_PWR
VSUS_ON
VSUS_ON_PWR
FORCE_OFF#
3V_5V_PWRGD
ENBL
+5VAO
+5VO
+3VO
+5VSUS
+3VSUS
+5VA
(6A)
(3A)
(0.5A)
(0.4A)
AC_BAT_SYS
SHORT_PIN
1MM_OPEN_5MIL
PD5101
RB751V-40
PD5100
FS1J4TP
PD5102
FS1J4TP
PQ5100
SI4800BDY
PQ5101
SI4800BDY
PQ5102
SI4800BDY
PQ5103
SI4800BDY
PL5100
3.8UH
Irat=6A
PL5101
3.8UH
Irat=6A
ASUSALPHATeK COMPUTER INC.
Title : POWER_SYSTEM
Engineer: Amos Yu
Project Name
TERESA
Size
Custom
Rev
1.1
Date: Monday, February 05, 2007
Sheet 51 of 57



ASUSALPHA	Title : POWER_I/O_1.5VS & 1.05VS	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 52 of 57	



ASUSALPHAT

Title : POWER_I/O_DDR & VTT

ASUSALPHATeK COMPUTER INC. **Engineer: Amos Yu**

Size	Project Name	Rev
Custom	TERESA	1.1

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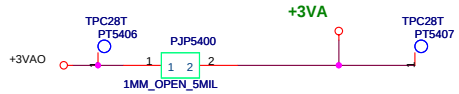
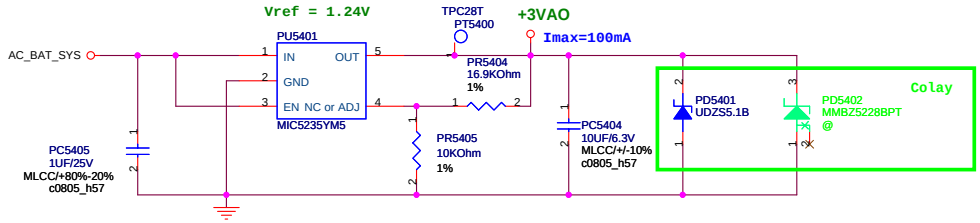
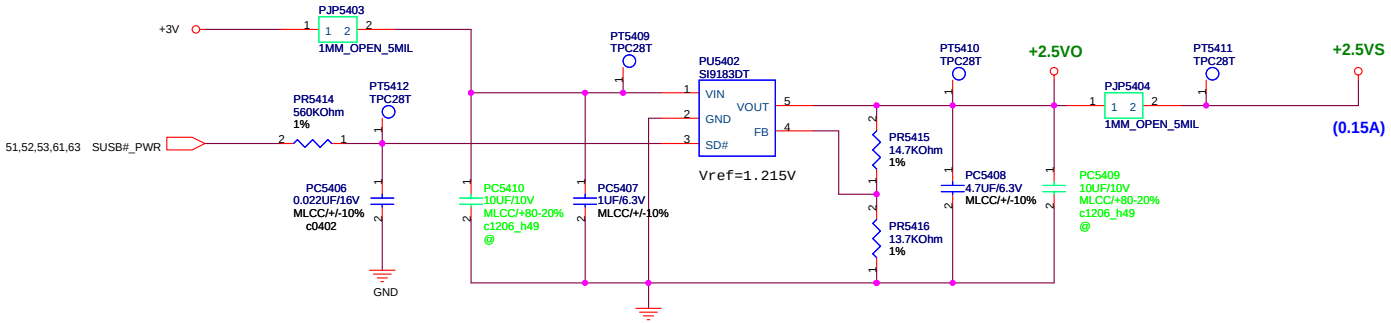
+3VAO

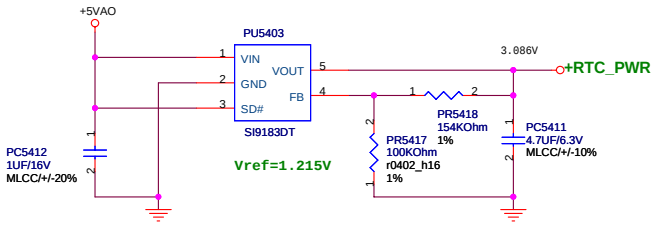




+2.5VS



+RTC_PWR



ASUSALPHA	Title : POWER_I/O_+3VA & +2.5V	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
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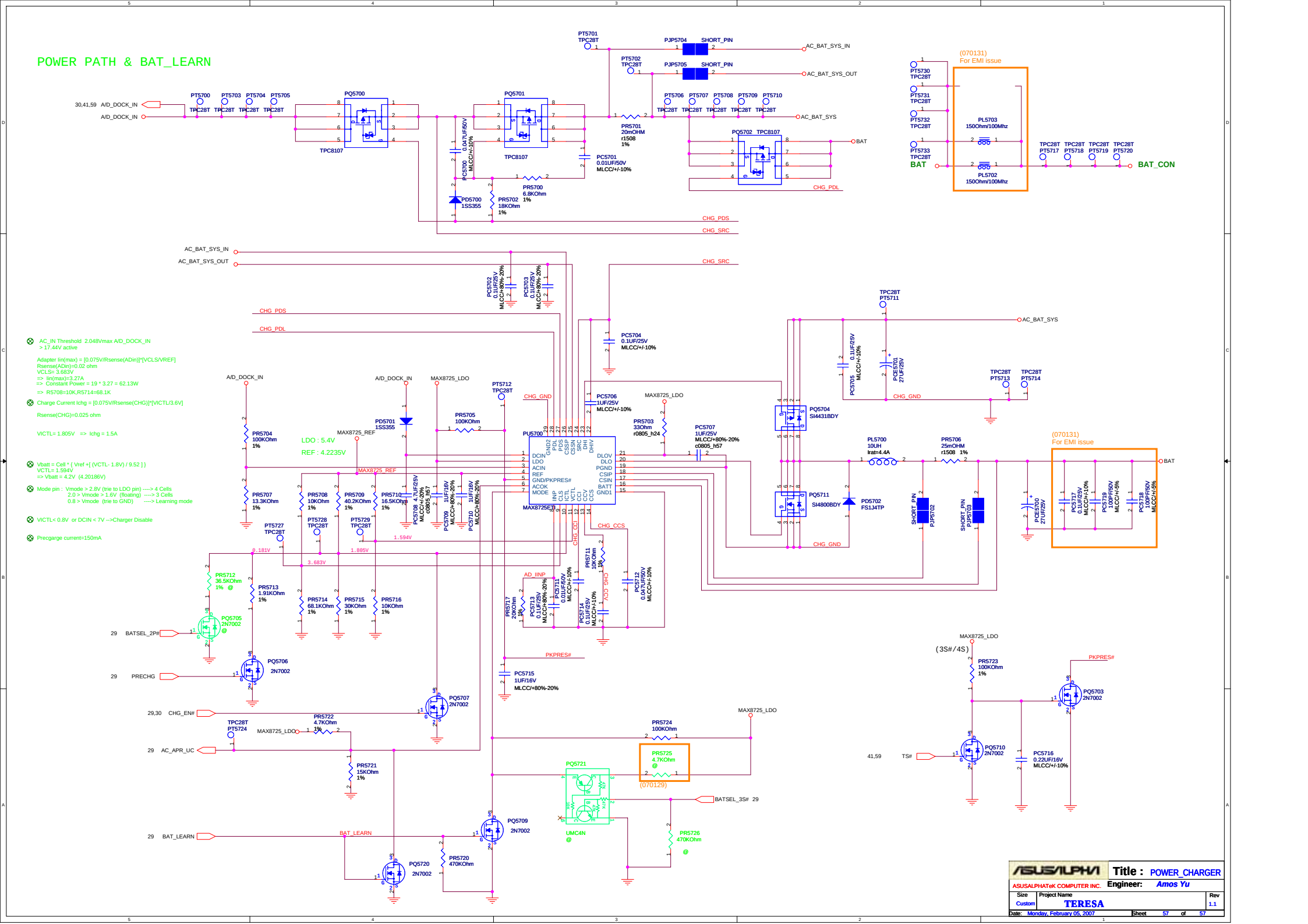
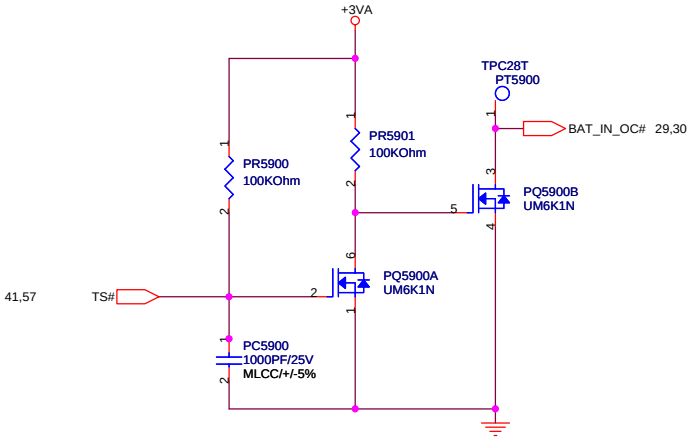
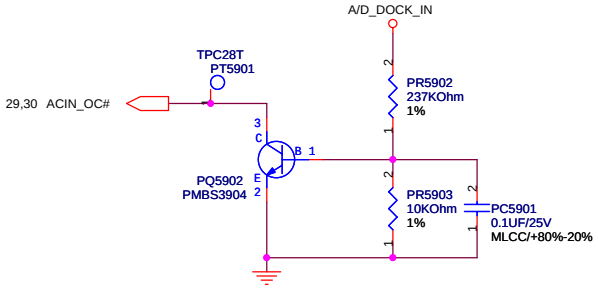
POWER PATH & BAT_LEARN



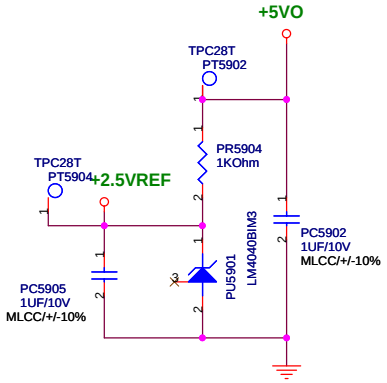
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



ASUSALPHAteK COMPUTER INC.

Title : POWER_DETECT

Engineer: Amos Yu

Size	Project Name	Rev
Custom	TERESA	1.1

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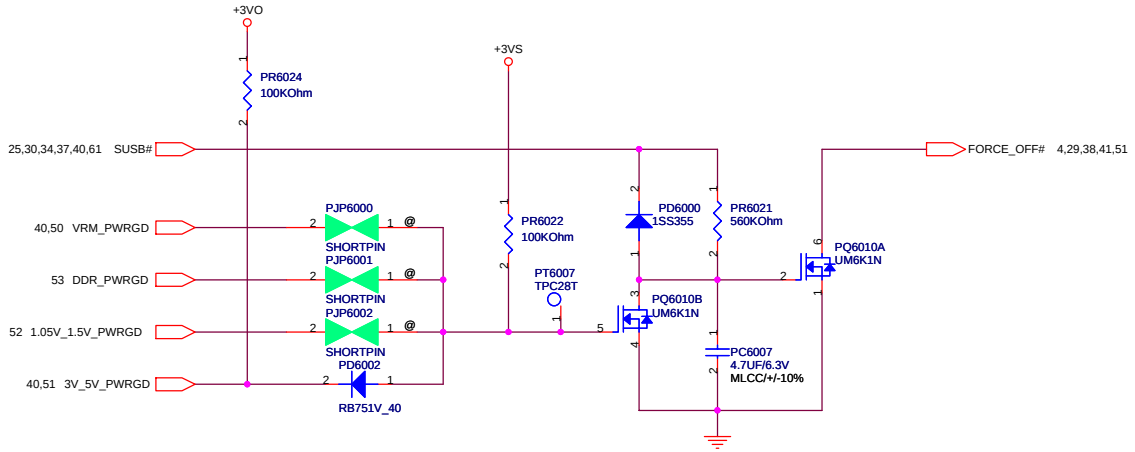
POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD

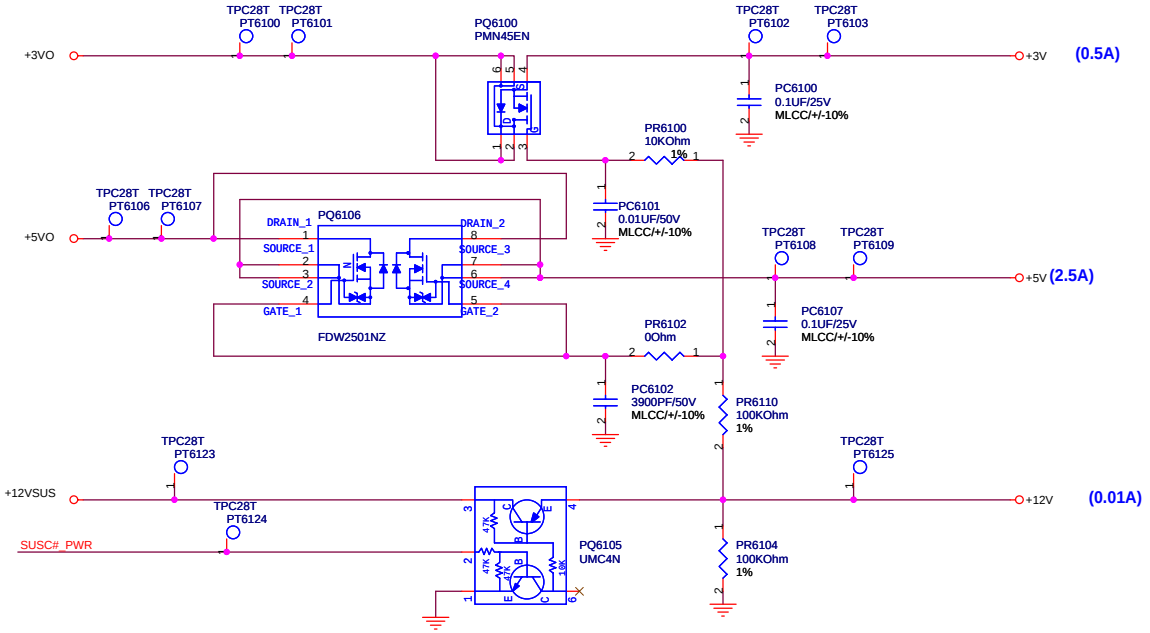
TPC28T PT6004 1 DDR_PWRGD

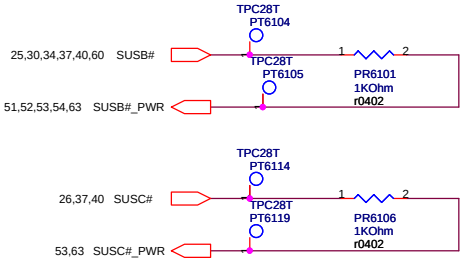
TPC28T PT6005 1 3V_5V_PWRGD

TPC28T PT6006 1 1.05V_1.5V_PWRGD

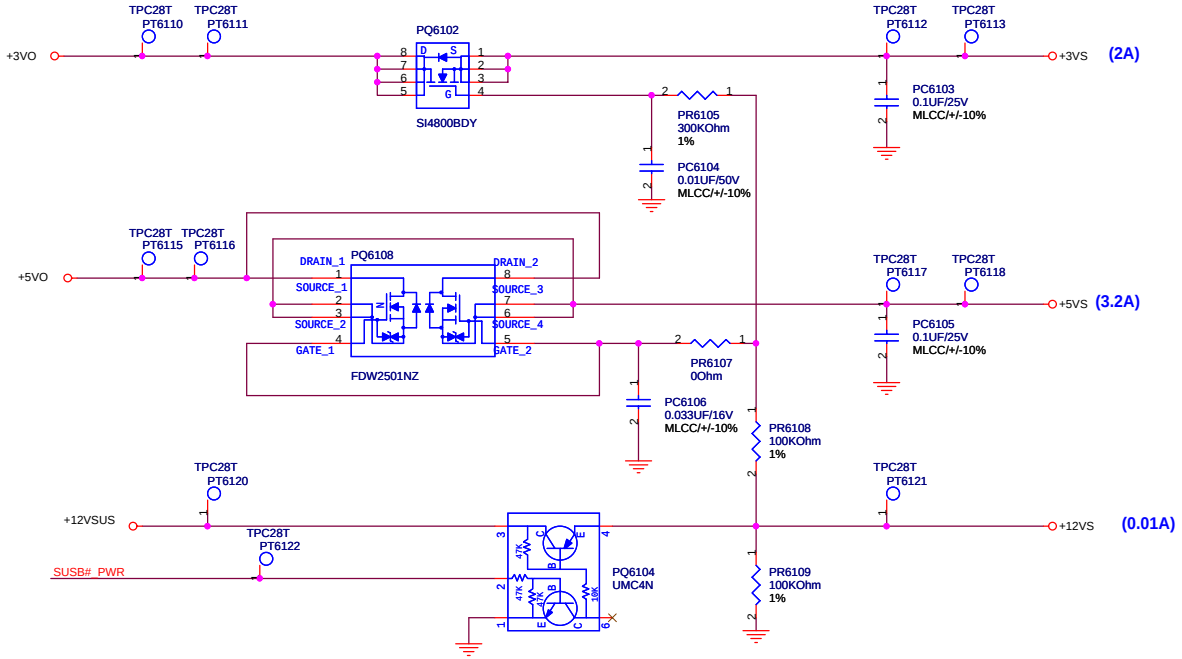
ASUSALPHA	Title : POWER_PROTECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 60 of 57	

SUSC#_PWR POWER





SUSB#_PWR POWER



ASUSALPHA	Title : POWER_LOAD SWITCH	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
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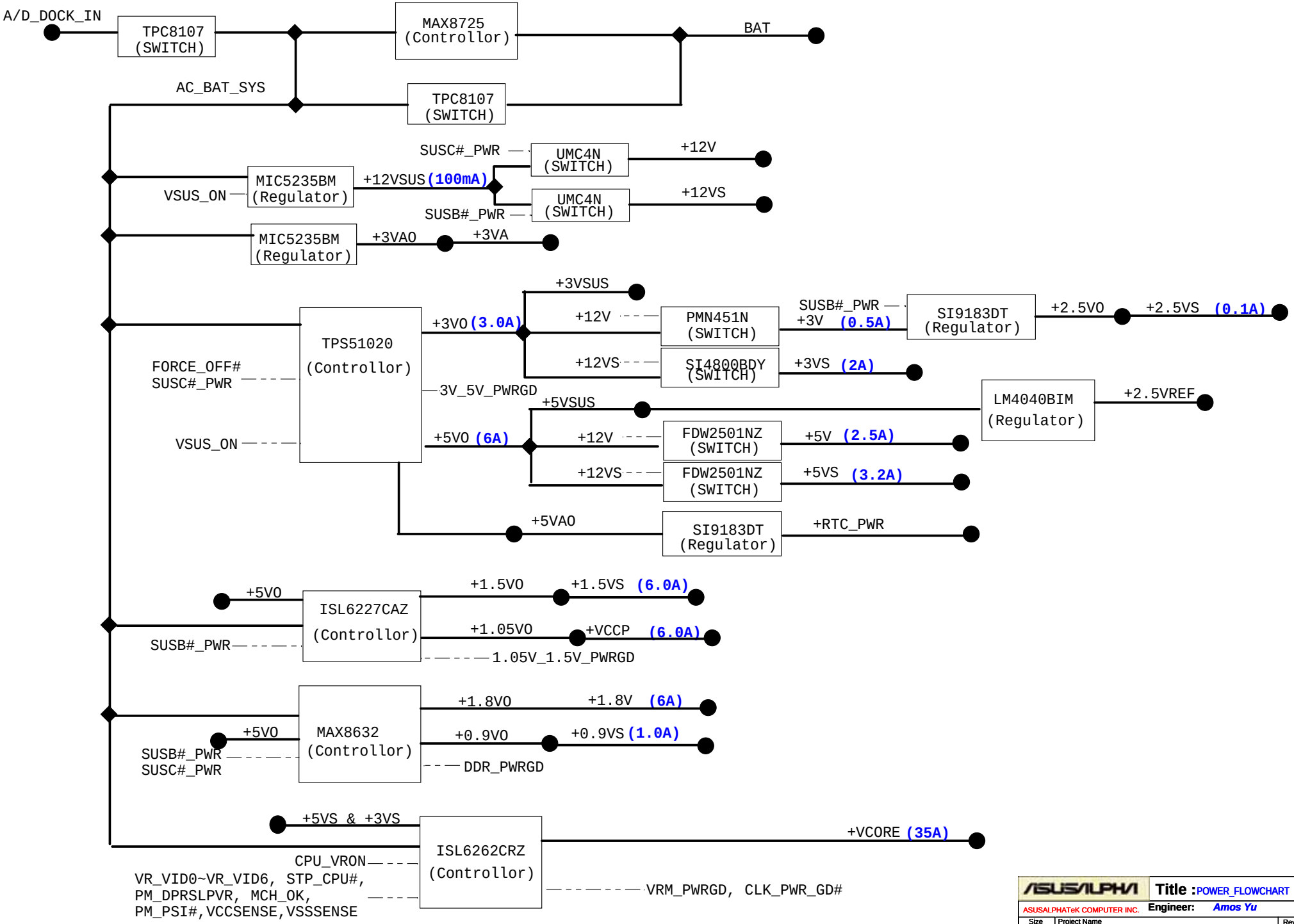

ASUSALPHA	Title : POWER_FLOWCHART	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
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AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA → +3VA 4,12,22,29,37,38,40,41,54,59

+5VA → +5VA 51

+5VO → +5VO 51,52,53,59,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 18,19,20,25,29,30,34,35,40,51

+5VSUS → +5VSUS 20,30,36,51

+3V → +3V 12,18,26,37,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 37,61

+12VS → +12VS 12,13,22,33,37,61

+5V → +5V 16,30,36,37,44,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,37,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,16,37,53

+VCCP → +VCCP 2,6,9,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH → +VCCP_GMCH 9,10

+VCCP_ICH → +VCCP_ICH 17,20

+0.9VS → +0.9VS 16,37,53

BAT → BAT 30,57

+2.5VREF → +2.5VREF 59

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

+RTC_PWR → +RTC_PWR 20,54

FOR POWER TEST

+3VA

PJP6300 (SGL_JUMP): 1 — 1 2 — 2 → CPU_VRON_PWR 50

@PJP6301 (SGL_JUMP): 1 — 1 2 — 2 → SUSB#_PWR → SUSB#_PWR 51,52,53,54,61

@PJP6302 (SGL_JUMP): 1 — 1 2 — 2 → SUSC#_PWR → SUSC#_PWR 53,61

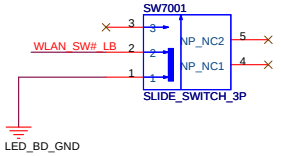
@PJP6303 (SGL_JUMP): 1 — 1 2 — 2 → VSUS_ON_PWR → VSUS_ON_PWR 51

@

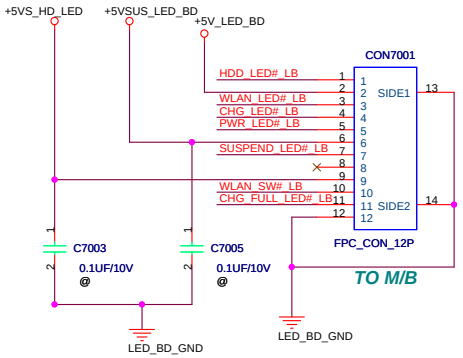
ASUSALPHA	Title : POWER_SIGNAL	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 63 of 57	

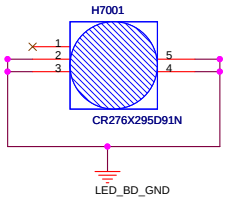
LEFT & RIGHT Button remove to TP BOARD

New added SW for Teresa

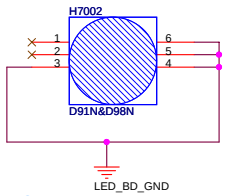


070115 Change pin define





DETAIL: Q



DETAIL: S

CON to T/P remove to TP BOARD

IR receive module removed

ASUSALPHA	Title : LED Board	
ASUSALPHATeK COMPUTER INC.	Engineer: Potter_Huang	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Monday, February 05, 2007	Sheet 70 of 57	

TERESA SCHEMATIC V1.0

ASUSALPHA

Title : Content & History

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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