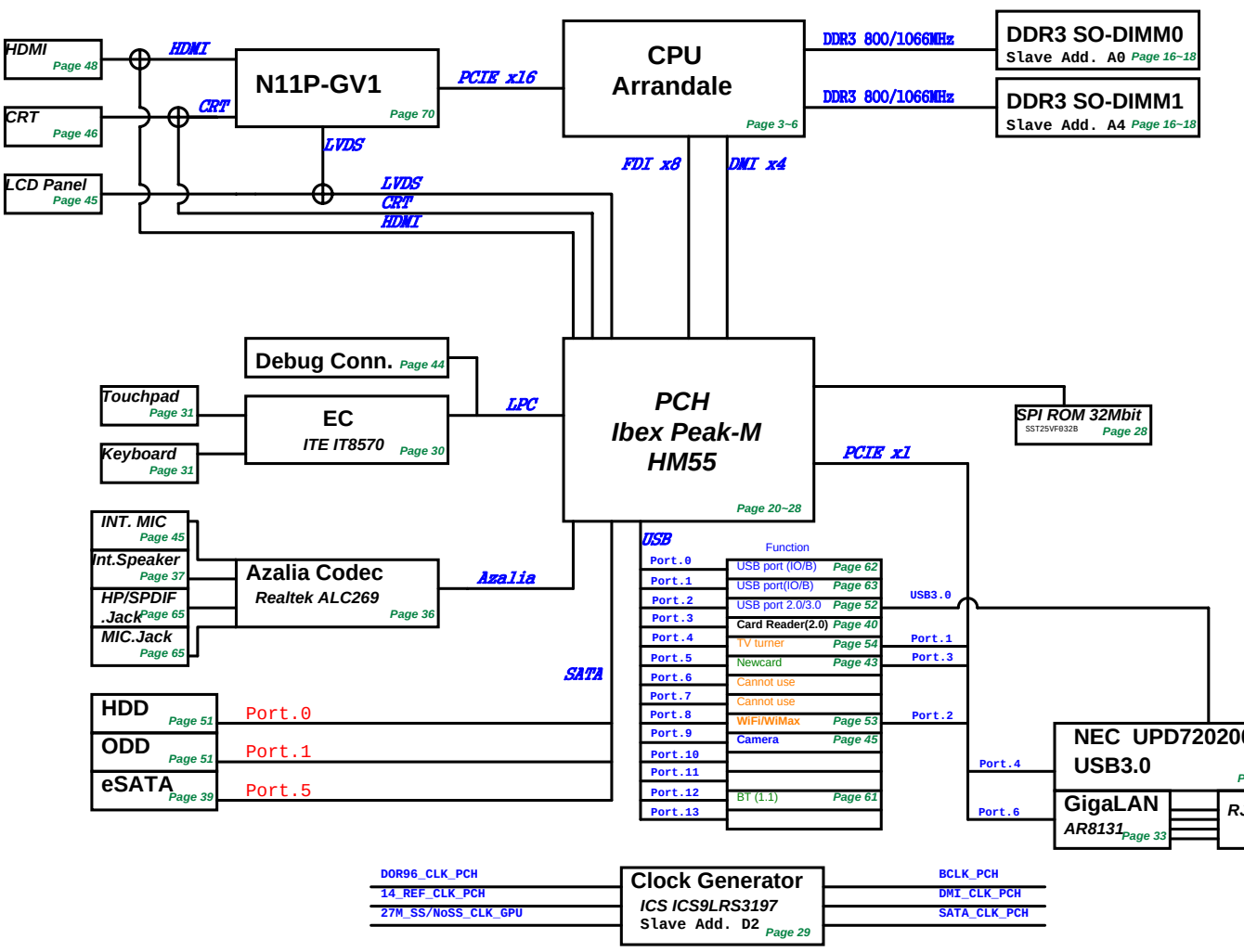
N61Jv SCHEMATIC Revision 2.0

SYSTEM PAGE REF.

N61Jv BLOCK DIAGRAM



Power

- VCORE — Page 80
- System — Page 81
- 1.5VS & 1.05VS — Page 82
- DDR & VTT — Page 83
- +2.5VS — Page 84
- Charger — Page 86
- Detect — Page 90
- Load Switch — Page 91
- Power Protect — Page 92

PWM Fan	Reset Circuit	Discharge Circuit	DC & BATT. Conn.	Skew Holes
Page 50	Page 32	Page 57	Page 60	Page 65

ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: yun-feng_yan

Size	Project Name	Rev
C	N61Jv	1.0

Date: Thursday, December 17, 2009 Sheet 1 of 95

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	INT TBD	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPO	NC_TP	INT TBD	+3VS
GPIO 07	GPO	NC_TP	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	-	+3VSUS
GPIO 14	GPO	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPI	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1#_TV	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3#_NEWCARD	EXT PD	+3VSUS
GPIO 26	GPI	CLK_REQ4#_CB	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	EXT PD	+3VSUS
GPIO 29	Native	NC_TP	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPO	SATA_CLK_REQ#	EXT PD	+3VS
GPIO 36	GPI	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	EXT PU	+3VSUS
GPIO 46	Native	NC_TP	EXT PU	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PU	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPIO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	Native	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	DGPU_PWM_SELECT#	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	Native	NC_TP	INT TBD	+3VS
GPIO 67	Native	EDID_SELECT#	INT TBD	+3VS
GPIO 72	Native	PM_BATLOW#	EXT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8541

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		-
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2		ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0	O	-
GPF1		-
GPF2	I	EXP_GATE#
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SUSPWRDNACK_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	ALS_AD
GPI6	I	CAP_ACK_A#
GPI7	I	CAP_ACK_B#
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		-

EC IT8301 R1.3 removed

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2		-
GPIO3		-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	ME_PWROK
GPIO13		-
GPIO14	O	ME_SLP_M_EC#
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LRS3197)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
VID Controller(ASM8272)	0011011x (36)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor(G781)	1001100x (9A)	
VGA Thermal IC(G781-1)	1001101x (9E)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st	06G023048011	G781F
S		
S		
S		

	Clock Gen P/N:	component name
1st	06G011604010	ICS9LRS3197
S		
S		

	VGA Thermal Sensor	component name
1st	06G023048020	G781-1
S		
S		

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	Card reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

ASUSTeK COMPUTER INC. NB4

Title : System Setting

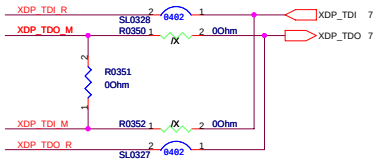
Engineer: yun-feng_yan

Size	Project Name	Rev
C	N61Jv	1.0

Date: Wednesday, November 11, 2009 Sheet 2 of 95

Main Board

JTAG MAPPING



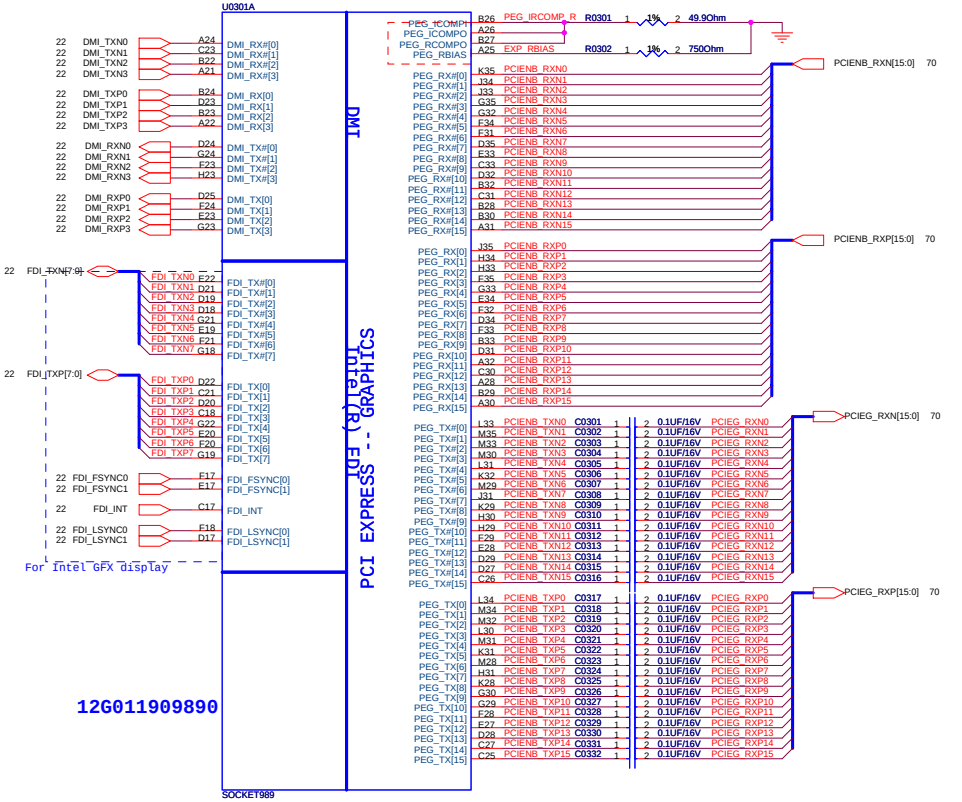
FDI disable: (For discrete graphic)

1. NC:
   FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
   VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1K ≠ 5% resistor:
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving.(DG R0.8 P.70)
3. Connected to GND:
   VCCAXG,
4. Can be connected to GND directly:
   DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
   VCCFDIPLL

DG R1.1 P.83:

"FDI_FSYNC[0],FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.

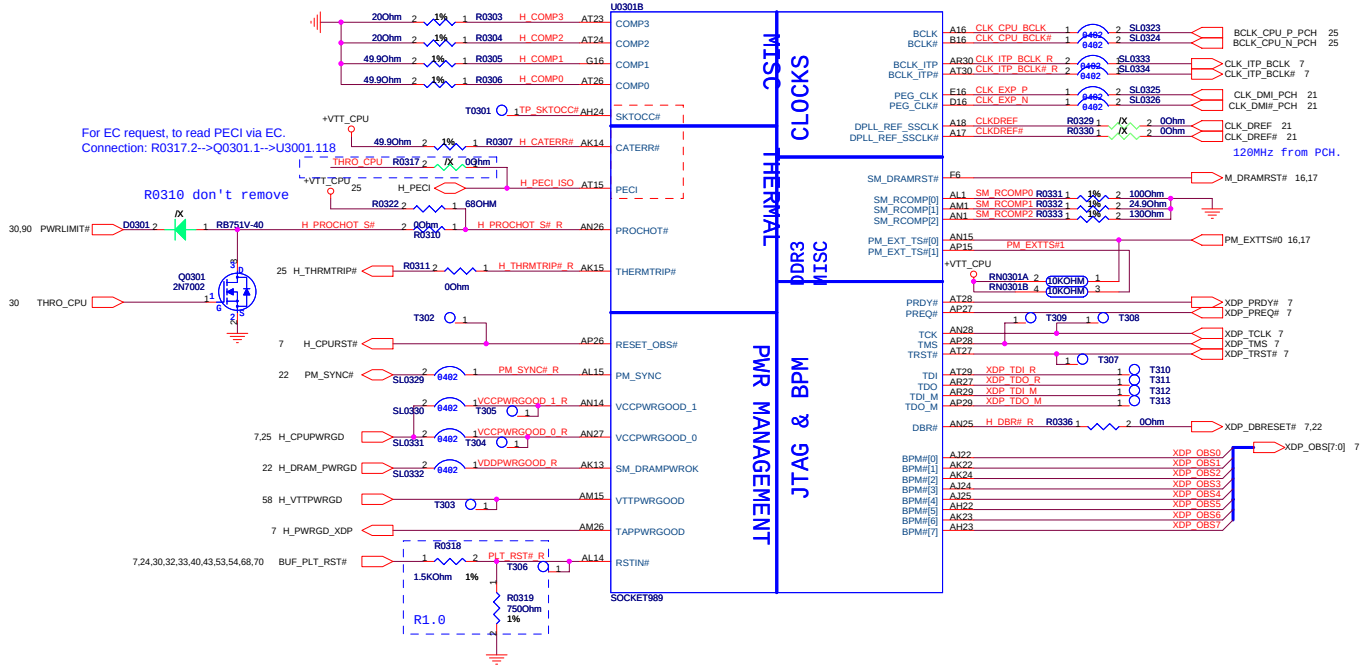
"On the other hand,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.



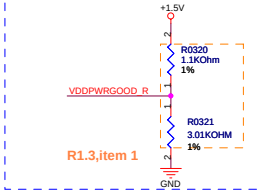
12G011909890

R0370,R0371,R0372 near U0301

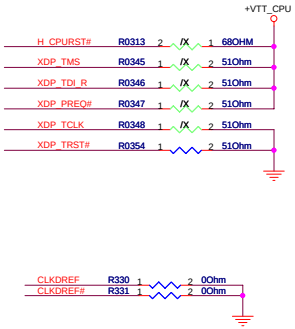
SKTOCC#:pulled to ground on processor.
may use to determine if CPU is present



DRAMPWROK: (DGU R1.52)

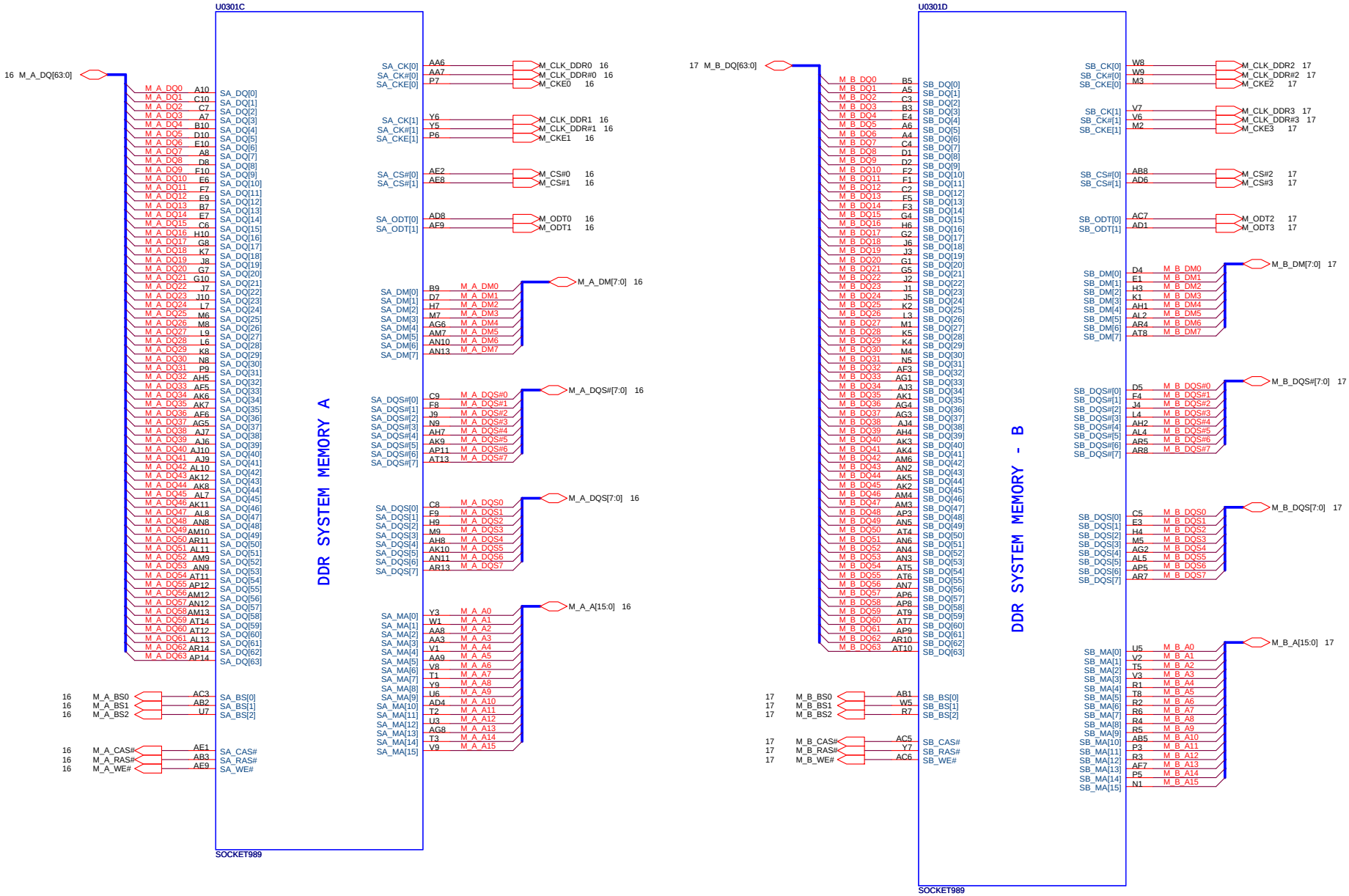


R1.3,item 1

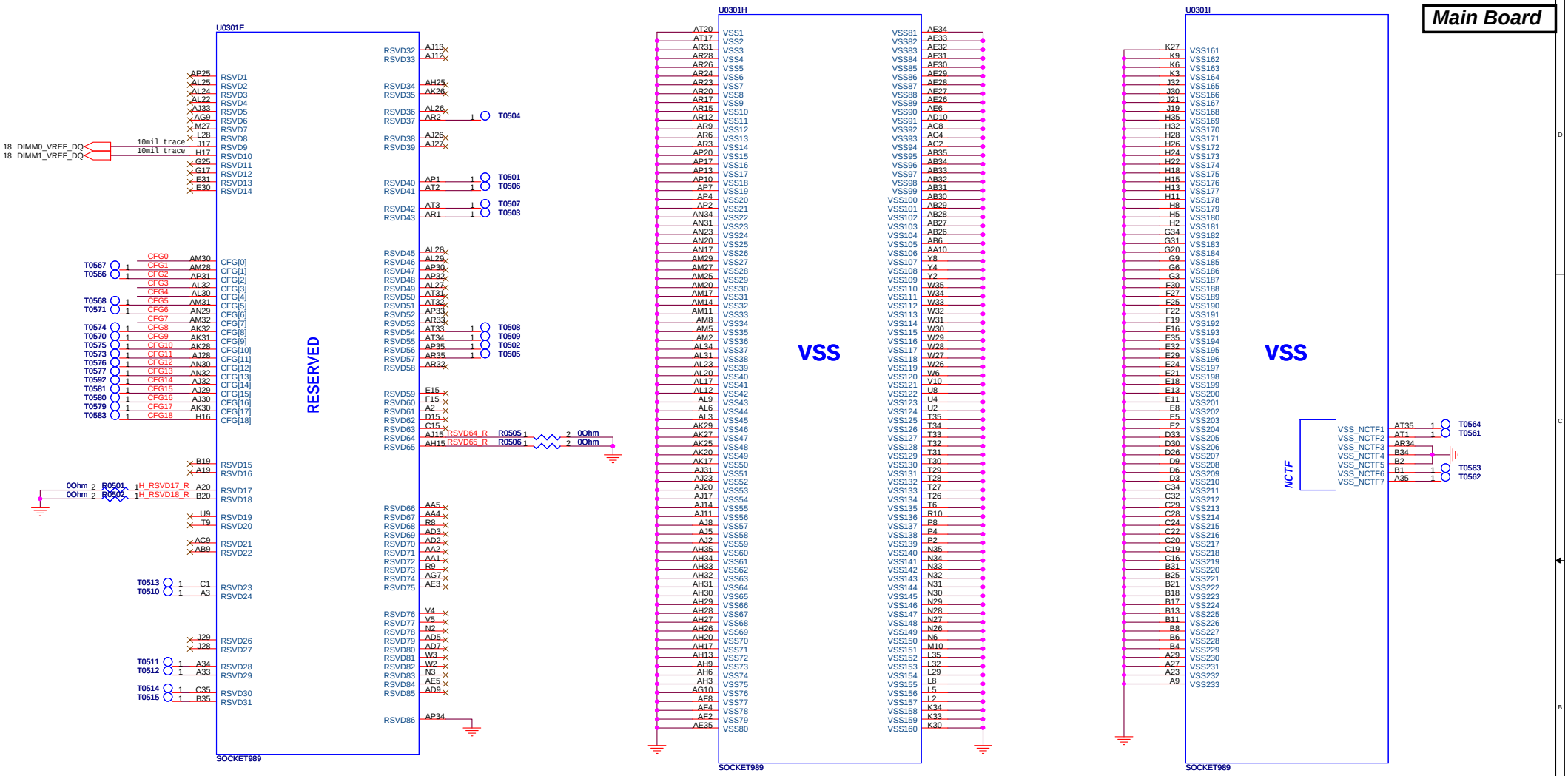


ASUSTeK COMPUTER INC. NB1	Title : DMI,PEG,FDI,CLK		
	Engineer: yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 3 of 95		

Main Board



ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 4 of 95	



CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation (Clarksfield Only)

- 11 : 1 x 16 PEG (Default)
- 10 : 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal (Auburndale Only)

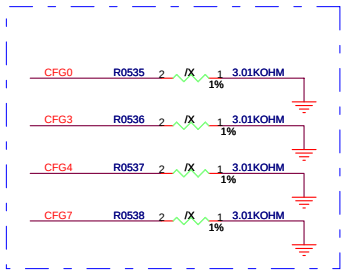
- 1 : Normal Operation (Default)
- 0 : Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection (Auburndale Only)

- 1 : Disabled - No Physical Display Port attached to eDP
- 0 : Enabled - An external Display Port device is connected to eDP

CFG[7]: Fixed for PCI Express 2.0 jitter specifications (Clarksfield)

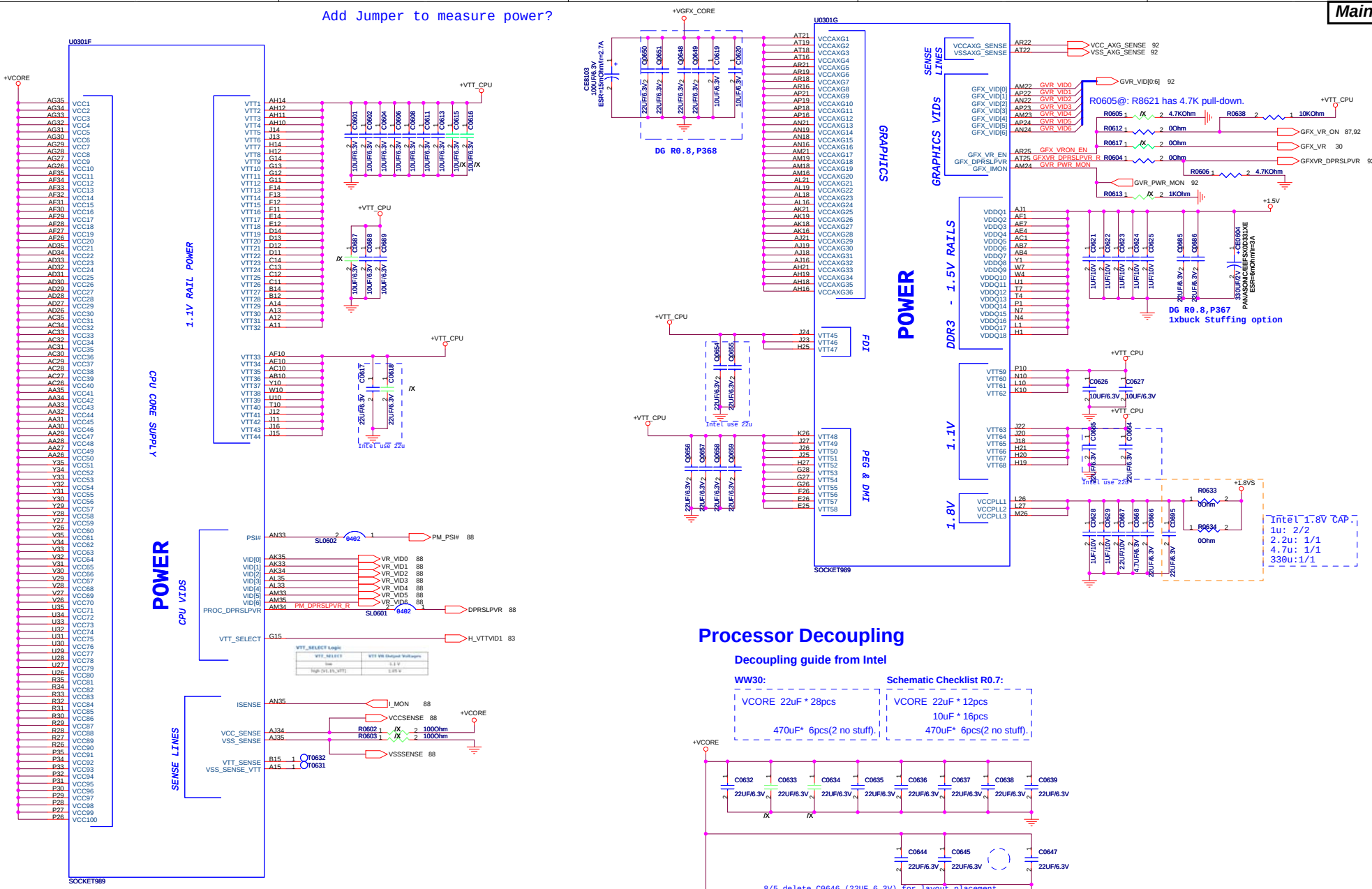
- only for early samples pre-ES1 : Connect to GND with 3.01K Ohm 5% resistor



* Note:
Auburndale Hardware Straps are sampled on asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.
Clarksfield Hardware Straps are sampled after RSTIN# de-assertion.

ASUSTeK COMPUTER INC. NB1	Title : CFG,RSVD,GND	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 5 of 95	

Add Jumper to measure power?



Processor Decoupling

Decoupling guide from Intel

WW30:

VCORE 22uF * 28pcs

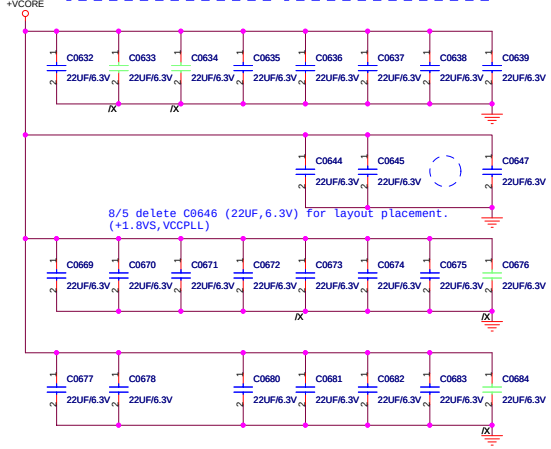
470uF* 6pcs(2 no stuff).

Schematic Checklist R0.7:

VCORE 22uF * 12pcs

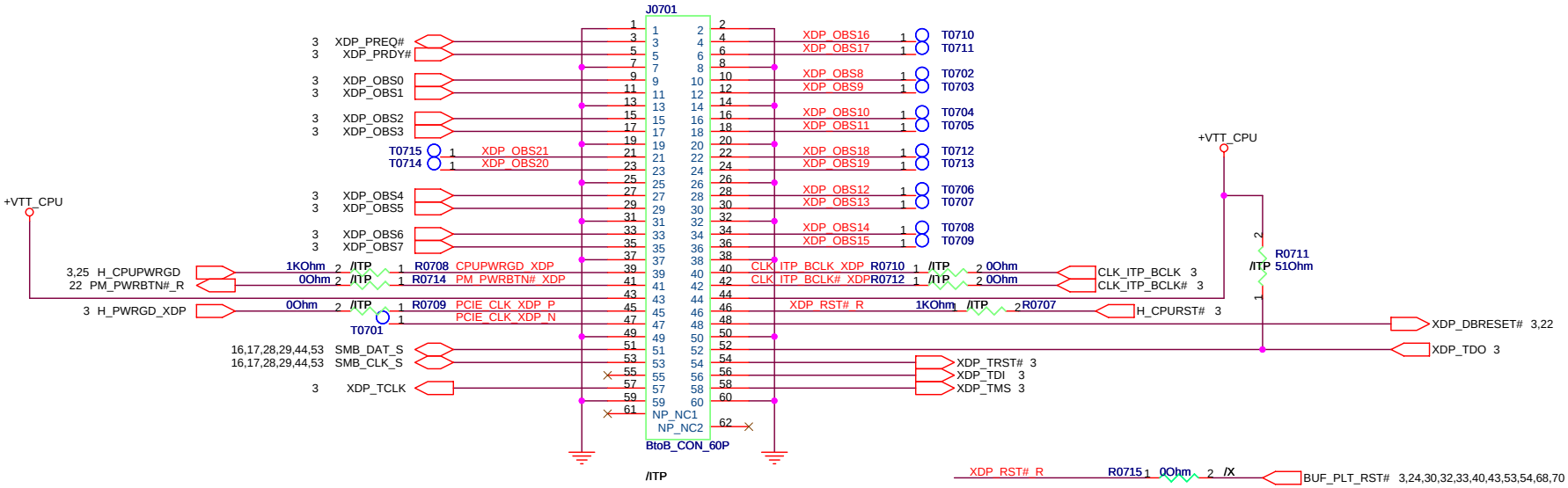
10uF * 16pcs

470uF* 6pcs(2 no stuff).



Intel 1.8V CAP.
1u: 2/2
2.2u: 1/1
4.7u: 1/1
330u:1/1

ASUSTeK COMPUTER INC. NB1	Title : CPU(4)_PWR		
	Engineer: yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 6 of 95		



CPU XDP connector

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP		
	Engineer: Yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 7 of 95		

Title :	NB_****		
ASUSTeK COMPUTER INC. NB1	Engineer:	CH_Lin	
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 8 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB ****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 9 of 95	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 10 of 95	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 11 of 95	

Main Board

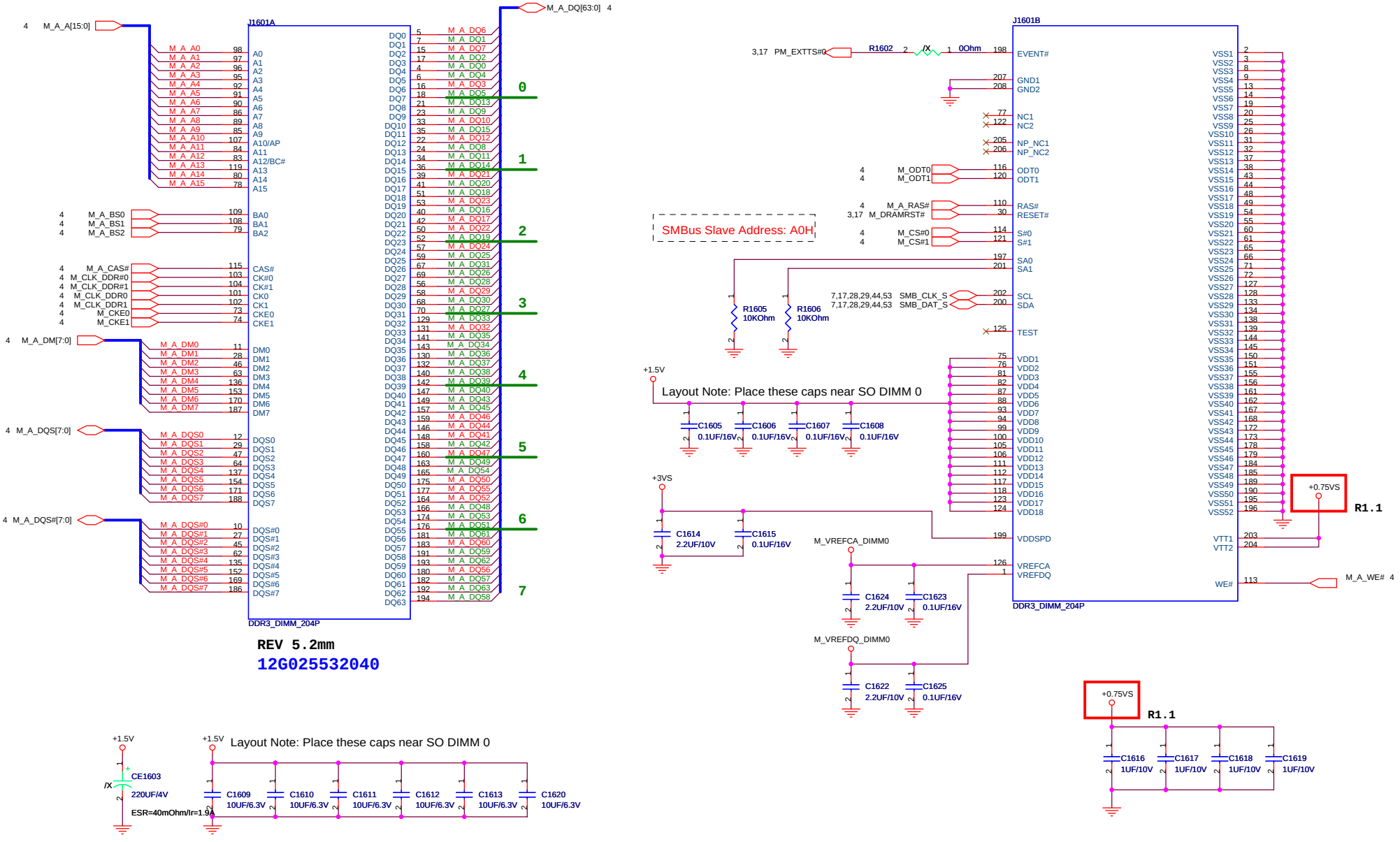
ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 12 of 95	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 13 of 95	

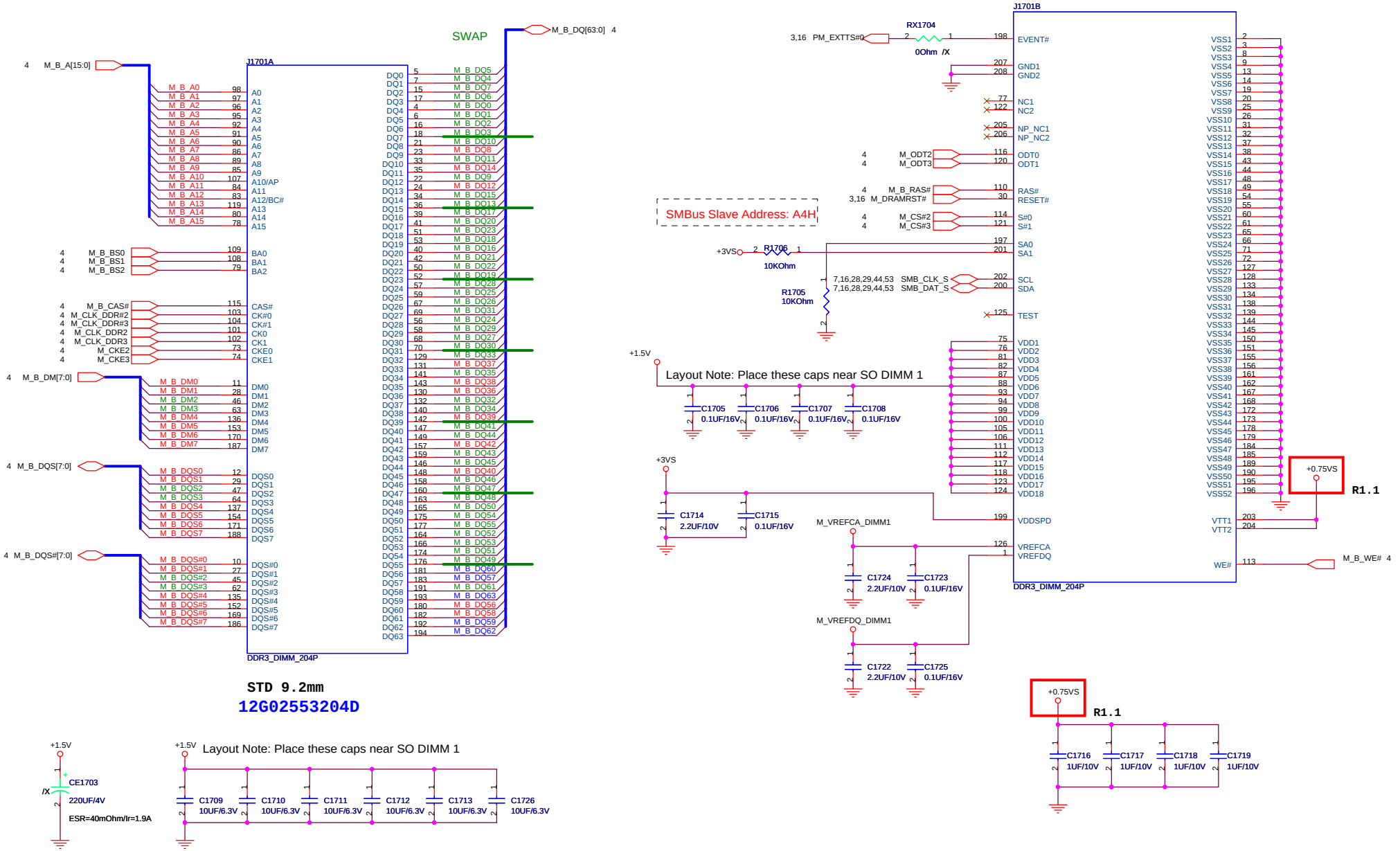
ASUSTeK COMPUTER INC. NB6	Title :	
	Engineer: CH_Lin	
Size: A	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 14 of 95	

ASUSTeK COMPUTER INC. NB6	Title :	
	Engineer: CH_Lin	
Size: A	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 15 of 95	



ASUSTeK COMPUTER INC. NB6	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 16 of 95	

Title: DDR3 SO-DIMM_0

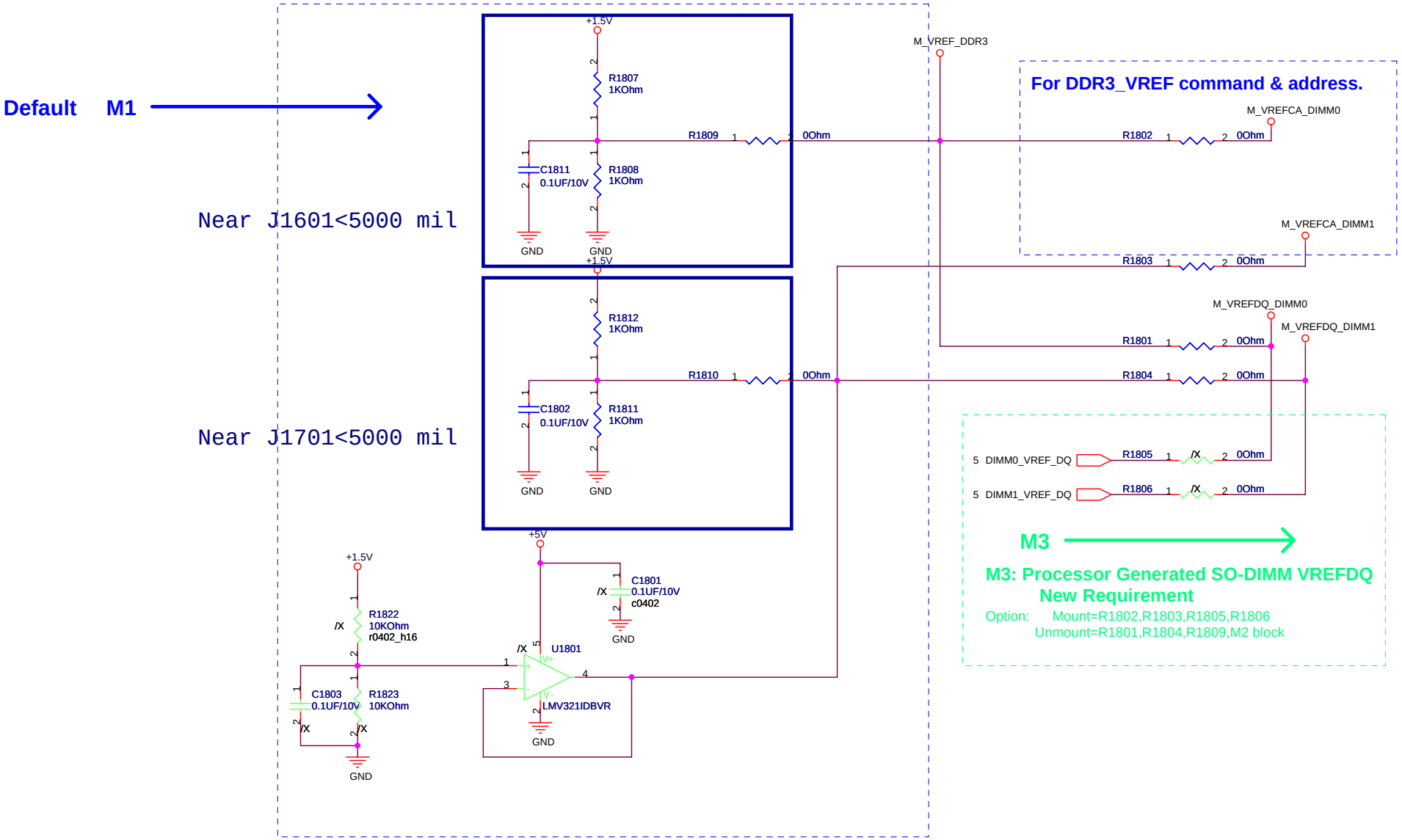


ASUSTeK COMPUTER INC. NB6	Title: DDR3 SO-DIMM_1	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 17 of 95	

Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

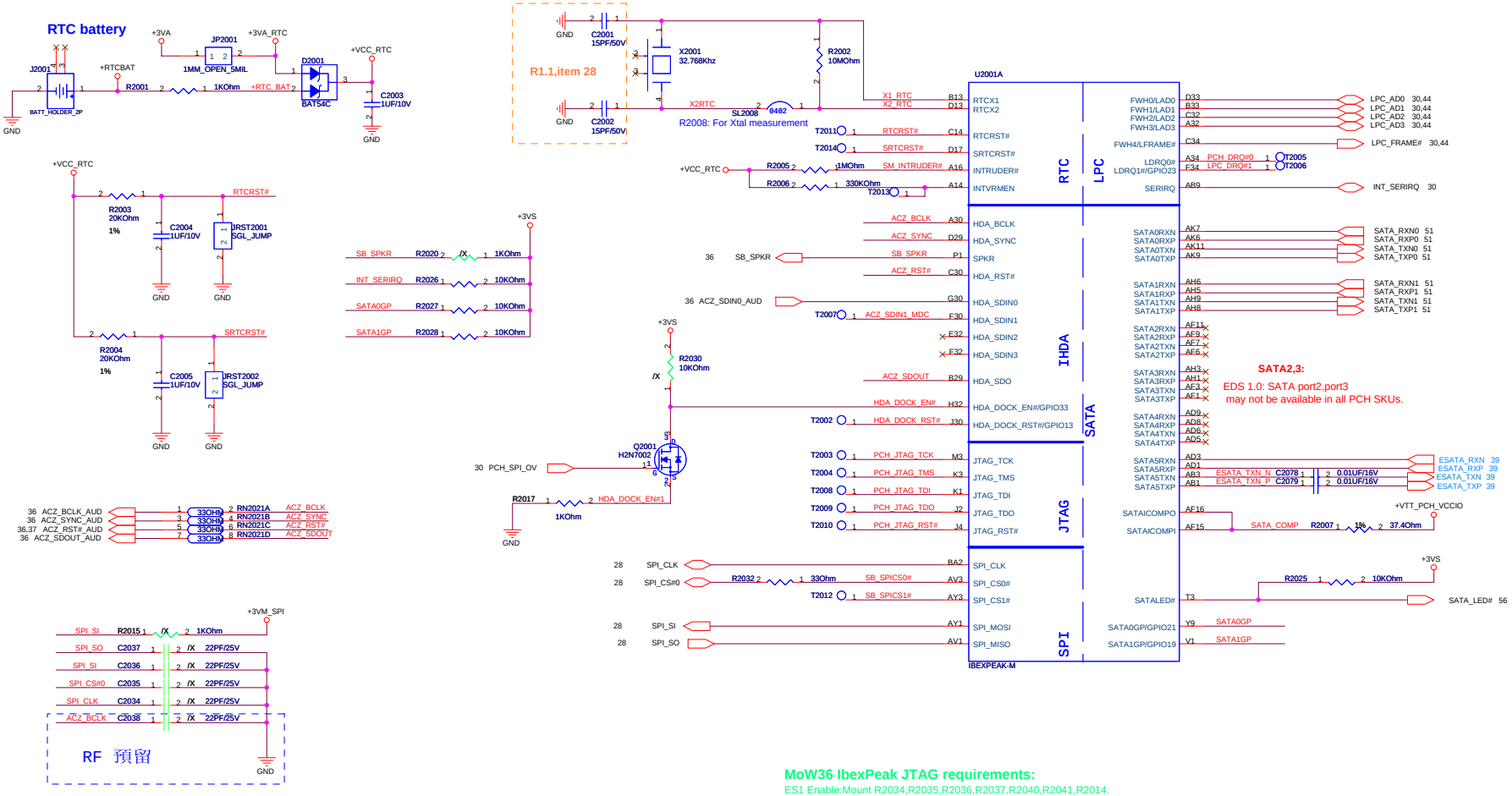
DDR3 Vref

Intel Document Number: 400755



ASUSTeK COMPUTER INC. NB6	Title : CA_DQ VOLTAGE	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 18 of 95	

Engineer Name>	
ASUSTeK COMPUTER INC. NB1	Title : VID
	Engineer:
Size: Custom	Project Name: N61Jv
	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 19 of 95



MoW36 IbexPeak JTAG requirements:

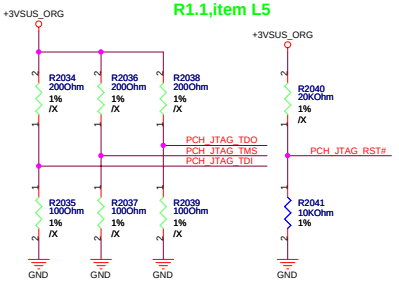
ES1 Enable:Mount R2034,R2035,R2036,R2037,R2040,R2041,R2014.
DNI R2038,R2039. (TDO)
ES1 Disable:Mount R2040,R2041,R2014.
DNI: others.

R1.2,item L5

MoW50 IbexPeak JTAG requirements:

Stuff for pre-production

R1.1,item L5



ES2 Mount :R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041,R2014.

414044 Design Guide R1.11 Update: page9

GPIO33:
This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

Without connecting GPIO33,
customers may not be able to override SPI flash contents.

Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High:Enable

HDA_DOCK_EN#:
1.Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2.GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)

ASUSTeK COMPUTER INC. NB6	Title : SATA,IHDA,RTC,LPC		
	Engineer: yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 20 of 95		

PCIE 1	TV Tuner
PCIE 2	WLAN
PCIE 3	NewCard
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	LAN
PCIE 7	
PCIE 8	

U2001B

PCI-E* Controller Link

SMBus

PEG

From CLK BUFFER

Clock Flex

iBEXPEAK-M

PCIE7,8:

EDS 1.0: port7,port8 may not be available in all PCH SKUs.

Note: Place these resisters near to PCIe Slots

PCH CLKREQ Setting:

Not connected to device.

Connected to device.

Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

R1.2,item L1

R1.1,item 25

R2120: For Xtal measurement

Title : PCIE,CLK,SMB,PEG

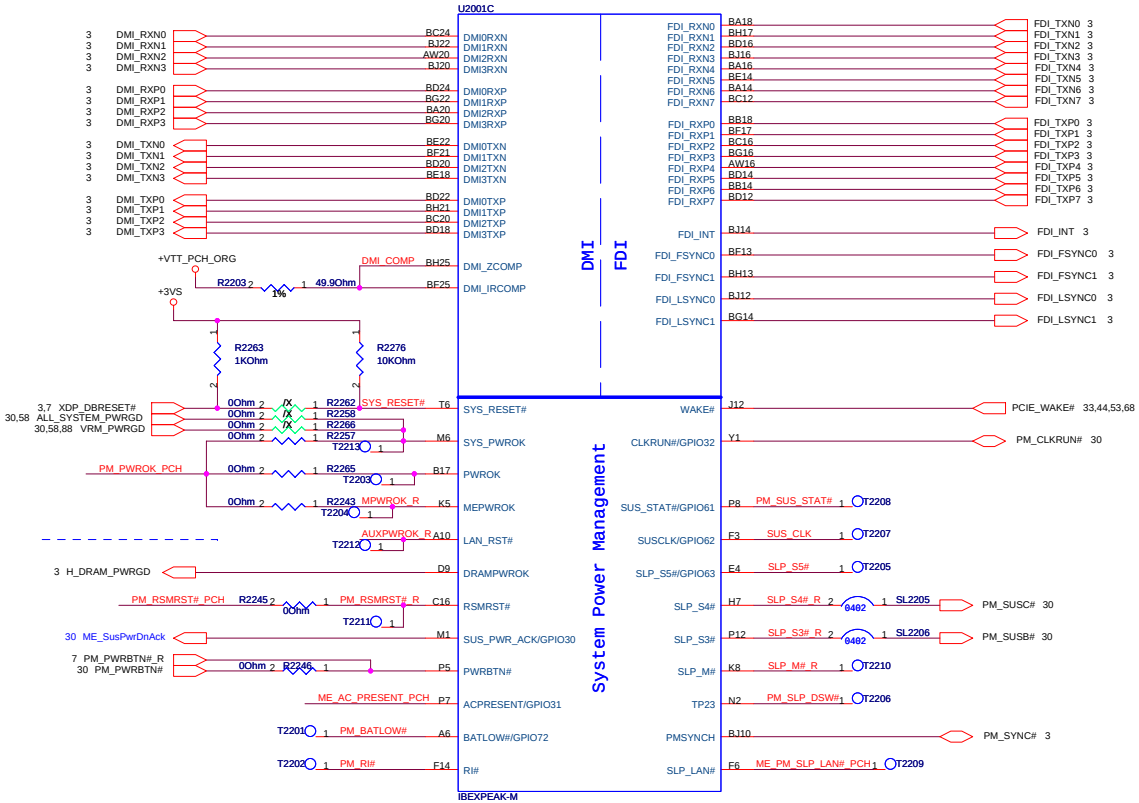
ASUSTeK COMPUTER INC. NB6

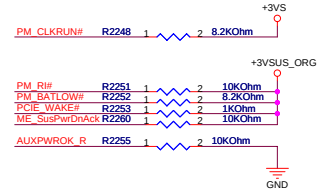
Engineer: yun-feng_yan

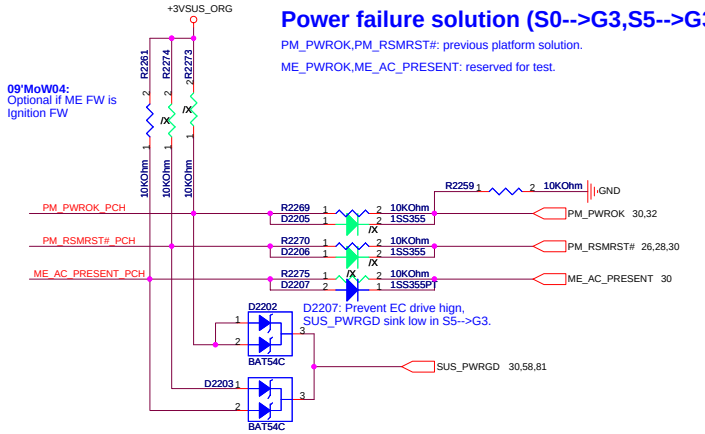
Size: Custom | Project Name: N61Jv | Rev: 1.0

Date: Friday, December 11, 2009 | Sheet 21 of 95

pre-ES1 not support
Reversal Feature





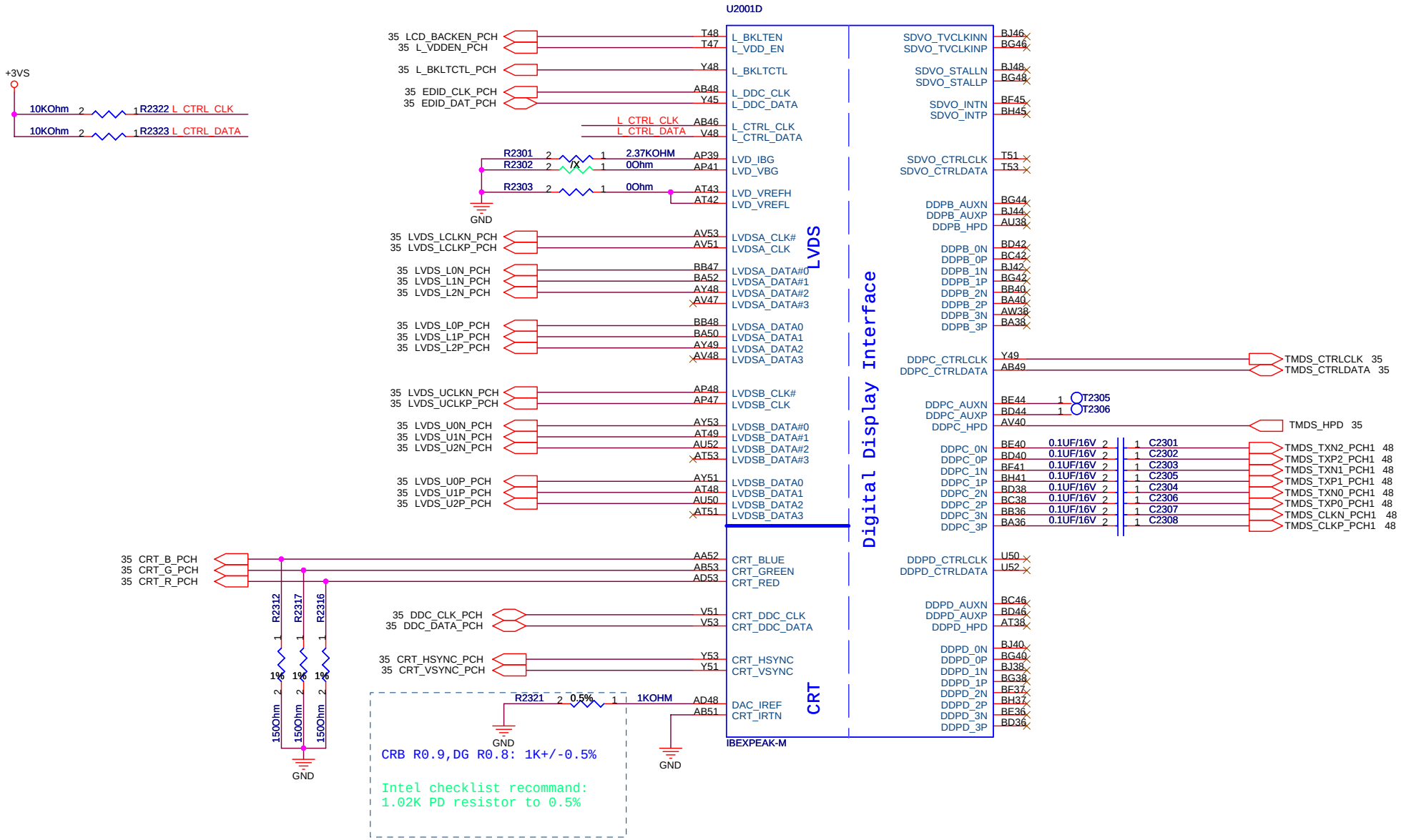


Power failure solution (S0-->G3,S5-->G3):

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

ASUSTeK COMPUTER INC. NB6	Title : FDI,DMI,SYS PWR		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 22 of 95		



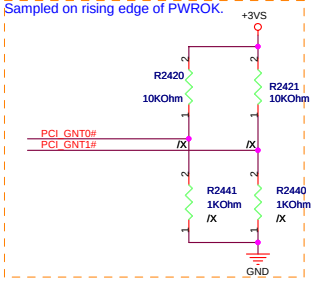
ASUSTeK COMPUTER INC. NB6	Title : DP,LVDS,CRT	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 23 of 95	

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

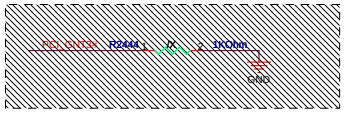
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.



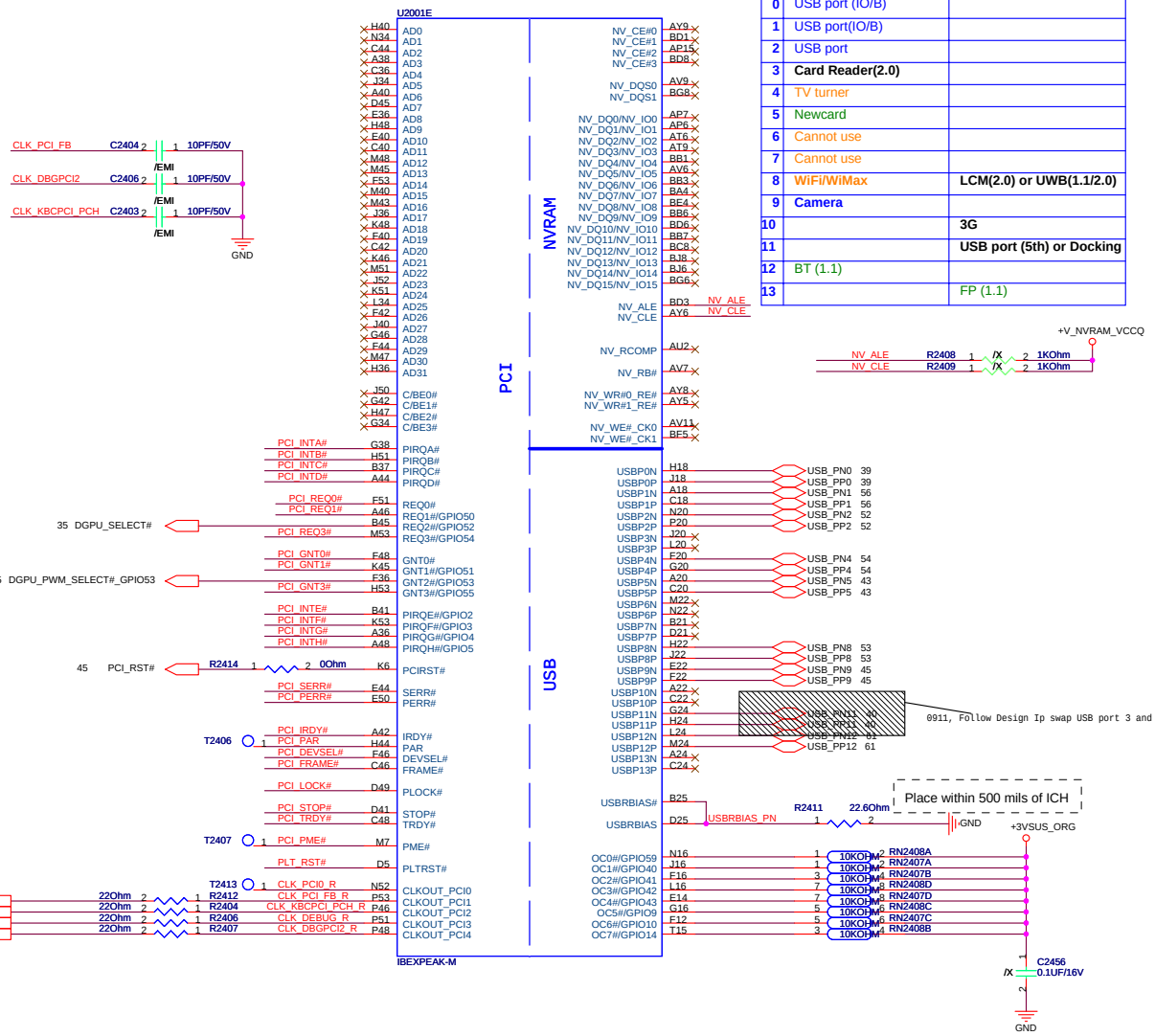
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

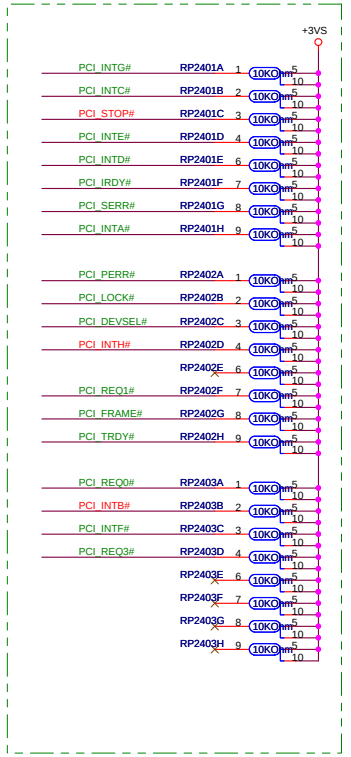
Low=Enabled A16 swap override/ Top-Block swap override
High=Default



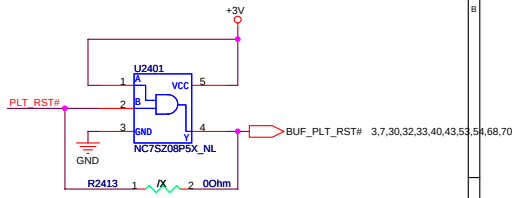
DGPU_SELECT#:
0=dGPU, 1=iGPU

	N61Jv	Recommand settings
0	USB port (IO/B)	
1	USB port(IO/B)	
2	USB port	
3	**Card Reader(2.0)**	
4	TV turner	
5	Newcard	
6	Cannot use	
7	Cannot use	
8	WiFi/WiMax	**LCM(2.0) or UWB(1.1/2.0)**
9	**Camera**	
10		**3G**
11		**USB port (5th) or Docking**
12	BT (1.1)	
13		FP (1.1)





R1.2,item L2

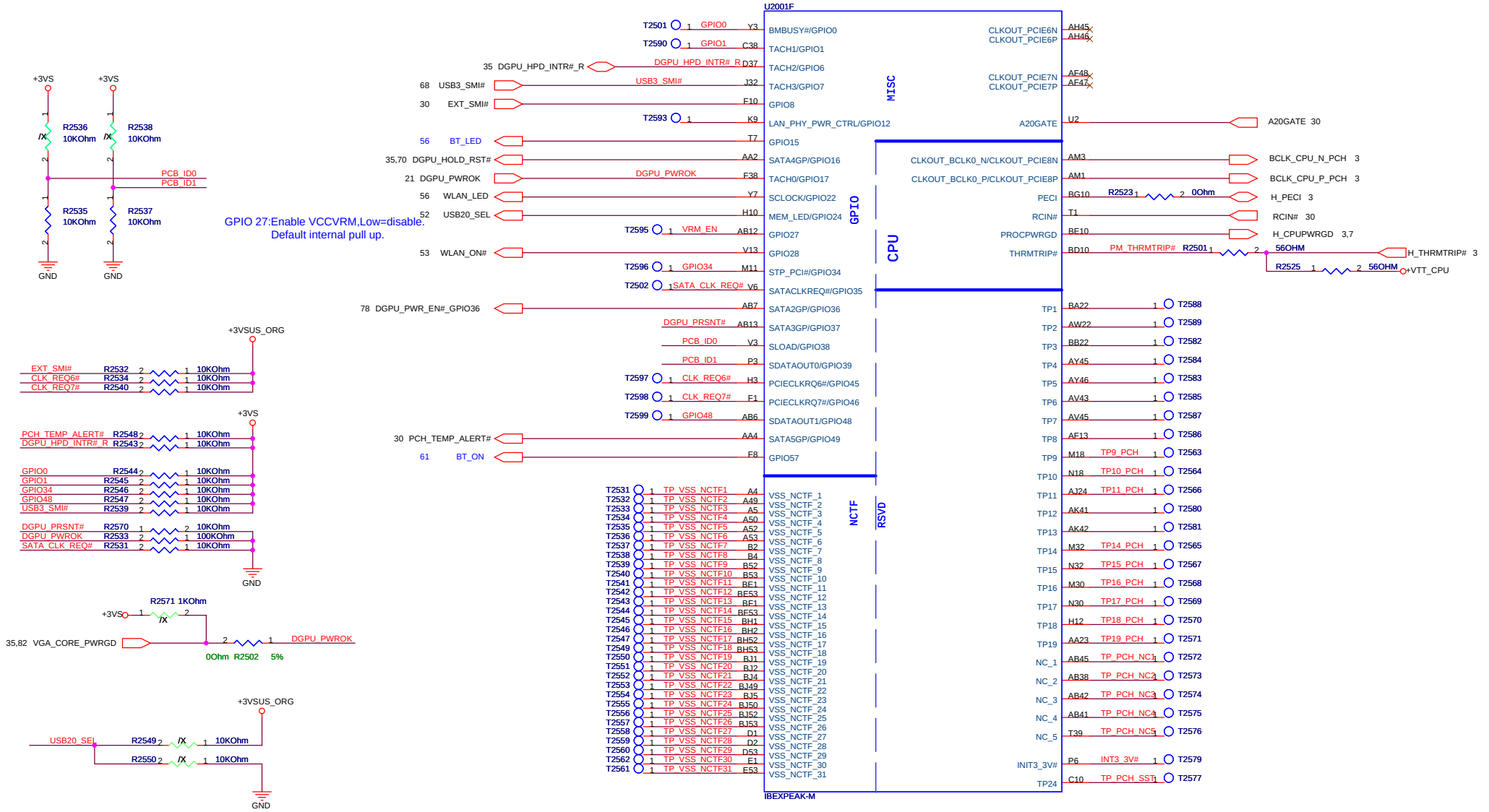


ASUSTeK COMPUTER INC. NB6
Engineer: yun-feng_yan

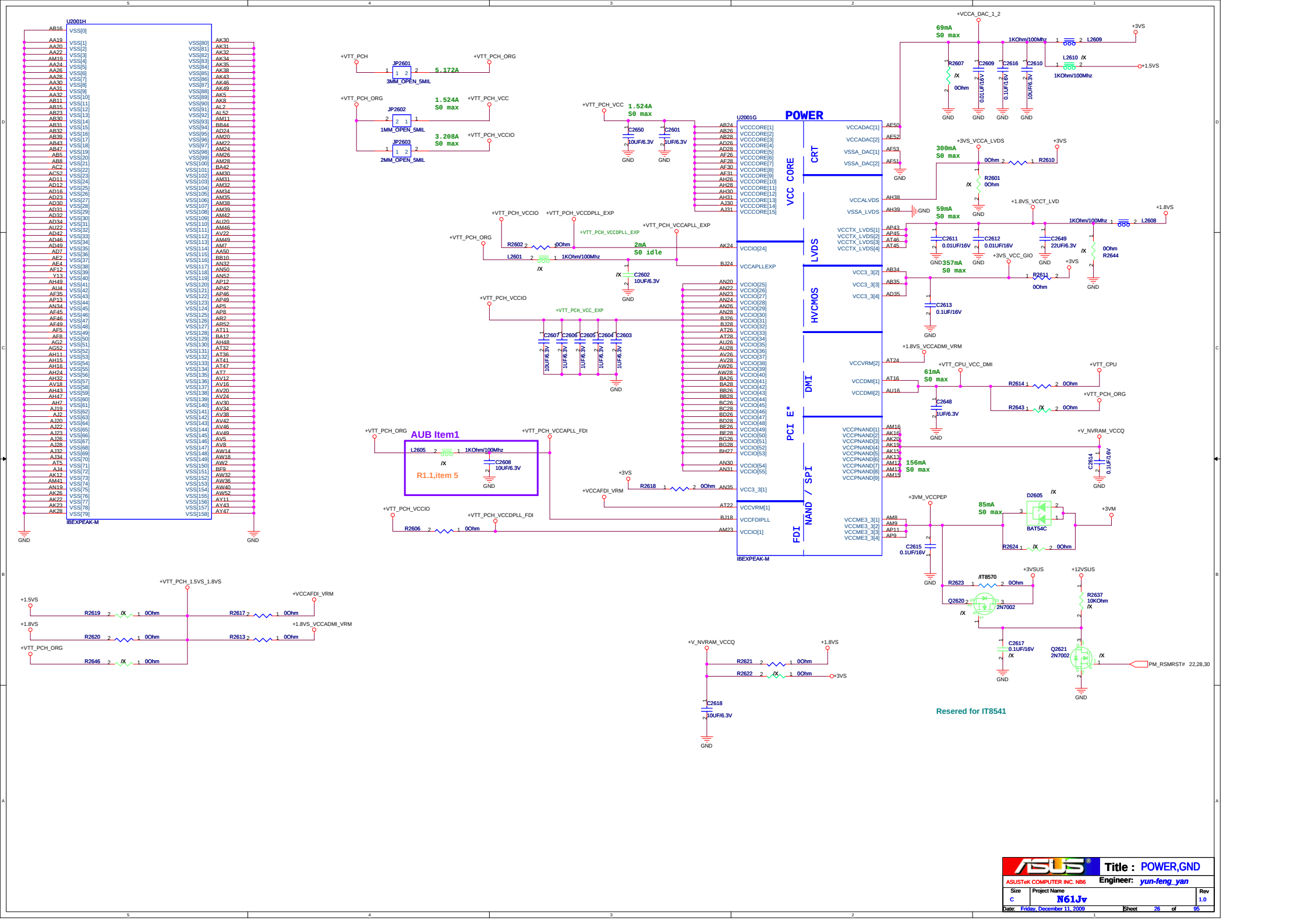
Title : PCI,NVRAM,USB

Size	Project Name	Rev
Custom	N61Jv	1.0

Date: Tuesday, December 15, 2009 Sheet 24 of 95



Title : CPU,GPIO,MISC			
ASUSTeK COMPUTER INC. NB6	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 25 of 95		


U2001H
IBEXPEAK-M
U2001G
IBEXPEAK-M
POWER
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
AUB Item1
R1.1,item 5
Resered for IT8541
Title : POWER,GND
ASUSTeK COMPUTER INC. NB6
Engineer: yun-feng_yan
Project Name N61Jv
Size C
Rev 1.0
Date: Friday, December 11, 2009
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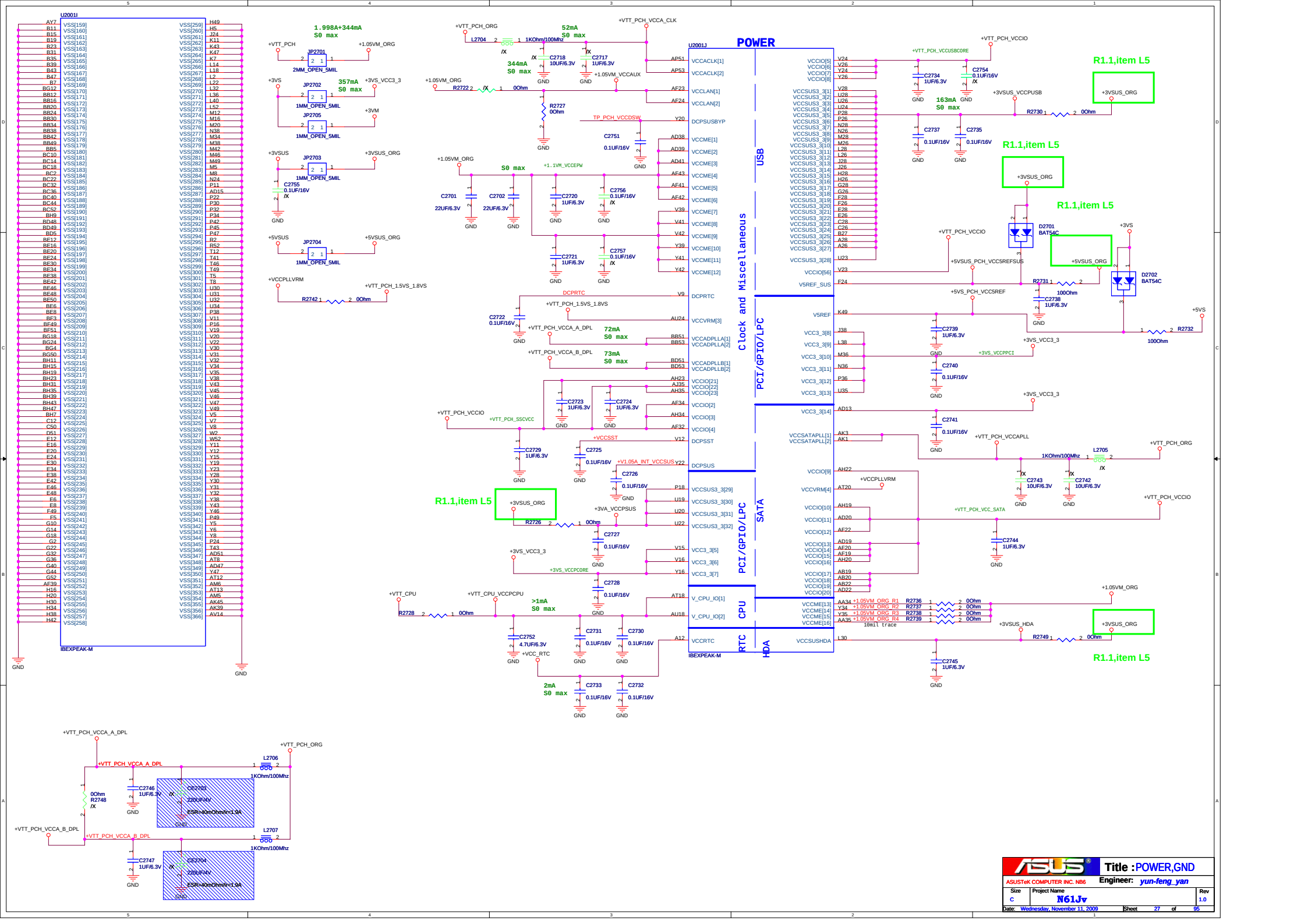
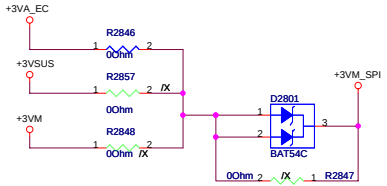

POWER
U2001J
iBEXPEAK-M
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
1.998A+344mA
S0 max
52mA
S0 max
344mA
S0 max
357mA
S0 max
73mA
S0 max
72mA
S0 max
163mA
S0 max
2mA
S0 max
>1mA
S0 max
R1.1,item L5
+VTT_PCH_VCCA_CLK
+VTT_PCH_ORG
+VTT_PCH
+1.05VM_ORG
+1.05VM_VCCAUX
+3VS
+3VM
+3VS_VCC3_3
+3VSUS
+5VSUS
+VCCPLLVRM
+VTT_PCH_1.5VS_1.8VS
+1.1VM_VCCEPW
+VTT_PCH_VCCIO
+VTT_PCH_VCCUSBCORE
+3VSUS_VCCPUSB
+5VSUS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VS_VCCPPCI
+VTT_PCH_VCCAPLL
+VTT_PCH_VCC_SATA
+3VA_VCCPSUS
+3VS_VCCPCORE
+VTT_CPU
+VTT_CPU_VCCPCPU
+VCC_RTC
+V1.05A_INT_VCCSUS
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+3VSUS_ORG
+5VSUS_ORG
+3VS
+5VS
+1.05VM_ORG
+3VSUS_HDA
+VCCPLLVRM
+VTT_PCH_ORG
+VTT_PCH_VCCIO
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG
iBEXPEAK-M
Title :POWER,GND
ASUSTeK COMPUTER INC. NB6
Engineer: yun-feng_yan
Size C
Project Name N61Jv
Rev 1.0
Date: Wednesday, November 11, 2009
Sheet 27 of 95

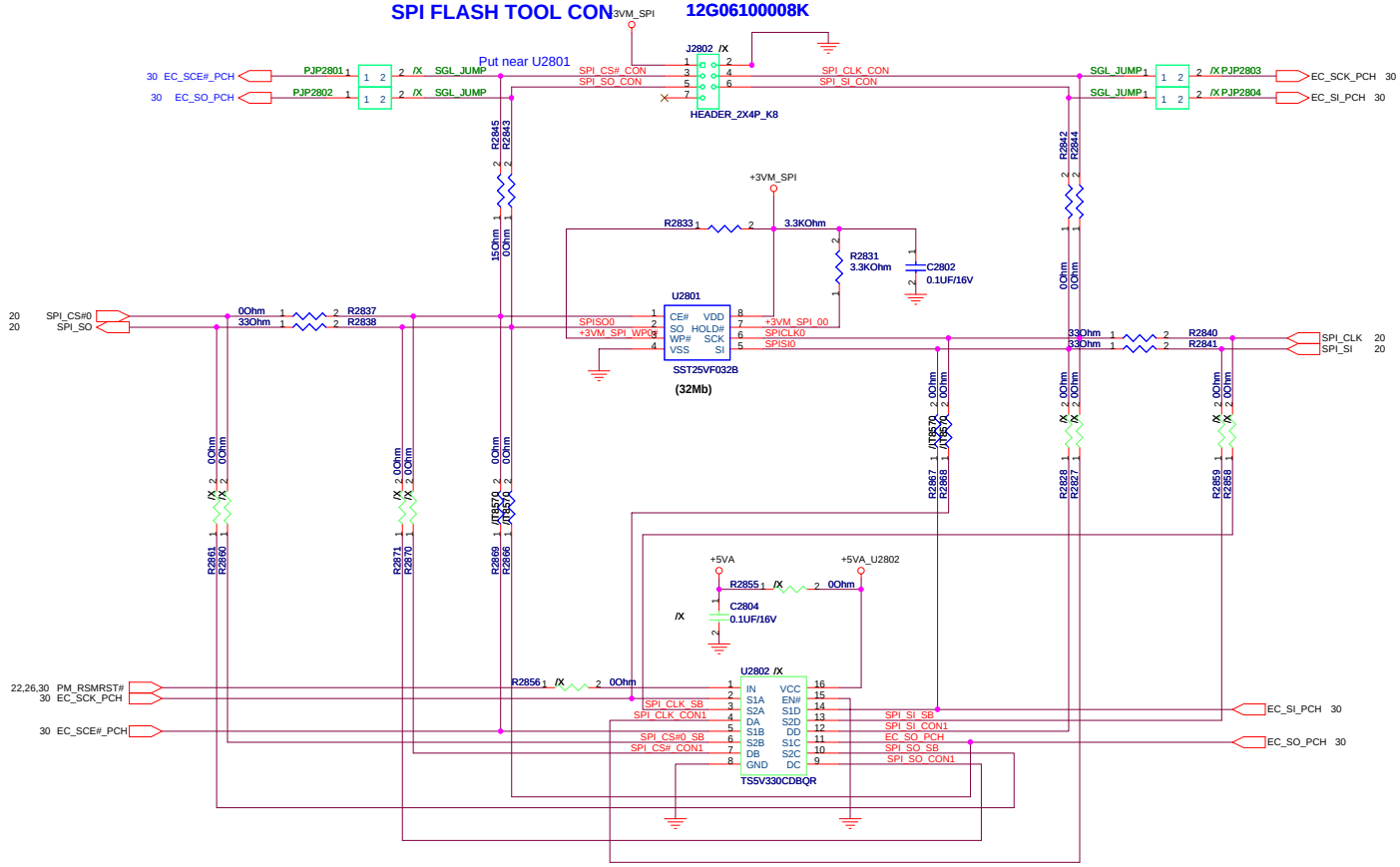
PCH SPI ROM



SPI FLASH TOOL CON

12G06100008K

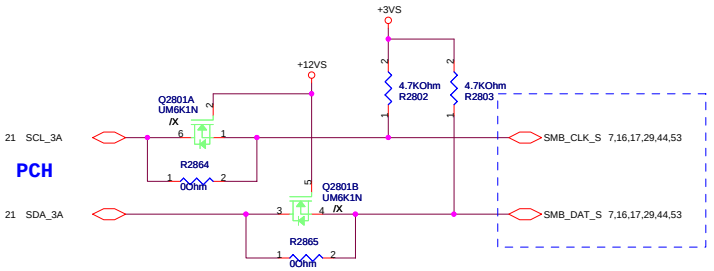
Put near U2801

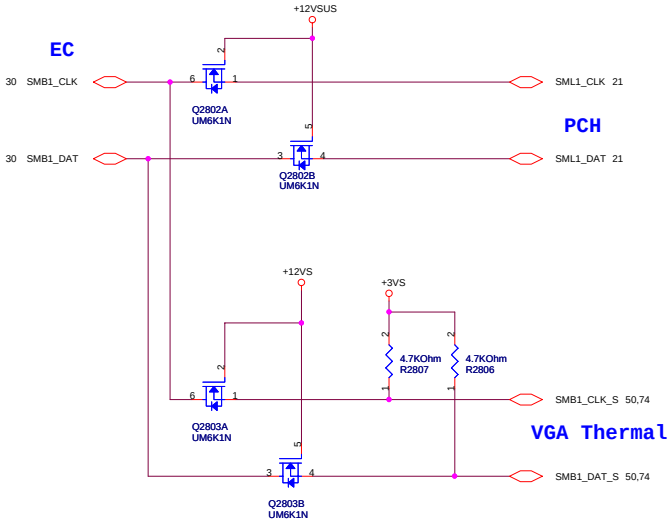


SMBUS Link device:

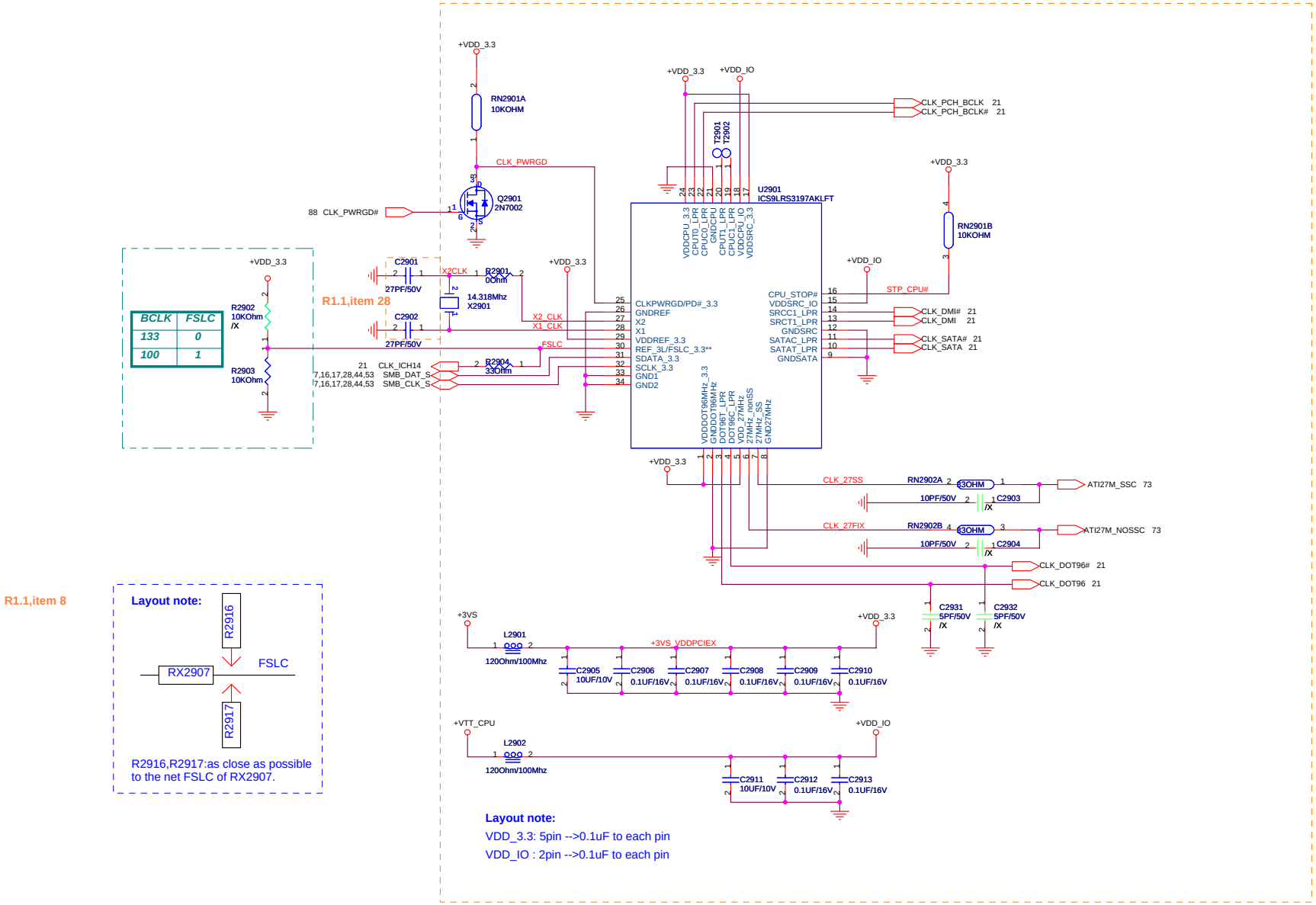
[M52J] SPD, CLKGEN,DEBUG,WLAN,
CPU XDP,PCH XDP,VID CONTROLLER

[G50J] FM2010,GAME LED,





ASUSTeK COMPUTER INC. NB6	Title : SPI ROM,OTH	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 28 of 95	

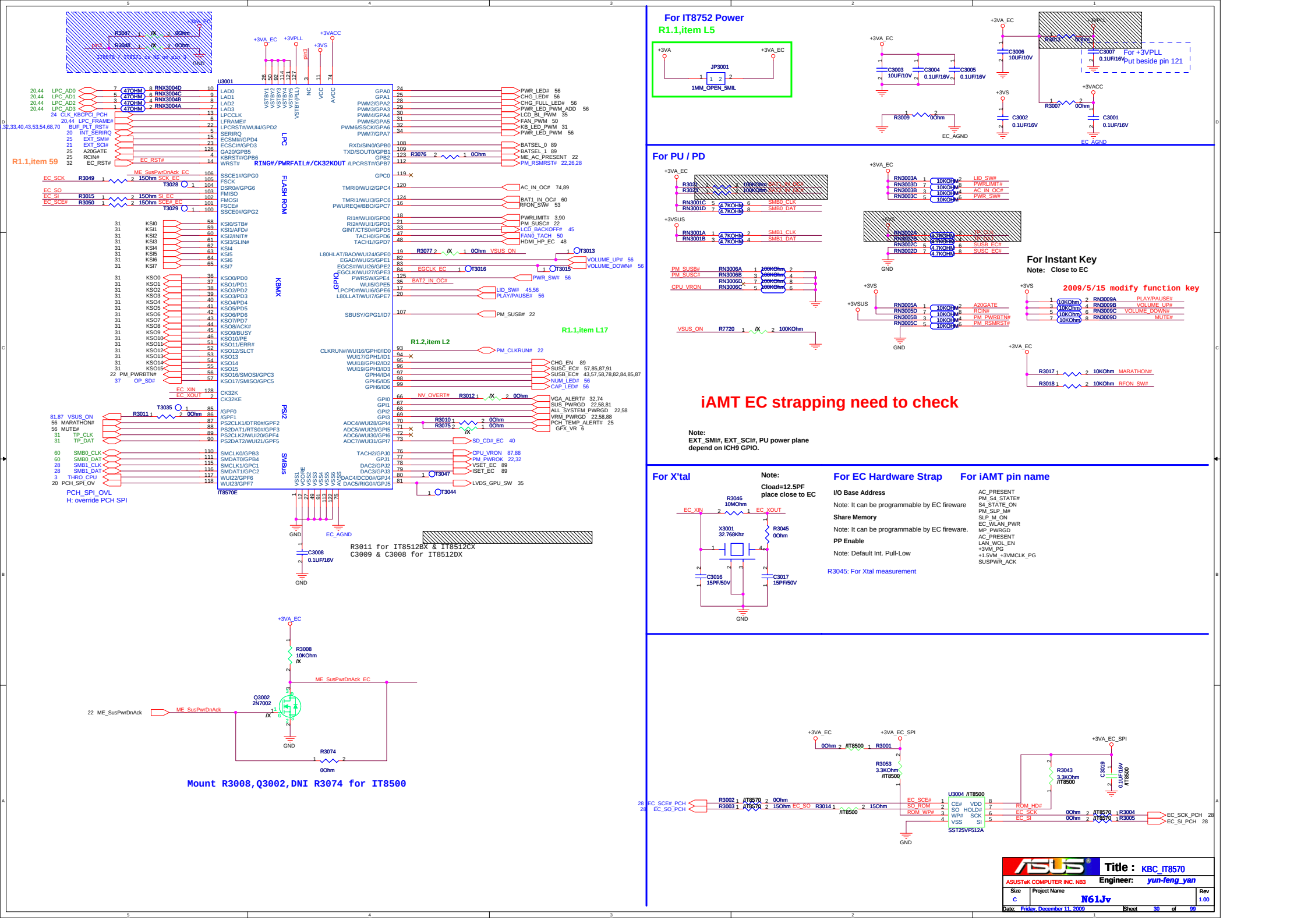


R1.1,item 8

Layout note:

R2916,R2917:as close as possible to the net FSLC of RX2907.

ASUSTeK COMPUTER INC. NB4	Title : CLK_ICS9LRS3197		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 29 of 95		


For IT8752 Power
R1.1,item L5
JP3001
1MM_OPEN_5MIL
For PU / PD
For Instant Key
Note: Close to EC
2009/5/15 modify function key
iAMT EC strapping need to check
Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH9 GPIO.
For X'tal
Note:
Cload=12.5PF
place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
R3045: For Xtal measurement
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
R1.1,item 59
R1.1,item L17
R1.2,item L2
PCH_SPI_OVL
H: override PCH SPI
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
Mount R3008,Q3002,DNI R3074 for IT8500
Title : KBC_IT8570
ASUSTeK COMPUTER INC. NB3
Engineer: yun-feng_yan
Size C
Project Name N61Jv
Rev 1.00
Date: Friday, December 11, 2009
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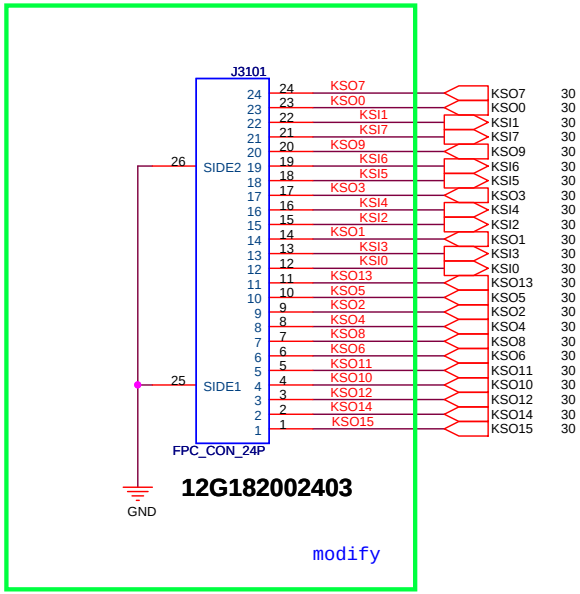
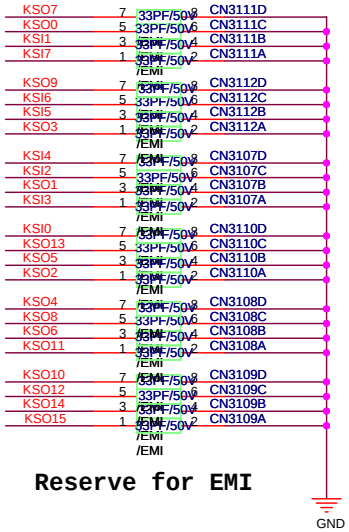
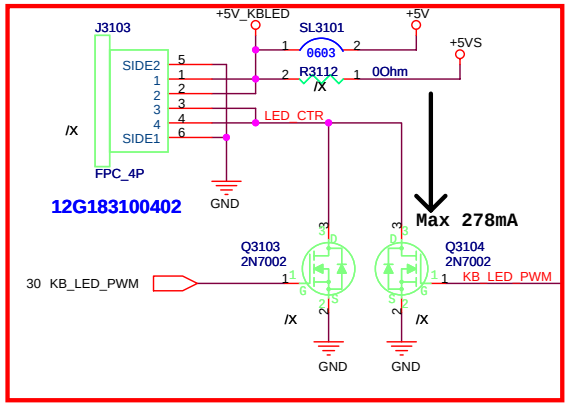
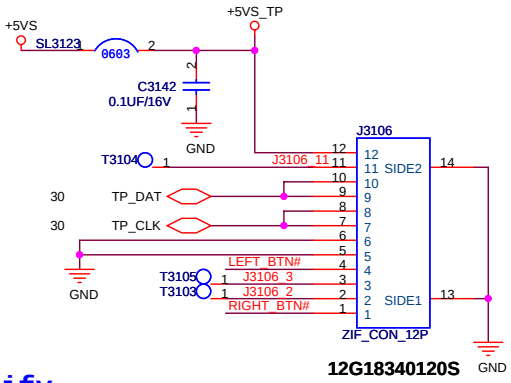
For Keyboard

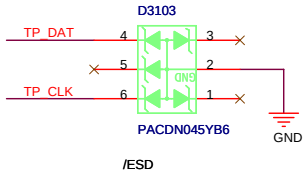




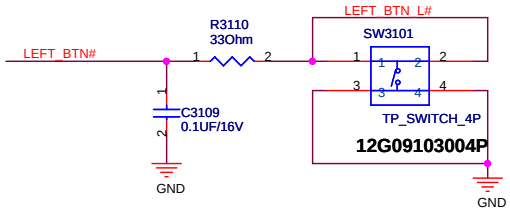
KB LED

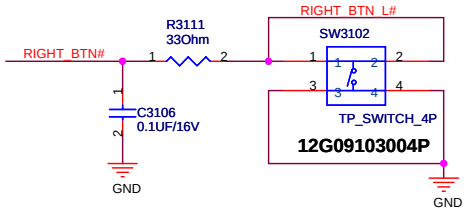






modify

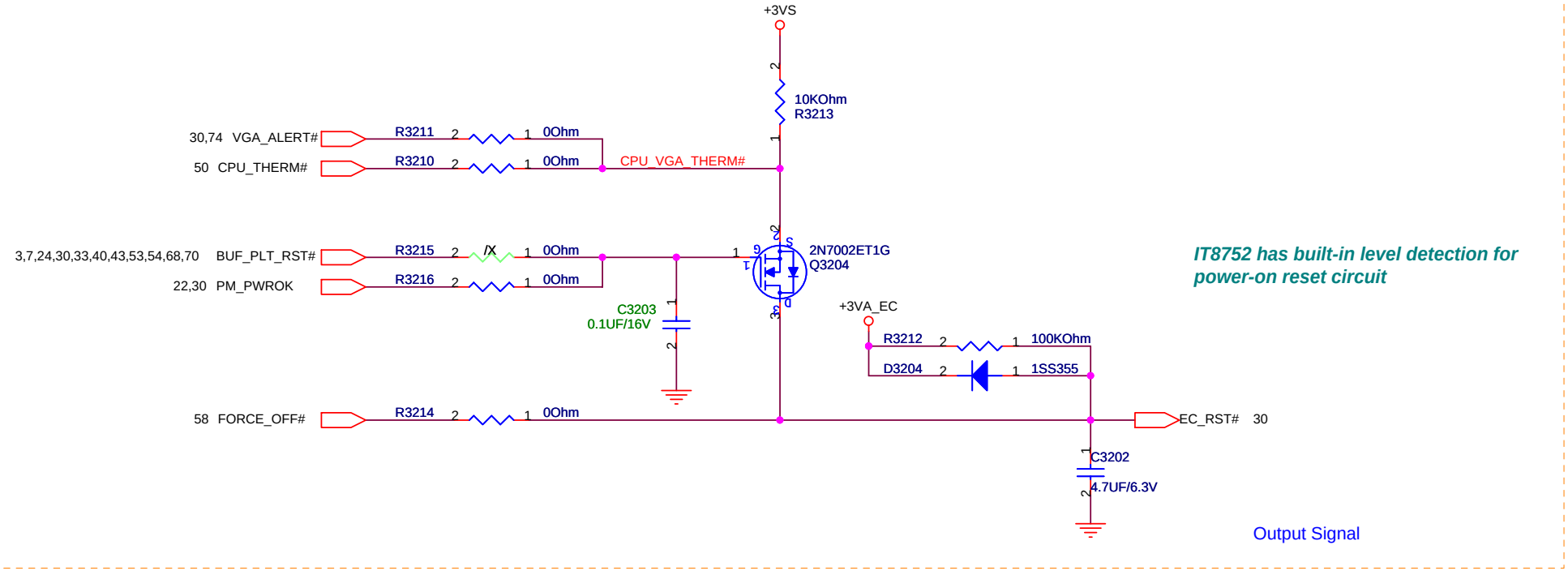




Main Board

Title :	IT8512_KB, TP
ASUSTeK COMPUTER INC. NB4	Engineer: yun-feng_yan
Size: Custom	Project Name: N61Jv
Rev: 1.0	
Date: Tuesday, December 15, 2009	Sheet 31 of 95

Main Board



ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 32 of 95	

AR8131:Remove R3301,C3318
AR8121:Remove L3302,C3317,R3302

C3318 close to Pin 1

PIN_1

PIN_6

2009/5/18 change

AR8131:C3319=0.1uF
AR8121:C3319=1uF

AR8131 with overclock: Remove R3315

AR8121:Remove R3315

RF 預留

AR8131:Remove L3303
AR8131:C3321=0.1uF, Remove C3322

With overclock:Remove R3312
Not overclock:Remove R3304

AR8131:L3304=0ohm

For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301
For AR8121: Remove C3327 R3308
Q3301 close to Pin8

PIN_5

AR8121: Remove R3313
AR8131: Remove R3314

AR8121:Remove R3310
AR8131/25MHz:Remove R3310 C3333
AR8131/48MHz:Remove C3333

ground pad要打散熱孔

For AR8131 : Remove R3309

AR8121:Remove C3328
AR8131/25MHz: Remove C3328
AR8131/48MHz: Remove C3329 C3330 X3301

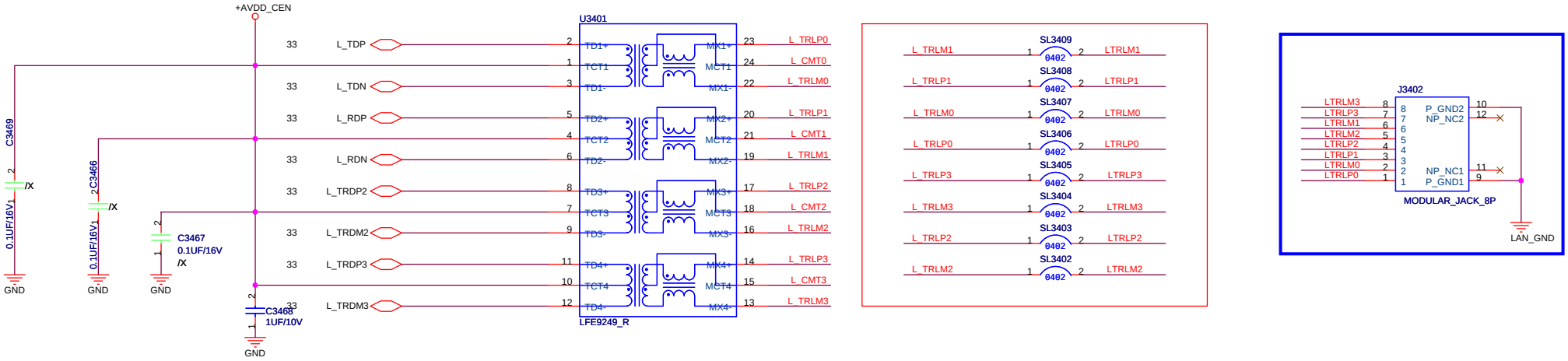
4/10 限高問題, 換料為 07G010S22500

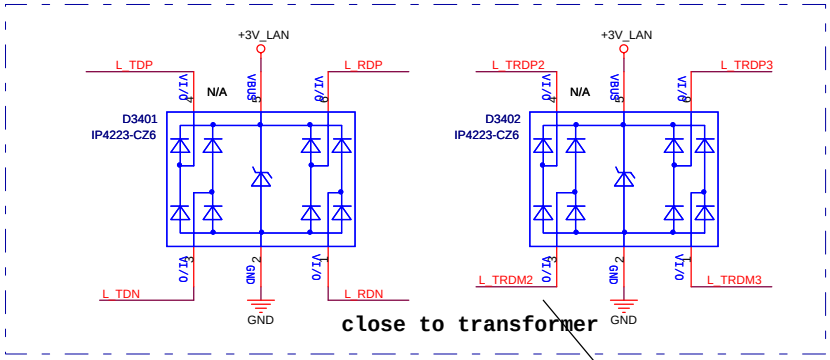
C3301 C3302 C3303 C3304 close to pin2

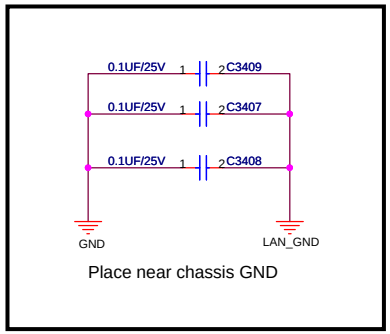
C3305 close to pin15

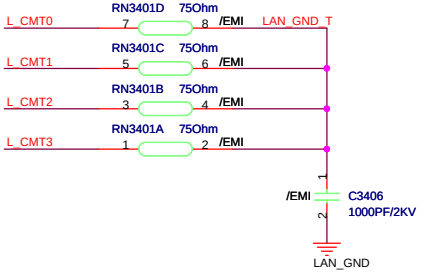
C3308 close to pin45/46

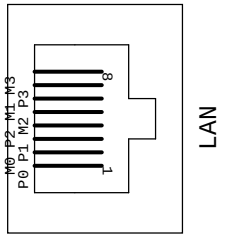
Title :	LAN AR8131
ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan
Size: Custom	Project Name: N61Jv
Rev: 1.0	
Date: Friday, December 11, 2009	Sheet 33 of 95









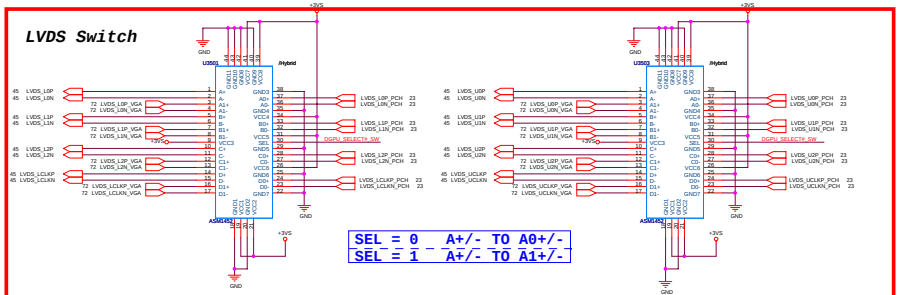


07G001250010 э 07G028075010 (3/30)

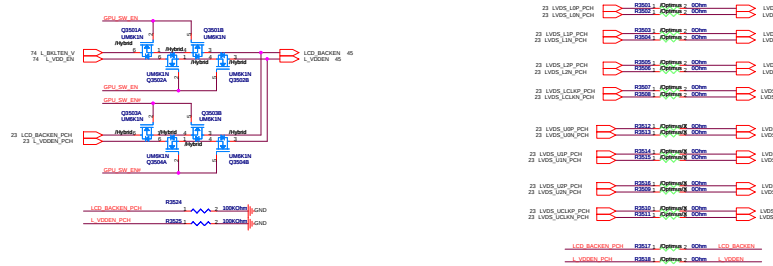
0911, change D3401 and D3402 stuff by default.

ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Monday, December 14, 2009	Sheet 34 of 95	

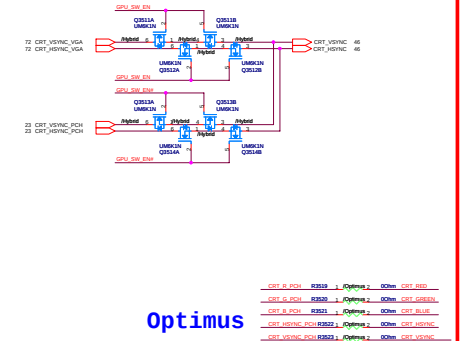
LVDS Switch



Optimus

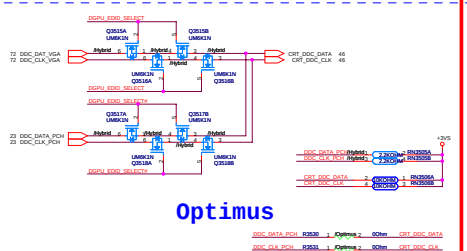


Optimus

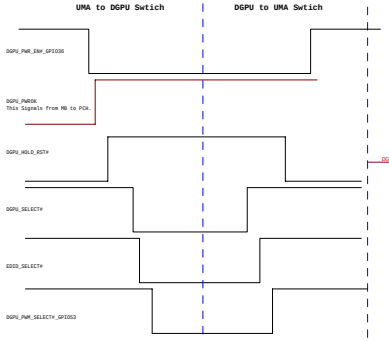


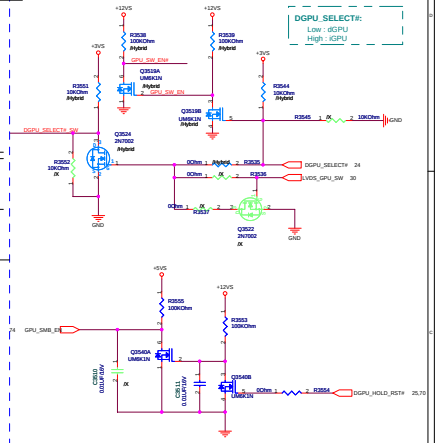
Optimus

Optimus

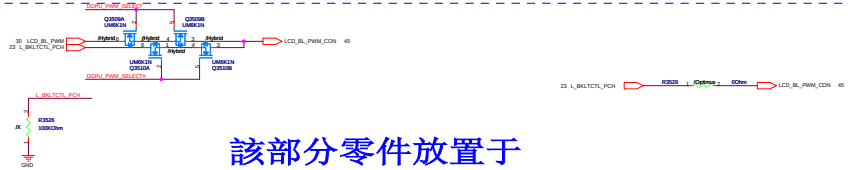


Control Signal from PCH

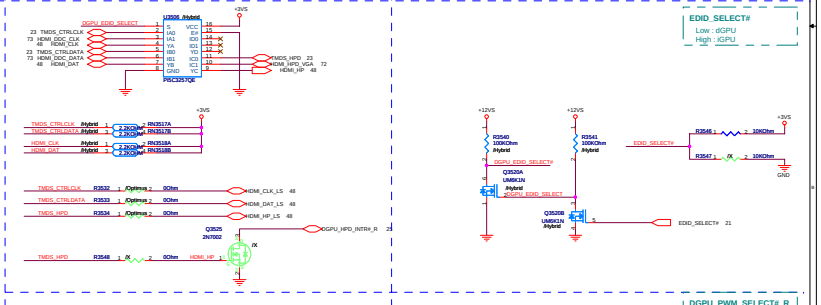


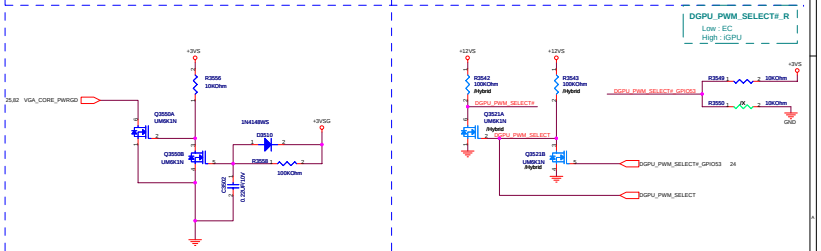


該部分零件放置于 LVDS Connector J4502 附近



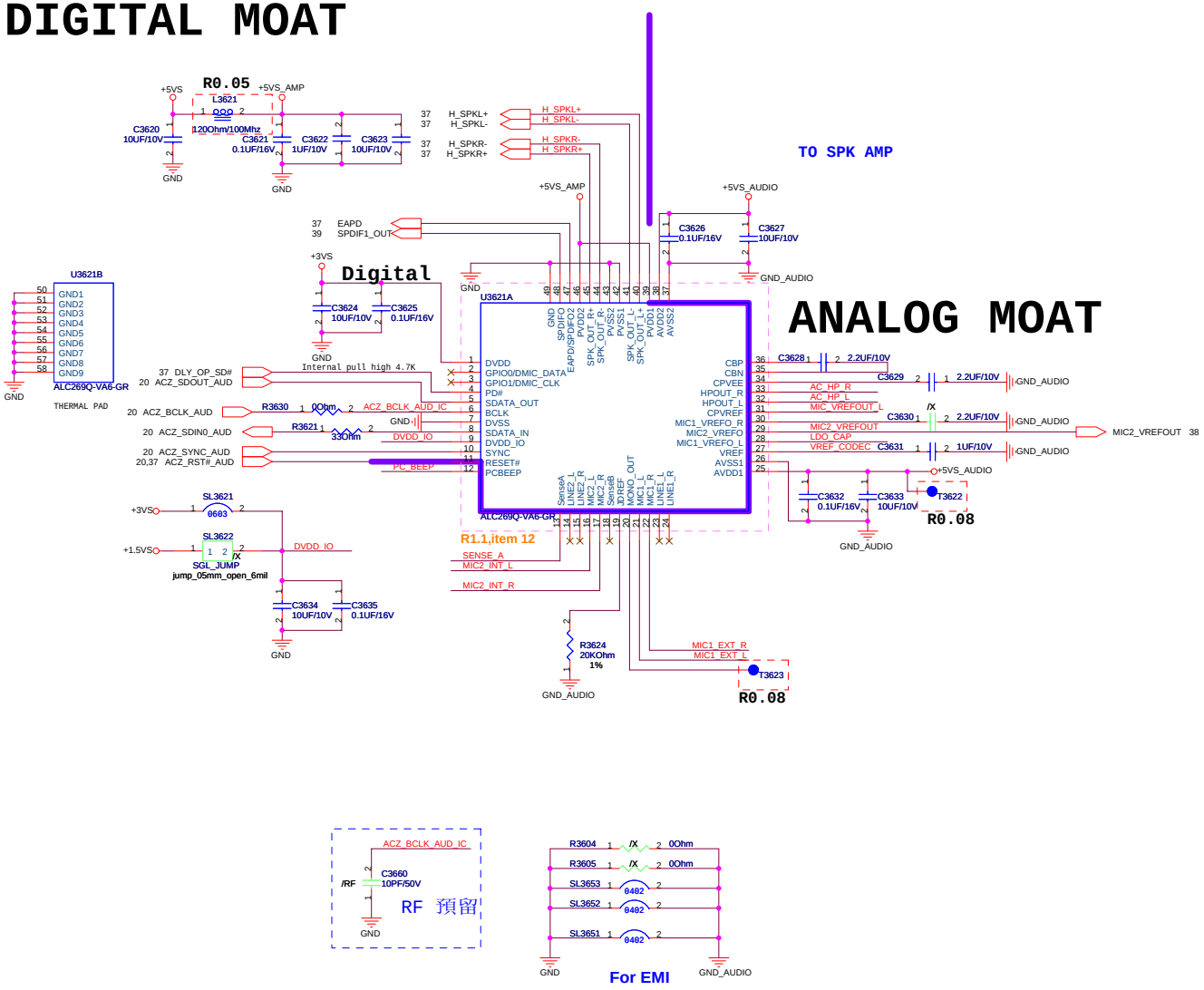
該部分零件放置于 VGA Connector J4601 附近



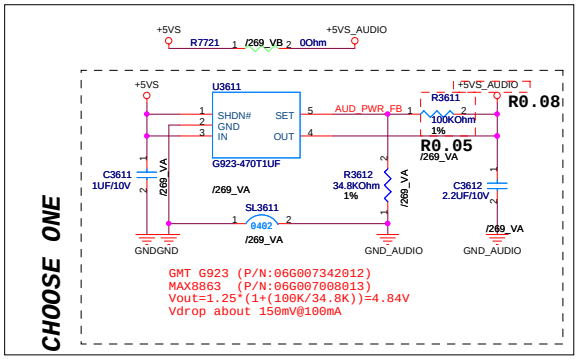


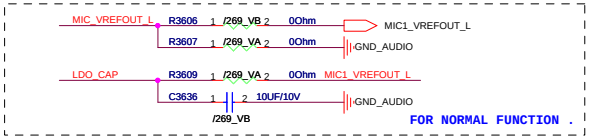
ASUSTeK COMPUTER INC. NB1	Title : Hybrid Switch		
	Engineer: yuan-feng_yan		
Size: Custom	Project Name: N61Jv	Rev: 1.0	
Date: Tuesday, December 16, 2008	Sheet 35 of 55		

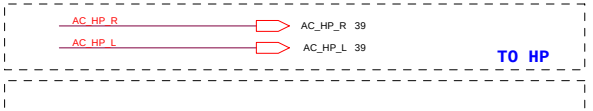
DIGITAL MOAT

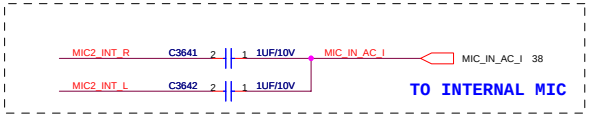


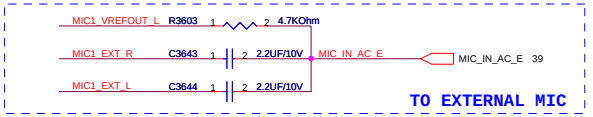
AUDIO POWER

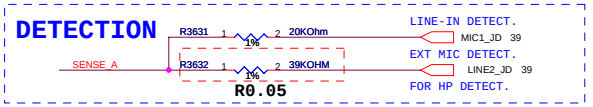


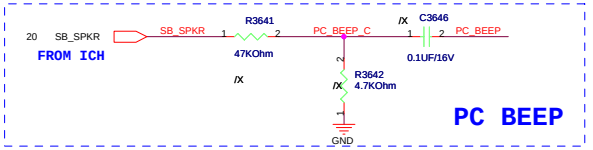












<Variant Name>
Title : CODEC ALC 269
ASUSTeK COMPUTER INC. NB2
Engineer: yun-feng_yan
Size: Custom
Project Name: N61Jv
Rev: 1.0
Date: Friday, December 11, 2009
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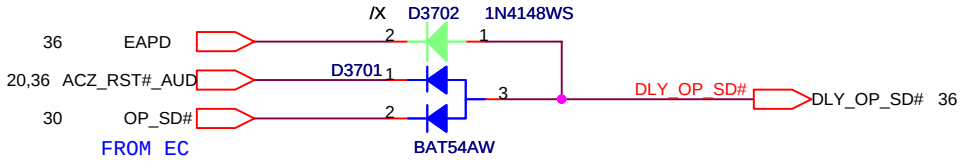
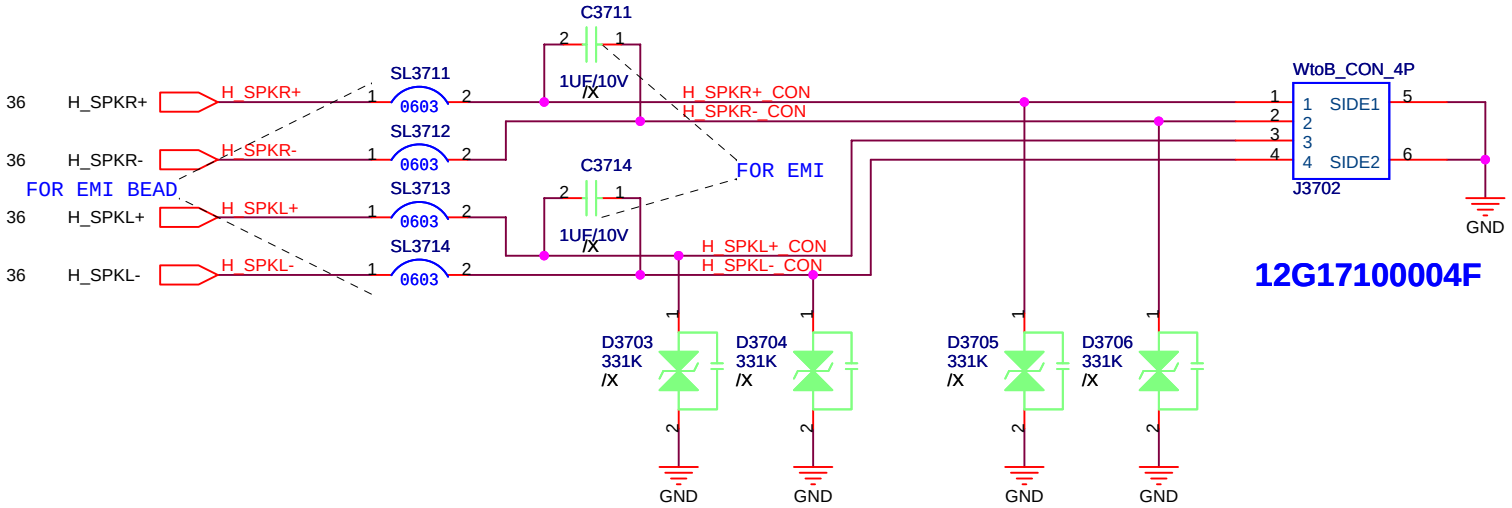
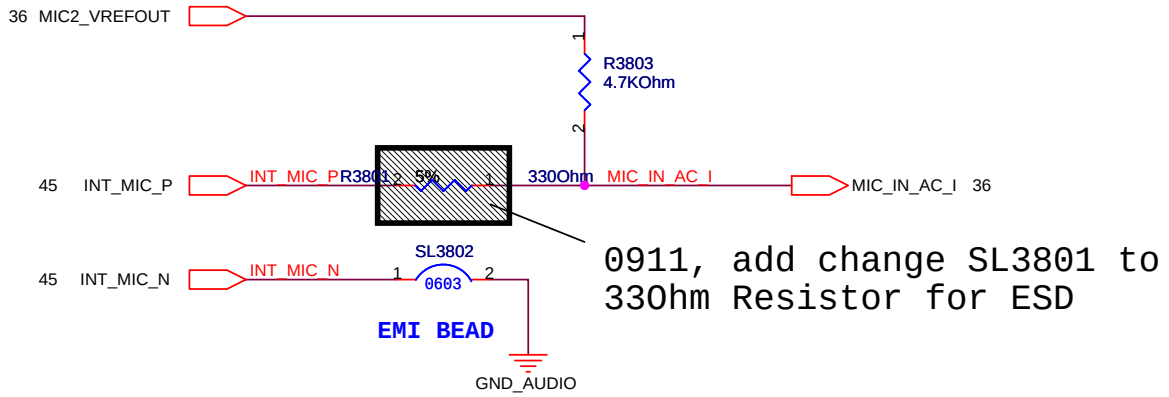
MUTE CONTROL





ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 37 of 95	

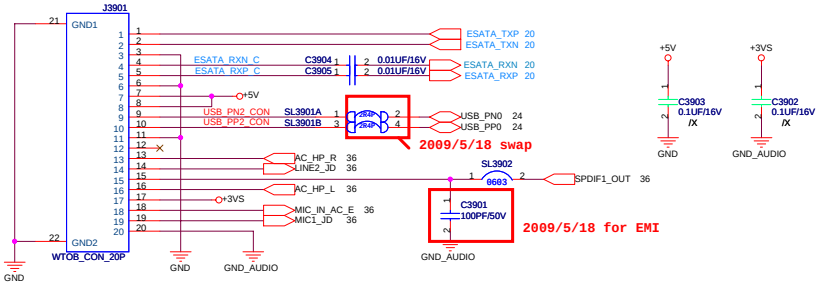
INTERNAL MICROPHONE



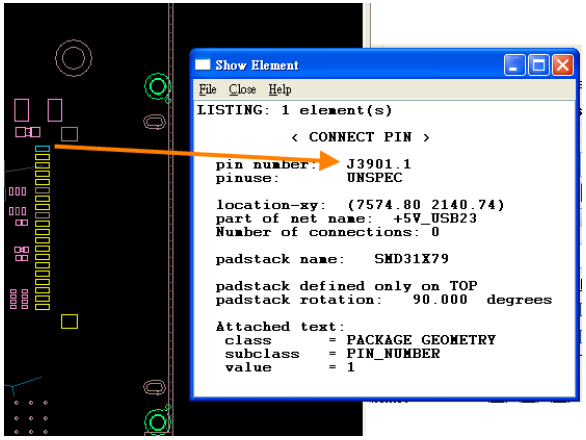
<Variant Name>

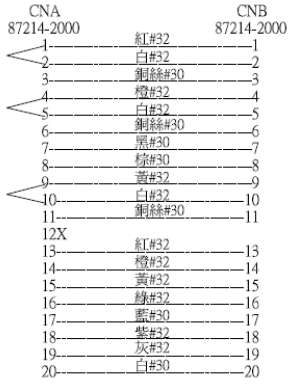
ASUSTeK COMPUTER INC. NB1	Title : MIC	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 38 of 95	

modify 0410

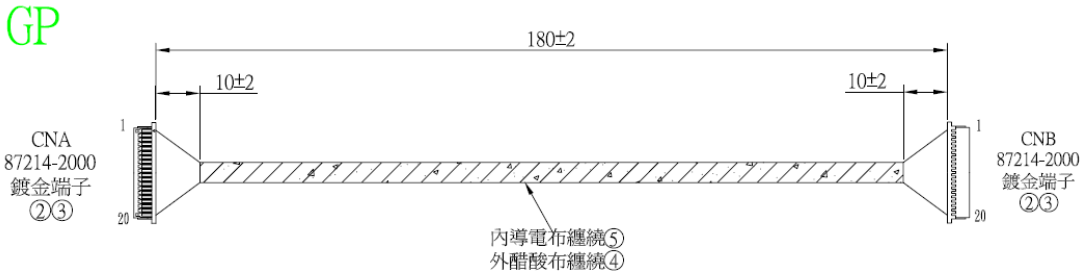


pin define

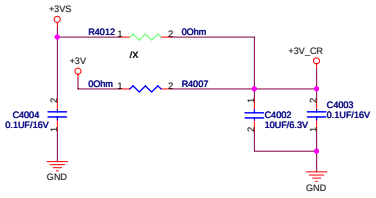


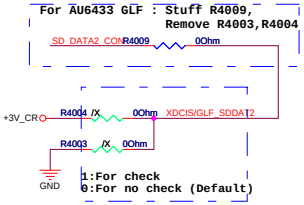


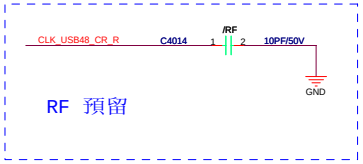
Follow U50 IO cable



ASUSTeK COMPUTER INC. NB1	Title : ****	
	Engineer: CH_Lin	
Size: C	Project Name: N61JA	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 39 of 95	

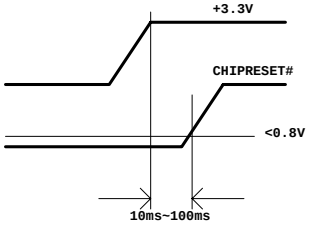


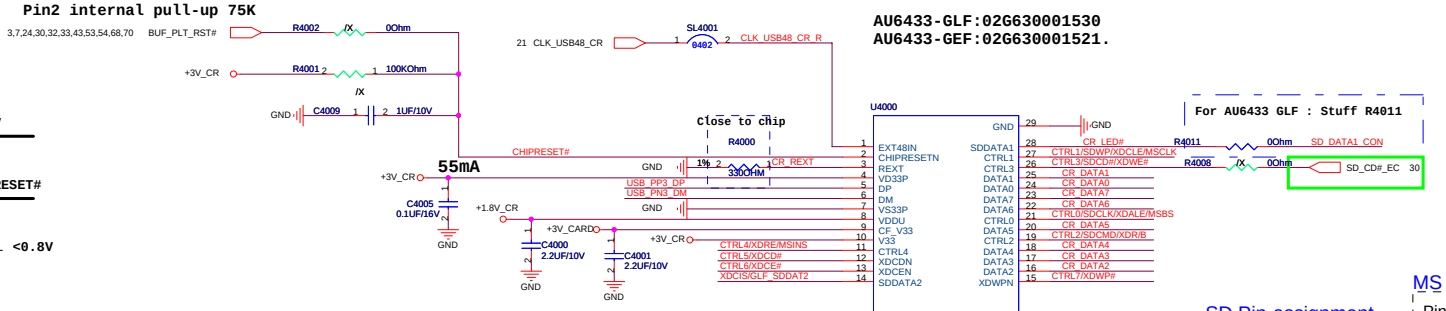




Pin2 internal pull-up 75K

Chip reset Timing:

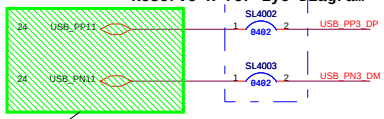




AU6433-GLF:02G630001530
AU6433-GEF:02G630001521.

02G630001530

Reserve R for Eye Diagram



0911, Follow Design Ip swap USB port 3 and Port 11

xD Pin-assignment

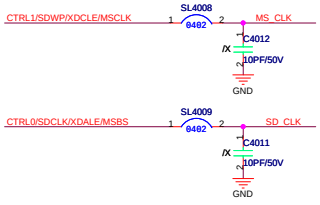
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

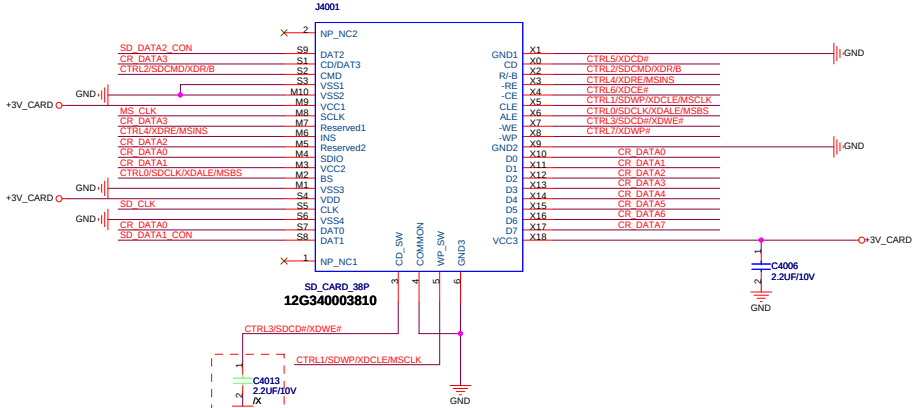
SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2

MS Pin-assignment

Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

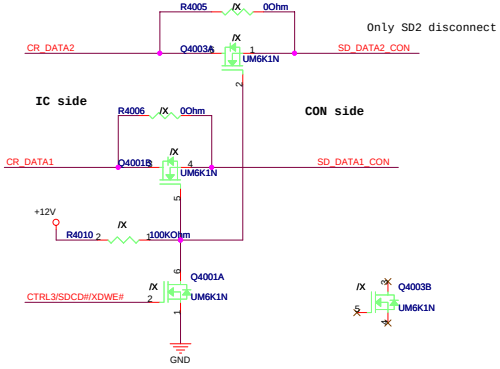




Modify: 0512

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

For AU6433-GLF: No stuff All
For AU6433-GEF: Stuff Q4000,Q4001,Q4003,R4010



Main Board

Title : HMDI Switch

ASUSTeK COMPUTER INC. NB4

Engineer: yun-feng_yan

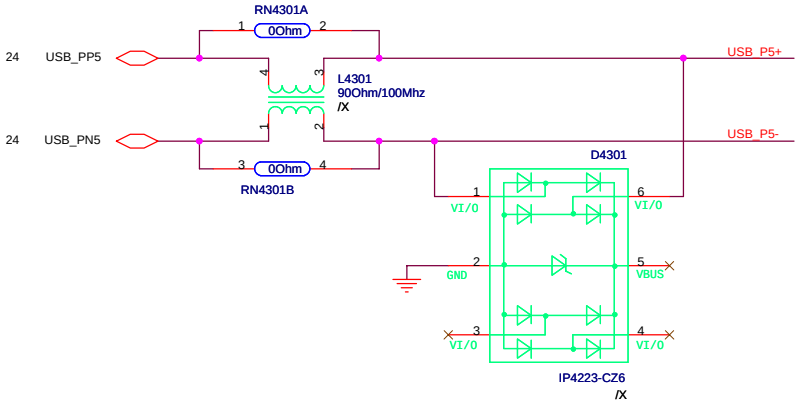
Size	Project Name	Rev
B	N61Jv	1.0

Date: Wednesday, November 11, 2009 Sheet 41 of 95

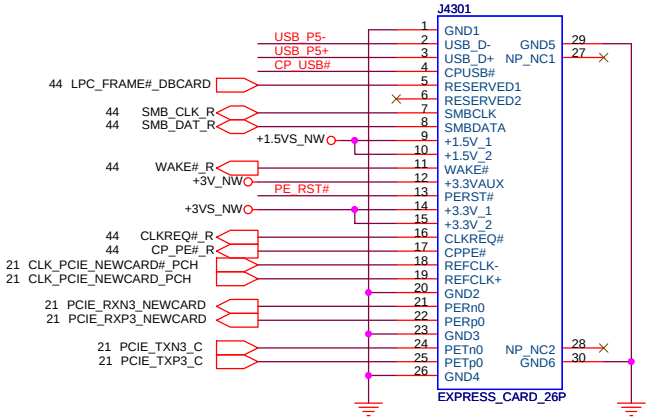
Main Board

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 42 of 95	

Main Board

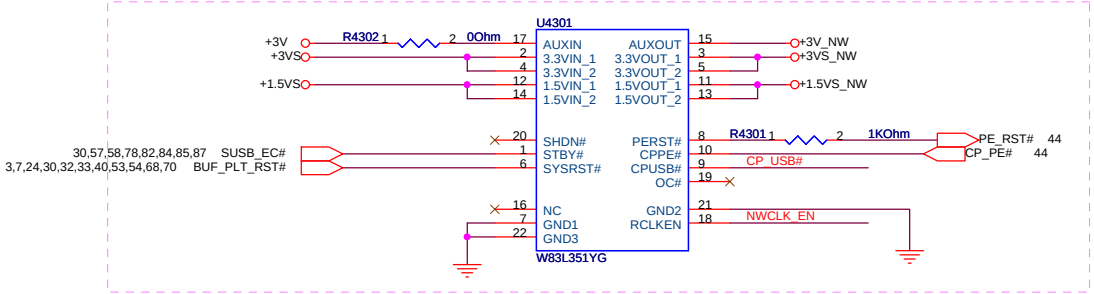


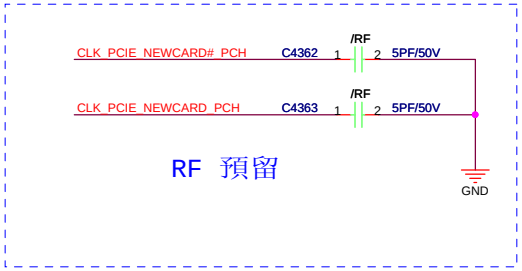
NewCard Header

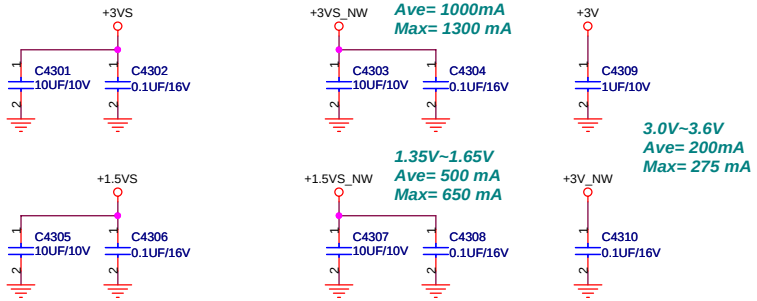


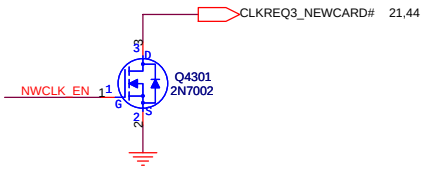
12G161300261

R2.00,item L9

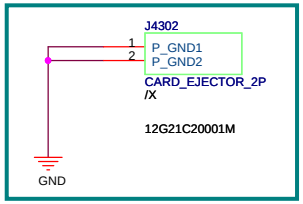






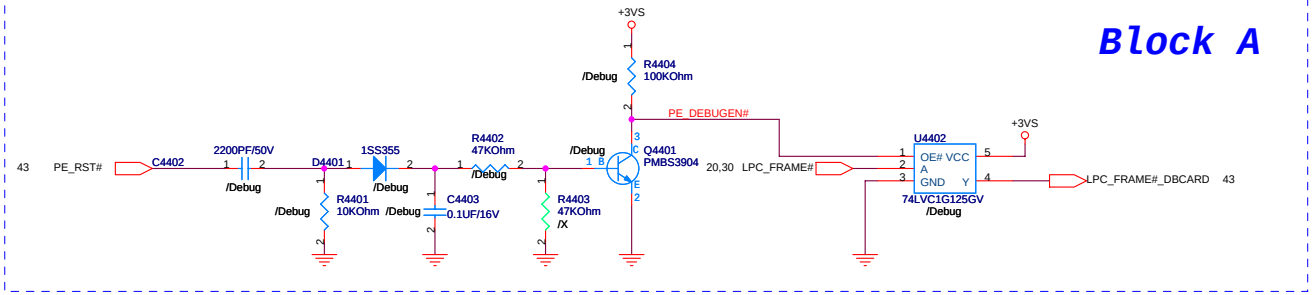


NewCard Ejecter

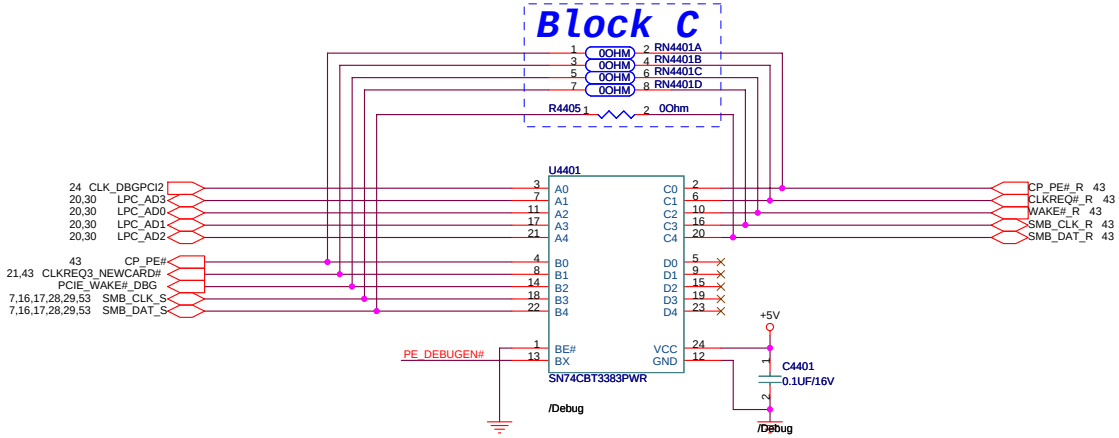


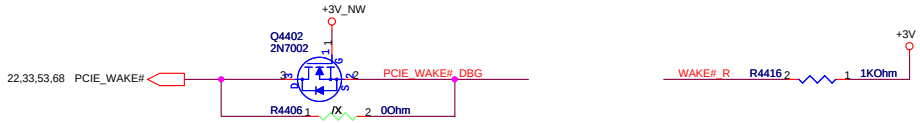
ASUSTeK COMPUTER INC. NB4	Title : CB_NewCard	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 43 of 95	

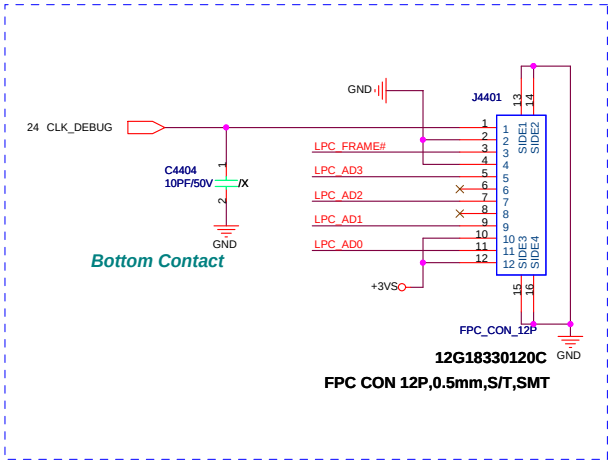
Block A



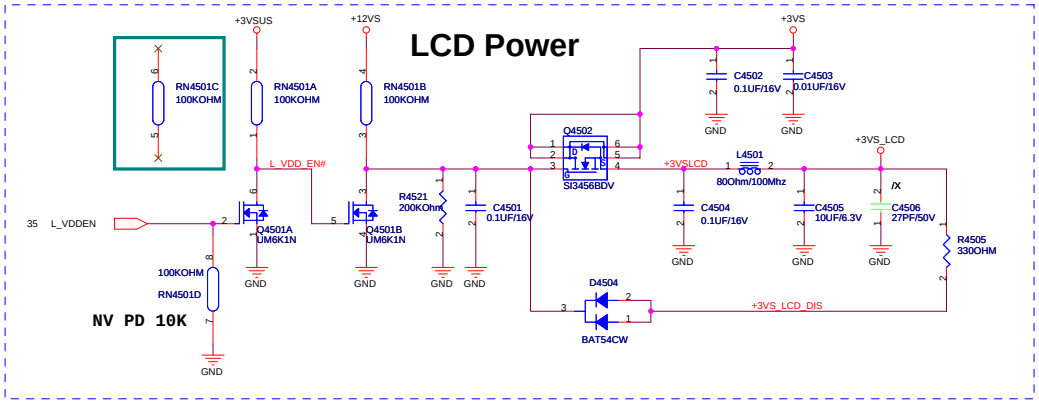
Block C

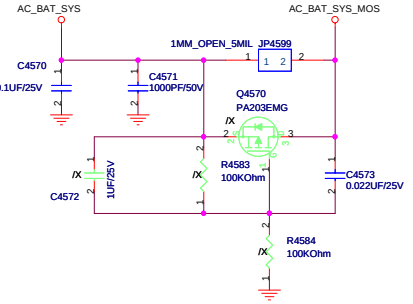


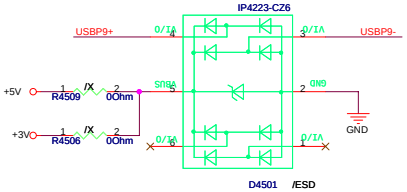


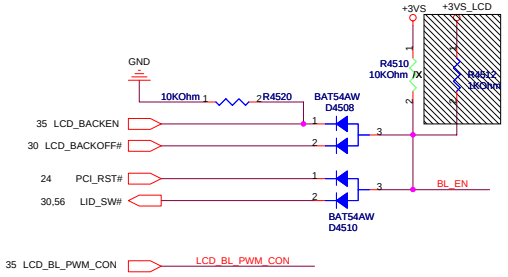


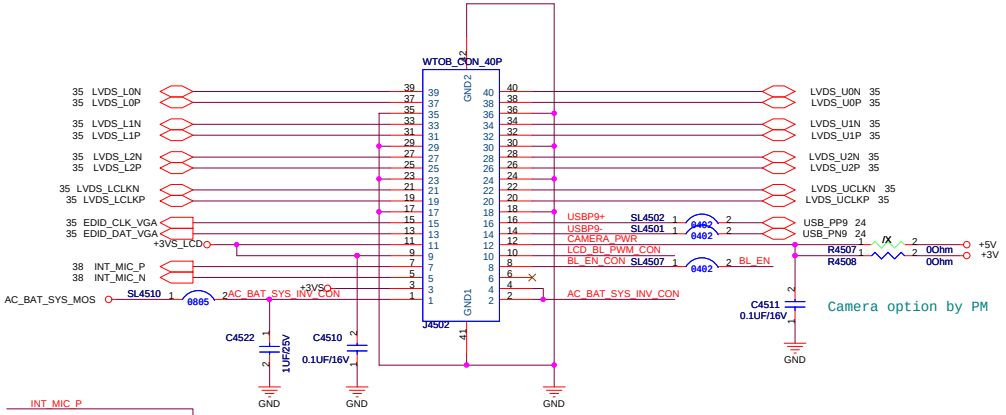
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 44 of 95	

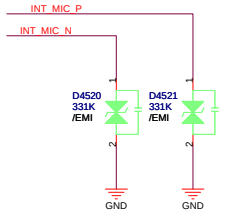




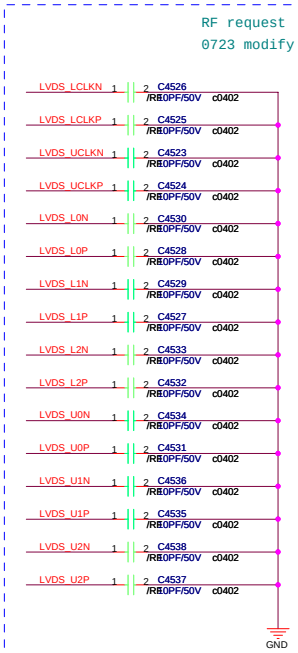








12G170010409



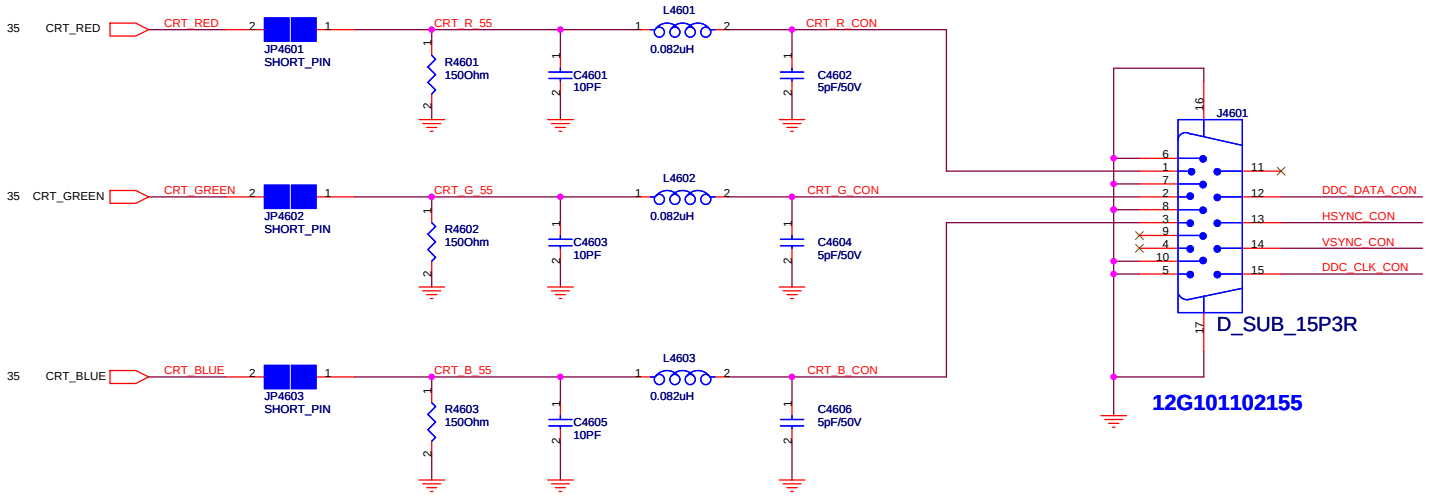
ASUSTeK COMPUTER INC. NB1

Title : LVDS

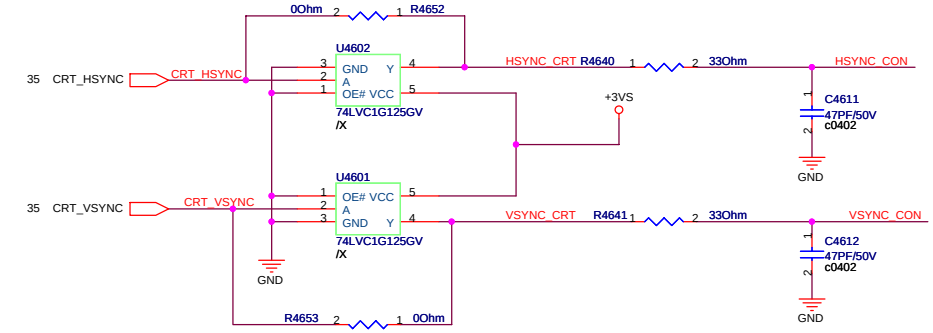
Engineer: Yun-feng_yan

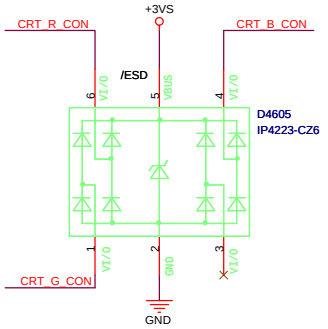
Size	Project Name	Rev
Custom	N61Jv	1.0

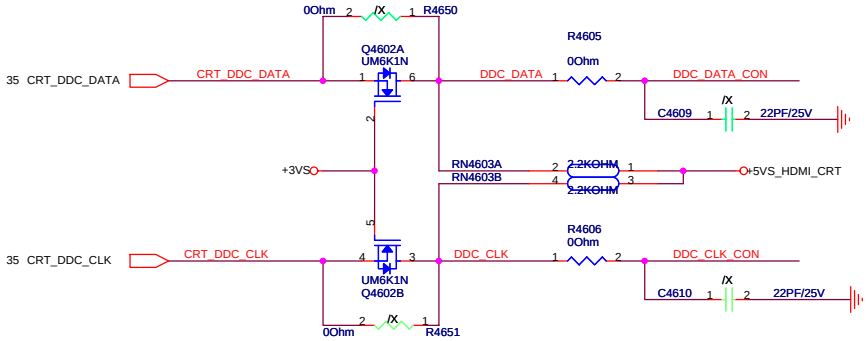
Date: Tuesday, December 15, 2009 Sheet 45 of 95

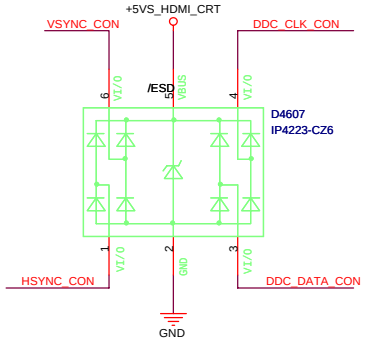


PLACE ESD Diodes near connector







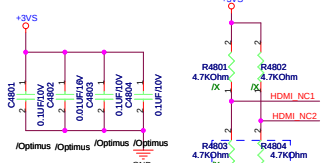


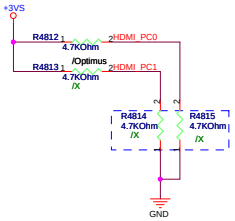
ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 46 of 95	

Main Board

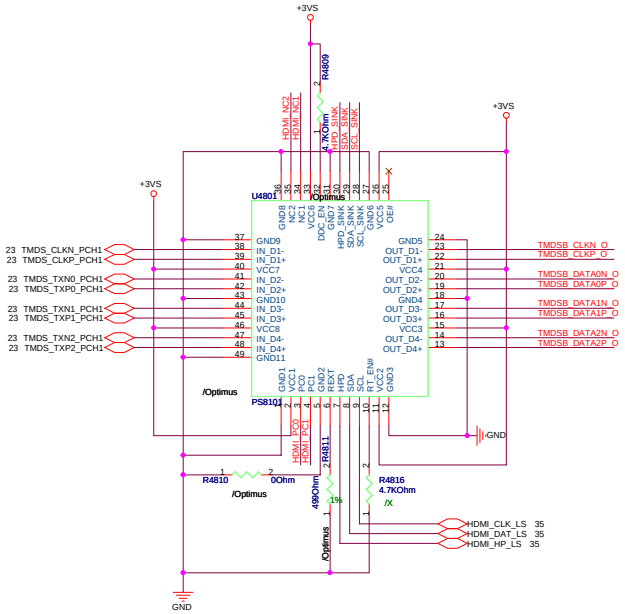
ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 47 of 95	

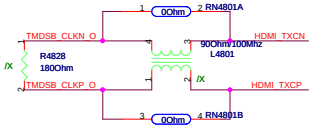
Optimus

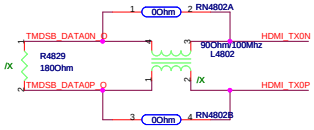


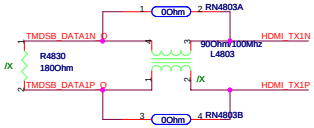


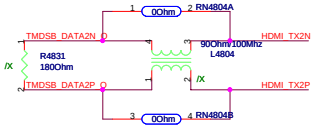
NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3
Recommended Equalization[PC1,PC0]=01, 4dB

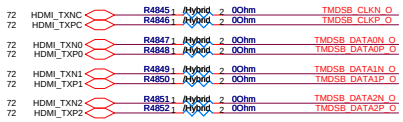


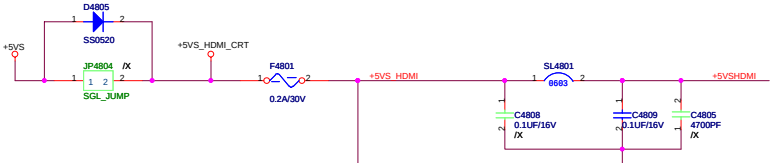




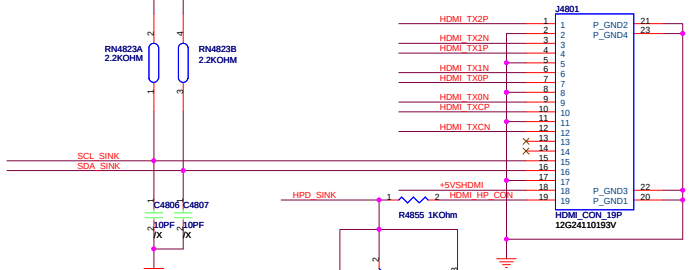






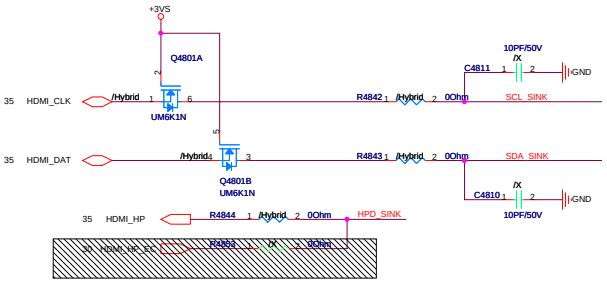


HDMI CON.



From Level Shifter
From Level Shifter

SDVO_CTRLDATA=HDMI_DDC_DATA
Strapping:
Low = No SDVO/HDMI (default)
High = SDVO/HDMI

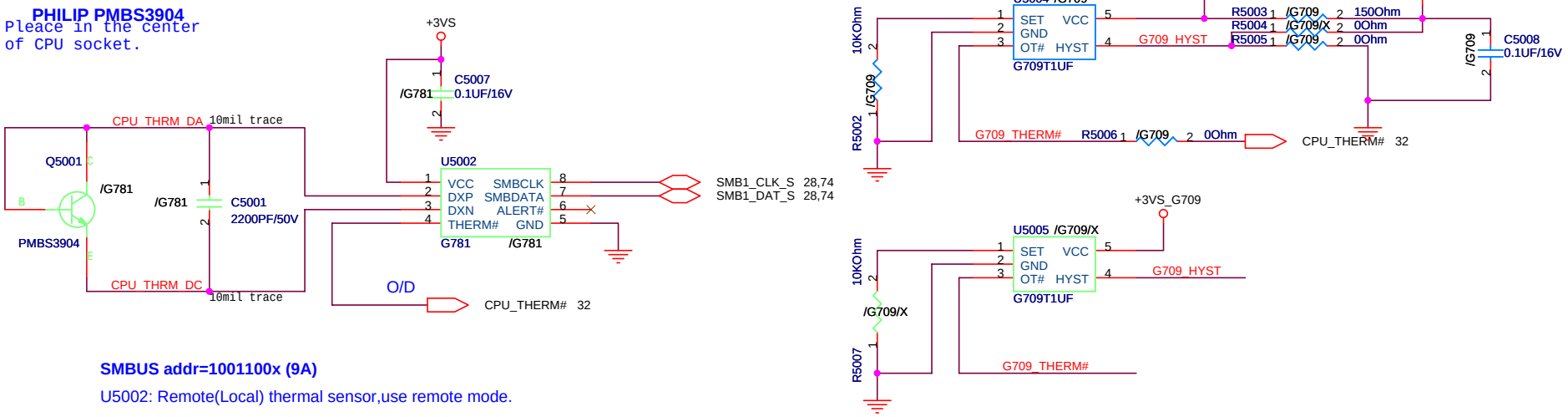


ASUSTeK COMPUTER INC	Title : HDMI		
	Engineer: Yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 48 of 95		

Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 49 of 95	

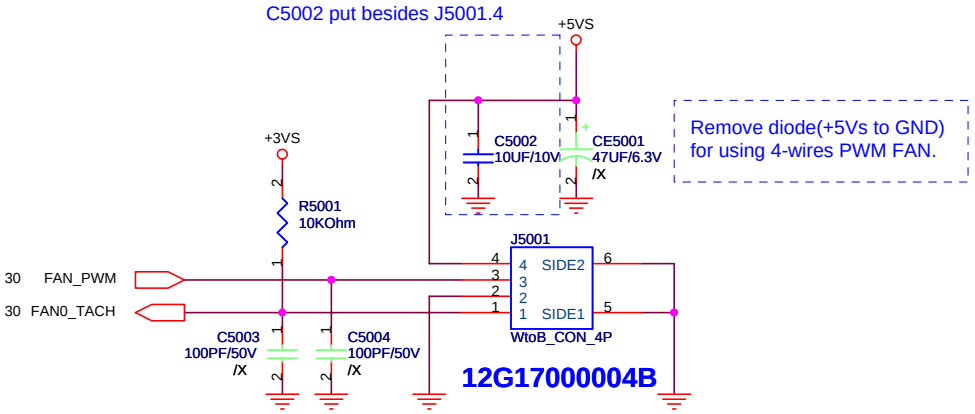
CPU Thermal Sensor



SMBUS addr=1001100x (9A)

U5002: Remote(Local) thermal sensor,use remote mode.

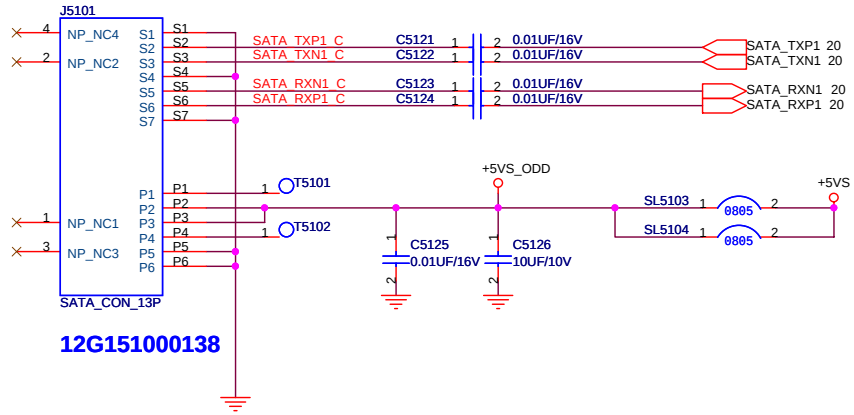
PWM Fan



ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 50 of 95	

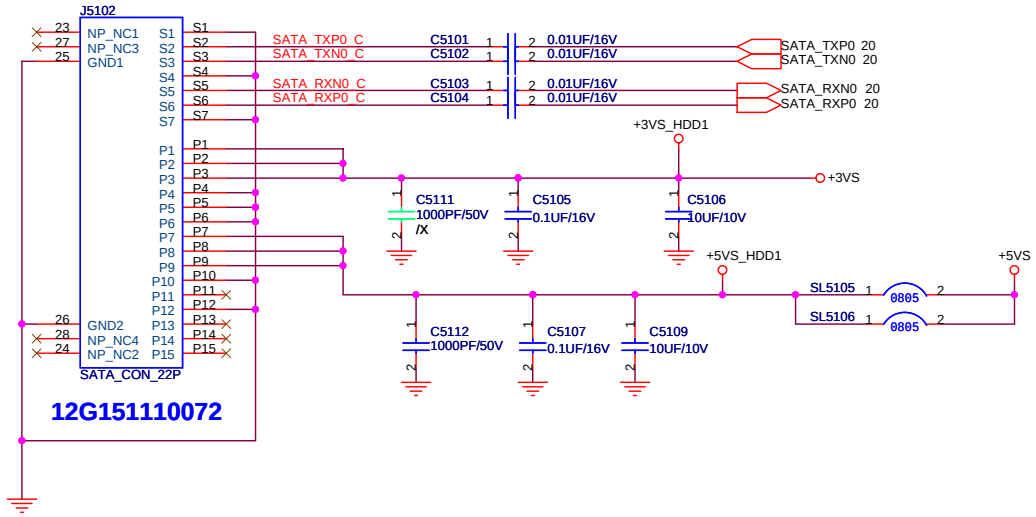
Main Board

ODD



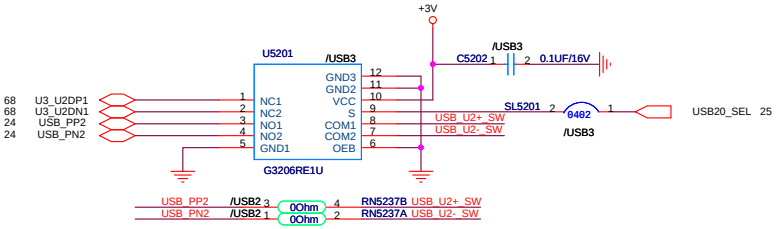
12G151000138

HDD

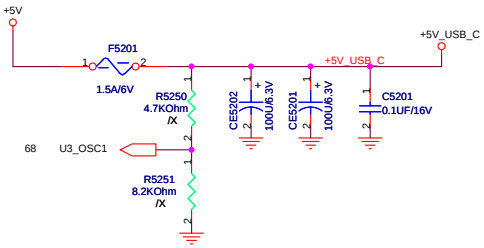


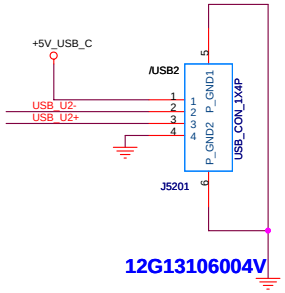
12G151110072

ASUSTeK COMPUTER INC. NB4	Title : HDD & ODD	
	Engineer: Yun-feng_yan	
Size: B	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 51 of 95	

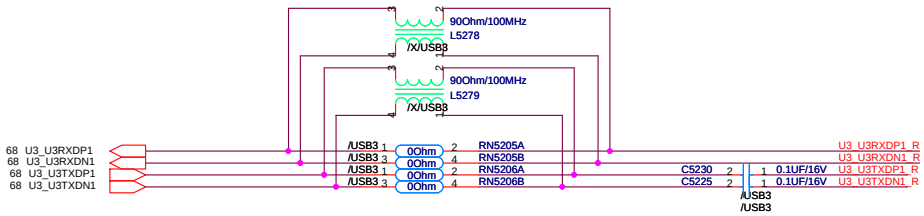


S ="L" COM=NC (USB3.0 chip)
S ="H" COM=NO (PCH)

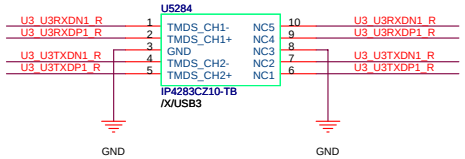


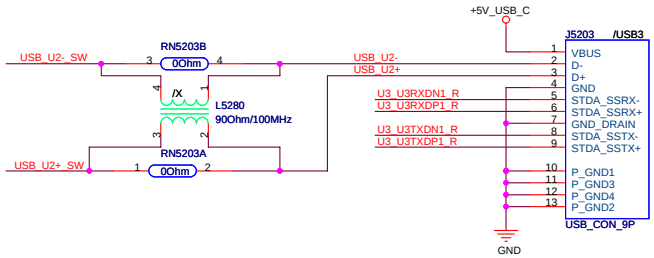


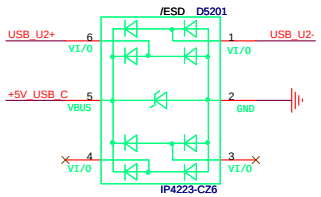
12G13106004V



USB3.0/USB 2.0 ESD-Protection



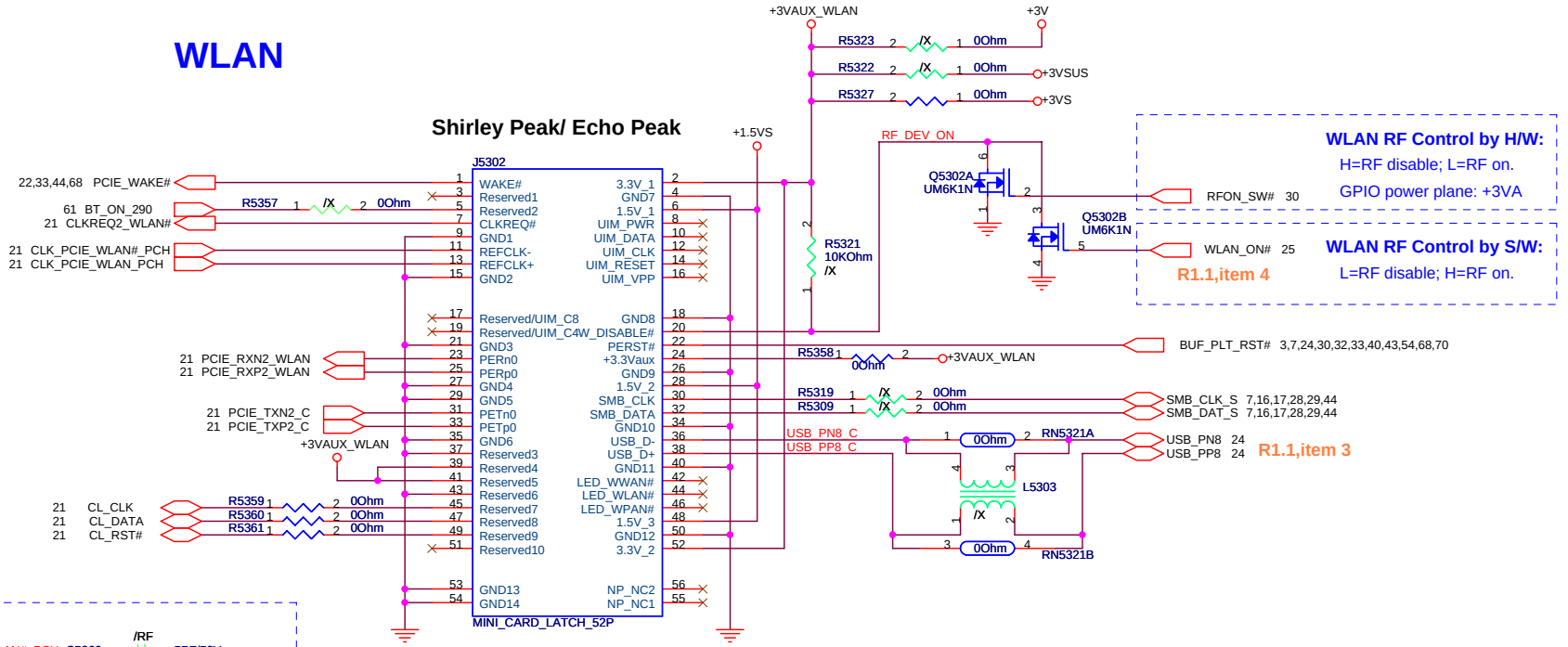




12G131010095----USB3
12G13106004V----USB2

ASUSTeK COMPUTER INC. NB4	Title : USB 3.0 Port *1	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 52 of 95	

WLAN

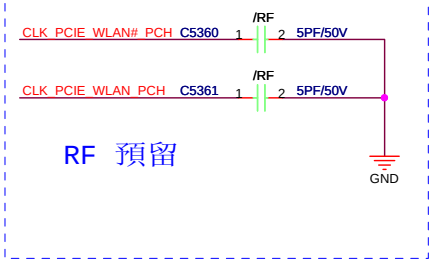


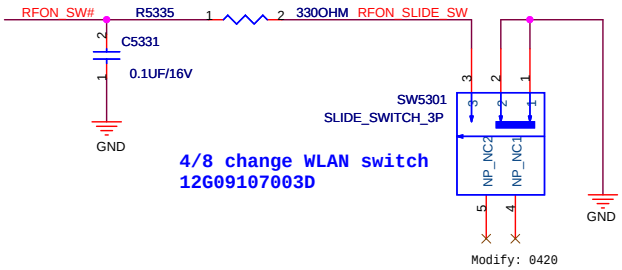
12G03000052B

footprint厂ノ 12G030000526
BOM い惠眩 12G03000052B もゃ

R1.1,item L1

RF 預留

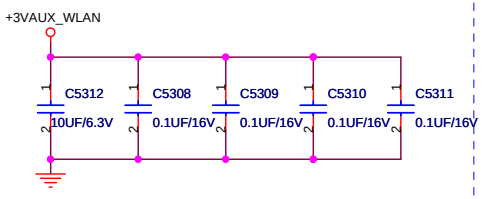




WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

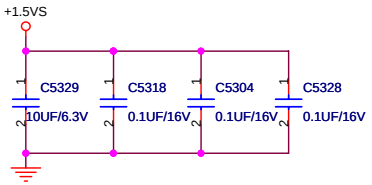
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

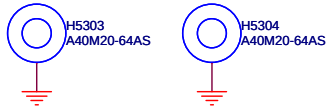


WLAN NUT for :

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.



13G021029050

ASUSTeK COMPUTER INC. NB6

Title : MINICARD(WLAN)

Engineer: Yun-feng_yan

Size	Project Name	Rev
Custom	N61Jv	1.0

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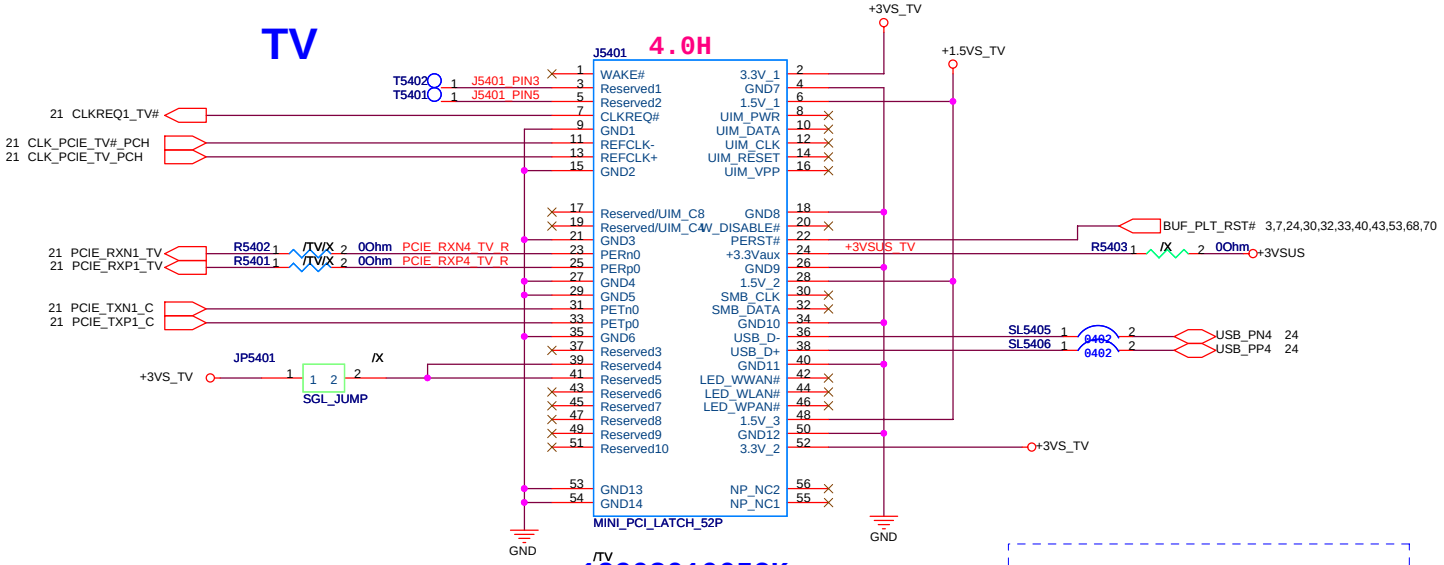
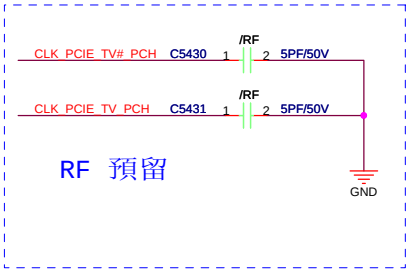
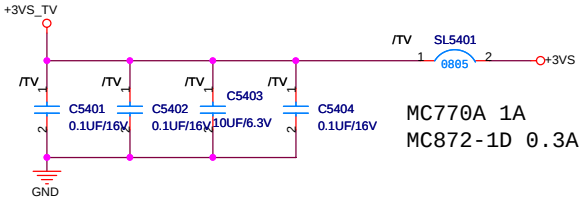
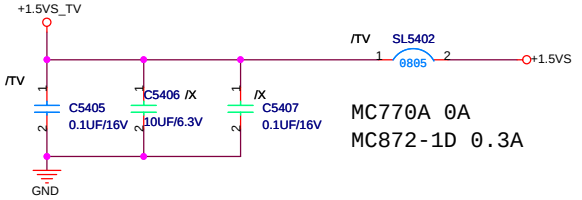
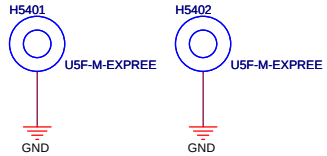








Module Name	Interface	Function
MC770A	USB	ATV+ DVB-T
MC872-1D	USB	DVB-T only



Parts Difference with Design IP

N52	Design IP
R5438	none
R5439	none
R5440	none
R5441	none
SL5403	none
SL5404	none
R5442	none
R5443	none
none	J5304
none	H5303
none	H5304

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Net Difference with Design IP

N52	Design IP
PCIE_RXN4_TV	PCIE_RXN5_TV
PCIE_RXP4_TV	PCIE_RXP5_TV
PCIE_TXN4_C	PCIE_TXN5_TV
PCIE_TXP4_C	PCIE_TXP5_TV
TV_ON_C	none
USB_PN6	USB_PN6_TV
USB_PP6	USB_PP6_TV

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ASUSTeK COMPUTER INC. NB1

Title : TV TUN / 3G

Engineer: Yun-feng_yan

Size	Project Name	Rev
Custom	N61Jv	1.0

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ASUSTeK COMPUTER INC. NB4	Title : SIO_****
	Engineer: Yun-feng_yan
Size: A	Project Name: N61Jv
	Rev: 1.0
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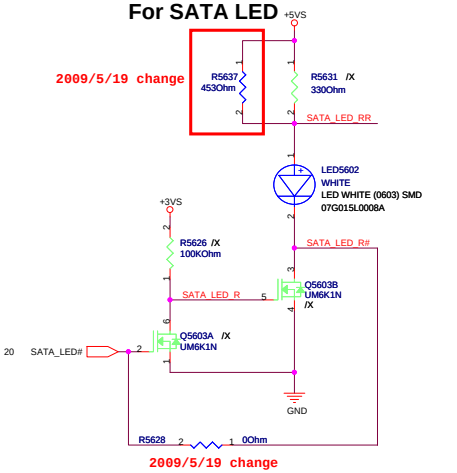
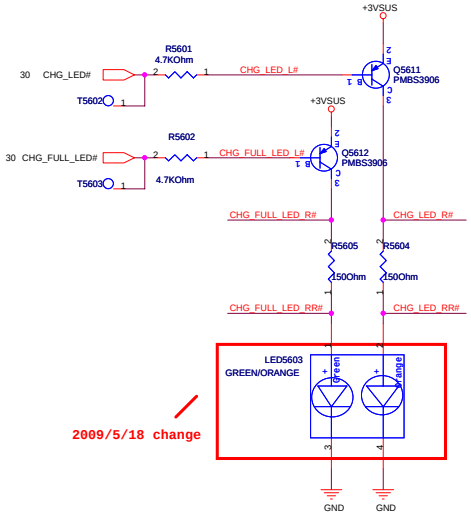
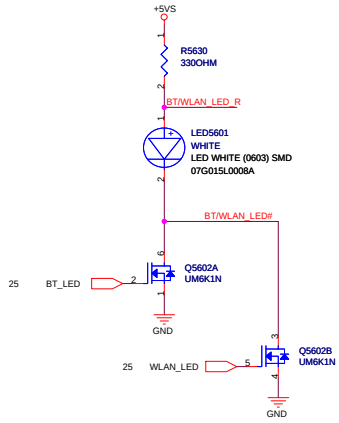
For SATA LED



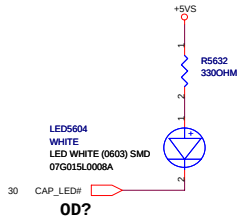
For Battery LED



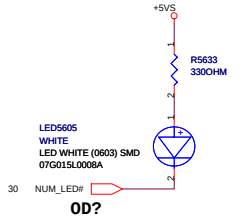
For BT/WLAN LED



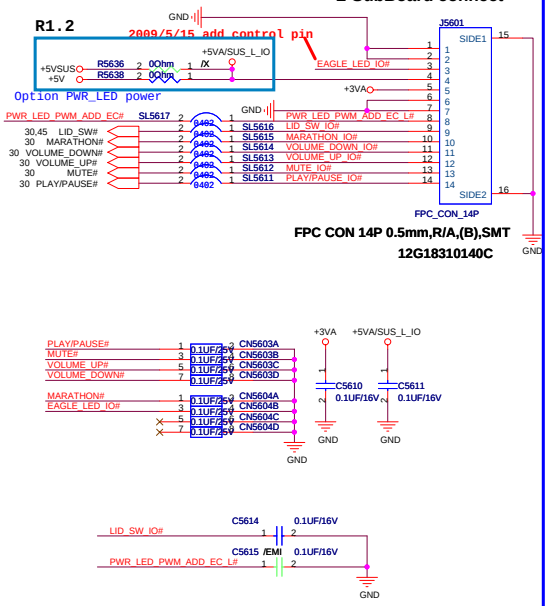
For Caps. Lock



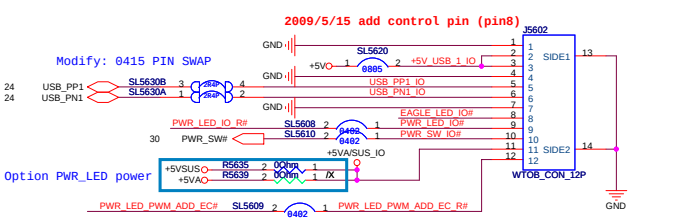
For NUM. Lock

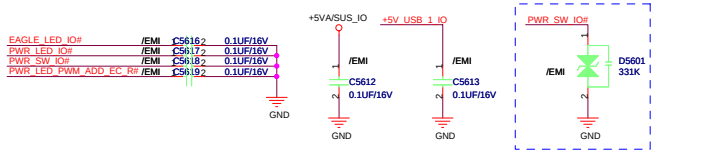


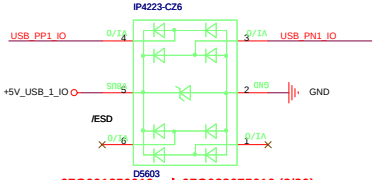
L-SubBoard connect



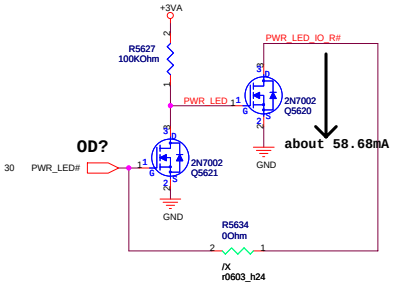
R-SubBoard connect

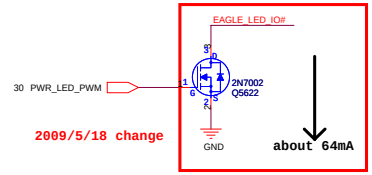


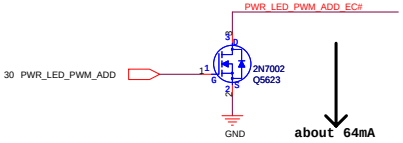




For PWR LED



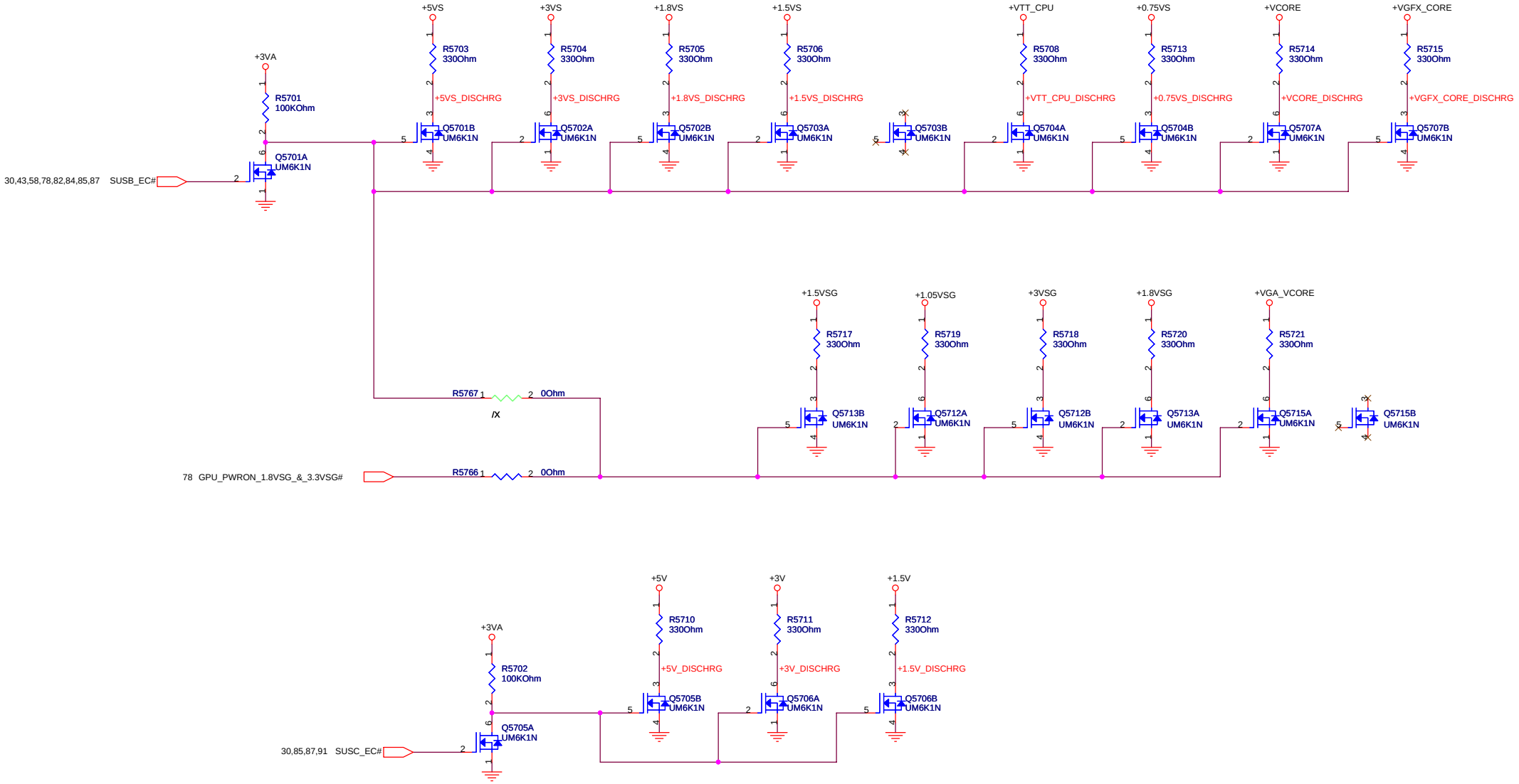




ASUSTeK COMPUTER INC. NB1	Title : LED & SW	
	Engineer: Yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 56 of 95	

Main Board

Remove +2.5Vs is for ATI GFX



ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
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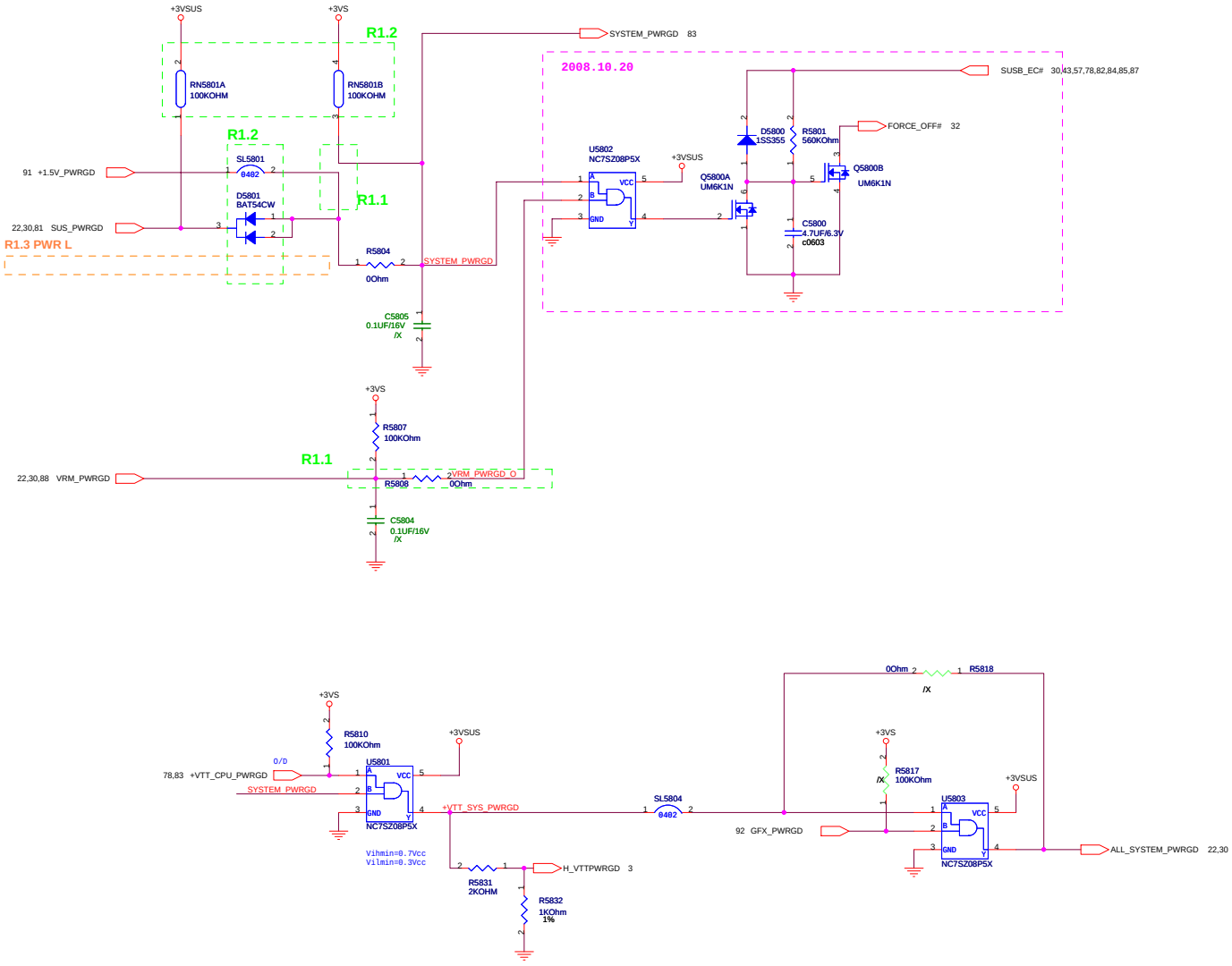
POWER GOOD DETECTER



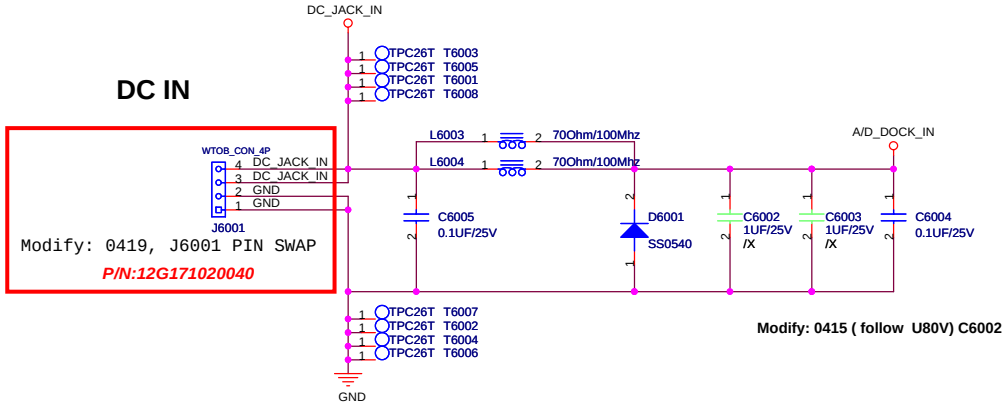
2008-08-04,James Wu add.

ASUSTeK COMPUTER INC. NB3	Title : POWER_PROTECT	
	Engineer: Yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 58 of 95	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : DJ ****	
	Engineer: CH_Lin	
Size: C	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 59 of 95	

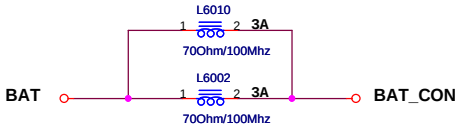
DC IN



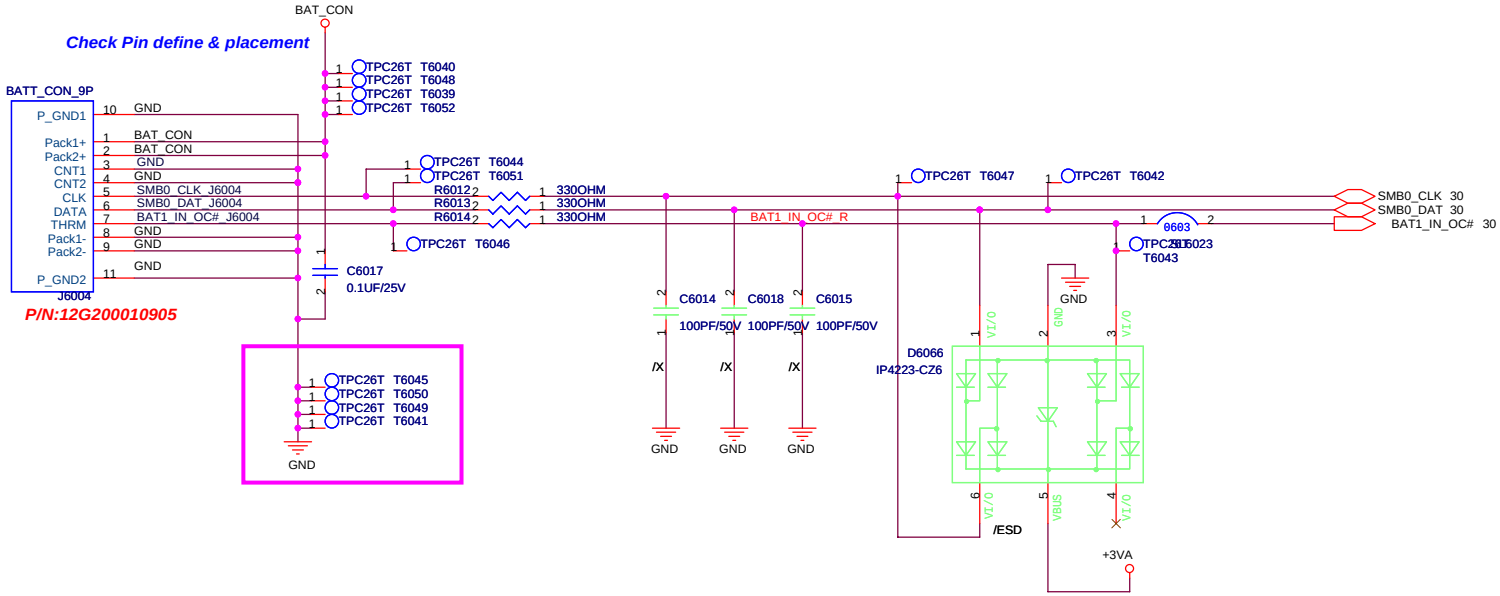
Modify: 0419, J6001 PIN SWAP

P/N:12G171020040

Modify: 0415 (follow U80V) C6002



BAT IN



P/N:12G200010905

07G001250010 э丿 07G028075010 (3/30)

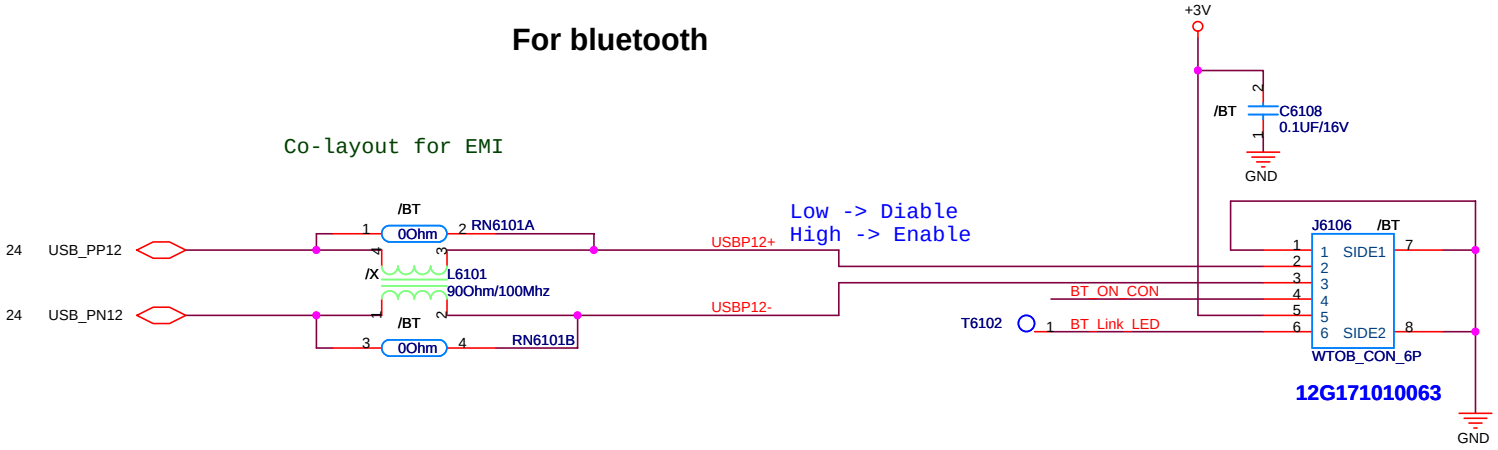
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 60 of 95	

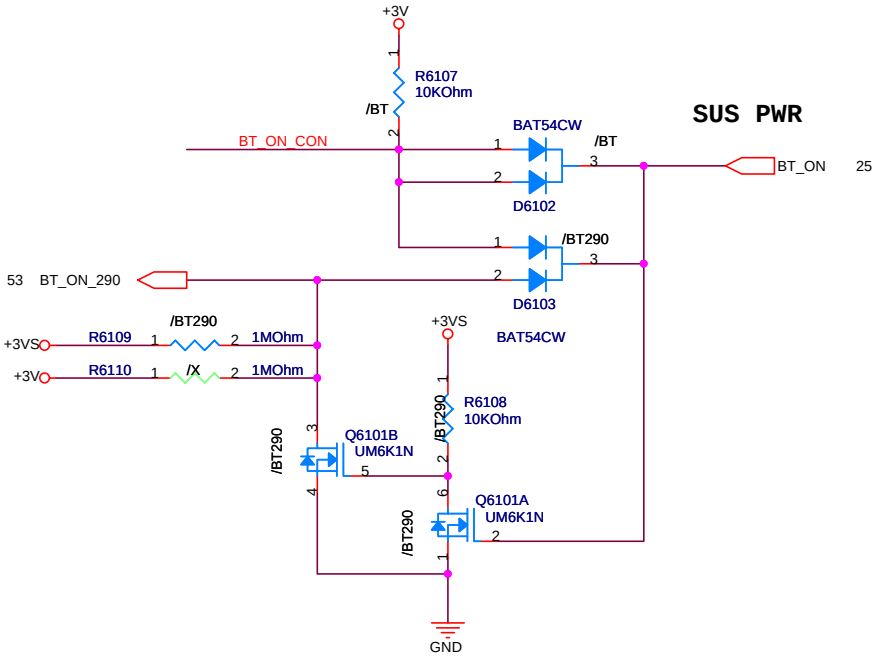
Bluetooth Conn.

For bluetooth

Co-layout for EMI

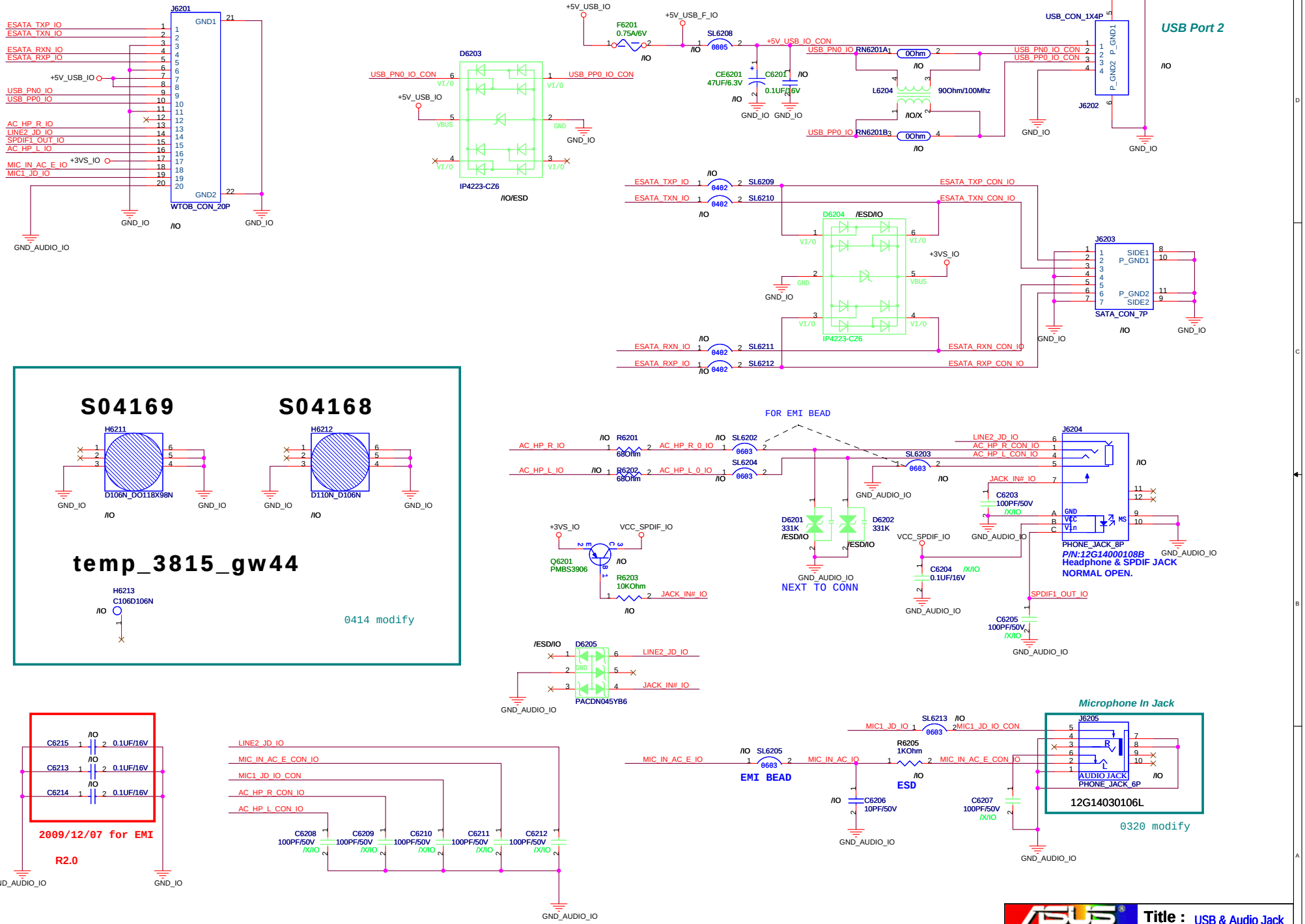


SUS PWR



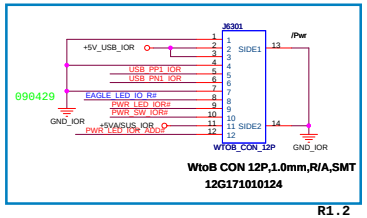
ASUSTeK COMPUTER INC. NB1	Title : BT	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 61 of 95	

I/O Board



ASUSTeK COMPUTER INC. NB1	Title : USB & Audio Jack	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 62 of 95	

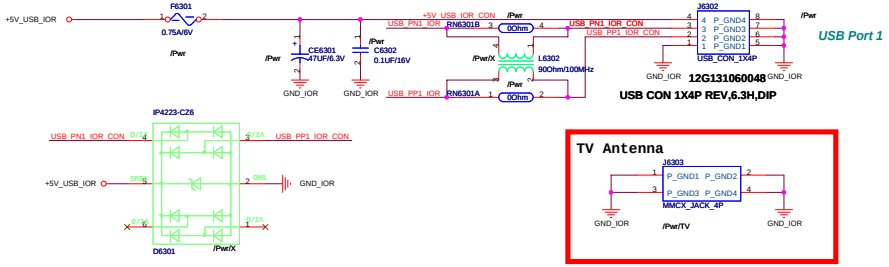
POWER BOARD



WtoB CON 12P,1.0mm,R/A,SMT

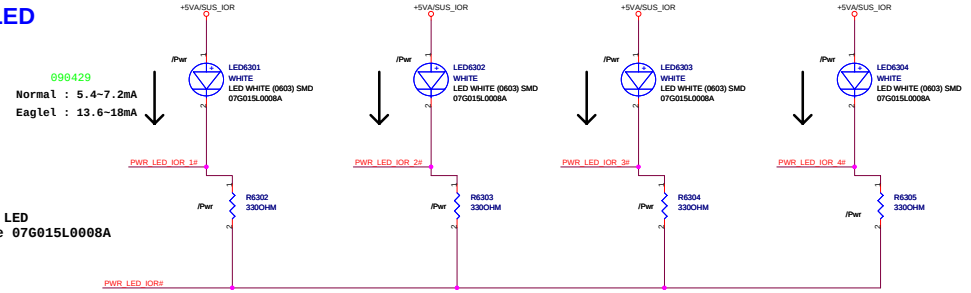
12G171010124

R1.2



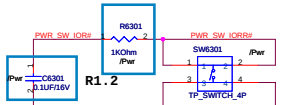
0518 change to P/N:14G152231000

Power LED



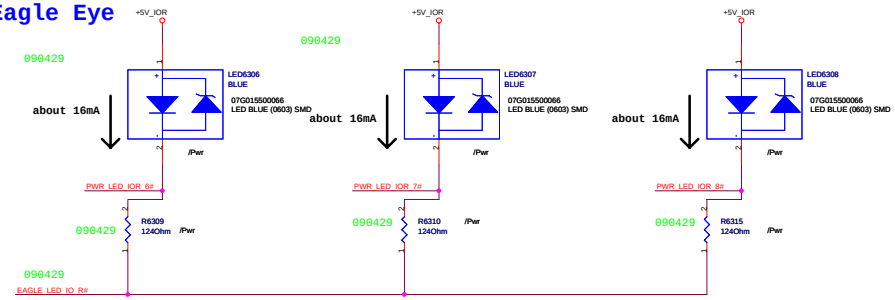
R2.1
ALL POWER LED
P/N change 07G015L0008A

POWER SW

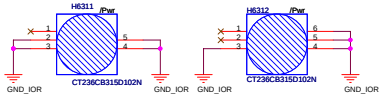


12G09103004P
T.P SWITCH 4P SMT

Eagle Eye



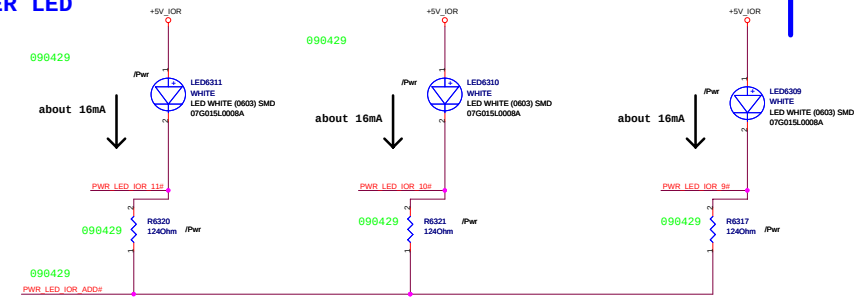
A: S04172 B: S04173

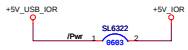


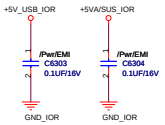
temp_5824_fh05

R1.2

ADD POWER LED



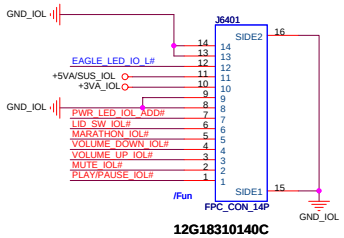




ASUSTeK COMPUTER INC. NB1		Title : POWER BOARD	
		Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009		Sheet 63 of 95	

FUNCTION BOARD

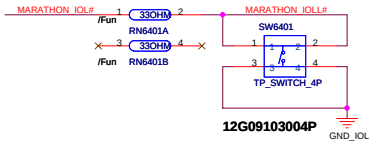
2009/5/18 swap



12G18310140C

FPC CON 14P 0.5mm,R/A,(B),SMT

MARATHON switch

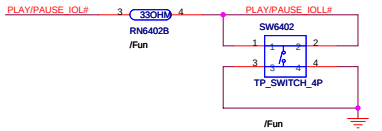


12G09103004P

T.P SWITCH 4P SMT

/Fun

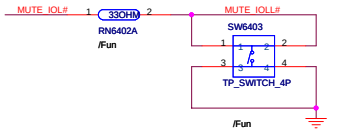
PLAY/PAUSE switch



12G09103004P

T.P SWITCH 4P SMT

MUTE switch



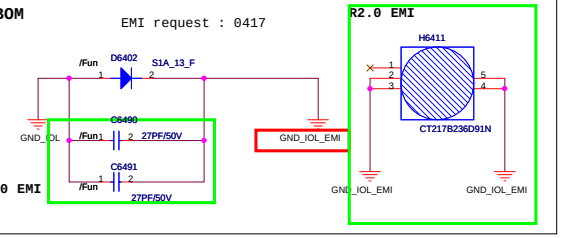
12G09103004P

T.P SWITCH 4P SMT

R1.2

R1.1 BOM

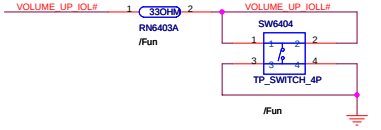
EMI request : 0417



R2.0 EMI

2009/5/18 change for factory

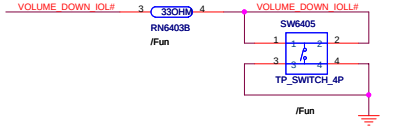
VOLUME UP switch



12G09103004P

T.P SWITCH 4P SMT

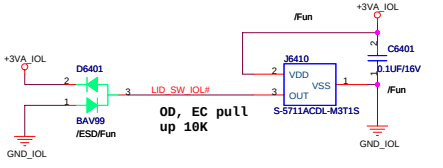
VOLUME DOWN switch

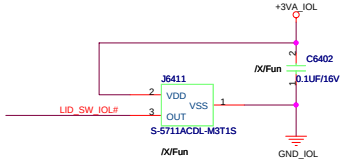


12G09103004P

T.P SWITCH 4P SMT

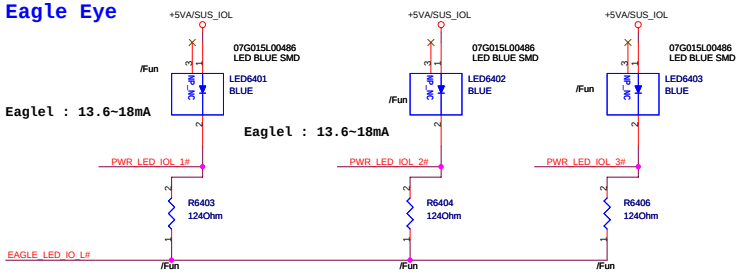
Lid Switch



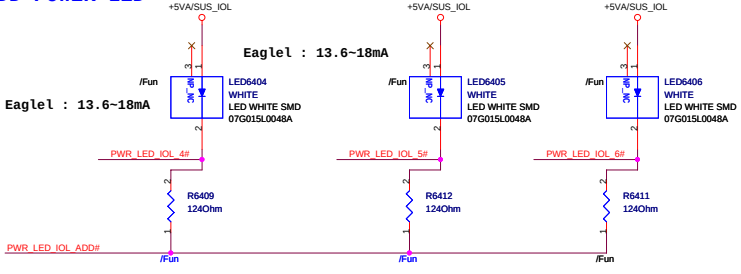


R2.1 LED chang 07G015L0048A

Eagle Eye

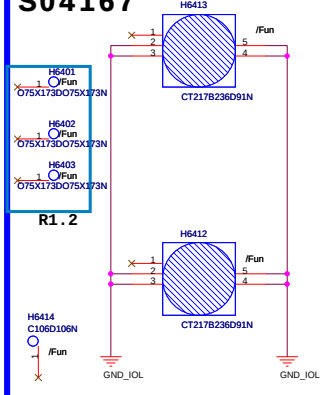


ADD POWER LED



S04167

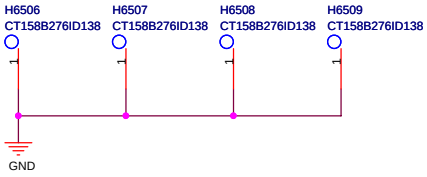
2009/5/18 for ME



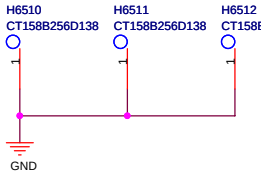
R1.2

ASUSTeK COMPUTER INC. NB1	Title : FUNCTION BOARD	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 64 of 95	

CPU (F : S04153)



GPU (G : S04170)

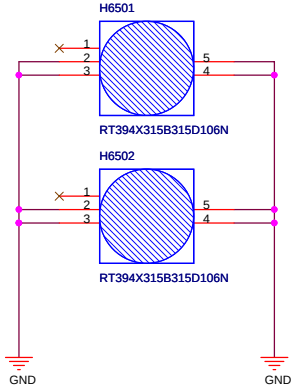


Modify: 0414

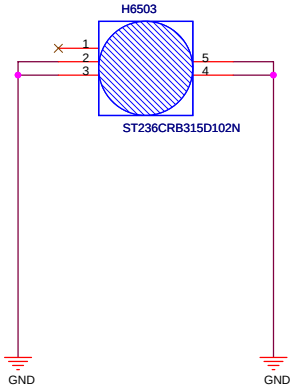
HOLD

Modify: 0415

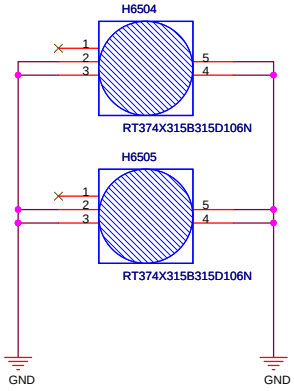
A: S04148



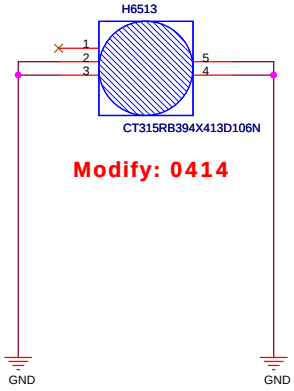
C: S04150



E: S04152

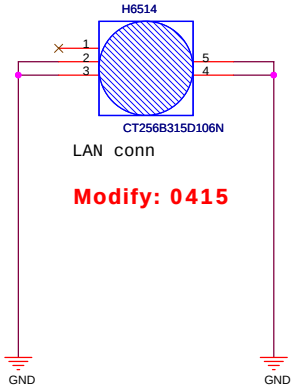


H: S04171



Modify: 0414

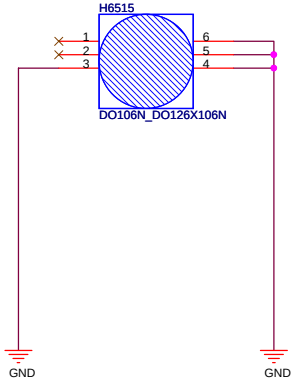
K: S04157



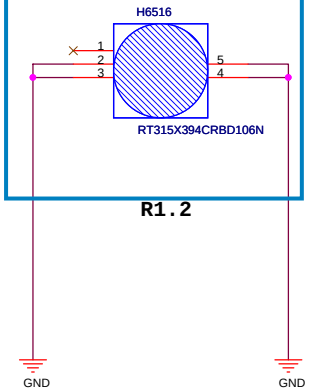
LAN conn

Modify: 0415

L: S04158

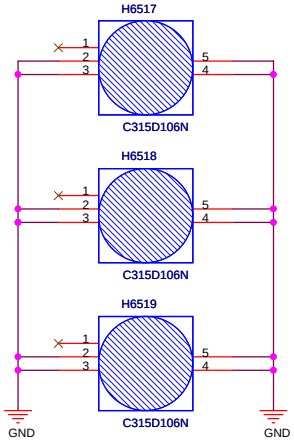


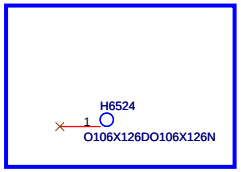
M: S04159



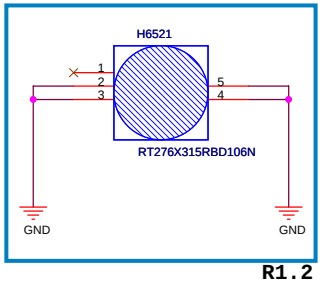
R1.2

N: S04160



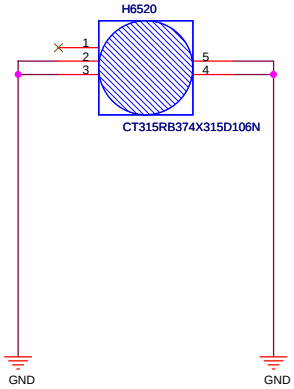


090505 Ellipse



R1.2

O: S04161



ASUSTeK COMPUTER INC. NB1	Title : NUT	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Sunday, November 15, 2009	Sheet 65 of 95	

Title :	ESA_ESATA
ASUSTeK COMPUTER INC. NB4	Engineer: Yun-feng_yan
Size: A	Project Name: N61Jv
Rev: 1.0	
Date: Wednesday, November 11, 2009	Sheet 66 of 95

Title :	PCH_XDP, ONFI
ASUSTeK COMPUTER INC. NB4	Engineer: *Yun-feng_yan*
Size: A	Project Name: **N61Jv**
Rev: 1.0	
Date: Wednesday, November 11, 2009	Sheet 67 of 95

PCI Express Interface
trace最大線長為12.5cm(6 inches).

U6801A

PCI Express Interface

+3.3V Power Supply

USB Interface

+1.0V Power Supply

SPI Interface

System Clock

System Interface Signal

Analog Power

Analog Signal

UPD720200F1-DAK-A

(1)USB3.0 Interface trace最大線長為10cm(4 inches).
(2)USB Interface differential trace torlerence = 0.12mm(5 mail).

Power on Reset.

從南橋找一根可以發SMI的GPI pin, PWR Plate is Main PWR.

可以接受外部輸入48MHz Clock.
若要拉板子上的Clock,
請參考USB3.0 datasheet.

Close to USB IC

Close to P12

P12腳N12 Layout,
叫叭ㄆ把○NEC Layout guide_Page31.

0.3B Beta

Standard Circuit	
USB3.0	uPD720200
REV.	U3_03B BETA

UPD720200
/X/UPD720200

U6802B

UP7706U8

U6802A

UP7706U8

U6801B

UPD720200F1-DAK-A

Title : USB 3.0_NEC

ASUSTeK COMPUTER INC. NB4

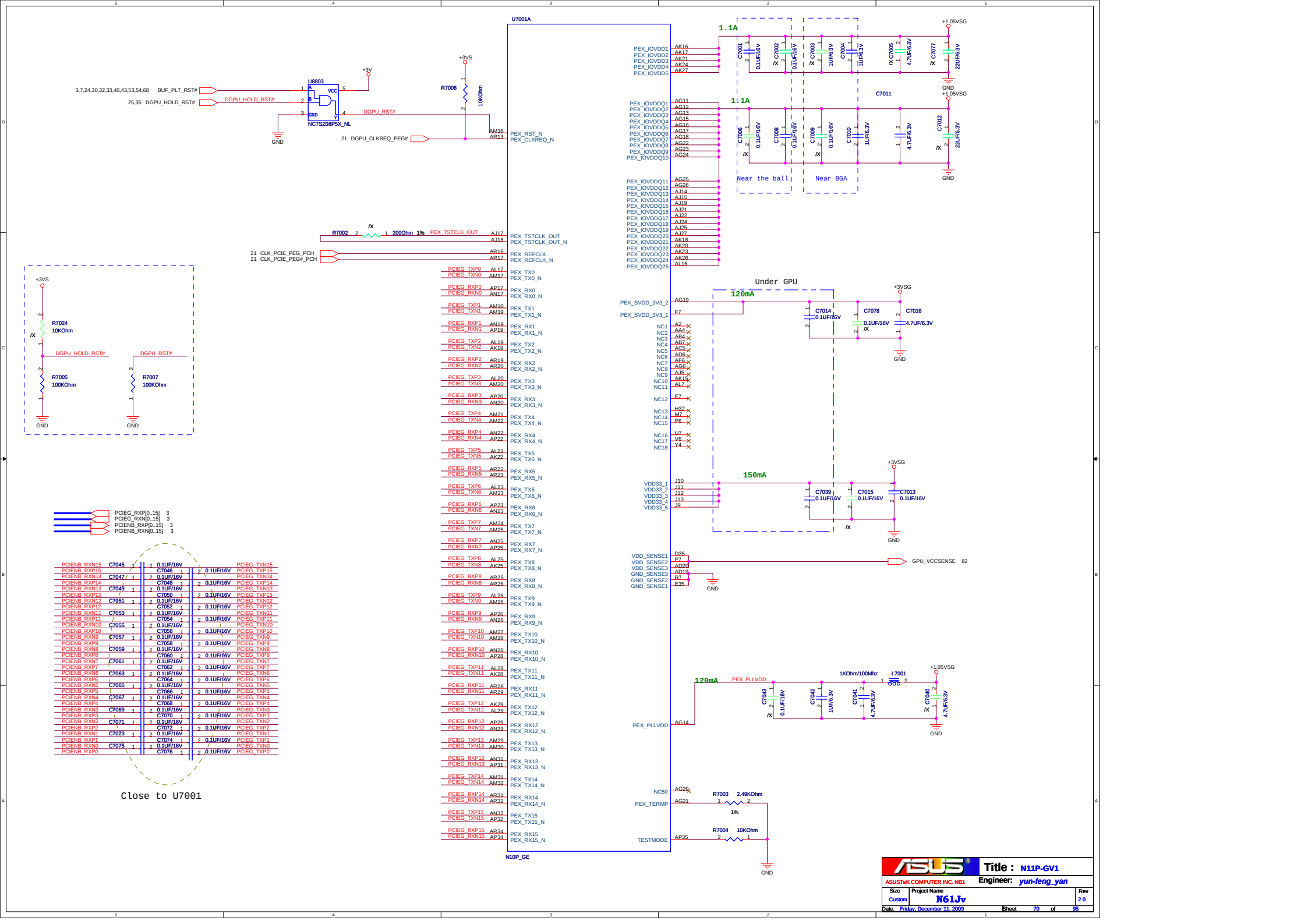
Engineer: Yun-feng_yan

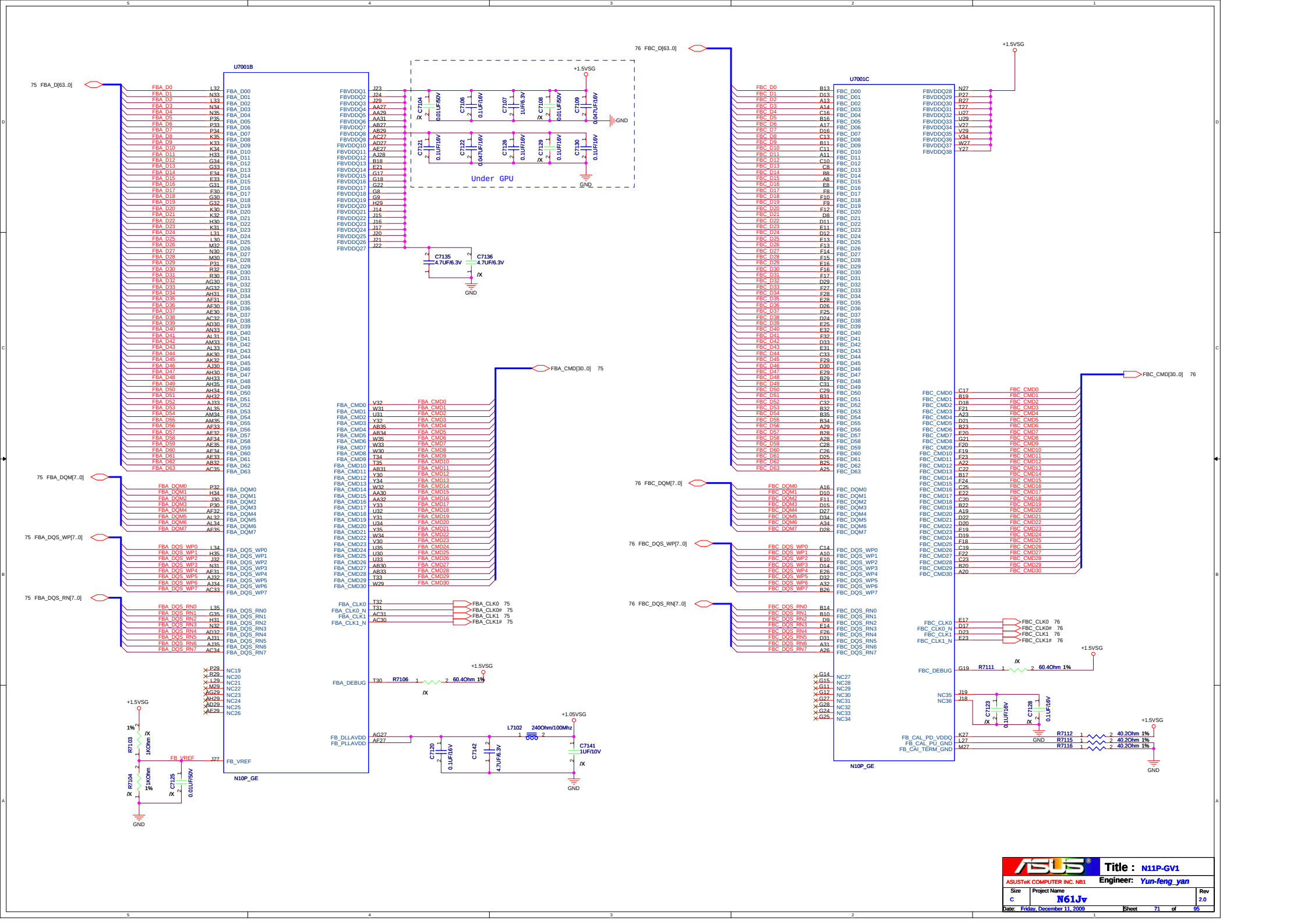
Size	Project Name	Rev
Custom	N61Jv	1.0

Date: Friday, December 11, 2009 Sheet 68 of 95

0.3B Beta

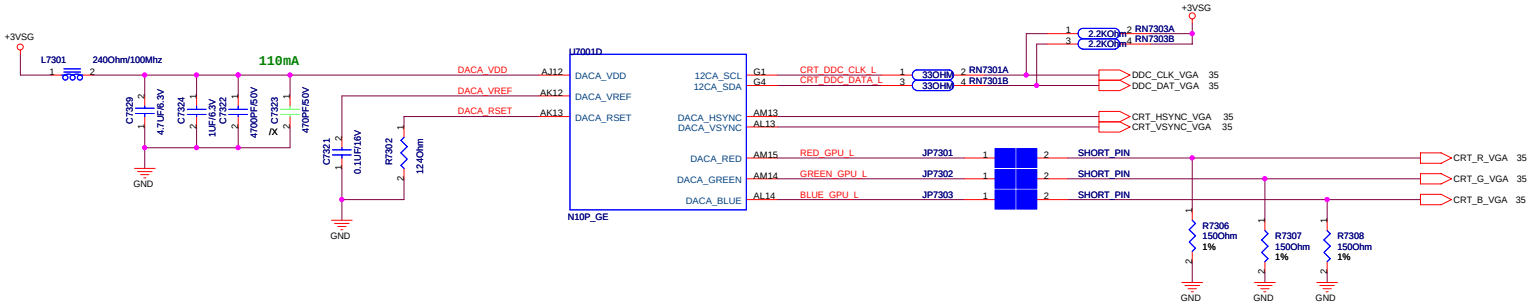
ASUSTeK COMPUTER INC. NB4	Title : USB 3.0_NEC (2)	
	Engineer: yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 69 of 95	


U7001A
U8803
NC7SZ08P5X_NL
R7006
10KOhm
+3VS
+3V
GND
BUF_PLT_RST#
DGPU_HOLD_RST#
DGPU_RST#
DGPU_CLKREQ_PEG#
PEX_RST_N
PEX_CLKREQ_N
R7002
200Ohm 1%
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
CLK_PCIE_PEG_PCH
CLK_PCIE_PEG#_PCH
PEX_REFCLK
PEX_REFCLK_N
R7024
10KOhm
R7005
100KOhm
R7007
100KOhm
PCIEG_RXP[0..15] 3
PCIEG_RXN[0..15] 3
PCIENB_RXP[0..15] 3
PCIENB_RXN[0..15] 3
Close to U7001
1.1A
C7001
C7002
C7003
C7004
C7005
C7077
C7011
C7006
C7008
C7009
C7010
C7012
Near the ball
Near BGA
Under GPU
120mA
C7014
C7078
C7016
150mA
C7039
C7015
C7013
VDD_SENSE1
VDD_SENSE2
VDD_SENSE3
GND_SENSE3
GND_SENSE2
GND_SENSE1
GPU_VCCSENSE 82
PEX_PLLVDD
1KOhm/100Mhz
L7001
C7043
C7042
C7041
C7040
NC50
PEX_TERMP
TESTMODE
R7003 2.49KOhm 1%
R7004 10KOhm
N10P_GE

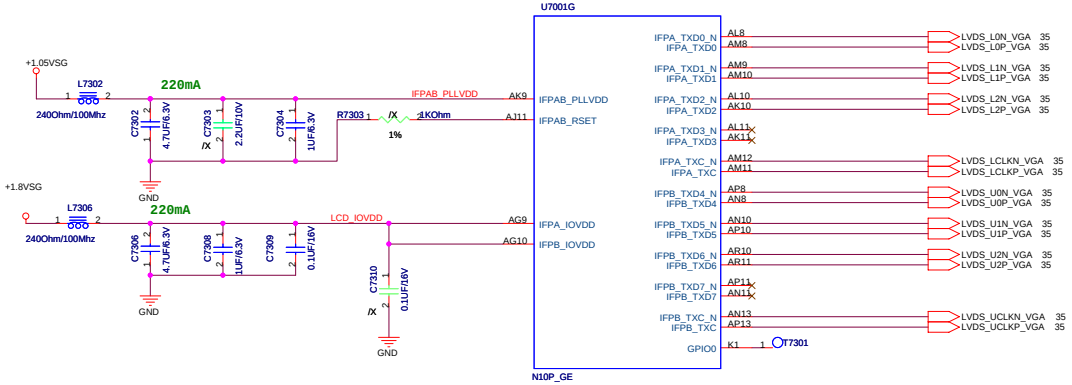


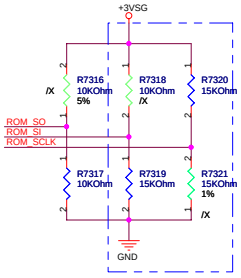
ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1		
	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 71 of 95		

VGA



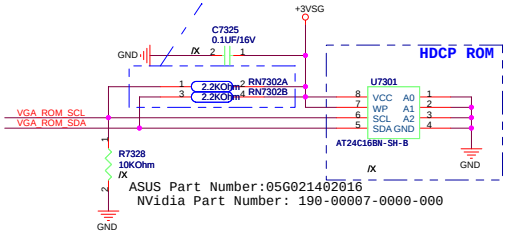
LVDS

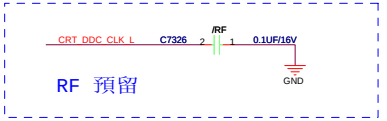




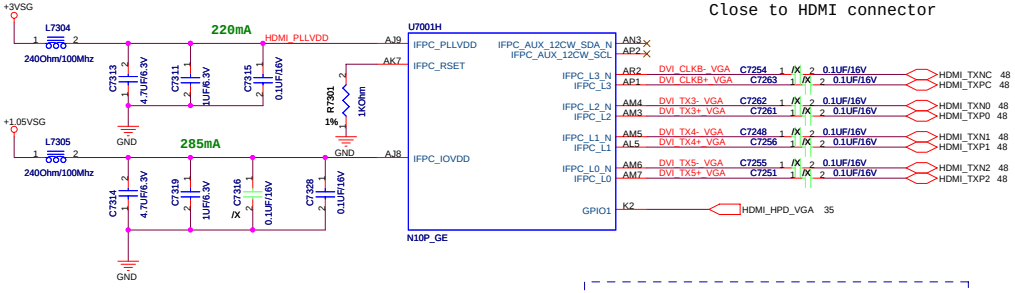
RAM_CFG[3:0]	Definitions	ROM_SI
0010	Hynix 64Mx16 DDR3	R7319 15kohm down
0011	Samsung 64Mx16 DDR3	R7319 20kohm down

nVidia DG-04131-001_V01_secured.pdf
section 9.3

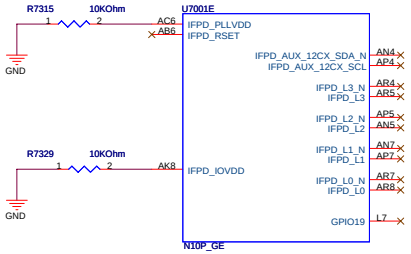


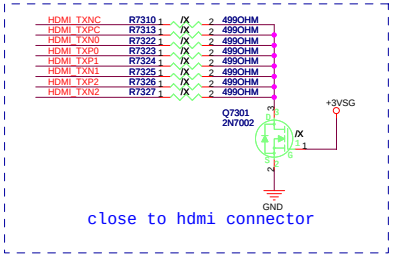


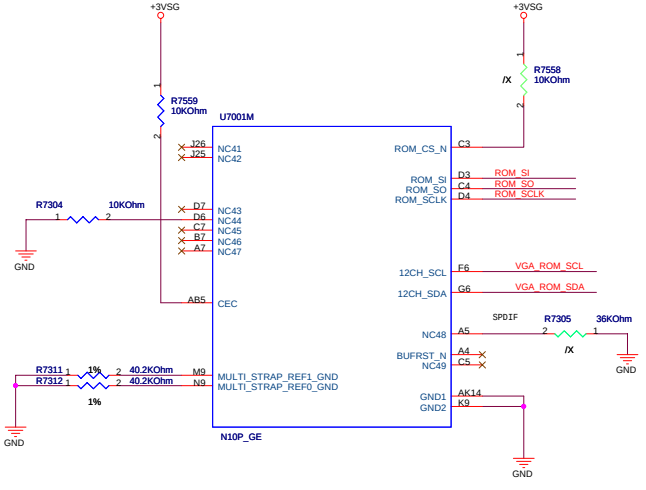
HDMI



Close to HDMI connector







ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1		
	Engineer: Yun-feng_yan		
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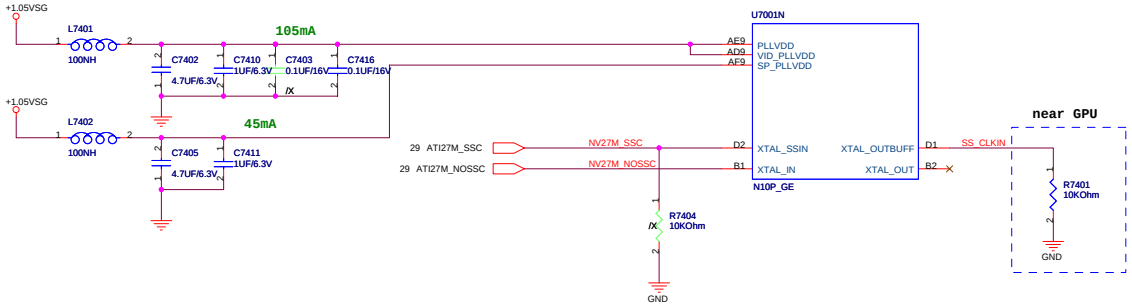
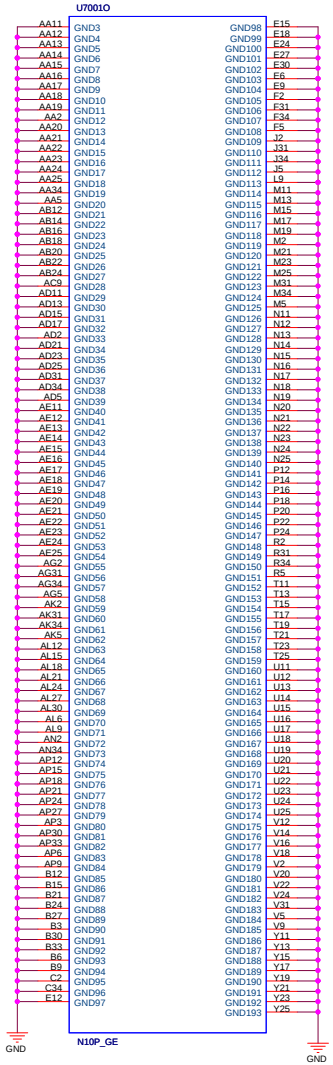
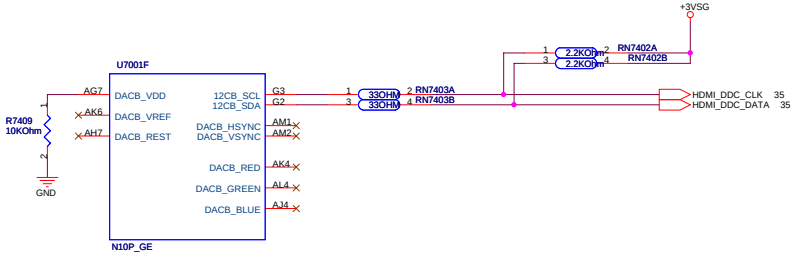
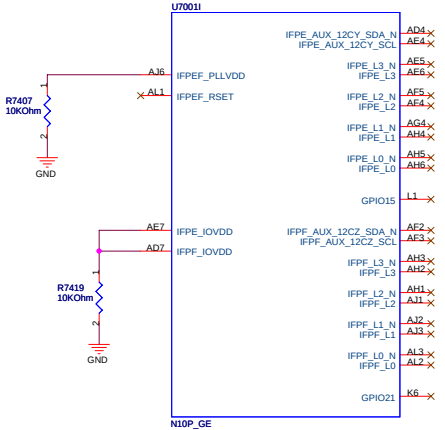
Xtal

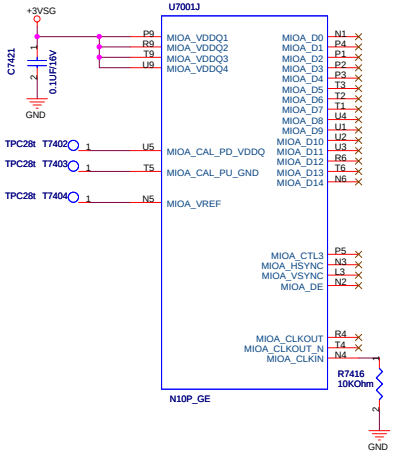


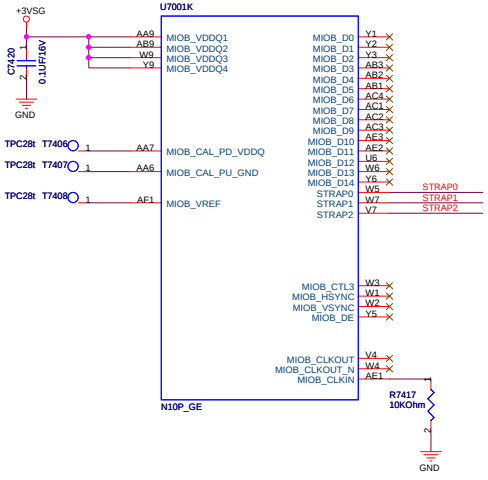


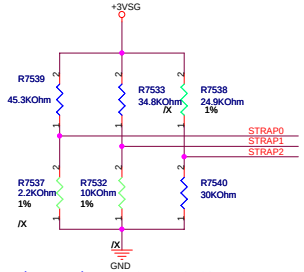
Other











Device ID is 0x0A35, set Strap2 R7540 PD 30K

ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1	
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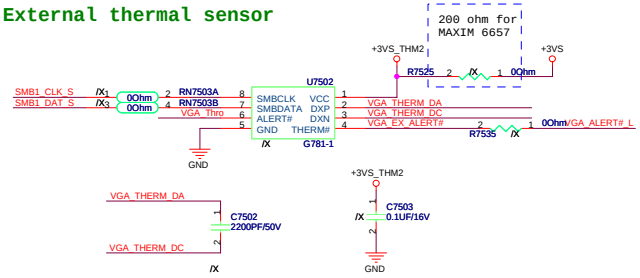
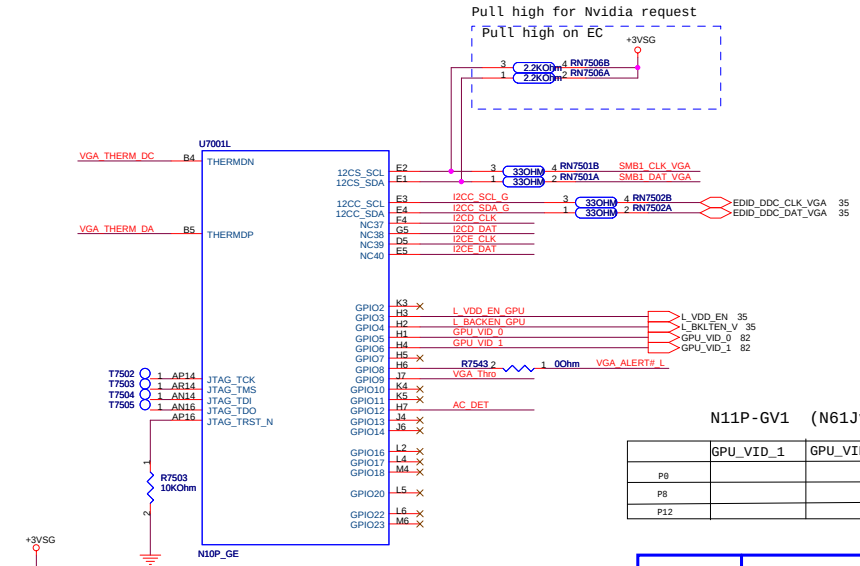
GPIO

External thermal sensor



GPIO ASSIGNMENTS

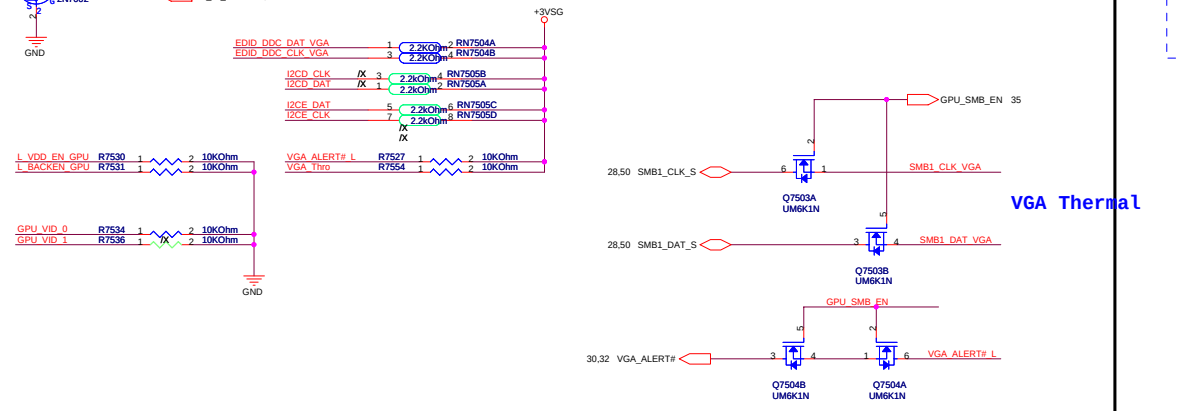
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL



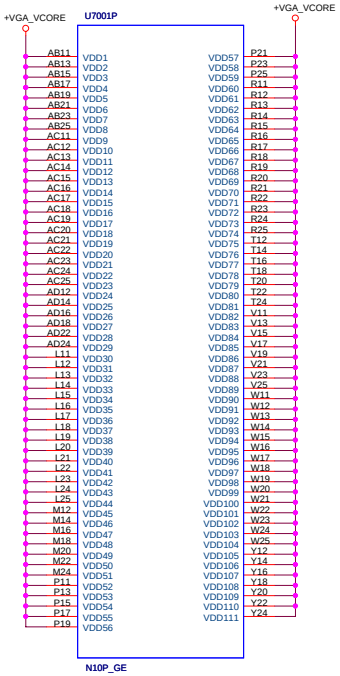
N11P-GV1 (N61Jv)

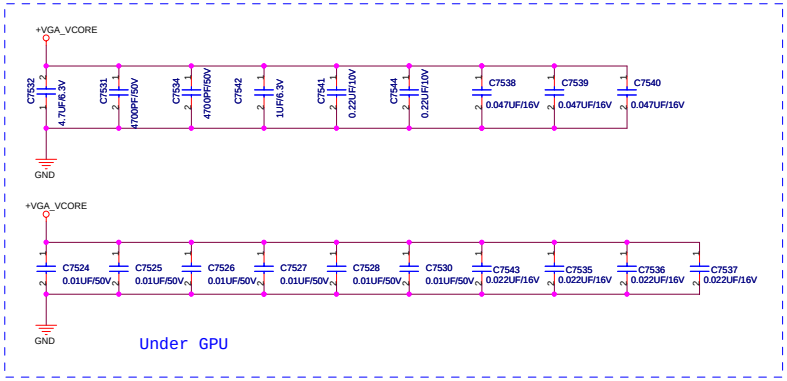
	GPU_VID_1	GPU_VID_0	+VGA_VCORE_0
P0			0.85V
P8			0.85V
P12			0.85V

GPIO5	GPIO6	VGA_VCORE	
0	0	0.8	-10%
0	1	0.85	-5%
1	0	0.9	Normal
1	1	0.95	+5%



VGA Thermal





ASUS	Title : N11P-GV1		
ASUSTeK COMPUTER INC. NB1	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 2.0
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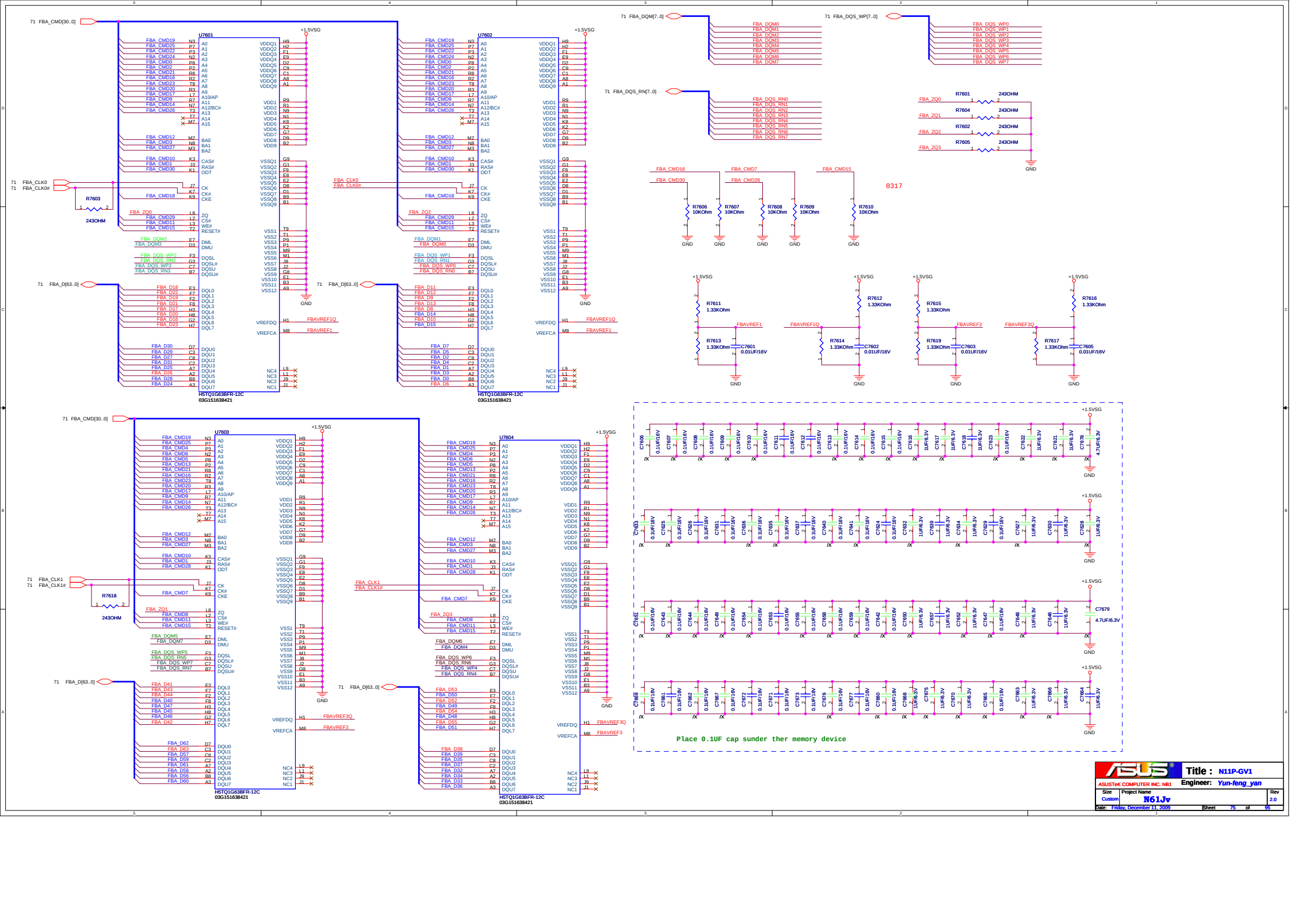
71 FBA_CMD[30..0]
U7601
U7602
U7603
U7604
+1.5VSG
GND
R7603 243OHM
R7618 243OHM
71 FBA_CLK0
71 FBA_CLK0#
71 FBA_CLK1
71 FBA_CLK1#
FBA_ZQ0
FBA_ZQ1
FBA_ZQ2
FBA_ZQ3
71 FBA_D[63..0]
H5TQ1G63BFR-12C
03G151638421
71 FBA_DQM[7..0]
71 FBA_DQS_WP[7..0]
71 FBA_DQS_RN[7..0]
R7601 243OHM
R7604 243OHM
R7602 243OHM
R7605 243OHM
FBA_CMD18
FBA_CMD30
FBA_CMD7
FBA_CMD28
FBA_CMD15
0317
R7606 10KOhm
R7607 10KOhm
R7608 10KOhm
R7609 10KOhm
R7610 10KOhm
R7611 1.33KOhm
R7612 1.33KOhm
R7615 1.33KOhm
R7616 1.33KOhm
R7613 1.33KOhm
R7614 1.33KOhm
R7619 1.33KOhm
R7617 1.33KOhm
C7601 0.01UF/16V
C7602 0.01UF/16V
C7603 0.01UF/16V
C7605 0.01UF/16V
FBAVREF1
FBAVREF1Q
FBAVREF3
FBAVREF3Q
Place 0.1UF cap sunder ther memory device
C7679 4.7UF/6.3V
Title : N11P-GV1
ASUSTeK COMPUTER INC. NB1
Engineer: Yun-feng_yan
Size: Custom
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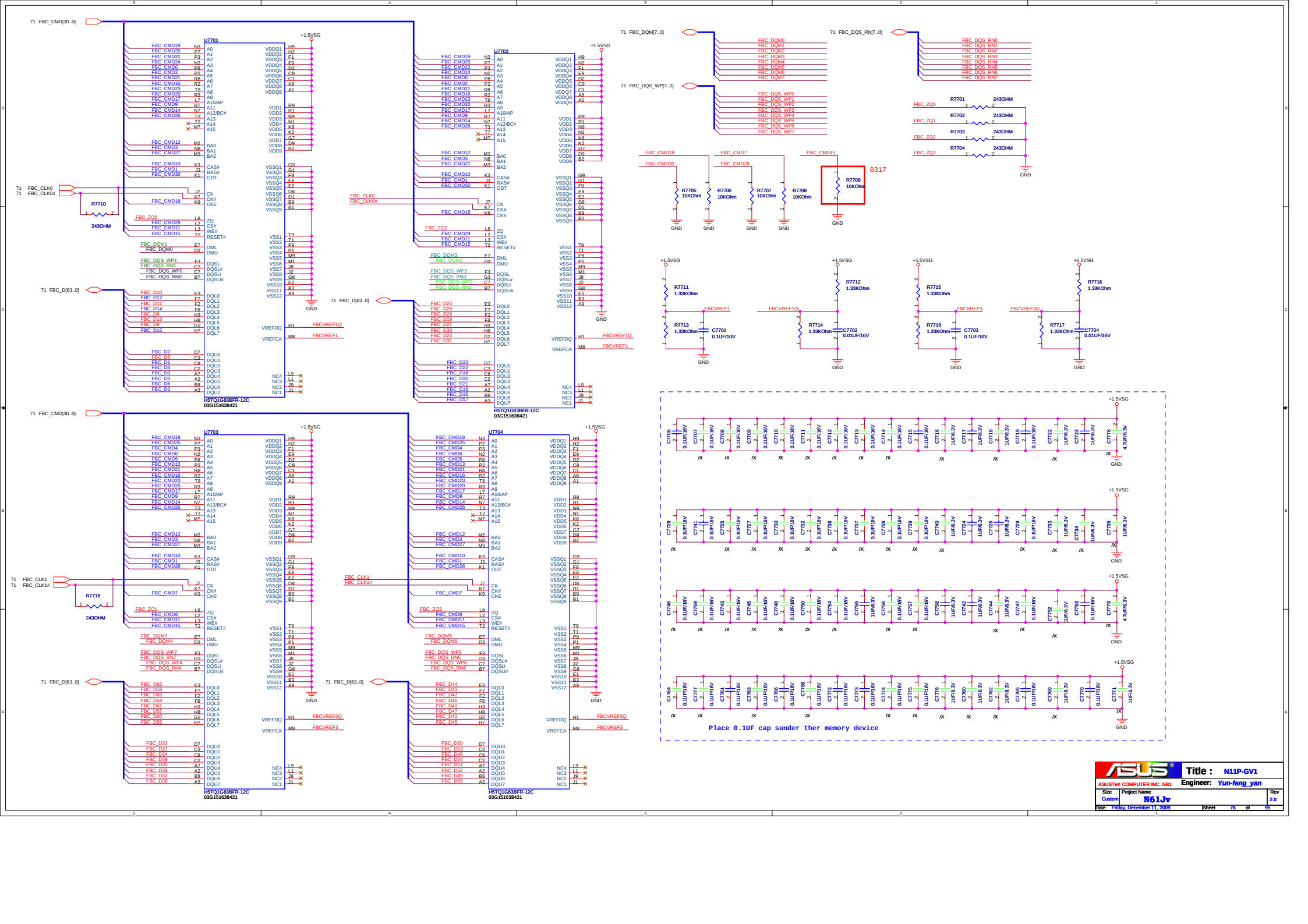
71 FBC_CMD[30..0]
U7701
U7702
U7703
U7704
+1.5VSG
GND
71 FBC_CLK0
71 FBC_CLK0#
R7710
243OHM
71 FBC_CLK1
71 FBC_CLK1#
R7718
71 FBC_D[63..0]
H5TQ1G63BFR-12C
03G151638421
71 FBC_DQM[7..0]
71 FBC_DQS_WP[7..0]
71 FBC_DQS_RN[7..0]
R7701 243OHM
R7702 243OHM
R7703 243OHM
R7704 243OHM
FBC_ZQ0
FBC_ZQ1
FBC_ZQ2
FBC_ZQ3
FBC_CMD18
FBC_CMD30
FBC_CMD7
FBC_CMD28
FBC_CMD15
R7705 10KOhm
R7706 10KOhm
R7707 10KOhm
R7708 10KOhm
R7709 10KOhm
0317
R7711 1.33KOhm
R7712 1.33KOhm
R7713 1.33KOhm
R7714 1.33KOhm
R7715 1.33KOhm
R7716 1.33KOhm
R7717 1.33KOhm
R7719 1.33KOhm
FBCVREF1
FBCVREF1Q
FBCVREF3
FBCVREF3Q
C7701 0.01UF/10V
C7702 0.01UF/16V
C7703 0.1UF/10V
C7704 0.01UF/16V
Place 0.1UF cap sunder ther memory device
Title : N11P-GV1
ASUSTeK COMPUTER INC. NB1
Engineer: Yun-feng_yan
Size: Custom
Project Name: N61Jv
Rev: 2.0
Date: Friday, December 11, 2009
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Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, November 11, 2009
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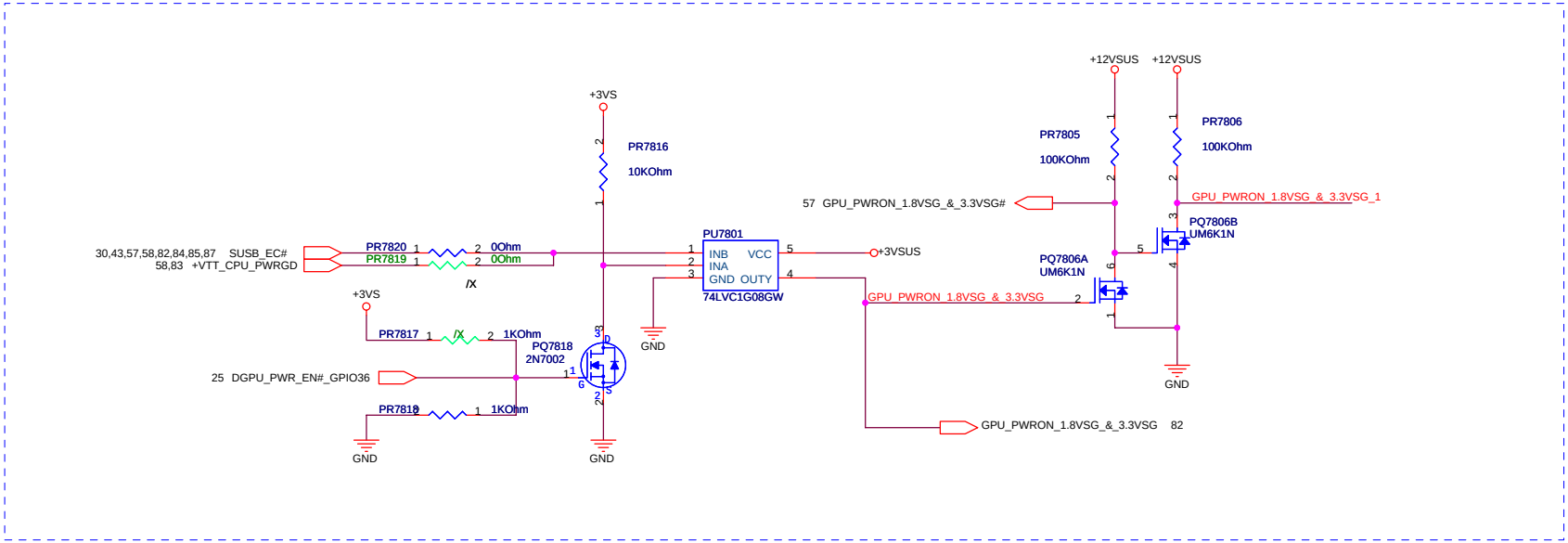
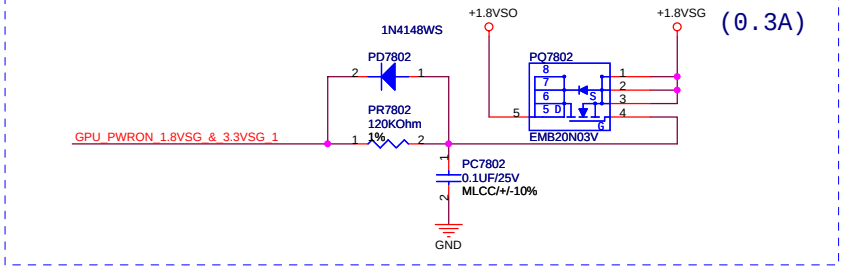
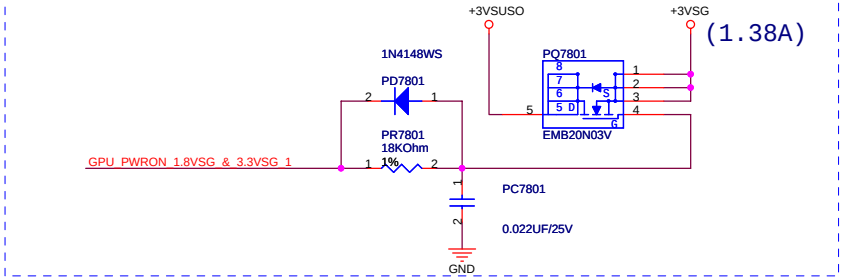
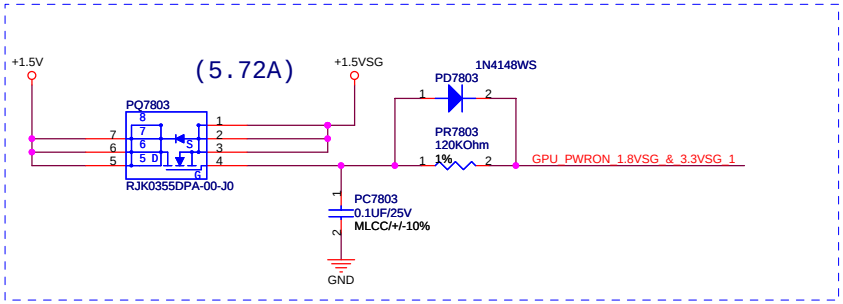
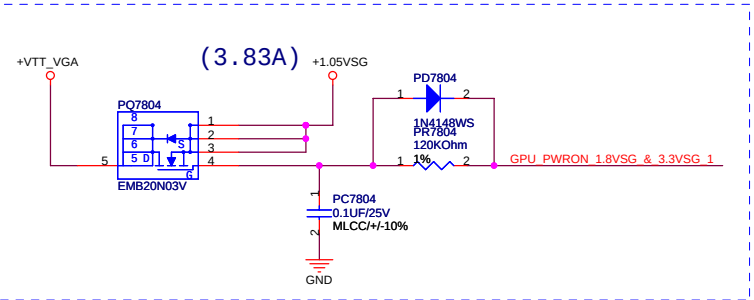


7/15 Change R7606 and C7604 for power on sequence

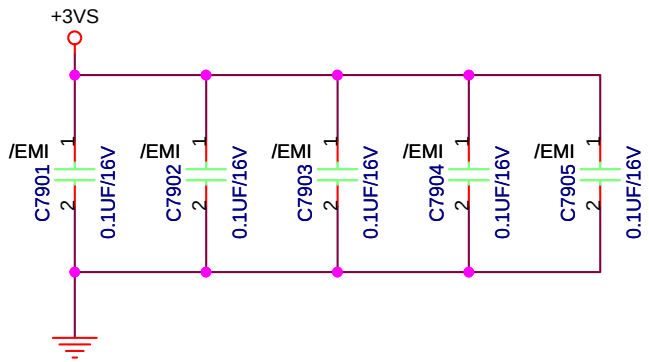


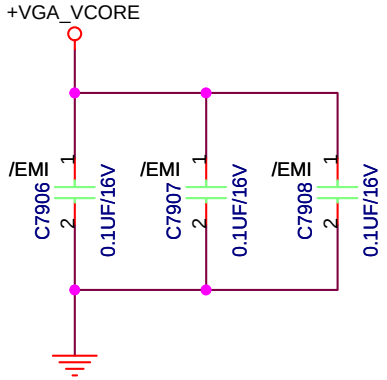


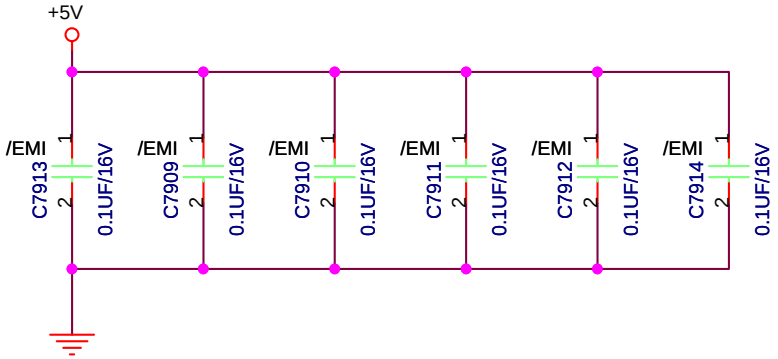




ASUSTeK COMPUTER INC. NB4	Title : Madison Power Sel	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 78 of 95	







ASUSTeK COMPUTER INC. NB4	Title : EMI	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
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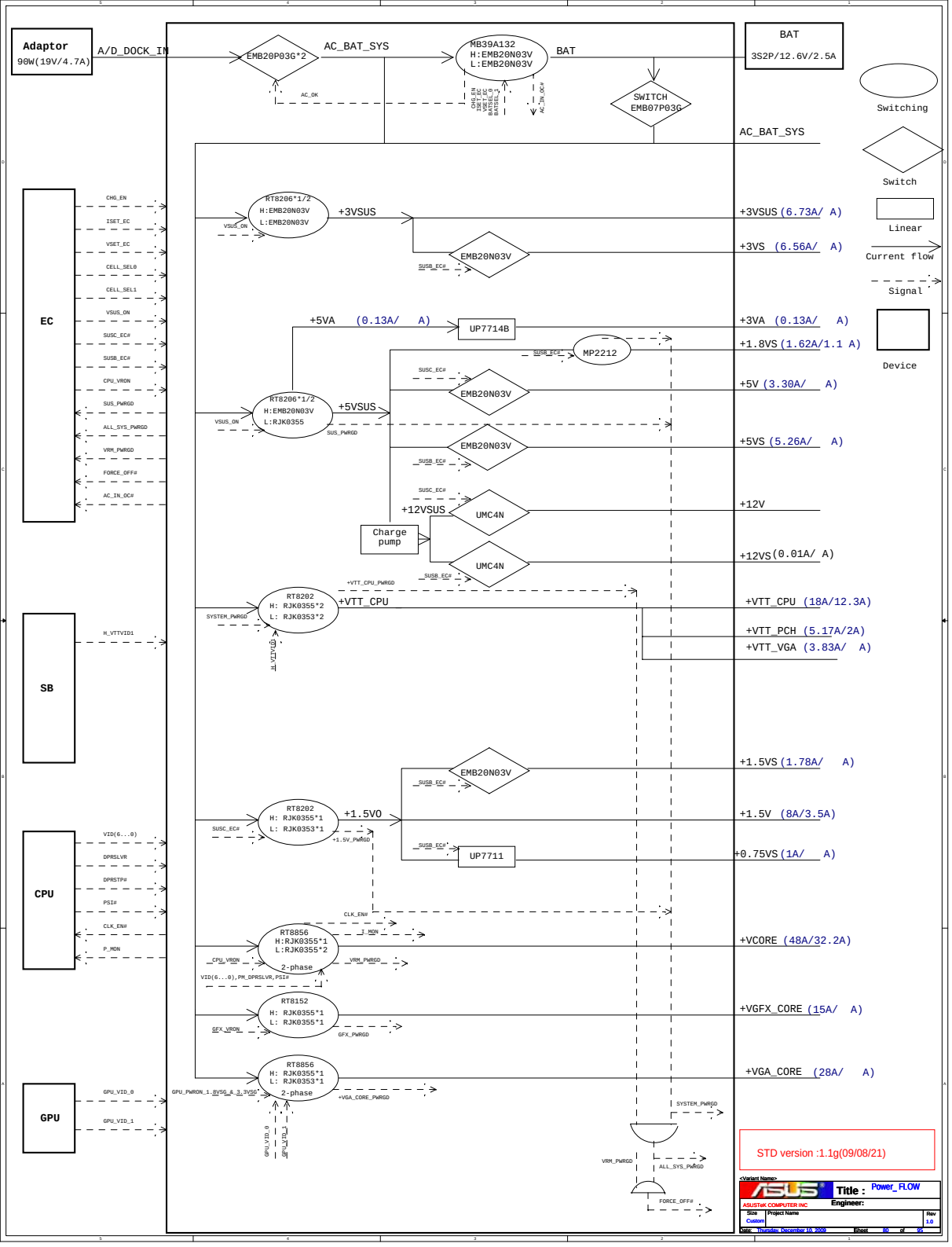
Adaptor
90W(19V/4.7A)
A/D_DOCK_IN
EMB20P03G*2
AC_BAT_SYS
MB39A132
H:EMB20N03V
L:EMB20N03V
BAT
BAT
3S2P/12.6V/2.5A
SWITCH
EMB07P03G
AC_OK
Switching
Switch
Linear
Current flow
Signal
Device
EC
SB
CPU
GPU
RT8206*1/2
H:EMB20N03V
L:EMB20N03V
+3VSUS
+3VSUS (6.73A/ A)
EMB20N03V
+3VS (6.56A/ A)
+5VA (0.13A/ A)
UP7714B
+3VA (0.13A/ A)
MP2212
+1.8VS (1.62A/1.1 A)
+5V (3.30A/ A)
RT8206*1/2
H:EMB20N03V
L:RJK0355
+5VSUS
+5VS (5.26A/ A)
+12V
Charge pump
+12VSUS
UMC4N
+12VS (0.01A/ A)
RT8202
H: RJK0355*2
L: RJK0353*2
+VTT_CPU
+VTT_CPU (18A/12.3A)
+VTT_PCH (5.17A/2A)
+VTT_VGA (3.83A/ A)
+1.5VS (1.78A/ A)
RT8202
H: RJK0355*1
L: RJK0353*1
+1.5VO
+1.5V (8A/3.5A)
+0.75VS (1A/ A)
UP7711
RT8856
H:RJK0355*1
L:RJK0355*2
2-phase
+VCORE (48A/32.2A)
RT8152
H: RJK0355*1
L: RJK0355*1
+VGFX_CORE (15A/ A)
RT8856
H: RJK0355*1
L: RJK0353*1
2-phase
+VGA_CORE (28A/ A)
STD version :1.1g(09/08/21)
Title : Power_FLOW
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name
Rev: 1.0
Date: Thursday, December 10, 2009
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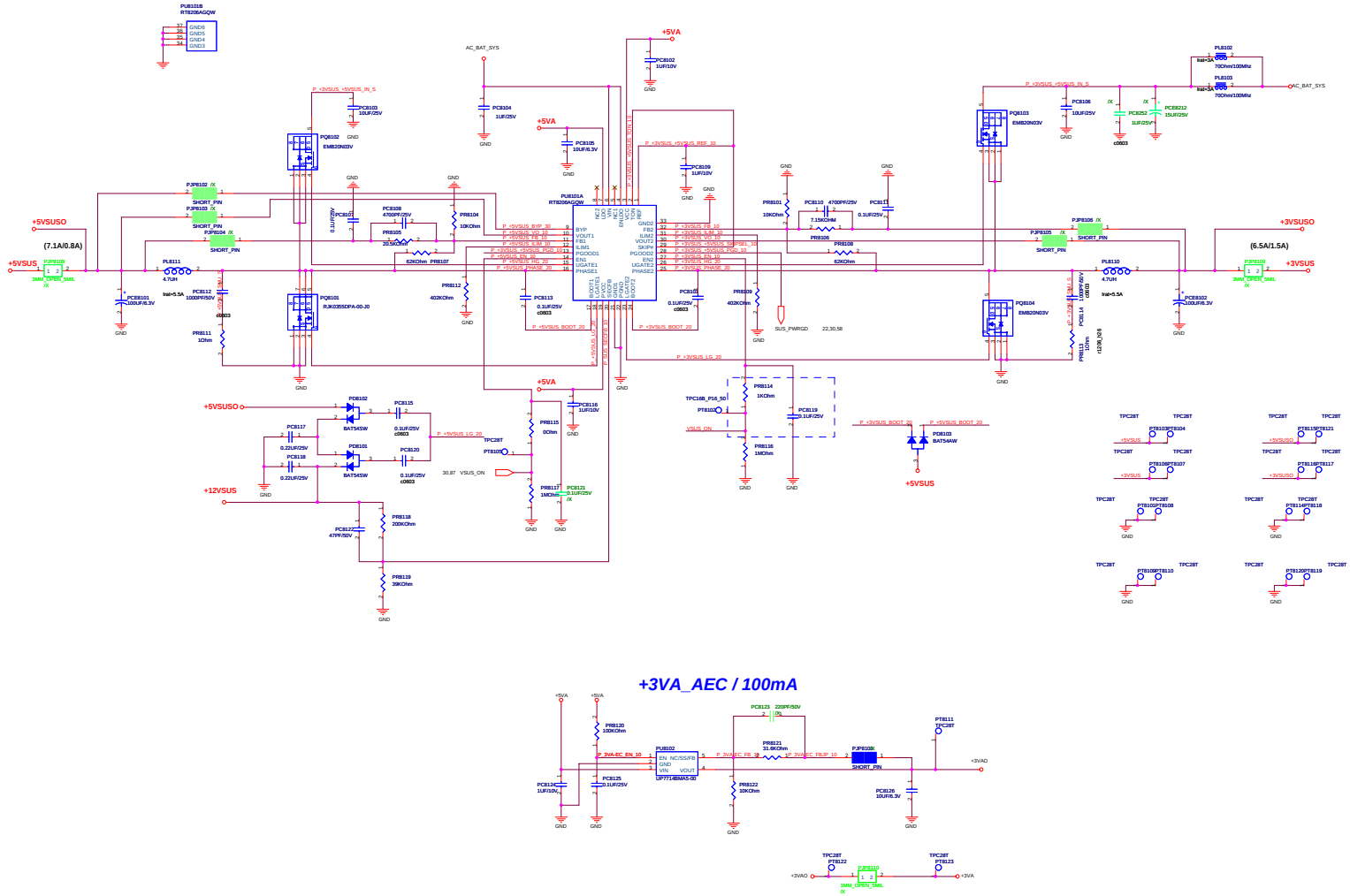

Power stage	+3VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =1.375A	
2. Ripple Current:	
I rip =1.152A	
I spec=2.5A ⊙1	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=1.55A	
ESR / 1 pcs =15mohm	
〉V =23.25mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25)
I peak = 32A	(Pause ≦10 us)
L-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25)
I peak = 32 A	(Pause ≦10 us)

Power stage	+5VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =2.082A	
2. Ripple Current:	
I rip =1.012A	
I spec=2.5A ⊙1	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=2.58A	
ESR / 1 pcs =15 mohm	
〉V =38.72mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm	(Vgs=4.5 V)
I cont = 8 A	(T =25)
I peak = 32A	(Pause ≦10 us)
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm	(Vgs=4.5 V)
I cont = 30 A	(T =25)
I peak = 120 A	(Pause ≦10 us)

Controller	+3VSUS
1. Voltage & Current:	
+3VSUS=3.3V@6.73A	
2. Frequency:	
fosc=375KHz	
3. OCP:	
Set PR8109=402Kohm	
Iocp=8.74A	
4. Soft start time:	
Tss=2ms	
5.Inrush Current:	
C total = 100 uF	
I inrush= 0.165 A	

Controller	+5VSUS
1. Voltage & Current:	
+5VSUS=5V@5.27A	
2. Frequency:	
fosc=300KHz	
3. OCP:	
Set PR8112=402Kohm	
Iocp=17A	
8. Soft start time:	
Tss=2ms	
10.Inrush Current:	
C total = 100 uF	
I inrush= 0.275 A	

ASUSTeK Computer INC

Title : Power +5SUS&+3VSUS&+12VSUS

Engineer: ZHI-KUN_LIU

Size: Custom | Project Name: N61JV | Rev: 1.2

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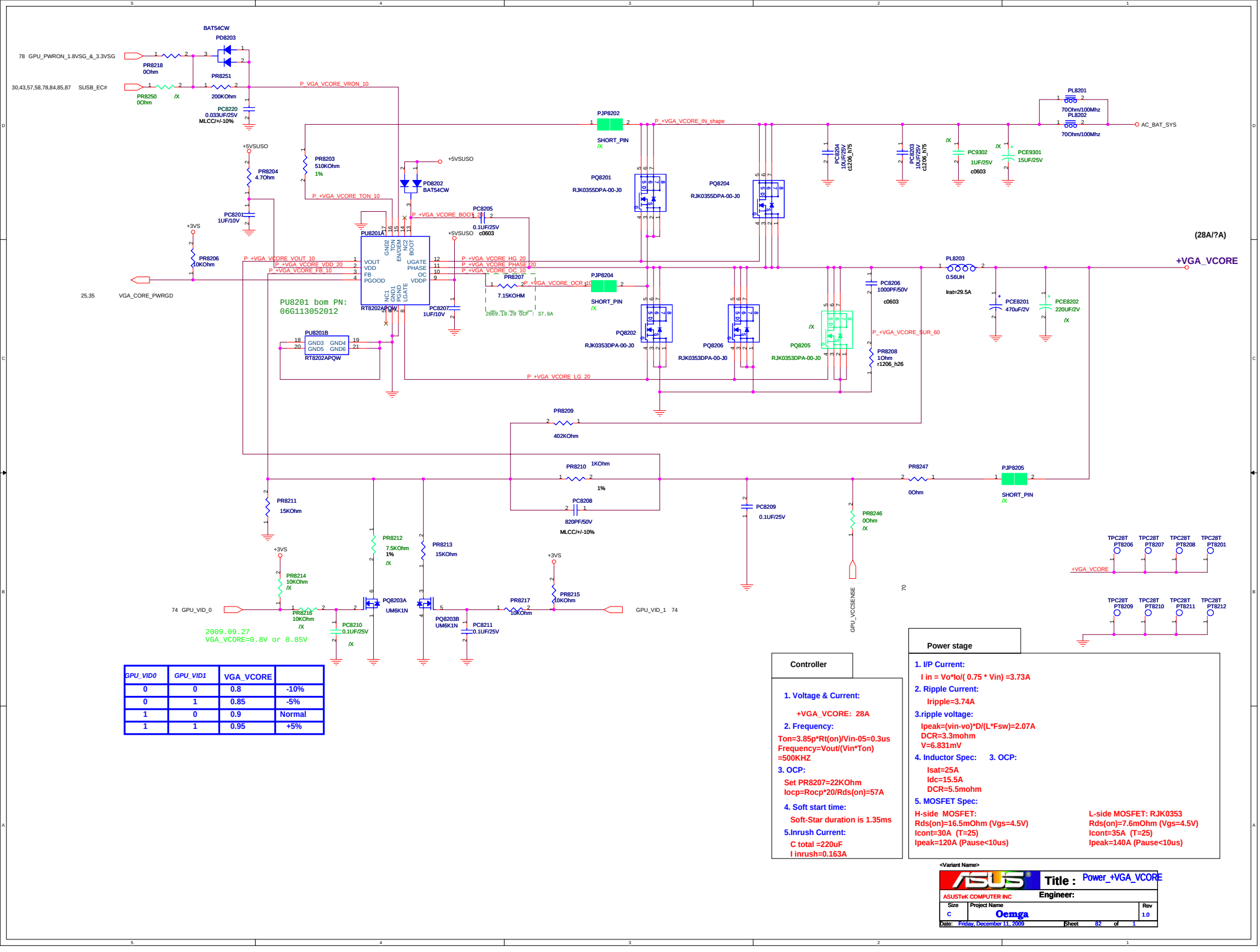


GPU_VID0	GPU_VID1	VGA_VCORE	
0	0	0.8	-10%
0	1	0.85	-5%
1	0	0.9	Normal
1	1	0.95	+5%

Controller

1. Voltage & Current:

   +VGA_VCORE: 28A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

Set PR8207=22KOhm
Iocp=Rocp*20/Rds(on)=57A

4. Soft start time:

Soft-Star duration is 1.35ms

5.Inrush Current:

C total =220uF
I inrush=0.163A

Power stage

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =3.73A

2. Ripple Current:

Iripple=3.74A

3.ripple voltage:

Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
DCR=3.3mohm
V=6.831mV

4. Inductor Spec: 3. OCP:

Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:

H-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

L-side MOSFET: RJK0353
Rds(on)=7.6mOhm (Vgs=4.5V)
Icont=35A (T=25)
Ipeak=140A (Pause<10us)

<Variant Name>

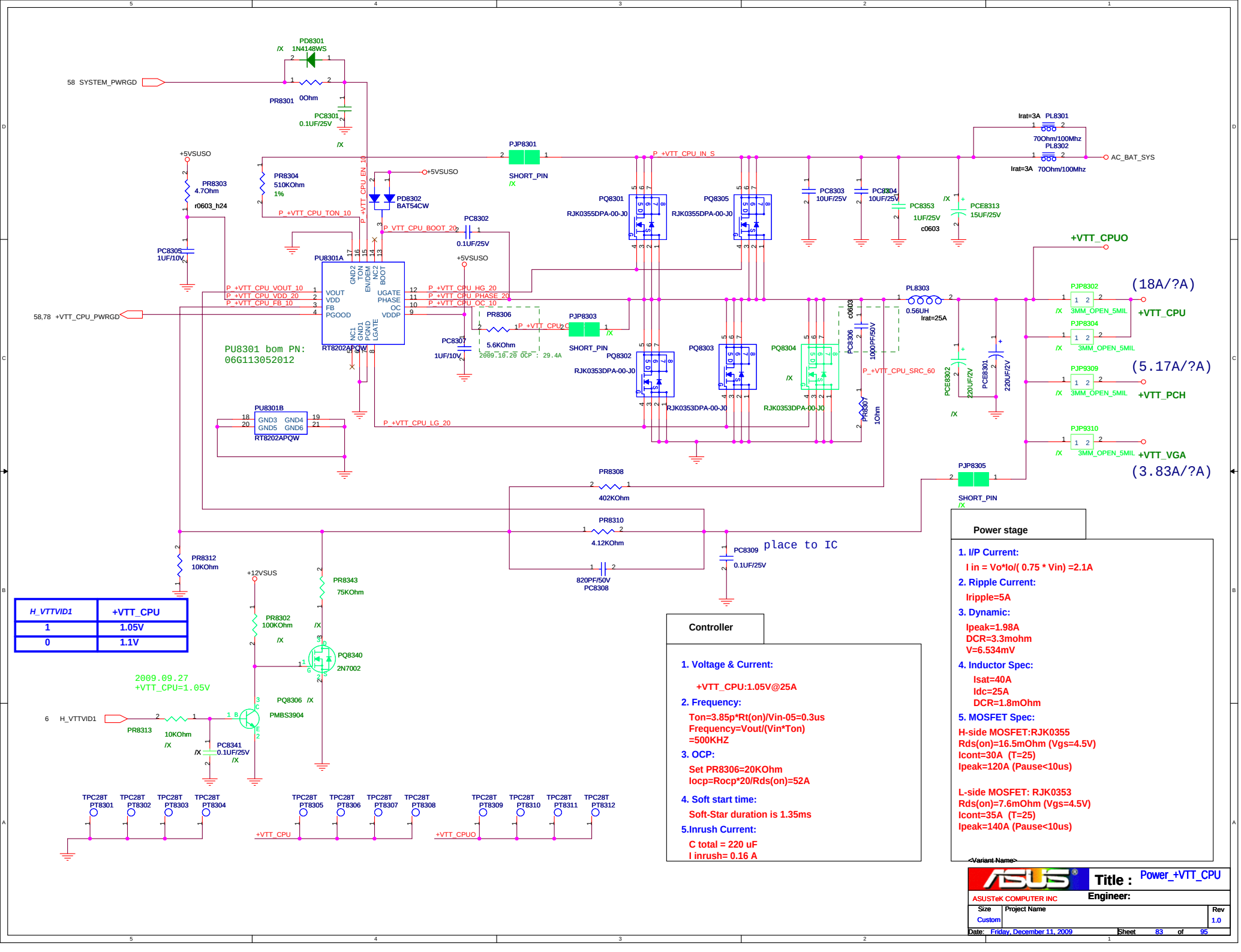
ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Friday, December 11, 2009 Sheet 82 of 1



H_VTTVID1	+VTT_CPU
1	1.05V
0	1.1V

Controller

1. Voltage & Current:
   +VTT_CPU:1.05V@25A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8306=20KOhm
   Iocp=Rocp*20/Rds(on)=52A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.1A
2. Ripple Current:
   Iripple=5A
3. Dynamic:
   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.8mOhm
5. MOSFET Spec:

H-side MOSFET:RJK0355
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

L-side MOSFET: RJK0353
Rds(on)=7.6mOhm (Vgs=4.5V)
Icont=35A (T=25)
Ipeak=140A (Pause<10us)

<Variant Name>

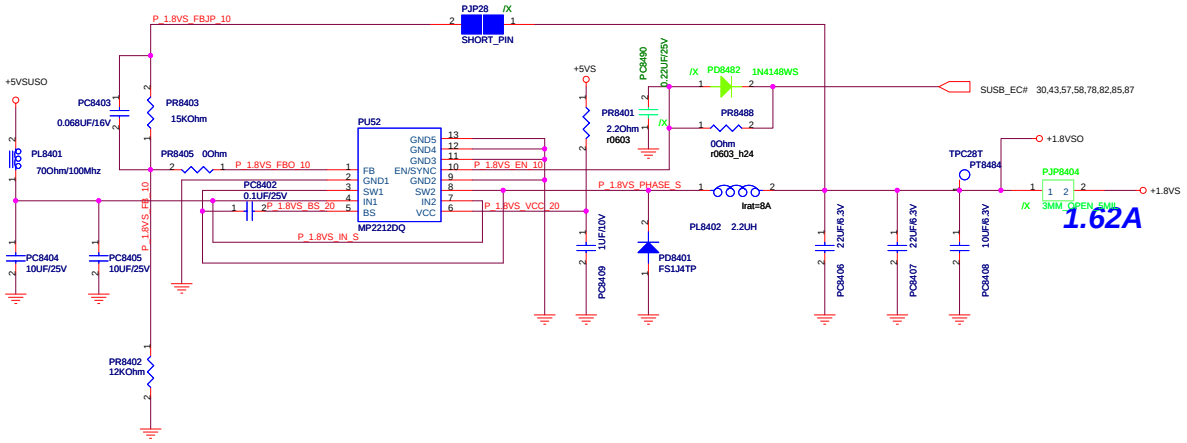
ASUSTeK COMPUTER INC

Title : Power_+VTT_CPU

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, December 11, 2009 Sheet 83 of 95



Power stage

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =0.73A

2. Ripple Current:

I rip =1.08A
I spec=2.5A ⊙1 pcs

3. Inductor Spec:

I sat=14 A
I dc =8 A
DCR=18 mohm

Controller

1. Voltage & Current:

+1.8VS@1.62A

2. Frequency:

Fosc=600KHz

3. Current Limit:

6A

4.Continue Current:

3.75A

5. POR:

POR Hysteresis =0.2V
V on =2.8V

6. Enable Voltage:

V = 1.6V

7. Soft start time:

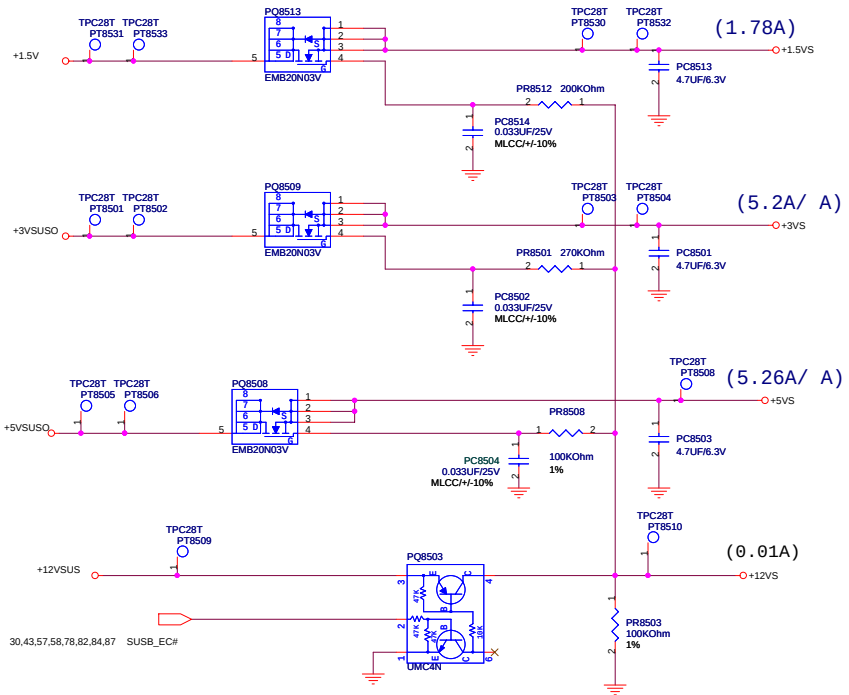
Tss=120us

8.Inrush Current:

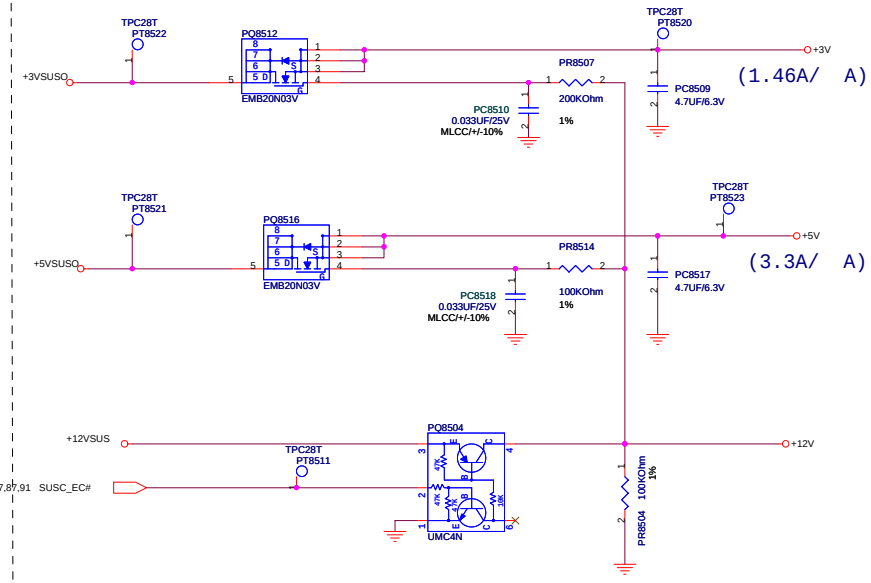
C total = 54 uF
I inrush=
0.473A

ASUSTek Computer INC	Title : +1.8VS	
	Engineer:	
Size: C	Project Name: N61JV	Rev: <RevCode>
Date: Friday, December 11, 2009	Sheet 84 of 95	

SUSB#_PWR POWER



SUSC#_PWR POWER



<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_Load_Switch

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, December 11, 2009 Sheet 85 of 95

<Variant Name>

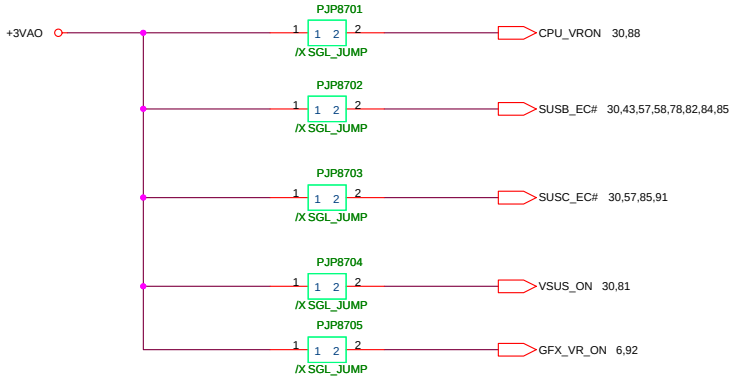
ASUSTeK COMPUTER INC

Title : Power_good_detecter

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, December 10, 2009 Sheet 86 of 95



<Variant Name>

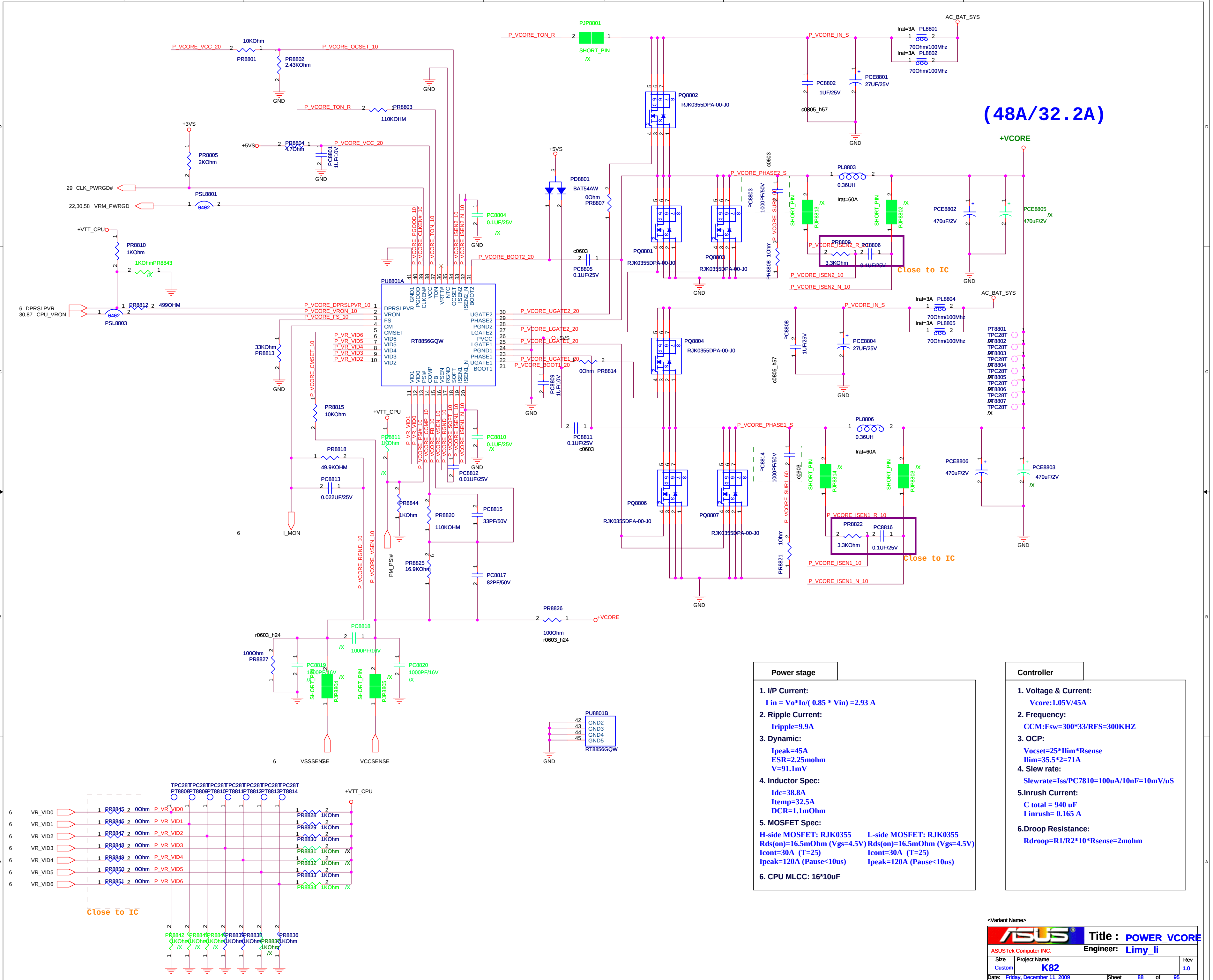
ASUSTeK COMPUTER INC

Title : Power_for_test

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, December 11, 2009 Sheet 87 of 95



Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
   Iripple=9.9A
3. Dynamic:
   Ipeak=45A
   ESR=2.25mohm
   V=91.1mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:

H-side MOSFET: RJK0355	L-side MOSFET: RJK0355
Rds(on)=16.5mOhm (Vgs=4.5V)	Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)	Icont=30A (T=25)
Ipeak=120A (Pause<10us)	Ipeak=120A (Pause<10us)

6. CPU MLCC: 16*10uF

Controller

1. Voltage & Current:
   Vcore:1.05V/45A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vocset=25*Ilim*Rsense
   Ilim=35.5*2=71A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 940 uF
   I inrush= 0.165 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=2mohm

<Variant Name>

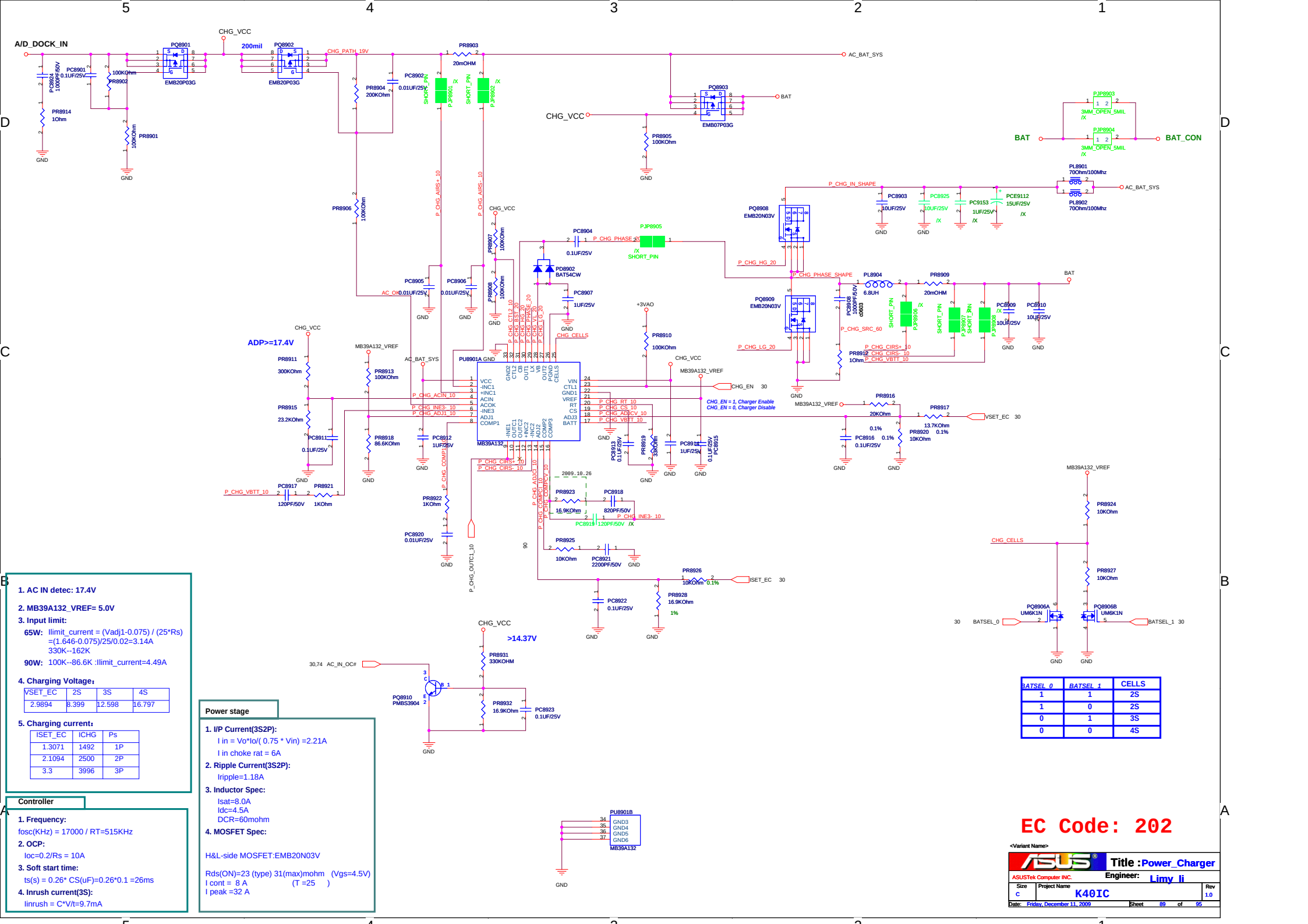
ASUSTek Computer INC.

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
Custom	K82	1.0

Date: Friday, December 11, 2009 Sheet 88 of 95



1. AC IN detec: 17.4V

2. MB39A132_VREF= 5.0V

3. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

4. Charging Voltage:

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

5. Charging current:

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:
fosc(KHz) = 17000 / RT=515KHz
2. OCP:
Ioc=0.2/Rs = 10A
3. Soft start time:
ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms
4. Inrush current(3S):
Iinrush = C*V/t=9.7mA

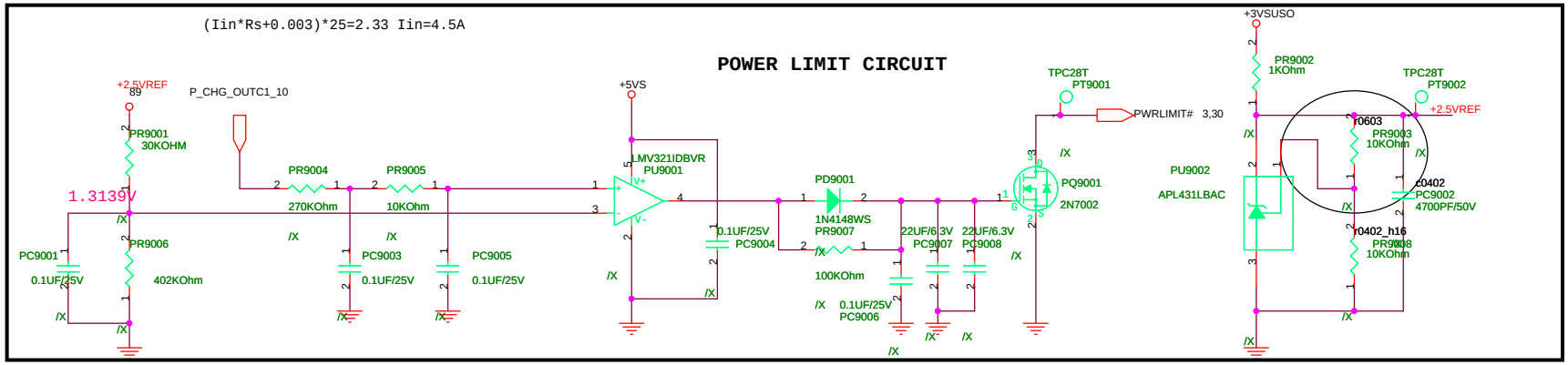
Power stage

1. I/P Current(3S2P):
I in = Vo*Io/(0.75 * Vin) =2.21A
I in choke rat = 6A
2. Ripple Current(3S2P):
Iripple=1.18A
3. Inductor Spec:
Isat=8.0A
Idc=4.5A
DCR=60mohm
4. MOSFET Spec:

H&L-side MOSFET:EMB20N03V

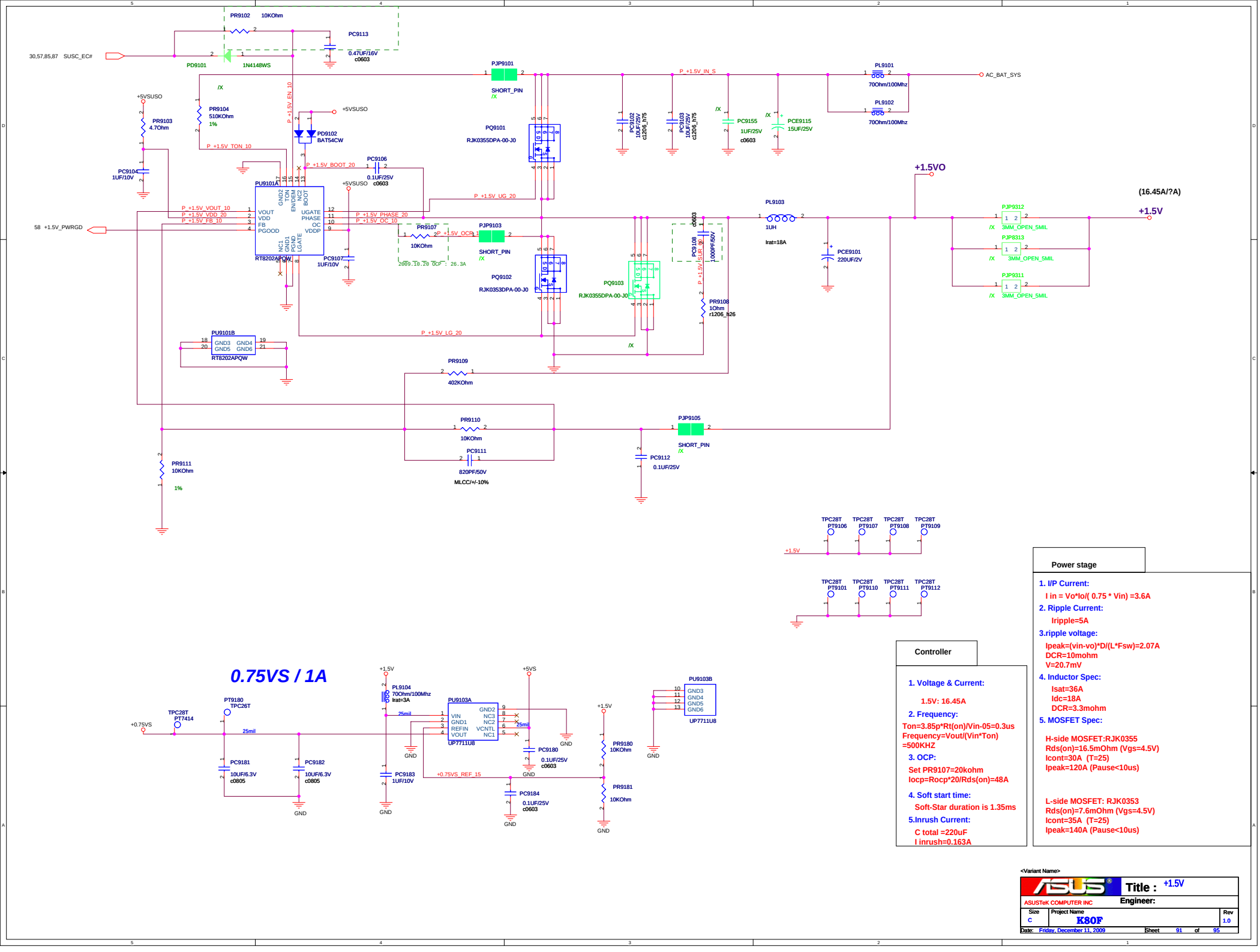
Rds(ON)=23 (type) 31(max)mohm (Vgs=4.5V)
I cont = 8 A (T =25)
I peak =32 A

BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S



<Variant Name>

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Limy_li	
Size: A3	Project Name: F83T	Rev: 2.1G
Date: Friday, December 11, 2009	Sheet 90 of 95	



Power stage

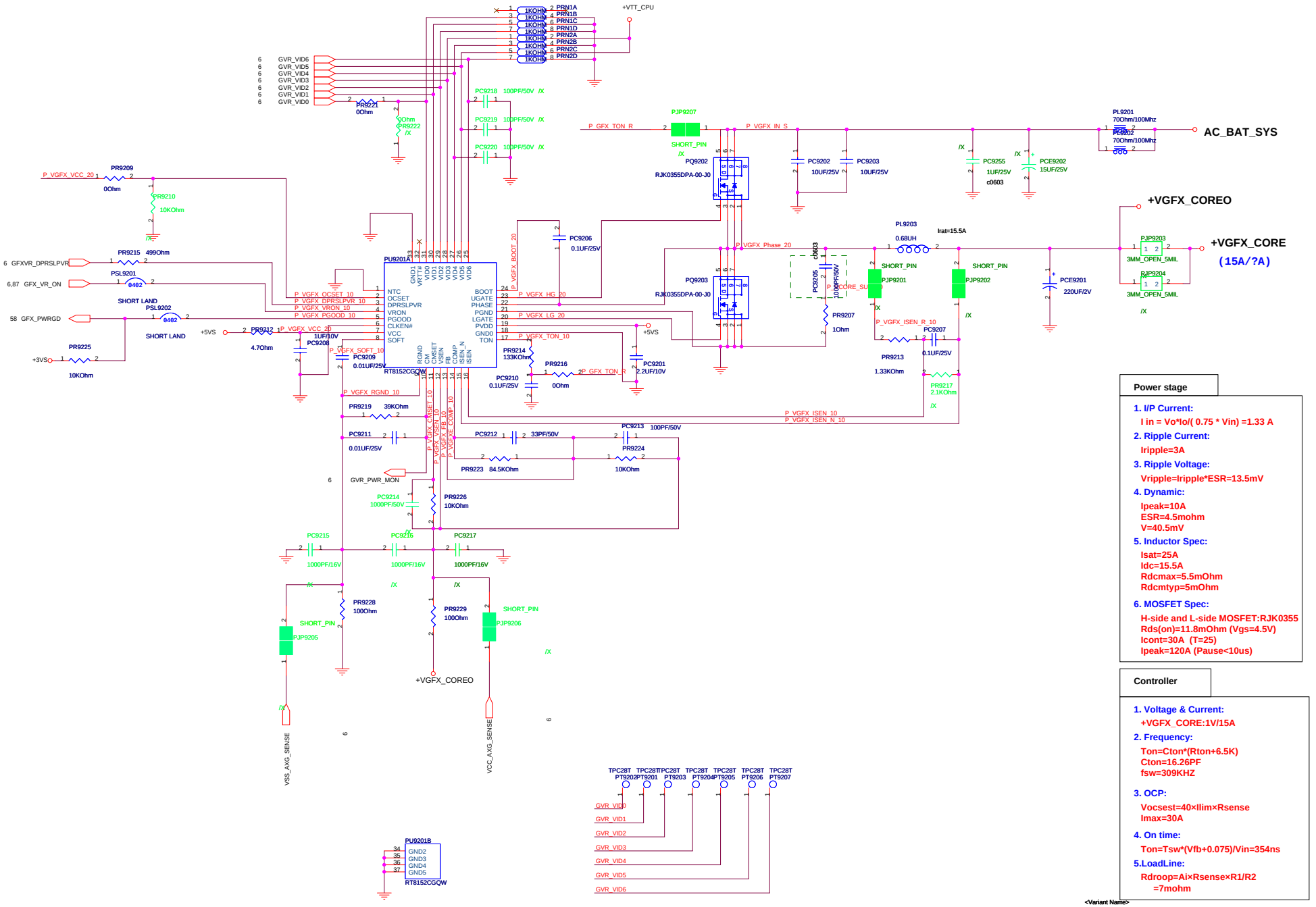
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =3.6A
2. Ripple Current:
   Iripple=5A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=10mohm
   V=20.7mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:
   H-side MOSFET:RJK0355
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)
   L-side MOSFET: RJK0353
   Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

Controller

1. Voltage & Current:
   1.5V: 16.45A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR9107=20kohm
   Iocp=Rocp*20/Rds(on)=48A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

<Variant Name>

ASUSTeK COMPUTER INC	Title : +1.5V	
	Engineer:	
Size: C	Project Name: K80F	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 91 of 95	



Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocset=40×Ilim×Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai×Rsense×R1/R2
   =7mohm

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
C	UX21	1.0

Date: Friday, December 11, 2009 Sheet 92 of 95

1.將58頁+3V0改為+3VSUS。
2. Add change SL3801 to 33Ohm Resistor for ESD
3.change D3401 and D3402 stuff by default.
4.Follow Design Ip swap USB port 3 and Port 11
5、Change SL3402,SL3403,SL3404,SL3405,SL3406,SL3407,SL3408,SL3409 to 0402 SL
6.Change R5638 to 5V, eagle eye,add power led to 5V for prevent eagle eye,add power led will flash when insert AC.
7.Mount C3634,C3635,C3409,C5607,D4505,D4506,change R6301 from 27.4ohm to 1K,reverse D6402 for EMI suggestion.
8.Change card reader from port3 to port11 for follow Design IP.
9.Change R4007,R4012 footprint to 0603 for power.
10.Add R0638 for ATS graphic power test.
11.Add U6802,R6811,R6812,C6861,C6862,C6863,C6864 and SL6802 for USB30 +1.05V support.
12.Change R3021,R3023 to 100K for follow EC Design IP.
13.umount R0605.
14.Stuff R0606.
15.Delete SL3313.
16.umount R7404.
17.change EC8512 to EC8570.
18.Add USB2.0 signal Switch U5201.
19.JP5401 don't be short.
20.EC SMB1 Pull High to +3VSUS.
21.Add Support NB290 schematic------Page61.
22.Delete DGPU HDMI output.
23.Add thermal sensor G709 Support.

ER---------->>>>> PR

1.change SL4513 to R4509;----P45
2.change R3554.Pin2 from DGPU_PWROK to DGPU_HOLD_RST# ,Change R3555.Pin1 Pull High to +5VS,Add C3510,C3511;----P35
3.connect U6802.Pin7 to R6811.Pin2;----P68
4.Add SL6322,change LED6306,LED6307,LED6308,LED6309,LED6310,LED6311 Pin1 from +5VA/SUS_IOR to +5V_IOR.----P63
5.Change J6303 part number to 14G152231000;----P63
6.Add C6213,C6214,C6215, Add GND_AUDIO_IO for headphone speaker;----P62
7.Mount D6001;----P60
8.Add USB2.0 Port J5201;----P52
9.Mount C4611,C4612;----P46
10.change R2533 from 10k to 100k;----P25
11.change R4512 to 1k for samsung panel voltage;----P45
12.Umount R5817;------P58
13.Add 07G001007100 Second source 07G001007230---D2205,D2206,D2207,D3207,D4401,D5800
14.Add C3203-------P32;
15.Q3550,R3556,D3510,R3558,C3502 for VGA_CORE_PWRGD;----P35
16.Delete R3602;------P36
17.Umount U5002,C5007,C5001,Q5001;----P50
18.Delete CN5601,Add C5616,C5617,C5618,C5619 for EMI;----P56
19.Add C6303,C6304 for EMI;----P63
20.Add L6204,RN6201,RN6301,L6302,D6301 for EMI;
21.Umount C7254,C7263,C7262,C7261,C7248,C7256,C7255,C7251,R7310,R7313,R7322,R7323,
R7324,R7325,R7326,R7327,Q7301.----P72
22.Mount CN5603,CN5604,C5610,C5611, C5614, C4511;
23.Umount R3509,R3510,R3511,R3512,R3513,R3514,R3515,R3516;----P35
24.Add U2801 secondsource 05G001602110;
25.SKU2 BOM add J6106.
26.Mount C0613,C0654;
27.Umount R5401,R5402.

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

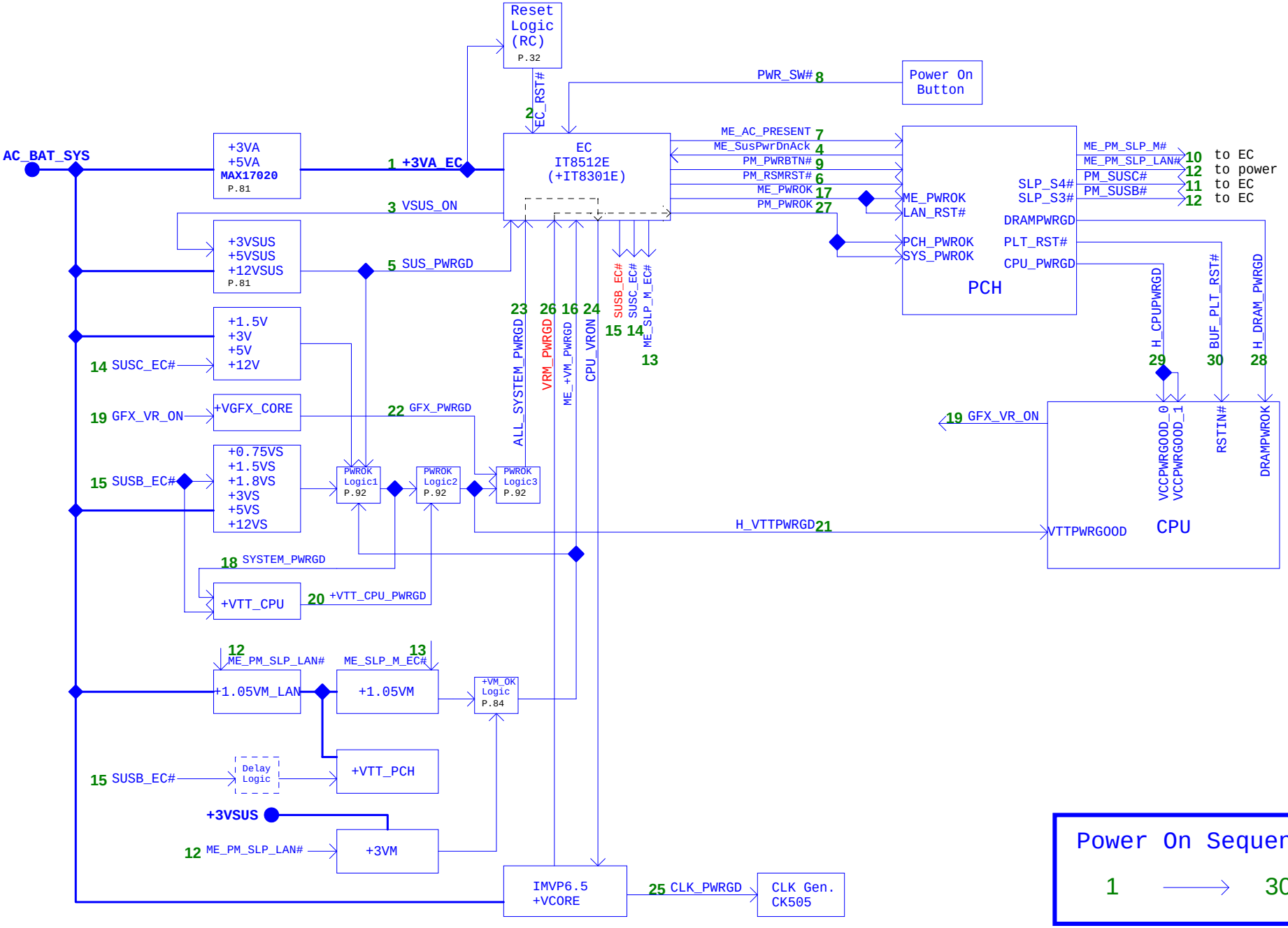
Engineer: yun-feng_yan

Size	Project Name	Rev
B	N61Jv	1.0

Date: Tuesday, December 15, 2009 Sheet 93 of 95

AC-IN Mode

N61Jv Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 30

ASUSTeK COMPUTER INC

Title : POWER SEQUENCE

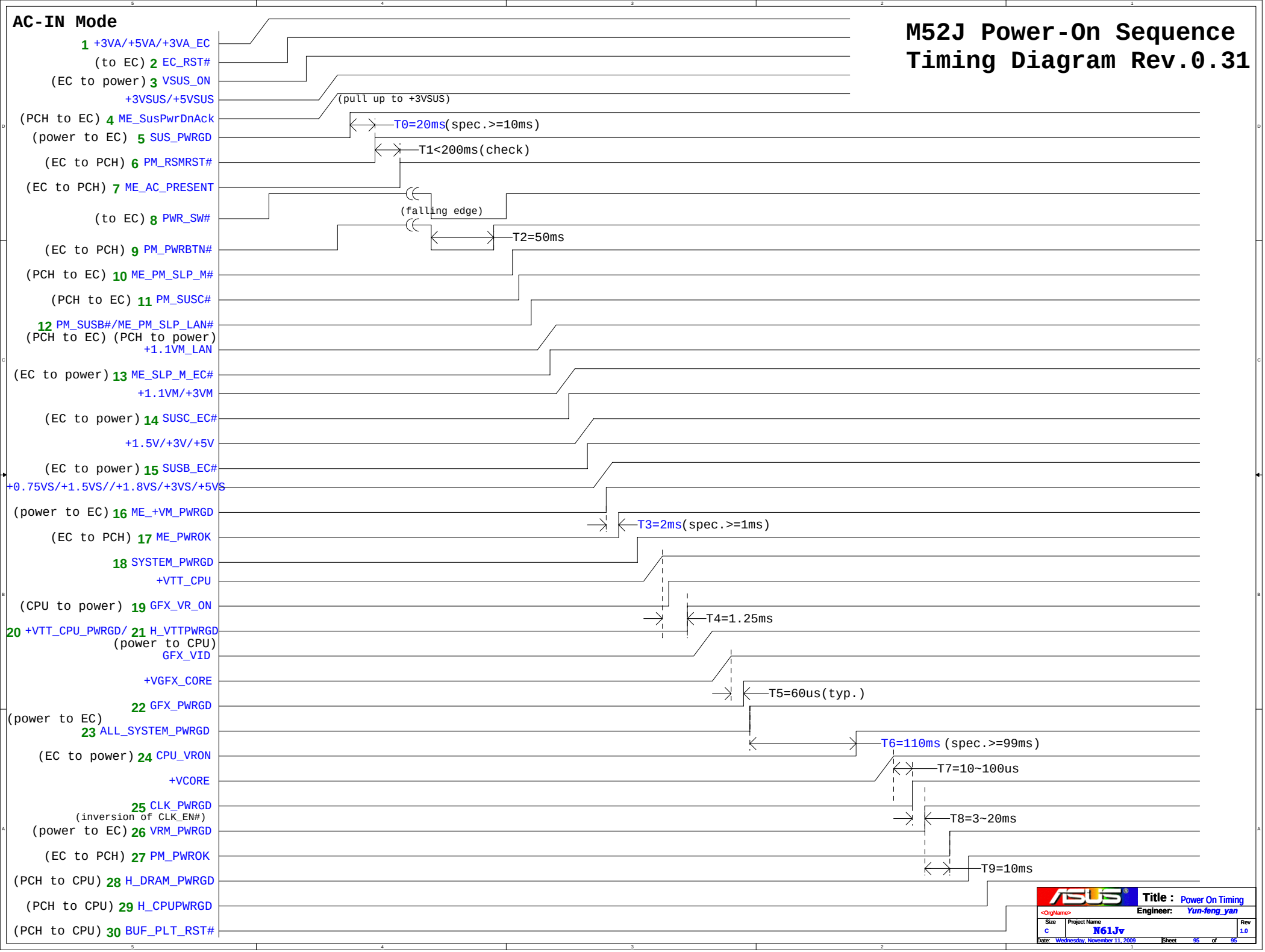
Engineer: Yun-feng_yan

Size	Project Name	Rev
C	N61Jv	1.0

Date: Wednesday, November 11, 2009 Sheet 94 of 95

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode



ASUS	Title : Power On Timing	
<OrgName>	Engineer: Yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 95 of 95	