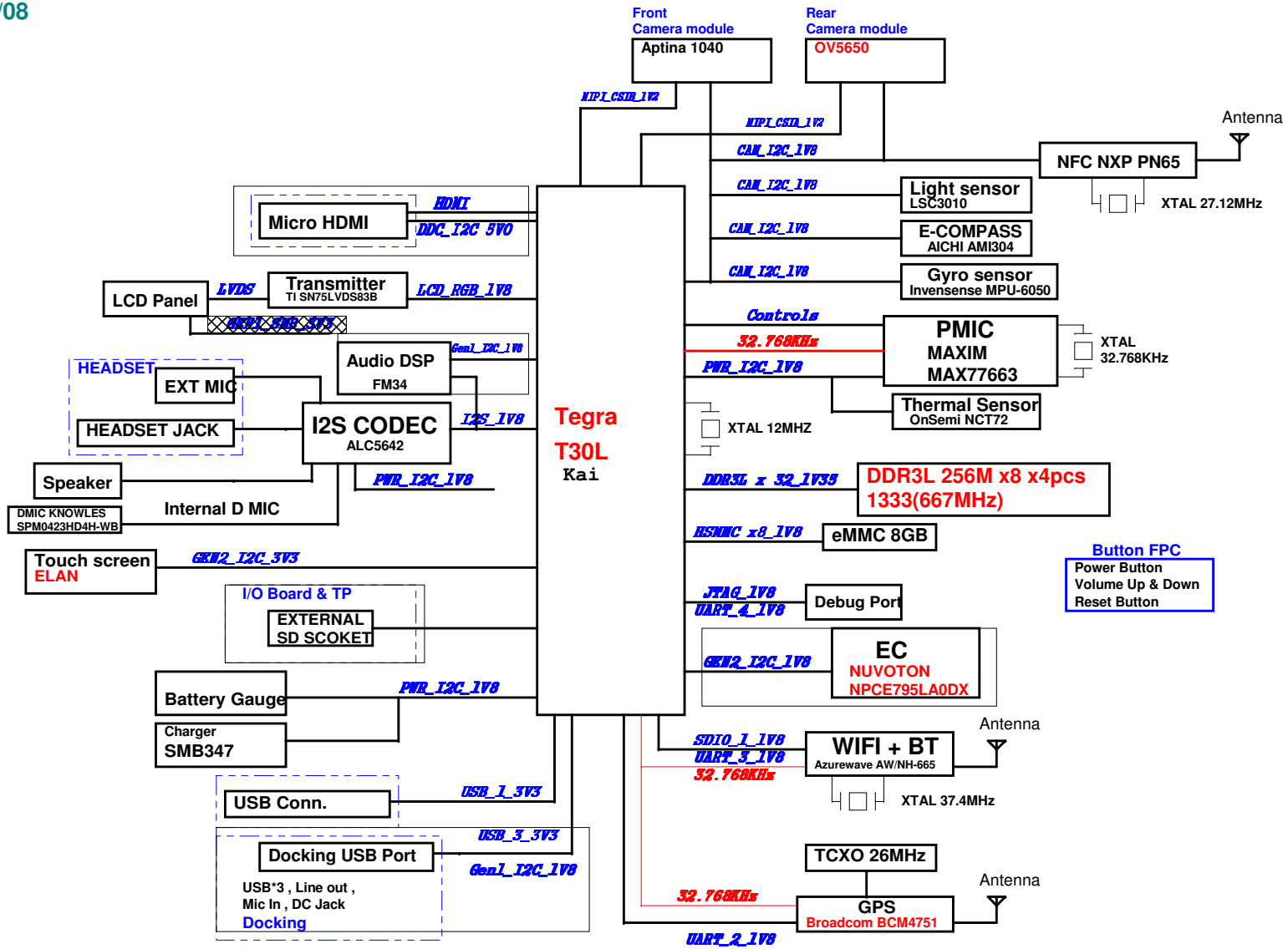
ME370T (Nakasi)

1.0

2012/02/08



ME370T (Nakasi)
Power Tree

Power Source

USB Conn. — VDD_USB1_VBUS
Dock Conn. — DOCK_5V
page 49 Charger SMB347 — VBATT — Battery

page 49 — VCC_LED

VDD_AC_BAT (VPH_PWR_CHGR)

page 48 Buck-Boost TPS63020 → +3VSUS 3.3V, 2A
EN_3V3_SYS(PMU GPIO3)

page 48 Boost RT9276GQW → VDD_5V0_SYS 5V, 1A
EN_5V0_SBY(T30 GMI_AD11)

page 29 U30 LDO S-1167 3.3V, 150mA → for Touch Sensor TP_3V3 page 29
VDD_5V0_SYS enable

page 50~52 PMIC MAX77663
- Internal Usage (MBATT, MON, GPIO_INA & AVSD)
- SD0 → VDD_1V0_GEN 1.05V, 6A, PMIC → T30 CPU VDD_CPU 1.05V, 6.1A, Terga (Tj=90, 1.3GHz)
- SD1 → VDD_1V2_SOC 1.2V, 3A, PMIC → T30 CORE VDD_CORE 1.2V, 2.5A, Terga
- SD2
- SD3 → +1.35V 1.35V, 1.5A, PMIC
- IN_LDO4/6: LDO4 → VDD_PMU_LDO4_1V2 1.2V, 150mA, PMIC → T30 VDD_RTC
- IN_LDO4/6: LDO6 → VDD_PMU_LDO6_3V1V8 3/1.8V, 150mA, PMIC → T30 VDDIO_SDMMC1

page 31 U27 LDO S-1132 2.8V, 300mA → AVDD_CAM1 Camera AVDD
CAM1_LDO_EN(T30 KB_ROW6)

page 31 U28 LDO S-1132 2.8V, 300mA → AVDD_VCM CAMERA AF VCM
CAM2_LDO_EN(T30 KB_ROW8)

page 27 → VDD_SPK Codec Speaker Amp.
page 44 → NFC_VBAT NFC VBAT

page 52 PMIC MAX77663
- IN_LDO2: LDO2 → VDD_PMU_LDO2_2V8 2.8V, 150mA, PMIC → T30 VDD_DDR_RX
- IN_LDO3/5: LDO3 → VDD_PMU_LDO3_2V8 2.8V, 300mA, PMIC → page 20 VCORE_EMMC_S 200mA for eMMC VCC
- LDO5 → VDD_PMU_LDO5 2.8V, 300mA, PMIC → page 31 VDDIO_CAM Camera VDDIO

+3VSUS_CPU → page 5 U1 Power SW NCT352 → T30 VDD_FUSE
EN_VDD_FUSE (T30 LCD_PWR1)
T30 VDD_3V3_GMI

page 14 U14 Power SW NCT352 → T30 AVDD_USB
EN_AVDD_USB (MAX77663 GPIO2)

page 26 VCORE_TEMP for Thermal Sensor

T30 VDDIO_PEX_CTL TBD (no use)

VDD_PNL → page 21 U8 Power SW NCT352 → VCC_LCD3V3 for LCD Panel
EN_VDD_PNL (T30 LCD_M1)

page 22 VDD_LVDS_30 VCC → for LVDS Transmitter VDD_LVDS_30
LVDSVCC → VDD_LVDS_F_30
PLLVCC → VDD_LVDS_PLL_30

page 25 VDD_ALS for Hall Sensor, ALS
page 26 VDD_GYRO for Gyro VDD
page 26 AVDD_ECOM for E-compass AVDD
page 41 WiFi_BT_VCC_3V3 for Wifi/BT Module
page 41 GPS_VDD_BAT_3V3 for GPS

VDD_1V8_GEN 1.8V, 2.0A, PMIC

page 52 PMIC MAX77663
- IN_LDO0/1: LDO0 → VDD_PMU_LDO0_1V0 1.0V, 150mA, PMIC → T30 VDD_DDR_HS
- LDO1 → VDD_PMU_LDO1 150mA, PMIC → No usage
- IN_LDO7/8: LDO7 → VDD_PMU_LDO7_1V2 1.2V, 450mA, PMIC → T30 AVDD_DSI_CSI
- LDO8 → VDD_PMU_LDO8_1V2 1.2V, 300mA, PMIC → T30 AVDD_PLLA_P_C, AVDD_PLLM, AVDD_PLLU_D, AVDD_PLLX

T30 VDDIO_DDR Max. 710mA

DRAM Chip 256Mb x8bits x4pcs
page 19 170mA x4, each DRAM chip → VDD_DDR3L for DDR3L VDD
VDDQ_DDR3L for DDR3L VDDQ

VDD_1V8_GEN_CPU
- T30 AVDD_OSC
- T30 VDDIO_SYS
- T30 VDDIO_CAM
- T30 VDDIO_LCD
- T30 VDDIO_BB
- T30 VDDIO_UART
- T30 VDD_IO_AUDIO
- T30 VDDIO_SDMMC4
- T30 VDDIO_SDMMC3

page 14 Q2 Load SW PMOS → T30 AVDD_USB_PLL
CORE_PWR_REQ

page 20 → for eMMC VCCQ VDDIO_HSMMC
page 22 → IOVCC for LVDS Transmitter IOVCC_30
page 26 → VDDIO_GYRO for Gyro VLOGIC
page 26 → DVDD_ECOM for E-compass DVDD

page 27 VDD_1V8_CDC → for Audio Codec
- DBVDD → VDB_CDC
- CPVDD → VCP_CDC
- AVDD → AVDD_CDC_F
- DCVDD → DACREF_CDC

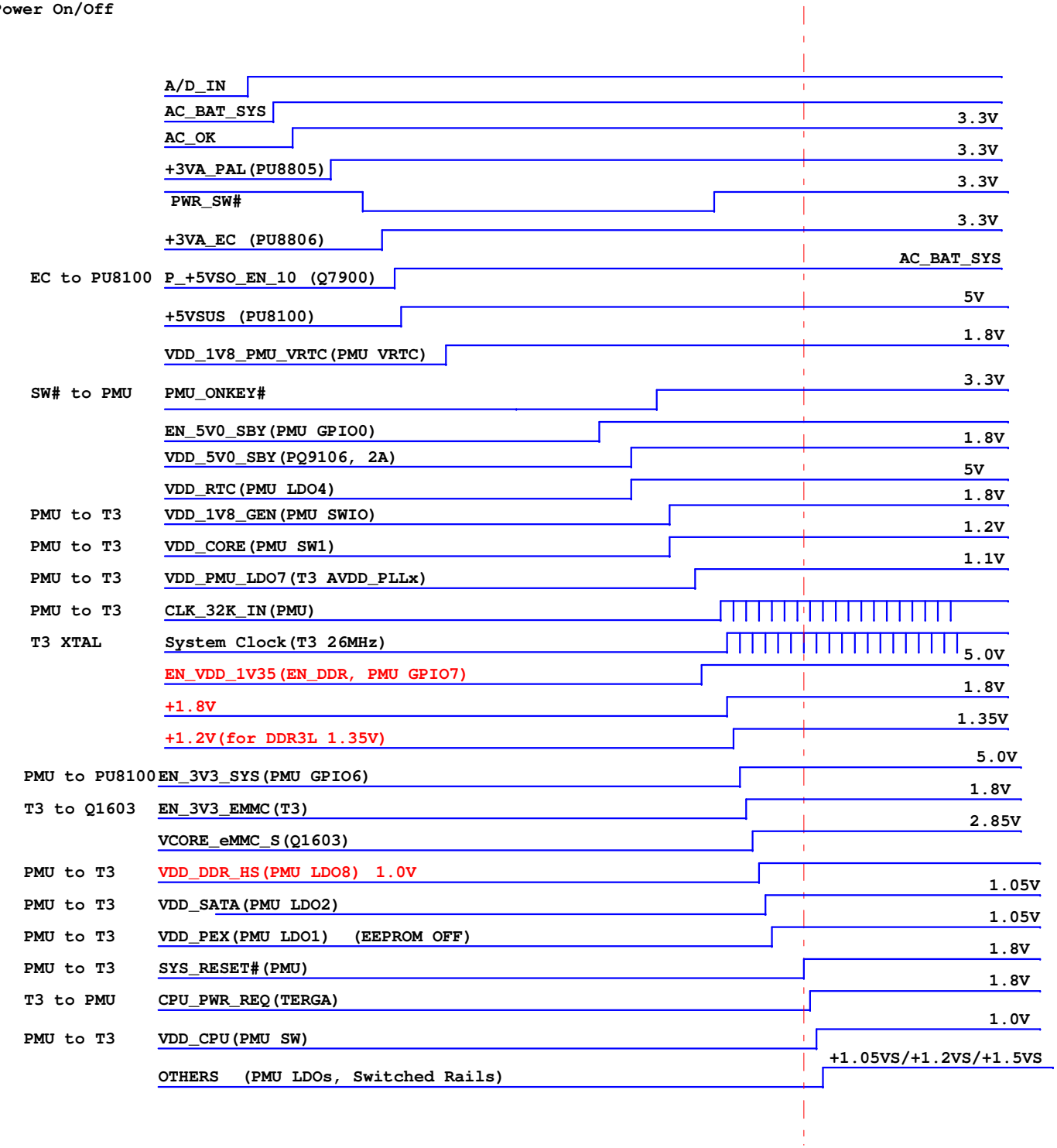
page 27 → VDD_1V8_DMIC for DMIC VDD

page 41 → WiFi_BT_VDDIO_1V8 for Wifi/BT Module
page 43 → GPS_VDD_IO_1V8 for GPS
page 44 → NFC_PVDD for NFC

page 50 PMIC MAX77663 — Internal Usage GPIO_INB

ASUSTeK COMPUTER INC. EPAD
Title : 02.POWER TREE
Engineer: Richard Lin
Size: Custom | Project Name: ME370T | Rev: 2.0
Date: Thursday, March 01, 2012 | Sheet 2 of 60

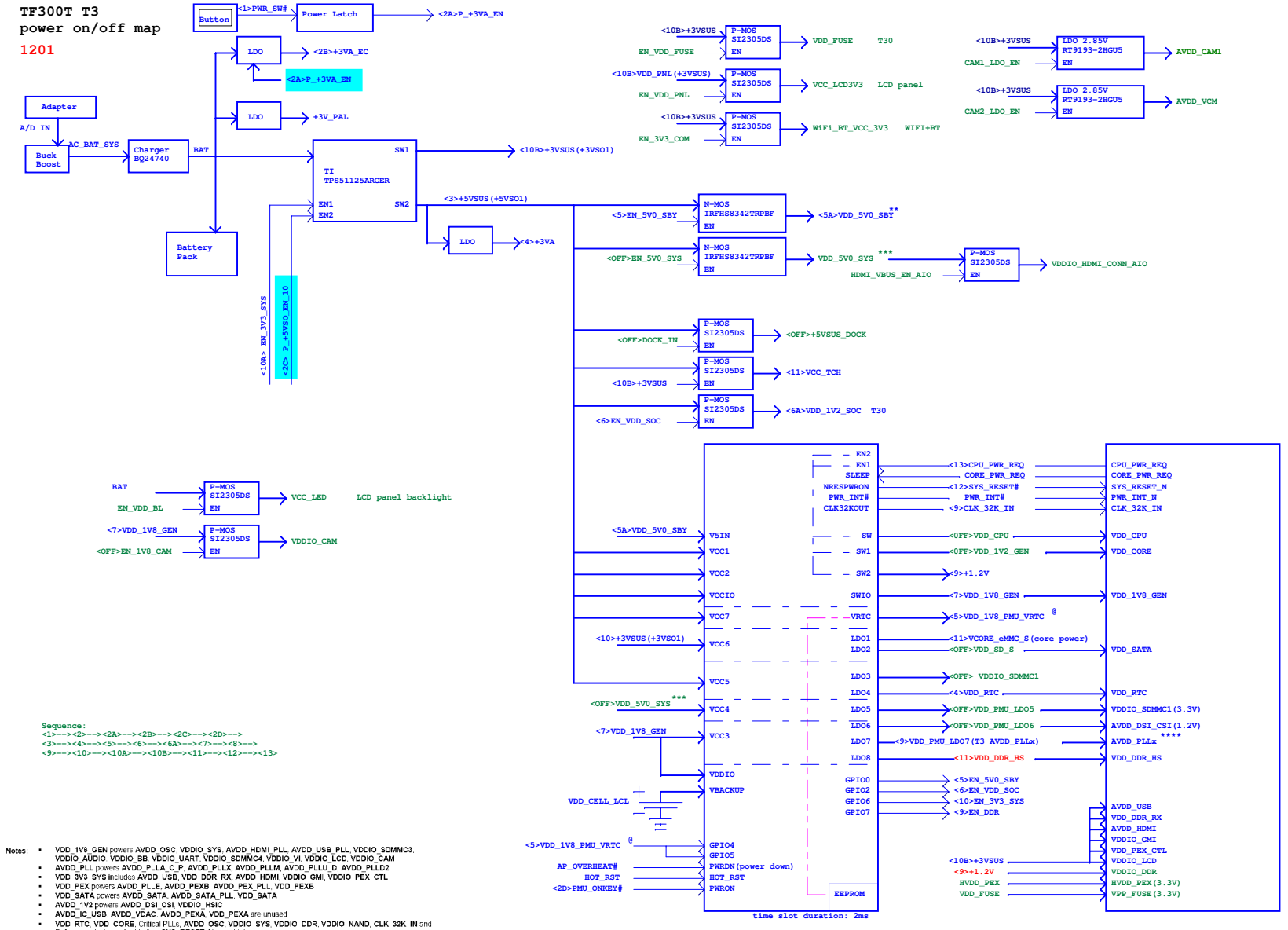
TF300T_T3
Power On/Off



ASUSTeK COMPUTER INC. EPAD
Title : Timing
Engineer: Richard Lin
Size: Custom
Project Name: ME370T
Rev: 2.0
Date: Thursday, March 01, 2012
Sheet 3 of 60

TF300T T3
power on/off map

1201



Sequence:
<1>--><2>--><2A>--><2B>--><2C>--><2D>-->
<3>--><4>--><5>--><6>--><6A>--><7>--><8>-->
<9>--><10>--><10A>--><10B>--><11>--><12>--><13>

Notes:

- VDD_1V8_GEN powers AVDD_OSC, VDDIO_SYS, AVDD_HDMI_PLL, AVDD_USB_PLL, VDDIO_SDMMC3, VDDIO_AUDIO, VDDIO_BB, VDDIO_UART, VDDIO_SDMMC4, VDDIO_VI, VDDIO_LCD, VDDIO_CAM
- AVDD_PLL powers AVDD_PLLA_C_P, AVDD_PLLX, AVDD_PLLM, AVDD_PLLU_D, AVDD_PLLD2
- VDD_3V3_SYS includes AVDD_USB, VDD_DDR_RX, AVDD_HDMI, VDDIO_GMI, VDDIO_PEX_CTL
- VDD_PEX powers AVDD_PLLE, AVDD_PEXB, AVDD_PEX_PLL, VDD_PEXB
- VDD_SATA powers AVDD_SATA, AVDD_SATA_PLL, VDD_SATA
- AVDD_1V2 powers AVDD_DSI_CSI, VDDIO_HSIC
- AVDD_IC_USB, AVDD_VDAC, AVDD_PEXA, VDD_PEXA are unused
- VDD_RTC, VDD_CORE, Critical PLLs, AVDD_OSC, VDDIO_SYS, VDDIO_DDR, VDDIO_NAND, CLK_32K_IN and Reference clock required before SYS_RESET_N goes high
- Recommended Power-down sequence is reverse of Power-up.

BOM需修改為 02004-00120000 C.S T30-R-A3 FCBGA-728

0620

1.2V — VDD_PMU_LDO4_1V2 — MAX77663 LDO4 — VDD_RTC

0.9~1.0V — VDD_1V0_GEN — MAX77663 SD0(6A) — VDD_CPU

1.0~1.2V — VDD_1V2_SOC — MAX77663 SD1(3A) — VDD_CORE

0622

+3VSUS_CPU — R1 0R2J /@ (Unmount) — VDD_FUSE

U1 NCT3521U N/A (IN, OUT, GND, DIS, EN)

0720

VDD_FUSE_DISABLE — R2 300R1F N/A

C24 0.1U6.3VX5RC1K N/A

VDDIO_UART — R3 100KR1J /@ (Unmount)

10 EN_VDD_FUSE

R4 100KR1J N/A

0720 default disable FUSE function

U2A — 1/22 CORE POWER — T30L-R-P-A3 T30

1.2V (1.0 ~ 1.2V)

VDD_RTC_0001, VDD_RTC_0002 — V22, V23 — VDD_RTC

0.9~1.0V (0.9 ~ 1.0V)

VDD_CPU_01 … VDD_CPU_22 — H10, J10, J8, K8, K9, M7, M8, M9, N8, N9, P14, P15, P16, P17, R14, R17, T14, T17, U14, U15, U16, U17 — VDD_CPU

1.0~1.2V (1.0 ~ 1.2V)

VDD_CORE_01 … VDD_CORE_28 — M13, M15, M17, M19, N12, N14, N16, N18, N7, P13, P19, R12, R18, R7, R8, R9, T13, T19, T8, T9, U18, V13, V15, V17, V19, W14, W16, W18 — VDD_CORE

VDD_CPU_SENSE — AB12 — VDD_CPU_SENSE_T30

GND_CPU_SENSE — AB15 — GND_CPU_SENSE_T30

VVDD_CPU_SENSE — AB16

VGND_CORE_SENSE — AA23

VDD_CORE_SENSE — W23 — VDD_CORE_SENSE_T30

GND_CORE_SENSE — W22 — GND_CORE_SENSE_T30

(3.3V) VPP_FUSE — AB8

(3.3V) VPP_KFUSE — AA4 — VPP_KFUSE

R5 10KR1J N/A

R6 1KR1J /@ (Unmount)

VDD_FUSE — C30 0.1U6.3VX5RC1K N/A

VDD_RTC — C1 N/A 0.1U6.3VX5RC1K

VDD_CPU — C2 N/A 0.1U6.3VX5RC1K; C4 N/A 0.1U6.3VX5RC1K; C6 N/A 0.1U6.3VX5RC1K; C8 N/A 4.7U6.3VX5RC2M; C7 N/A 4.7U6.3VX5RC2M; C3 N/A 4.7U6.3VX5RC2M; C10 N/A 4.7U6.3VX5RC2M; C13 N/A 4.7U6.3VX5RC2M

0906 NV add

VDD_CPU — C5 N/A 4.7U6.3VX5RC2M; C29 /@ 4.7U6.3VX5RC2M; C9 N/A 4.7U6.3VX5RC2M; C11 N/A 8P25VNPOC1J

1220 add

VDD_CORE — C14 N/A 22U6.3VX5RC5M; C17 N/A 22U6.3VX5RC5M

VDD_CORE — C15 N/A 0.1U6.3VX5RC1K; C12 N/A 0.1U6.3VX5RC1K; C20 N/A 0.1U6.3VX5RC1K; C22 N/A 4.7U6.3VX5RC2M; C18 N/A 4.7U6.3VX5RC2M; C26 N/A 4.7U6.3VX5RC2M; C27 N/A 4.7U6.3VX5RC2M; C28 N/A 4.7U6.3VX5RC2M; C25 N/A 33P25VNPOC1J

0906 NV add

VDD_CORE — C16 N/A 4.7U6.3VX5RC2M; C19 N/A 4.7U6.3VX5RC2M; C21 /@ 4.7U6.3VX5RC2M; C23 /@ 0.1U6.3VX5RC1K

0614 remove VDD_CPU_SENSE

Note: Place the 0402 shunts close to Tegra side

VDD_CPU_SENSE_T30 — PJP1 SHORT_PIN /@ — VDD_CPU_SENSE — VDD_CPU_SENSE 51

GND_CPU_SENSE_T30 — PJP2 SHORT_PIN /@ — GND_CPU_SENSE — GND_CPU_SENSE 51

MAX77663 SD0 sense

Short Copper

VDD_CORE_SENSE_T30 — PJP3 SHORT_PIN /@ — VDD_CORE_SENSE — VDD_CORE_SENSE 51

GND_CORE_SENSE_T30 — PJP4 SHORT_PIN /@ — GND_CORE_SENSE — GND_CORE_SENSE 51

MAX77663 SD1 sense

Short Copper

Title	T30 Core & Fuse
ASUSTeK COMPUTER INC. EPAD	Engineer: Richard Lin
Size	C
Project Name	ME370T
Rev	2.0
Date:	Saturday, March 24, 2012
Sheet	5 of 60

Power from MAX77663

MAX77663 LDO8 1.2V to T30 AVDD_PLLx

MAX77663 SD2 1.8V (VDD_1V8_PMU_DCDC2) to VDD_1V8_GEN

Signal to & from MAX77663

SYS_RESET# from MAX77663 nRSTIO, check reset circuit(p.32) and PMU side

PWR_INT# from MAX77663 nIRQ, check PU resister in PMU side(100k PU to VDD_1V8_GEN)

CORE_PWR_REQ to MAX77663 EN1, check PU resister in PMU side(100k PU to VDD_1V8_GEN)

CPU_PWR_REQ to MAX77663 EN2, check PD resister in PMU side(100k PD)

CLK_32K_IN from MAX77663 GPIO4, check PU resister in PMU side(100k PU to VDD_1V8_GEN)

1.2V VDD_PMU_LDO8_1V2 — MAX77663 LDO8 — VDD_PMU_LDO8_1V2_CPU

1.2V VDD_PMU_LDO8_1V2_CPU — AVDD_PLLA_P_C

1.2V VDD_PMU_LDO8_1V2_CPU — AVDD_PLLU_D

1.2V Remove AVDD_PLLX

1.2V Remove AVDD_PLLM

1.8V VDD_1V8_GEN — R8 0R0J N/A — VDD_1V8_GEN_CPU

MAX77663 SD2 (2A)
VDD_1V8_PMU_DCDC2

1.8V VDD_1V8_GEN_CPU — VDDIO_SYS

1.8V VDD_1V8_GEN_CPU — L7 600 30Ohm/100Mhz — AVDD_OSC

0906 NV change

PMU	VDD_PMU_LDO7
R1.0	1.1V
R1.2	1.2V

AVDD_OSC: C31 4.7U6.3VX5RC2M N/A
AVDD_PLLA_P_C: C34 0.1U6.3VX5RC1K N/A
AVDD_PLLU_D: C37 0.1U6.3VX5RC1K N/A
VDDIO_SYS: C38 0.1U6.3VX5RC1K N/A

Remove C35, C36 for AVDD_PLLX & AVDD_PLLM

PJ1 /@ SHORT_PIN — Short Copper

U2B — 2/22 OSC, PLL & SYS

AVDD_OSC	F30	1.8V AVDD_OSC	
AVDD_PLLA_P_C	H13	1.2V AVDD_PLLA_P_C	AUDIO&PERIPHERAL
	J12	1.2V AVDD_PLLX	CPU
	J13	1.2V AVDD_PLLM	DRAM
AVDD_PLLU_D	AA8	1.2V AVDD_PLLU_D	USB&DSI
	AD7	AVDD_PLLU_D2	
AVDD_PLLE no use	AA22	1.05V AVDD_PLLE	PCIE&SATA
VDDIO_SYS	K29	1.8V VDDIO_SYS_1	
	K30	VDDIO_SYS_2	

XTAL_IN T30 — XTAL_IN
XTAL_OUT T29 — XTAL_OUT — R9 N/A 2MR2J
XTAL_OUT_R — R14 0R1J N/A — Change — X1 N/A 12MHz — Change
C32 12P50VNPOC2J N/A — Change
C33 12P50VNPOC2J N/A
X1 change to 12MHz XTAL
C32 & C33 change to 12pF
TXC/7V12000011
NC37 H12 — remove PLL_SYS_PLL_LF 0721

VDDIO_SYS — R11 1KR1J N/A — R12 1KR1J N/A
1227 R0732 100K -> 10K
VDDIO_SYS — R14 100KR1J N/A — 0229 NV change 10k -> 100k

PWR_I2C_SCL	M24	PWR_I2C_SCL	PWR_I2C_SCL 26,27,49,50
PWR_I2C_SDA	N27	PWR_I2C_SDA	PWR_I2C_SDA 26,27,49,50
SYS_RESET_N	N28	SYS_RESET#	SYS_RESET# 20,32,50
			Unmount R16 1KR1J N/A — JTAG_TRST#
PWR_INT_N	M22	PWR_INT#	PWR_INT# 50
CORE_PWR_REQ	N25	CORE_PWR_REQ	CORE_PWR_REQ 14,50
CPU_PWR_REQ	R24	CPU_PWR_REQ	CPU_PWR_REQ 50
SYS_CLK_REQ	T23		
CLK_32K_IN	R22	CLK_32K_IN	CLK_32K_IN 50
CLK_32K_OUT	U27	CLK_32K_OUT	46,47,48

R15 100KR1J N/A
CPU_PWR_REQ PD 100k in KAI design

KB_COL00	J30	KB_COL0	PWR_SW#_BUTTON_R 33
KB_COL01	N26	KB_COL1	
KB_COL02	V25	KB_COL2	VOL_UP_BUTTON 32
KB_COL03	R26	KB_COL3	VOL_DWN_BUTTON 32
KB_COL04	W26	PCB_ID2	SNN_KB_COL4
KB_COL05	R30	PCB_ID5	SNN_KB_COL5
KB_COL06	P27		SNN_KB_COL6
KB_COL07	N29	PCB_ID3	SNN_KB_COL7

0802 ID5

KB_ROW00	T26	KB_ROW0	KB_ROW0 32,33
KB_ROW01	M23	KB_ROW1	
KB_ROW02	V27	KB_ROW2	PCB_ID4
KB_ROW03	M28	SNN_KB_ROW3	NFC_GPIO4_R 44
KB_ROW04	N24	PCB_ID0	SNN_CAM_I2C_SEL0
KB_ROW05	N30	PCB_ID1	SNN_CAM_I2C_SEL1
KB_ROW06	T24	CAM1_LDO_EN	CAM1_LDO_EN 31
KB_ROW07	T25	NC	CAM2_LDO_EN
KB_ROW08	R27	CAM2_LDO_EN	CAM3_LDO_EN
KB_ROW09	M26		SNN_CAM1_AF_PWDN* SMB347_USB51HC 33
KB_ROW10	P25		SNN_CAM2_AF_PWDN* SMB347_SUSP 33
KB_ROW11	M27		CAM3_AF_PWDN* TEMP_ALERT# KAI 26
KB_ROW12	N23	LL_BAT_T30	SNN_KB_ROW12 LL_BAT_T30 33
KB_ROW13	V28		SNN_KB_ROW13
KB_ROW14	M25	1V8_O_LID#	SNN_KB_ROW14 1V8_O_LID# 25
KB_ROW15	V26		SNN_KB_ROW15 NFC_VEN 44

ROW10, 11 for charger control
TEMP_ALERT# KAI form Thermal Sensor

JTAG_TCK	T27	JTAG_TCK	JTAG_TCK 24
JTAG_TDI	R29	JTAG_TDI	JTAG_TDI 24
JTAG_TDO	T28	JTAG_TDO	JTAG_TDO 24
JTAG_TMS	R23	JTAG_TMS	JTAG_TMS 24
JTAG_TRST_N	T22	JTAG_TRT_N	JTAG_TRST# 24
JTAG_RTCK	V24	JTAG_RTCK	JTAG_RTCK 24

R21 0R1J @ Unmount

THERM_DN	M30	THERMD_N	THERMD_N 26
THERM_DP	M29	THERMD_P	THERMD_P 26
OWR	N22		
HDMI_CEC	AC18		
TEST_MODE_EN	R28	TEST_MODE_EN	R26 0R1J N/A

JTAG_TRT_N — R24 100KR1J N/A

<Value> T30L-R-P-A3 N/A

VDDIO_SYS	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
COL0	UP 100K	PU	Config.	Reset
COL1	UP 100K	PU	Config.	Reset
COL2	UP 100K	PU	Config.	Reset
COL3	UP 100K	PU	Config.	Reset
COL4	UP 100K	PU	Config.	Reset
COL5	UP 100K	PU	Config.	Reset
COL6	UP 100K	PU	Config.	Reset
COL7	UP 100K	PU	Config.	Reset
ROW0	DOWN 100K	PD	Config.	Reset
ROW1	DOWN 100K	PD	Config.	Reset
ROW2	DOWN 100K	PD	Config.	Reset
ROW3	DOWN 100K	PD	Config.	Reset
ROW4	DOWN 100K	PD	Config.	Reset
ROW5	DOWN 100K	PD	Config.	Reset
ROW6	DOWN 50K	PD	Config.	Reset
ROW7	DOWN 50K	PD	Config.	Reset
ROW8	DOWN 50K	PD	Config.	Reset
ROW9	DOWN 50K	PD	Config.	Reset
ROW10	DOWN 50K	PD	Config.	Reset
ROW11	DOWN 50K	PD	Config.	Reset
ROW12	DOWN 50K	PD	Config.	Reset
ROW13	DOWN 50K	PD	Config.	Reset
ROW14	DOWN 50K	PD	Config.	Reset
ROW15	DOWN 50K	PD	Config.	Reset

PCBID
ID5 ID4 ID3
0 0 0 for ME370T SR3

PCBID
ID2 = 0 for BCM47511
ID2 = 1 for BCM4751

PCBID
ID1 ID0

Pin to Pin	0 0	AW-NH660	BCM4330
	1 0	AW-NH665	BCM4330

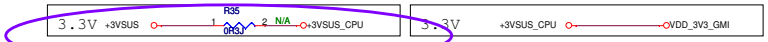
VDD_1V8_GEN_CPU

PCB_ID0	R18	@/PCBID/WIFI	Unmount
	R17	/PCBID/WIFI	
PCB_ID1	R19	/PCBID/WIFI	Unmount
	R20	@/PCBID/WIFI	
PCB_ID2	R22	/PCBID/GPS	Unmount
	R27	@/PCBID/GPS	
PCB_ID3	R23	@/PCBID/PROJECT	Unmount
	R25	/PCBID/PROJECT	
PCB_ID4	R31	@/PCBID/PROJECT	Unmount
	R28	/PCBID/PROJECT	
PCB_ID5	R30	@/PCBID/PROJECT	Unmount
	R29	/PCBID/PROJECT	

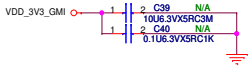
All: 100KR1J 2 1

ASUSTeK COMPUTER INC. EPAD	Engineer: Richard Lin				
Size C	Project Name ME370T			Rev 2.0	
Date: Thursday, March 22, 2012	Sheet 6 of 60				

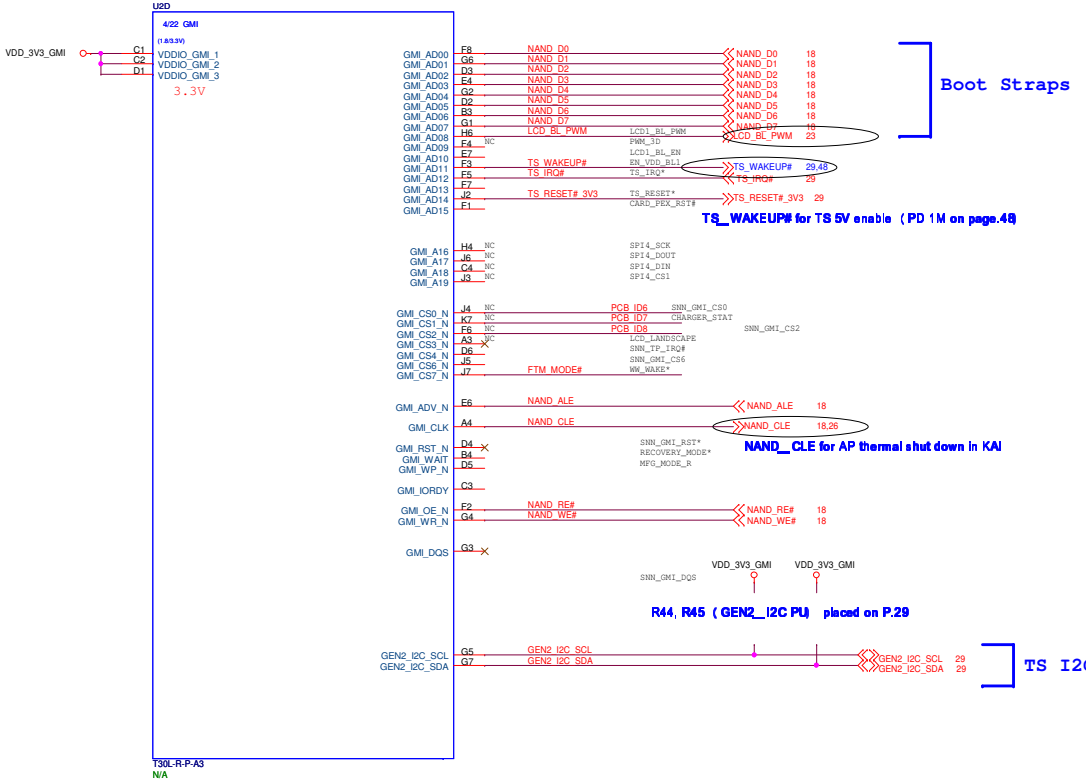
Title : 01.Block Diagram



TPS63020 buck-boost



VDDIO_GMI	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
AD00	None	Z	Disable	Reset
AD01	None	Z	Disable	Reset
AD02	None	Z	Disable	Reset
AD03	None	Z	Disable	Reset
AD04	None	Z	Disable	Reset
AD05	None	Z	Disable	Reset
AD06	None	Z	Disable	Reset
AD07	None	Z	Disable	Reset
AD08	None	Z	Disable	Reset
AD09	None	Z	Disable	Reset
AD10	DOWN 100K	PD	Disable	Reset
AD11	DOWN 100K	PD	Disable	Reset
AD12	None	Z	Disable	Reset
AD13	None	Z	Disable	Reset
AD14	None	Z	Disable	Reset
AD15	None	Z	Disable	Reset
A16	None	Z	Config.	Hold
A17	None	Z	Config.	Hold
A18	None	Z	Config.	Hold
A19	None	Z	Config.	Hold
CS0	UP 100K	PU	Config.	Reset
CS1	UP 100K	PU	Config.	Reset
CS2	UP 100K	1	Disable	Reset
CS3	UP 100K	1	Disable	Reset
CS4	UP 100K	PU	Config.	Reset
CS6	UP 100K	PU	Disable	Reset
CS7	UP 100K	PU	Config.	Reset
ADV_N	None	1	Disable	Reset
CLK	None	0	Disable	Reset
RST_N	UP 100K	0	Disable	Reset
WAIT	UP 100K	PU	Disable	Reset
WP_N	UP 100K	PU	Config.	Reset
IORDY	UP 100K	PU	Config.	Reset
OE_N	None	1	Disable	Reset
WR_N	None	1	Disable	Reset
DQS	None	Z	Disable	Reset



Boot Straps

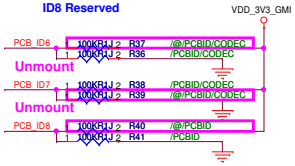
TS_WAKEUP# for TS 5V enable (PD 1M on page.48)

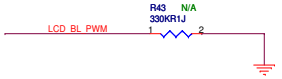
R44, R45 (GEN2_I2C PU) placed on P.29

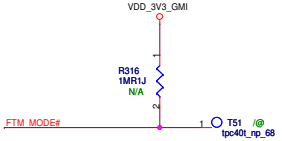
TS I2C

PCBID
ID7 ID6
0 0 ALC5631Q
0 1 WM8903
1 0 ALC5642
1 1 Reserved

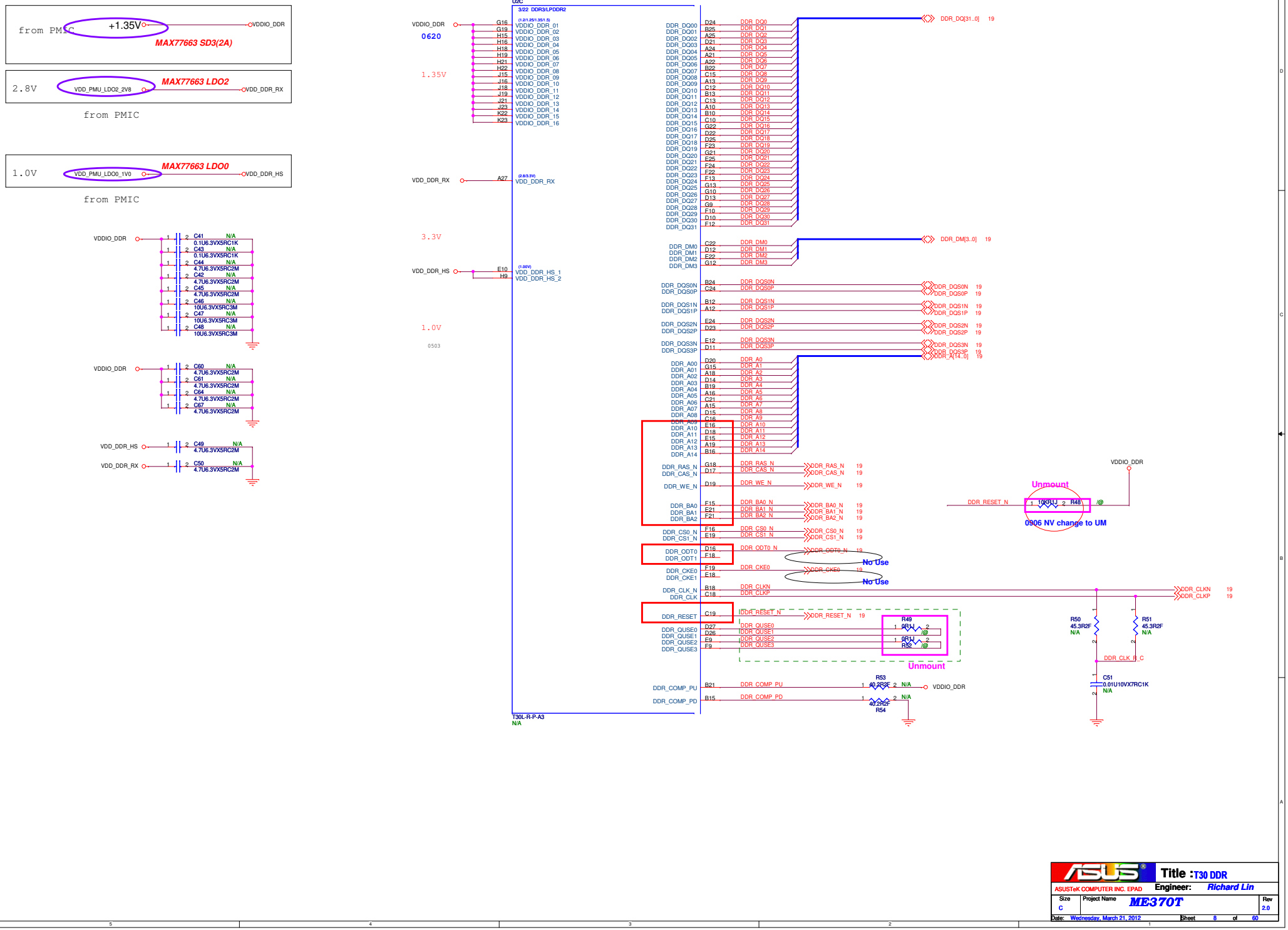
PCBID
ID8 Reserved

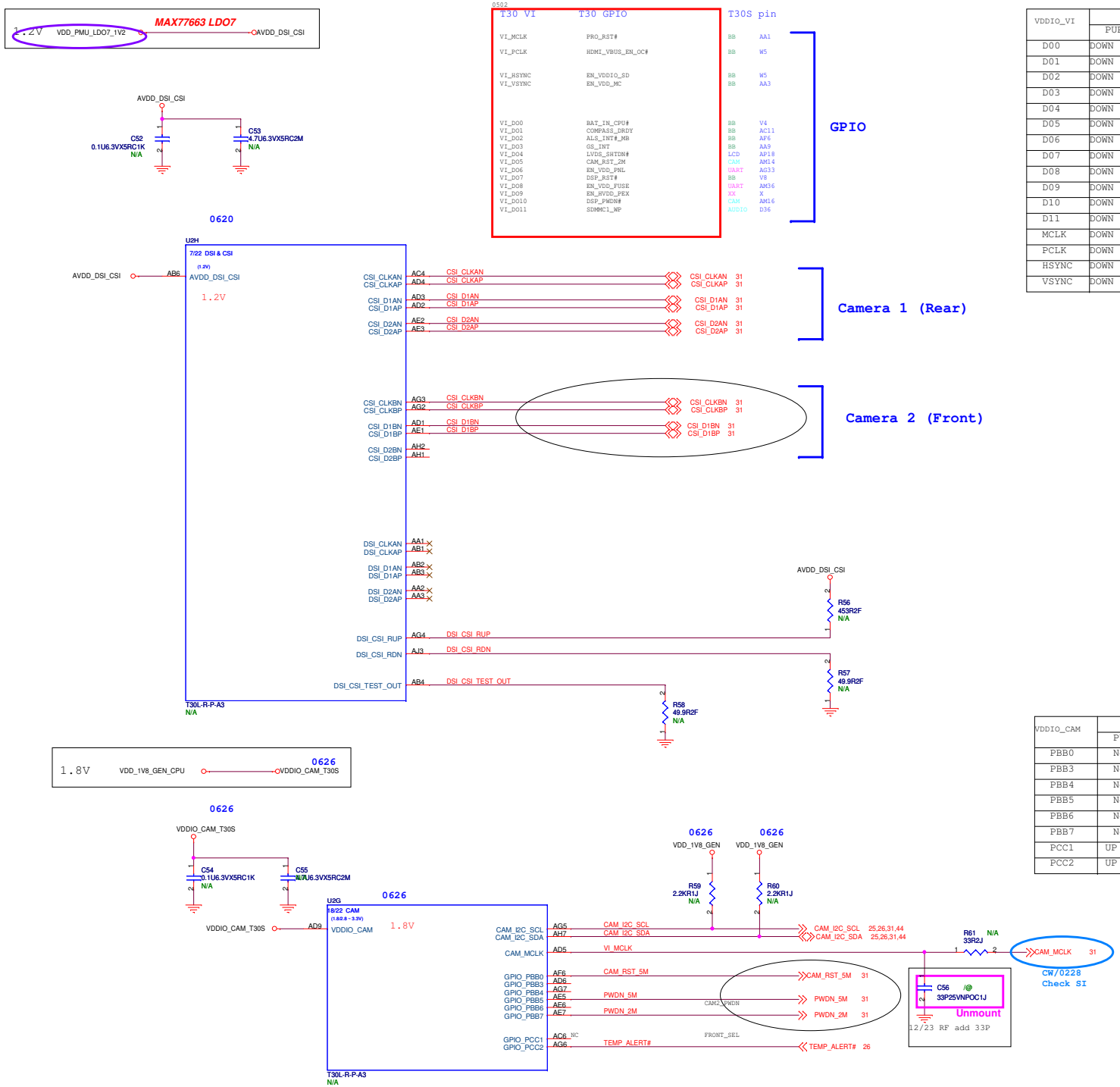






ASUSTeK COMPUTER INC. EPAD	Title : T30 GMI IF		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Wednesday, March 21, 2012	Sheet 7 of 60		


from PMIC
+1.35V
VDDIO_DDR
MAX77663 SD3(2A)
2.8V
VDD_PMU_LDO2_2V8
MAX77663 LDO2
VDD_DDR_RX
from PMIC
1.0V
VDD_PMU_LDO0_1V0
MAX77663 LDO0
VDD_DDR_HS
from PMIC
U2C
3/22 DDR3/LPDDR2
T30L-R-P-A3
N/A
0620
1.35V
3.3V
1.0V
0503
Unmount
0906 NV change to UM
No Use
No Use
Unmount
Title :T30 DDR
ASUSTeK COMPUTER INC. EPAD
Engineer: Richard Lin
Size C
Project Name ME370T
Rev 2.0
Date: Wednesday, March 21, 2012
Sheet 8 of 60



VDDIO_VI	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
D00	DOWN 15K	PD	Disable	Hold
D01	DOWN 15K	PD	Disable	Hold
D02	DOWN 15K	PD	Disable	Hold
D03	DOWN 15K	PD	Config.	Hold
D04	DOWN 15K	PD	Disable	Hold
D05	DOWN 15K	PD	Disable	Hold
D06	DOWN 15K	PD	Disable	Hold
D07	DOWN 15K	PD	Disable	Hold
D08	DOWN 15K	PD	Disable	Hold
D09	DOWN 15K	PD	Disable	Hold
D10	DOWN 15K	PD	Disable	Hold
D11	DOWN 15K	PD	Disable	Hold
MCLK	DOWN 15K	PD	Disable	Hold
PCLK	DOWN 15K	PD	Disable	Hold
HSYNC	DOWN 15K	PD	Disable	Hold
VSYNC	DOWN 15K	PD	Disable	Hold

VDDIO_CAM	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
PBB0	None	Z	Config.	Hold
PBB3	None	Z	Config.	Hold
PBB4	None	Z	Config.	Hold
PBB5	None	Z	Config.	Hold
PBB6	None	Z	Config.	Hold
PBB7	None	Z	Config.	Hold
PCC1	UP 50K	PU	Config.	Hold
PCC2	UP 50K	PU	Config.	Reset

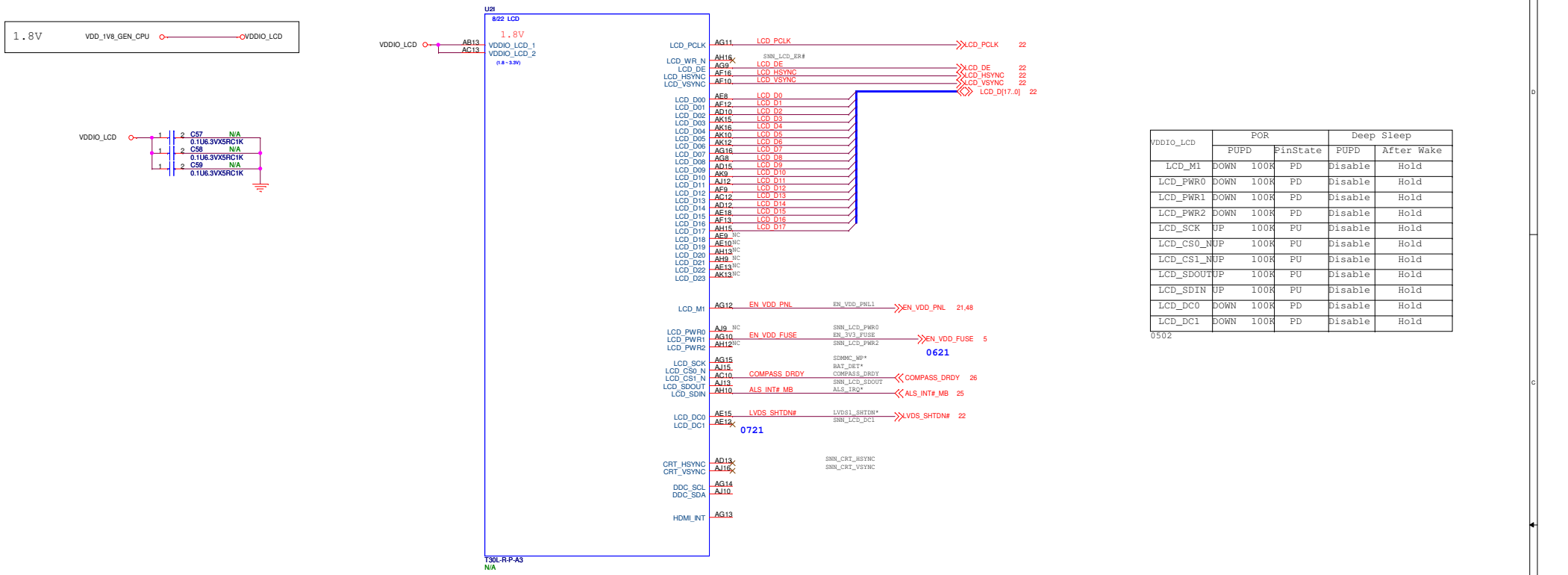
ASUSTeK COMPUTER INC. EPAD

Title : T30 DSI/CSI,CAM

Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

Date: Tuesday, March 20, 2012 Sheet 9 of 60



VDDIO_LCD	POR			Deep Sleep	
	PUPD		PinState	PUPD	After Wake
LCD_M1	DOWN	100K	PD	Disable	Hold
LCD_PWR0	DOWN	100K	PD	Disable	Hold
LCD_PWR1	DOWN	100K	PD	Disable	Hold
LCD_PWR2	DOWN	100K	PD	Disable	Hold
LCD_SCK	UP	100K	PU	Disable	Hold
LCD_CS0_N	UP	100K	PU	Disable	Hold
LCD_CS1_N	UP	100K	PU	Disable	Hold
LCD_SDOUT	UP	100K	PU	Disable	Hold
LCD_SDIN	UP	100K	PU	Disable	Hold
LCD_DC0	DOWN	100K	PD	Disable	Hold
LCD_DC1	DOWN	100K	PD	Disable	Hold

0502

ASUSTeK COMPUTER INC. EPAD

Title : T30 LCD

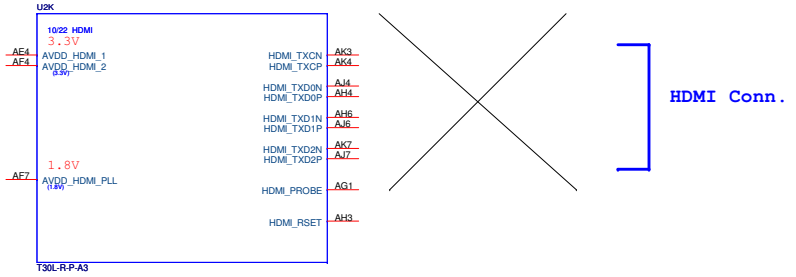
Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

Date: Tuesday, March 20, 2012 Sheet 10 of 60

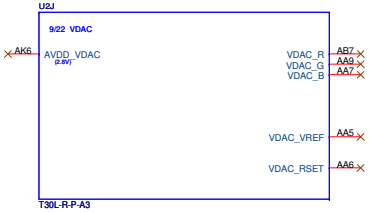
3.3V

1.8V



HDMI Conn.

All HDMI pins & powers leave NC when HDMI is not be used.

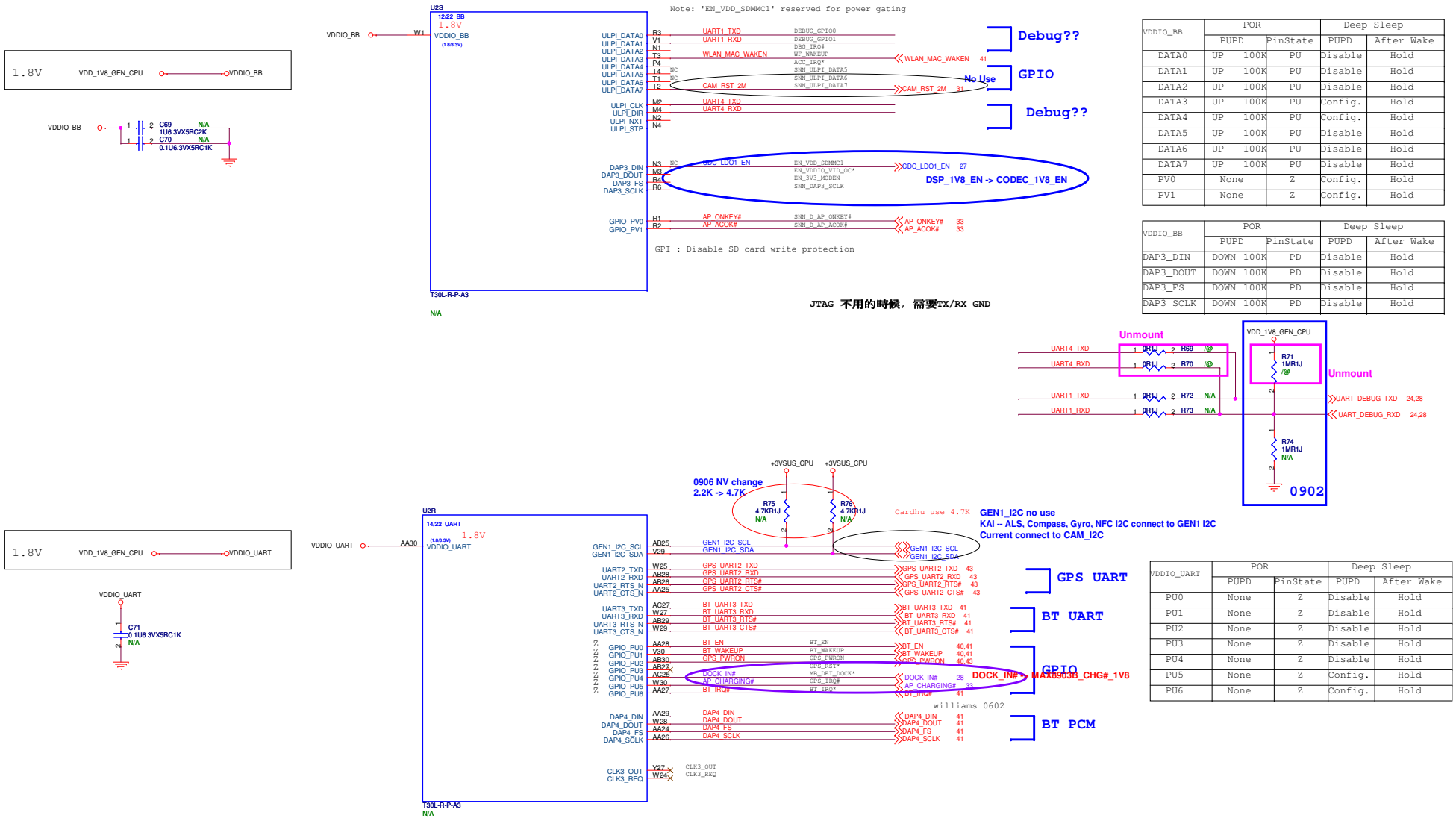


All VDAC pins & powers leave NC

CEC

0818 NC son't support CEC

ASUSTeK COMPUTER INC. EPAD	Title : T30 HDMI,VGA		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Saturday, March 03, 2012	Sheet 11 of 60		

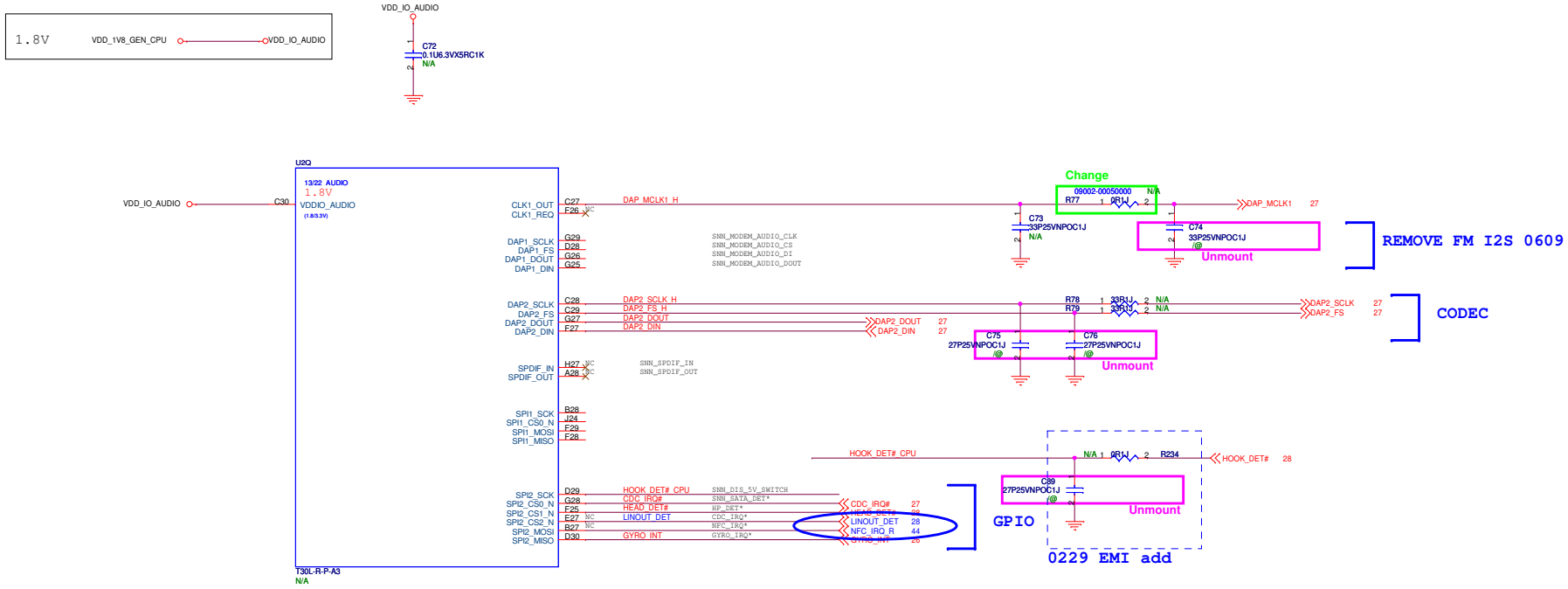


VDDIO_BB	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
DATA0	UP 100K	PU	Disable	Hold
DATA1	UP 100K	PU	Disable	Hold
DATA2	UP 100K	PU	Disable	Hold
DATA3	UP 100K	PU	Config.	Hold
DATA4	UP 100K	PU	Config.	Hold
DATA5	UP 100K	PU	Disable	Hold
DATA6	UP 100K	PU	Disable	Hold
DATA7	UP 100K	PU	Disable	Hold
PV0	None	Z	Config.	Hold
PV1	None	Z	Config.	Hold

VDDIO_BB	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
DAP3_DIN	DOWN 100K	PD	Disable	Hold
DAP3_DOUT	DOWN 100K	PD	Disable	Hold
DAP3_FS	DOWN 100K	PD	Disable	Hold
DAP3_SCLK	DOWN 100K	PD	Disable	Hold

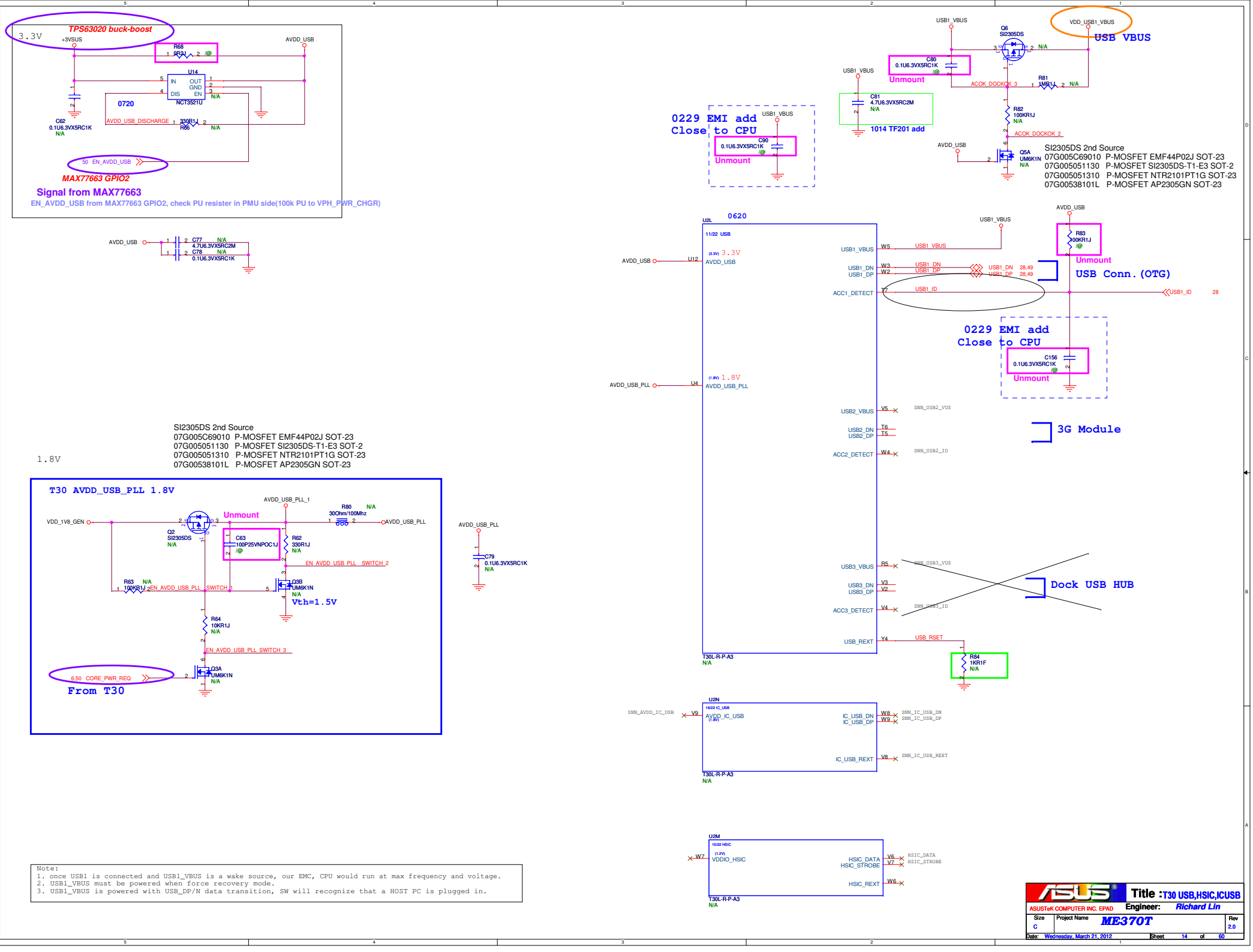
VDDIO_UART	POR		Deep Sleep	
	PUPD	PinState	PUPD	After Wake
PU0	None	Z	Disable	Hold
PU1	None	Z	Disable	Hold
PU2	None	Z	Disable	Hold
PU3	None	Z	Disable	Hold
PU4	None	Z	Disable	Hold
PU5	None	Z	Config.	Hold
PU6	None	Z	Config.	Hold

ASUSTeK COMPUTER INC. EPAD	Title : T30 BB,UART		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 12 of 60		



VDD_IO_AUDIO	POR			Deep Sleep	
	PUPD		PinState	PUPD	After Wake
SPI2_SCK	UP	100K	PU	Disable	Reset
SPI2_CS0_N	UP	100K	PU	Disable	Reset
SPI2_CS1_N	UP	100K	PU	Config.	Hold
SPI2_CS2_N	UP	100K	PU	Config.	Hold
SPI2_MOSI	DOWN	100K	PD	Disable	Hold
SPI2_MISO	DOWN	100K	PD	Disable	Hold

ASUSTeK COMPUTER INC. EPAD	Title : T30 AUDIO		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 13 of 60		


TPS63020 buck-boost
3.3V
+3VSUS
AVDD_USB
R68
0R2J
U14
IN
OUT
GND
DIS
EN
NCT3521U
0720
C62
0.1U6.3V5RC1K
N/A
AVDD_USB_DISCHARGE
330R1J
R86
N/A
50 EN_AVDD_USB
MAX77663 GPIO2
Signal from MAX77663
EN_AVDD_USB from MAX77663 GPIO2, check PU resister in PMU side(100k PU to VPH_PWR_CHGR)
AVDD_USB
C77
4.7U6.3V5RC2M
C78
0.1U6.3V5RC1K
1.8V
SI2305DS 2nd Source
07G005C69010 P-MOSFET EMF44P02J SOT-23
07G005051130 P-MOSFET SI2305DS-T1-E3 SOT-2
07G005051310 P-MOSFET NTR2101PT1G SOT-23
07G00538101L P-MOSFET AP2305GN SOT-23
T30 AVDD_USB_PLL 1.8V
AVDD_USB_PLL_1
R80
30Ohm/100Mhz
VDD_1V8_GEN
AVDD_USB_PLL
Unmount
Q2
SI2305DS
C63
100P25VNPOC1J
R62
330R1J
EN_AVDD_USB_PLL_SWITCH_2
R63
100KR1J
EN_AVDD_USB_PLL_SWITCH_1
Q3B
UM6K1N
Vth=1.5V
R64
10KR1J
EN_AVDD_USB_PLL_SWITCH_3
6,50 CORE_PWR_REQ
Q3A
UM6K1N
From T30
AVDD_USB_PLL
C79
0.1U6.3V5RC1K
USB VBUS
USB1_VBUS
VDD_USB1_VBUS
Q6
SI2305DS
C80
0.1U6.3V5RC1K
Unmount
ACOK_DOCKOK_3
R81
1MR1J
C81
4.7U6.3V5RC2M
1014 TF201 add
R82
100KR1J
ACOK_DOCKOK_2
Q5A
UM6K1N
0229 EMI add
Close to CPU
C90
0.1U6.3V5RC1K
Unmount
SI2305DS 2nd Source
07G005C69010 P-MOSFET EMF44P02J SOT-23
07G005051130 P-MOSFET SI2305DS-T1-E3 SOT-2
07G005051310 P-MOSFET NTR2101PT1G SOT-23
07G00538101L P-MOSFET AP2305GN SOT-23
0620
U2L
11/22 USB
AVDD_USB
U12
3.3V
USB1_VBUS
USB1_DN
USB1_DP
ACC1_DETECT
R83
100KR1J
Unmount
USB Conn.(OTG)
USB1_ID
28
0229 EMI add
Close to CPU
C156
0.1U6.3V5RC1K
Unmount
AVDD_USB_PLL
U4
1.8V
USB2_VBUS
USB2_DN
USB2_DP
ACC2_DETECT
SNN_USB2_VUS
SNN_USB2_ID
3G Module
USB3_VBUS
USB3_DN
USB3_DP
ACC3_DETECT
SNN_USB3_VUS
SNN_USB3_ID
Dock USB HUB
USB_REXT
USB_RSET
R84
1KR1F
T30L-R-P-A3
N/A
U2N
16/22 IC_USB
SNN_AVDD_IC_USB
AVDD_IC_USB
IC_USB_DN
IC_USB_DP
IC_USB_REXT
SNN_IC_USB_DN
SNN_IC_USB_DP
SNN_IC_USB_REXT
U2M
15/22 HSIC
VDDIO_HSIC
HSIC_DATA
HSIC_STROBE
HSIC_REXT
Note:
1. once USB1 is connected and USB1_VBUS is a wake source, our EMC, CPU would run at max frequency and voltage.
2. USB1_VBUS must be powered when force recovery mode.
3. USB1_VBUS is powered with USB_DP/N data transition, SW will recognize that a HOST PC is plugged in.
Title : T30 USB,HSIC,ICUSB
ASUSTeK COMPUTER INC. EPAD
Engineer: Richard Lin
Size C
Project Name ME370T
Rev 2.0
Date: Wednesday, March 21, 2012
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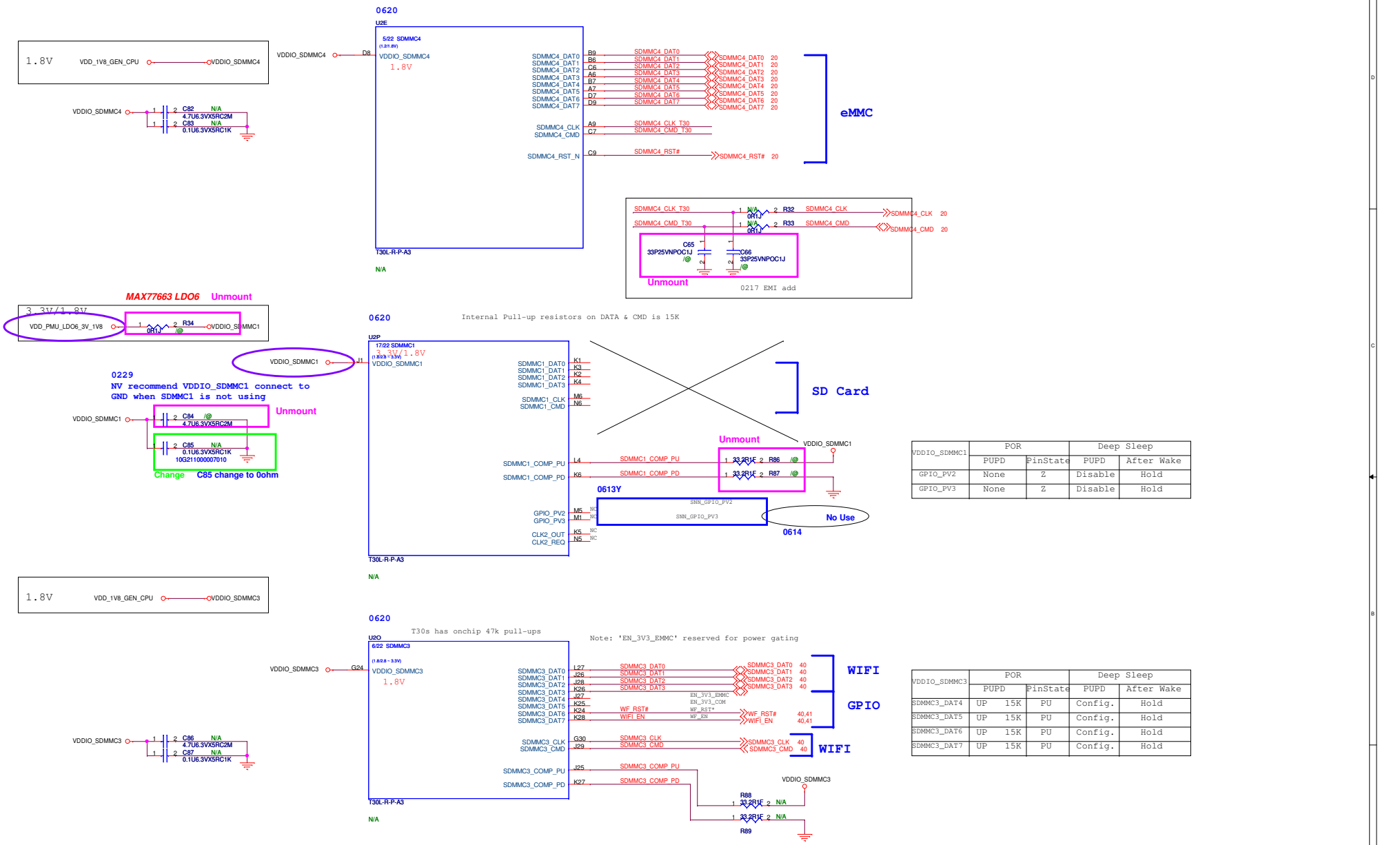
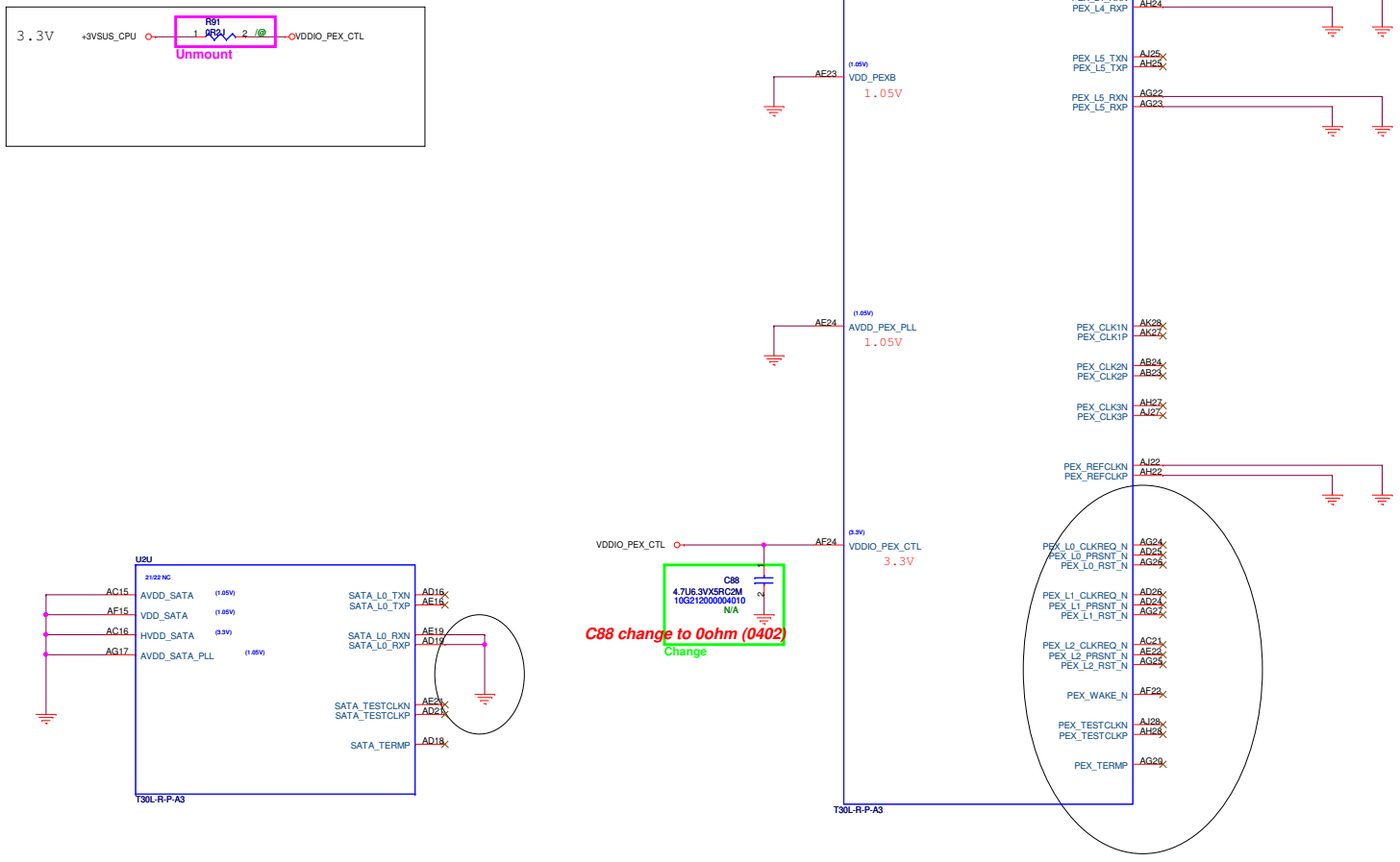
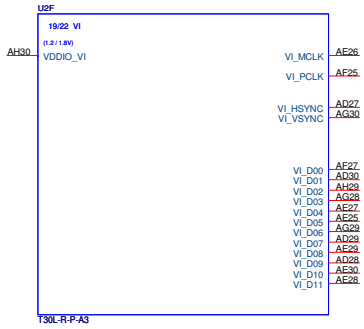
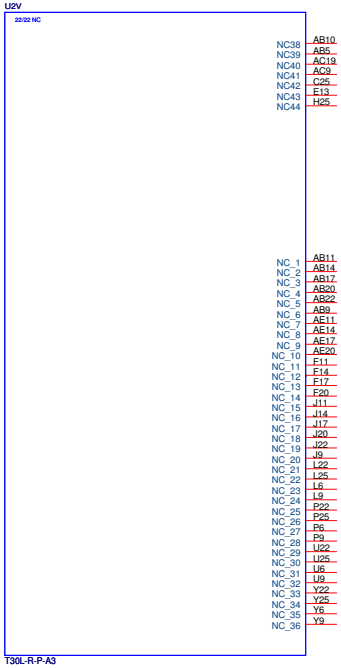


Title	T30 SDMMC,eMMC		
ASUSTeK COMPUTER INC. EPAD	Engineer:	Richard Lin	
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 15 of 60		



ASUSTeK COMPUTER INC. EPAD	Title : T30 PCIe		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Saturday, March 03, 2012	Sheet 16 of 60		





ASUSTeK COMPUTER INC. EPAD

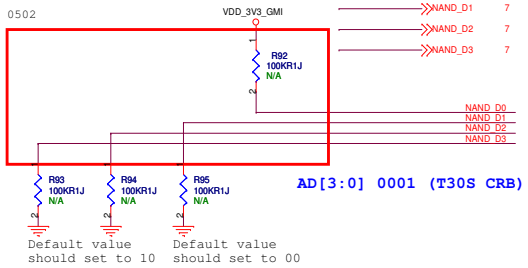
Title : T30 NC

Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

Date: Saturday, March 03, 2012 Sheet 17 of 60

Boot Source:eMMC as default



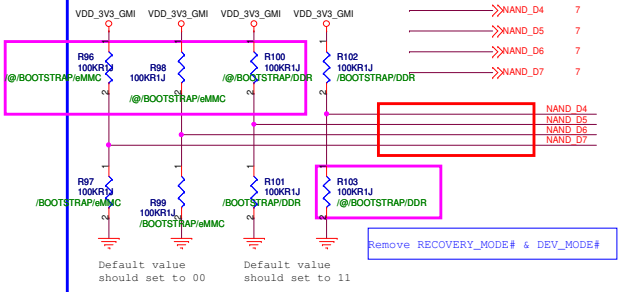
Note:
1. NAND_D[3:0] have internal 100K pull up.

AD3	AD2	AD1	AD0	Determine Boot Device to be config.
0	0	0	0	eMMC primary x4
0	0	0	1	eMMC primary x8
0	0	1	0	eMMC secondary x4
0	0	1	1	NAND
0	1	0	0	NAND w/ block & page offset=1
0	1	0	1	Mobile LBA NAND
0	1	1	0	FlexMuxOneNAND
0	1	1	1	eSD x4
1	0	0	0	SPI Flash
1	0	0	1	SNOR (Muxed, x16)
1	0	1	0	SNOR (Muxed, x32)
1	0	1	1	SNOR (Non-Muxed, x16)
1	1	0	0	MuxOneNAND
1	1	0	1	SATA
1	1	1	0	eMMC secondary x8
1	1	1	1	Use fuse data

YM 0502
DG05576900 V1.3 P75

RAM Code

AD[7:0] 0000 (T30S CRB)



Note:
1. NAND_D[7:4] do NOT have internal 100K pull up.

	AD5	AD4	Select Memory Type	
SKU1&3	0	0	ELPIDA DDR3LRS 256MBx4 EDJ2108EDBG-DJL-F	03006-00030900
SKU2&4	0	1	Hynix DDR3LM 256MBx4 H5TC2G83CFR-H9R	03006-00031200
	1	0	TBD	
	1	1	TBD	

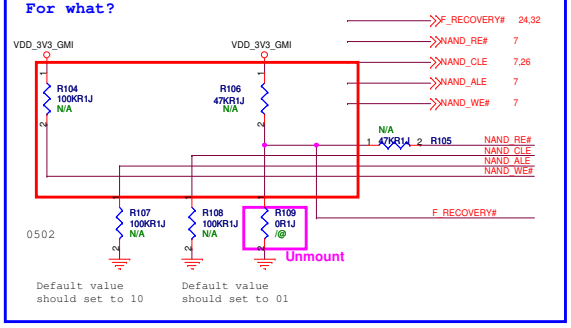
20120302

R100	R101	R102	R103
	V		V
	V	V	
V			V
V		V	

	AD7	AD6	Select eMMC Type	
SKU1&2	0	0	HYNIX 8GB H26M42001FMR FBGA-153	03100-00120000
SKU3&4	0	1	Kingston 8GB KE44B-26BN FBGA169	05G002514010
	1	0	TBD	
	1	1	TBD	

R96	R97	R98	R99
	V		V
	V	V	
V			V
V		V	

For what?



NAND_CLE	NAND_ALE	Description
0	0	Serial JTAG chain, MPCORE and AVP
0	1	MPCore only JTAG
1	0	AVP only JTAG
1	1	Reserved

RECOVERY	Description
0	USB Recovery Mode
1	Boot from secondary device

ASUSTeK COMPUTER INC. EPAD

Title : Boot Straps

Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

Date: Tuesday, March 20, 2012 Sheet 18 of 60

+1.35V from PMIC

MAX77663 SD3(2A)

VDDQ_DDR3L VDD_DDR3L

03006-00030900

ELPIDA DDR3LRS 256MBx4 EDJ2108EDBG-DJL-F

03006-00031200

Hynix DDR3LM 256MBx4 H5TC2G83CFR-H9R

8 DDR_DQ[31..0]

8 DDR_DM[3..0]

8 DDR_A[14..0]

U3 /DDR — 03006-00031200 HYNIX/H5TC2G83CFR-H9R

U4 /DDR — 03006-00031200 HYNIX/H5TC2G83CFR-H9R

U5 /DDR — 03006-00031200 HYNIX/H5TC2G83CFR-H9R

U6 /DDR — 03006-00031200 HYNIX/H5TC2G83CFR-H9R

C91 0.1U6.3VX5RC1K N/A

C92 N/A 0.1U6.3VX5RC1K

C93 N/A 10U6.3VX5RC3M

C94 0.1U6.3VX5RC1K N/A

C95 N/A 0.1U6.3VX5RC1K

C96 N/A 10U6.3VX5RC3M

C97 N/A 0.1U6.3VX5RC1K

C98 N/A 0.1U6.3VX5RC1K

C99 N/A 0.1U6.3VX5RC1K

C100 N/A 0.1U6.3VX5RC1K

C101 N/A 0.1U6.3VX5RC1K

C102 N/A 0.1U6.3VX5RC1K

C103 N/A 0.1U6.3VX5RC1K

C104 N/A 0.1U6.3VX5RC1K

C105 N/A 4.7U6.3VX5RC2M

C106 N/A 4.7U6.3VX5RC2M

C107 N/A 10U6.3VX5RC3M

C108 N/A 10U6.3VX5RC3M

C109 N/A 0.1U6.3VX5RC1K

C110 N/A 0.1U6.3VX5RC1K

C111 N/A 0.1U6.3VX5RC1K

C112 N/A 0.1U6.3VX5RC1K

C113 N/A 0.1U6.3VX5RC1K

C114 N/A 0.1U6.3VX5RC1K

C115 N/A 0.1U6.3VX5RC1K

C116 N/A 0.1U6.3VX5RC1K

C117 N/A 0.1U6.3VX5RC1K

C118 N/A 0.1U6.3VX5RC1K

C119 N/A 0.1U6.3VX5RC1K

C120 N/A 0.1U6.3VX5RC1K

C121 N/A 0.1U6.3VX5RC1K

C122 N/A 0.1U6.3VX5RC1K

C123 N/A 0.1U6.3VX5RC1K

C124 N/A 0.1U6.3VX5RC1K

C125 N/A 4.7U6.3VX5RC2M

C126 N/A 4.7U6.3VX5RC2M

C127 0.1U6.3VX5RC1K N/A

C128 N/A 0.1U6.3VX5RC1K

C129 0.1U6.3VX5RC1K N/A

C130 N/A 0.1U6.3VX5RC1K

C131 0.1U6.3VX5RC1K N/A

C132 0.1U6.3VX5RC1K N/A

R111 243R1F N/A

R112 243R1F N/A

R113 7.5KOhm 1% N/A

R114 7.5KOhm 1% N/A

R115 7.5KOhm 1% N/A

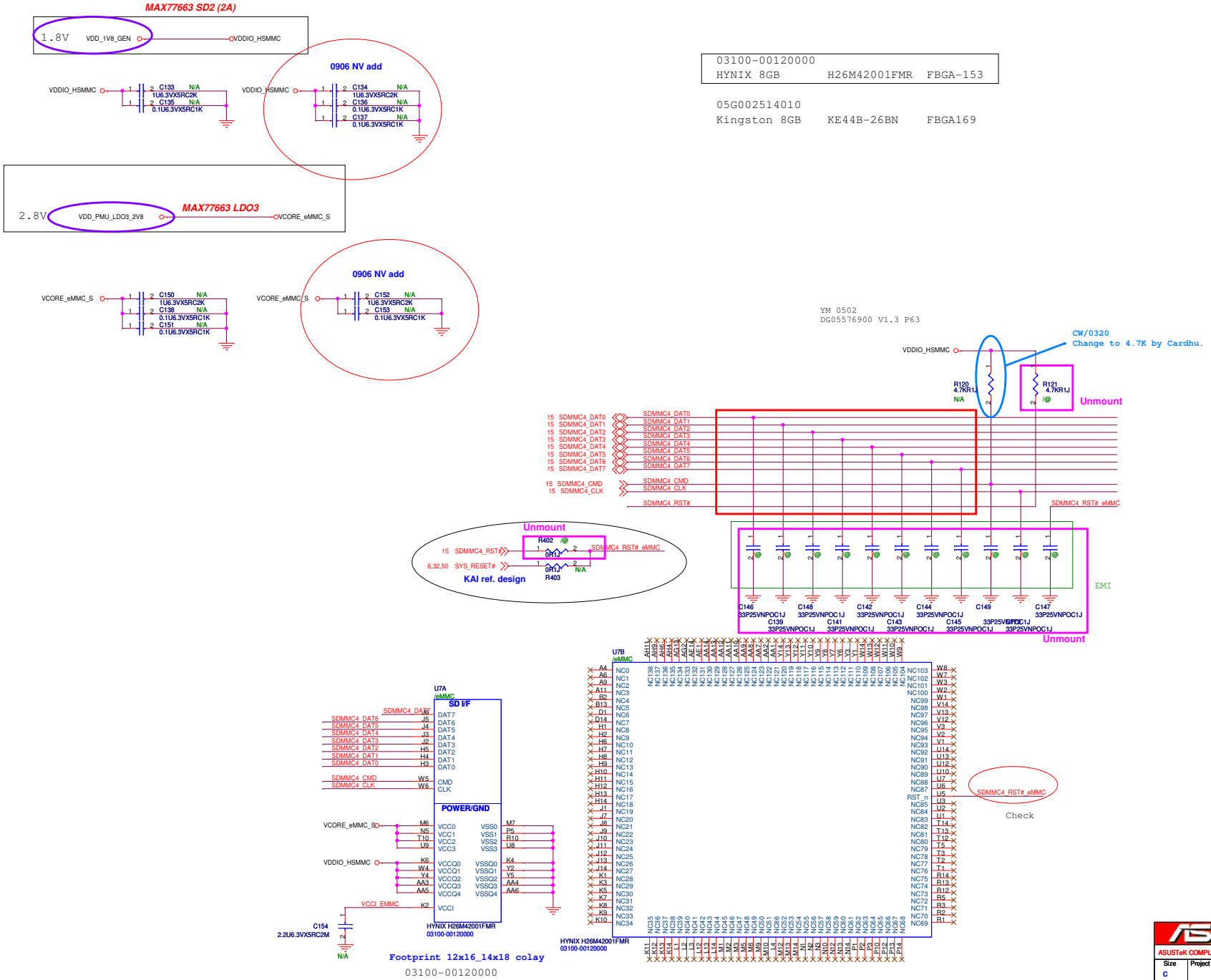
R116 243R1F N/A

R117 243R1F N/A

R118 7.5KOhm 1% N/A

Title : DDR3L	
ASUSTeK COMPUTER INC. EPAD	Engineer: Richard Lin
Size: C	Project Name: ME370T
Rev: 2.0	
Date: Tuesday, March 20, 2012	Sheet 19 of 60

eMMC I/F


MAX77663 SD2 (2A)
1.8V
VDD_1V8_GEN
VDDIO_HSMMC
0906 NV add
VDDIO_HSMMC
C133 N/A 1U6.3VX5RC2K
C135 N/A 0.1U6.3VX5RC1K
C134 N/A 1U6.3VX5RC2K
C136 N/A 0.1U6.3VX5RC1K
C137 N/A 0.1U6.3VX5RC1K
2.8V
VDD_PMU_LDO3_2V8
MAX77663 LDO3
VCORE_eMMC_S
0906 NV add
VCORE_eMMC_S
C150 N/A 1U6.3VX5RC2K
C138 N/A 0.1U6.3VX5RC1K
C151 N/A 0.1U6.3VX5RC1K
C152 N/A 1U6.3VX5RC2K
C153 N/A 0.1U6.3VX5RC1K
03100-00120000
HYNIX 8GB H26M42001FMR FBGA-153
05G002514010
Kingston 8GB KE44B-26BN FBGA169
YM 0502
DG05576900 V1.3 P63
CW/0320
Change to 4.7K by Cardhu.
VDDIO_HSMMC
R120 4.7KR1J N/A
R121 4.7KR1J /@
Unmount
15 SDMMC4_DAT0
15 SDMMC4_DAT1
15 SDMMC4_DAT2
15 SDMMC4_DAT3
15 SDMMC4_DAT4
15 SDMMC4_DAT5
15 SDMMC4_DAT6
15 SDMMC4_DAT7
15 SDMMC4_CMD
15 SDMMC4_CLK
SDMMC4_RST# eMMC
Unmount
15 SDMMC4_RST#
6,32,50 SYS_RESET#
R402 /@ 0R1J
R403 N/A
KAI ref. design
EMI
C146 33P25VNPOC1J
C148 33P25VNPOC1J
C142 33P25VNPOC1J
C144 33P25VNPOC1J
C149
C147 33P25VNPOC1J
C139 33P25VNPOC1J
C141 33P25VNPOC1J
C143 33P25VNPOC1J
C145 33P25VNPOC1J
Unmount
U7A eMMC
SD I/F
DAT7
DAT6
DAT5
DAT4
DAT3
DAT2
DAT1
DAT0
CMD
CLK
POWER/GND
VCC0
VCC1
VCC2
VCC3
VSS0
VSS1
VSS2
VSS3
VCCQ0
VCCQ1
VCCQ2
VCCQ3
VCCQ4
VSSQ0
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VCCI
VCCI_EMMC
VCORE_eMMC_S
VDDIO_HSMMC
C154 2.2U6.3VX5RC2M
N/A
HYNIX H26M42001FMR
03100-00120000
Footprint 12x16_14x18 colay
03100-00120000
U7B eMMC
NC0
NC1
NC2
NC3
NC4
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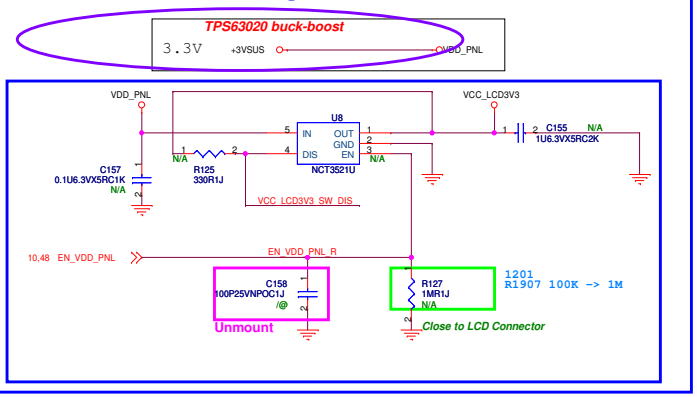
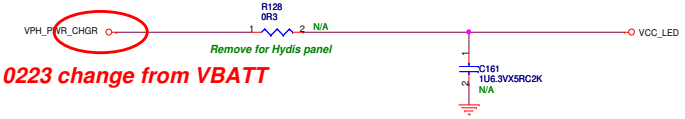
NC85
RST_n
NC87
NC88
NC89
NC90
NC91
NC92
NC93
NC94
NC95
NC96
NC97
NC98
NC99
NC100
NC101
NC102
NC103
SDMMC4_RST# eMMC
Check
HYNIX H26M42001FMR
03100-00120000
ASUSTeK COMPUTER INC. EPAD
Title : eMMC
Engineer: Richard Lin
Size C
Project Name ME370T
Rev 2.0
Date: Tuesday, March 20, 2012
Sheet 20 of 60

LCD PNL power Switch



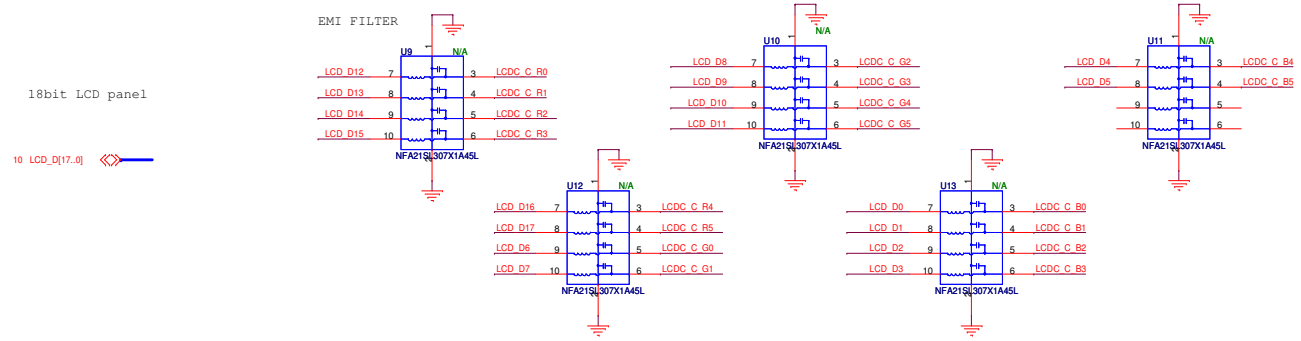
LCD BL power Switch

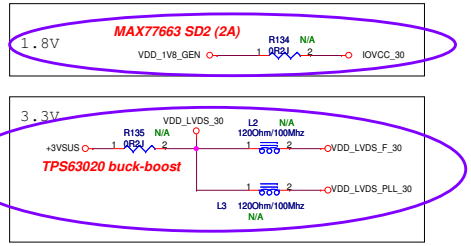
2.8~5.5V

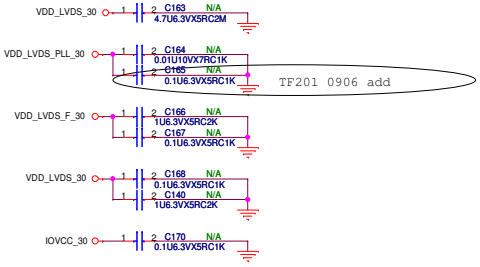


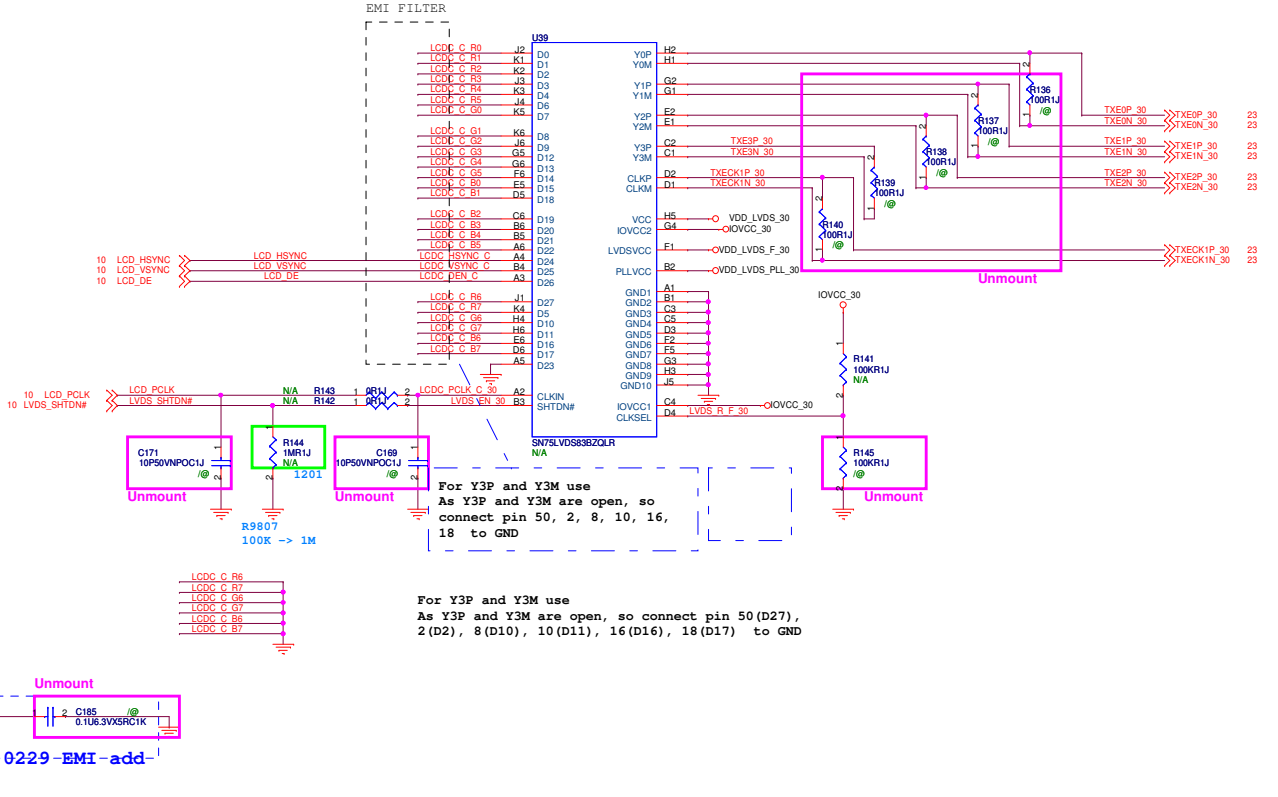
0223 change from VBATT

ASUSTeK COMPUTER INC. EPAD	Title : LCD panel power	
	Engineer: Richard Lin	
Size: C	Project Name: ME370T	Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 21 of 60	









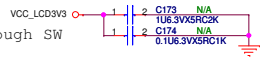
ASUSTeK COMPUTER INC. EPAD	Title : LVDS transmitter_30		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 22 of 60		

LCD PNL power Switch

From +3VSUS

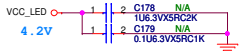
3.3V

From +3VSUS through SW

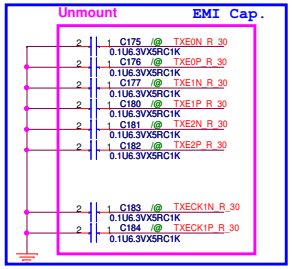


Close to LCD Connector

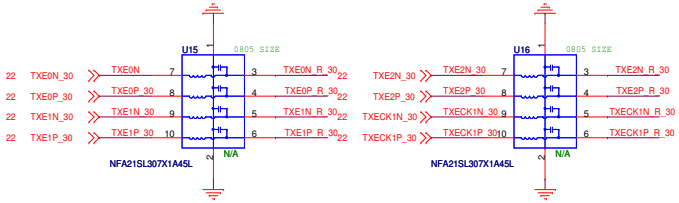
LCD BL power Switch

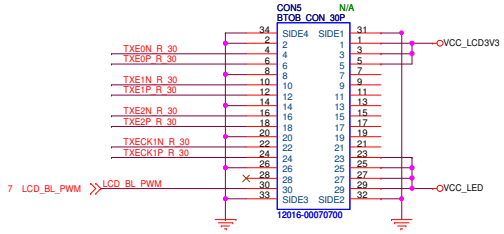


Close to LCD Connector



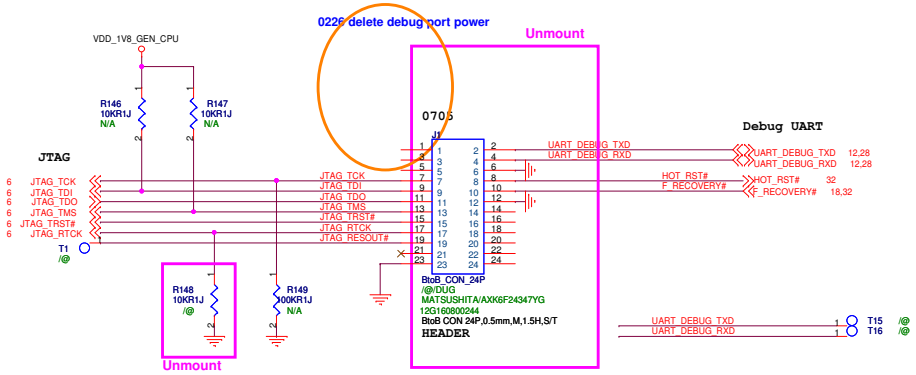
LVDS EMI Filter





CON5 2nd source
MATSUSHITA/AXT530124
12G161H00307

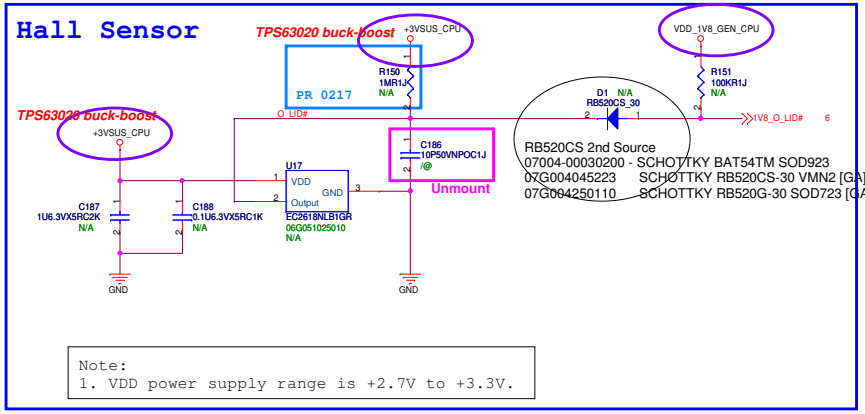
ASUSTeK COMPUTER INC. EPAD	Title : LCD Connector		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 23 of 60		



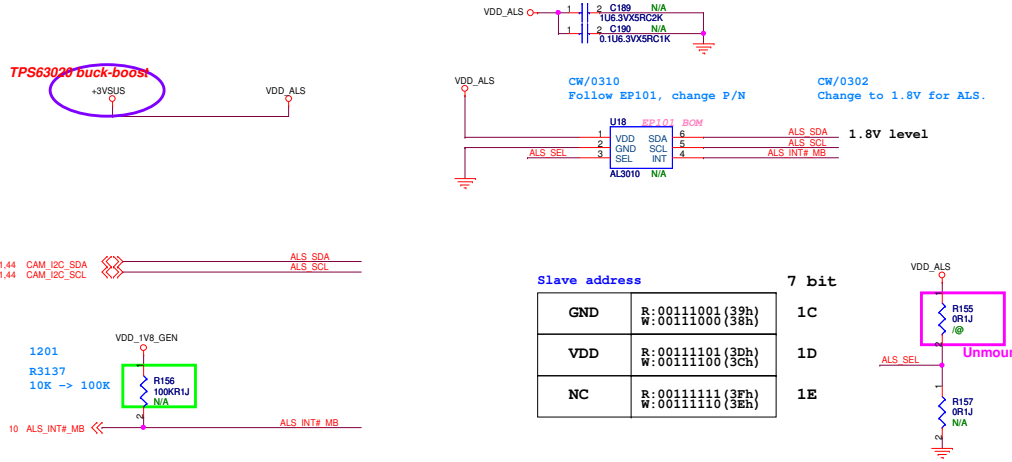
ASUSTeK COMPUTER INC. EPAD	Title : Debug Connector		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 24 of 60		

MAX77663 SD2 (2A)

Hall Sensor



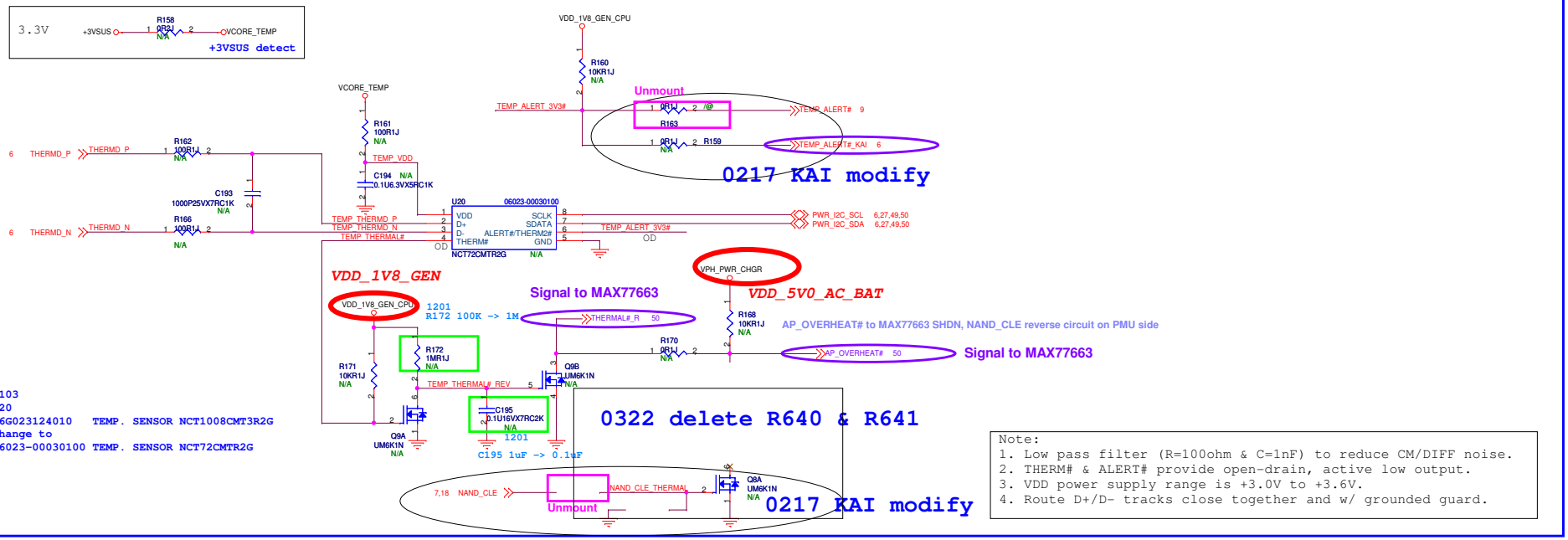
Ambient Light Sensor



Slave address		7 bit
GND	R:00111001(39h) W:00111000(38h)	1C
VDD	R:00111101(3Dh) W:00111100(3Ch)	1D
NC	R:00111111(3Fh) W:00111110(3Eh)	1E

ASUSTeK COMPUTER INC. EPAD	Title : Hall & ALS		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Wednesday, March 21, 2012	Sheet 25 of 60		

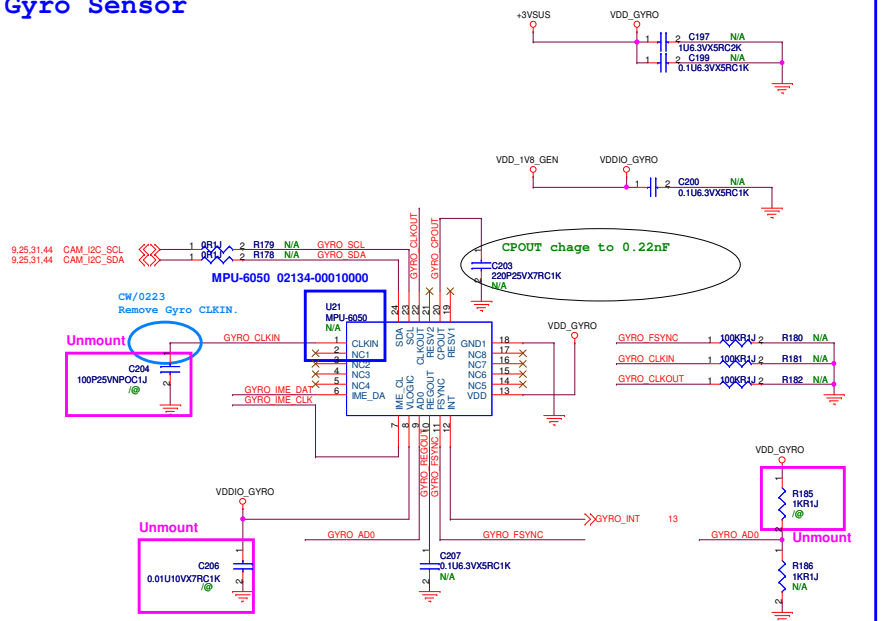
Thermal Sensor 1



1103
U20
06G023124010 TEMP. SENSOR NCT1008CMT3R2G
change to
06023-00030100 TEMP. SENSOR NCT72CMTR2G

Note:
1. Low pass filter (R=100ohm & C=1nF) to reduce CM/DIFF noise.
2. THERM# & ALERT# provide open-drain, active low output.
3. VDD power supply range is +3.0V to +3.6V.
4. Route D+/D- tracks close together and w/ grounded guard.

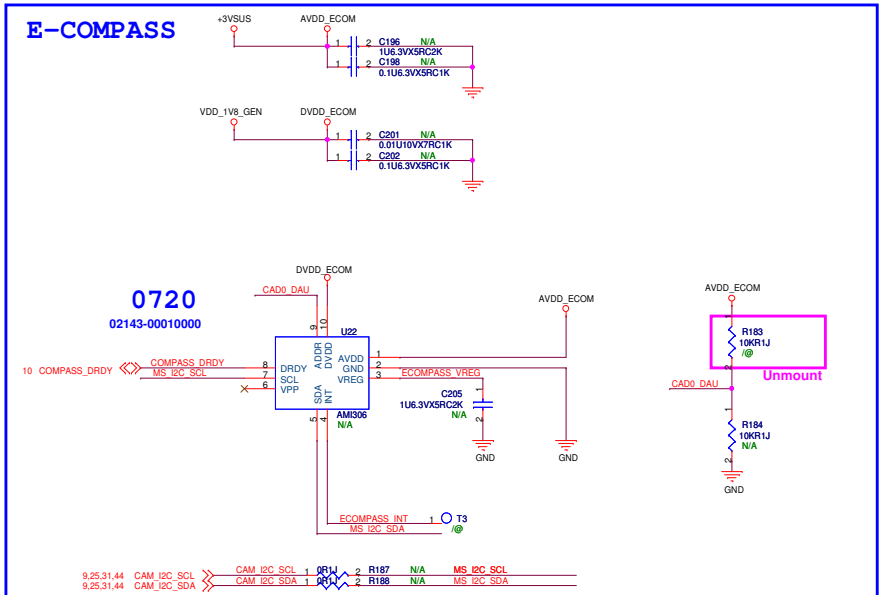
Gyro Sensor



Note:
1. VDD power supply range is +1.8V to +3.6V.
2. VIO max. voltage is VDD.
3. VOH=0.9xVIO & VOL=0.3xVIO.
4. VIH=0.8xVIO & VIL=0.2xVIO

Gyro AD0 High : I2C Address 1101001b
Gyro AD0 Low : I2C Address 1101000b

E-COMPASS



Note:
1. DVDD power supply range is +1.7V to +2.8V.
2. AVDD power supply range is +2.4V to +3.6V.
3. Let VREG & VPP NC for reference.
4. DRDY is +1.8V level out and active high.

ADDR	I2C Address	
H	1Fh/read	1Eh/write
L	1Dh/read	1Ch/write

ASUSTeK COMPUTER INC. EPAD
Title : Sensors
Engineer: Richard Lin
Size C | Project Name ME370T | Rev 2.0
Date: Thursday, March 22, 2012 | Sheet 26 of 60

Codec VDD 1.8V

VDD_1V8_GEN → VDD_1V8_CDC

0226

Codec 1.8V change to system 1.8V power VDD_1V8_GEN

PMU LDO5 change to camera 1.8V

1.8V

VDD_1V8_CDC → R189 N/A 0R2J → VDB_CDC

R190 N/A 0R2J → VCP_CDC

L4 10Ohm/100Mhz N/A → AVDD_CDC_F

AVDD_CDC_F → L5 10Ohm/100Mhz N/A → DACREF_CDC

VDD_1V8_GEN → R193 N/A 0R2J → VDD_1V8_DMIC

VDB_CDC: C208 N/A 2.2U6.3VX5RC2M, C209 N/A 0.1U6.3VX5RC1K → GND

VCP_CDC: C210 N/A 10U6.3VX5RC3M, C211 N/A 0.1U6.3VX5RC1K → GND

AVDD_CDC_F: C213 N/A 10U6.3VX5RC3M, C214 N/A 0.1U6.3VX5RC1K → GND

DACREF_CDC: C215 N/A 10U6.3VX5RC3M, C216 N/A 0.1U6.3VX5RC1K → GND

VDD_5V0_AC_BAT

VPH_PWR_CHGR → L6 80Ohm/100Mhz N/A → VDD_SPK

VPH

VDD_SPK: C217 N/A 10U6.3VX5RC3M, C218 N/A 0.1U6.3VX5RC1K → GND

VDD_MIC_CDC: C219 N/A 2.2U6.3VX5RC2M, C220 N/A 0.1U6.3VX5RC1K → GND

DMIC

Unmount

VDD_1V8_DMIC: C221 /@ 1U6.3VX5RC2K, C222 N/A 0.1U6.3VX5RC1K

Unmount

VDD_1V8_DMIC → R197 10KR1J /@ → DMIC_CS

U23 N/A

1	Ground2	Power(Vdd)	6
2	Left/Right	Data	5
3	Ground2	Clock	4

SPM0423HD4H-WB 04G160008210

R209 10KR1J N/A

C223 33P25VNPOC1J /@

C224 33P25VNPOC1J /@

DMIC_DAT_U23, DMIC_LR_U23

Unmount

CS	Drives data after	High-Z after
High	Rising clock edge	Falling clock edge
Low	Falling clock edge	Rising clock edge

Forte media: 04G160007713

KNOWLES/SPM0423HD4H-WB:04G160008210

DMIC_DAT_U23 → R214 2 0R1J 1 N/A → DMIC_DAT

DMIC_LR_U23 → R213 2 0R1J 1 N/A → DMIC_LR

0229 EMI add

Codec Realtek ALC5642

VDD_1V8_CDC → R313 10KR1J N/A → CDC_LDO1_EN_5642

12 CDC_LDO1_EN → From T30 → R199 0R1J /@ → R198 1MR1J /@ Unmount → GND

VDD_SPK, VDD_MIC_CDC, AVDD_CDC_F → VCORE_CDC, VDB_CDC, VCP_CDC

VCORE_CDC: C225 N/A 2.2U6.3VX5RC2M, C226 N/A 0.1U6.3VX5RC1K → GND

U24 — ALC5642 N/A

AVDD, MICVDD, SPKVDDR, SPKVDDL, DCVDD, DBVDD, CPVDD

C229 N/A 2.2U10VX5RC3K

CPP2, CPN2, CPP1, CPN1

C230 N/A 2.2U10VX5RC3K

CPVPP, CPVEE

C231 N/A 2.2U6.3VX5RC2M

C227 N/A 2.2U6.3VX5RC2M → GND

28 MICBIAS → MICBIAS1

HPO_L, HPO_R, HPOFB → HP_OUT_L, HP_OUT_R → 28

GND

DMIC_DAT → IN1P/DMIC1_DAT

28 MIC1_P, 28 MIC1_N → IN1N/DMIC2_DAT/JD1, IN2P, IN2N/JD2

DACREF_CDC

C228 N/A 4.7U6.3VX5RC2M, C235 N/A 4.7U6.3VX5RC2M → ALC5642_VREF2, ALC5642_VREF1 → DACREF, VREF2, VREF1 → GND

SPO_LP, SPO_LN, SPO_RP, SPO_RN → SPK_OUT_L+, SPK_OUT_L-, SPK_OUT_R+, SPK_OUT_R-

MONOP, MONON → MONOOUTP, MONOOUTN

LOUTR, LOUTL → LINEOUTR, LINEOUTL

GPIO2/DMIC_SCL, GPIO1/IRQ, LDO1_EN → DMIC_LR, CDC_IRQ#, CDC_LDO1_EN_5642 → CDC_IRQ# 13

T30 DAP2

13	DAP_MCLK1	0R1J	N/A	R203	DAP_MCLK1_5642
13	DAP2_SCLK	0R1J	N/A	R204	DAP2_SCLK_5642
13	DAP2_FS	0R1J	N/A	R206	DAP2_FS_5642
13	DAP2_DOUT	0R1J	N/A	R208	DAP2_DOUT_5642
13	DAP2_DIN	0R1J	N/A	R207	DAP2_DIN_5642

MCLK, BCLK1, LRCK1, DACDAT1, ADCDAT1

BCLK2, LRCK2, DACDAT2, ADCDAT2

SCL, SDA → CODEC_I2C_SCL, CODEC_I2C_SDA → R211 0R1J N/A, R210 0R1J N/A → PWR_I2C_SCL 6,26,49,50; PWR_I2C_SDA 6,26,49,50

AGND, GND1, GND2, CPGND → GND

C258 27P25VNPOC1J /@, C259 27P25VNPOC1J /@ Unmount → GND GND

0229 EMI add

DAP_MCLK1_5642

DAP2_SCLK_5642

C239 27P25VNPOC1J /@, R212 100R1J /@, C240 27P25VNPOC1J /@ Unmount

DAP2_FS_5642

C243 27P25VNPOC1J /@ Unmount

SPEAKER CONN.

Unmount

SPK_OUT_L+ → R201 0R1J → SPK_OUT_L+_CON

Unmount N/A C232 27P25VNPOC1J /@ → GND

C233 27P25VNPOC1J /@ → GND

SPK_OUT_L- → R200 0R1J N/A → SPK_OUT_L-_CON

C234 27P25VNPOC1J /@ → GND

SPK_OUT_R- → R205 0R1J N/A → SPK_OUT_R-_CON

Unmount C236 27P25VNPOC1J /@ → GND

C237 27P25VNPOC1J /@ → GND

SPK_OUT_R+ → R202 0R1J N/A → SPK_OUT_R+_CON

C238 27P25VNPOC1J /@ → GND

CON2 WTOB_CON_4P N/A 12G171030040 → GND

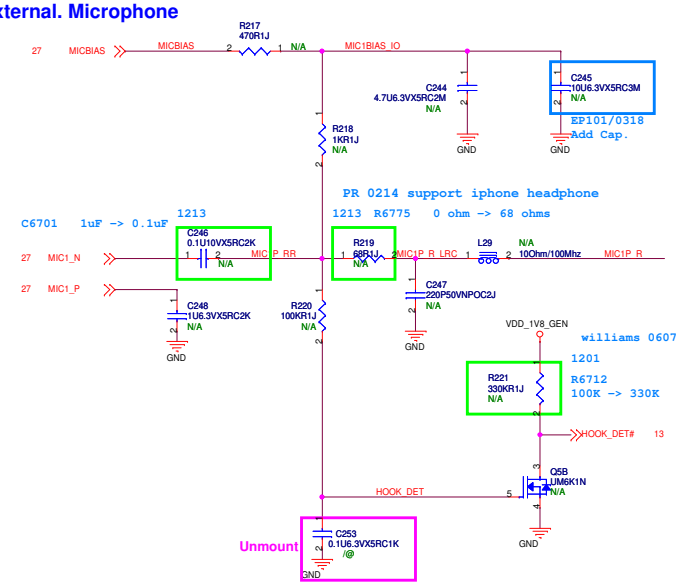
HP_OUT_L → C241 N/A 0.1U6.3VX5RC1K → HP_OUT_L_C

HP_OUT_R → C242 N/A 0.1U6.3VX5RC1K → HP_OUT_R_C

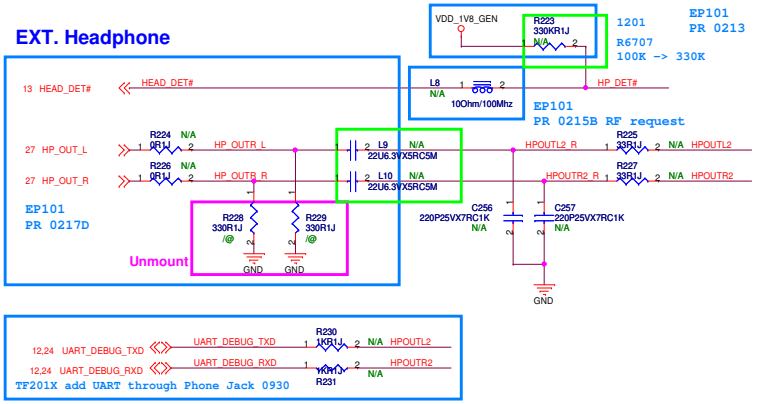
R215 20R1F N/A, R216 20R1F N/A → GND

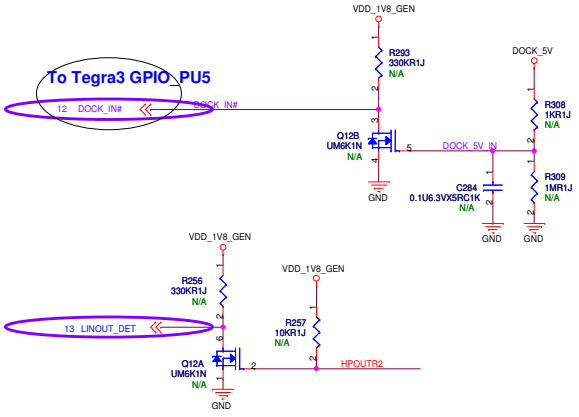
ASUSTeK COMPUTER INC. EPAD	Title : Codec ALC5642		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 27 of 60		

External. Microphone



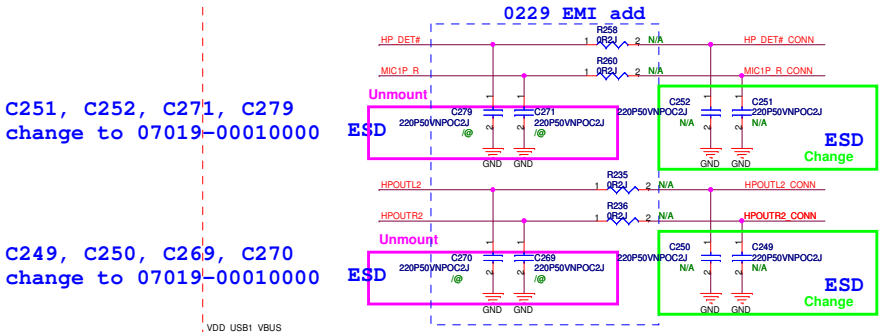
EXT. Headphone

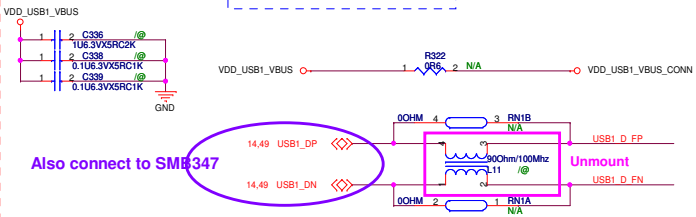


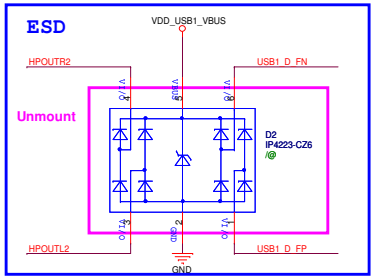


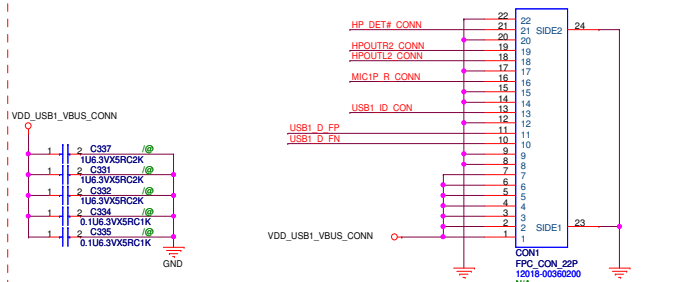
22pin FFC Connector

Mic & Headphone Conn.

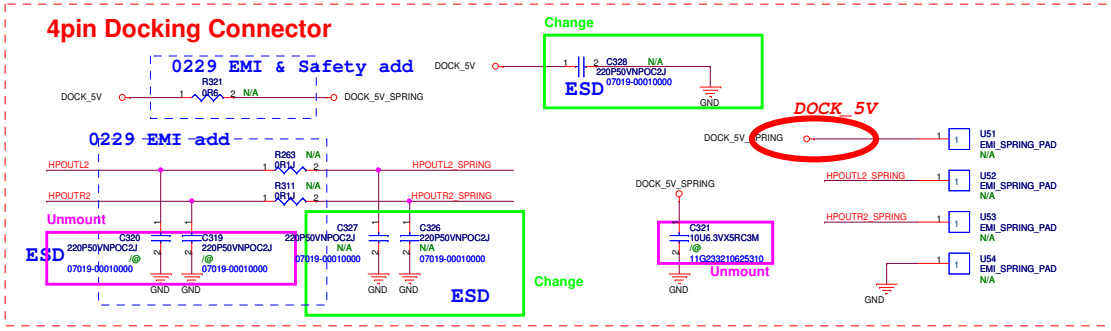






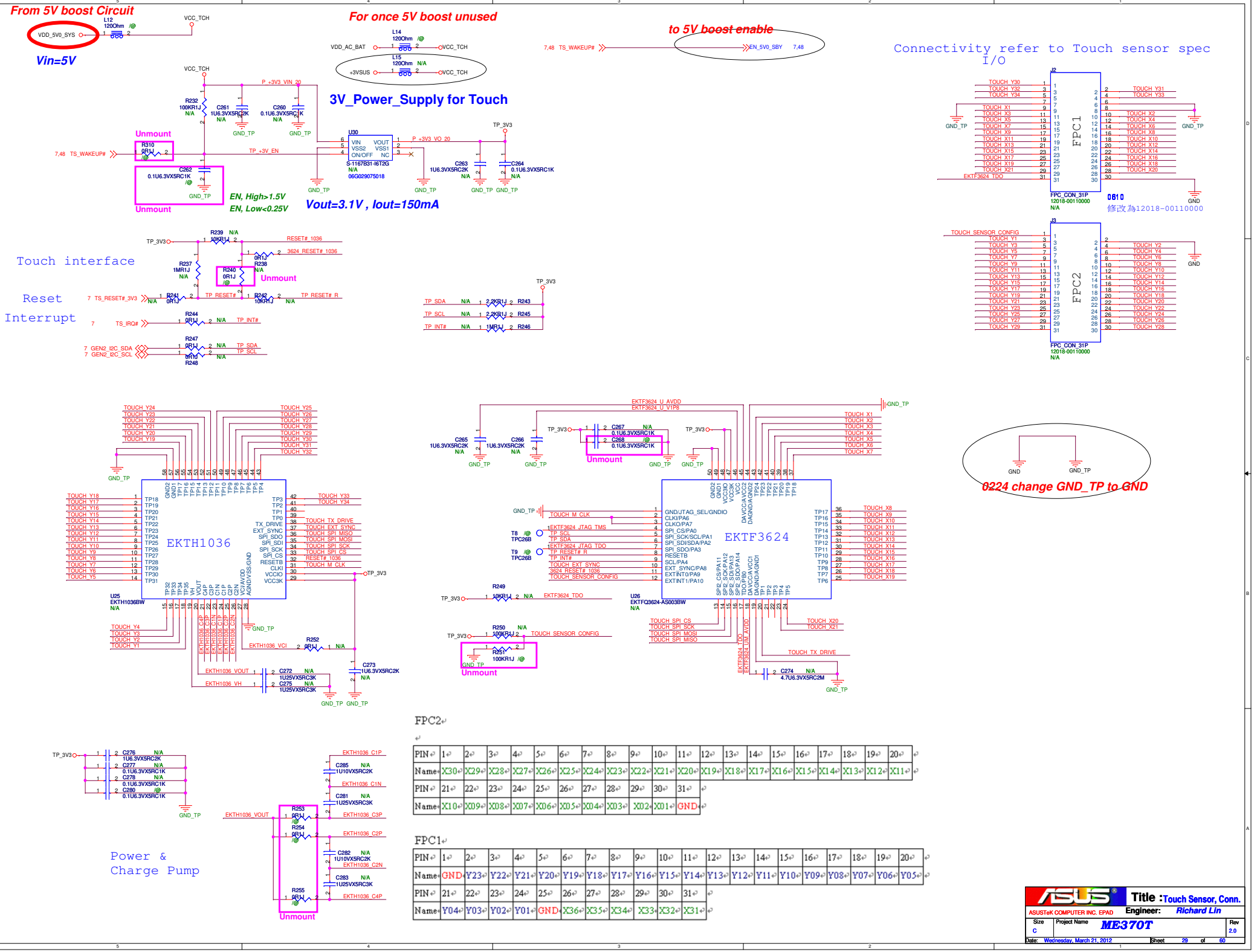


4pin Docking Connector



C319, C320, C326, C327, C328 change
to 07019-00010000

ASUSTeK COMPUTER INC. EPAD	Title : Audio/USB Conn.	
	Engineer: Richard Lin	
Size: C	Project Name: ME370T	Rev: 2.0
Date: Saturday, March 24, 2012	Sheet 28 of 60	



FPC2

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Name	X30	X29	X28	X27	X26	X25	X24	X23	X22	X21	X20	X19	X18	X17	X16	X15	X14	X13	X12	X11
PIN	21	22	23	24	25	26	27	28	29	30	31									
Name	X10	X09	X08	X07	X06	X05	X04	X03	X02	X01	GND									

FPC1

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Name	GND	Y23	Y22	Y21	Y20	Y19	Y18	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y09	Y08	Y07	Y06	Y05
PIN	21	22	23	24	25	26	27	28	29	30	31									
Name	Y04	Y03	Y02	Y01	GND	X36	X35	X34	X33	X32	X31									

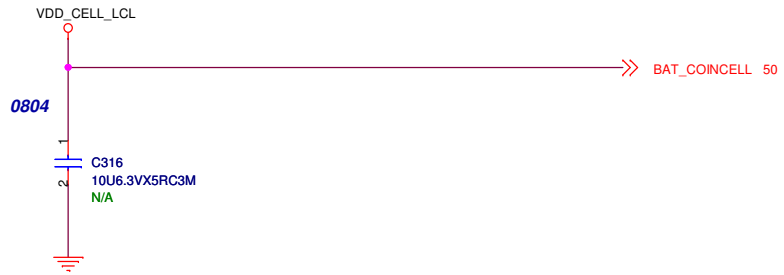
ASUSTeK COMPUTER INC. EPAD

Title : Touch Sensor, Conn.

Engineer: Richard Lin

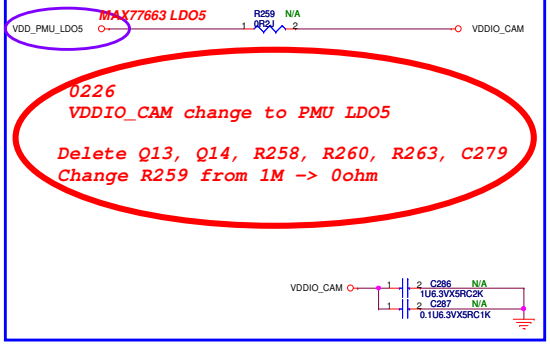
Size	Project Name	Rev
C	ME370T	2.0

Date: Wednesday, March 21, 2012 Sheet 29 of 60

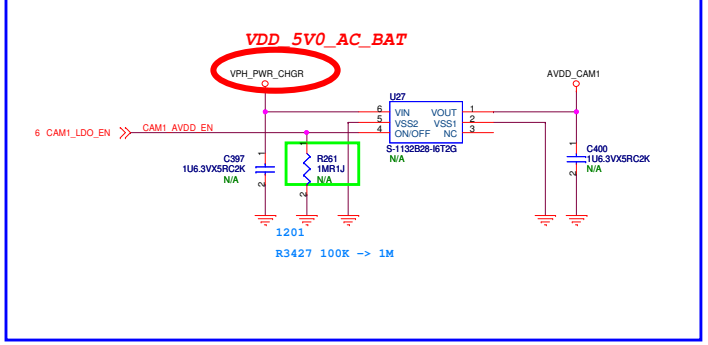


ASUSTeK COMPUTER INC. EPAD	Title : Coin Cell		
	Engineer: Richard Lin		
Size: B	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 30 of 60		

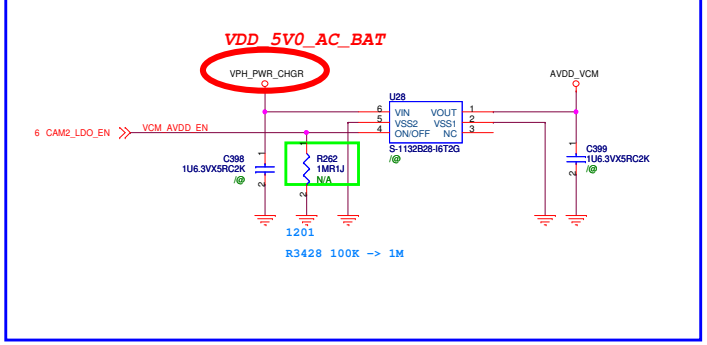
Camera VDDIO 1.8V



Camera AVDD

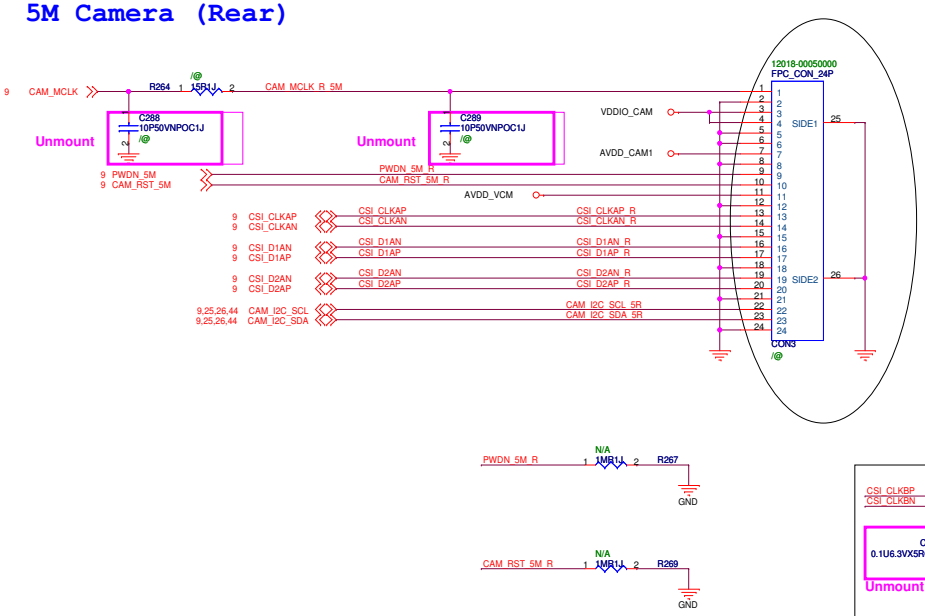


Camera VCM Power

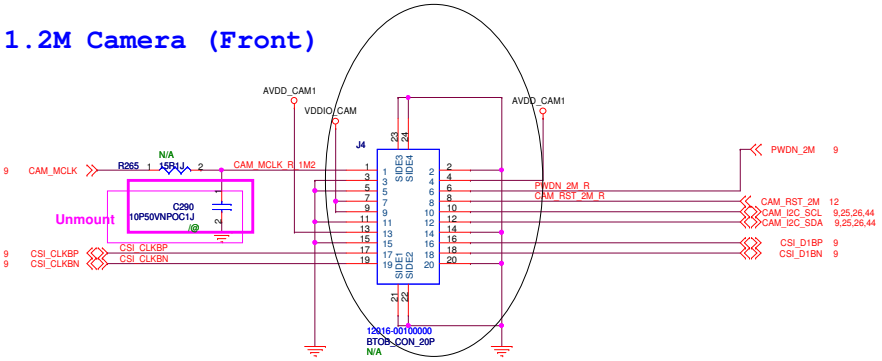


MIPI

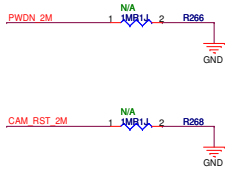
5M Camera (Rear)

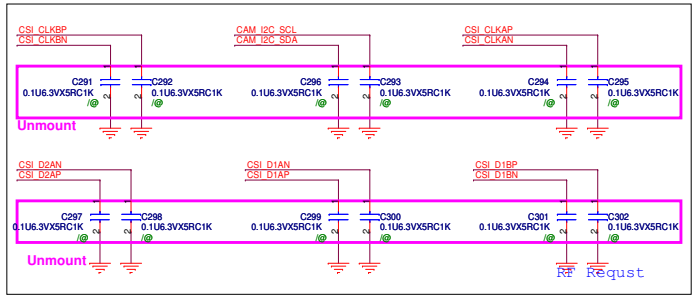


1.2M Camera (Front)



J4 2nd source
PANASONIC/AXT520124
12G161H0020A

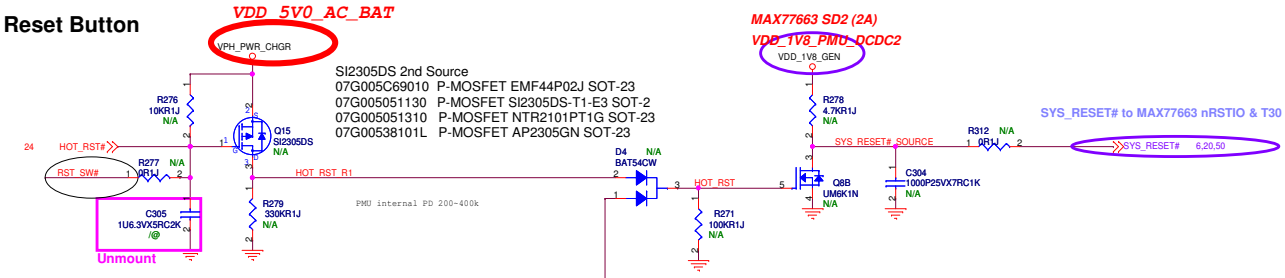




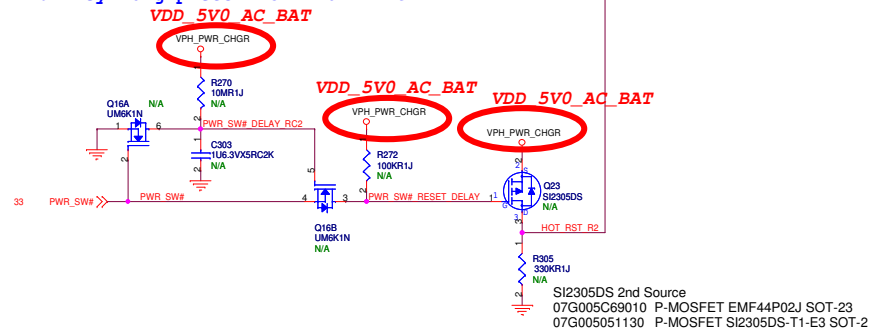
ASUSTeK COMPUTER INC. EPAD	Title : 01.Block Diagram		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 27, 2012	Sheet 31 of 60		

HOT_RST# inverse for PMIC

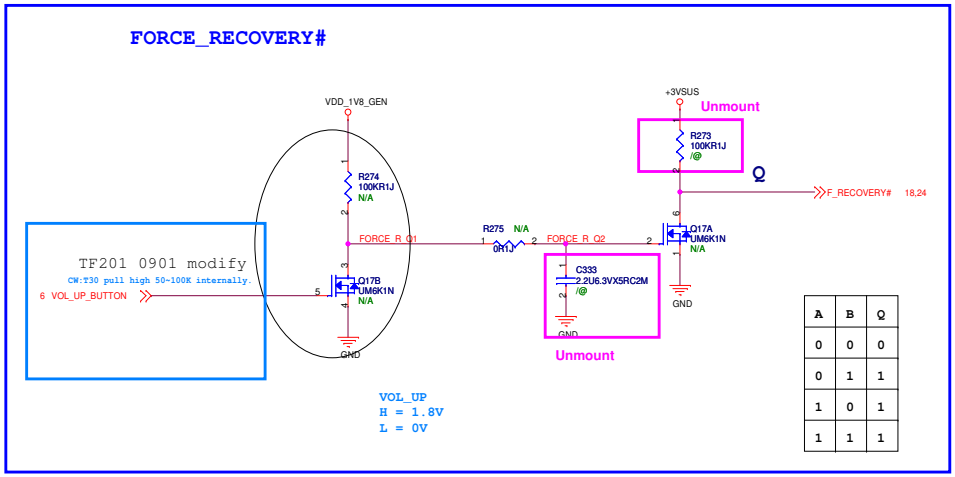
Reset Button



PWRON Key long press RESET for PMIC

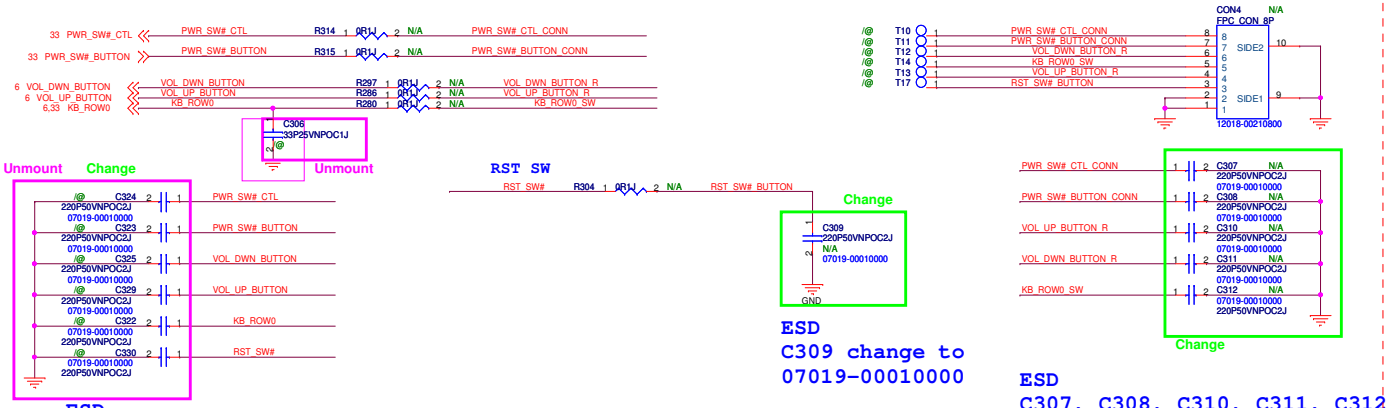


FORCE_RECOVERY#



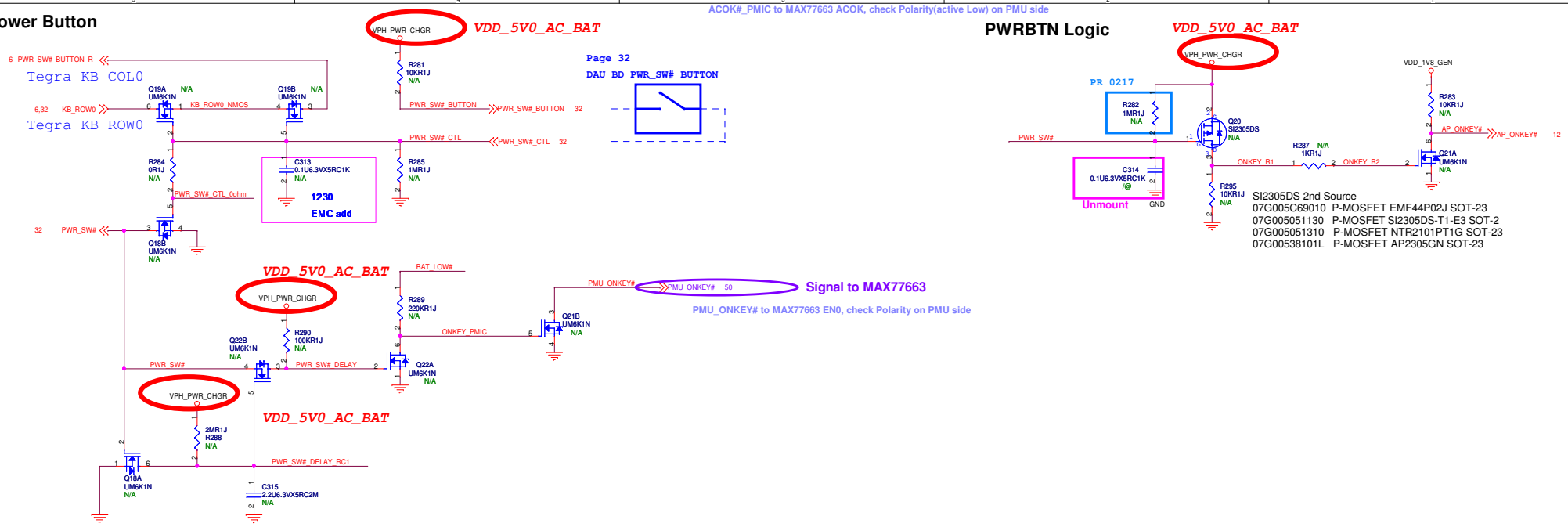
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

8pin Button Connector



Title :	Buttons /Conn.
ASUSTeK COMPUTER INC. EPAD	Engineer: Richard Lin
Size: C	Project Name: ME370T
Rev: 2.0	
Date: Wednesday, March 21, 2012	Sheet 32 of 60

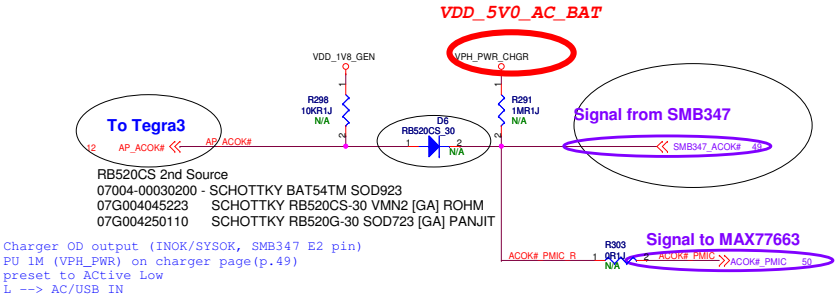
Power Button



PWRBTN Logic

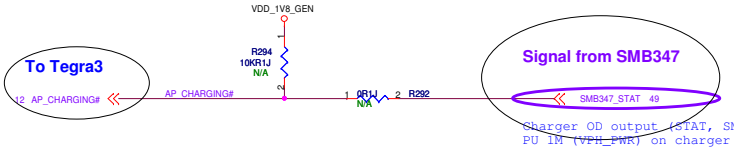
SI2305DS 2nd Source
07G005C69010 P-MOSFET EMF44P02J SOT-23
07G005051130 P-MOSFET SI2305DS-T1-E3 SOT-2
07G005051310 P-MOSFET NTR2101PT1G SOT-23
07G00538101L P-MOSFET AP2305GN SOT-23

Charger Related Signals

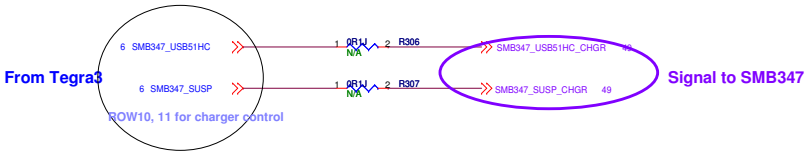


RB520CS 2nd Source
07004-00030200 - SCHOTTKY BAT54TM SOD923
07G004045223 SCHOTTKY RB520CS-30 VMN2 [GA] ROHM
07G004250110 SCHOTTKY RB520G-30 SOD723 [GA] PANJIT

Charger OD output (INOK/SYSOK, SMB347 E2 pin)
PU 1M (VPH_PWR) on charger page(p.49)
preset to ACtive Low
L --> AC/USB IN

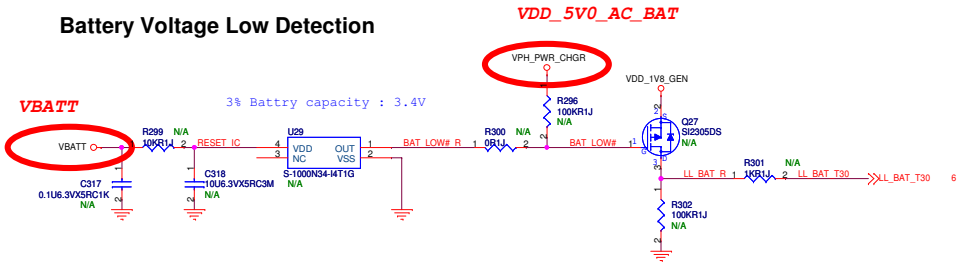


Charger OD output (STAT, SMB347 F5 pin)
PU 1M (VPH_PWR) on charger page(p.49)
preset to ACtive Low
L --> charging
H --> other status



ROW10, 11 for charger control

Battery Voltage Low Detection



SI2305DS 2nd Source
07G005C69010 P-MOSFET EMF44P02J SOT-23
07G005051130 P-MOSFET SI2305DS-T1-E3 SOT-2
07G005051310 P-MOSFET NTR2101PT1G SOT-23
07G00538101L P-MOSFET AP2305GN SOT-23

ASUSTeK COMPUTER INC. EPAD

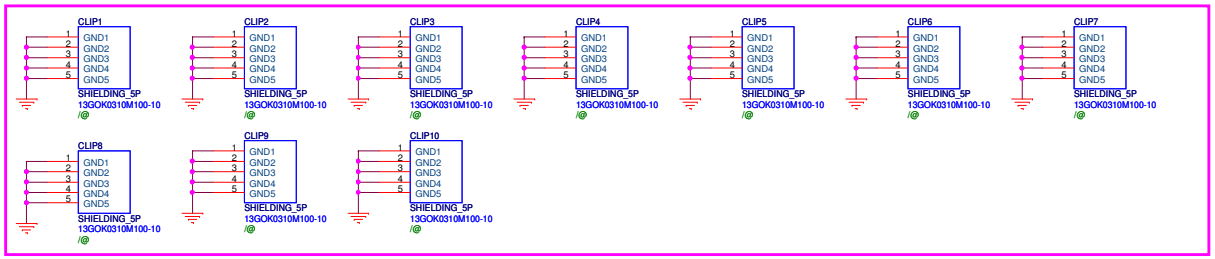
Title : T30 Core & Fuse

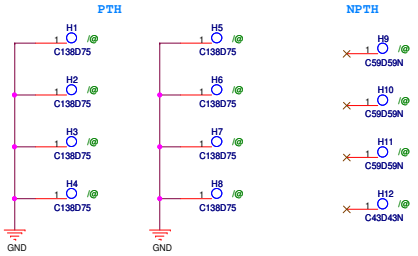
Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

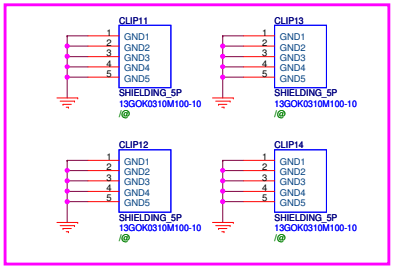
Date: Wednesday, March 21, 2012 Sheet 33 of 60

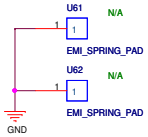
Unmount



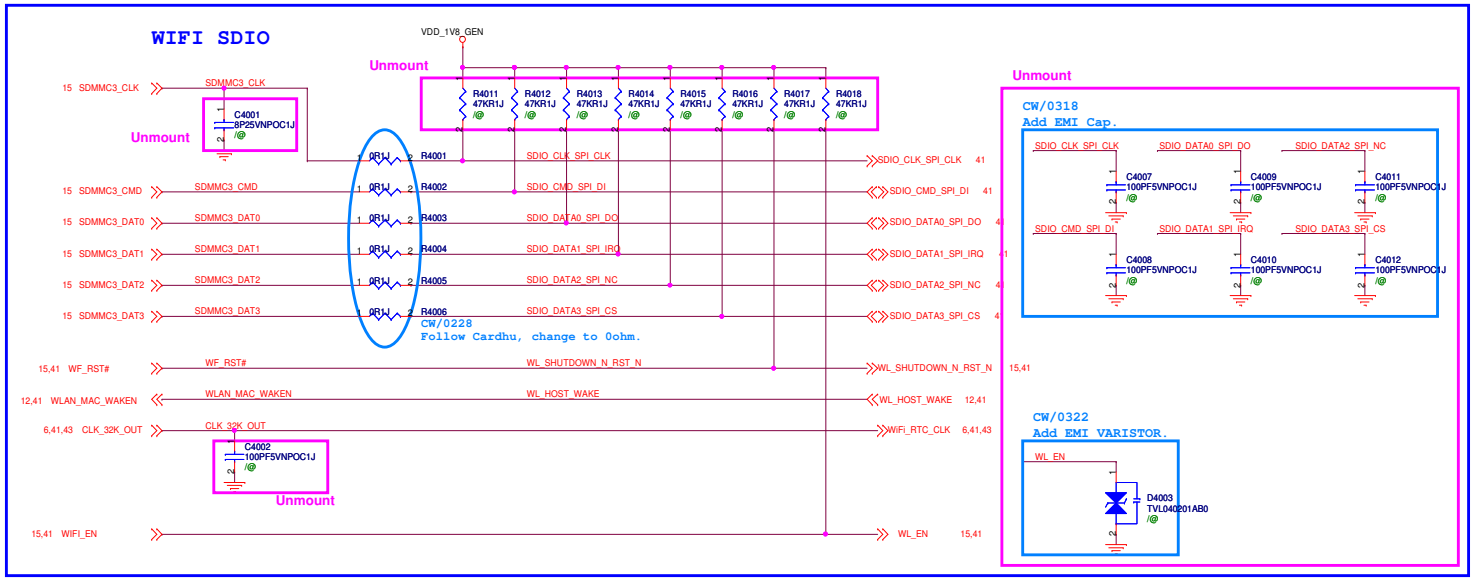


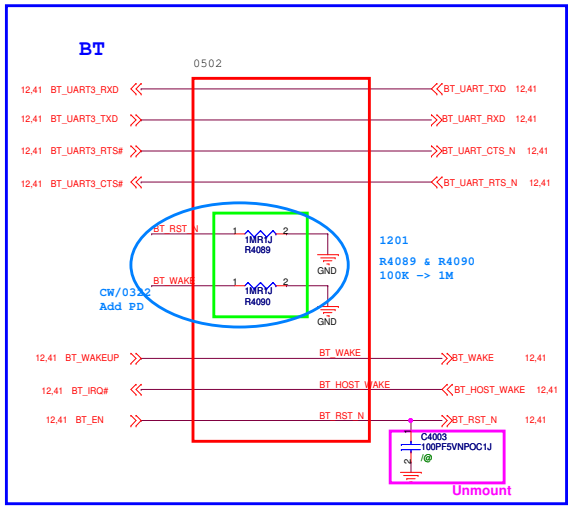
Unmount

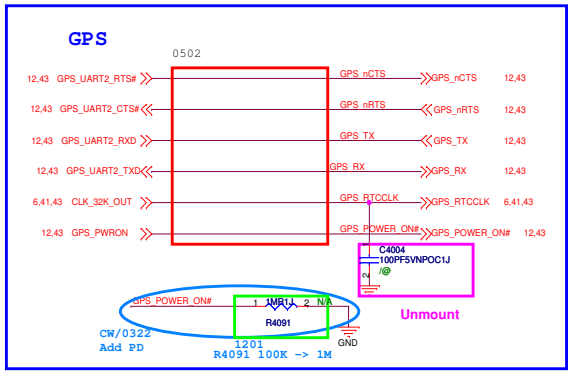




ASUSTeK COMPUTER INC. EPAD	Title : EMC, Screw hole		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 27, 2012	Sheet 39 of 60		

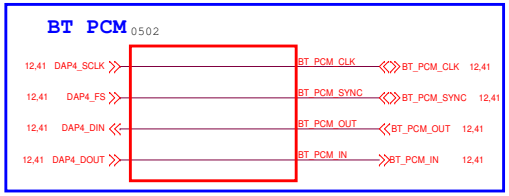






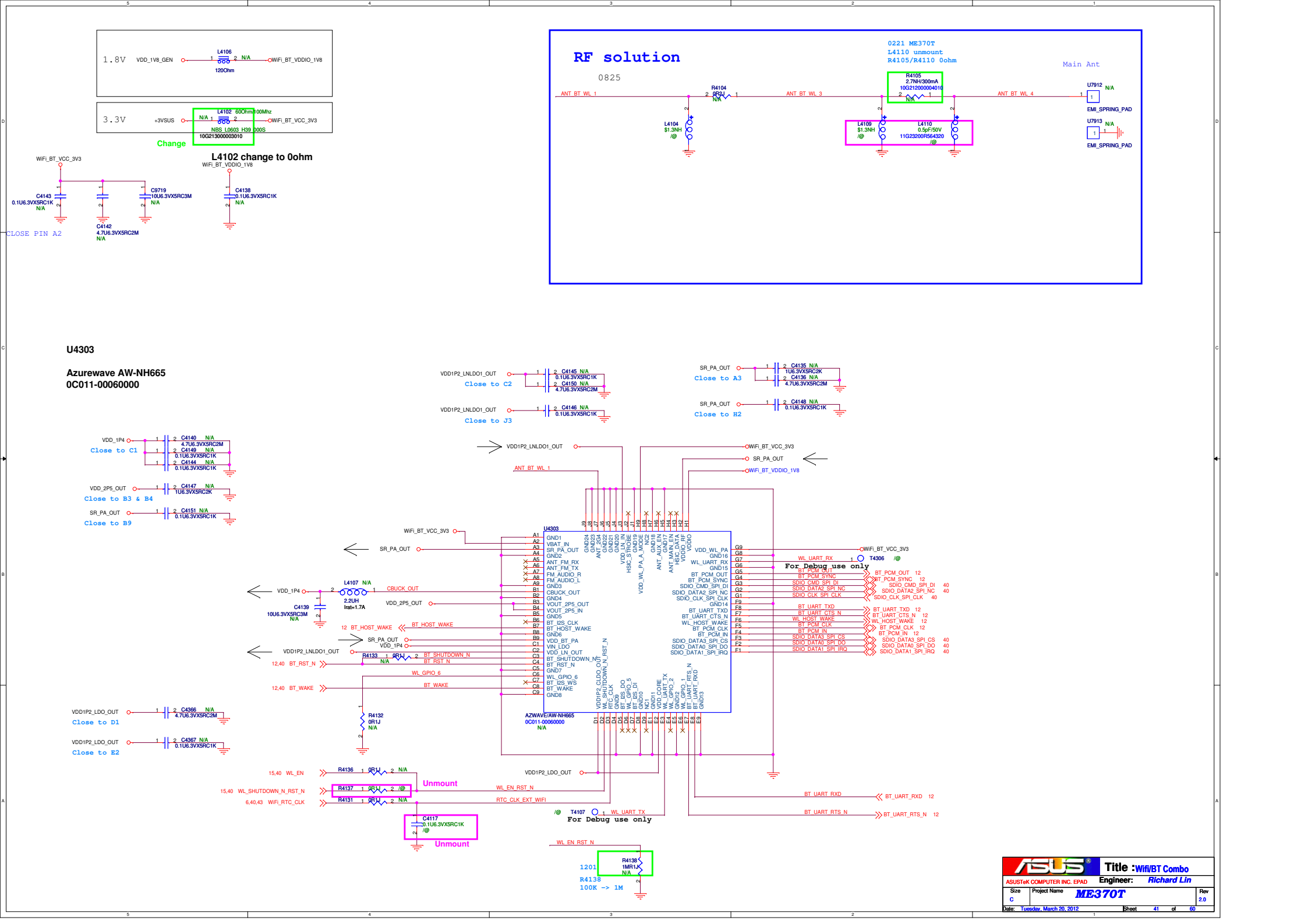
remove FM

remove FM audio interface,



remove proximity to 3G path control 0609

ASUSTeK COMPUTER INC. EPAD	Title : RF Interface		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 40 of 60		



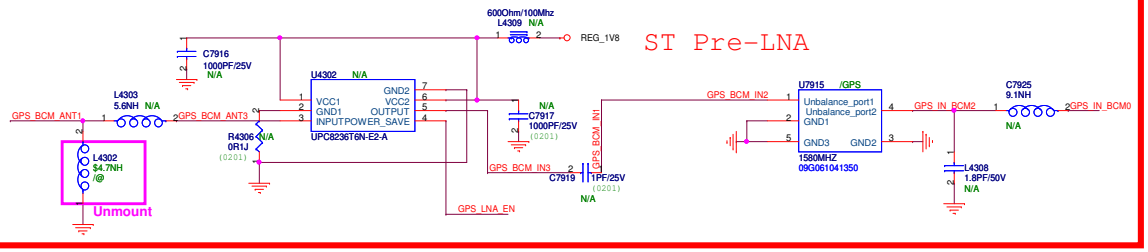
Title	Wifi/BT Combo
Engineer	Richard Lin
Company	ASUSTeK COMPUTER INC. EPAD
Size	C
Project Name	ME370T
Rev	2.0
Date	Tuesday, March 20, 2012
Sheet	41 of 60

02G561020900 C.S BCM4751IFBG FBGA100
02038-00010100 C.S BCM47511IFBG FBGA100

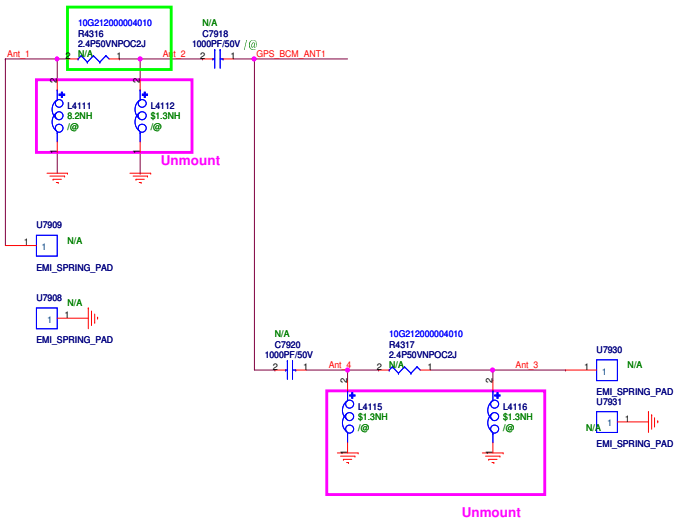
09G061041350 SAW FILTER 1575.42MHZ
09G061226010 SAW FILTER 1580MHZ

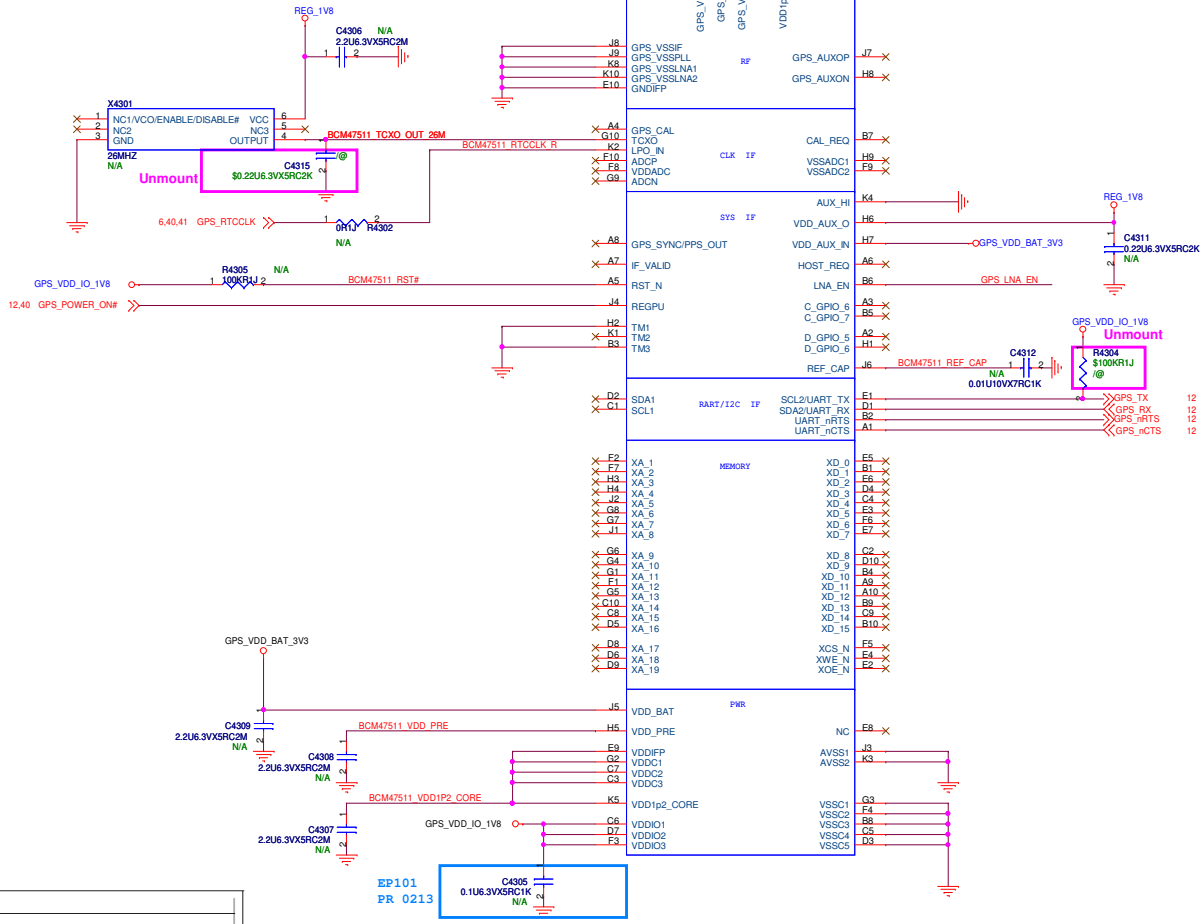
U4301	BCM4751	BCM47511
	02G561020900	02038-00010100
U7915	09G061041350	09G061226010

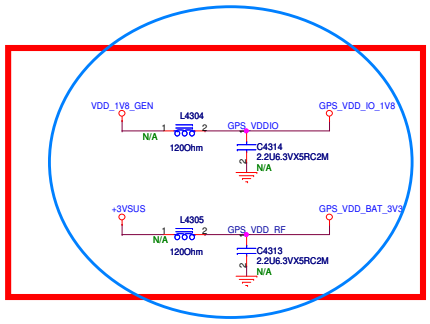
ST Pre-LNA

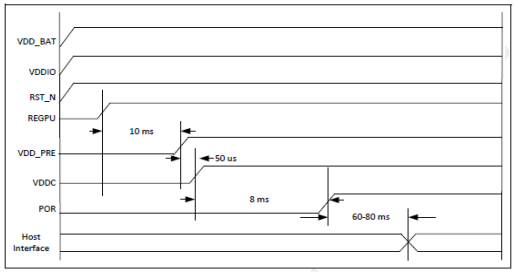


0221 ME370T
L4111 unmount
R4316/R4317 0ohm





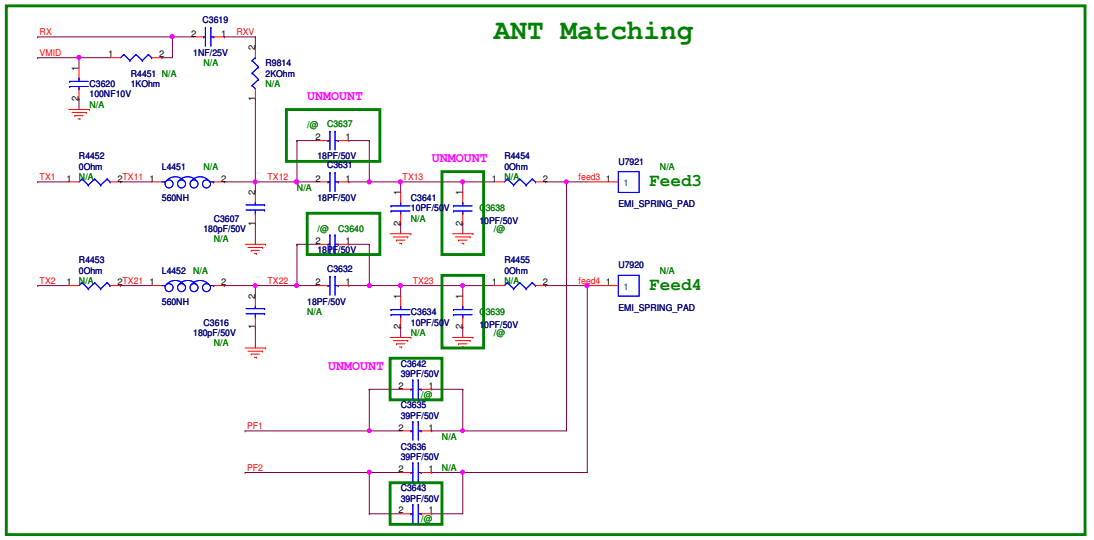




CW/0228
Check VDD_BAT & VDDIO & RST_N sequence.

remove proximity to 3G path control 0609

ASUSTeK COMPUTER INC. EPAD	Title : GPS		
	Engineer: Richard Lin		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 43 of 60		



9,25,26,31 CAM_I2C_SDA
9,25,26,31 CAM_I2C_SCL
13 NFC_IRQ_R
6 NFC_GPIO4_R
6 NFC_VEN

NFC_SDA_R 0R1J R4401 N/A NFC_SDA
NFC_SCL_R 0R1J R4402 N/A NFC_SCL
NFC_IRQ_R 0R1J R4403 N/A NFC_IRQ
NFC_GPIO4_R 0R1J R4404 N/A NFC_GPIO4
NFC_VEN
R4405 1MR1J N/A

1.8V VDD_1V8_GEN R4411 0R2J N/A NFC_PVDD

VDD_5V0_AC_BAT
VPH_PWR_CHGR R4412 0R2J N/A NFC_VBAT

NFC_PVDD C4401 N/A 1U6.3VX5RC2K
C4402 N/A 0.1U6.3VX5RC1K
NFC_VBAT C4403 N/A 1U6.3VX5RC2K
C4404 N/A 0.1U6.3VX5RC1K

U4401
PN65NET1/C205020
N/A

NFC_VBAT	D8	
NFC_VCO	F8	VBAT
NFC_VDHF	D1	VBAT2
	C1	VCO_VDD
	A8	VDHF
	G7	PMUVCC
	F6	PMU_GND
	G1	VSS
NFC_AVDD	F2	AVDD_in
NFC_DVDD	A5	AVDD_out
	A4	DVDD
NFC_TVDD	G8	PVDD
	F7	TVDD
	E8	TVDD_OUT
NFC_VEN	B7	VEN_MON
	E4	VEN
NFC_IF1	B4	IF0
NFC_SDA	C4	IF1
NFC_SCL	D4	IF2
NFC_IRQ	A3	IF3
	C8	IRQ
	E7	SVDD
	D7	SIGIN
	B8	SIGOUT
	C7	SIMVCC
	D6	SWIO
	H6	EXT_SW_CTRL
TX1	H7	TX1
TX2	H4	TX2
RX	G4	RX
VMID	G5	VMID
PF1	G6	ANT1
PF2		ANT2

	A6	TEST1
	B6	TEST2
	C5	TEST3
	D5	TEST4
	E5	TEST5
	H2	TEST6
	F3	TEST7
	G2	TEST8
	G3	TEST9
	C6	TEST10
	E3	GPIO0
	D3	GPIO1
	C3	GPIO2
	C2	GPIO3
NFC_GPIO4	B1	GPIO4
	B2	GPIO5
	B3	GPIO6
	A1	GPIO7
NFC_GPIO6	A7	RFU1
	E6	RFU2
	H1	RFU3
	A2	IFSEL0
IF_SEL1	F4	IFSEL1
	F5	IFSEL2
	H8	TVSS2
	H5	TVSS1
	B5	PVSS
	D2	DVSS
	H3	AVSS2
	E2	AVSS1
NFC_XTAL1	E1	XTAL1
NFC_XTAL2	F1	XTAL2

NFC_PVDD
R4407 100KR1J N/A
R4408 0R1J /@ UNMOUNT

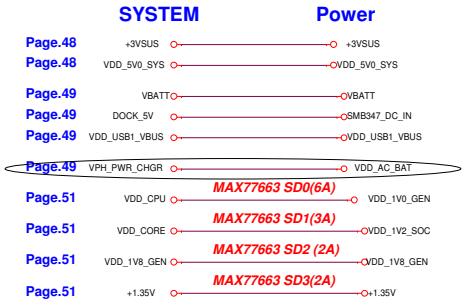
NFC_IF1
R4406 0R1J N/A

C4405 0.1U6.3VX5RC1K N/A
C4406 N/A 1UF6.3VX5RC2K
C4407 1UF6.3VX5RC2K N/A
C4408 0.1U6.3VX5RC1K N/A
C4409 1UF6.3VX5RC2K N/A
C4410 0.1U6.3VX5RC1K N/A

IF0(ADDR0)	IF1(ADDR1)	ADDRESS
0	0	28H
0	1	29H
1	0	2AH
1	1	2BH

NFC_XTAL1
NFC_XTAL2
N/A X4401 27.12Mhz
C4411 10P50VNPOC1J N/A
C4412 10P50VNPOC1J N/A

ASUSTeK COMPUTER INC. EPAD	Title : NFC		
	Engineer: Jamie Tseng		
Size C	Project Name ME370T		Rev 2.0
Date: Thursday, March 22, 2012	Sheet 44 of 60		



ASUSTeK COMPUTER INC. EPAD

Title : BB-POWER I/F

Engineer: Richard Lin

Size	Project Name	Rev
C	ME370T	2.0

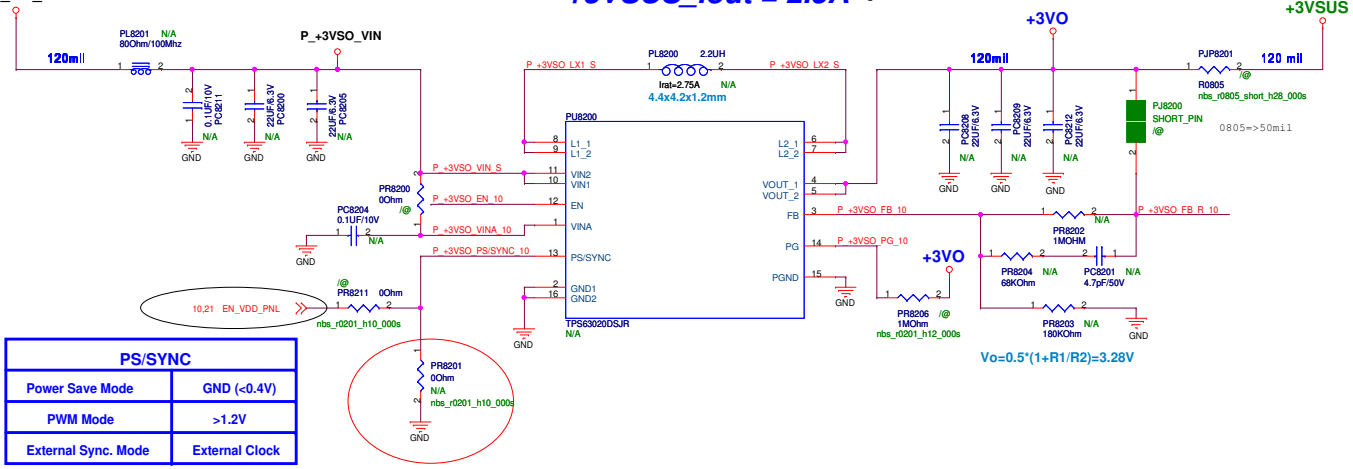
Date: Thursday, March 01, 2012 Sheet 45 of 60

+3VSUS POWER SUPPLY

BAT=3V~4.2V

VDD_AC_BAT

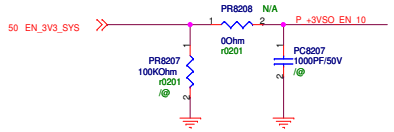
+3VSUS_Iout = 2.5A `Iq=50uA , Isd=1uA`



PS/SYNC	
Power Save Mode	GND (<0.4V)
PWM Mode	>1.2V
External Sync. Mode	External Clock

Vo=0.5*(1+R1/R2)=3.28V

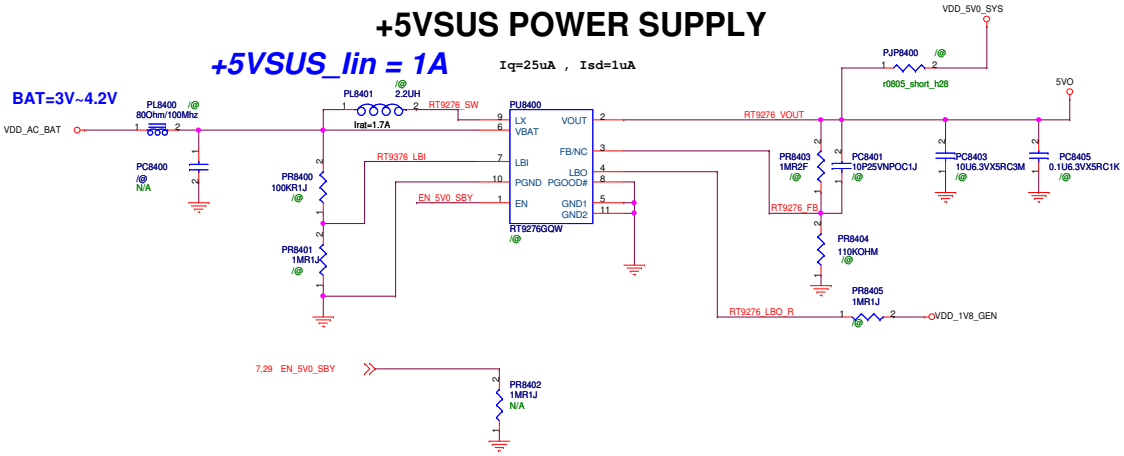
PS/SYNC , EN
Hi ----> over 1.2V
Low --> under 0.4V



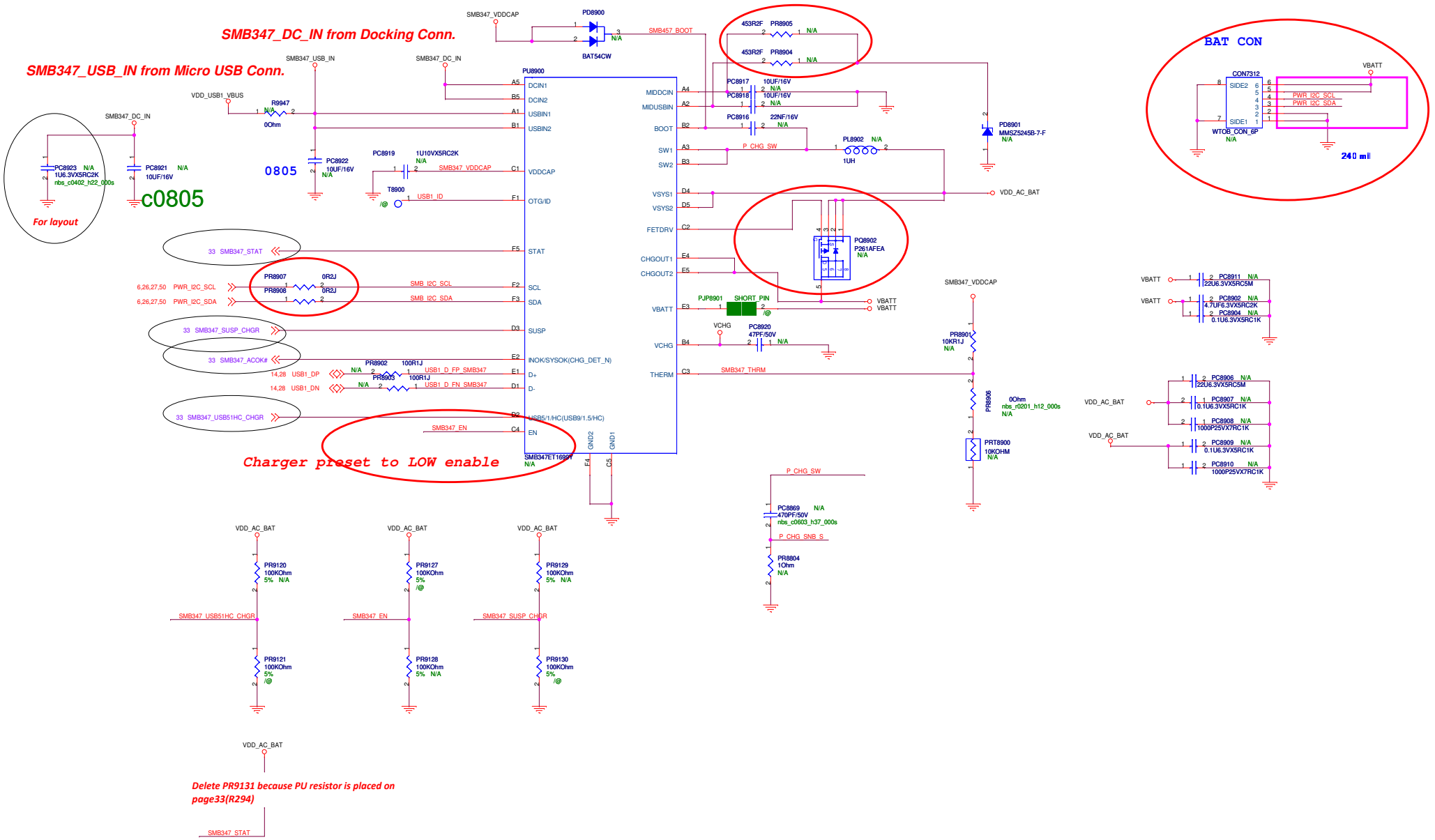
+5VSUS POWER SUPPLY

+5VSUS_Iin = 1A `Iq=25uA , Isd=1uA`

BAT=3V~4.2V

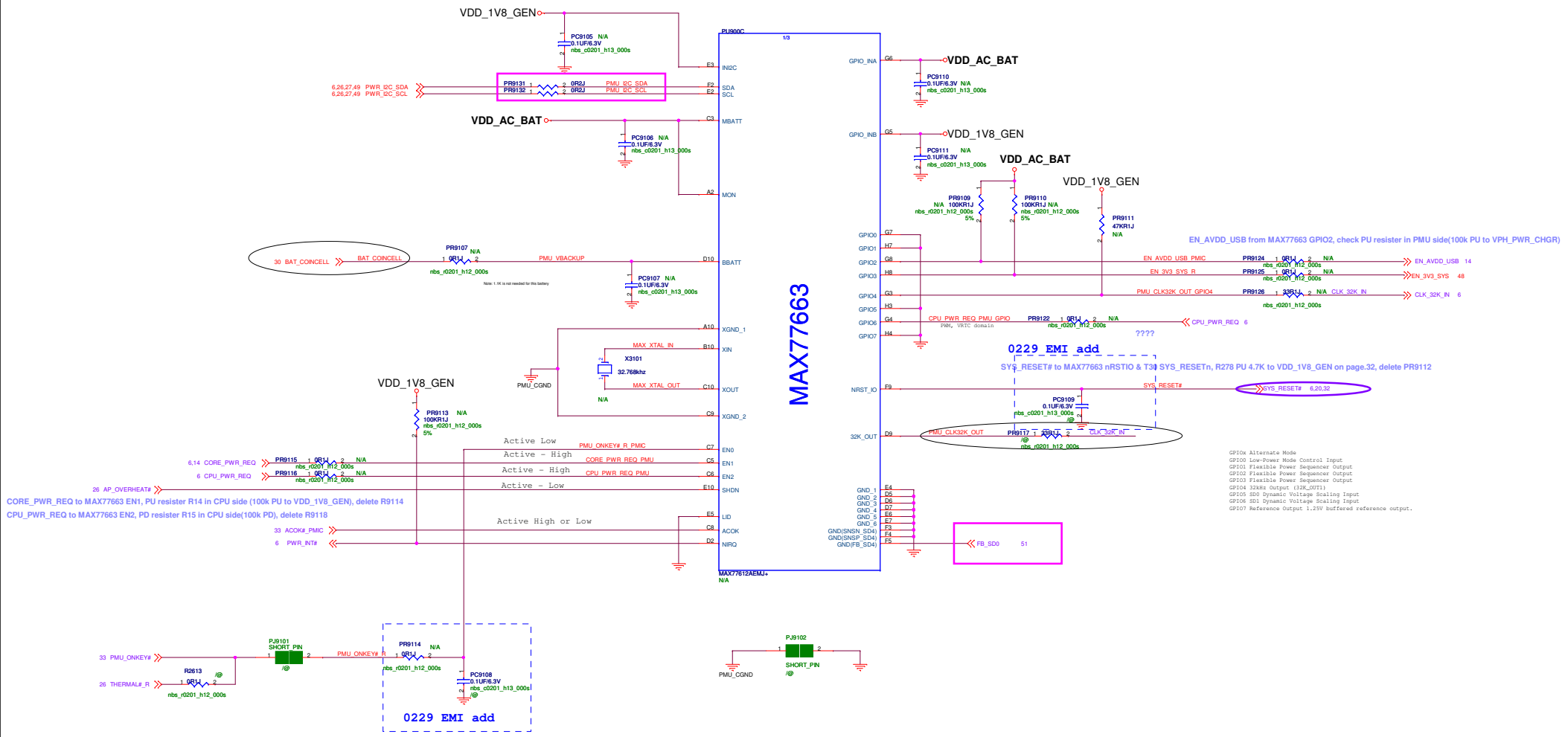


ASUSTeK COMPUTER INC. EPAD	Title : 5V & 3.3V External		
	Engineer: Timmy Wu		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Wednesday, March 21, 2012	Sheet 48 of 60		



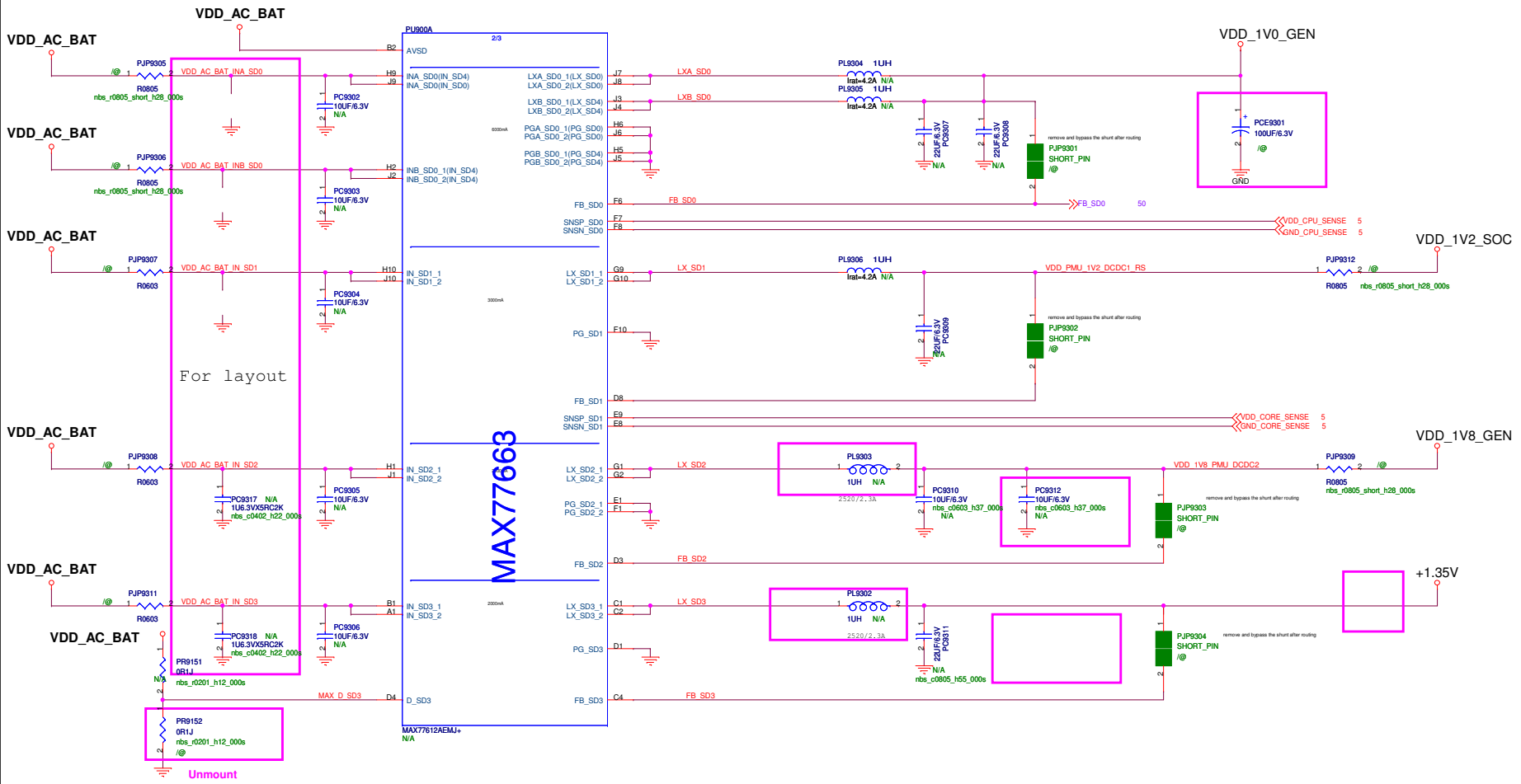
ASUSTeK COMPUTER INC. EPAD	Title : Charger SMB347		
	Engineer: Timmy Wu		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Wednesday, March 21, 2012	Sheet 49 of 60		

Main PMIC Page 1 of 3 (DC I/P, Reset, GPIO & Crystals)



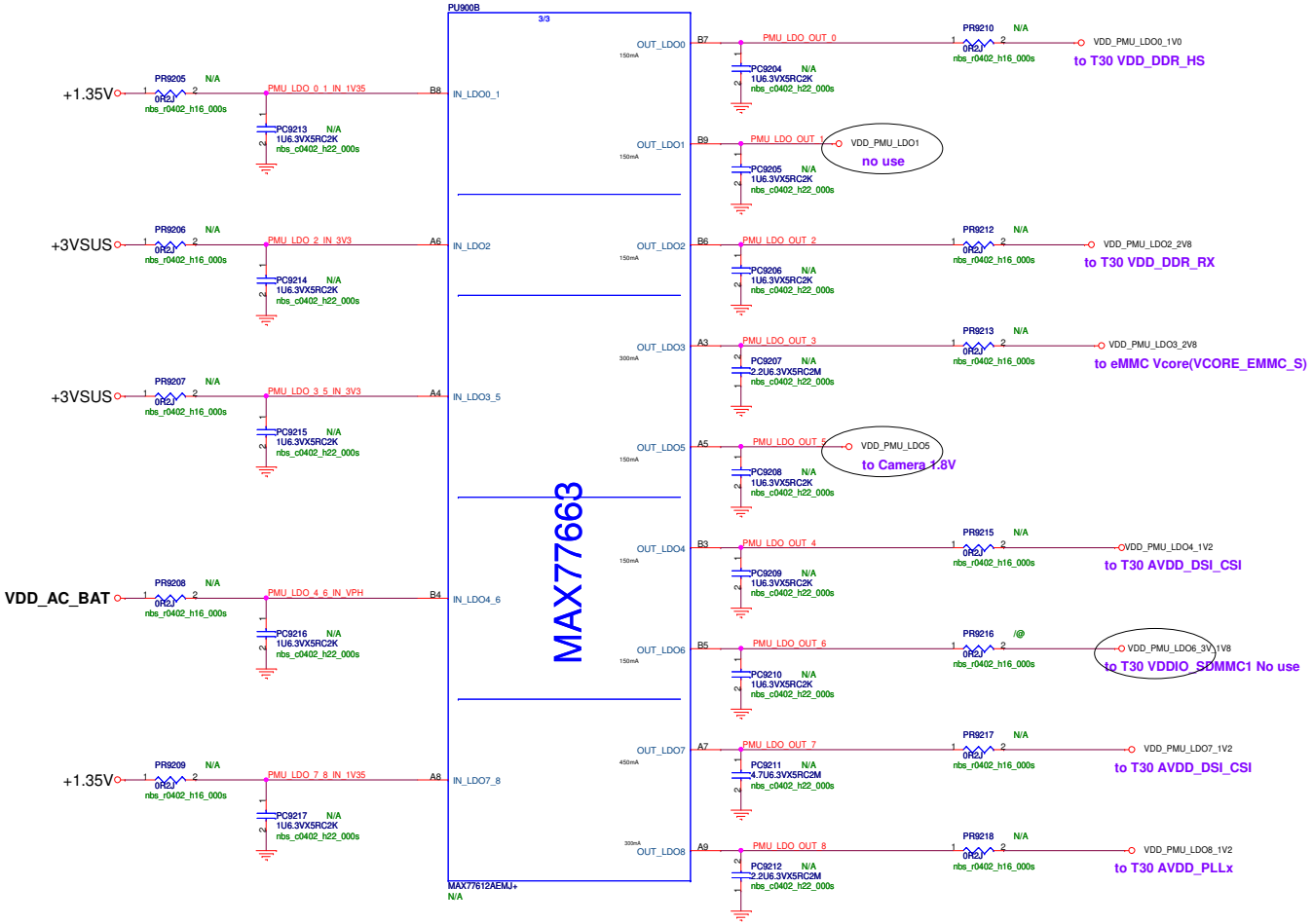
ASUSTeK COMPUTER INC. EPAD	Title : PMIC 1/3		
	Engineer: Timmy Wu		
Size: Custom	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 50 of 60		

Main PMIC Page 2 of 3 (Main DC/DC Converters)



ASUS	Title : PMIC 2/3		
ASUSTeK COMPUTER INC. EPAD	Engineer: Timmy Wu		
Size: C	Project Name: ME370T		Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 51 of 60		

Main PMIC Page 3 of 3 (LDO's)



ASUSTeK COMPUTER INC. EPAD	Title : PMIC 3/3	
	Engineer: Timmy Wu	
Size: C	Project Name: ME370T	Rev: 2.0
Date: Tuesday, March 20, 2012	Sheet 52 of 60	