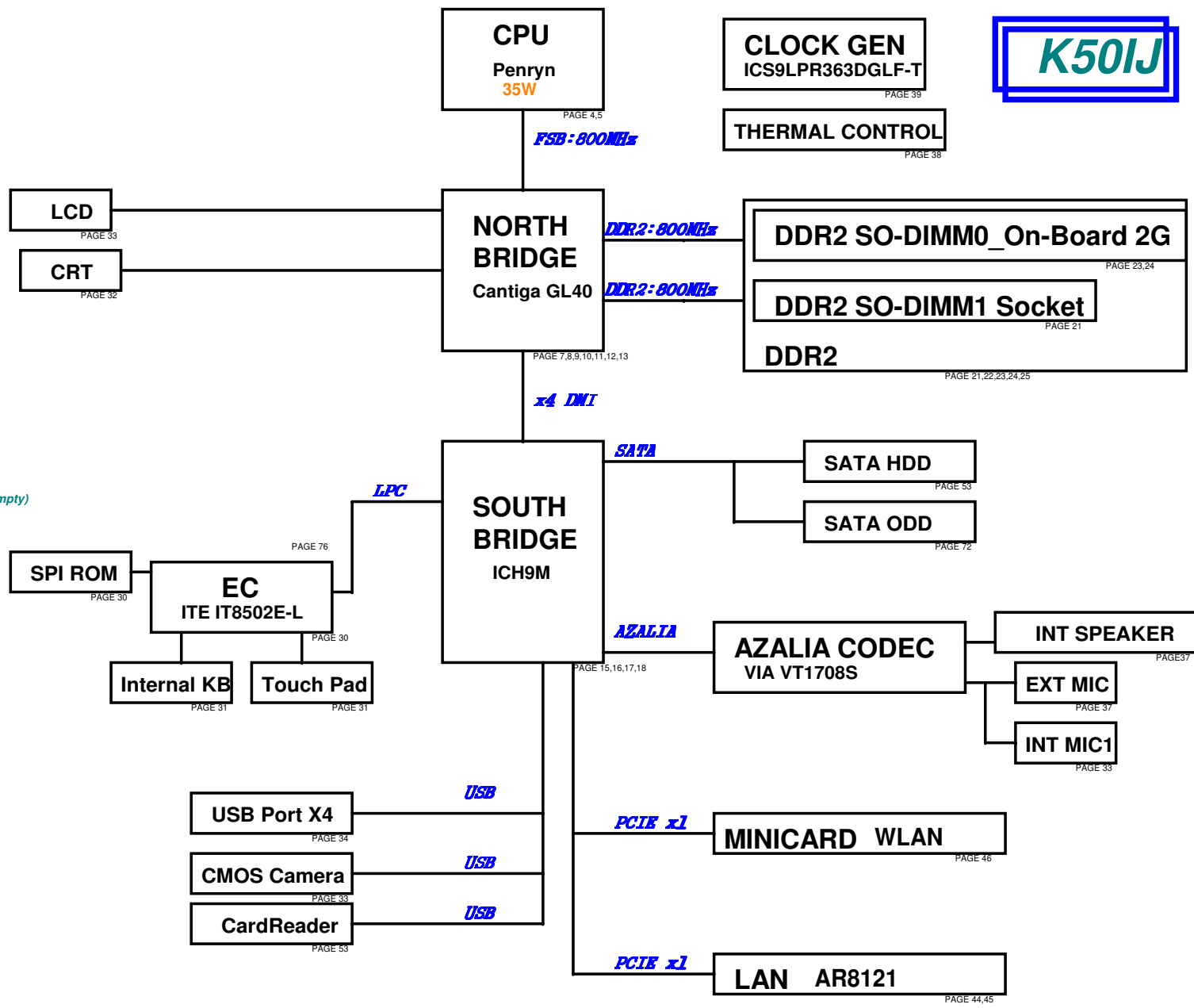


01	Block Diagram	61	*
02	System Setting	62	USB CONN
03	POWER SEQUENCE	63	*
04	CPU-Penryn(HOST)	64	*
05	CPU-Penryn(PWR)	65	*
06	*	66	*
07	Cantiga(HOST)	67	DEBUG CONN
08	Cantiga(DMI & CFG)	68	DC & BAT IN
09	Cantiga(GRAPHIC)	69	*
10	Cantiga(DDR2)	70	*
11	Cantiga(PWR)	71	*
12	Cantiga(PWR2)	72	SATA-HDD & ODD
13	Cantiga(GND)	73	*
14	*	74	HOLE & Spring
15	SB-ICH9M(1)_SATA	75	*
16	SB-ICH9M(2)_PCIE/USB	76	EXPRESS GATE
17	SB-ICH9M(3)_PM/GPIO	77	History
18	SB-ICH9M(PWR)	78	*
19	*	79	*
20	DDR2 SO-DIMM0	80	POWER_VCORE
21	DDR2 SO-DIMM1	81	POWER_SYSTEM
22	DDR2 TERMINATION	82	POWER_I/O_1.5VS & 1.05VS
23	*	83	POWER_I/O_DDR & VTT
24	*	84	POWER_I/O(Empty)
25	*	85	POWER_VGA_CORE&1.1VS(Empty)
26	*	86	POWER_MCH_CORE(Empty)
27	*	87	POWER_CHARGER
28	*	88	POWER_DETECT
29	*	89	POWER_LOAD SWITCH
30	EC_IT8512E-L(1/2)	90	POWER_PROTECT
31	EC_IT8512E-L(2/2)	91	POWER_SIGNAL
32	CRT	92	POWER_FLOWCHART
33	LVDS & INVERTER CONNECTOR	93	POWER_HISTORY
34	BT		
35	*		
36	CONEXANT CX20582		
37	CONEXANT_HP/MIC		
38	THER SENSOR & FAN		
39	CLOCK GEN-ICS9LPR363DGLF-T		
40	*		
41	Switch Button & LED		
42	DISCHARGE		
43	*		
44	PCI-E LAN_RTL8111C		
45	MDC & RJ45+11		
46	Mini card_WLAN+3G		
47	*		
48	*		
49	*		
50	*		
51	*		
52	*		
53	CardReader & SIM CONN & TPM		
54	NEWCARD		
55	*		
56	HDA level shifter		
57	iHDMI		
58	*		
59	*		
60	*		



ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(Programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#EXT PU	+5VS
GPIO 06	GPI	EXT PU	+3VS
GPIO 07	GPO	SEL_VID2 -	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	SUS_PWR_ACK EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI)	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLEPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO)	+3VS
GPIO 18	GPO	SEL_VID3 -	+3VS
GPIO 19	GPO	SEL_VID0 -	+3VS
GPIO 20	GPO	SEL_VID4 - INT PD*	+3VS
GPIO 21	GPO	VID_SW - High Active	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	SEL_VID5	+3VSUS
GPIO 28	GPO	SEL_VID6	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	SEL_VID1 -	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	NEWCARD_OC#	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	EXT PU	+3VSUS
GPIO 57	GPI	EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	LINKALERT#	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FANO_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FANO_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSTATUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM/+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	
-	-	-	
-	-	-	
-	-	-	
-	-	-	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIe Device	Bus	PCIe Device	Bus
Robson	PE(T/R)(p/n)1	3G/TV	PE(T/R)(p/n)4
WLAN	PE(T/R)(p/n)2	UWB	PE(T/R)(p/n)5
NEWCARD	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6619)	1001100x (98)

INT PU*: PU or PD in special time
 GPIO33 Internal Pull High, Go Low= Flash -
 Descriptor Security will be overridden

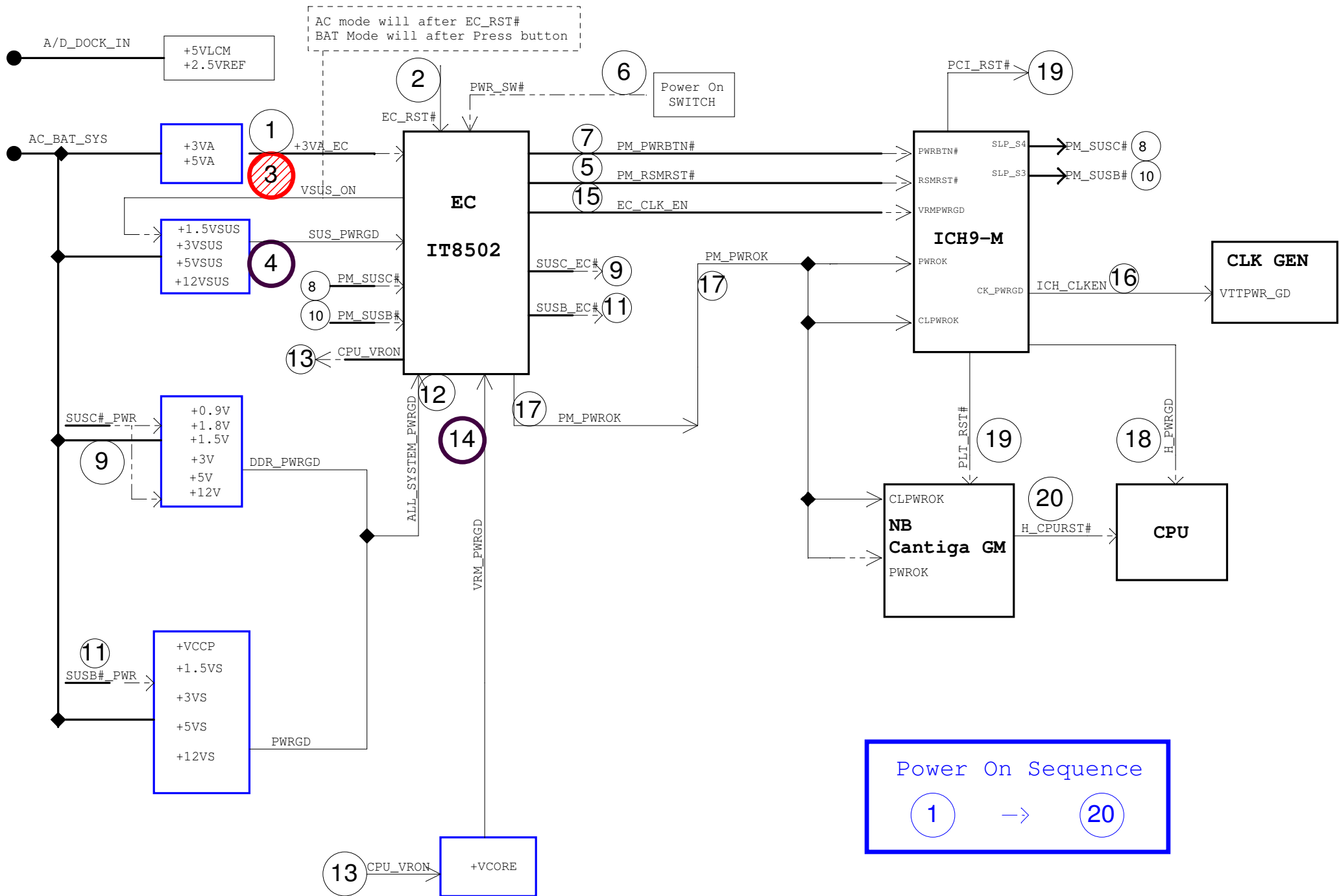
<Variant Name>

Title : System Setting
Engineer: Alex & Bruce

ASUSTek Computer INC. NB1

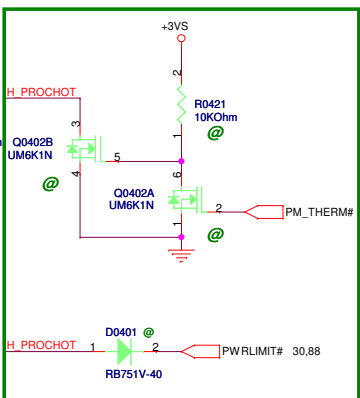
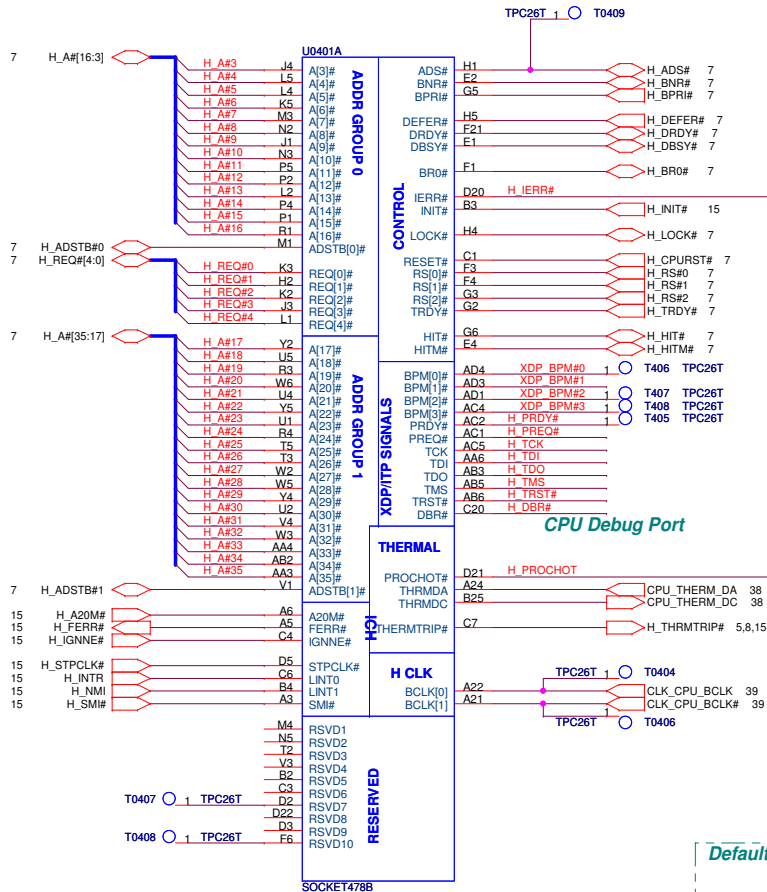
Size	Project Name	Rev
Custom	K401J/K501J	1.1

Date: Monday, March 09, 2009 Sheet 2 of 96

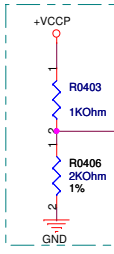


+VCCP +VCCP 5,7,8,9,11,12,15,18,39,42,82

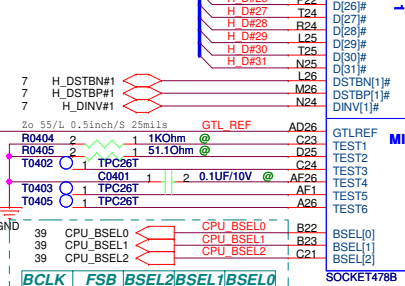
add test point



AGTL+ I/O Voltage Reference



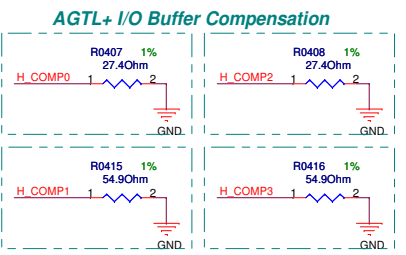
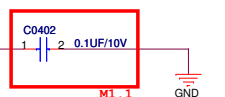
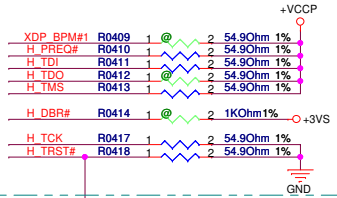
CPU Debug Port



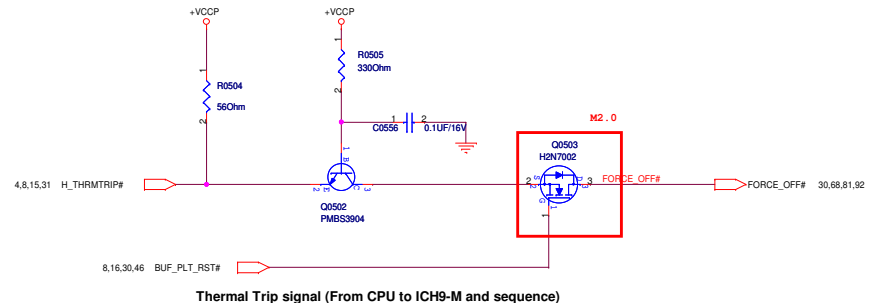
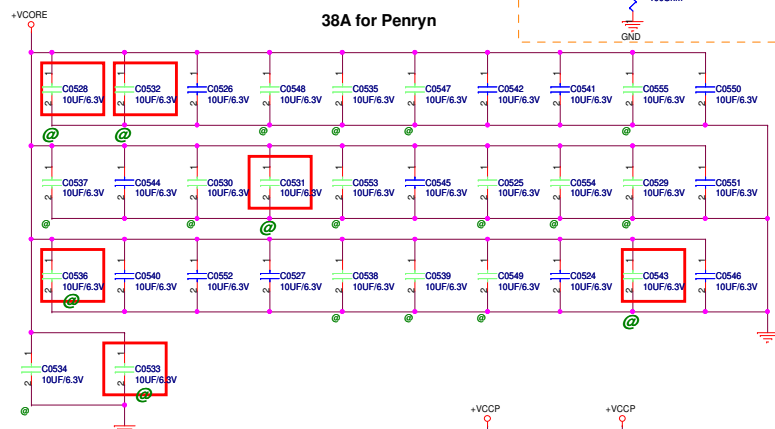
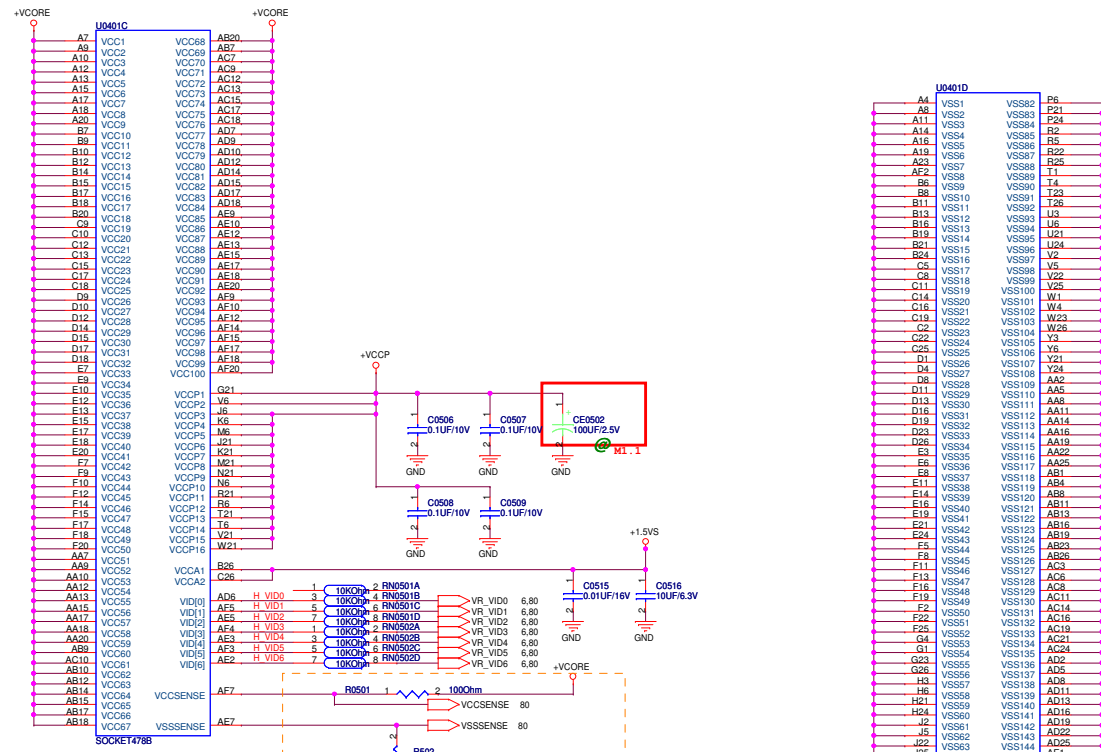
AGTL+ I/O Buffer Compensation

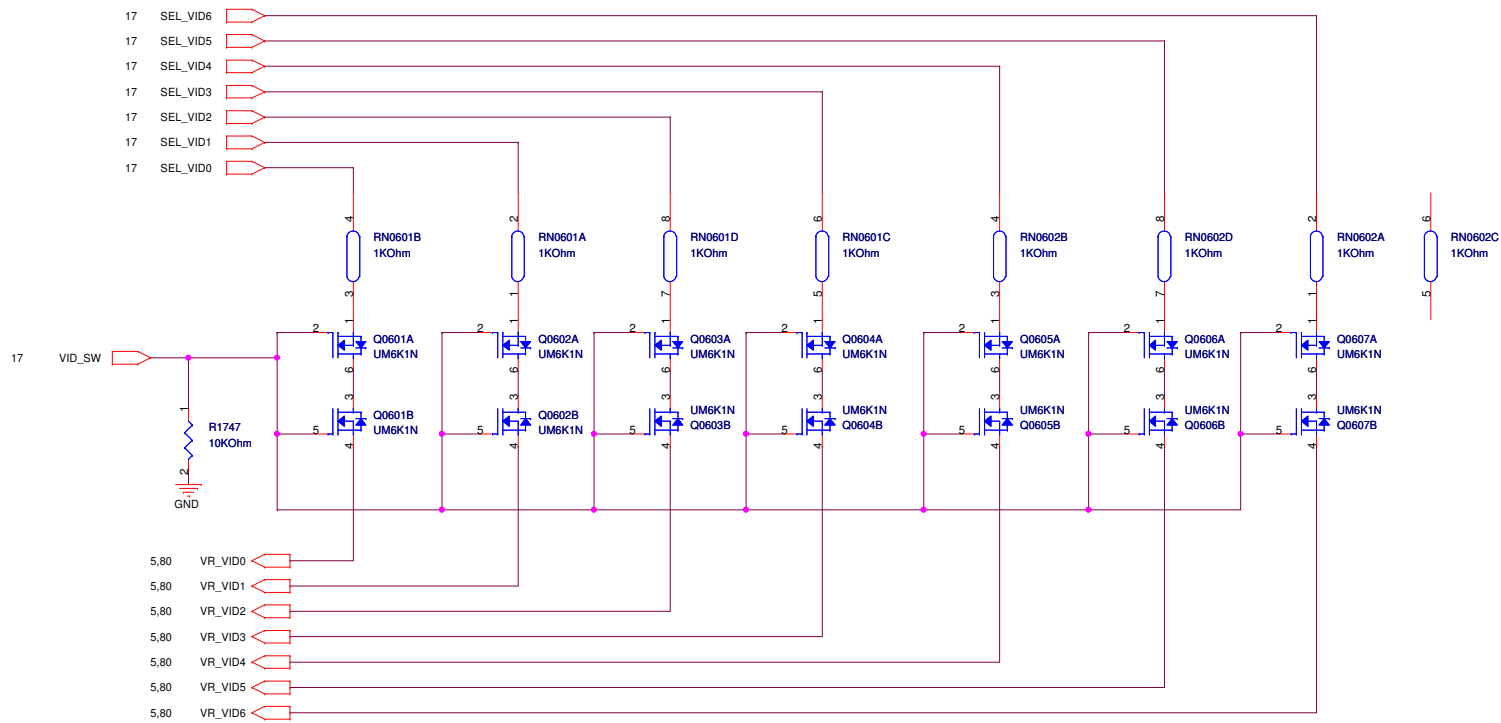
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1066	L	L	L

Default Strapping When Not Used



<Variant Name>

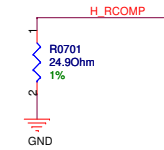




<Variant Name>

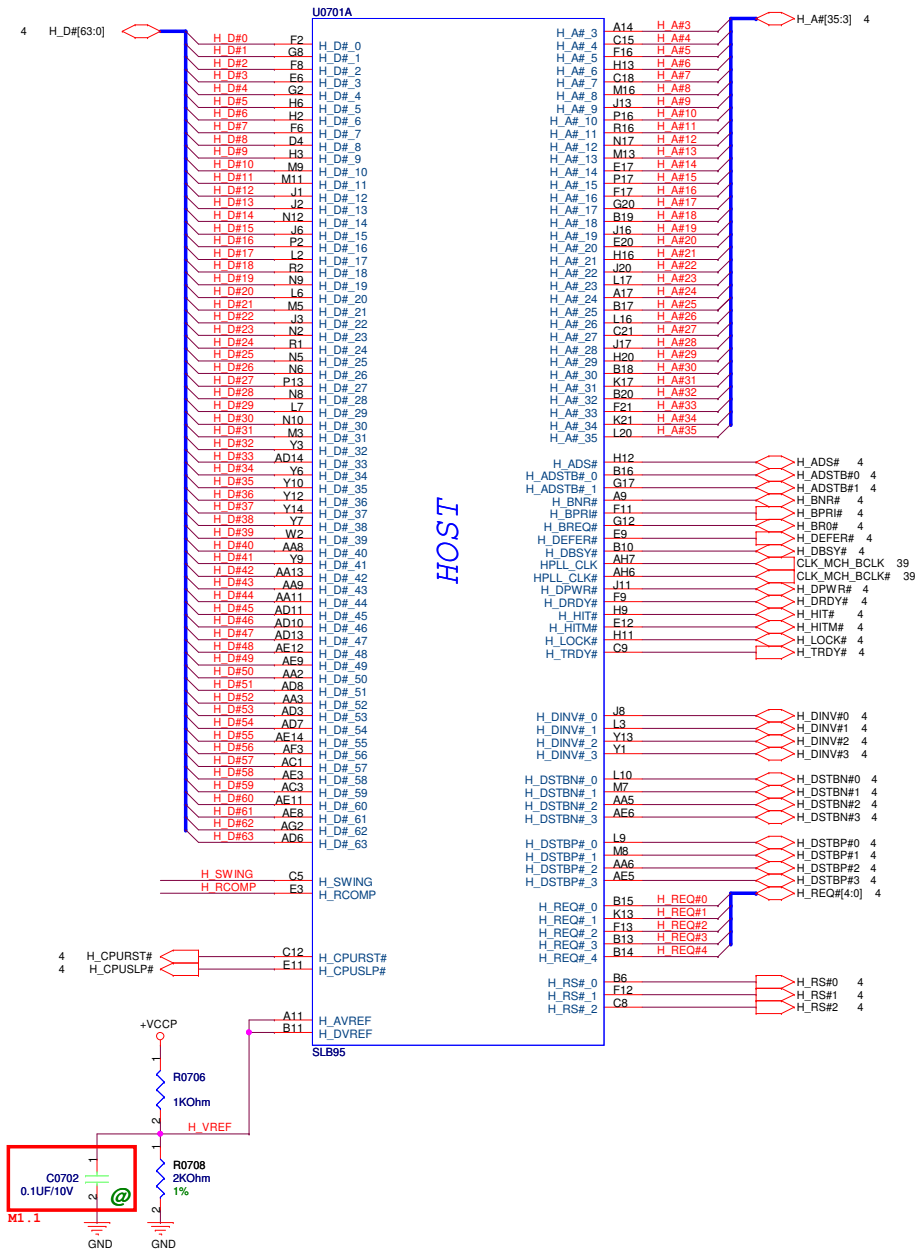
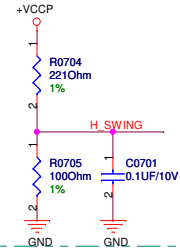
RCOMP

For Calibrating the FSB I/O Buffer

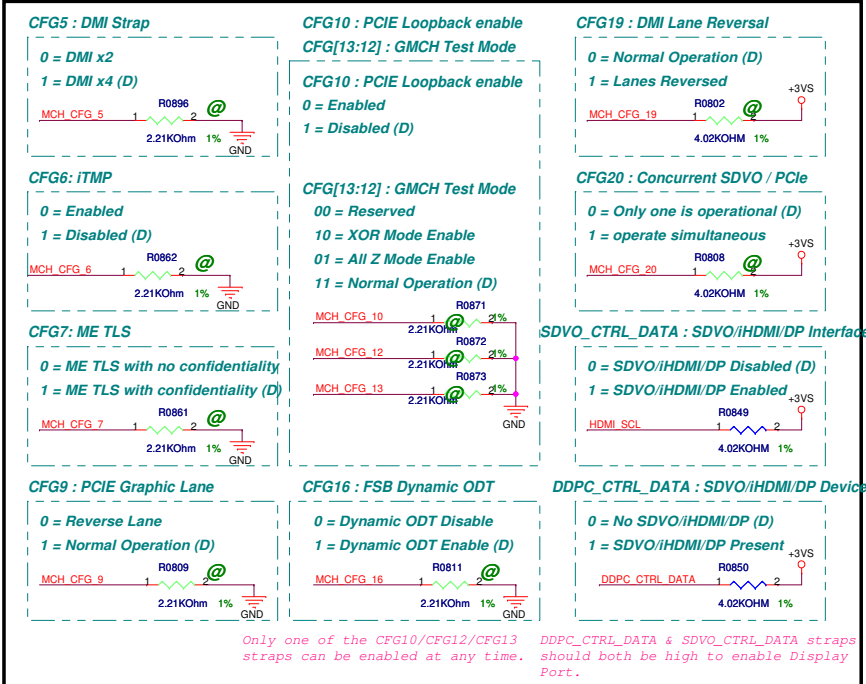


Voltage Swing

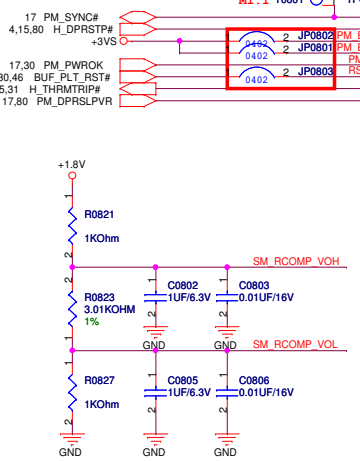
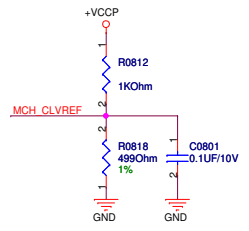
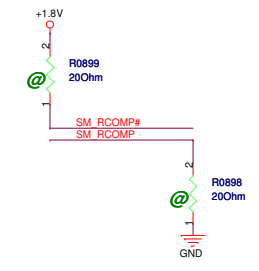
For Providing a Reference Voltage to The FSB RCOMP circuits



GMCH Strapping



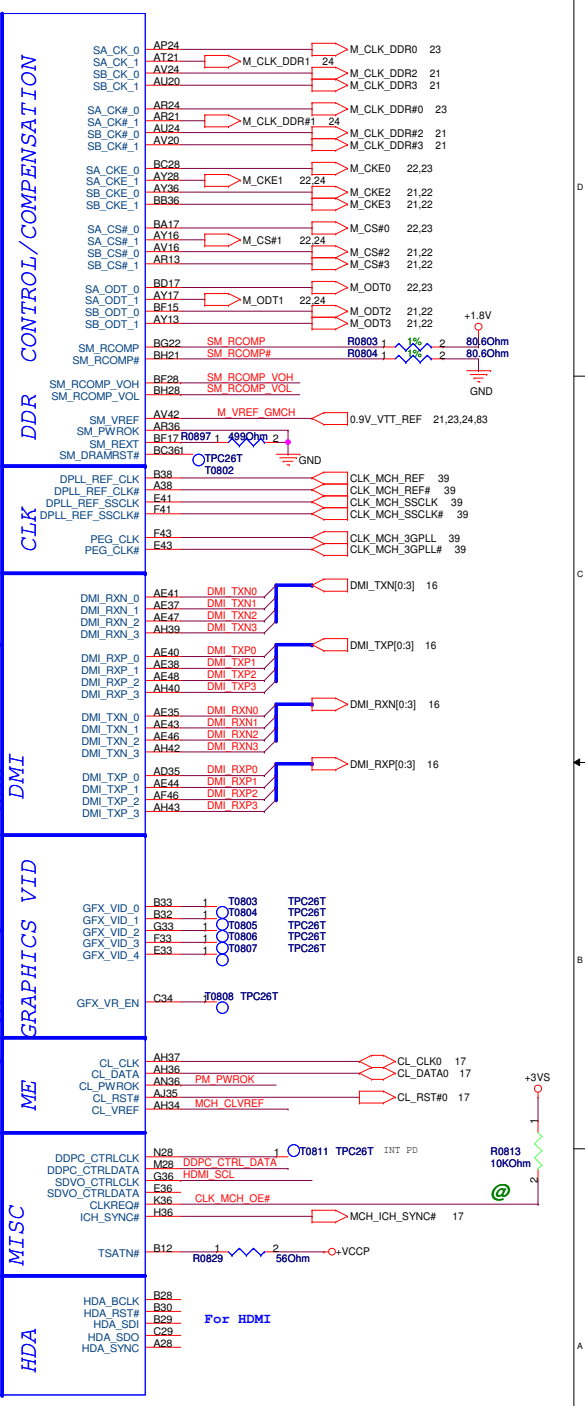
Only one of the CFG10/CFG12/CFG13 DDPG_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

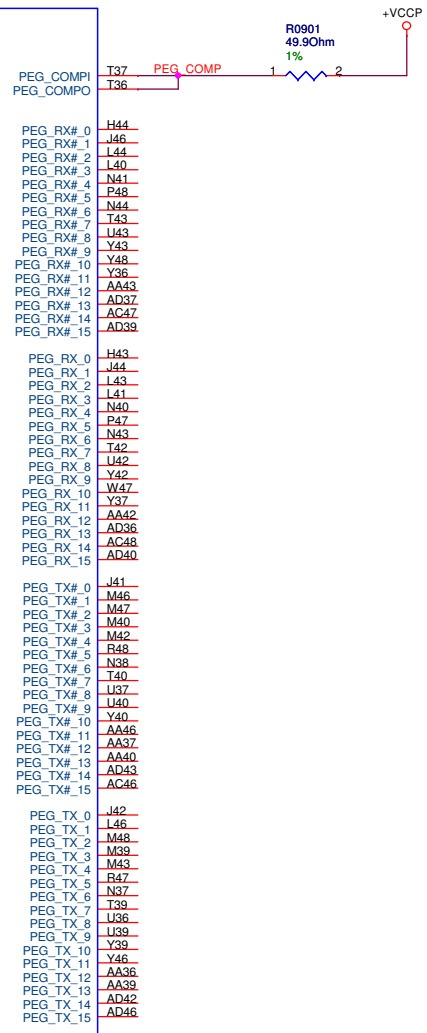
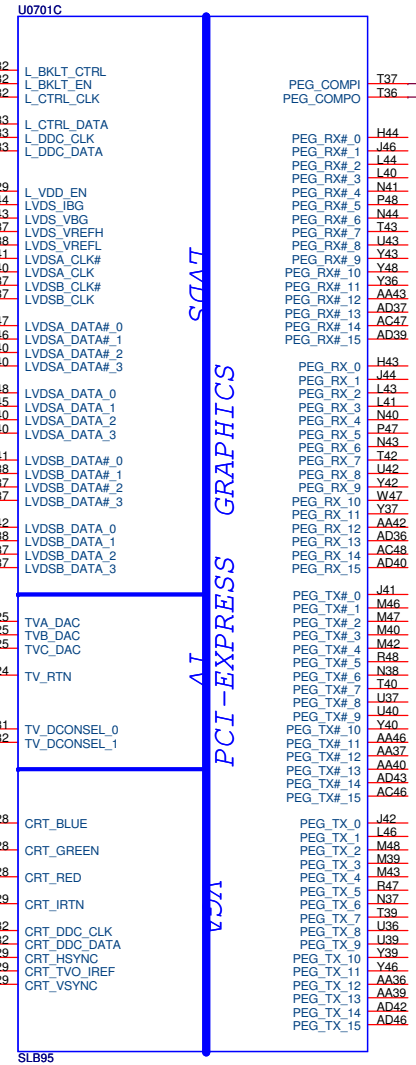
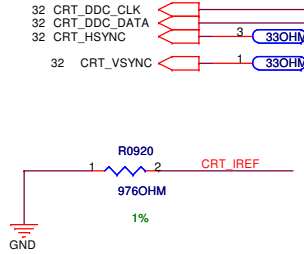
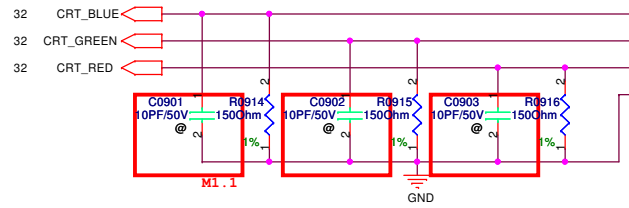
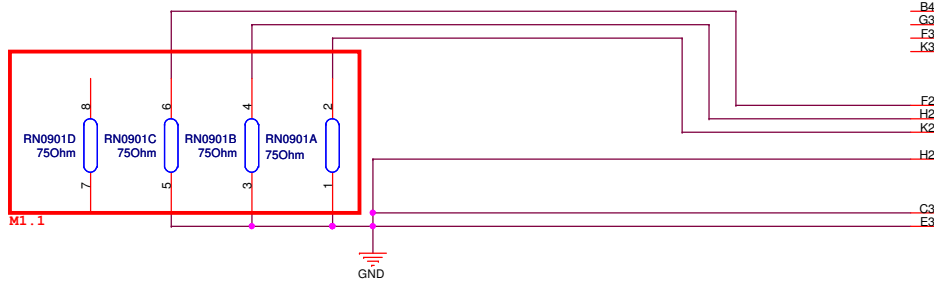
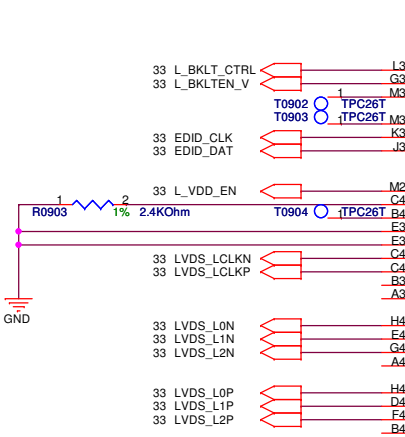
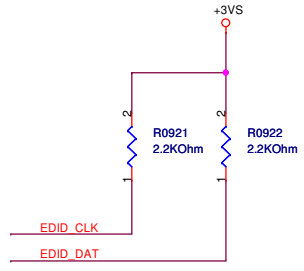


BCLK	FSB	BSEL2	BSEL1	BSEL0
266	1066	L	L	L
166	667	L	H	H
200	800	L	H	L

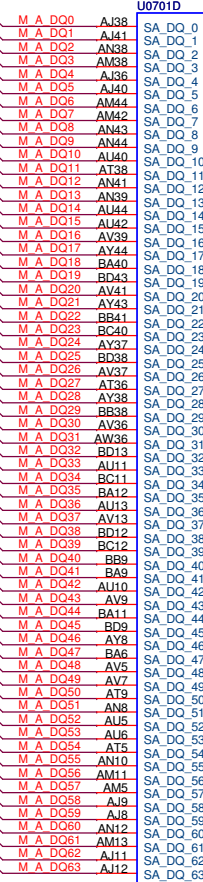
- 39 MCH_BSEL0
- 39 MCH_BSEL1
- 39 MCH_BSEL2
- MCH_CFG_5
- MCH_CFG_6
- MCH_CFG_7
- MCH_CFG_9
- MCH_CFG_10
- MCH_CFG_12
- MCH_CFG_13
- MCH_CFG_16
- MCH_CFG_19
- MCH_CFG_20

- M36
- N36
- F33
- T33
- AH9
- AH10
- AH12
- AH13
- K12
- AL34
- AK34
- AN35
- AM35
- T24
- B31
- AJ6
- M1
- AY21
- A47
- BG23
- BF23
- BH18
- BF18
- RSVD1
- RSVD2
- RSVD3
- RSVD4
- RSVD5
- RSVD6
- RSVD7
- RSVD8
- ME_JTAG_TCK
- ME_JTAG_TDI
- ME_JTAG_TDO
- ME_JTAG_TMS
- RSVD11
- VSS
- RSVD13
- RSVD14
- NC
- RSVD16
- RSVD17
- RSVD18
- RSVD19
- NC_1
- NC_2
- NC_3
- NC_4
- NC_5
- NC_6
- NC_7
- NC_8
- NC_9
- NC_10
- NC_11
- NC_12
- NC_13
- NC_14
- NC_15
- NC_16
- NC_17
- NC_18
- NC_19
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- NC_21
- NC_22
- NC_23
- NC_24
- NC_25

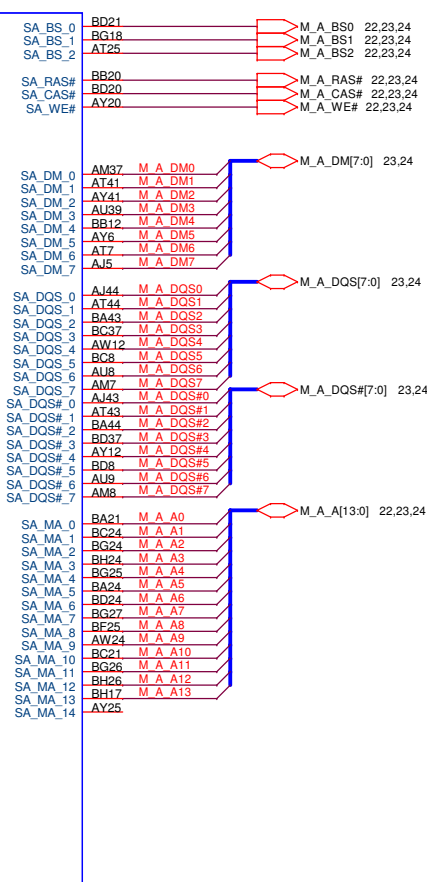




23,24 M_A_DQ[63:0]

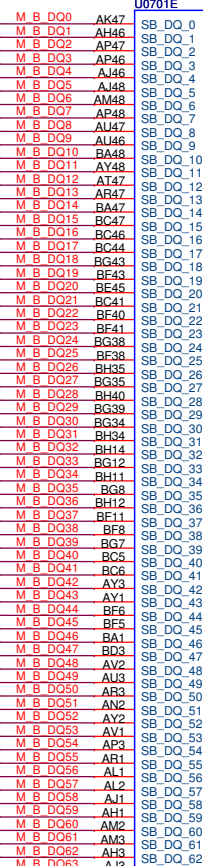


DDR SYSTEM MEMORY A

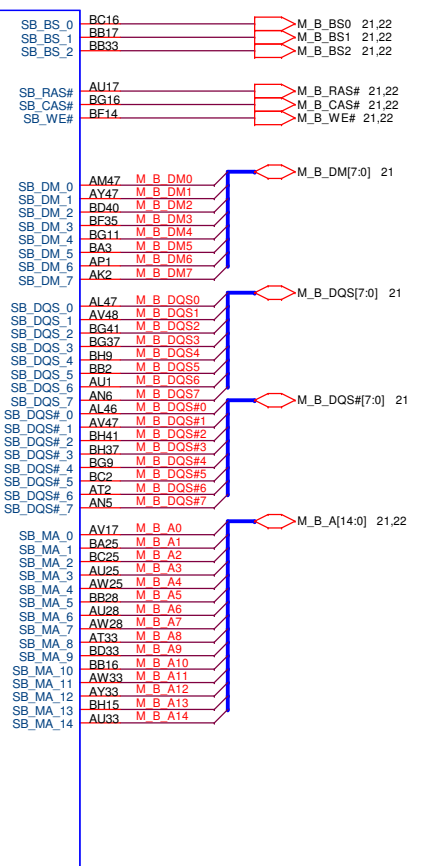


SLB95

21 M_B_DQ[63:0]



DDR SYSTEM MEMORY B



SLB95

<Variant Name>

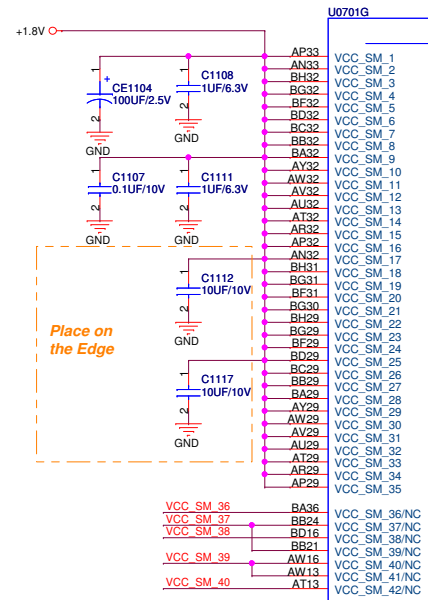


ASUSTeK COMPUTER INC. NB1 Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

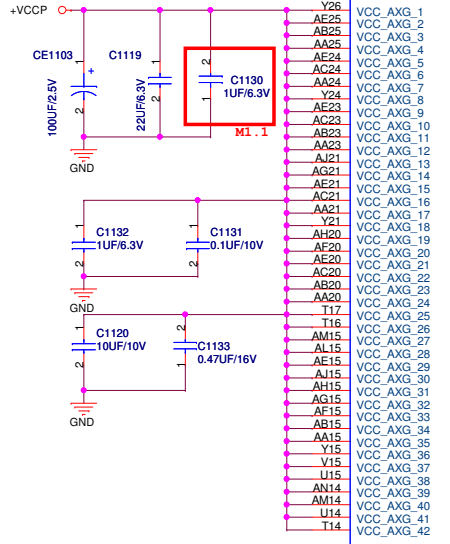
Date: Monday, March 09, 2009 Sheet 10 of 96

Max : 3000mA(DDR2)



- VCC_SM_36 BA36
- VCC_SM_37 BB24
- VCC_SM_38 BD16
- VCC_SM_39 BB21
- VCC_SM_40 AW16
- AW13
- AT13

Max : 8700mA(Graphic Core)



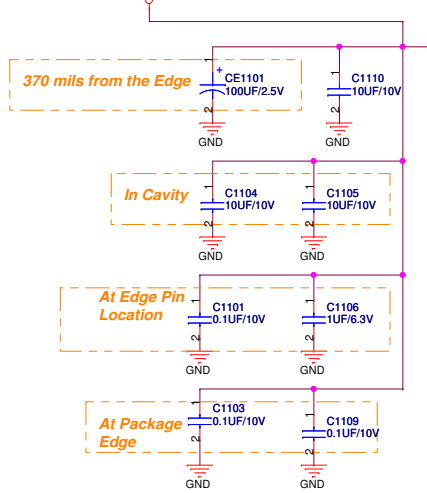
- VCC_AGX_1 Y26
- VCC_AGX_2 AE25
- VCC_AGX_3 AB25
- VCC_AGX_4 AA25
- VCC_AGX_5 AE24
- VCC_AGX_6 AC24
- VCC_AGX_7 Y24
- VCC_AGX_8 AE23
- VCC_AGX_9 AC23
- VCC_AGX_10 AB23
- VCC_AGX_11 AA23
- VCC_AGX_12 AJ21
- VCC_AGX_13 AC21
- VCC_AGX_14 AG21
- VCC_AGX_15 AE21
- VCC_AGX_16 AC21
- VCC_AGX_17 AA21
- VCC_AGX_18 Y21
- VCC_AGX_19 AH20
- VCC_AGX_20 AF20
- VCC_AGX_21 AC20
- VCC_AGX_22 AB20
- VCC_AGX_23 AA20
- VCC_AGX_24 TI17
- VCC_AGX_25 TI16
- VCC_AGX_26 AM15
- VCC_AGX_27 AL15
- VCC_AGX_28 AE15
- VCC_AGX_29 AH15
- VCC_AGX_30 AF15
- VCC_AGX_31 AG15
- VCC_AGX_32 AH15
- VCC_AGX_33 AF15
- VCC_AGX_34 AB15
- VCC_AGX_35 AA15
- VCC_AGX_36 Y15
- VCC_AGX_37 U15
- VCC_AGX_38 AN14
- VCC_AGX_39 AM14
- VCC_AGX_40 U14
- VCC_AGX_41 TI14
- VCC_AGX_42 TI14

- T1301 A14
- T1302 AH14

Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.

(Graph Core)

Max : 2900mA(Core)

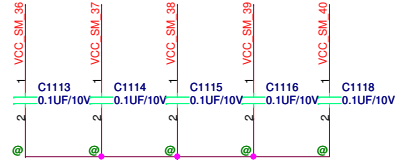


- VCC_1 AG34
- VCC_2 AC34
- VCC_3 AB34
- VCC_4 AA34
- VCC_5 Y34
- VCC_6 U34
- VCC_7 AM33
- VCC_8 AK33
- VCC_9 AJ33
- VCC_10 AG33
- VCC_11 AF33
- VCC_12 AE33
- VCC_13 AC33
- VCC_14 AA33
- VCC_15 Y33
- VCC_16 U33
- VCC_17 W33
- VCC_18 V33
- VCC_19 U33
- VCC_20 AH28
- VCC_21 AF28
- VCC_22 AC28
- VCC_23 AA28
- VCC_24 AG26
- VCC_25 AE26
- VCC_26 AC26
- VCC_27 AH25
- VCC_28 AG25
- VCC_29 AF25
- VCC_30 AG24
- VCC_31 AJ23
- VCC_32 AH23
- VCC_33 AF23
- VCC_34 T32

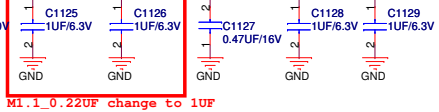
VCC CORE POWER

VCC NCTF

- VCC_NCTF_1 AM32
- VCC_NCTF_2 AL32
- VCC_NCTF_3 AK32
- VCC_NCTF_4 AH32
- VCC_NCTF_5 AG32
- VCC_NCTF_6 AE32
- VCC_NCTF_7 AC32
- VCC_NCTF_8 AA32
- VCC_NCTF_9 Y32
- VCC_NCTF_10 W32
- VCC_NCTF_11 U32
- VCC_NCTF_12 U32
- VCC_NCTF_13 AM30
- VCC_NCTF_14 AL30
- VCC_NCTF_15 AH30
- VCC_NCTF_16 AG30
- VCC_NCTF_17 AB30
- VCC_NCTF_18 AF30
- VCC_NCTF_19 AC30
- VCC_NCTF_20 AB30
- VCC_NCTF_21 AE29
- VCC_NCTF_22 AA30
- VCC_NCTF_23 W30
- VCC_NCTF_24 V30
- VCC_NCTF_25 U30
- VCC_NCTF_26 U30
- VCC_NCTF_27 AL29
- VCC_NCTF_28 AK29
- VCC_NCTF_29 AH29
- VCC_NCTF_30 AG29
- VCC_NCTF_31 AE29
- VCC_NCTF_32 AC29
- VCC_NCTF_33 AA29
- VCC_NCTF_34 Y29
- VCC_NCTF_35 W29
- VCC_NCTF_36 V29
- VCC_NCTF_37 U29
- VCC_NCTF_38 AL28
- VCC_NCTF_39 AK28
- VCC_NCTF_40 AL26
- VCC_NCTF_41 AK26
- VCC_NCTF_42 AK25
- VCC_NCTF_43 AK24
- VCC_NCTF_44 AK23

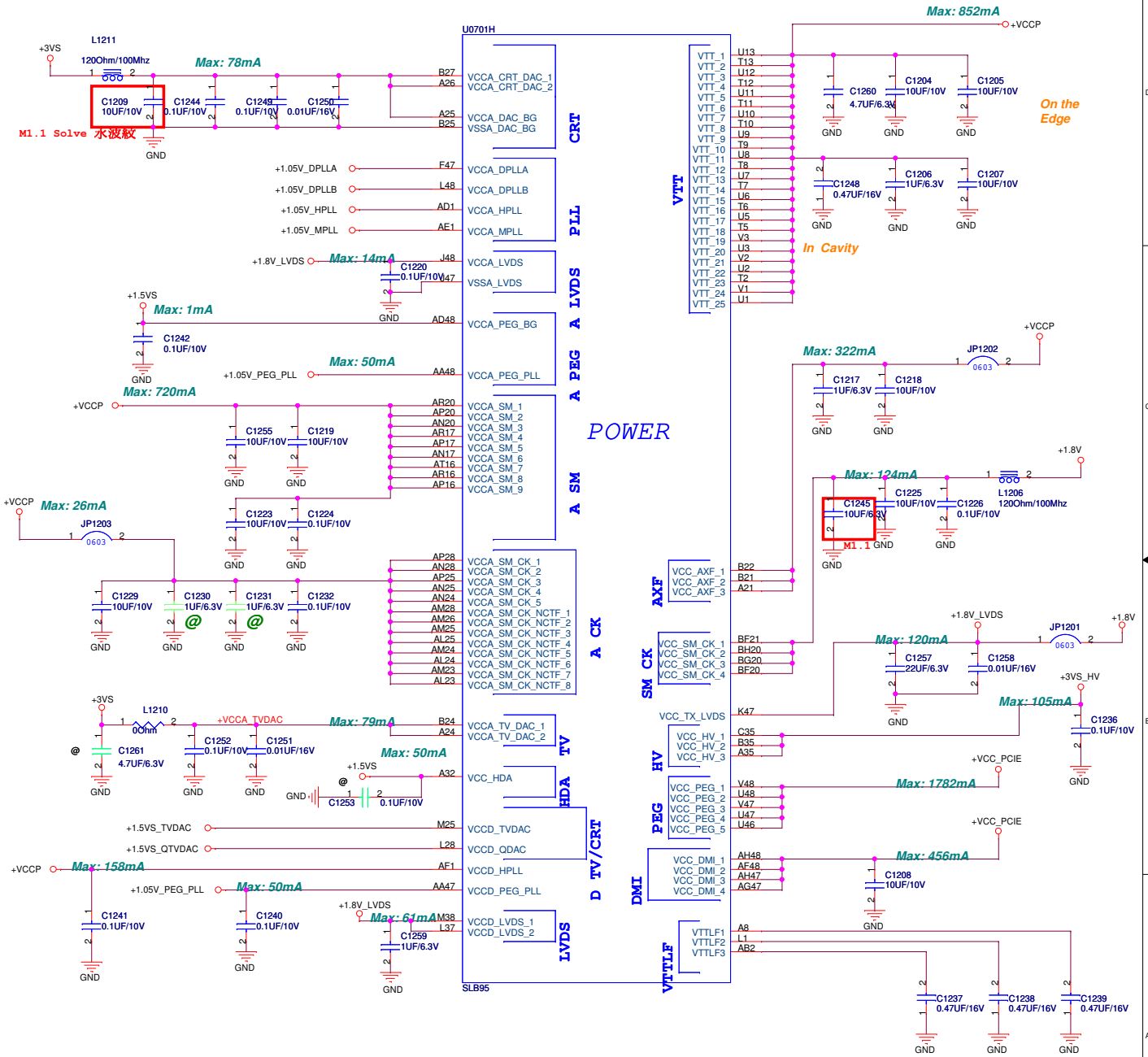
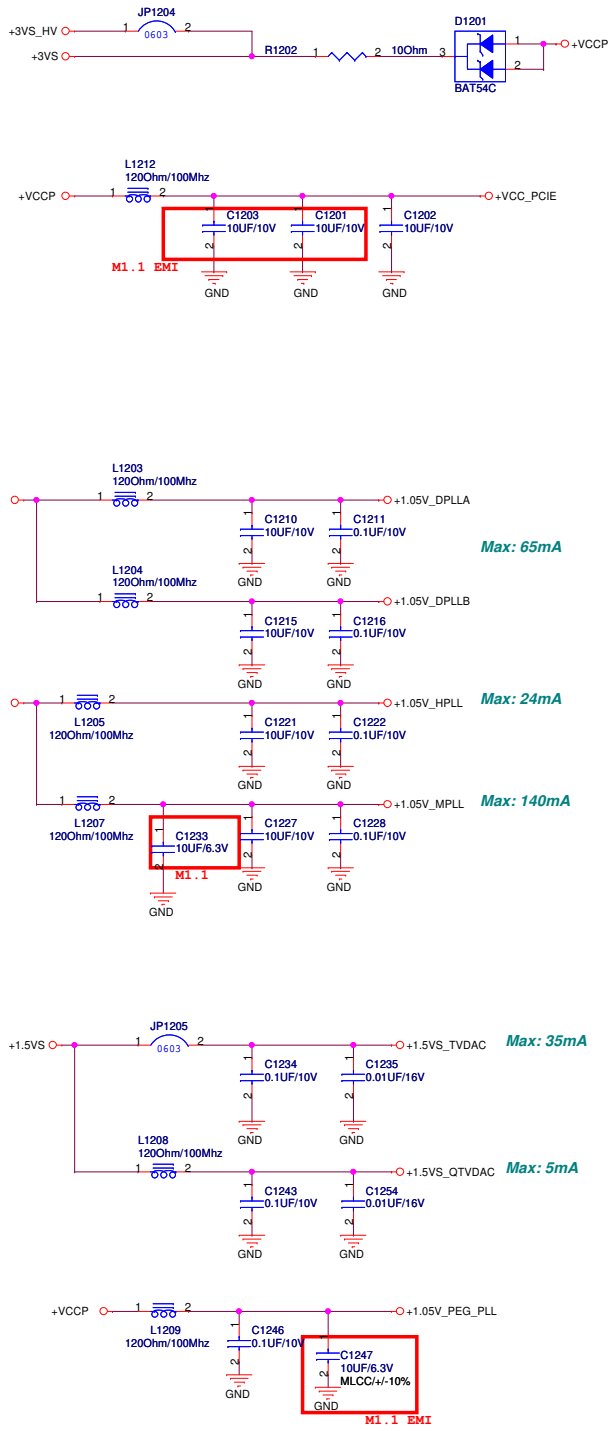


- VCC_SM_LF1 AV44
- VCC_SM_LF2 BA37
- VCC_SM_LF3 AM40
- VCC_SM_LF4 AV21
- VCC_SM_LF5 AV5
- VCC_SM_LF6 AM10
- VCC_SM_LF7 BB13



-Variant Name-

ASUS		Title : NB_Cantiga(PWR)	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet	11	of 96



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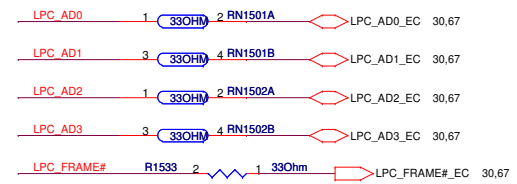
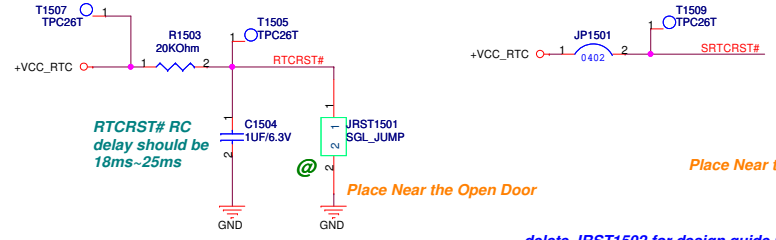
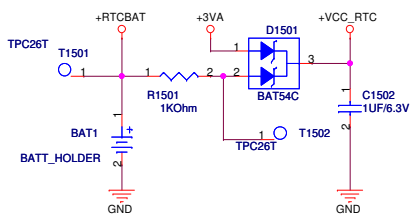
B

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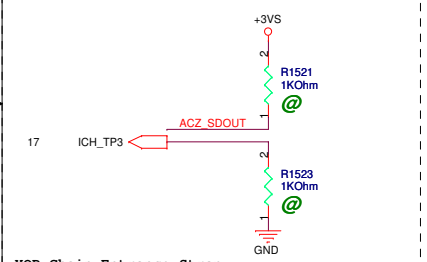
<Variant Name>

		Title : Schematic page name
ASUSTeK COMPUTER INC		Engineer: N/A
Size	Project Name	Rev
C	K40LJ/K50LJ	1.1
Date: Monday, March 09, 2009		Sheet 14 of 95



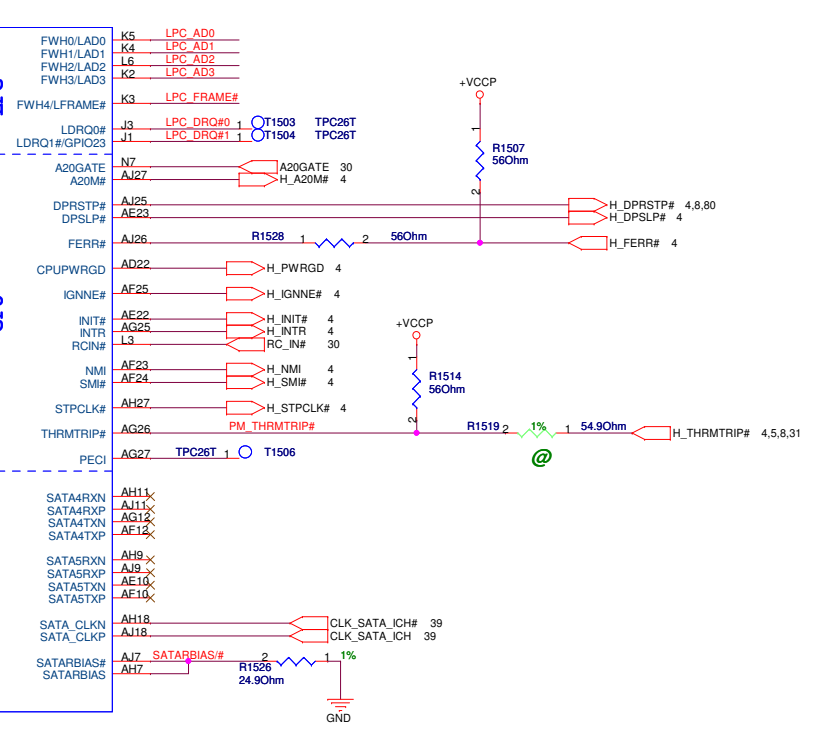
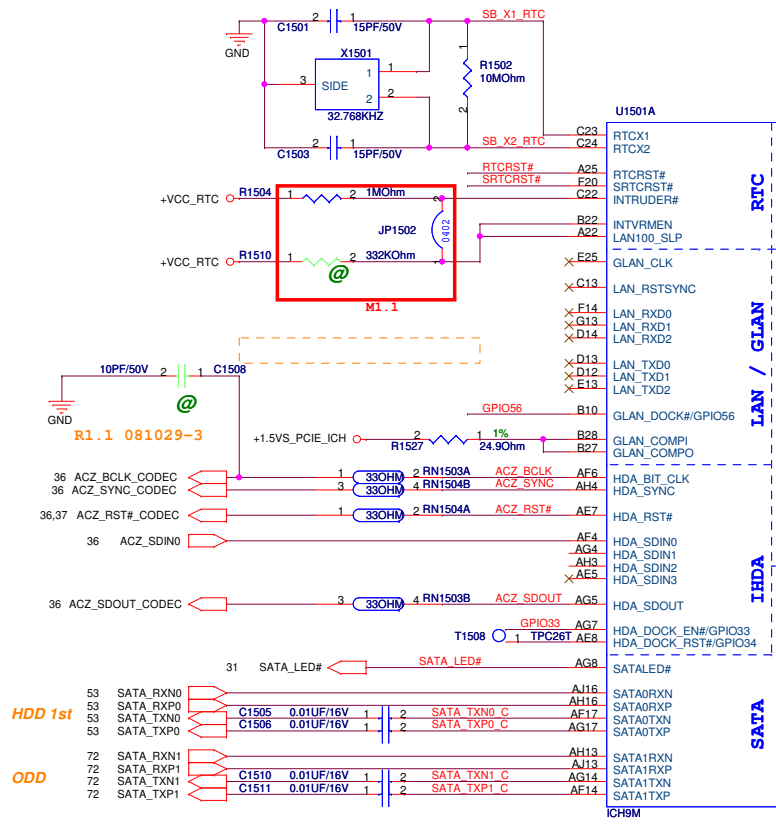
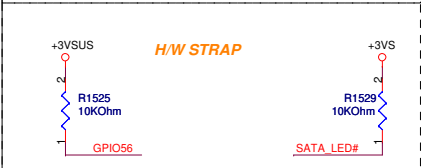
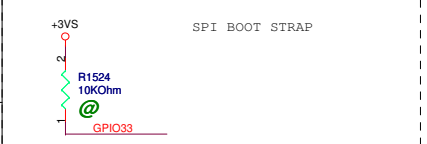
delete JRS1502 for design guide recommendation.

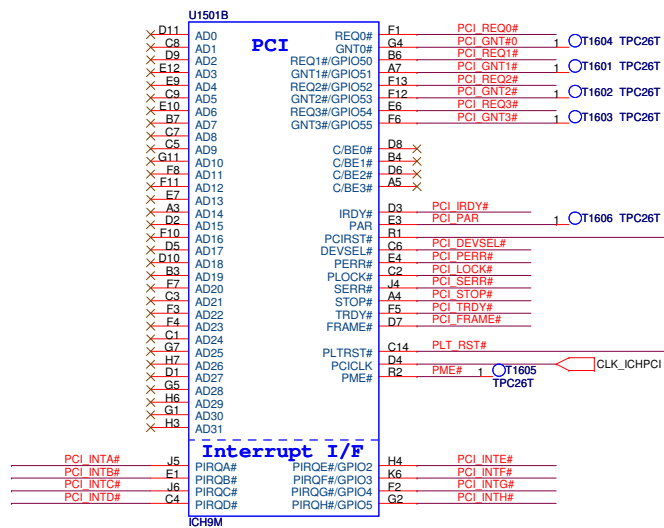
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
 Low - Disabled Internal VR
 High - Enable Internal VR(D)
 ICH_LAN100(VCCLAN1_05,VCCCL1_05)
 Low - Disabled Internal VR
 High - Enable Internal VR(D)



XOR Chain Entrance Strap

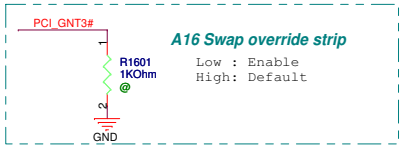
ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1



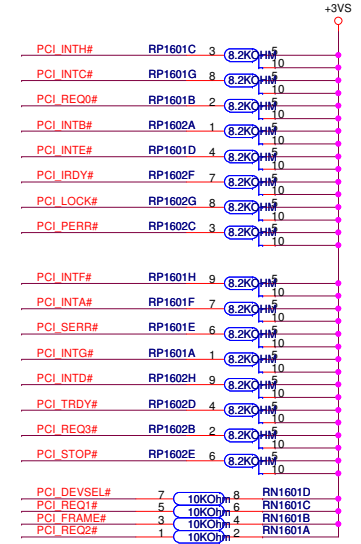


ICH8 Boot BIOS Select

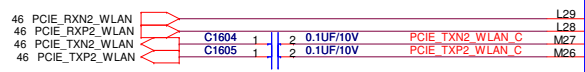
	GNT#0	CS#1
LPC	H	H
PCI	H	L
SPI	L	H



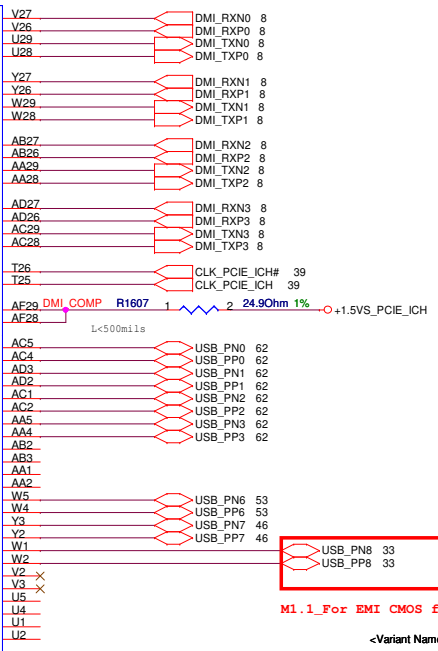
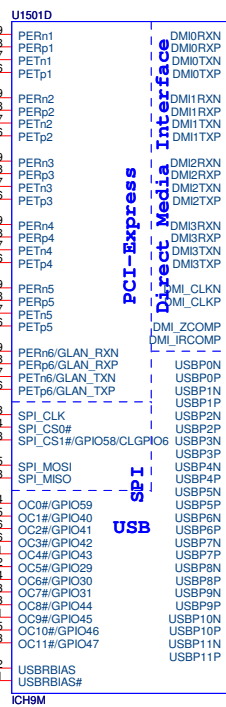
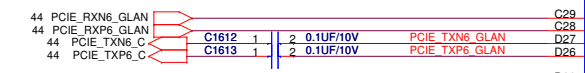
Buffer to Reduce Loading on PLT_RST#



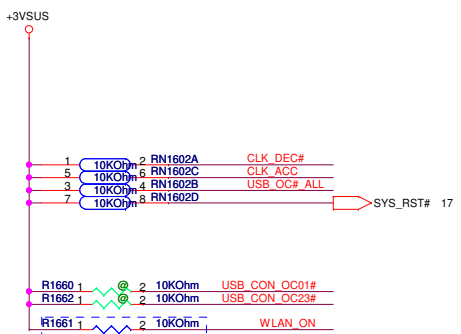
WLAN



GLAN



USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	USB Conn.(M/B)
USB 4	Reverse
USB 5	Reverse
USB 6	Card Reader
USB 7	WLAN
USB 8	CMOS Camera(D/B)
USB 9	Reverse
USB 10	Reverse
USB 11	Reverse



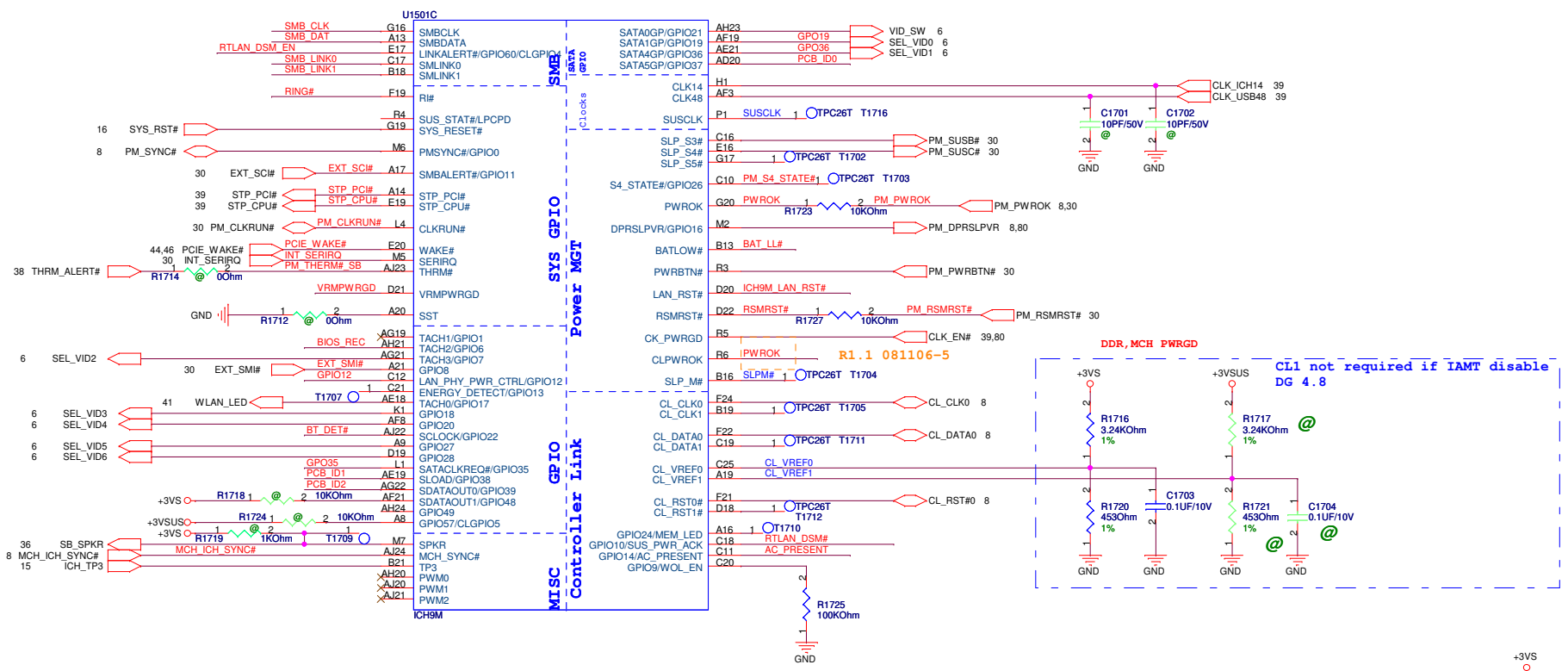
When supporting CLK GEN Turbo PIN, un-mount R1661.

ASUS Title : SB-ICH9M(2)

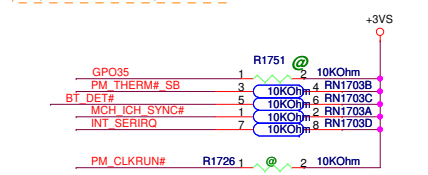
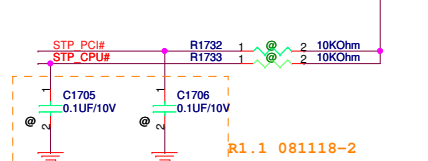
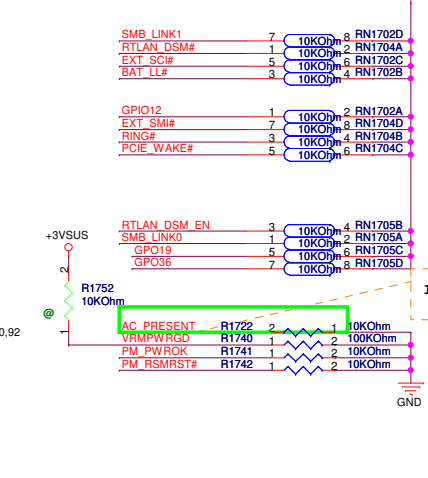
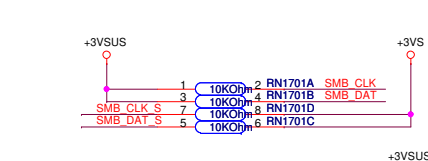
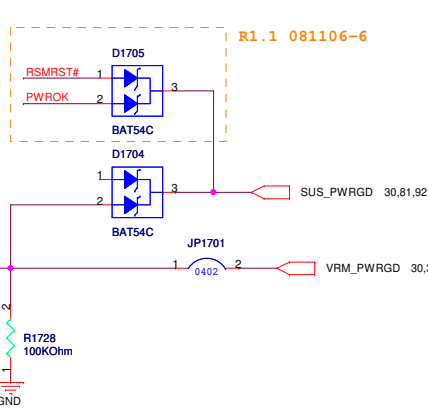
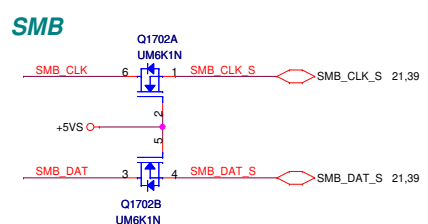
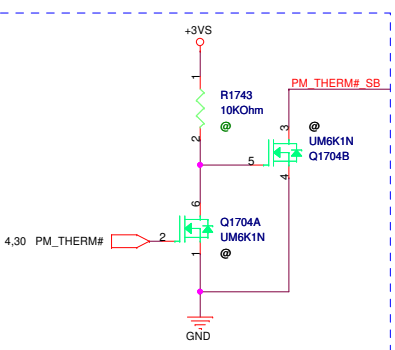
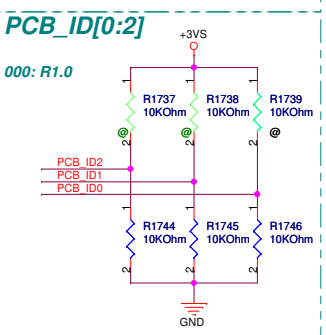
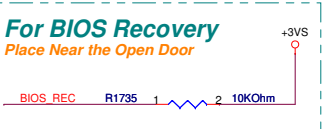
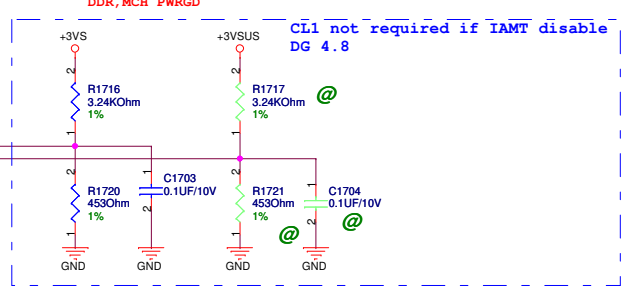
ASUSTek COMPUTER INC. NBI Engineer: N/A

Size Project Name
Custom K40J/K50J

Date: Monday, March 09, 2009 Sheet 16 of 96

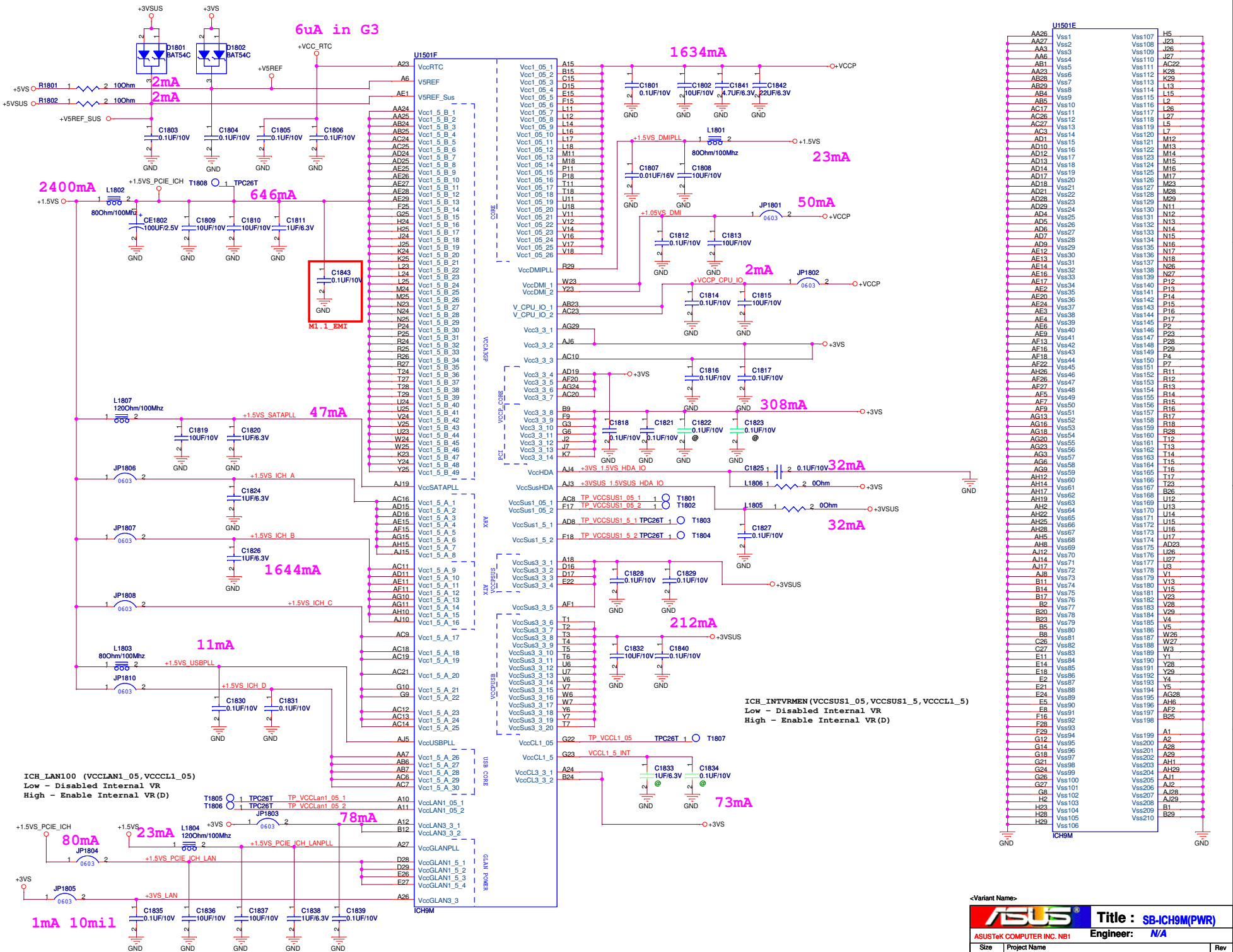


No Reboot Strap
Low = Default
High = No Reboot



If mount Q1701, VRMPWRGD must be pulled high.

ASUS Title : SB-ICH9M(3)
ASUSTek COMPUTER INC. NBI Engineer: N/A
Size Project Name
Custom K40IJ/K50IJ
Date: Monday, March 09, 2009 Sheet 17 of 96



U1501E

AA26	Vss1	Vss107
AA27	Vss2	Vss108
AA3	Vss3	Vss109
AA6	Vss4	Vss110
AB1	Vss5	Vss111
AB2	Vss6	Vss112
AB3	Vss7	Vss113
AB4	Vss8	Vss114
AB5	Vss9	Vss115
AC17	Vss10	Vss116
AC26	Vss11	Vss117
AC27	Vss12	Vss118
AC3	Vss13	Vss119
AD1	Vss14	Vss120
AD10	Vss15	Vss121
AD12	Vss16	Vss122
AD13	Vss17	Vss123
AD14	Vss18	Vss124
AD17	Vss19	Vss125
AD18	Vss20	Vss126
AD21	Vss21	Vss127
AD22	Vss22	Vss128
AD23	Vss23	Vss129
AD29	Vss24	Vss130
AD4	Vss25	Vss131
AD5	Vss26	Vss132
AD6	Vss27	Vss133
AD7	Vss28	Vss134
AD9	Vss29	Vss135
AE12	Vss30	Vss136
AE13	Vss31	Vss137
AE14	Vss32	Vss138
AE16	Vss33	Vss139
AE17	Vss34	Vss140
AE20	Vss35	Vss141
AE24	Vss36	Vss142
AE3	Vss37	Vss143
AE4	Vss38	Vss144
AE6	Vss39	Vss145
AE9	Vss40	Vss146
AF13	Vss41	Vss147
AF16	Vss42	Vss148
AF18	Vss43	Vss149
AF22	Vss44	Vss150
AH26	Vss45	Vss151
AE26	Vss46	Vss152
AF27	Vss47	Vss153
AE5	Vss48	Vss154
AF7	Vss49	Vss155
AF9	Vss50	Vss156
AG13	Vss51	Vss157
AG16	Vss52	Vss158
AG18	Vss53	Vss159
AG20	Vss54	Vss160
AG23	Vss55	Vss161
AG3	Vss56	Vss162
AG6	Vss57	Vss163
AG9	Vss58	Vss164
AH12	Vss59	Vss165
AH14	Vss60	Vss166
AH17	Vss61	Vss167
AH19	Vss62	Vss168
AH2	Vss63	Vss169
AH22	Vss64	Vss170
AH25	Vss65	Vss171
AH28	Vss66	Vss172
AH5	Vss67	Vss173
AH8	Vss68	Vss174
AH12	Vss69	Vss175
AH14	Vss70	Vss176
AH17	Vss71	Vss177
AH8	Vss72	Vss178
B11	Vss73	Vss179
B14	Vss74	Vss180
B17	Vss75	Vss181
B2	Vss76	Vss182
B23	Vss77	Vss183
B25	Vss78	Vss184
B5	Vss79	Vss185
B8	Vss80	Vss186
C27	Vss81	Vss187
C27	Vss82	Vss188
E11	Vss83	Vss189
E18	Vss84	Vss190
E18	Vss85	Vss191
E2	Vss86	Vss192
E21	Vss87	Vss193
E2	Vss88	Vss194
E4	Vss89	Vss195
E5	Vss90	Vss196
E8	Vss91	Vss197
F16	Vss92	Vss198
F28	Vss93	Vss199
F29	Vss94	Vss200
G12	Vss95	Vss201
G14	Vss96	Vss202
G21	Vss97	Vss203
G24	Vss98	Vss204
G26	Vss99	Vss205
G27	Vss100	Vss206
H2	Vss101	Vss207
H2	Vss102	Vss208
H23	Vss103	Vss209
H28	Vss104	Vss210
H29	Vss105	Vss210
H29	Vss106	Vss210

ICH_INTVRMEN (VCCSUS1_05, VCCSUS1_5, VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR (D)

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	19 of 96

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<Variant Name>

		Title : DDR2 SO-DIMM0
ASUSTeK COMPUTER INC. NB1		Engineer: N/A

Size	Project Name	Rev
A3	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009		Sheet 20 of 96

5

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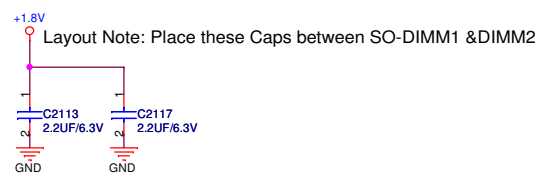
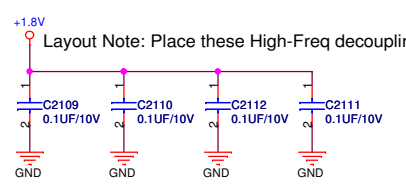
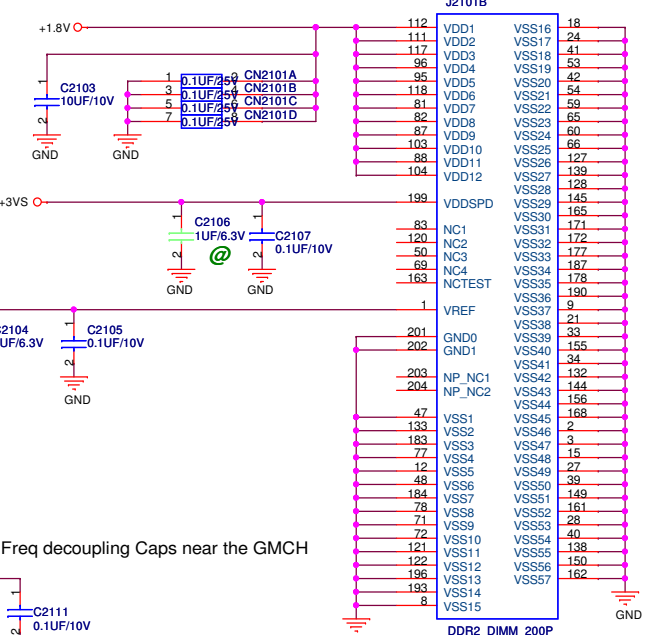
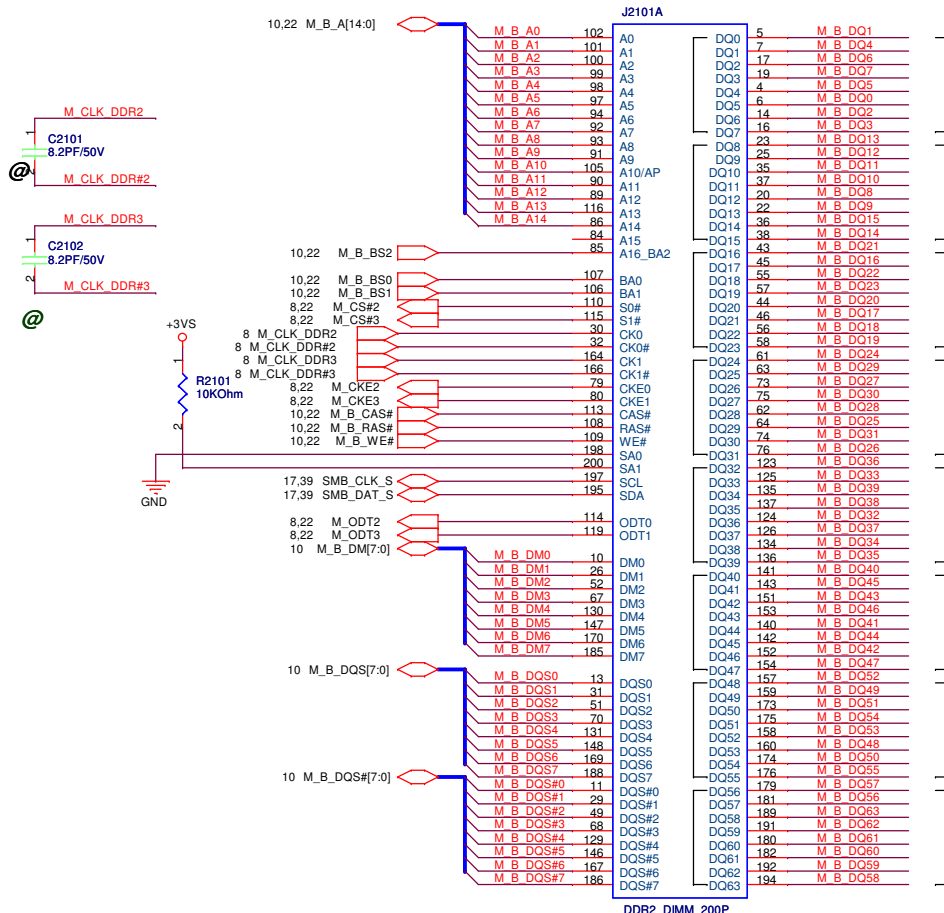
3

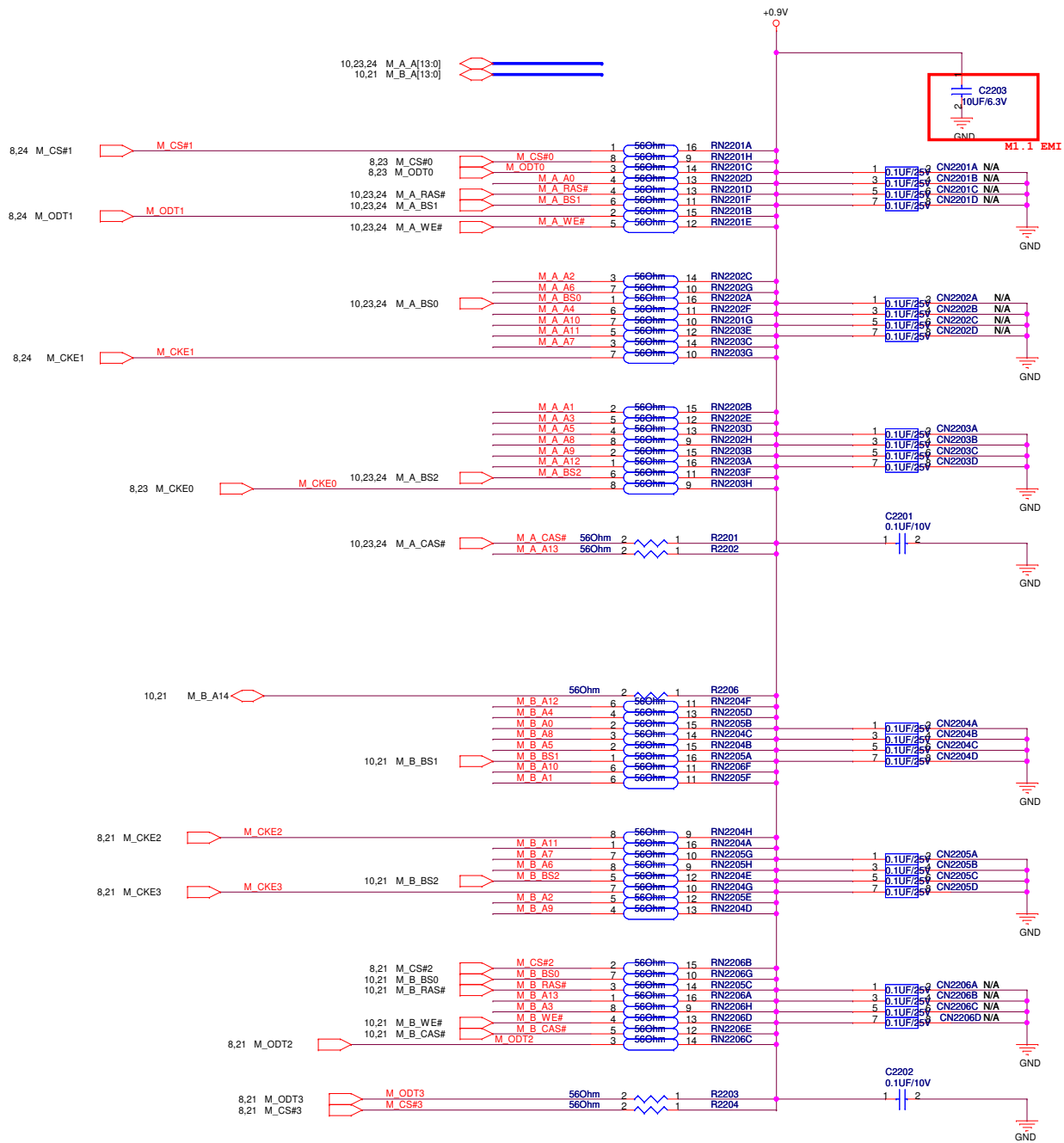
2

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DDR2 200P H=9.2mm (Reverse Type)

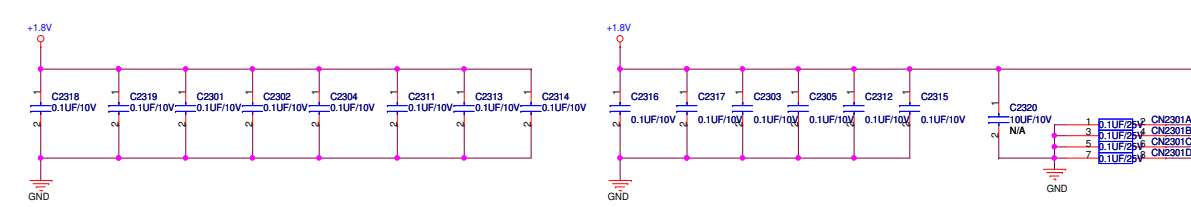
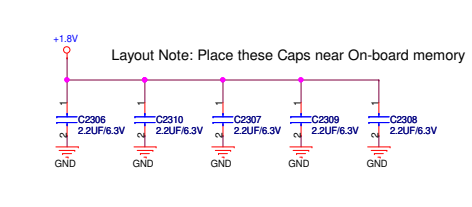
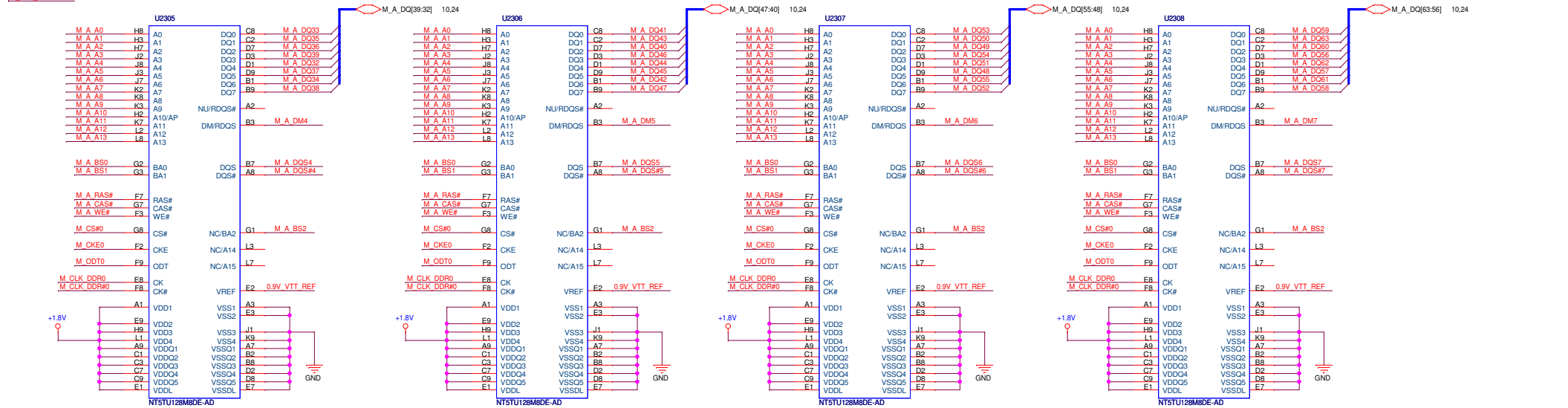
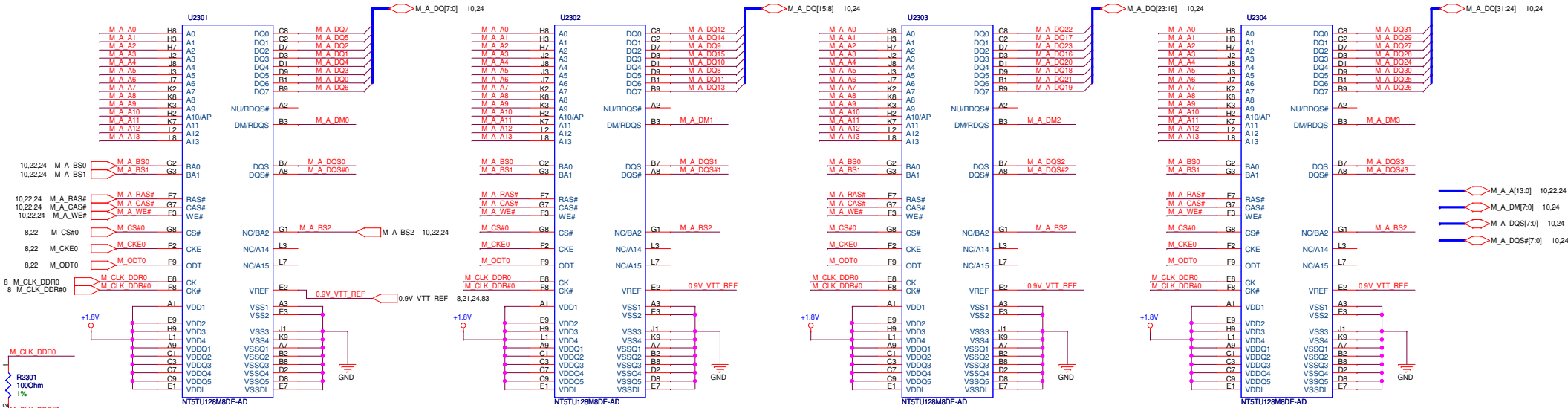
M_B_DQ[63:0] 10





<Variant Name>

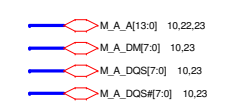
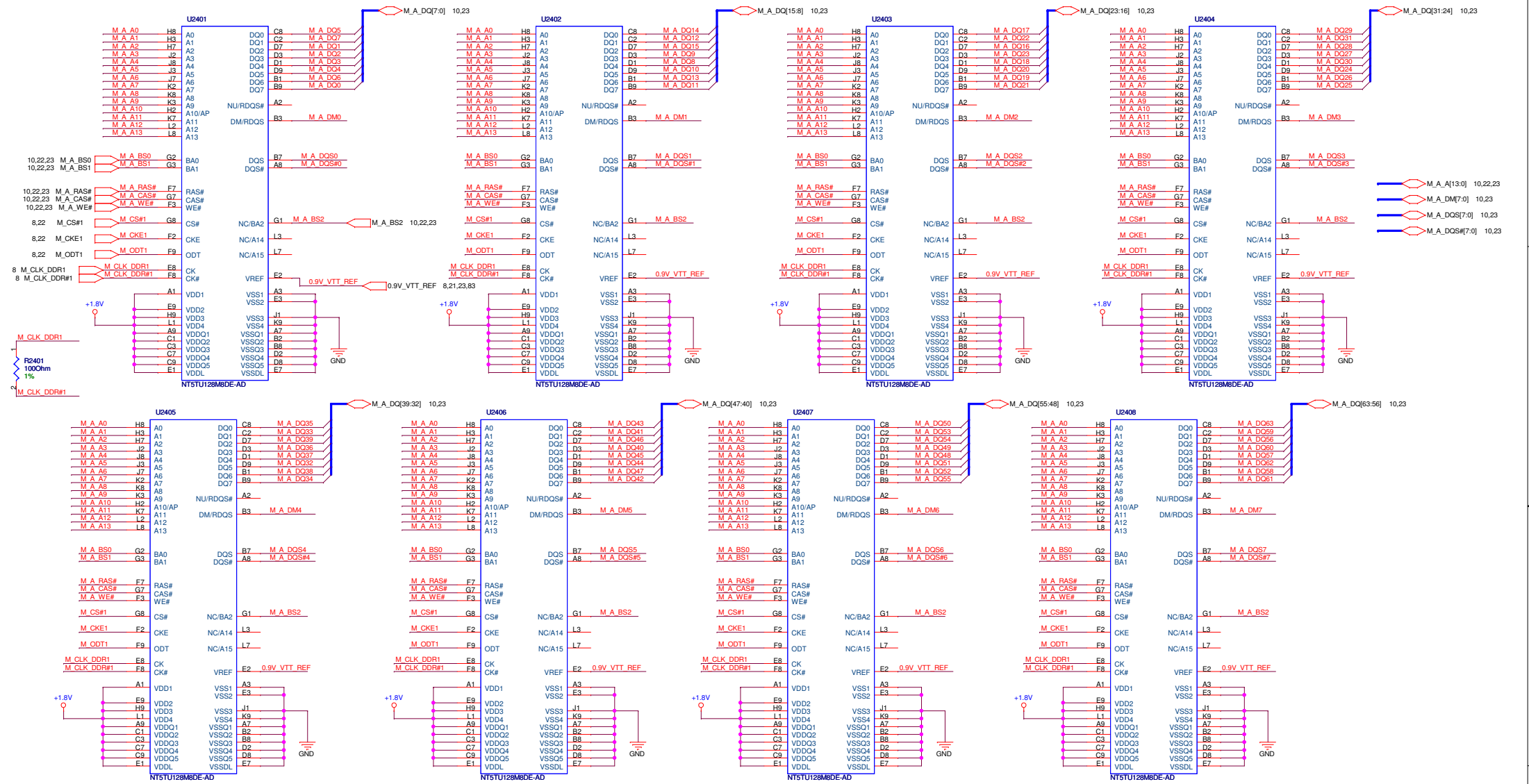
ASUS		Title : DDR2 TERMINATION	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet	22	of 96

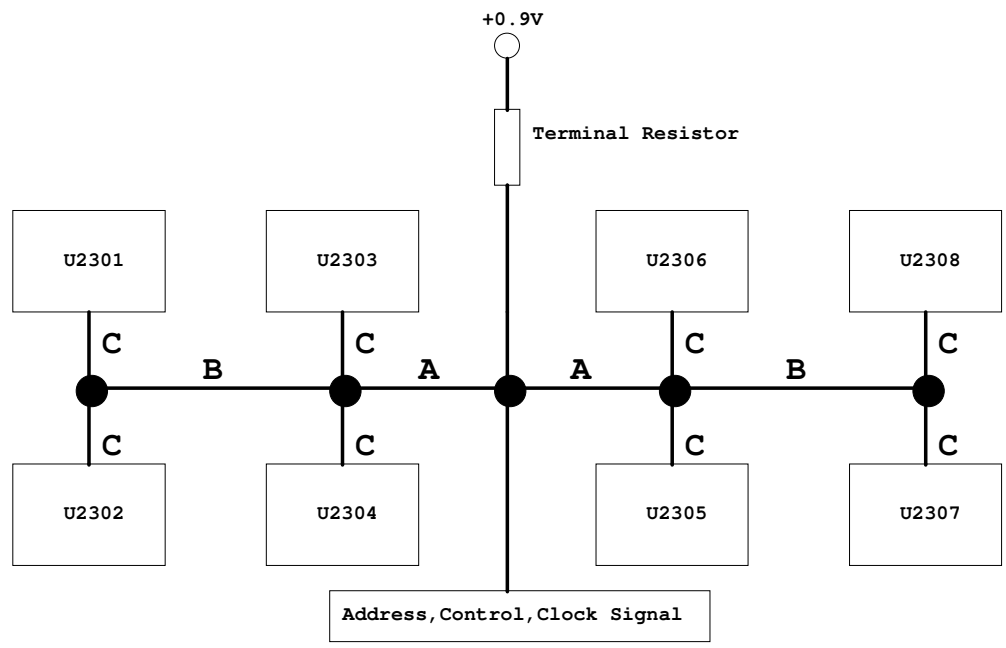


Legend:

- M_A_A[13:0] 10.22.24
- M_A_DM[7:0] 10.24
- M_A_DSQ[7:0] 10.24
- M_A_DSQ[7:0] 10.24

ASUS
Title : Schematic page name
 ASUSTek COMPUTER INC Engineer: N/A
 Size Project Name
 Custom **K40LJ/K50LJ**
 Date: Monday, March 09, 2009 Sheet 23 of 96





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<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: Alex&Bruce	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	26 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet 27	of 96	

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B

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A

<Variant Name>

		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet	28	of 96

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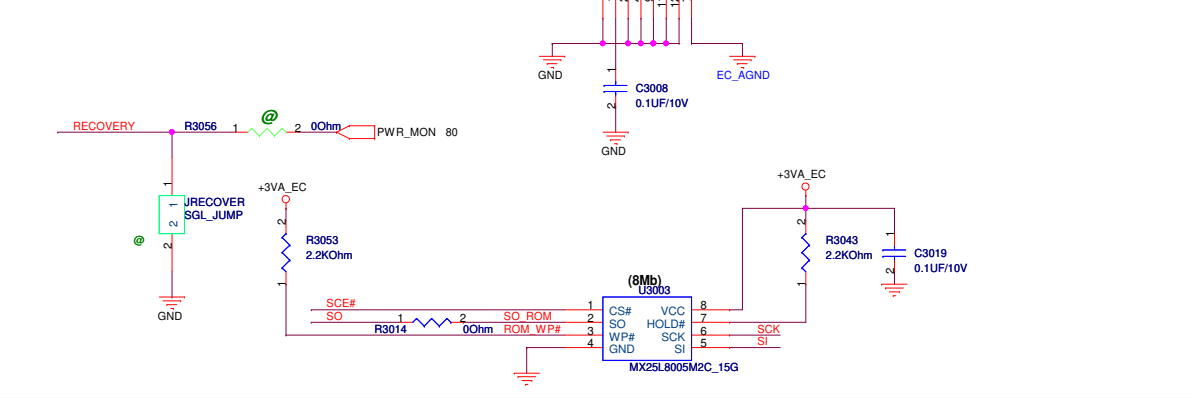
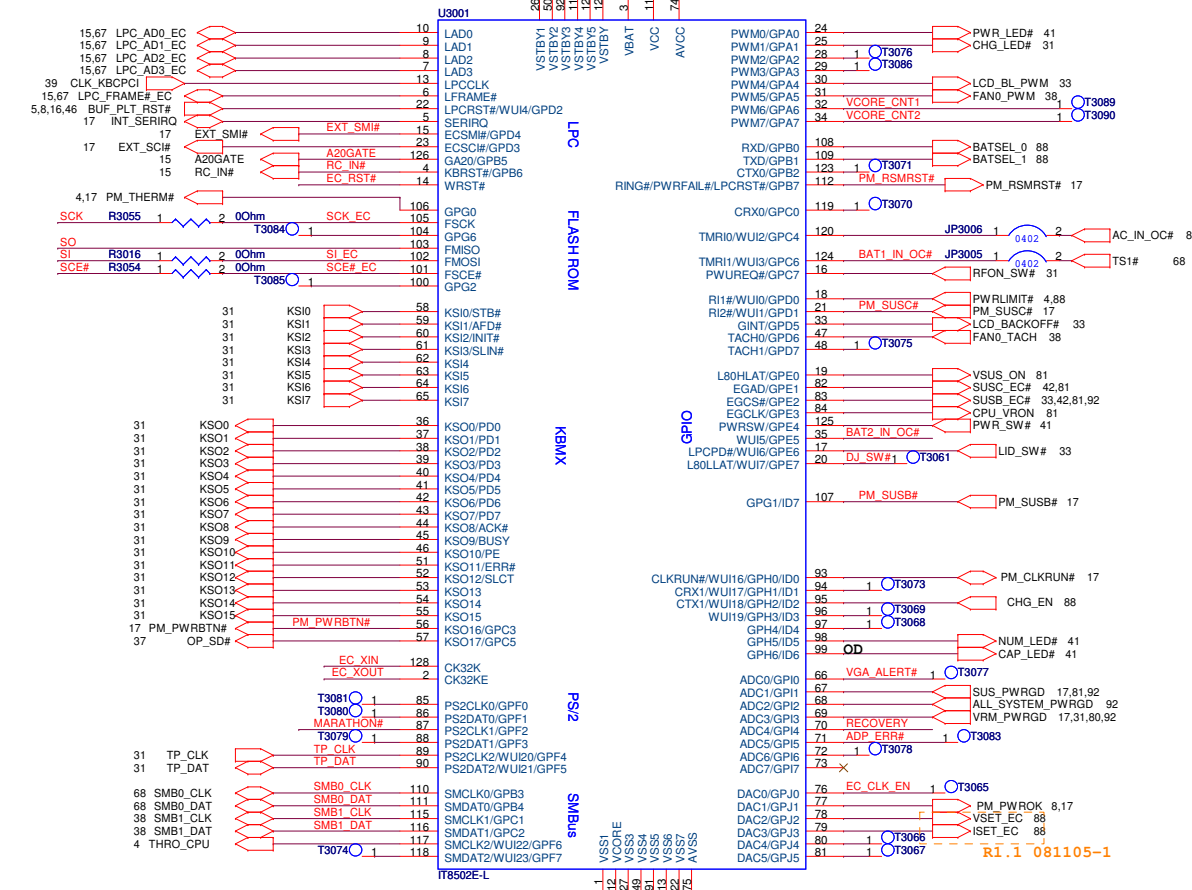
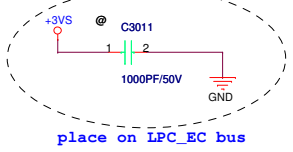
B

A

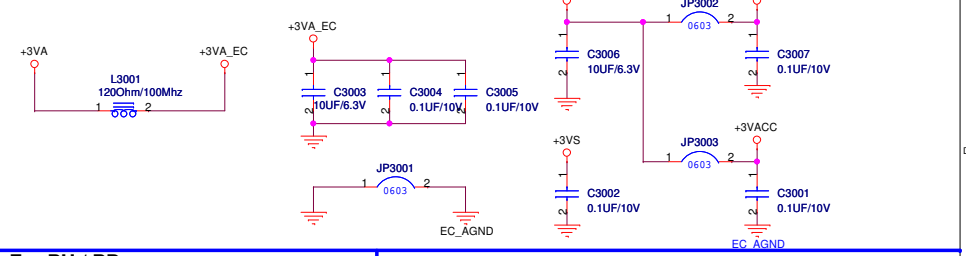
A

<Variant Name>

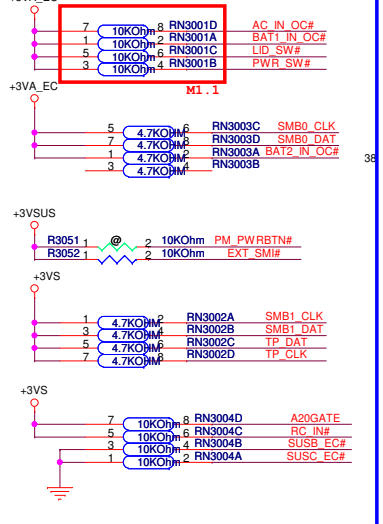
		Title : N/A	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	29 of 96



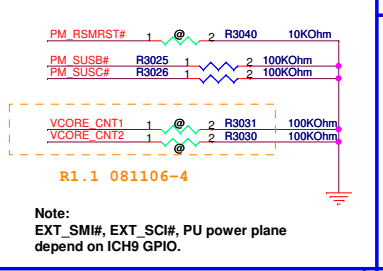
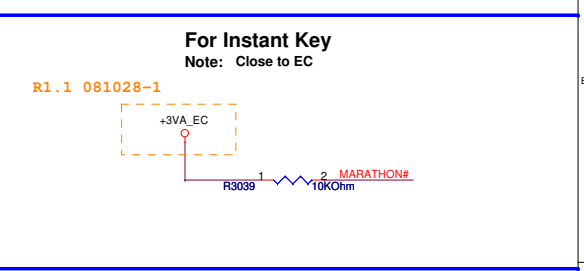
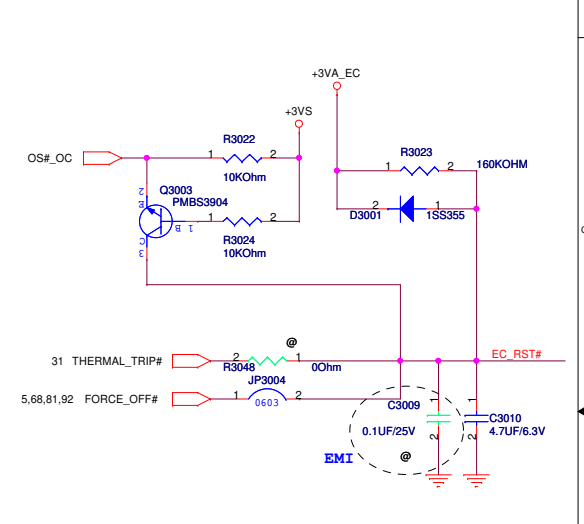
For IT8702 Power



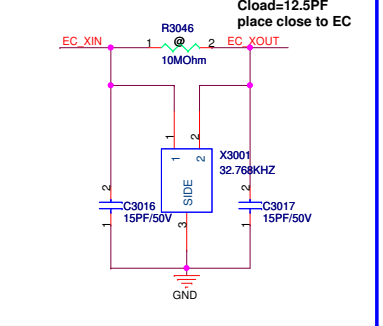
For PU / PD



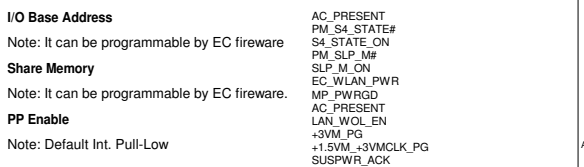
For EC Reset



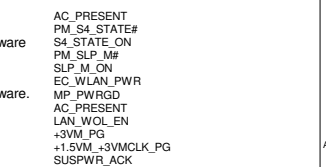
For X'tal



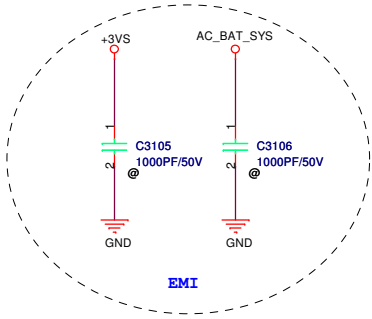
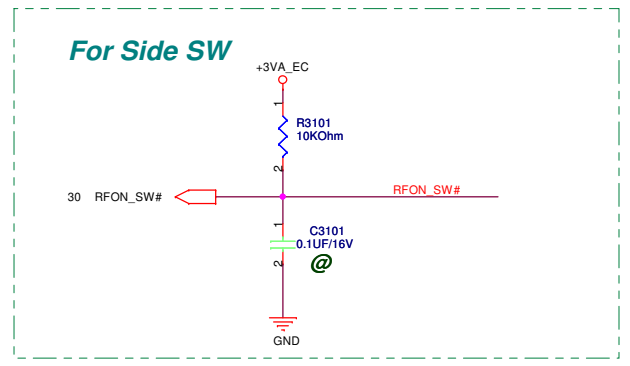
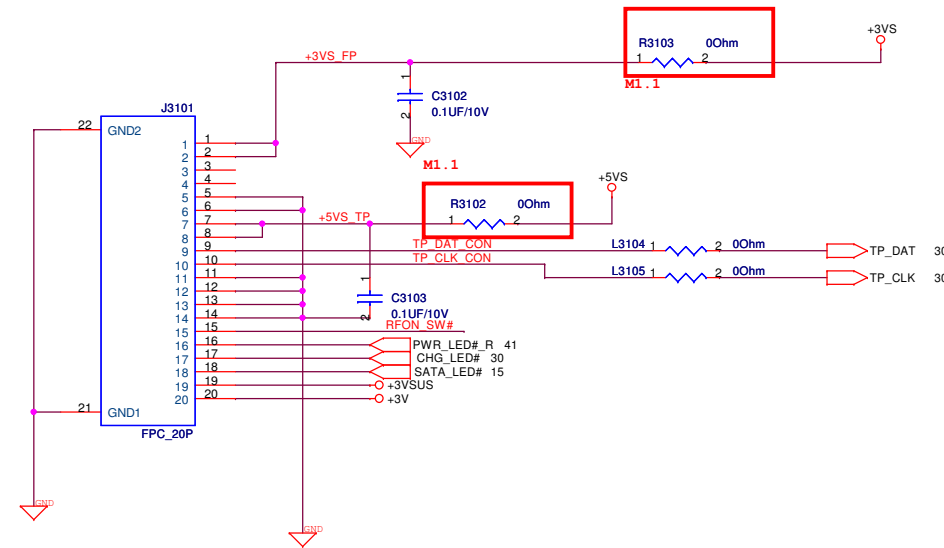
For EC Hardware Strap



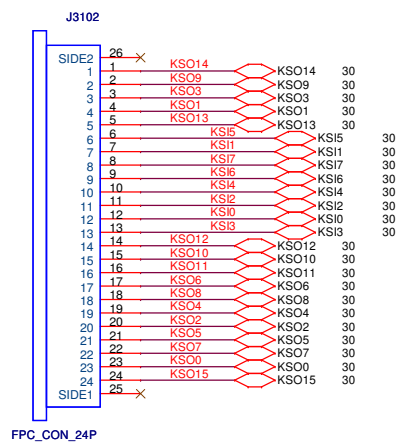
For iAMT pin name



TouchPad & FingerPrint

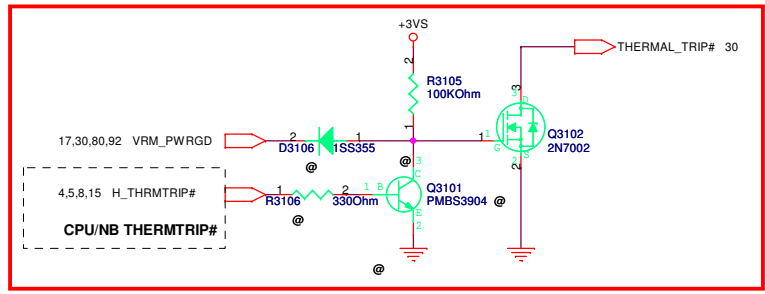


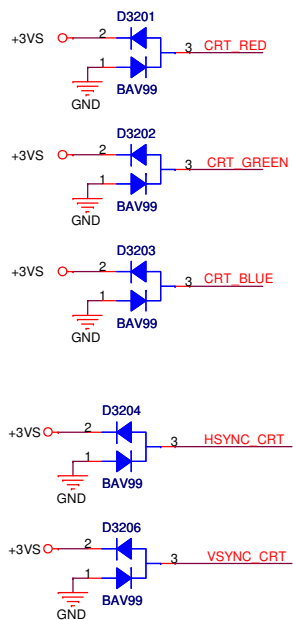
Keyboard Connector



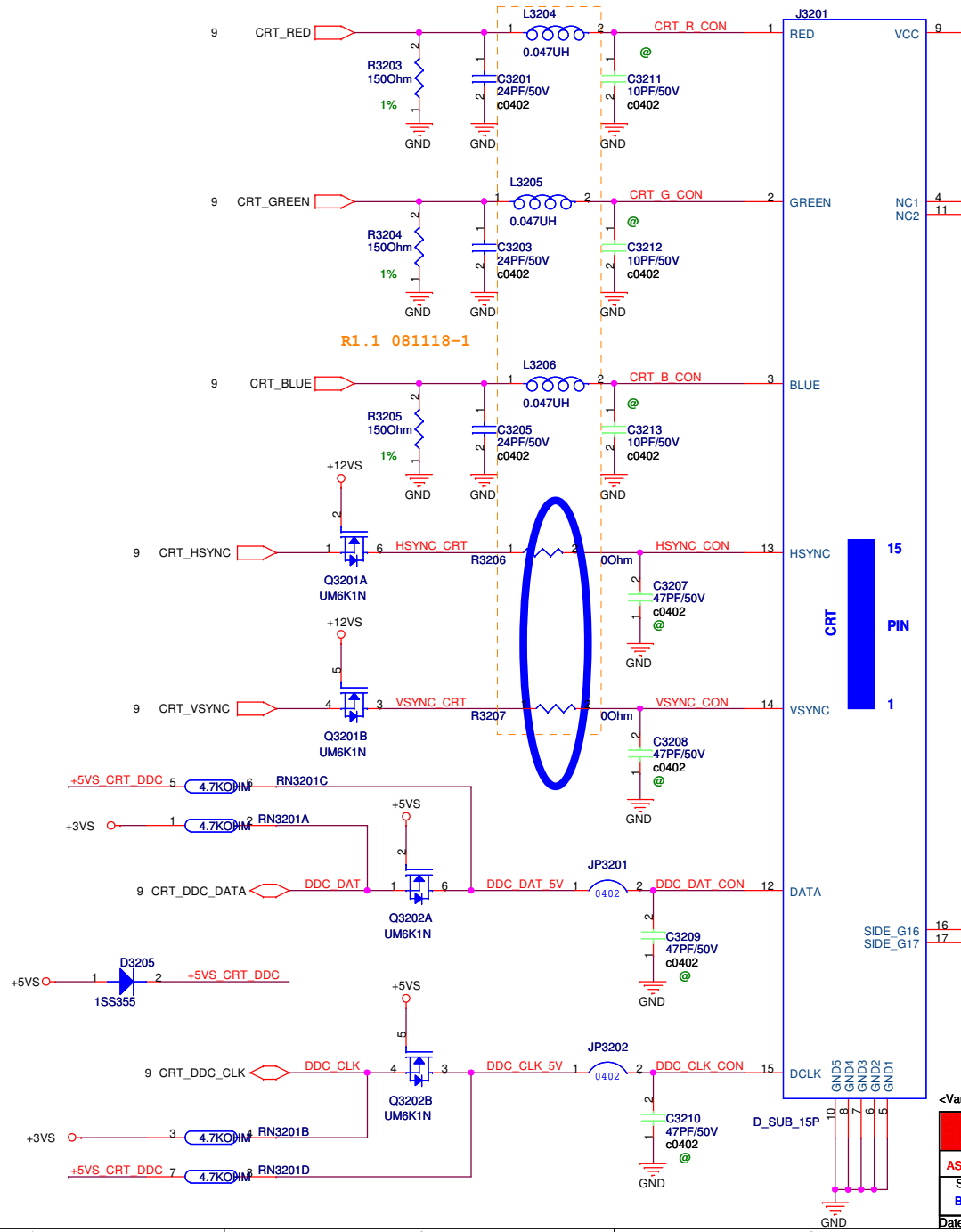
For Thermal Control Method

Remove redundant components





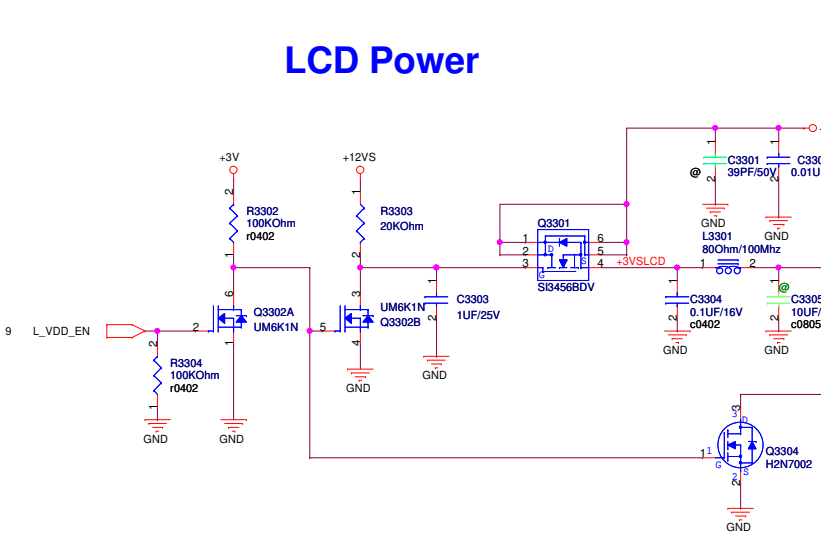
PLACE ESD Diodes near VGA port



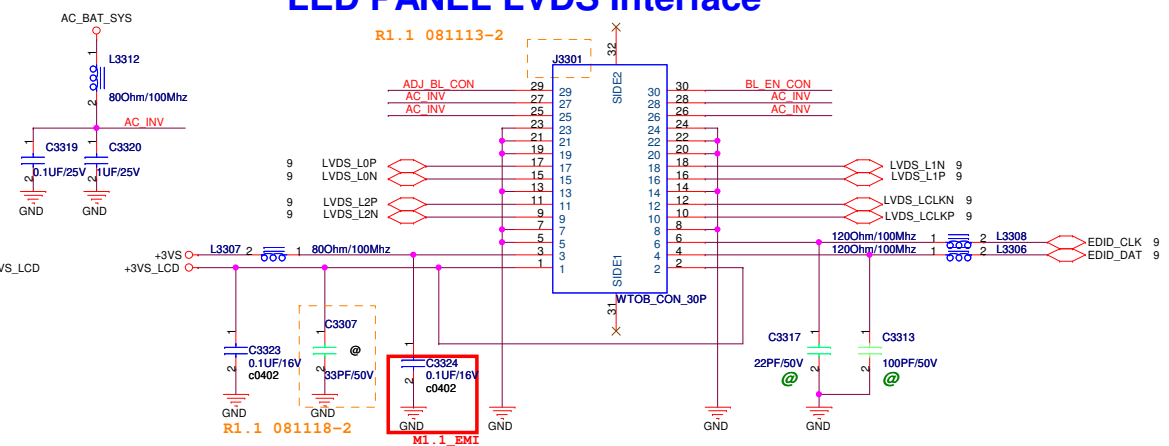
<Variant Name>

		Title : CRT
ASUSTeK COMPUTER INC		Engineer: N/A
Size B	Project Name K401J/K501J	Rev 1.1
Date: Monday, March 09, 2009	Sheet 32	of 96

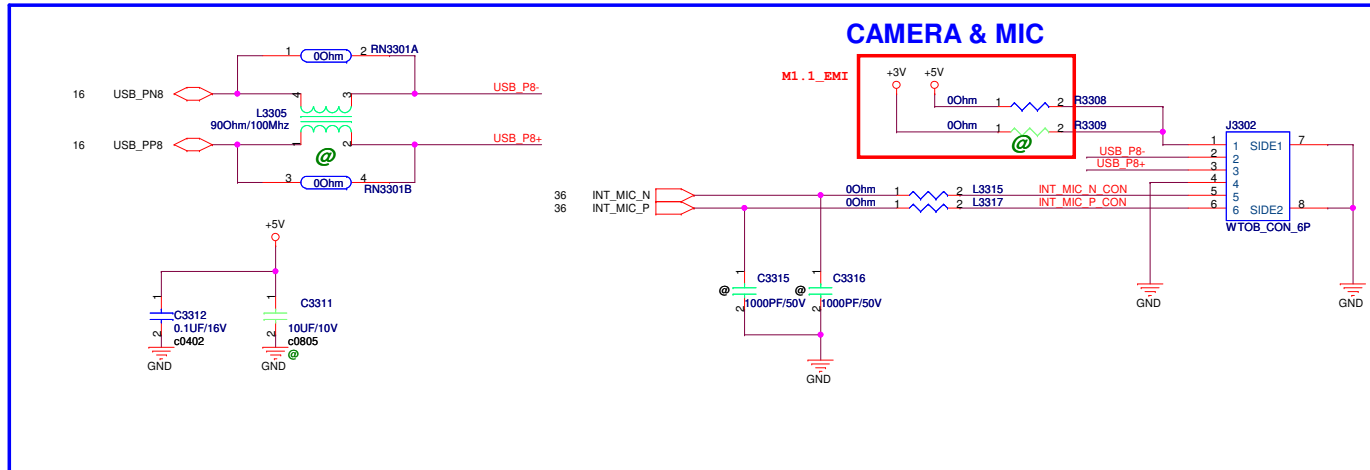
LCD Power



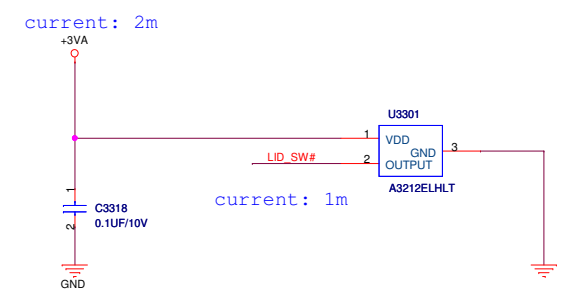
LED PANEL LVDS Interface



CAMERA & MIC



Hall effect switch



R1.1 081029-1

R1.1 081113-2

R1.1 081118-2

M1.1_EMI

<Variant Name>

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40LJ/K50LJ		1.1
Date: Monday, March 09, 2009	Sheet	33	of 96

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For Bluetooth

<Variant Name>

		Title : BT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	34 of 96

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ASUS [®]		Title : N/A	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	35 of 96

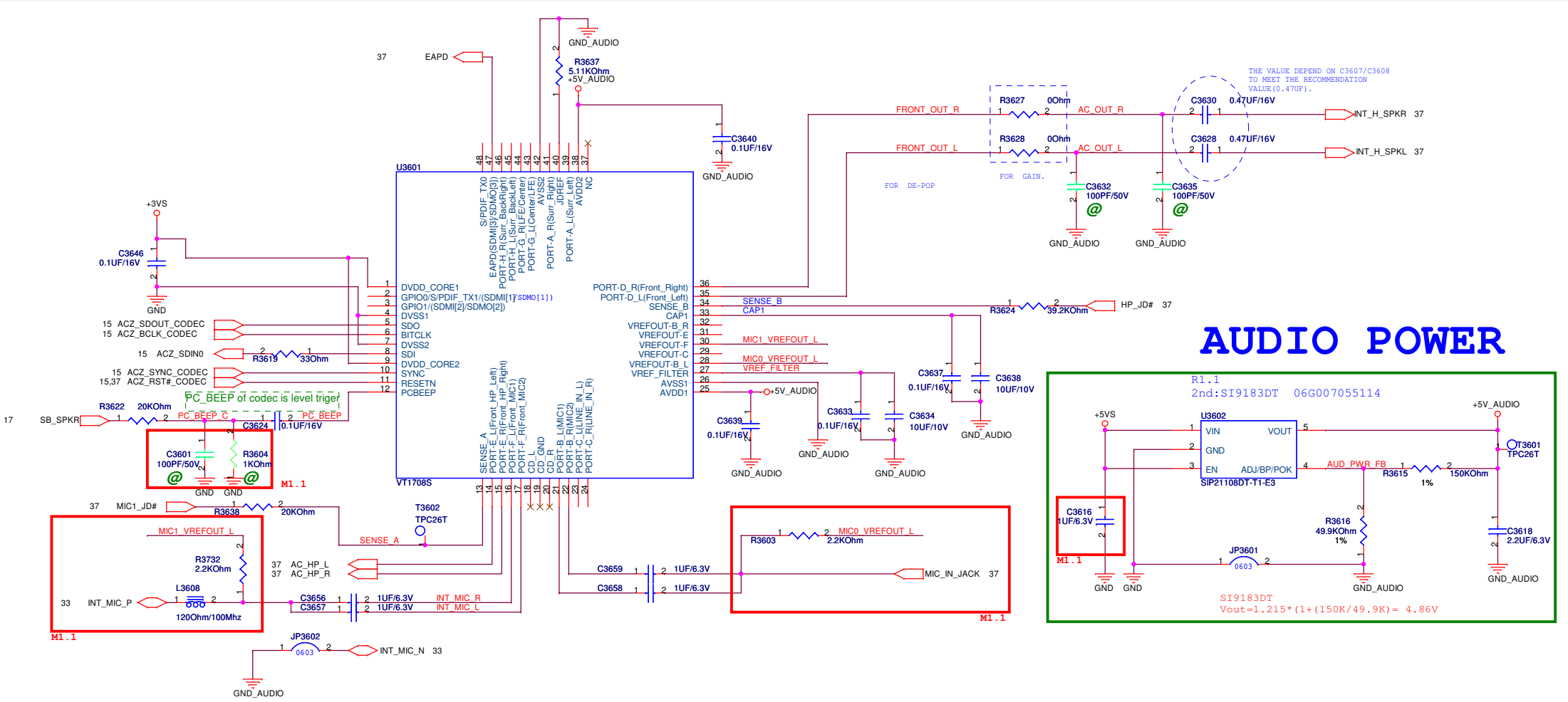
5

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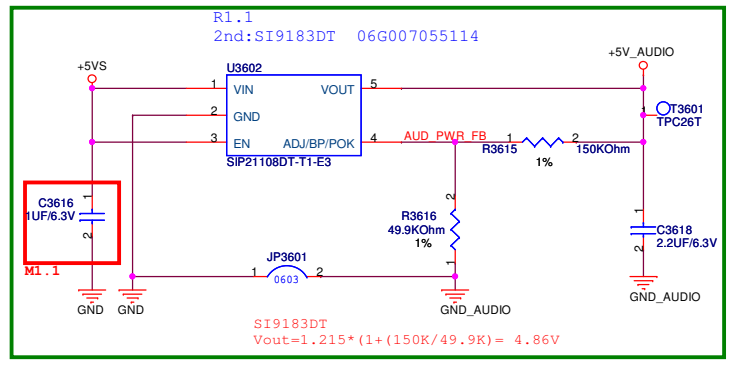
3

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AUDIO POWER



<Variant Name>

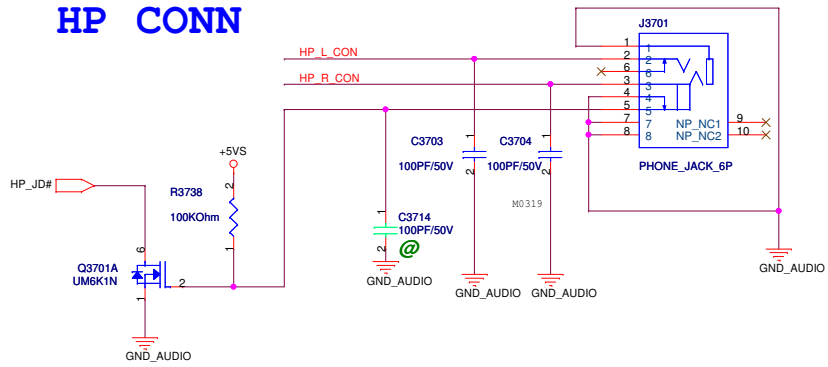
ASUS Title : CONEXANT CX20582

ASUSTeK COMPUTER INC Engineer: N/A

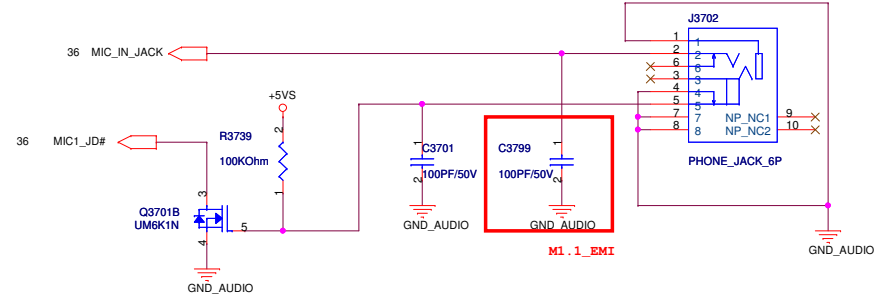
Size	Project Name	Rev
Custom	K40LJ/K50LJ	1.1

Date: Monday, March 09, 2009 Sheet 36 of 96

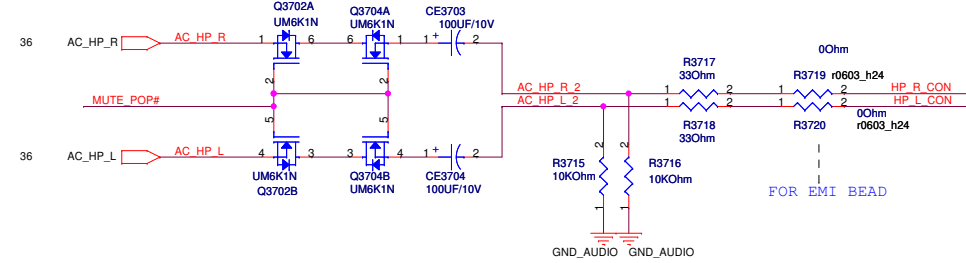
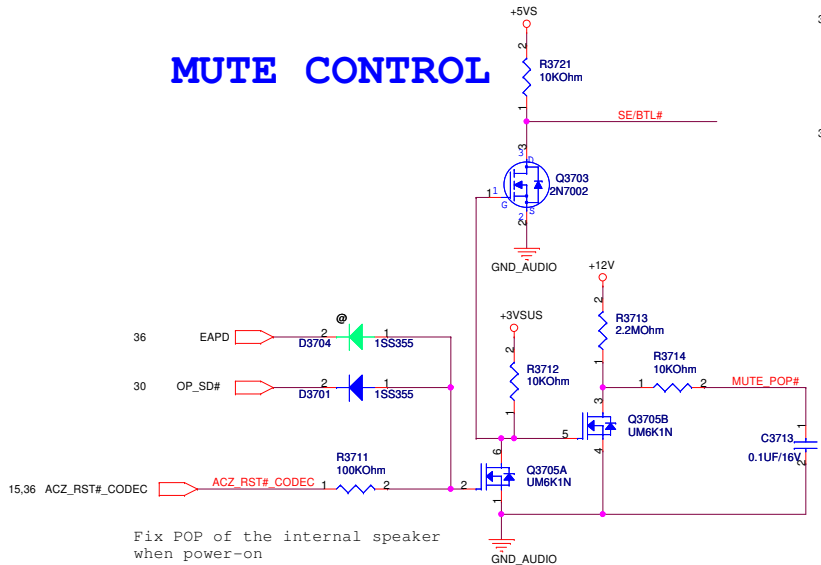
HP CONN



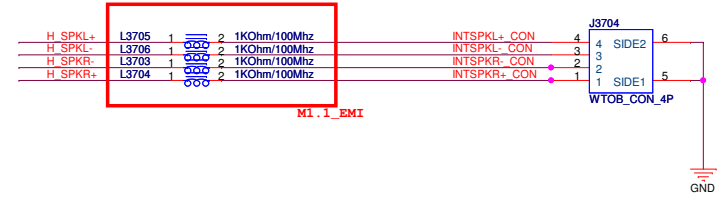
External MIC CONN



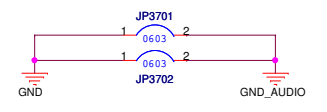
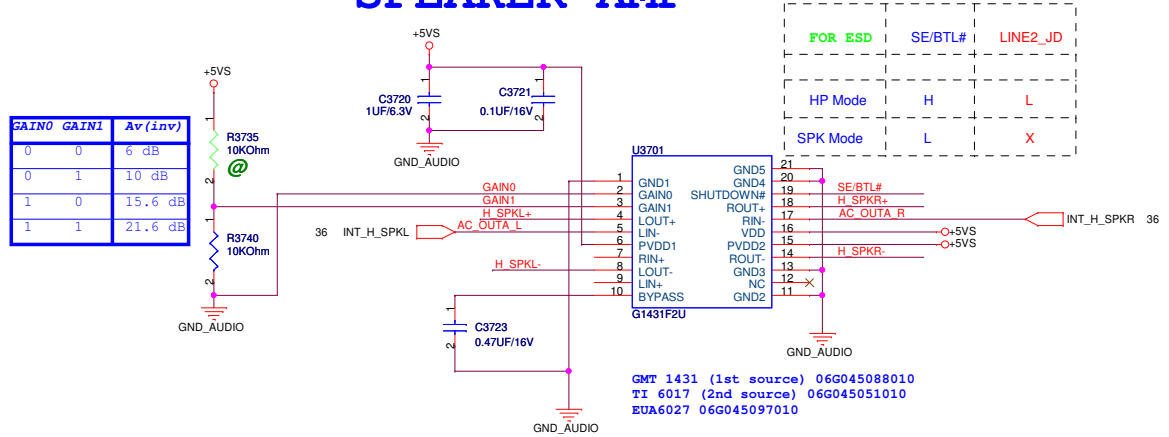
MUTE CONTROL



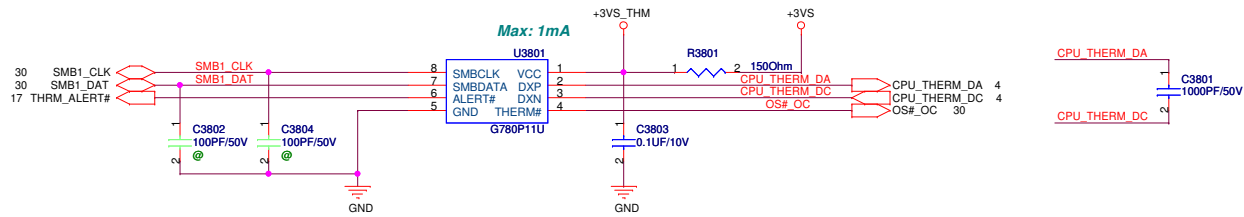
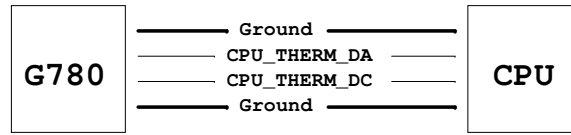
SPEAKER CONNECTOR (2W)



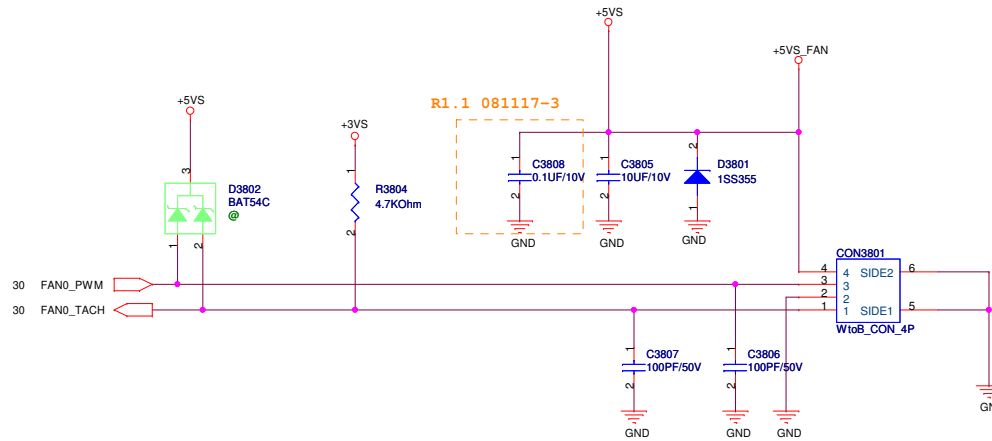
SPEAKER AMP



Thermal Sensor

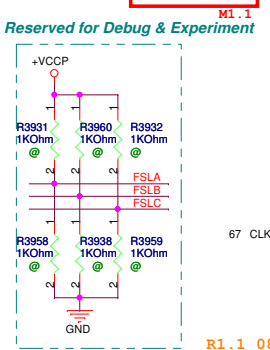
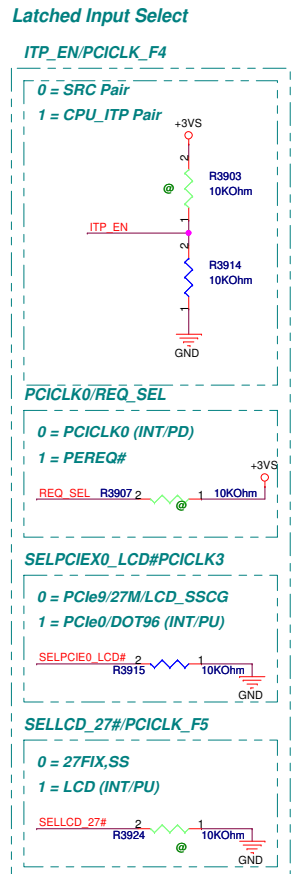
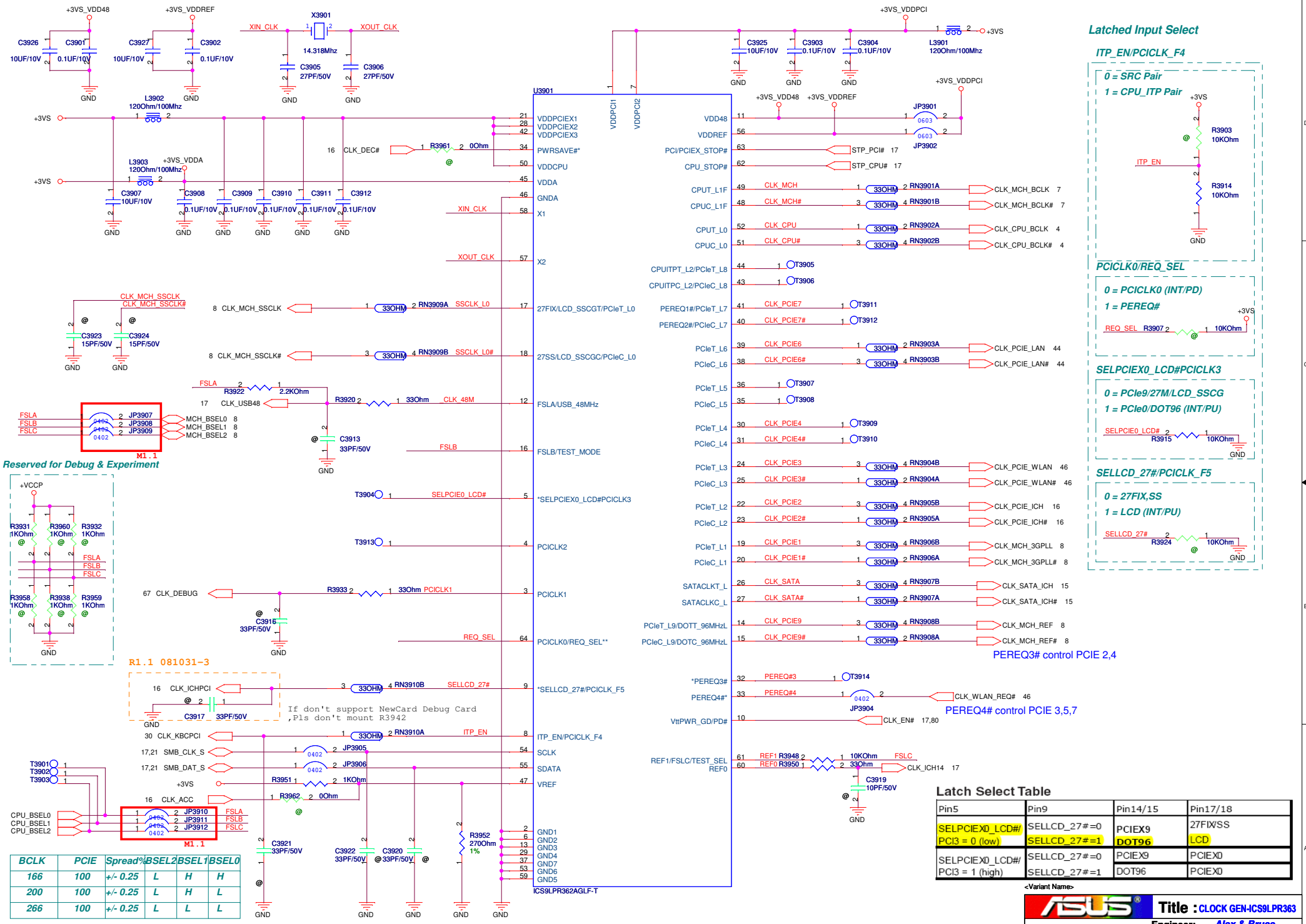


add 2nd source :06G023096010



<Variant Name>

ASUS		Title : THER SENSOR & FAN	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
Date: Monday, March 09, 2009		Sheet	38 of 96



BCLK	PCIE	Spread%	BSEL2	BSEL1	BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L
266	100	+/- 0.25	L	L	L

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=#0 SELLCD_27#=#1	PCIE9 DOT96	27FIX/SS LCD
SELPCIE0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=#0 SELLCD_27#=#1	PCIE9 DOT96	PCIEX0 PCIEX0

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	40 of 96

5

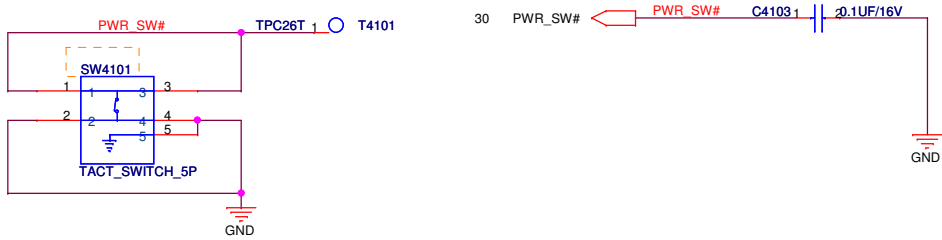
4

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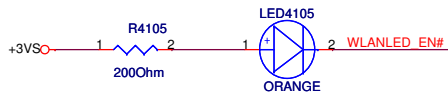
1

SWITCH BUTTON

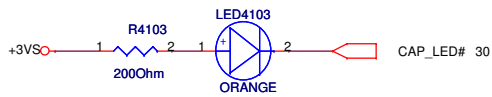


LED

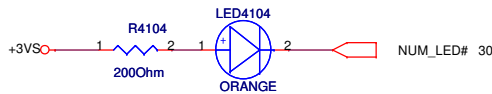
For WireLess LED



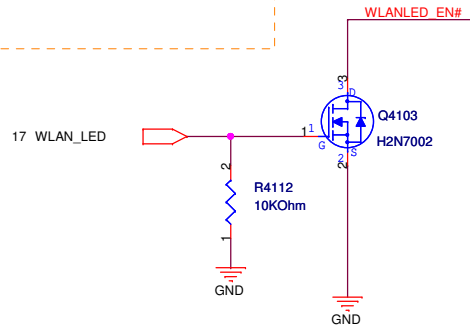
for Cap. Lock



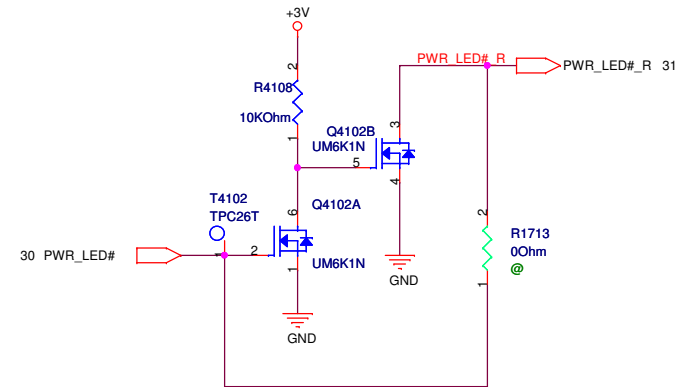
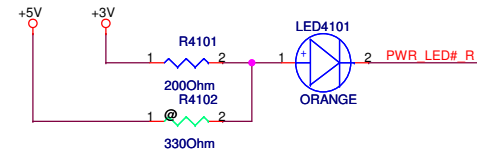
for Num Lock



R1.1 081031-4

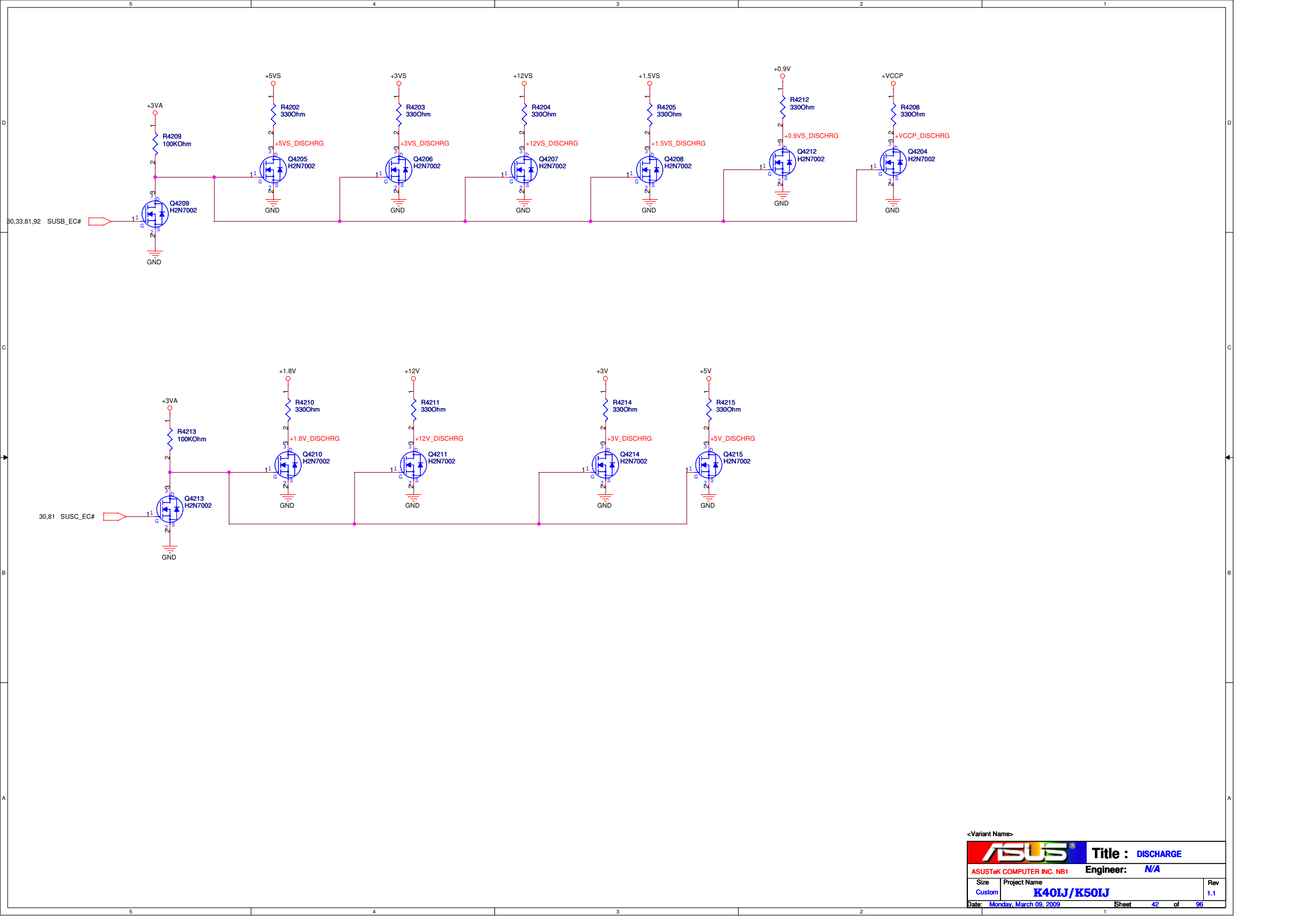


For POWER LED



<Variant Name>

ASUS		Title :Switch Button & LED	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
B	K401J/K501J		1.1
Date: Monday, March 09, 2009		Sheet	41 of 96



<Variant Name>

ASUS		Title : DISCHARGE
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40J/K50J	1.1
Date: Monday, March 09, 2009	Sheet	42 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	43 of 96

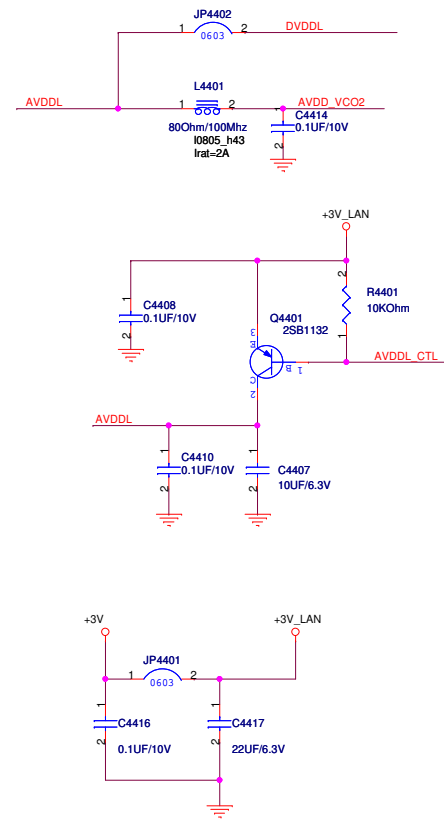
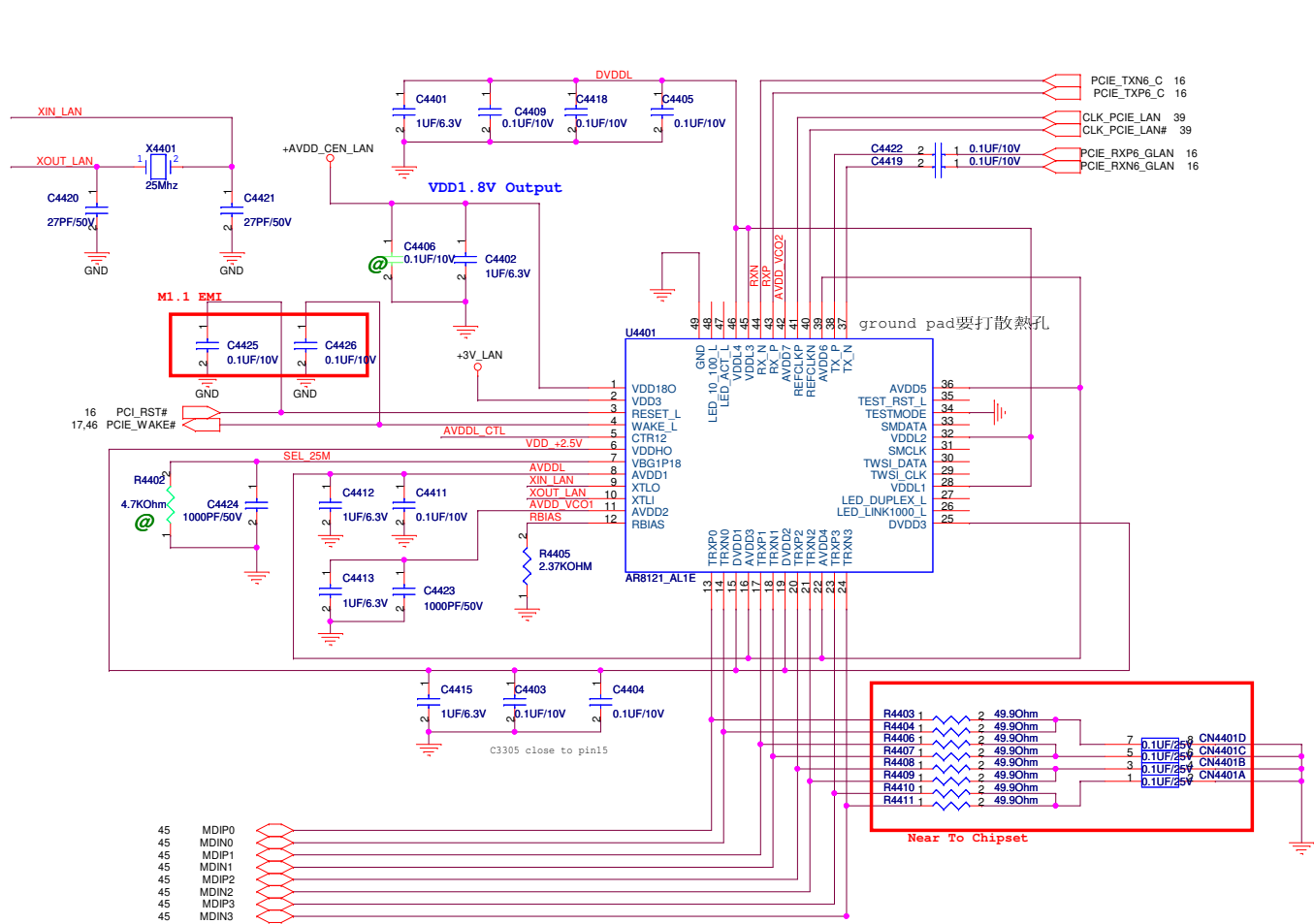
5

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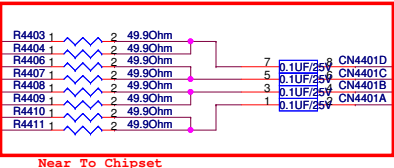
3

2

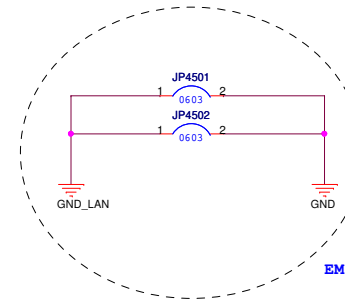
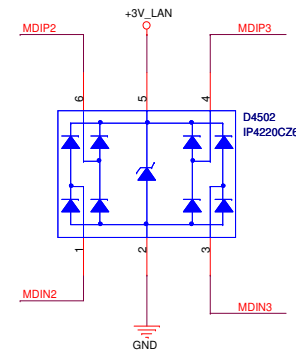
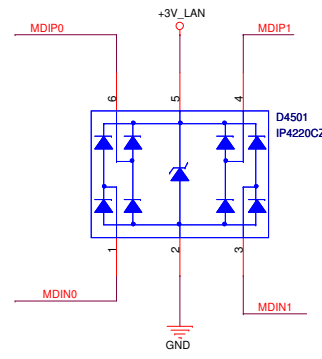
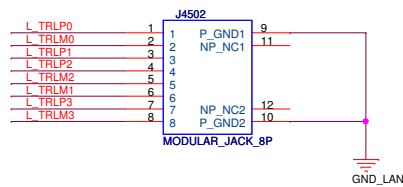
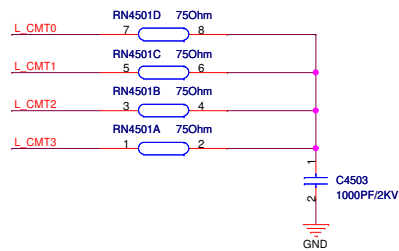
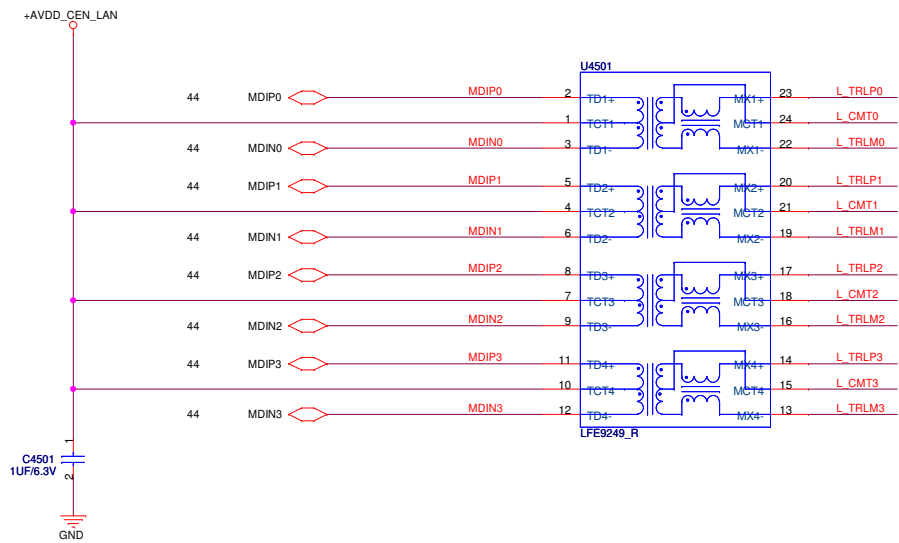
1



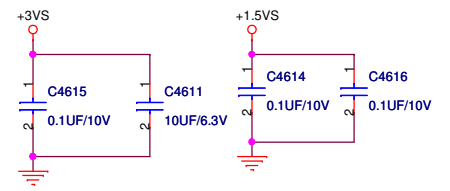
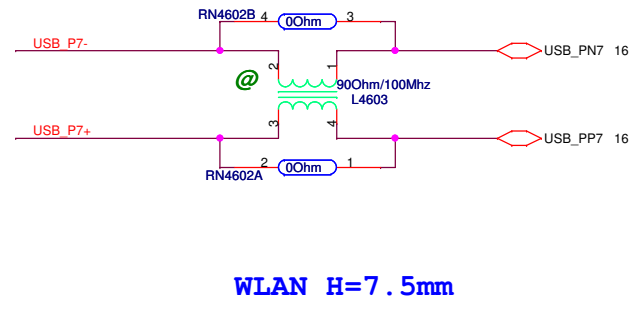
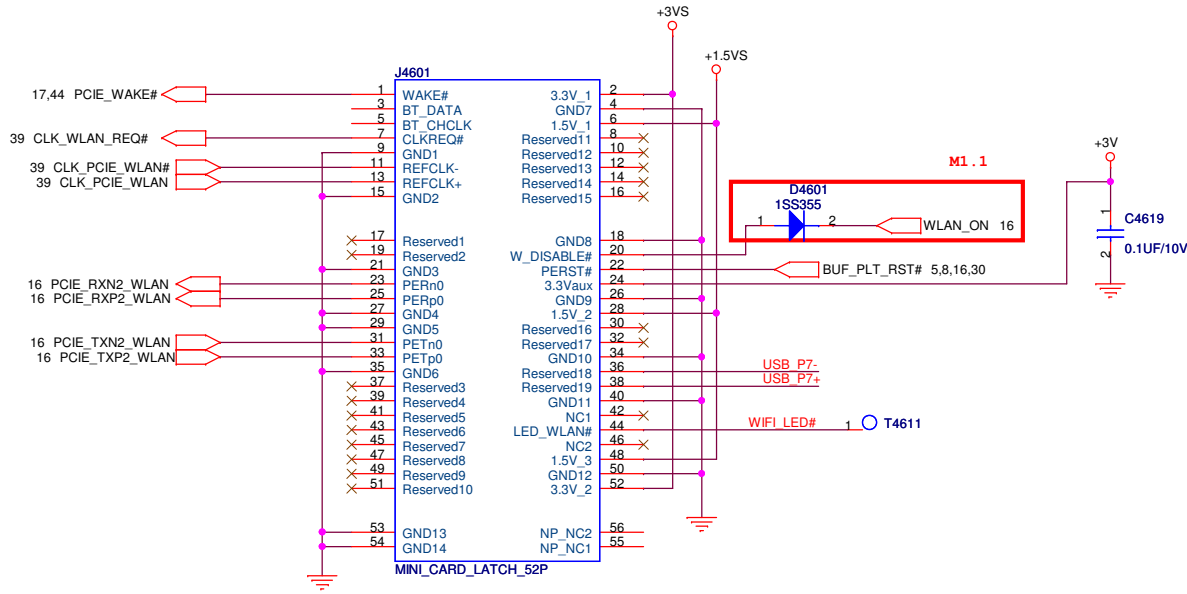
- 45 MDIP0
- 45 MDIN0
- 45 MDIP1
- 45 MDIN1
- 45 MDIP2
- 45 MDIN2
- 45 MDIP3
- 45 MDIN3



LAN CONN.



<Variant Name>



WLAN H=7.5mm

<Variant Name>

ASUS		Title :Mini card_WLAN+3G	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	46 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	47 of 96

5

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<Variant Name>

		Title :Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	48 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	49 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	50 of 96

5

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<Variant Name>



Title : *N/A*

ASUSTeK COMPUTER INC. NB1 Engineer: *N/A*

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: *Monday, March 09, 2009* Sheet 51 of 96

5

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	52 of 96

5

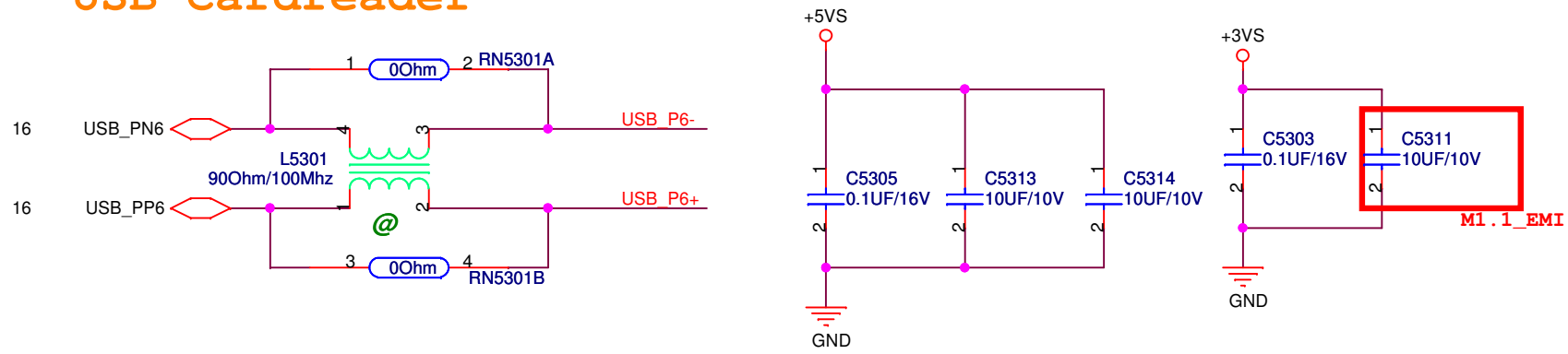
4

3

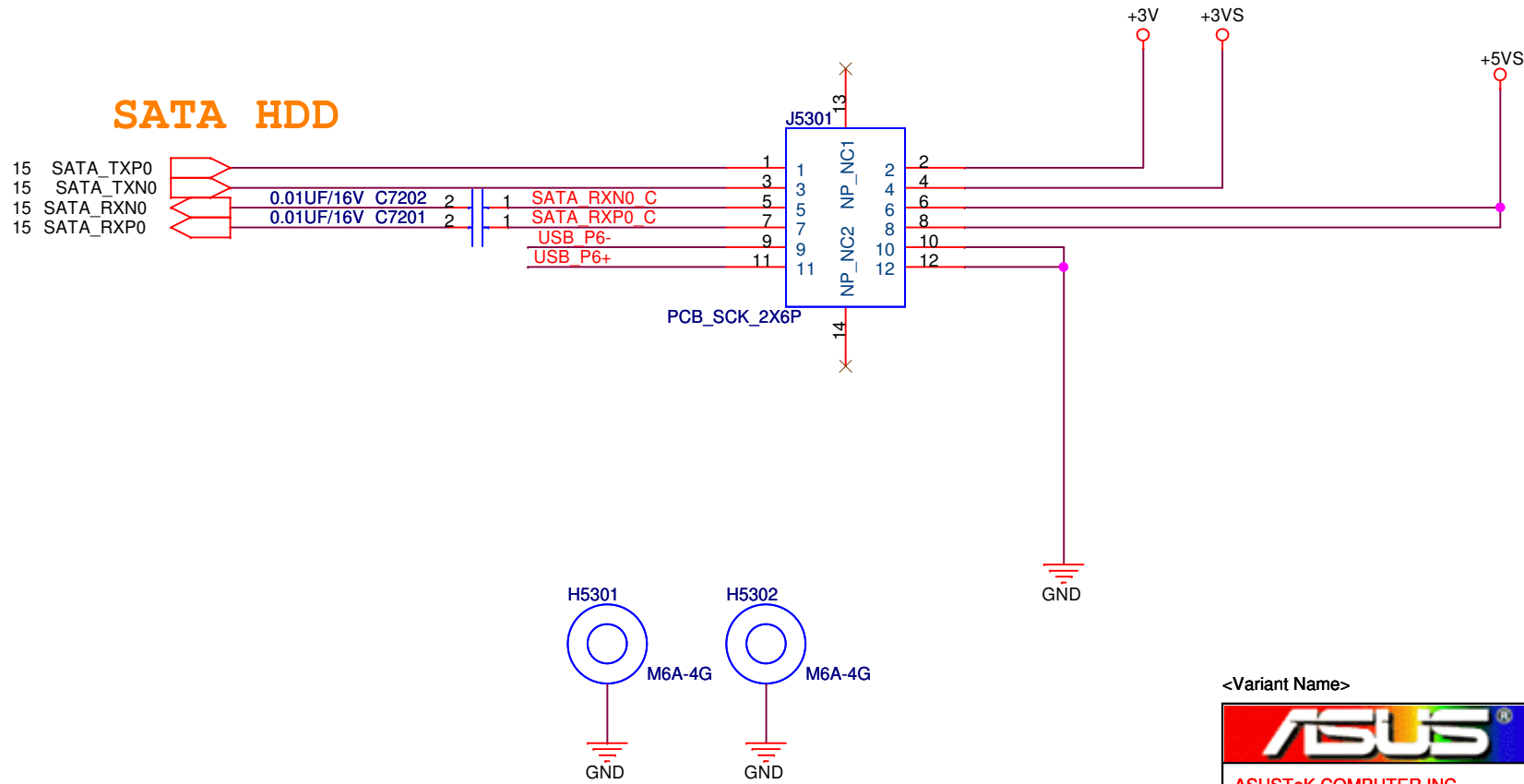
2

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USB Cardreader



SATA HDD



<Variant Name>

ASUS		Title :SATA_HDD & Cardreader	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size Custom	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 53 of 96	

5

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<Variant Name>

		Title : NEWCARD
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
B	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009		Sheet 54 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	55 of 96

5

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<Variant Name>

		Title : HDA level shifter	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>N/A</i>	
Size Custom	Project Name K40LJ/K50LJ		Rev 1.1
Date: <i>Monday, March 09, 2009</i>		Sheet <i>56</i> of <i>96</i>	

5

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HDMI WtoB Connector

HDCP ROM

<Variant Name>

		Title : iHDMI
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size B	Project Name	Rev 1.1
Date: Monday, March 09, 2009		Sheet 57 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	58 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	59 of 96

5

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<Variant Name>



Title : Schematic page name

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 60 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	61 of 96

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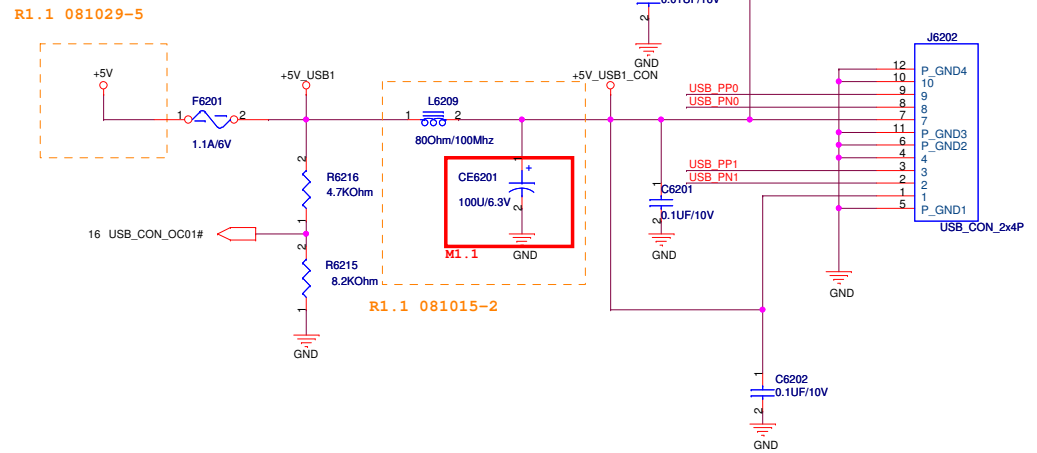
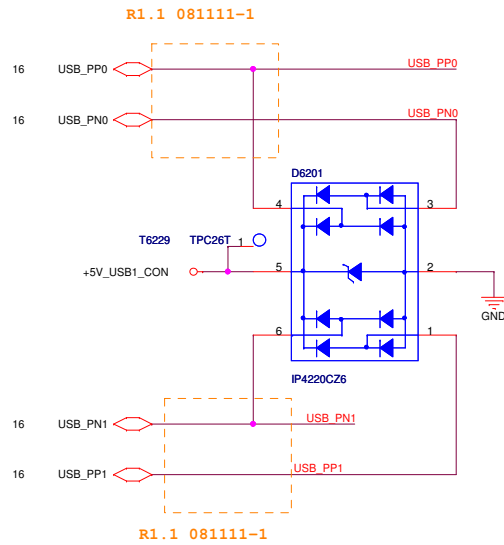
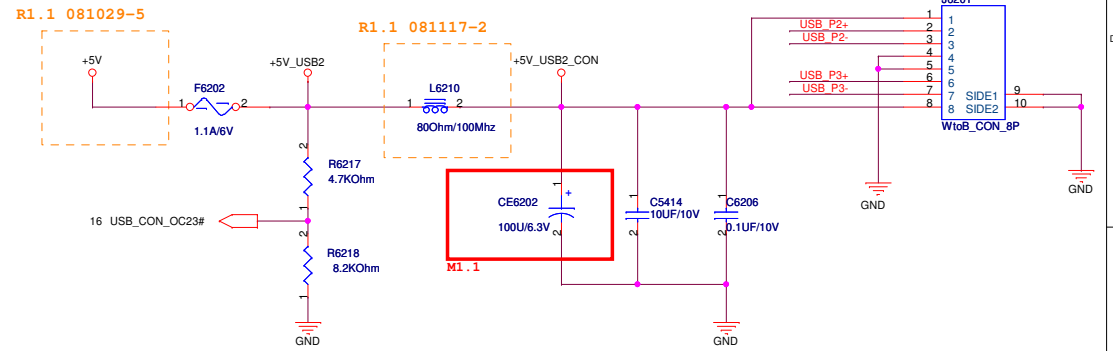
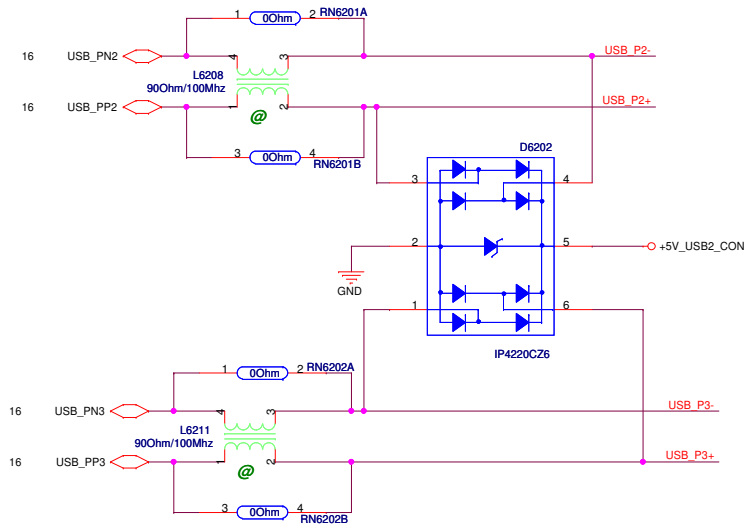
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USB IO Board



<Variant Name>

ASUS		Title : USB CONN	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
Date: Monday, March 09, 2009	Sheet	62	of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	63 of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009	Sheet 64	of 96	

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<Variant Name>

		Title : SPI ROM	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	65 of 96

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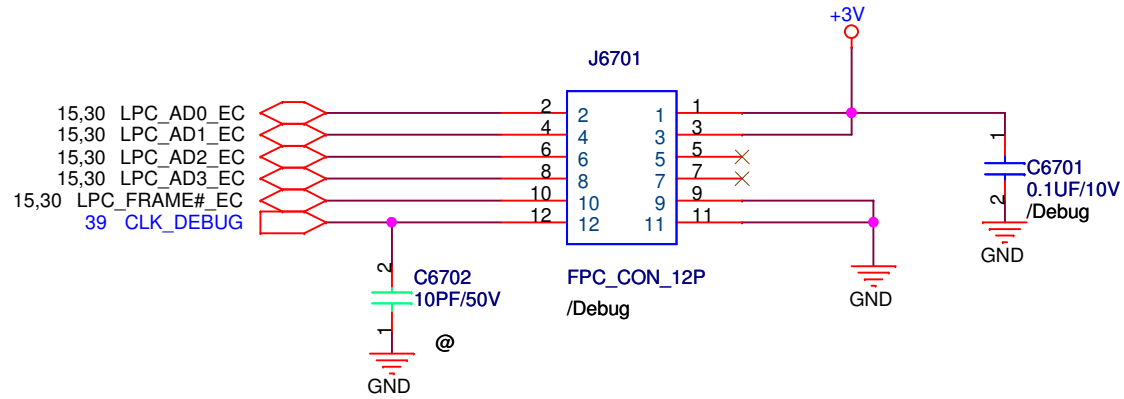
A

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<Variant Name>

		Title : LED	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	66 of 96

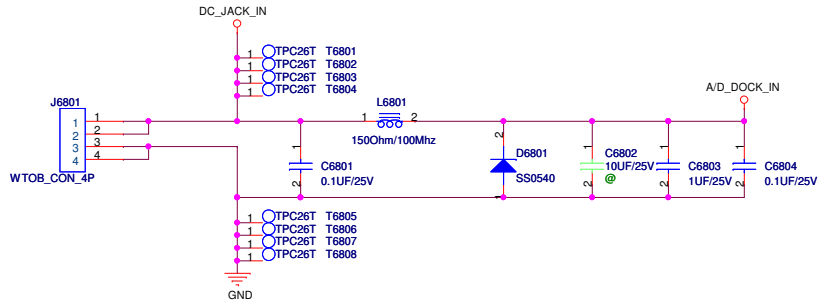
LPC DEBUG PORT



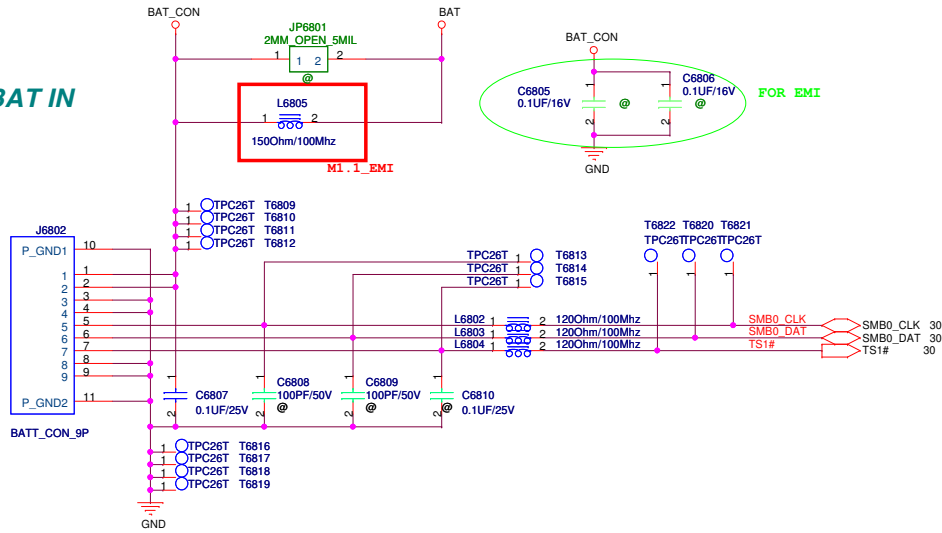
<Variant Name>

ASUS		Title : DEBUG CONN
ASUSTeK COMPUTER INC		Engineer: N/A
Size A	Project Name K40IJ/K50IJ	Rev 1.1
Date: Monday, March 09, 2009		Sheet 67 of 96

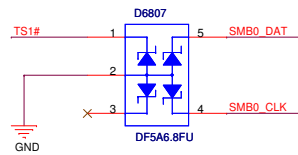
DC IN



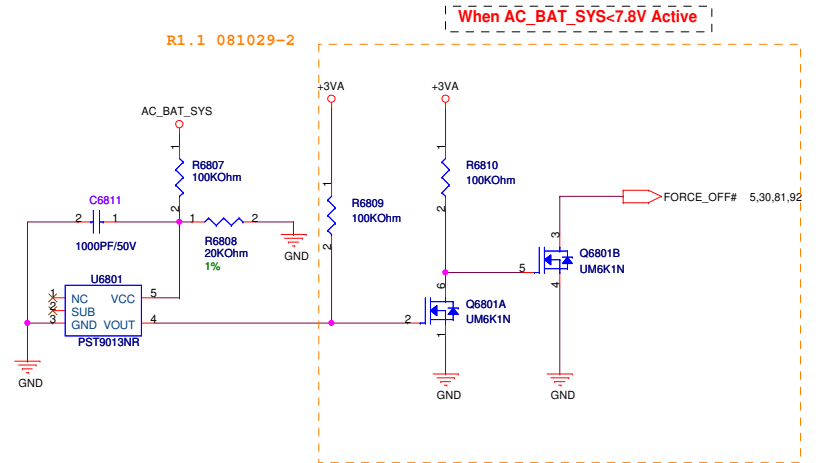
BAT IN



Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.



Without Battery & Pull out Adapter



<Variant Name>

ASUS		Title : DC & BAT IN	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40J/K50J	1.1	
Date: Monday, March 09, 2009	Sheet	68	of 96

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	69 of 96

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<Variant Name>



Title : Debug CONN.

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009 Sheet 70 of 96

5

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date:	Monday, March 09, 2009	Sheet	71 of 96

5

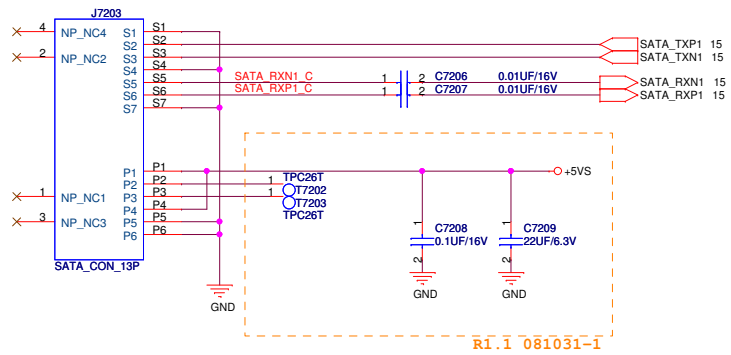
4

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ODD



<Variant Name>

		Title : SATA-ODD
ASUSTeK COMPUTER INC. NB1		Engineer: N/A
Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009	Sheet	72 of 96

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	73 of 96

5

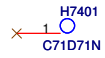
4

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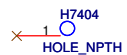
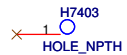
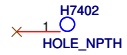
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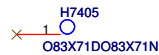
Hole-A



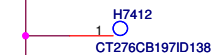
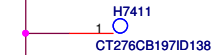
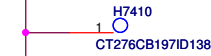
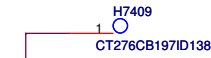
Hole-B



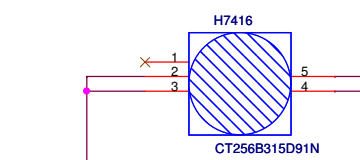
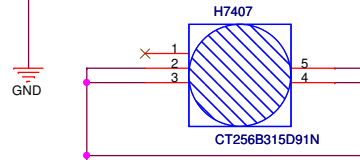
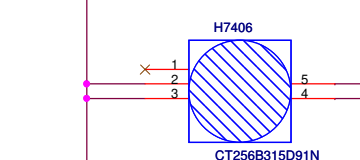
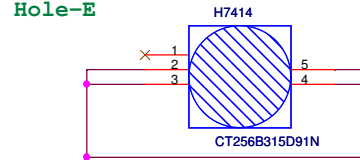
Hole-C



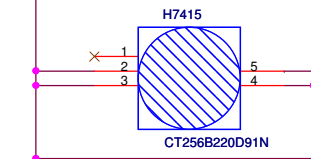
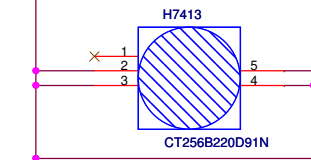
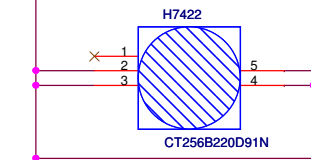
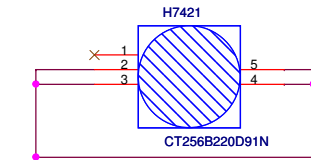
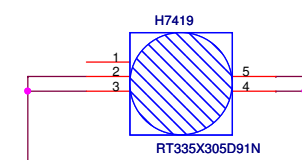
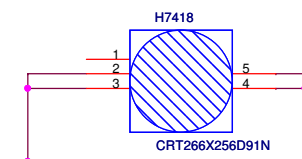
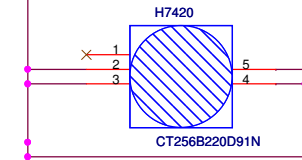
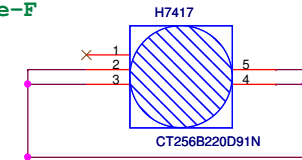
Hole-D



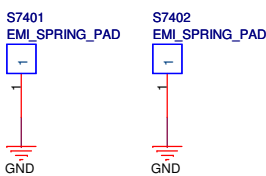
Hole-E



Hole-F



Spring



<Variant Name>		
		Title : Hole
ASUSTeK COMPUTER INC		Engineer: Leon Guo
Size	Project Name	Rev
B	K40IJ/K50IJ	1.1
Date: Monday, March 09, 2009	Sheet 74 of 96	

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	75 of 96

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<Variant Name>

	Title :EXPRESS GATE
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ASUSTeK COMPUTER INC	Engineer: N/A
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Size Custom	Project Name K40IJ/K50IJ	Rev 1.1
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R1.1 Modify List

P04_Q0402,R0401 No mount
P36_INT_MIC Change
P37_J2704 speaker_H_SPK1+/H_SPK1-/H_SPKR+/H_SPKR- Signal modify,Del R3732
P05_C80502,C0528,31,32,33,36,43 NO-Stuff
P07_C0702 NO-Stuff
P08_R0813 NO-Stuff,R0815/R0816 10K OHM change to 0 OHM(E/R Check if ok change to J8112 to J8113
R0817 100 OHM Change to Short JP
P12_C1223,C1245 100F/10V(1206) change to 100F/6.3V(0805) for reduce
P24_Add On-board memory to 2G
P30_change "BATSEL_28#" to "BATSEL_0"
change "BATSEL_38#" to "BATSEL_1"
Merge R3020,21,27,29 to array resistor
P36_C3616 Y5V change to X7R for reduce component count
P37_C3720 Y5V change to X7R for reduce component count
P39_Delete RN3901,RN3902
P44_Change LAN Chip from RTL8111DL to AN8121
P09_R0910,11,12 change to RN0901 array package
R3002,03,05,28 change package
P18_Add C1843,C3324,C2203,C4425,C4426 for EMI
Del R3506
Change ReferenceC7213,03,05,11 to C53013,03,05,11
P16_For EMI CMOS form Port 4 change to Port 8
P62_C86202 Change package
P11_C1125,26,30 0.22UF change to 1UF cost down
P3601_Reserve C3601,R3604 for Vendor request
P31_L3102,03 change to R3103,02
Add JP1502 del R1511
Del R0918,R0919 add RN0902
P39_Del R3946 ,add RN3910
P04_C0402,03 add for EMI
P04_C0402 add for EMI

Power List 1/15
change J8112 to J8112
nostuff C8121
change J8110 to J8110
change J8113 to J8113
change J8114 to J8114
change J8115 to J8115
change J8103 to J8103
change J8106 to J8106
change J8109 to J8109
change J8111 to J8111
change J8105 to J8105

page 82
change JP8203 to J8203

page 83
change JP8303 to J8303
change JP8304 to J8304

page 84
add JP8402
Change U8401 to APL5930 from APL5913

Page 88
change JP8805 to J8805

1/14
page 80
change Q8001 and Q8003 to 07G005A15011 from 07G005C34010.
change Q8002 and Q8004 to 07G005B71010 from 07G005C33010.
stuff C8003

page 83
change R8304 to 10G212150214030 from 10G212750114010.

1/08
Change all 2MM_SHORT_SMI1 to 2MM_OPEN_SMI1(s00496)

page 81
change "L7020_DLL1" to "8206_DLL1".

page 88
add L8802 between BAT and BAT_CON
change R8823.2 to GND from SGND_CHG.
change "BATSEL_28#" to "BATSEL_0"
change "BATSEL_38#" to "BATSEL_1"

01/07
Delete Empty Page 85,86,87,89,90

Page 80
Change R8010, R8013, R8020, R8035, R8040, R8046 to temp.4759_ch01 from 10G212000004010
Change C8003, C8017 to Unmount
Delete R8050

Page 81
change R8116, R8119, R8125, R8110, R8107 to temp.4759_ch01 from 10G212000004010
Delete R8102, R8118
Change D8103 to 07G004069020 from 07G001007230

Page 82
Change D8201 to 07G004069020 from 07G001007230

Page 83
Change D8301 to 07G004069020 from 07G001007230

Page 84
Delete R8404
Delete Netname 5913_VCNFL

Page 88
Change D8804 to 07G004069020 from 07G001007230

Page 91
Change R9105, R9108 to 10G252100314030 from 10G212100314030

12/31
page 80
change Q8002, Q8004 to 07G005C35010 from 07G005C33010
change U8001 to 06G008425013 from 06G008692010
change R8026 to 10G212680114010 from 10G212953114010

12/26
page 81
change CE8101, CE8102 to 11G08D21075A from 11G09X222755.

page 82
delete Q8203.
delete C8207.
change CE8202 to 11G08D2227D1 from 11G09X222755.
change U8201.7, U8201.15, R8205.1 to SGND.

page 83
change CE8301 to 11G08D2227D1 from 11G09X222755.
change JP8301 to 2MM.

page 88
change U8801.6 net name to CHG_INE3 from CHG_COMP3.
change C8806, C8809 to 11G233110412030 from 11G23210412360.
change Q8802, Q8803 PCB Footprint to soic_8p_50_197x236.

page 91
change R9107 to 10G212220214030 from 10G213220213010.
page80
add net name "SNB_PH1" between R8020 and C8040
add net name "SNB_PH2" between R8021 and C8041
change C8040 to 11G232115214320 from 11G233115214320.
change C8041 to 11G232115214320 from 11G233115214320.

page 84
change JP8402.1 connection to +1.8V from +1.8V0
add net name "5930_VIN" on U8401.5 and U8401.9
change net name "5913_FB" to "5930_FB" on U8401.2

page 88
add net name "SNB_CHG" between R8804 and C8803
add net name "CHG_BST" between R8810 and C8802
change C8803 to 11G232115214320 from 11G233115214320.



M1

P05_Del JP0501
P16_Add R1602
P33_Add R3308,R3309

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<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	78 of 98

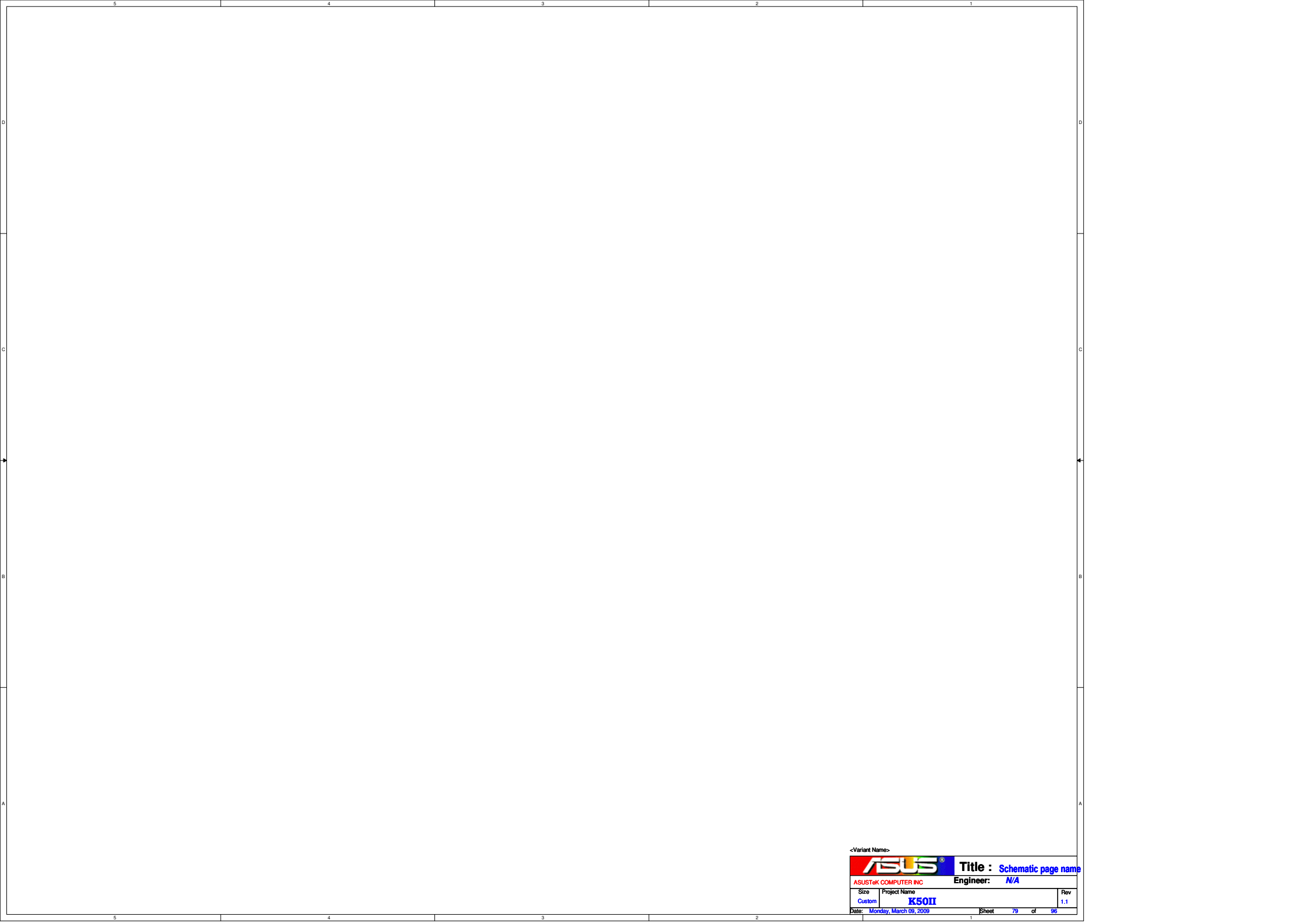
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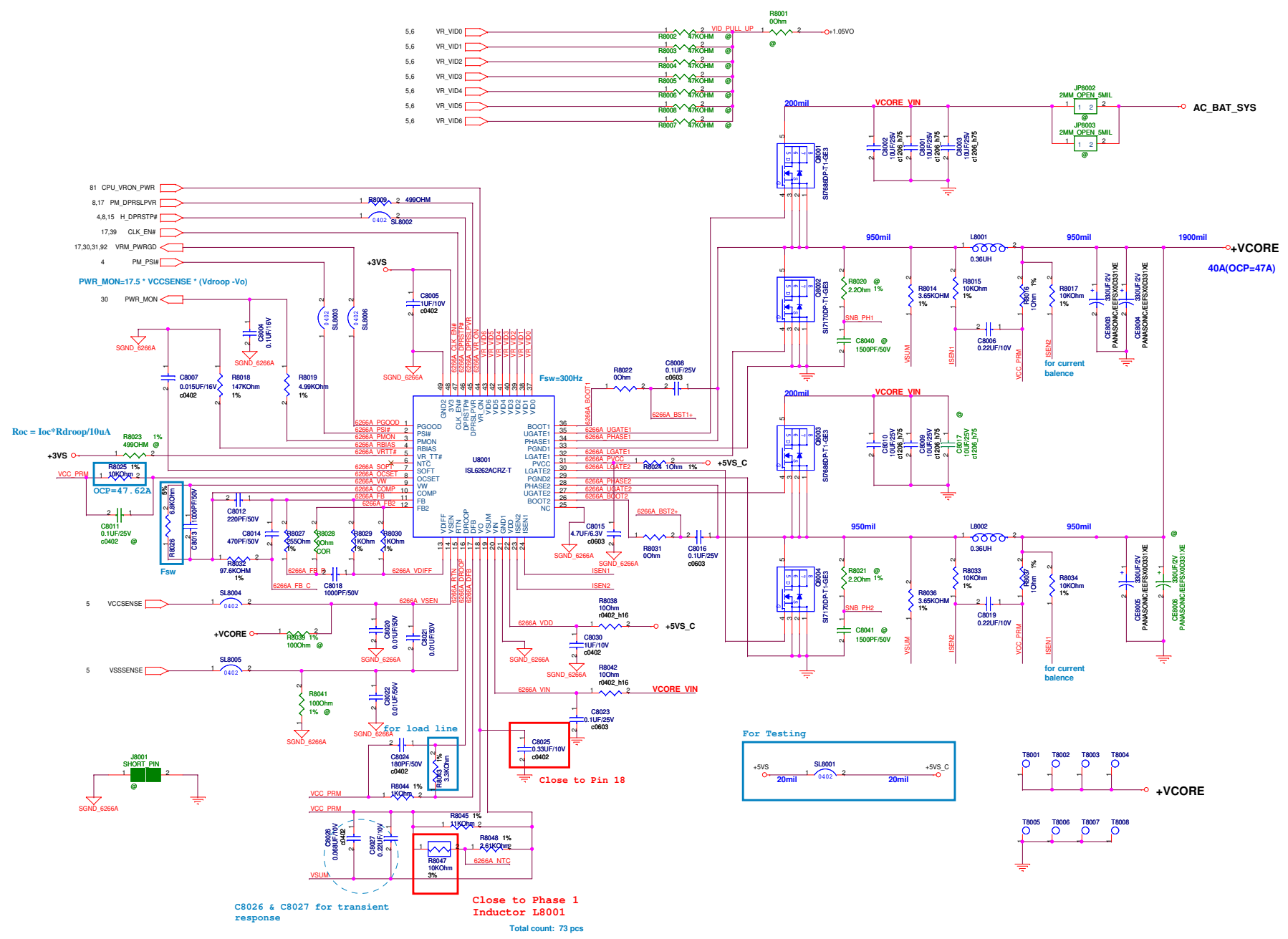
2

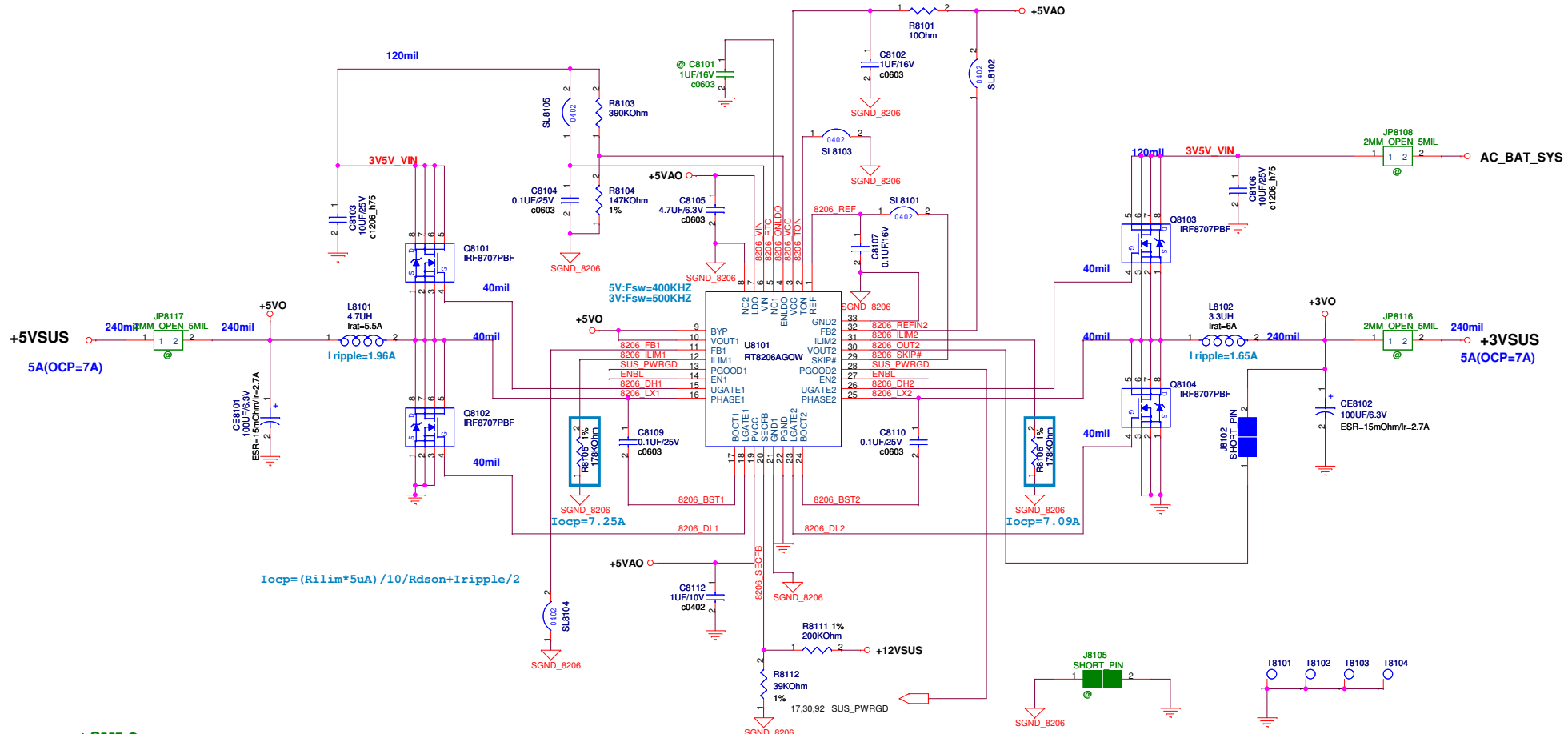
1



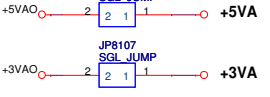
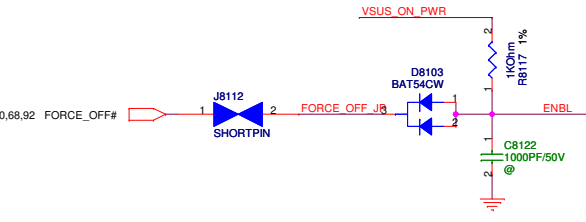
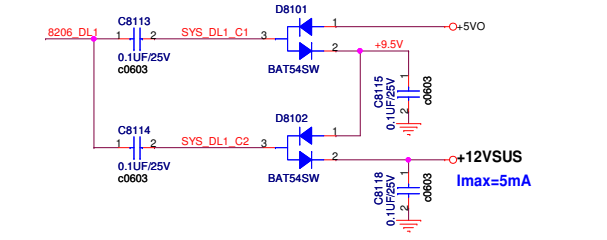
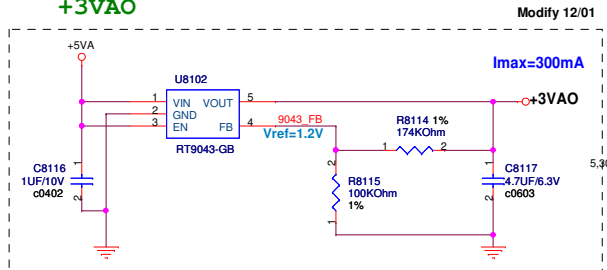
<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K50II	1.1	
Date: Monday, March 09, 2009		Sheet	79 of 96



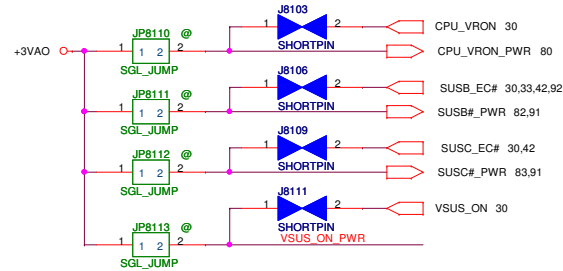


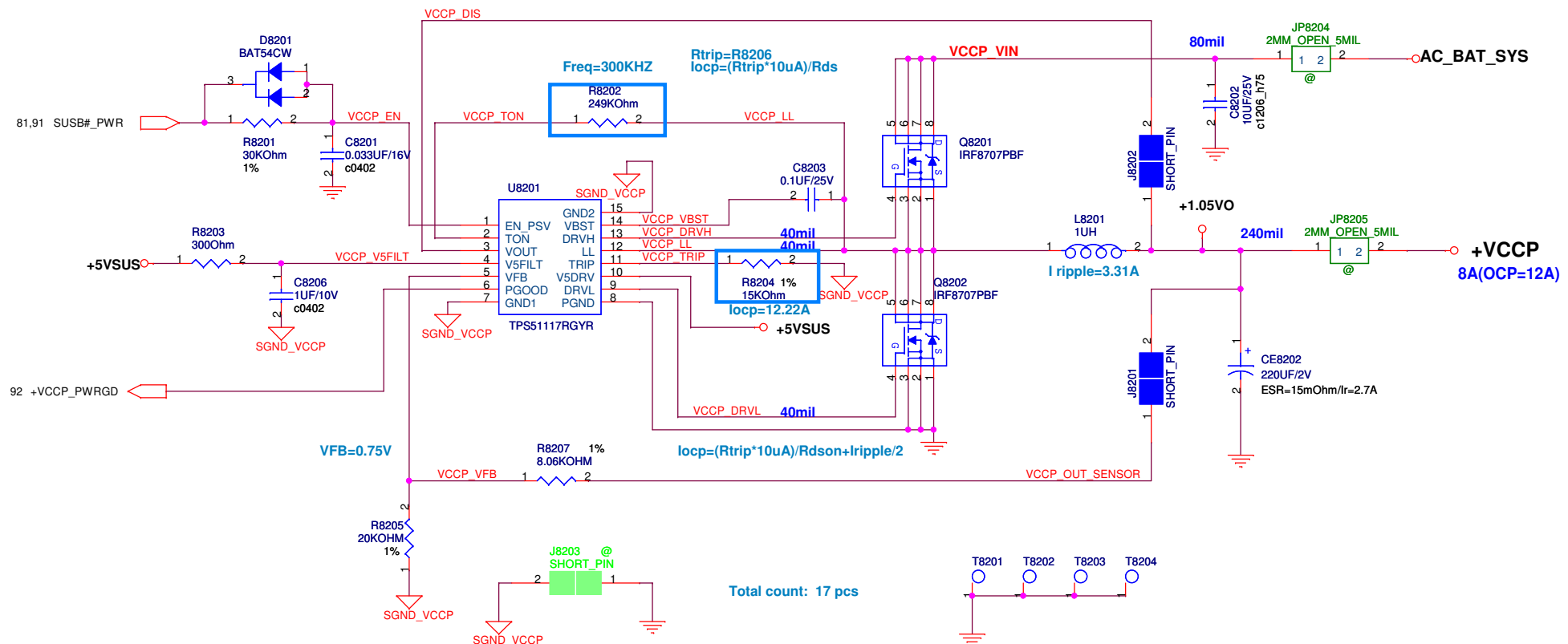
$$I_{ocp} = (R_{lim} * 5uA) / 10 / R_{ds(on)} + I_{ripple} / 2$$

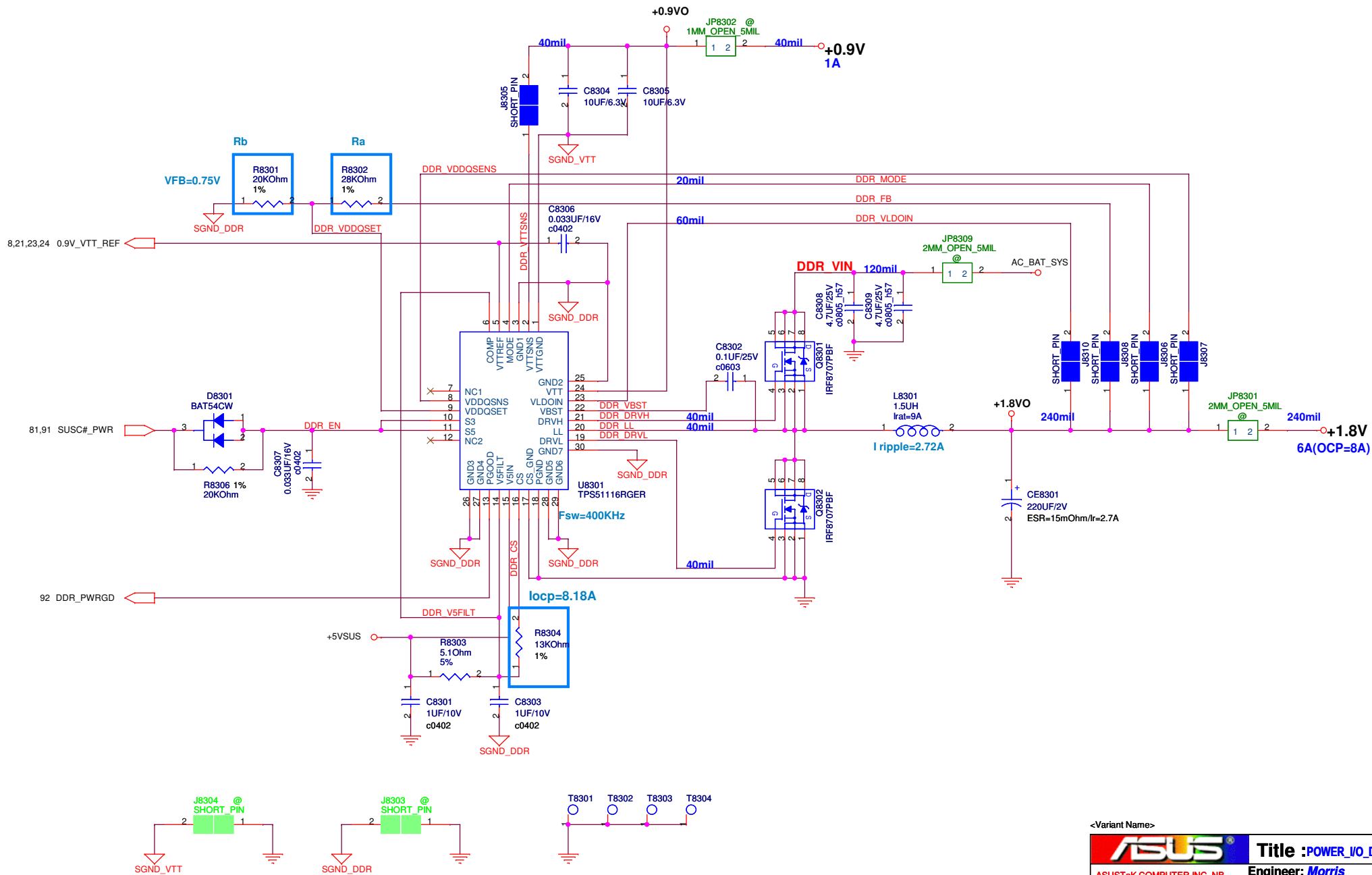


Total count: 44 pcs

FOR POWER TEST

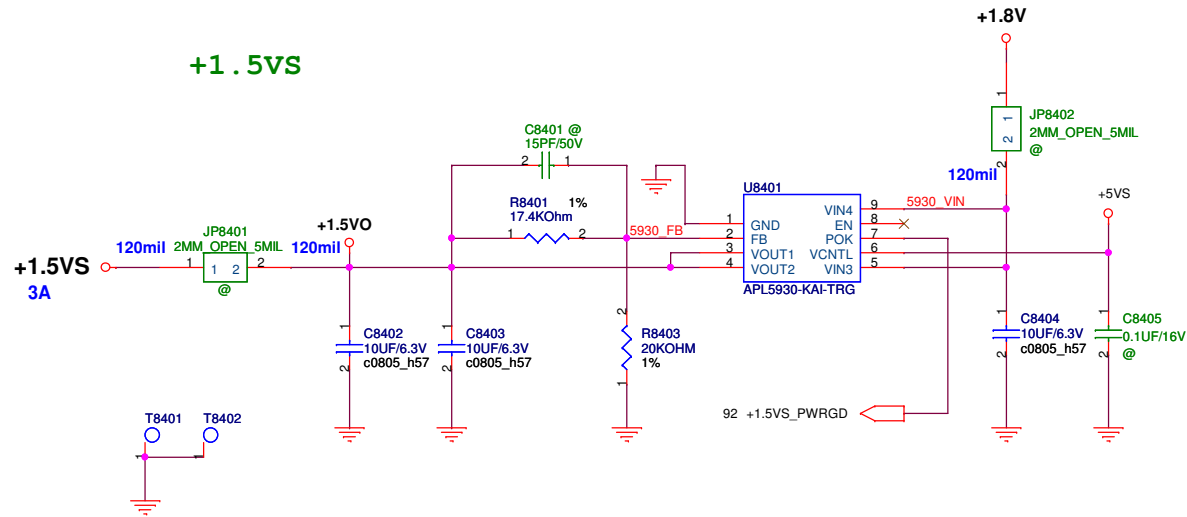






<Variant Name>

ASUS		Title :POWER_I/O_DDR
ASUSTeK COMPUTER INC. NB		Engineer: Morris
Size B	Project Name K50	Rev 1.0
Date: Monday, March 09, 2009		Sheet 83 of 96



Total count: 7 pcs

<Variant Name>

		Title : POWER_IO_+1.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Morris	
Size	Project Name		Rev
B	K50		1.0
Date: Monday, March 09, 2009		Sheet	84 of 96

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<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
A		1.0

Date: Monday, March 09, 2009 Sheet 85 of 96

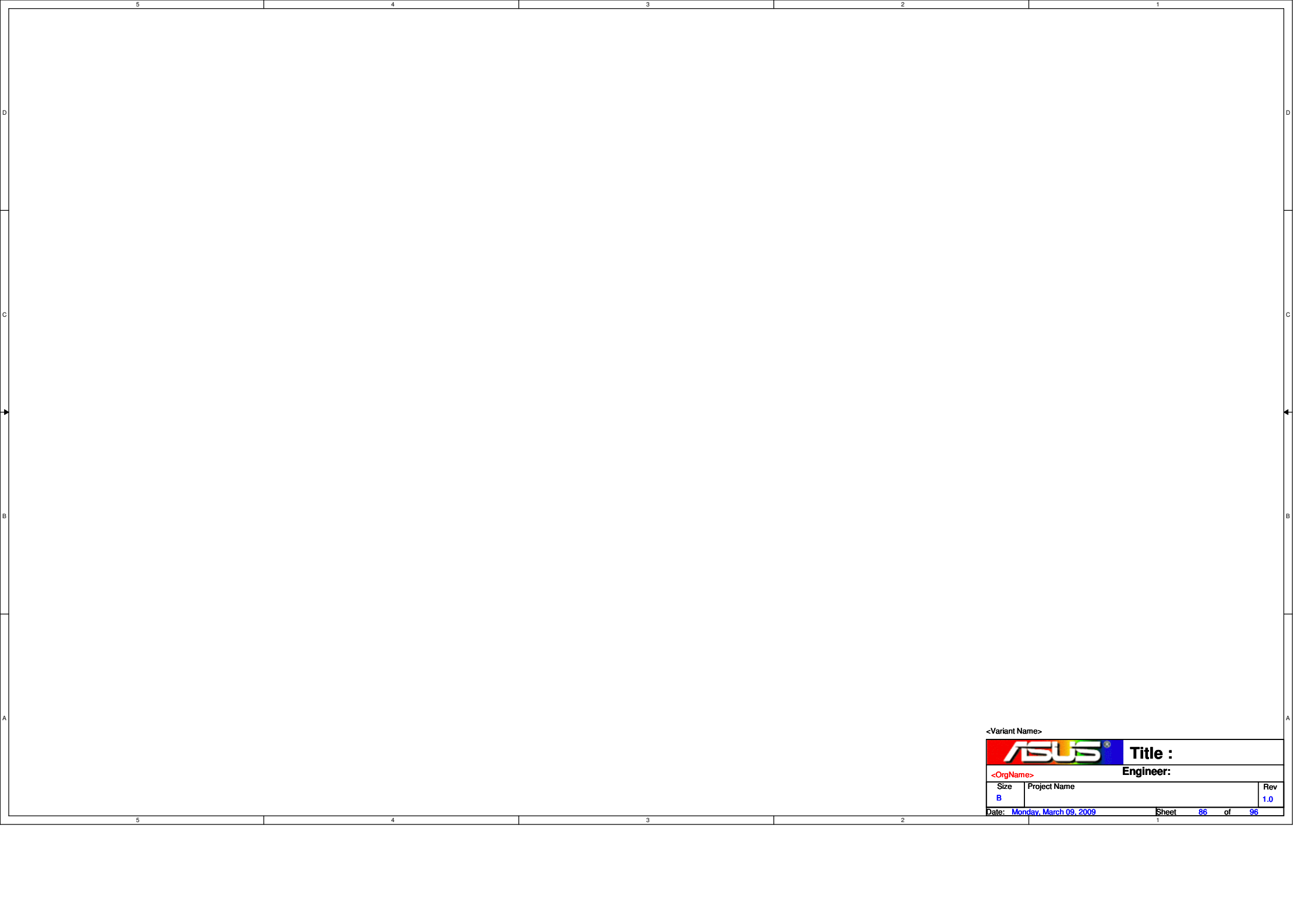
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<Variant Name>		
		Title :
<OrgName>		Engineer:
Size	Project Name	Rev
B		1.0
Date: Monday, March 09, 2009		Sheet 86 of 96

5

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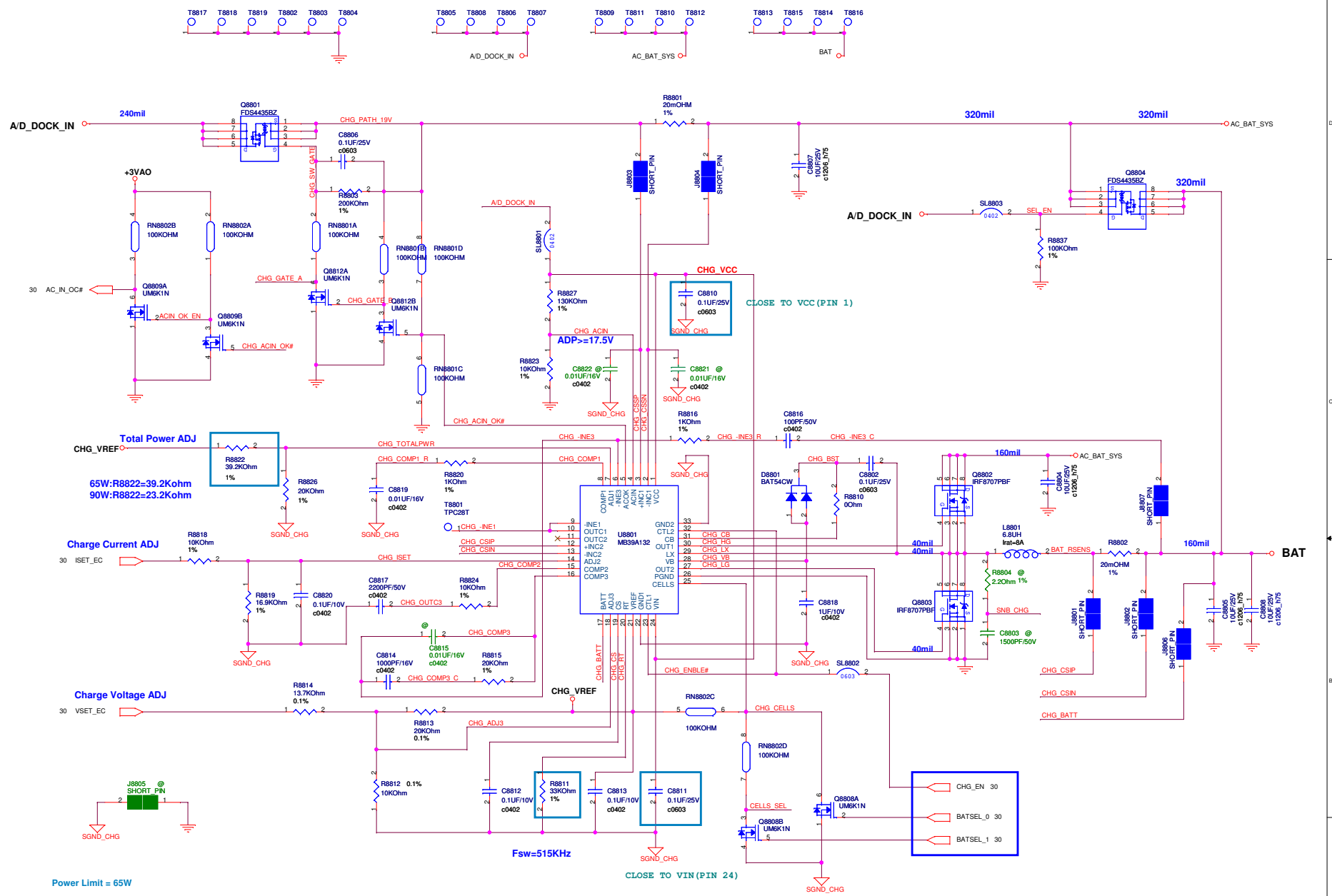
A

<Variant Name>



<OrgName> **Engineer:**

Size	Project Name	Rev
Custom		1.0

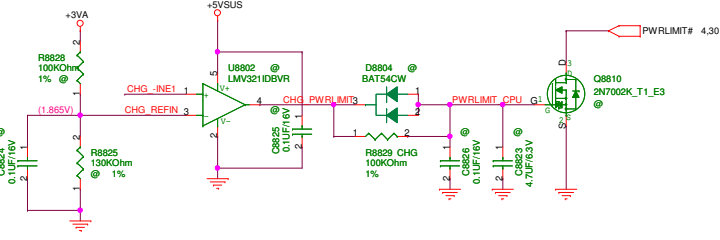


Total Power ADJ
 65W: R8822=39.2Kohm
 90W: R8822=23.2Kohm

Charge Current ADJ
 R8818 10KOhm 1%

Charge Voltage ADJ
 R8814 13.7KOhm 0.1%

Power Limit = 65W



TOTAL COUNT: 56 PCS

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

5

4

3

2

1

D

D

C

C


B

B

A


A

<Variant Name>

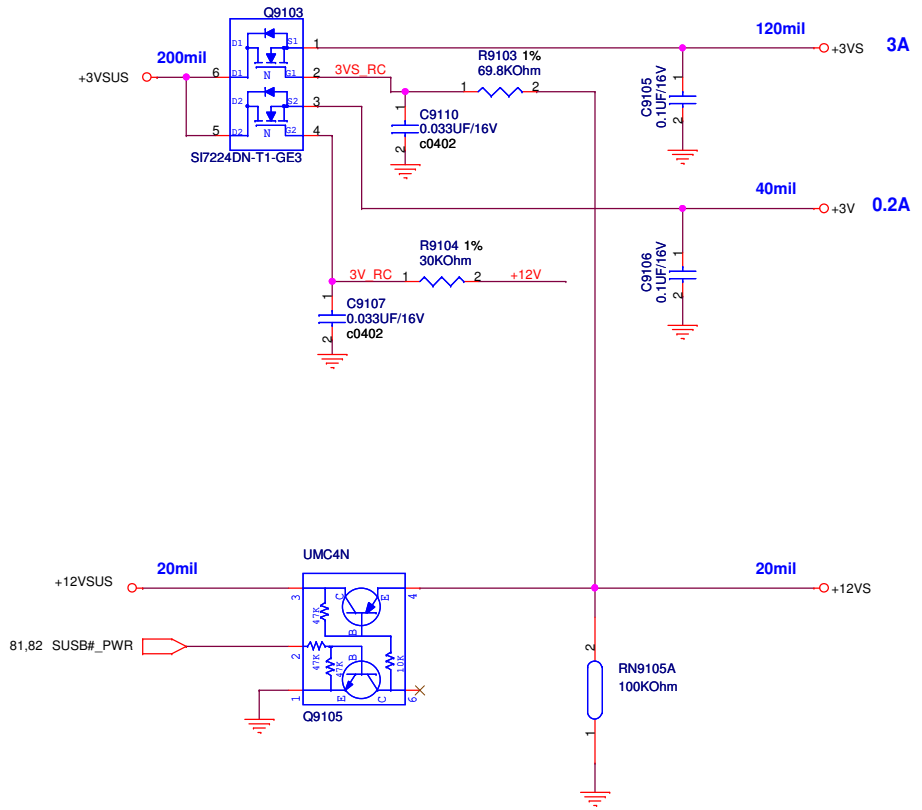
		Title :
<OrgName>		Engineer:
Size	Project Name	Rev
Custom		1.0
Date: Monday, March 09, 2009	Sheet	89 of 96

BATTERY IN DETECT

<Variant Name>

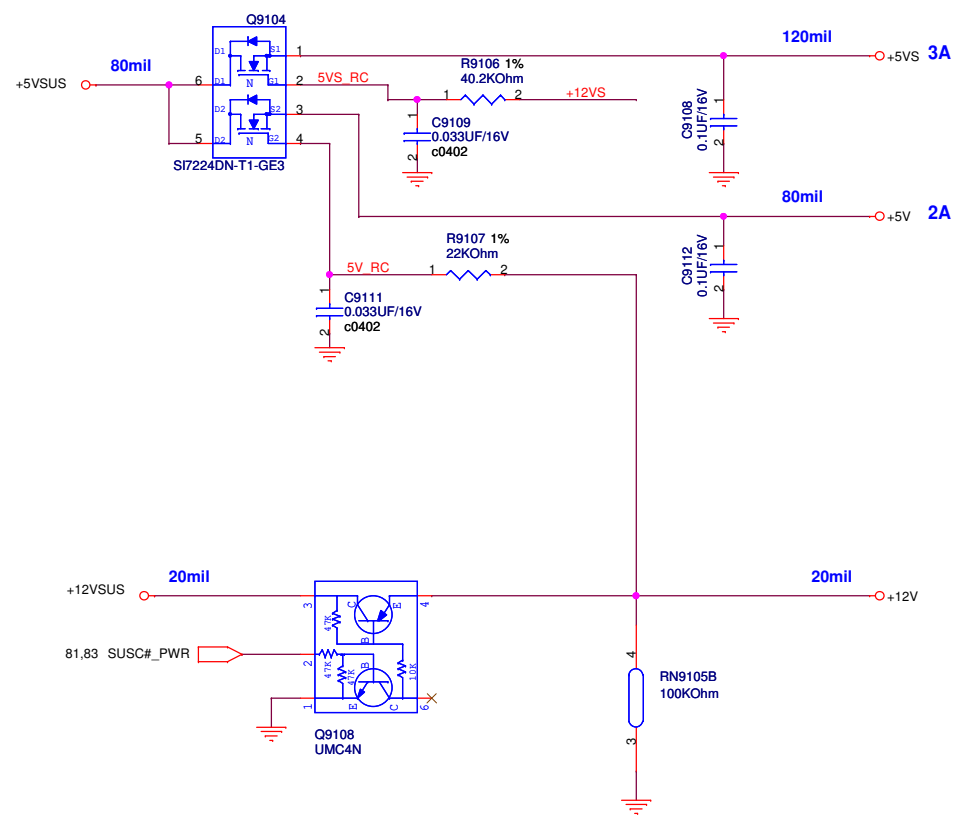
		Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
Custom	K50II	1.0	
Date: Monday, March 09, 2009		Sheet	90 of 96

SUSB#_PWR POWER



Total count: 19 pcs

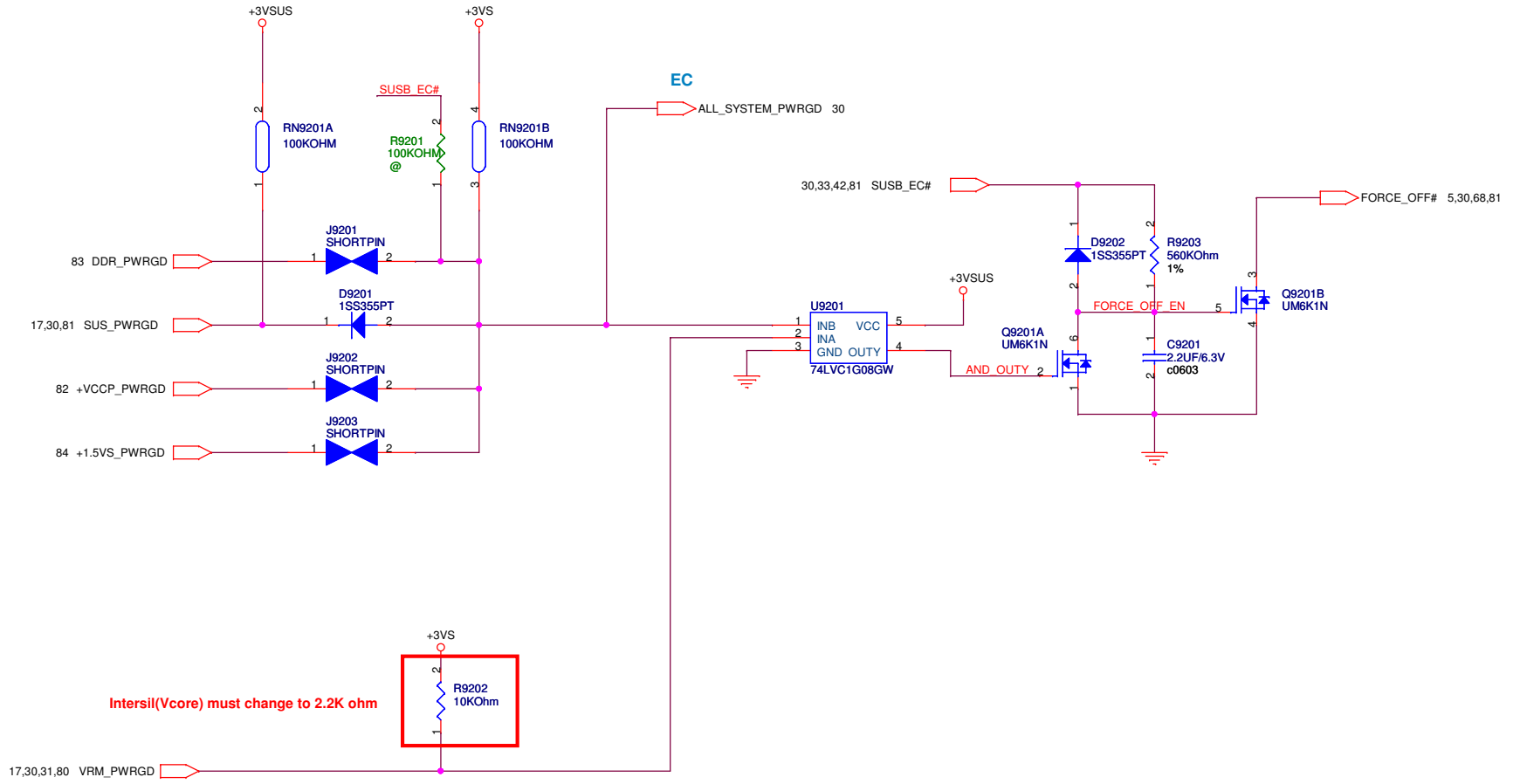
SUSC#_PWR POWER



<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size	Project Name	Rev	
B	K50	1.0	
Date: Monday, March 09, 2009		Sheet	91 of 96

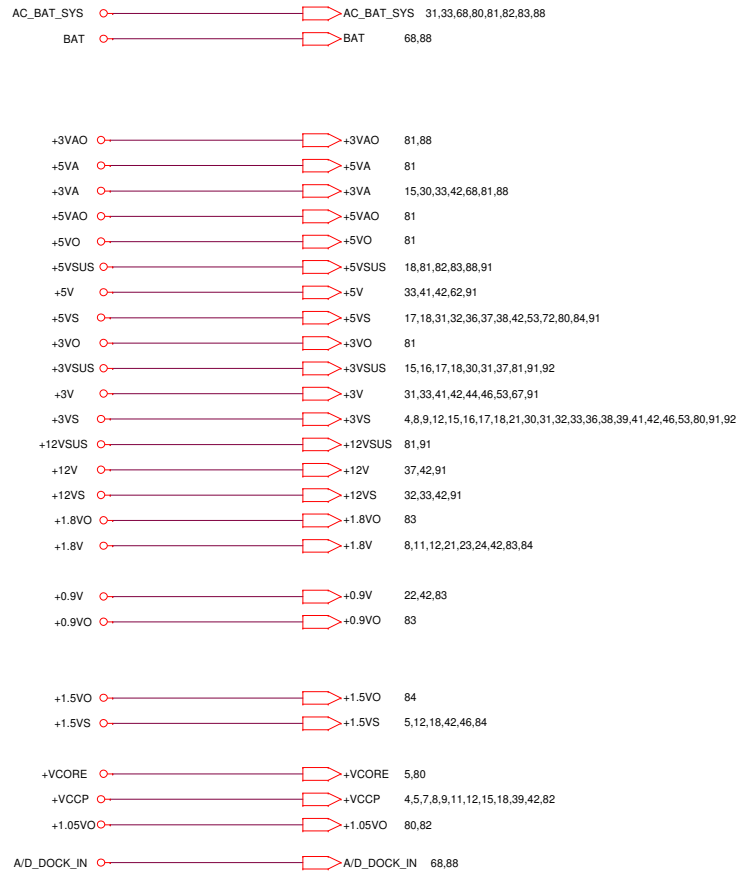
POWER GOOD DETECTOR



Total count: 8 pcs

<Variant Name>

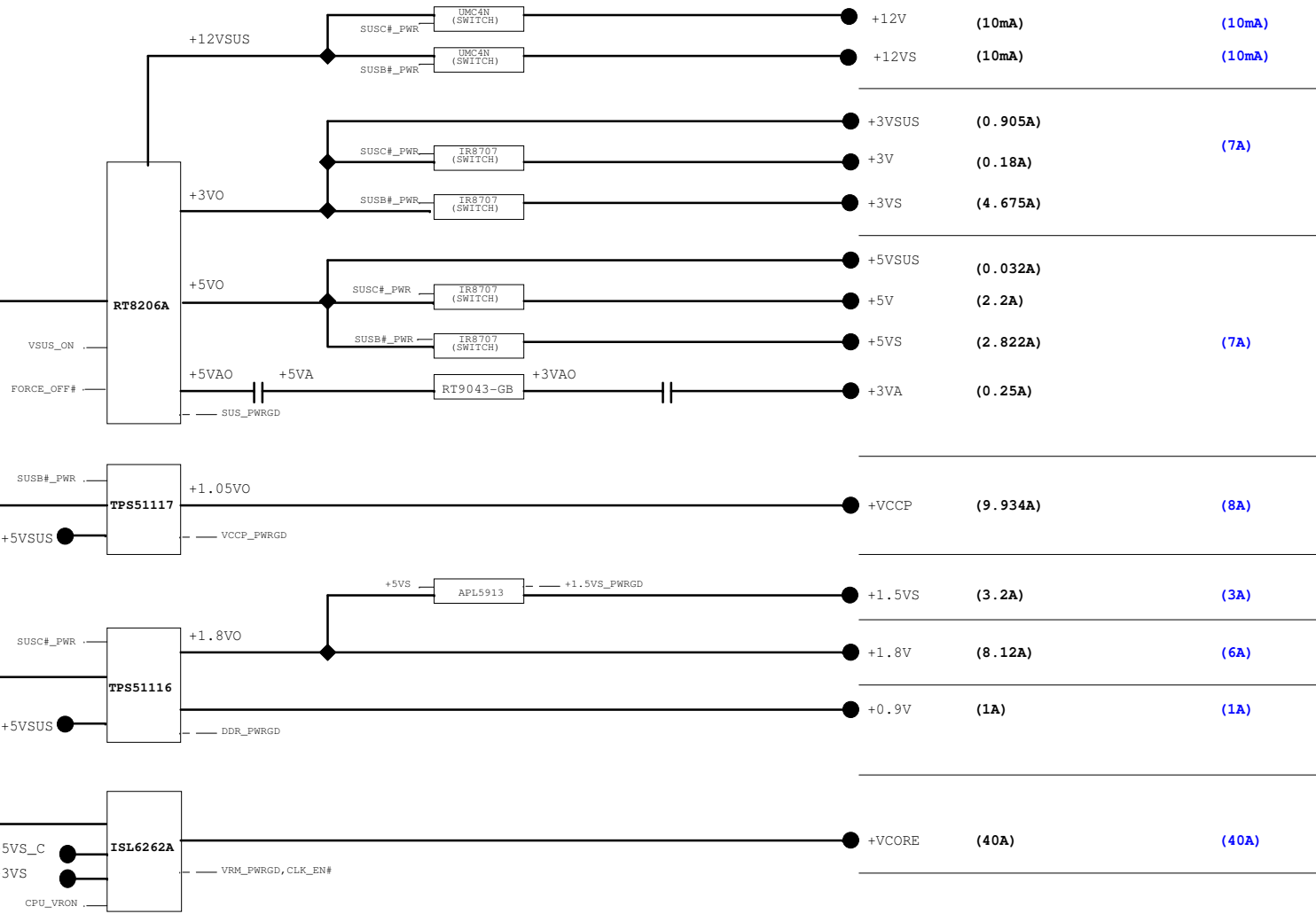
		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size B	Project Name K50	Rev 1.0	
Date: Monday, March 09, 2009		Sheet	92 of 96



<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: Morris	
Size	Project Name	Rev	
Custom	K50	1.0	
Date: Monday, March 09, 2009		Sheet 93 of 96	

AC_BAT_SYS



VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLEPR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON

K50
Non-IAMT **Design rating**

Output	Current	Design rating
+12V	(10mA)	(10mA)
+12VS	(10mA)	(10mA)
+3VSUS	(0.905A)	(7A)
+3V	(0.18A)	
+3VS	(4.675A)	
+5VSUS	(0.032A)	
+5V	(2.2A)	
+5VS	(2.822A)	(7A)
+3VA	(0.25A)	
+VCCP	(9.934A)	(8A)
+1.5VS	(3.2A)	(3A)
+1.8V	(8.12A)	(6A)
+0.9V	(1A)	(1A)
+V_CORE	(40A)	(40A)

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