K40AB SCHEMATIC R1.3

SYSTEM PAGE REF.

POWER PAGE REF.

ASUSTeK COMPUTER INC. NB1

Title : Page Reference

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

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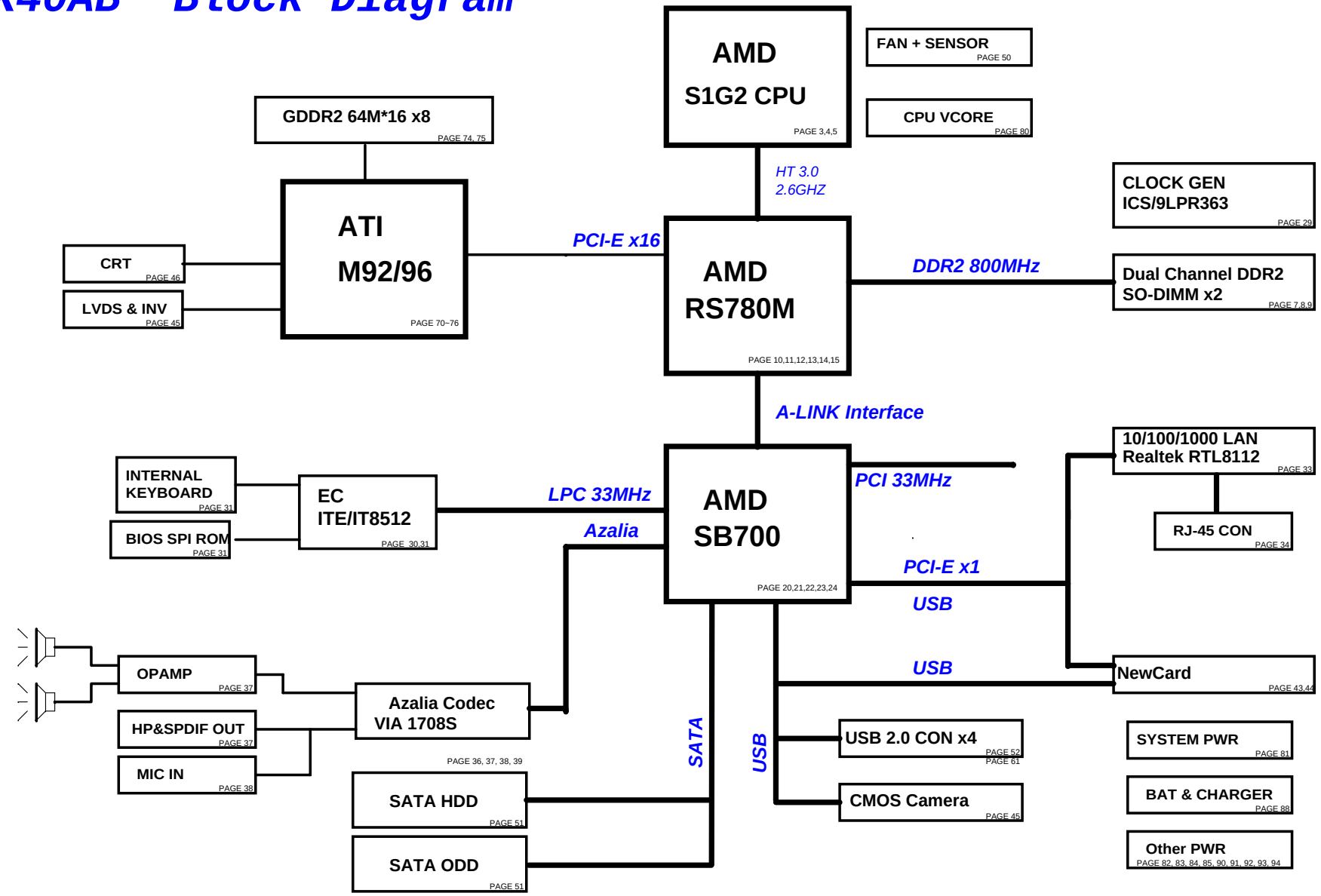
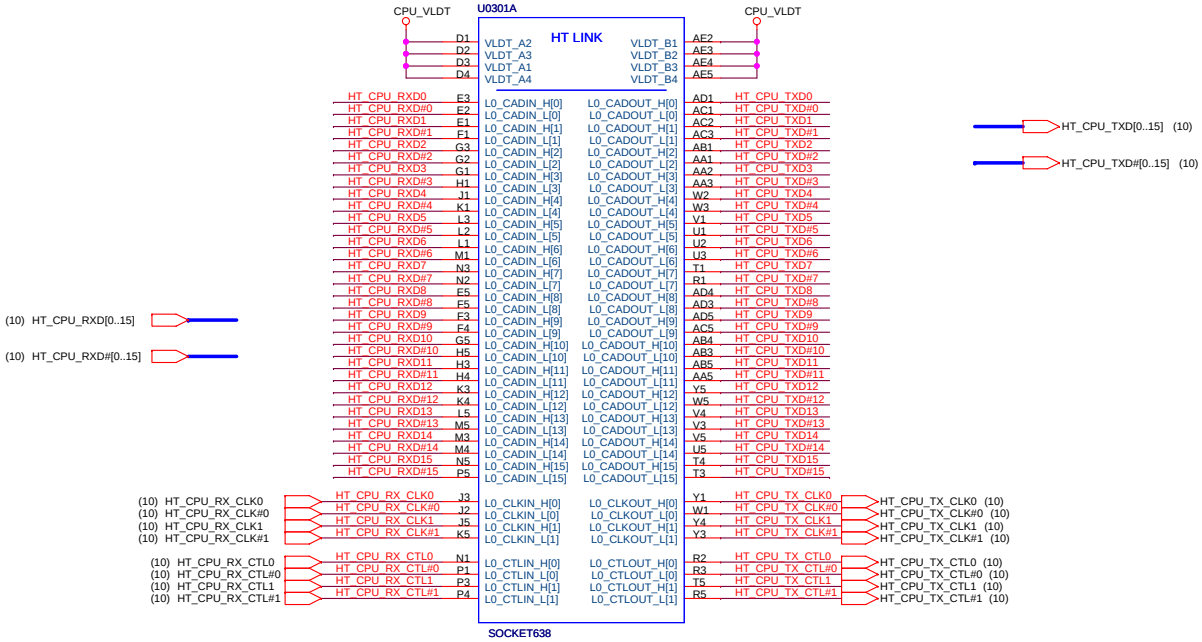
K40AB Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AB	Rev: R1.3
Date: Wednesday, April 08, 2009	Sheet 2 of 94	

1.5A



(10) HT_CPU_RXD[0..15]

(10) HT_CPU_RXD#[0..15]

HT_CPU_TXD[0..15] (10)

HT_CPU_TXD#[0..15] (10)

(10) HT_CPU_RX_CLK0
(10) HT_CPU_RX_CLK#0
(10) HT_CPU_RX_CLK1
(10) HT_CPU_RX_CLK#1

HT_CPU_TX_CLK0 (10)
HT_CPU_TX_CLK#0 (10)
HT_CPU_TX_CLK1 (10)
HT_CPU_TX_CLK#1 (10)

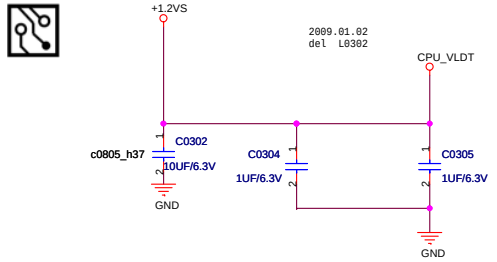
(10) HT_CPU_RX_CTL0
(10) HT_CPU_RX_CTL#0
(10) HT_CPU_RX_CTL1
(10) HT_CPU_RX_CTL#1

HT_CPU_TX_CTL0 (10)
HT_CPU_TX_CTL#0 (10)
HT_CPU_TX_CTL1 (10)
HT_CPU_TX_CTL#1 (10)

Change P/N to 12G011306380

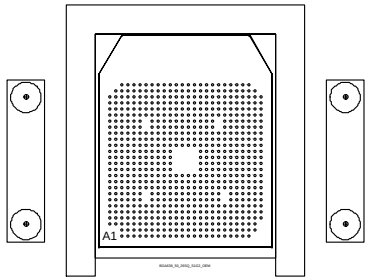
071113

Do not cross plane.



Place close to socket

*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**



ASUSTeK COMPUTER INC. NB1	Title : Griffin HT I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AB	Rev: R1.3
Date: Wednesday, April 08, 2009	Sheet 3 of 94	

Processor Memory Interface

0.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

place close to PROCESSOR within 1.5 inch

place close to PROCESSOR within 1.5 inch

071114

071115

U0301B

MEM:CMD/CTRL/CLK

SOCKET638

U0301C

MEM:DATA

SOCKET638

To SODIMM socket 1

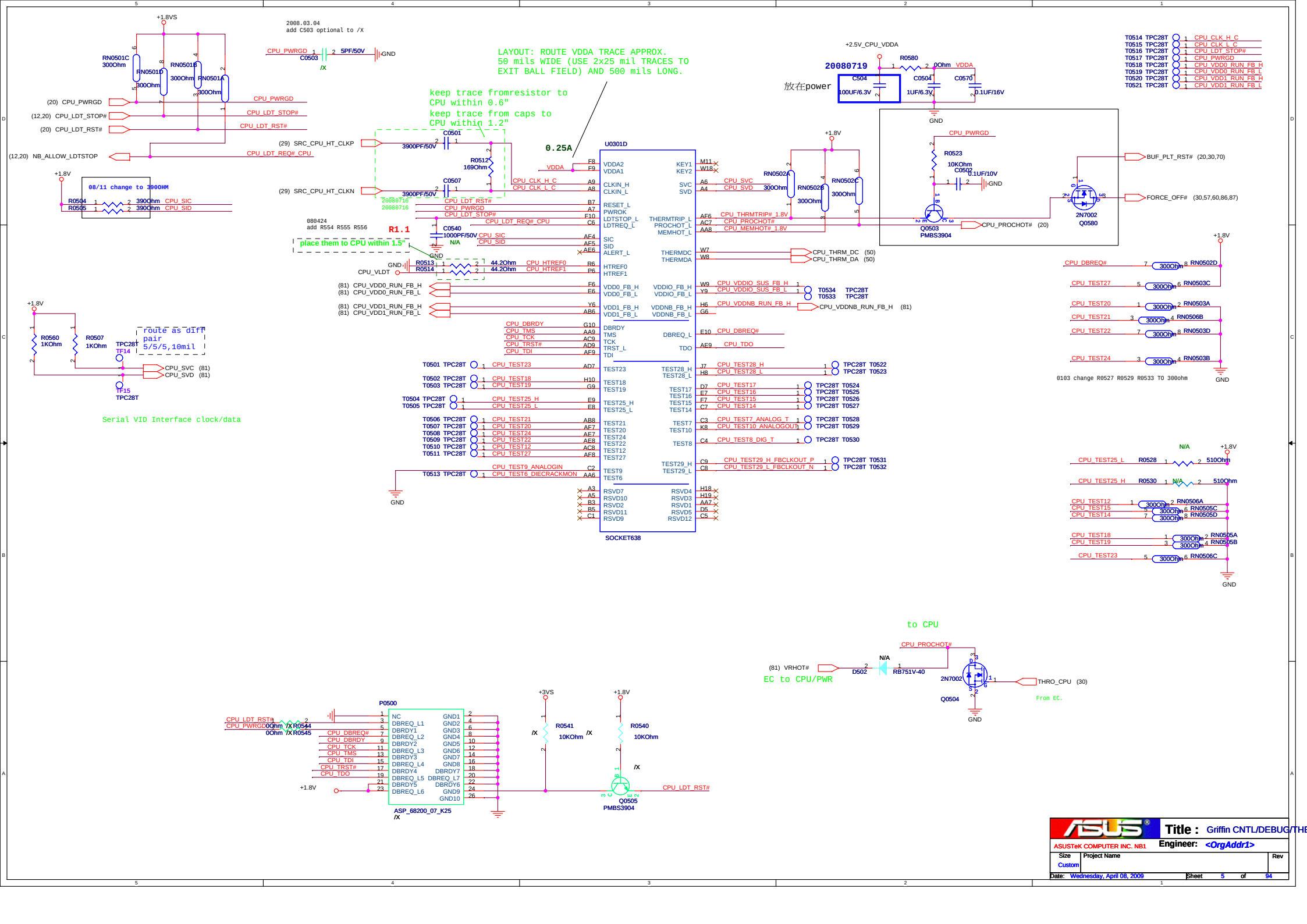
To SODIMM socket 0

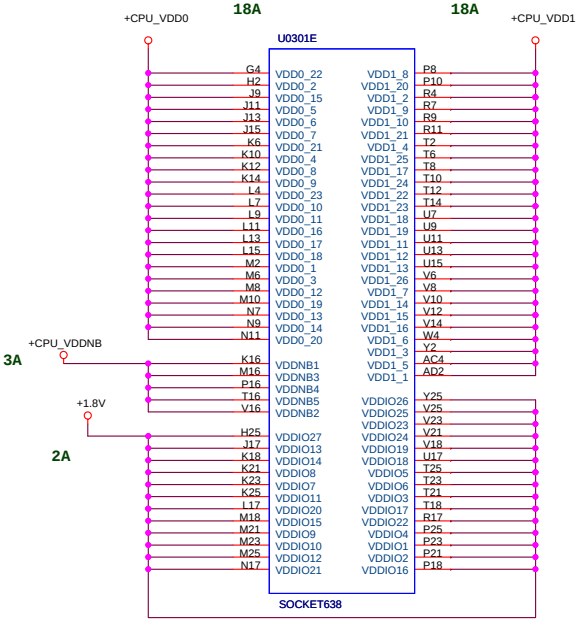
sensing point for op-amp feedback routed near CPU

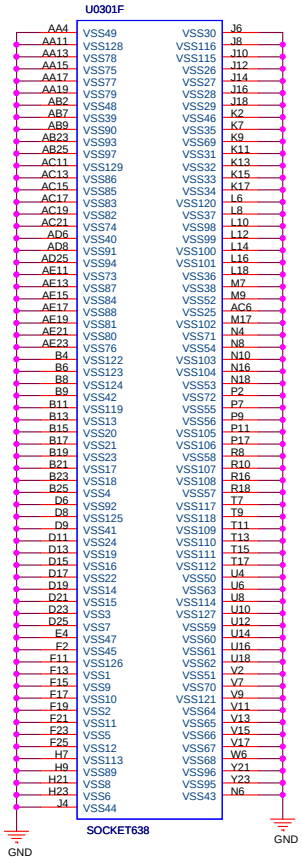
PLACE CLOSE TO CPU

09/23 2.0

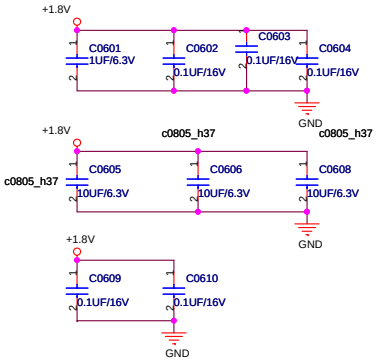
Title :	Griffin DDR2 MEMORY I/F		
ASUSTeK COMPUTER INC. NB1	Engineer:	<OrgAddr1>	
Size: Custom	Project Name		Rev
Date: Wednesday, April 08, 2009	Sheet 4	of 94	


+1.8VS
RN0501C 300Ohm
RN0501D 300Ohm
RN0501B 300Ohm
RN0501A 300Ohm
(20) CPU_PWRGD
(12,20) CPU_LDT_STOP#
(20) CPU_LDT_RST#
(12,20) NB_ALLOW_LDTSTOP
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
CPU_LDT_REQ#_CPU
2008.03.04
add C503 optional to /X
CPU_PWRGD
C0503
5PF/50V
GND
/X
LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
0.25A
+2.5V_CPU_VDDA
20080719
放在power
R0580
0Ohm VDDA
C504
100UF/6.3V
C0504
1UF/6.3V
C0570
0.1UF/16V
GND
T0514 TPC28T CPU_CLK_H_C
T0515 TPC28T CPU_CLK_L_C
T0516 TPC28T CPU_LDT_STOP#
T0517 TPC28T CPU_PWRGD
T0518 TPC28T CPU_VDD0_RUN_FB_H
T0519 TPC28T CPU_VDD0_RUN_FB_L
T0520 TPC28T CPU_VDD1_RUN_FB_H
T0521 TPC28T CPU_VDD1_RUN_FB_L
+1.8V
08/11 change to 300OHM
R0504 390Ohm CPU_SIC
R0505 390Ohm CPU_SID
(29) SRC_CPU_HT_CLKP
(29) SRC_CPU_HT_CLKN
C0501
3900PF/50V
C0507
3900PF/50V
R0512
169Ohm
20080716
20080716
CPU_CLK_H_C
CPU_CLK_L_C
CPU_LDT_RST#
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_REQ#_CPU
080424
add R554 R555 R556
R1.1
C0540
1000PF/50V
N/A
place them to CPU within 1.5"
CPU_SIC
CPU_SID
GND
R0513 44.2Ohm CPU_HTREF0
R0514 44.2Ohm CPU_HTREF1
CPU_VLDT
(81) CPU_VDD0_RUN_FB_H
(81) CPU_VDD0_RUN_FB_L
(81) CPU_VDD1_RUN_FB_H
(81) CPU_VDD1_RUN_FB_L
U0301D
VDDA
VDDA2
VDDA1
CLKIN_H
CLKIN_L
RESET_L
PWROK
LDTSTOP_L
LDTREQ_L
SIC
SID
ALERT_L
HTREF0
HTREF1
VDD0_FB_H
VDD0_FB_L
VDD1_FB_H
VDD1_FB_L
DBRDY
TMS
TCK
TRST_L
TDI
TEST23
TEST18
TEST19
TEST25_H
TEST25_L
TEST21
TEST20
TEST24
TEST22
TEST12
TEST27
TEST9
TEST6
RSVD7
RSVD10
RSVD2
RSVD11
RSVD9
KEY1
KEY2
SVC
SVD
THERMTRIP_L
PROCHOT_L
MEMHOT_L
THERMDC
THERMDA
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
DBREQ_L
TDO
TEST28_H
TEST28_L
TEST17
TEST16
TEST15
TEST14
TEST7
TEST10
TEST8
TEST29_H
TEST29_L
RSVD4
RSVD3
RSVD1
RSVD5
RSVD12
SOCKET638
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
T0501 TPC28T CPU_TEST23
T0502 TPC28T CPU_TEST18
T0503 TPC28T CPU_TEST19
T0504 TPC28T CPU_TEST25_H
T0505 TPC28T CPU_TEST25_L
T0506 TPC28T CPU_TEST21
T0507 TPC28T CPU_TEST20
T0508 TPC28T CPU_TEST24
T0509 TPC28T CPU_TEST22
T0510 TPC28T CPU_TEST12
T0511 TPC28T CPU_TEST27
CPU_TEST9_ANALOGIN
T0513 TPC28T CPU_TEST6_DIECRACKMON
GND
+1.8V
RN0502A 300Ohm
RN0502B 300Ohm
RN0502C 300Ohm
CPU_THRMTRIP# 1.8V
CPU_PROCHOT#
CPU_MEMHOT# 1.8V
CPU_THRM_DC (50)
CPU_THRM_DA (50)
CPU_VDDIO_SUS_FB_H
CPU_VDDIO_SUS_FB_L
T0534 TPC28T
T0533 TPC28T
CPU_VDDNB_RUN_FB_H
CPU_VDDNB_RUN_FB_H (81)
CPU_DBREQ#
CPU_TDO
CPU_TEST28_H
CPU_TEST28_L
T0522 TPC28T
T0523 TPC28T
CPU_TEST17
CPU_TEST16
CPU_TEST15
CPU_TEST14
T0524 TPC28T
T0525 TPC28T
T0526 TPC28T
T0527 TPC28T
CPU_TEST7_ANALOG_T
CPU_TEST10_ANALOGOUT
T0528 TPC28T
T0529 TPC28T
CPU_TEST8_DIG_T
T0530 TPC28T
CPU_TEST29_H_FBCLKOUT_P
CPU_TEST29_L_FBCLKOUT_N
T0531 TPC28T
T0532 TPC28T
CPU_PWRGD
R0523
10KOhm
C0502
0.1UF/10V
GND
Q0503
PMBS3904
2N7002
Q0580
BUF_PLT_RST# (20,30,70)
FORCE_OFF# (30,57,60,86,87)
CPU_PROCHOT# (20)
CPU_DBREQ# RN0502D 300Ohm
CPU_TEST27 RN0503C 300Ohm
CPU_TEST20 RN0503A 300Ohm
CPU_TEST21 RN0506B 300Ohm
CPU_TEST22 RN0503D 300Ohm
CPU_TEST24 RN0503B 300Ohm
0103 change R0527 R0529 R0533 TO 300ohm
GND
+1.8V
R0560 1KOhm
R0507 1KOhm
route as diff pair 5/5/5,10mil
TPC28T TF14
TF15 TPC28T
CPU_SVC (81)
CPU_SVD (81)
Serial VID Interface clock/data
N/A
+1.8V
CPU_TEST25_L R0528 510Ohm
CPU_TEST25_H R0530 N/A 510Ohm
CPU_TEST12 RN0506A 300Ohm
CPU_TEST15 RN0505C 300Ohm
CPU_TEST14 RN0505D 300Ohm
CPU_TEST18 RN0505A 300Ohm
CPU_TEST19 RN0505B 300Ohm
CPU_TEST23 RN0506C 300Ohm
GND
to CPU
CPU_PROCHOT#
(81) VRHOT#
N/A
D502
RB751V-40
EC to CPU/PWR
2N7002
Q0504
THRO_CPU (30)
From EC.
GND
P0500
CPU_LDT_RST#
CPU_PWRGD
0Ohm /X R0544
0Ohm /X R0545
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
+1.8V
NC
DBREQ_L1
DBRDY1
DBREQ_L2
DBRDY2
DBREQ_L3
DBRDY3
DBREQ_L4
DBRDY4
DBREQ_L5
DBRDY5
DBREQ_L6
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
DBRDY7
DBREQ_L7
DBRDY6
GND9
GND10
ASP_68200_07_K25
/X
+3VS
R0541 10KOhm /X
+1.8V
R0540 10KOhm /X
Q0505
PMBS3904
CPU_LDT_RST#



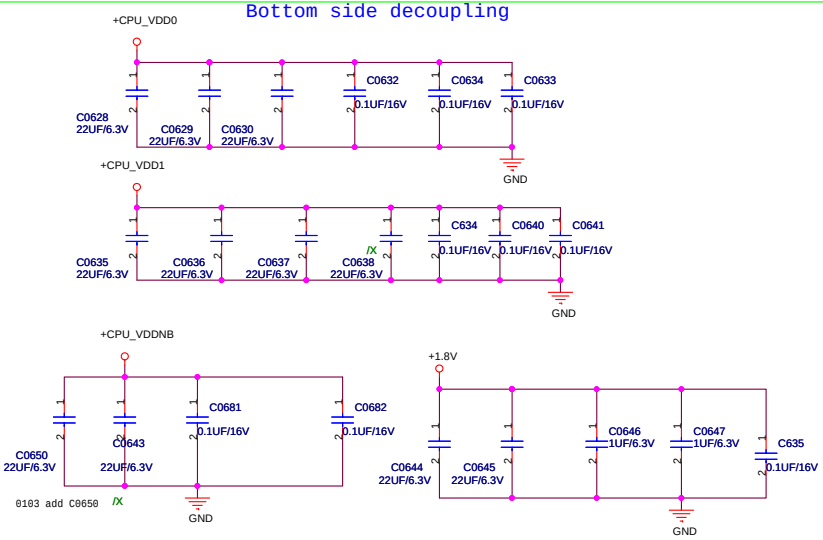


Decoupling between Processor and DIMMs, Place close to Porcessor as possible



place close to socket

Bottom side decoupling



ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER		
	Engineer: <OrgAddr1>		
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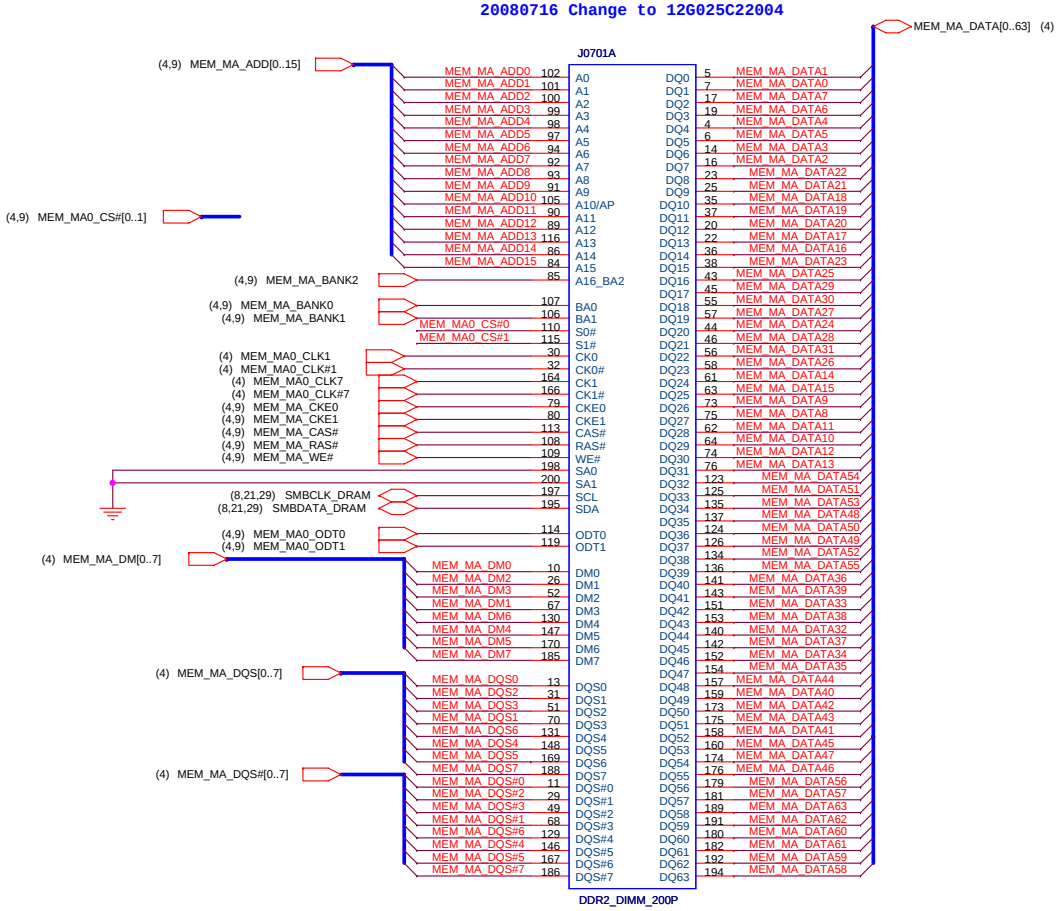
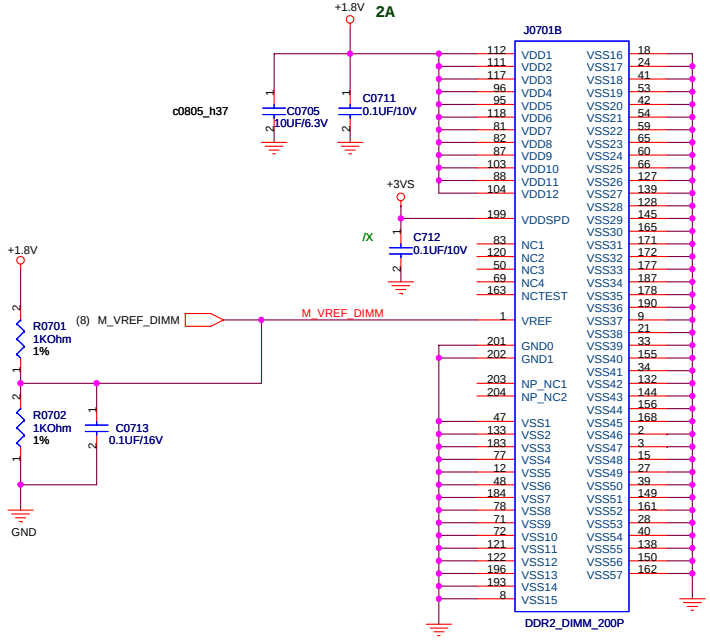
20080716 Change to 12G025C22004



High



ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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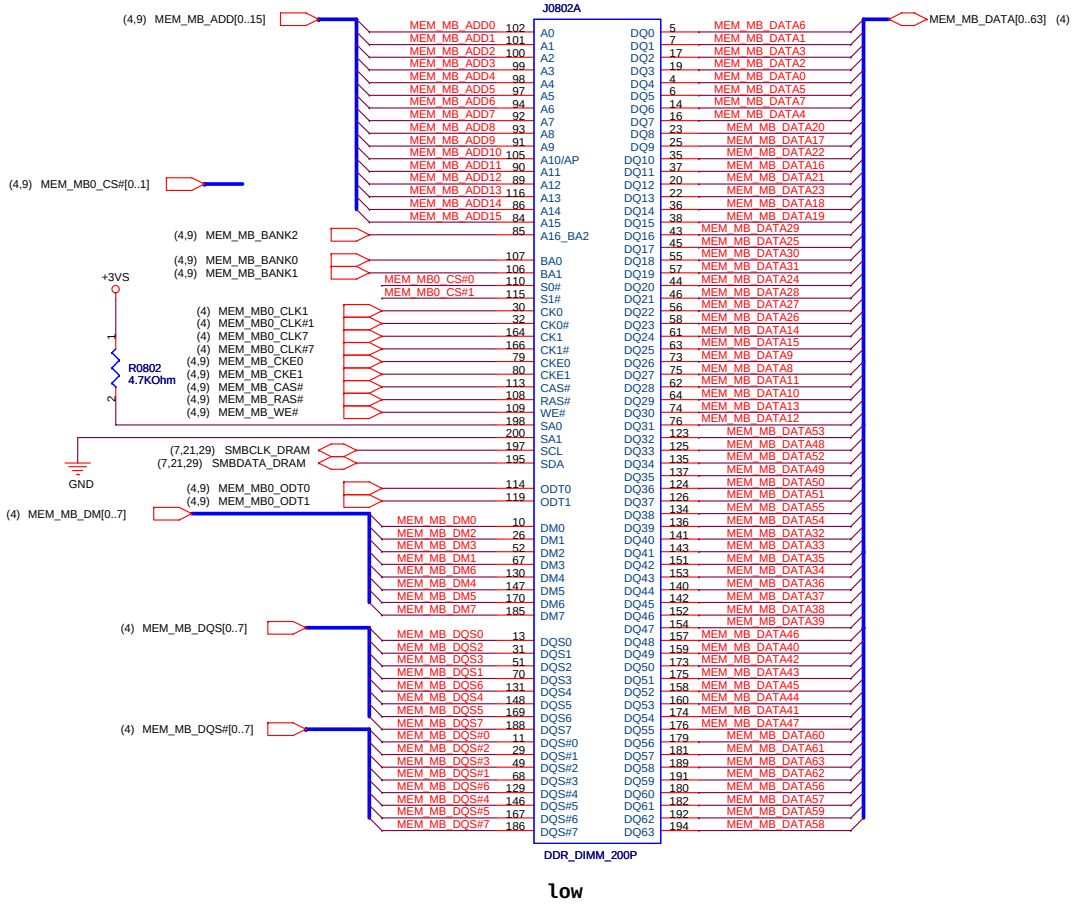

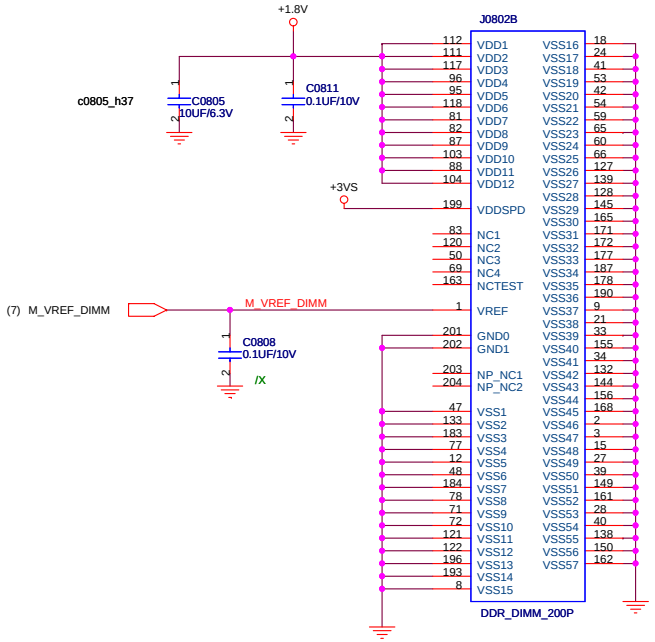

ASUSTeK COMPUTER INC. NB1

Title : DDR2 SO-DIMM1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

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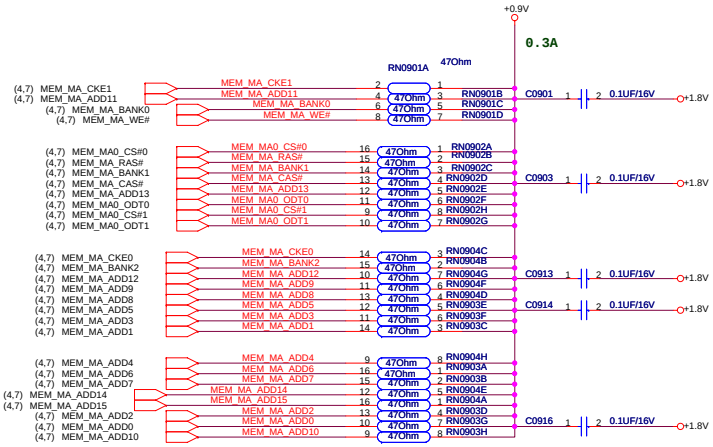
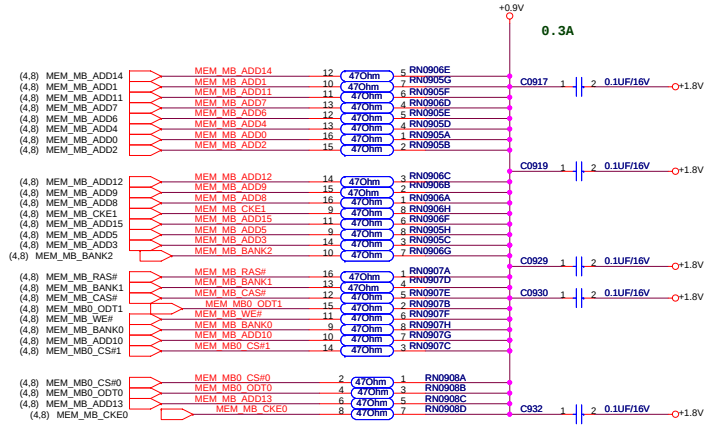
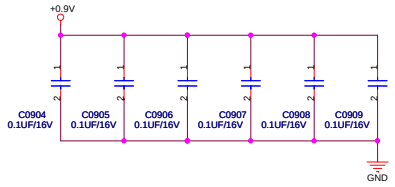
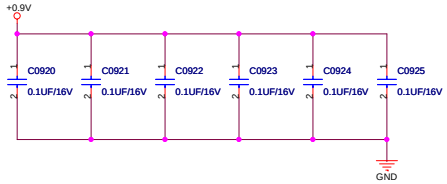
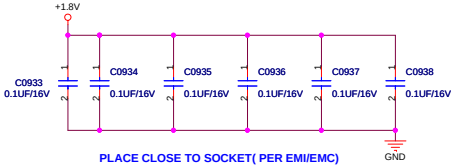


20080803 Remove R907









PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
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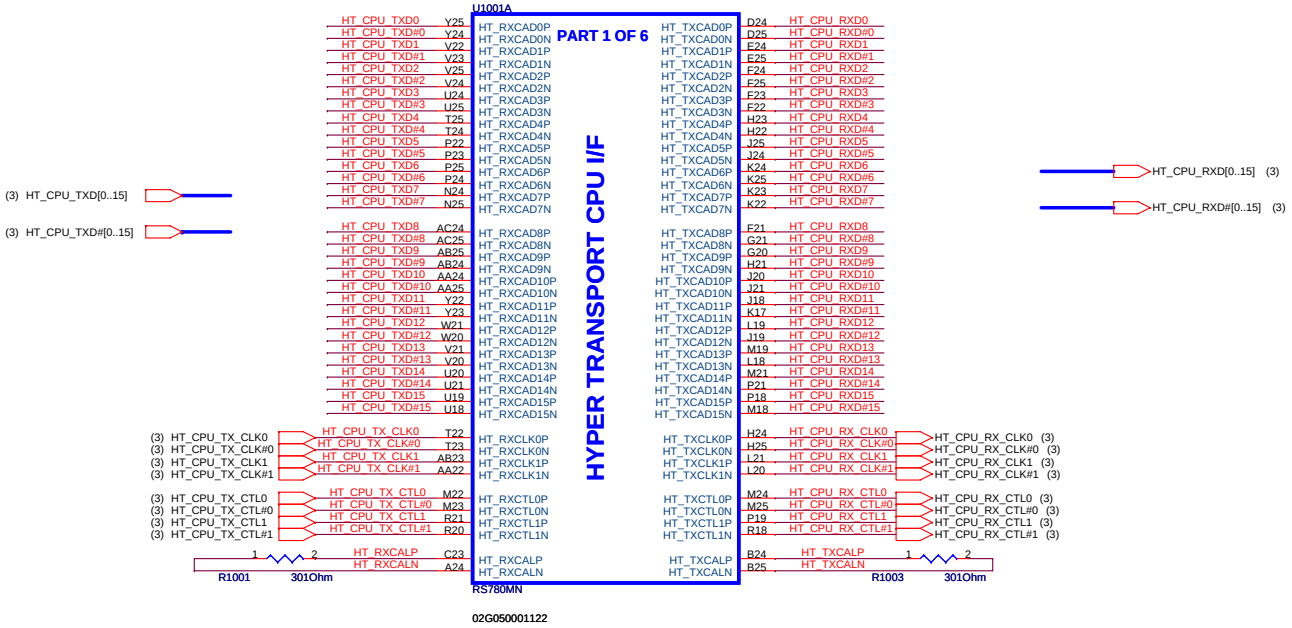
Title : DDR2_TERMINATIONS



02G050001122

ASUSTeK COMPUTER INC. NB1	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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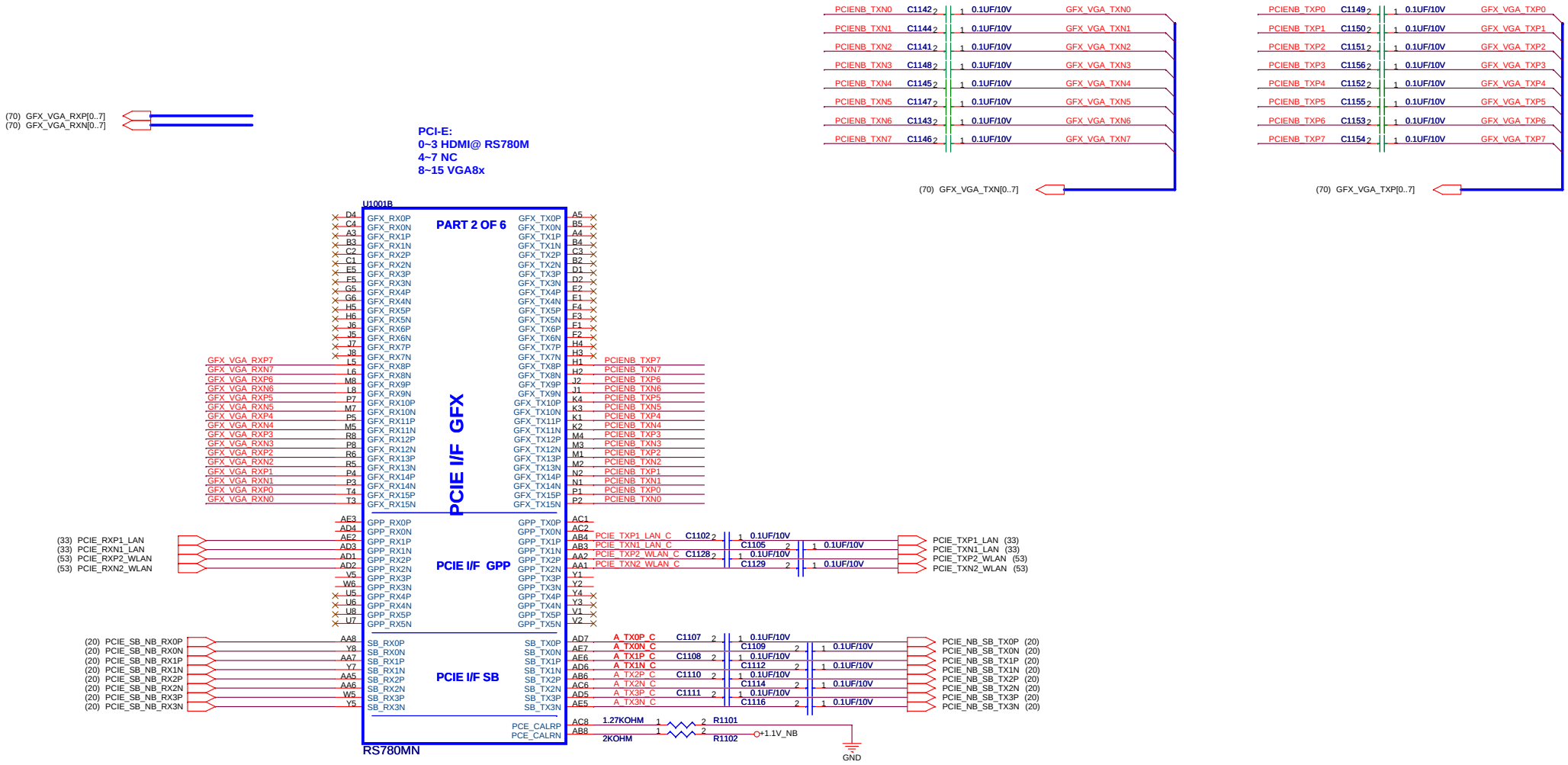

ASUSTeK COMPUTER INC. NB1	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name		Rev
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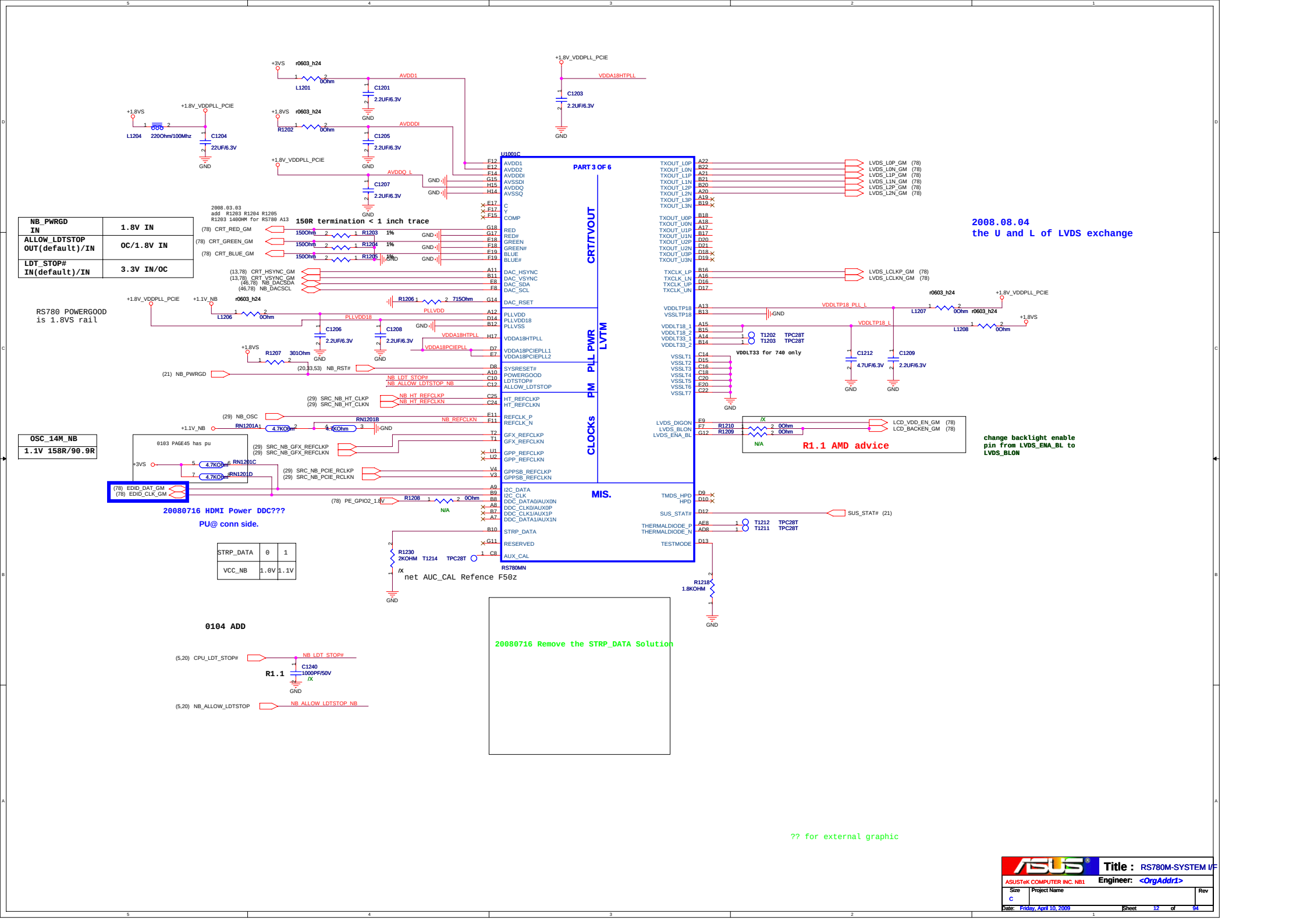

NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

2008.03.03
add R1203 R1204 R1205
R1203 1400HM for RS780 A13

150R termination < 1 inch trace

RS780 POWERGOOD is 1.8VS rail

OSC_14M_NB
1.1V 158R/90.9R

0103 PAGE45 has pu

20080716 HDMI Power DDC???

PU@ conn side.

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

0104 ADD

(5,20) CPU_LDT_STOP#
NB_LDT_STOP#
R1.1
C1240
1000PF/50V
/X
(5,20) NB_ALLOW_LDTSTOP
NB_ALLOW_LDTSTOP_NB

20080716 Remove the STRP_DATA Solution

2008.08.04
the U and L of LVDS exchange

change backlight enable pin from LVDS_ENA_BL to LVDS_BLON

R1.1 AMD advice

?? for external graphic

Title : RS780M-SYSTEM I/F		
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: C	Project Name	Rev
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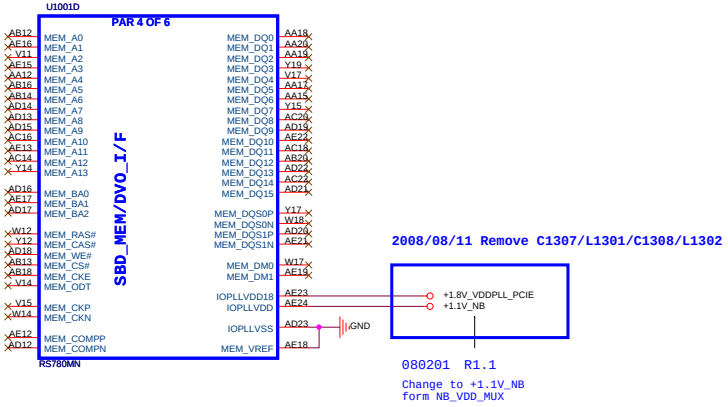
R1.11 080319

Change the NB Part number to RS780 (A13)



2008/08/11 Remove C1307/L1301/C1308/L1302

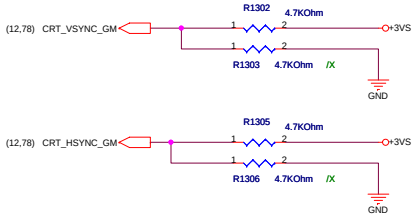
080201 R1.1

Change to +1.1V_NB
form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

ASUSTeK COMPUTER INC. NB1

Title : RS780M-SPMEM/STRAPS

Engineer: <OrgAddr1>

Size: C | Project Name | Rev

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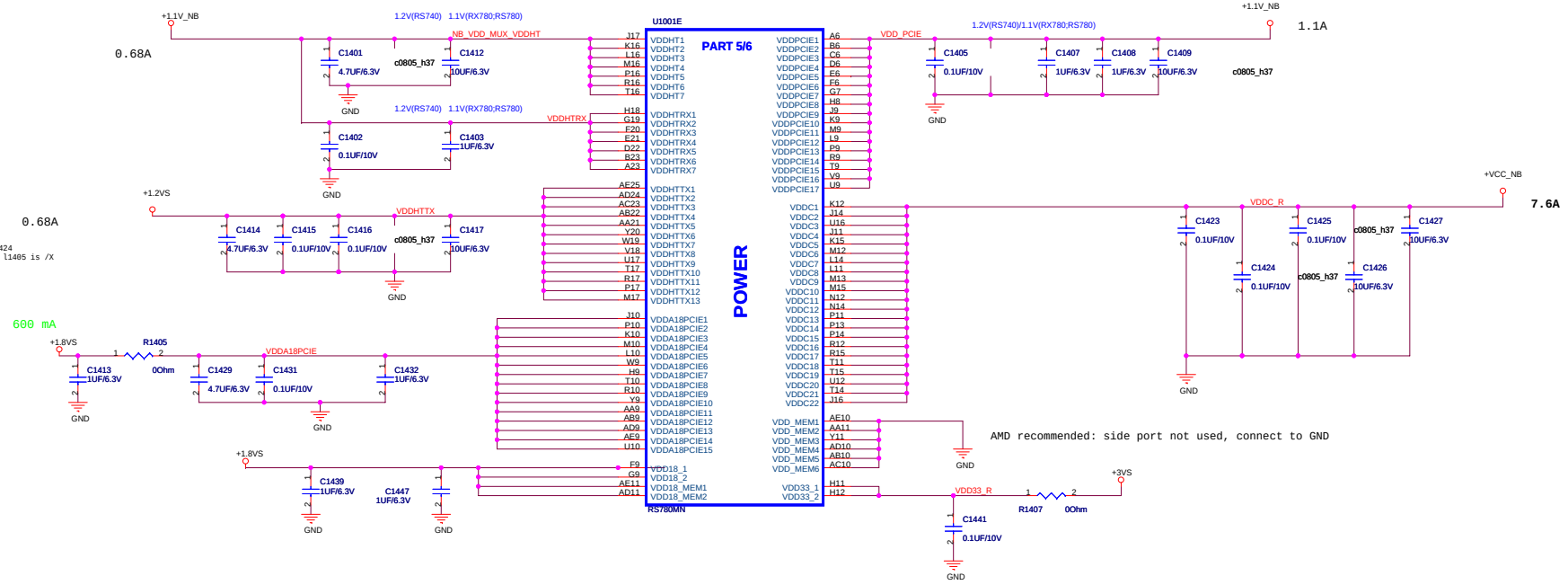

ASUSTeK COMPUTER INC. NB1	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name		Rev
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2008/08/11 AMD Review

SB700
Part 1 of 5
U2001A

DEL 0 OHM

2008.03.05
R2009 R2036 R2037 PN to 10G212000004010

Refence F50z

internal Pull Up 8.2K

0109

2008.03.11
C2018乙C2019乙C2020乙C2017乙C2021乙 C2022 change to 15pf,optional is N/A

080424
add R2042 R2041 R2040

080423
ADD R2039 Q2001

2008.03.03
D2001 R2022 optional change to /X, R2035 change to N/A

0110 add for safety

2008/0805 Add C2024 for NB_RST# Glitch

02G050001810

Title :	SB700_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>
Size: C	Project Name
Rev	
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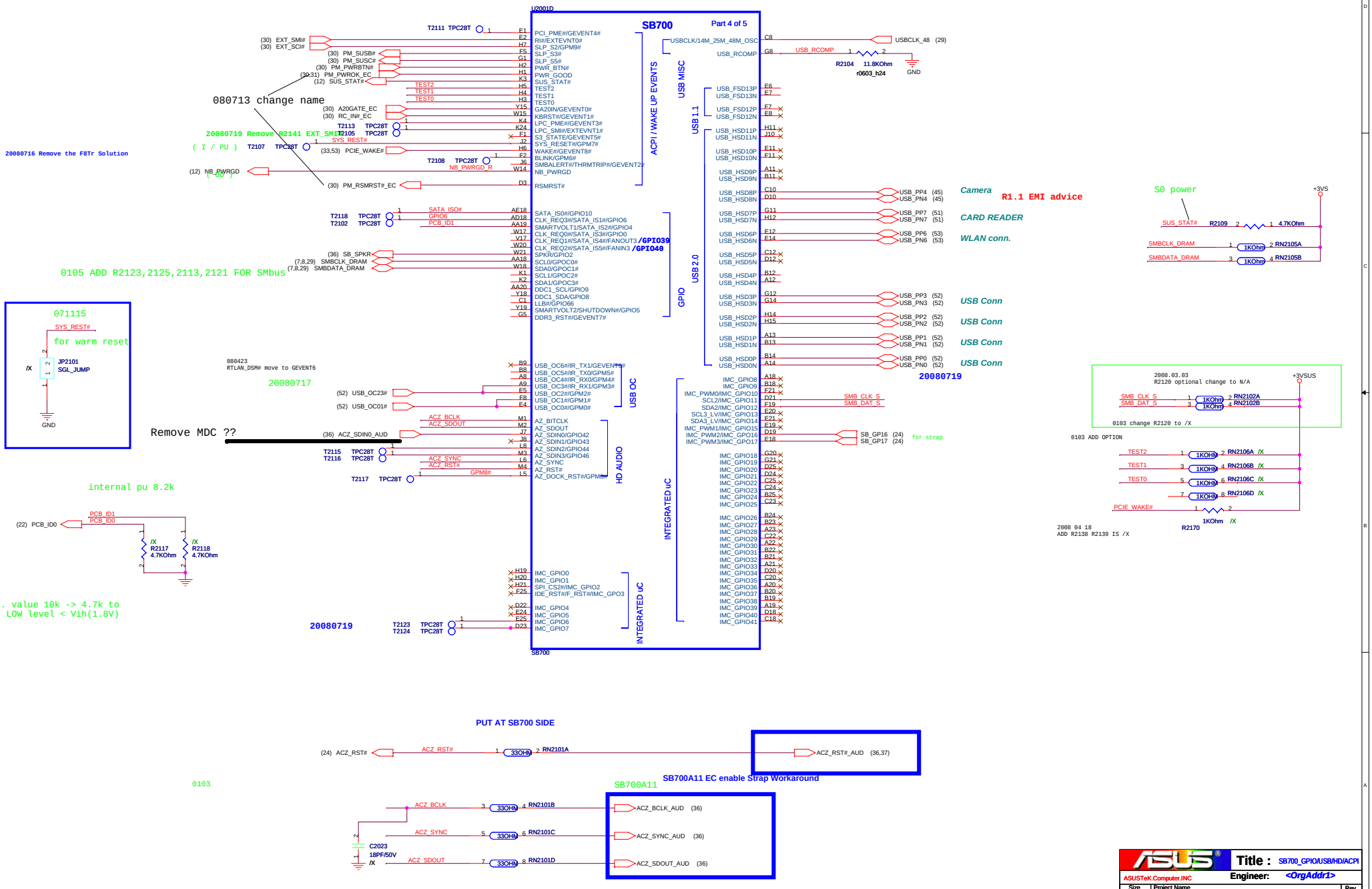

U2001D
SB700
Part 4 of 5
SB700
080713 change name
20080719 Remove R2141 EXT_SMI#
20080716 Remove the F8Tr Solution
(I / PU)
(OD)
0105 ADD R2123,2125,2113,2121 FOR SMbus
071115
SYS_REST#
for warm reset
JP2101
SGL_JUMP
GND
Remove MDC ??
080423
RTLAN_DSM# move to GEVENT6
20080717
internal pu 8.2k
PCB_ID1
PCB_ID0
R2117
4.7KOhm
R2118
4.7KOhm
res. value 10k -> 4.7k to
get LOW level < Vih(1.8V)
20080719
20080719
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3 /GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3 /GPIO48
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT9#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
R2104 11.8KOhm r0603_h24
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
Camera
R1.1 EMI advice
CARD READER
WLAN conn.
USB Conn
USB Conn
USB Conn
USB Conn
20080719
S0 power
+3VS
SUS_STAT#
R2109 4.7KOhm
SMBCLK_DRAM
SMBDATA_DRAM
RN2105A
RN2105B
2008.03.03
R2120 optional change to N/A
+3VSUS
RN2102A
RN2102B
0103 change R2120 to /X
0103 ADD OPTION
TEST2
TEST1
TEST0
RN2106A /X
RN2106B /X
RN2106C /X
RN2106D /X
PCIE_WAKE#
R2170 1KOhm /X
2008 04 18
ADD R2138 R2139 IS /X
PUT AT SB700 SIDE
ACZ_RST#
33OHM
RN2101A
ACZ_RST#_AUD (36,37)
SB700A11 EC enable Strap Workaround
0103
SB700A11
ACZ_BCLK
ACZ_SYNC
ACZ_SDOUT
RN2101B
RN2101C
RN2101D
C2023
18PF/50V
ACZ_BCLK_AUD (36)
ACZ_SYNC_AUD (36)
ACZ_SDOUT_AUD (36)
Title : SB700_GPIO/USB/HD/ACPI
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name
Rev
Date: Wednesday, April 08, 2009
Sheet 21 of 94

2008.03.03
R2208 R2209 R2210 R2211 R2212 R2213 from 4.99OHM to 0OHM

2008/08/11 Remove R2208/R2209/R2210/R2211/R2212/R2213

for SATA HDD

for SATA ODD

(51) SATA_TXP0_HDD
(51) SATA_TXN0_HDD
(51) SATA_RXN0_HDD
(51) SATA_RXP0_HDD
(51) SATA_TXP1
(51) SATA_TXN1
(51) SATA_RXN1
(51) SATA_RXP1

U2001B

SB700
Part 2 of 5

SERIAL ATA
SATA_TX0P AD9
SATA_TX0N AE9
SATA_RX0N AB10
SATA_RX0P AC10
SATA_TX1P AE10
SATA_TX1N AD10
SATA_RX1N AD11
SATA_RX1P AE11
SATA_TX2P AB12
SATA_TX2N AC12
SATA_RX2N AE12
SATA_RX2P AD12
SATA_TX3P AD13
SATA_TX3N AE13
SATA_RX3N AB14
SATA_RX3P AC14
SATA_TX4P AE14
SATA_TX4N AD14
SATA_RX4N AD15
SATA_RX4P AE15
SATA_TX5P AB16
SATA_TX5N AC16
SATA_RX5N AE16
SATA_RX5P AD16

ATA 66/100/133
IDE_IORDY AA24
IDE_IRQ AA25
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE23
IDE_D3/GPIO18 AC23
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM
SPI_DI/GPIO12 G6
SPI_DO/GPIO11 D2
SPI_CLK/GPIO47 D1
SPI_HOLD#/GPIO31 F4
SPI_CS1#/GPIO32 F3
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

WLAN_ON (53)
WLAN_ON#----> WLAN_ON

FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
PCB_ID0 (21)

FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8

HW MONITOR
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
GPIO61 T2228 TPC28T
TEMPIN_NB T2229 TPC28T
R2218 0Qhm
GPIO63
GPIO64 T2231 TPC28T /X
OS#_OC (30,50)

VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7
GPIO53 T2232 TPC28T
GPIO54
L_ISOLATE# (33)
WLAN_LED_ON (56)

GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！

SATA PWR
PLLVDD_SATA AA11
XTLVDD_SATA W12

SATA_CAL V12
SATA_X1 Y12
SATA_X2 AA12
SATA_ACT#/GPIO67 W11
(31) SATA_LED#

AVDD F6
AVSS G7
AVDD_HWM
+3VSUS

SB700

Place SATA_CAL
RES very close
to ball of SB700

R2201 1KOhm 1% SATA_CAL
R2205 10MOhm
X2201 25Mhz
C2209 27PF/50V N/A
C2210 27PF/50V N/A
GND

+1.2VS
+1.2VS_SATA
R2207 0Ohm
R2250 0Ohm
PLLVDD_SATA
C2211 1UF/10V
C2213 0.1UF/10V
R1.1

080423
C2211 C2212 TO 2.2U(0603)

+3VS
XTLVDD_SATA
C2217 0.1UF/10V
C2216 close
to the ball
of SB700

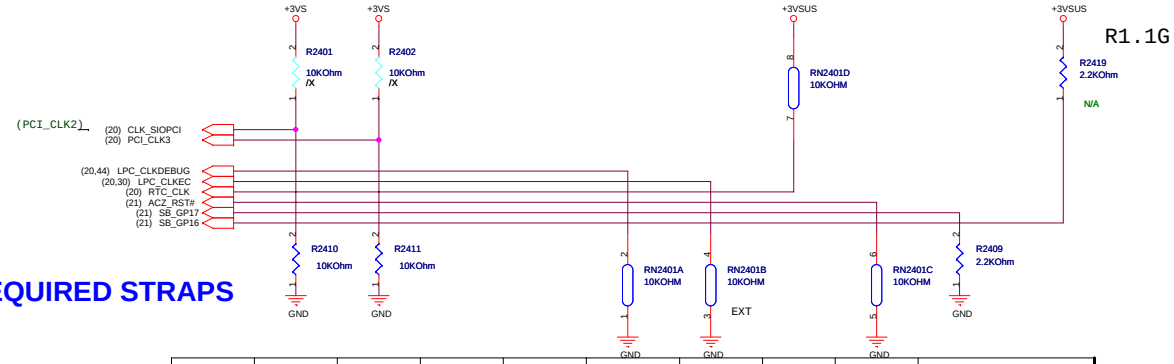
C2214 0.1UF/16V
/X
GND
GND trace at
least 10mil
wide

WLAN_LED_ON
R2202 10KOhm
GND

TEMP_COMM
GND

ASUSTeK.COMPUTER.INC	Title : SB700_PATA/SATA		
	Engineer: <OrgAddr1>		
Size C	Project Name		Rev
Date: Wednesday, April 08, 2009	Sheet 22 of 94		

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	32-kHz clock ENABLED	INTERNAL RTC DEFAULT	Integrated Microcontroller ENABLED	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	32-kHz clock DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	Integrated Microcontroller DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

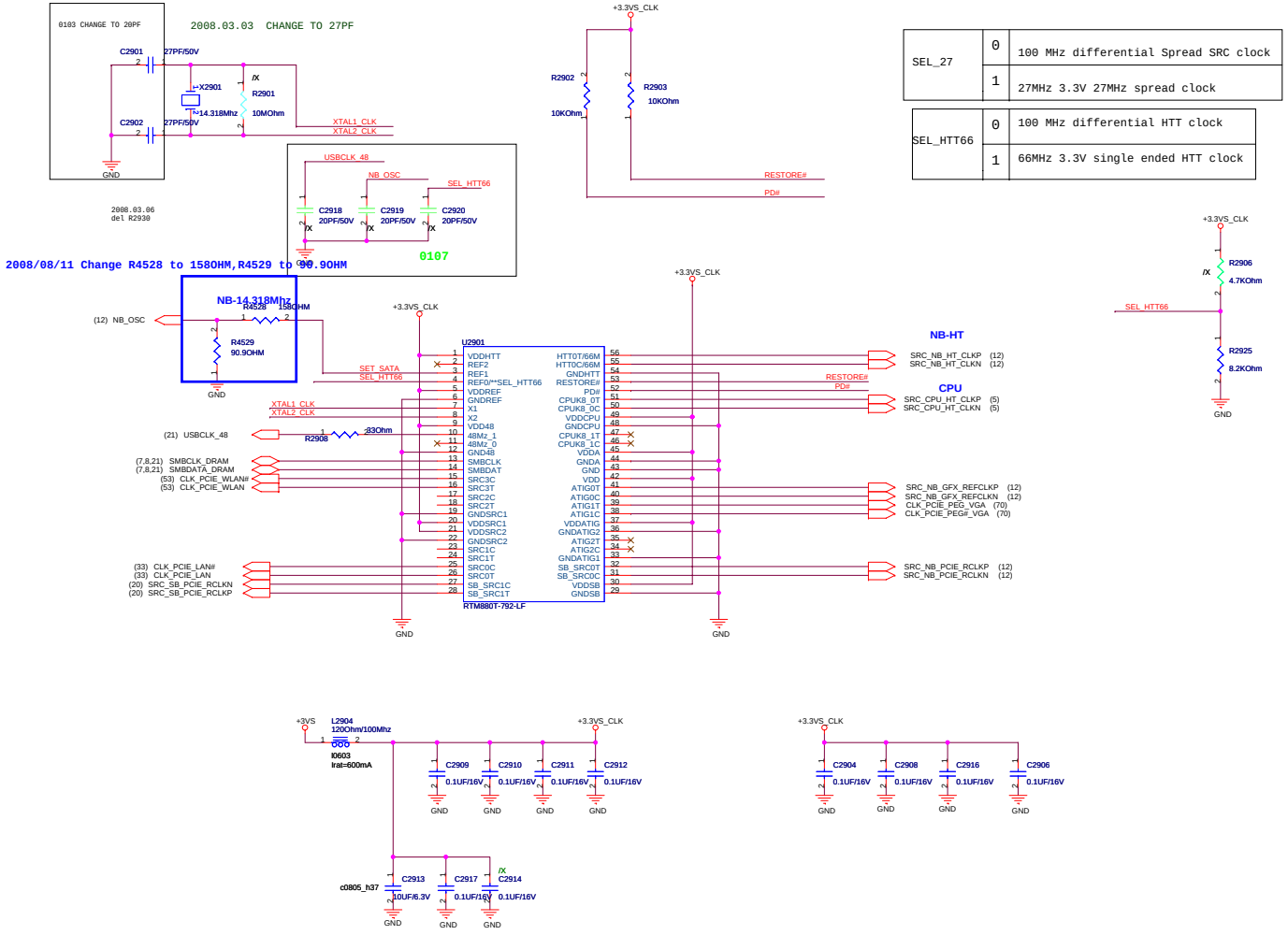
ASUSTeK.Computer.INC

Title : SB700_STRAP

Engineer: <OrgAddr1>

Size: C | Project Name | Rev

Date: Wednesday, April 08, 2009 | Sheet 24 of 94



<Variant Name>

Title : ICS9LPRS489AGLFT

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A2		

Date: Wednesday, April 08, 2009 Sheet 29 of 94

R2.05

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

080131 R1.1
Check EC power

080130
R1.1
Change EC from IT8752 to IT8512

080712

080712 Internet

080712

080712

080712

080712

080712

080712

U3001
IT8512E-L

LPC
FLASH-ROM
KBMX
GPIO
PS/2
SMBus

R2.0 080401
Un-mount C3018 for ITE suggestion

080204 R1.1
IT8512 I~J

U3003
SST25VF080B
(8Mb)

For IT8512 Power

R2.01 080411
Change P/N to
09G013120103

R2.0 080327
Add test point for
factory ICT test

For PU / PD

080215 R1.1
change 4.7K P/N from
10G2124720040 to
10G2124720040

Change pull up resistor
from 10K to 47K ohm

071115

R1.1G

080215 change P/N

Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R2.0 080327
Follow the design IP

11/05

080130

For Instant Key

Note: Close to EC

080713 Add Coloren#

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

071116

Reserve for current leakage
issue (Reference to F5R)

R3008 33Ohm
R3010 33Ohm

071129

R2.02 080519
Un-Mount R3059 and
Q3002 for cost down

071207
AMD review

Q3002
BSS138

080713 ?????

EC Check (AC Auto Boot Issue)

071113
Change Net name
from PM_RSMRST#

080123 R1.1
D3002 1SS355
1KOhm R3052 @

071113
Change Net name
from PM_RSMRST#_EC

PM_RSMRST#

(21) PM_RSMRST#_EC

(21,31) PM_PWROK_EC

071113
Change Net name
from PM_PWROK

R3054 10KOhm

071203

071203
refer page31.

071116
Reserve "Auto power on"
solution for ATI Chipset

PM_PWROK

071113
Change Net name
from PM_PWROK_EC

ASUSTeK COMPUTER INC. NB1

Title : EC_IT8512 (1/2)

Engineer: <OrgAddr1>

Size: Custom | Project Name | Rev

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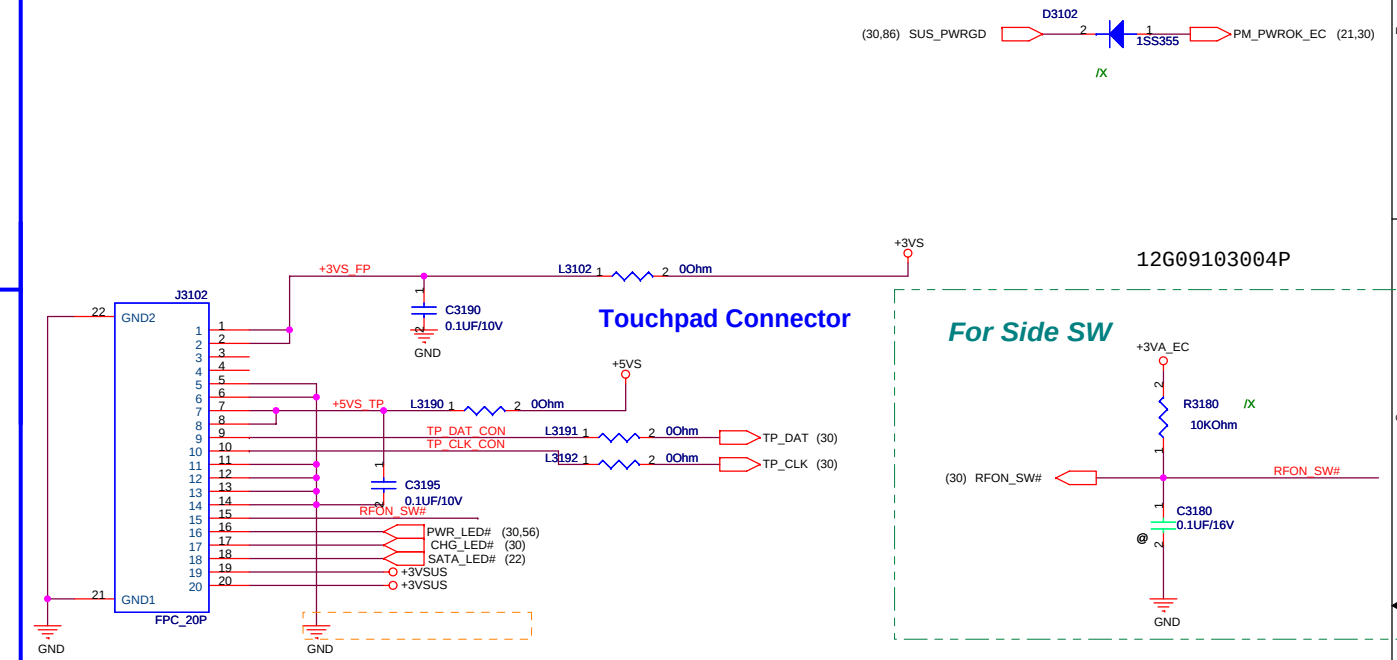


close to connector

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

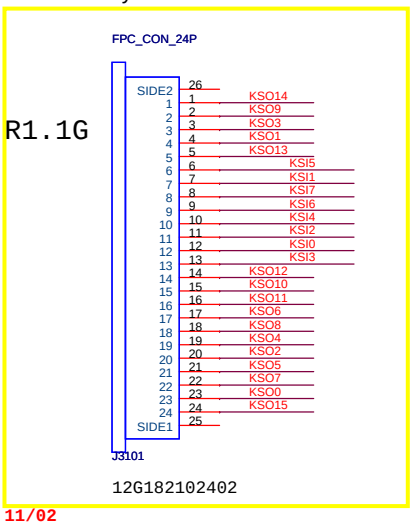
Keyboard Connector

KSO[15:0] (30)

KSI[7:0] (30)

F7/N1 Keyboard

R1.1G



12G182102402

11/02

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512 (2/2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 31 of 94	

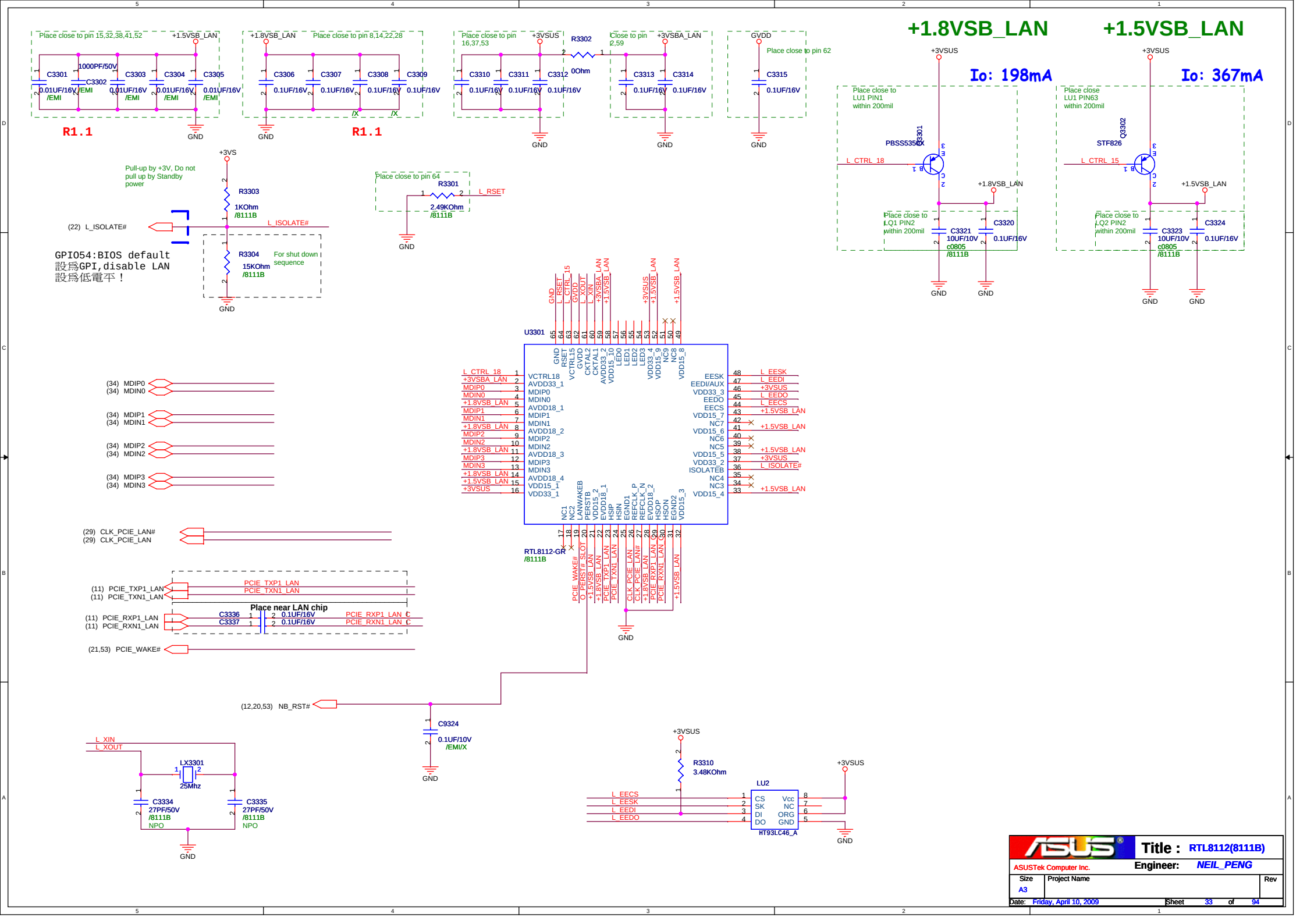
Title : POWER-ON SEQUENCE

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

Date: Wednesday, April 08, 2009 Sheet 32 of 94


+1.8VSB_LAN
+1.5VSB_LAN
Io: 198mA
Io: 367mA
Place close to pin 15,32,38,41,52
Place close to pin 8,14,22,28
Place close to pin 16,37,53
Close to pin 2,59
Place close to pin 62
R1.1
R1.1
R3302
0Ohm
GND
Pull-up by +3V, Do not pull up by Standby power
R3303
1KOhm
/8111B
(22) L_ISOLATE#
L_ISOLATE#
R3304
15KOhm
/8111B
For shut down sequence
GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！
Place close to pin 64
R3301
2.49KOhm
/8111B
L_RSET
Place close to LU1 PIN1 within 200mil
Place close to LU1 PIN63 within 200mil
PBSS5350X
STF826
Q3301
Q3302
L_CTRL_18
L_CTRL_15
Place close to LQ1 PIN2 within 200mil
Place close to LQ2 PIN2 within 200mil
C3321
10UF/10V
c0805
/8111B
C3320
0.1UF/16V
C3323
10UF/10V
c0805
/8111B
C3324
0.1UF/16V
U3301
RTL8112-GR
/8111B
(34) MDIP0
(34) MDIN0
(34) MDIP1
(34) MDIN1
(34) MDIP2
(34) MDIN2
(34) MDIP3
(34) MDIN3
(29) CLK_PCIE_LAN#
(29) CLK_PCIE_LAN
(11) PCIE_TXP1_LAN
(11) PCIE_TXN1_LAN
Place near LAN chip
C3336
C3337
0.1UF/16V
(11) PCIE_RXP1_LAN
(11) PCIE_RXN1_LAN
(21,53) PCIE_WAKE#
(12,20,53) NB_RST#
C9324
0.1UF/10V
/EMI/X
L_XIN
L_XOUT
LX3301
25Mhz
C3334
27PF/50V
/8111B
NPO
C3335
27PF/50V
/8111B
NPO
R3310
3.48KOhm
LU2
HT93LC46_A
L_EECS
L_EESK
L_EEDI
L_EEDO
Title : RTL8112(8111B)
ASUSTek Computer Inc.
Engineer: NEIL_PENG
Size A3
Project Name
Rev
Date: Friday, April 10, 2009
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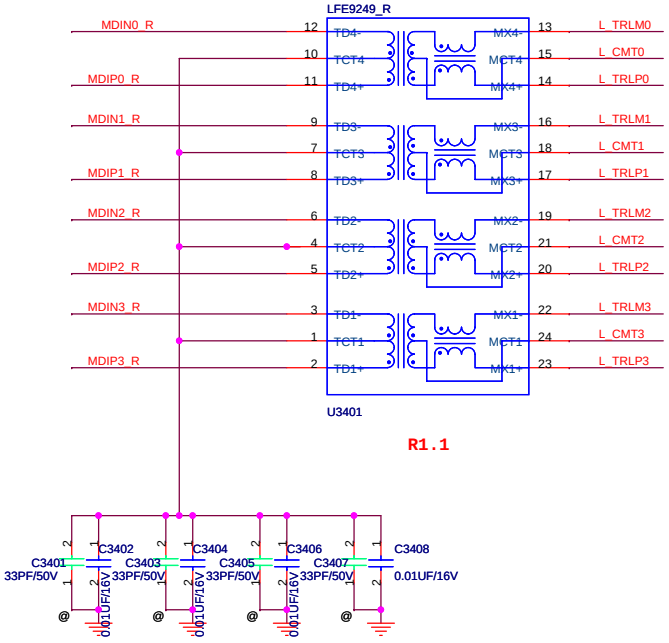
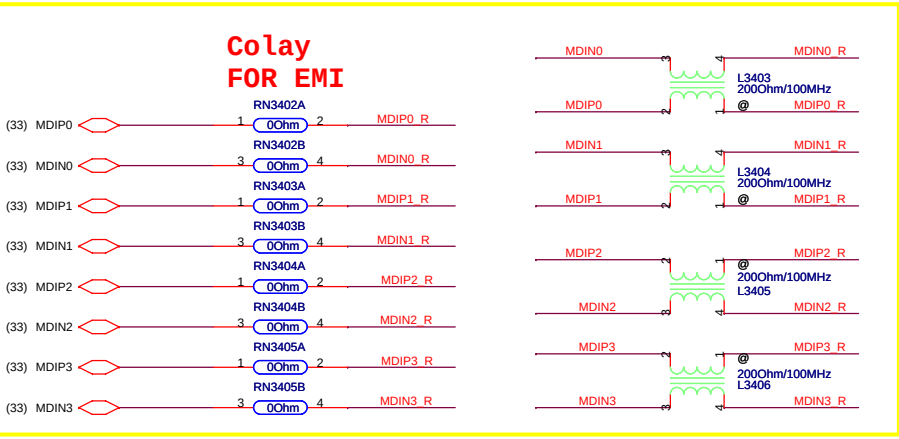
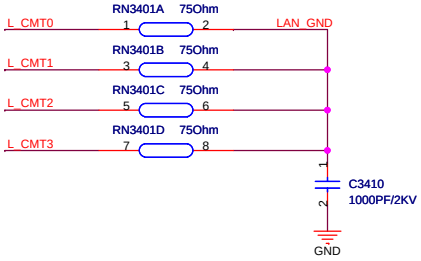
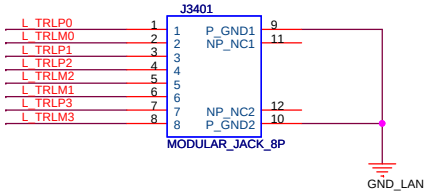
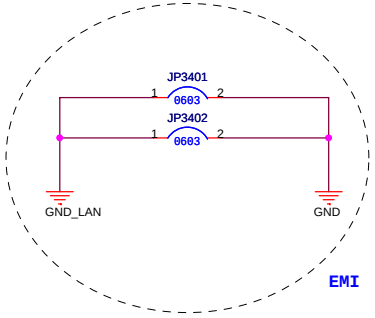


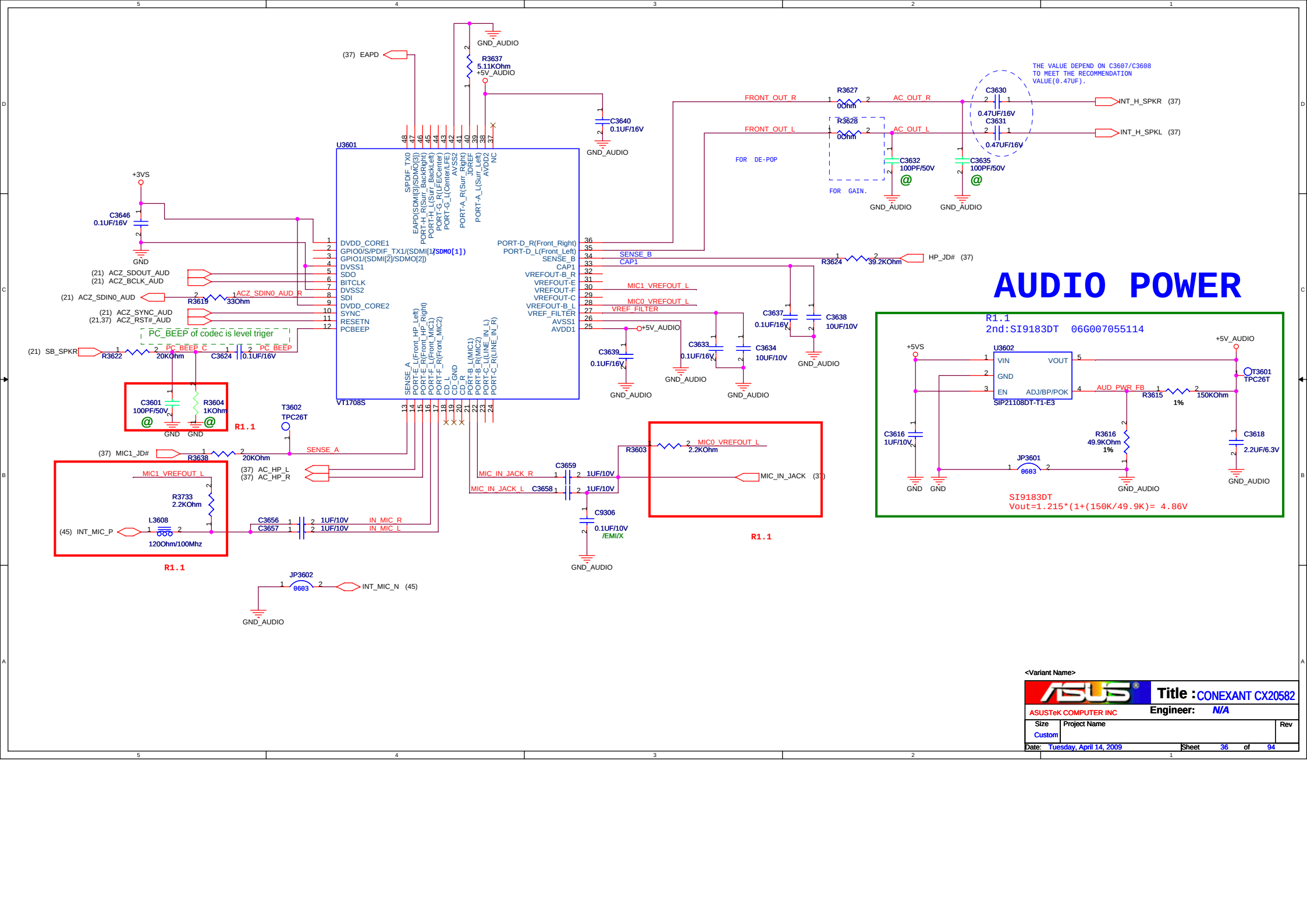




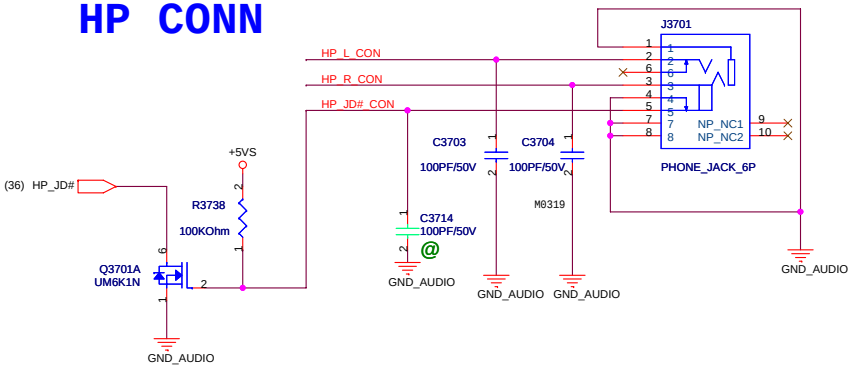




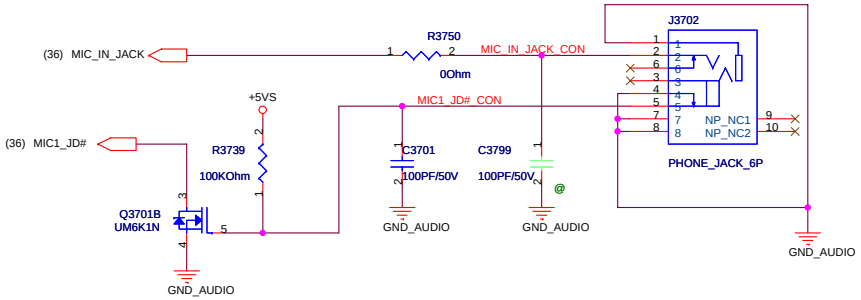
ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 34 of 94	


AUDIO POWER
U3601
VT1708S
DVDD_CORE1
GPIO0/S/PDIF_TX1/(SDMI[1]/SDMO[1])
GPIO1/(SDMI[2]/SDMO[2])
DVSS1
SDO
BITCLK
DVSS2
SDI
DVDD_CORE2
SYNC
RESETN
PCBEEP
SPDIF_TX0
EAPD/(SDMI[3]/SDMO[3])
PORT-H_R(Surr_Back(Right))
PORT-H_L(Surr_Back(Left))
PORT-G_R(LFE/Center)
PORT-G_L(Center/LFE)
AVSS2
PORT-A_R(Surr_Right)
JDREF
PORT-A_L(Surr_Left)
AVDD2
NC
PORT-D_R(Front_Right)
PORT-D_L(Front_Left)
SENSE_B
CAP1
VREFOUT-B_R
VREFOUT-E
VREFOUT-F
VREFOUT-C
VREFOUT-B_L
VREF_FILTER
AVSS1
AVDD1
SENSE_A
PORT-E_L(Front_HP_Left)
PORT-E_R(Front_HP_Right)
PORT-F_R(Front_MIC1)
PORT-F_L(Front_MIC2)
CD_L
CD_GND
CD_R
PORT-B_L(MIC1)
PORT-B_R(MIC2)
PORT-C_L(LINE_IN_L)
PORT-C_R(LINE_IN_R)
(37) EAPD
GND_AUDIO
R3637 5.11KOhm +5V_AUDIO
C3640 0.1UF/16V
+3VS
C3646 0.1UF/16V
GND
(21) ACZ_SDOUT_AUD
(21) ACZ_BCLK_AUD
(21) ACZ_SDIN0_AUD
ACZ_SDIN0_AUD_R
R3619 33Ohm
(21) ACZ_SYNC_AUD
(21,37) ACZ_RST#_AUD
PC_BEEP of codec is level triger
(21) SB_SPKR
R3622 20KOhm
PC_BEEP_C
C3624 0.1UF/16V
PC_BEEP
C3601 100PF/50V @
R3604 1KOhm @
R1.1
T3602 TPC26T
(37) MIC1_JD#
R3638 20KOhm
SENSE_A
(37) AC_HP_L
(37) AC_HP_R
MIC1_VREFOUT_L
R3733 2.2KOhm
L3608
(45) INT_MIC_P
120Ohm/100Mhz
C3656 1UF/10V
C3657 1UF/10V
IN_MIC_R
IN_MIC_L
JP3602 0603
INT_MIC_N (45)
FRONT_OUT_R
FRONT_OUT_L
R3627 0Ohm
R3628 0Ohm
AC_OUT_R
AC_OUT_L
FOR DE-POP
FOR GAIN.
C3632 100PF/50V @
C3635 100PF/50V @
C3630 0.47UF/16V
C3631 0.47UF/16V
THE VALUE DEPEND ON C3607/C3608
TO MEET THE RECOMMENDATION
VALUE(0.47UF).
INT_H_SPKR (37)
INT_H_SPKL (37)
SENSE_B
CAP1
R3624 39.2KOhm
HP_JD# (37)
MIC1_VREFOUT_L
MIC0_VREFOUT_L
VREF_FILTER
+5V_AUDIO
C3639 0.1UF/16V
C3633 0.1UF/16V
C3634 10UF/10V
C3637 0.1UF/16V
C3638 10UF/10V
R3603 2.2KOhm
MIC0_VREFOUT_L
MIC_IN_JACK_R
MIC_IN_JACK_L
C3658
C3659 1UF/10V
1UF/10V
MIC_IN_JACK (37)
C9306 0.1UF/10V /EMI/X
R1.1
R1.1 2nd:SI9183DT 06G007055114
U3602
VIN
VOUT
GND
EN
ADJ/BP/POK
SIP21108DT-T1-E3
+5VS
+5V_AUDIO
AUD_PWR_FB
R3615 150KOhm 1%
T3601 TPC26T
C3616 1UF/10V
R3616 49.9KOhm 1%
JP3601 0603
C3618 2.2UF/6.3V
SI9183DT
Vout=1.215*(1+(150K/49.9K)= 4.86V
<Variant Name>
Title : CONEXANT CX20582
ASUSTeK COMPUTER INC
Engineer: N/A
Size Custom
Project Name
Rev
Date: Tuesday, April 14, 2009
Sheet 36 of 94

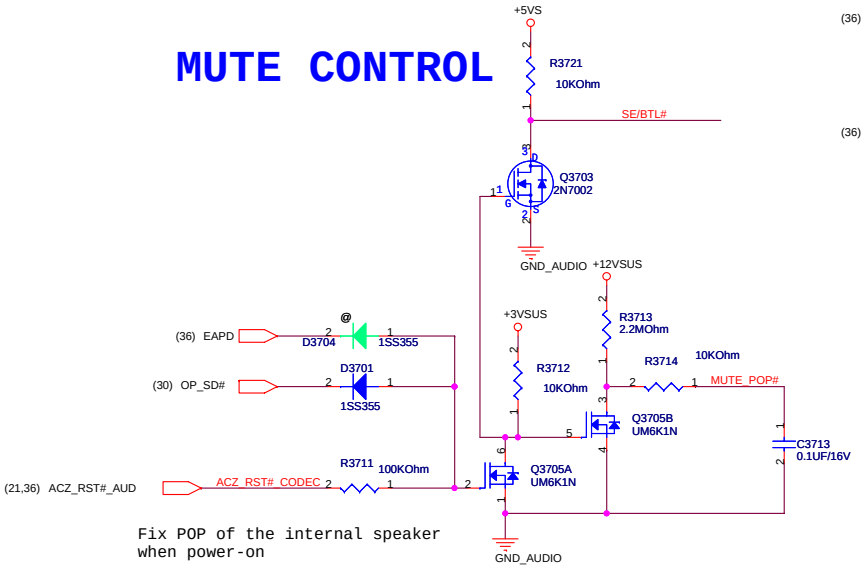
HP CONN



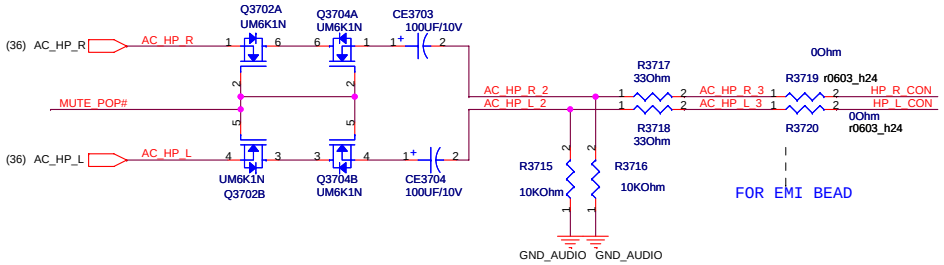
External MIC CONN



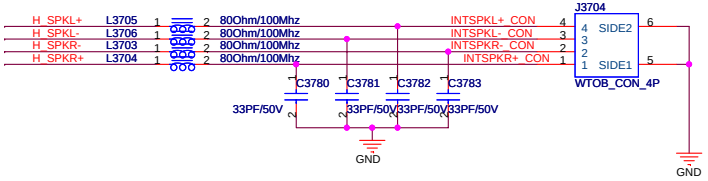
MUTE CONTROL



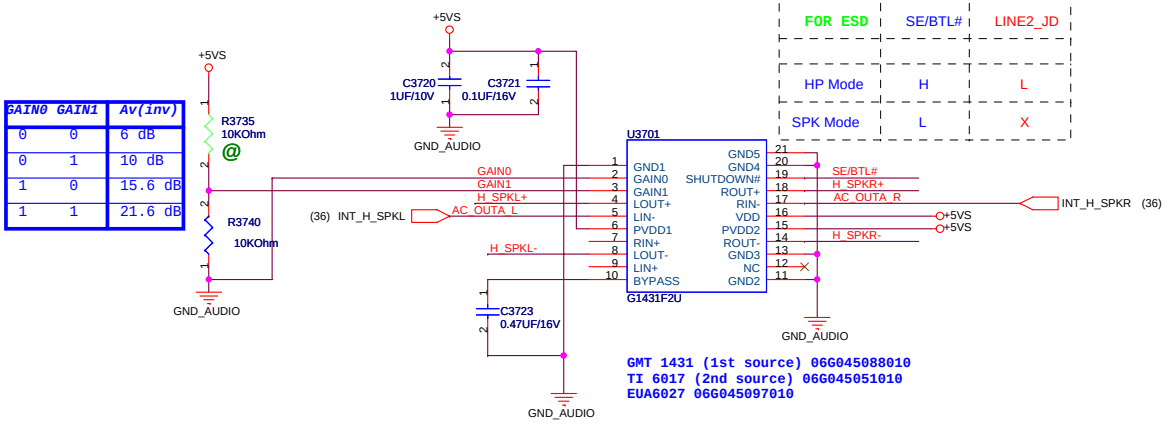
Fix POP of the internal speaker
when power-on



SPEAKER CONNECTOR(2W)

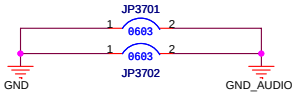


SPEAKER AMP



GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

FOR ESD	SE/BTL#	LINE2_JD
HP Mode	H	L
SPK Mode	L	X



GMT 1431 (1st source) 06G045088010
TI 6017 (2nd source) 06G045051010
EUA6027 06G045097010

ASUSTeK COMPUTER INC. NB1

Title : AUDIO HP/MIC

Engineer: N/A

Size	Project Name	Rev
Custom		

Date: Wednesday, April 08, 2009 Sheet 37 of 94

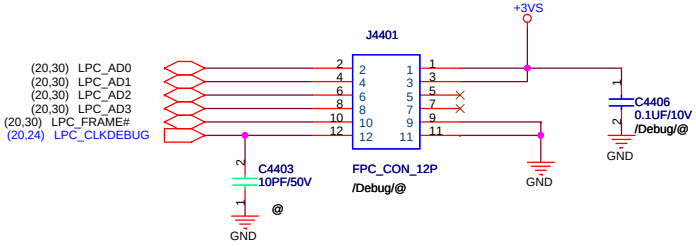
Title : MIC&LINEIN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

Date: Wednesday, April 08, 2009 Sheet 38 of 94



If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

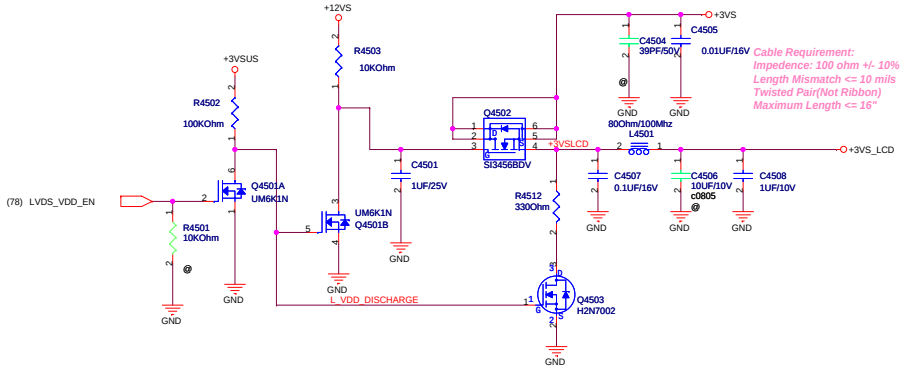
For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 44 of 94	

LCD Backlight Control

LCD Power



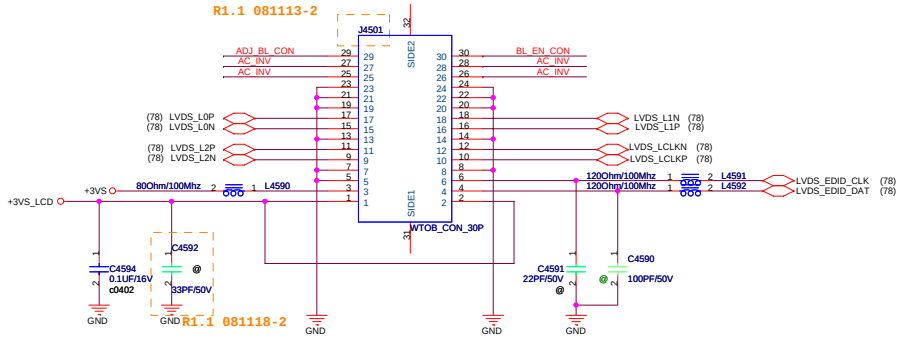
LVDS_LCLKN
LVDS_LCLKP
C4502
10PF/50V
N/A

11/19

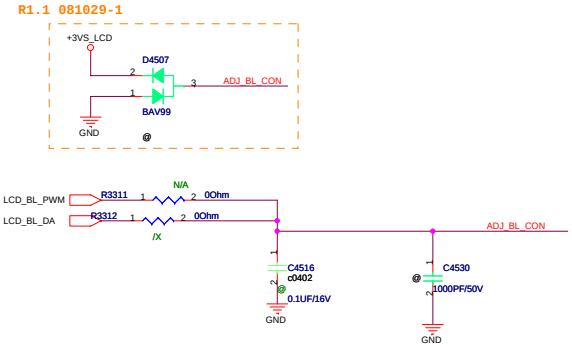
11/19

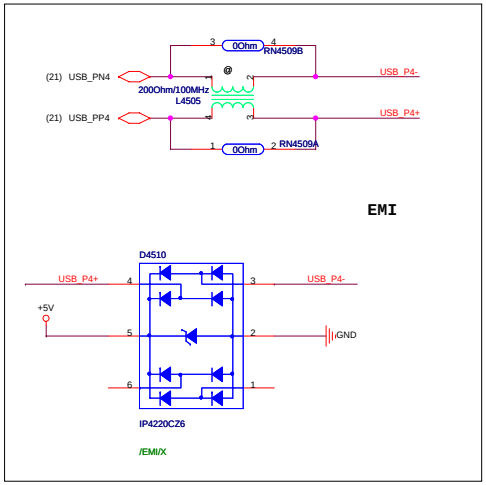
check

LED PANEL LVDS Interface

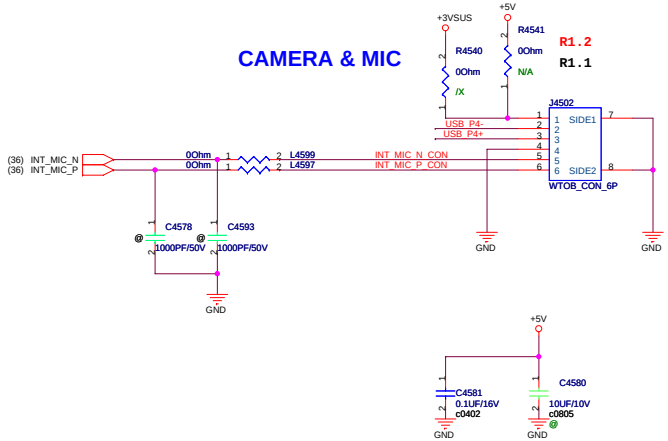


INVERTER
Interface/Speaker CONN.

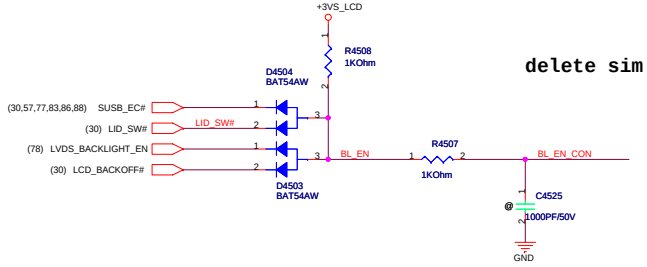




CAMERA & MIC

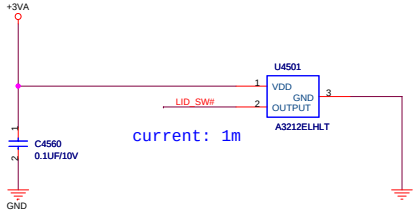


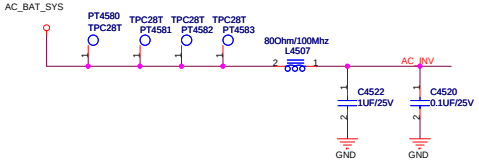
delete sim card function 20080804



Hall effect switch

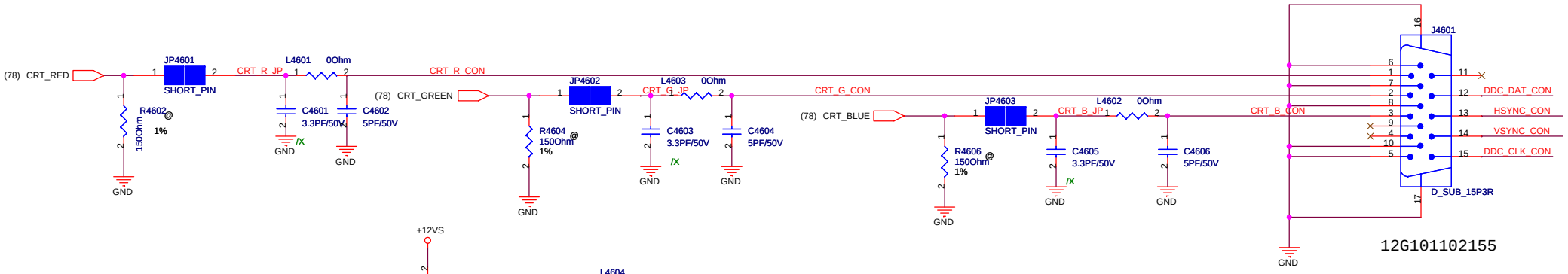
current: 2m



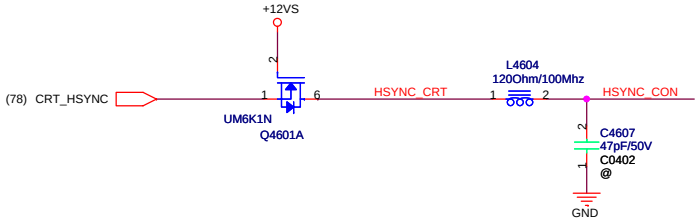


ASUSTeK COMPUTER INC. NB1		Title: LVDS & Inverter CON	
		Engineer: <OrgAddr1>	
Size: C	Project Name		Rev
Date: Thursday, April 09, 2009		Sheet 45 of 94	

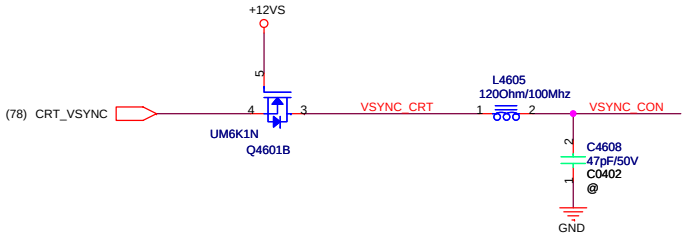
R1.1　VGA部分調整：L4601、L4602、L4603調成0 ohm，C4601、C4603、C4605改爲"/X", C4602、C4604、C4606改成5PF.

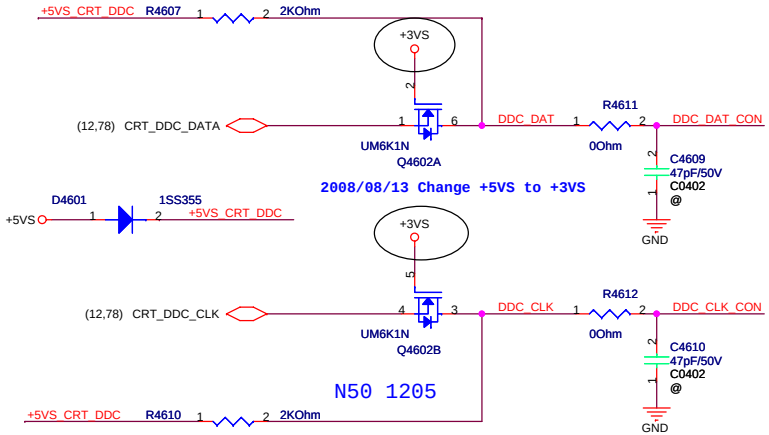


12G101102155

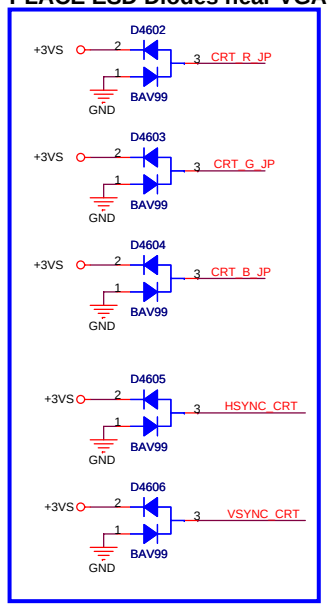


2008/0807 Remove U4601/U4602



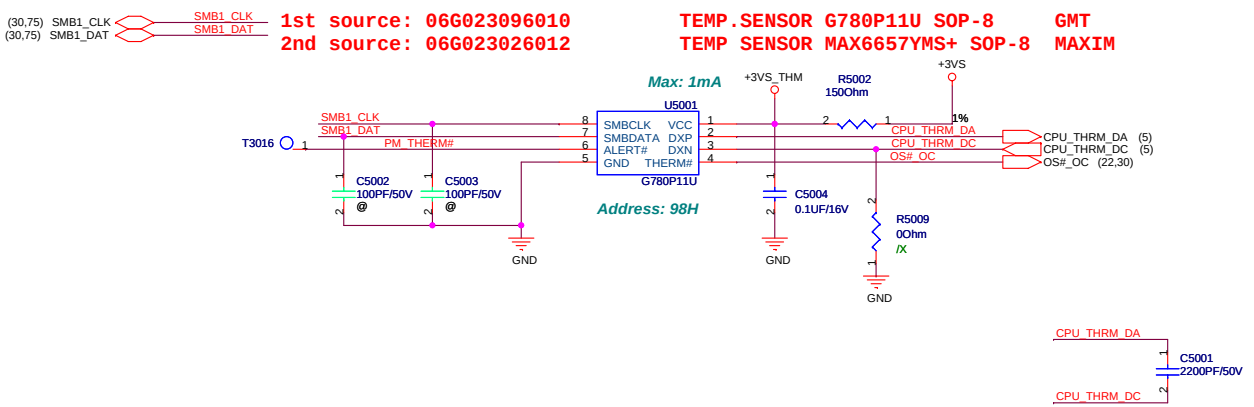


PLACE ESD Diodes near VGA port

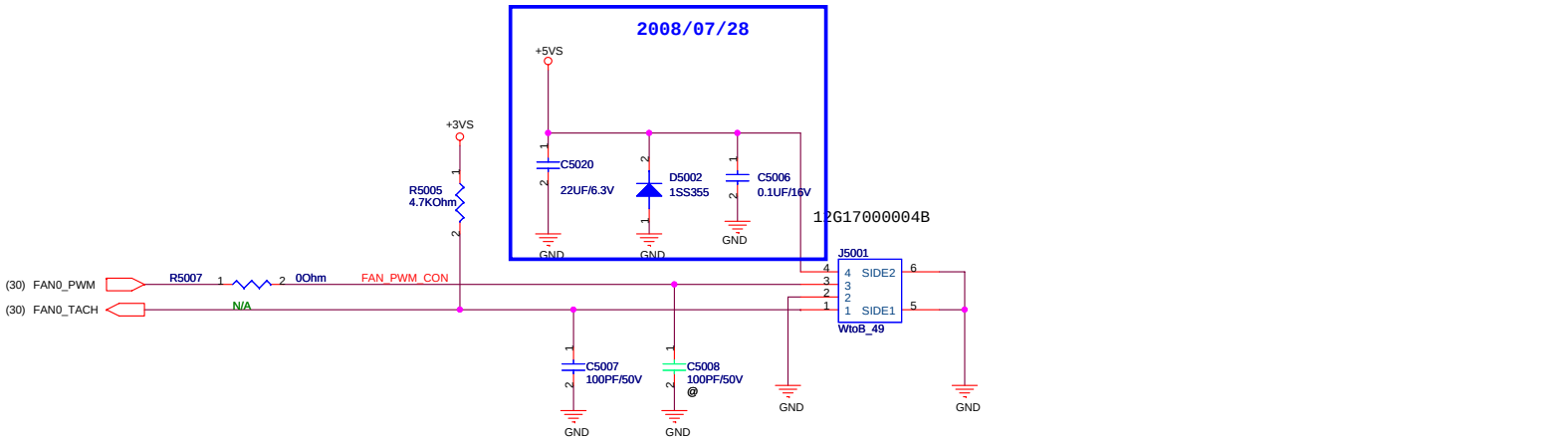


ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 46 of 94	

Thermal Sensor

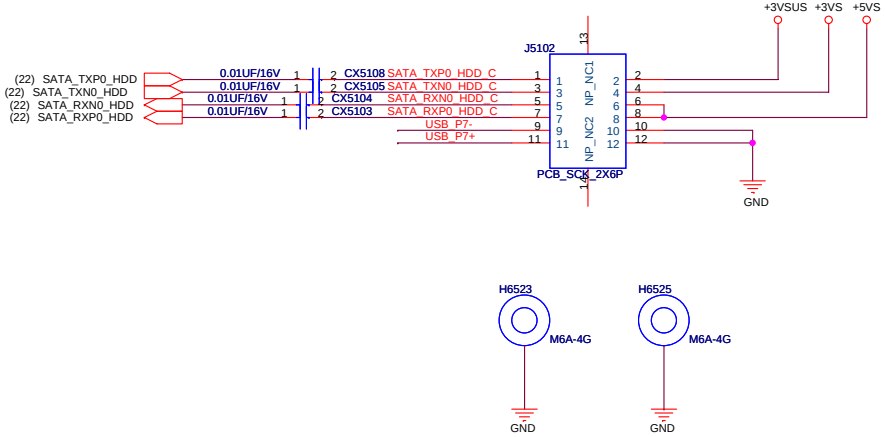


DC FAN Control

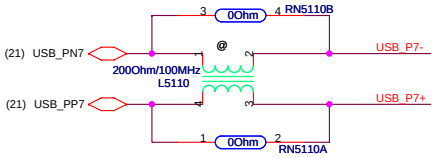


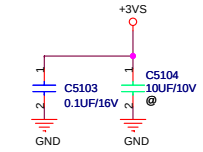
ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 50 of 94	

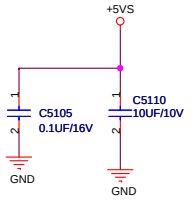
SATA HDD



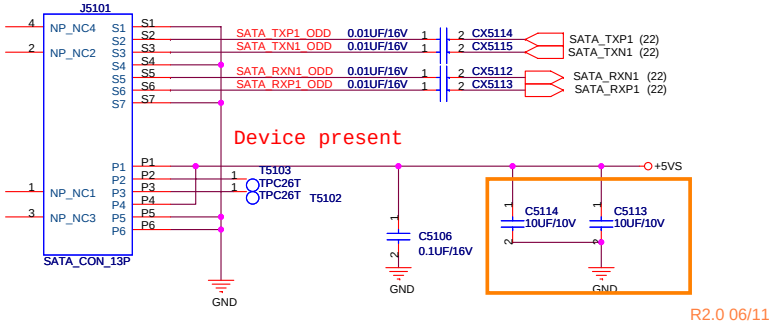
USB Cardreader







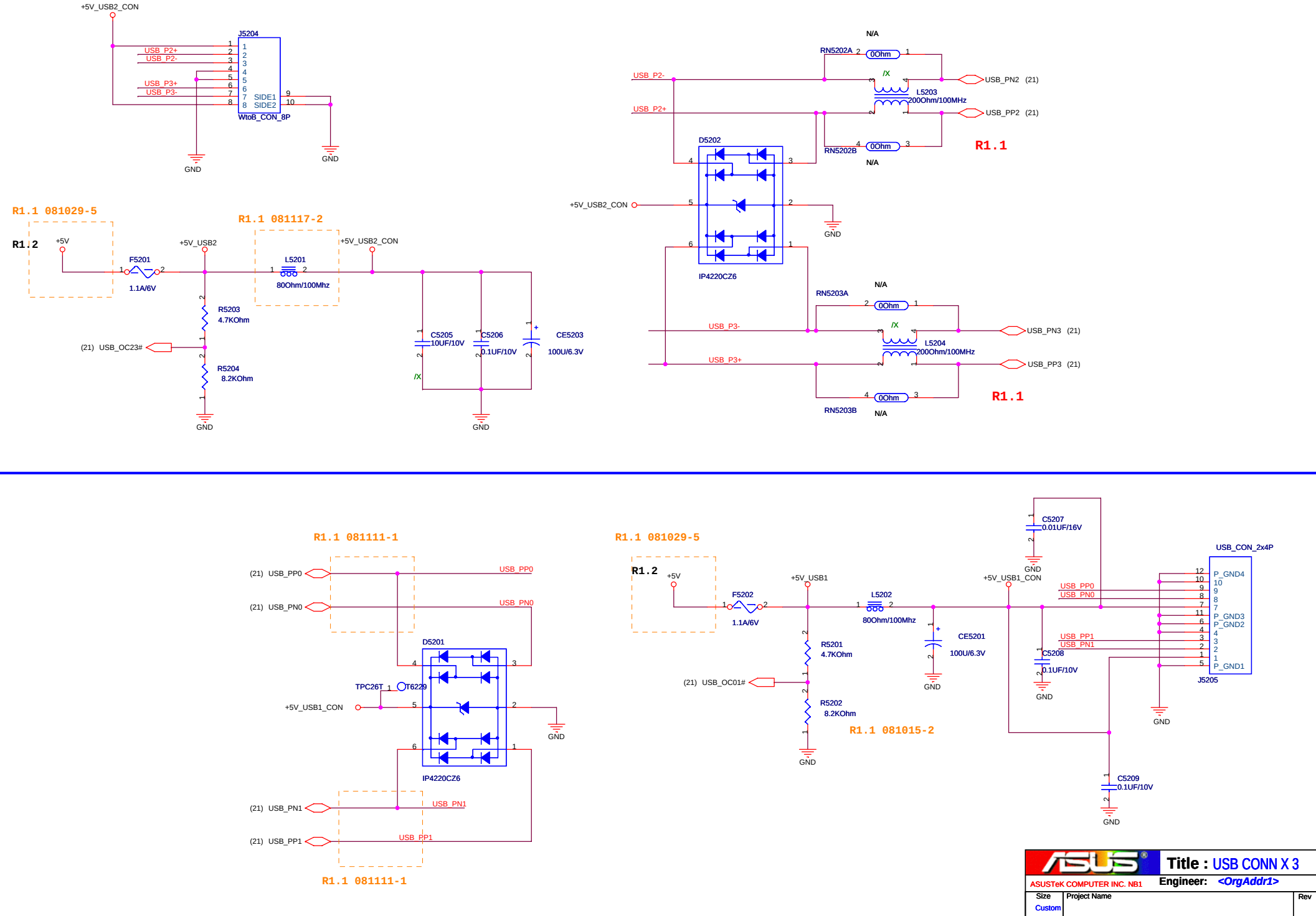
ODD



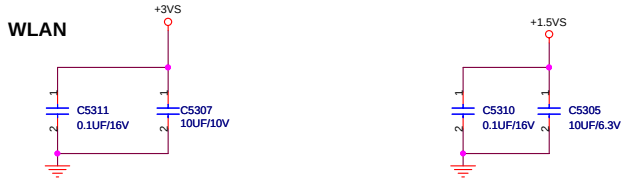
R2.0 06/11

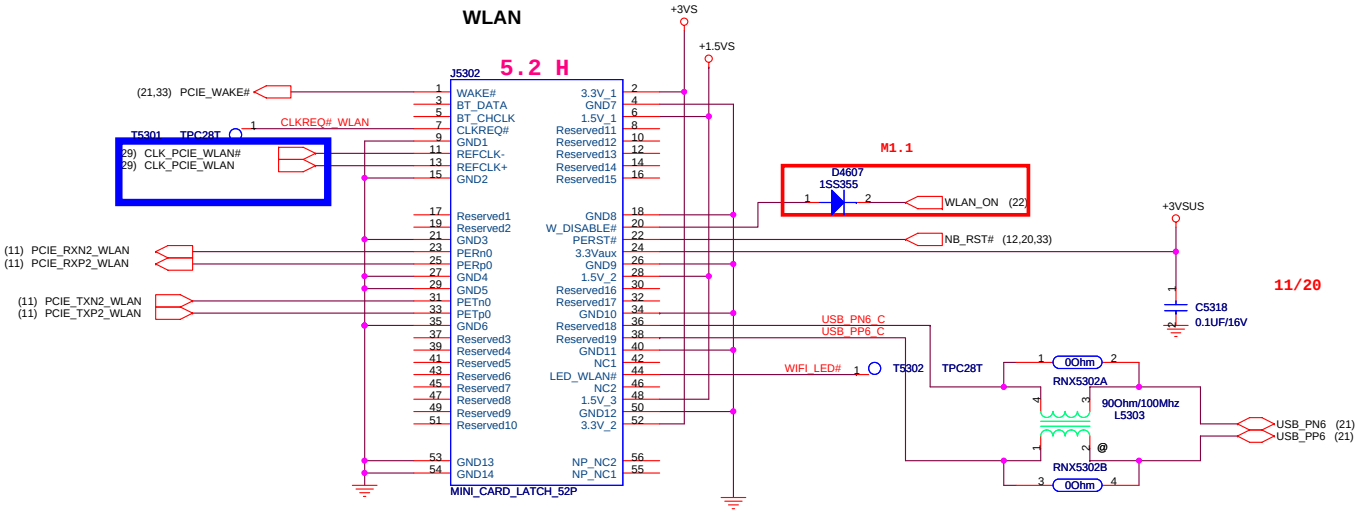
ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 51 of 94	

USB IO Board



ASUSTeK COMPUTER INC. NB1	Title : USB CONN X 3	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 52 of 94	

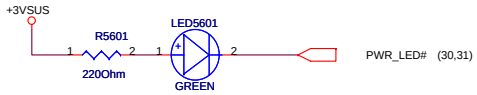




ASUSTeK COMPUTER INC. NB1	Title : Minicard card & Nut	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 53 of 94	

For Power LED

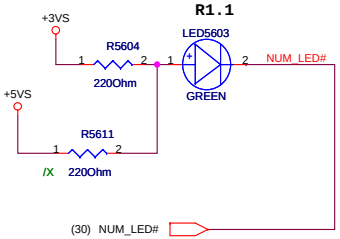
3/13 Orange



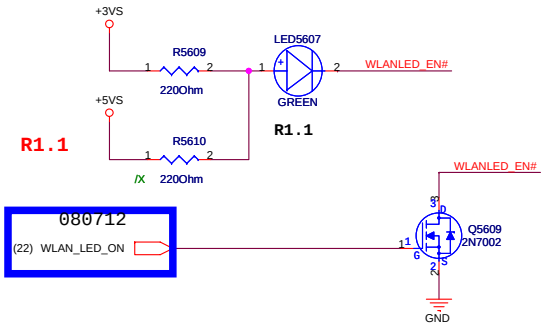
R1.1

For Number Lock

R1.1



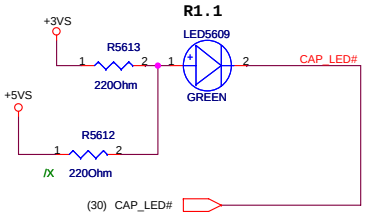
For WireLess LED



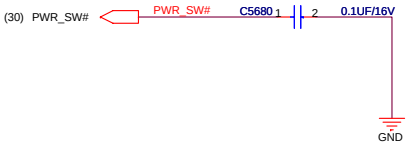
2008/07/30 Remove 3G Function

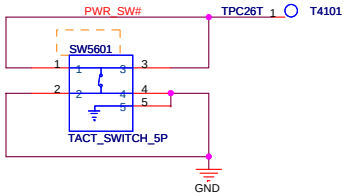
For Caps. Lock

R1.1



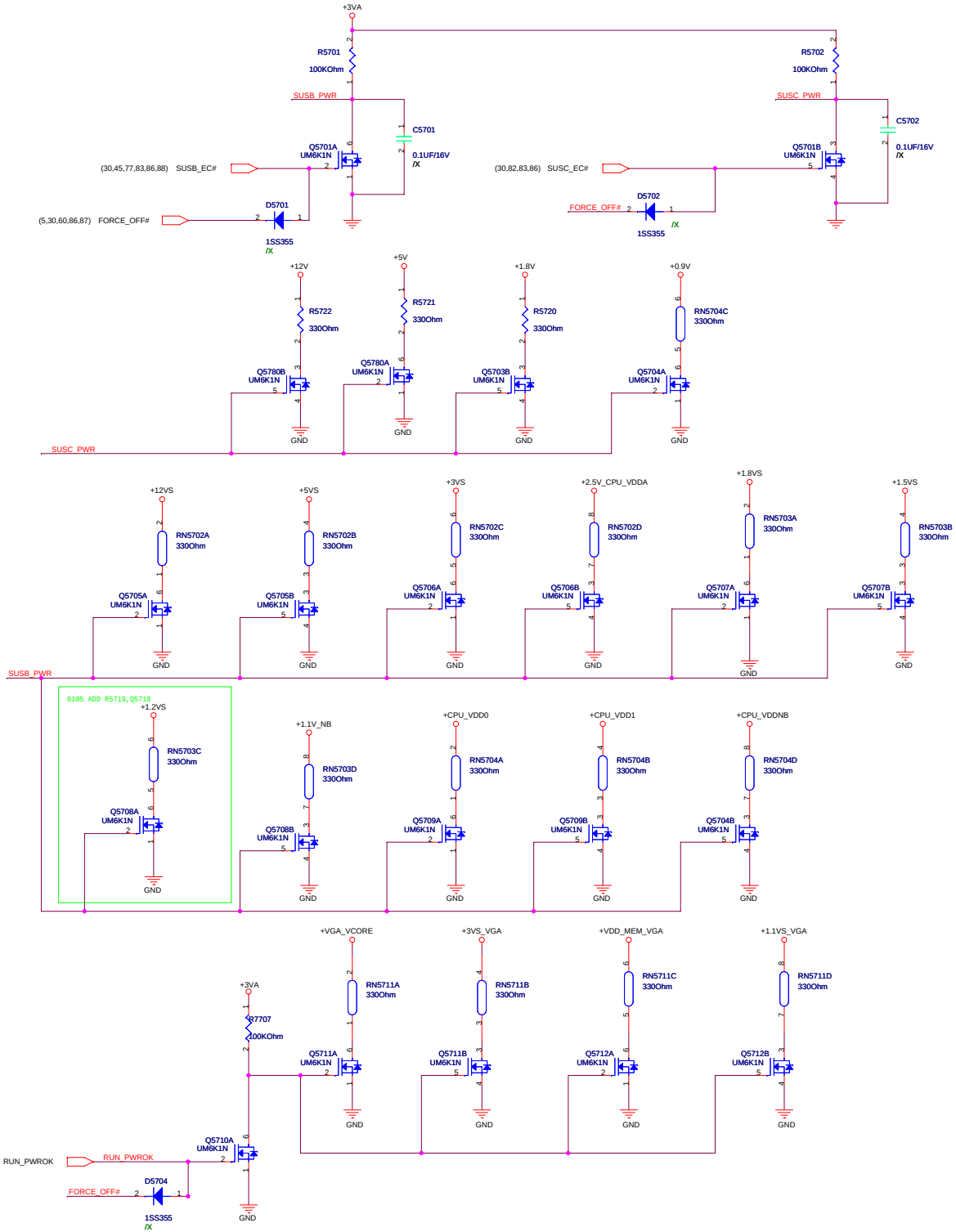
SW





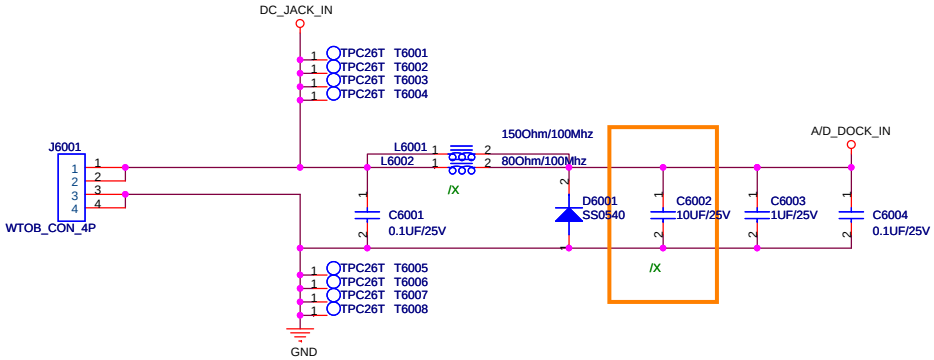
SHUT_DOWN#

ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 56 of 94	

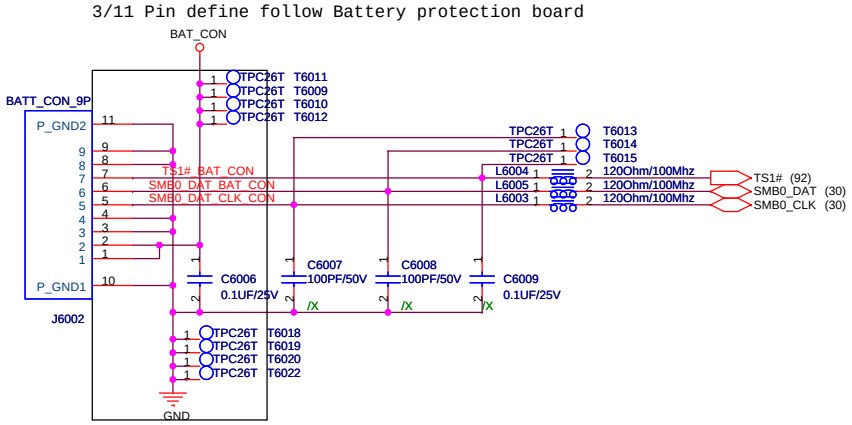


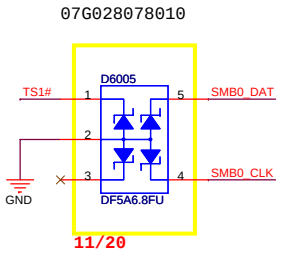
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 57 of 94	

DC IN

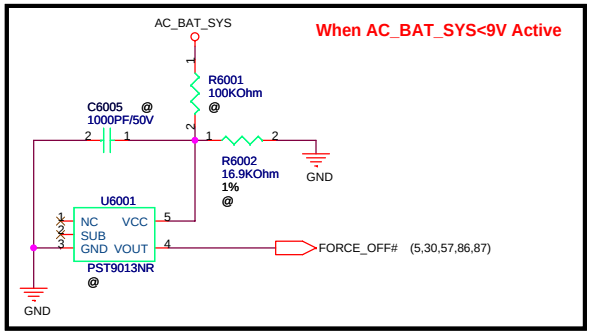


BAT IN





Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 60 of 94	

Hole-A

H6501
HOLE_NPTH

Hole-B

H6502
HOLE_NPTH

H6503
HOLE_NPTH

H6504
HOLE_NPTH

Hole-C

H6505
O83X71DO83X71N

Spring

S6501
EMI_SPRING_PAD
/X
GND

R1.2

Hole-D

H6509
CT276CB197ID138

H6510
CT276CB197ID138

H6511
CT276CB197ID138

H6512
CT276CB197ID138

GND

Hole-E

H6514
CT256B315D91N

H6506
CT256B315D91N

H6507
CT256RB276X287D91N

H6508
CT256B220D91N

GND

R1.1

H6516
CT256B315D91N

GND_AUDIO

Hole-F

H6517
CT256B220D91N

H6520
CT256B220D91N

GND

H6518
CRT266X256D91N

GND

H6519
RT335X305D91N

GND

H6521
CT256B220D91N

H6522
CT256B220D91N

H6513
CT256B220D91N

H6515
CT256B220D91N

GND

ASUSTeK COMPUTER INC. NB1	Title MDC NUT & Hinksink NUT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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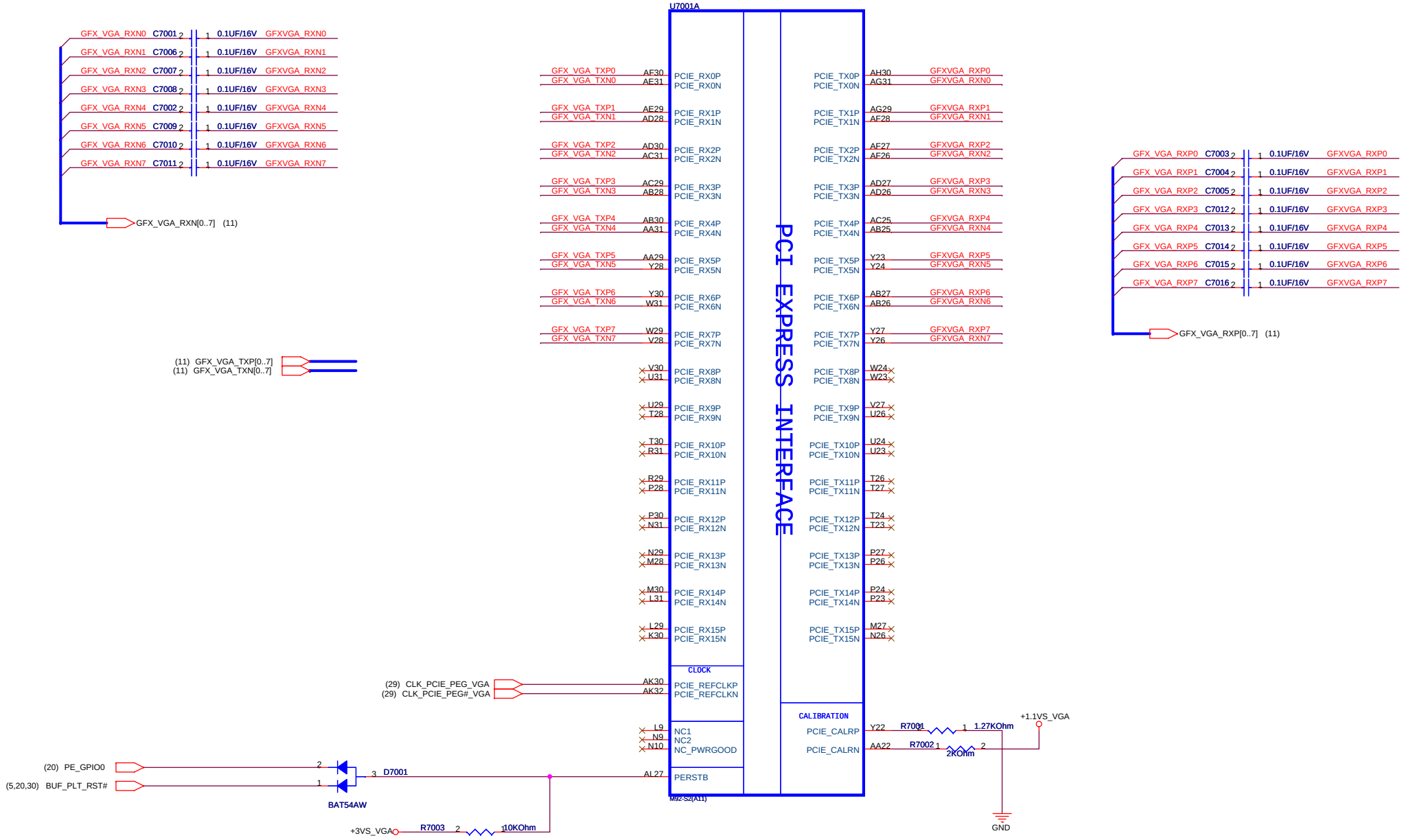

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

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PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O	
L	L	1.2V	1.182V
H	L	1.10V	1.082V
L	H	1.0V	0.997V
H	H	0.9V	0.925

U7001B

MUTI GFX

DPA: TXCAP_DPA3P AE2, TXCAM_DPA3N AF4, TX0P_DPA2P AG3, TX0M_DPA2N AG5, TX1P_DPA1P AH3, TX1M_DPA1N AH1

DPB: TX2P_DPA0P AK3, TX2M_DPA0N AK1, TXCBP_DPB3P AK5, TXCBM_DPB3N AM3, TX3P_DPB2P AK6, TX3M_DPB2N AM5, TX4P_DPB1P AJ7, TX4M_DPB1N AH6, TX5P_DPB0P AK8, TX5M_DPB0N AL7

DVPCNTL_MVP_0 AA1, DVPCNTL_MVP_1 Y4, DVPCNTL_0 AC7, DVPCNTL_1 Y2, DVPCNTL_2 U5, DVPCLK U1, DVPDATA_0 Y7, DVPDATA_1 V2, DVPDATA_2 Y8, DVPDATA_3 V4, DVPDATA_4 AE7, DVPDATA_5 W1, DVPDATA_6 AB8, DVPDATA_7 W3, DVPDATA_8 AB9, DVPDATA_9 W5, DVPDATA_10 AC6, DVPDATA_11 W6, DVPDATA_12 AD7, DVPDATA_13 AA3, DVPDATA_14 AC8, DVPDATA_15 AA5, DVPDATA_16 AE8, DVPDATA_17 AA6, DVPDATA_18 AE9, DVPDATA_19 AB4, DVPDATA_20 AD9, DVPDATA_21 AB2, DVPDATA_22 AC10, DVPDATA_23 AC5

T7112 PANEL_ID0, T7107 PANEL_ID1

(76) MEMTYPE_0, (76) MEMTYPE_1, (76) MEMTYPE_2, (76) MEMTYPE_3

I2C: SCL R1, SDA R3

+3VS_VGA — R7117 4.7KOhm — R7120 4.7KOhm

(78) EDID_CLK_VGA, (78) EDID_DAT_VGA

GENERAL PURPOSE I/O

(76) ATI_GPIO0 — ATI_GPIO0 U6
(76) ATI_GPIO1 — ATI_GPIO1 U10
(76) ATI_GPIO2 — ATI_GPIO2 T10
T7122 — ATI_GPIO3 U8
T7123 — ATI_GPIO4 U7
(76) ATI_GPIO5 — ATI_GPIO5 T9
T7125 — ATI_GPIO6 T8
(73) BLON_VGA — GPIO_7_BLON T7
(76) SPI_SO — SPI_SO P10
(76) SPI_SI — SPI_SI P4
(76) ATI_GPIO[13:11] — SPI_SCK P2
T7127
ATI_GPIO11 N6
ATI_GPIO12 N5
ATI_GPIO13 N3
T7121 — HDTV_EN# Y9
(91) PWRCNTL_0 — PWRCNTL_0 N1
(76) ATI_GPIO16 — ATI_GPIO16 M4
(75) M92_THRM# — R7122 0Ohm — ATI_GPIO17 R6
T7120 — ATI_GPIO18 W10
M2
(75) CTF — PWRCNTL_1 P8
(91) PWRCNTL_1 — ATI_GPIO21 P7
GND — R7131 /X — 10KOhm — GPIO_23_CLKREQB N8
T7119 — N7
T11
R11
T7124 — GPIO_TRSTB L6
L5
L3
L1
K4
GND — 1KOhm VR2 — AF24
T7117 — AB13
W8
W9
T7118 — W7
AD10
AC14

GPIO_0 U6, GPIO_1 U10, GPIO_2 T10, GPIO_3_SMBDATA U8, GPIO_4_SMBCLK U7, GPIO_5_AC_BATT T9, GPIO_6 T8, GPIO_7_BLON T7, GPIO_8_ROMSO P10, GPIO_9_ROMSI P4, GPIO_10_ROMSCK P2, GPIO_11 N6, GPIO_12 N5, GPIO_13 N3, GPIO_14_HPD2 Y9, GPIO_15_PWRCNTL_0 N1, GPIO_16_SSIN M4, GPIO_17_THERMAL_INT R6, GPIO_18_HPD3 W10, GPIO_19_CTF M2, GPIO_20_PWRCNTL_1 P8, GPIO_21_BB_EN P7, GPIO_22_ROMCSB N8, GPIO_23_CLKREQB N7, GPIO_29_DRM_0 T11, GPIO_30_DRM_1 R11

JTAG_TRSTB L6, JTAG_TDI L5, JTAG_TCK L3, JTAG_TMS L1, JTAG_TDO K4, TESTEN AF24

GENERICA AB13, GENERICB W8, GENERICC W9, GENERICD W7, GENERICE_HPD4 AD10, HPD1 AC14

+VREFG — VREFG AC16

PLL/CLOCK

DPLL_PVDD AF14, DPLL_PVSS AE14 — +DPLL_PVDD — 3%; 120mA
DPLL_VDDC AD14 — +DPLL_VDDC — 300mA
XTALIN AM28, XTALOUT AK28 — R7127 1MOhm — X7101 27Mhz — C7123 18PF/50V — C7124 18PF/50V

THERMAL

DPLUS T4, DMINUS T2 — (75) VGA_THERMDA, (75) VGA_THERMDC

TS_FDO R5, TSVDD AD17, TSVSS AC17 — +TSVDD — 20mA

DAC1

R AM26 PEG_CRT_RED_VGA, RB AK26 — R7107 150Ohm 1% — R7118 150Ohm 1% — R7119 150Ohm 1% — RED_VGA (78)
G AL25 PEG_CRT_GREEN_VGA, GB AJ25 — GREEN_VGA (78)
B AH24 PEG_CRT_BLUE_VGA, BB AG25 — BLUE_VGA (78)
HSYNC AH26 HSYNC_VGA_R — R7129 0Ohm — HSYNC_VGA (76,78)
VSYNC AJ27 VSYNC_VGA_R — R7130 0Ohm — VSYNC_VGA (76,78)
RSET AD22 M92_RSET — R7121 499Ohm — GND
AVDD AG24 (85mA) +AVDD — 70mA
AVSSQ AE22 GND
VDD1DI AE23 (66mA) +VDD1DI — 45mA
VSS1DI AD23 GND

DAC2

R2 AM12, R2B AK12
G2 AL13, G2B AJ11
B2 AK10, B2B AL9
C AH12, Y AM10, COMP AJ9
H2SYNC AL13, V2SYNC AJ13 — T7126
VDD2DI AD19, VSS2DI AC19 — +VDD1DI — 45mA
A2VDD AE20 (135mA) +A2VDD — 65mA
A2VDDQ AE17 (2.4mA) +A2VDDQ — 1mA
A2VSSQ AE19 GND
R2SET AG13 — R7128 715Ohm — GND

DDC/AUX

DDC1CLK AE6, DDC1DATA AE5 — DDC_CLK_VGA (78), DDC_DATA_VGA (78)
AUX1P AD2, AUX1N AD4
DDC2CLK AC11, DDC2DATA AC13
AUX2P AD13, AUX2N AD11
RSVD2 AB22, RSVD3 AC22
DDCCLK_AUX5P AE16, DDCDATA_AUX5N AD16
DDC6CLK AC1, DDC6DATA AC3
NC_DDCCLK_AUX7P AD20, NC_DDCDATA_AUX7N AC20

HDMI

M92-S2(A11)

+1.8VS_VGA — R7123 499Ohm — R7126 249Ohm — C7112 0.1UF/25V — +VREFG

ATI_GPIO5 — Q7105 2N7002K_T1_E3 — (92) AC_OK

L7101 0Ohm: +1.8VS_VGA — +DPLL_PVDD — C7115 4.7uF/6.3V — C7138 0.1UF/16V

L7105 0Ohm: +1.1VS_VGA — +DPLL_VDDC +DPLL_VDDC — C7119 4.7uF/6.3V — C7140 0.1UF/16V

L7107 0Ohm: +1.8VS_VGA — +TSVDD — C7121 1UF/6.3V N/A — C7142 0.1UF/16V

L7102 0Ohm: +AVDD — C7110 4.7uF/6.3V — C7129 0.1UF/16V — +1.8VS_VGA

L7103 0Ohm: +VDD1DI — C7114 1UF/6.3V — C7131 0.1UF/16V — +1.8VS_VGA

L7106 0Ohm: +A2VDD — C7122 1UF/6.3V — C7133 0.1UF/16V N/A — +3VS_VGA

L7108 0Ohm: +A2VDDQ — C7128 1UF/6.3V — C7135 0.1UF/16V — +1.8VS_VGA

<Variant Name>

ASUSTeK COMPUTER INC.

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

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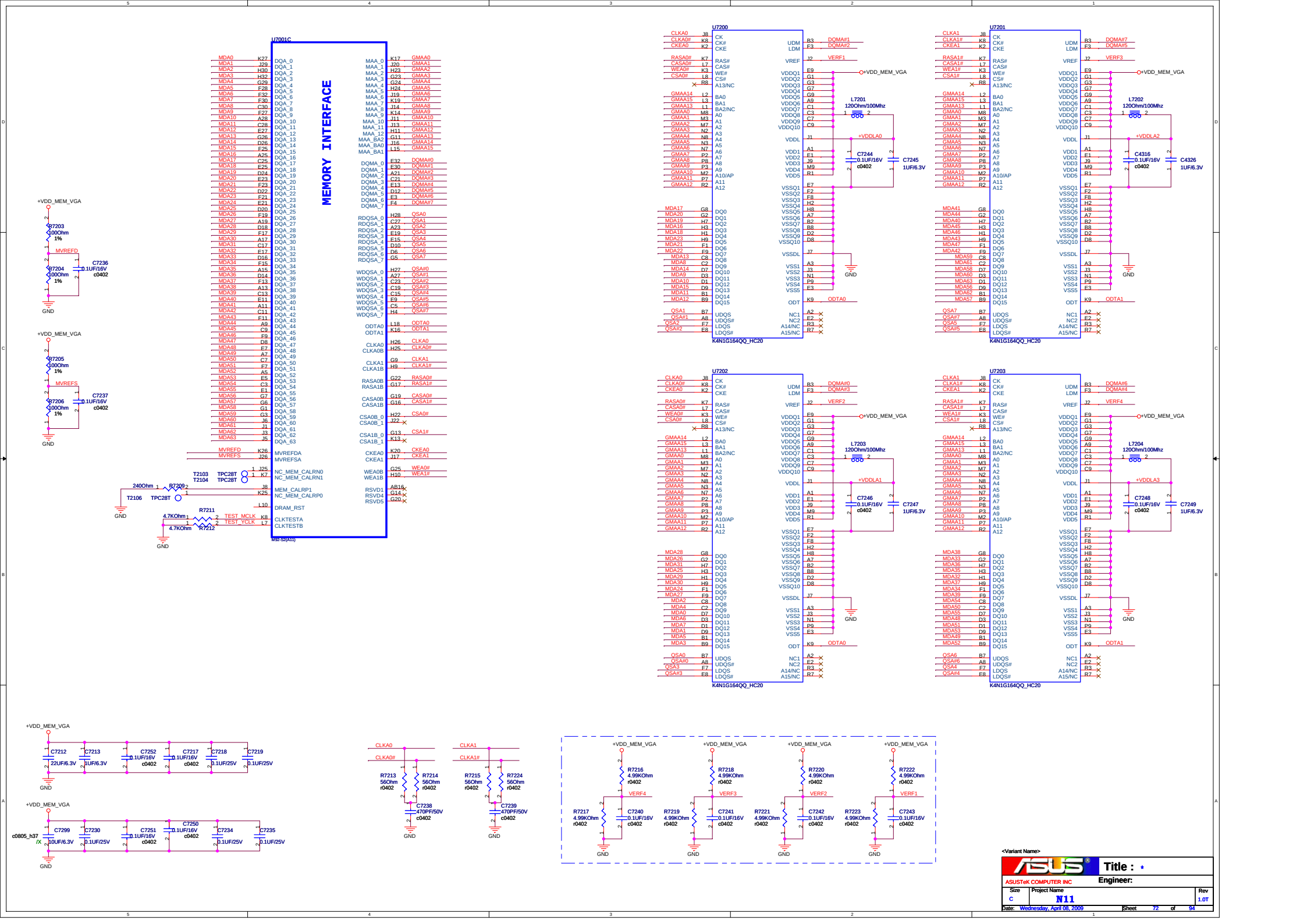
MEMORY INTERFACE
U7001C
M92-S2(A11)
U7200
U7201
U7202
U7203
K4N1G164QQ_HC20
L7201 120Ohm/100Mhz
L7202 120Ohm/100Mhz
L7203 120Ohm/100Mhz
L7204 120Ohm/100Mhz
+VDD_MEM_VGA
+VDDLA0
+VDDLA1
+VDDLA2
+VDDLA3
GND
R7203 100Ohm 1%
R7204 100Ohm 1%
R7205 100Ohm 1%
R7206 100Ohm 1%
MVREFD
MVREFS
C7236 0.1UF/16V c0402
C7237 0.1UF/16V c0402
C7244 0.1UF/16V c0402
C7245 1UF/6.3V
C7246 0.1UF/16V c0402
C7247 1UF/6.3V
C7248 0.1UF/16V c0402
C7249 1UF/6.3V
C4316 0.1UF/16V c0402
C4326 1UF/6.3V
T2103 TPC28T
T2104 TPC28T
T2106 TPC28T
R7209 240Ohm
R7211 4.7KOhm
R7212 4.7KOhm
TEST_MCLK
TEST_YCLK
C7212 22UF/6.3V
C7213 1UF/6.3V
C7252 0.1UF/16V c0402
C7217 0.1UF/16V c0402
C7218 0.1UF/25V
C7219 0.1UF/25V
C7299 10UF/6.3V c0805_h37
C7230 0.1UF/25V
C7251 0.1UF/16V c0402
C7250 0.1UF/16V c0402
C7234 0.1UF/25V
C7235 0.1UF/25V
R7213 56Ohm r0402
R7214 56Ohm r0402
R7215 56Ohm r0402
R7224 56Ohm r0402
C7238 470PF/50V c0402
C7239 470PF/50V c0402
R7216 4.99KOhm r0402
R7217 4.99KOhm r0402
R7218 4.99KOhm r0402
R7219 4.99KOhm r0402
R7220 4.99KOhm r0402
R7221 4.99KOhm r0402
R7222 4.99KOhm r0402
R7223 4.99KOhm r0402
C7240 0.1UF/16V c0402
C7241 0.1UF/16V c0402
C7242 0.1UF/16V c0402
C7243 0.1UF/16V c0402
VERF1
VERF2
VERF3
VERF4
VERF5
VERF6
VERF7
VERF8
<Variant Name>
Title :
Engineer:
ASUSTeK COMPUTER INC
Size C
Project Name N11
Rev 1.0T
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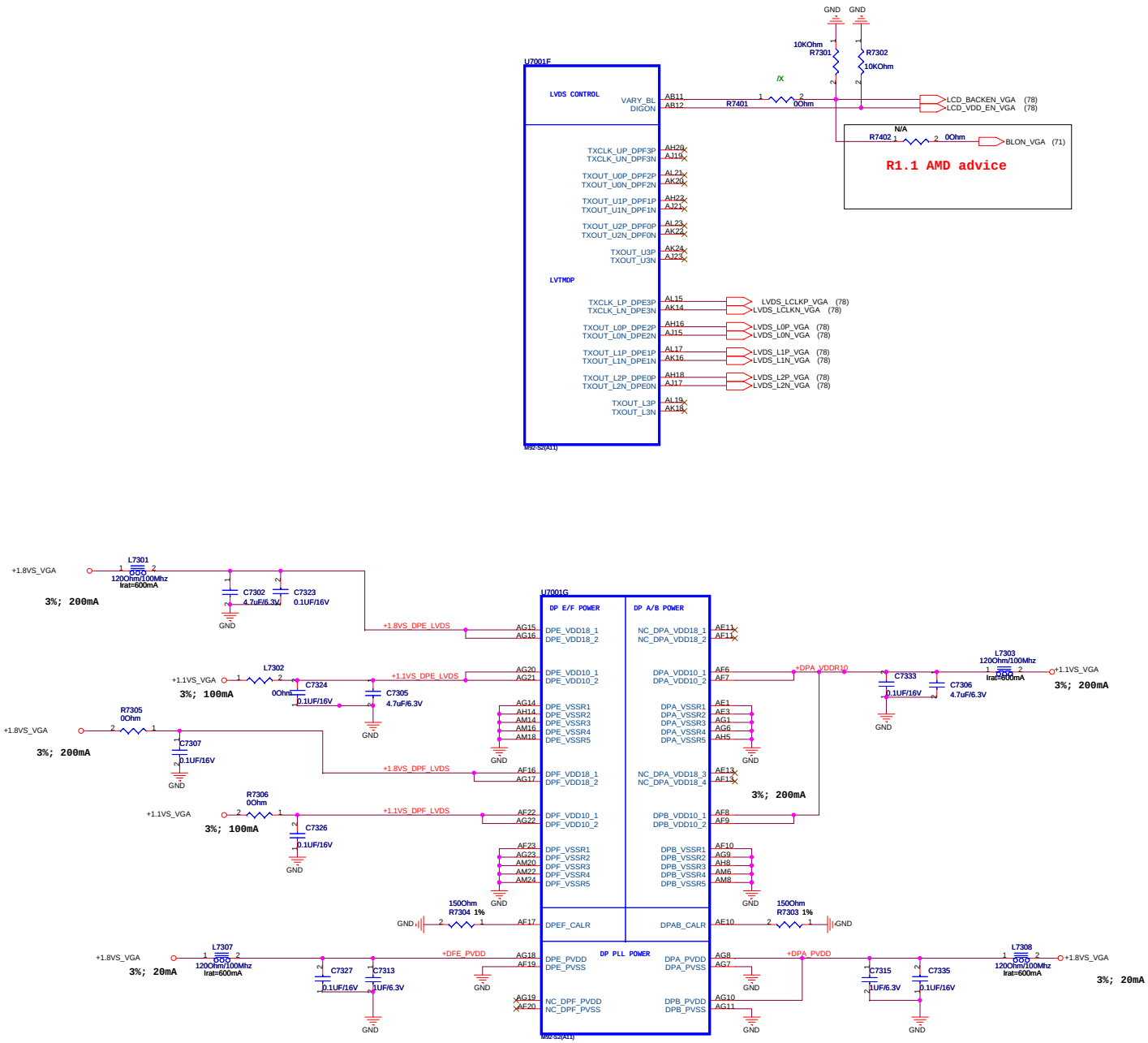

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

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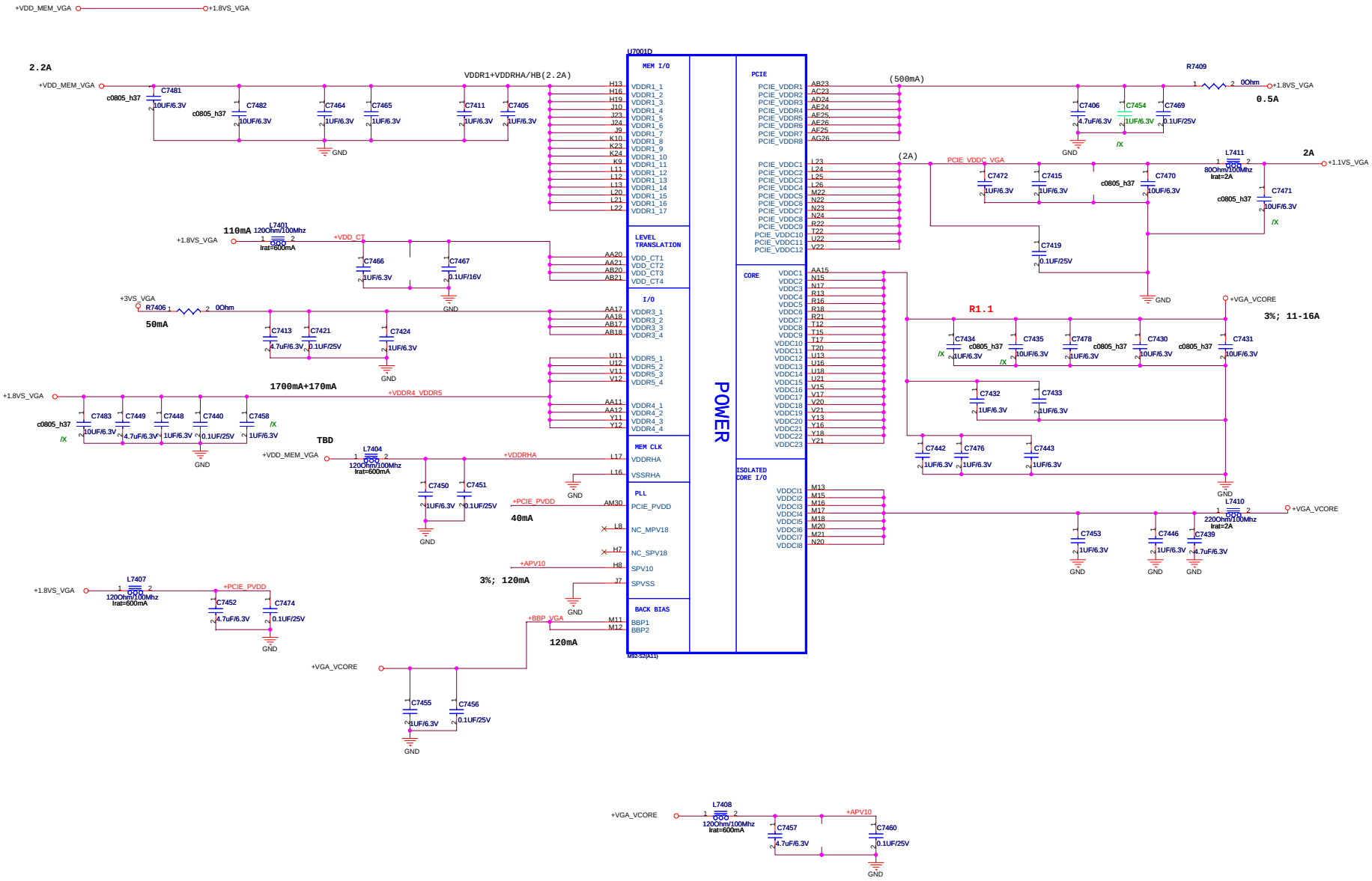
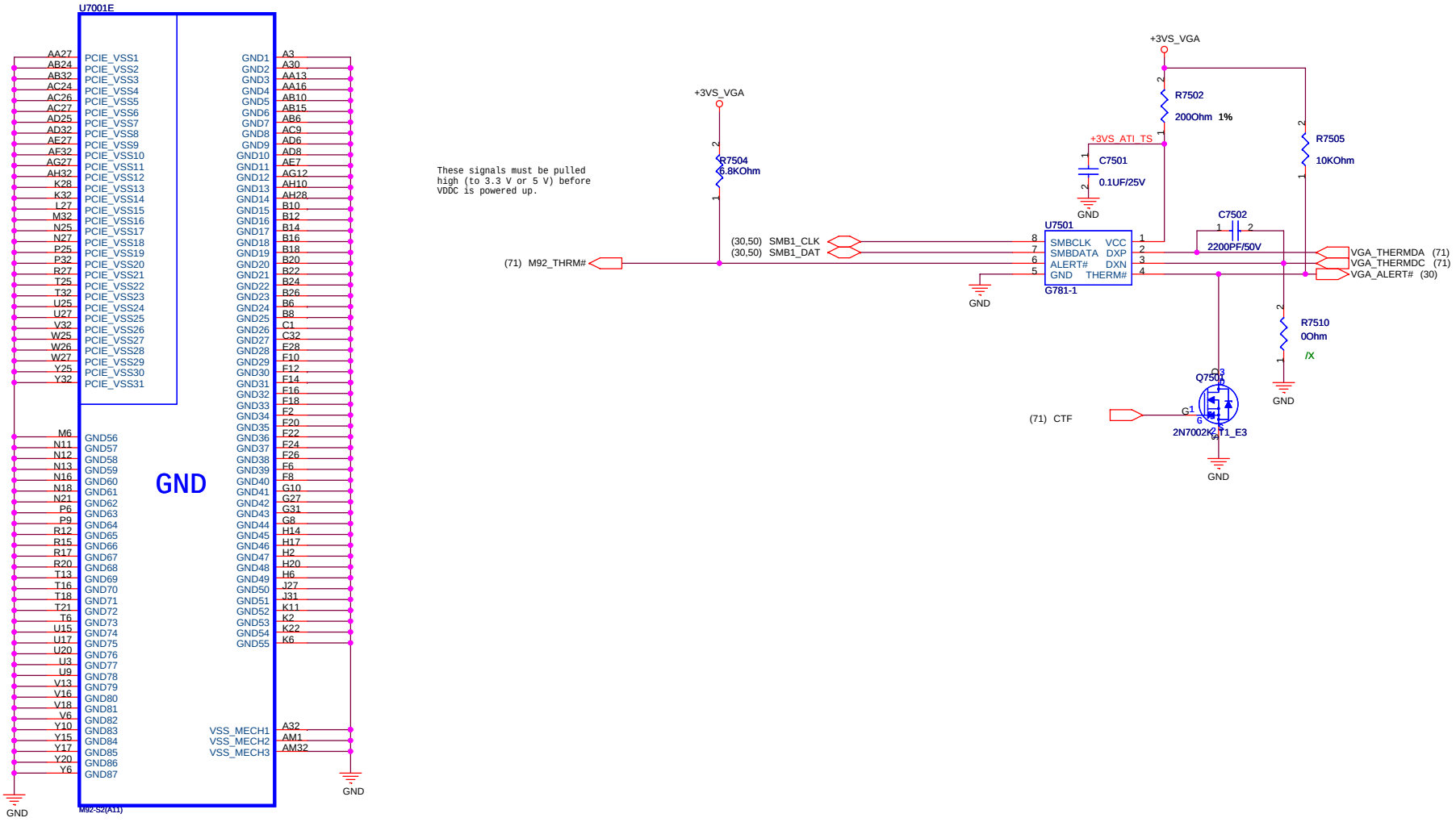

+VDD_MEM_VGA
+1.8VS_VGA
U7001D
POWER
MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
ISOLATED CORE I/O
VDDR1+VDDRHA/HB(2.2A)
2.2A
110mA
1700mA+170mA
TBD
40mA
3%; 120mA
120mA
(500mA)
(2A)
0.5A
2A
R1.1
3%; 11-16A
+VGA_VCORE
+1.1VS_VGA
+3VS_VGA
50mA
+VDD_CT
+VDDR4_VDDR5
+VDDRHA
+PCIE_PVDD
+APV10
+BBP_VGA
PCIE_VDDC
+VGA_VCORE



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

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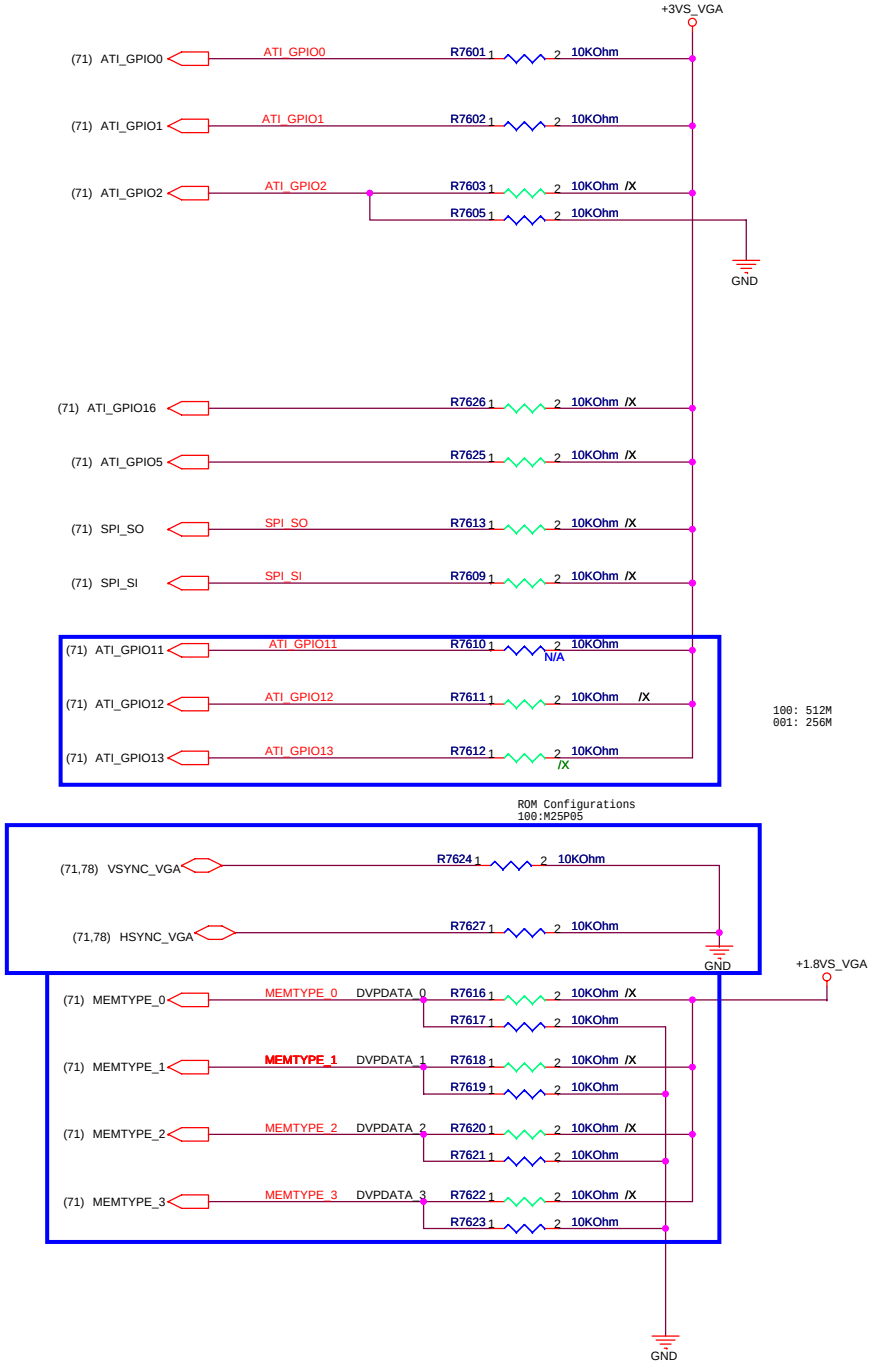

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO_1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO_2 - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

GPIO(11,13,12) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

GPIO_8 - BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_5 - AMD BOARD FEATURES I
0: 1 RANK OF MEMORY 1: 2 RANKS OF MEMORY

GPIO_16 - AMD BOARD FEATURES II
BANK SELECT;

GPIO_7 - TV OUT STANDARD
0 - PAL TVO
1 - NTSC TVO

V2SYNC - VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

GPIO_9 - VGA DISABLE : 1 for disable (set to 0 for normal operation)

HSYNC;VSYNC - AUD[1:0]
00 - No audio function
01 - Audio for DisplayPort and HDMI if adapter is detected
10 - Audio for DisplayPort only
11 - Audio for both DisplayPort and HDMI.

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	64M*16	
Samsung	0001	1	64M*16	
Hynix				
Micron				

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

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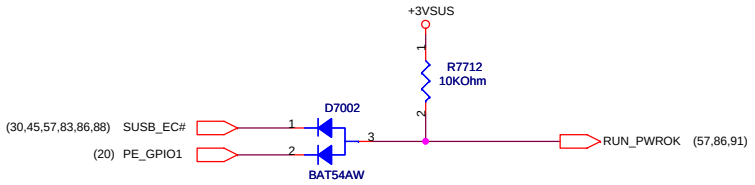
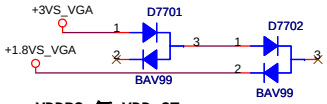
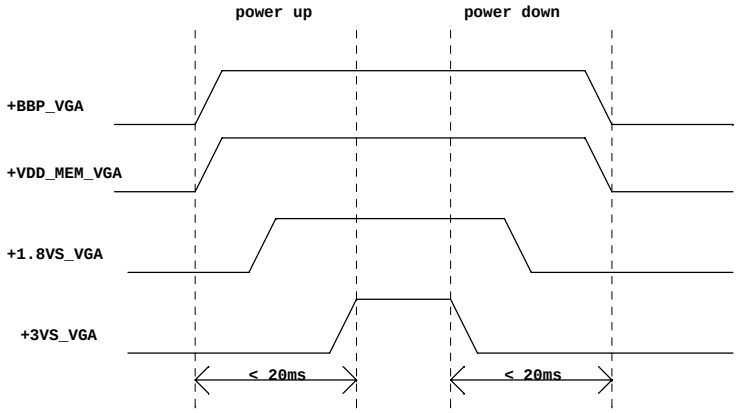
GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V





VDDR3 每 VDD_CT
< 2V



1.1-V rails should ramp before, or together with the 1.8-V rails.
The 1.1-V nominal voltage rails should never lag the 1.8-V nominal
voltage rails by more than 1.1 V within a 1 ms window.

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

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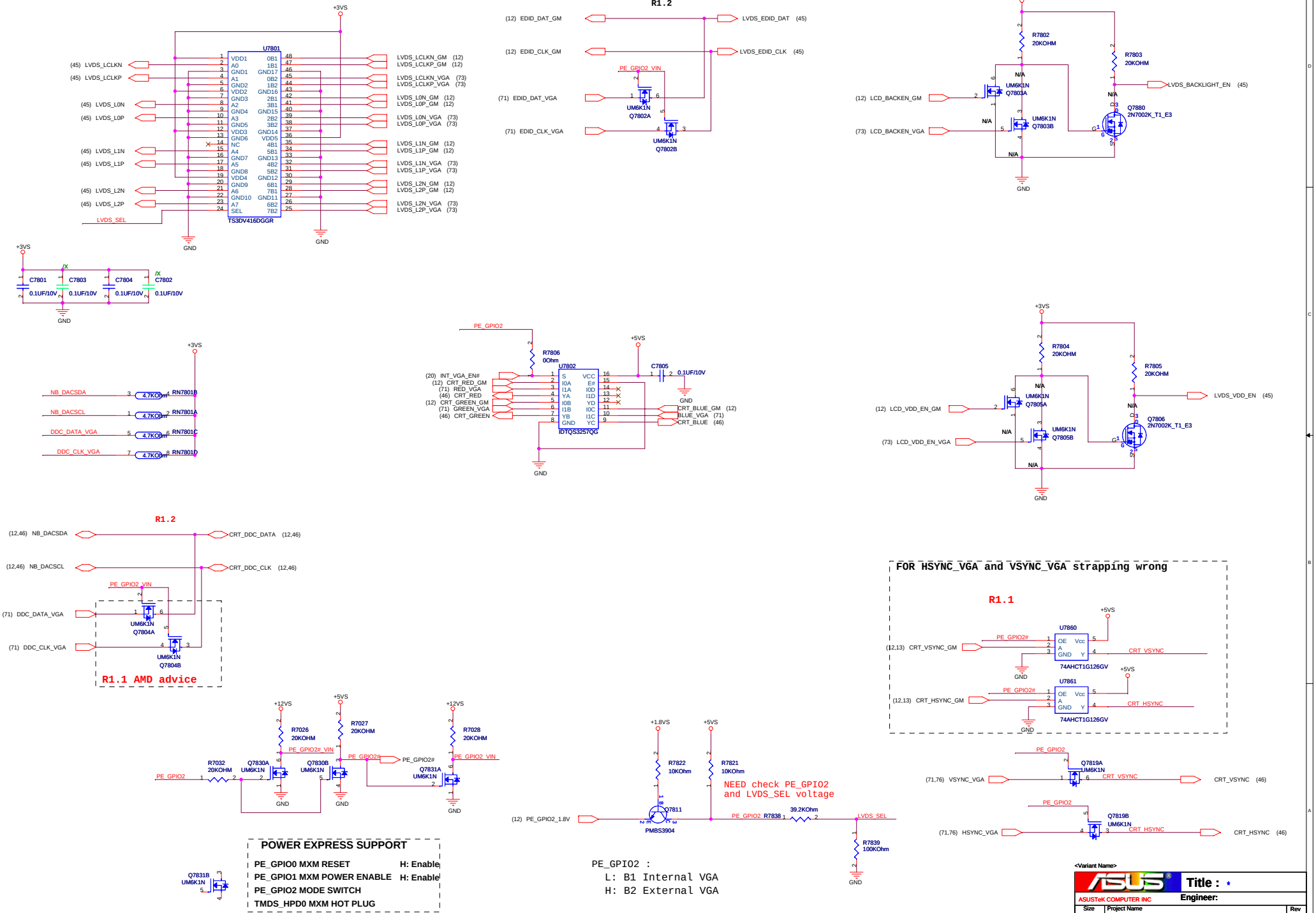
U7801
TS3DV416DGGR
LVDS_SEL
R1.2
PE_GPIO2_VIN
Q7802A
Q7802B
R7802 20KOHM
R7803 20KOHM
Q7880 2N7002K_T1_E3
LVDS_BACKLIGHT_EN (45)
C7801 0.1UF/10V
C7803 0.1UF/10V
C7804 0.1UF/10V
C7802 0.1UF/10V
RN7801B
RN7801A
RN7801C
RN7801D
R7806 0Ohm
U7802
IDTQS3257QG
C7805 0.1UF/10V
R7804 20KOHM
R7805 20KOHM
Q7806 2N7002K_T1_E3
LVDS_VDD_EN (45)
R1.2
R1.1 AMD advice
FOR HSYNC_VGA and VSYNC_VGA strapping wrong
R1.1
U7860
U7861
74AHCT1G126GV
R7026 20KOHM
R7027 20KOHM
R7028 20KOHM
R7032 20KOHM
Q7830A
Q7830B
Q7831A
R7822 10KOhm
R7821 10KOhm
Q7811
PMBS3904
NEED check PE_GPIO2 and LVDS_SEL voltage
R7838 39.2KOhm
R7839 100KOhm
Q7819A
Q7819B
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
PE_GPIO2 :
L: B1 Internal VGA
H: B2 External VGA
<Variant Name>
Title :
Engineer:
ASUSTeK COMPUTER INC.
Project Name N11
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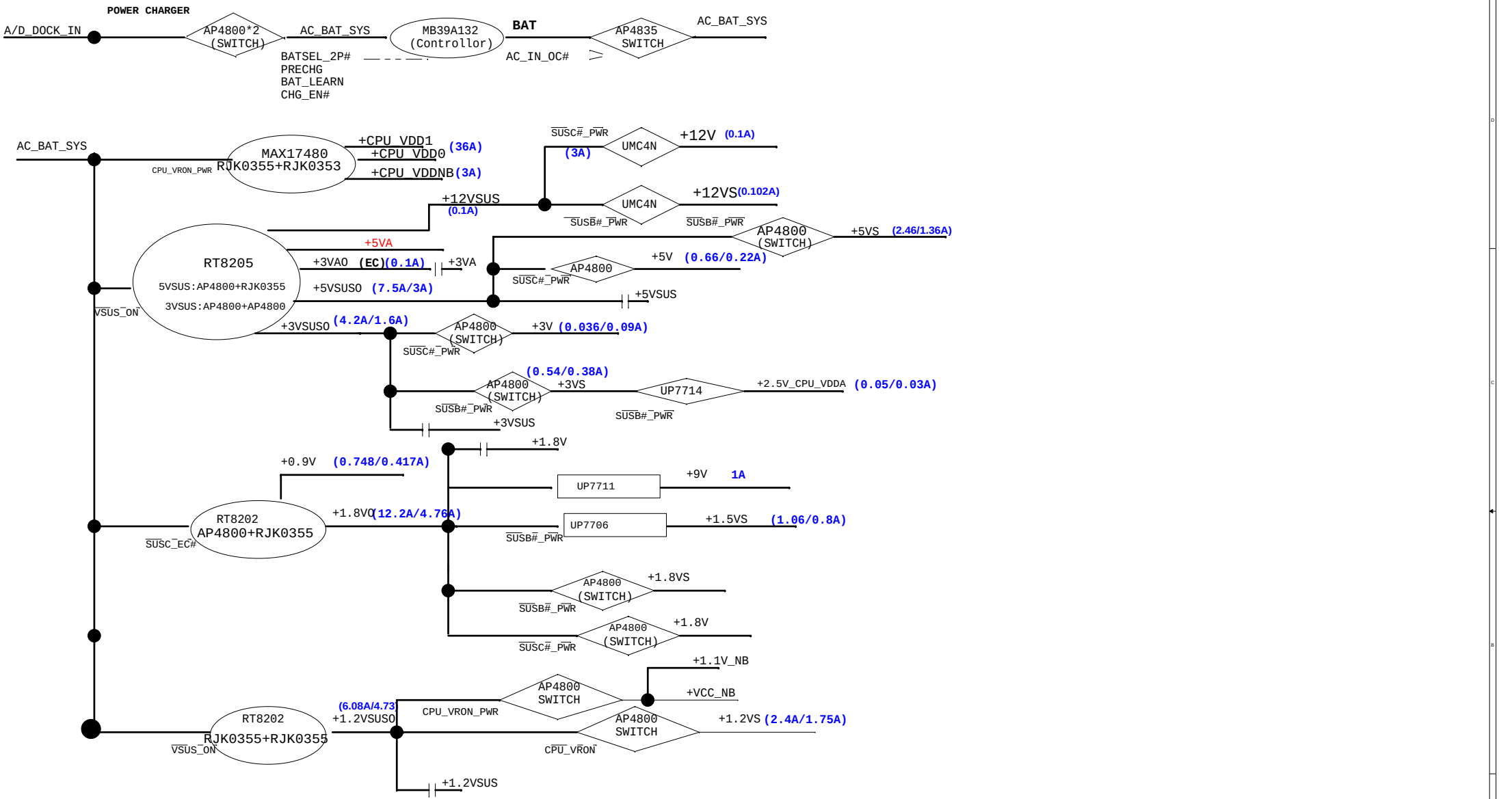

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_FLOW

Engineer: N/A

Size	Project Name	Rev
A2	Oemga	1.0

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<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_ FLOW	
	Engineer: N/A	
Size: A	Project Name: Oemga	Rev: 1.0
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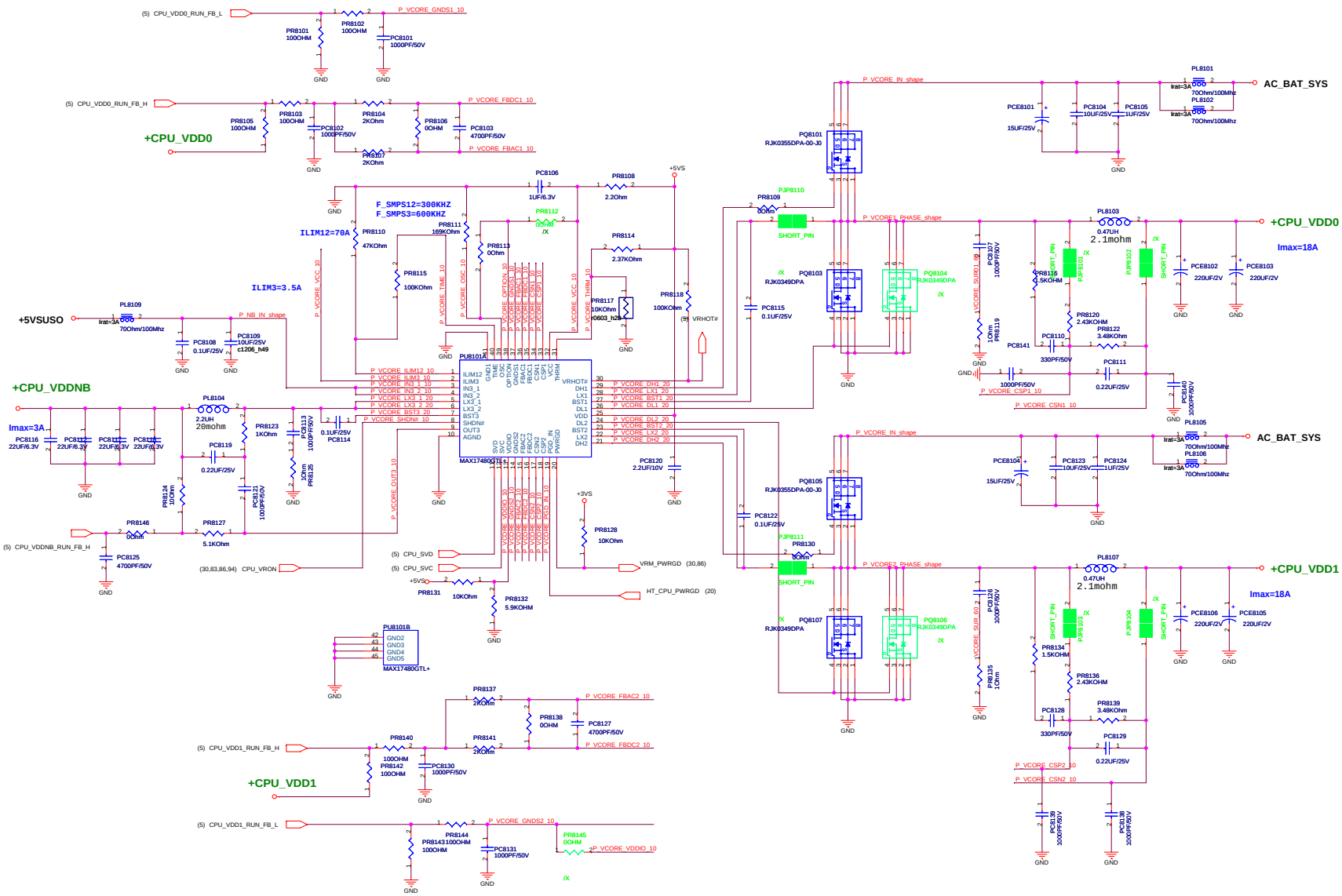

<Variant Name>

ASUSTeK COMPUTER INC

Title : +VCORE

Engineer:

Size	Project Name	Rev
Custom	Oemga	1.0

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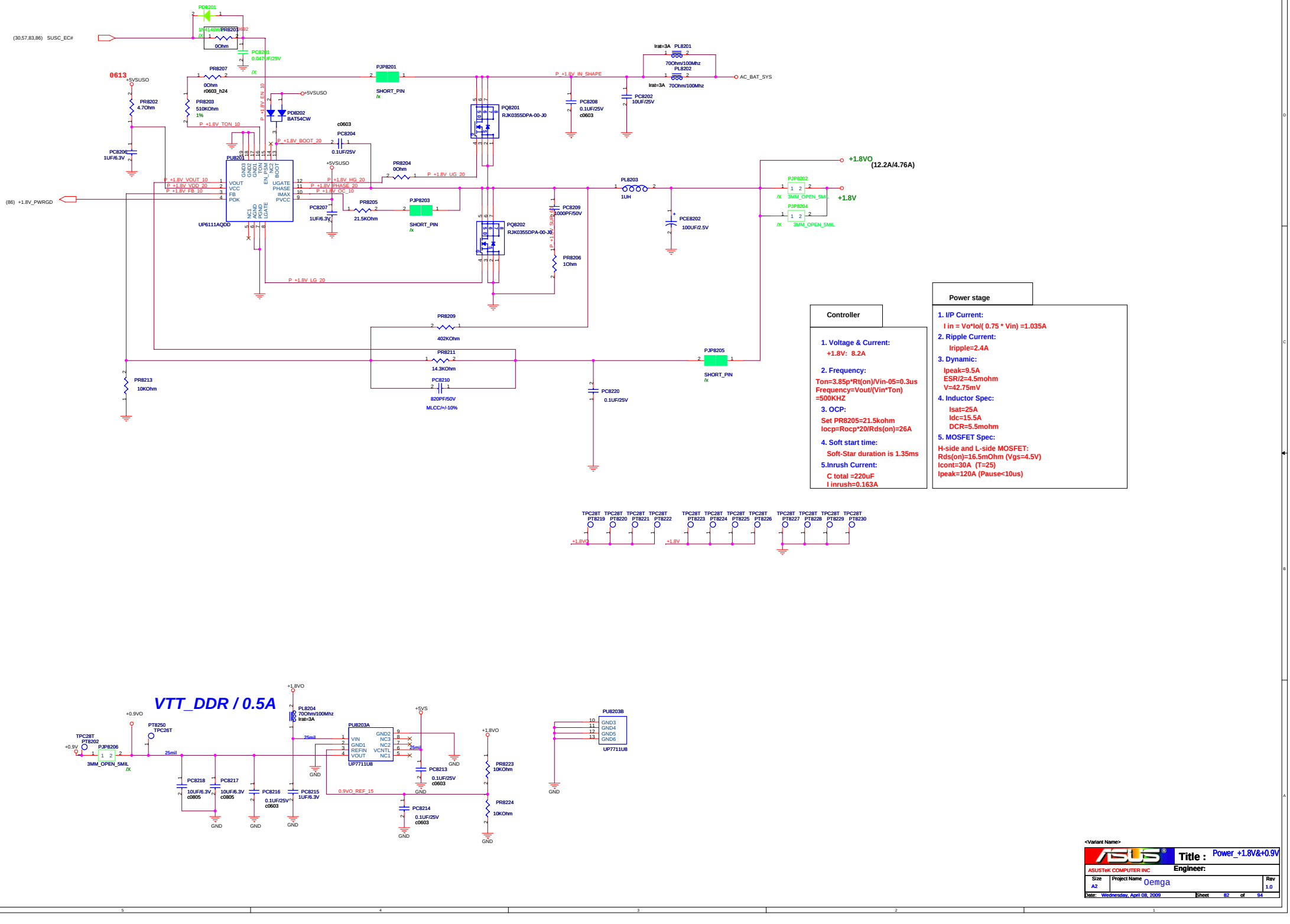

Controller

1. Voltage & Current:
   +1.8V: 8.2A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8205=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.035A
2. Ripple Current:
   Iripple=2.4A
3. Dynamic:
   Ipeak=9.5A
   ESR/2=4.5mohm
   V=42.75mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+1.8V&+0.9V

Engineer:

Size	Project Name	Rev
A2	Oemga	1.0

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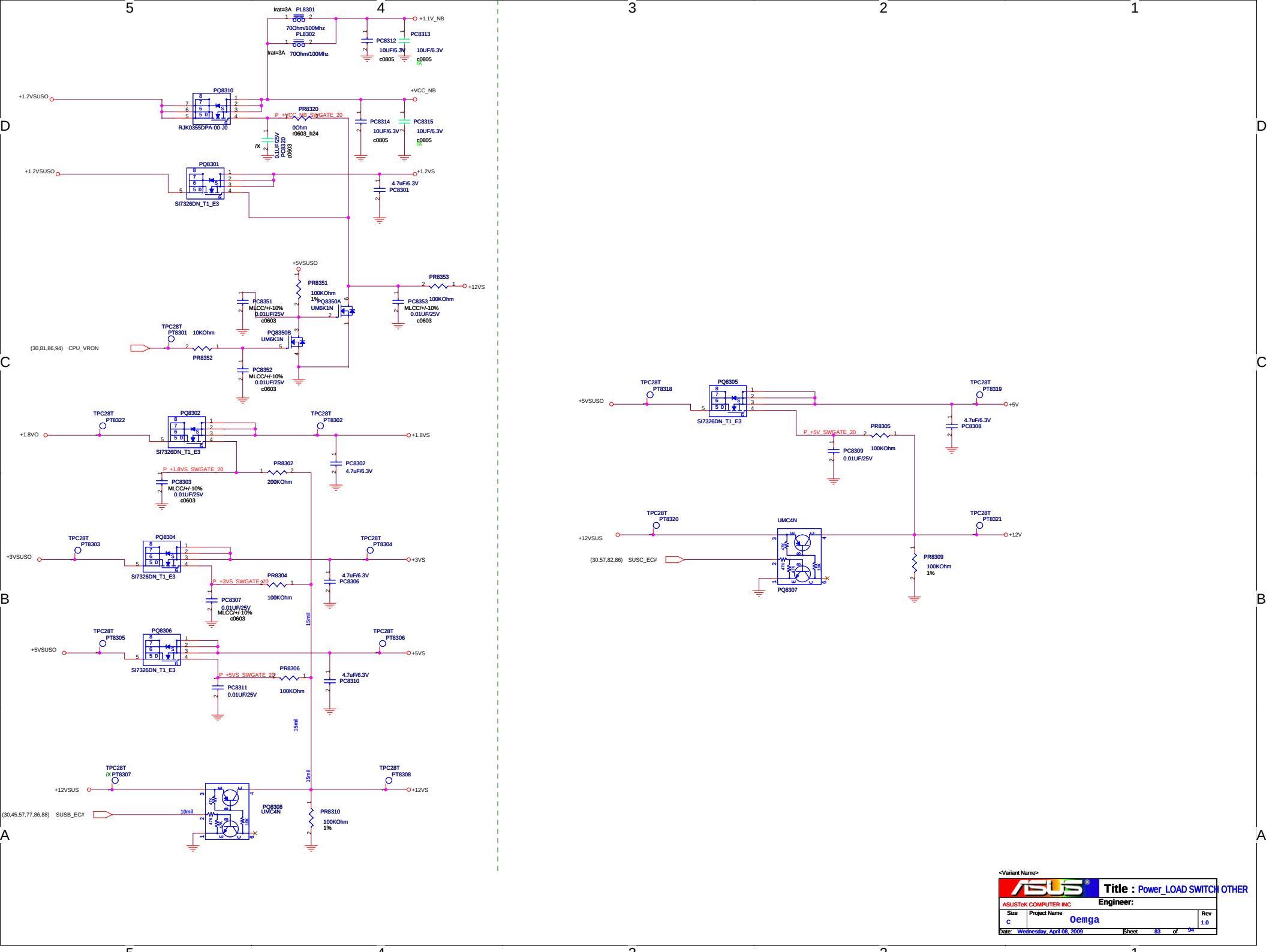

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_LOAD SWITCH OTHER

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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<Variant Name>

Title : Power_Charger

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
Custom		1.0

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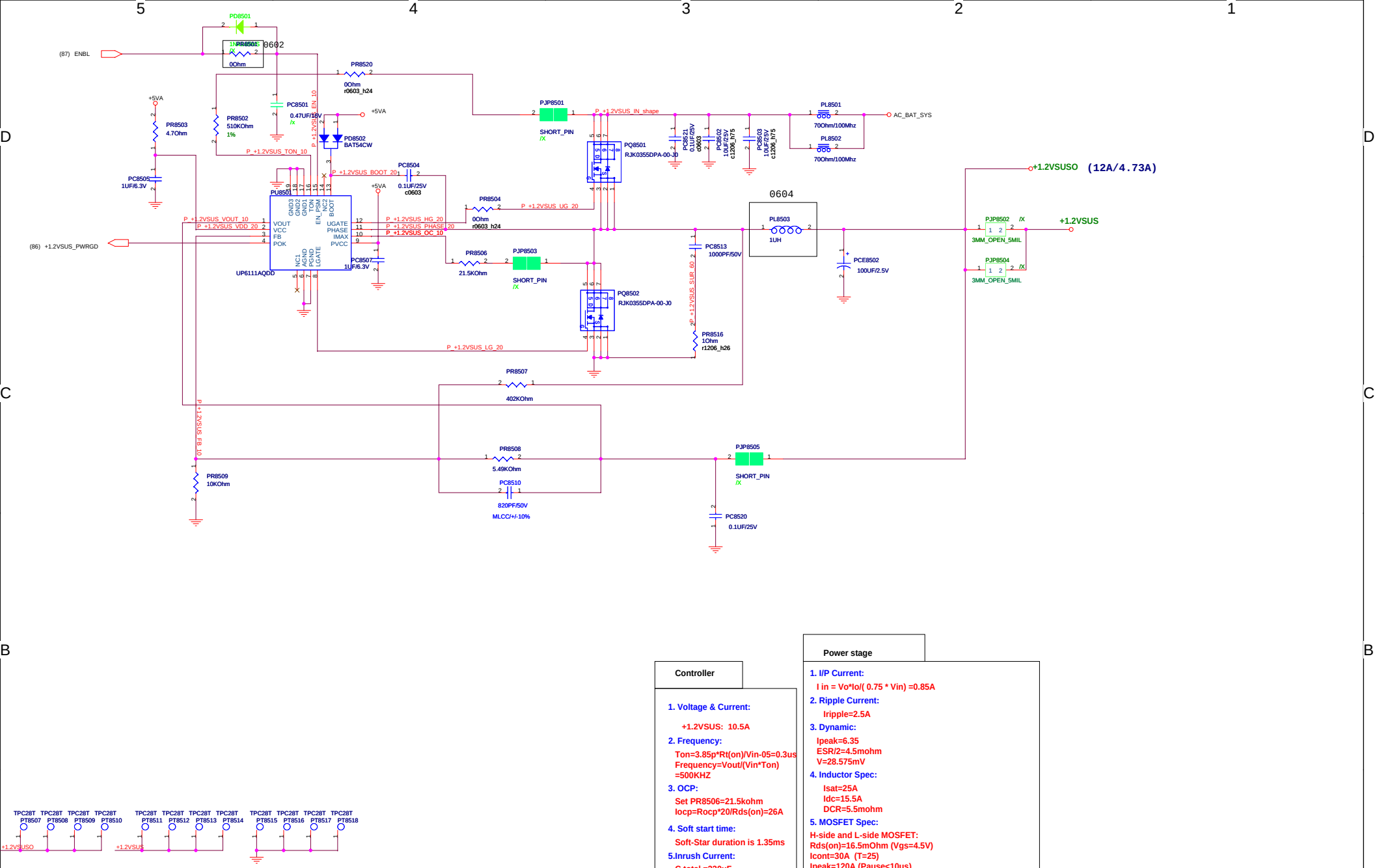

Controller

1. Voltage & Current:
   +1.2VSUS: 10.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=2.5A
3. Dynamic:
   Ipeak=6.35
   ESR/2=4.5mohm
   V=28.575mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_1.2VSUS

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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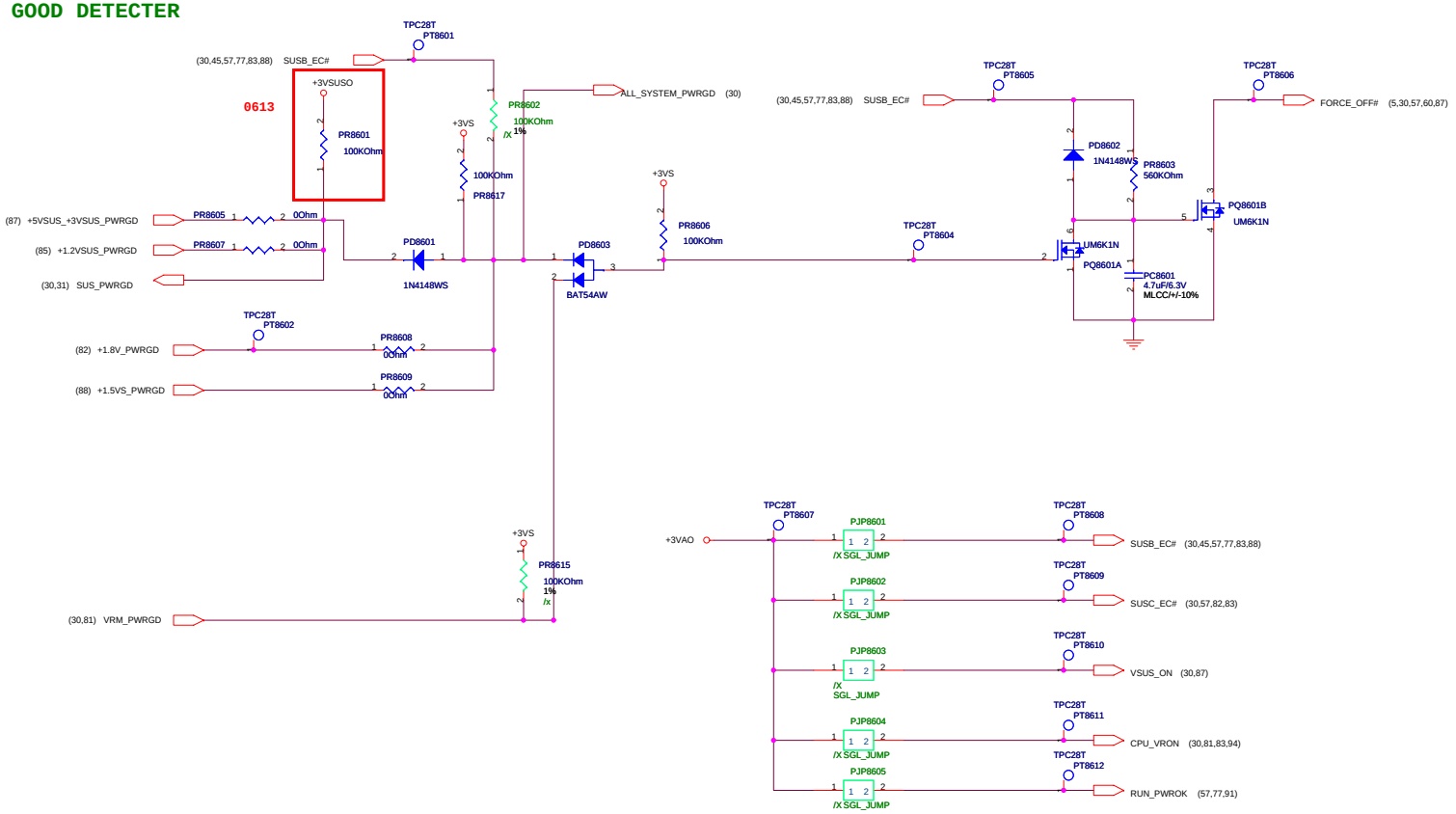
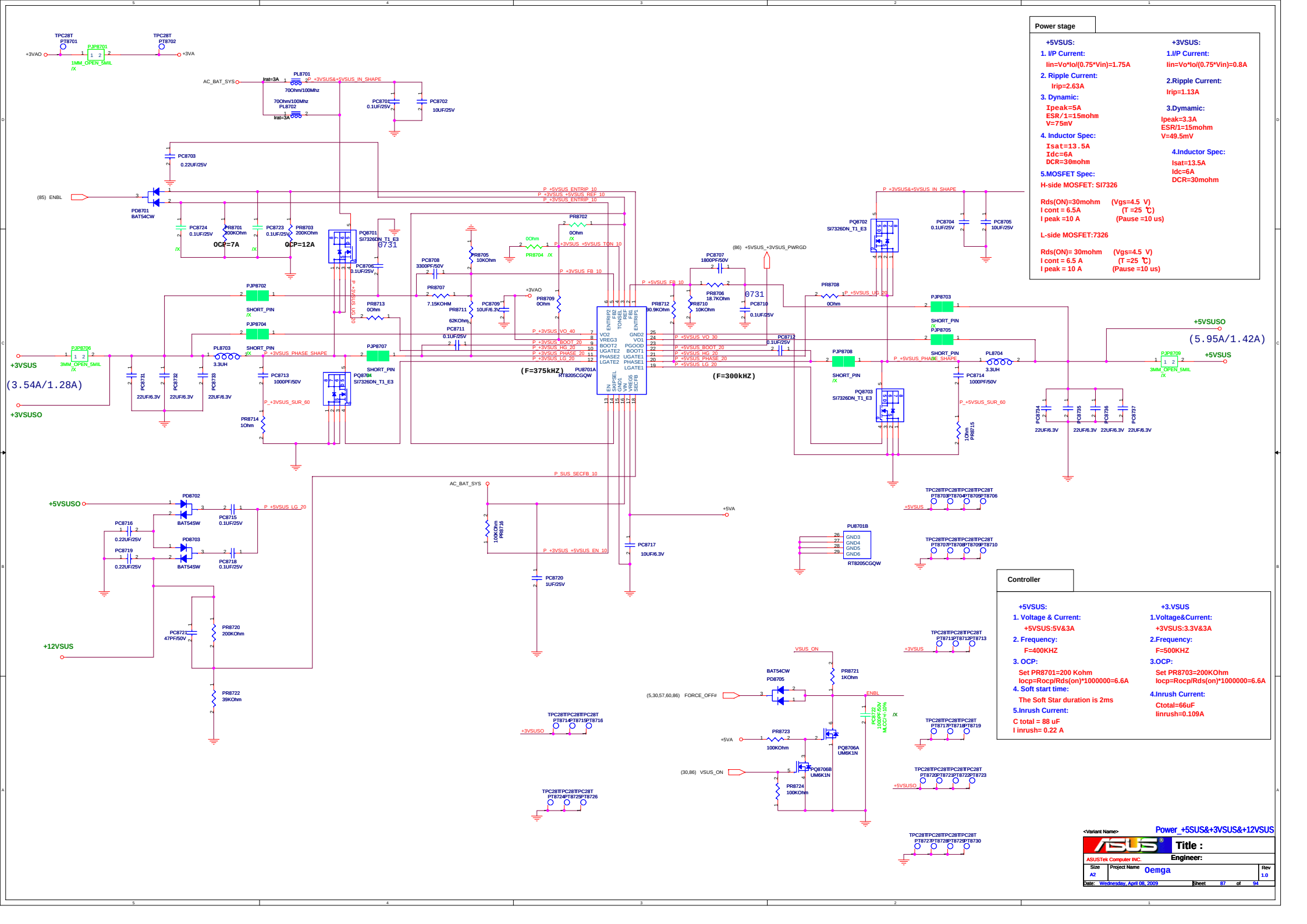
POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_GOOD_DETECTER	
	Engineer:	
Size: C	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 86 of 94	


Power stage
+5VSUS:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=1.75A
2. Ripple Current:
Irip=2.63A
3. Dynamic:
Ipeak=5A
ESR/1=15mohm
V=75mV
4. Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
5.MOSFET Spec:
H-side MOSFET: SI7326
Rds(ON)=30mohm (Vgs=4.5 V)
I cont = 6.5A (T =25 ℃)
I peak =10 A (Pause =10 us)
L-side MOSFET:7326
Rds(ON)= 30mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 10 A (Pause =10 us)
+3VSUS:
1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=0.8A
2.Ripple Current:
Irip=1.13A
3.Dymamic:
Ipeak=3.3A
ESR/1=15mohm
V=49.5mV
4.Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
Controller
+5VSUS:
1. Voltage & Current:
+5VSUS:5V&3A
2. Frequency:
F=400KHZ
3. OCP:
Set PR8701=200 Kohm
Iocp=Rocp/Rds(on)*1000000=6.6A
4. Soft start time:
The Soft Star duration is 2ms
5.Inrush Current:
C total = 88 uF
I inrush= 0.22 A
+3.VSUS
1.Voltage&Current:
+3VSUS:3.3V&3A
2.Frequency:
F=500KHZ
3.OCP:
Set PR8703=200KOhm
Iocp=Rocp/Rds(on)*1000000=6.6A
4.Inrush Current:
Ctotal=66uF
Iinrush=0.109A
+3VSUS
(3.54A/1.28A)
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
OCP=7A
OCP=12A
(F=375kHZ)
(F=300kHZ)
PU8701A RT8205CGQW
PU8701B RT8205CGQW
PQ8701 SI7326DN_T1_E3
PQ8702 SI7326DN_T1_E3
PQ8703 SI7326DN_T1_E3
PQ8704 SI7326DN_T1_E3
PQ8706A UM6K1N
PQ8706B UM6K1N
PD8701 BAT54CW
PD8702 BAT54SW
PD8703 BAT54SW
PD8705 BAT54CW
AC_BAT_SYS
+3VAO
+5VA
(85) ENBL
(86) +5VSUS_+3VSUS_PWRGD
(5,30,57,60,86) FORCE_OFF#
(30,86) VSUS_ON
VSUS_ON
ENBL
P_+5VSUS_ENTRIP_10
P_+3VSUS_+5VSUS_REF_10
P_+3VSUS_ENTRIP_10
P_+3VSUS&+5VSUS_IN_SHAPE
P_+3VSUS_+5VSUS_TON_10
P_+3VSUS_FB_10
P_+5VSUS_FB_10
P_+5VSUS_UG_20
P_+3VSUS_VO_40
P_+5VSUS_VO_30
P_+3VSUS_BOOT_20
P_+5VSUS_BOOT_20
P_+3VSUS_HG_20
P_+5VSUS_HG_20
P_+3VSUS_PHASE_20
P_+5VSUS_PHASE_20
P_+3VSUS_LG_20
P_+5VSUS_LG_20
P_+3VSUS_PHASE_SHAPE
P_+5VSUS_PHASE_SHAPE
P_+3VSUS_SUR_60
P_+5VSUS_SUR_60
P_SUS_SECFB_10
P_+3VSUS_+5VSUS_EN_10
<Variant Name>
Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTek Computer INC.
Engineer:
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
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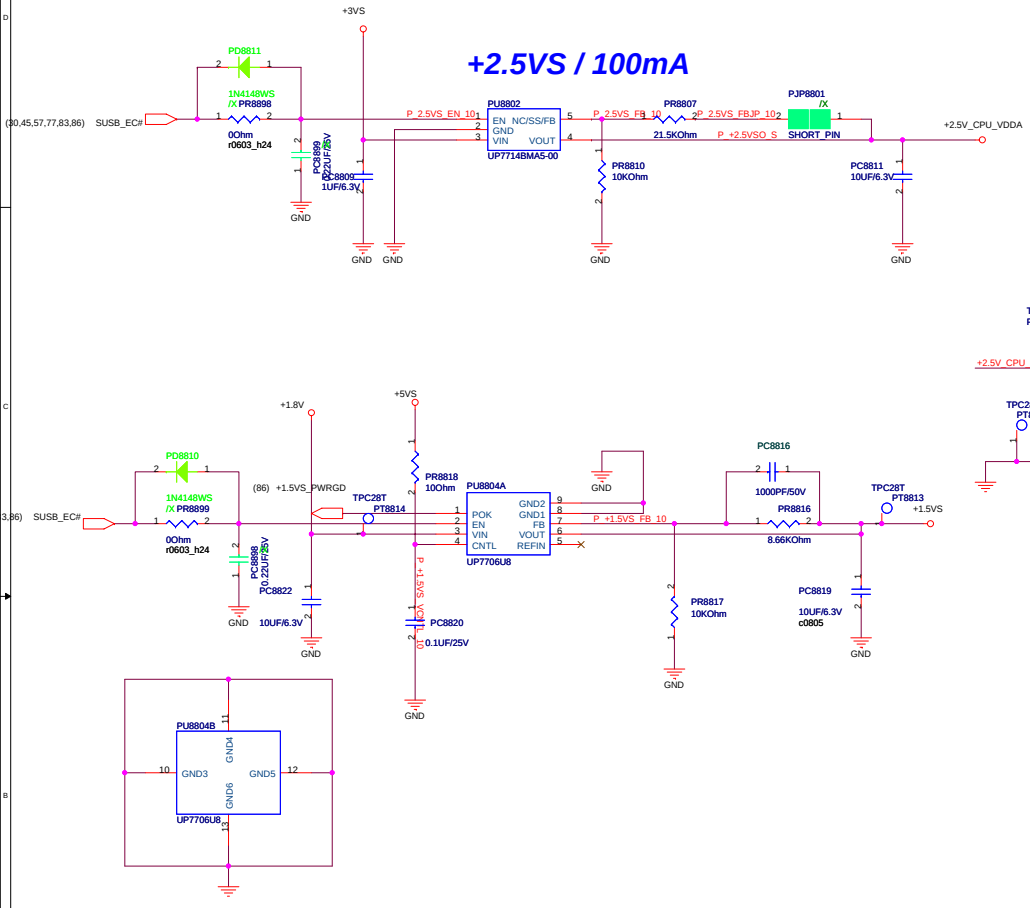


2.5V @ 0.2A

1. Dropout Voltage:

△V = 0.21V (Io =0.3A)

2. Current Limit:

I limit =320mA

3. Continue Current:

I cont = 300mA

4. Power Dissipation:

Rthjc = 250℃/W
Pd = 0.4W

5. EN Voltage:

V rising = 2V
V falling = 0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

+1.5VS @ 1.2A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =4A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc = 52℃/W
Pd =1.9W

5. EN Voltage:

V rising = 1.4V
V falling = 0.8V

6. Supply Voltage:

Vcc =5V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

<Variant Name>

Power_+2.5V&+1.5VS&+1.1V_NB

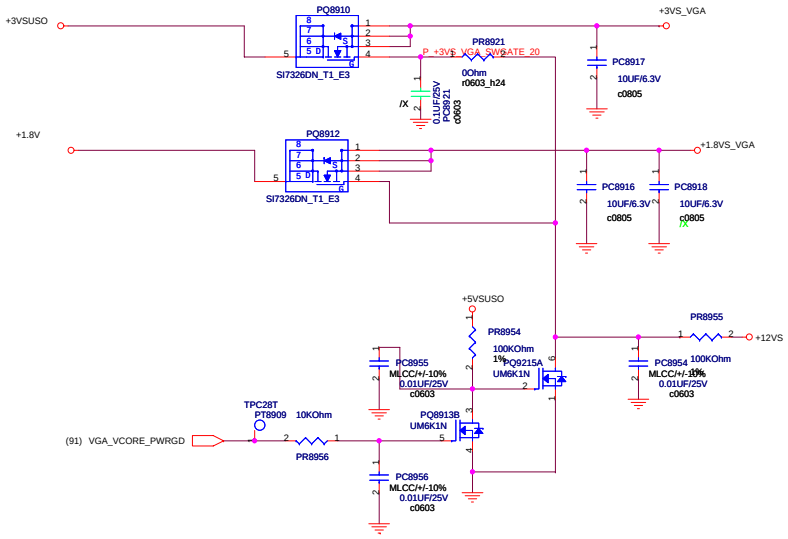
Title :

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 88 of 94



<Variant Name>

Title :

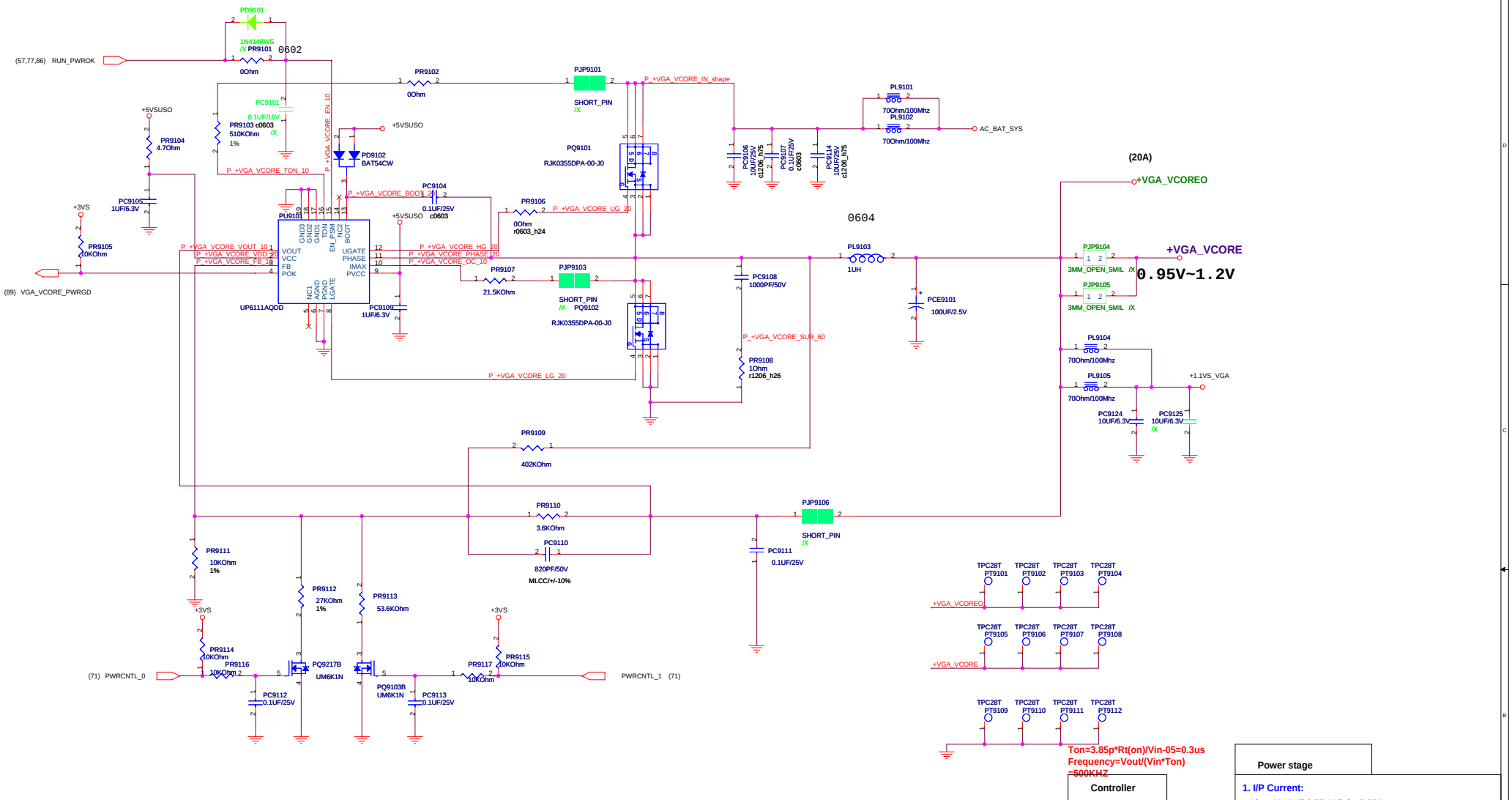
ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 89 of 94

ASUSTek Computer INC.	Title :	
	Engineer:	
Size: Custom	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 90 of 94	



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	1.02	-5%
0	1	1.071	Normal
1	0	1.12	+5%
1	1	1.171	+10%

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
~500KHZ

Controller

1. Voltage & Current:
   +1.2VSUS: 16A
2. Frequency:
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=3.74A
3. Dynamic:
   Ipeak=6.1A
   ESR/2=4.5mohm
   V=27.5mohm
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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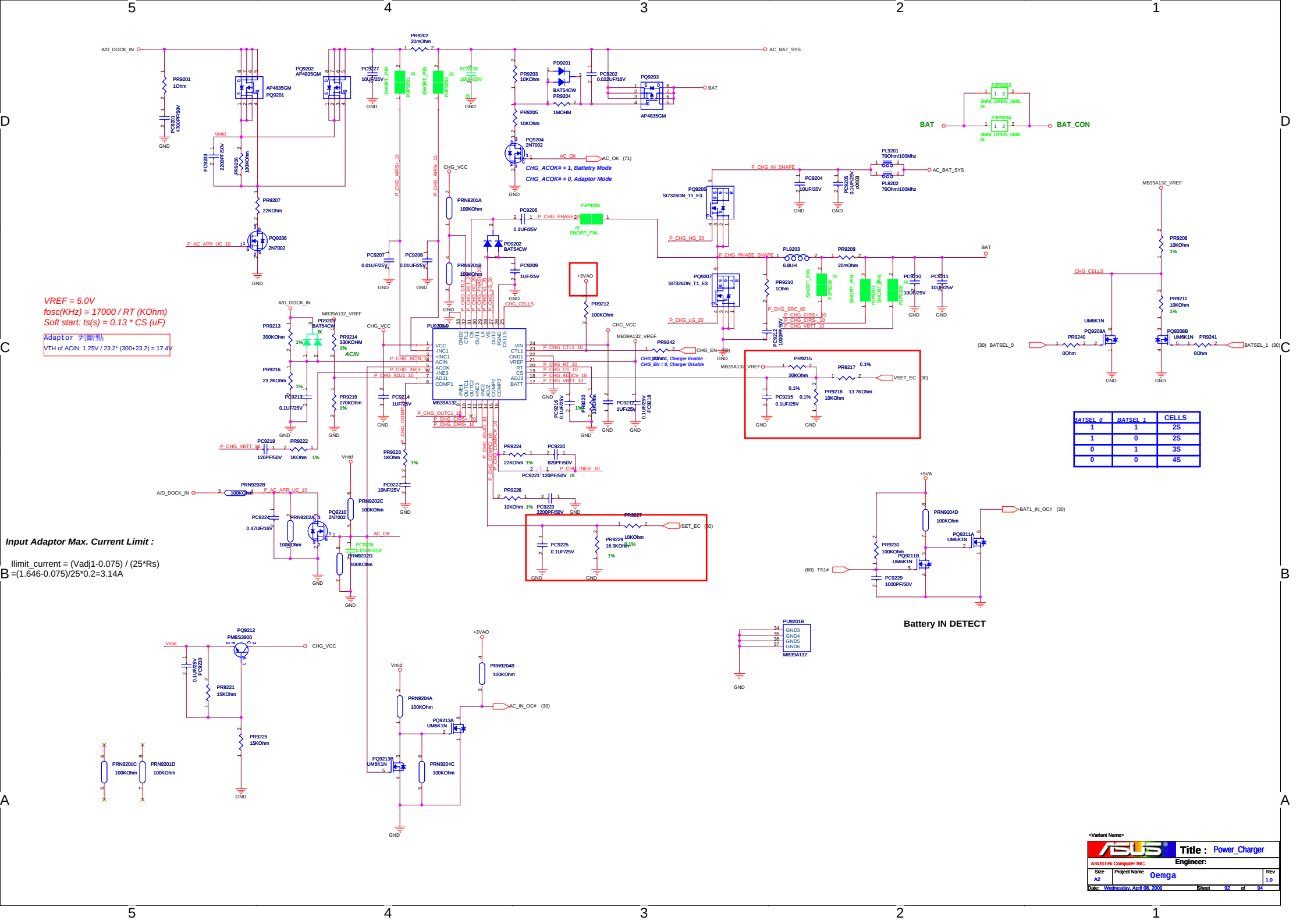
VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
Adaptor 判斷點
VTH of ACIN: 1.25V / 23.2* (300+23.2) = 17.4V
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25*0.2=3.14A
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
CHG_EN = 1, Charger Enable
CHG_EN = 0, Charger Disable
ACIN
Battery IN DETECT
BATSEL_0 BATSEL_1 CELLS
1 1 2S
1 0 2S
0 1 3S
0 0 4S
Title : Power_Charger
Engineer:
ASUSTek Computer INC.
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
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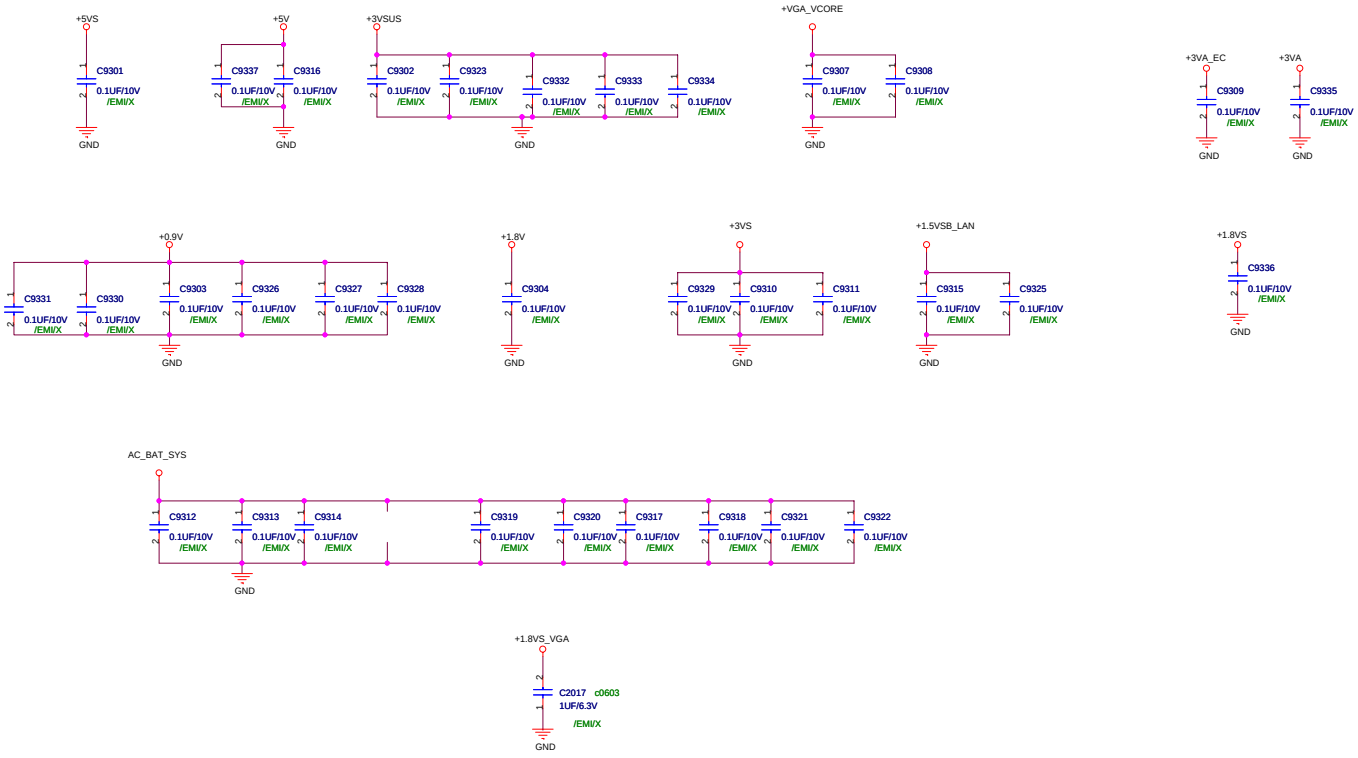


<Variant Name>

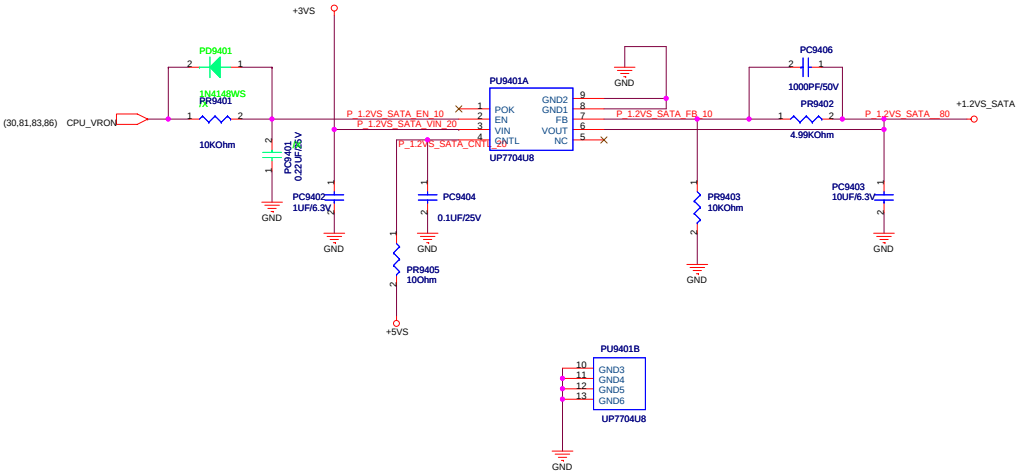
Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C		

Date: Wednesday, April 08, 2009 Sheet 93 of 94



+1.2VS_SATA /

220mA/350mA

1.2V @ 0.1A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =2.5A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc =52℃/W
Pd = 1.8W

5. EN Voltage:

V rising = 2V
V falling =
0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush =
0.063A

<Variant Name>

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
C		

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