K40AA SCHEMATIC R1.2

SYSTEM PAGE REF.

POWER PAGE REF.

ASUSTeK COMPUTER INC. NB1

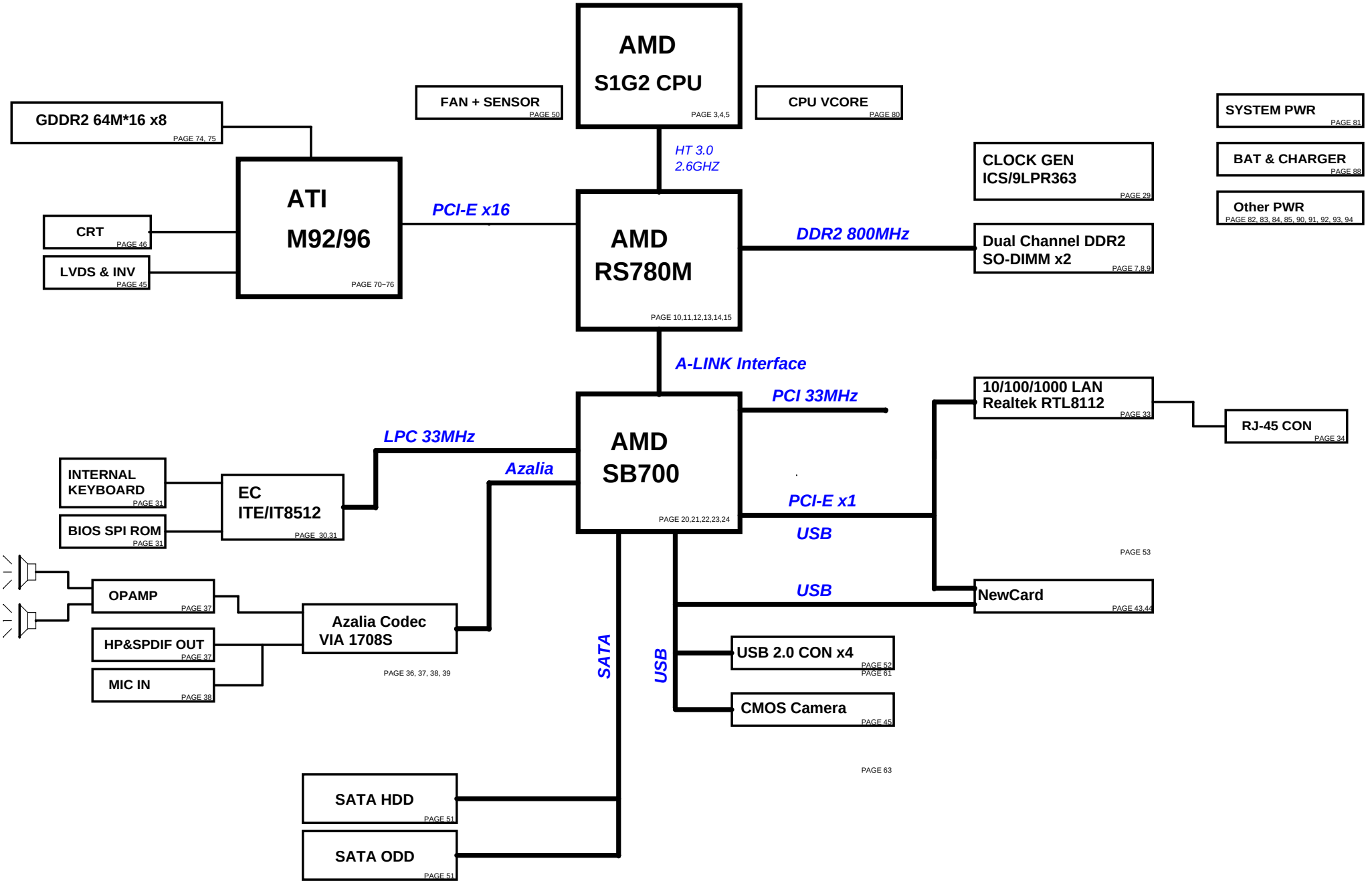
Title : Page Reference

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	K40AA	1.00

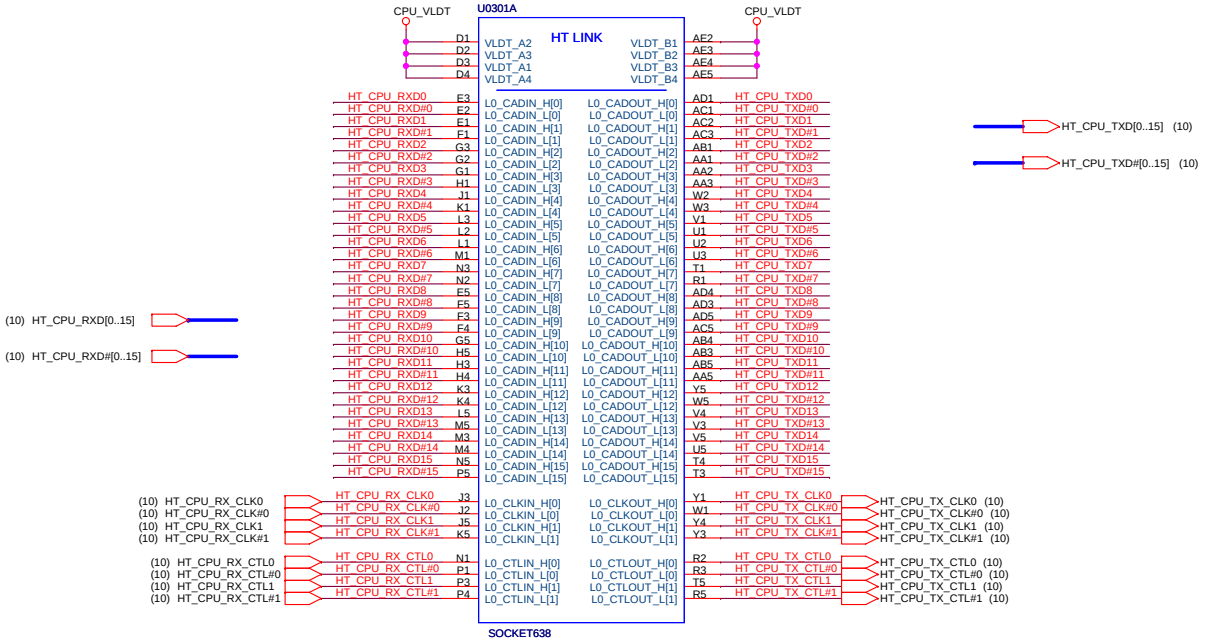
Date: Wednesday, April 08, 2009 Sheet 1 of 94

K40AA Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 2 of 94	

1.5A



(10) HT_CPU_RXD[0..15]

(10) HT_CPU_RXD#[0..15]

HT_CPU_TXD[0..15] (10)

HT_CPU_TXD#[0..15] (10)

(10) HT_CPU_RX_CLK0
(10) HT_CPU_RX_CLK#0
(10) HT_CPU_RX_CLK1
(10) HT_CPU_RX_CLK#1

HT_CPU_TX_CLK0 (10)
HT_CPU_TX_CLK#0 (10)
HT_CPU_TX_CLK1 (10)
HT_CPU_TX_CLK#1 (10)

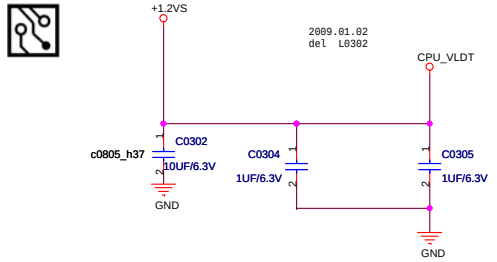
(10) HT_CPU_RX_CTL0
(10) HT_CPU_RX_CTL#0
(10) HT_CPU_RX_CTL1
(10) HT_CPU_RX_CTL#1

HT_CPU_TX_CTL0 (10)
HT_CPU_TX_CTL#0 (10)
HT_CPU_TX_CTL1 (10)
HT_CPU_TX_CTL#1 (10)

Change P/N to 12G011306380

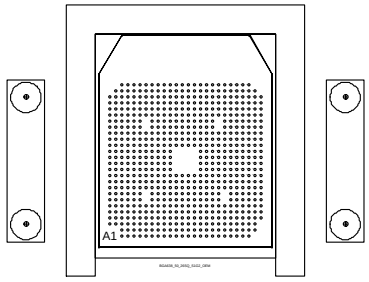
071113

Do not cross plane.



Place close to socket

*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**



ASUSTeK COMPUTER INC. NB1	Title : Griffin HT I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 3 of 94	

Processor Memory Interface

place close to PROCESSOR within 1.5 inch

(7) MEM_MA0_CLK7 — MEM_MA0_CLK_H7 — C0405 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L7 — (7) MEM_MA0_CLK7#

(7) MEM_MA0_CLK1 — MEM_MA0_CLK_H1 — C0406 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L1 — (7) MEM_MA0_CLK#1

071114

place close to PROCESSOR within 1.5 inch

(8) MEM_MB0_CLK7 — MEM_MB0_CLK_H7 — C0407 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L7 — (8) MEM_MB0_CLK7#

(8) MEM_MB0_CLK1 — MEM_MB0_CLK_H1 — C0408 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L1 — (8) MEM_MB0_CLK#1

0.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8V — R0401 39.2OHM — M_ZP — AE10 — R0402 39.2OHM — M_ZN — AE10 — T0401 TPC28T — MEM_MA_RESET# — H16

U0301B

MEM:CMD/CTRL/CLK

+0.9V — D10, C10, B10, AD10 — VTT2, VTT8, VTT3, VTT1

M_ZP, M_ZN

RSVD8

MA0_ODT[0], MA0_ODT[1], MA1_ODT[0], MA1_ODT[1]

MA0_CS_L[0], MA0_CS_L[1], MA1_CS_L[0], MA1_CS_L[1]

MA_CKE[0], MA_CKE[1]

MA_CLK_H[5], MA_CLK_L[5], MA_CLK_H[1], MA_CLK_L[1], MA_CLK_H[7], MA_CLK_L[7], MA_CLK_H[4], MA_CLK_L[4]

MA_ADD[0] … MA_ADD[15]

MA_BANK[0], MA_BANK[1], MA_BANK[2]

MA_RAS_L, MA_CAS_L, MA_WE_L

VTT4, VTT5, VTT6, VTT7, VTT9 — W10, AC10, AB10, AA10, A10 — +0.9V

VTT_SENSE — Y10 — T0417 TPC28T — 071115

M_VREF — W17 — CPU_M_VREF

RSVD6 — B18 — MEM_MB_RESET# — TPC28T — T0410

MB0_ODT[0], MB0_ODT[1], MB1_ODT[0] — W26, W23, Y26 — MEM_MB0_ODT0 (8,9), MEM_MB0_ODT1 (8,9), MEM_MB1_ODT0 — T0411 TPC28T

MB0_CS_L[0], MB0_CS_L[1], MB1_CS_L[0] — V26, W25, U22 — MEM_MB0_CS#0 (8,9), MEM_MB0_CS#1 (8,9)

MB_CKE[0], MB_CKE[1] — J25, H26 — MEM_MB_CKE0 (8,9), MEM_MB_CKE1 (8,9)

MB_CLK_H[5], MB_CLK_L[5], MB_CLK_H[1], MB_CLK_L[1], MB_CLK_H[7], MB_CLK_L[7], MB_CLK_H[4], MB_CLK_L[4] — P22, R22, A17, A18, AF18, AF17, R26, R25 — MEM_MB0_CLK_H1, MEM_MB0_CLK_L1, MEM_MB0_CLK_H7, MEM_MB0_CLK_L7

MB_ADD[0] … MB_ADD[15] — P24, N24, P26, N23, N26, L23, N25, L24, M26, K26, T26, L26, L25, W24, J23, J24 — MEM_MB_ADD[0..15] (8,9)

MB_BANK[0], MB_BANK[1], MB_BANK[2] — R24, U26, J26 — MEM_MB_BANK0 (8,9), MEM_MB_BANK1 (8,9), MEM_MB_BANK2 (8,9)

MB_RAS_L, MB_CAS_L, MB_WE_L — U25, U24, U23 — MEM_MB_RAS# (8,9), MEM_MB_CAS# (8,9), MEM_MB_WE# (8,9)

SOCKET638

(7,9) MEM_MA0_ODT0, (7,9) MEM_MA0_ODT1 — T19, V22 — MEM_MA1_ODT0, MEM_MA1_ODT1 — U21, V19

(7,9) MEM_MA0_CS#0, (7,9) MEM_MA0_CS#1 — T20, U19, U20, V20

(7,9) MEM_MA_CKE0, (7,9) MEM_MA_CKE1 — J22, J20

MEM_MA0_CLK_H1, MEM_MA0_CLK_L1, MEM_MA0_CLK_H7, MEM_MA0_CLK_L7 — N19, N20, F16, F16, Y16, AA16, P19, P20

(7,9) MEM_MA_ADD[0..15] — MEM_MA_ADD0 … MEM_MA_ADD15 — N21, M20, N22, M19, M22, L20, M24, L21, L19, K22, R21, L22, K20, V24, K24, K19

(7,9) MEM_MA_BANK0, (7,9) MEM_MA_BANK1, (7,9) MEM_MA_BANK2 — R20, R23, J21

(7,9) MEM_MA_RAS#, (7,9) MEM_MA_CAS#, (7,9) MEM_MA_WE# — R19, T22, T24

+1.8V — R0403 1KOhm 1% — CPU_M_VREF — C0403 0.1UF/16V — R0404 1KOhm 1% — GND

sensing point for op-amp feedback routed near CPU

PLACE CLOSE TO CPU

09/23 2.0

+0.9V — c0805_h37 — C0432 10UF/6.3V — C0433 10UF/6.3V — GND

+0.9V — C0434 0.1UF/16V — C0435 0.1UF/16V — C0436 0.1UF/16V — C0437 0.1UF/16V — GND

+0.9V — C0430 0.1UF/16V — C0431 0.1UF/16V — GND

(7) MEM_MA_DQS[0..7]

(7) MEM_MA_DQS#[0..7]

(8) MEM_MB_DQS[0..7]

(8) MEM_MB_DQS#[0..7]

U0301C

MEM:DATA

(8) MEM_MB_DATA[0..63] — MEM_MB_DATA0 … MEM_MB_DATA63 — C11, A11, A14, B14, G11, E11, D12, A13, A15, A16, A19, A20, C14, D14, C18, D18, D20, A21, D24, C25, B20, C20, B24, C24, E23, E24, G25, G26, C26, D26, G23, G24, AA24, AA23, AD24, AE24, AA26, AA25, AD26, AE25, AC22, AD22, AE20, AF20, AE24, AF23, AC20, AD20, AD18, AE18, AC14, AD14, AF19, AC18, AF16, AF15, AF13, AC12, AB11, Y11, AE14, AF14, AF11, AD11

(8) MEM_MB_DM[0..7] — MEM_MB_DM0 … MEM_MB_DM7 — A12, B16, A22, E25, AB26, AE22, AC16, AD12

MEM_MB_DQS0 … MEM_MB_DQS#7 — C12, B12, D16, C16, A24, A23, F26, E26, AC25, AC26, AF21, AF22, AE16, AD16, AF12, AE12

MB_DATA[0] … MB_DATA[63] — MA_DATA[0] … MA_DATA[63]

MB_DM[0] … MB_DM[7] — MA_DM[0] … MA_DM[7]

MB_DQS_H[0], MB_DQS_L[0], MB_DQS_H[1], MB_DQS_L[1], MB_DQS_H[2], MB_DQS_L[2], MB_DQS_H[3], MB_DQS_L[3], MB_DQS_H[4], MB_DQS_L[4], MB_DQS_H[5], MB_DQS_L[5], MB_DQS_H[6], MB_DQS_L[6], MB_DQS_H[7], MB_DQS_L[7] — MA_DQS_H[0], MA_DQS_L[0], MA_DQS_H[1], MA_DQS_L[1], MA_DQS_H[2], MA_DQS_L[2], MA_DQS_H[3], MA_DQS_L[3], MA_DQS_H[4], MA_DQS_L[4], MA_DQS_H[5], MA_DQS_L[5], MA_DQS_H[6], MA_DQS_L[6], MA_DQS_H[7], MA_DQS_L[7]

SOCKET638

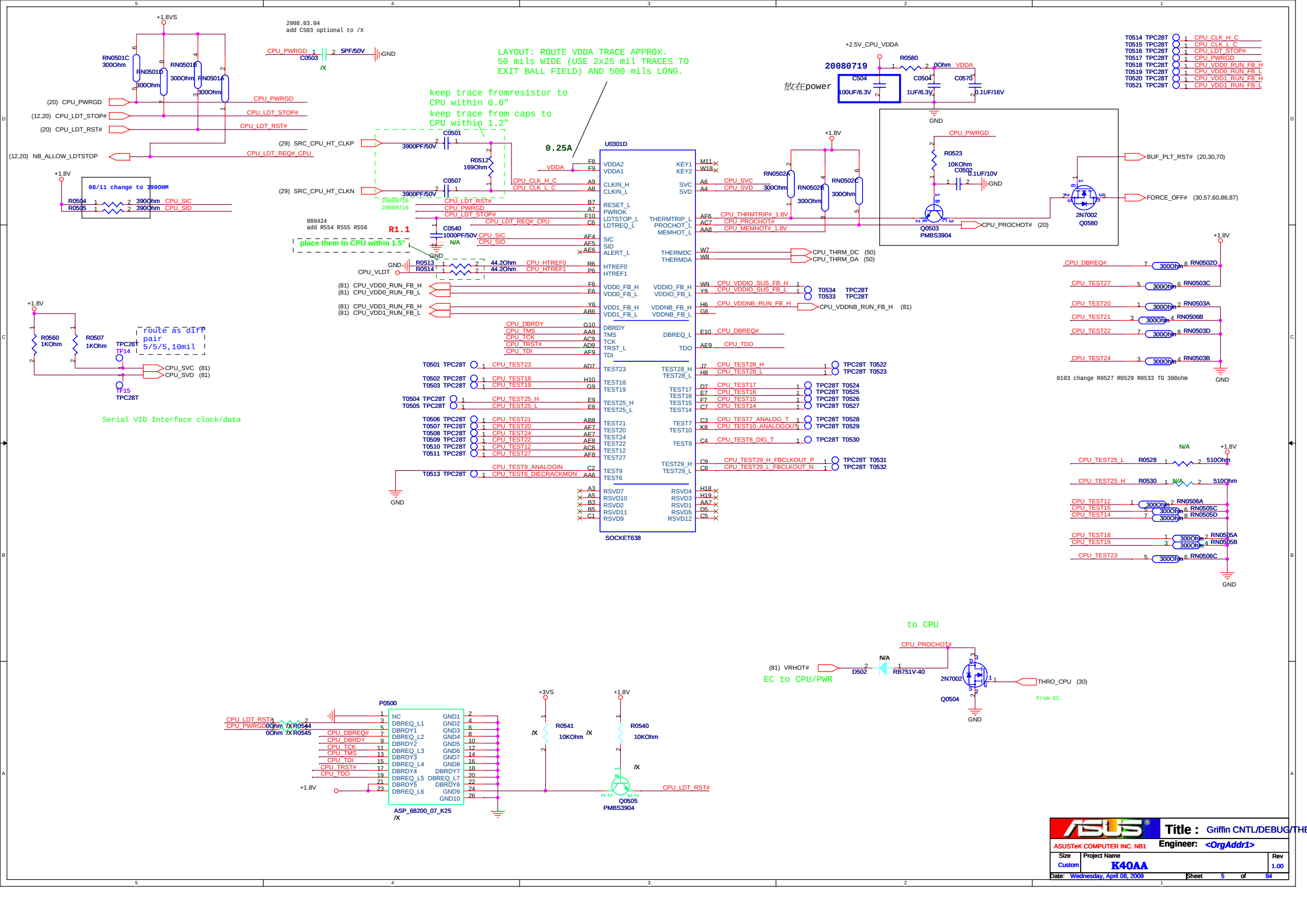
To SODIMM socket 1

To SODIMM socket 0

MEM_MA_DATA[0..63] (7) — G12, F12, H14, G14, H11, H12, C13, E13, H15, E15, E17, H17, E14, F14, C17, G17, G18, C19, D22, E20, E18, B22, C23, F20, F22, H24, J19, E21, F22, H20, H22, Y24, AB24, AB22, AA21, W22, W21, Y22, AA22, Y20, AA20, AA18, B18, AB21, AD21, AD19, Y18, AD17, W16, W14, Y14, Y17, AB17, AB15, AD15, AB13, AD13, Y12, W11, AB14, AA14, AB12, AA12

MEM_MA_DM[0..7] (7) — E12, C15, E19, F24, AC24, Y19, AB16, Y13

MEM_MA_DQS0 … MEM_MA_DQS#7 — G13, H13, G16, G15, C22, C21, G22, G21, AD23, AC23, AB19, AB20, Y15, W15, W12, W13



ASUSTeK COMPUTER INC. NB1	Title : Griffin CNTL/DEBUG/THE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
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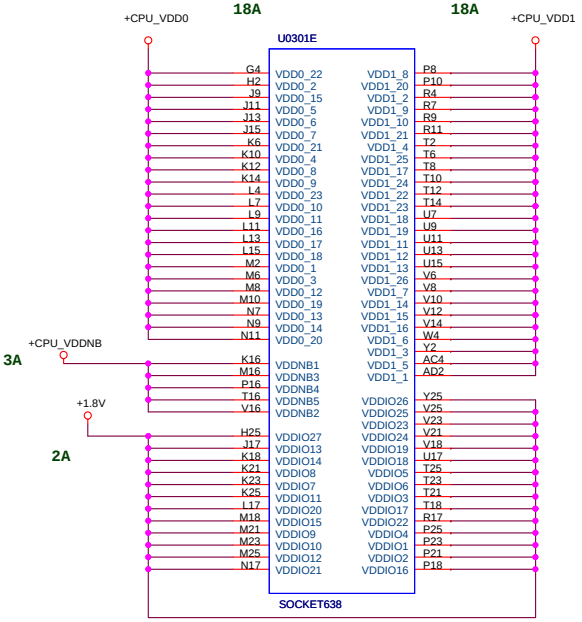
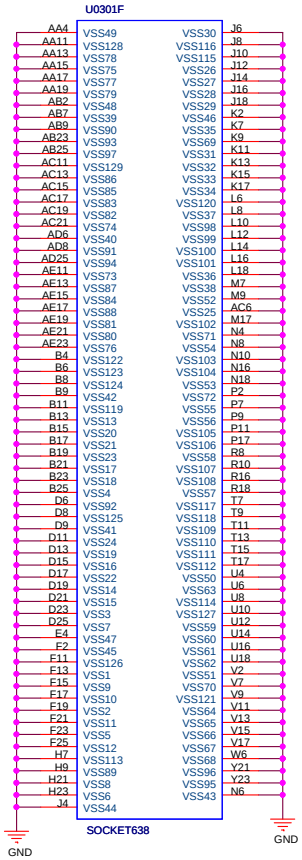
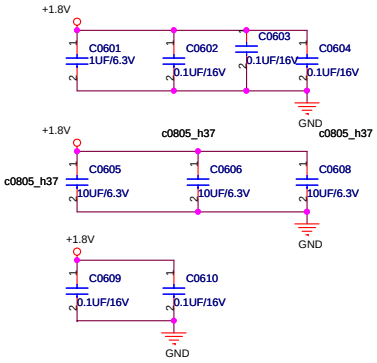


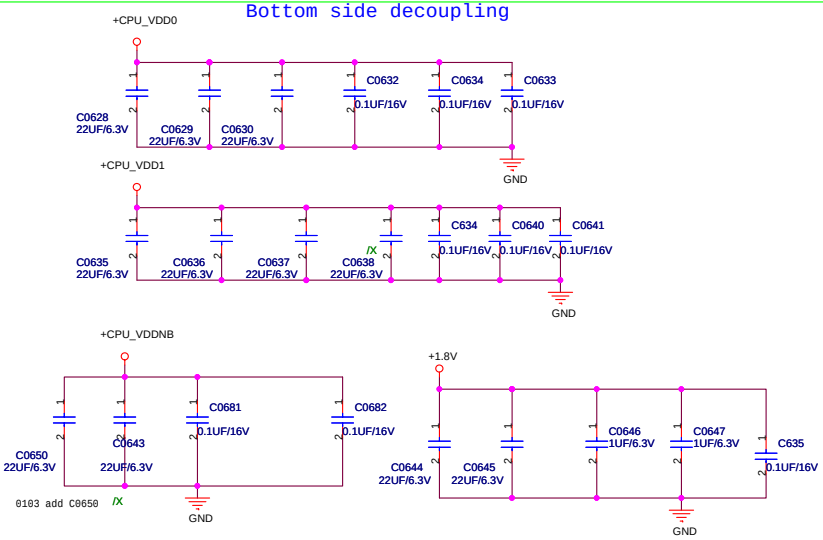


Decoupling between Processor and DIMMs, Place close to Porcessor as possible



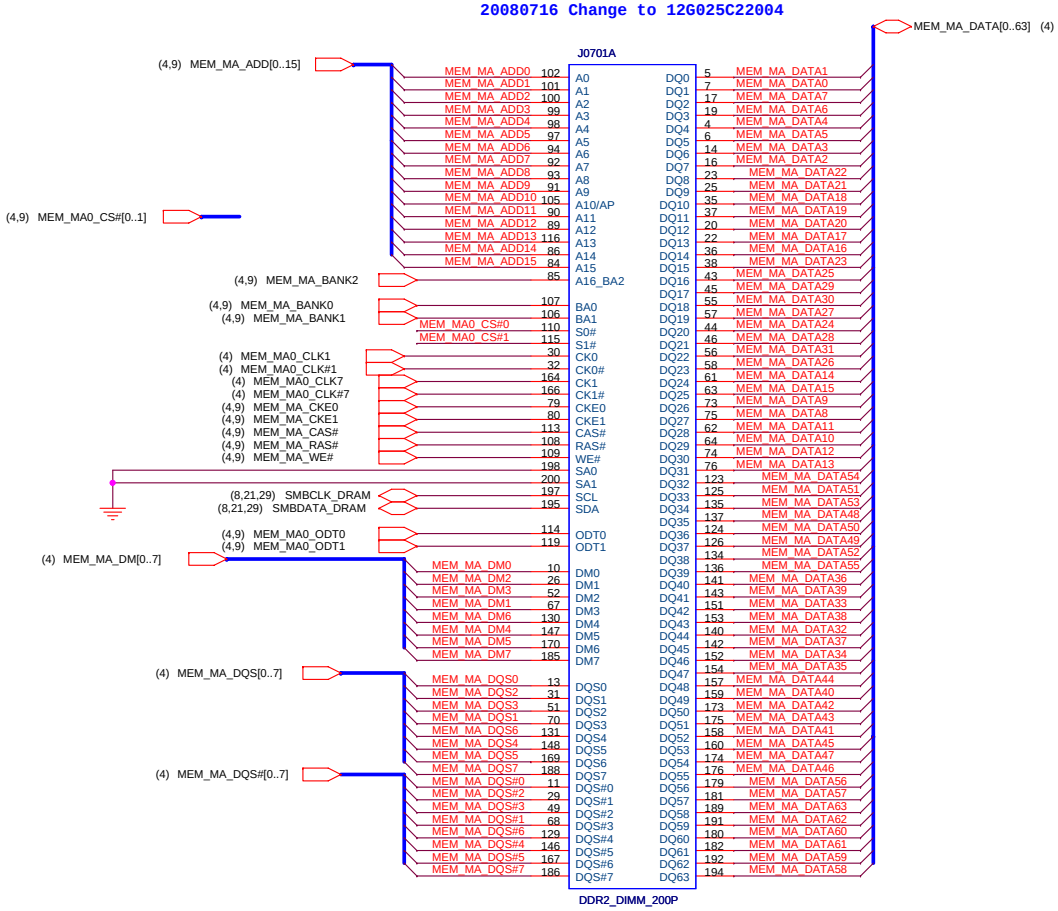
place close to socket

Bottom side decoupling

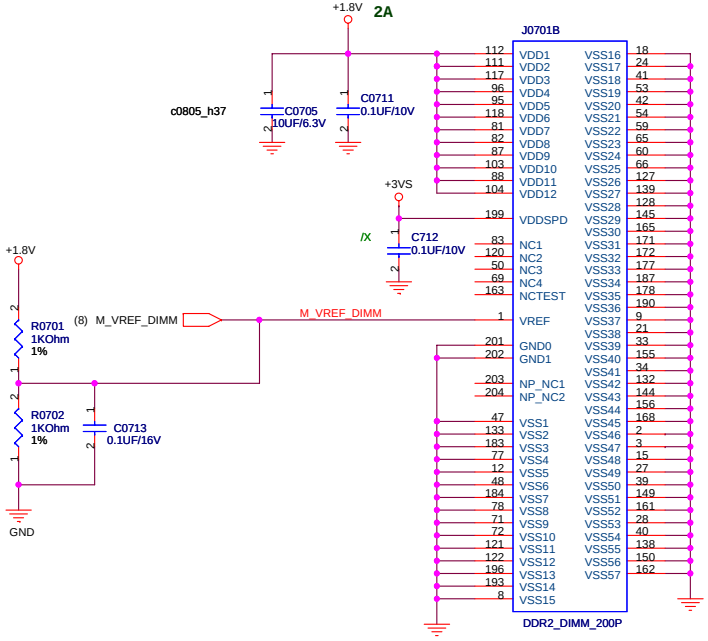


ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 6 of 94	

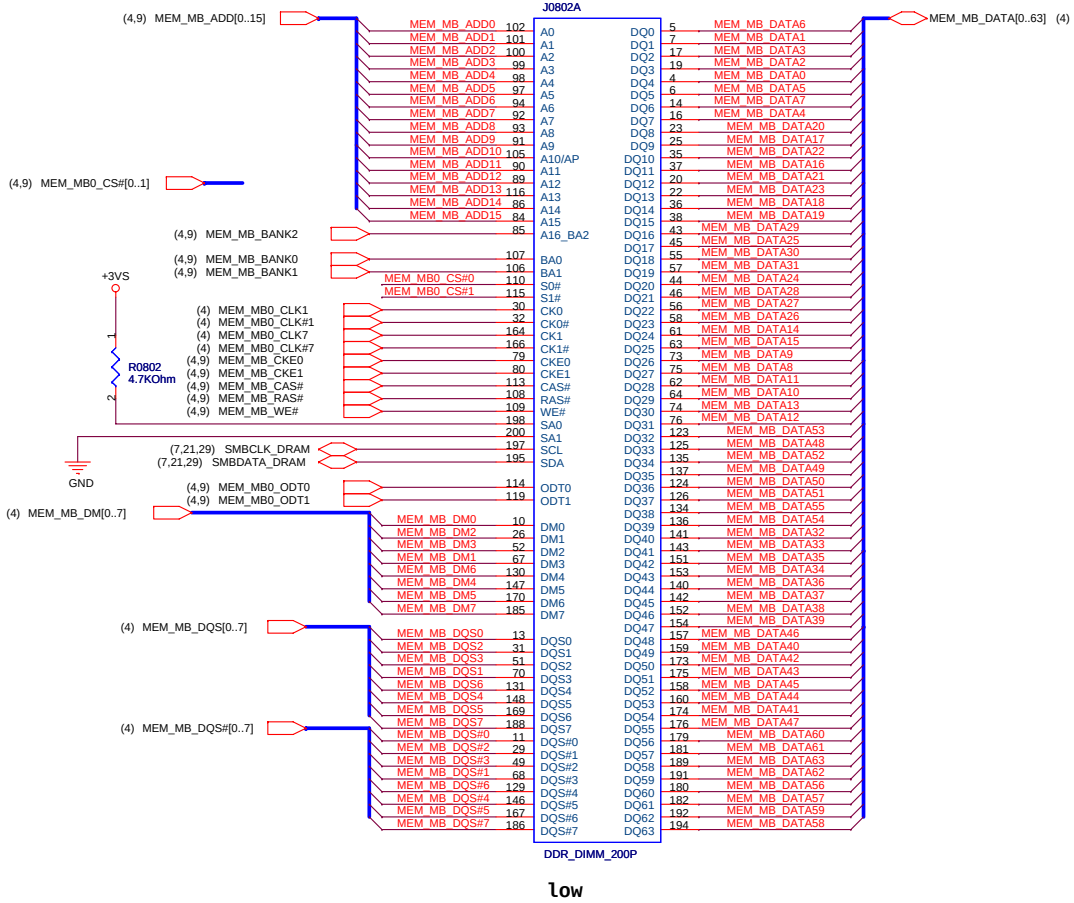
20080716 Change to 12G025C22004

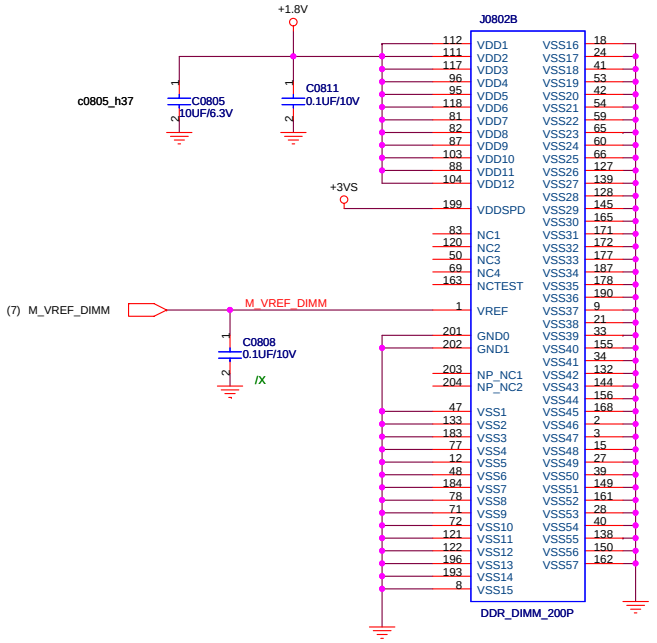


High

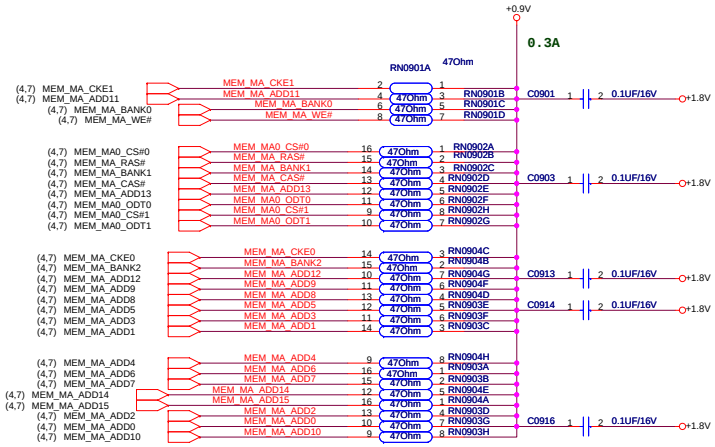


ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 7 of 94	

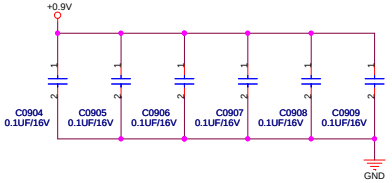


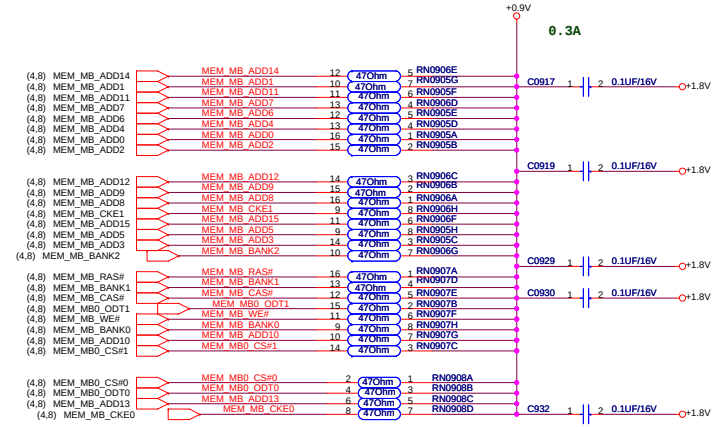


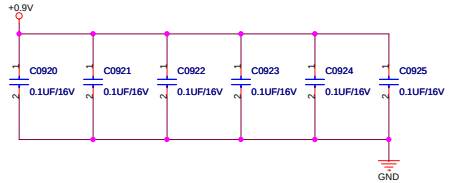
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 8 of 94	

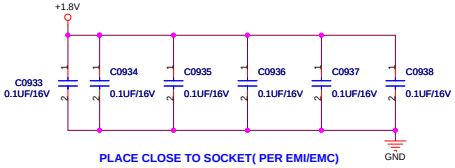


20080803 Remove R907









PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC. NB1	Title : DDR2_TERMINATIONS	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
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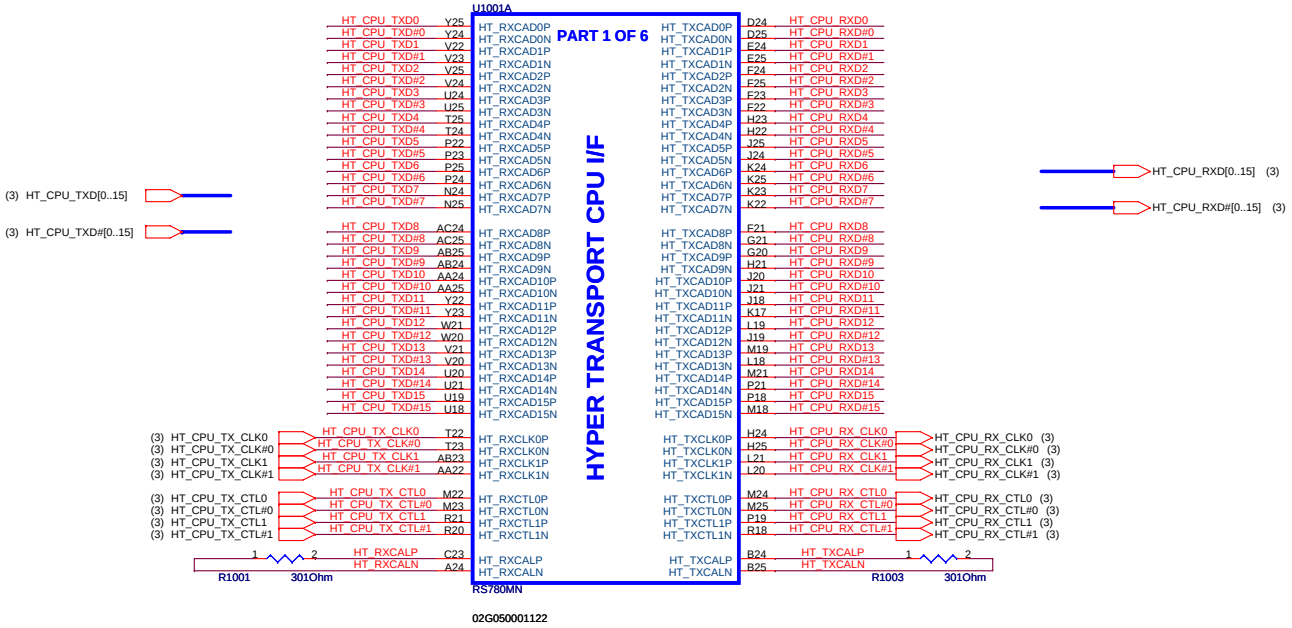
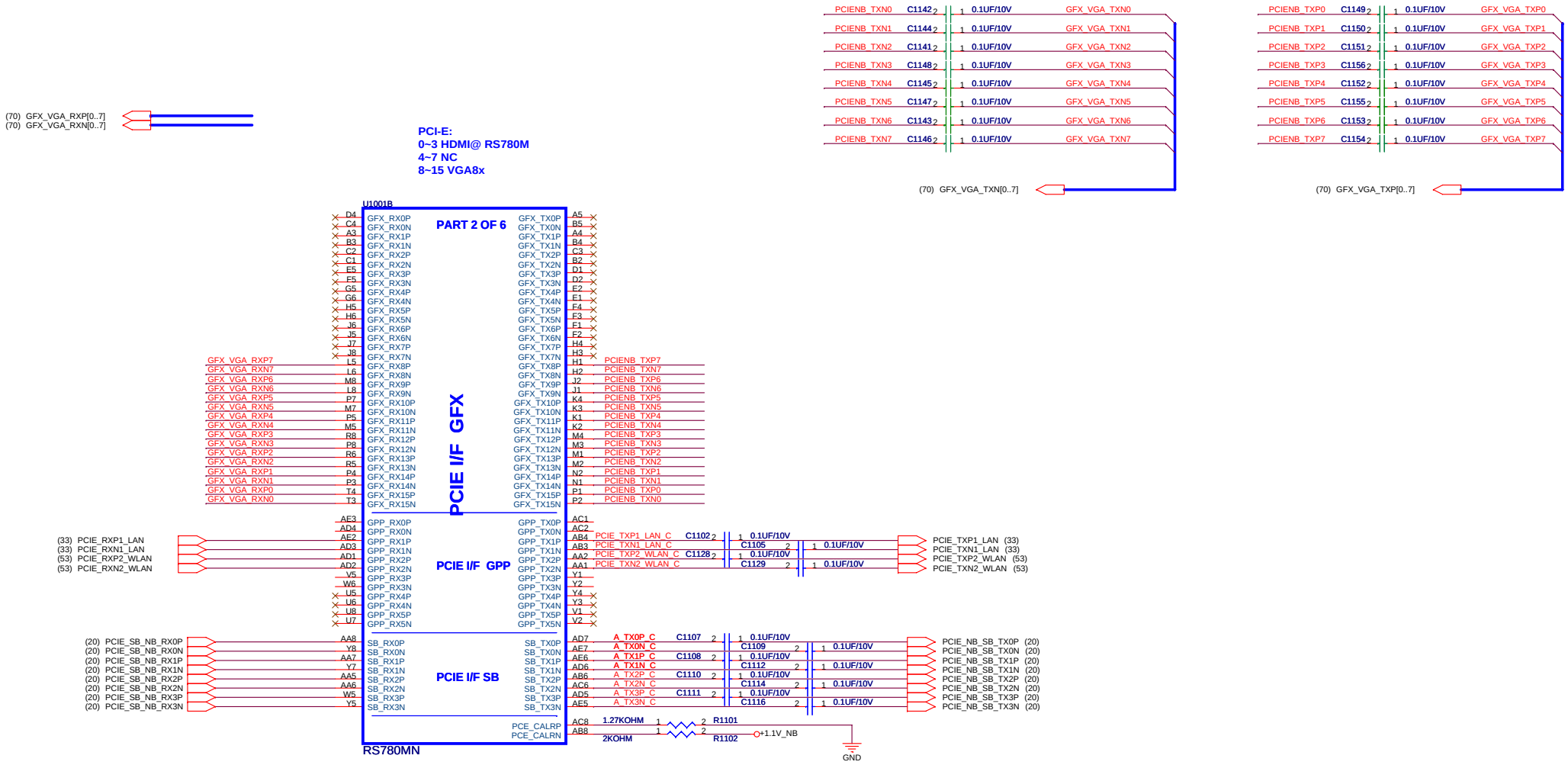
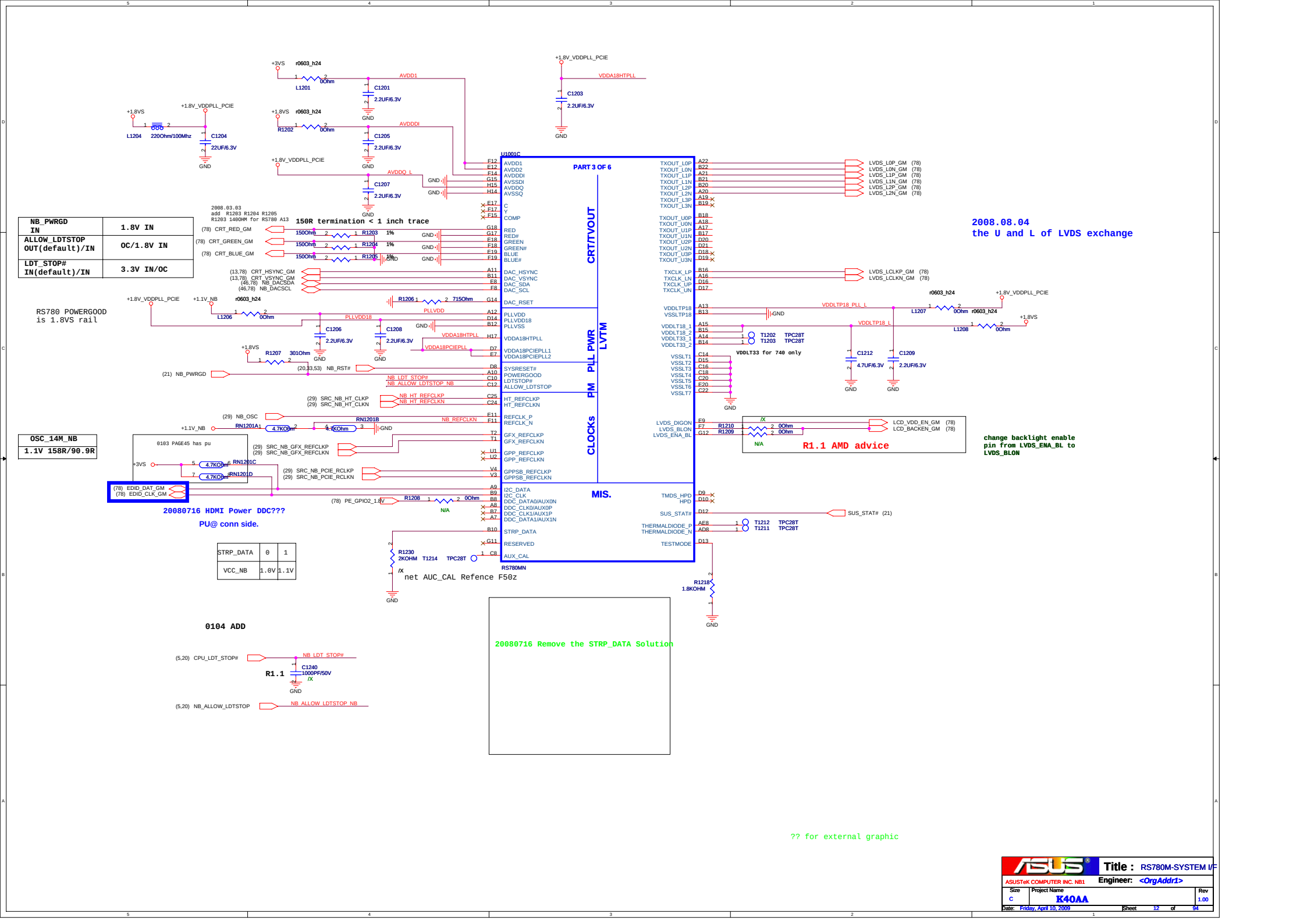


02G050001122

ASUSTeK COMPUTER INC. NB1	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 10 of 94	



ASUSTeK COMPUTER INC. NB1	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 11 of 94		



NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

RS780 POWERGOOD is 1.8VS rail

OSC_14M_NB
1.1V 158R/90.9R

0103 PAGE45 has pu

2008.03.03
add R1203 R1204 R1205
R1203 1480HM for RS780 A13

150R termination < 1 inch trace

20080716 HDMI Power DDC???

PU@ conn side.

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

net AUC_CAL Refence F50z

0104 ADD

R1.1

20080716 Remove the STRP_DATA Solution

2008.08.04
the U and L of LVDS exchange

change backlight enable pin from LVDS_ENA_BL to LVDS_BLON

R1.1 AMD advice

?? for external graphic

Title : RS780M-SYSTEM I/F		
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: C	Project Name: K40AA	Rev: 1.00
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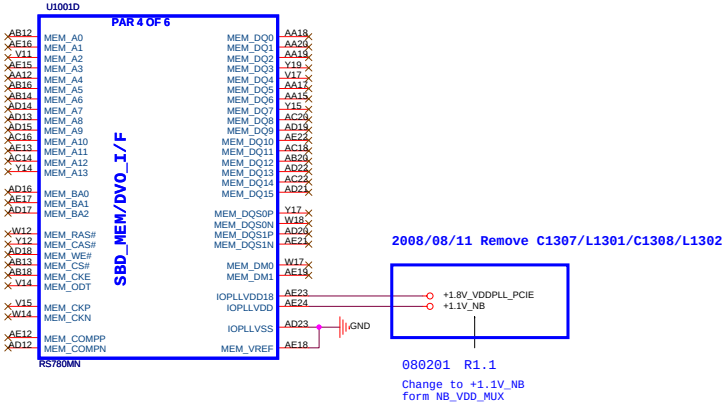
R1.11 080319

Change the NB Part number to RS780 (A13)



2008/08/11 Remove C1307/L1301/C1308/L1302

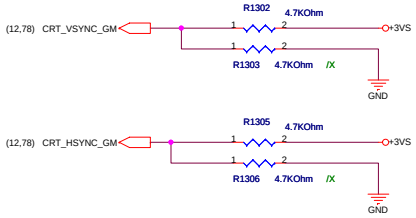
080201 R1.1

Change to +1.1V_NB
form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

ASUSTeK COMPUTER INC. NB1

Title : RS780M-SPMEM/STRAPS

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	K40AA	1.00

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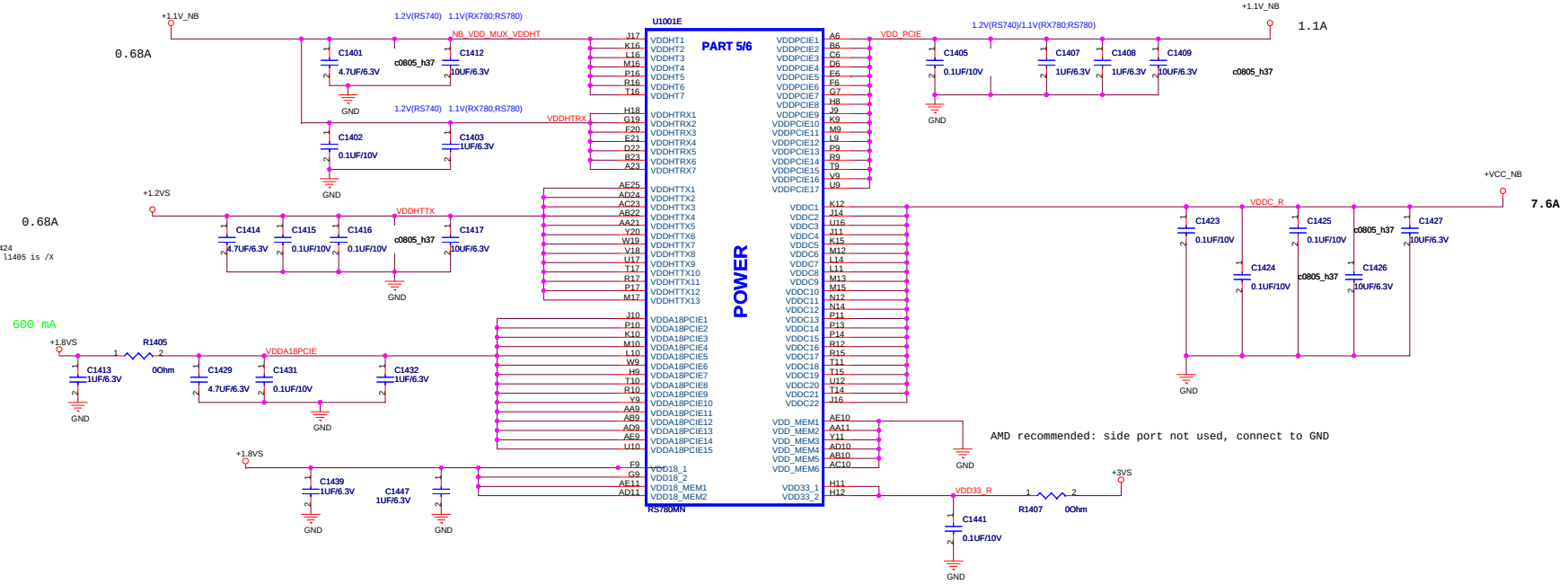


ASUSTeK COMPUTER INC. NB1	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 14 of 94		

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: *<OrgAddr1>*
Size: A	Project Name: **K40AA**
	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 15 of 94

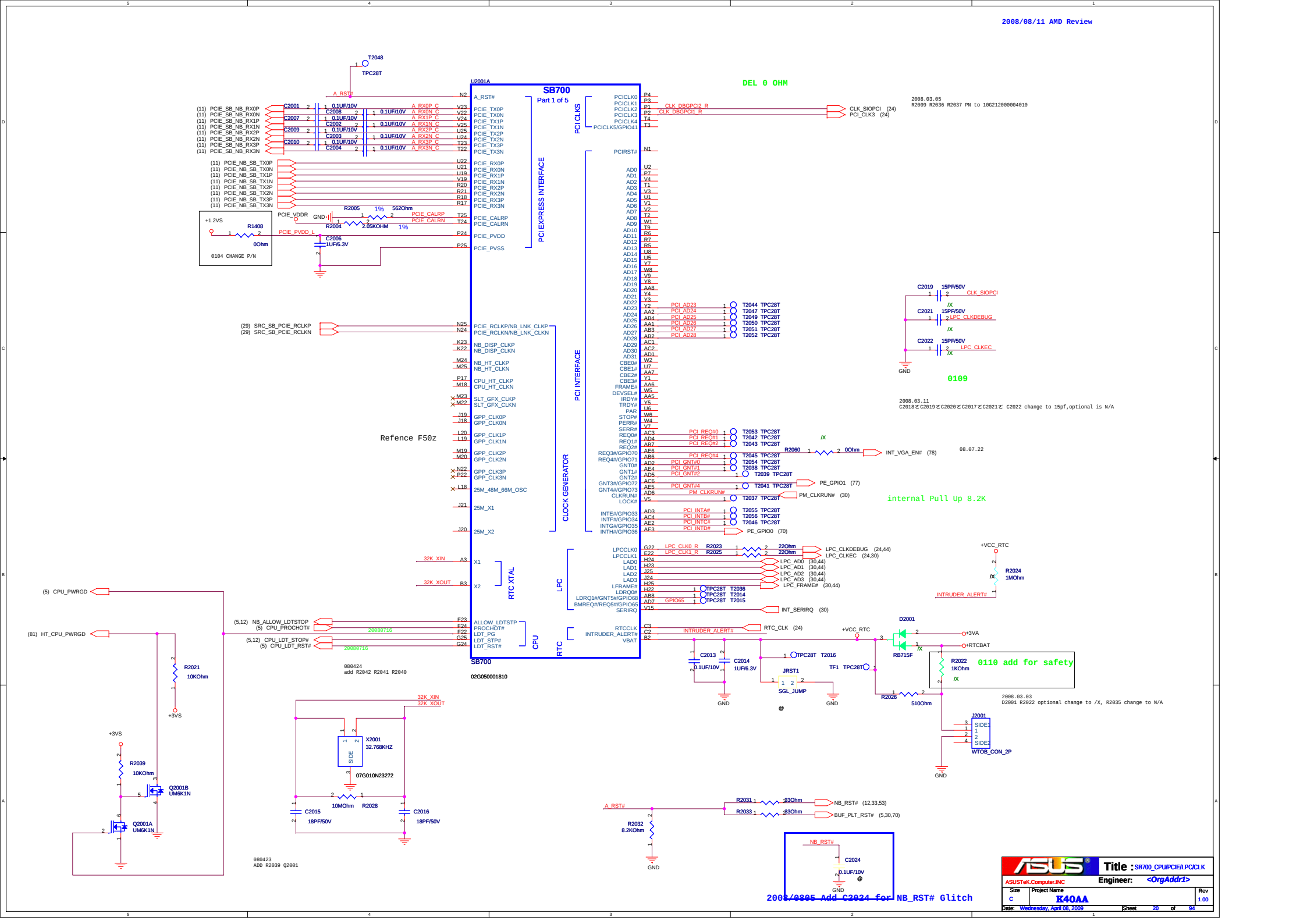
ASUSTeK COMPUTER INC	Title : BLANK			
	Engineer:			
Size: A	Project Name: K40AA			Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 16 of 94			

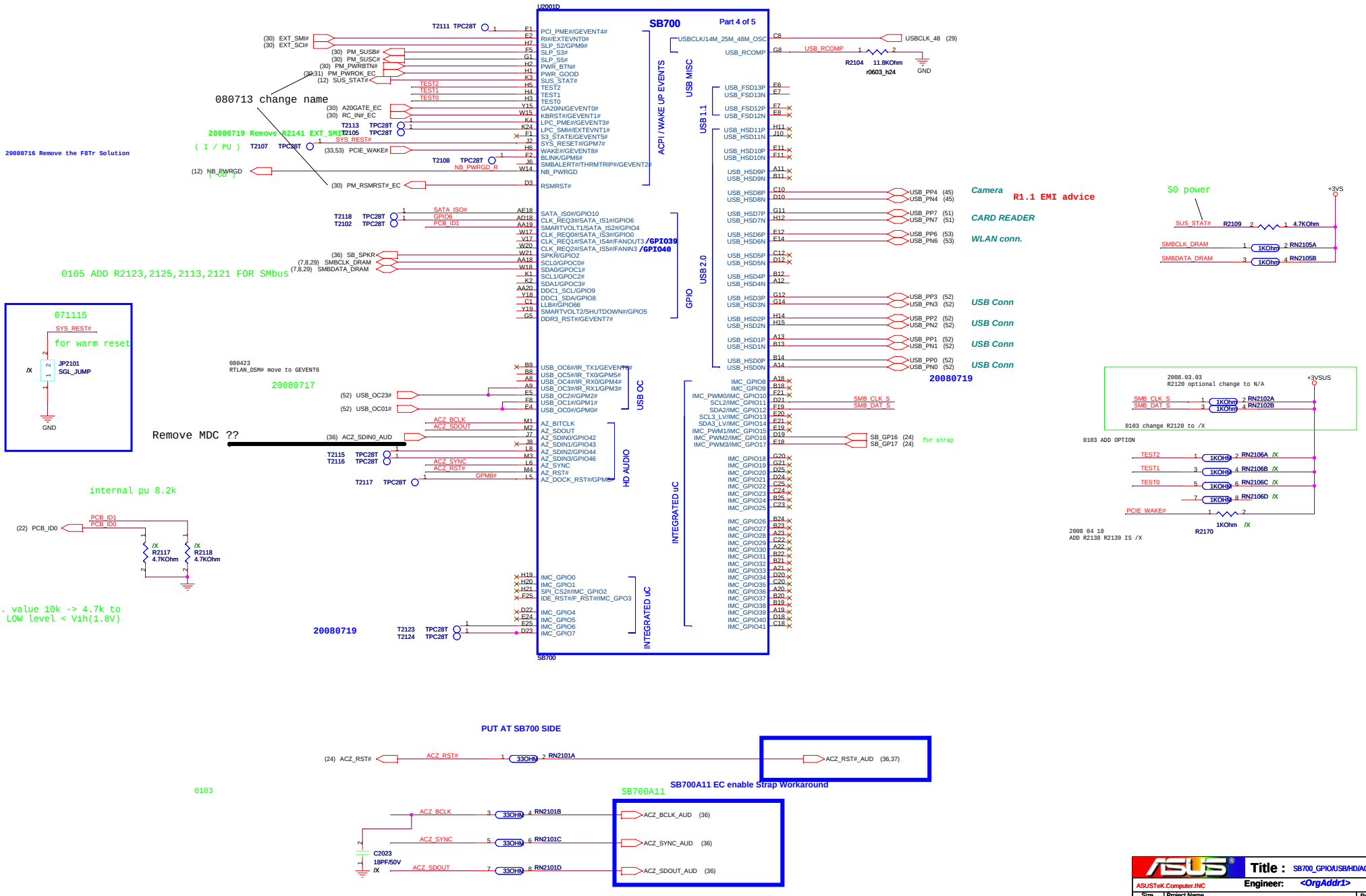
Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 17 of 94

ASUS	Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:		
Size A	Project Name **K40AA**		Rev 1.00
Date: Wednesday, April 08, 2009	Sheet 18 of 94		

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 19 of 94

2008/08/11 AMD Review





ASUSTeK.COMPUTER.INC	Title :	SB700_GPIO/USB/HD/ACPI	
	Engineer:	<OrgAddr1>	
Size: C	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 21 of 94		

2008.03.03
R2208 R2209 R2210 R2211 R2212 R2213 from 4.99OHM to 0OHM

2008/08/11 Remove R2208/R2209/R2210/R2211/R2212/R2213

for SATA HDD

for SATA ODD

(51) SATA_TXP0_HDD
(51) SATA_TXN0_HDD
(51) SATA_RXN0_HDD
(51) SATA_RXP0_HDD
(51) SATA_TXP1
(51) SATA_TXN1
(51) SATA_RXN1
(51) SATA_RXP1

U2001B

SB700
Part 2 of 5

SERIAL ATA
SATA_TX0P AD9
SATA_TX0N AE9
SATA_RX0N AB10
SATA_RX0P AC10
SATA_TX1P AE10
SATA_TX1N AD10
SATA_RX1N AD11
SATA_RX1P AE11
SATA_TX2P AB12
SATA_TX2N AC12
SATA_RX2N AE12
SATA_RX2P AD12
SATA_TX3P AD13
SATA_TX3N AE13
SATA_RX3N AB14
SATA_RX3P AC14
SATA_TX4P AE14
SATA_TX4N AD14
SATA_RX4N AD15
SATA_RX4P AE15
SATA_TX5P AB16
SATA_TX5N AC16
SATA_RX5N AE16
SATA_RX5P AD16

ATA 66/100/133
IDE_IORDY AA24
IDE_IRQ AA25
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE23
IDE_D3/GPIO18 AC23
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM
SPI_DI/GPIO12 G6
SPI_DO/GPIO11 D2
SPI_CLK/GPIO47 D1
SPI_HOLD#/GPIO31 F4
SPI_CS1#/GPIO32 F3
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

WLAN_ON (53)
WLAN_ON#----> WLAN_ON

FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
PCB_ID0 (21)

FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8

HW MONITOR
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

SATA PWR
SATA_ACT#/GPIO67 W11
PLLVDD_SATA AA11
XTLVDD_SATA W12

SATA_CAL V12
SATA_X1 Y12
SATA_X2 AA12

AVDD F6
AVSS G7

SB700

Place SATA_CAL
RES very close
to ball of SB700

R2201 1KOhm 1% SATA_CAL
GND

SATA_X1
R2205 10MOhm
SATA_X2
(31) SATA_LED#
X2201 25Mhz
PLLVDD_SATA
XTLVDD_SATA
C2209 27PF/50V N/A
C2210 27PF/50V N/A
GND

+1.2VS
+1.2VS_SATA
R2207 0Ohm
R2250 0Ohm /X
PLLVDD_SATA
C2211 1UF/10V
C2213 0.1UF/10V
R1.1

080423
C2211 C2212 TO 2.2U(0603)

+3VS
XTLVDD_SATA
C2217 0.1UF/10V
C2216 close
to the ball
of SB700

TEMP_COMM
GPIO61
T2228 TPC28T
TEMPIN_NB
T2229 TPC28T
GPIO63
R2218 0Ohm /X
OS#_OC (30,50)
GPIO64
T2231 TPC28T /X

GPIO53
T2232 TPC28T
GPIO54
L_ISOLATE# (33)
WLAN_LED_ON (56)

GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！

AVDD_HWM
+3VSUS
C2214 0.1UF/16V /X
GND

GND trace at
least 10mil
wide

WLAN_LED_ON
R2202 10KOhm
GND

TEMP_COMM
GND

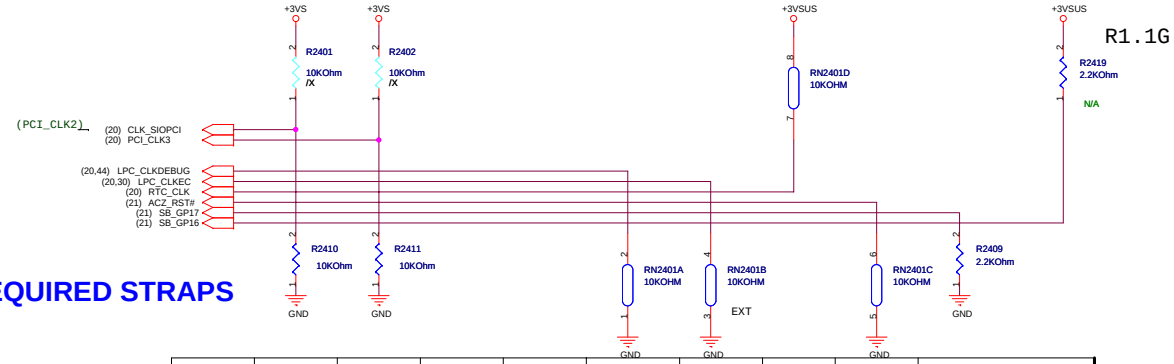
ASUSTeK.COMPUTER.INC

Title : SB700_PATA/SATA
Engineer: <OrgAddr1>

Size	Project Name	Rev
C	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 22 of 94

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	32-kHz clock ENABLED	INTERNAL RTC DEFAULT	Integrated Microcontroller ENABLED	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	32-kHz clock DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	Integrated Microcontroller DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

ASUSTeK.Computer.INC	Title : SB700_STRAP	
	Engineer: <OrgAddr1>	
Size: C	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 24 of 94	

Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

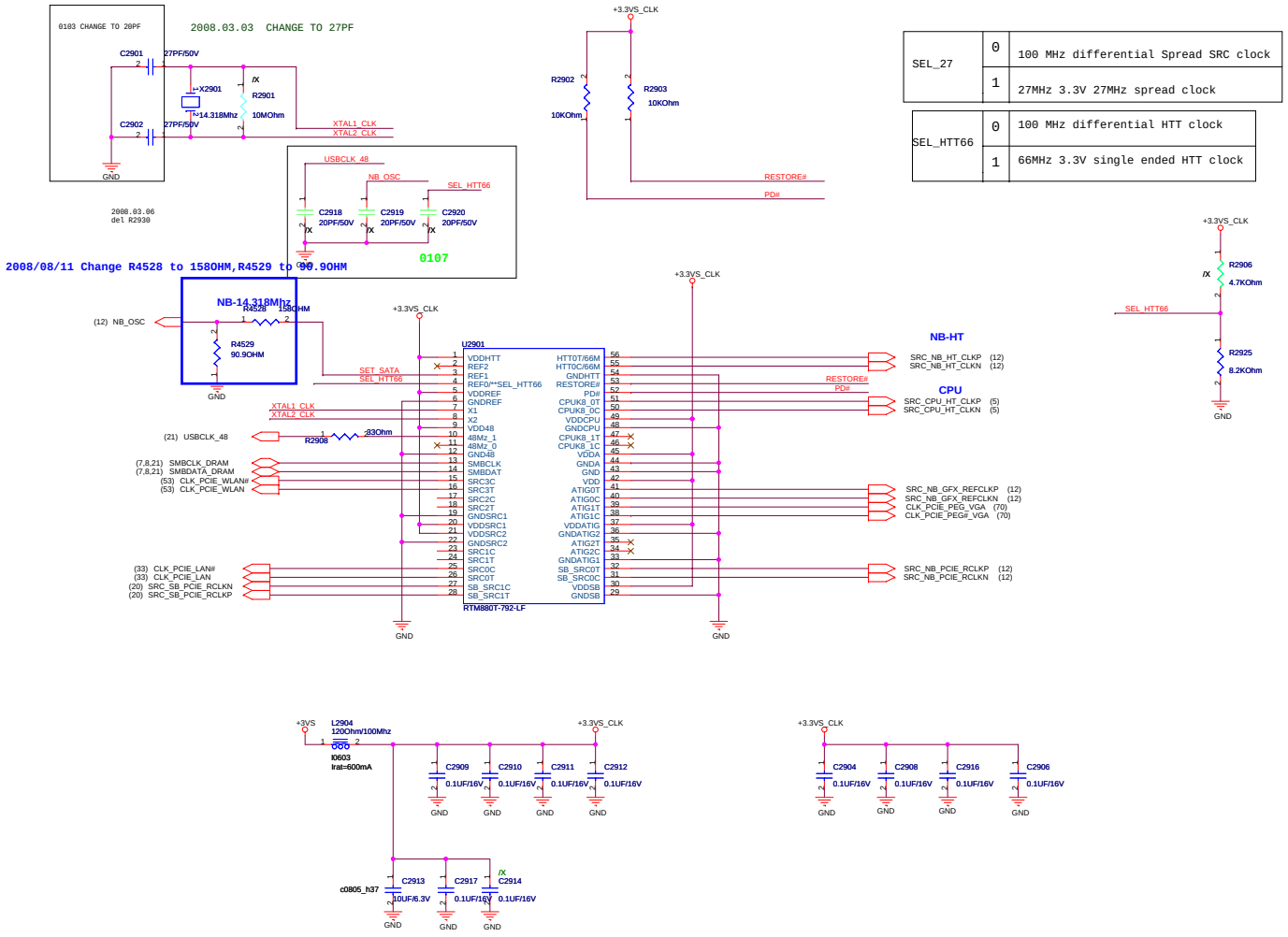
Size	Project Name	Rev
A	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 25 of 94

ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 26 of 94	

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 27 of 94		

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 28 of 94		



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICS9LPRS489AGLFT

Engineer:

Size	Project Name	Rev
A2	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 29 of 94

R2.05

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

080131 R1.1
Check EC power

080130
R1.1
Change EC from IT8752 to IT8512

080712

080712 Internet

080712

080712

080712

080712

080712

080712

U3001
IT8512E-L

LPC
FLASH-ROM
KBMX
GPIO
PS/2
SMBus

R2.0 080401
Un-mount C3018 for ITE suggestion

080204 R1.1
IT8512 I~J

U3003
SST25VF080B
(8Mb)

For IT8512 Power

R2.01 080411
Change P/N to
09G013120103

R2.0 080327
Add test point for
factory ICT test

For PU / PD

080215 R1.1
change 4.7K P/N from
10G2124720040 to
10G2124720040

Change pull up resistor
from 10K to 47K ohm

071115

R1.1G

080215 change P/N

Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R2.0 080327
Follow the design IP

11/05

For Instant Key

Note: Close to EC

080713 Add Coloren#

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

071116
Reserve for current leakage
issue (Reference to F5R)

R3008 33Ohm
R3010 33Ohm

071129

R2.02 080519
Un-Mount R3059 and
Q3002 for cost down

071207
AMD review

Q3002
BSS138

080713 ?????

EC Check (AC Auto Boot Issue)

071113
Change Net name
from PM_RSMRST#

080123 R1.1
D3002 1SS355
1KOhm R3052 @

071113
Change Net name
from PM_RSMRST#_EC

PM_RSMRST#

(21) PM_RSMRST#_EC

(21,31) PM_PWROK_EC

071113
Change Net name
from PM_PWROK

R3054 10KOhm

071203

071203
refer page31.

071116
Reserve "Auto power on"
solution for ATI Chipset

PM_PWROK

071113
Change Net name
from PM_PWROK_EC

ASUSTeK COMPUTER INC. NB1

Title : EC_IT8512 (1/2)

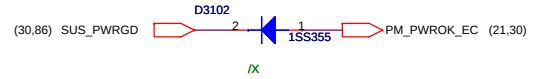
Engineer: <OrgAddr1>

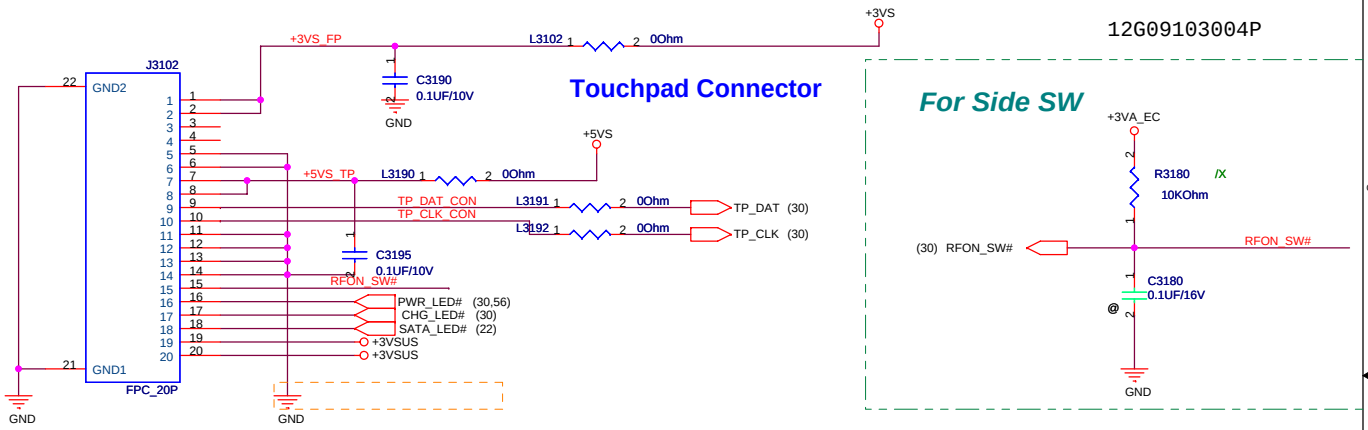
Size	Project Name	Rev
Custom	K40AA	1.00

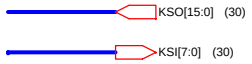
Date: Wednesday, April 08, 2009 Sheet 30 of 94

close to connector

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present.
Need to add bidirectional diode to protect this pin.



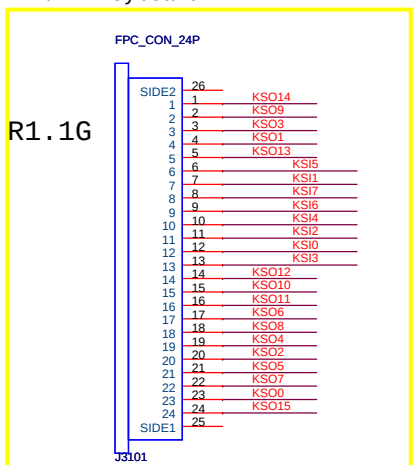




Keyboard Connector

F7/N1 Keyboard

R1.1G



12G182102402

11/02

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512 (2/2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 31 of 94	

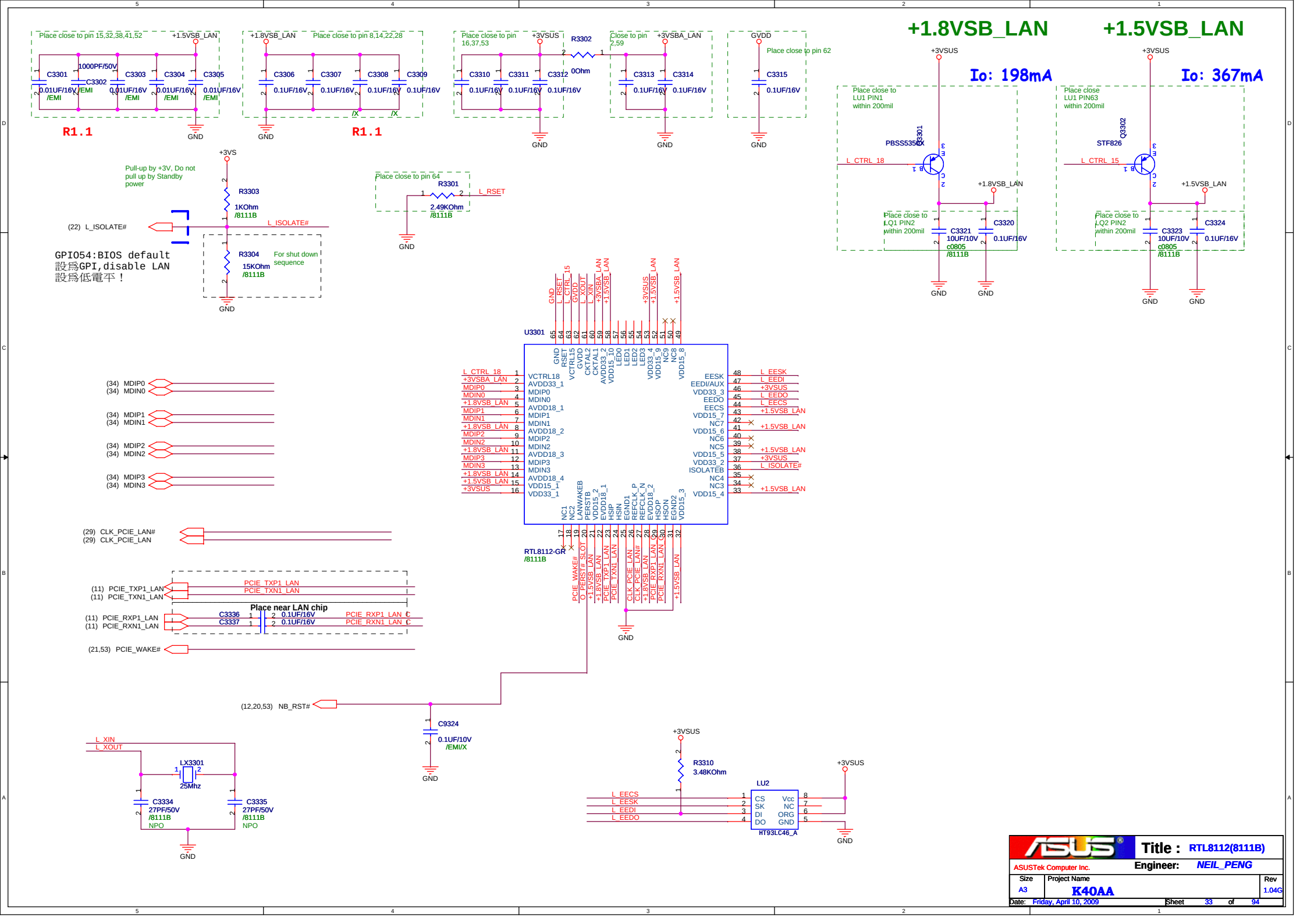
Title : POWER-ON SEQUENCE

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 32 of 94


+1.8VSB_LAN
+1.5VSB_LAN
Io: 198mA
Io: 367mA
R1.1
R1.1
Place close to pin 15,32,38,41,52
+1.5VSB_LAN
C3301
1000PF/50V
C3302
C3303
C3304
C3305
0.01UF/16V /EMI
+1.8VSB_LAN
Place close to pin 8,14,22,28
C3306
C3307
C3308
C3309
0.1UF/16V
/X
Place close to pin 16,37,53
+3VSUS
R3302
0Ohm
C3310
C3311
C3312
0.1UF/16V
Close to pin 2,59
+3VSBA_LAN
C3313
C3314
GVDD
Place close to pin 62
C3315
GND
Pull-up by +3V, Do not pull up by Standby power
+3VS
R3303
1KOhm
/8111B
(22) L_ISOLATE#
L_ISOLATE#
R3304
15KOhm
/8111B
For shut down sequence
GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！
Place close to pin 64
R3301
2.49KOhm
/8111B
L_RSET
Place close to LU1 PIN1 within 200mil
Q3301
PBSS5350X
L_CTRL_18
C3321
10UF/10V
c0805
/8111B
C3320
0.1UF/16V
Place close to LQ1 PIN2 within 200mil
Place close to LU1 PIN63 within 200mil
Q3302
STF826
L_CTRL_15
C3323
10UF/10V
c0805
/8111B
C3324
0.1UF/16V
Place close to LQ2 PIN2 within 200mil
U3301
RTL8112-GR
/8111B
(34) MDIP0
(34) MDIN0
(34) MDIP1
(34) MDIN1
(34) MDIP2
(34) MDIN2
(34) MDIP3
(34) MDIN3
(29) CLK_PCIE_LAN#
(29) CLK_PCIE_LAN
(11) PCIE_TXP1_LAN
(11) PCIE_TXN1_LAN
Place near LAN chip
C3336
C3337
0.1UF/16V
(11) PCIE_RXP1_LAN
(11) PCIE_RXN1_LAN
(21,53) PCIE_WAKE#
(12,20,53) NB_RST#
C9324
0.1UF/10V
/EMI/X
L_XIN
L_XOUT
LX3301
25Mhz
C3334
27PF/50V
/8111B
NPO
C3335
27PF/50V
/8111B
NPO
R3310
3.48KOhm
LU2
HT93LC46_A
L_EECS
L_EESK
L_EEDI
L_EEDO
Title : RTL8112(8111B)
ASUSTek Computer Inc.
Engineer: NEIL_PENG
Size A3
Project Name K40AA
Rev 1.04G
Date: Friday, April 10, 2009
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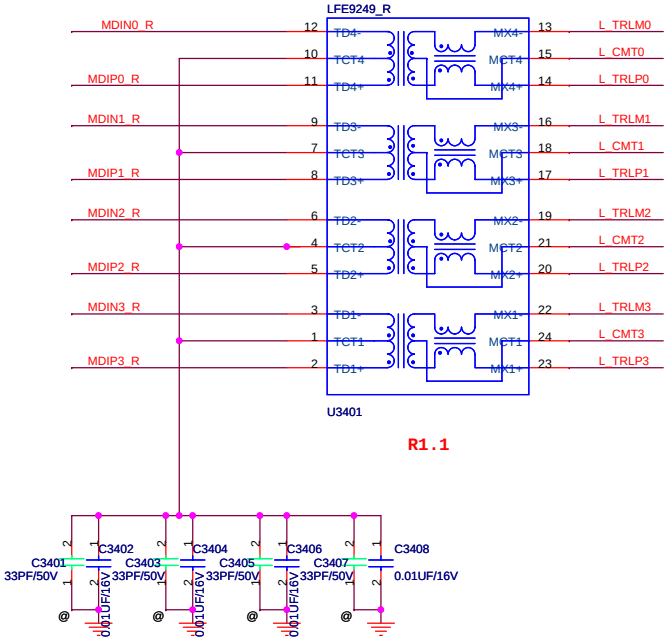
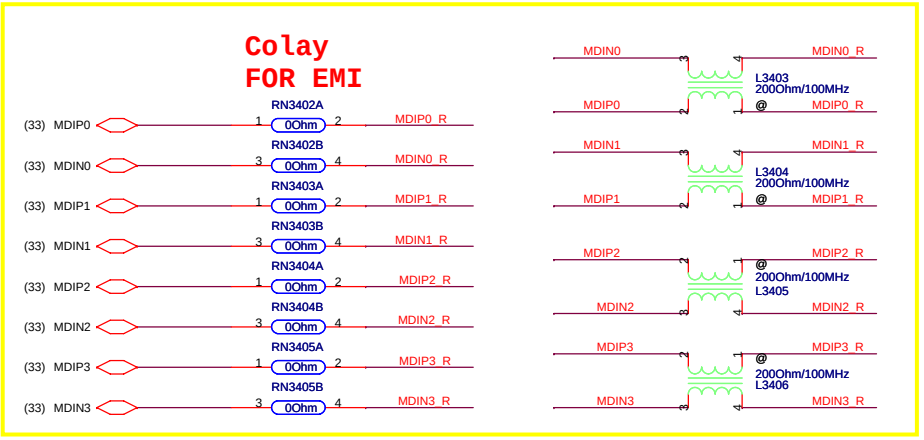
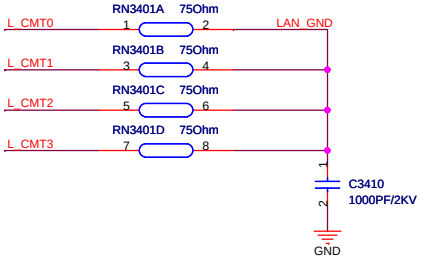
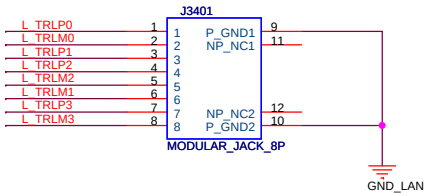
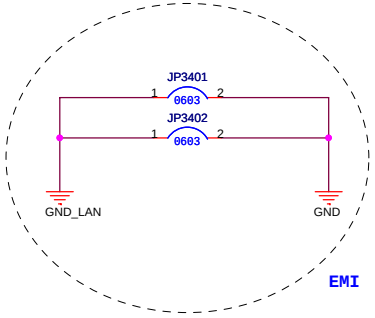




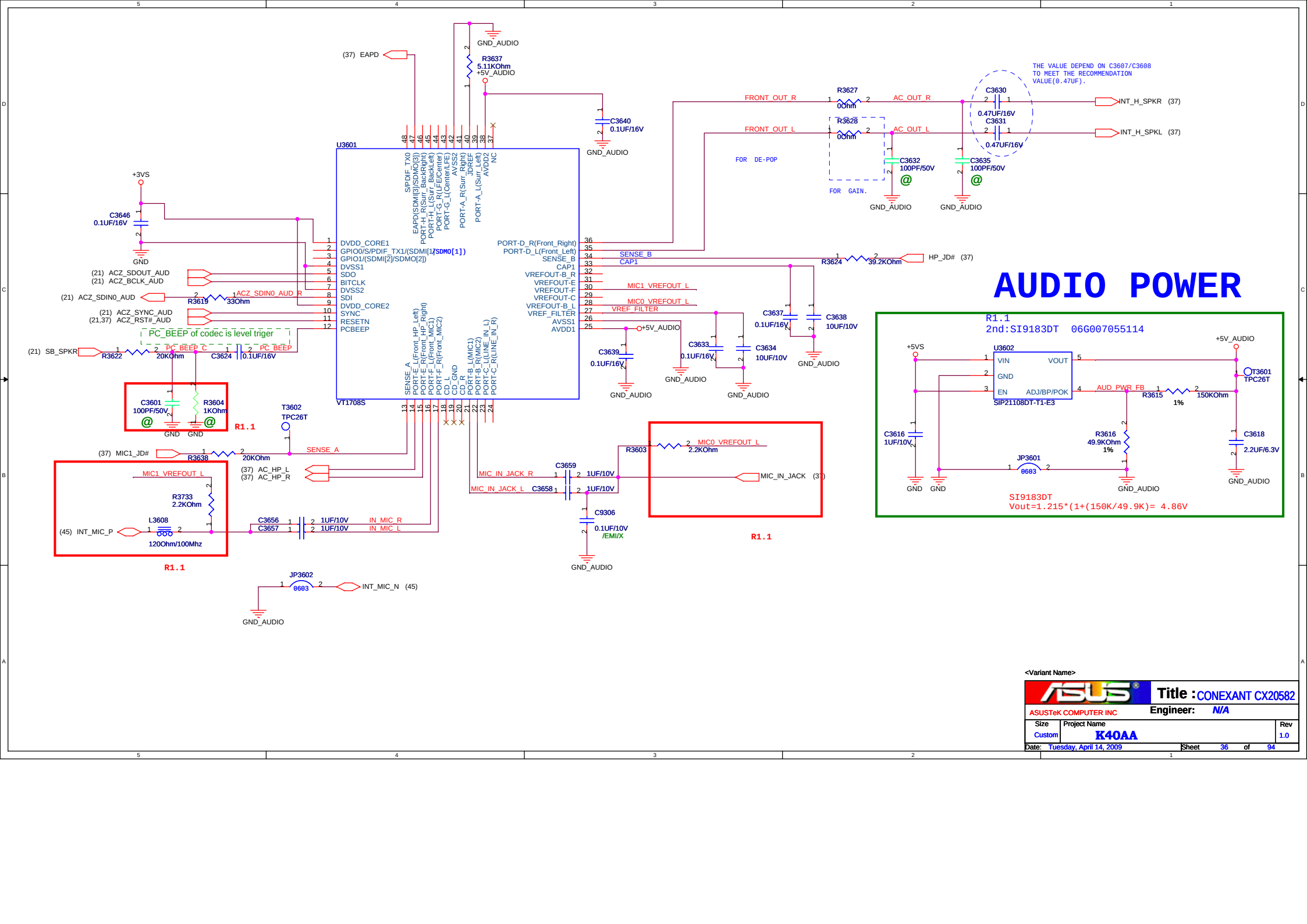




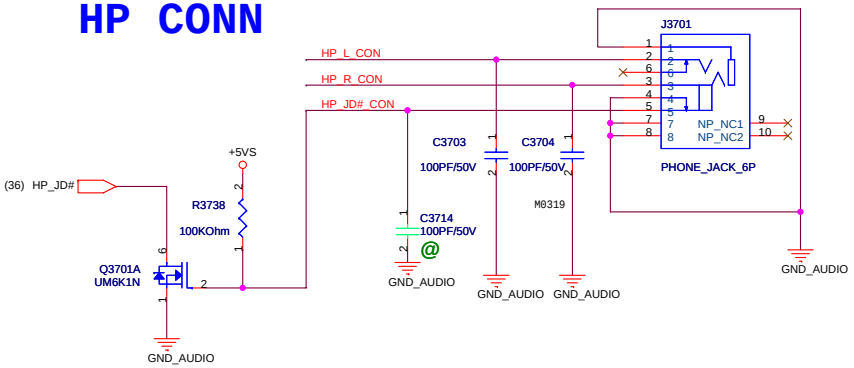


ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 34 of 94	

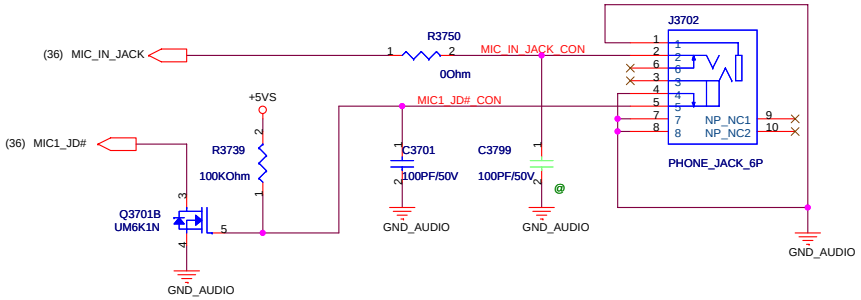
Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 35 of 94


AUDIO POWER
U3601
VT1708S
DVDD_CORE1
GPIO0/S/PDIF_TX1/(SDMI[1]/SDMO[1])
GPIO1/(SDMI[2]/SDMO[2])
DVSS1
SDO
BITCLK
DVSS2
SDI
DVDD_CORE2
SYNC
RESETN
PCBEEP
SPDIF_TX0
EAPD(SDMI[3]/SDMO[3])
PORT-H_R(Surr_Back(Right))
PORT-H_L(Surr_Back(Left))
PORT-G_R(LFE/Center)
PORT-G_L(Center/LFE)
AVSS2
PORT-A_R(Surr_Right)
JDREF
PORT-A_L(Surr_Left)
AVDD2
NC
PORT-D_R(Front_Right)
PORT-D_L(Front_Left)
SENSE_B
CAP1
VREFOUT-B_R
VREFOUT-E
VREFOUT-F
VREFOUT-C
VREFOUT-B_L
VREF_FILTER
AVSS1
AVDD1
SENSE_A
PORT-E_L(Front_HP_Left)
PORT-E_R(Front_HP_Right)
PORT-F_R(Front_MIC1)
PORT-F_L(Front_MIC2)
CD_L
CD_GND
CD_R
PORT-B_L(MIC1)
PORT-B_R(MIC2)
PORT-C_L(LINE_IN_L)
PORT-C_R(LINE_IN_R)
(37) EAPD
GND_AUDIO
R3637 5.11KOhm +5V_AUDIO
C3640 0.1UF/16V
+3VS
C3646 0.1UF/16V
GND
(21) ACZ_SDOUT_AUD
(21) ACZ_BCLK_AUD
(21) ACZ_SDIN0_AUD
ACZ_SDIN0_AUD_R
R3619 33Ohm
(21) ACZ_SYNC_AUD
(21,37) ACZ_RST#_AUD
PC_BEEP of codec is level triger
(21) SB_SPKR
R3622 20KOhm
PC_BEEP_C
C3624 0.1UF/16V
PC_BEEP
C3601 100PF/50V @
R3604 1KOhm @
R1.1
T3602 TPC26T
(37) MIC1_JD#
R3638 20KOhm
SENSE_A
(37) AC_HP_L
(37) AC_HP_R
MIC1_VREFOUT_L
R3733 2.2KOhm
L3608
(45) INT_MIC_P
120Ohm/100Mhz
C3656 1UF/10V
C3657 1UF/10V
IN_MIC_R
IN_MIC_L
JP3602 0603
INT_MIC_N (45)
MIC_IN_JACK_R
MIC_IN_JACK_L
C3658
C3659 1UF/10V
1UF/10V
R3603 2.2KOhm
MIC0_VREFOUT_L
MIC_IN_JACK (37)
C9306 0.1UF/10V /EMI/X
FRONT_OUT_R
FRONT_OUT_L
R3627 0Ohm
R3628 0Ohm
AC_OUT_R
AC_OUT_L
FOR DE-POP
FOR GAIN.
C3632 100PF/50V @
C3635 100PF/50V @
C3630 0.47UF/16V
C3631 0.47UF/16V
THE VALUE DEPEND ON C3607/C3608
TO MEET THE RECOMMENDATION
VALUE(0.47UF).
INT_H_SPKR (37)
INT_H_SPKL (37)
MIC1_VREFOUT_L
MIC0_VREFOUT_L
VREF_FILTER
C3637 0.1UF/16V
C3638 10UF/10V
C3639 0.1UF/16V
C3633 0.1UF/16V
C3634 10UF/10V
R3624 39.2KOhm
HP_JD# (37)
R1.1
2nd:SI9183DT 06G007055114
+5VS
+5V_AUDIO
U3602
VIN
VOUT
GND
EN
ADJ/BP/POK
SIP21108DT-T1-E3
AUD_PWR_FB
R3615 150KOhm 1%
T3601 TPC26T
C3616 1UF/10V
R3616 49.9KOhm 1%
JP3601 0603
C3618 2.2UF/6.3V
SI9183DT
Vout=1.215*(1+(150K/49.9K)= 4.86V
<Variant Name>
Title : CONEXANT CX20582
ASUSTeK COMPUTER INC
Engineer: N/A
Size Custom
Project Name K40AA
Rev 1.0
Date: Tuesday, April 14, 2009
Sheet 36 of 94

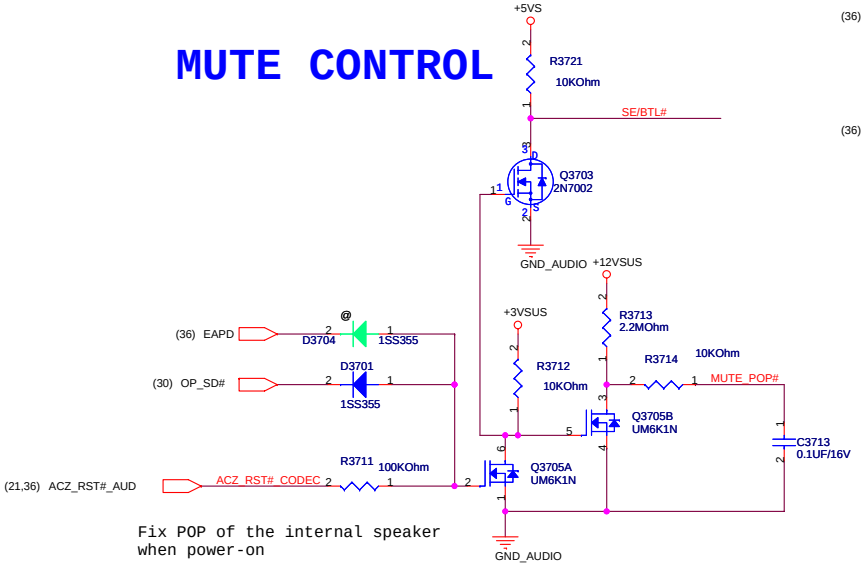
HP CONN

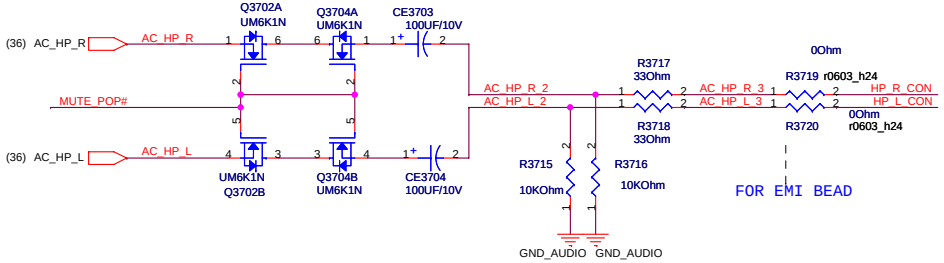


External MIC CONN

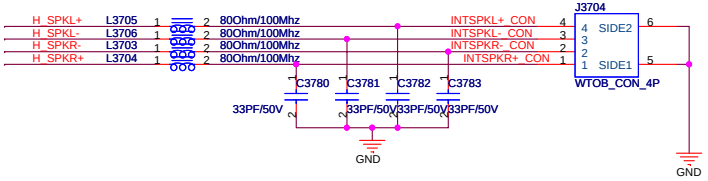


MUTE CONTROL

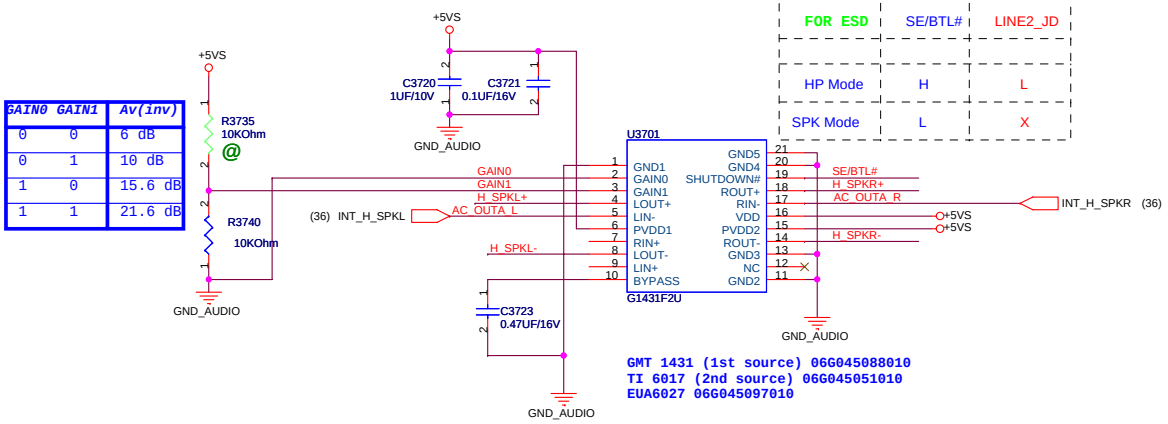




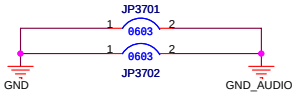
SPEAKER CONNECTOR(2W)



SPEAKER AMP



GMT 1431 (1st source) 06G045088010
TI 6017 (2nd source) 06G045051010
EUA6027 06G045097010



ASUSTeK COMPUTER INC. NB1	Title : AUDIO HP/MIC	
	Engineer: N/A	
Size: Custom	Project Name: K40AA	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 37 of 94	

Title : MIC&LINEIN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 38 of 94

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 39 of 94

Title :	CARDBUS R5C833 (1)
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 40 of 94

Title :	CARDBUS R5C833 (2)
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 41 of 94

Title : 1394&CardReader CON

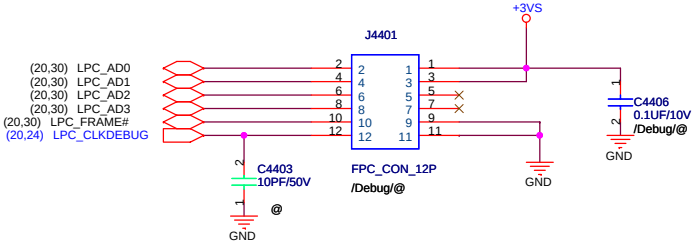
ASUSTeK COMPUTER INC. NB1

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 42 of 94

Title :	NEW CARD
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 43 of 94



If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

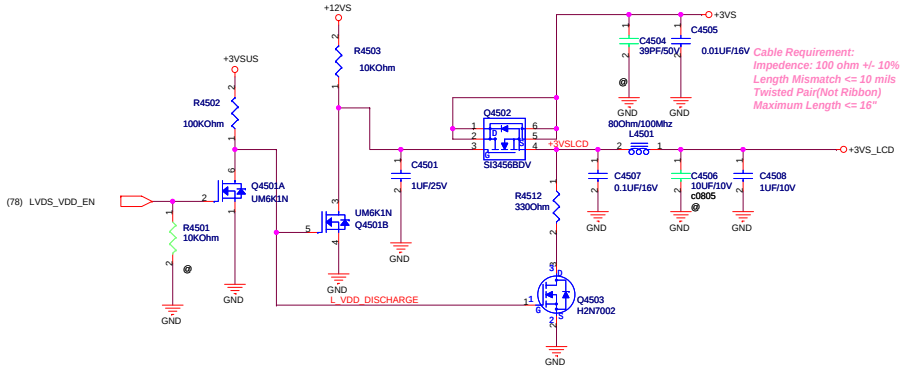
For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 44 of 94	

LCD Backlight Control

LCD Power



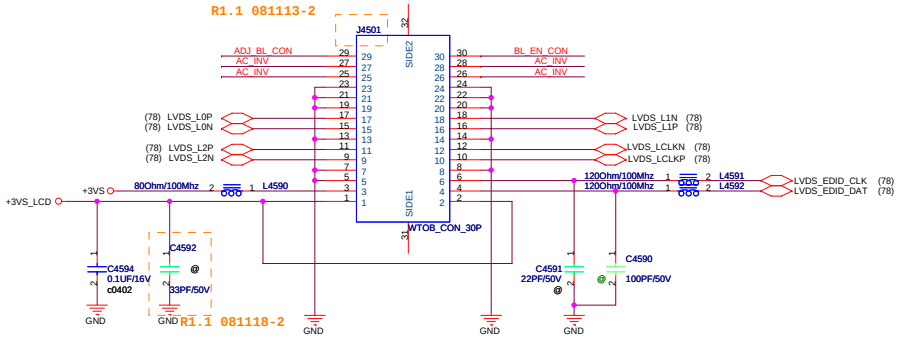
LVDS_LCLKN
LVDS_LCLKP
C4502 10PF/50V N/A

11/19

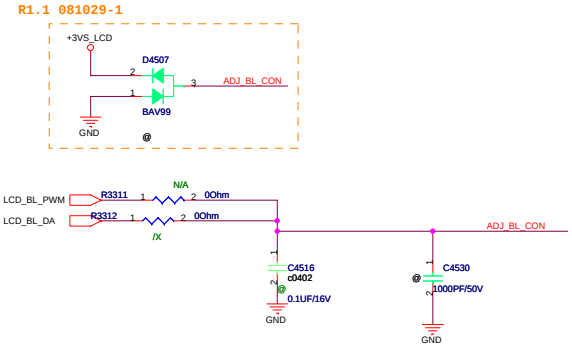
11/19

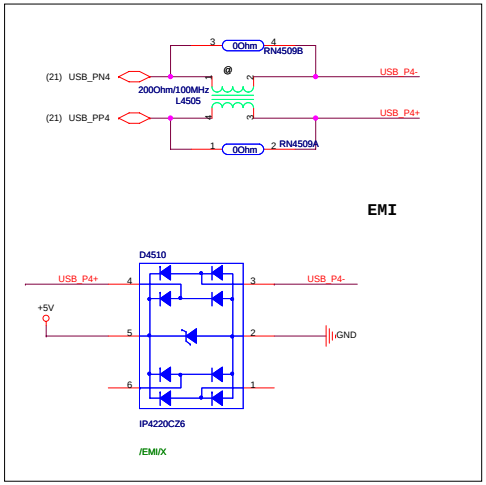
check

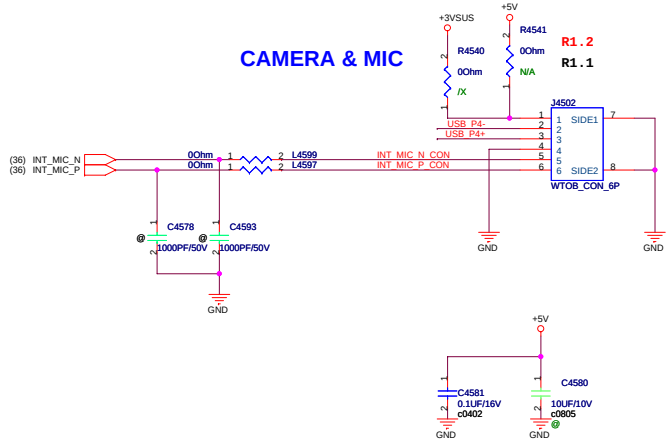
LED PANEL LVDS Interface



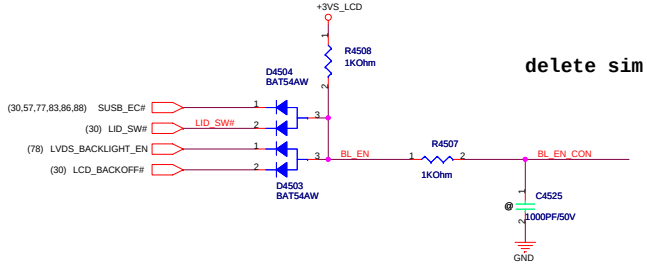
INVERTER
Interface/Speaker CONN.





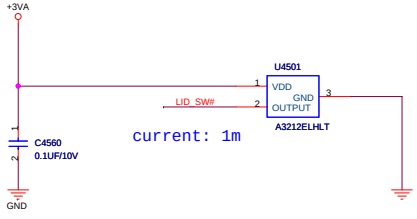


delete sim card function 20080804

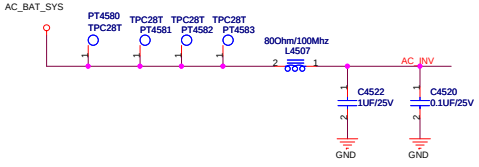


Hall effect switch

current: 2m

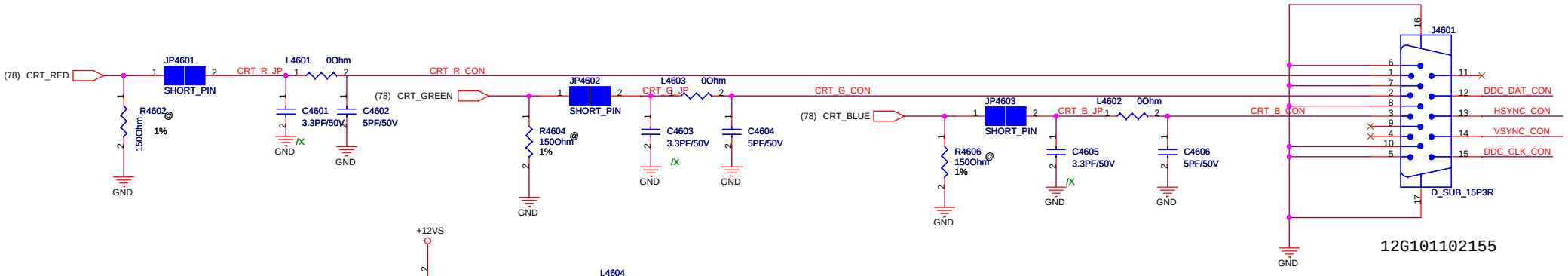


current: 1m

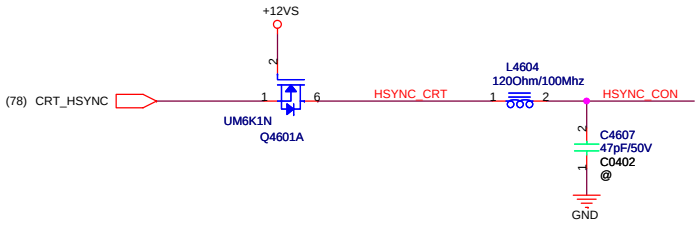


ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: <OrgAddr1>	
Size: C	Project Name: K40AA	Rev: 1.00
Date: Thursday, April 09, 2009	Sheet 45 of 94	

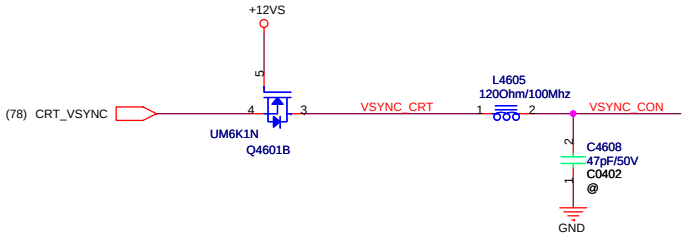
R1.1　VGA部分調整：L4601、L4602、L4603調成0 ohm，C4601、C4603、C4605改爲"/X", C4602、C4604、C4606改成5PF.

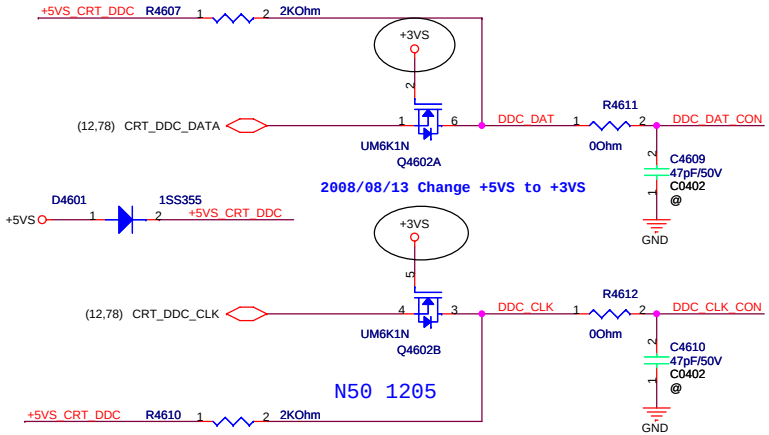


12G101102155

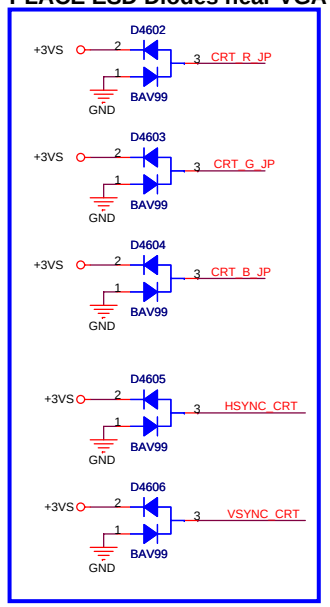


2008/0807 Remove U4601/U4602





PLACE ESD Diodes near VGA port



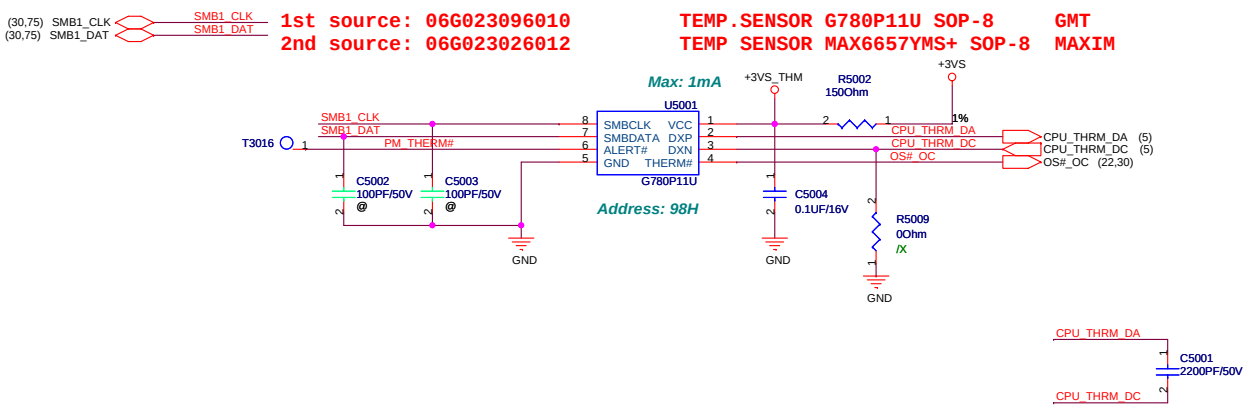
ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 46 of 94	

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 47 of 94

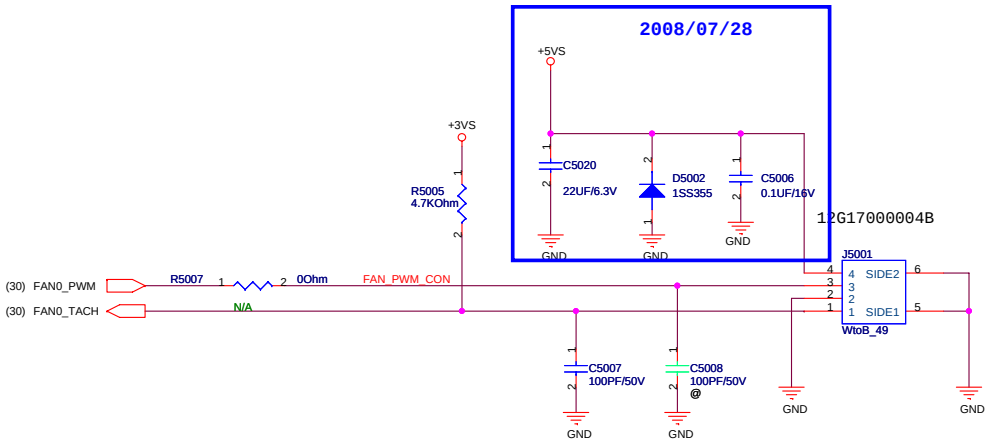
Title :	HDMI
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: K40AA
Rev: 1.00	
Date: Wednesday, April 08, 2009	Sheet 48 of 94

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 49 of 94

Thermal Sensor

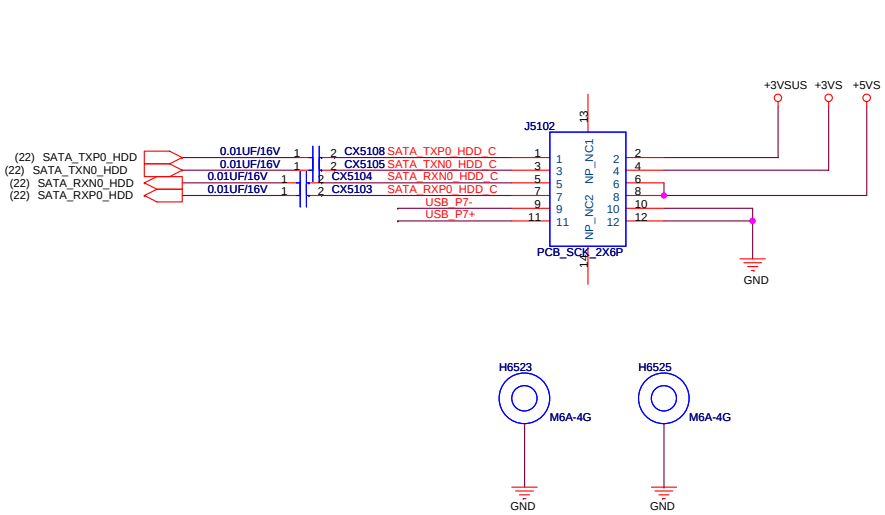


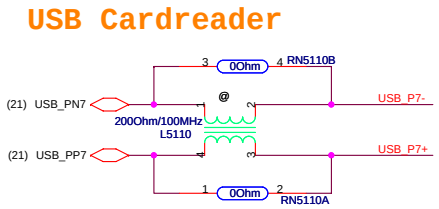
DC FAN Control

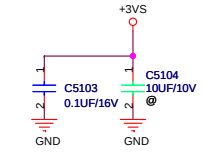


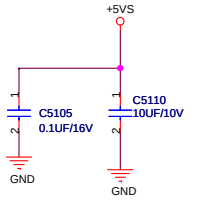
ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 50 of 94	

SATA HDD

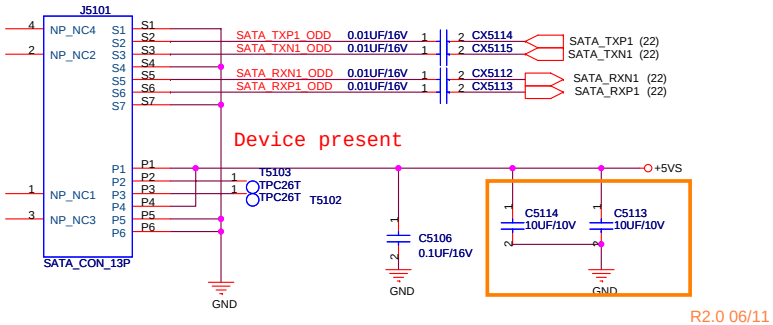








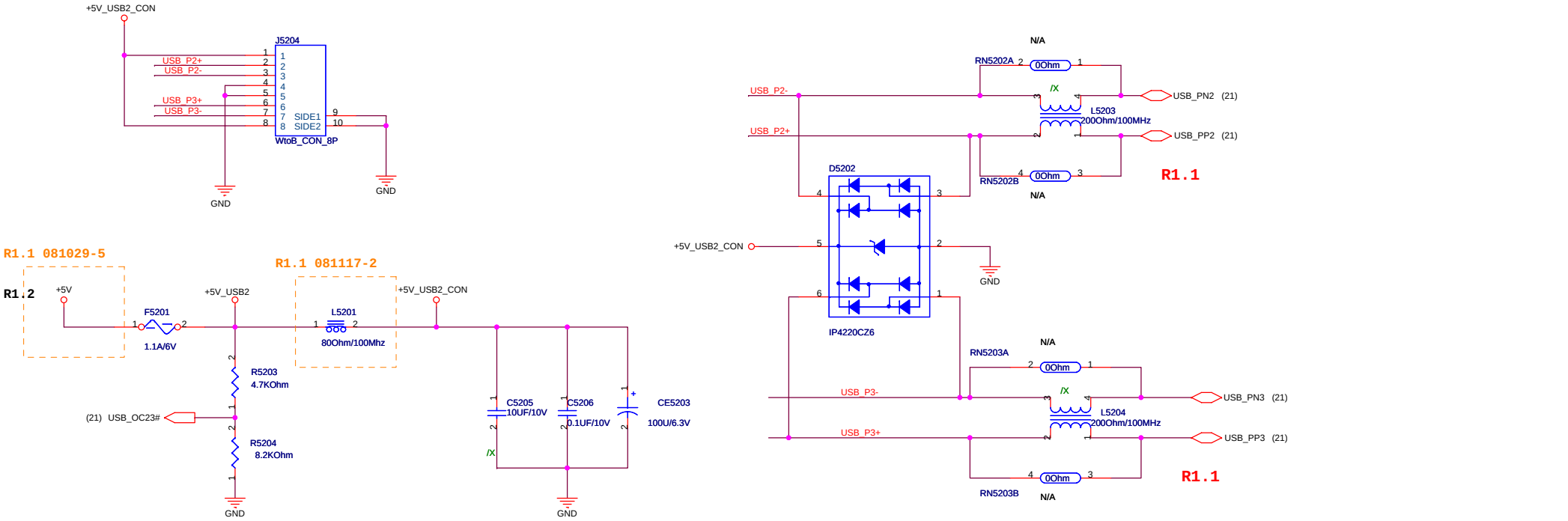
ODD

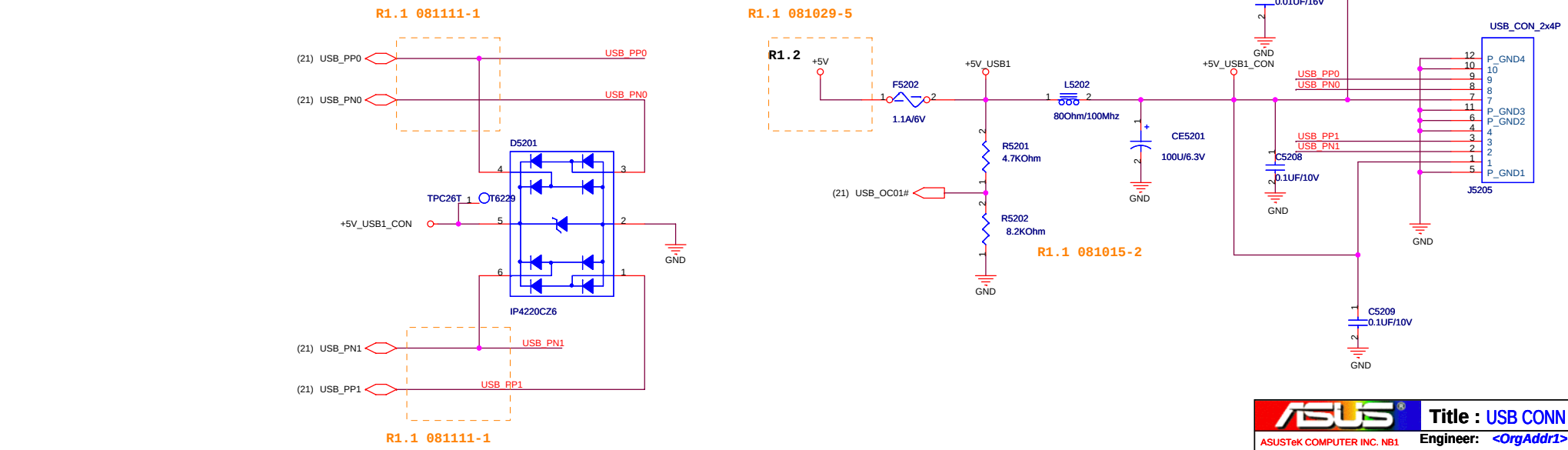


R2.0 06/11

ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: K40AA		Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 51 of 94		

USB IO Board





ASUSTeK COMPUTER INC. NB1

Title : USB CONN X 3

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	K40AA	1.00

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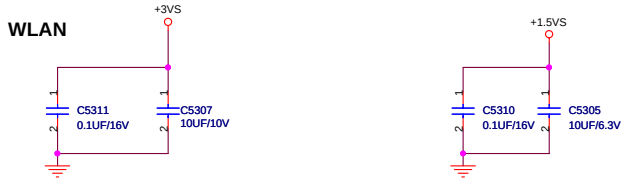
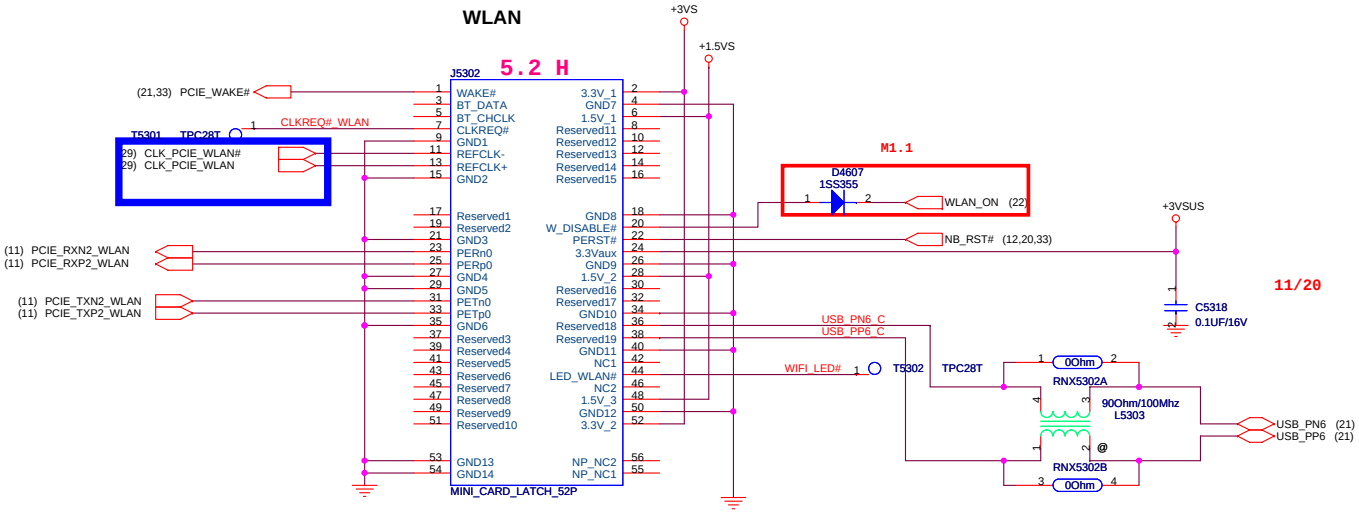




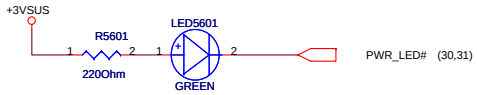
ASUSTeK COMPUTER INC. NB1	Title : Minicard card & Nut	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 53 of 94	

ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 54 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 55 of 94	

For Power LED

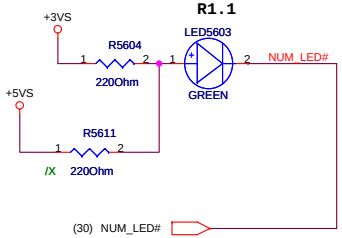
3/13 Orange



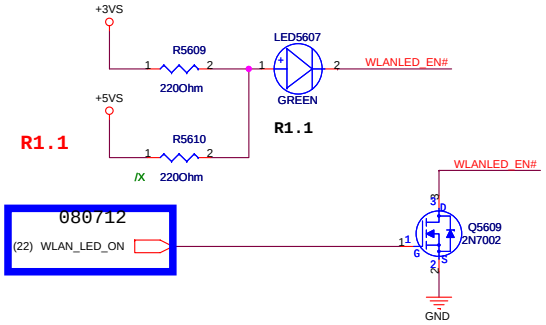
R1.1

For Number Lock

R1.1



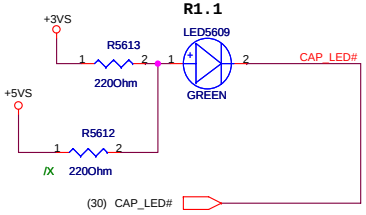
For WireLess LED



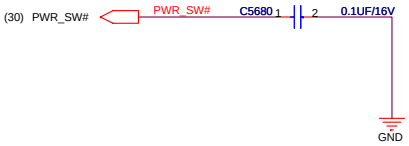
2008/07/30 Remove 3G Function

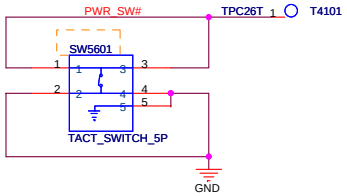
For Caps. Lock

R1.1



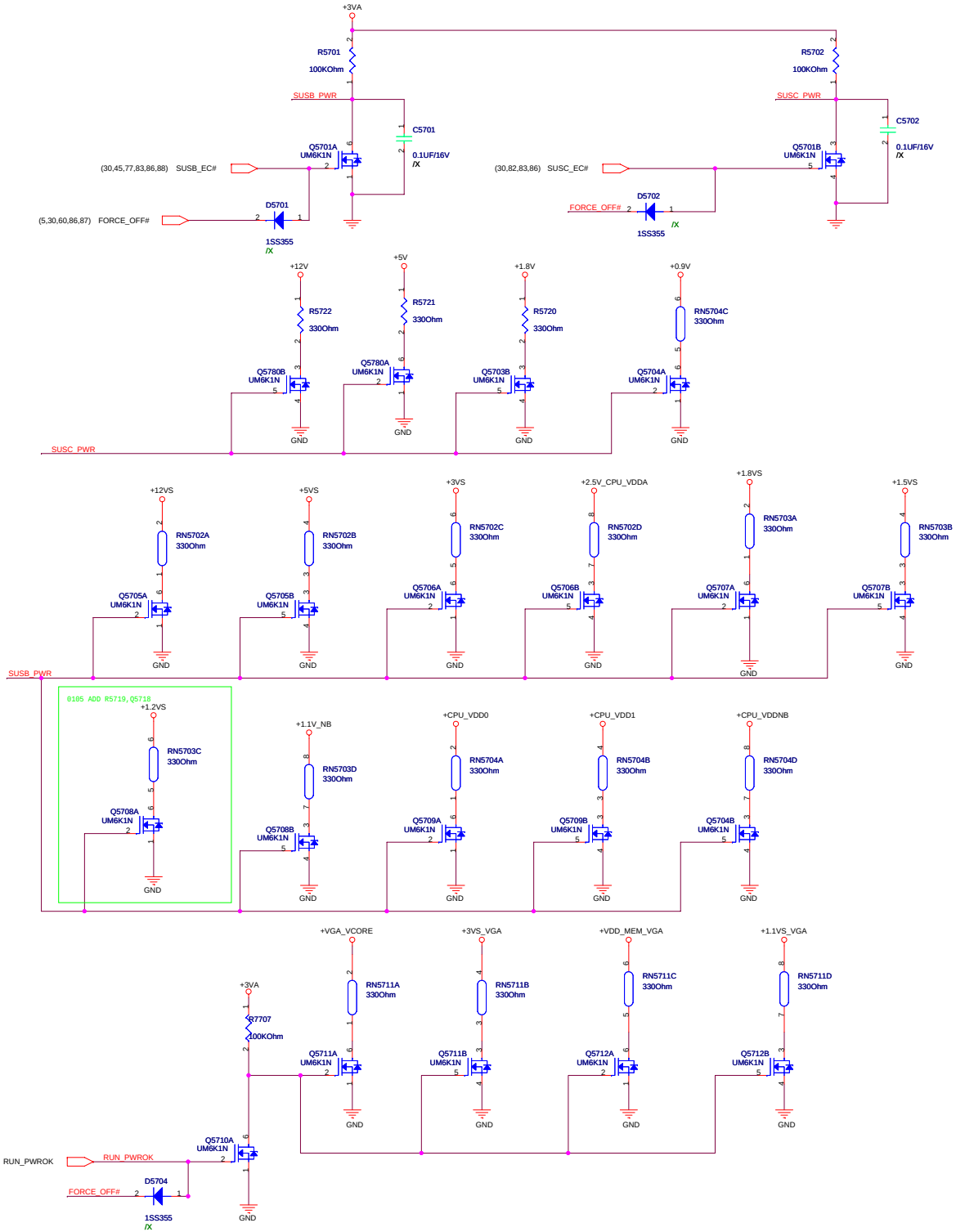
SW





SHUT_DOWN#

ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 56 of 94	



ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 57 of 94	

Title : UWB Minicard card

ASUSTeK COMPUTER INC. NB1

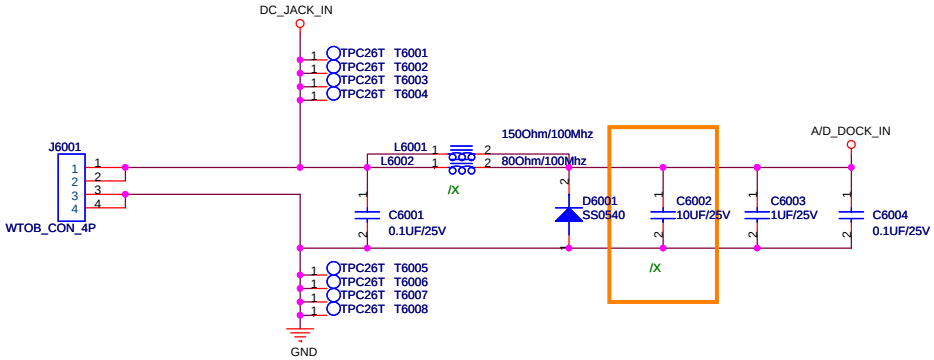
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	K40AA	1.1

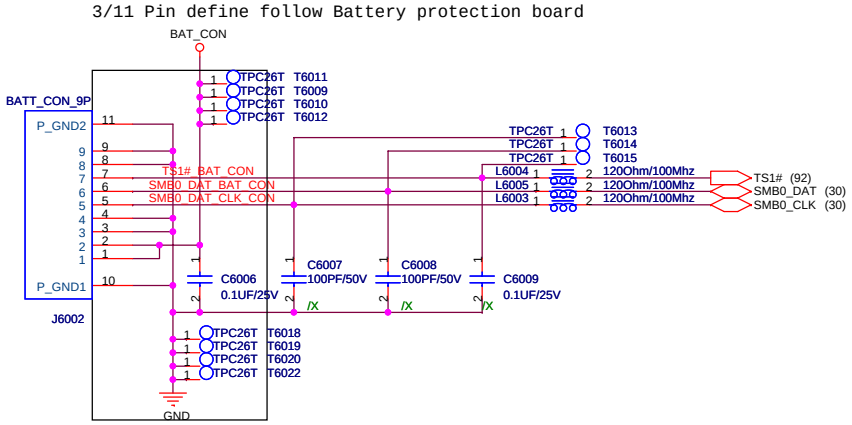
Date: Wednesday, April 08, 2009 Sheet 58 of 94

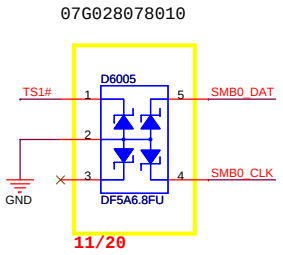
ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 59 of 94	

DC IN

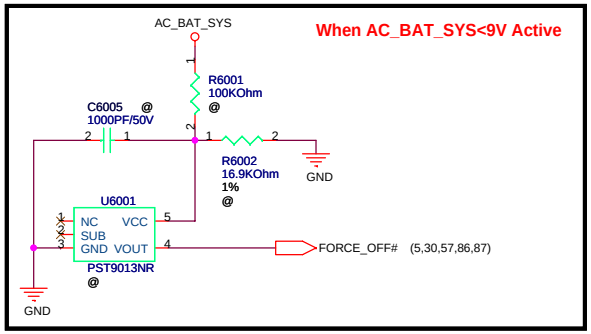


BAT IN





Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 60 of 94	

Hole-A

H6501
HOLE_NPTH

Hole-B

H6502
HOLE_NPTH

H6503
HOLE_NPTH

H6504
HOLE_NPTH

Hole-C

H6505
O83X71DO83X71N

Spring

S6501
EMI_SPRING_PAD
/X

R1.2

GND

Hole-D

H6509
CT276CB197ID138

H6510
CT276CB197ID138

H6511
CT276CB197ID138

H6512
CT276CB197ID138

GND

Hole-E

R1.1

H6514
CT256B315D91N

H6506
CT256B315D91N

H6507
CT256RB276X287D91N

H6508
CT256B220D91N

GND

H6516
CT256B315D91N

GND_AUDIO

Hole-F

H6517
CT256B220D91N

H6520
CT256B220D91N

GND

H6518
CRT266X256D91N

GND

H6519
RT335X305D91N

GND

H6521
CT256B220D91N

H6522
CT256B220D91N

H6513
CT256B220D91N

H6515
CT256B220D91N

GND

ASUSTeK COMPUTER INC. NB1	Title MDC NUT & Hinksink NUT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AA	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 65 of 94	

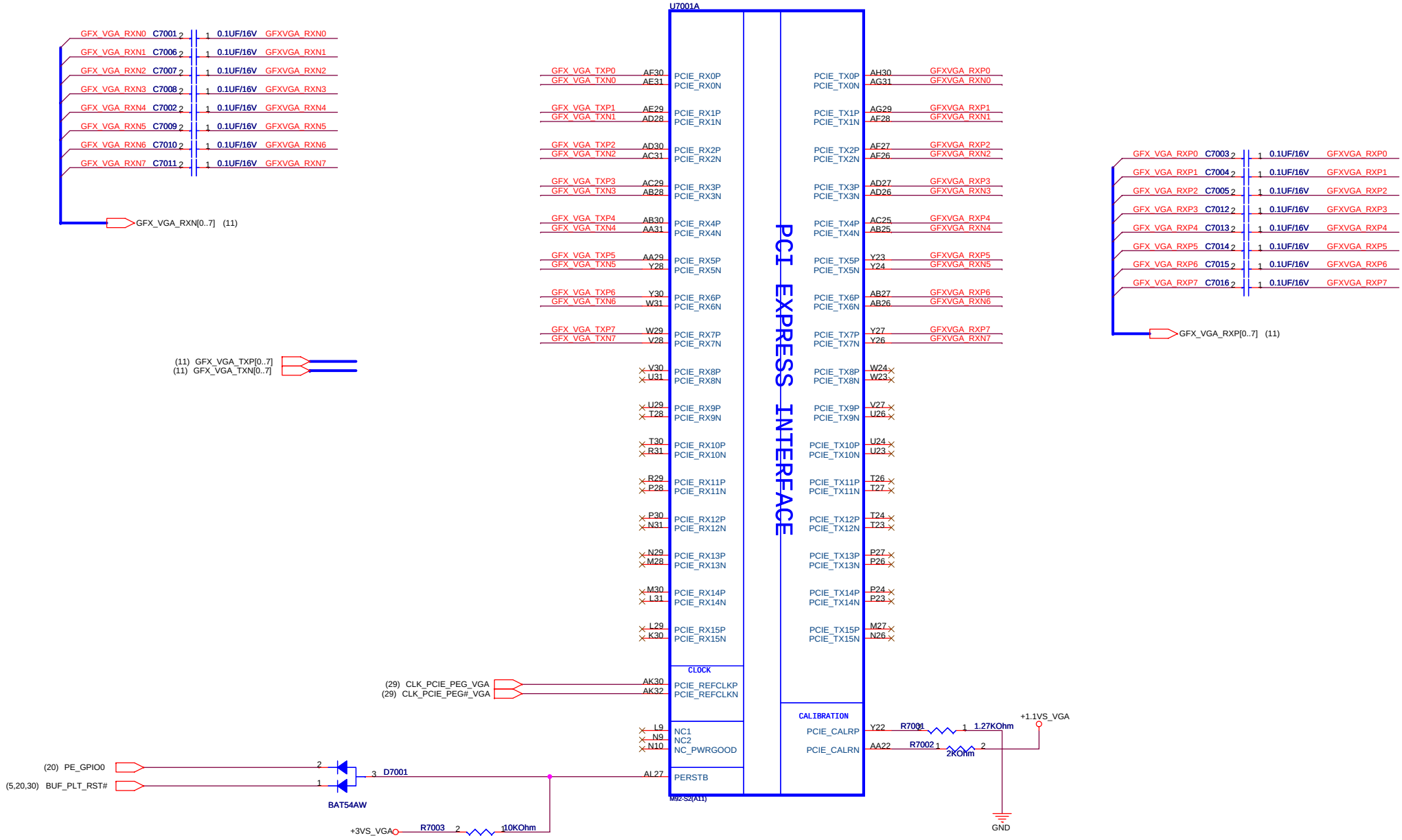
ASUSTeK COMPUTER INC. NB1

Title :

Engineer: <OrgAddr1>

Size	Project Name	Rev
D	K40AA	1.00

Date: Wednesday, April 08, 2009 Sheet 68 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 70 of 94

PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O	
L	L	1.2V	1.182V
H	L	1.10V	1.082V
L	H	1.0V	0.997V
H	H	0.9V	0.925

U7001B

MUTI GFX

DPA

DPB

I2C

GENERAL PURPOSE I/O

DAC1

DAC2

PLL/CLOCK

DDC/AUX

THERMAL

HDMI

<Variant Name>

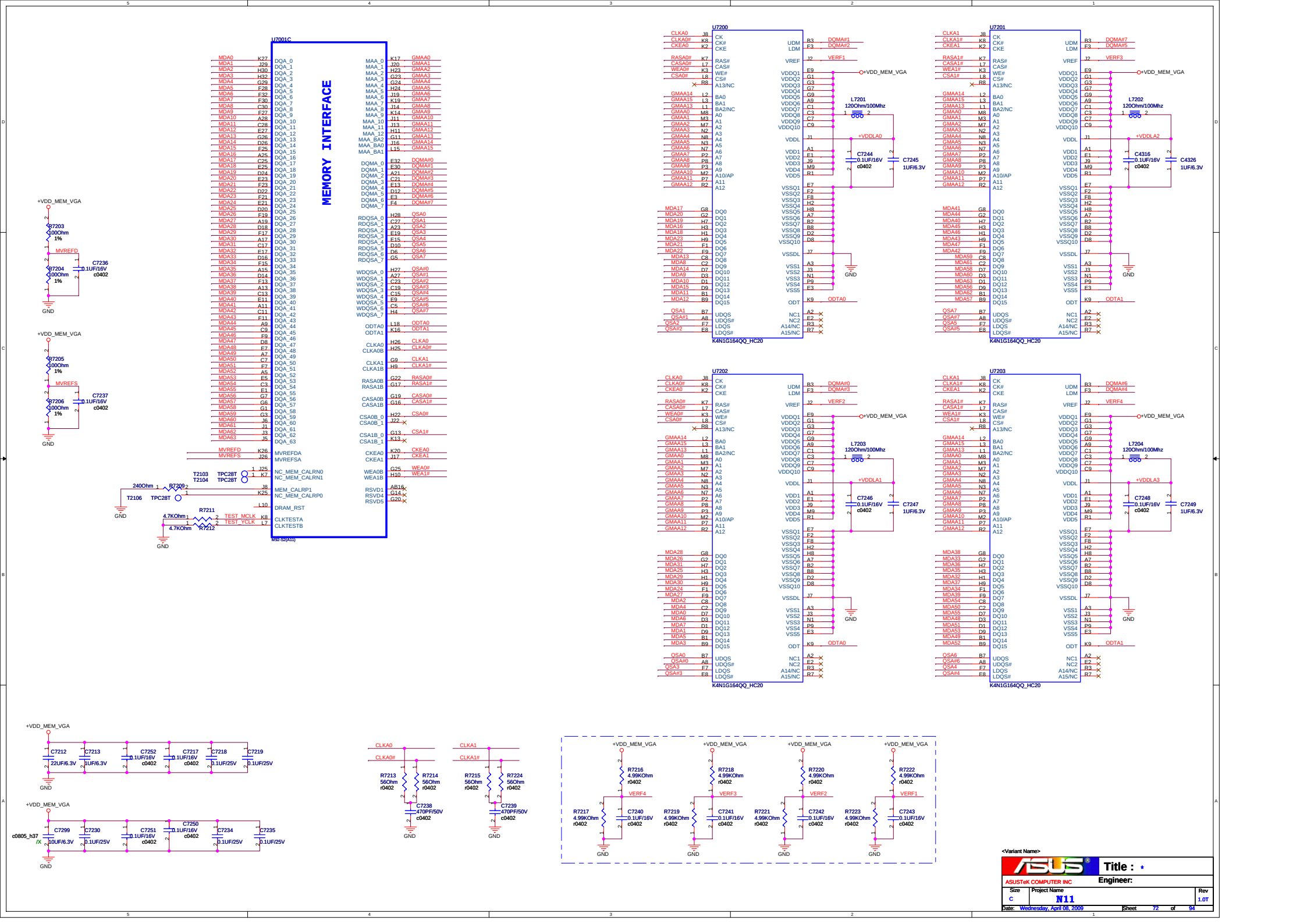
ASUSTeK COMPUTER INC.

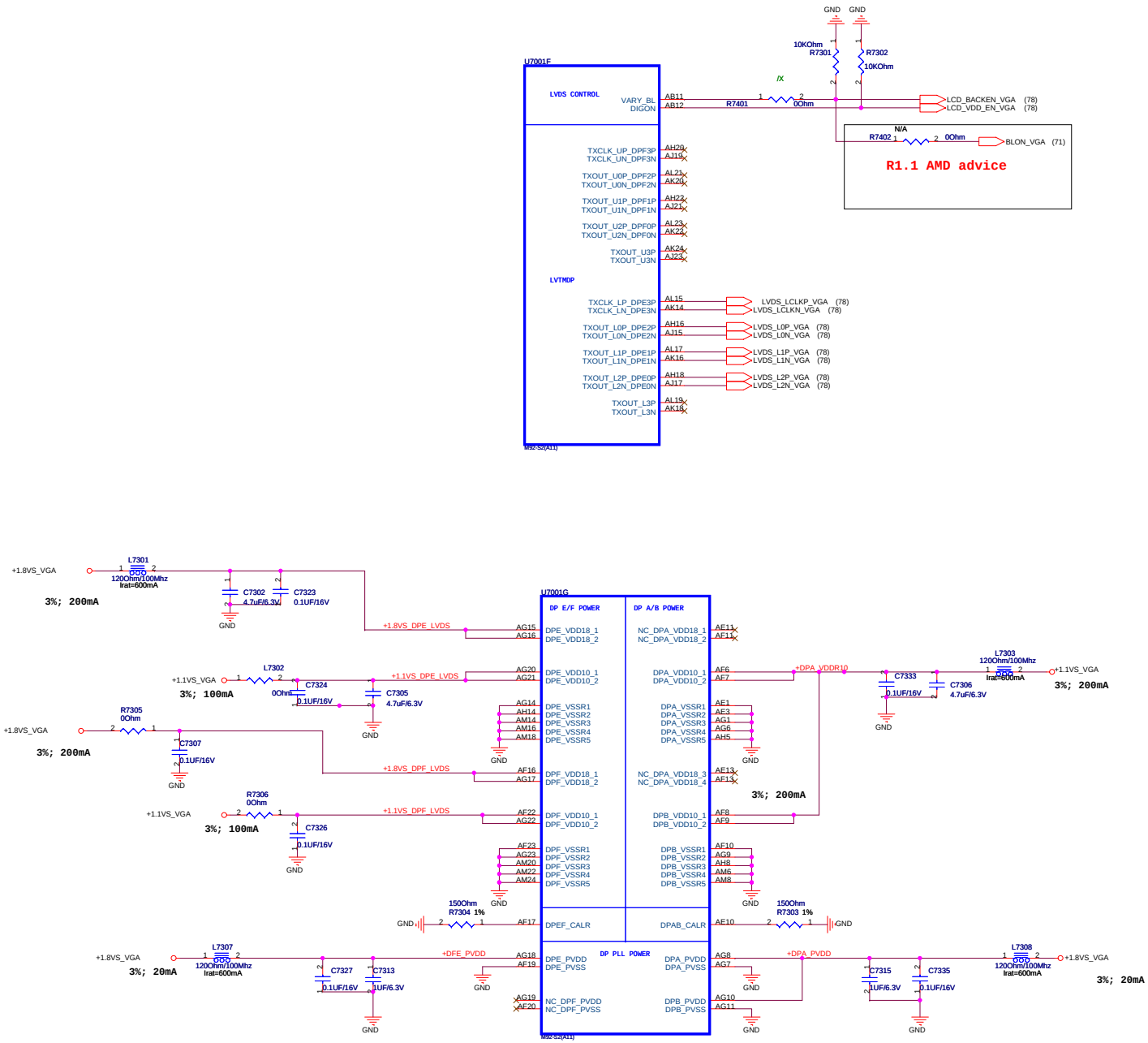
Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 71 of 94


MEMORY INTERFACE
U7001C
U7200
U7201
U7202
U7203
K4N1G164QQ_HC20
L7201 120Ohm/100Mhz
L7202 120Ohm/100Mhz
L7203 120Ohm/100Mhz
L7204 120Ohm/100Mhz
+VDD_MEM_VGA
+VDDLA0
+VDDLA1
+VDDLA2
+VDDLA3
GND
R7203 100Ohm 1%
R7204 100Ohm 1%
MVREFD
C7236 0.1UF/16V c0402
R7205 100Ohm 1%
R7206 100Ohm 1%
MVREFS
C7237 0.1UF/16V c0402
T2103 TPC28T
T2104 TPC28T
T2106 TPC28T
R7209 240Ohm
R7211 4.7KOhm
R7212 4.7KOhm
TEST_MCLK
TEST_YCLK
C7212 22UF/6.3V
C7213 1UF/6.3V
C7252 0.1UF/16V c0402
C7217 0.1UF/16V c0402
C7218 0.1UF/25V
C7219 0.1UF/25V
C7299 10UF/6.3V c0805_h37
C7230 0.1UF/25V
C7251 0.1UF/16V c0402
C7250 0.1UF/16V c0402
C7234 0.1UF/25V
C7235 0.1UF/25V
R7213 56Ohm r0402
R7214 56Ohm r0402
R7215 56Ohm r0402
R7224 56Ohm r0402
C7238 470PF/50V c0402
C7239 470PF/50V c0402
R7216 4.99KOhm r0402
R7217 4.99KOhm r0402
R7218 4.99KOhm r0402
R7219 4.99KOhm r0402
R7220 4.99KOhm r0402
R7221 4.99KOhm r0402
R7222 4.99KOhm r0402
R7223 4.99KOhm r0402
C7240 0.1UF/16V c0402
C7241 0.1UF/16V c0402
C7242 0.1UF/16V c0402
C7243 0.1UF/16V c0402
C7244 0.1UF/16V c0402
C7245 1UF/6.3V
C4316 0.1UF/16V c0402
C4326 1UF/6.3V
C7246 0.1UF/16V c0402
C7247 1UF/6.3V
C7248 0.1UF/16V c0402
C7249 1UF/6.3V
VERF1
VERF2
VERF3
VERF4
ASUSTeK COMPUTER INC
Title :
Engineer:
Size C
Project Name N11
Rev 1.0T
Date: Wednesday, April 08, 2009
Sheet 72 of 94



<Variant Name>

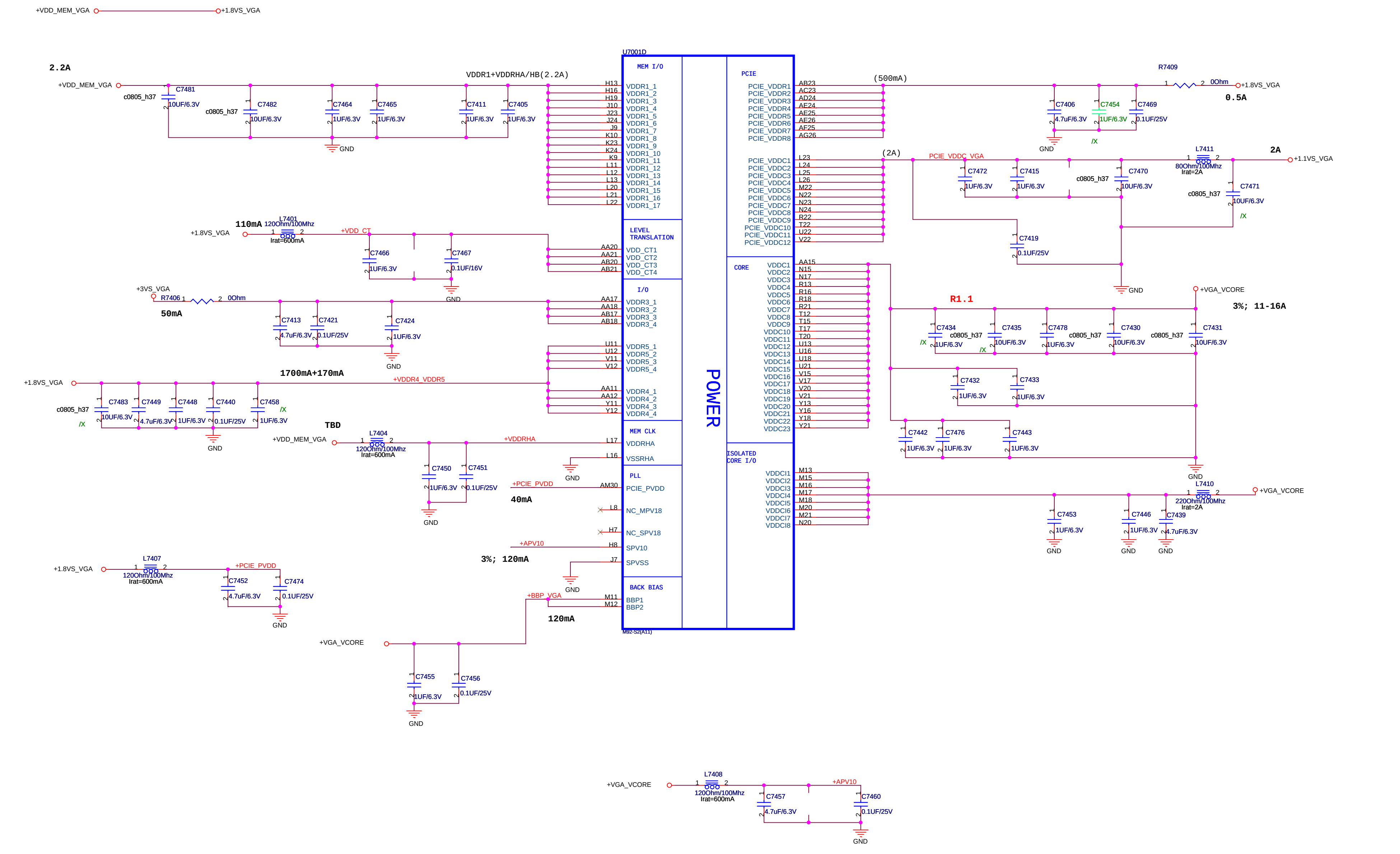
ASUSTeK COMPUTER INC

Title : *

Engineer:

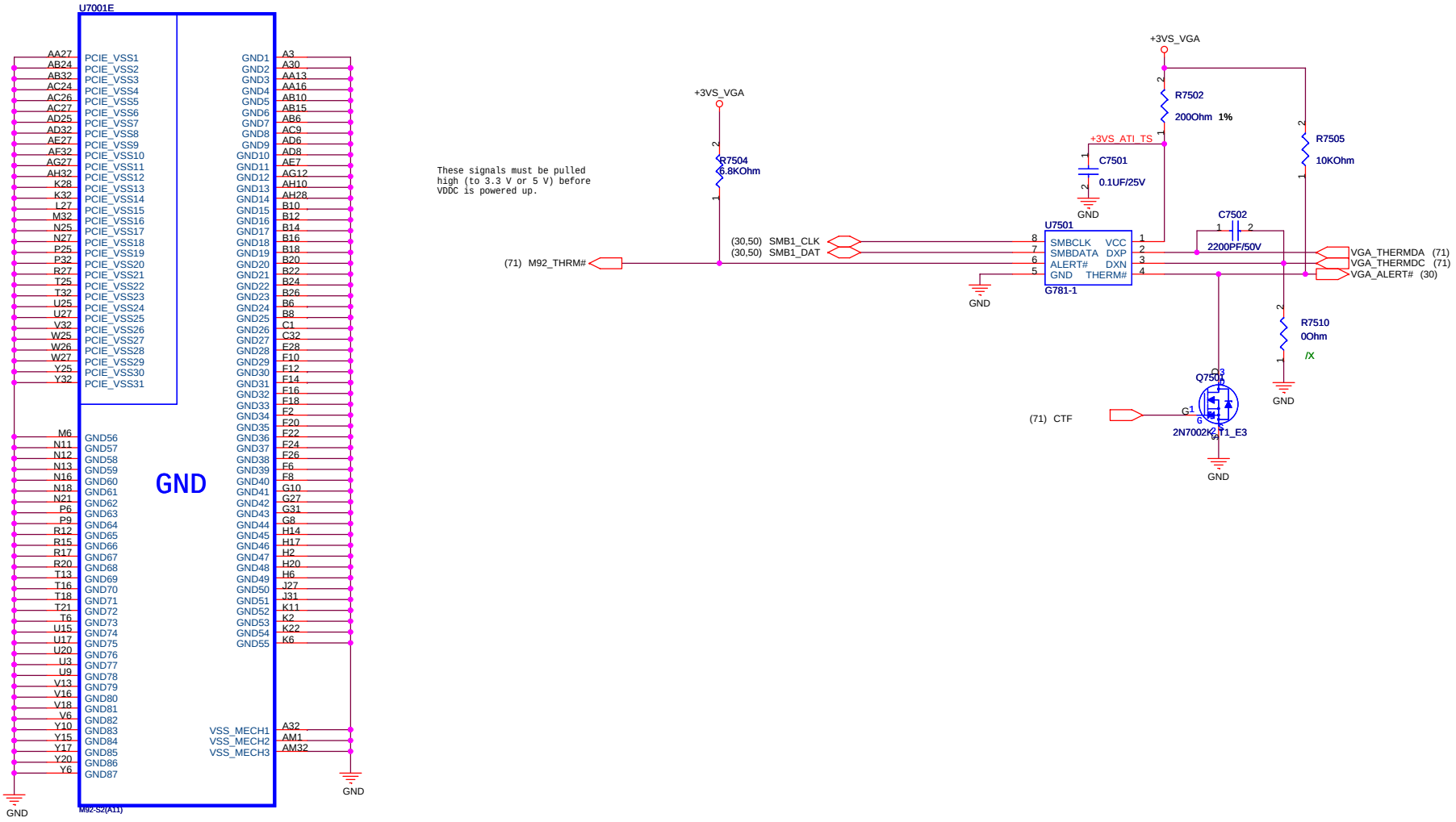
Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 73 of 94


+VDD_MEM_VGA
+1.8VS_VGA
U7001D
2.2A
VDDR1+VDDRHA/HB(2.2A)
MEM I/O
PCIE
(500mA)
R7409
0Ohm
0.5A
(2A)
PCIE_VDDC_VGA
L7411
80Ohm/100Mhz
Irat=2A
2A
+1.1VS_VGA
110mA
L7401
120Ohm/100Mhz
Irat=600mA
+VDD_CT
LEVEL TRANSLATION
+3VS_VGA
R7406
50mA
I/O
CORE
R1.1
+VGA_VCORE
3%; 11-16A
1700mA+170mA
+VDDR4_VDDR5
TBD
L7404
+VDDRHA
MEM CLK
PLL
+PCIE_PVDD
40mA
+APV10
3%; 120mA
L7407
BACK BIAS
+BBP_VGA
120mA
POWER
ISOLATED CORE I/O
L7410
220Ohm/100Mhz
L7408
GND
M92-S2(A11)

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer:	
Size: C	Project Name: N11	Rev: 1.0T
Date: Wednesday, April 08, 2009	Sheet 74 of 94	



<Variant Name>

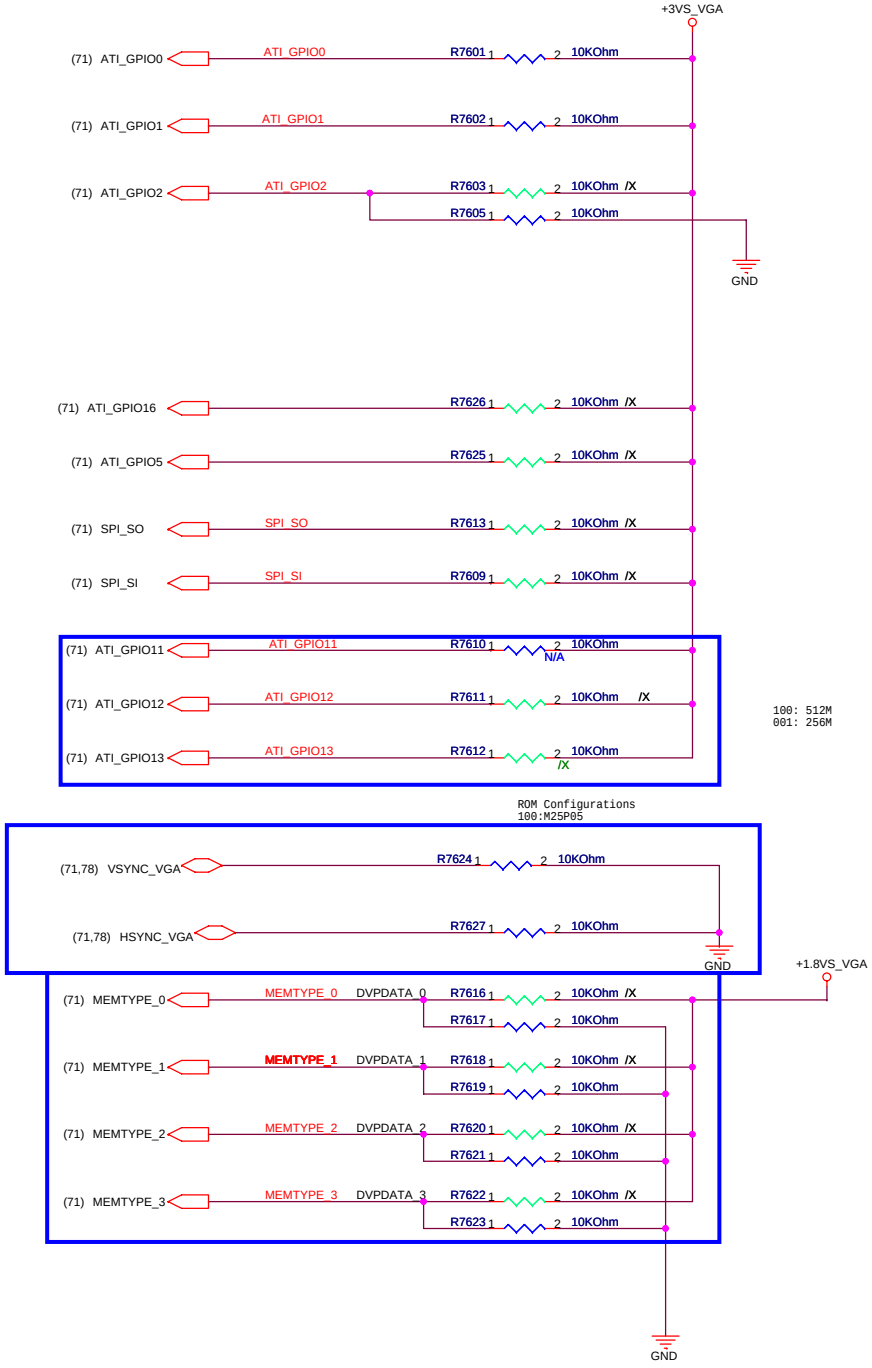
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 75 of 94




```
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO_1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO_2 - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

GPIO(11,13,12) - CONFIG[2..0]
                100 - 512Kbit  M25P05A      (ST)
CONFIG[2]       101 - 1Mbit    M25P10A      (ST)
                101 - 2Mbit    M25P20       (ST)
CONFIG[1]       101 - 4Mbit    M25P40       (ST)
                101 - 8Mbit    M25P80       (ST)
CONFIG[0]       100 - 512Kbit  Pm25LV512    (Chingis)
                101 - 1Mbit    Pm25LV010    (Chingis)

GPIO_8 - BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_5 - AMD BOARD FEATURES I
0: 1 RANK OF MEMORY 1: 2 RANKS OF MEMORY

GPIO_16 - AMD BOARD FEATURES II
BANK SELECT;

GPIO_7 - TV OUT STANDARD
0 - PAL TVO
1 - NTSC TVO

V2SYNC - VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine
whether or not a VIP slave device (e.g. Theater chip) is connected
(i.e. 0 indicates yes, 1 indicates no).

GPIO_9 - VGA DISABLE : 1 for disable (set to 0 for normal operation)

HSYNC;VSYNC - AUD[1:0]
00 - No audio function
01 - Audio for DisplayPort and HDMI if adapter is detected
10 - Audio for DisplayPort only
11 - Audio for both DisplayPort and HDMI.
```

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	64M*16	
Samsung	0001	1	64M*16	
Hynix				
Micron				

<Variant Name>

ASUSTeK COMPUTER INC

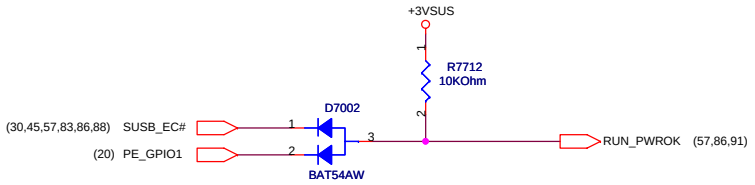
Title : *

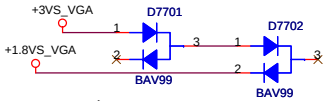
Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

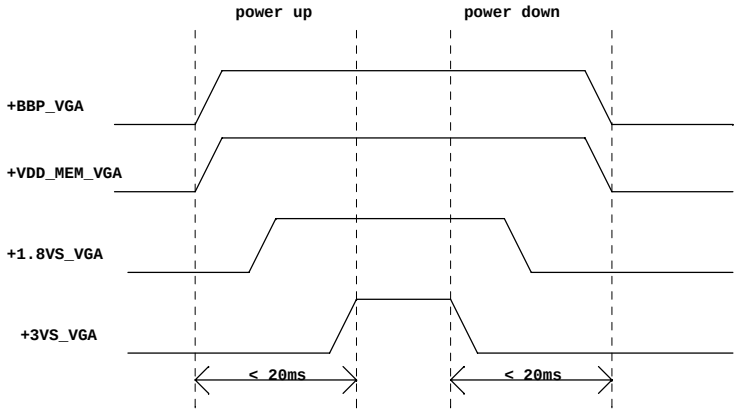
Date: Thursday, April 09, 2009 Sheet 76 of 94

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V





VDDR3 每 VDD_CT
< 2V



1.1-V rails should ramp before, or together with the 1.8-V rails.
The 1.1-V nominal voltage rails should never lag the 1.8-V nominal voltage rails by more than 1.1 V within a 1 ms window.

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

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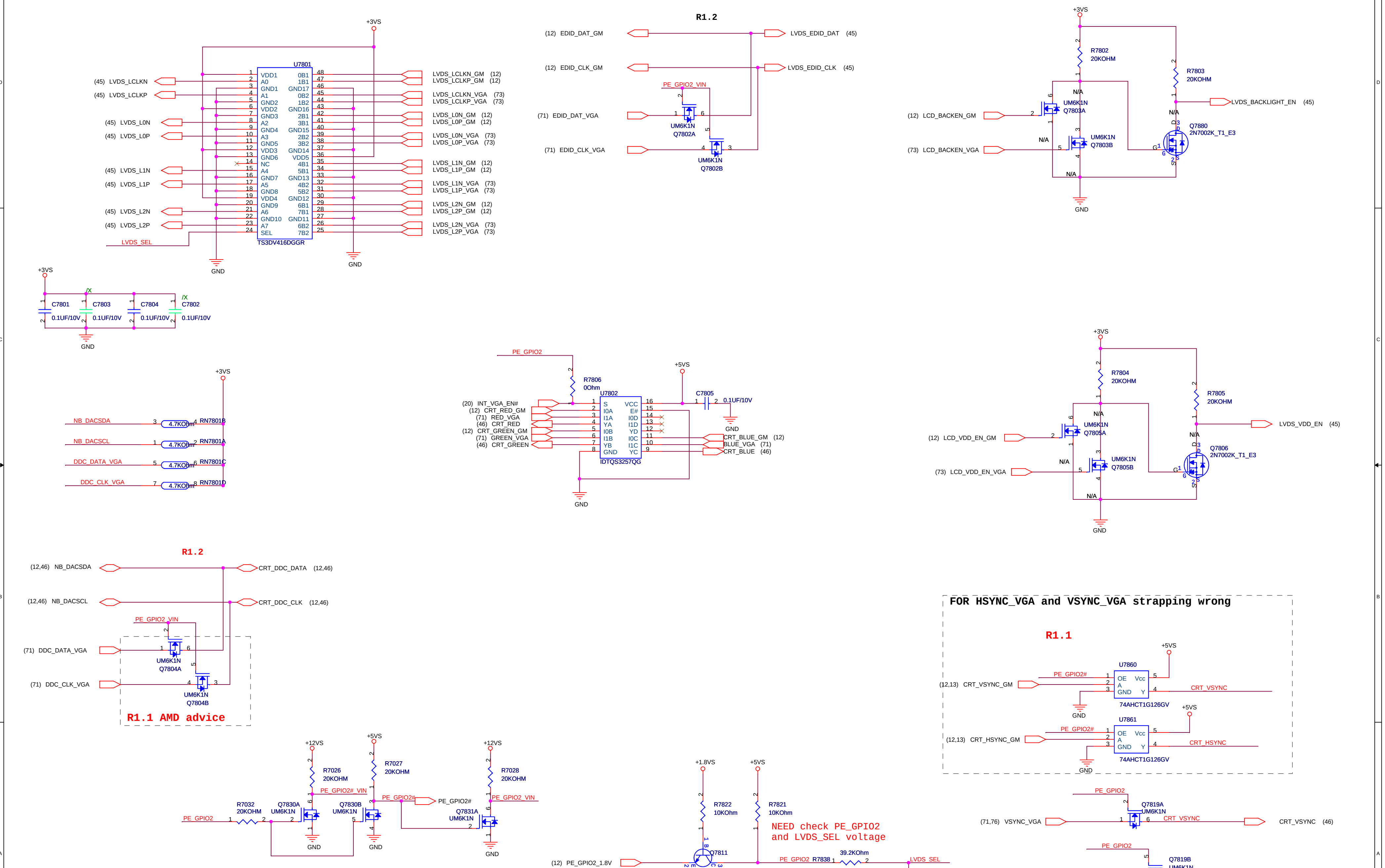
R1.2
(12) EDID_DAT_GM
LVDS_EDID_DAT (45)
(12) EDID_CLK_GM
LVDS_EDID_CLK (45)
PE_GPIO2_VIN
(71) EDID_DAT_VGA
(71) EDID_CLK_VGA
UM6K1N Q7802A
UM6K1N Q7802B
+3VS
U7801
TS3DV416DGGR
(45) LVDS_LCLKN
(45) LVDS_LCLKP
(45) LVDS_L0N
(45) LVDS_L0P
(45) LVDS_L1N
(45) LVDS_L1P
(45) LVDS_L2N
(45) LVDS_L2P
LVDS_SEL
LVDS_LCLKN_GM (12)
LVDS_LCLKP_GM (12)
LVDS_LCLKN_VGA (73)
LVDS_LCLKP_VGA (73)
LVDS_L0N_GM (12)
LVDS_L0P_GM (12)
LVDS_L0N_VGA (73)
LVDS_L0P_VGA (73)
LVDS_L1N_GM (12)
LVDS_L1P_GM (12)
LVDS_L1N_VGA (73)
LVDS_L1P_VGA (73)
LVDS_L2N_GM (12)
LVDS_L2P_GM (12)
LVDS_L2N_VGA (73)
LVDS_L2P_VGA (73)
GND
R7802 20KOHM
R7803 20KOHM
UM6K1N Q7803A
UM6K1N Q7803B
Q7880 2N7002K_T1_E3
LVDS_BACKLIGHT_EN (45)
(12) LCD_BACKEN_GM
(73) LCD_BACKEN_VGA
N/A
C7801 0.1UF/10V
C7803 0.1UF/10V
C7804 0.1UF/10V
C7802 0.1UF/10V
PE_GPIO2
R7806 0Ohm
U7802
IDTQS3257QG
+5VS
C7805 0.1UF/10V
(20) INT_VGA_EN#
(12) CRT_RED_GM
(71) RED_VGA
(46) CRT_RED
(12) CRT_GREEN_GM
(71) GREEN_VGA
(46) CRT_GREEN
CRT_BLUE_GM (12)
BLUE_VGA (71)
CRT_BLUE (46)
NB_DACSDA
NB_DACSCL
DDC_DATA_VGA
DDC_CLK_VGA
4.7KOhm
RN7801A
RN7801B
RN7801C
RN7801D
R7804 20KOHM
R7805 20KOHM
UM6K1N Q7805A
UM6K1N Q7805B
Q7806 2N7002K_T1_E3
LVDS_VDD_EN (45)
(12) LCD_VDD_EN_GM
(73) LCD_VDD_EN_VGA
R1.2
(12,46) NB_DACSDA
CRT_DDC_DATA (12,46)
(12,46) NB_DACSCL
CRT_DDC_CLK (12,46)
(71) DDC_DATA_VGA
(71) DDC_CLK_VGA
UM6K1N Q7804A
UM6K1N Q7804B
R1.1 AMD advice
FOR HSYNC_VGA and VSYNC_VGA strapping wrong
R1.1
U7860
U7861
74AHCT1G126GV
PE_GPIO2#
(12,13) CRT_VSYNC_GM
(12,13) CRT_HSYNC_GM
CRT_VSYNC
CRT_HSYNC
+12VS
R7026 20KOHM
R7027 20KOHM
R7028 20KOHM
R7032 20KOHM
PE_GPIO2#_VIN
UM6K1N Q7830A
UM6K1N Q7830B
UM6K1N Q7831A
UM6K1N Q7831B
+1.8VS
R7822 10KOhm
R7821 10KOhm
NEED check PE_GPIO2 and LVDS_SEL voltage
(12) PE_GPIO2_1.8V
Q7811 PMBS3904
R7838 39.2KOhm
R7839 100KOhm
(71,76) VSYNC_VGA
CRT_VSYNC (46)
(71,76) HSYNC_VGA
CRT_HSYNC (46)
UM6K1N Q7819A
UM6K1N Q7819B

POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET	H: Enable
PE_GPIO1 MXM POWER ENABLE	H: Enable
PE_GPIO2 MODE SWITCH	
TMDS_HPD0 MXM HOT PLUG	

PE_GPIO2 :
L: B1 Internal VGA
H: B2 External VGA

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

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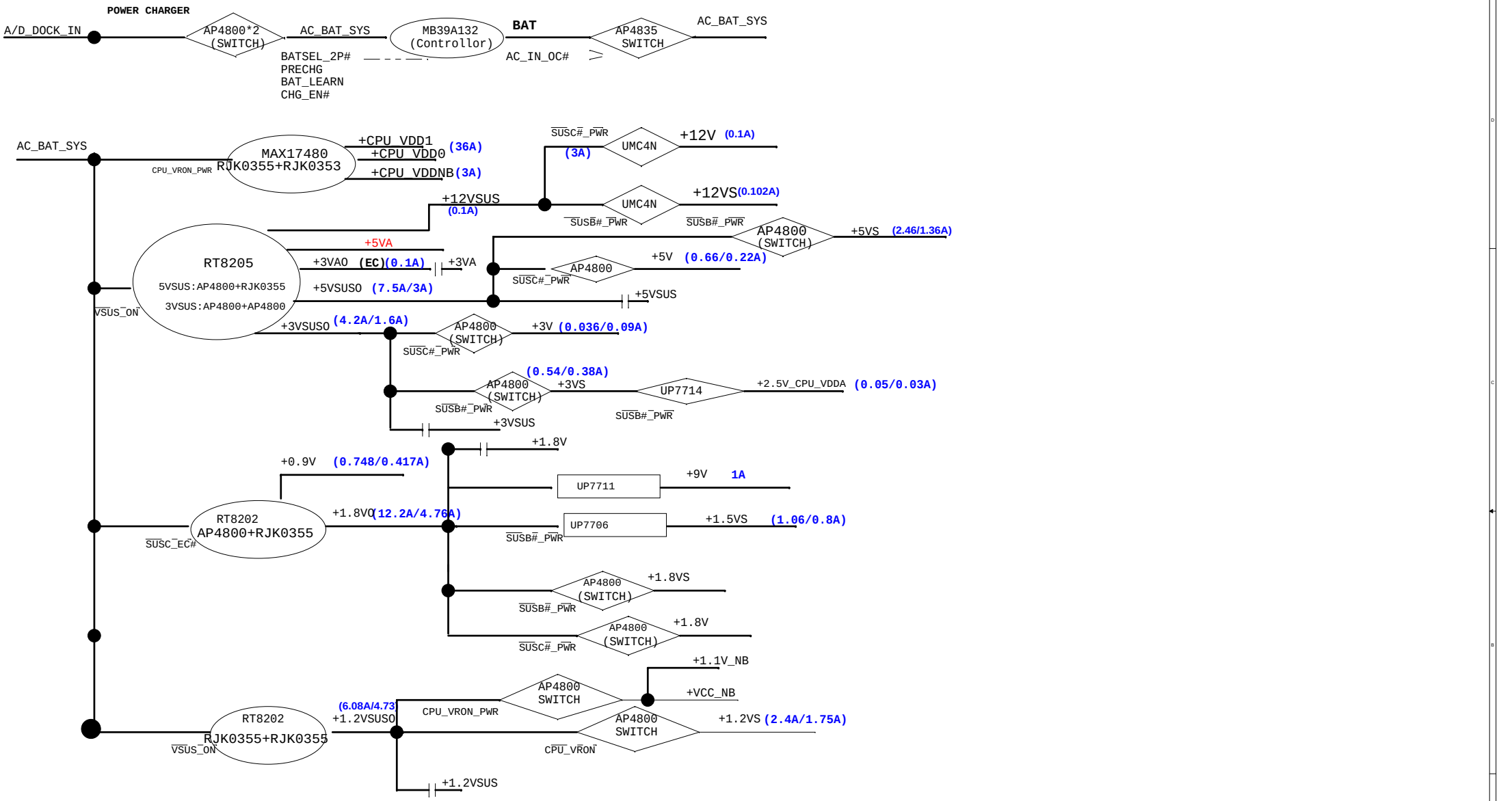


<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_FLOW

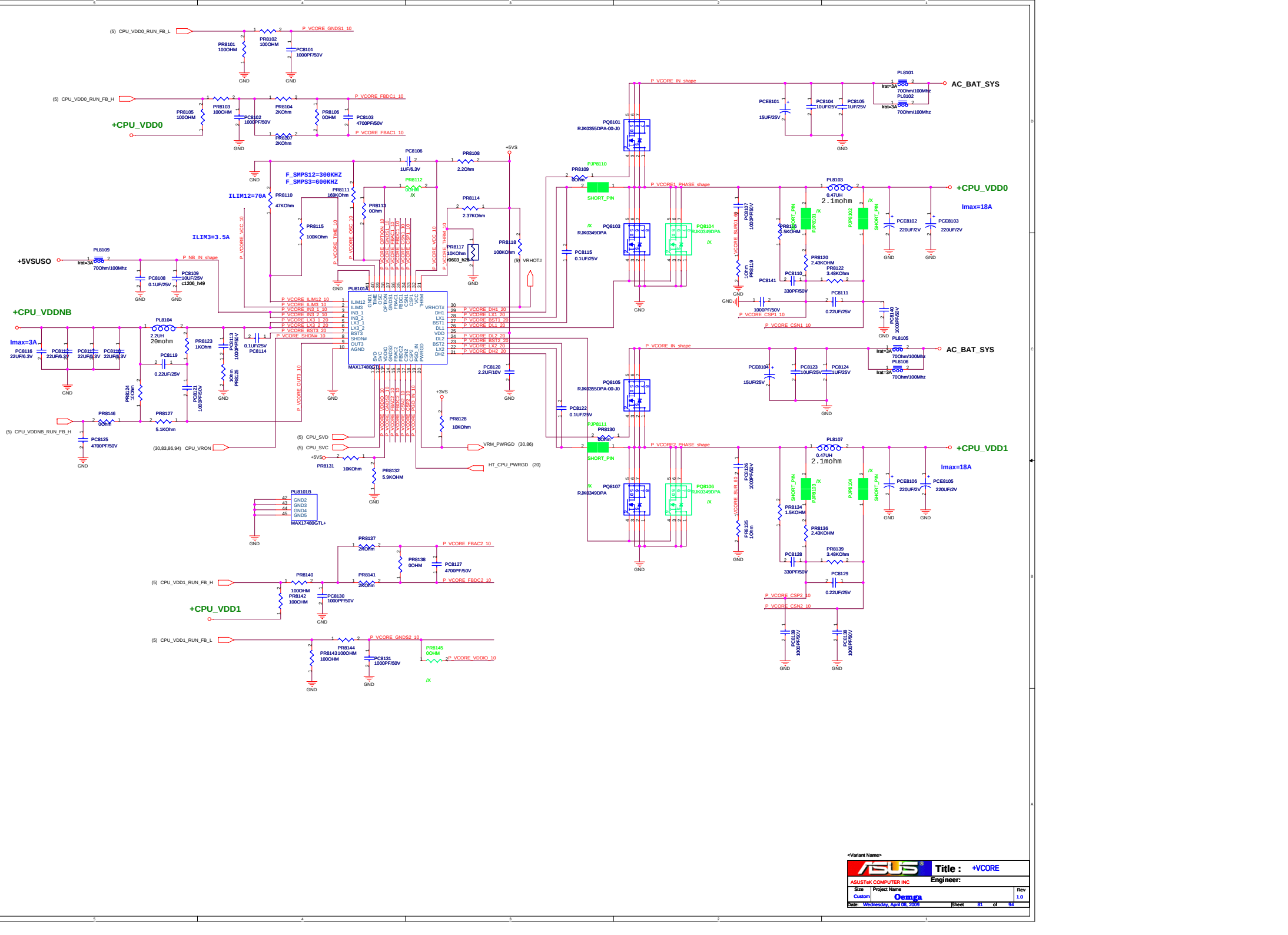
Engineer: N/A

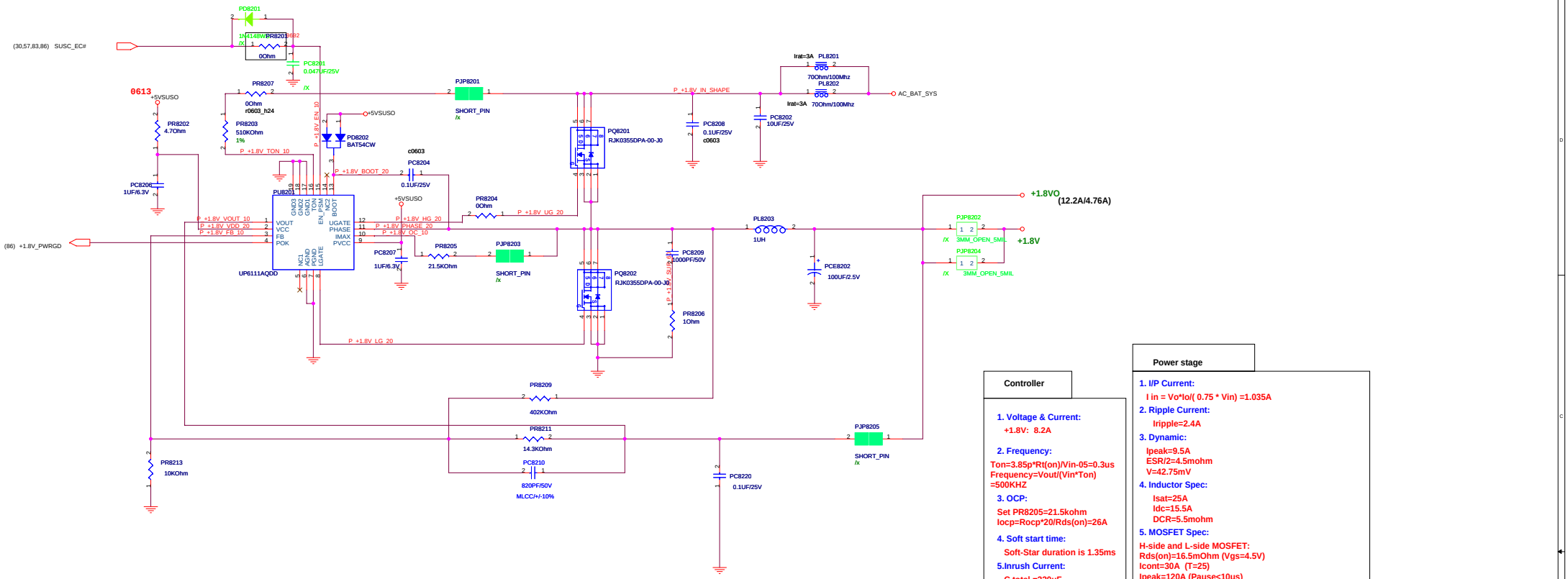
Size	Project Name	Rev
A2	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 79 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_ FLOW		
	Engineer: N/A		
Size: A	Project Name: Oemga		Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 80 of 94		


(5) CPU_VDD0_RUN_FB_L
P_VCORE_GNDS1_10
PR8101 100OHM
PR8102 100OHM
PC8101 1000PF/50V
(5) CPU_VDD0_RUN_FB_H
+CPU_VDD0
PR8105 100OHM
PR8103 100OHM
PC8102 1000PF/50V
PR8104 2KOhm
PR8106 0OHM
PC8103 4700PF/50V
PR8107 2KOhm
P_VCORE_FBDC1_10
P_VCORE_FBAC1_10
F_SMPS12=300KHZ
F_SMPS3=600KHZ
ILIM12=70A
ILIM3=3.5A
PR8110 47KOhm
PR8111 169KOhm
PR8112 0OHM
PR8113 0Ohm
PR8115 100KOhm
PC8106 1UF/6.3V
PR8108 2.2Ohm
PR8114 2.37KOhm
PR8117 10KOhm
PR8118 100KOhm
(5) VRHOT#
+5VSUSO
PL8109 70Ohm/100Mhz
PC8108 0.1UF/25V
PC8109 10UF/25V
PU8101A
MAX17480GTL+
+CPU_VDDNB
Imax=3A
PL8104 2.2UH 20mohm
PC8116 22UF/6.3V
PC8117 22UF/6.3V
PC8118 22UF/6.3V
PC8119 0.22UF/25V
PR8123 1KOhm
PC8113 1000PF/50V
PC8114 0.1UF/25V
PR8124 10Ohm
PR8125 10Ohm
PC8121 1000PF/50V
PR8146 0Ohm
PR8127 5.1KOhm
PC8125 4700PF/50V
(5) CPU_VDDNB_RUN_FB_H
(30,83,86,94) CPU_VRON
PC8120 2.2UF/10V
PR8128 10KOhm
PR8131 10KOhm
PR8132 5.9KOHM
(5) CPU_SVD
(5) CPU_SVC
VRM_PWRGD (30,86)
HT_CPU_PWRGD (20)
PU8101B
MAX17480GTL+
PR8137 2KOhm
PR8138 0OHM
PC8127 4700PF/50V
PR8140 100OHM
PR8141 2KOhm
PR8142 100OHM
PC8130 1000PF/50V
(5) CPU_VDD1_RUN_FB_H
(5) CPU_VDD1_RUN_FB_L
+CPU_VDD1
PR8144 100OHM
PR8143 100OHM
PC8131 1000PF/50V
PR8145 0OHM
P_VCORE_VDDIO_10
P_NB_IN_shape
P_VCORE_IN_shape
P_VCORE1_PHASE_shape
P_VCORE2_PHASE_shape
PQ8101 RJK0355DPA-00-J0
PQ8103 RJK0349DPA
PQ8104 RJK0349DPA
PQ8105 RJK0355DPA-00-J0
PQ8106 RJK0349DPA
PQ8107 RJK0349DPA
PJP8110 SHORT_PIN
PJP8111 SHORT_PIN
PC8115 0.1UF/25V
PC8122 0.1UF/25V
PL8101 70Ohm/100Mhz
PL8102 70Ohm/100Mhz
PCE8101 15UF/25V
PC8104 10UF/25V
PC8105 1UF/25V
AC_BAT_SYS
PL8103 0.47UH 2.1mohm
PC8107 1000PF/50V
PR8116 5KOHM
PR8120 2.43KOHM
PR8122 3.48KOhm
PC8110 330PF/50V
PC8141 1000PF/50V
PC8111 0.22UF/25V
PC8140 1000PF/50V
PCE8102 220UF/2V
PCE8103 220UF/2V
+CPU_VDD0
Imax=18A
PL8105 70Ohm/100Mhz
PL8106 70Ohm/100Mhz
PCE8104 15UF/25V
PC8123 10UF/25V
PC8124 1UF/25V
PL8107 0.47UH 2.1mohm
PC8126 1000PF/50V
PR8134 1.5KOHM
PR8136 2.43KOHM
PR8139 3.48KOhm
PC8128 330PF/50V
PC8129 0.22UF/25V
PC8139 1000PF/50V
PC8138 1000PF/50V
PCE8106 220UF/2V
PCE8105 220UF/2V
+CPU_VDD1
Imax=18A
P_VCORE_CSP2_10
P_VCORE_CSN2_10
P_VCORE_CSN1_10
<Variant Name>
Title : +VCORE
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: Oemga
Rev: 1.0
Date: Wednesday, April 08, 2009
Sheet 81 of 94

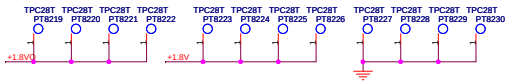


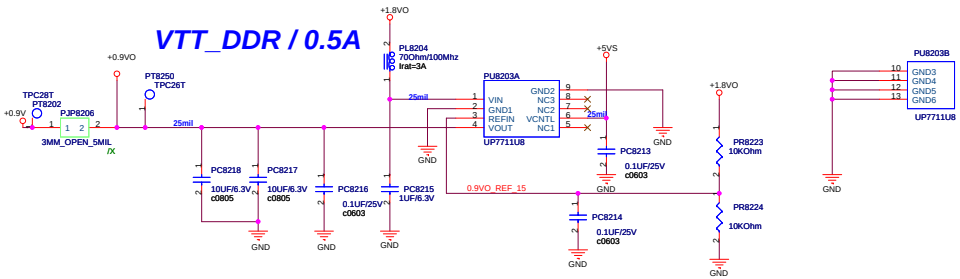
Controller

1. Voltage & Current:
   +1.8V: 8.2A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8205=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.035A
2. Ripple Current:
   Iripple=2.4A
3. Dynamic:
   Ipeak=9.5A
   ESR/2=4.5mohm
   V=42.75mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)





<Variant Name>

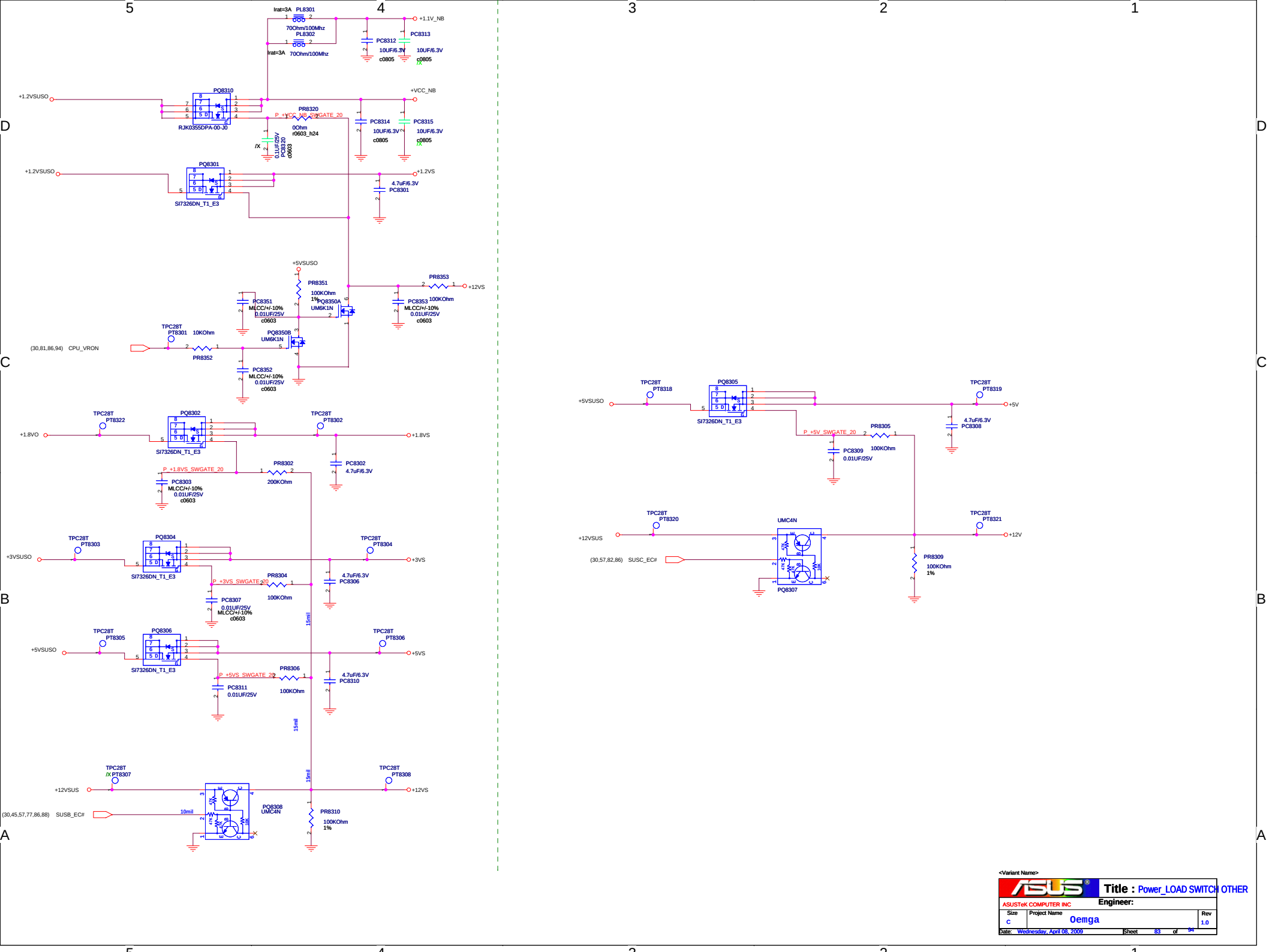
ASUSTeK COMPUTER INC

Title : Power_+1.8V&+0.9V

Engineer:

Size	Project Name	Rev
A2	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 82 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_LOAD SWITCH OTHER

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 83 of 94

<Variant Name>

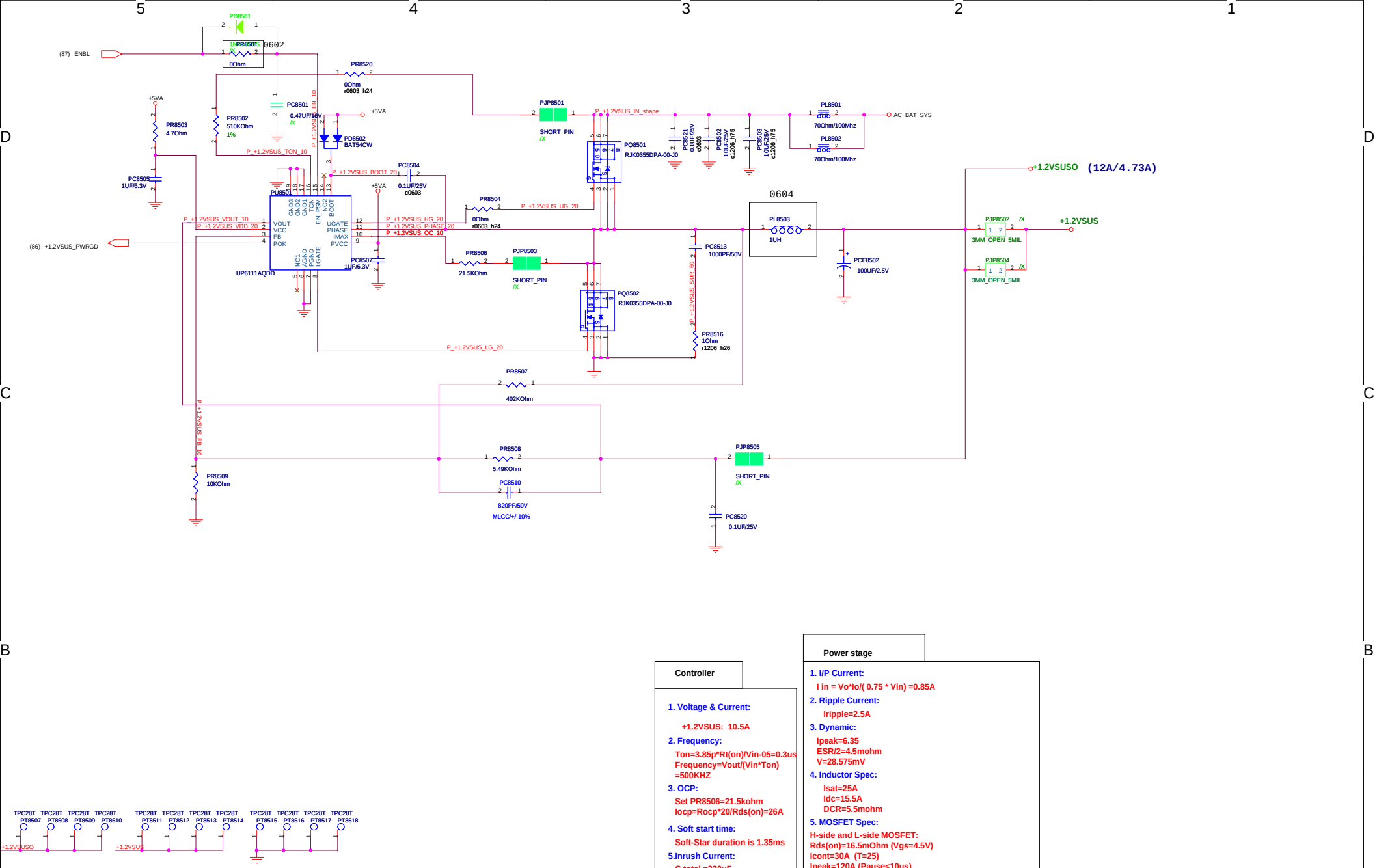
Title : Power_Charger

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Wednesday, April 08, 2009 Sheet 84 of 94



Controller

1. Voltage & Current:
   +1.2VSUS: 10.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=2.5A
3. Dynamic:
   Ipeak=6.35
   ESR/2=4.5mohm
   V=28.575mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

TPC28T PT8507 TPC28T PT8508 TPC28T PT8509 TPC28T PT8510 +1.2VSUSO
TPC28T PT8511 TPC28T PT8512 TPC28T PT8513 TPC28T PT8514 +1.2VSUS
TPC28T PT8515 TPC28T PT8516 TPC28T PT8517 TPC28T PT8518

<Variant Name>

ASUSTeK COMPUTER INC

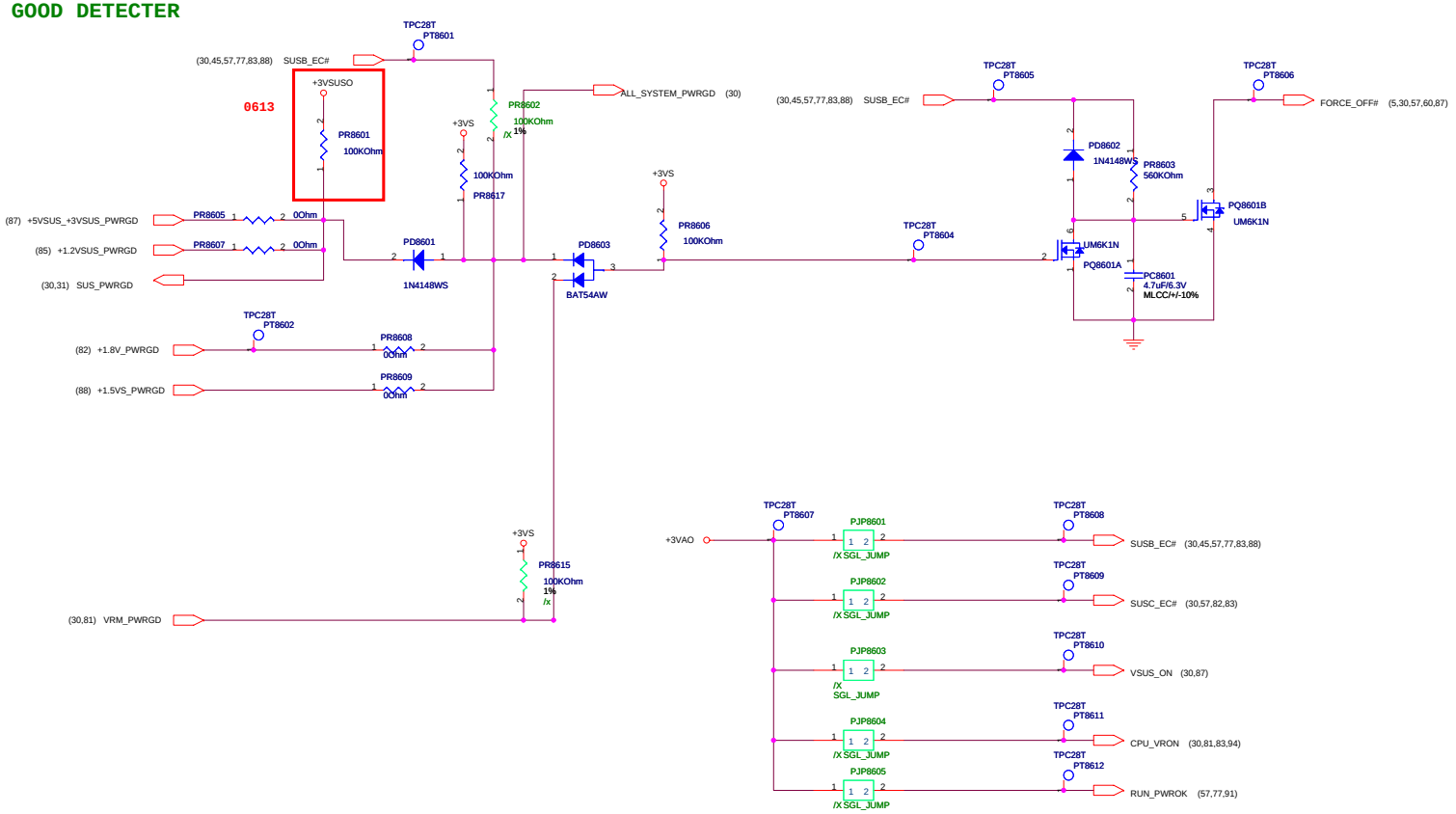
Title : Power_1.2VSUS

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

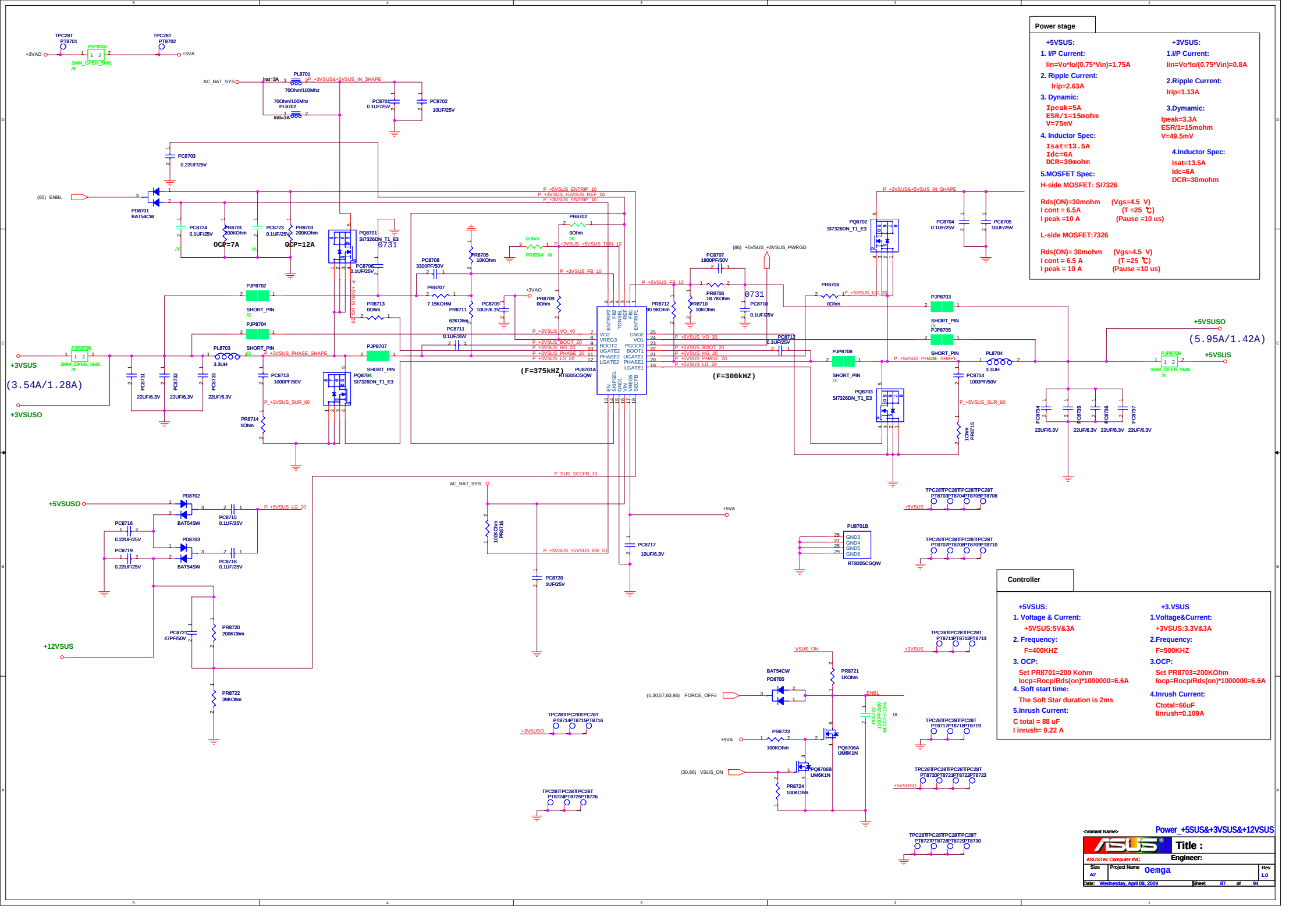
Date: Wednesday, April 08, 2009 Sheet 85 of 94

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_GOOD_DETECTER	
	Engineer:	
Size: C	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 86 of 94	


Power stage
+5VSUS:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=1.75A
2. Ripple Current:
Irip=2.63A
3. Dynamic:
Ipeak=5A
ESR/1=15mohm
V=75mV
4. Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
5.MOSFET Spec:
H-side MOSFET: SI7326
Rds(ON)=30mohm (Vgs=4.5 V)
I cont = 6.5A (T =25 ℃)
I peak =10 A (Pause =10 us)
L-side MOSFET:7326
Rds(ON)= 30mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 10 A (Pause =10 us)
+3VSUS:
1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=0.8A
2.Ripple Current:
Irip=1.13A
3.Dymamic:
Ipeak=3.3A
ESR/1=15mohm
V=49.5mV
4.Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
Controller
+5VSUS:
1. Voltage & Current:
+5VSUS:5V&3A
2. Frequency:
F=400KHZ
3. OCP:
Set PR8701=200 Kohm
Iocp=Rocp/Rds(on)*1000000=6.6A
4. Soft start time:
The Soft Star duration is 2ms
5.Inrush Current:
C total = 88 uF
I inrush= 0.22 A
+3.VSUS
1.Voltage&Current:
+3VSUS:3.3V&3A
2.Frequency:
F=500KHZ
3.OCP:
Set PR8703=200KOhm
Iocp=Rocp/Rds(on)*1000000=6.6A
4.Inrush Current:
Ctotal=66uF
Iinrush=0.109A
+3VSUS
(3.54A/1.28A)
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
OCP=7A
OCP=12A
(F=375kHZ)
(F=300kHZ)
PU8701A RT8205CGQW
PU8701B RT8205CGQW
PQ8701 SI7326DN_T1_E3
PQ8702 SI7326DN_T1_E3
PQ8703 SI7326DN_T1_E3
PQ8704 SI7326DN_T1_E3
PQ8706A UM6K1N
PQ8706B UM6K1N
PD8701 BAT54CW
PD8702 BAT54SW
PD8703 BAT54SW
PD8705 BAT54CW
AC_BAT_SYS
+3VAO
+5VA
(85) ENBL
(86) +5VSUS_+3VSUS_PWRGD
(5,30,57,60,86) FORCE_OFF#
(30,86) VSUS_ON
VSUS_ON
ENBL
P_+5VSUS_ENTRIP_10
P_+3VSUS_+5VSUS_REF_10
P_+3VSUS_ENTRIP_10
P_+3VSUS_+5VSUS_TON_10
P_+3VSUS_FB_10
P_+5VSUS_FB_10
P_+5VSUS_VO_30
P_+3VSUS_VO_40
P_+5VSUS_BOOT_20
P_+3VSUS_BOOT_20
P_+5VSUS_HG_20
P_+3VSUS_HG_20
P_+5VSUS_PHASE_20
P_+3VSUS_PHASE_20
P_+5VSUS_LG_20
P_+3VSUS_LG_20
P_SUS_SECFB_10
P_+3VSUS_+5VSUS_EN_10
P_+3VSUS&+5VSUS_IN_SHAPE
P_+5VSUS_UG_20
P_+5VSUS_PHASE_SHAPE
P_+3VSUS_SUR_60
P_+5VSUS_SUR_60
Variant Name: Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTek Computer INC.
Engineer:
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
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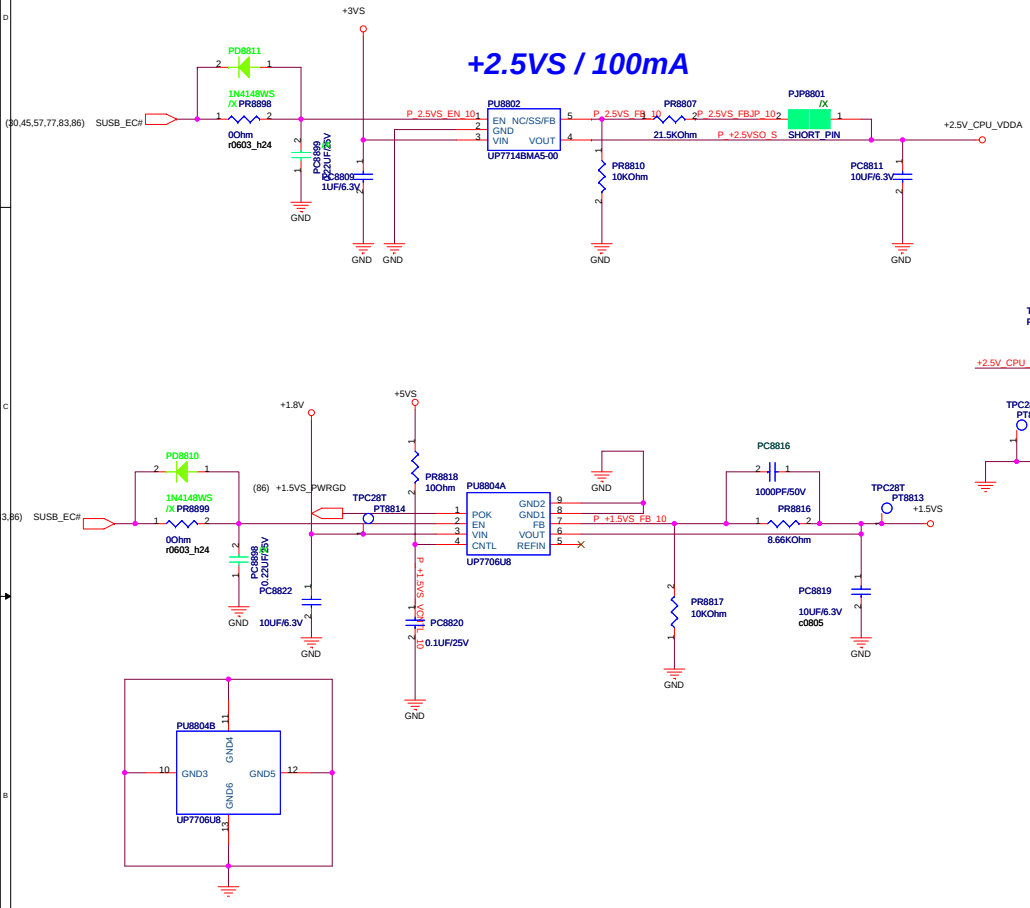
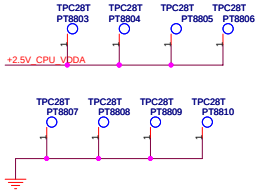




2.5V @ 0.2A

1. Dropout Voltage:

△V = 0.21V (Io =0.3A)

2. Current Limit:

I limit =320mA

3. Continue Current:

I cont = 300mA

4. Power Dissipation:

Rthjc = 250℃/W
Pd = 0.4W

5. EN Voltage:

V rising = 2V
V falling = 0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

+1.5VS @ 1.2A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =4A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc = 52℃/W
Pd =1.9W

5. EN Voltage:

V rising = 1.4V
V falling = 0.8V

6. Supply Voltage:

Vcc =5V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

<Variant Name>

Power_+2.5V&+1.5VS&+1.1V_NB

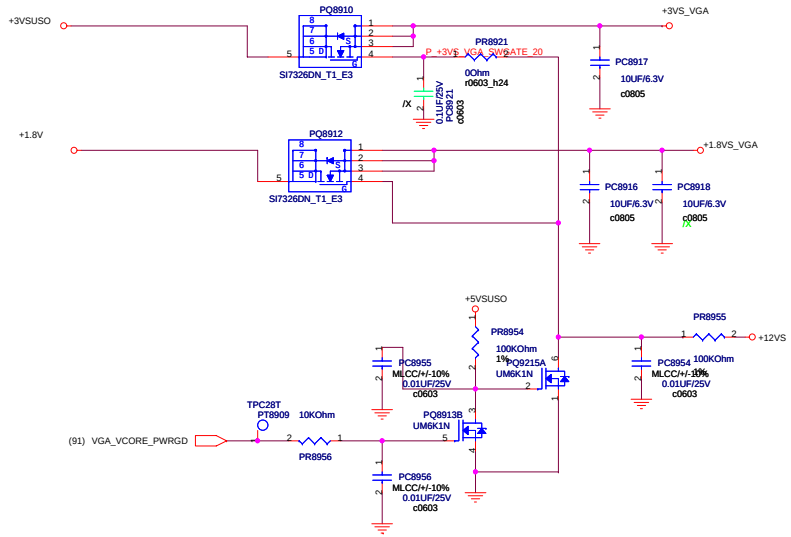
Title :

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 88 of 94



<Variant Name>

Title :

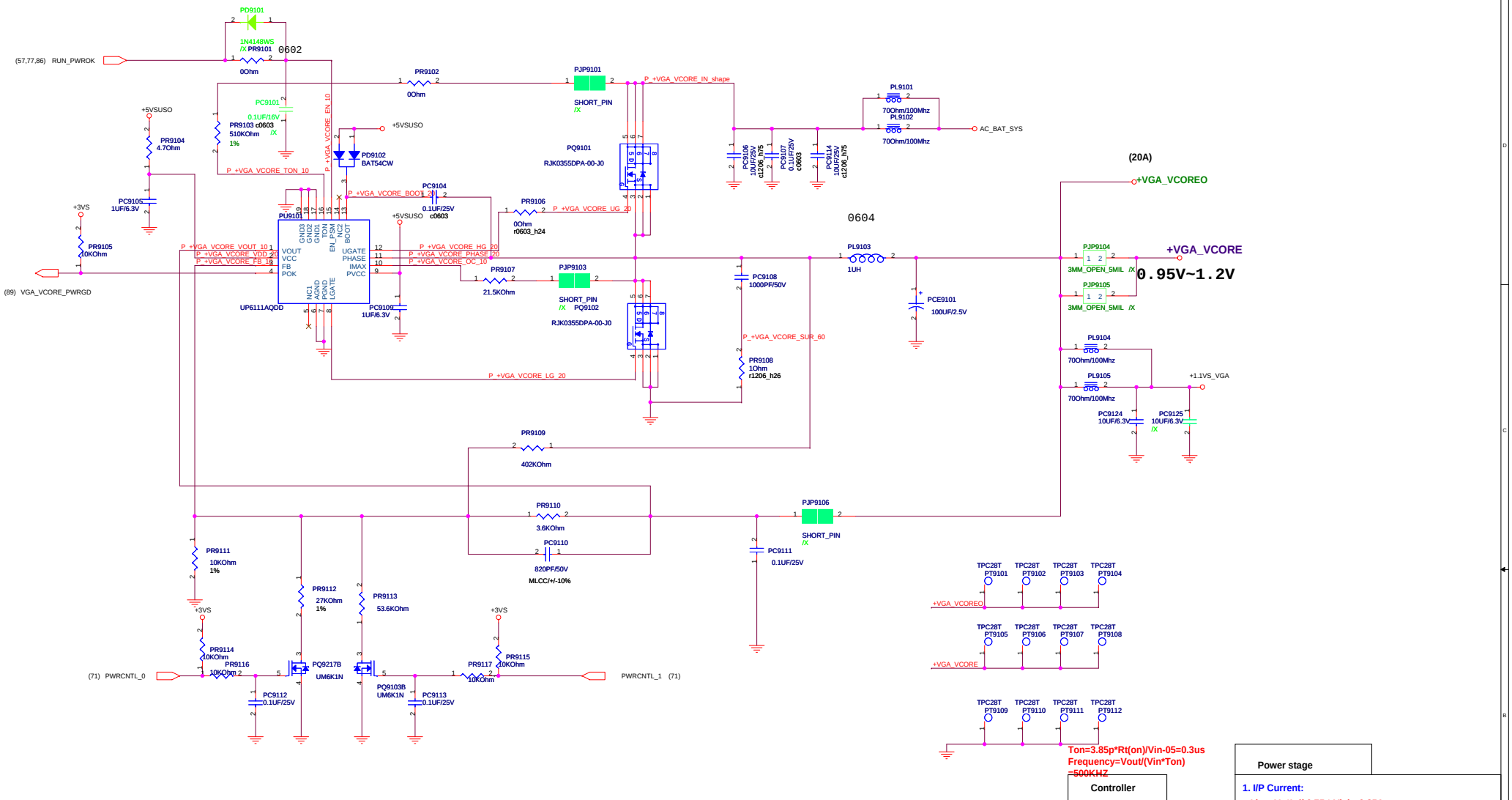
ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 89 of 94

ASUSTek Computer INC.	Title :	
	Engineer:	
Size: Custom	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 90 of 94	



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	1.02	-5%
0	1	1.071	Normal
1	0	1.12	+5%
1	1	1.171	+10%

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
~500KHZ

Controller

1. Voltage & Current:
   +1.2VSUS: 16A
2. Frequency:
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=3.74A
3. Dynamic:
   Ipeak=6.1A
   ESR/2=4.5mohm
   V=27.5mohm
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

Title : Power_+VGA_VCORE

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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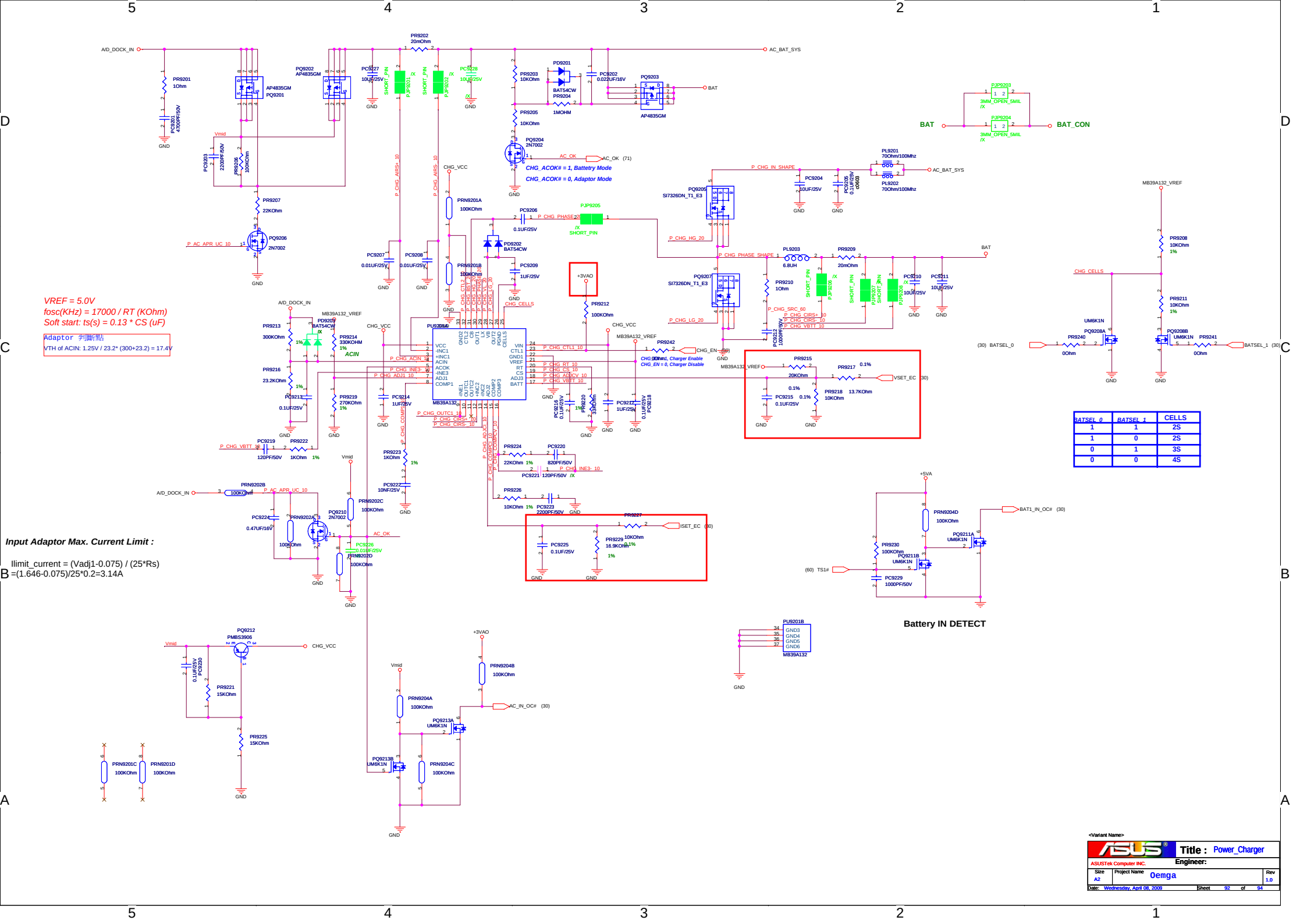
VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
Adaptor 判斷點
VTH of ACIN: 1.25V / 23.2* (300+23.2) = 17.4V
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25*0.2=3.14A
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
CHG_EN = 1, Charger Enable
CHG_EN = 0, Charger Disable
ACIN
BATSEL_0 BATSEL_1 CELLS
1 1 2S
1 0 2S
0 1 3S
0 0 4S
Battery IN DETECT
Title : Power_Charger
Engineer:
ASUSTek Computer INC.
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
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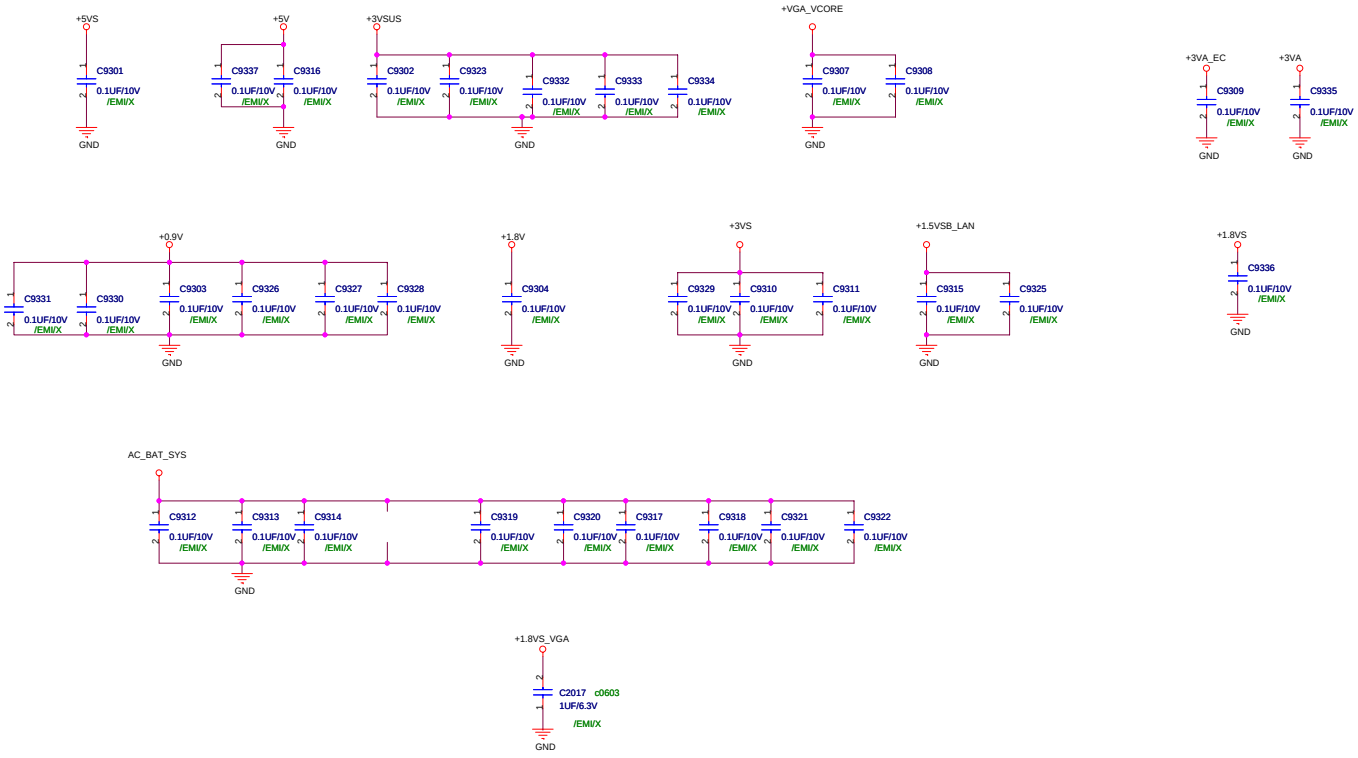
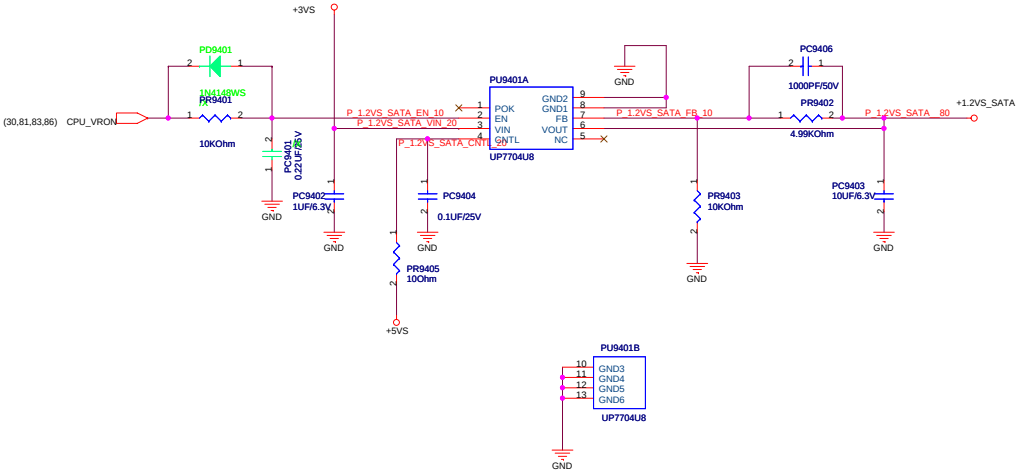


<Variant Name>

ASUSTeK COMPUTER INC	Title :
	Engineer:
Size: C	Project Name: K40AA
	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 93 of 94



+1.2VS_SATA /

220mA/350mA

1.2V @ 0.1A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =2.5A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc =52℃/W
Pd = 1.8W

5. EN Voltage:

V rising = 2V
V falling = 0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: C	Project Name: K40AA	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 94 of 94	