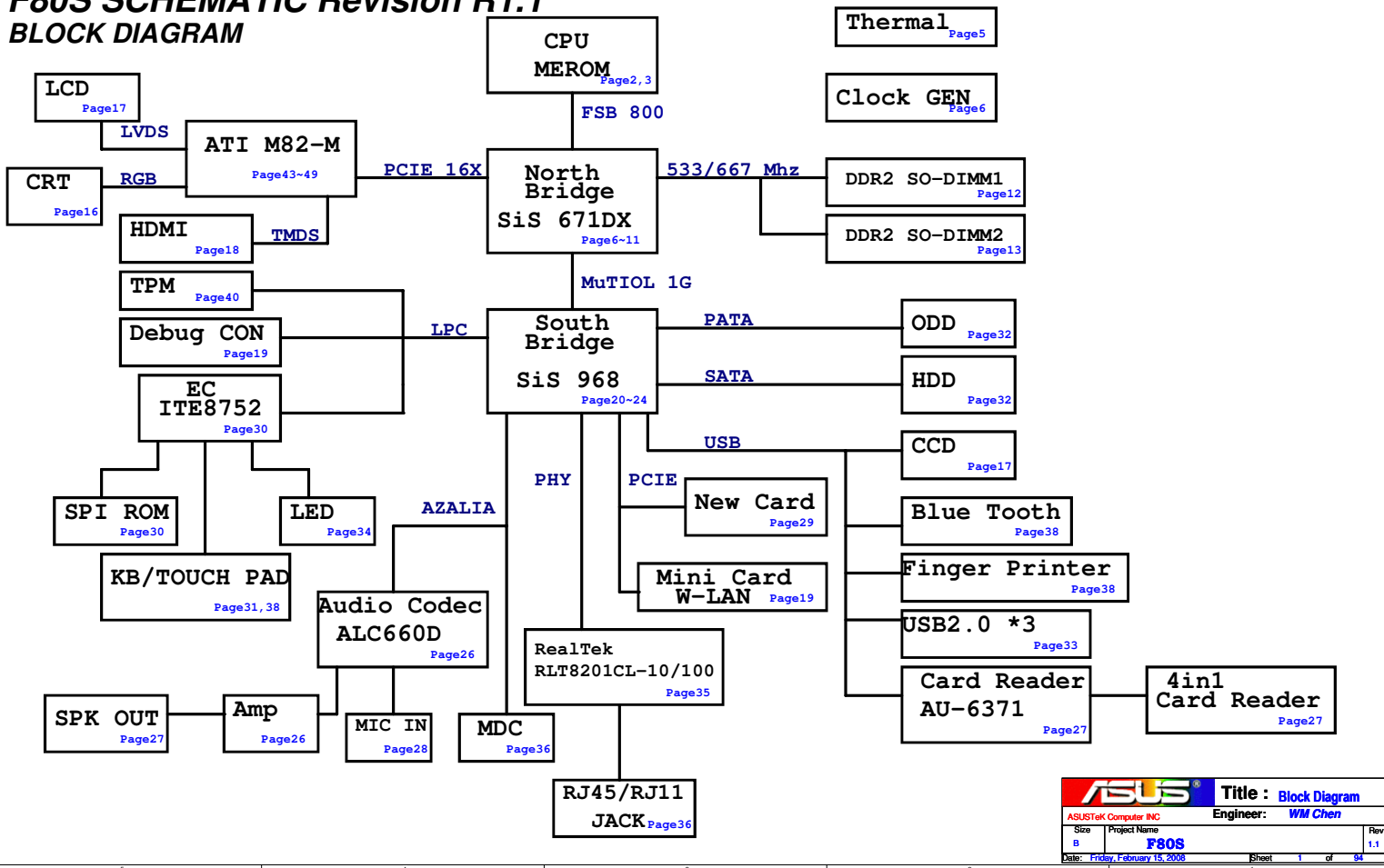
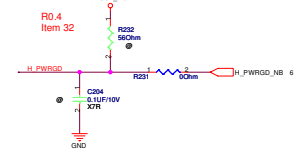
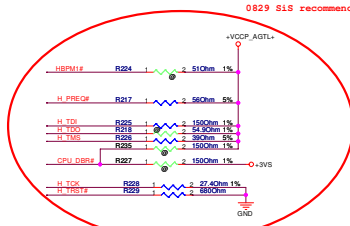
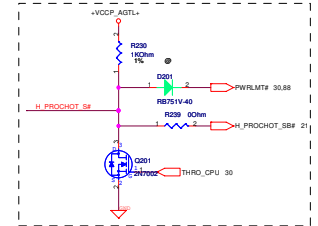
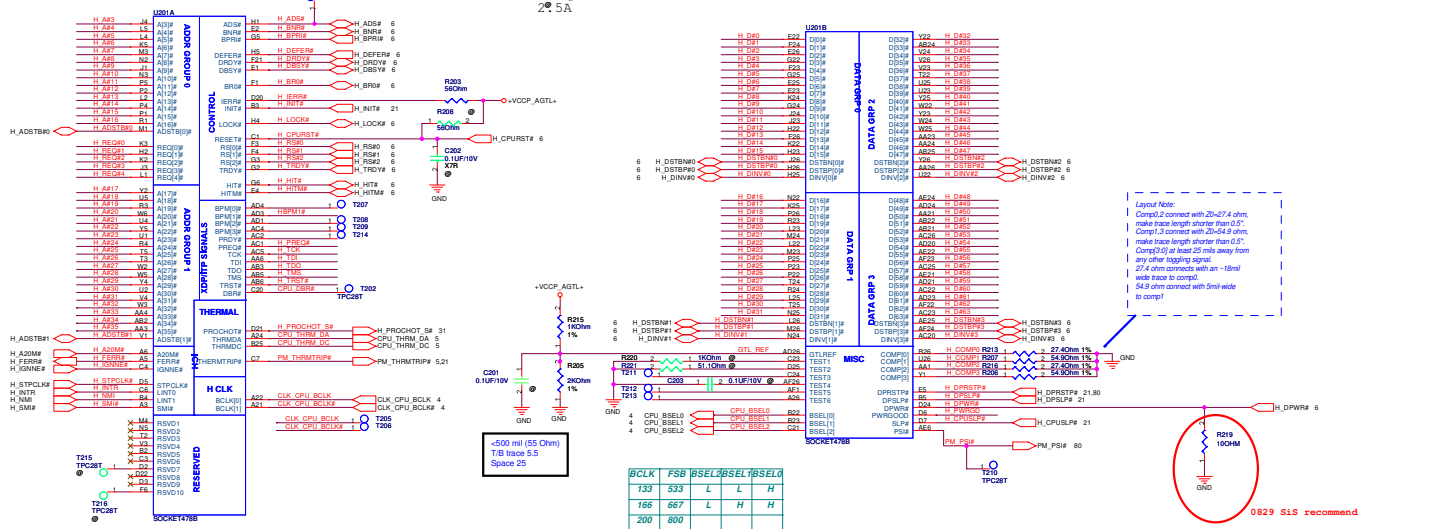
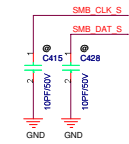
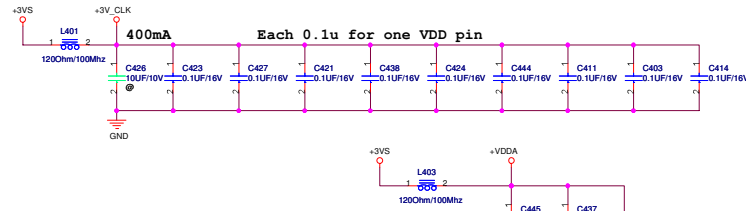
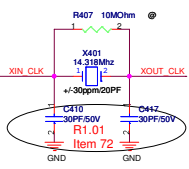


F80S SCHEMATIC Revision R1.1

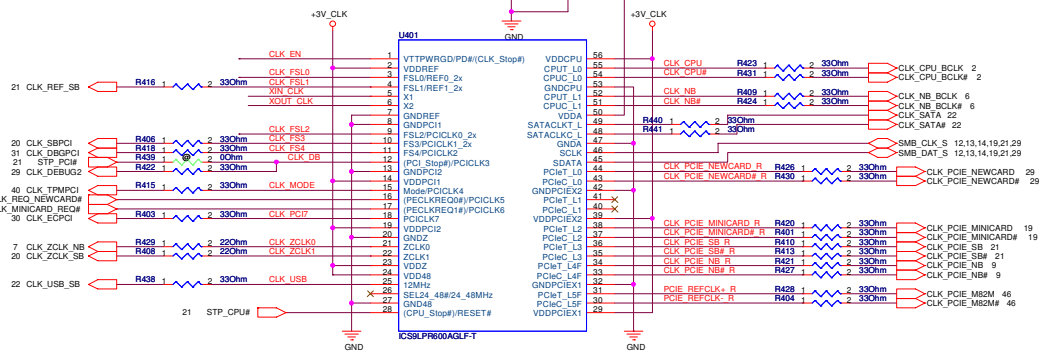
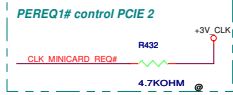
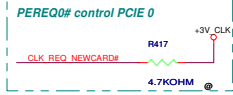
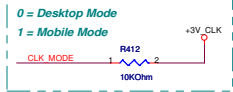
BLOCK DIAGRAM



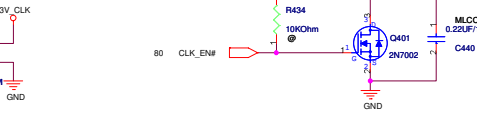
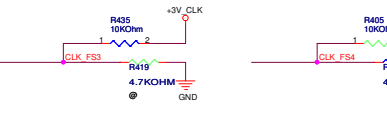
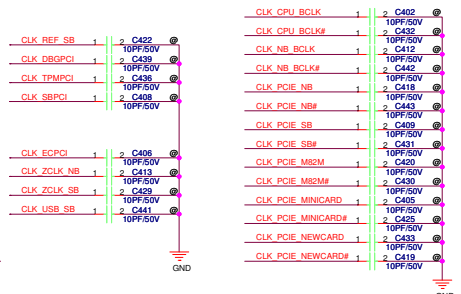
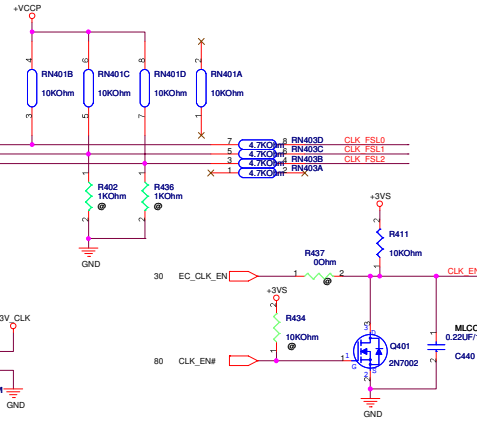




CLK_MODE

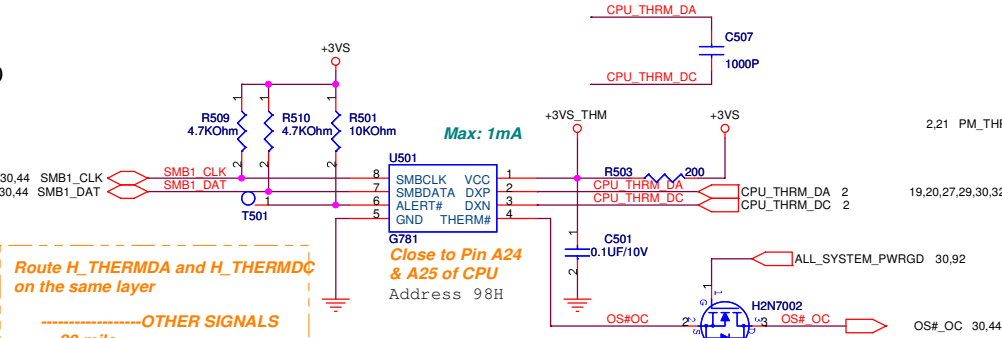


FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



ASUS Title : Clock GEN
 ASUSTek Computer Inc Engineer: **WM Chen**
 Size Project Name
 A3 F80S
 Date: Wednesday, February 13, 2008 Sheet 4 of 94

CPU Thermal Sensor

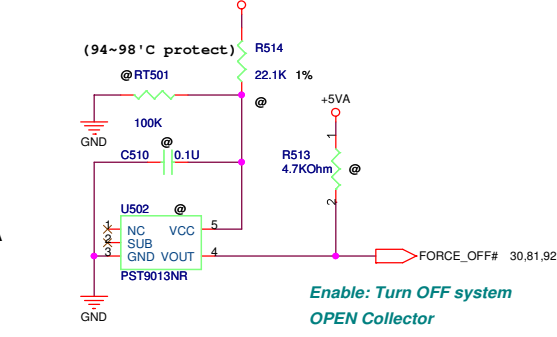


Route H_THERMDA and H_THERMDC on the same layer

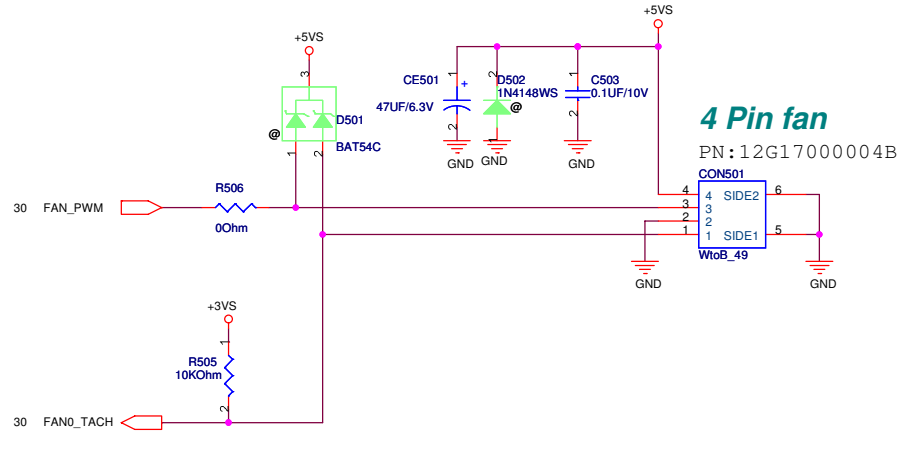
- OTHER SIGNALS
- 20 mils
- =====GND
- 10 mils
- =====H_THERMDA(10 mils)
- 10 mils
- =====H_THERMDC(10 mils)
- 10 mils
- =====GND
- 20 mils
- OTHER SIGNALS

Avoid FSB, Power

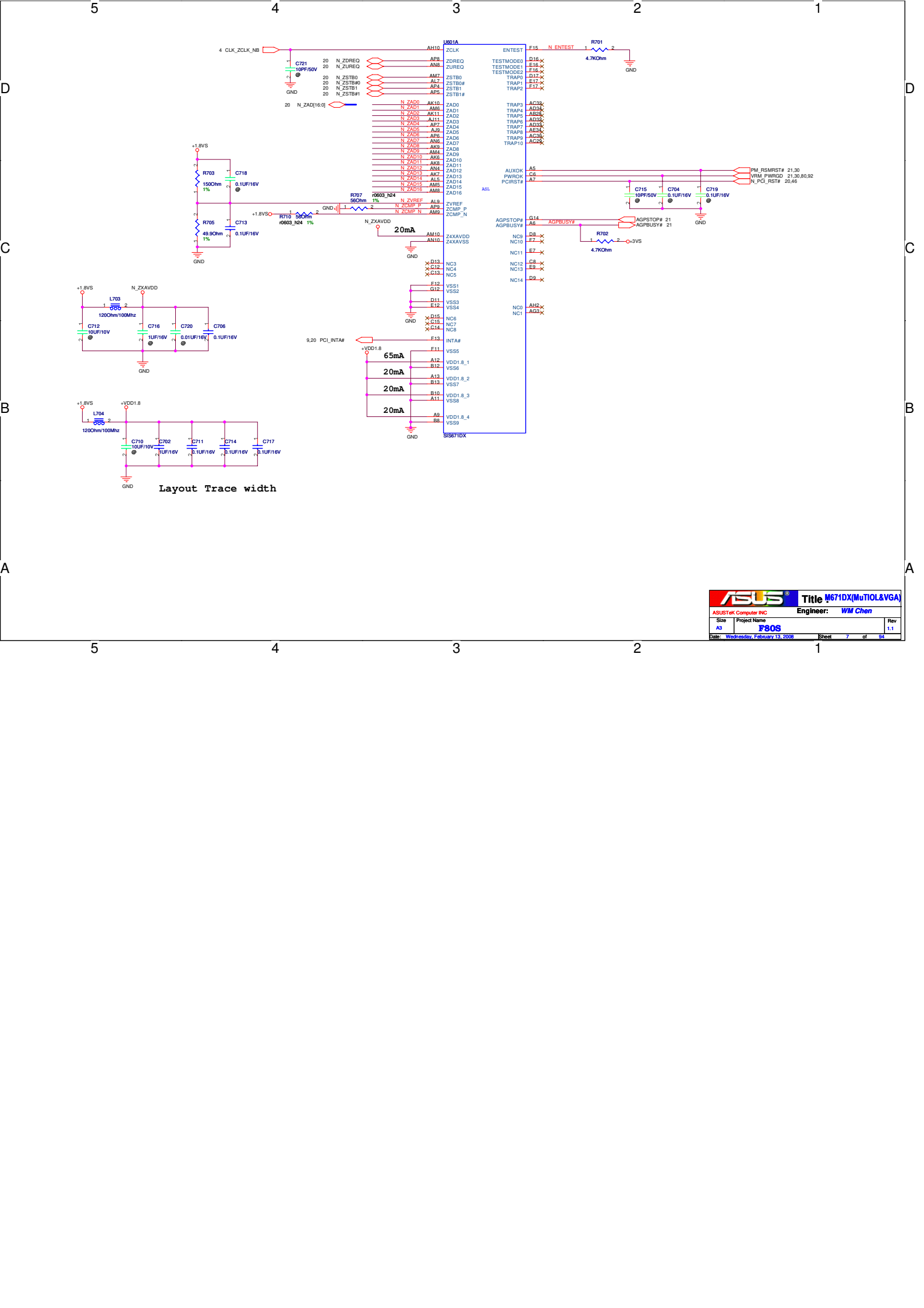
H/W Thermal Protect



DC FAN Control

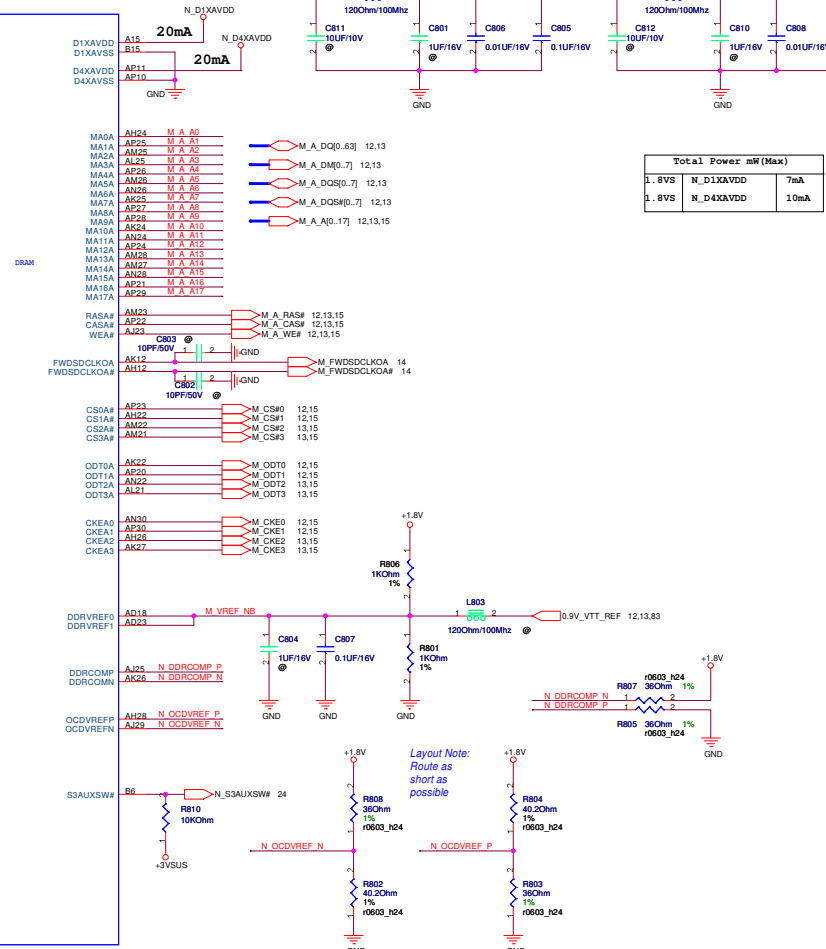


ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet	5 of 94



Layout Trace width

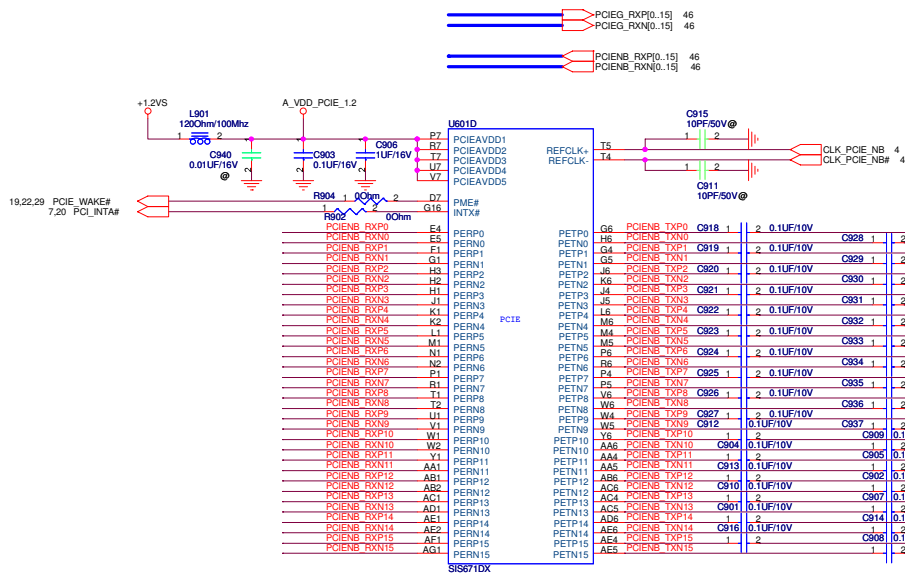
M_A_DQ00	AD0A	MD0A
M_A_DQ01	AD0B	MD0B
M_A_DQ02	AG04	MD2A
M_A_DQ03	AE02	MD5A
M_A_DQ04	AE02	MD5A
M_A_DQ05	AE02	MD5A
M_A_DQ06	AE02	MD5A
M_A_DQ07	AE02	MD5A
M_A_DQ08	AE02	MD5A
M_A_DQ09	AE02	MD5A
M_A_DQ10	AD0B	MD0B
M_A_DQ11	AD0B	MD0B
M_A_DQ12	AE02	MD5A
M_A_DQ13	AG04	MD2A
M_A_DQ14	AE02	MD5A
M_A_DQ15	AE02	MD5A
M_A_DQ16	AE02	MD5A
M_A_DQ17	AE02	MD5A
M_A_DQ18	AE02	MD5A
M_A_DQ19	AE02	MD5A
M_A_DQ20	AE02	MD5A
M_A_DQ21	AE02	MD5A
M_A_DQ22	AE02	MD5A
M_A_DQ23	AE02	MD5A
M_A_DQ24	AE02	MD5A
M_A_DQ25	AE02	MD5A
M_A_DQ26	AE02	MD5A
M_A_DQ27	AE02	MD5A
M_A_DQ28	AE02	MD5A
M_A_DQ29	AE02	MD5A
M_A_DQ30	AE02	MD5A
M_A_DQ31	AE02	MD5A
M_A_DQ32	AE02	MD5A
M_A_DQ33	AE02	MD5A
M_A_DQ34	AE02	MD5A
M_A_DQ35	AE02	MD5A
M_A_DQ36	AE02	MD5A
M_A_DQ37	AE02	MD5A
M_A_DQ38	AE02	MD5A
M_A_DQ39	AE02	MD5A
M_A_DQ40	AE02	MD5A
M_A_DQ41	AE02	MD5A
M_A_DQ42	AE02	MD5A
M_A_DQ43	AE02	MD5A
M_A_DQ44	AE02	MD5A
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M_A_DQ96	AE02	MD5A
M_A_DQ97	AE02	MD5A
M_A_DQ98	AE02	MD5A
M_A_DQ99	AE02	MD5A
M_A_DQ100	AE02	MD5A



Total Power mW (Max)		
1.8VS	N_D1XAVDD	7mA
1.8VS	N_D4XAVDD	10mA

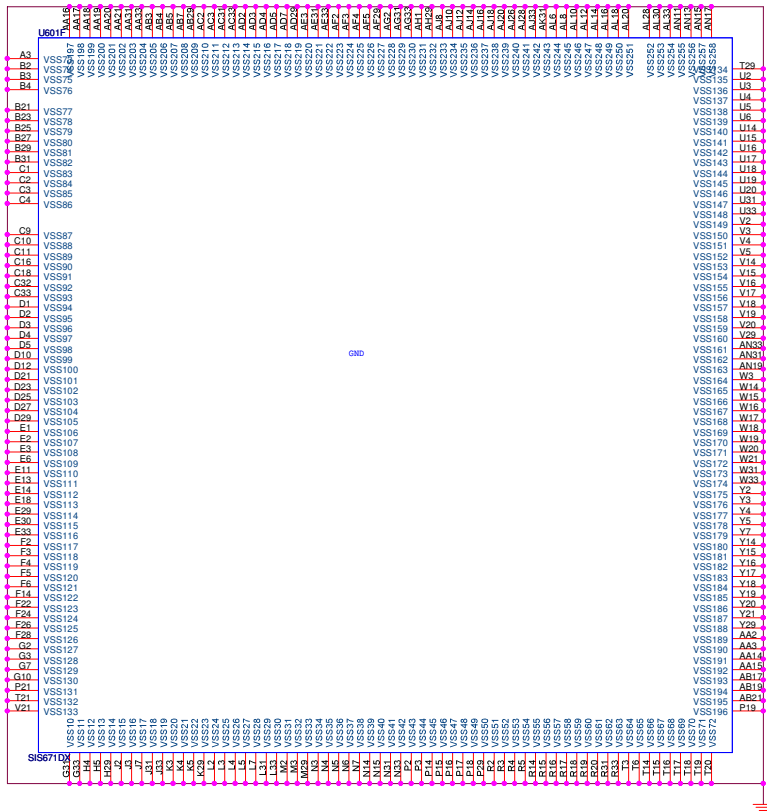
Layout Note:
Route as short as possible

ASUS Title: M671DX (DDR2)
 ASUSTek Computer INC Engineer: WM Chen
 Size A3 Project Name F80S Rev 1.1
 Date: Wednesday, February 13, 2008 Sheet 8 of 94



PERP0	G6	PCIENB_TXP0	C918	1	2	0.1UF/10V			PCIEG_RXP0				
PERP0	H6	PCIENB_TXN0					C928	1	2	0.1UF/10V	PCIEG_RXN0		
PERP1	G4	PCIENB_TXP1	C919	1	2	0.1UF/10V			PCIEG_RXP1				
PERP1	G5	PCIENB_TXN1					C929	1	2	0.1UF/10V	PCIEG_RXN1		
PERP2	J6	PCIENB_TXP2	C920	1	2	0.1UF/10V			PCIEG_RXP2				
PERP2	K6	PCIENB_TXN2					C930	1	2	0.1UF/10V	PCIEG_RXN2		
PERP3	J4	PCIENB_TXP3	C921	1	2	0.1UF/10V			PCIEG_RXP3				
PERP3	J5	PCIENB_TXN3					C931	1	2	0.1UF/10V	PCIEG_RXN3		
PERP4	L6	PCIENB_TXP4	C922	1	2	0.1UF/10V			PCIEG_RXP4				
PERP4	M6	PCIENB_TXN4					C932	1	2	0.1UF/10V	PCIEG_RXN4		
PERP5	M4	PCIENB_TXP5	C923	1	2	0.1UF/10V			PCIEG_RXP5				
PERP5	M5	PCIENB_TXN5					C933	1	2	0.1UF/10V	PCIEG_RXN5		
PERP6	P6	PCIENB_TXP6	C924	1	2	0.1UF/10V			PCIEG_RXP6				
PERP6	R6	PCIENB_TXN6					C934	1	2	0.1UF/10V	PCIEG_RXN6		
PERP7	P4	PCIENB_TXP7	C925	1	2	0.1UF/10V			PCIEG_RXP7				
PERP7	V6	PCIENB_TXN7					C935	1	2	0.1UF/10V	PCIEG_RXN7		
PERP8	W6	PCIENB_TXP8	C926	1	2	0.1UF/10V			PCIEG_RXP8				
PERP8	W5	PCIENB_TXN8					C936	1	2	0.1UF/10V	PCIEG_RXN8		
PERP9	W4	PCIENB_TXP9	C927	1	2	0.1UF/10V			PCIEG_RXP9				
PERP9	W5	PCIENB_TXN9	C912	1	2	0.1UF/10V			C937	1	2	0.1UF/10V	PCIEG_RXN9
PERP10	Y6	PCIENB_TXP10					C909				PCIEG_RXP10		
PERP10	AA6	PCIENB_TXN10	C904			0.1UF/10V					PCIEG_RXN10		
PERP11	AA4	PCIENB_TXP11					C905				PCIEG_RXP11		
PERP11	AA5	PCIENB_TXN11	C913			0.1UF/10V					PCIEG_RXN11		
PERP12	AB6	PCIENB_TXP12					C902				PCIEG_RXP12		
PERP12	AC6	PCIENB_TXN12	C910			0.1UF/10V					PCIEG_RXN12		
PERP13	AC4	PCIENB_TXP13					C907				PCIEG_RXP13		
PERP13	ACS	PCIENB_TXN13	C901			0.1UF/10V					PCIEG_RXN13		
PERP14	AD6	PCIENB_TXP14					C914				PCIEG_RXP14		
PERP14	AE6	PCIENB_TXN14	C916			0.1UF/10V					PCIEG_RXN14		
PERP15	AE4	PCIENB_TXP15					C908				PCIEG_RXP15		
PERP15	AE5	PCIENB_TXN15									PCIEG_RXN15		

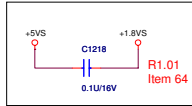
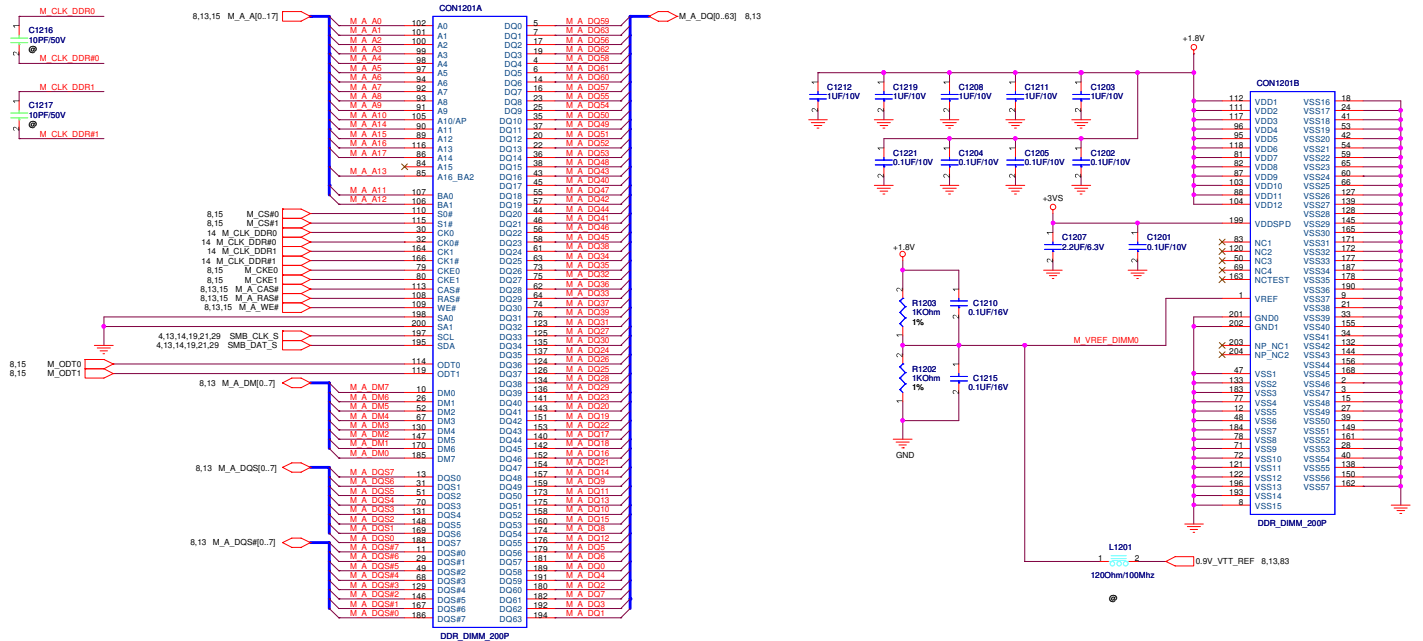
ASUS Title: M671DX (PCI-E)
 ASUSTeK Computer INC Engineer: WM Chen
 Size: Custom Project Name: F80S Rev: 1.1
 Date: Wednesday, February 13, 2008 Sheet: 8 of 94



ASUS		Title : M671DX (GND)	
ASUSTeK Computer INC		Engineer: WM Chen	
Size	Project Name	Rev 1.1	
Custom	F80S		
Date: Wednesday, January 30, 2008		Sheet	11 of 94

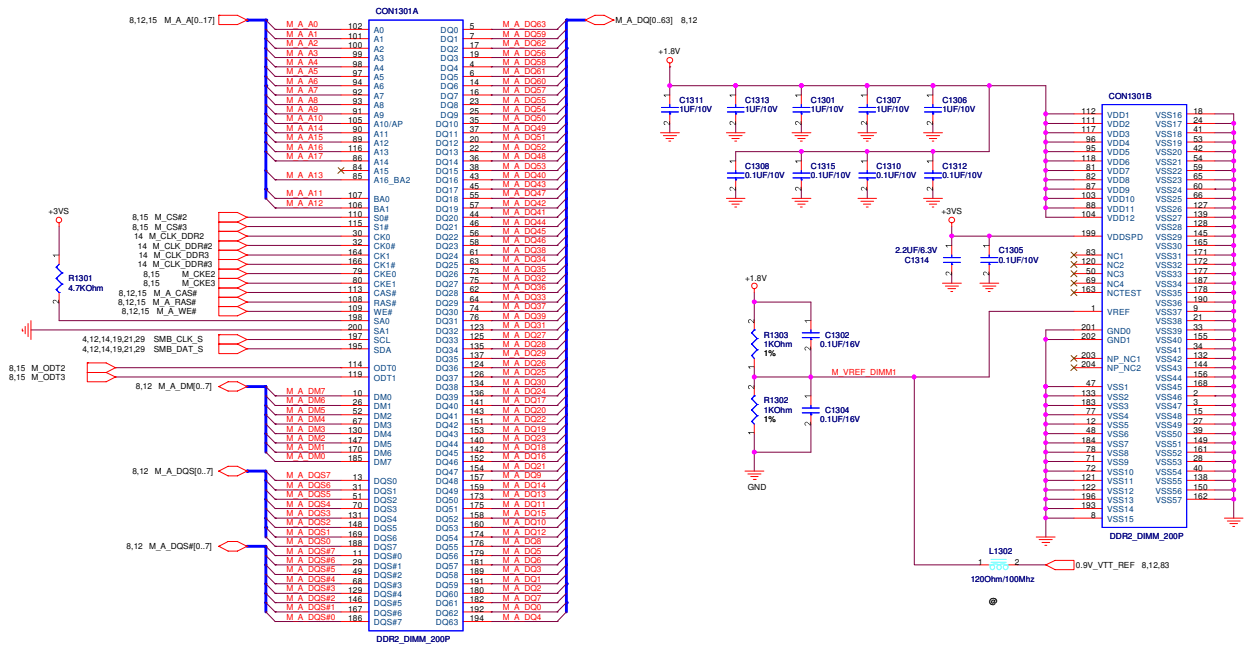
Reverse Type

R0.4
Item 30
P/N : 12G025122006 H:5.2mm

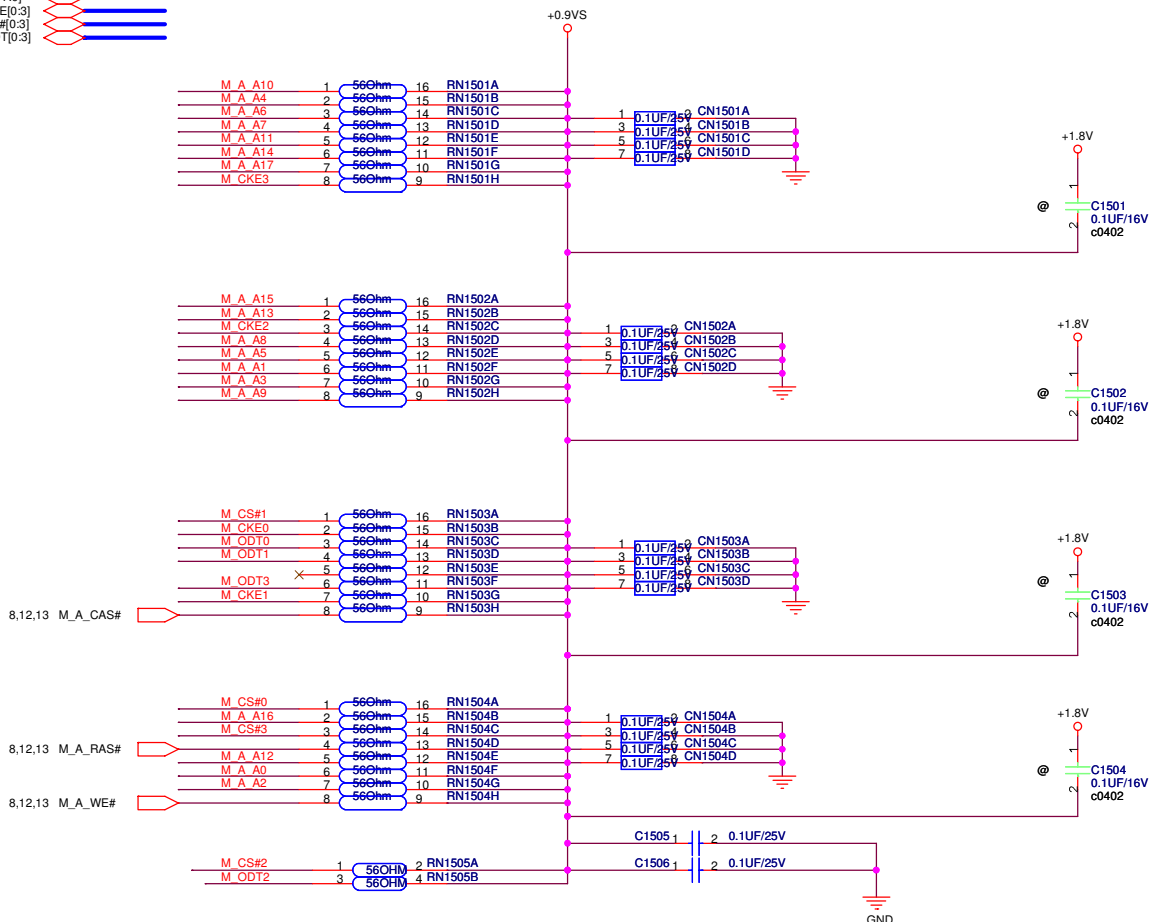


ASUS Title : DDR2 SO-DIMM1
ASUSTek Computer INC Engineer: *WM Chen*
Size Project Name
A3 F80S
Date: Wednesday, February 13, 2008 Sheet 12 of 94

R0.4
Item 30
P/N : 12G025C22002 H:9.2mm



8,12,13 M_A_A[17:0]
 8,12,13 M_CKE[0:3]
 8,12,13 M_CS#[0:3]
 8,12,13 M_ODT[0:3]

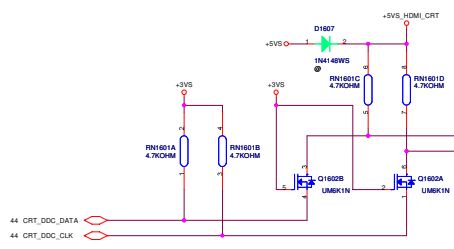
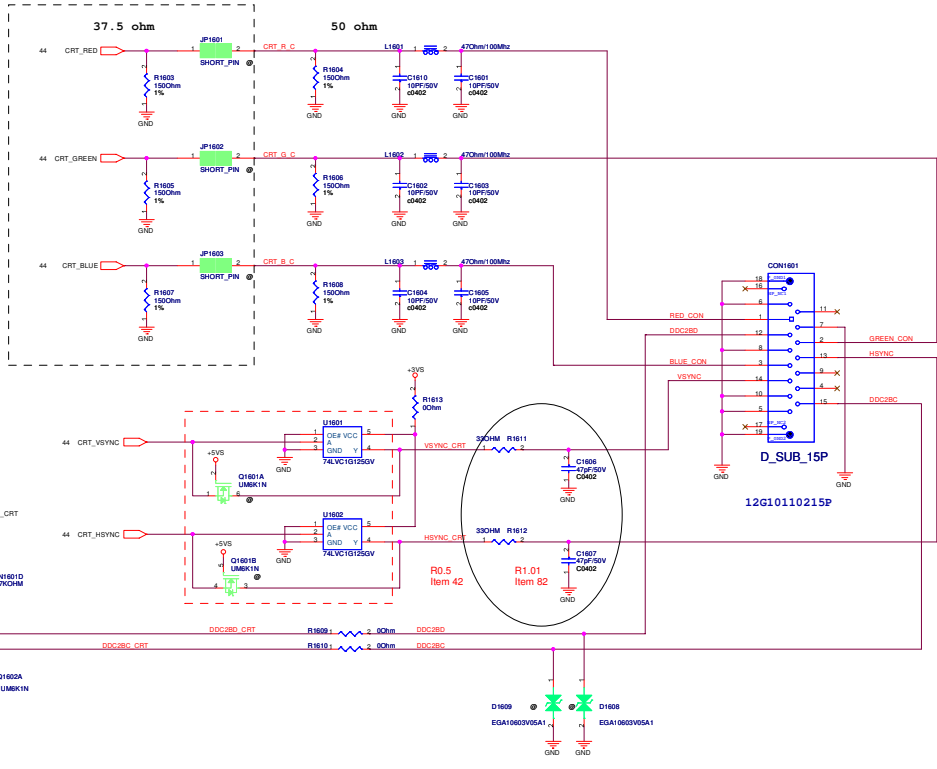
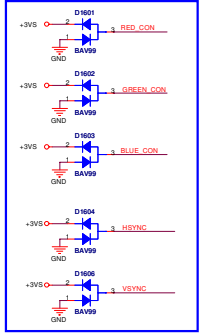


Layout note:
 Place one cap close to every 2 pull-up resistors terminated to +0.9VS

ASUS		Title : DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: <i>WM Chen</i>	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 15 of 94	

Layout note: Near U4401

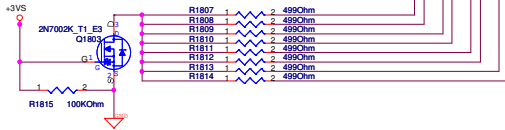
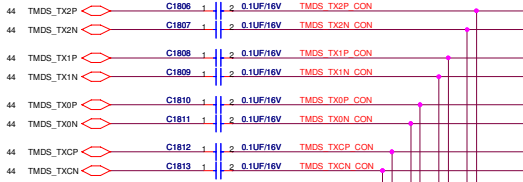
PLACE ESD Diodes near connector



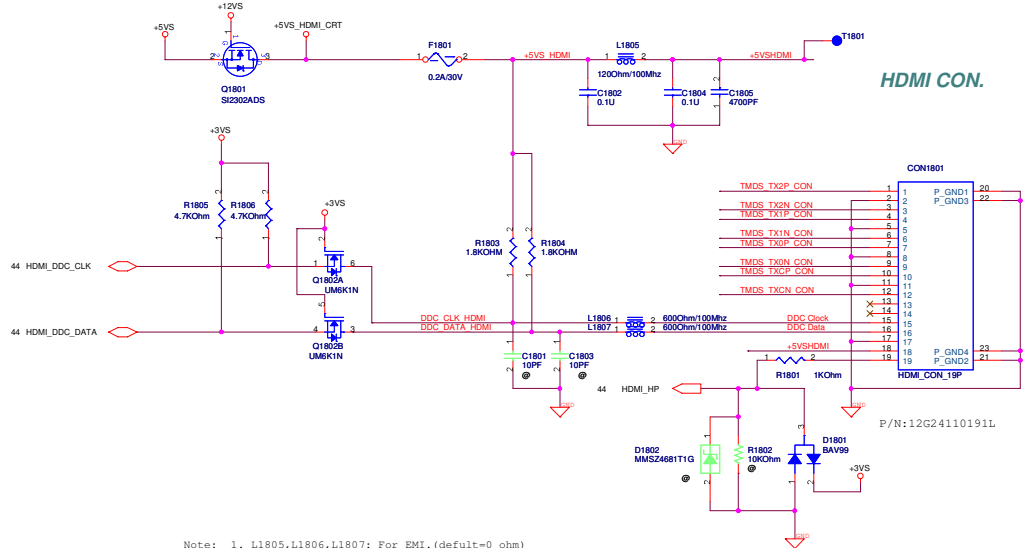
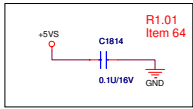
ASUS		Title : CRT	
ASUSTEK COMPUTER INC.		Engineer: WM Chen	
Size	Project Name	Rev	
C	F80S	1.1	
Date: Wednesday, February 18, 2009		Sheet: 16 of 24	

HDMI

near the HDMI connector



Reference should be +5VS, but Avl answer that +3VS is fine. As long as it can turn the MOSFET on.

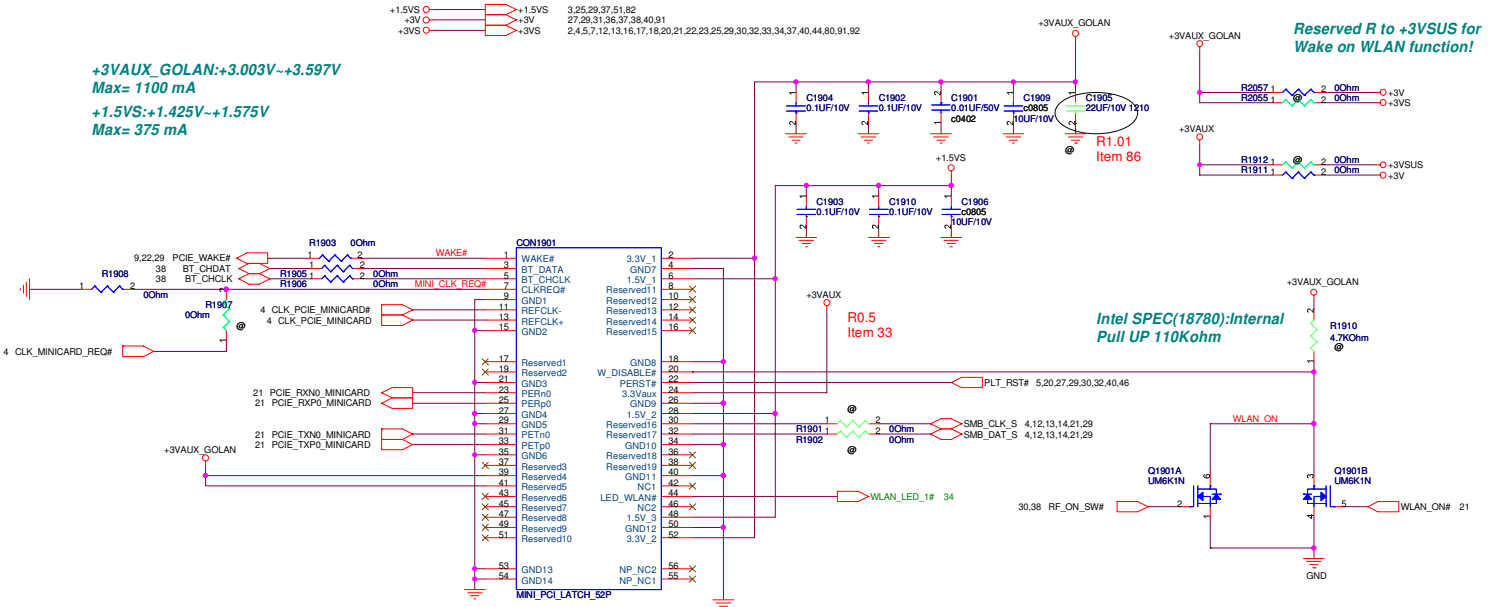


Note: 1. L1805,L1806,L1807: For EMI. (default=0 ohm)
 2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

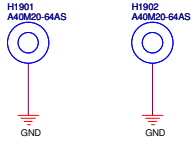
+3VAUX_GOLAN: +3.003V ~ +3.597V
Max= 1100 mA
+1.5VS: +1.425V ~ +1.575V
Max= 375 mA

+1.5VS 3,25,29,37,51,82
 +3V 27,29,31,36,37,38,40,91
 +3VS 2,4,5,7,12,13,16,17,18,20,21,22,23,25,29,30,32,33,34,37,40,44,80,91,92

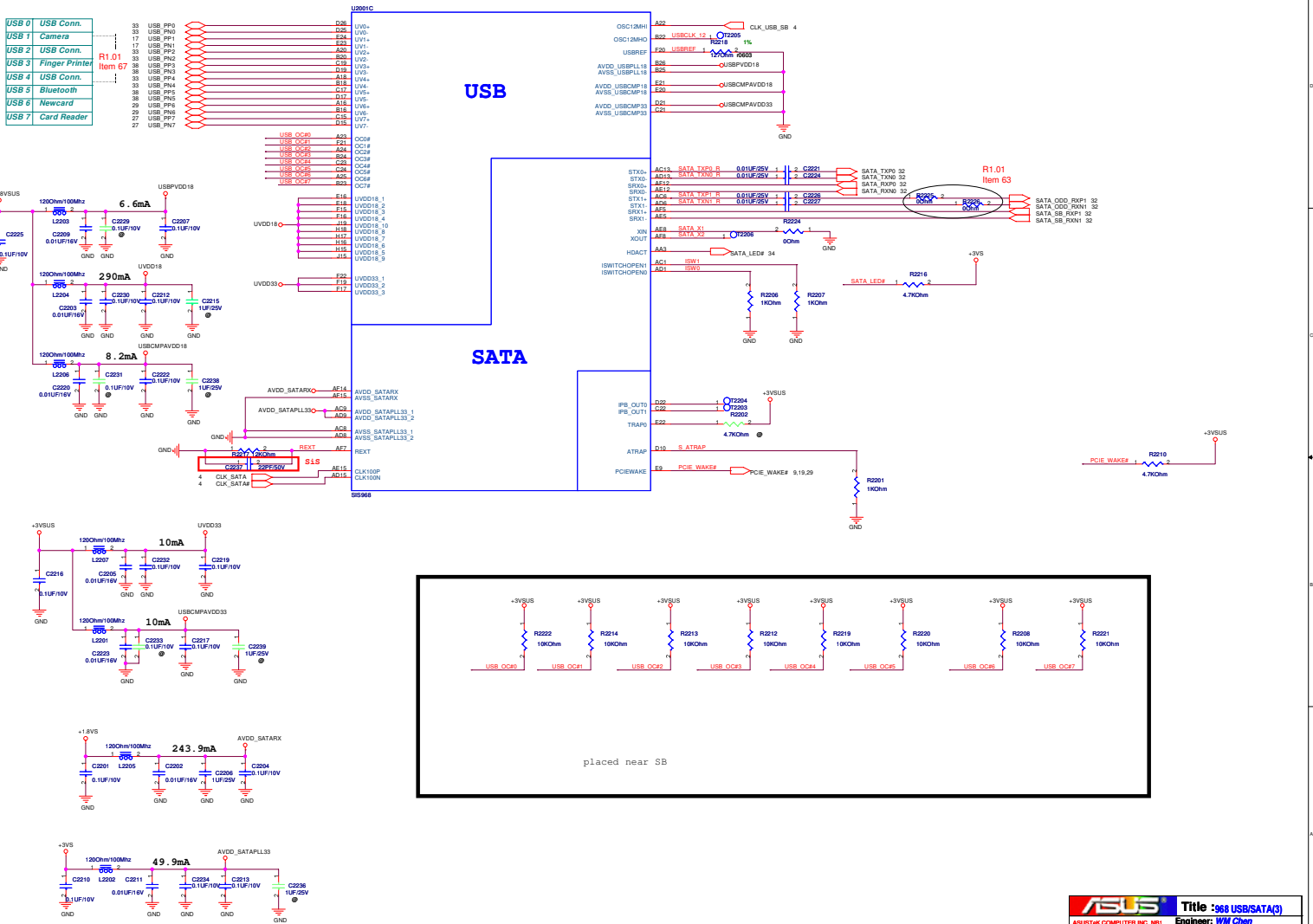
Reserved R to +3VSUS for Wake on WLAN function!

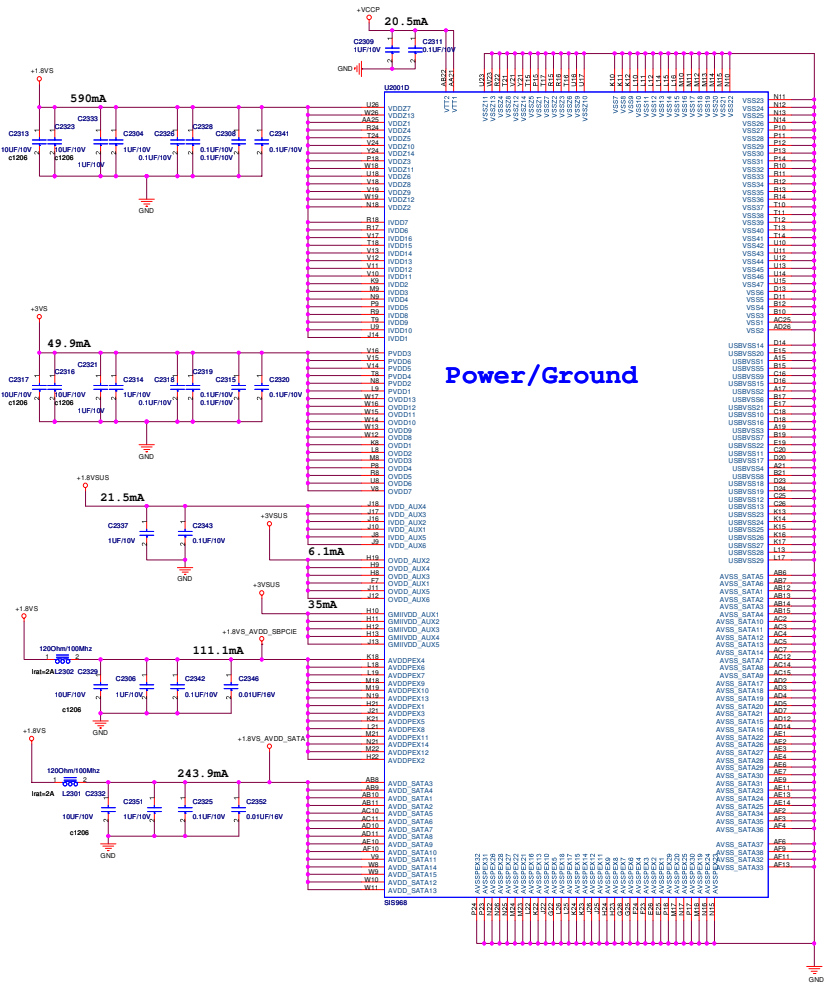


PN: 12G03000052B

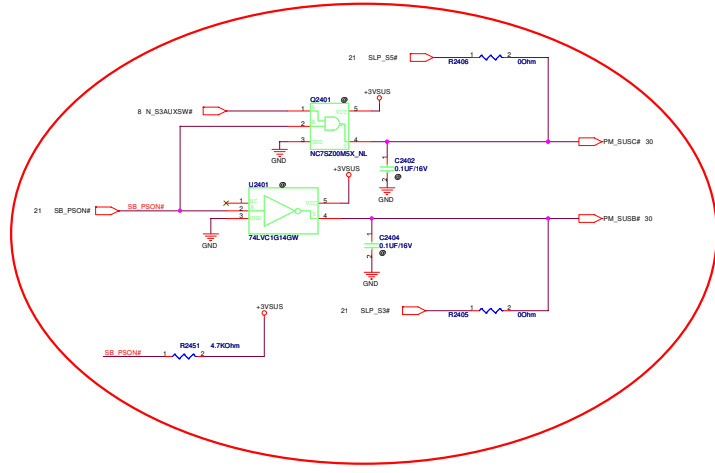


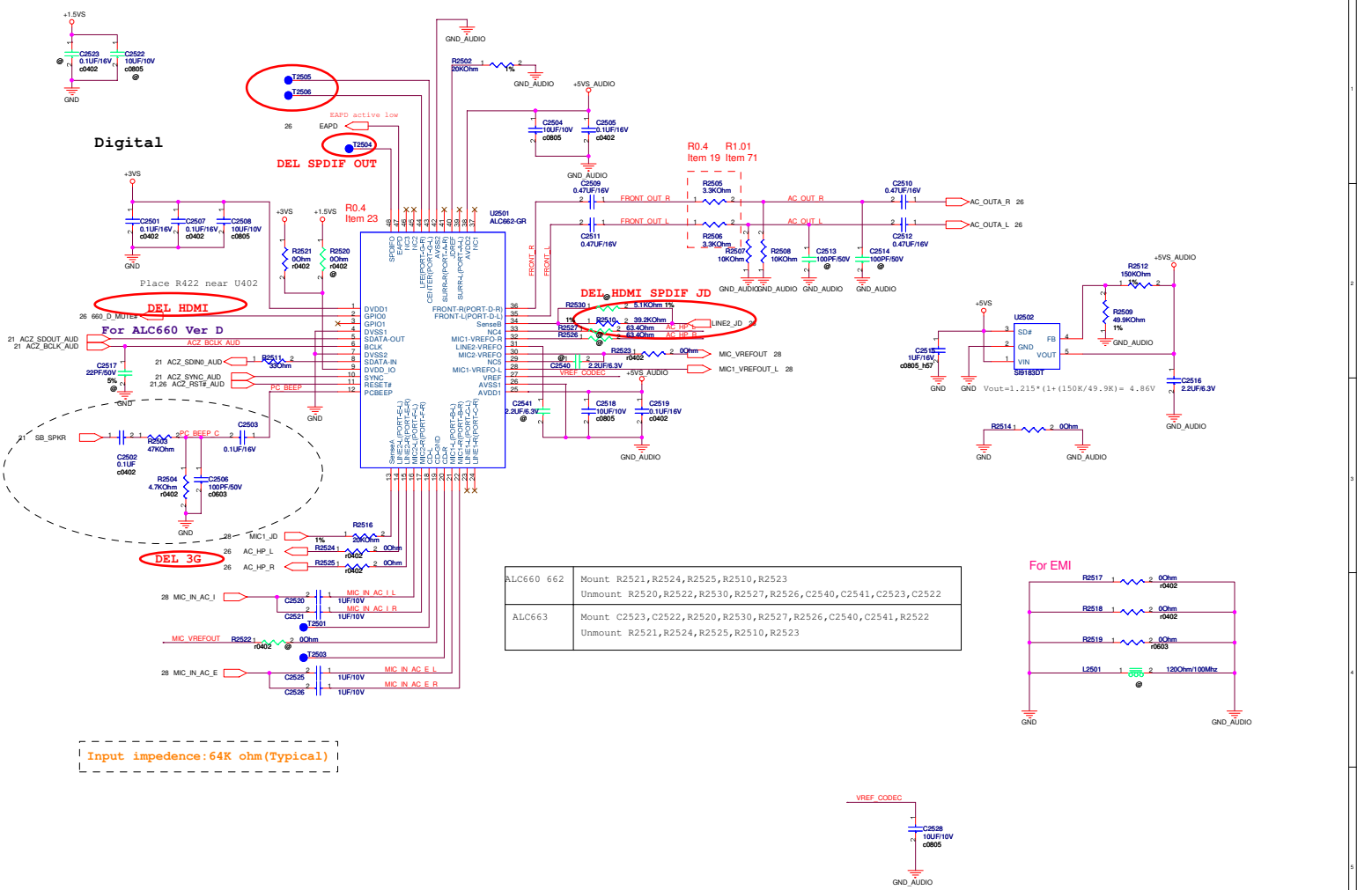
ASUS		Title : Mini card	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name	Rev	
B	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	19 of 94

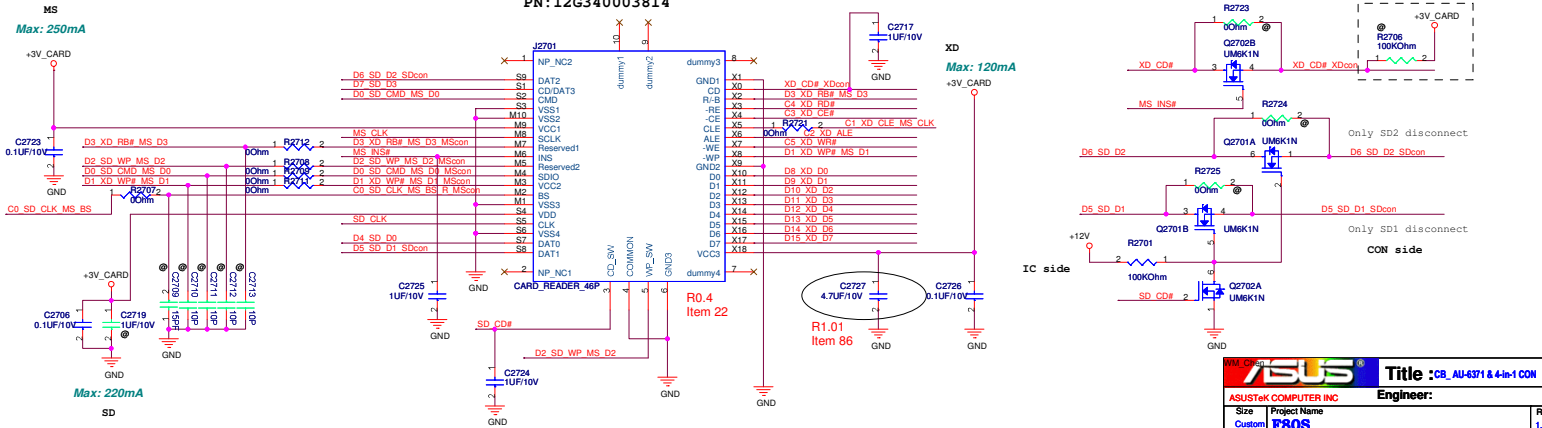
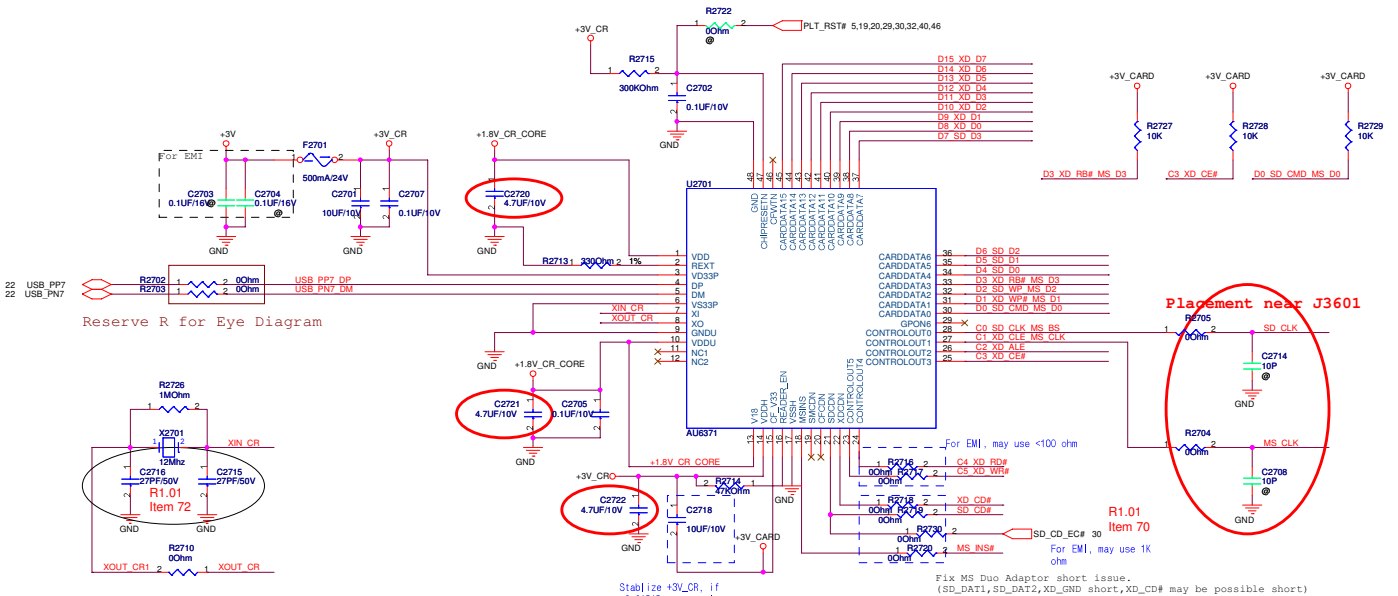




0829 SIS recommend

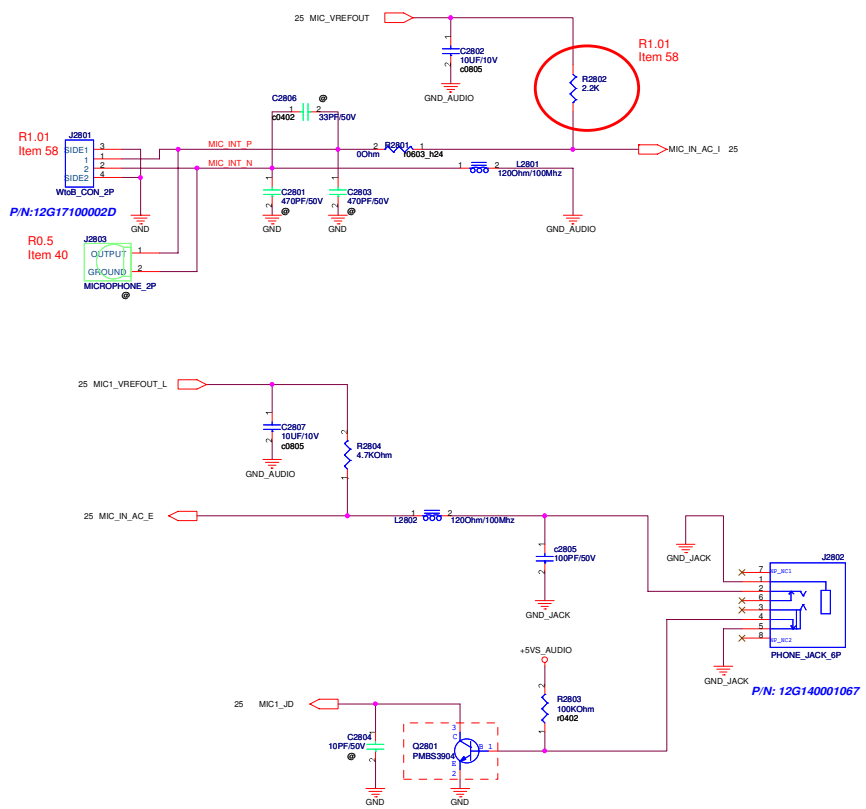






ASUS		Title : CB_AU-4371 & 4-in-1 COM	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Customer	Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008 Sheet 27 of 84			

Internal MIC Pre-Amplifier

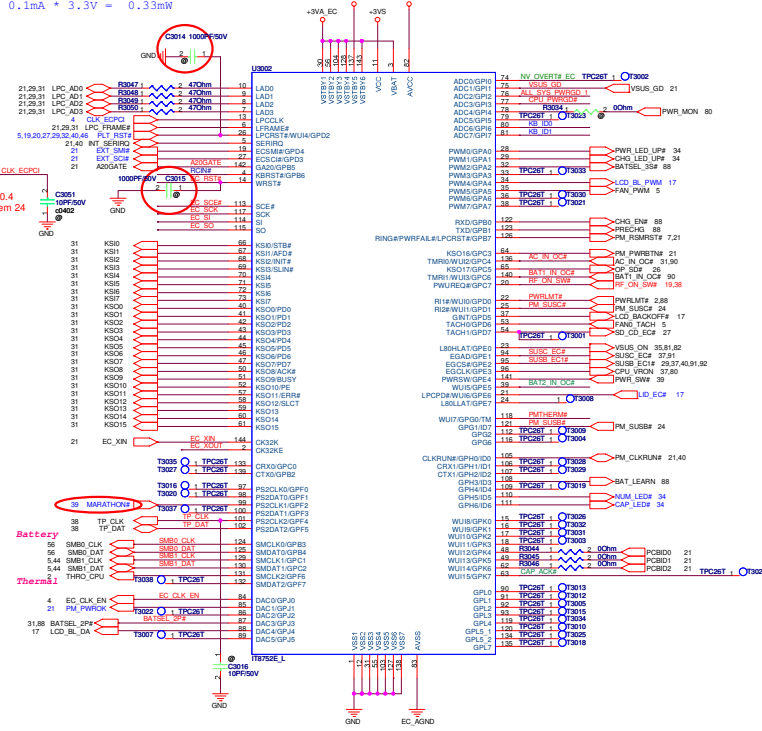


<Variant Name>

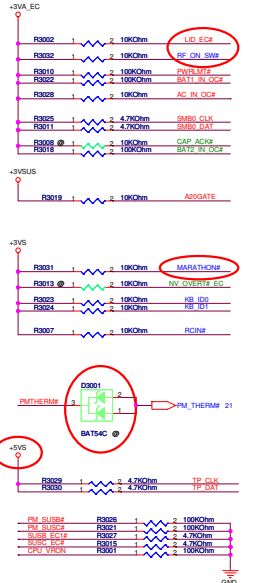
ASUS		Title : MICROPHONE
ASUSTEK COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 28 of 34

IT8752 Core Chip

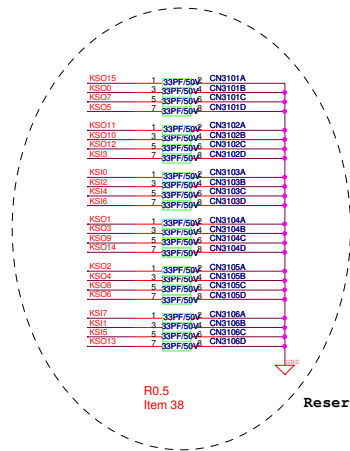
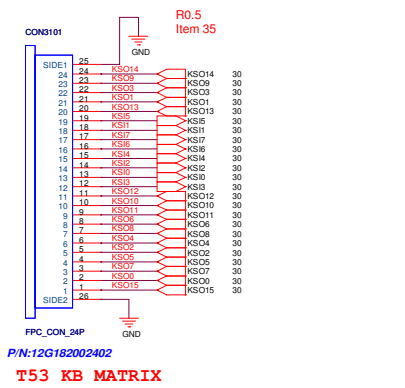
Standby (Sleep) Power Consumption:
0.1mA * 3.3V = 0.33mW



EC Pull-Up/Down

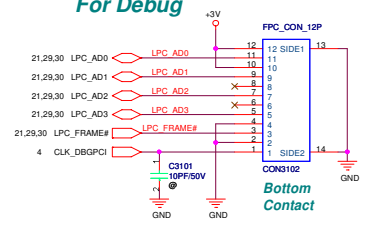


For Keyboard

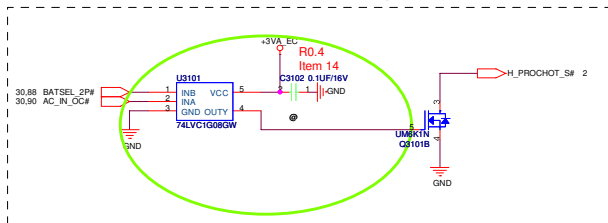


Reserve for EMI

For Debug



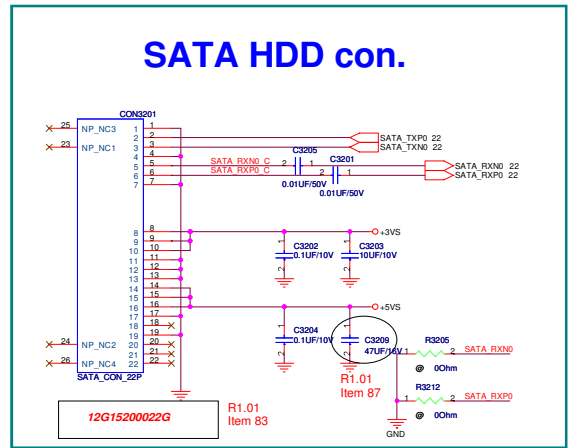
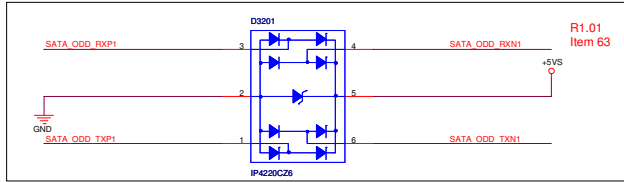
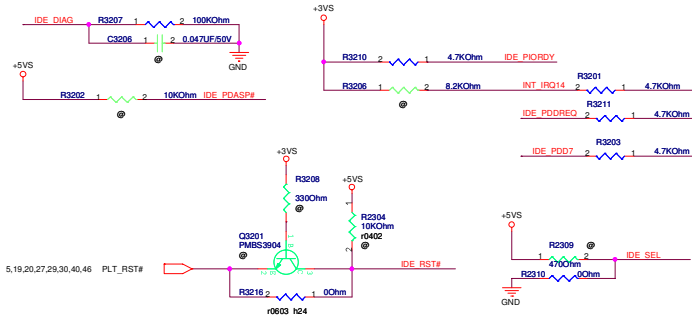
PWRLMT Circuit: For 65W adaptor.



<Variant Name>

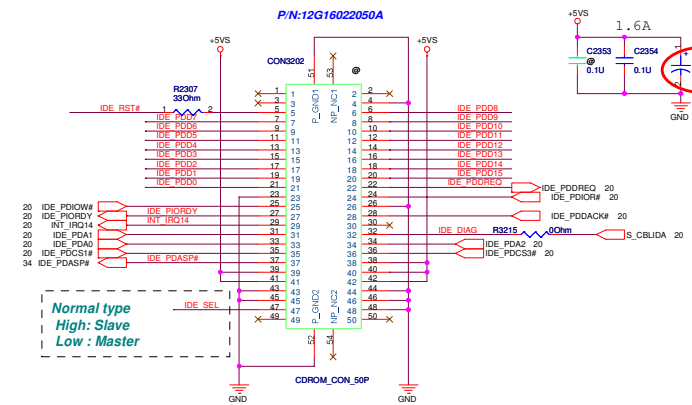
ASUS		Title : KB conn
ASUSTEK COMPUTER INC		Engineer: WM Chen
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	31 of 34





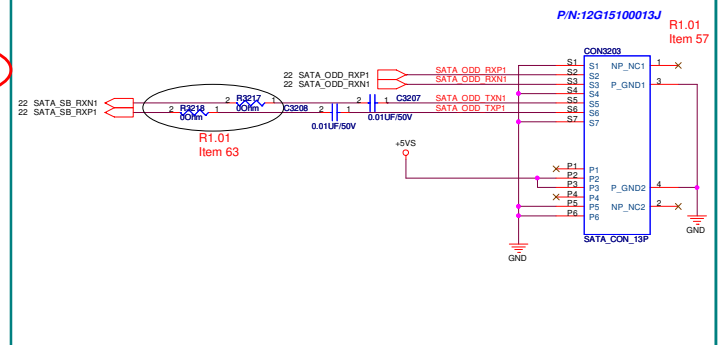
CD-ROM

PATA CD-ROM CON

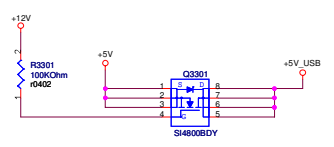
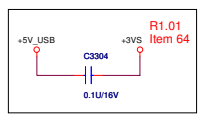
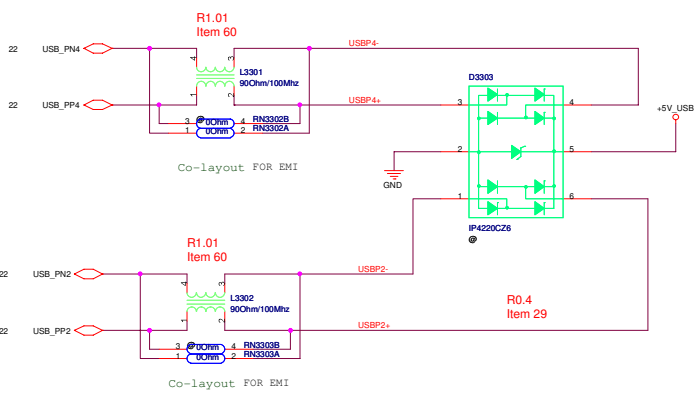


Normal type
High: Slave
Low: Master

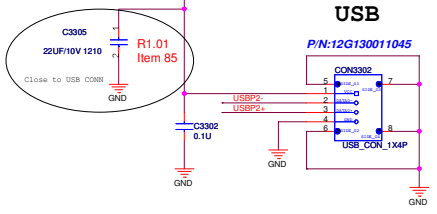
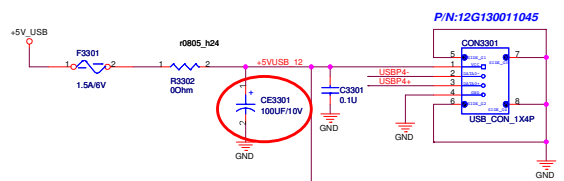
SATA CD-ROM con.



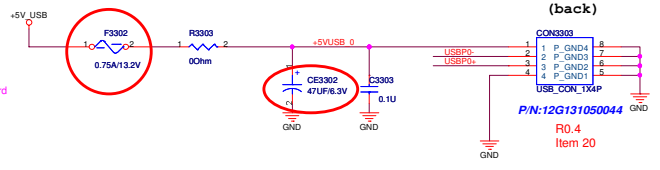
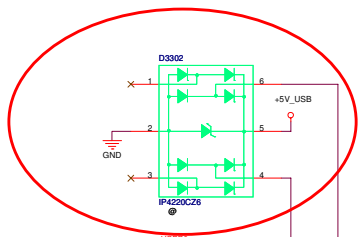
ASUS Title: HDD & CD-ROM
ASUSTEK COMPUTER INC Engineer: WM Chen
Site: Project Name: Review: 1.1
Custom: P80S
Date: Wednesday, February 13, 2008 Sheet: 32 of 34



USB



USB

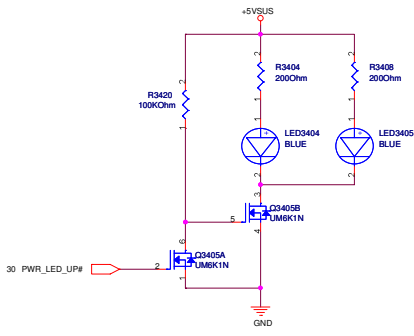


USB (back)

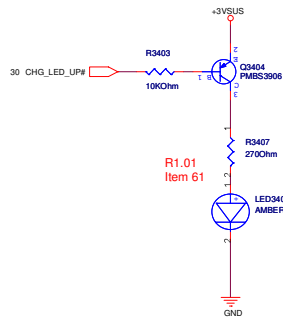
<Variant Name>

ASUS		Title : USB PORTS	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	FBOS	1.1	
Date: Wednesday, February 13, 2008		Sheet 33 of 34	

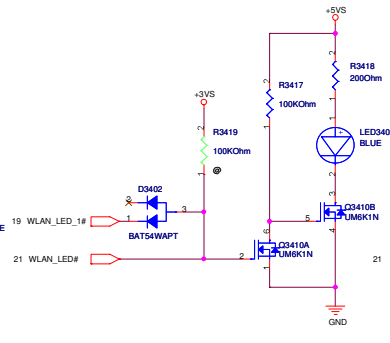
PWR LED



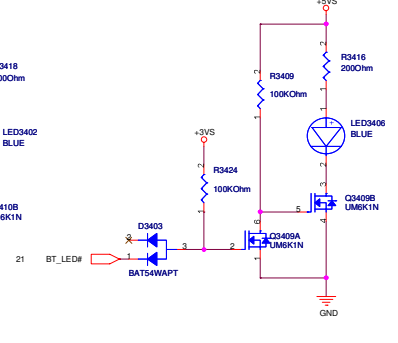
For BATTERY LED



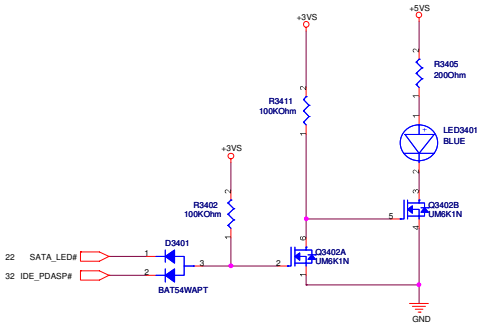
WireLess LED



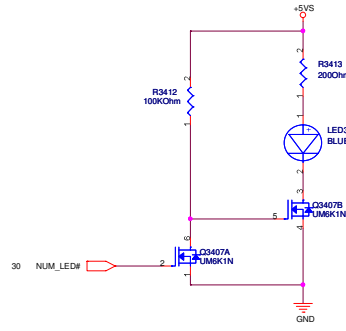
BT LED



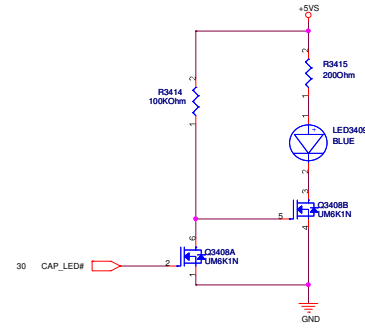
SATA/IDE LED



Num Lock

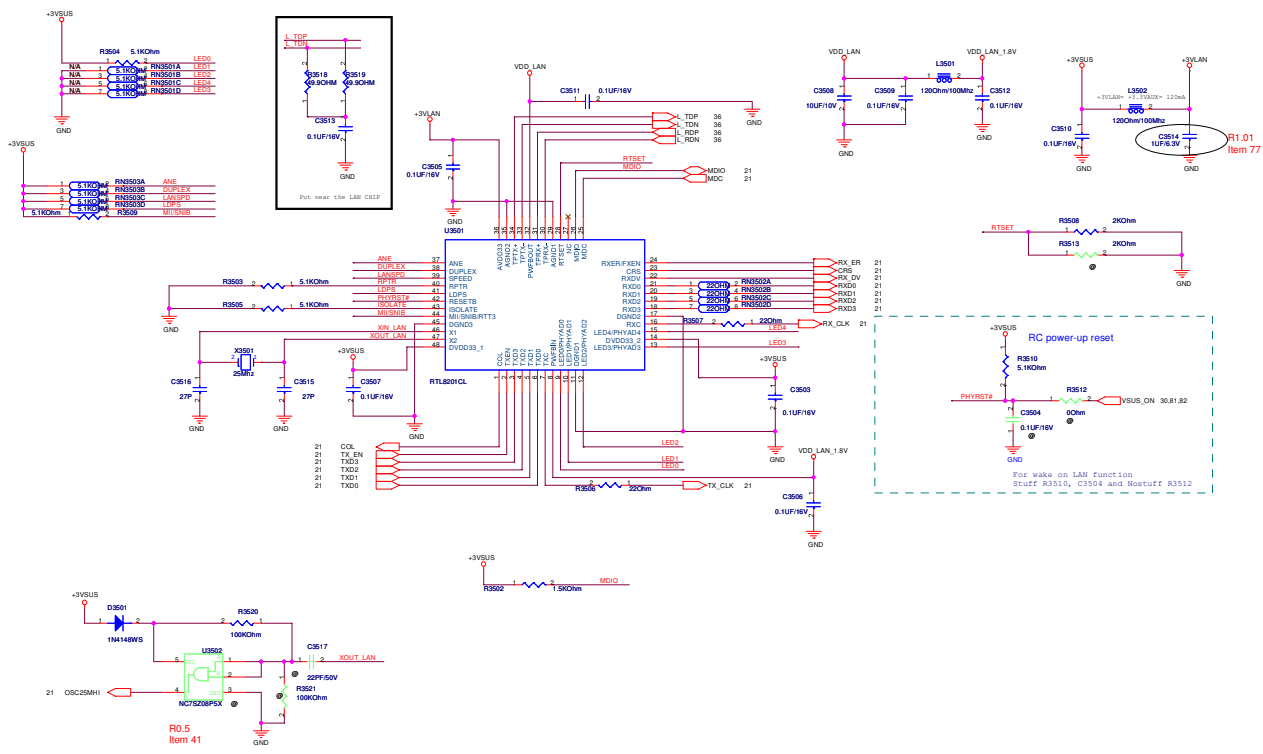


Cap. Lock



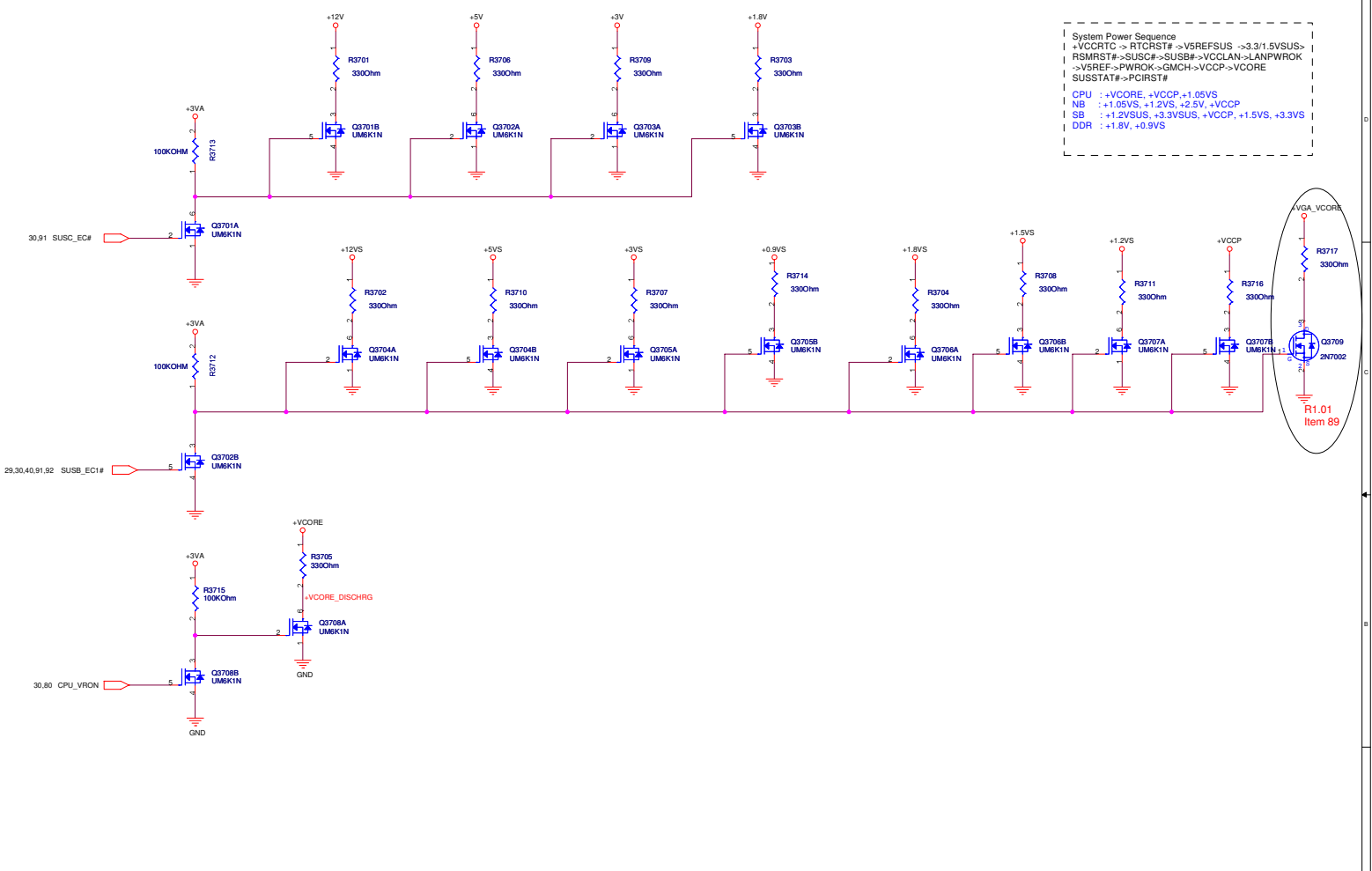
<Variant Name>

ASUS		Title : LED
ASUSTEK COMPUTER INC	Project Name	Engineer: WM Chen
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	34 of 34



System Power Sequence
 +VCCRSTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS->
 RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK->
 V5REF->PWROK->GMCH->VCCP->VCORE
 SUSSTAT#->PCIRST#

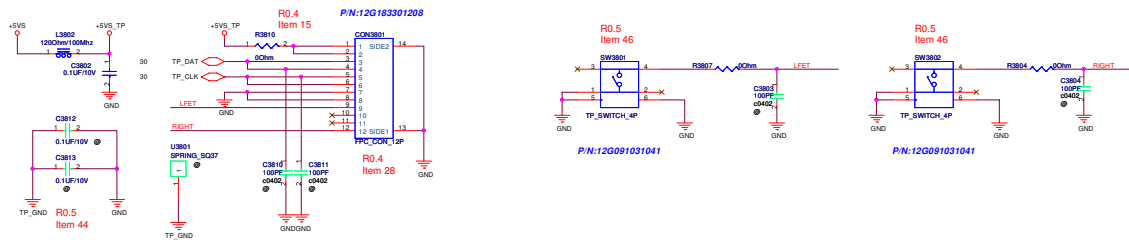
CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS



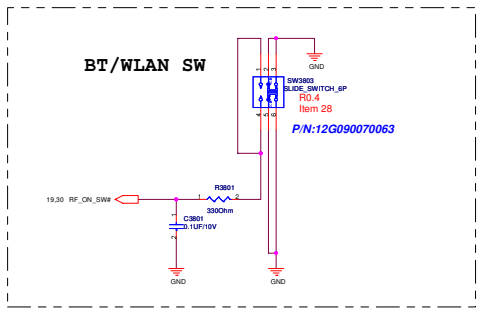
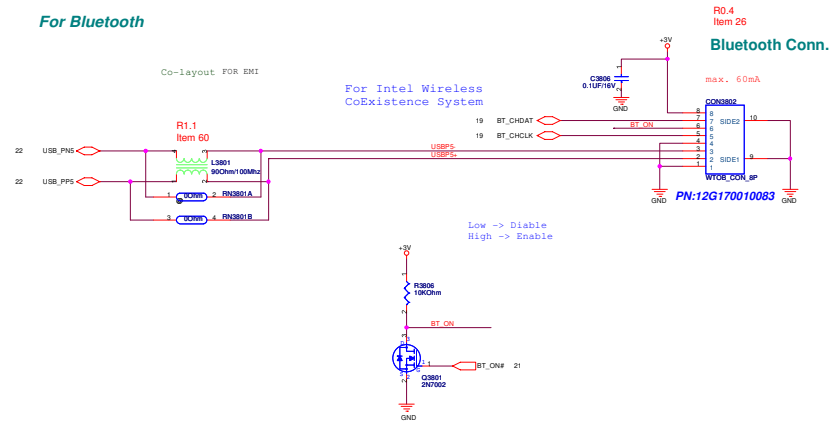
<Variant Name>

ASUS		Title : DISCHARGE CKT	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	37 of 34

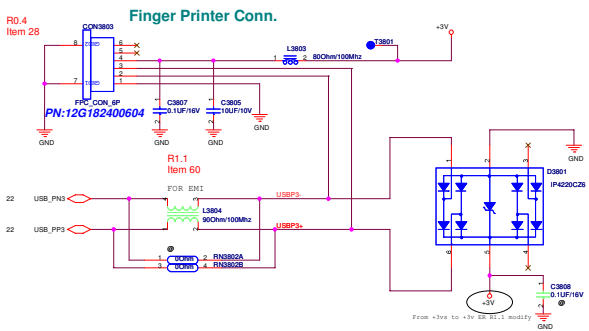
Touch-Pad



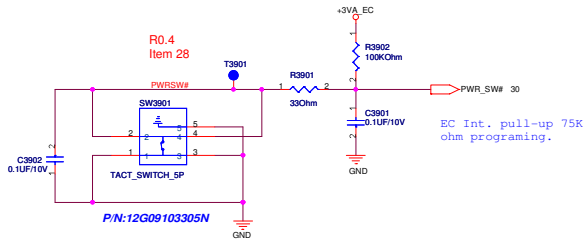
For Bluetooth



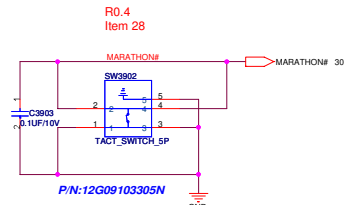
Finger Printer Conn.



Power Button



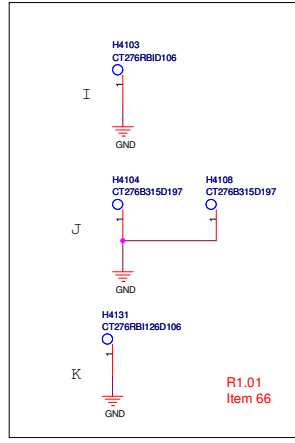
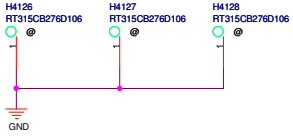
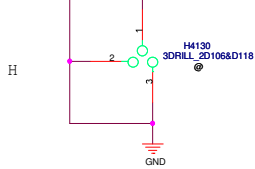
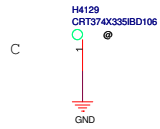
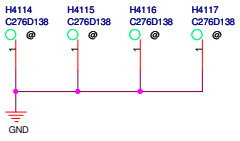
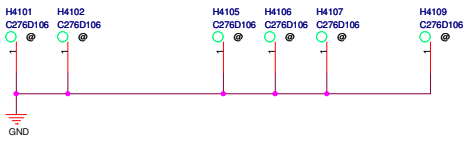
MARATHON#



<Variant Name>


ASUS		Title : SWITCH	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	39 of 34

R0.5
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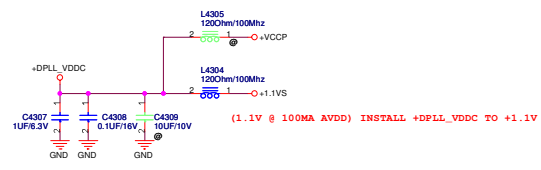
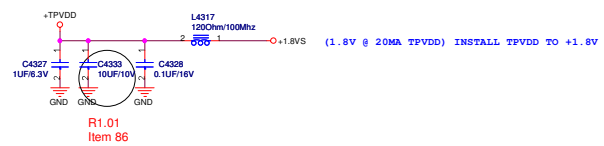
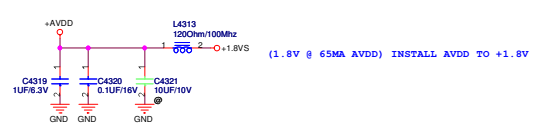
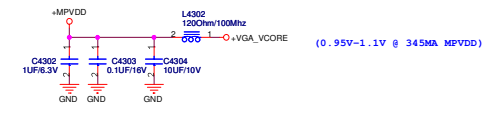
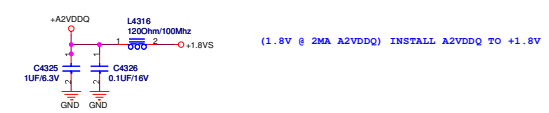
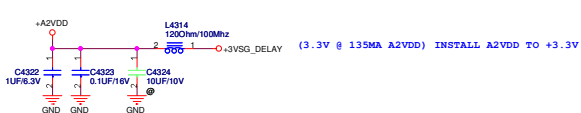
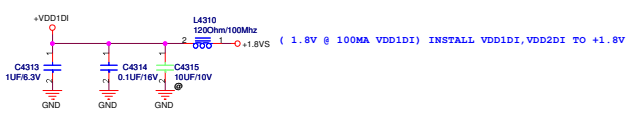
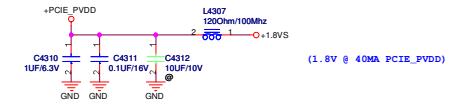
		Title : Screw hole	
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name		Rev
B	F80S		1.1
Date: Wednesday, January 30, 2008		Sheet	41 of 94



		Title : BLANK
ASUSTek COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
Custom	F80S	1-1
Date: Wednesday, February 13, 2008	Sheet	42 of 84

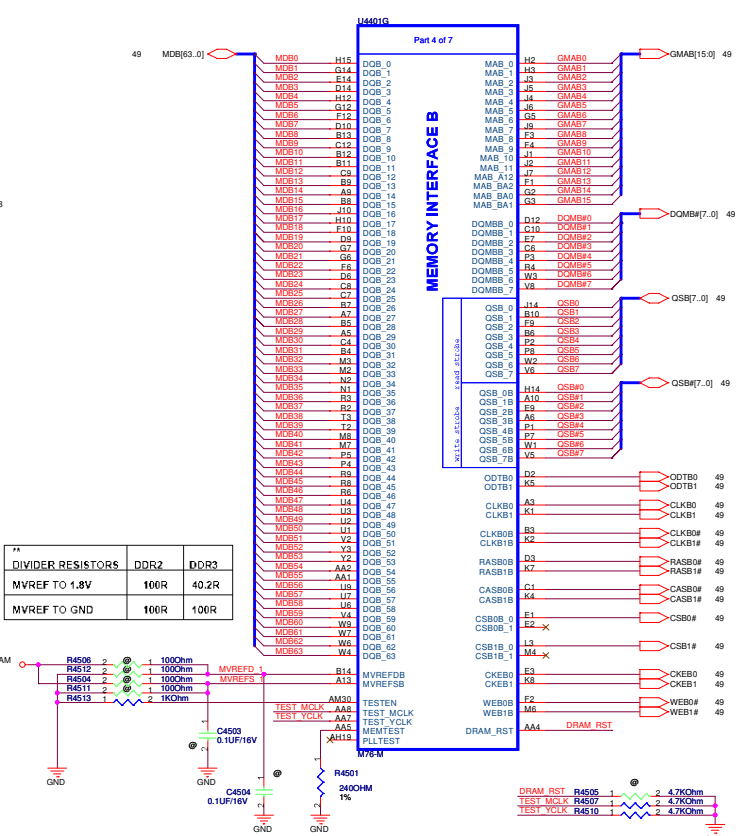
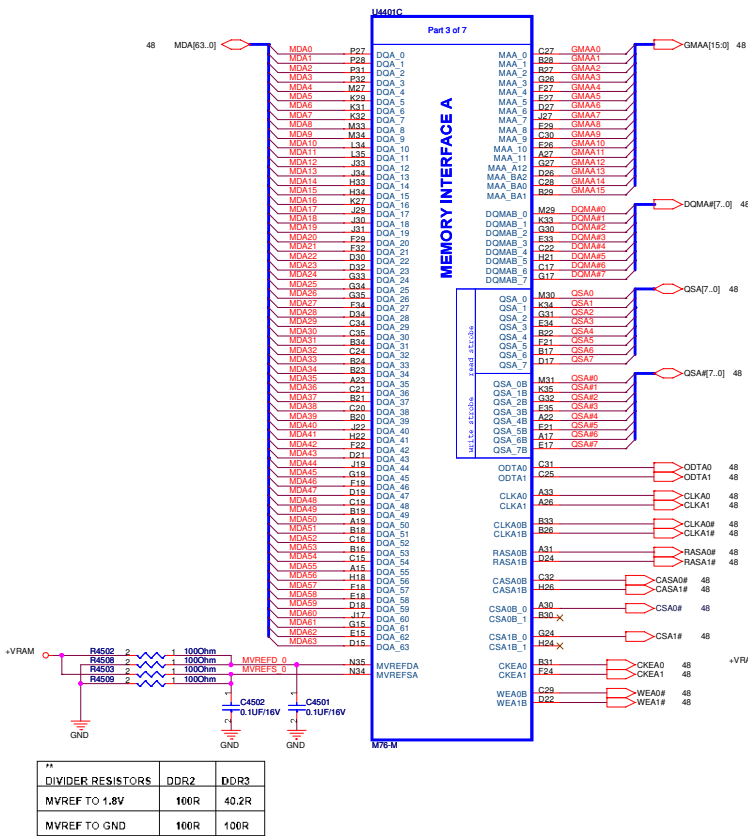
M8x Power

PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



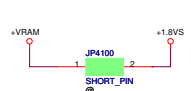
<Variant Name>

ASUS		Title : VGA M8x-M POWER	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, January 30, 2008		Sheet	43 of 84

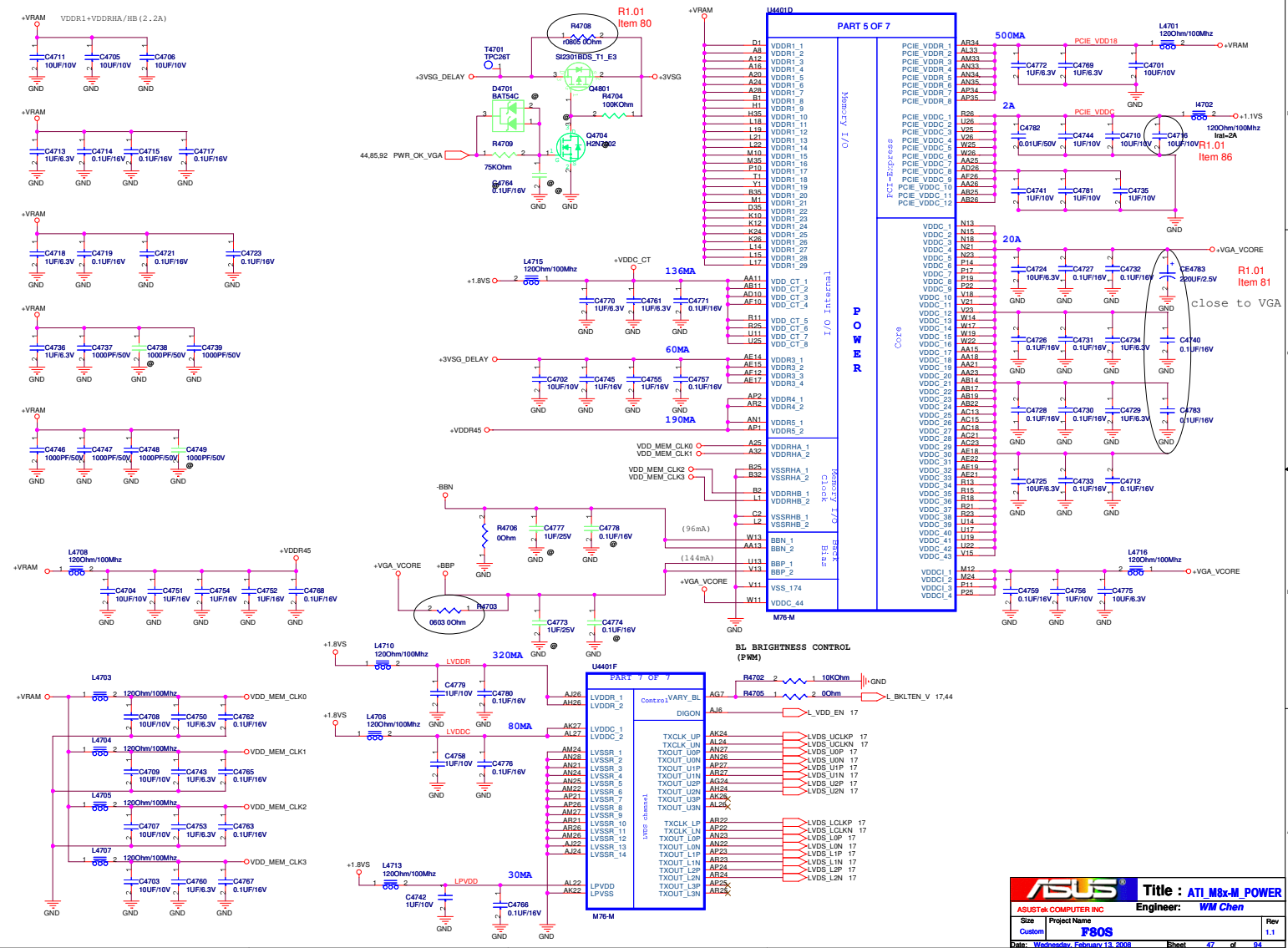


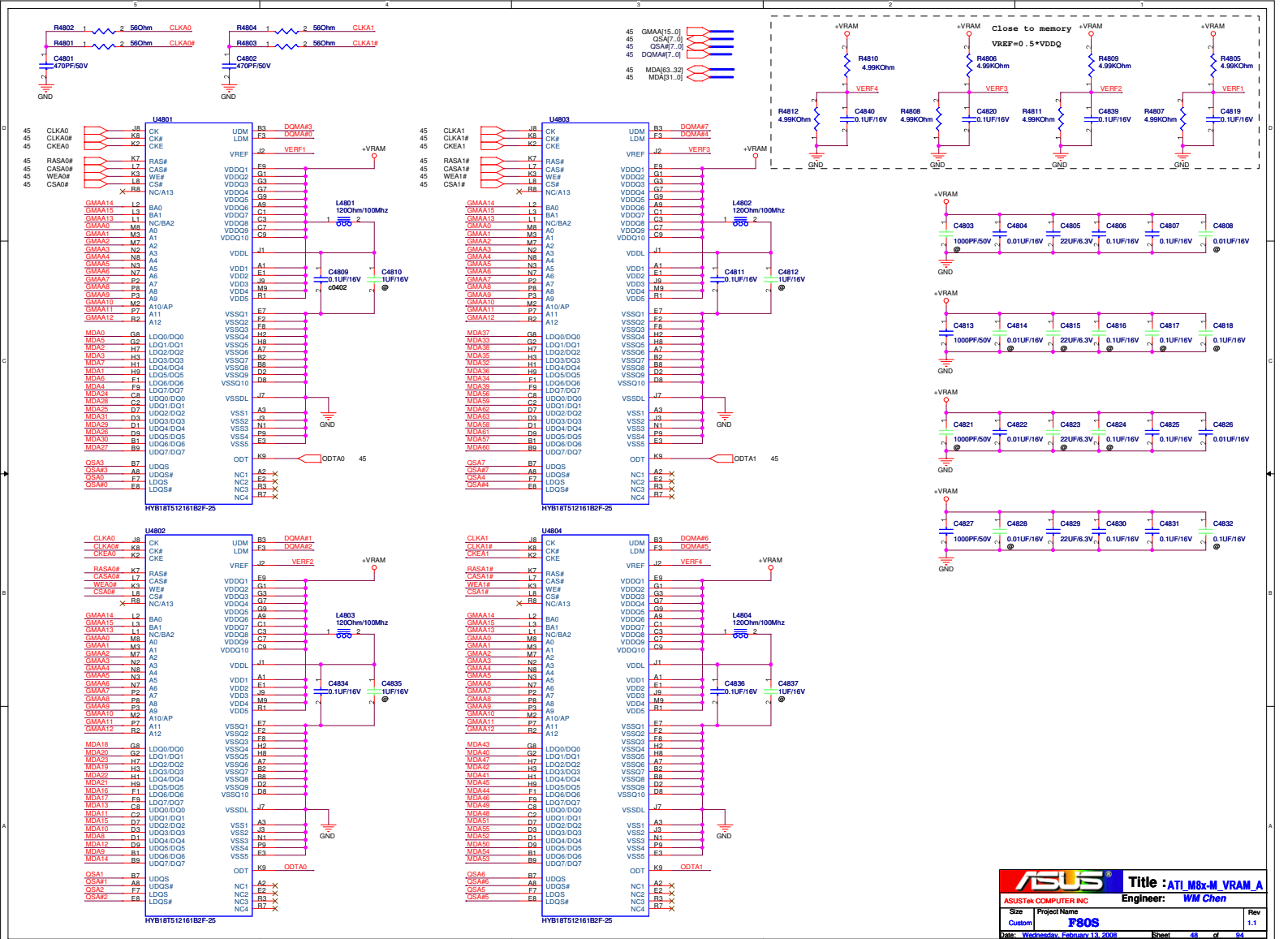
** DIVIDER RESISTORS, DDR2, DDR3		
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

** DIVIDER RESISTORS, DDR2, DDR3		
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



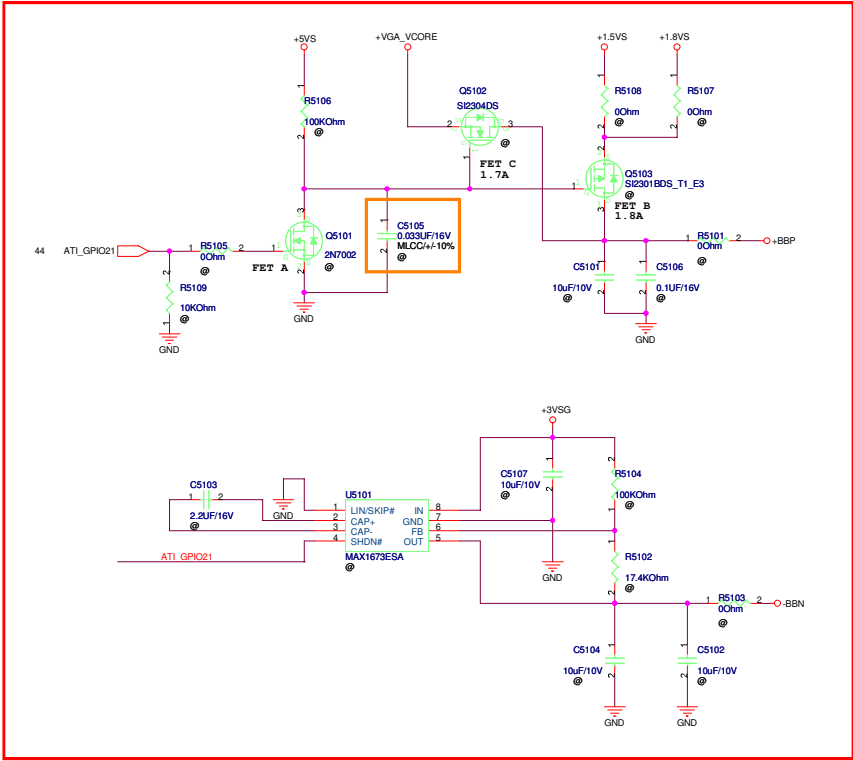
ASUS Title: **ATI M3x-M Memory**
 ASUSTek COMPUTER INC. Engineer: **WM Chen**
 Sub Project Name: **F80S**
 Date: **Wednesday, February 13, 2008** Sheet: **45** of **54**





**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

R0.4
Item 30



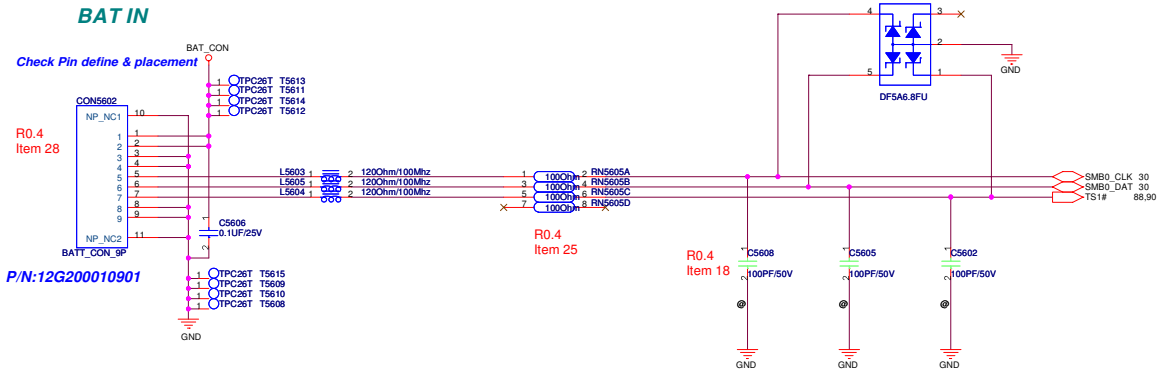
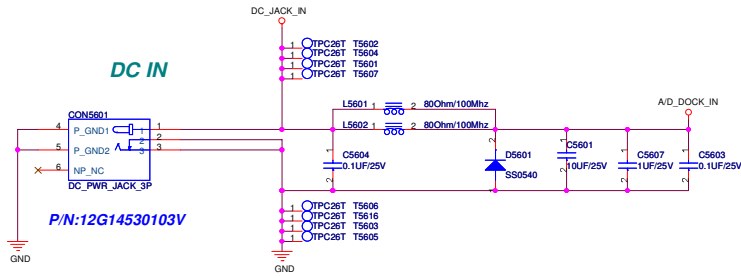
BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = +VGA_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V


GPIO_21_BB_EN	-BBN
0	GND
1	-0.5V


ASUS Title : **BACK BIAS**
 ASUSTeK COMPUTER INC. NB1 Engineer: **WM Chen**
 Size B Project Name **F80S** Rev 1.1
 Date: Wednesday, February 13, 2008 Sheet 51 of 94



ASUS		Title : AC/BAT JACK	
ASUSTek COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet 56	of 94	

R0.4
Item 31

		Title : Empty
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 57 of 94

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 58 of 94

R0.4 revision history:

1. Delete R511,R515,D503,C503,C509,Q505,R506 from 100K change to 0ohm for better signal quality .
2. Change D3302,D3303,D2107 from 1SS355 to 1N4148WS-L for cost down.
3. Change D3401,D3402,D2601,D2603 to BAT54WAPT for cost down and common part.
4. Change D2106 to BAT54C for cost down.
5. Change U1701 to AH180-WG-7 for cost down.
6. Delete RN301,RN302 for not use on board CPU cost down.
7. Add R3047-R3050 for newcard debug card.
8. Change CAP_ACK# from pin24 to pin63 for EC(page30) pin assignment R0.06.
9. Add R3028 for net:AC_IN_OC# pull hi.
10. Change C3002 from 1uF to 0.1uF for cost down.
11. Change Q4203 from 2N7002 to PMBS3904 for cost down and MIC jack.
12. Unmount R1727 for pull hi in p34.Change L1716 to R1710 for U1701 on MB.
13. Change USB connector J2401- J2403.
14. Unmount C3102 for cost down.
15. Reserve R3810 for prevent power short cause large current.
16. Change R3404,R3403,R3412,R3414 from 4.7K to 10K for power saving.
17. Change L3601,L3605 to R3622,R3623 for EMI fine tune cost down.
18. Unmount C5608,C5605,C5602 for EMI fine tune cost down.
19. Change R2505,R2506 from 680ohm to 2.7Kohm for 1W speaker.
20. Change CON3303,J2601 part number for ME request.
21. Change U2601 from TI to GMT,C2609 to 0.1uF for cost down.
22. Change card reader connector J2701 part number for connector in bottom side.
23. Change U2501 from 660 to 662 for the logo request codec need 2-ADC after 2008/6.
24. Reserve C3051 for fine tune CLK_ECPCI.
25. Add RN5605 for protect EC to prevent voltage damage.
26. Change CON3802 pin assignment for use W7 BT cable.
27. Unmount R2611 for ALC662 not need.
28. Change SW3901,SW3902,SW3801,SW3802,SW3803,J2801,CON5602,BAT2101,CON3801,CON3803 part number for ME request.
29. Delete D3301 for cost down.
30. Add VGA Back Bias on page51 for power play function
31. +1.2VSUS from page57 change to page82 for power circuit
32. Delete H_PWRGD_EC (Q202,R233) because it's not necessary.

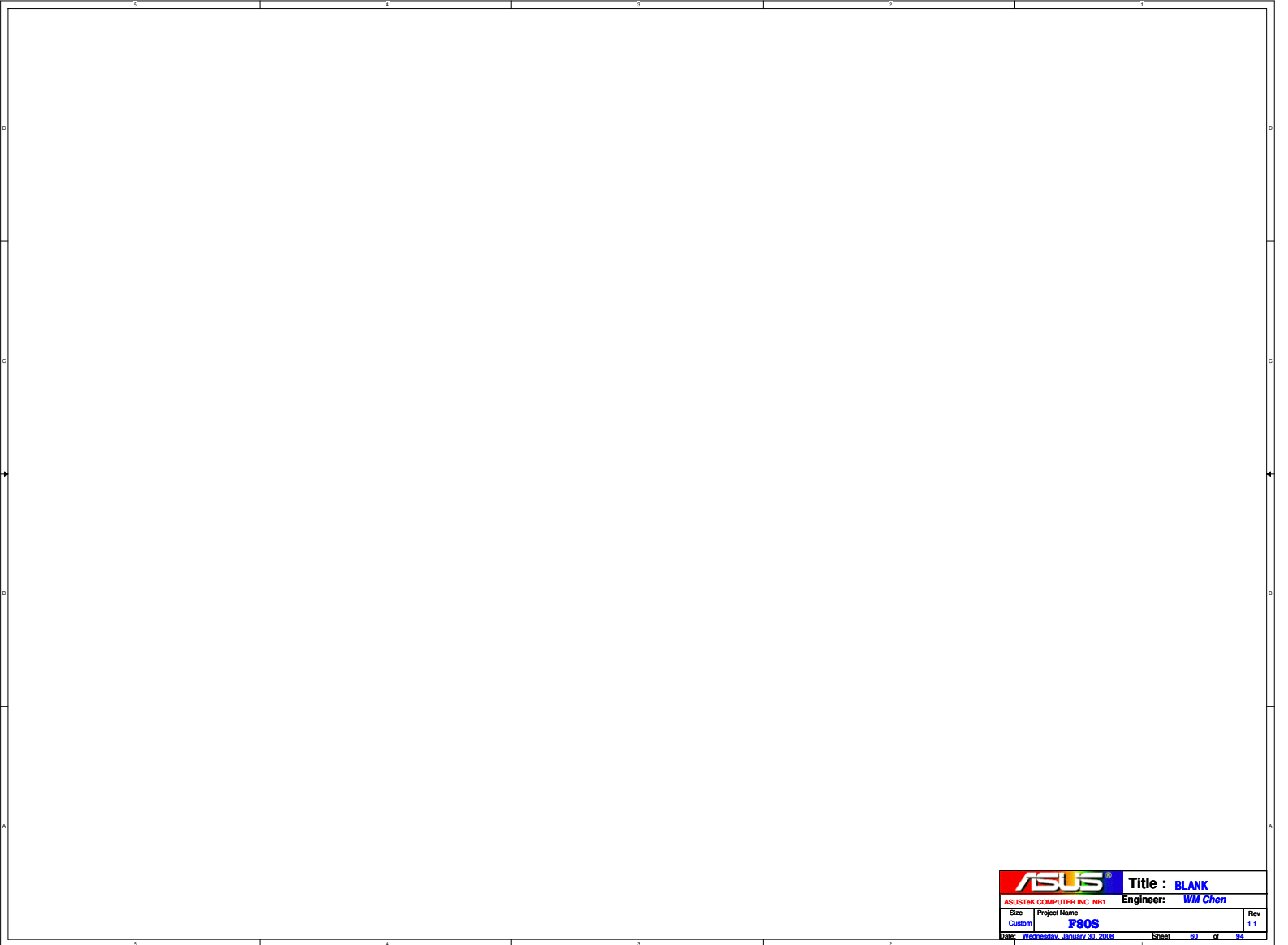
R0.5 revision history:


33. Reserve CON1901 pin24 to +3VAUX for Azurewave's Wireless-Lan Card.
34. Modify p25,p26 for colay ALC662 and ALC663 for sales reccommand.
35. Change KB connector CON3101 part number for ME request.
36. Change Screw hole for ME request .
37. Change CON3602 part number for ME request.
38. Cap. Array CN3101-CN3106 from 0805 change to 1206 size.
39. Add H4401,H4402 VGA NUT
40. Reserve internal mic J2803 for experiment.
41. Reserve U3502,U2103 circuit for experiment.
42. Add U1601,U1602 for NB output 3.3V level cost down.
43. Change page34 LED schematic for use Blue LED.
44. Reserve C3812,C3813 for EMI request TP_GND.
45. Modify Page 22,32 for sales require SATA ODD.
46. Change SW3801,SW3802 part number for ME request.
47. Change U3001 part number for cost down.
48. Reserve R208,C202 for H_CPURST#.
49. Add U3801 for EMI request.
50. Add RN1801-RN1804 for EMI request.
51. Delete VRAM termination
52. Add Q4405,R4411,C4466 for +3VSG
53. Change Hall-sensor U1701 part number for ME request.

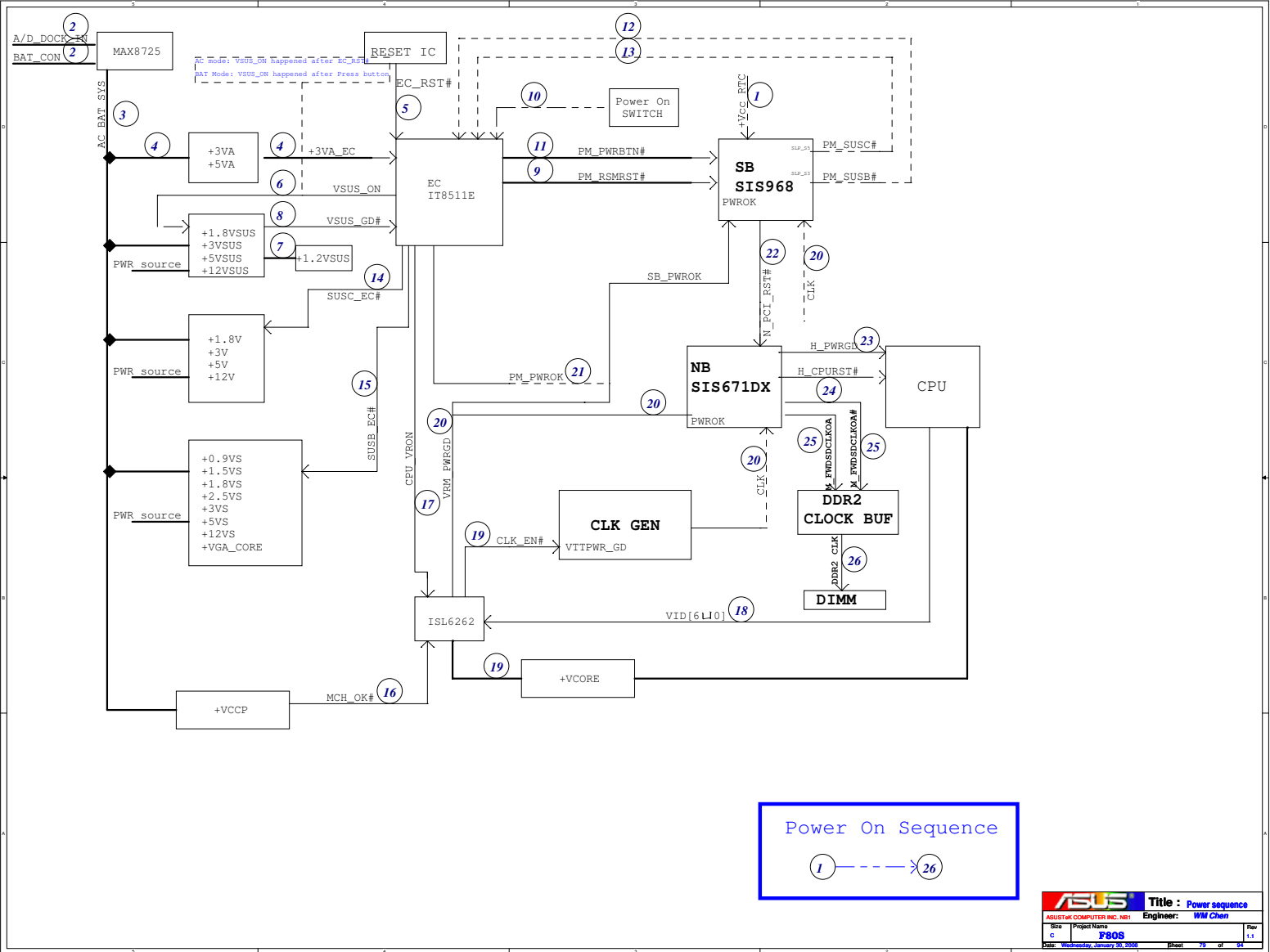
R1.01 revision history:

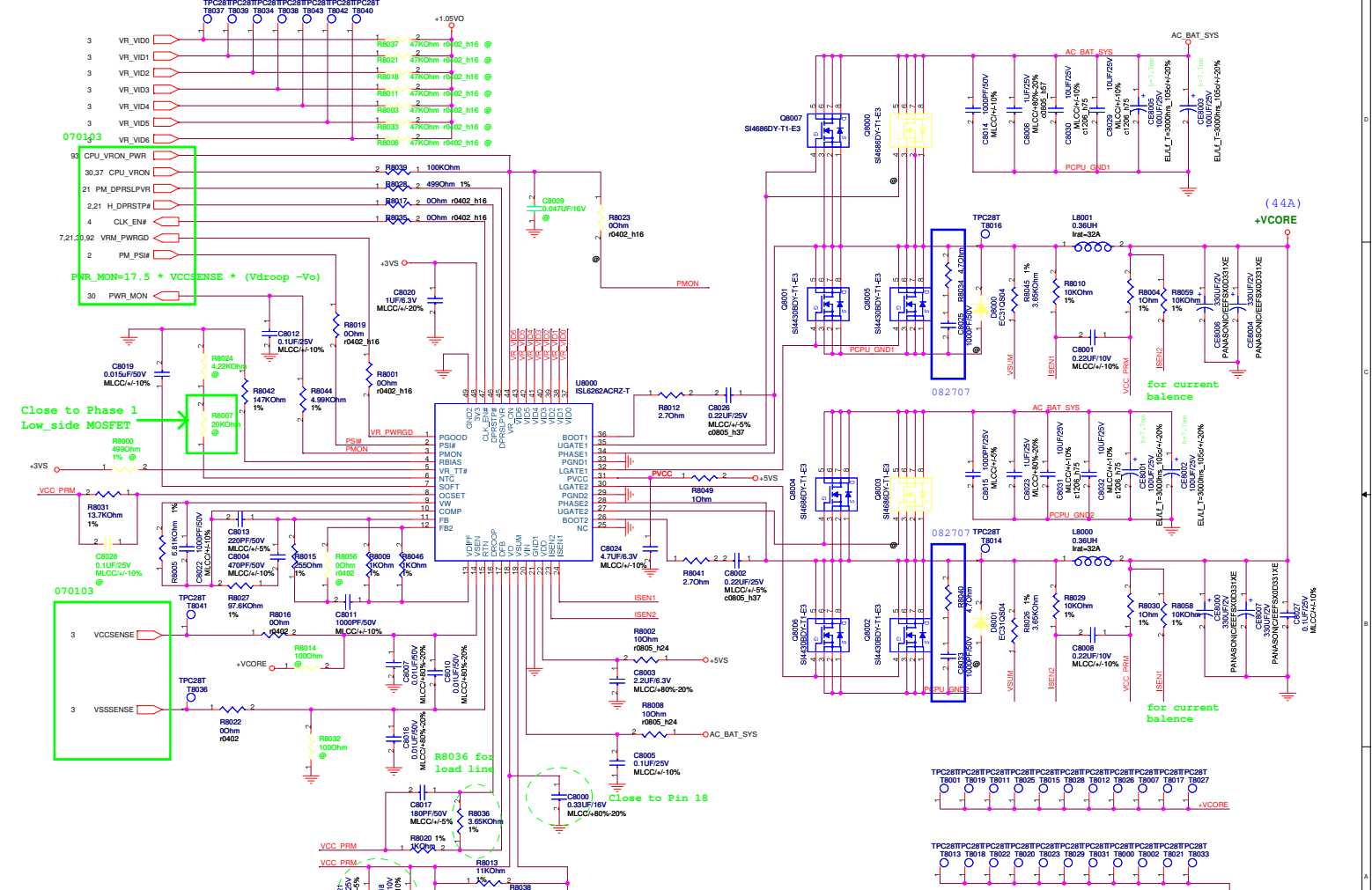
54. Unmount R4428 for leakage current issue.
55. Change R4435 from 71.5 to 150 for SIS request.
56. Mount R4440,R4441,R4443 37.4 ohm for VGA issue.
57. Change SATA ODD Connector CON3203 part number for ME request.
58. Change J2801 connector for Wire-MIC,change R2802 from 4.7K to 2.2K after test internal mic performance.
59. ADD D3603,C3609 for LAN ESD solution.
60. Change L1709,L3801,L3804,L3301,L3302,L3304,L2901 part number for colay footprint.
61. Change R3407,LED3403 value for meet factory LED spec.
62. Change VGA NUT H4401,H4402 to 13G021036001 for Thermal request.
63. Add D3201 IP4220C26 and R2225, R2226, R3217, R3218 0 ohm for EMI request.
64. Add C1218, C1707, C1814, C3304 0.1uF for EMI request.
65. Change R1402 from 22 to 10 for DDR Feedback quality.
66. Change Screw hole H4103, H4104, H4108 and Add H4131 for ME request.
67. Change USB external ports for controller.
68. Change CON3602 RJ11+45 part number for ME request.
69. Change R1705 from 100ohm to 330ohm for meet panel spec.
70. Add R2730 for factory recovery AU6371 driver CD.
71. Change R2505,R2506 from 2.7K to 3.3K for HDD-Speaker resonance issue.
72. Change C410,C417,C2101,C2115,C2715,C2716,C3006,C3010 value for TXC report suggest.
73. Del R1816,R1817 for SMT colay request.
74. Add R310 for +VCCA_CPU voltage ripple.
75. Add C2355 2.2uf for SB issue.
76. Unmount R3017,C3001,U3003,C3008,mount R3036,D3003,C3013,R3035,Add R3039 for cost down.
77. Add C3514 for Lan issue.
78. Mount R4459 and unmount Q4405, R4411,C4466 for cost down.
79. Add R4603 and unmount D4601 for cost down.
80. Mount R4708 and unmount Q4801,Q4704,R4709,R4704 for cost down.
81. ADD CE4783 220UF,C4740,C4783 0.1uF for VGA issue.
82. Mount R1611,R1612 from 0 ohm to 33 ohm and mount C1606,C1607 for meet spec.
83. Change CON3201 part number for ME request.
84. Add R2122,R2186 for SB issue.
85. Add C3305 22UF for meet spec.
86. Add C1905,C2727,C4333,C4334,C4335,C4716,Del C4331 for meet spec.
87. Del CE3202 100UF and Add C3209 47UF for ME request.
88. Change CE2601,CE2602 from 27uF to 47uF for better Low frequency response.
89. Add D4401,R3717,Q3709 for meet VGA spec.

		Title :	
ASUSTek COMPUTER INC. NBI		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
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		Title : BLANK	
ASUSTEK COMPUTER INC. NBI		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, January 30, 2008			Sheet 60 of 84





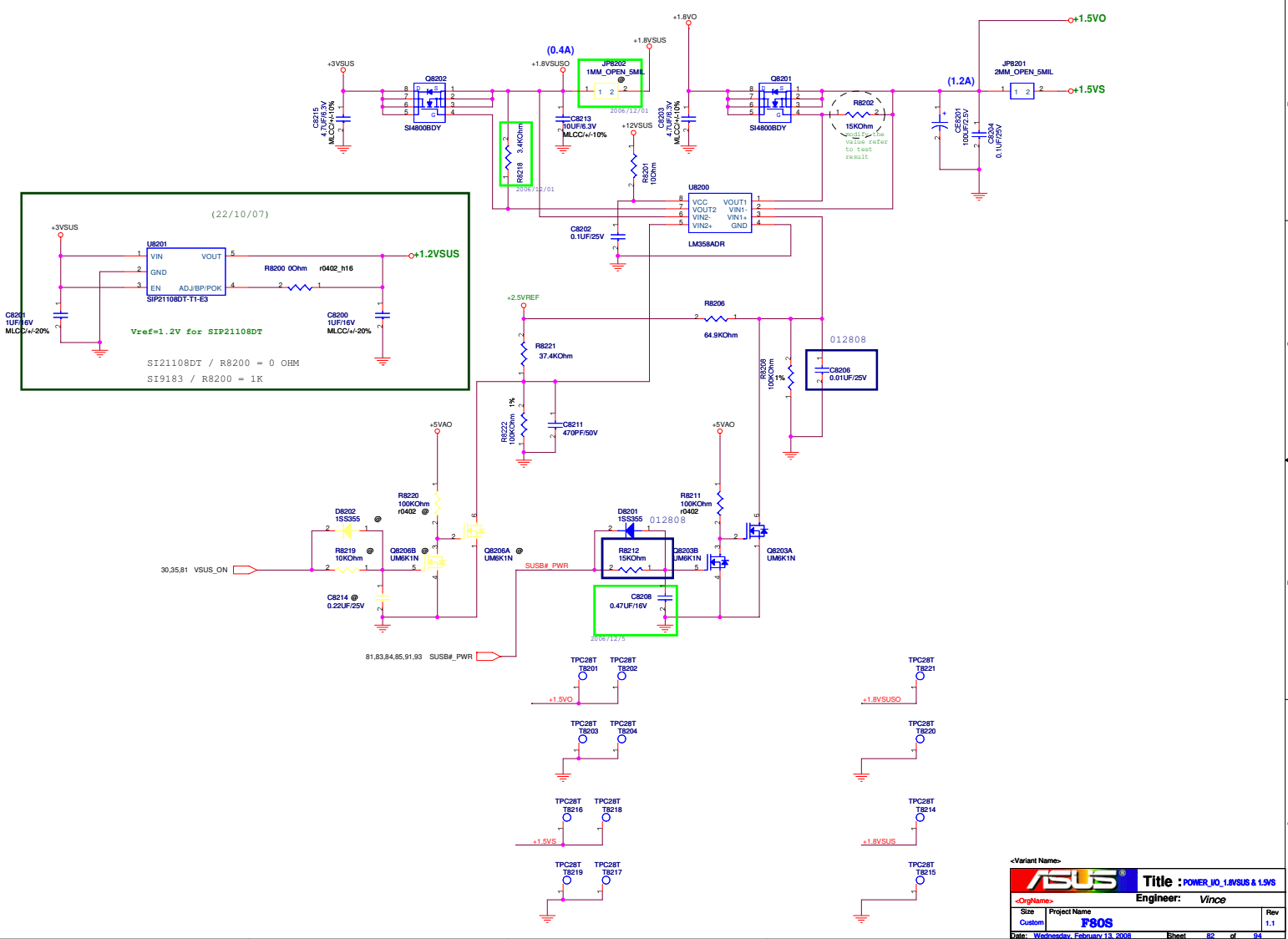
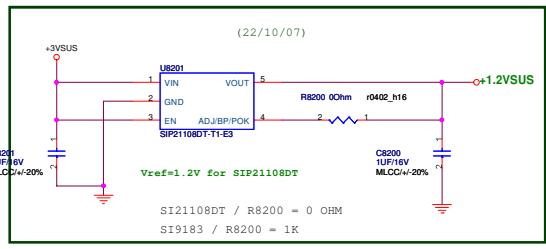
Close to Phase 1 Low_side MOSFET

Close to Phase 1 Inductor

C8021 & C8018 for transient response

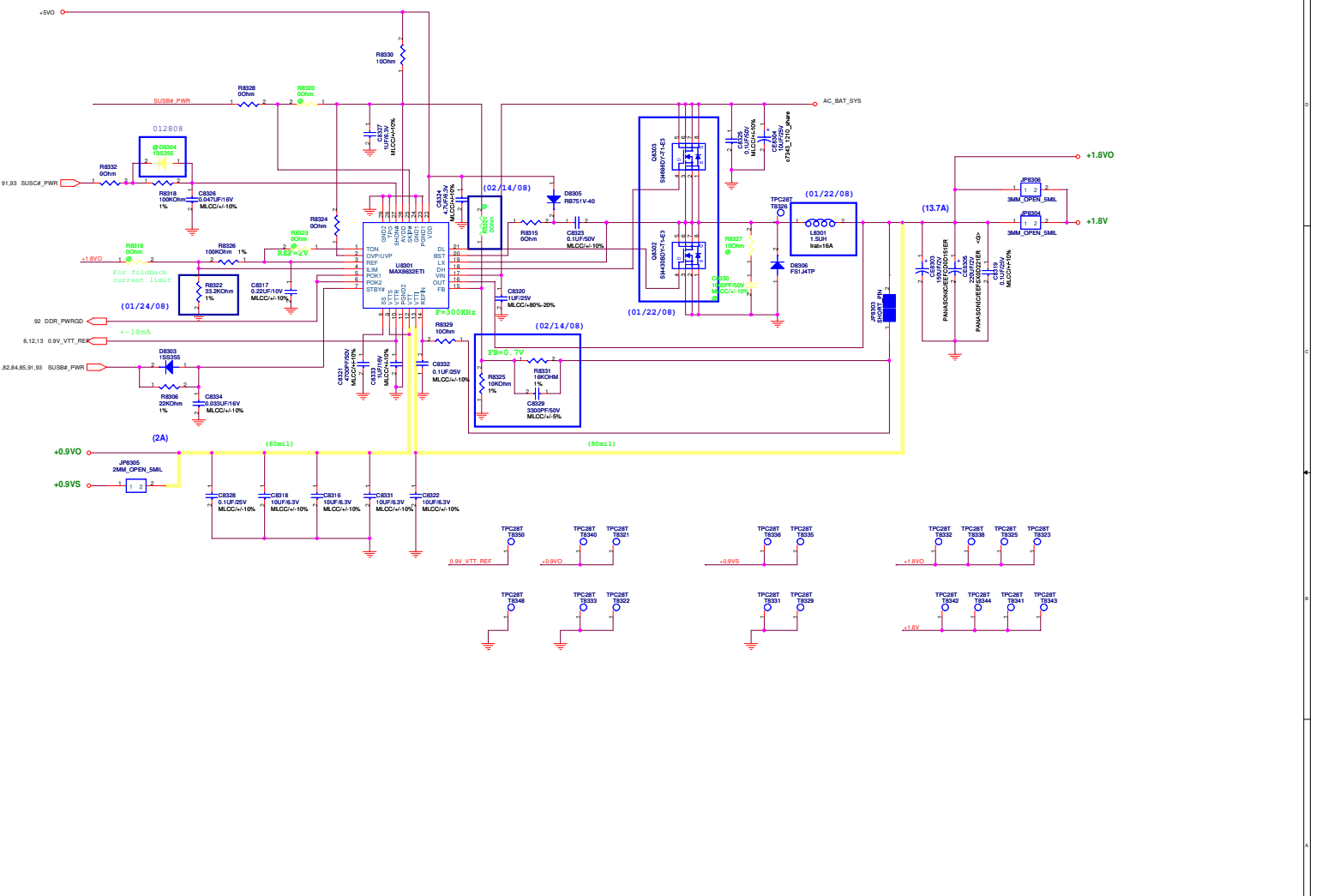
Close to Pin 18

ASUS Title: POWER_VCORE
 ASUSTEK COMPUTER INC. NB Engineer: Vince
 Size: Project Name: Custom
 Date: Wednesday, February 13, 2008 Sheet: 80 of 94

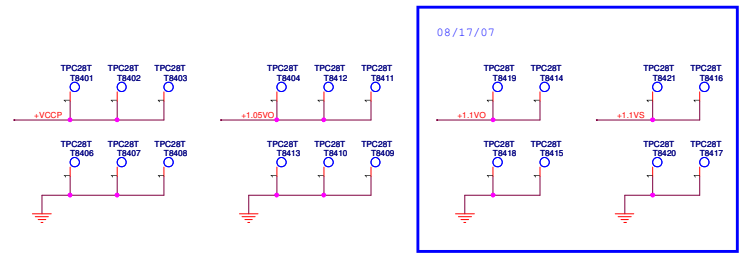
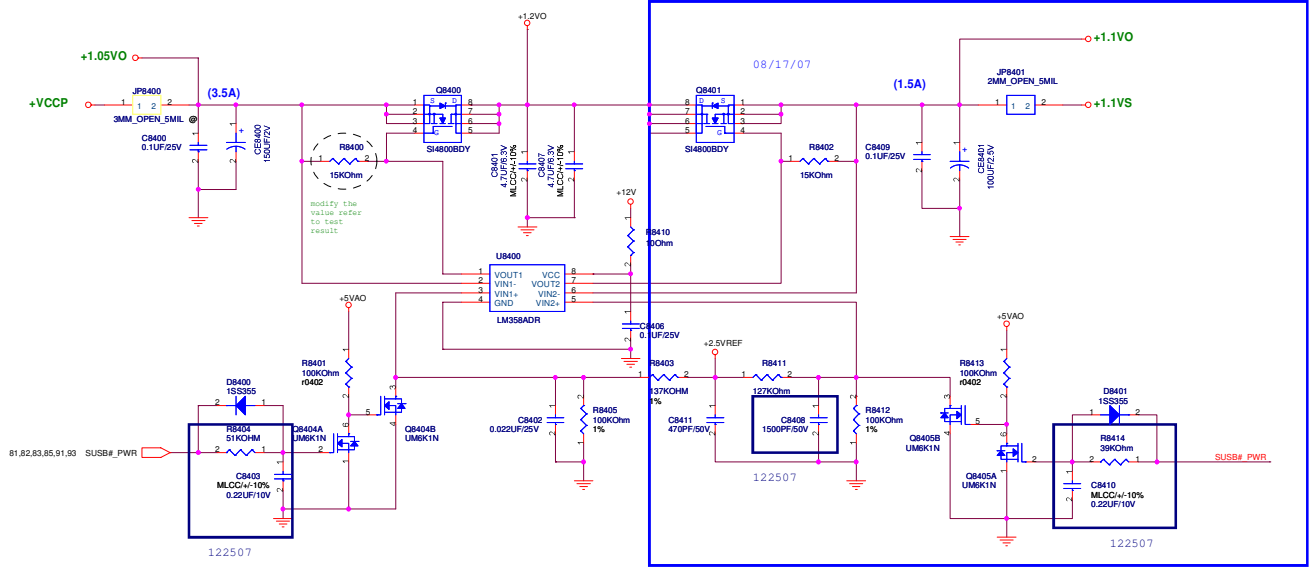


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ASUS		Title : POWER_IO_1.8VSUS & 1.5VS	
<OrigName>		Engineer: Vince	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet: 82	of	84



ASUS
Title : POWER_M0_DOR & VTT
 Engineer: Vince
 Project Name: F80S
 Date: Friday, February 15, 2008
 Sheet: 03 of 04



<Variant Name>

ASUS		Title : POWER_IQ_VCCP & 1.1VS	
<OrigName>		Engineer: vince	
Size	Project Name		Rev
Custom	F80S		1.1
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5

4

3

2

1

D

D

C


C

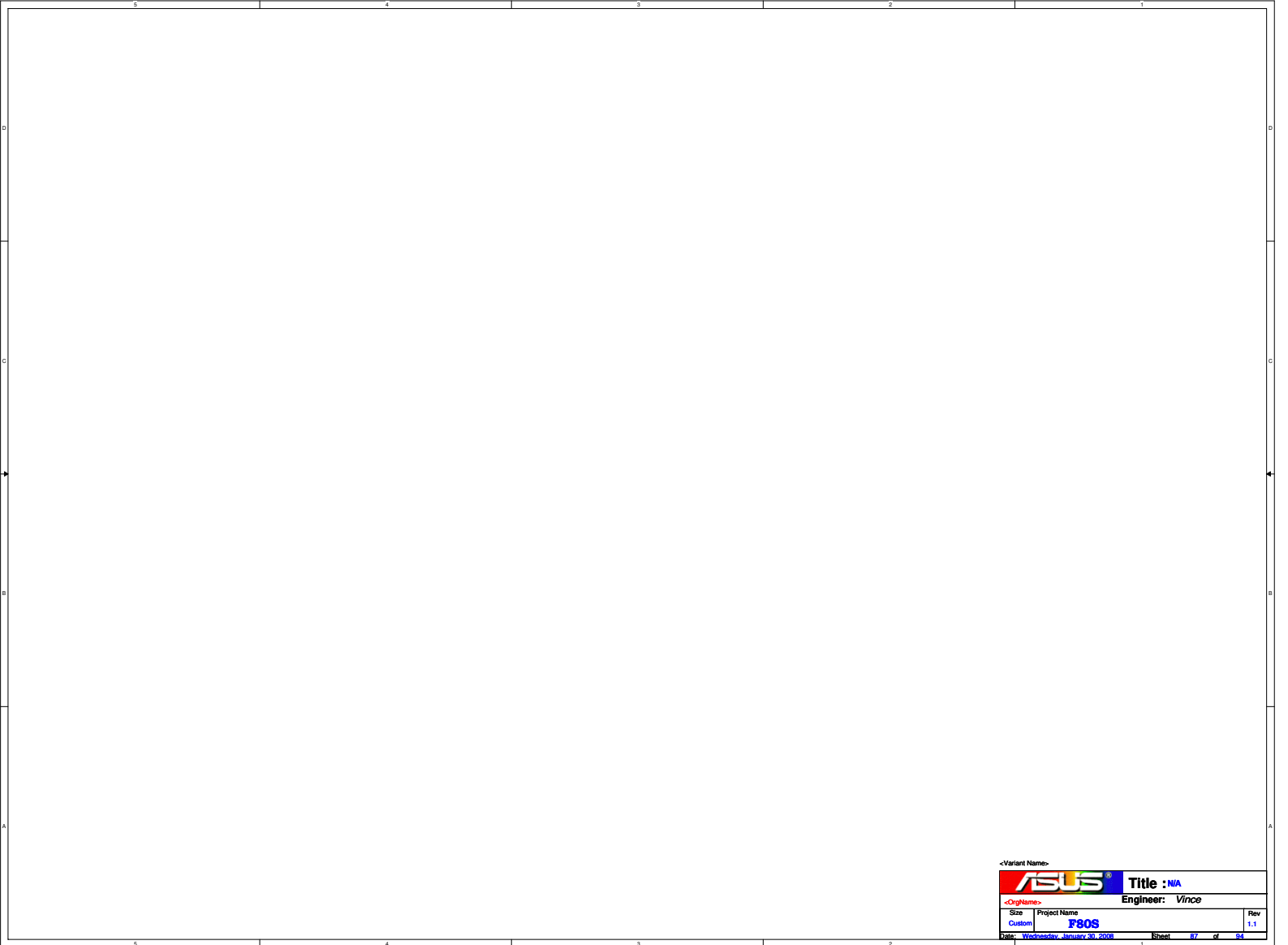
B


B

A

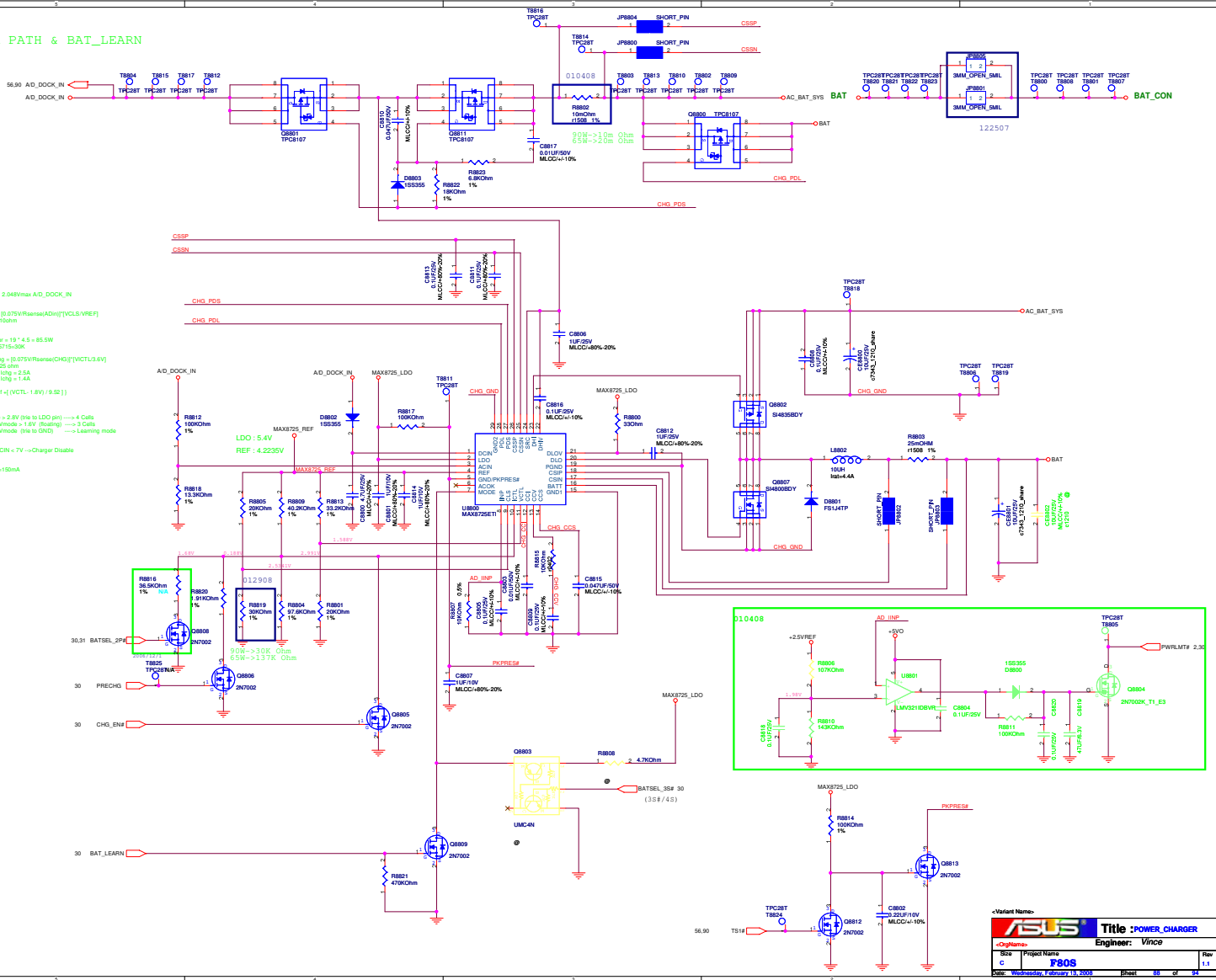
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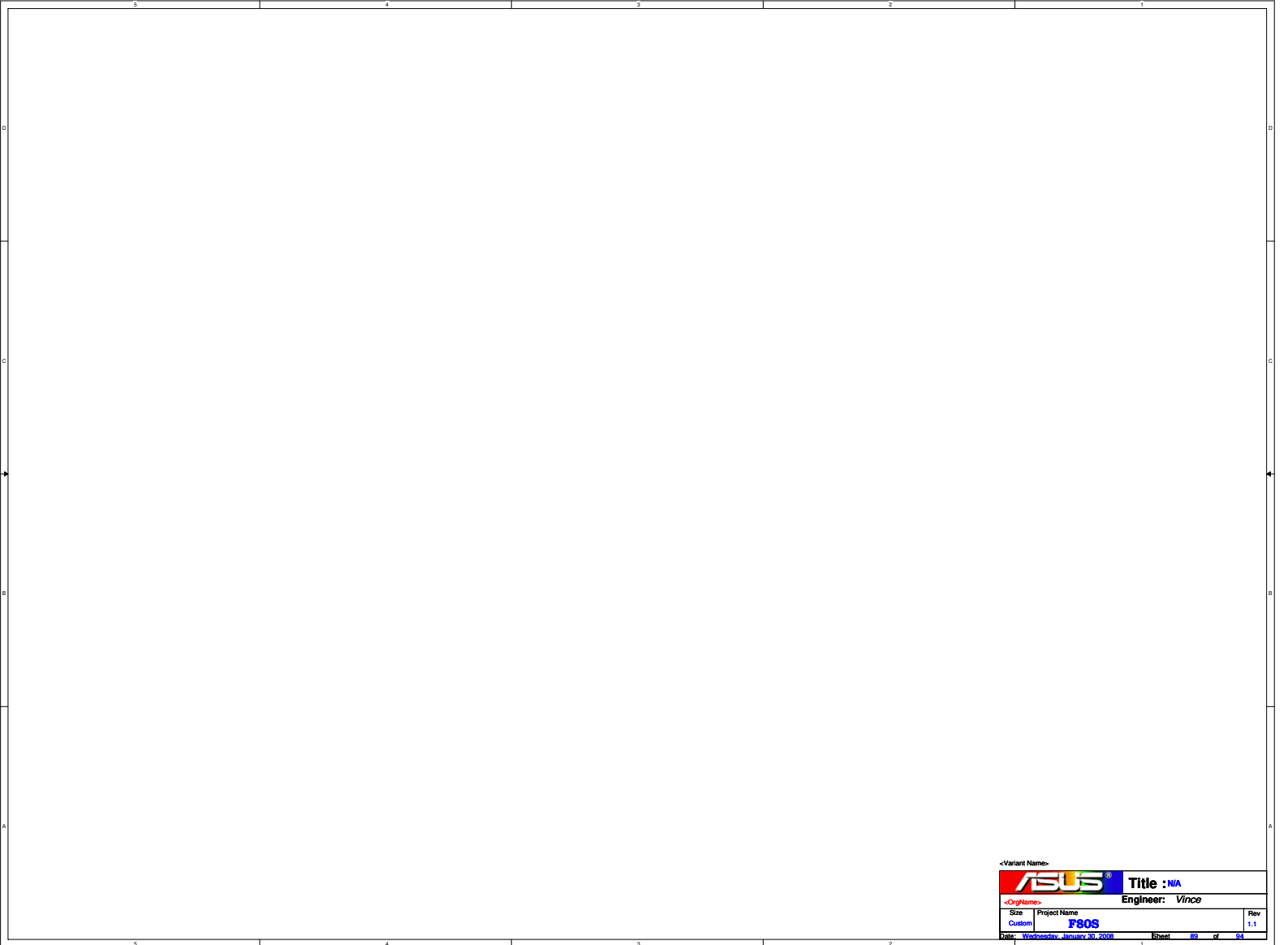
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<OrgName>		Engineer: <i>Vince</i>
Size B	Project Name F80S	Rev 1.1
Date: <i>Wednesday, January 30, 2008</i>		Sheet 86 of 94




<Variant Name>		
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<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 87 of 84

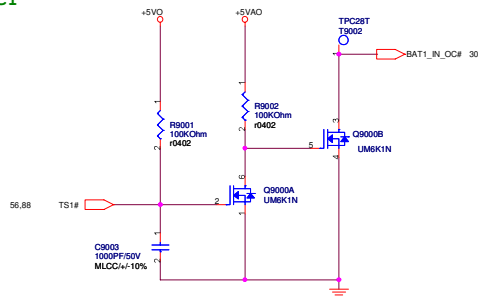
POWER PATH & BAT_LEARN



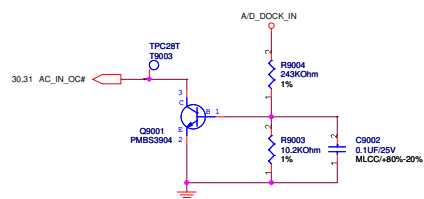


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Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 89 of 94

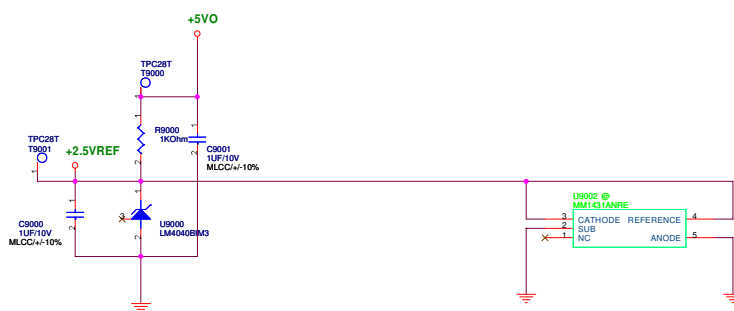
BATTERY IN DETECT



ADAPTER IN DETECT



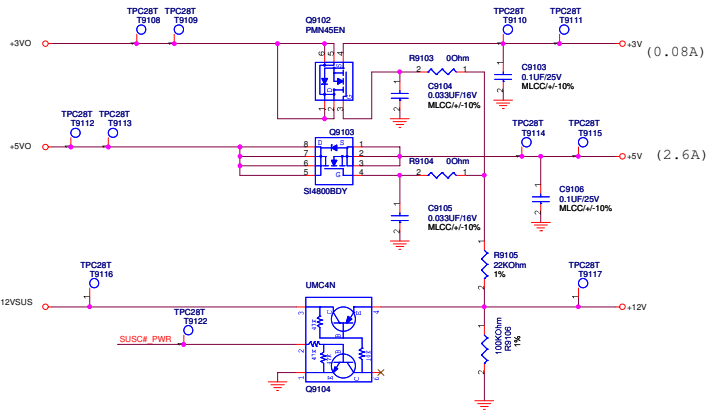
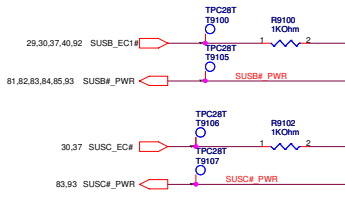
+2.5VREF



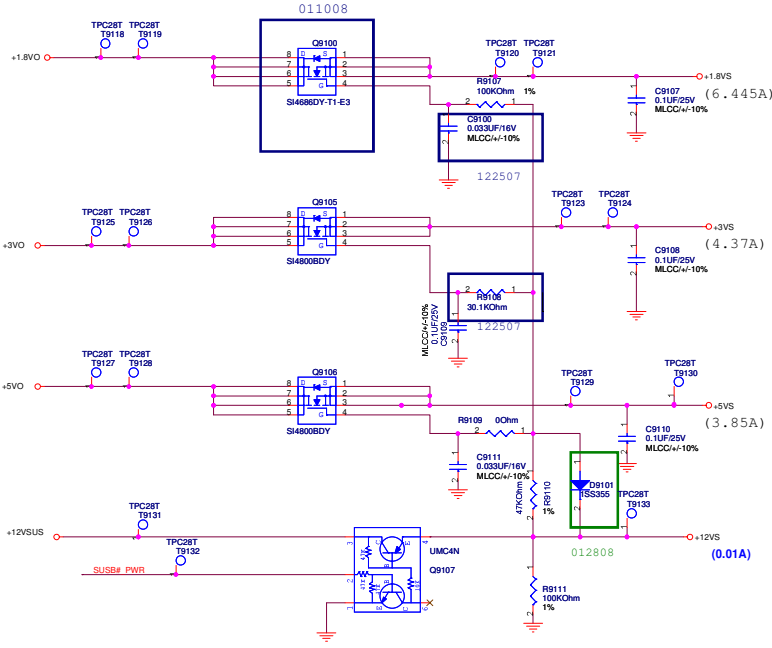
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		Title : POWER_DETECT
<OrigName>		Engineer: Vince
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 90 of 94

SUSC#_STAGE POWER



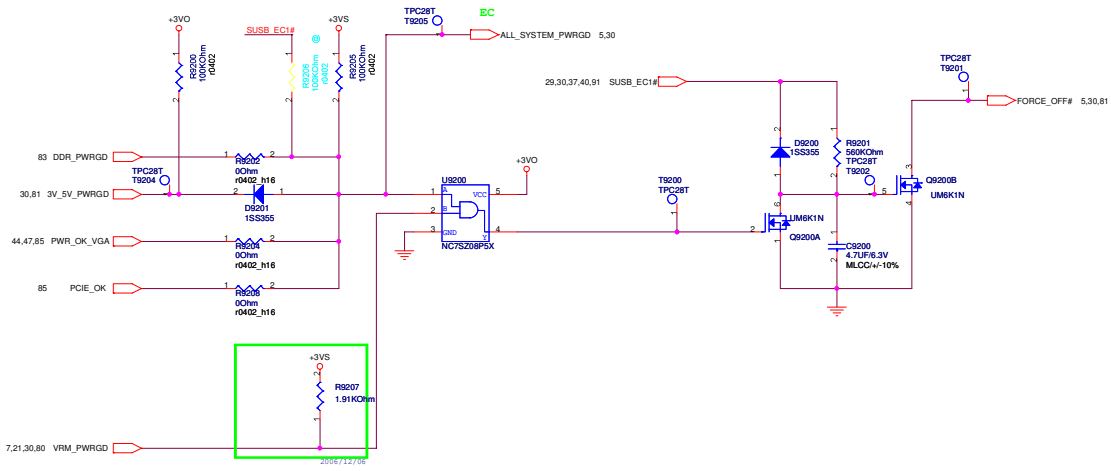
SUSB#_PWR POWER



<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
<OrigName>		Engineer: Vince	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	91 of 94

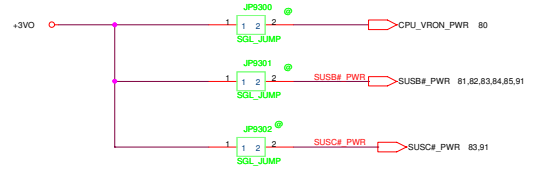
POWER GOOD DETECTOR



<Variant Name>		ASUS		Title : POWER_PROTECT	
<OrigName>		Project Name		Engineer: Vince	
Size	Project Name	Rev			
Custom	F80S	1.1			
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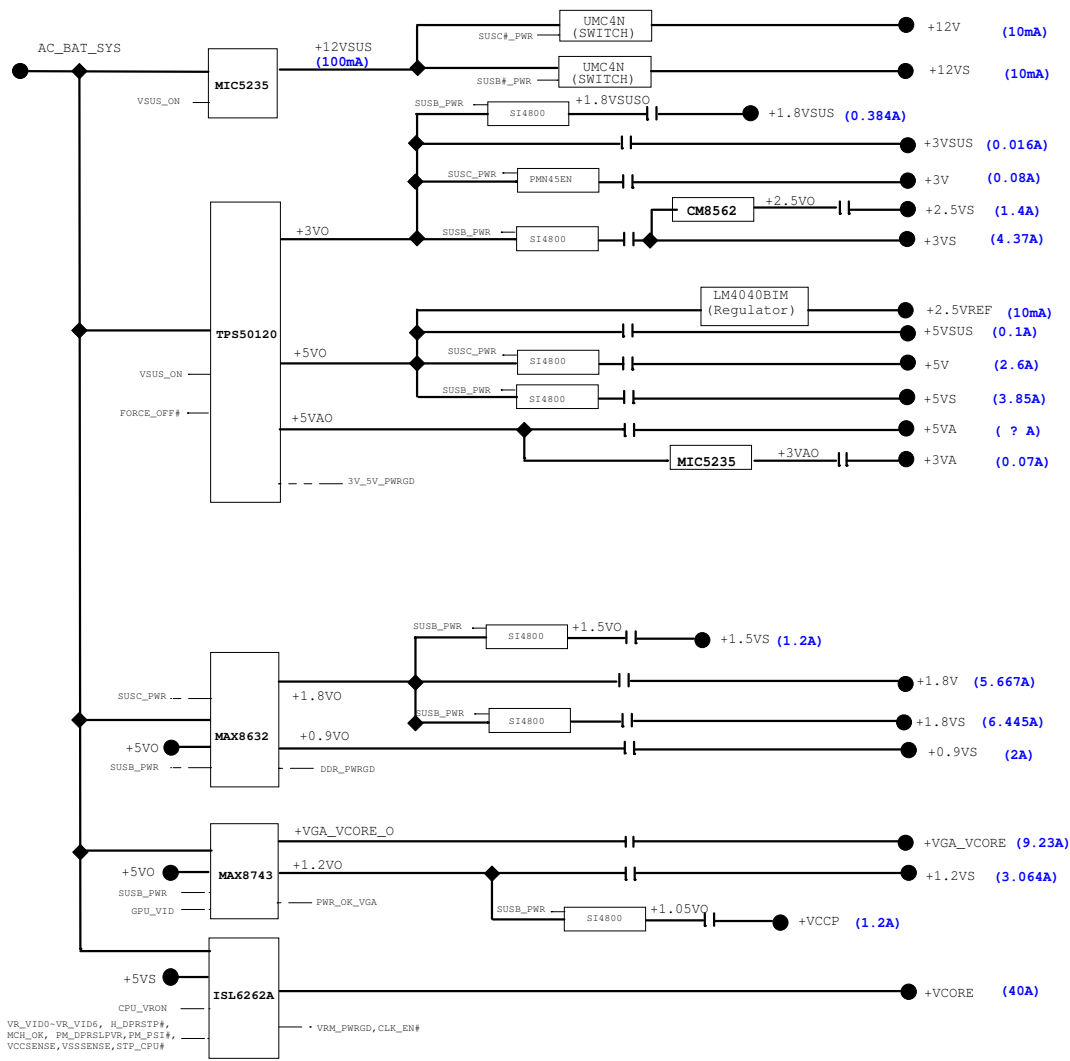


FOR POWER TEST



<Variant Name>

		Title : POWER_SIGNAL	
-<OrigName>		Engineer: Vince	
Size	Project Name	Rev	
Custom	F80S	1.1	
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