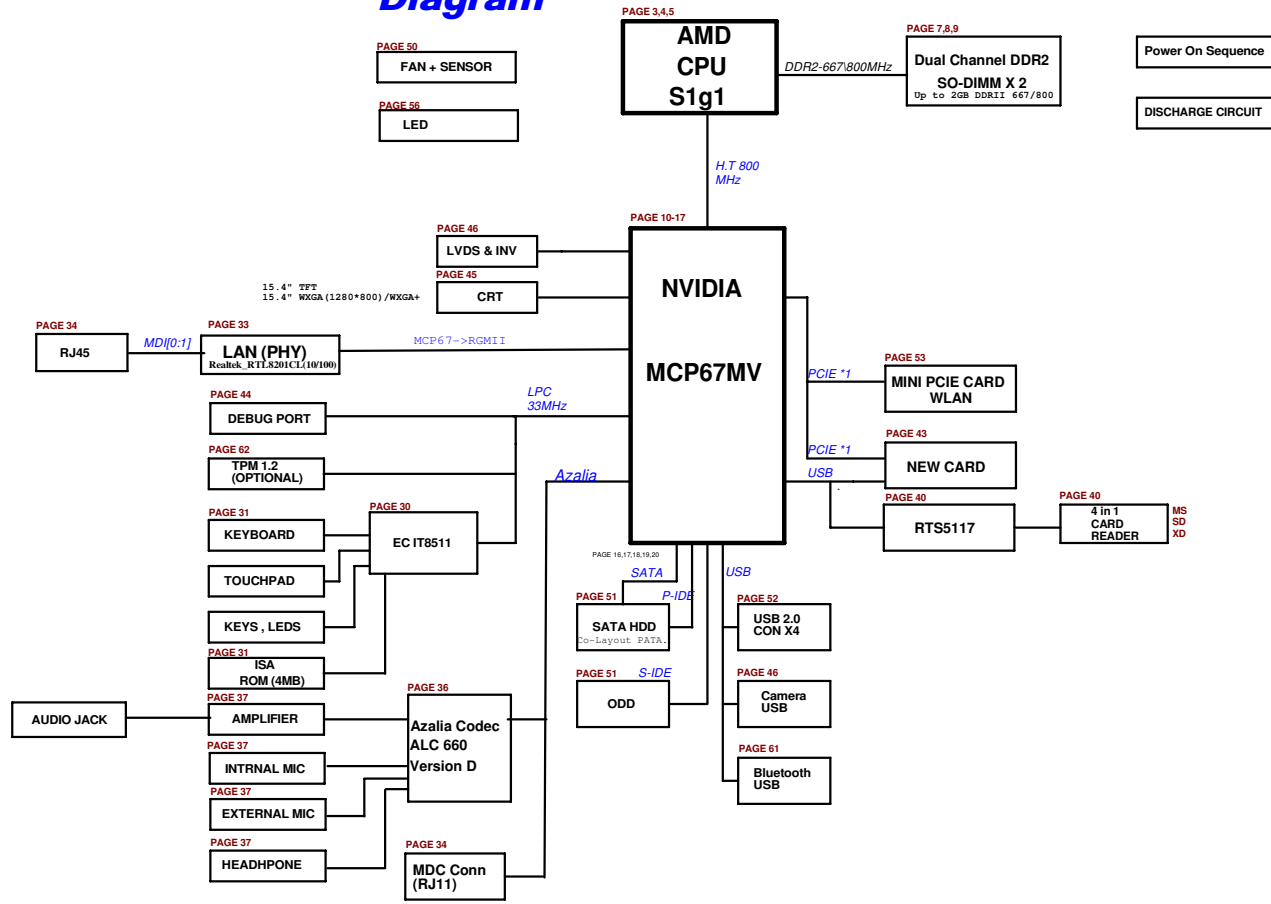

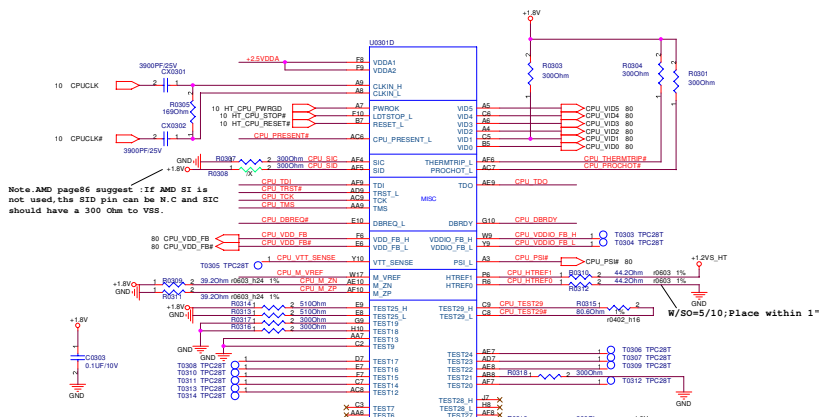


F5N Block Diagram



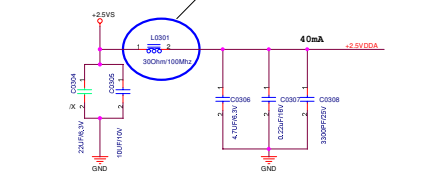
| | | | |
|---|--------------|-------------------|----------------|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | | Sheet: 3 of 28 |



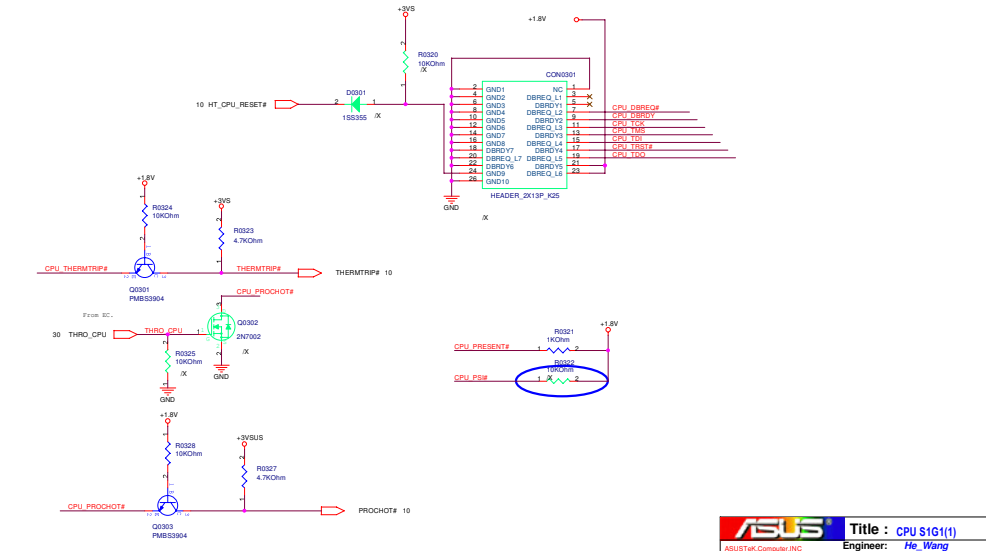
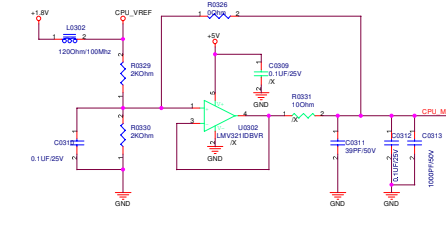
Note: AMD page(s) suggest if AMD 21 is not used, the SID pin can be N.C. and SIC should have a 300 Ohm to VSS.

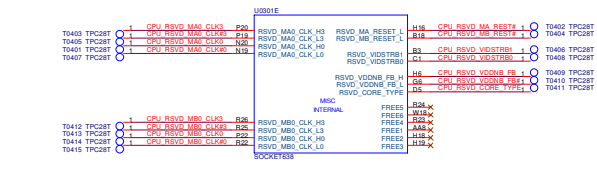
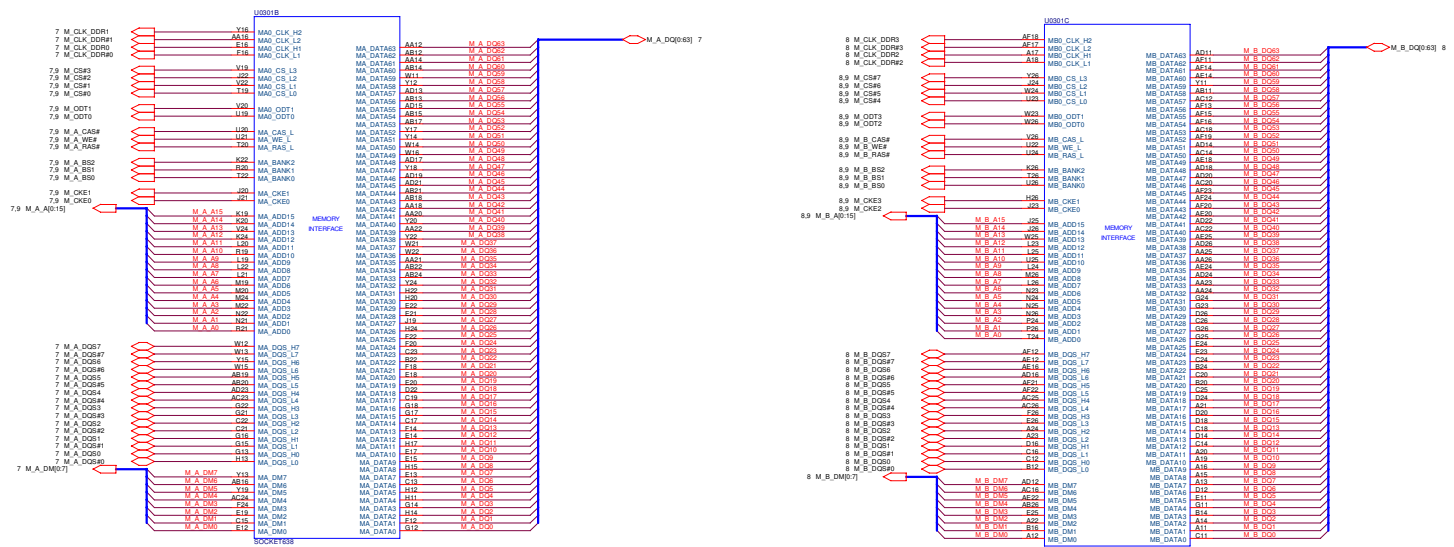
12G011306380

Best and design guide (DC Resistance $\leq 40\text{ m}\Omega$, Inductance $\leq 100\text{ nH}$, Impedance $\leq 1\text{ }\Omega$, approximately 35ohm)



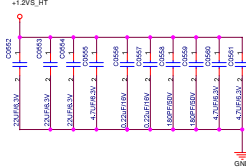
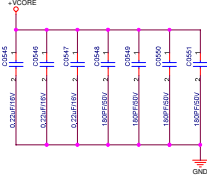
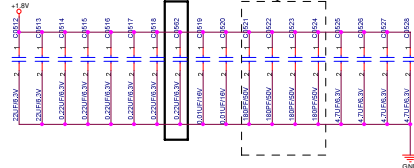
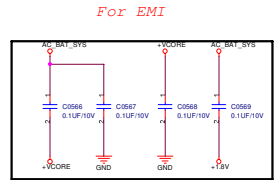
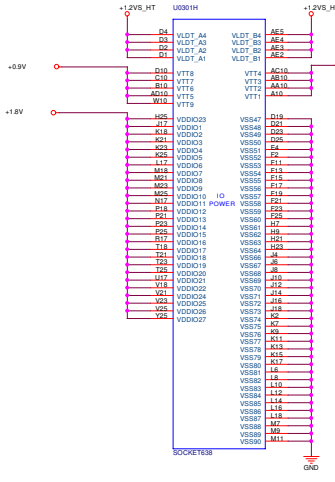
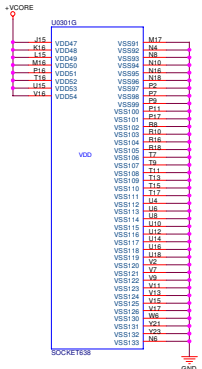
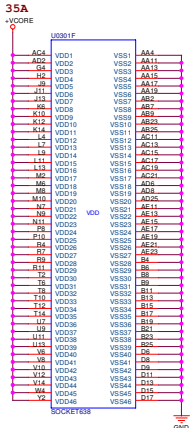
15milis trace, 20mil space /Shorter than 6"




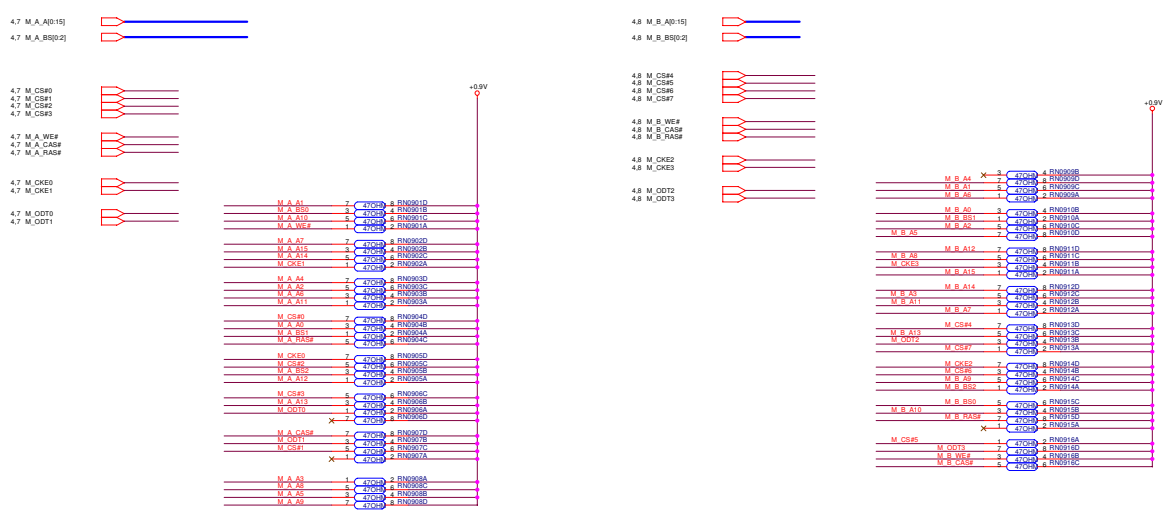


PLEASE CLOSE TO PROCESSOR WITHIN 1.2 INCH

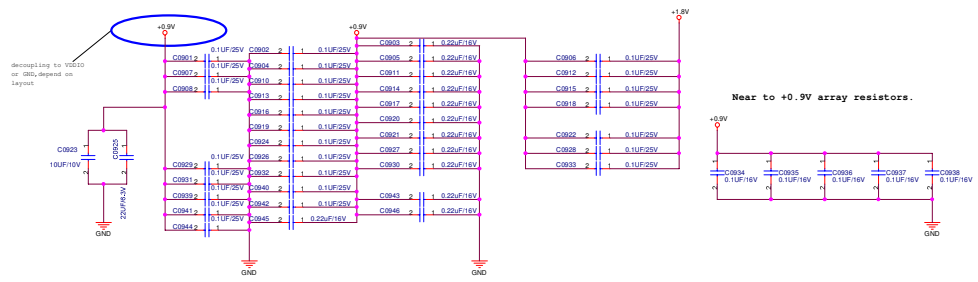
PLEASE CLOSE TO PROCESSOR WITHIN 1.2 INCH

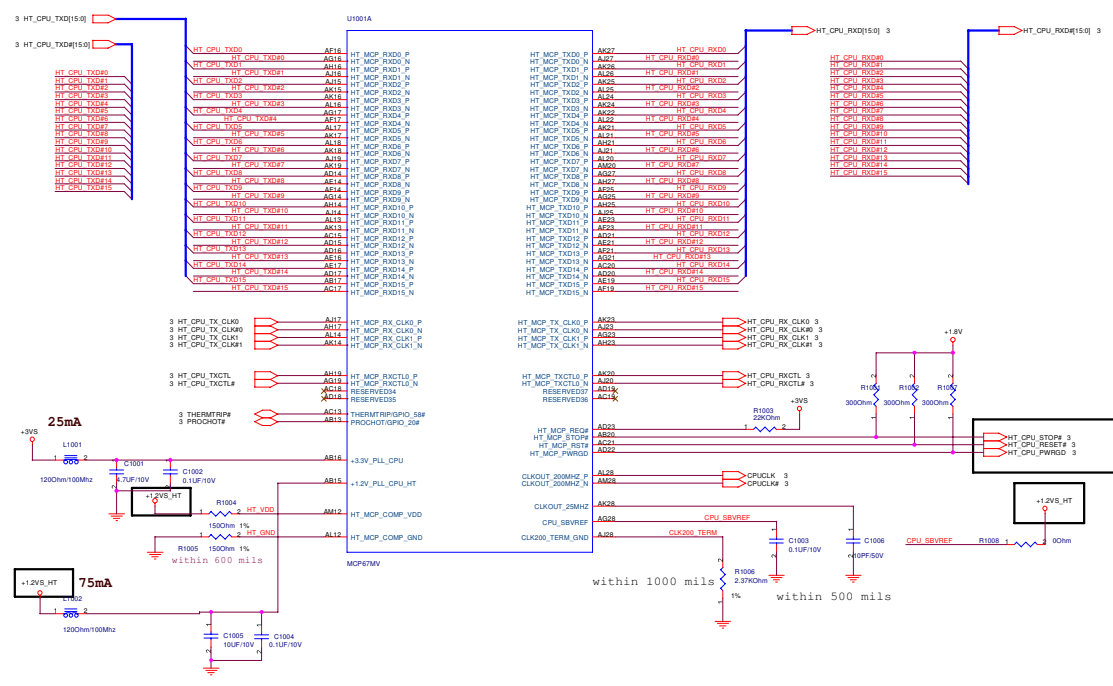


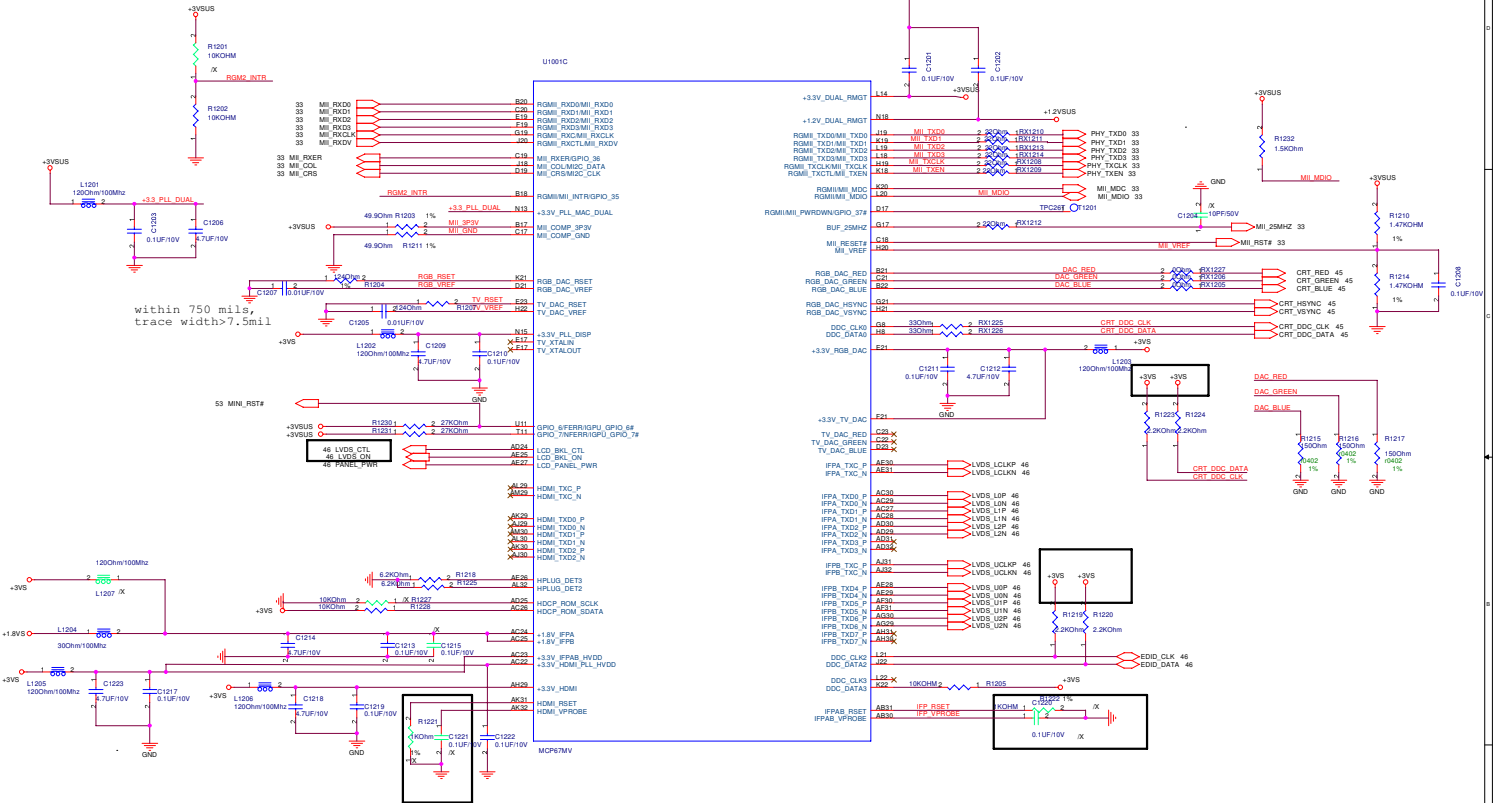
| | | | |
|---|--------------|-------------------|--|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-03-29 10:07 | | Sheet 6 of 26 | |



Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9V



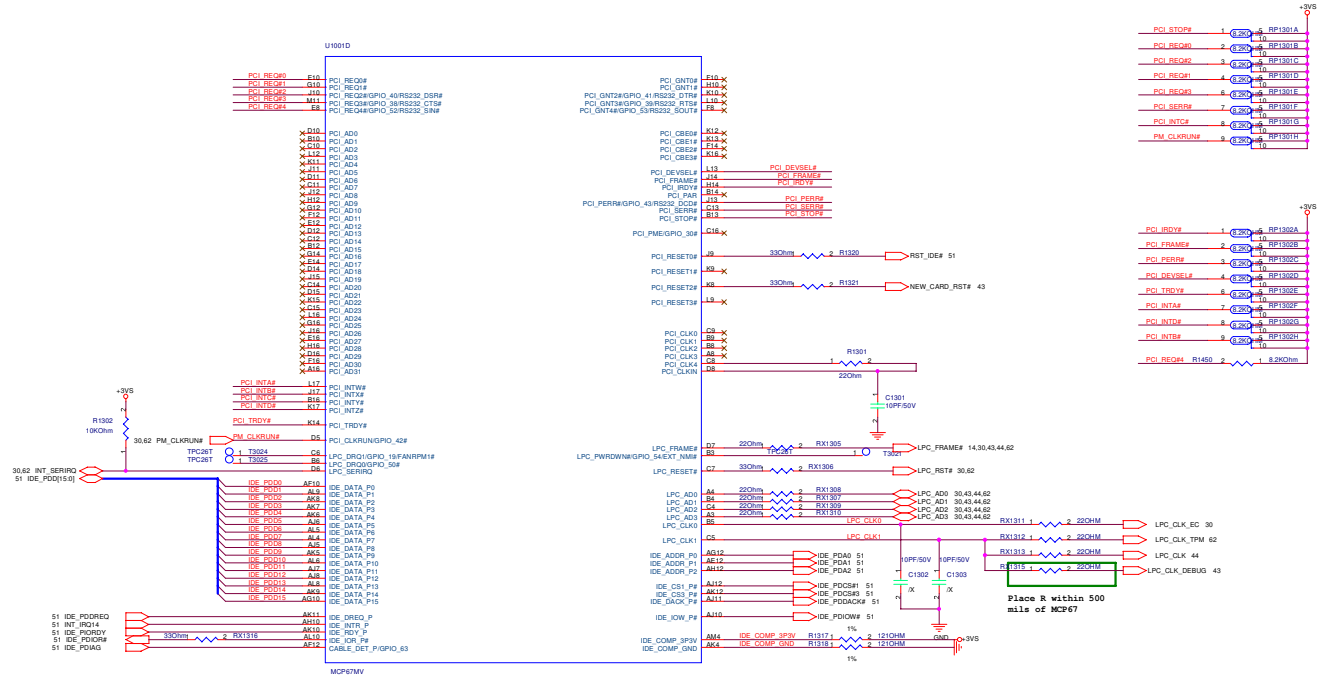


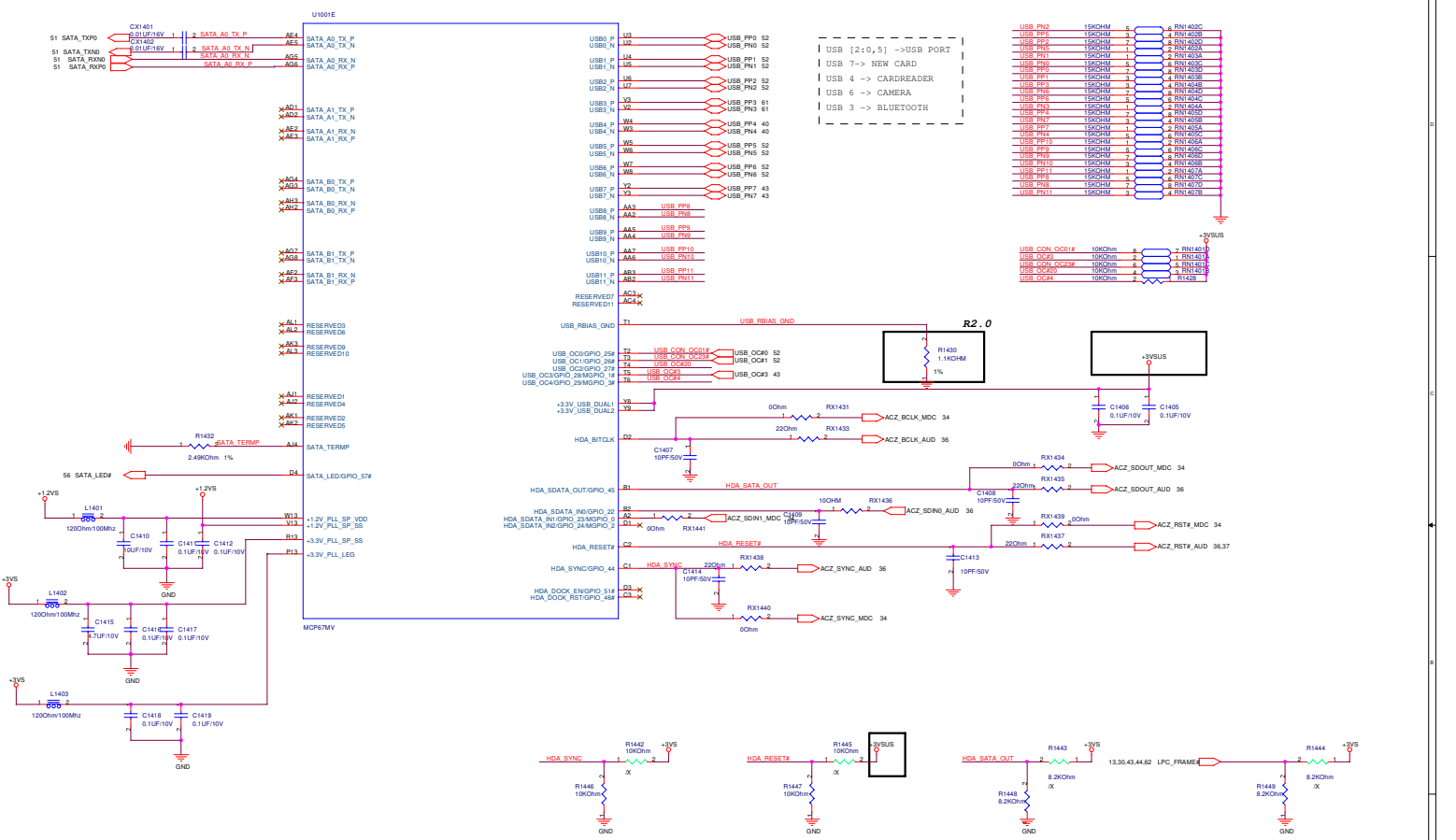


ASUS Title: FSU
ASUSTek Computer Inc. Engineer: He Wang

| Rev | Project Name | Rev |
|-----|--------------|-----|
| 1 | FSU | 1.0 |

Date: 2023-09-20 Time: 15:00:00 Sheet: 13 of 38



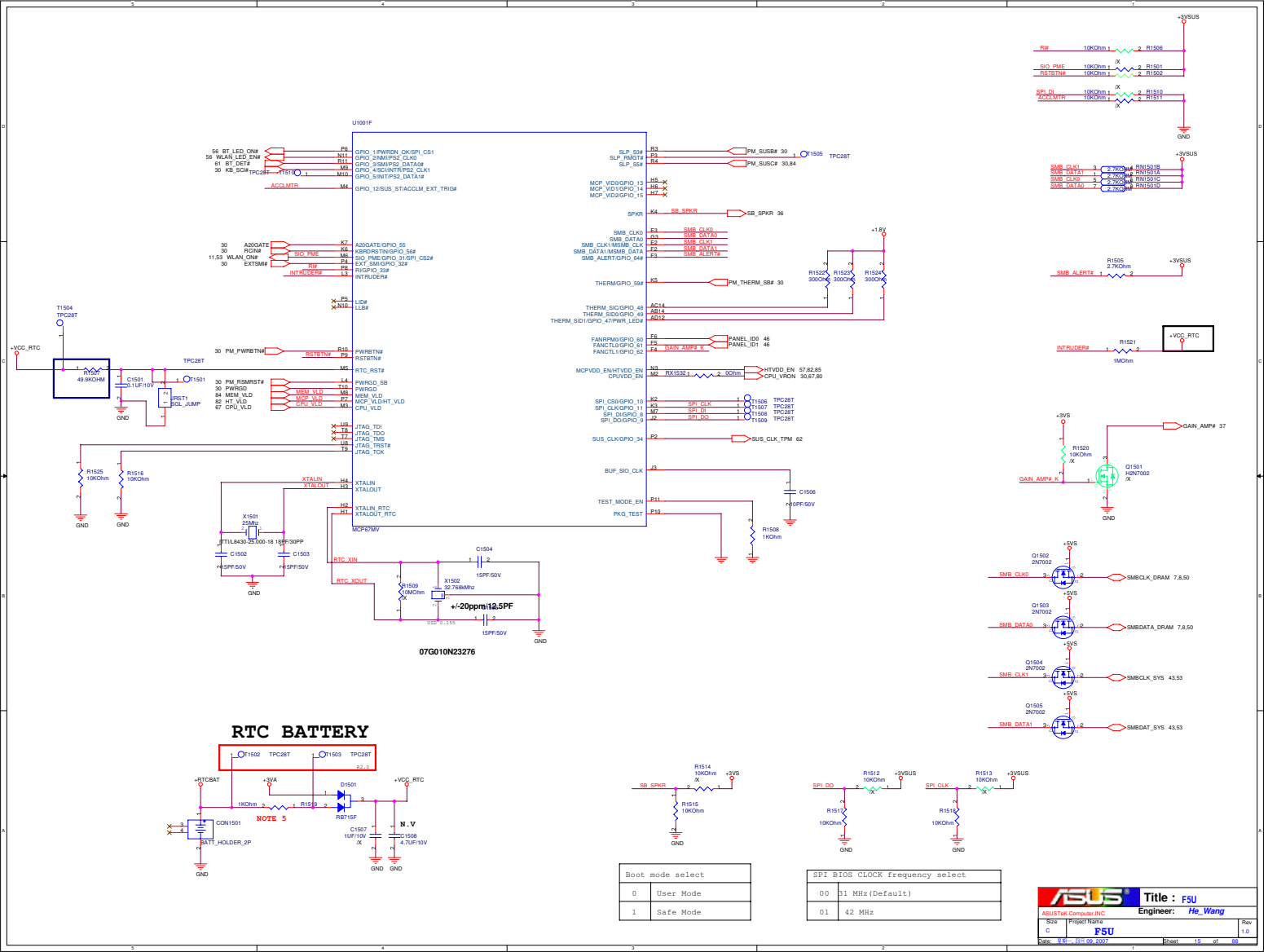


| SIO CLOCK select | |
|------------------|------------------------|
| 0 | 14.31818 MHz (Default) |
| 1 | 24 MHz |

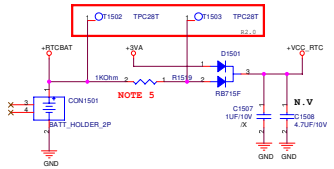
| Networking select | |
|-------------------|------|
| 0 | MII |
| 1 | RGMI |

| BIOS Select | |
|-------------|----------|
| 00 | LPC BIOS |
| 01 | PCI BIOS |

ASUS Title : FSU
 ASUSTek Computer INC Engineer: He Wang
 Rev: 1.0
 Date: 2014-09-23 10:07 Sheet: 14 of 26



RTC BATTERY

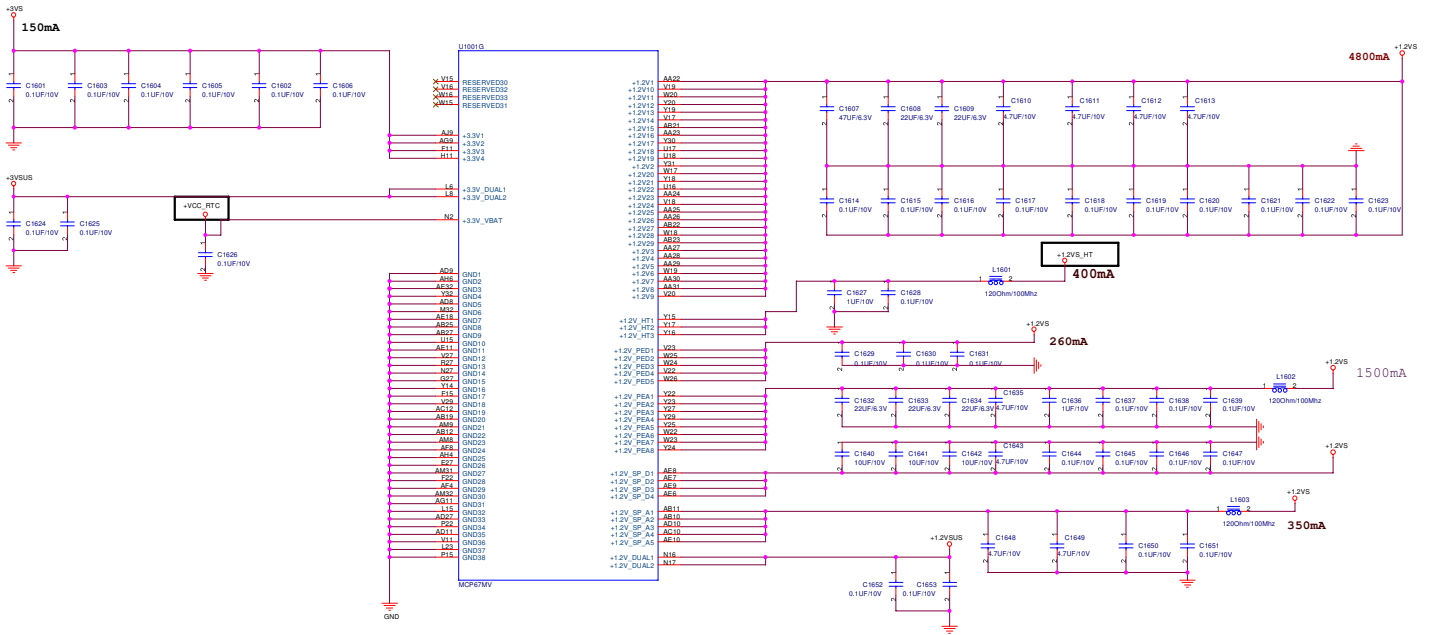


Boot mode select

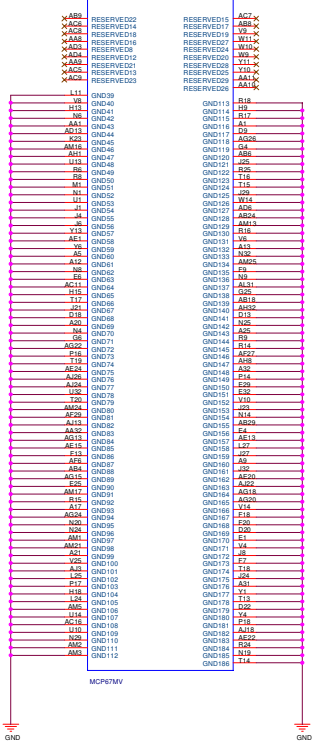
| | |
|---|-----------|
| 0 | User Mode |
| 1 | Safe Mode |

SPT BIOS CLOCK frequency select

| | |
|----|------------------|
| 00 | 81 MHz (Default) |
| 01 | 42 MHz |




UFD01H





RESERVE200
RESERVE201
RESERVE202
RESERVE203
RESERVE204
RESERVE205
RESERVE206
RESERVE207
RESERVE208
RESERVE209


AC7
AC8
AC9
AC10
AC11
AC12
AC13
AC14
AC15
AC16
AC17
AC18
AC19
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AC109
AC110
AC111
AC112


| | | | |
|------------------------|--------------|-------------------|-------|
| | | Title : FSU | |
| ASUSTek Computer INC | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | | 1.0 |
| Date: 2023-05-26 10:07 | | Sheet: 17 | of 26 |


| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-26 10:07 | | Sheet: 18 | of 28 |


| | | | |
|---|--------------|-------------------|----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-05-26 10:07 | Sheet: 18 | of | 28 |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 25 of 25 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 21 of 28 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 25 of 25 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 23 of 28 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 24 of 28 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | Sheet: 25 of 25 | |

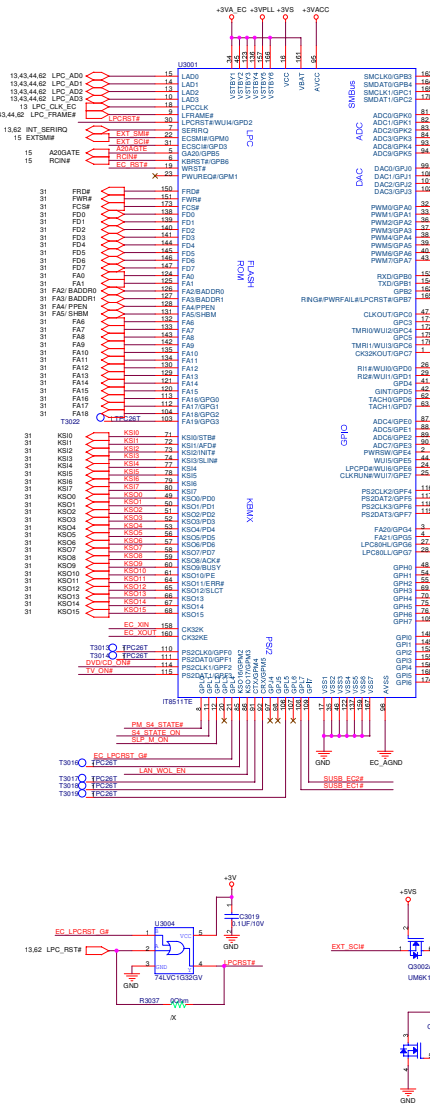
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|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | Sheet: 25 of 25 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 21 of 28 | |

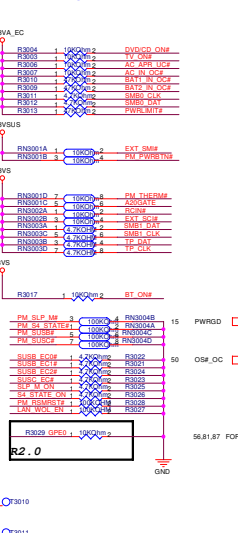
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|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 25 of 25 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 25 of 25 | |

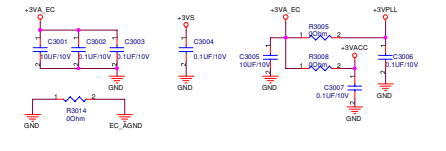
For IT8511 Core IC



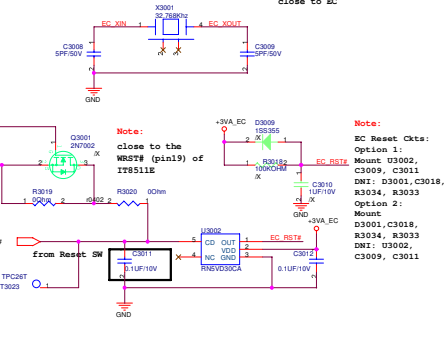
For Pull-up/Pull-down



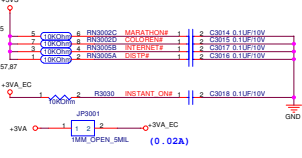
For IT8511 Power



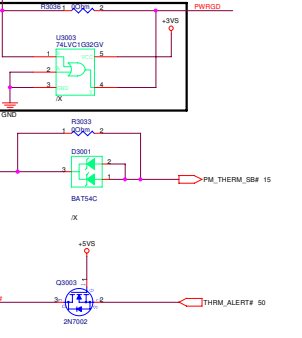
For Xtal



For Instant Key



For Instant Key

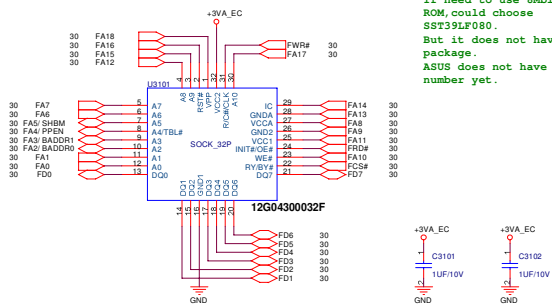


KBC connector

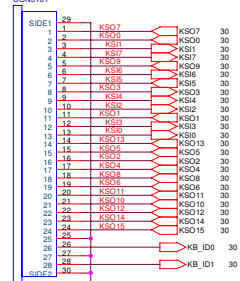
ISA ROM (4Mbits)

SST-PLCC32 4Mbits Flash ROM
 PN:05G001014110
 (FLASH SST S3239VF040-70-4C-NHE
 4M-70 PLCC-32)

If need to use 8Mbits ISA ROM, could choose SST39LF080.
 But it does not have PLCC32 package.
 ASUS does not have part number yet.



CON3101

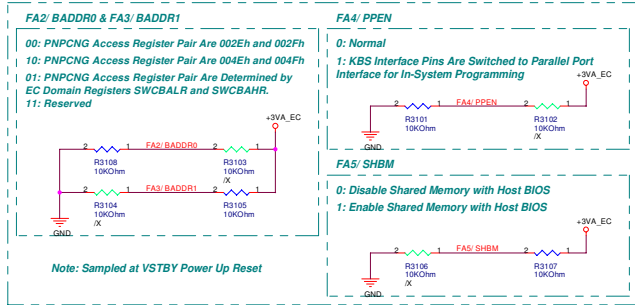


FFC_CON 28P
 12G182402806


| | | | |
|------|----|----|----|
| TYPE | JP | UK | US |
| KID1 | H | H | L |
| KID2 | L | H | L |

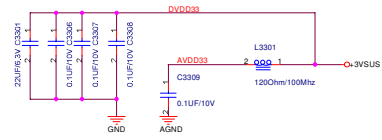
ISA ROM

EC Hardware Strapping

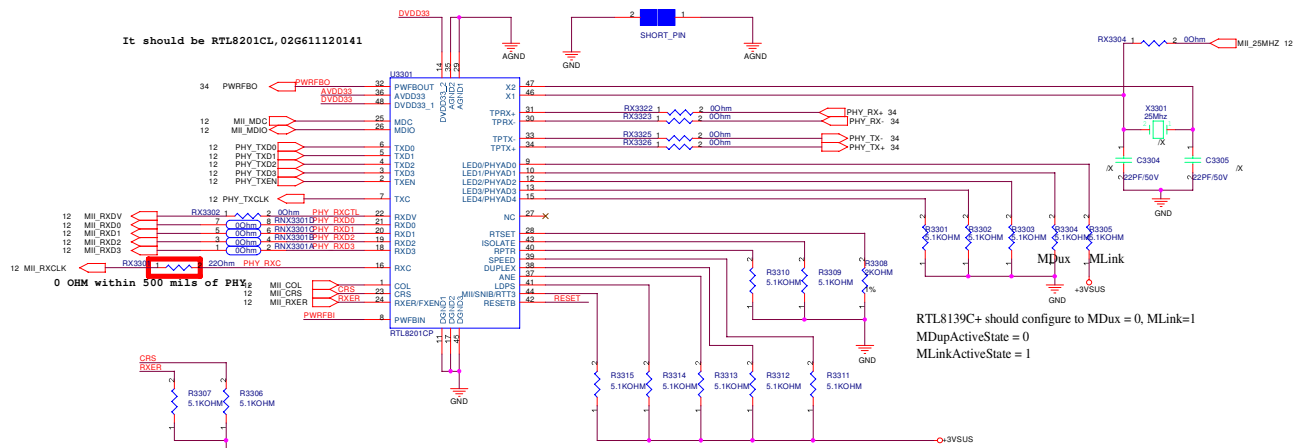


Note: Sampled at VSTBY Power Up Reset

| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2023-05-25 10:07 | | Sheet: 01 | of 01 |

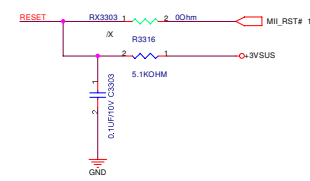
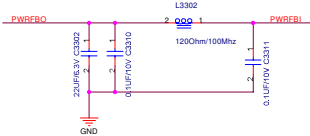


It should be RTL8201CL, 02G61120141

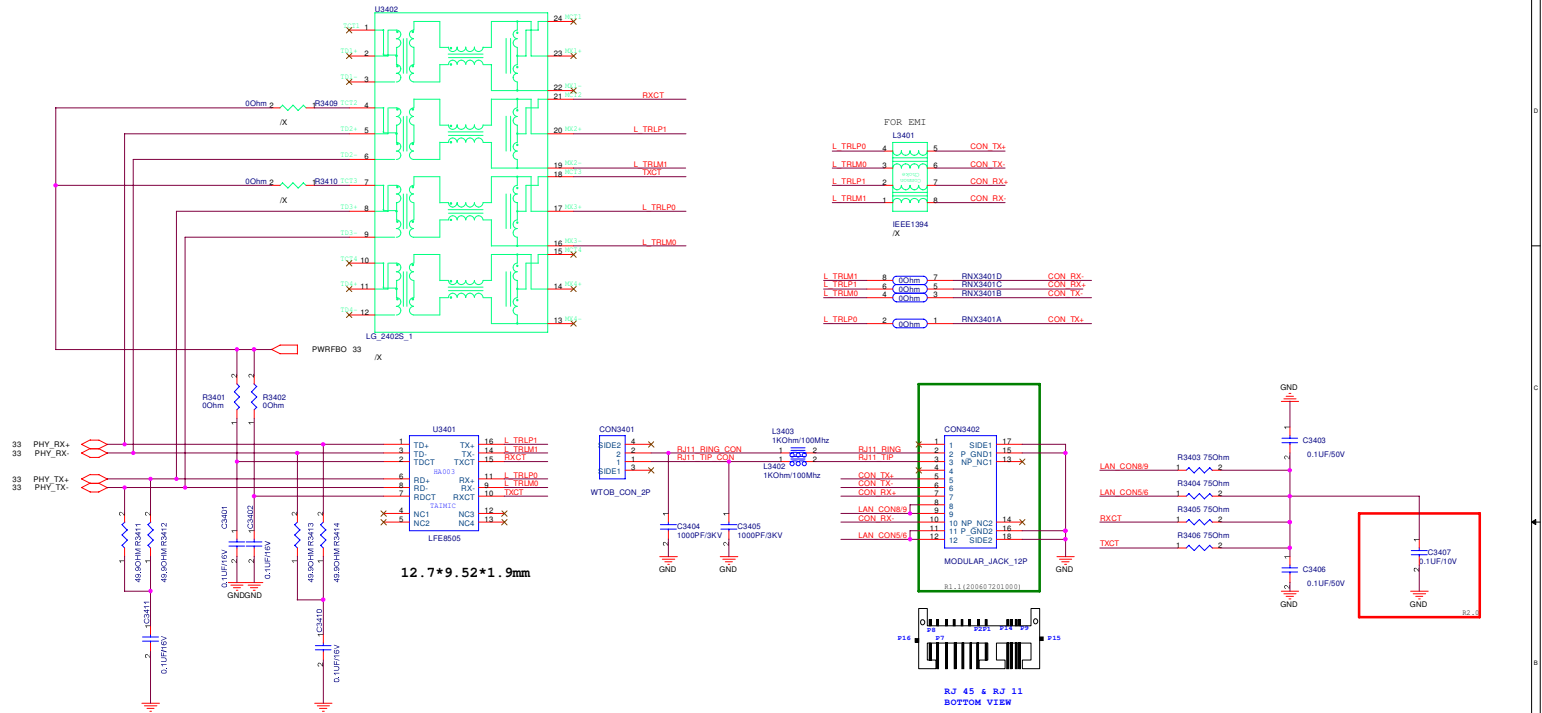


RTL8139C+ should configure to MDux = 0, MLink=1
 MDupActiveState = 0
 MLinkActiveState = 1

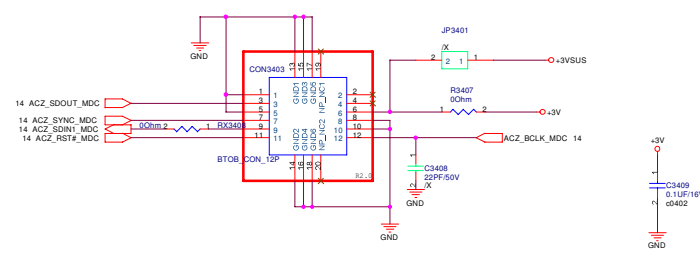
- ISOLATE: set high to isolate the RTL8201CP from the MAC this will also isolate the MC/MDIO managemet interface
- RPTR: set high to put the TRL8201CP into repeater mode
- SPEED: this pin is latched to input during a power on or reset condition. set high to put the RTL8201CP into 100Mbps operation
- DUPLEX: Set high to enable full duplex
- ANE: Set high to enable auto-negotiation mode, set low to force mode
- LDPS: set high to put the RTL8201CP into LDPS mode
- MII/SNIB: pull high to set the RTL8201CP into MII mode operation. set low for SNI mode

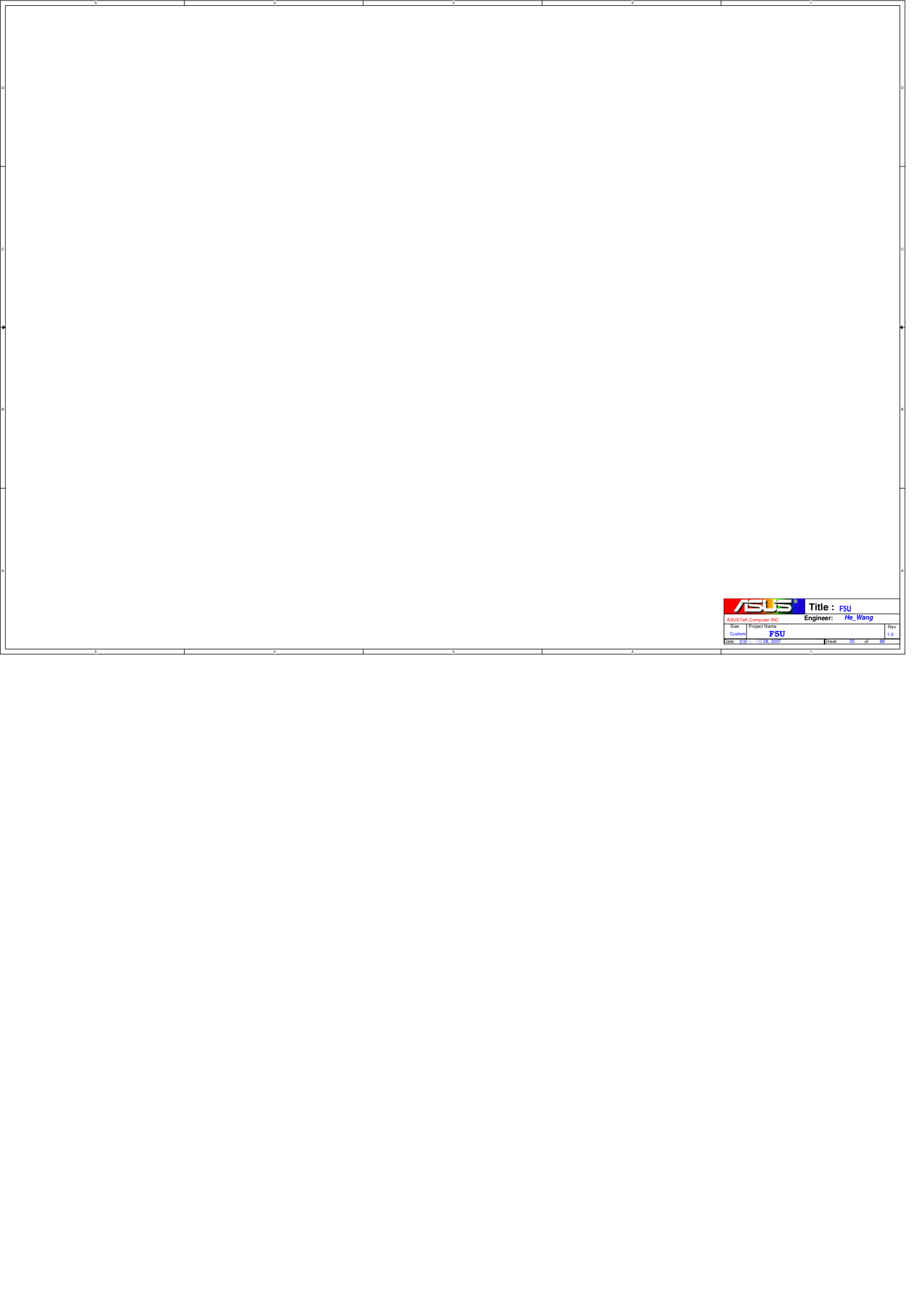


LAN PORT



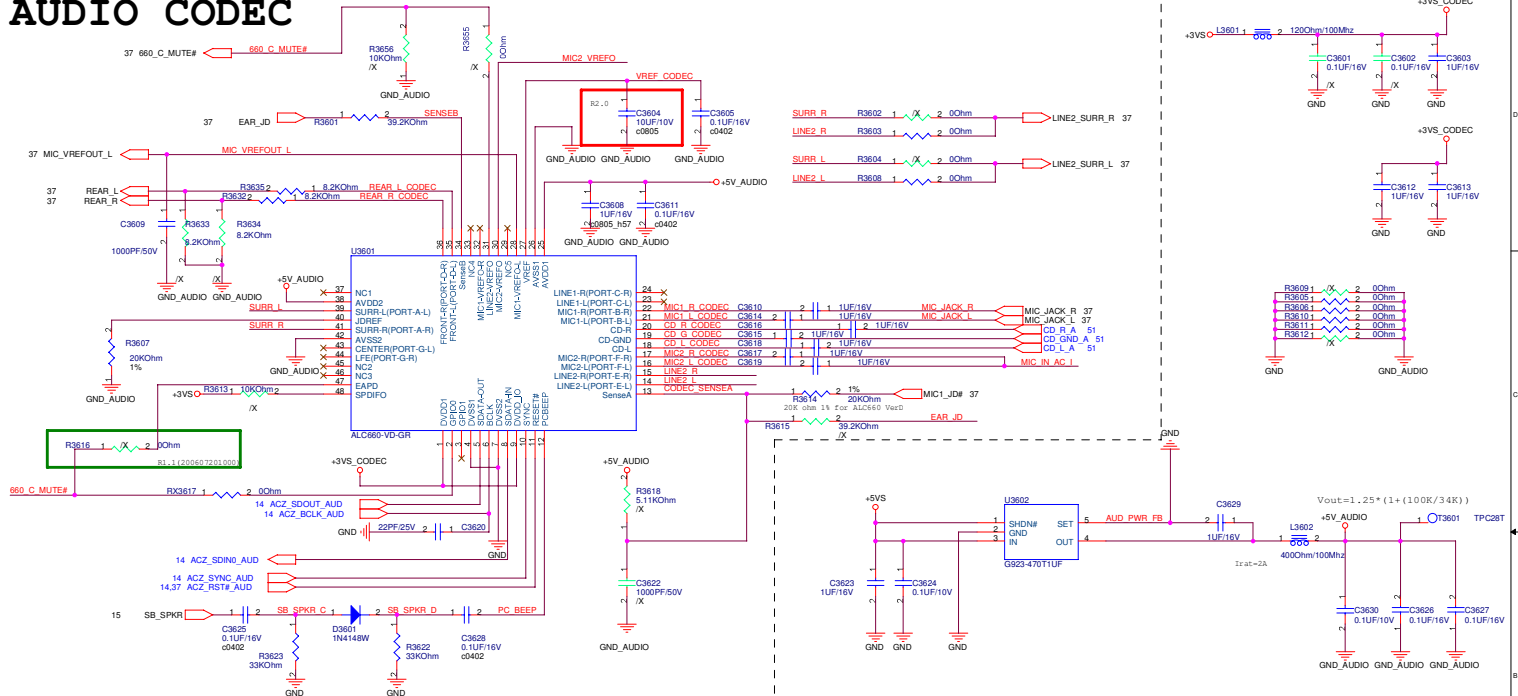
MDC CONN.



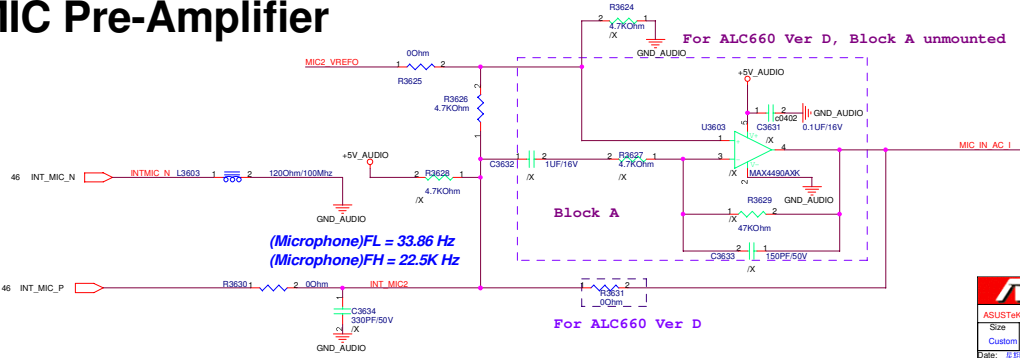


| | | |
|---|--------------|--------------------------|
|  | | Title : FSU |
| ASUS Tek Computer INC | | Engineer: He_Wang |
| Size | Project Name | Rev |
| Custom | FSU | 1.0 |
| Site: 010-11-28-2007 | | Sheet 05 of 08 |

AUDIO CODEC

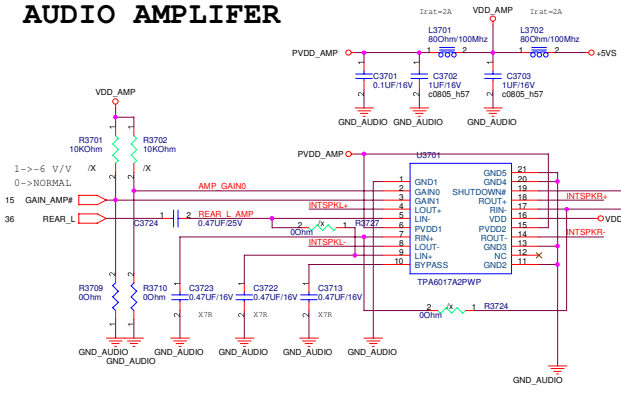


Internal MIC Pre-Amplifier



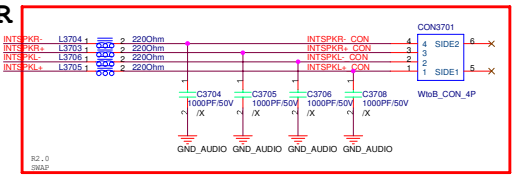
| | | | |
|-----------------------|--------------|--------------------|-------|
| ASUS | | Title : FSU | |
| ASUSTek Computer, INC | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| Custom | FSU | | 1.0 |
| Date: 11/09/2007 | Sheet | 36 | of 38 |

AUDIO AMPLIFIER

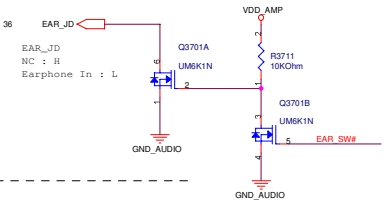


SPEAKER

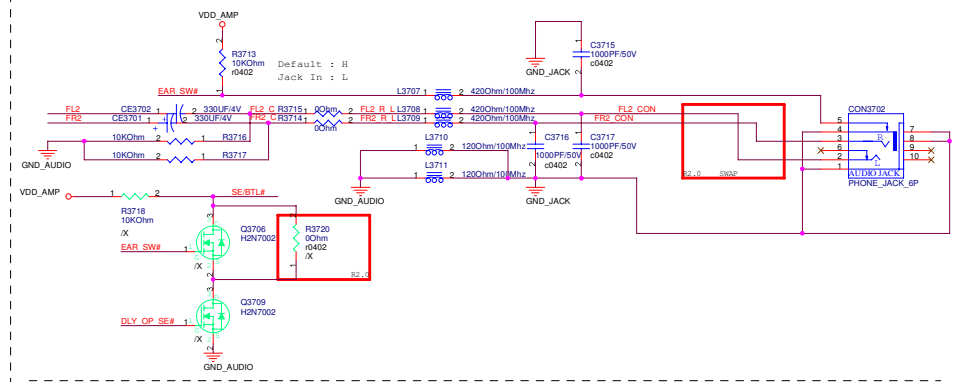
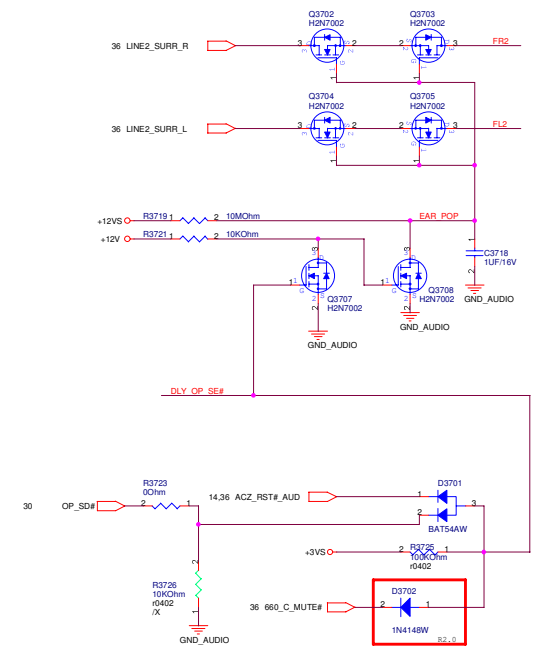
To Internal Speaker Connector



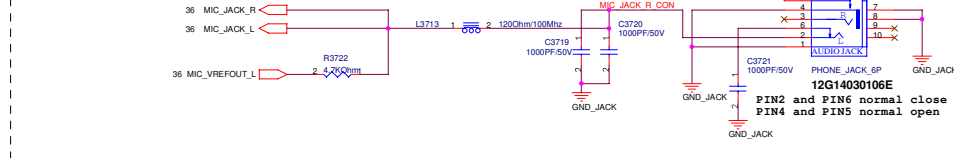
HeadPhone



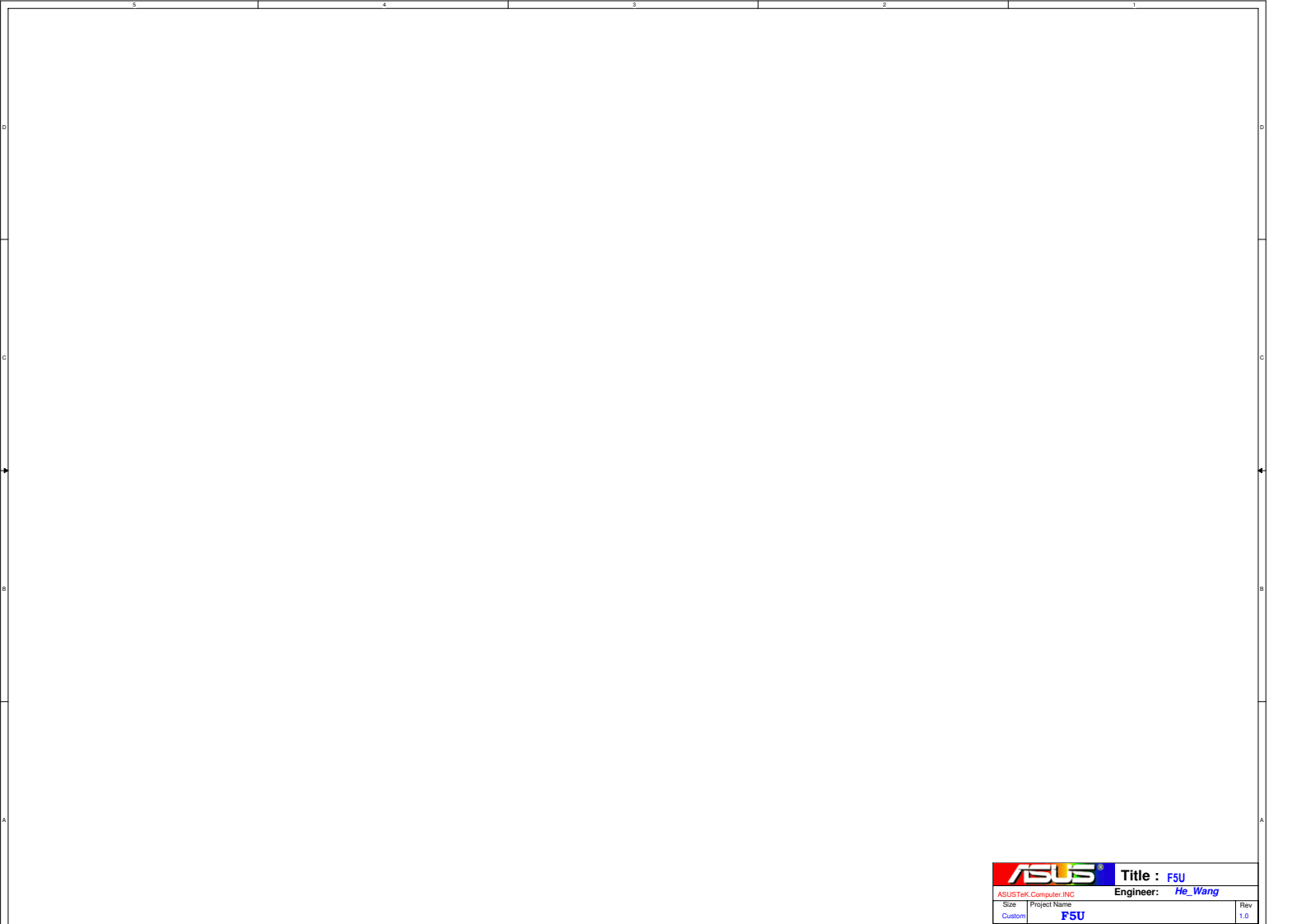
DEPOP CIRCUIT





External Microphone

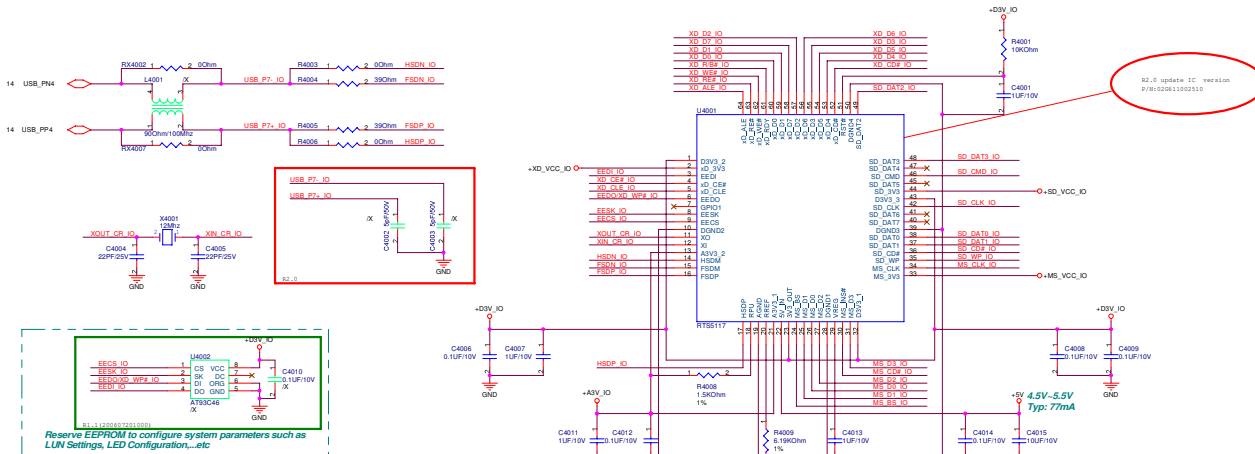


ASUS Title : FSU
 ASUSTeK Computer, INC Engineer: He_Wang
 Size Project Name
 Custom FSU
 Date: 11/19/09 2007 Sheet 37 of 38

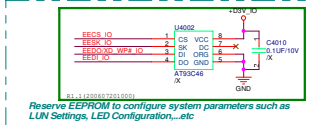
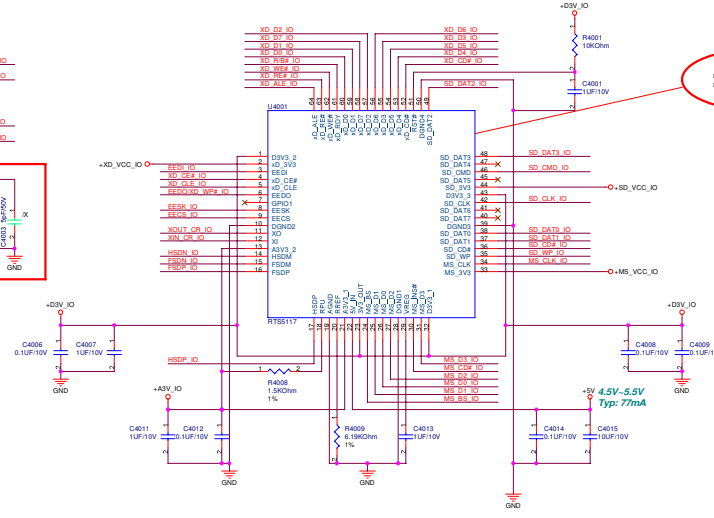


| | | | |
|---|--------------|--------------------------|----------|
|  | | Title : FSU | |
| ASUSTeK Computer INC | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| Custom | FSU | | 1.0 |
| Date: 2007-11-28 | | Sheet | 38 of 38 |

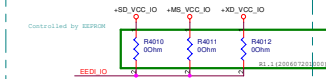
| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-05-25 10:07 | Sheet: 01 | | of 01 |



BIOS update IC version
P/N:0261100210



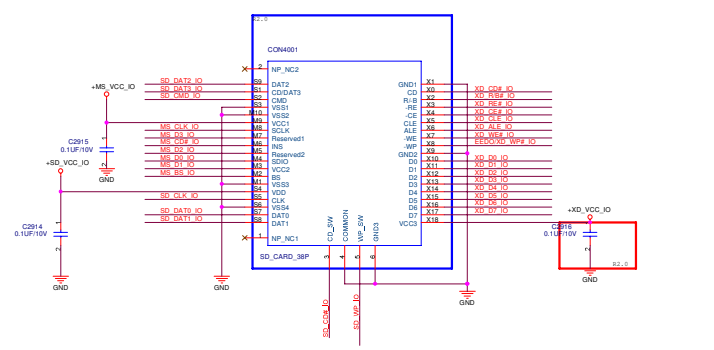
Reserve EEPROM to configure system parameters such as LUN Settings, LED Configuration...etc

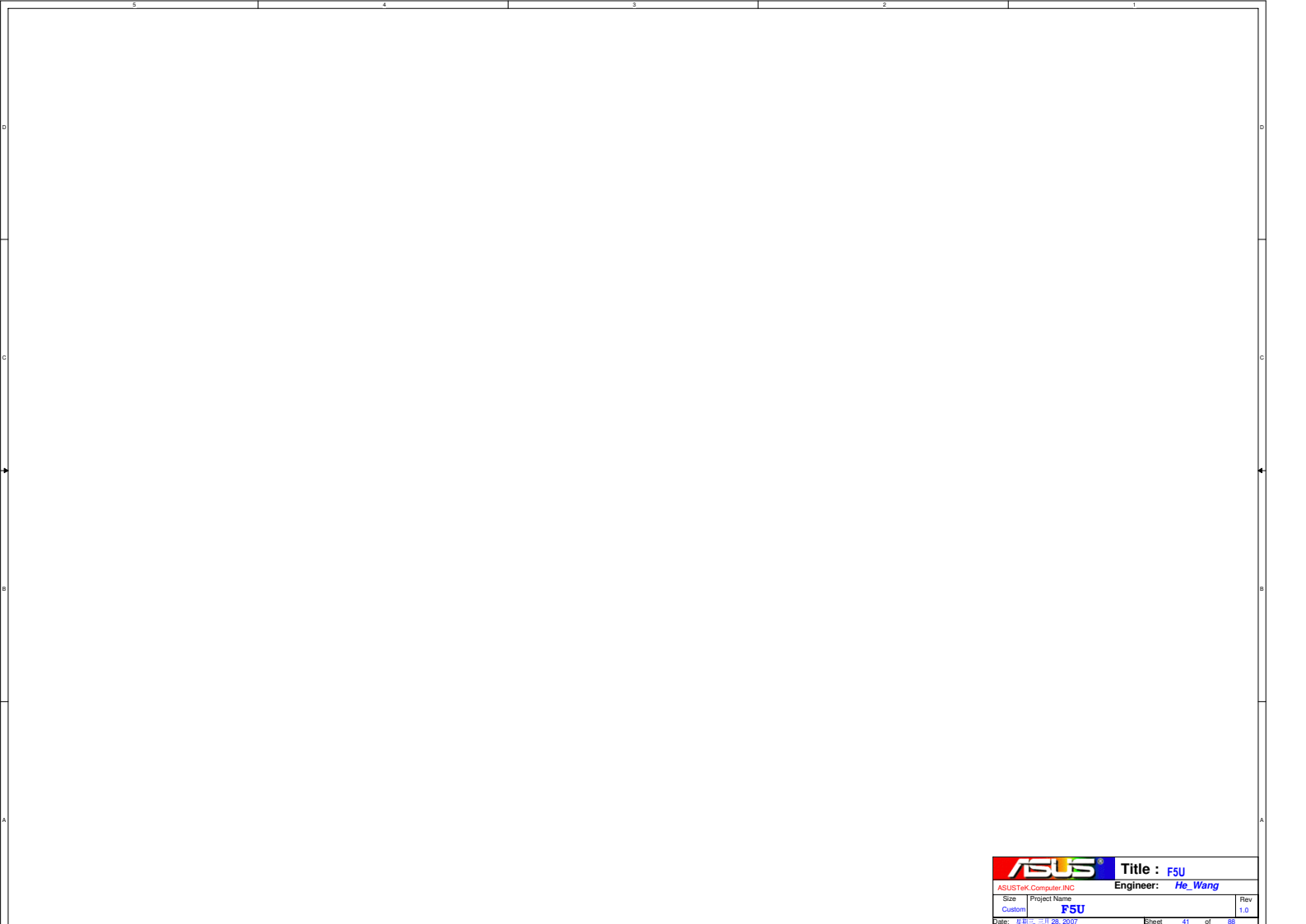



| | R2910 | R2911 |
|---|----------|----------|
| SD/MMC only | No Stuff | No Stuff |
| xD/SD/MMC/MS/MS-Pro Combo Support CPU C3 State | No Stuff | 4.7K |
| SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State | 4.7K | No Stuff |
| SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State | 4.7K | 4.7K |

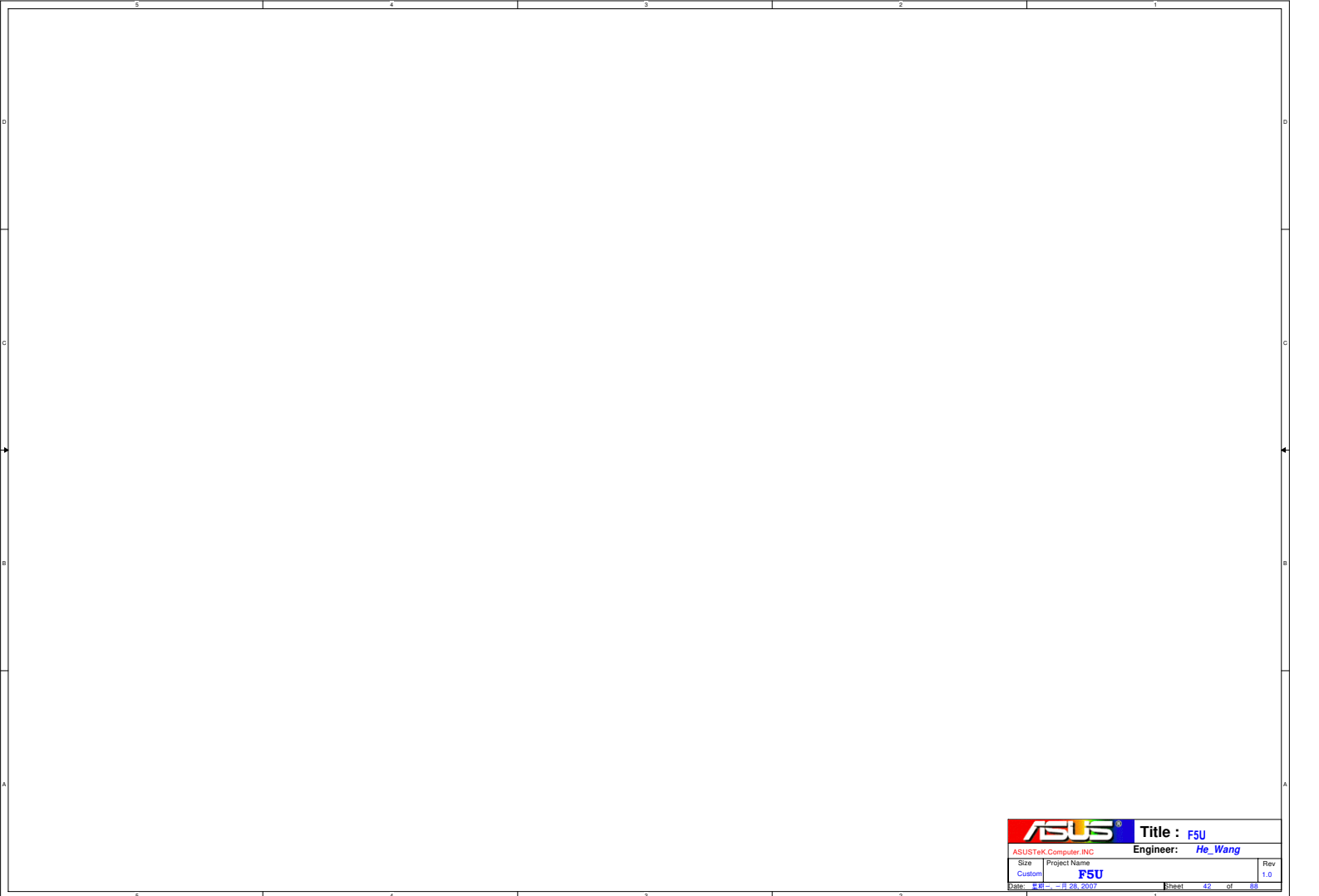
IO_R41 should be present if system doesn't use EEPROM to configure LED.


Through these pull-high resistors, EEPROM can be saved if no other requirement about other parameters.





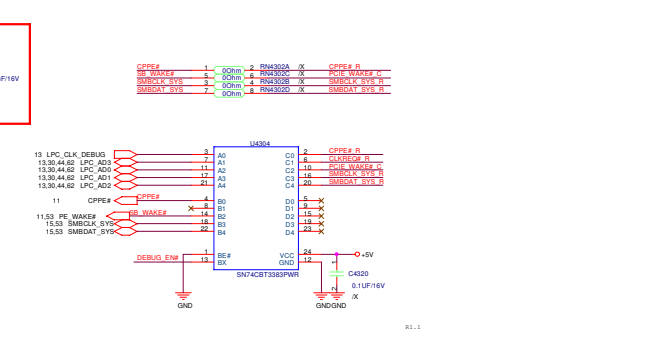
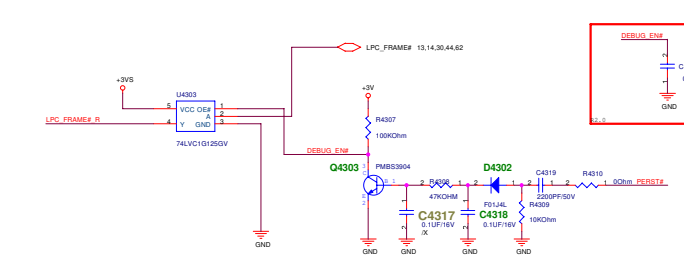
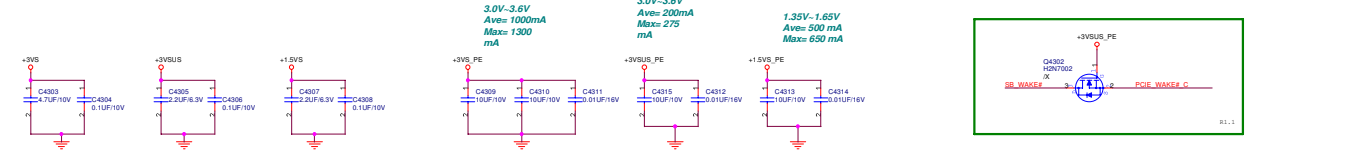
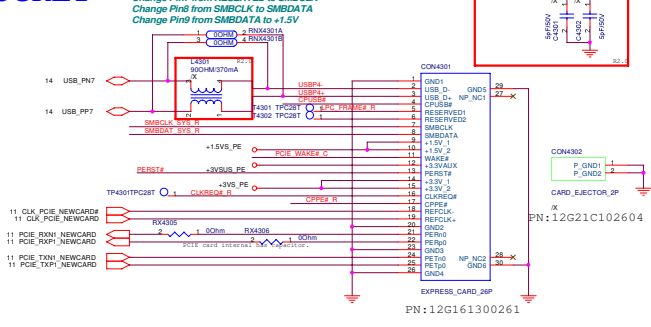
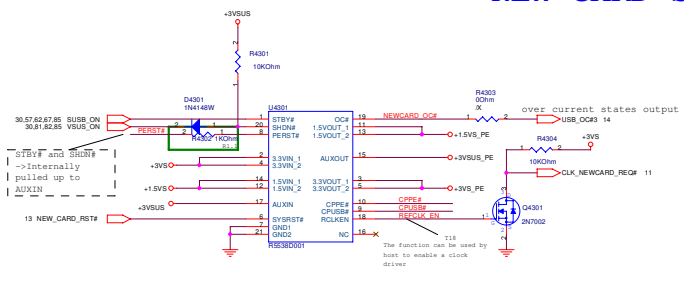
| | | |
|---|--------------|--------------------------|
|  | | Title : FSU |
| ASUSTeK Computer INC | | Engineer: He_Wang |
| Size | Project Name | Rev |
| Custom | FSU | 1.0 |
| Date: 11/23/2007 | Sheet | 41 of 88 |



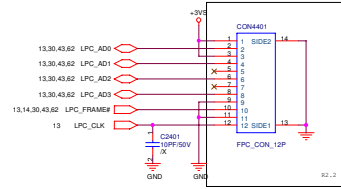
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|--|----------------|--------------------------|---|
|  | | Title : FSU | |
| ASUSTeK Computer INC | | Engineer: He_Wang | |
| Size | Project Name | Rev | |
| Custom | FSU | 1.0 | |
| Date: 08-28-2007 | Sheet 42 of 68 | | 1 |

NEW CARD SOCKET

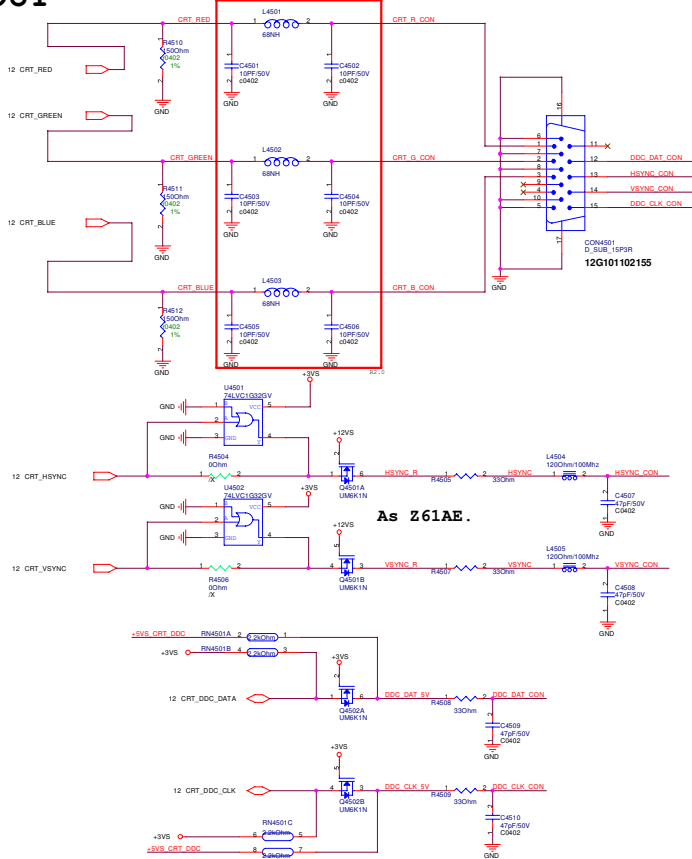
!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



LPC DEBUG CONNECTOR

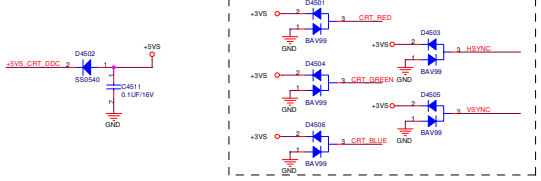


VGA OUT

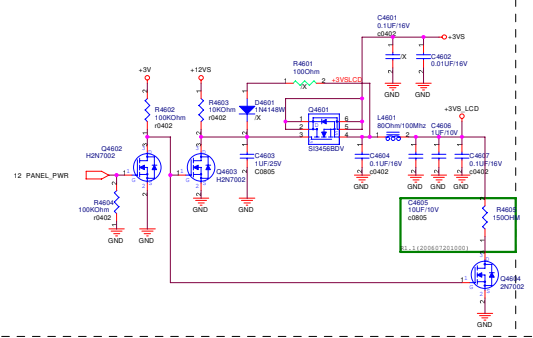


As Z61AE.

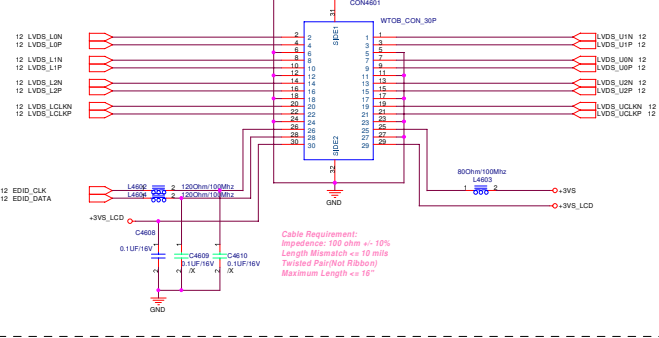
PLACE ESD Diodes near VGA port



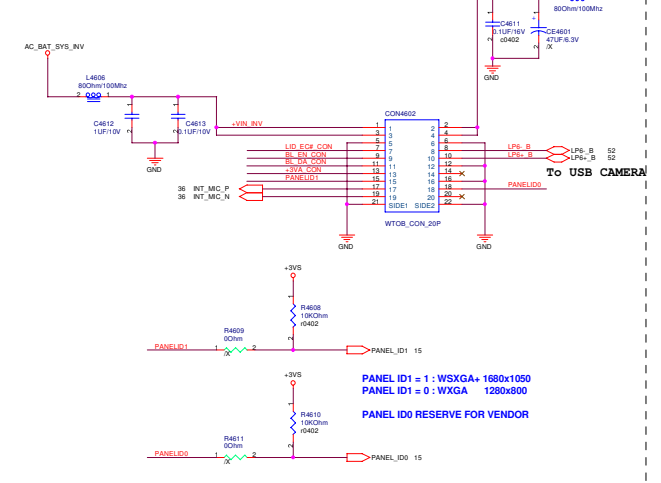
LCD Power



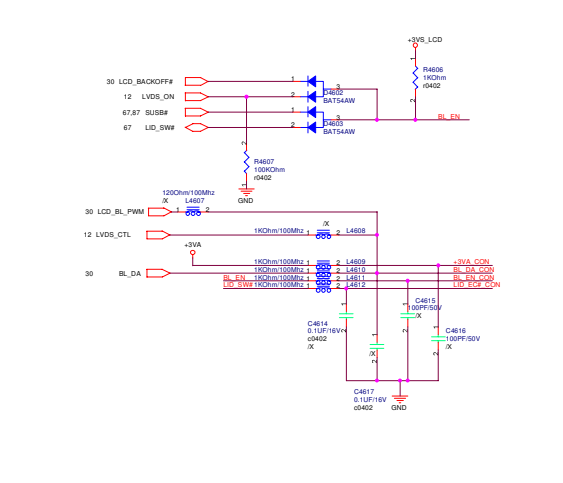
LCD LVDS Interface

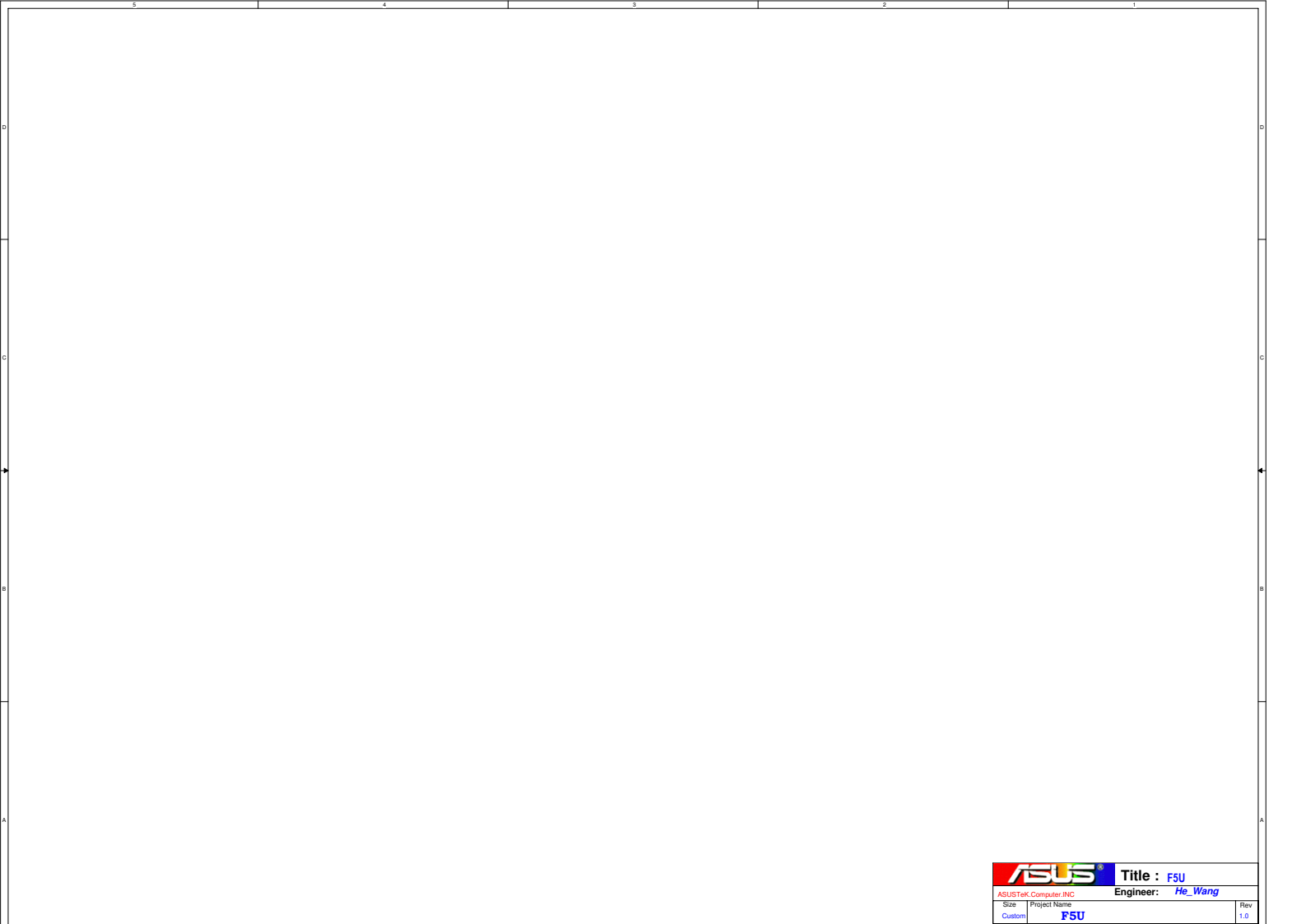



INVERTER Interface





Backlight Enable





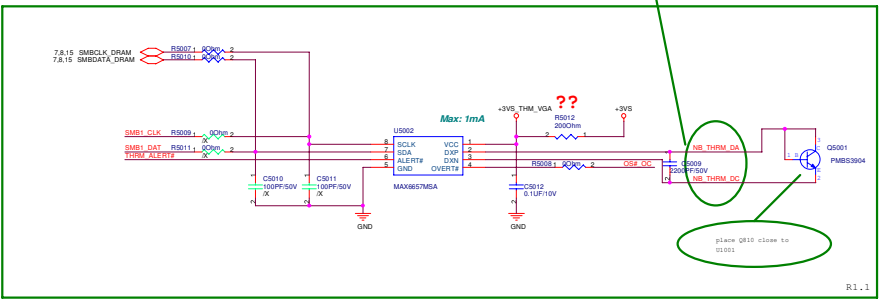
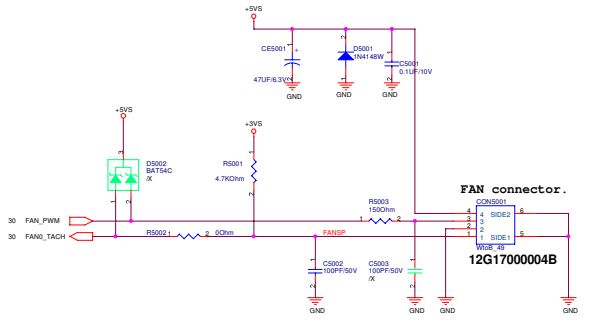
| | | | |
|---|--------------|--------------------------|----------|
|  | | Title : FSU | |
| ASUSTeK Computer INC | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| Custom | FSU | | 1.0 |
| Date: 2007-08-28 | | Sheet | 47 of 88 |

| | | | |
|---|--------------|--------------------------|-----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | | 1.0 |
| Date: 2023-09-29 10:07 | Sheet: 48 | of | 88 |

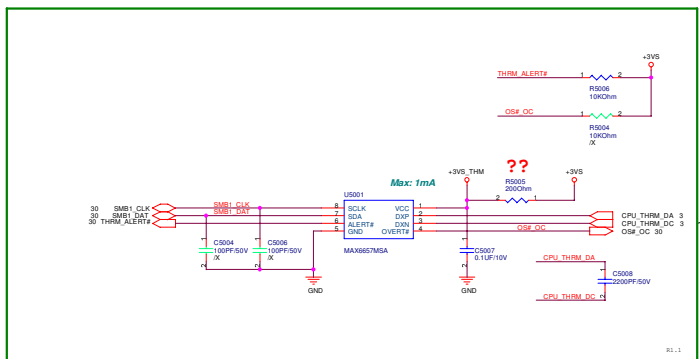
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|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2023-09-26 10:07 | | Sheet: 49 | of 50 |

DC FAN control

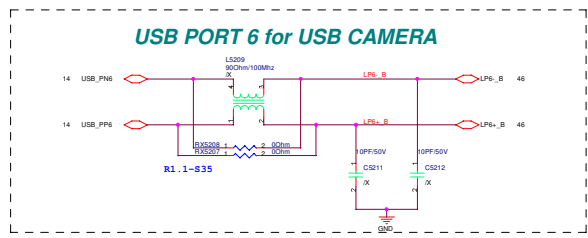
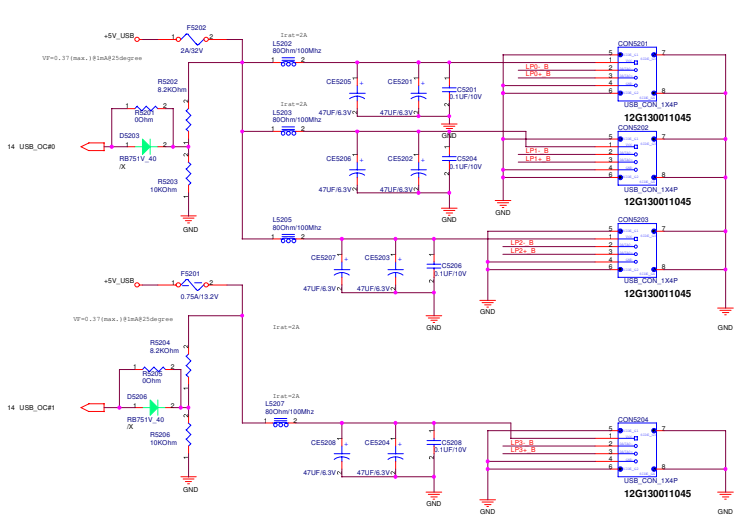
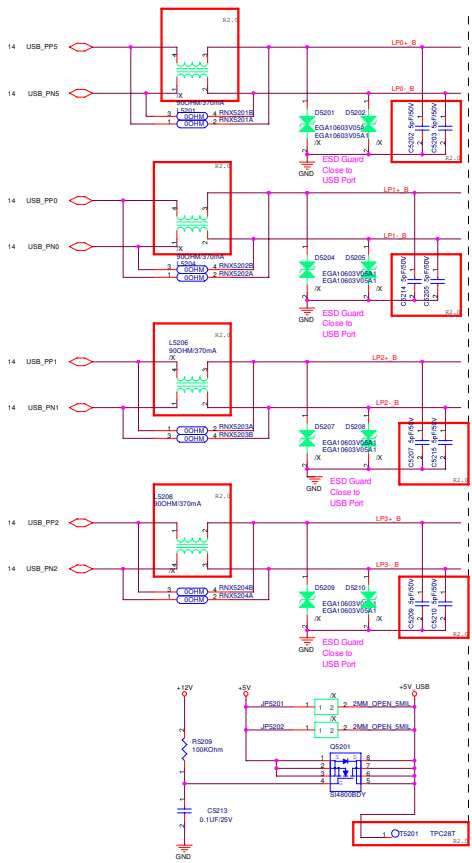
-----OTHER SIGNALS
 15 mils
 -----GND
 10 mils
 -----NB_THRM_DA(10 mils)
 10 mils
 -----NB_THRM_DC(10 mils)
 10 mils
 -----GND
 15 mils
 -----OTHER SIGNALS
 Avoid FSB,Power



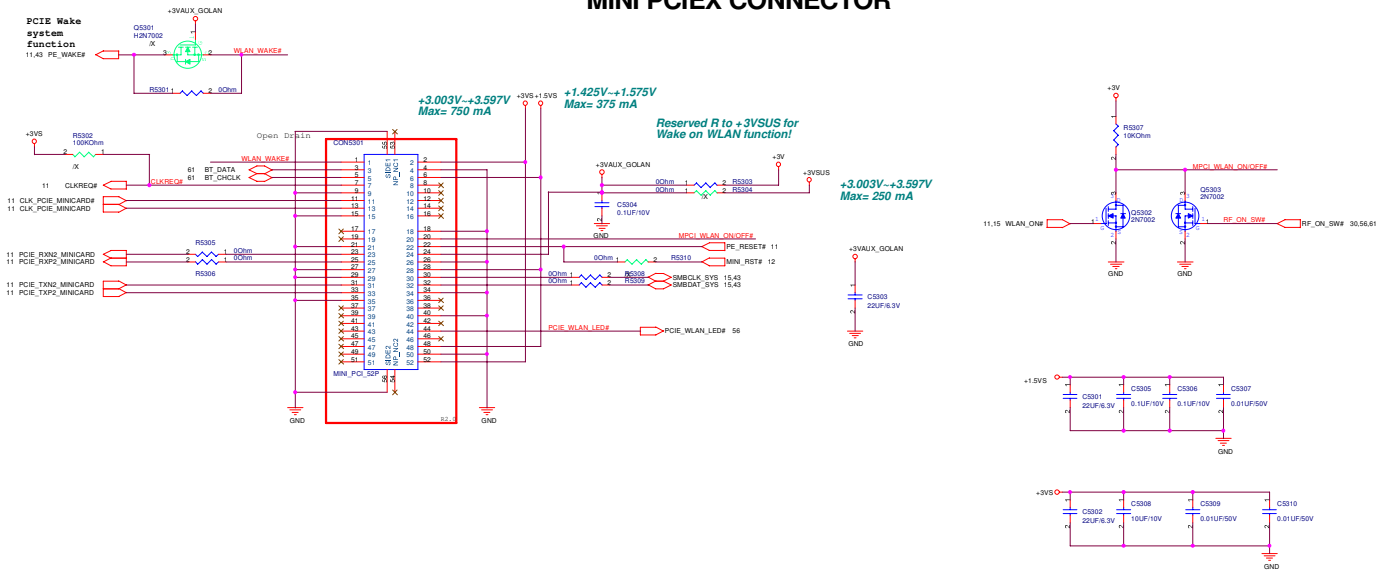
Thermal Sensor





Route CPU_THRM_DA and CPU_THRM_DC on the same layer
 15 mils
 -----GND
 10 mils
 -----H_THERMDA(10 mils)
 10 mils
 -----H_THERMDC(10 mils)
 15 mils
 -----GND
 -----OTHER SIGNALS
 Avoid FSB,Power

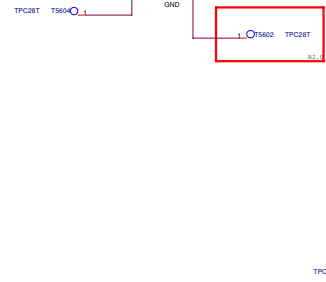
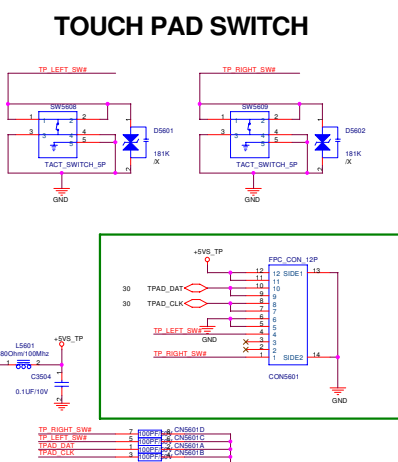
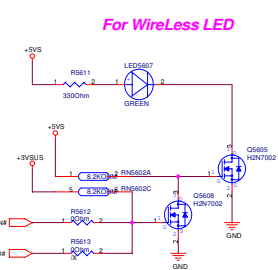
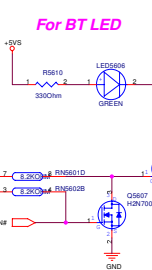
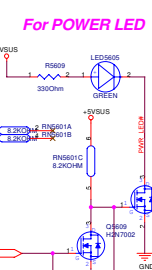
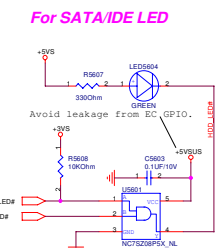
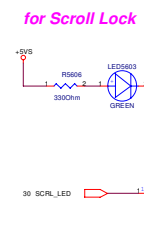
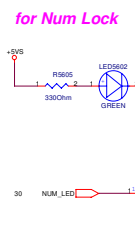
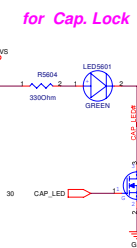
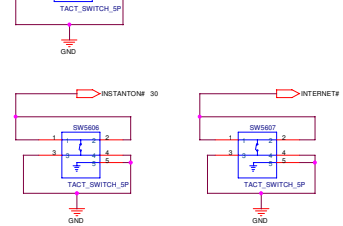
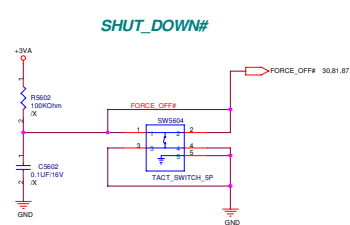
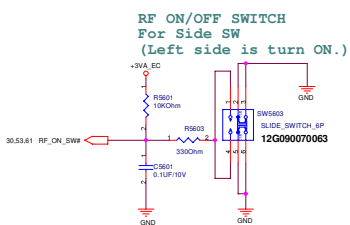
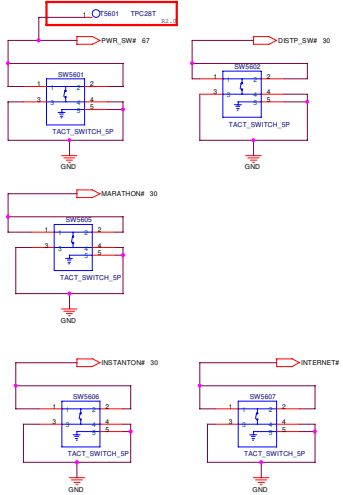


MINI PCIEX CONNECTOR

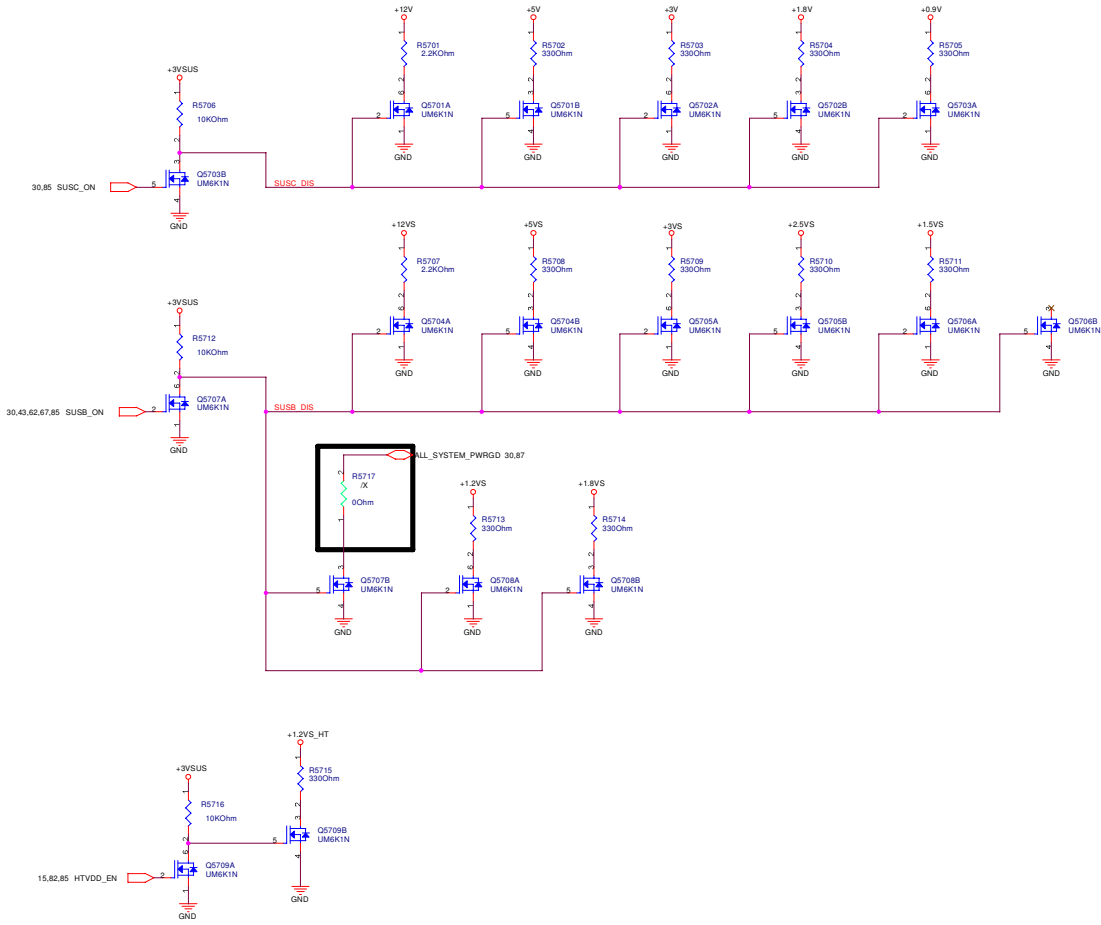



| | | | |
|---|--------------|--------------------------|----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-05-26 10:07 | Sheet: 54 | of | 58 |


| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-26 10:07 | | Sheet: 05 | of 05 |



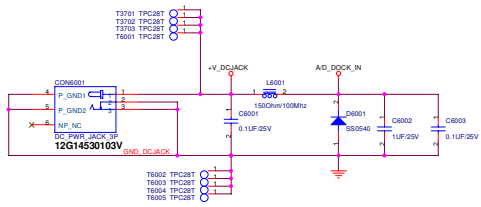
DISCHARGE CIRCUIT



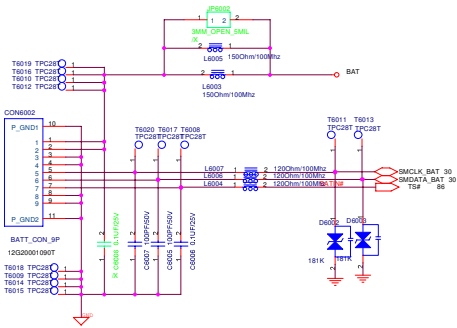
| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-25 10:07 | | Sheet: 01 | of 01 |

| | | | |
|---|--------------|--------------------------|-----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | | 1.0 |
| Date: 2011-03-29 10:07 | Sheet: 01 | of | 01 |

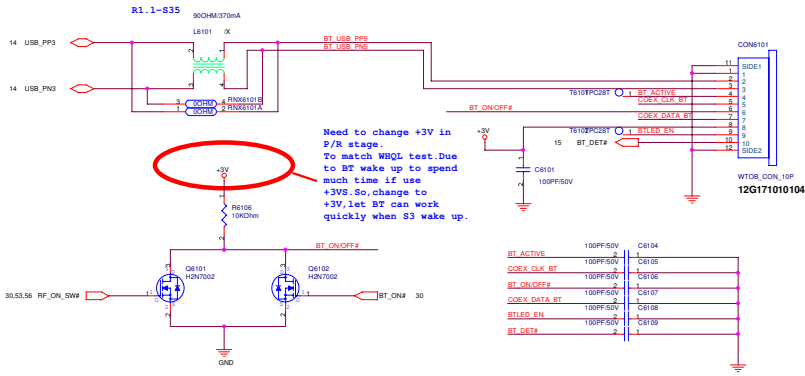
Adaptor IN Circuit



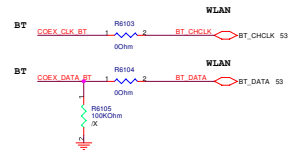
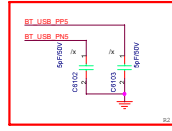
BATTERY IN CIRCUIT



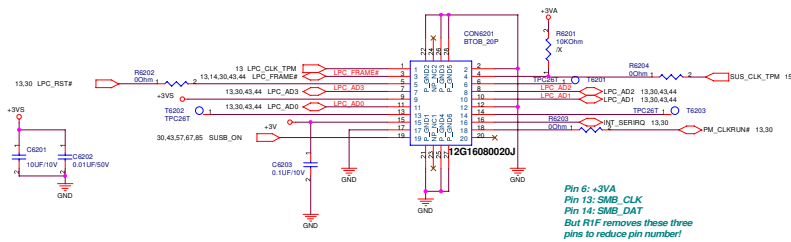
BLUETOOTH CONNECTOR





Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT





TPM CONN.

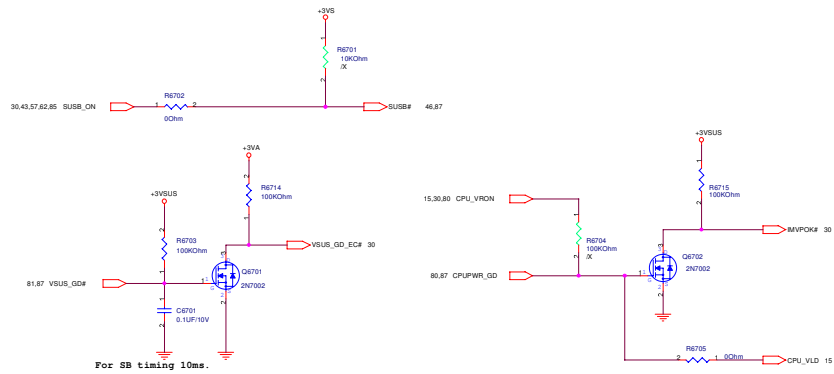


| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-26 10:07 | | Sheet: 61 | of 66 |

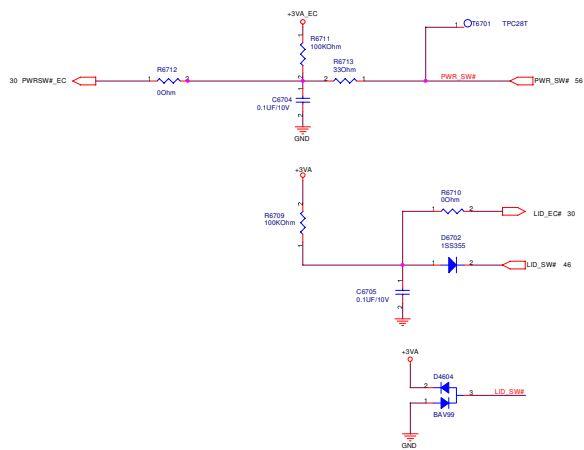
| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-03-29 10:07 | | Sheet: 64 | of 68 |

| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-25 10:07 | | Sheet: 65 | of 65 |

| | | | |
|---|--------------|-------------------|-------|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-05-25 10:07 | | Sheet: 01 | of 01 |

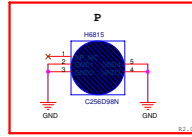
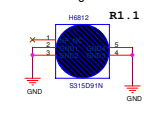
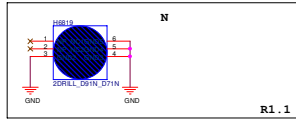
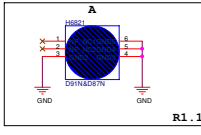
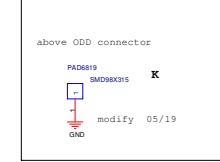
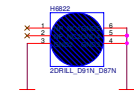
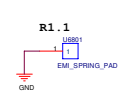
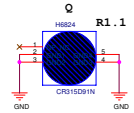
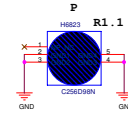
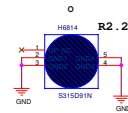
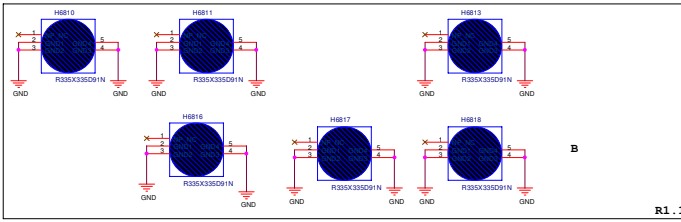
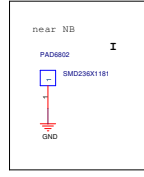
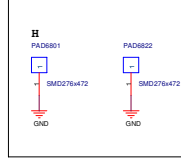
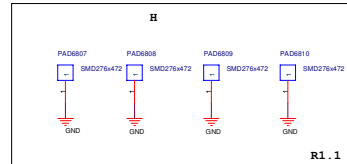
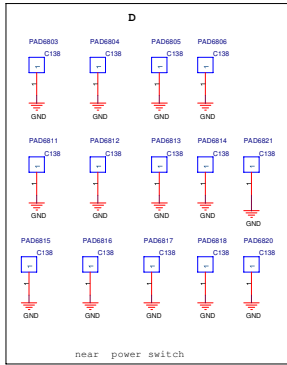
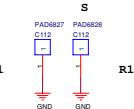
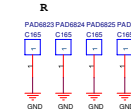
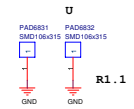
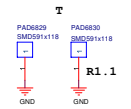
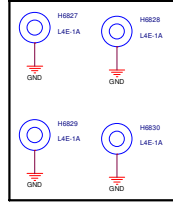
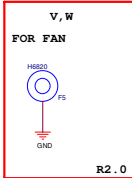
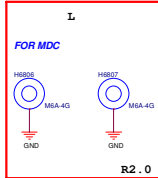
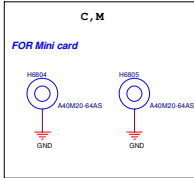
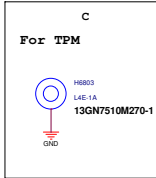
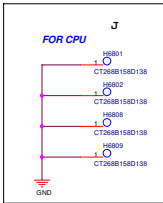



POWER SWITCH





| | | | |
|------------------------|--------------|--------------------|----|
| ASUS | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-01-20 10:07 | Sheet: 67 | of | 68 |


FOR Thermal
R2.0





| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | | 1.0 |
| Date: 2011-05-26 10:07 | Sheet: 01 | of | 01 |


| | | | |
|---|--------------|-------------------|----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | 1.0 | |
| Date: 2011-05-26 10:07 | Sheet: 01 | of | 01 |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 11 of 28 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2007-11-26 2007 | | Sheet: 15 of 28 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 13 of 28 | |


| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | Sheet: 14 of 28 | |

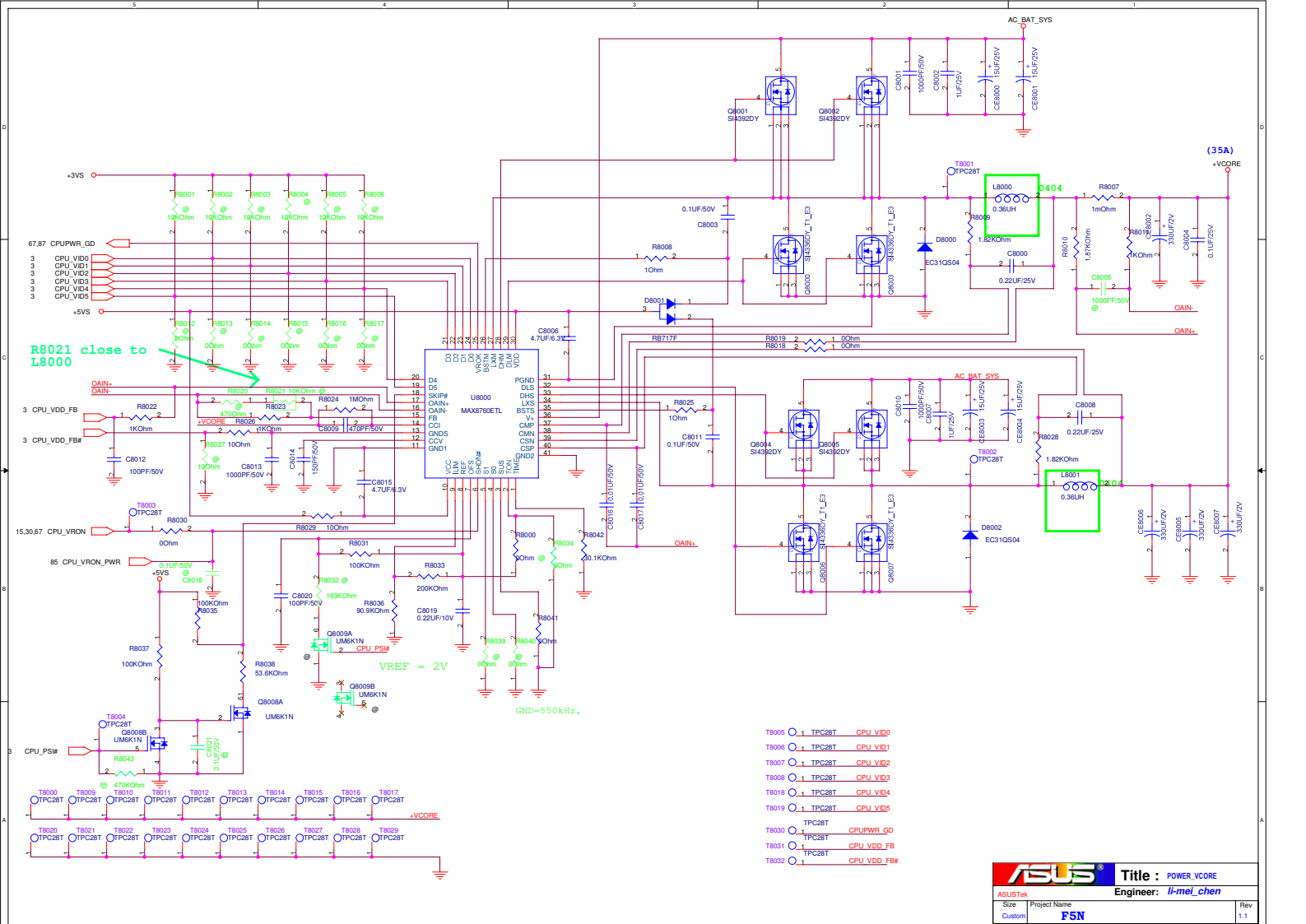
| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | Sheet: 15 of 28 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2017-11-28 20:07 | | Sheet: 16 of 28 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2011-11-28 2007 | | Sheet: 11 of 28 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTeK Computer INC. | | Engineer: He_Wang | |
| Size | Project Name | | Rev |
| C | FSU | | 1.0 |
| Date: 2007-11-26 2007 | | Sheet: 15 of 25 | |

| | | | |
|---|--------------|-------------------|-----|
|  | | Title : FSU | |
| ASUSTek Computer Inc. | | Engineer: He Wang | |
| Size | Project Name | Rev | |
| C | FSU | | 1.0 |
| Date: 2011-03-29 10:07 | Sheet: 01 | of | 01 |

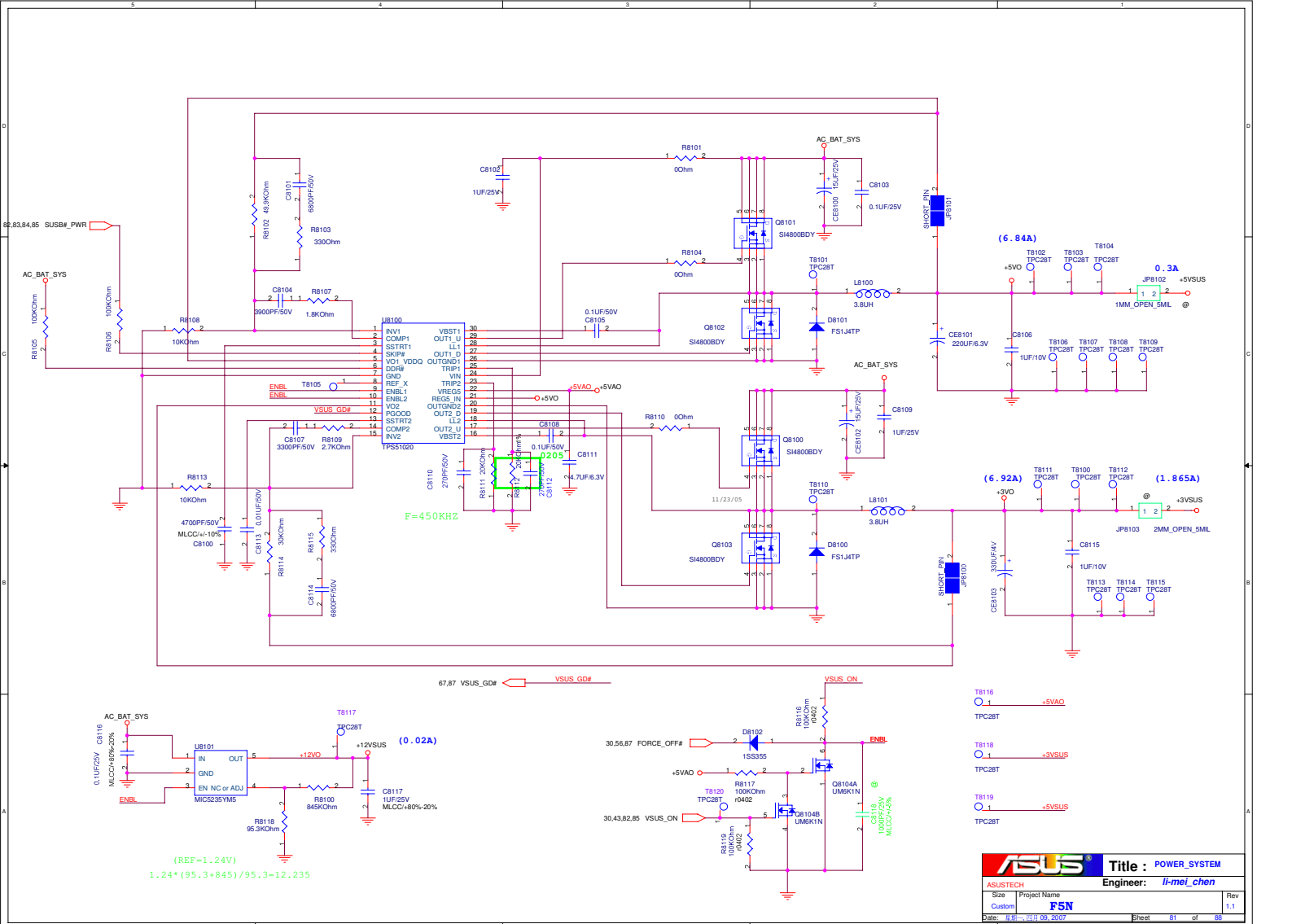


R8021 close to L8000

VREF = 2V
GND=550kHz

- T8005 1 TPC28T CPU_VD0
- T8006 1 TPC28T CPU_VD1
- T8007 1 TPC28T CPU_VD2
- T8008 1 TPC28T CPU_VD3
- T8018 1 TPC28T CPU_VD4
- T8019 1 TPC28T CPU_VD5
- T8030 1 TPC28T CPU_PWR_GD
- T8031 1 TPC28T CPU_VDD_FB
- T8032 1 TPC28T CPU_VDD_FB#

| | | | |
|------------------|--------------|----------------------------|---------|
| ASUS | | Title : POWER_VCORE | |
| ASUSTek | Project Name | Engineer: li-mei_chen | |
| Size | Custom | F5N | Rev 1.1 |
| Date: 11/09/2007 | Sheet 80 | of 88 | |



67.87 V_SUS_GD#

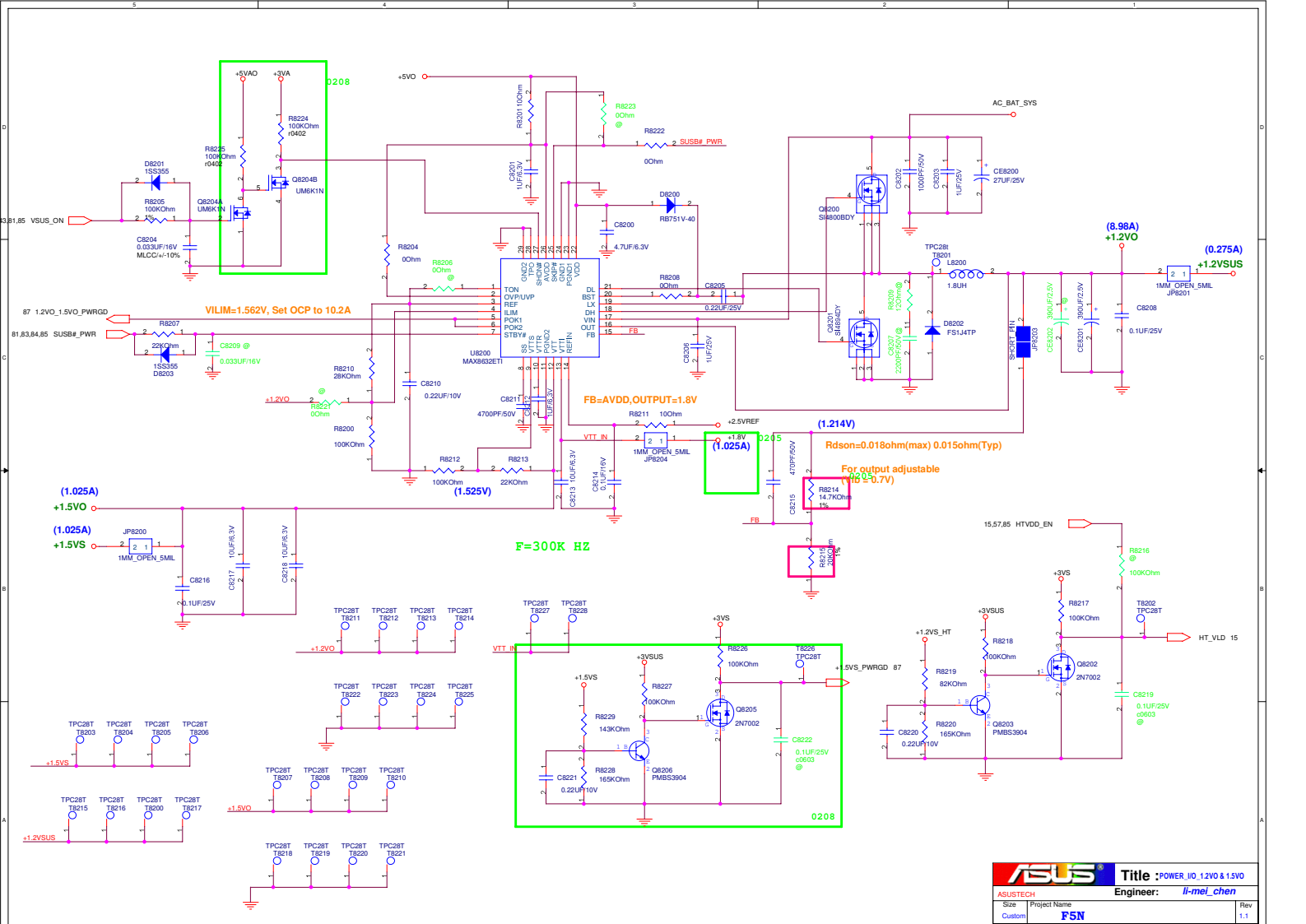
V_SUS_ON

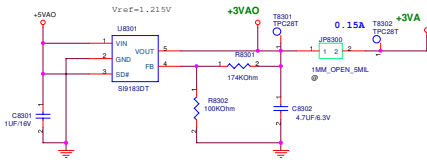
- T8116 1 +5VAO
- TPC28T
- T8118 1 +3VSUS
- TPC28T
- T8119 1 +5VSUS
- TPC28T

(REF=1.24V)
 $1.24 * (95.3 + 845) / 95.3 = 12.235$

(0.02A)

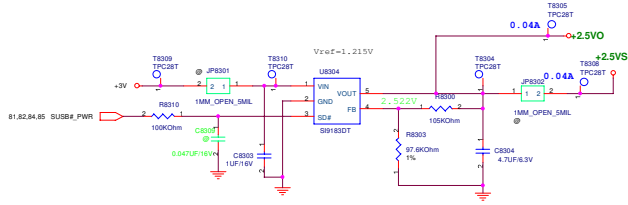
| Size | Project Name | Rev |
|--------|--------------|-----------------|
| Custom | F5N | 1.1 |
| Date: | 11/09/2007 | Sheet: 81 of 88 |



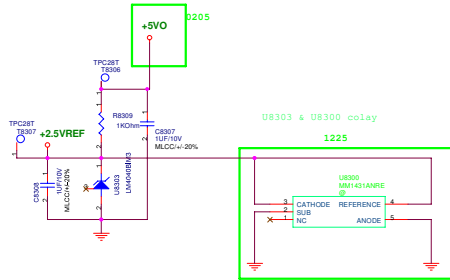


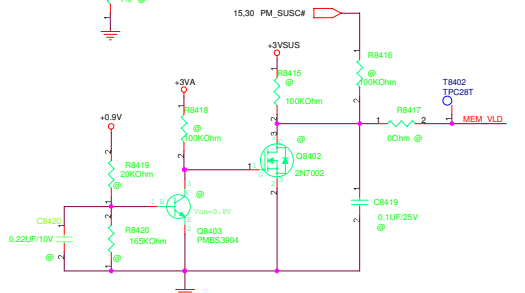
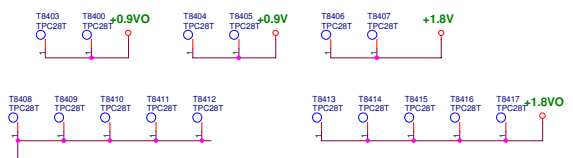
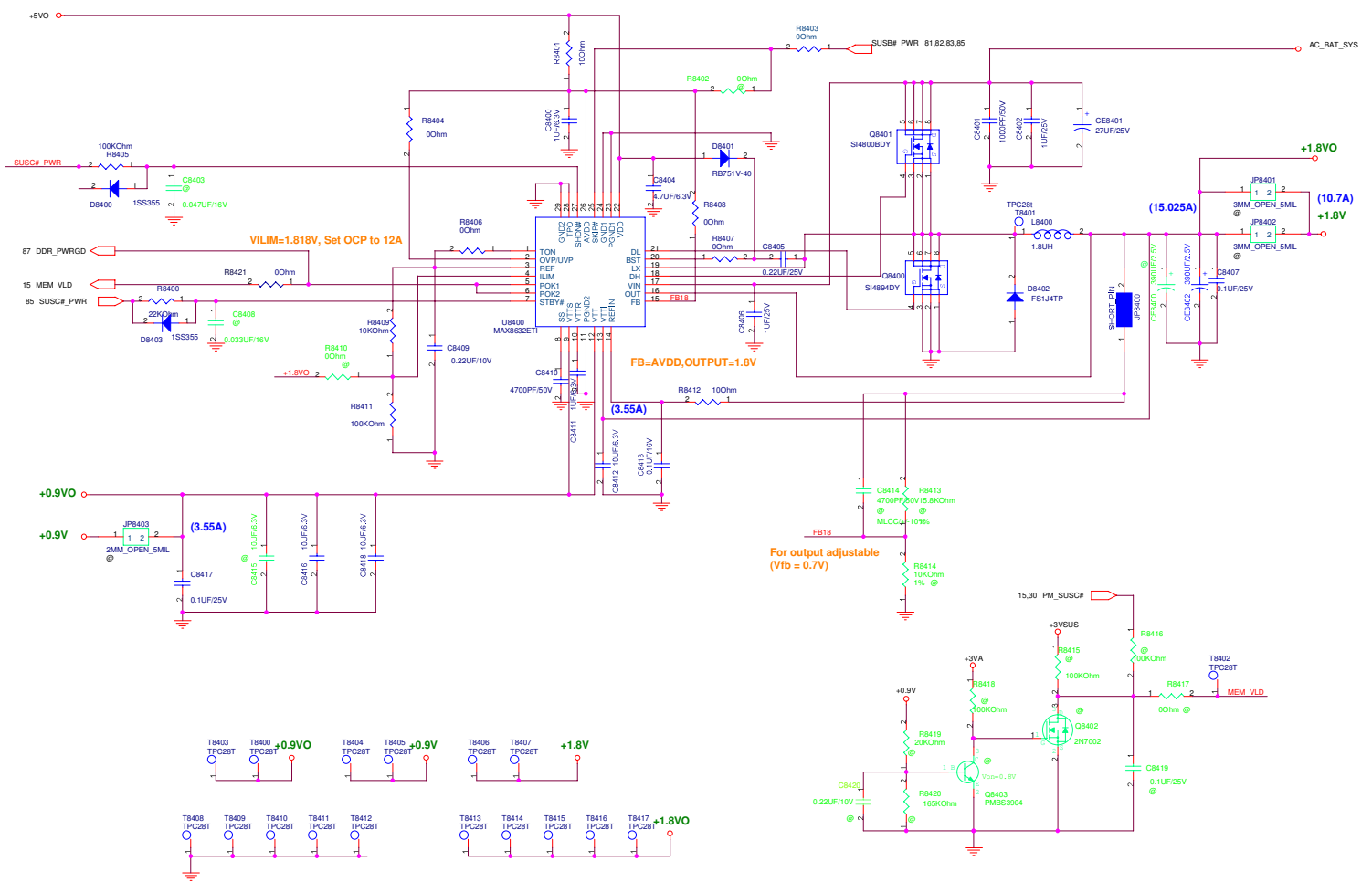
+3VA

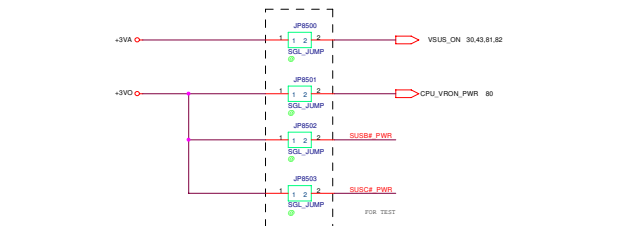
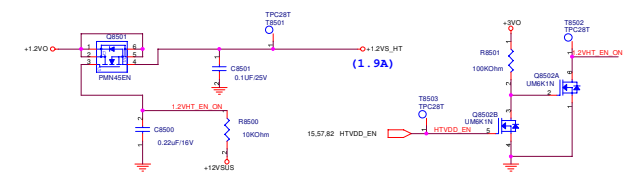
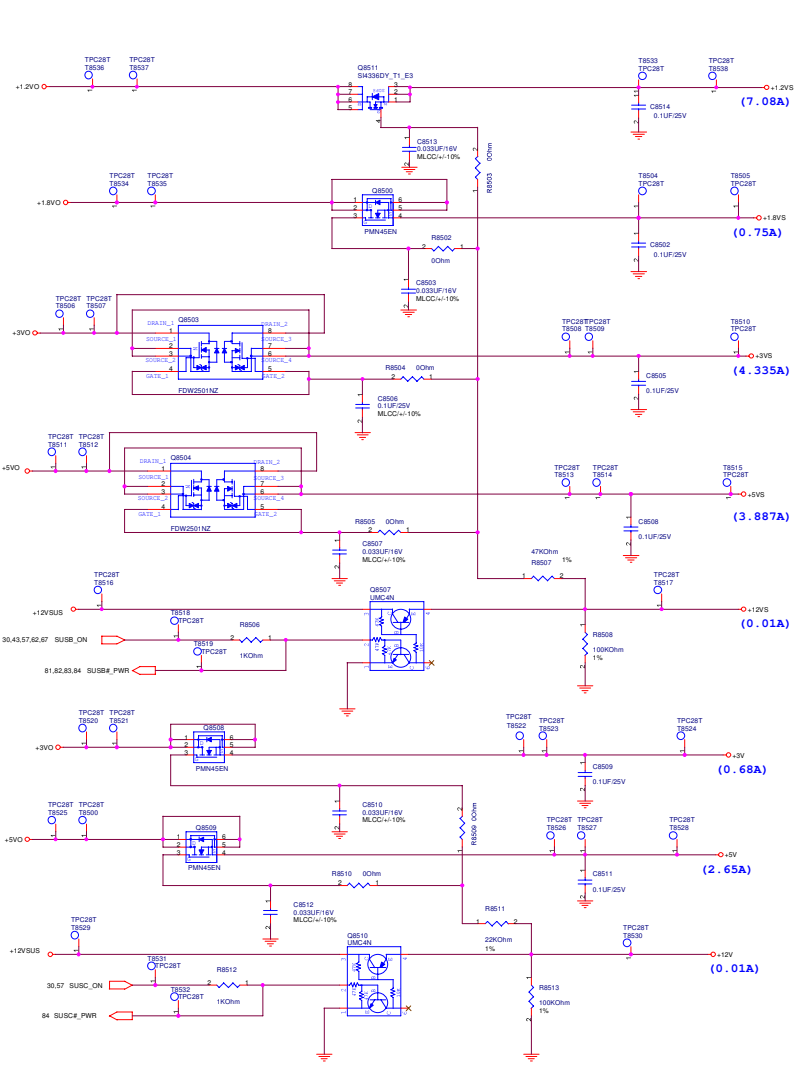
+2.5VS



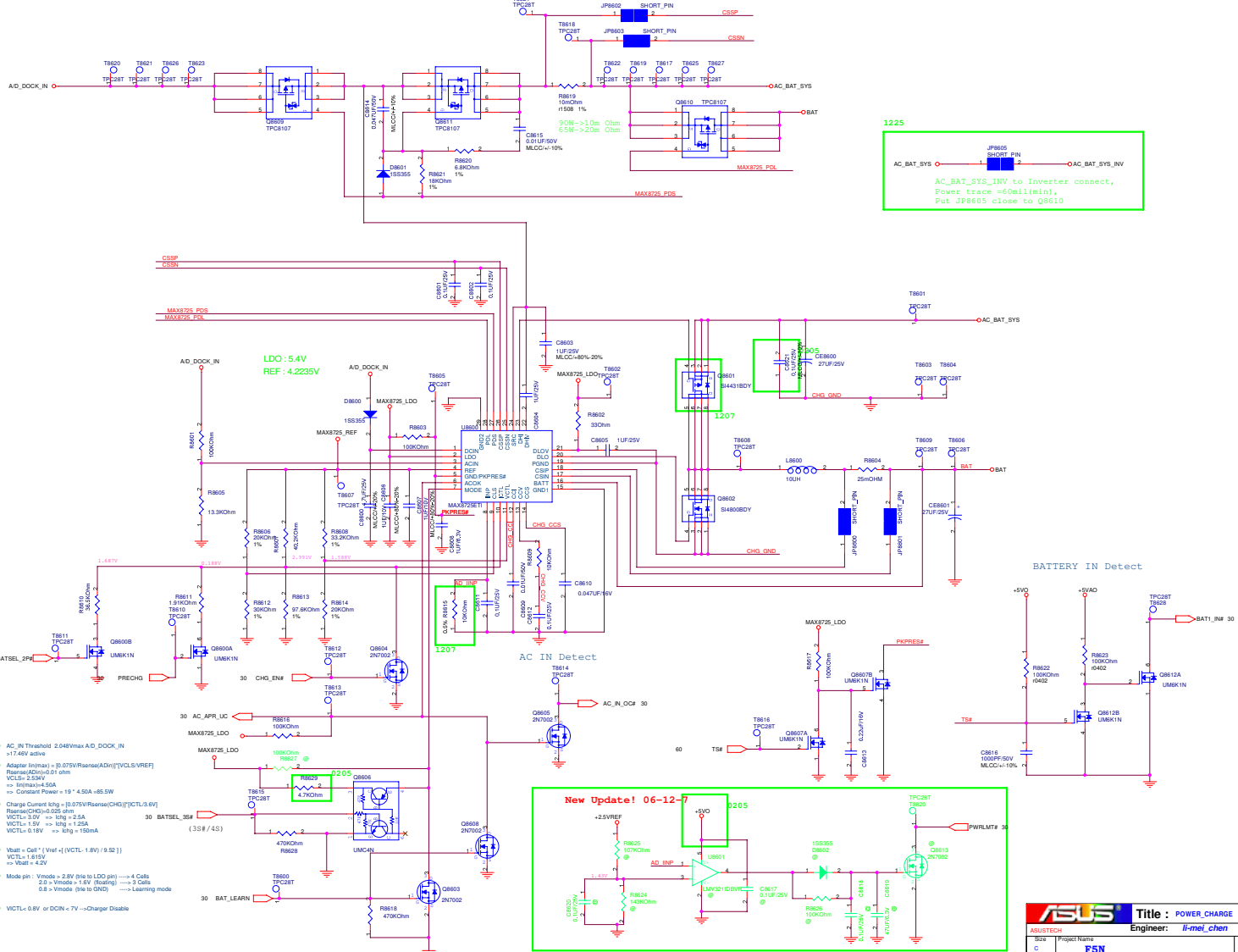
+2.5VREF







| | |
|------------|--|
| +3VA | 15.30, 46.56, 62.67, 82.83, 84 |
| +3V0 | 56.81, 82.83, 84, 86 |
| AC_BAT_SYS | 5.80, 81, 82, 84, 86 |
| AC_BAT_SYS | 5.80, 81, 82, 84, 86 |
| +VCORE | 5.80, 81, 82, 84, 86 |
| +5VAD | 81, 82, 83, 86 |
| +3V0 | 81 |
| +3V | 30.34, 43.46, 53.57, 61.62, 83 |
| +12V0US | 81 |
| +12V0_HT | 3.5, 10, 15, 57, 82 |
| +25V0 | 83 |
| +12V0USUS | 12, 16, 82 |
| +12V0S | 11, 14, 16, 57 |
| +3V5 | 3.7, 8, 10, 11, 12, 13, 14, 15, 16, 30, 36, 37, 43, 44, 45, 46, 50, 51, 53, 56, 57, 82, 87, 80, 82, 87 |
| +3V5S | 3.12, 14, 15, 16, 30, 33, 34, 43, 53, 56, 57, 87, 81, 82, 84, 87 |
| +0.9V | 5, 57, 84 |
| +12V | 37, 52, 57 |
| +12V5 | 37, 45, 46, 57 |
| +5V | 3, 7, 40, 43, 46, 52, 57 |
| +5V5 | 15, 30, 36, 37, 45, 50, 51, 56, 57, 80 |
| +2.5V5 | 3, 57, 83 |
| +1.8V0 | 84 |
| +1.8V | 3.5, 7, 8, 9, 10, 15, 57, 82, 84 |
| +1.8V5 | 12, 57 |
| BAT | 60, 86 |
| +2.5VREF | 82, 83, 86 |

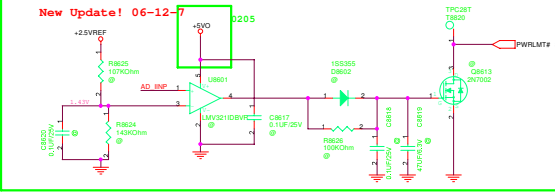


1225

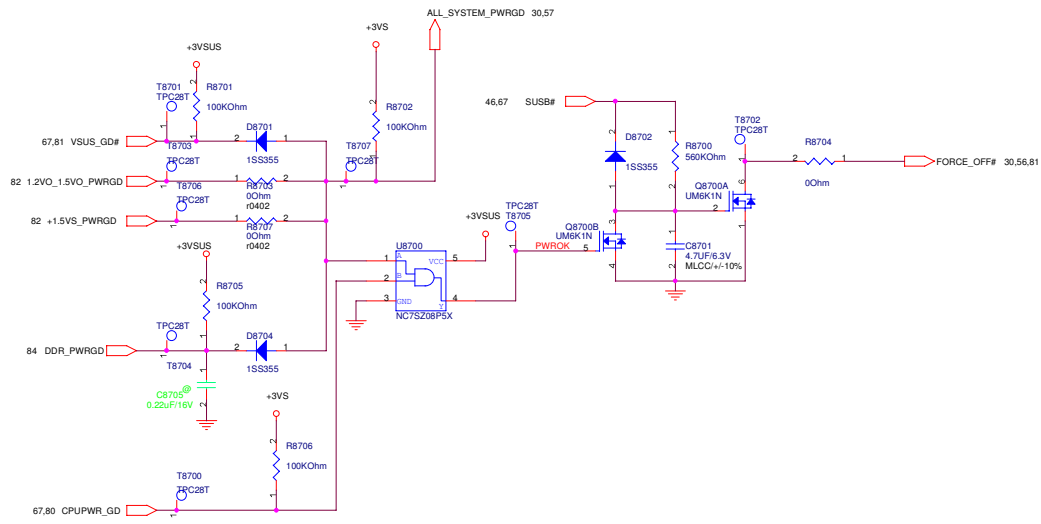
AC_BAT_SYS_INV

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8605 close to Q8610

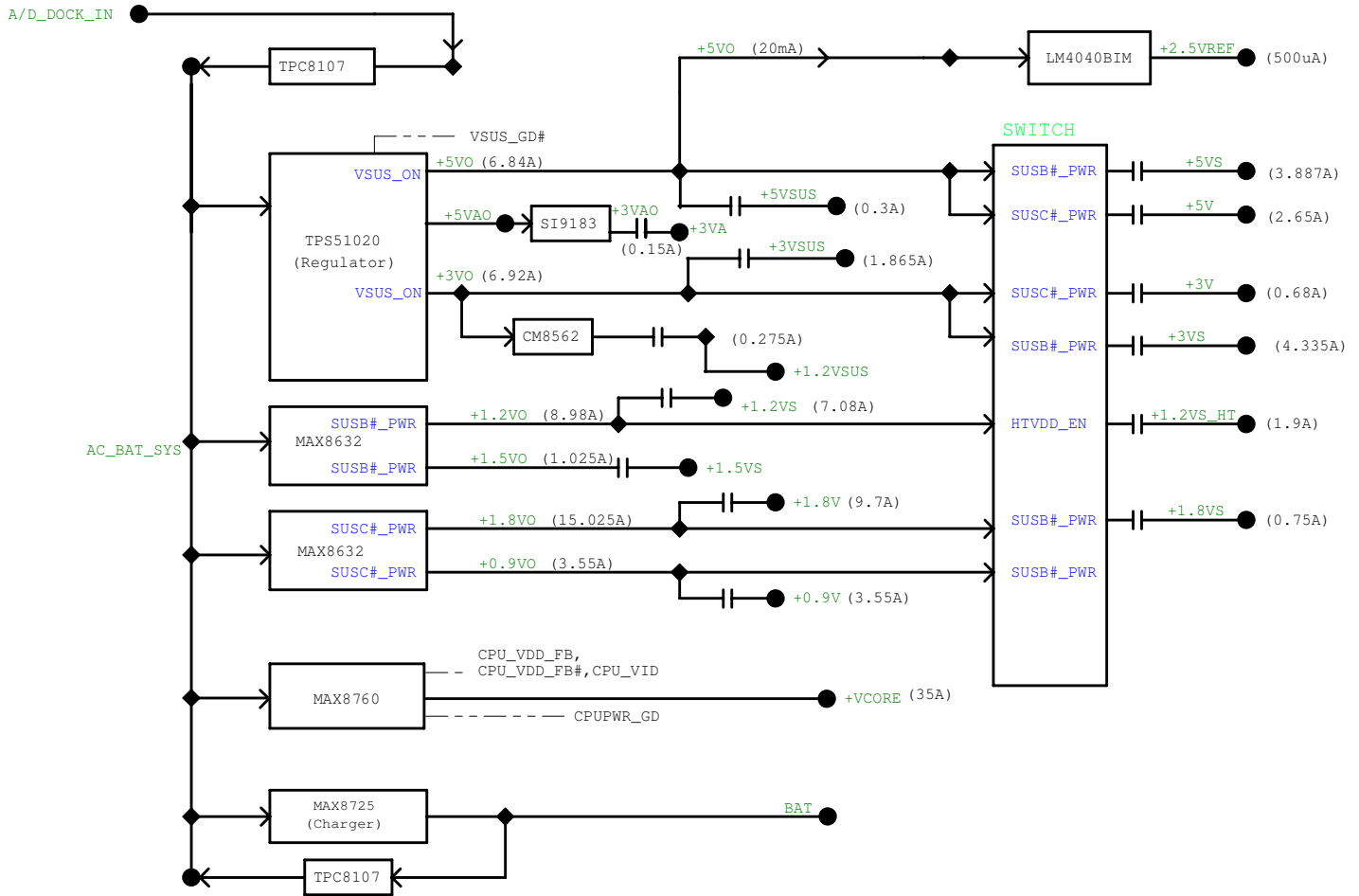
LDO : 5.4V
REF : 4.2235V



- AC_IN Threshold 2.048Vmax A/D_DOCK_IN
=> 1749V active
- Adapter In(max) = [0.075V/Rsense/A(D)]*(VCL5/VREF)
Rsense=40mΩ/0.01 ohm
VCL5 = 1.53V
=> In(max)=4.50A
- Charge Current kIq = [0.075V/Rsense/CHG]/(VCL3.8V)
Rsense=CHG=0.025 ohm
VCL3 = 3.8V => Iq = 2.5A
VCL1 = 1.5V => Iq = 1.25A
VCL1 = 0.18V => Iq = 150mA
- Vbat = Cell * [Vref / (VCL1 - Iq)] / (9.52)]
VCL1 = 1.515V
=> Vbat = 4.5V
- Mode pin : Vmode > 2.8V (High to LDO pin) => 4 Cells
2.8 > Vmode > 1.6V (Floating) => 3 Cells
0.5 > Vmode (pin to GND) => Learning mode
- VCL1 = 0.6V or DCIN < 7V --> Charger Disable



| | | | |
|------------------|--------------|------------------------------|---------|
| ASUS | | Title : POWER_PROTECT | |
| ASUSTECH | Project Name | Engineer: <i>li-mei_chen</i> | |
| Size | Custom | F5N | Rev 1.1 |
| Date: 2007-09-09 | Sheet 97 | of 88 | |



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