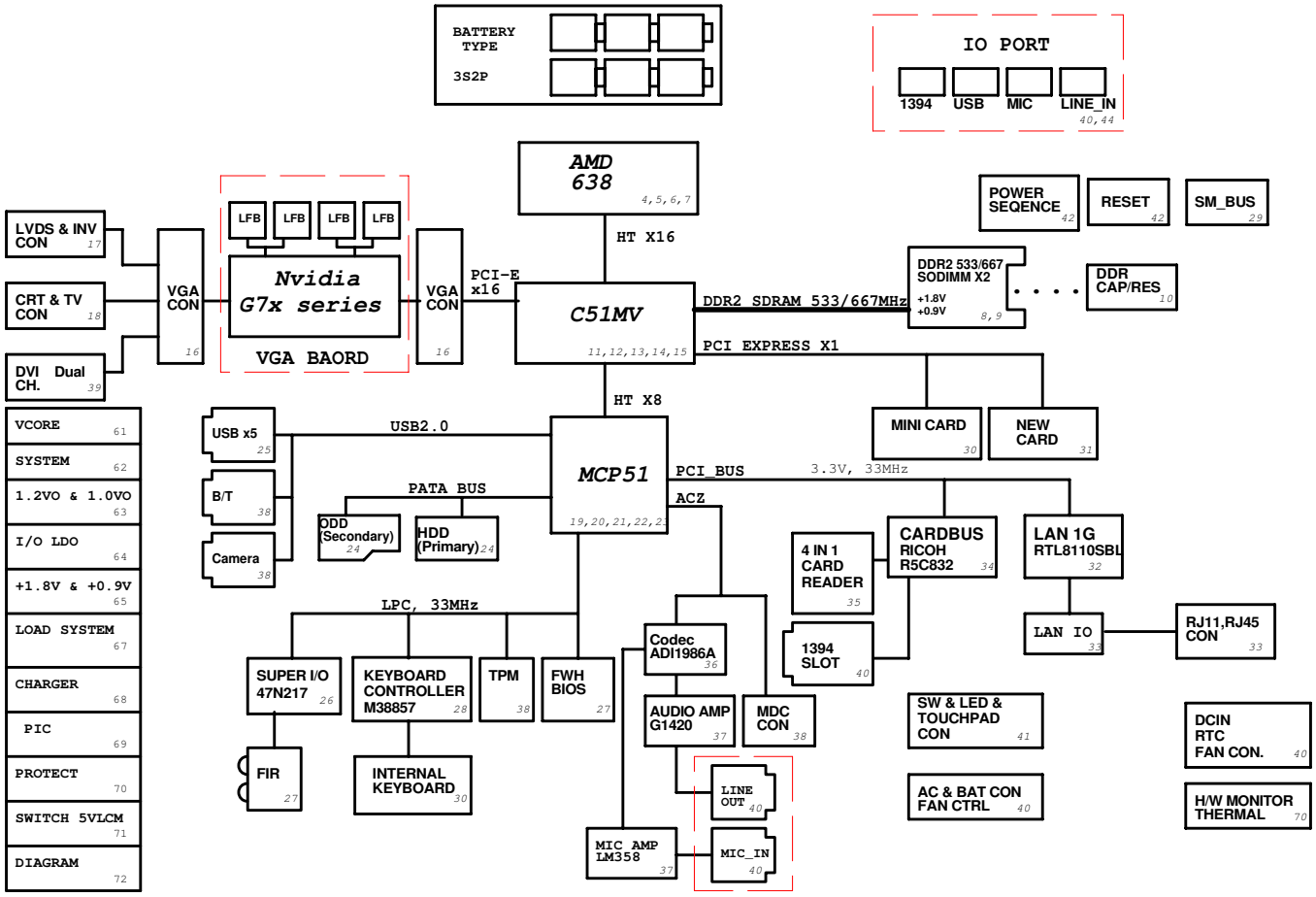
A8T/M SCHEMATIC R2.1

A8T/M AMD S1/C51MV BLOCK DIAGRAM



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 2 OF 55	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWRLMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_[11:16]		(CPU_VID[0:5])	+3VSUS
GPIO_17		(LFD#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDIN0_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	SIO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(RI#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

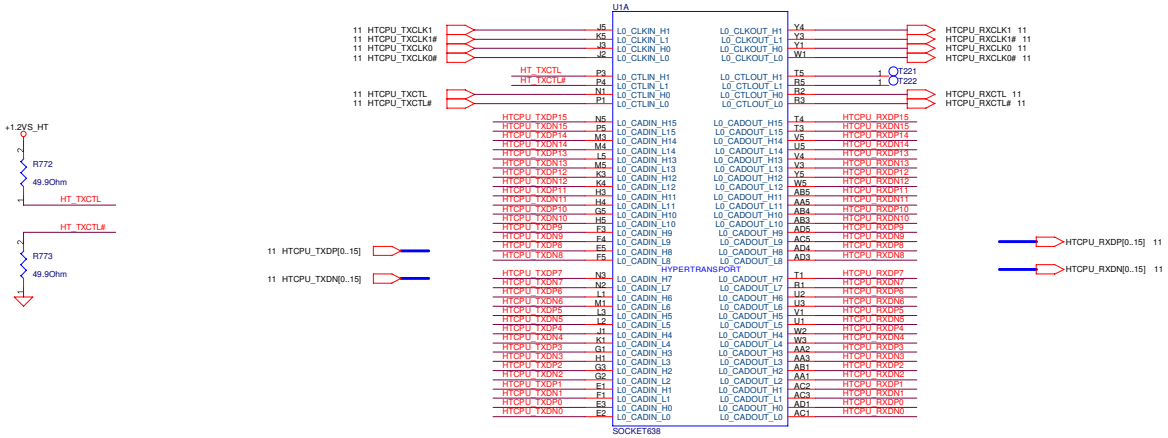
MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

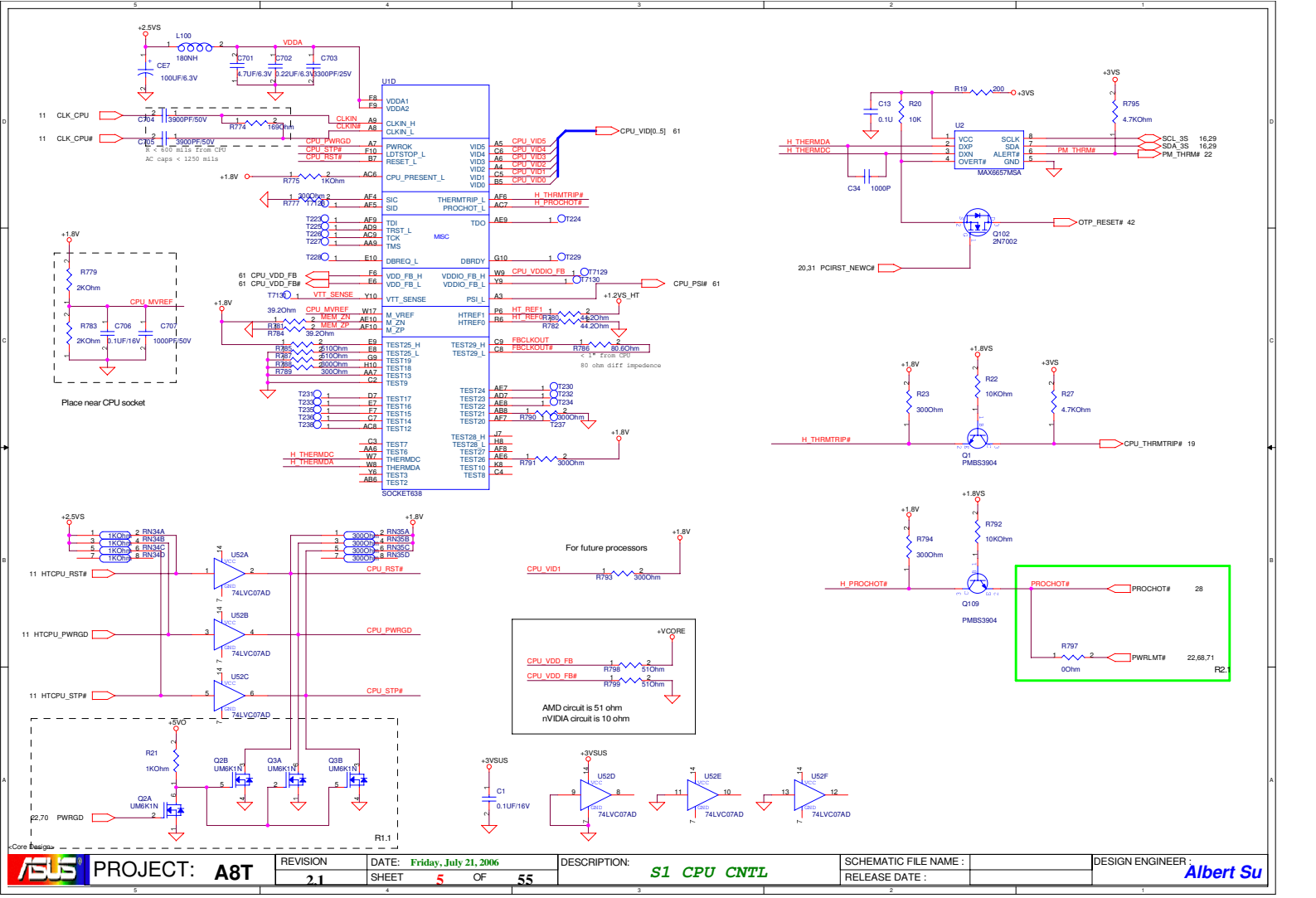
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 3 OF 55	DESCRIPTION: SCHEMATICS REF.	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

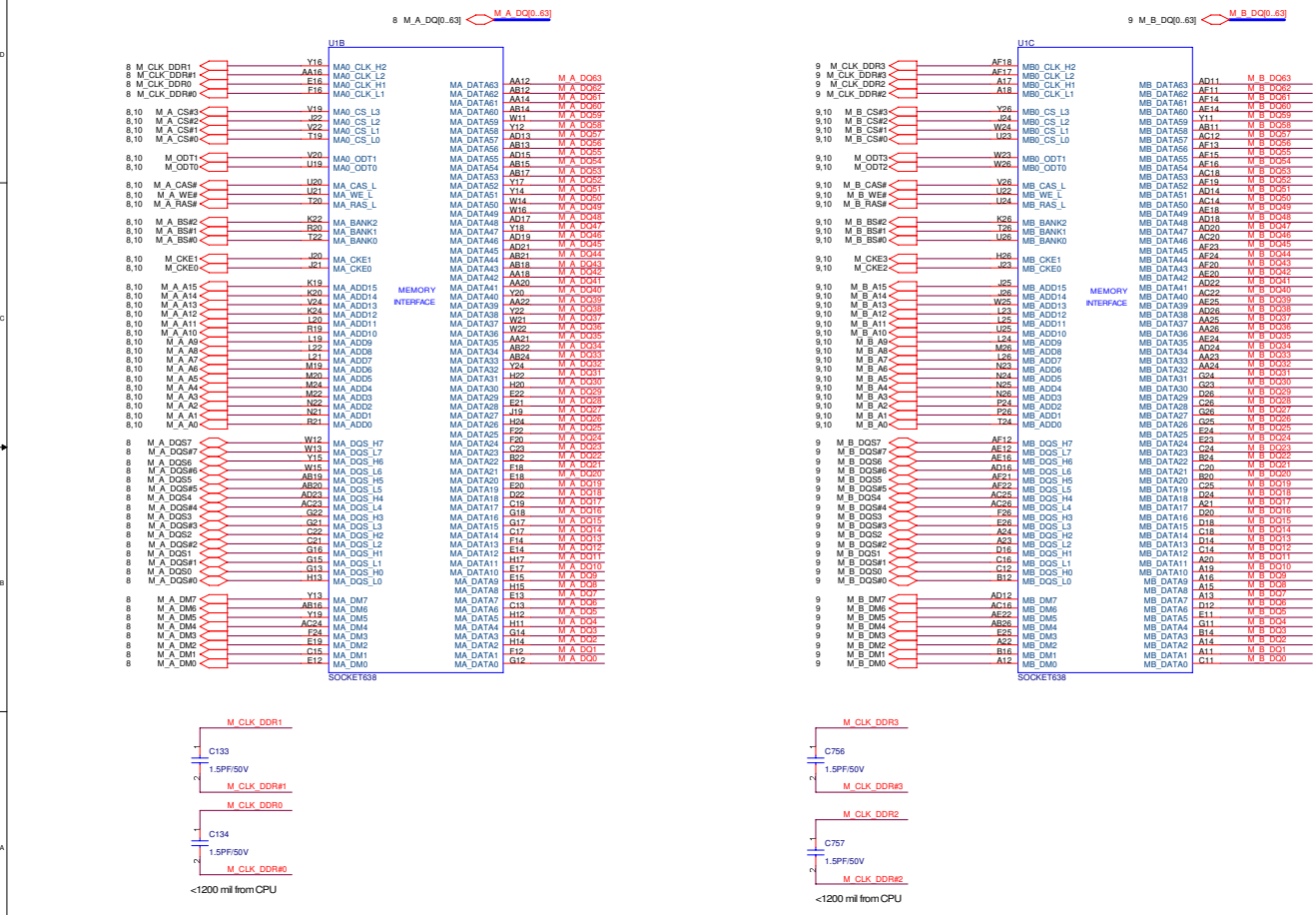


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 4 OF 55		RELEASE DATE :	

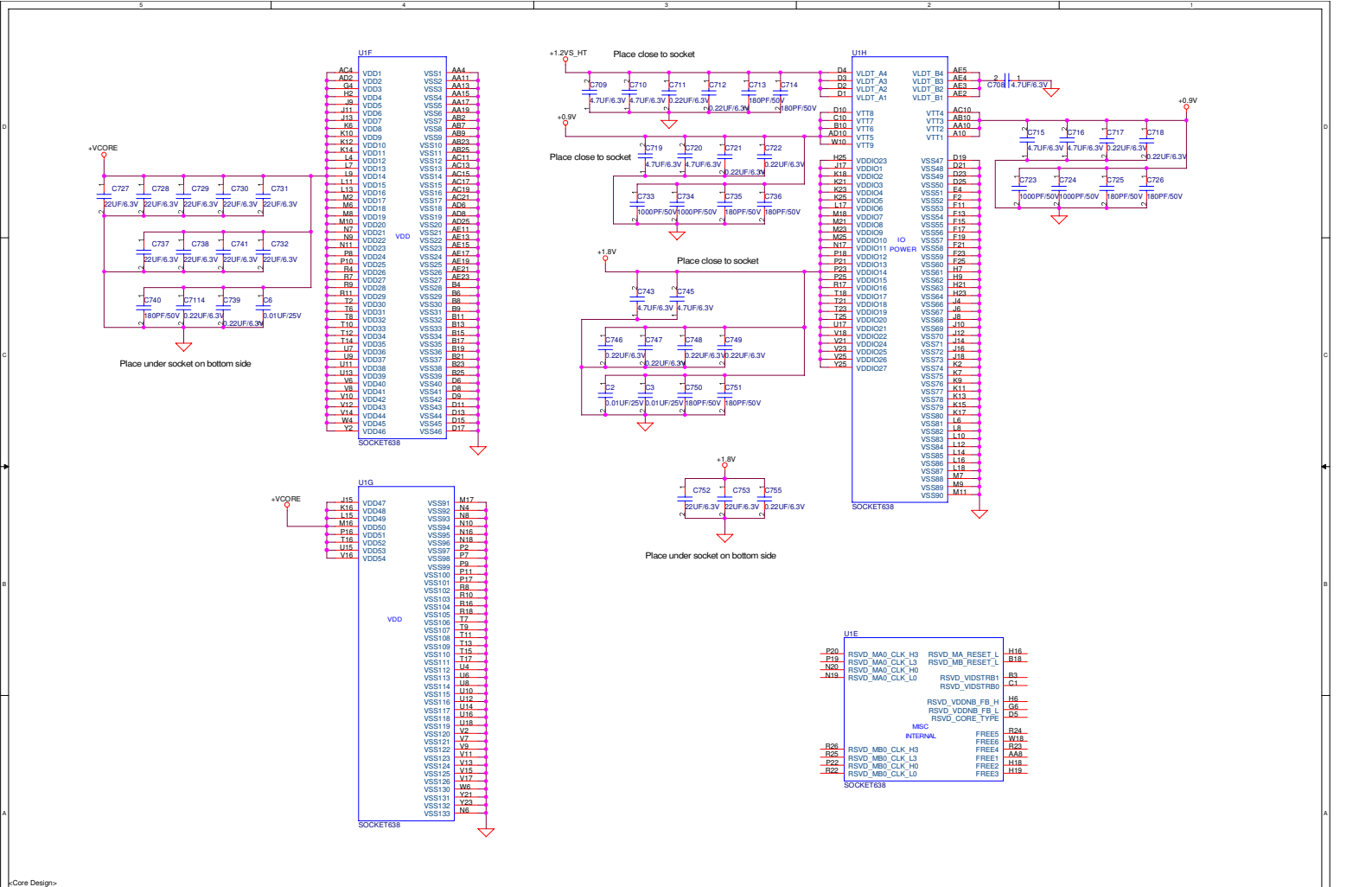


PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU CNTL	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 5 OF 55		RELEASE DATE :	



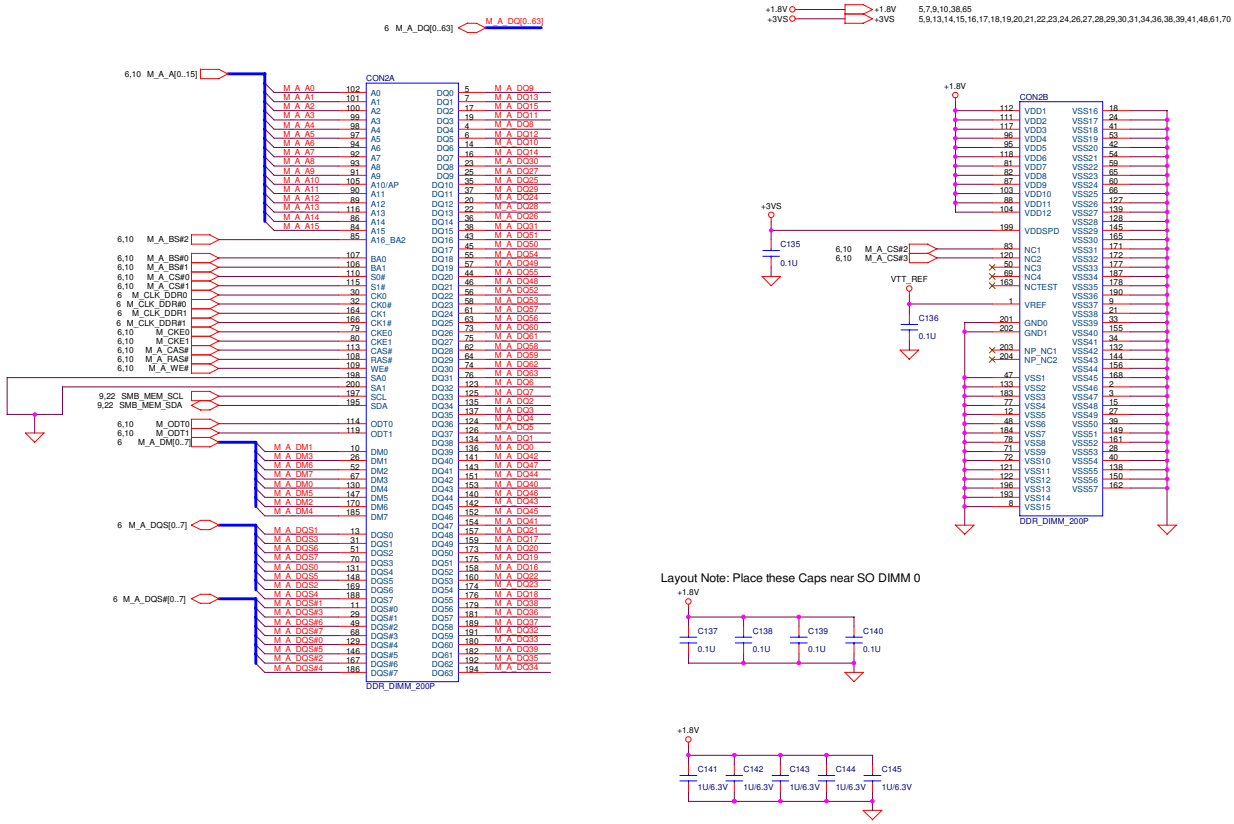
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU MEM	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 6 OF 55		RELEASE DATE :	



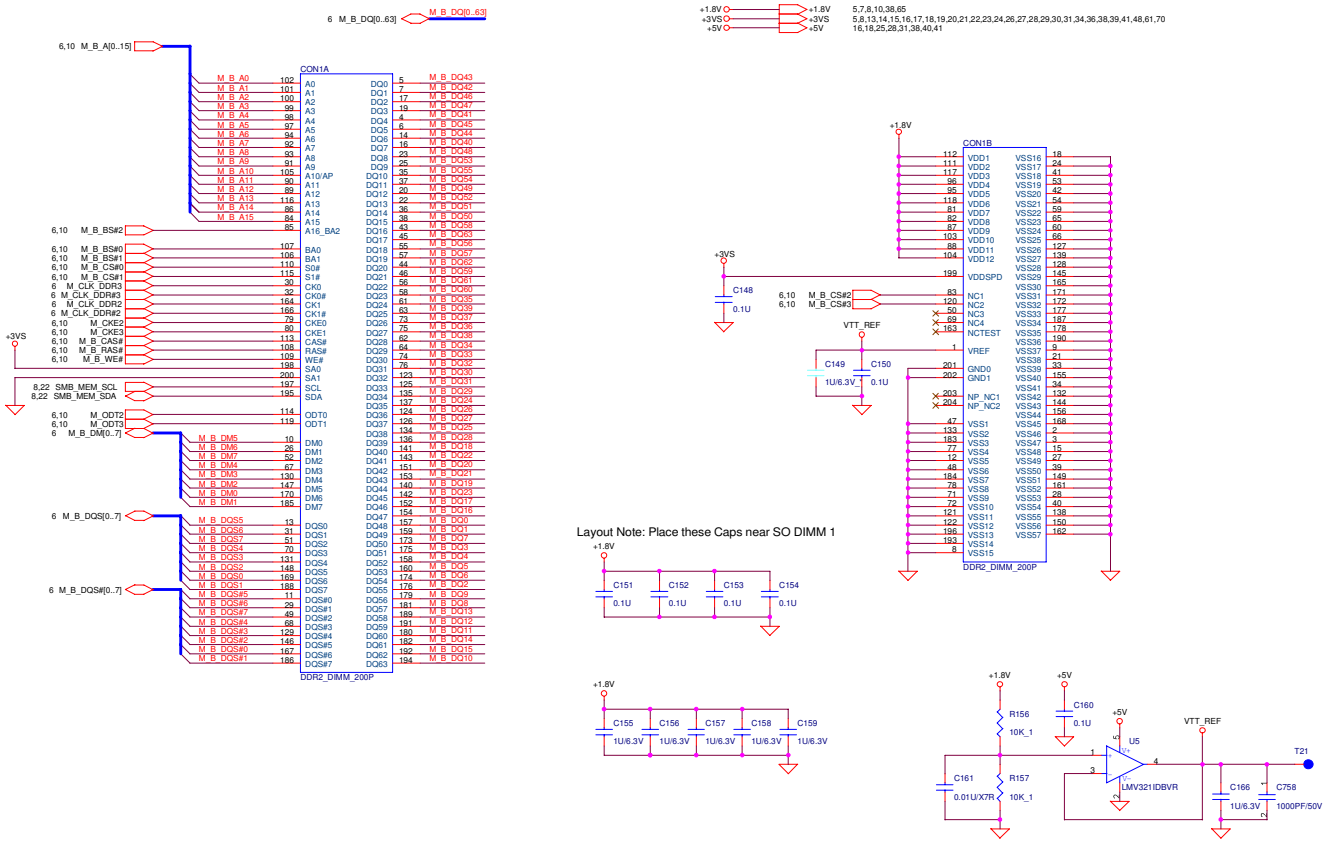
<Core Design>

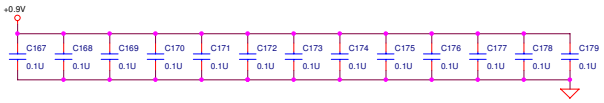
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 7 OF 55	DESCRIPTION: S1 CPU PWR/GND	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



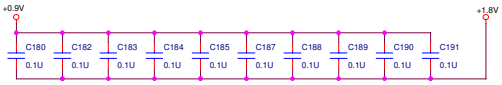
<Core Design>

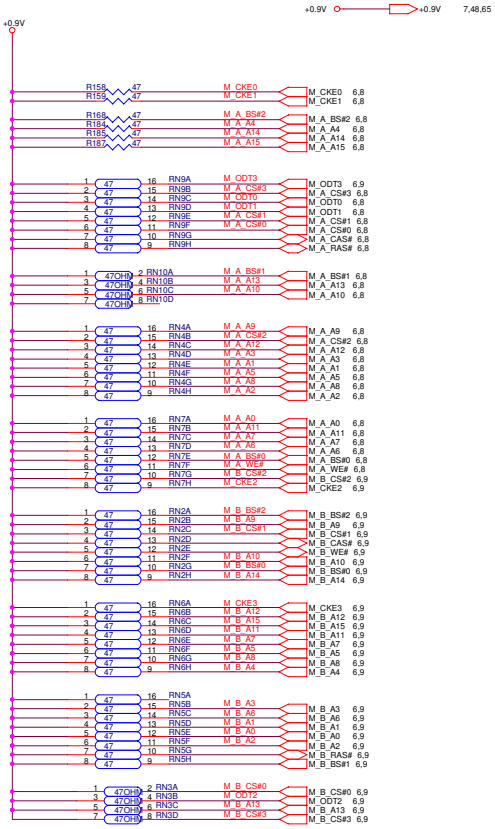
PROJECT: **A8T**	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: *DDR2 SO-DIMM0*	SCHEMATIC FILE NAME :		DESIGN ENGINEER : *Albert Su*
		SHEET 8 OF 55		RELEASE DATE :		


CON1A
DDR2_DIMM_200P
CON1B
DDR2_DIMM_200P
Layout Note: Place these Caps near SO DIMM 1
U5
LMV321IDBVR



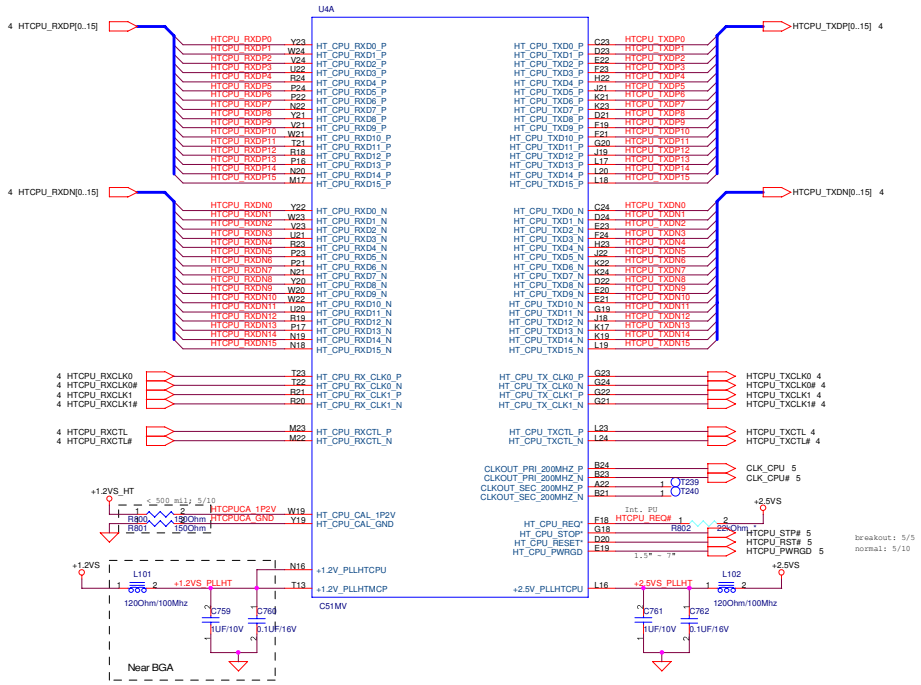
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V





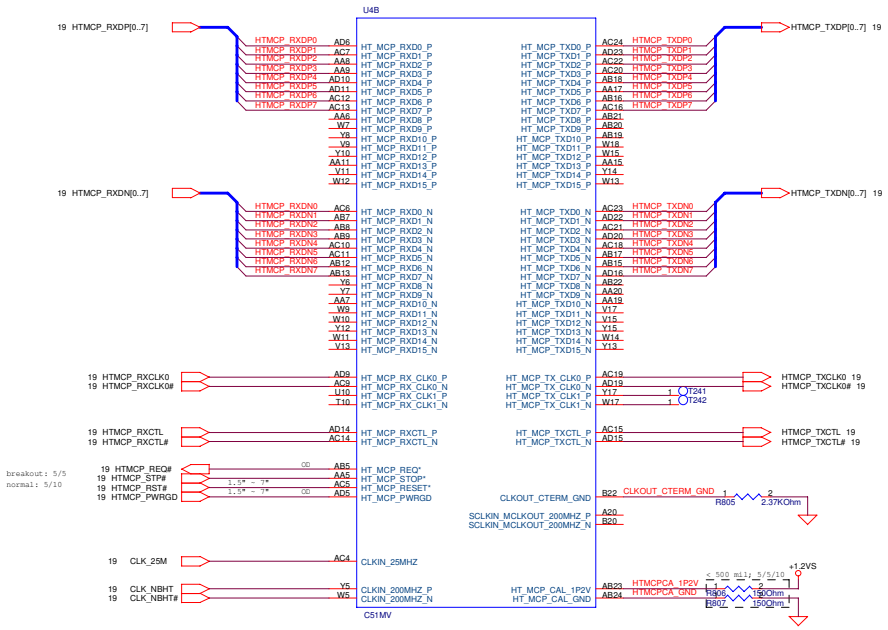
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 10 OF 55		RELEASE DATE :	



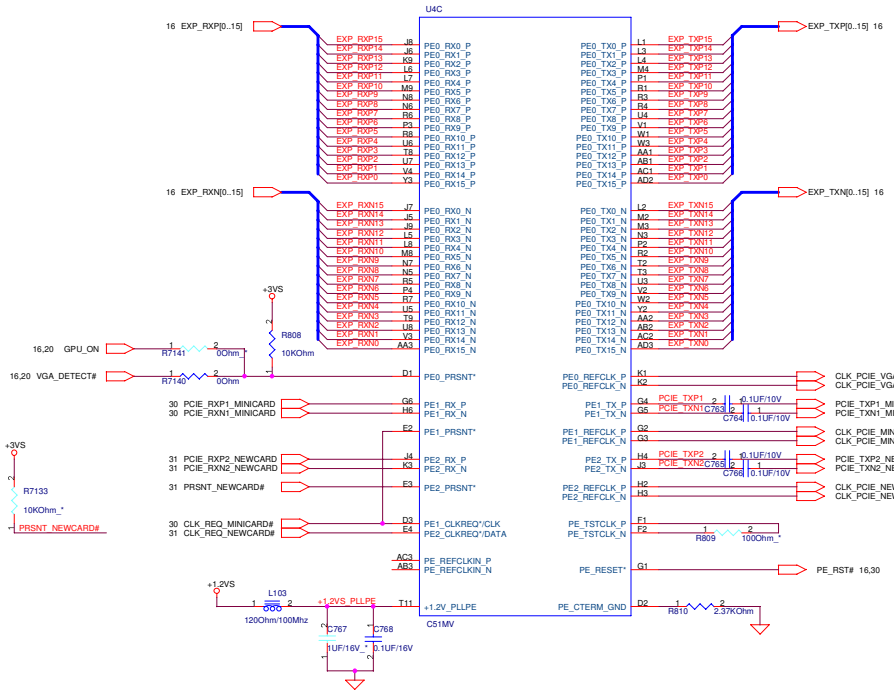
<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 11 OF 55		RELEASE DATE :	Albert Su



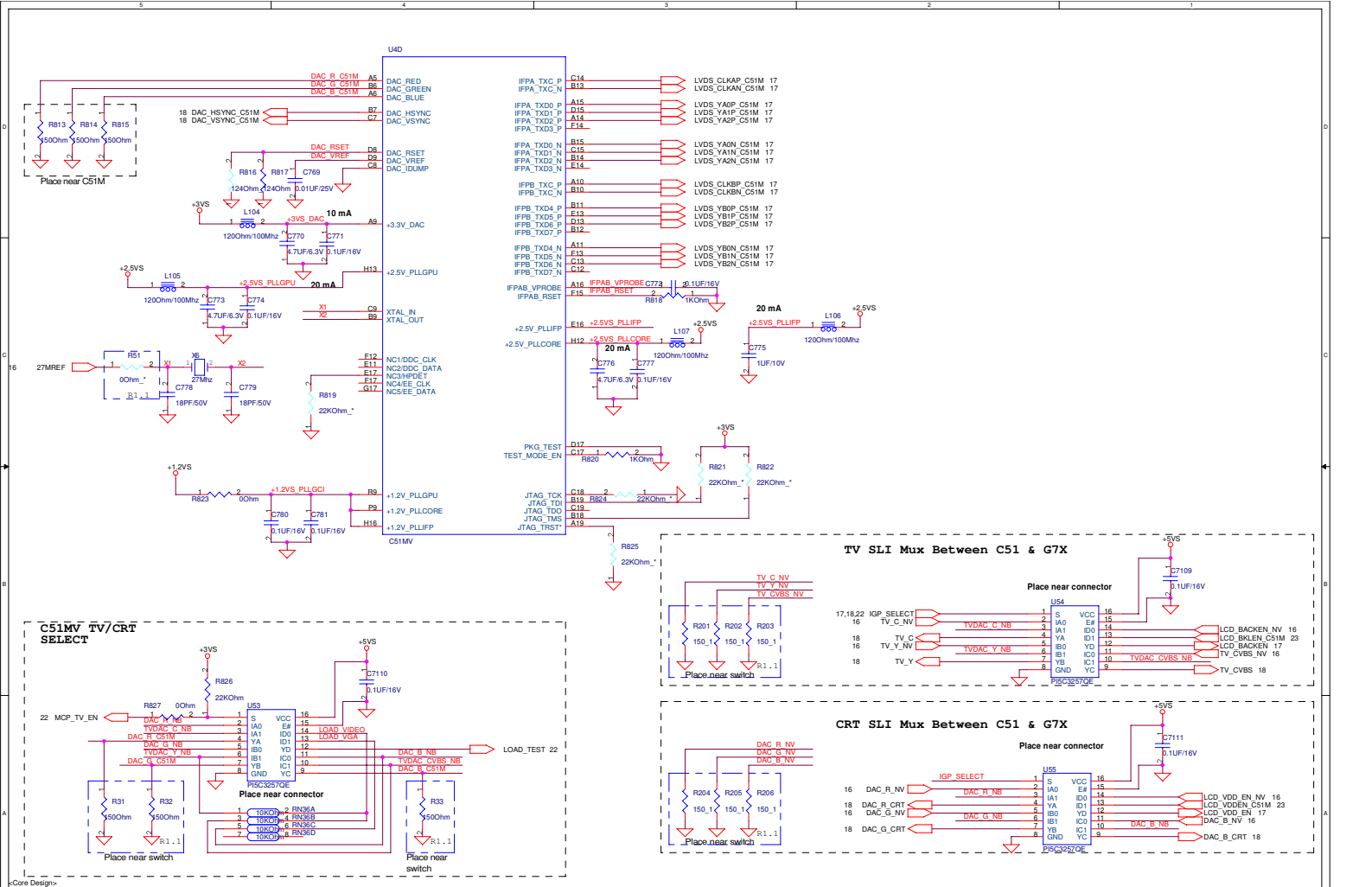
<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT TO MCP	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 12 OF 55		RELEASE DATE :	Albert Su



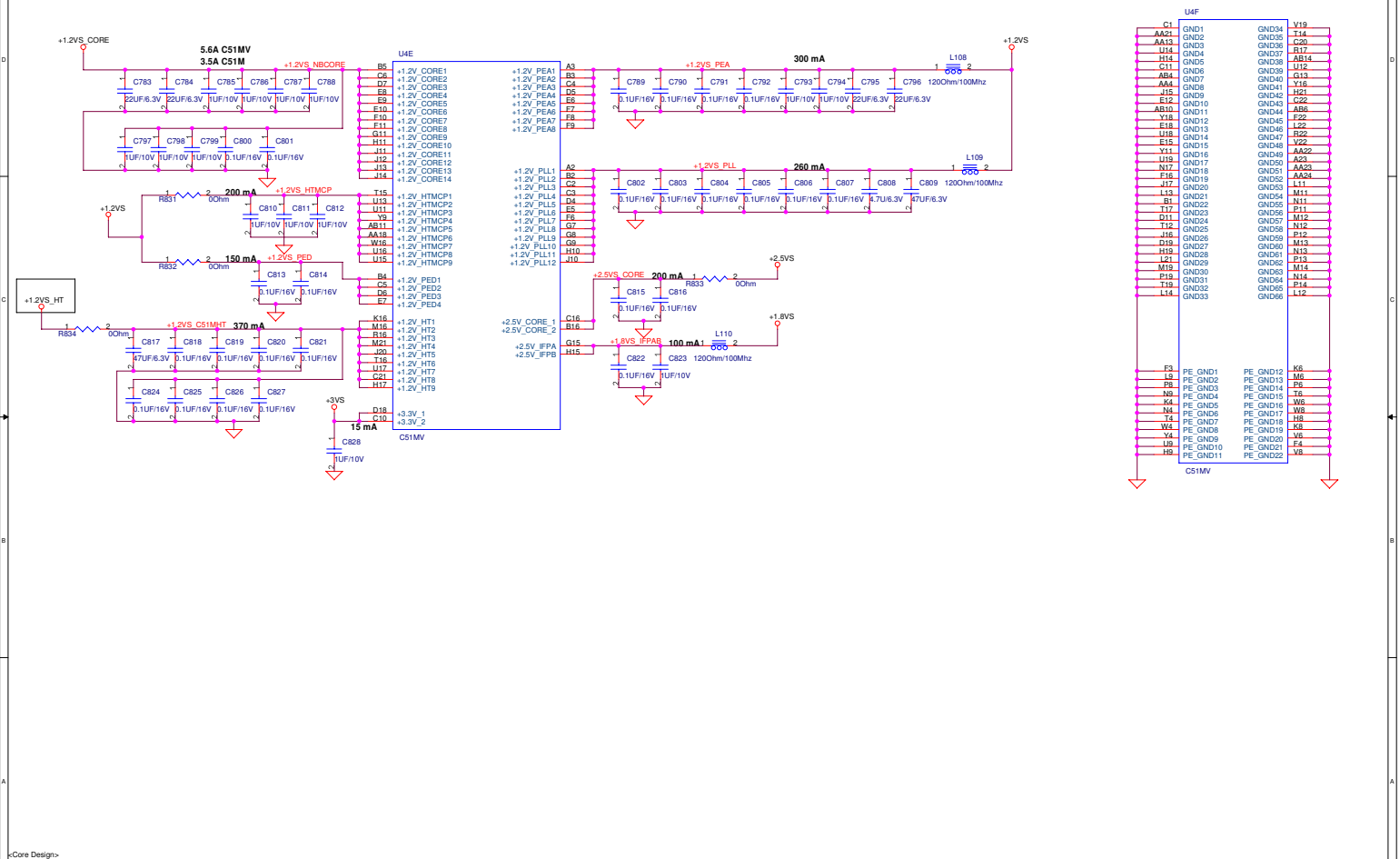
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 13 OF 55		RELEASE DATE :	



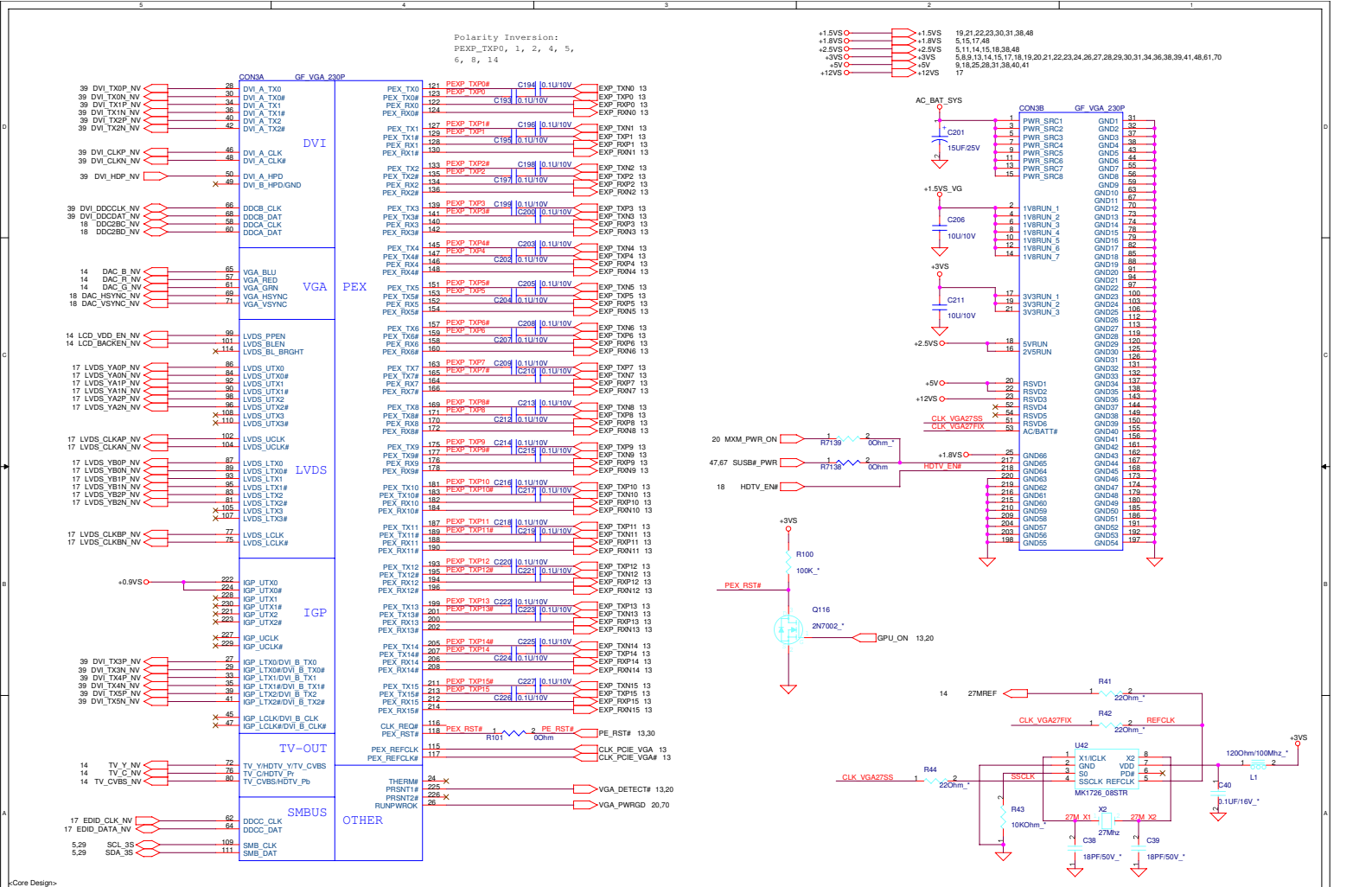
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M CRT&LVDS	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 14 OF 55		RELEASE DATE :		



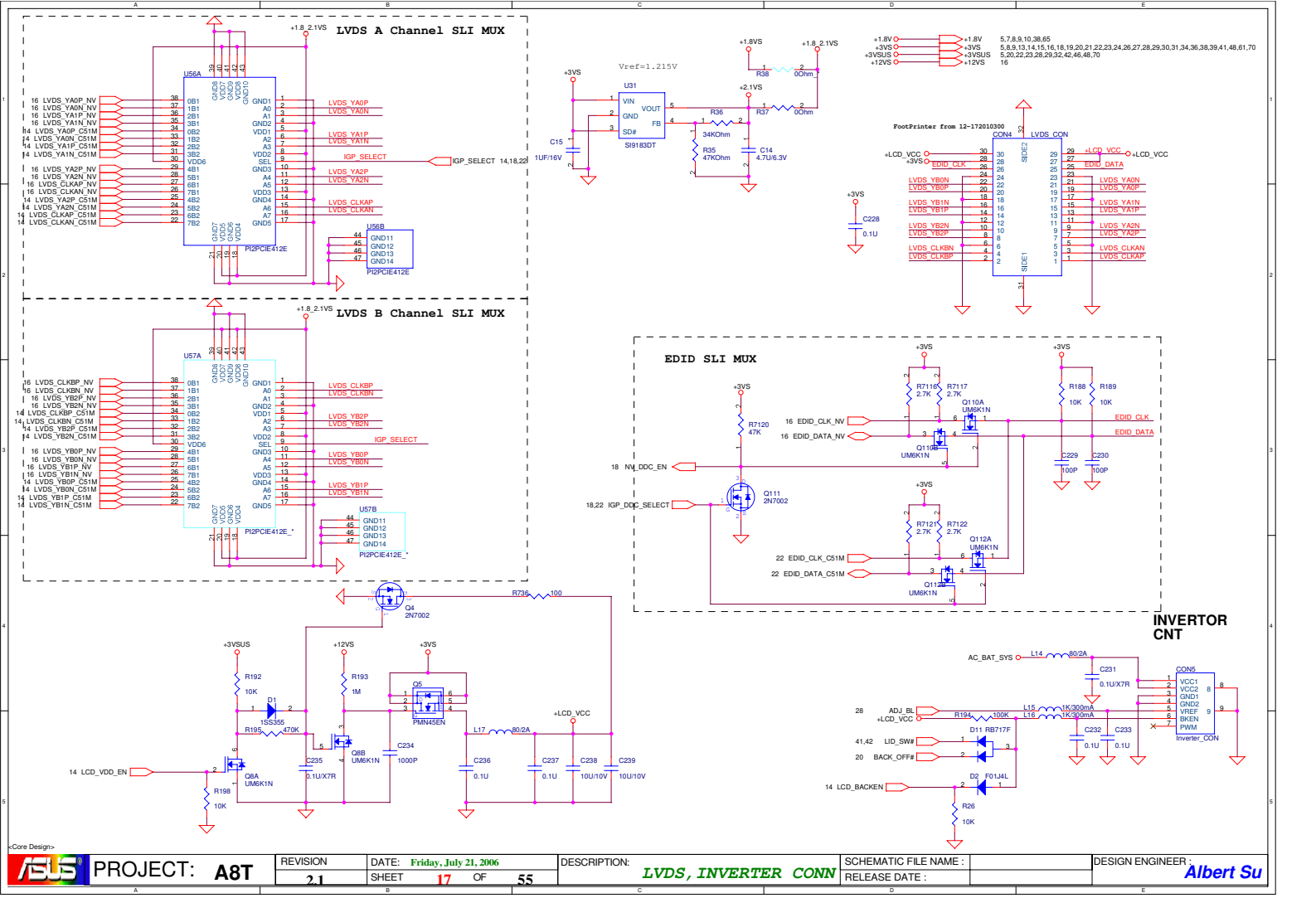
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 15 OF 55		RELEASE DATE :	



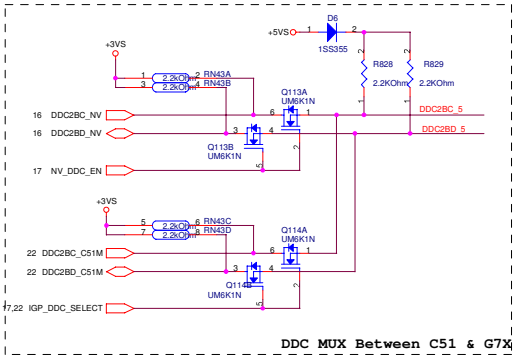
<Core Design>

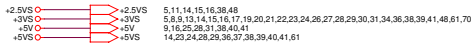
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 16 OF 55	DESCRIPTION: VGA CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

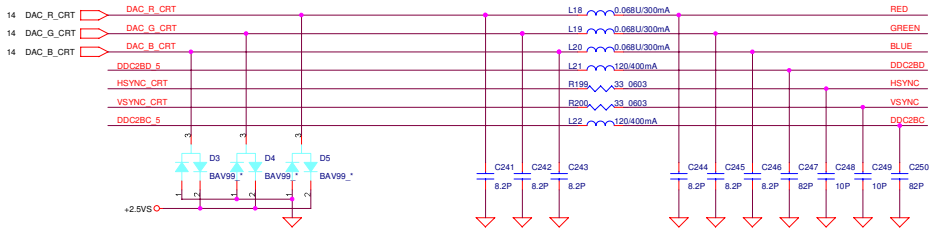


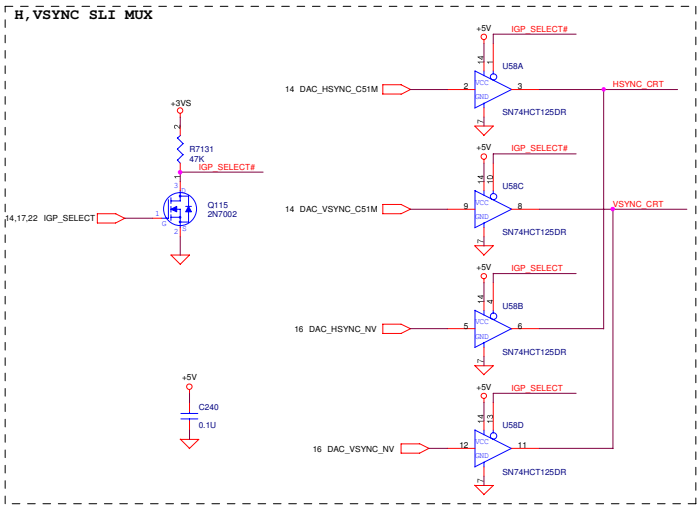
<Core Design>

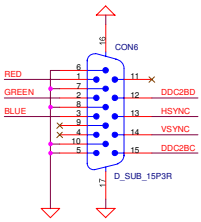
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: LVDS, INVERTOR CONN	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 17 OF 55		RELEASE DATE :		

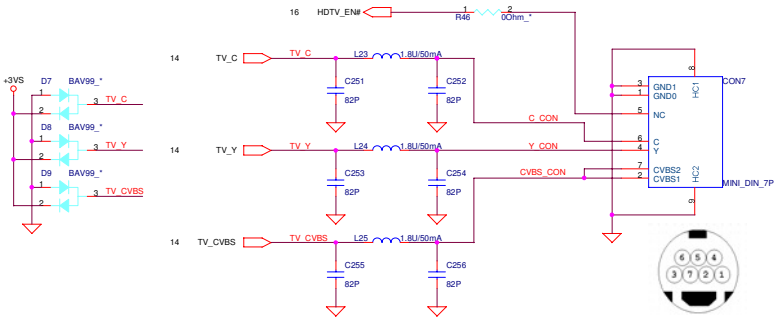






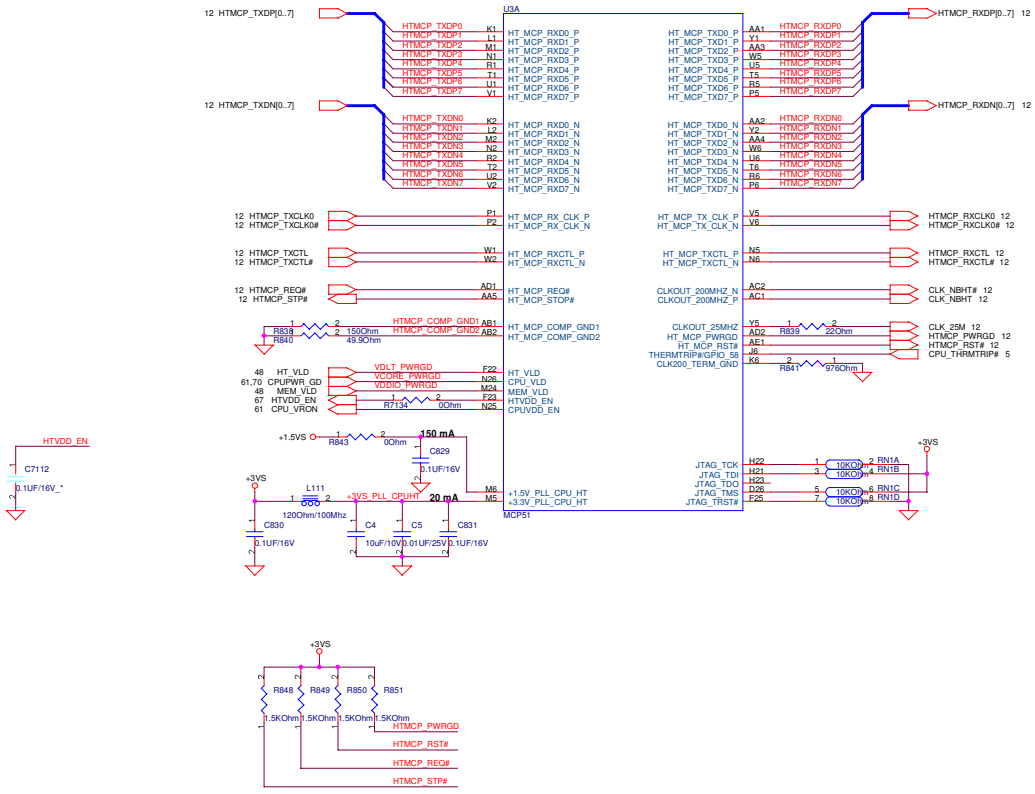






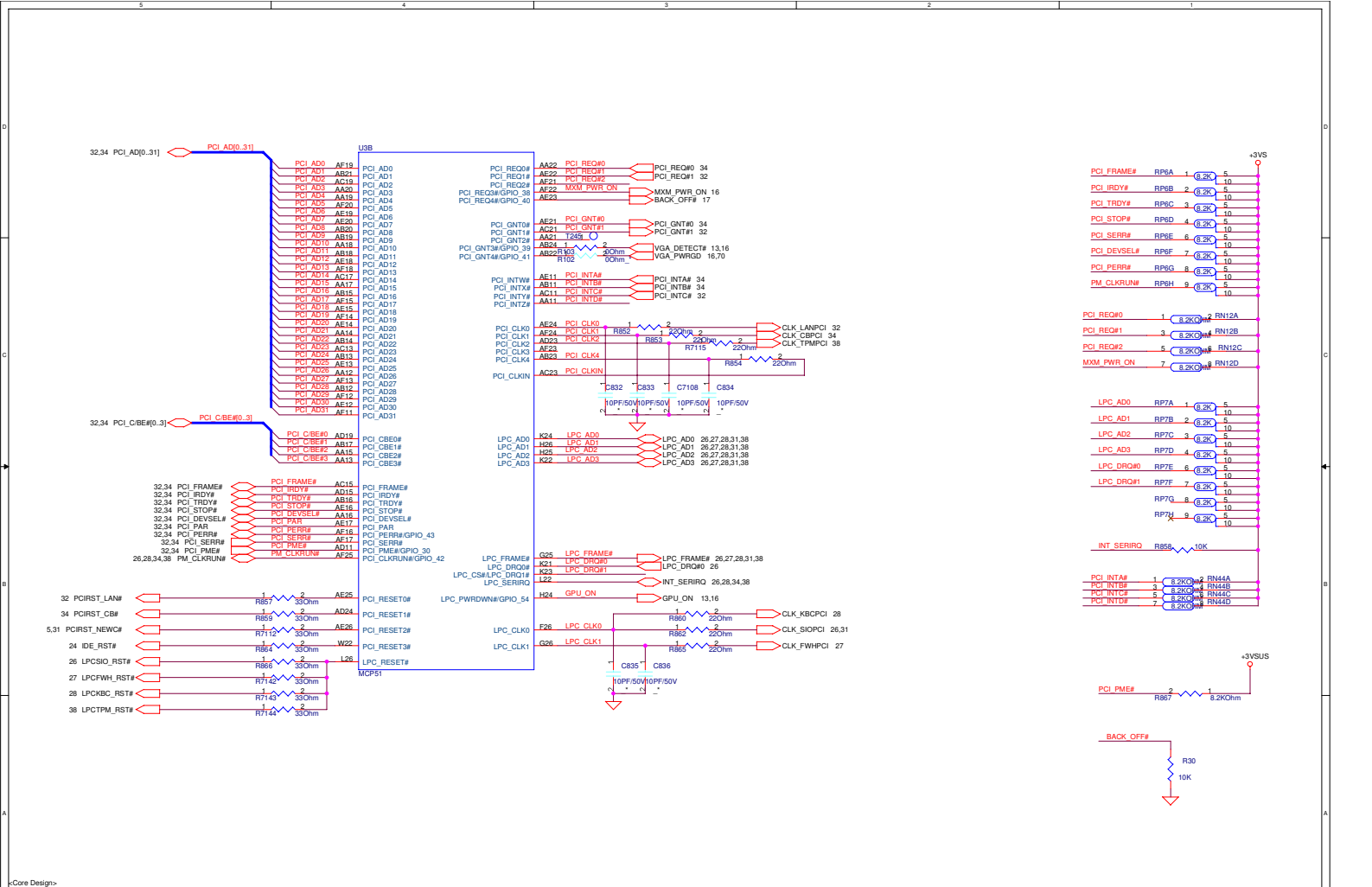
<Core Design>

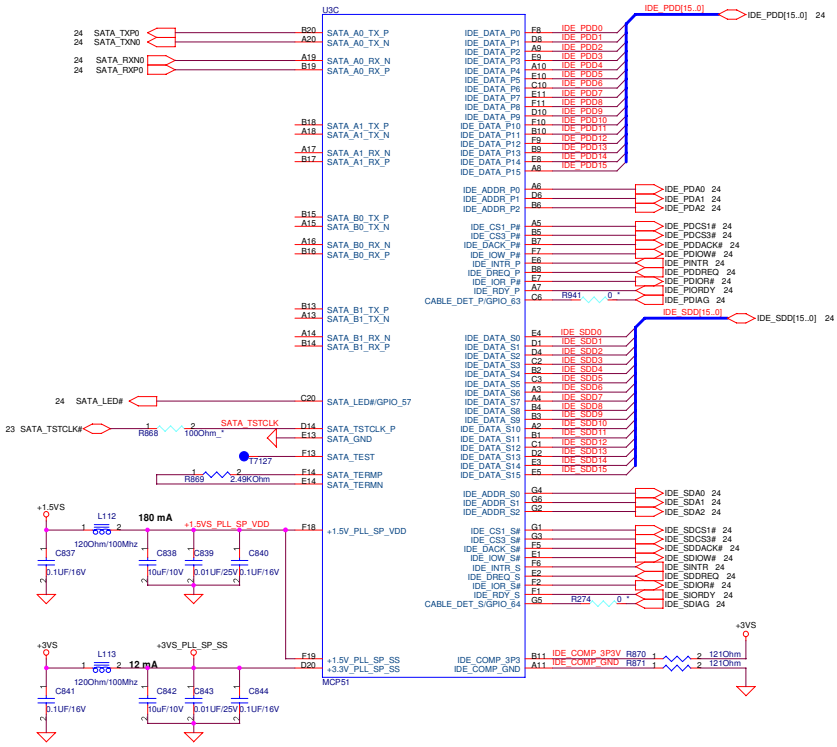
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 18 OF 55	CRT & TV OUT	RELEASE DATE :	Albert Su



<Core Design>

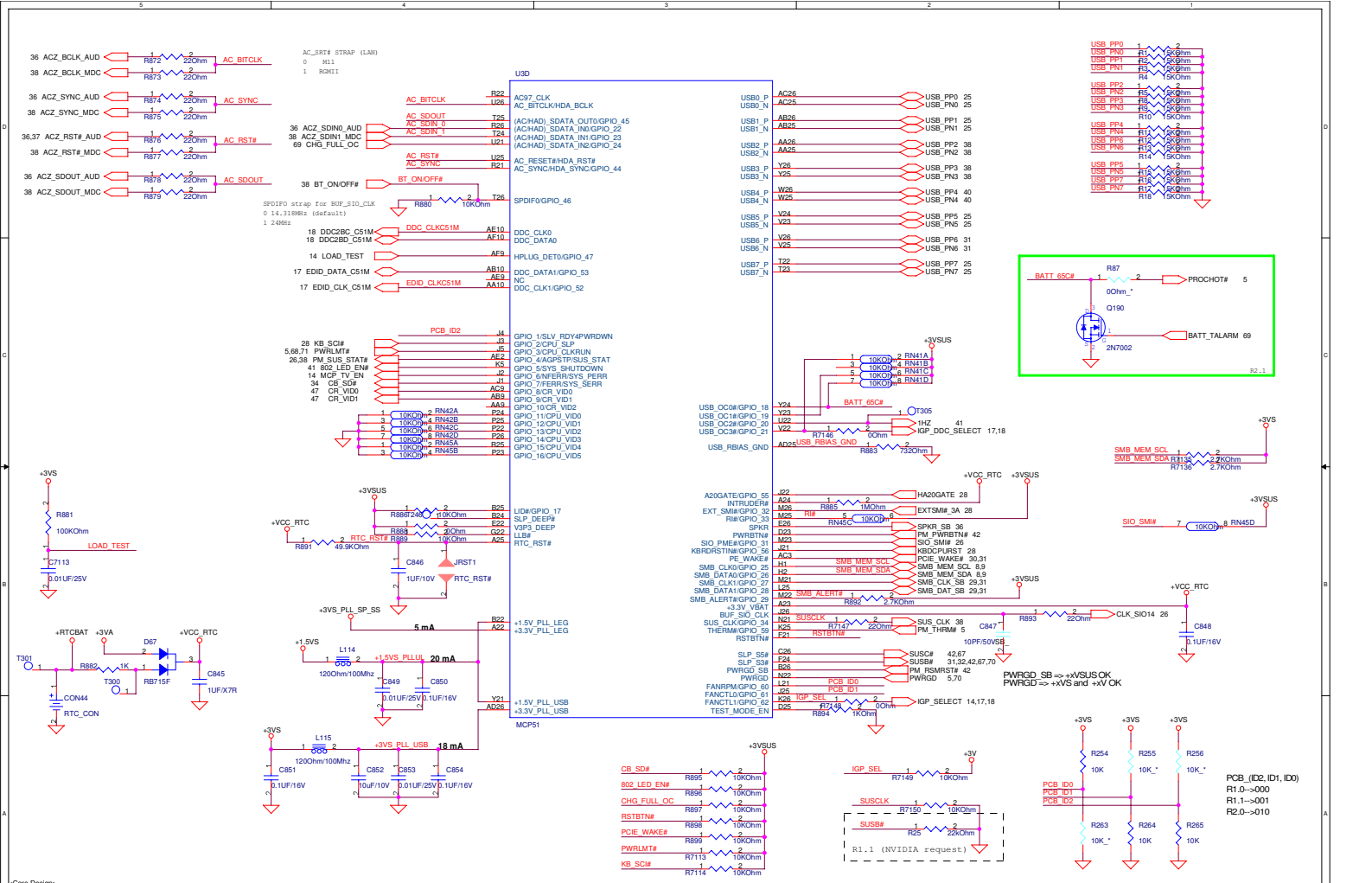
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 19 OF 55		RELEASE DATE :	


U3B
MCP51
PCI_AD[0..31]
PCI_C/BE#[0..3]
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_DEVSEL#
PCI_PAR
PCI_PERR#
PCI_SERR#
PCI_PME#
PM_CLKRUN#
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
MXM_PWR_ON
PCI_GNT0#
PCI_GNT1#
PCI_GNT2#
PCI_INTW#
PCI_INTX#
PCI_INTY#
PCI_INTZ#
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
PCI_CLKIN
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LPC_DRQ#0
LPC_DRQ#1
LPC_SERIRQ
GPU_ON
LPC_CLK0
LPC_CLK1
LPC_RESET#
PCIRST_LAN#
PCIRST_CB#
PCIRST_NEWC#
IDE_RST#
LPCSIO_RST#
LPCFWH_RST#
LPCKBC_RST#
LPCTPM_RST#
+3VS
+3VSUS
BACK_OFF#
INT_SERIRQ



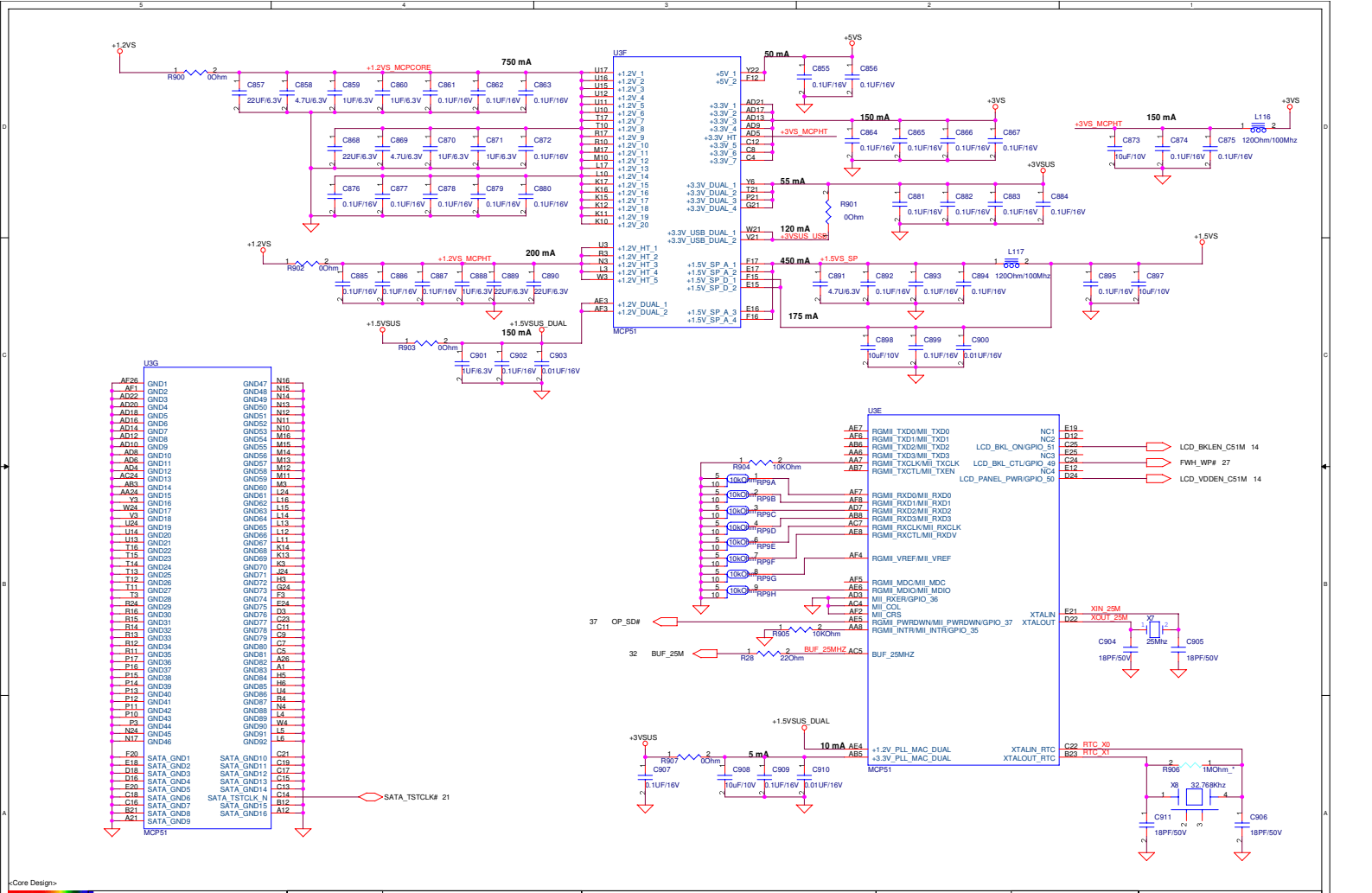
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 21 OF 55		RELEASE DATE :	



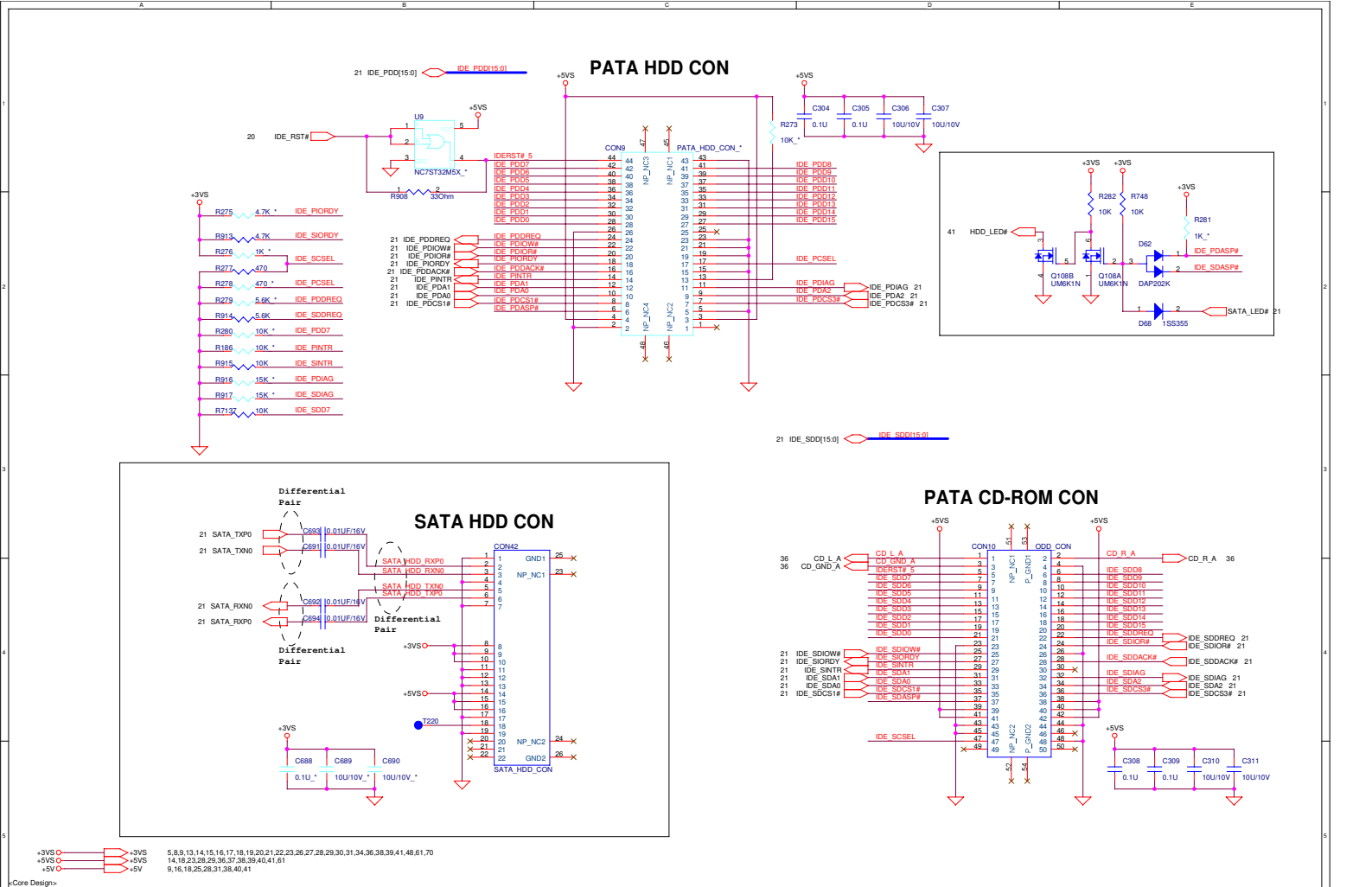
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 USB/HDA	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 22 OF 55		RELEASE DATE :		



<Core Design>

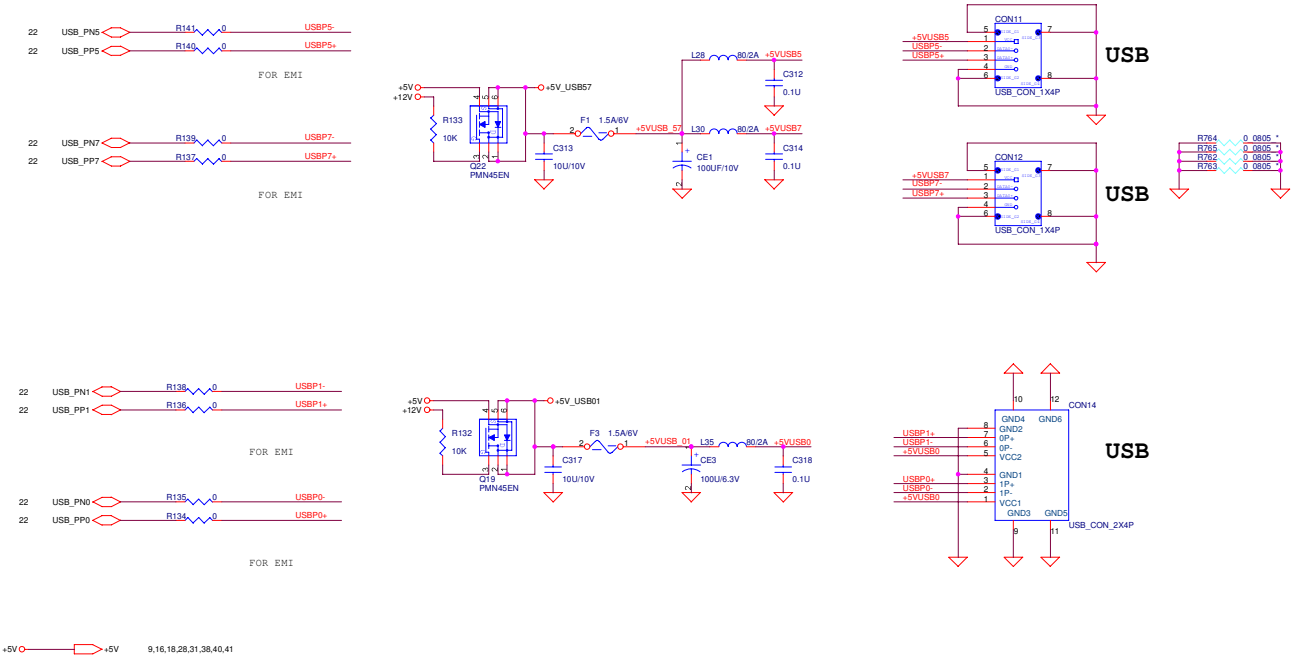
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 23 OF 55		RELEASE DATE :	



+3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30,31,34,36,38,39,41,48,61,70
+5VS 14,18,23,28,29,36,37,38,39,40,41,61
+5V 9,16,18,25,28,31,38,40,41

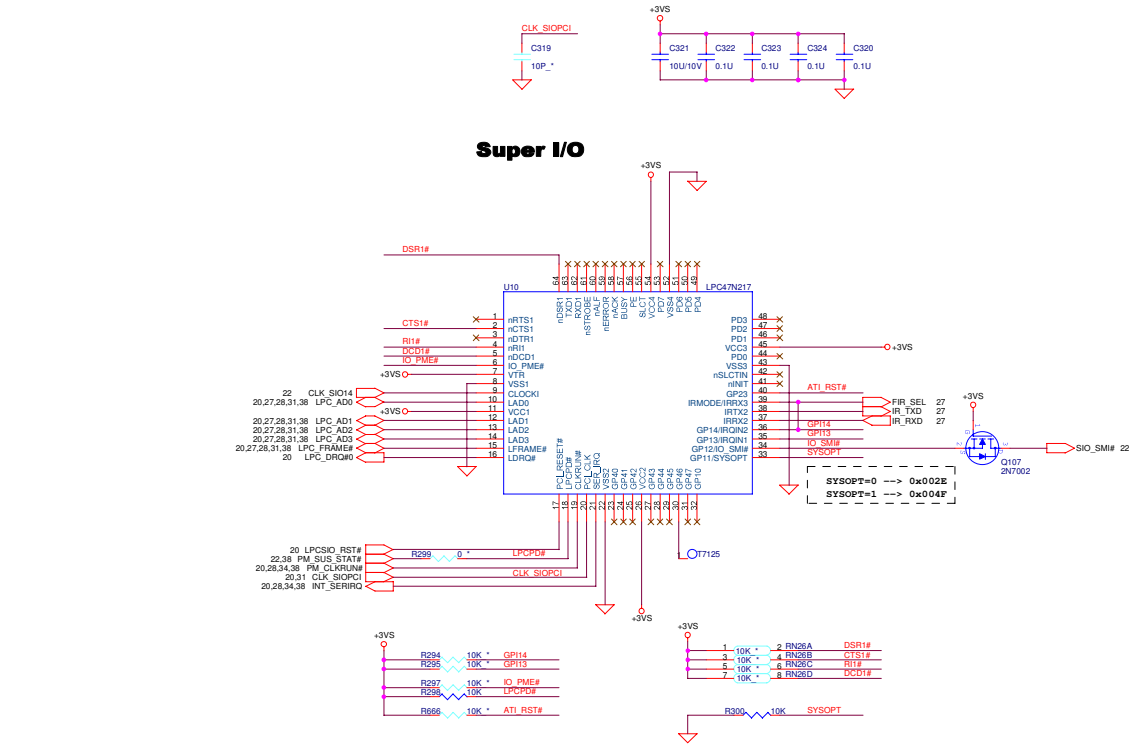
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: HDD & CD-ROM CONN	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 24 OF 55		RELEASE DATE :		



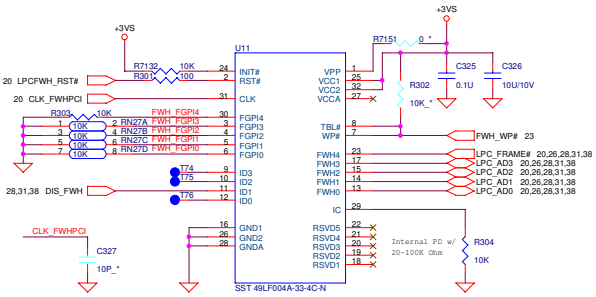
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 25 OF 55		RELEASE DATE :	

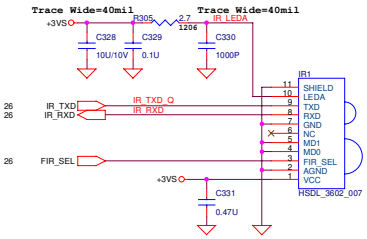


<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 26 OF 55		RELEASE DATE :	Albert Su



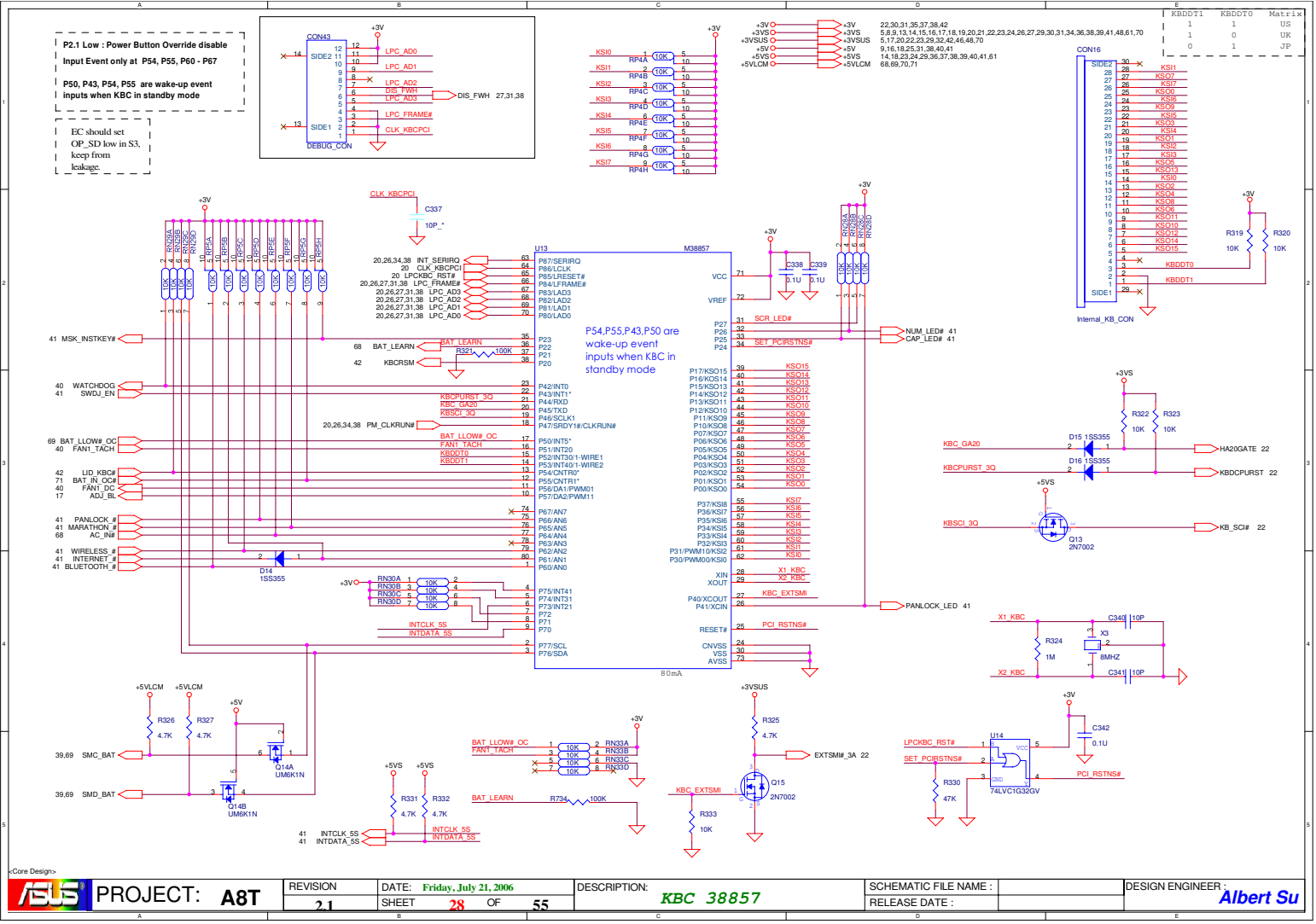
PLCC32 Socket Part Number :
12G043400324
Graphics from:
05-001005111



+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

<Core Design>

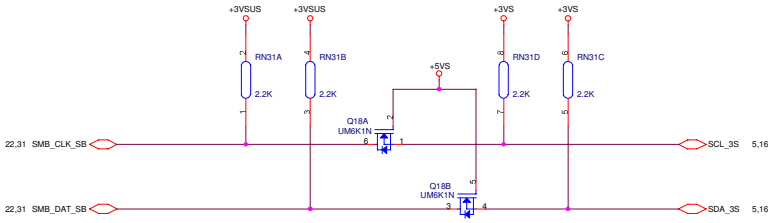
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: BIOS , IR	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 27 OF 55		RELEASE DATE :		



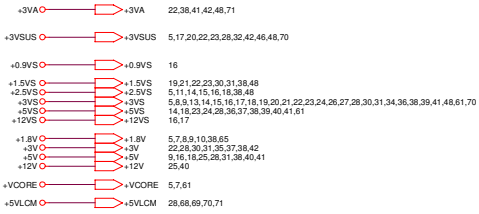
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 28 OF 55	DESCRIPTION: KBC 38857	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

MCP51

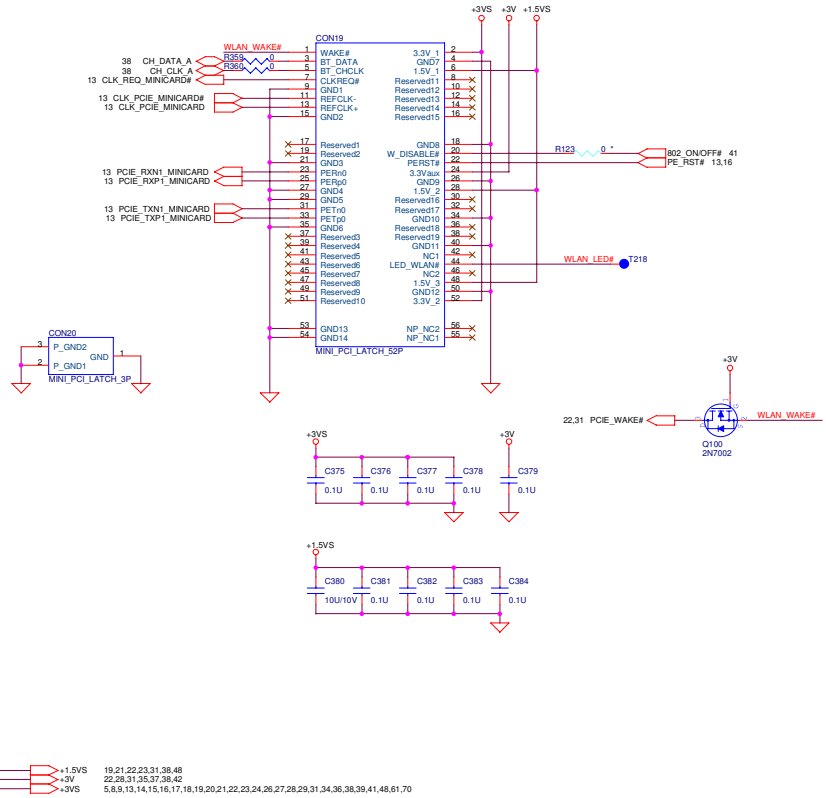


Termal Sensor,
TPM



<Core Design>

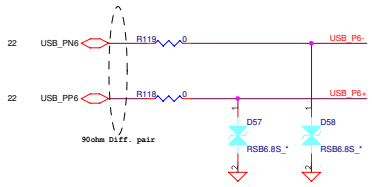
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 29 OF 55		RELEASE DATE :	

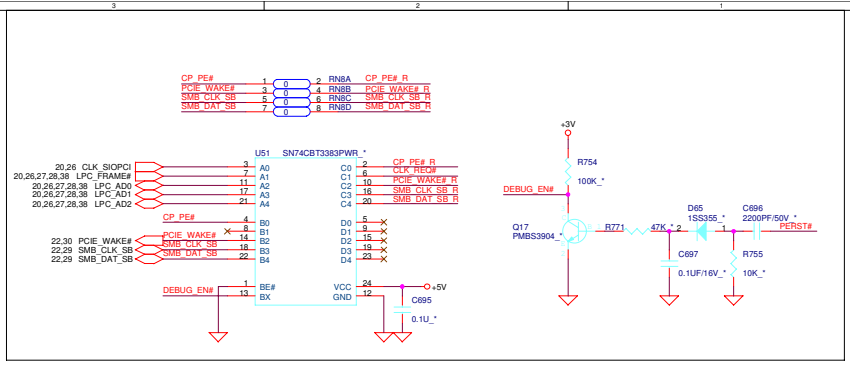


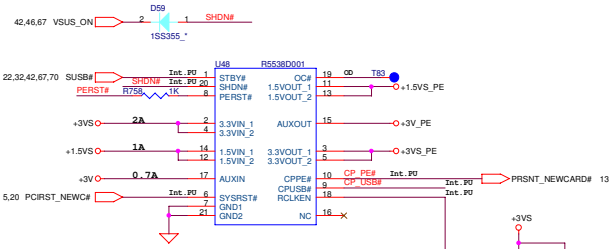
+1.5VS +1.5VS 19,21,22,23,31,38,48
+3V +3V 22,28,31,35,37,38,42
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,31,34,36,38,39,41,48,61,70

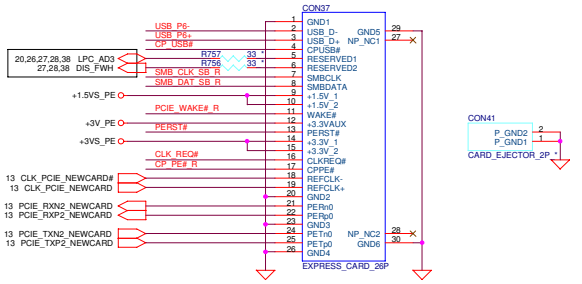
<Core Design>

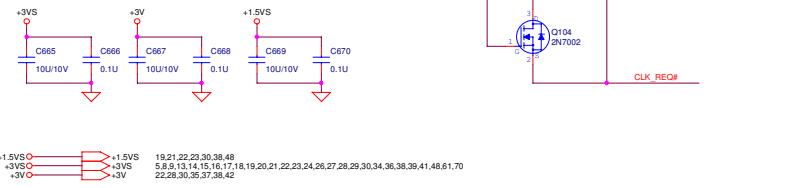
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 30 OF 55		RELEASE DATE :		

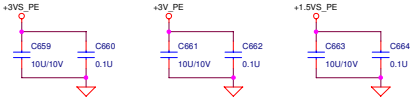








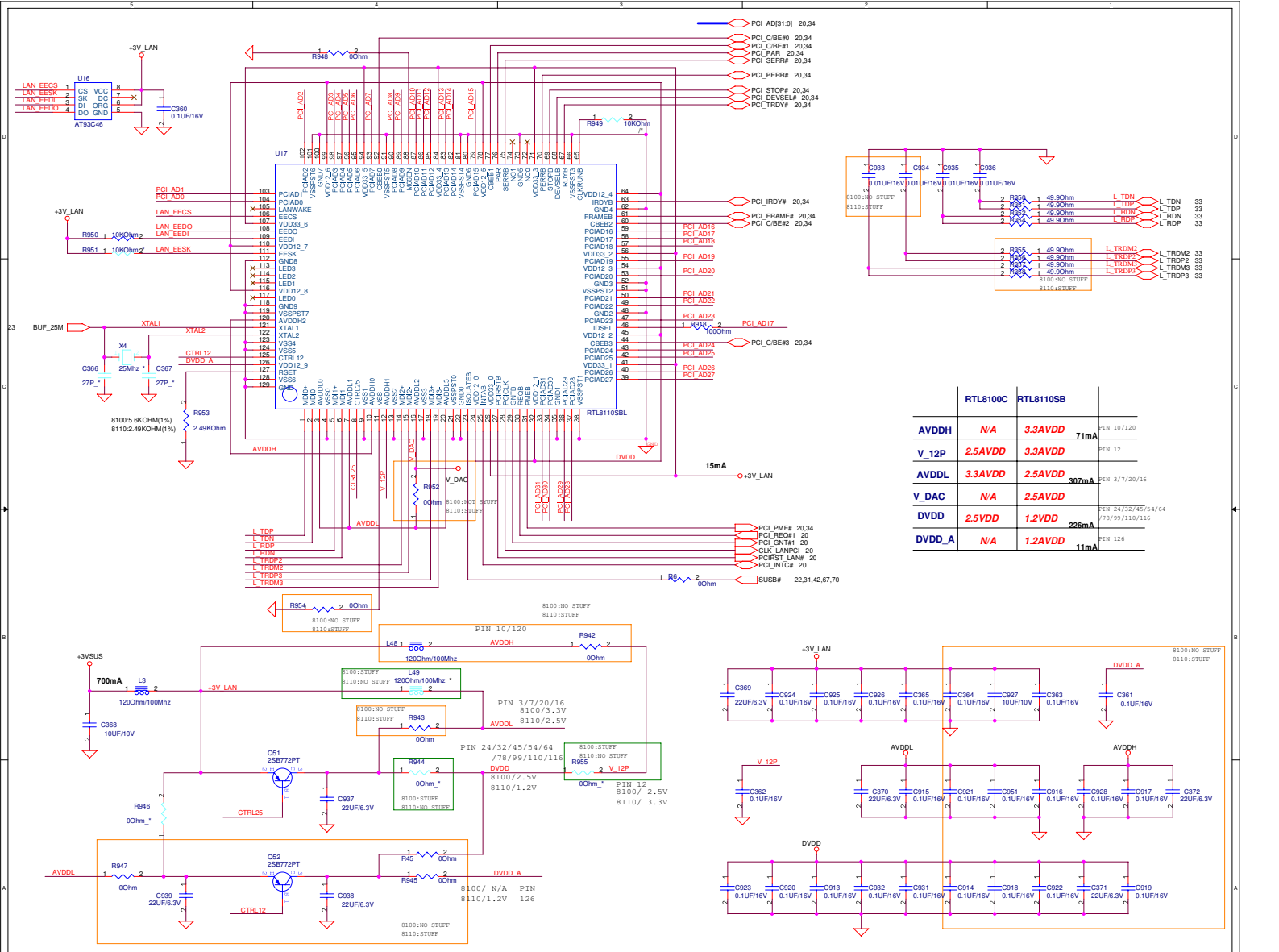




<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: NEW CARD	SCHEMATIC FILE NAME :
		SHEET 31 OF 55		RELEASE DATE :

DESIGN ENGINEER : Albert Su



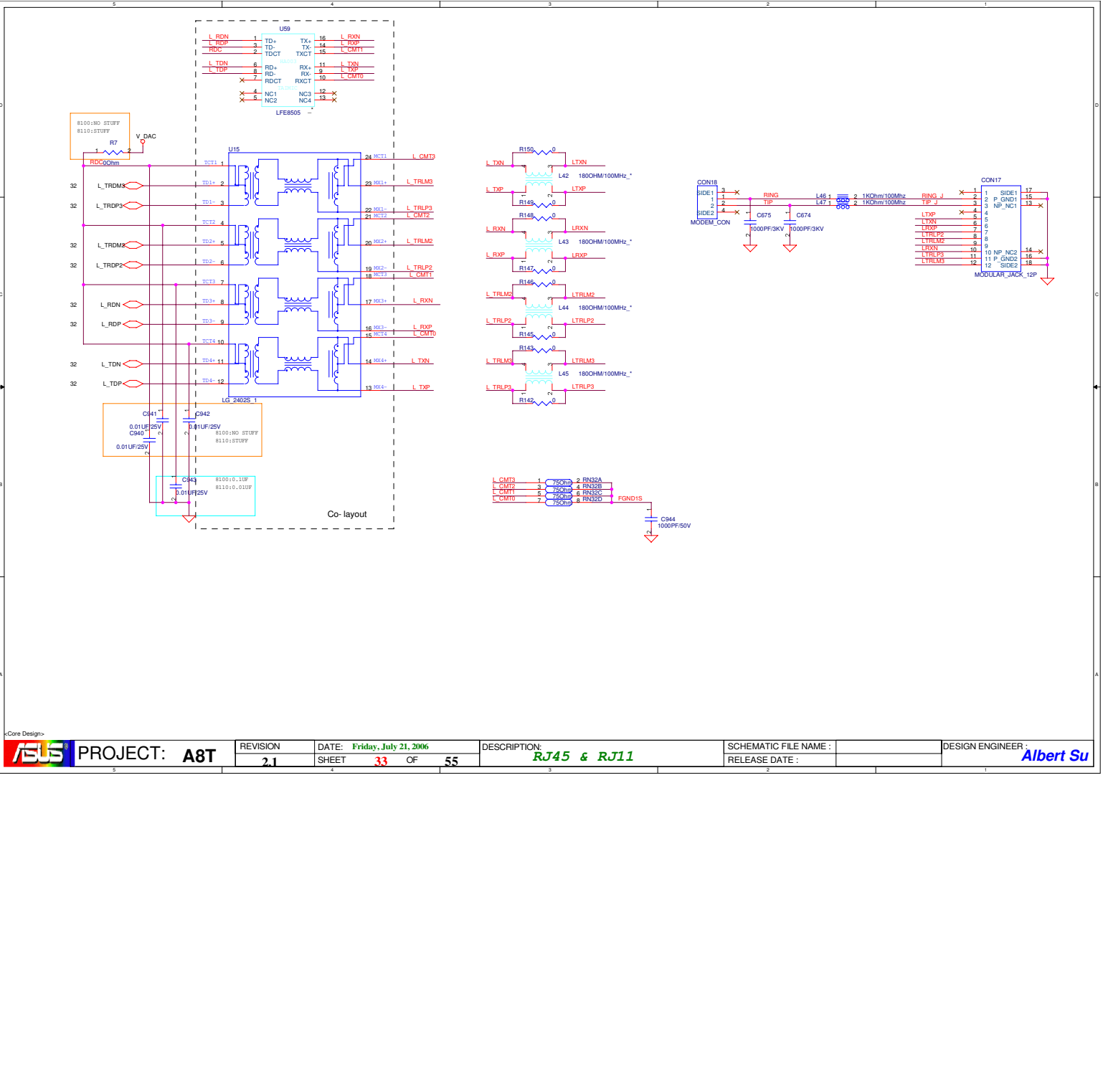
	RTL8100C	RTL8110SB	
AVDDH	N/A	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	
DVDD	2.5VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.2AVDD	PIN 126

71mA
307mA
226mA
11mA

8100:5.6KOHM(1%)
8110:2.49KOHM(1%)

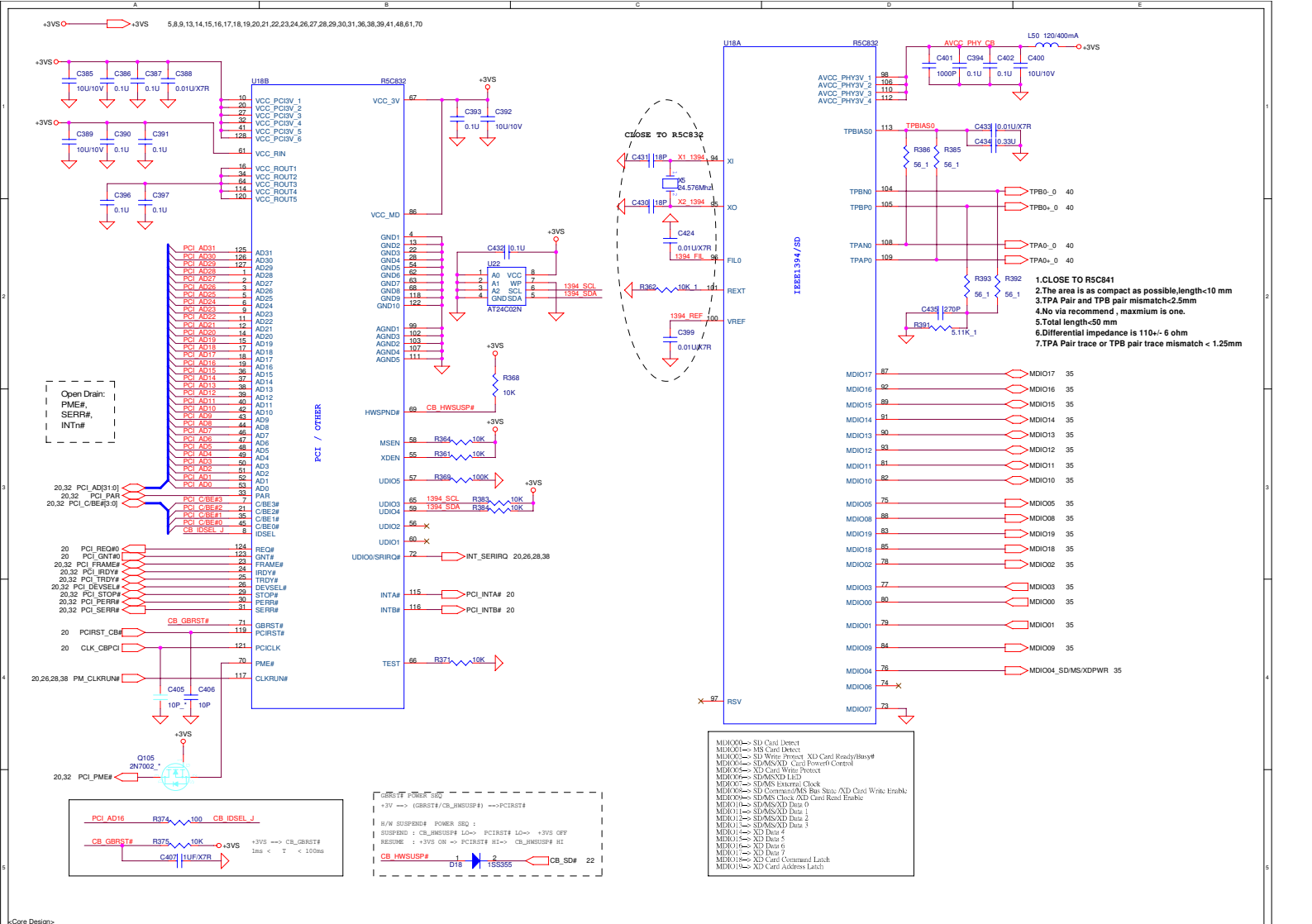
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 32 OF 55	DESCRIPTION: LAN -- RTL8110CL	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



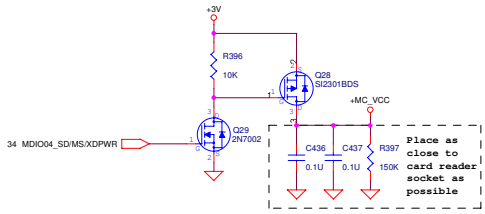
<Core Design>

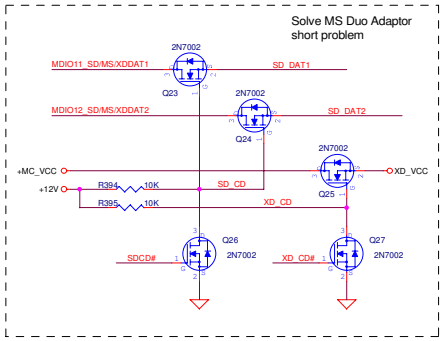
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
	2.1	SHEET 33 OF 55		RELEASE DATE :	

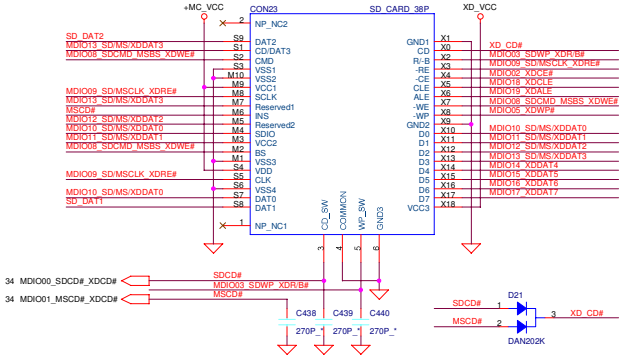


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 34 OF 55	DESCRIPTION: PCI R5C832	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



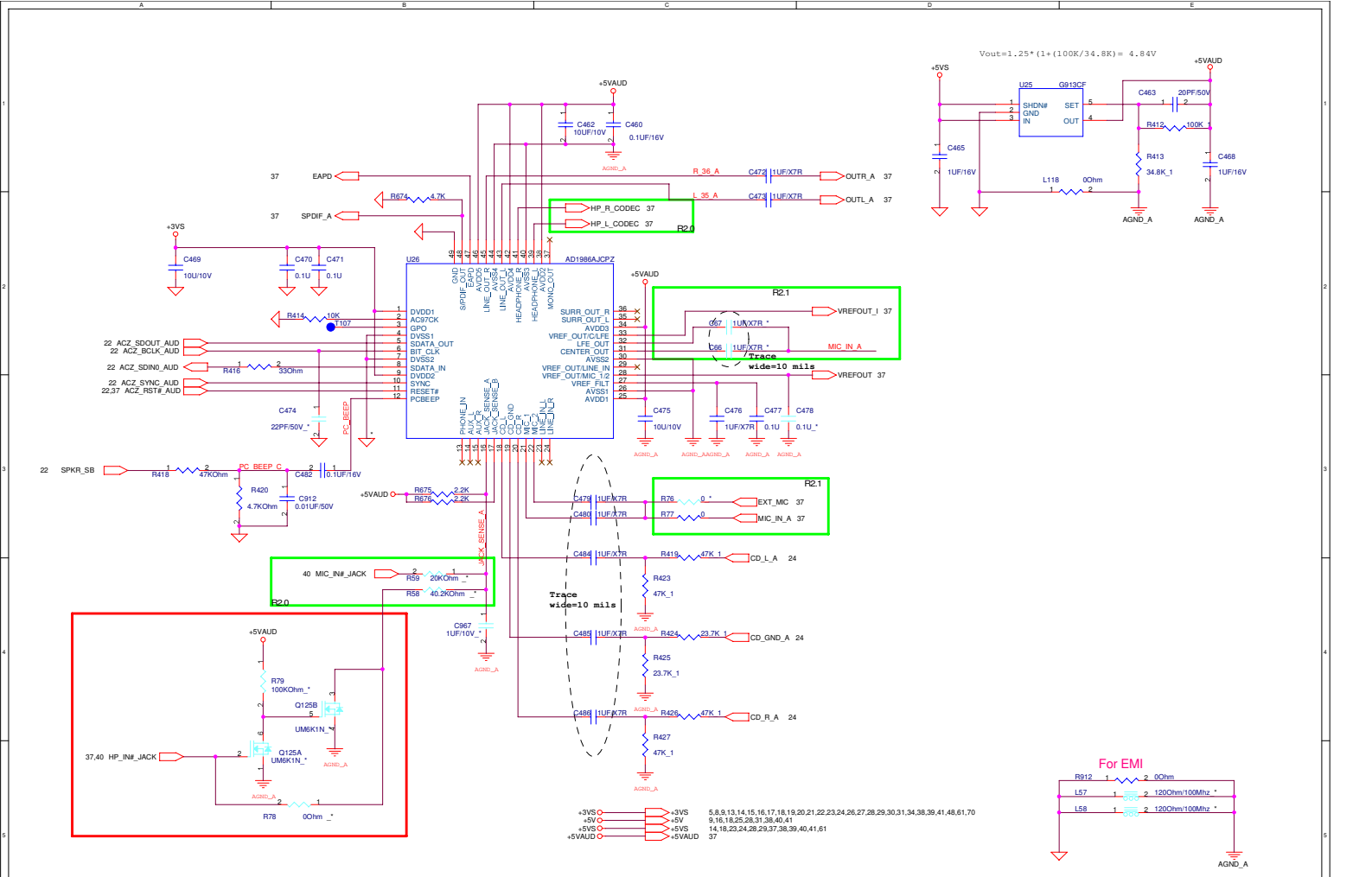




+3V +3V 22,28,30,31,37,38,42
+12V +12V 25,37,40,67

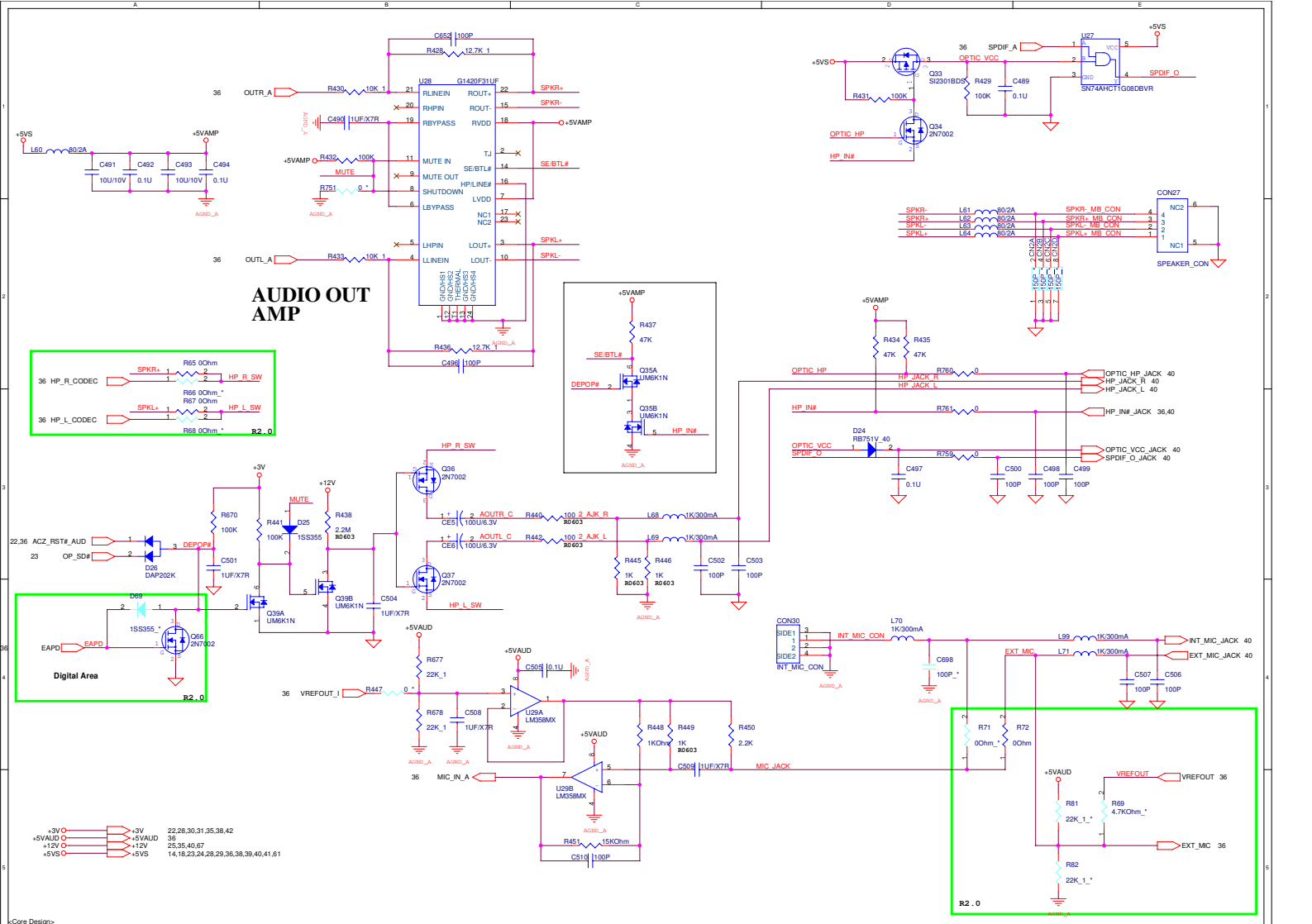
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 35 OF 55	DESCRIPTION: 4 IN 1 CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

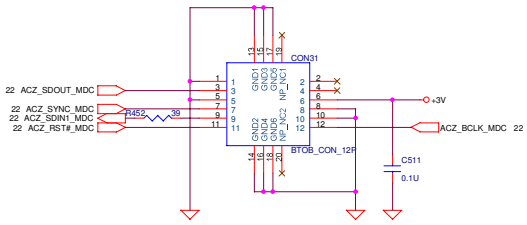


<Core Design>

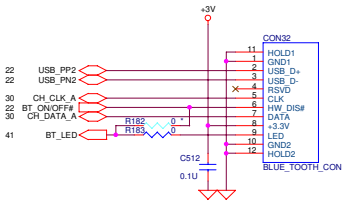
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 36 OF 55	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
					RELEASE DATE :		



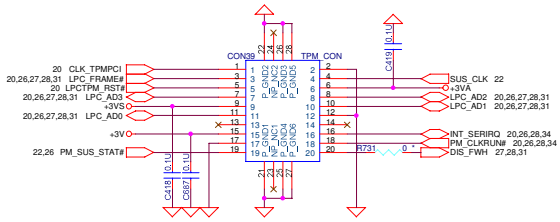
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: AUDIO_AMP(G1420)	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 37 OF 55		RELEASE DATE :		



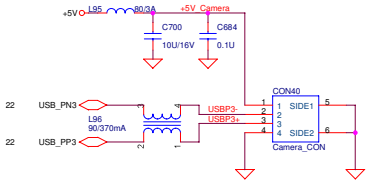
Azalia MDC MODEM CON



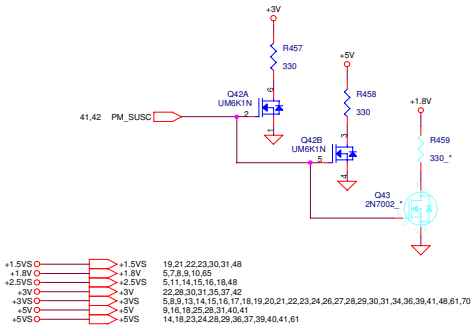
Bluetooth Module CON

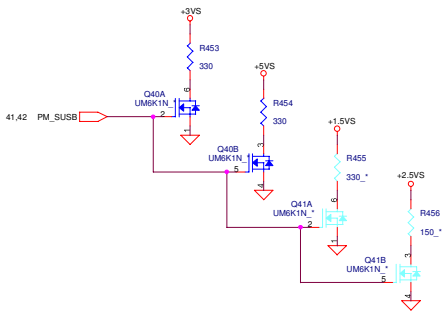


TPM Module CON



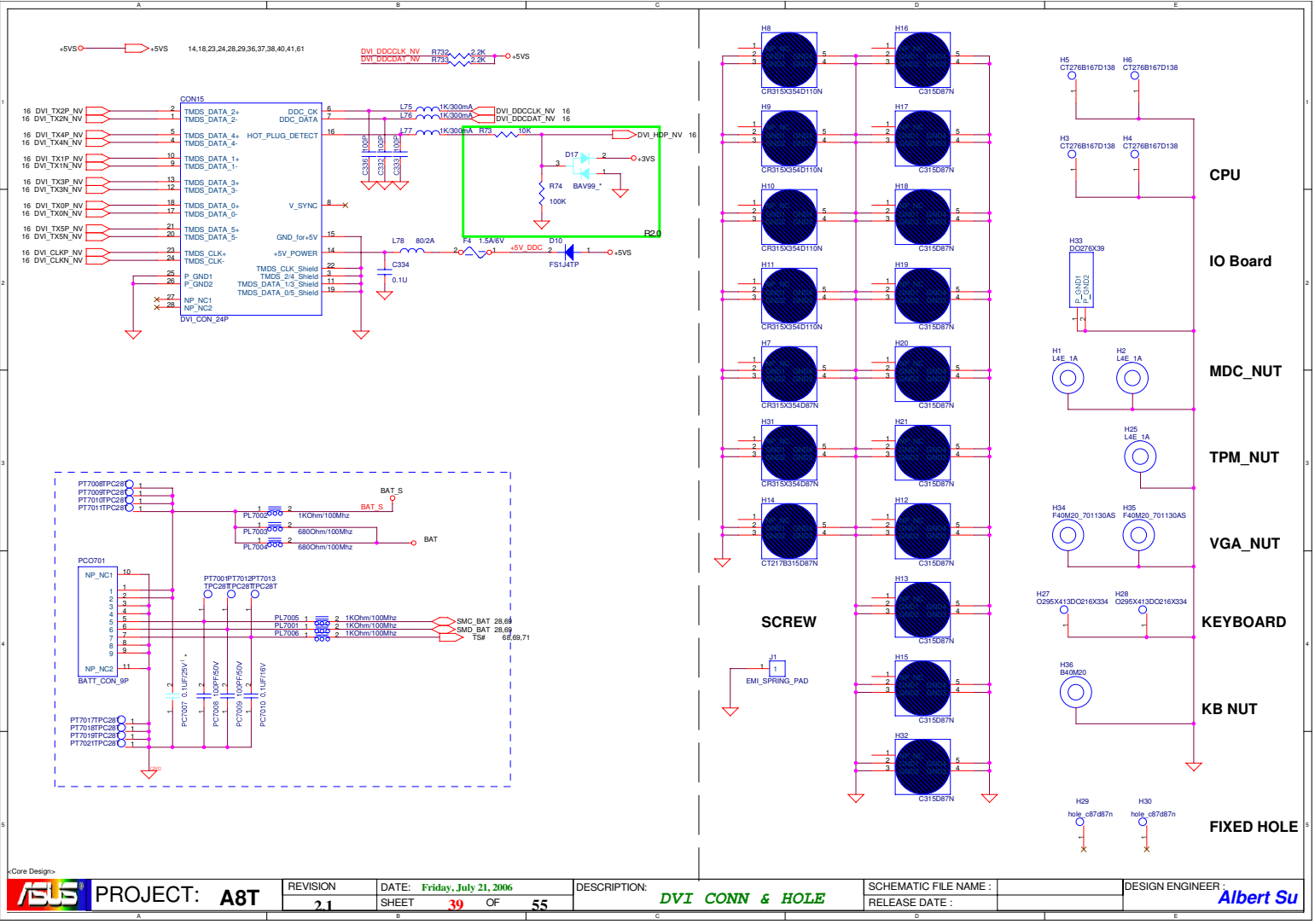
Camera Module CON





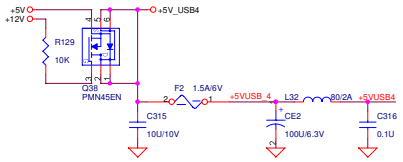
<Core Design>

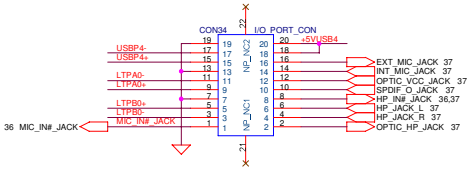
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 38 OF 55	DESCRIPTION: MDC,B/T,TPM,Camera & DISCHG	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



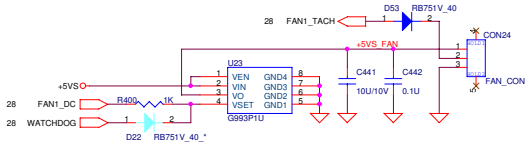
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 39 OF 55		RELEASE DATE :	

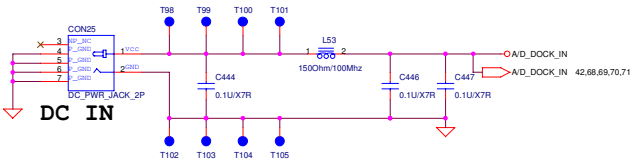




I/O PORT



FAN CONTROL

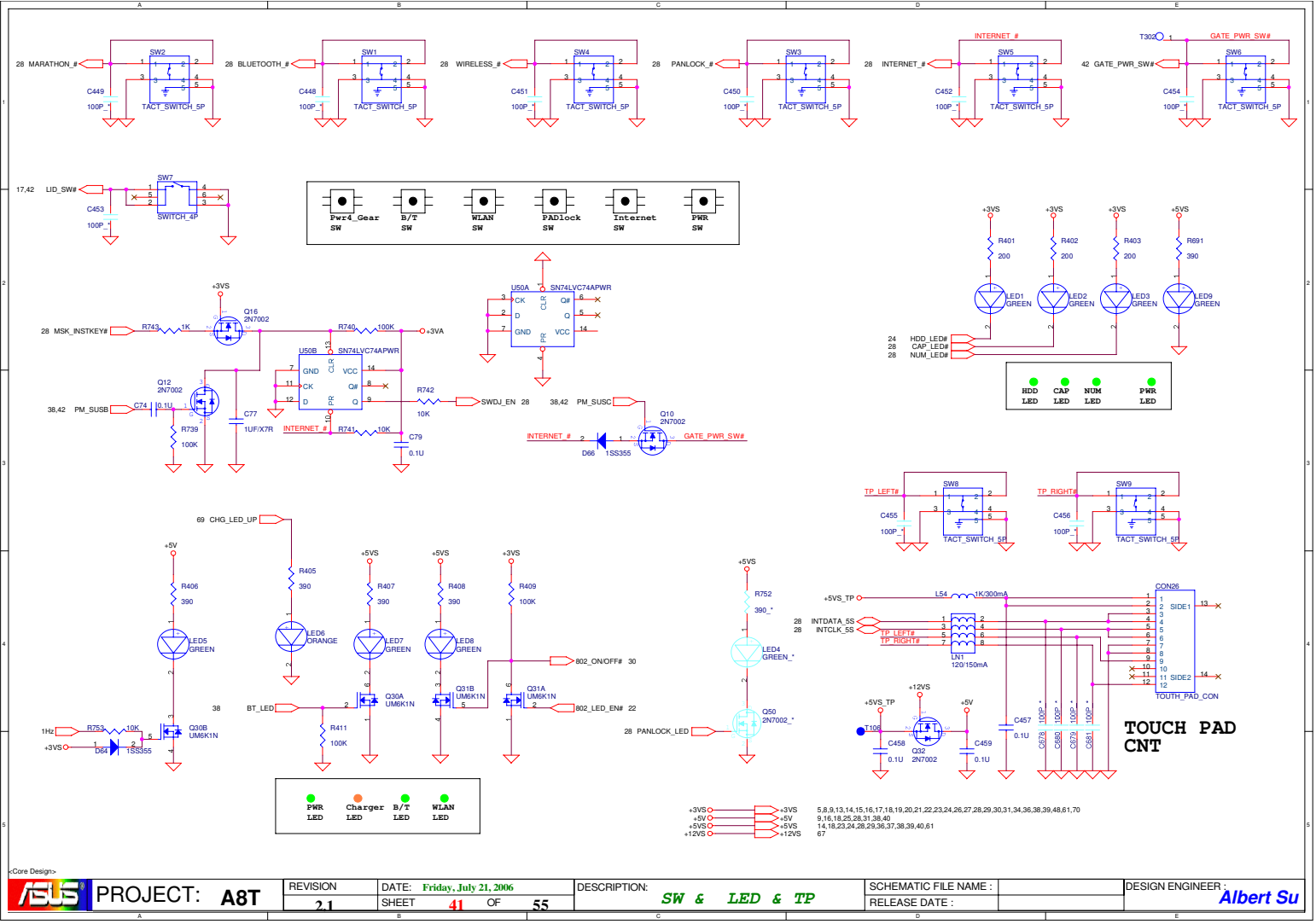


DC IN

ACIN_CONN

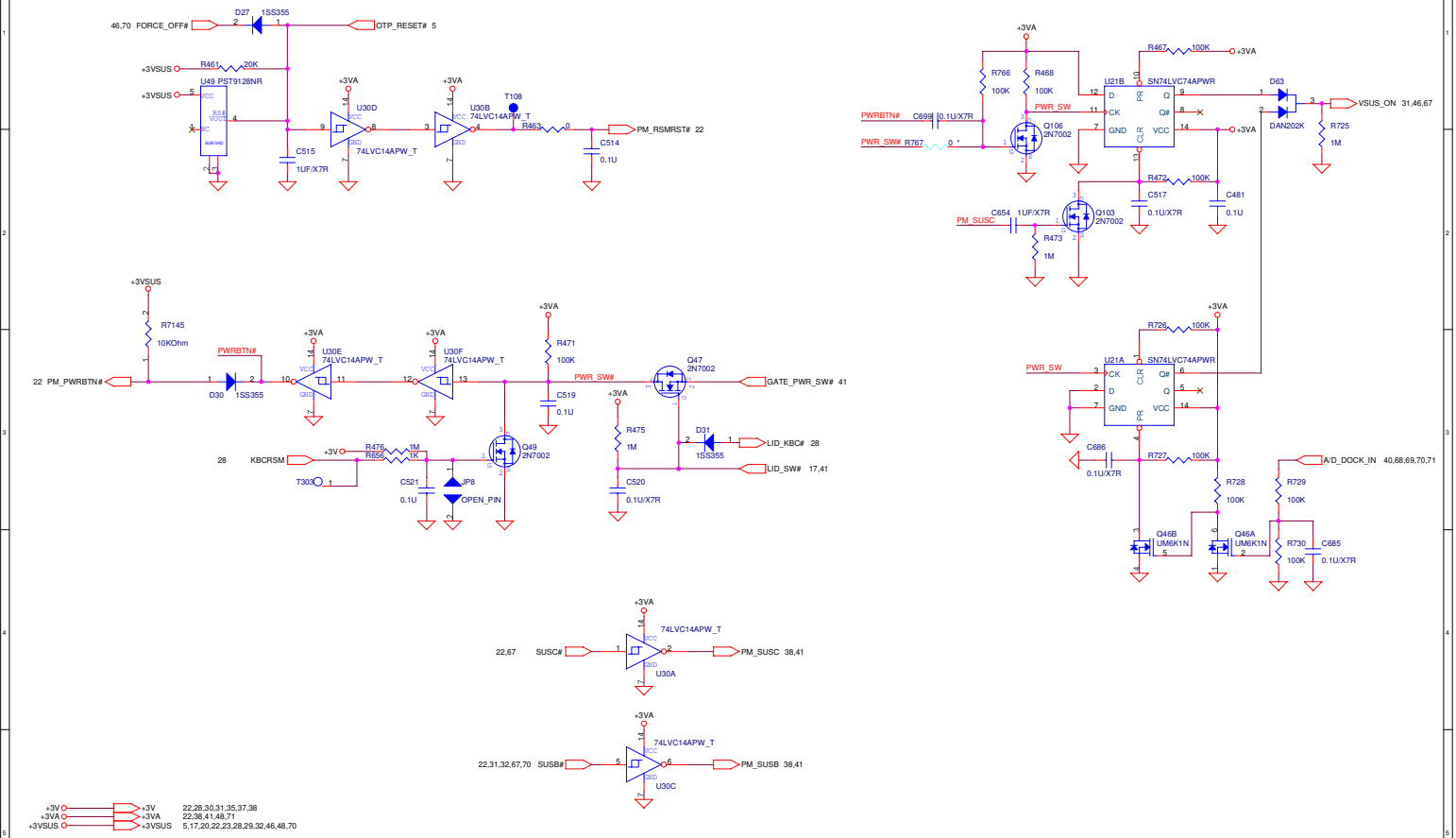
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 40 OF 55	DESCRIPTION: FAN_CTRL & ACIN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 41 OF 55		RELEASE DATE :	



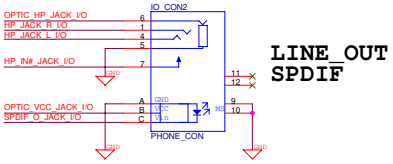
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 42 OF 55		RELEASE DATE :		

Revision History

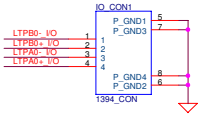
Power:

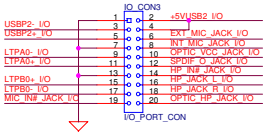
System:

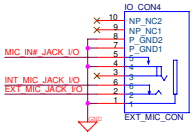


LINE_OUT
SPDIF

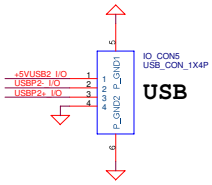
1394A



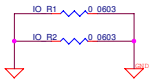




MIC

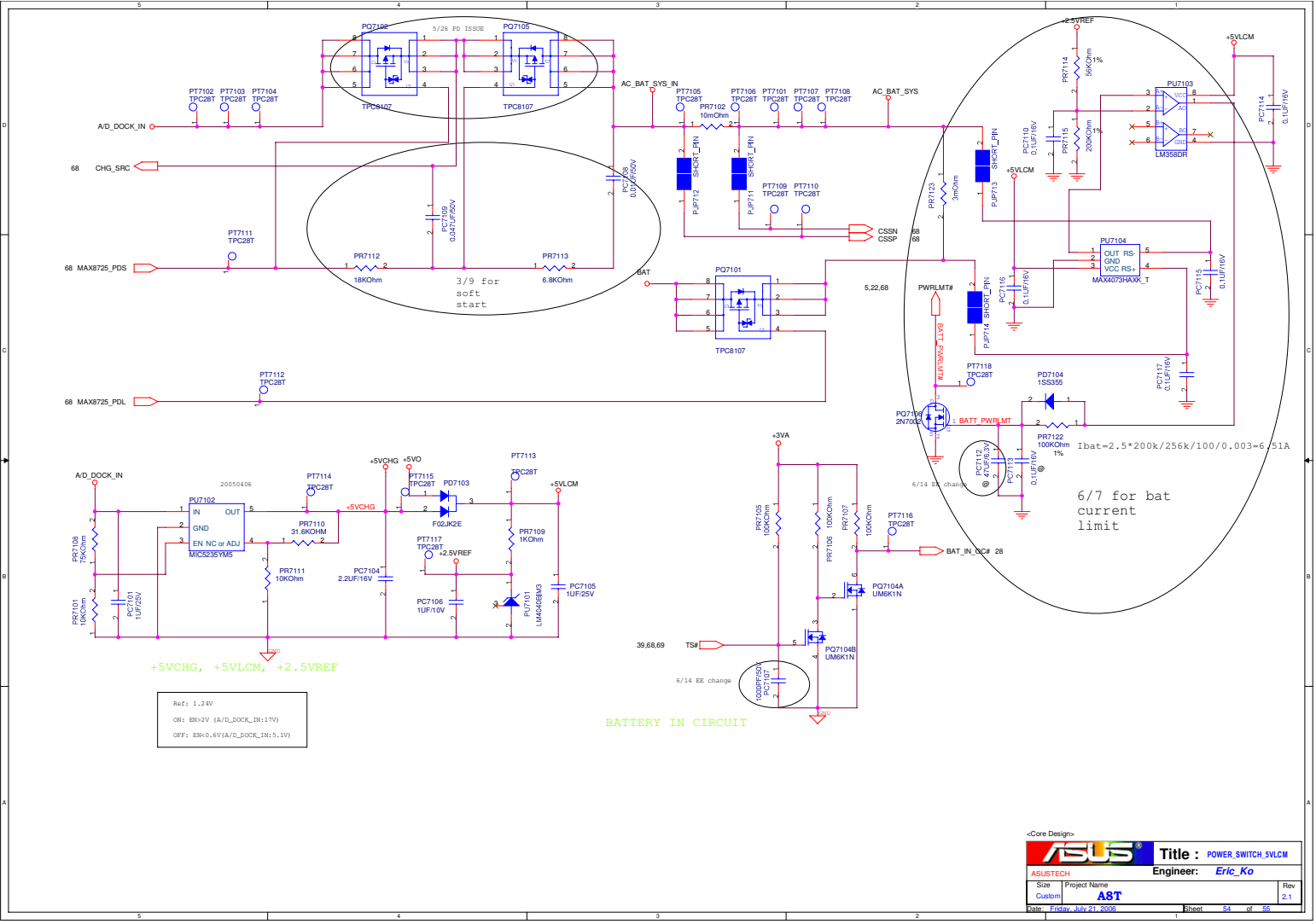


USB



<Core Design>

PROJECT: **A8T**	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: *I/O PORT*	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Albert Su*
		SHEET 44 OF 55		RELEASE DATE :	



<Core Design>

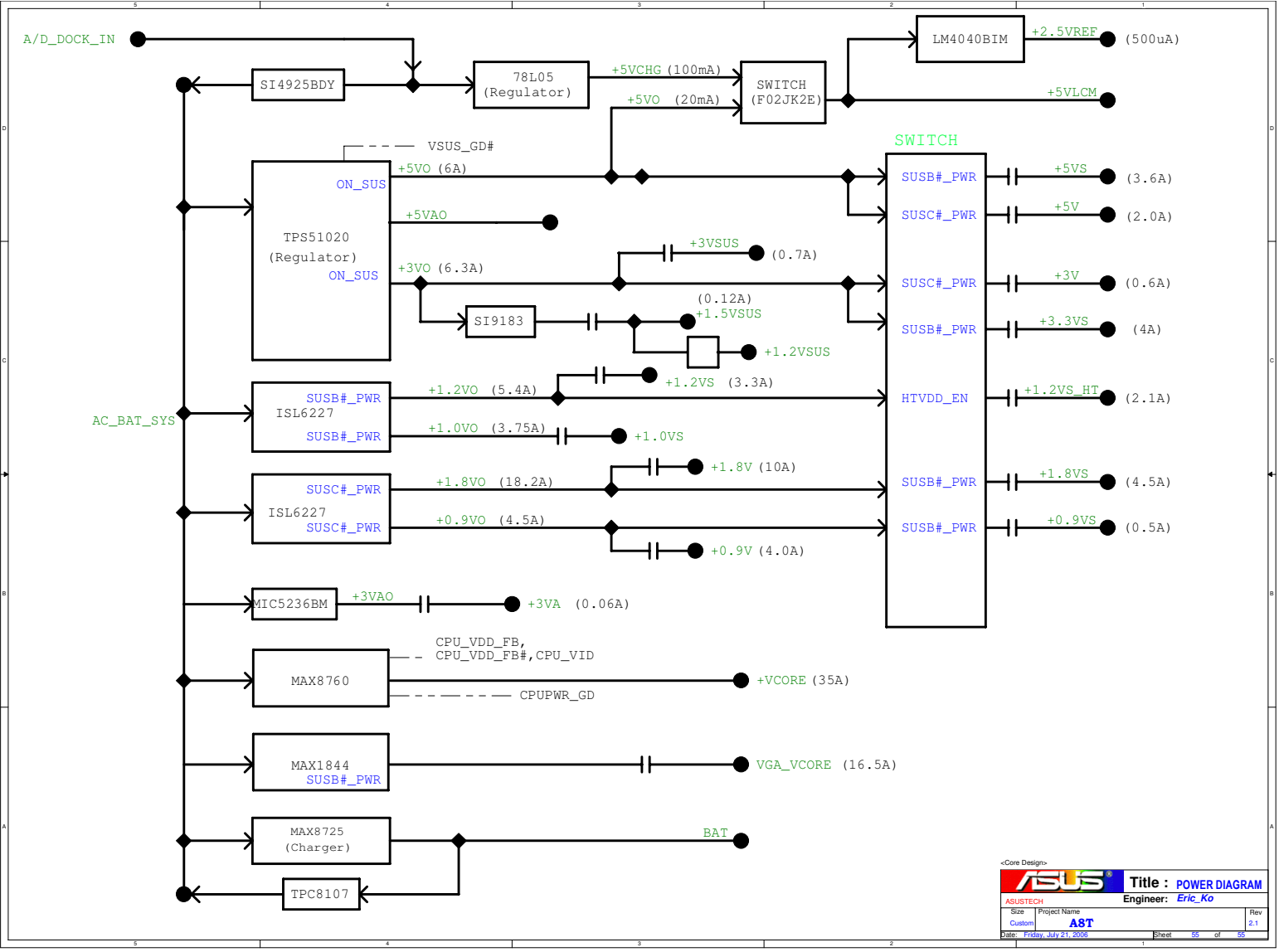
ASUSTECH

Title : POWER_SWITCH_5VLCM

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

Date: Friday, July 21, 2006 Sheet 54 of 55



<Core Design>

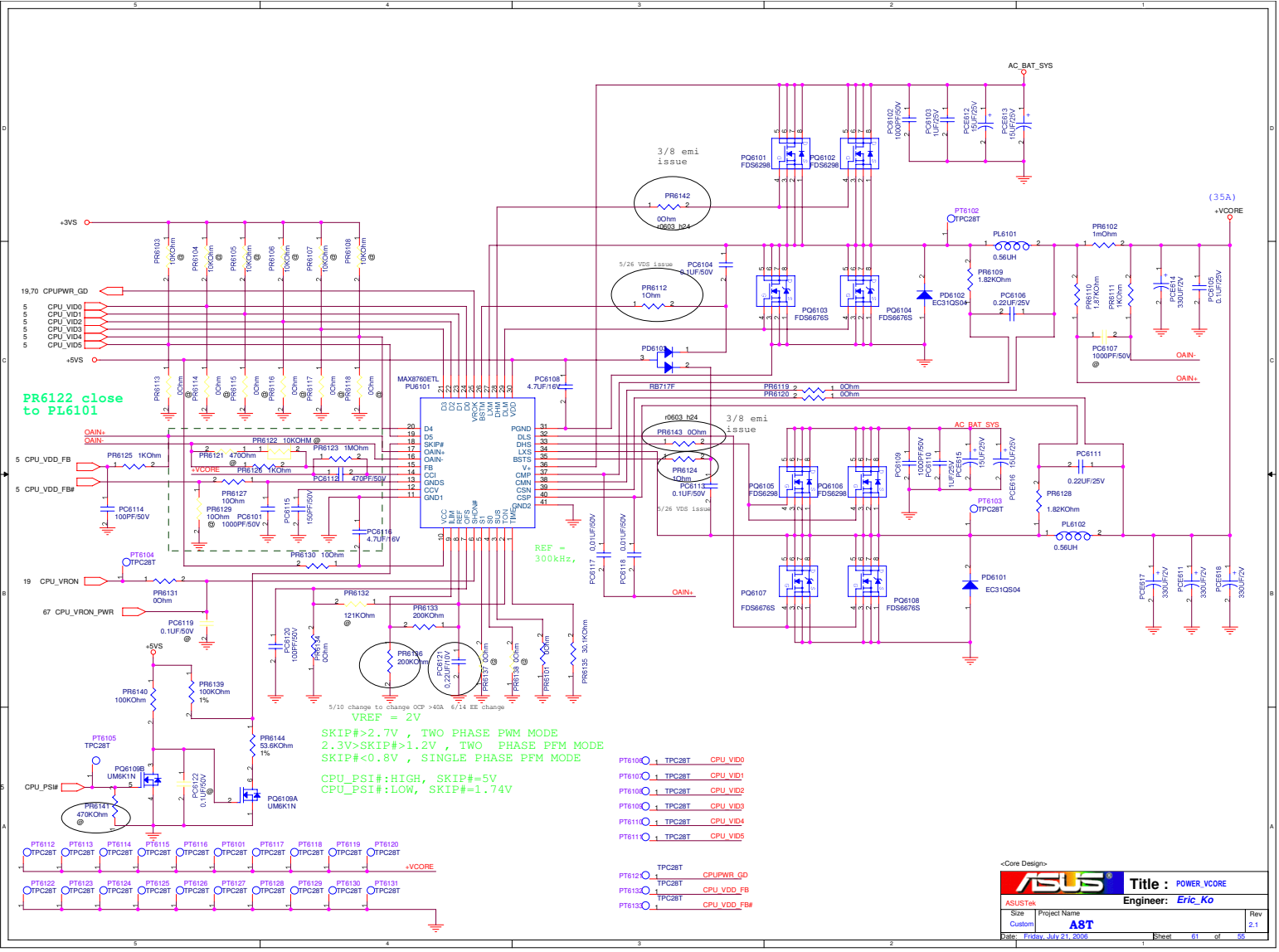
ASUSTECH

Title : POWER DIAGRAM

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

Date: Friday, July 21, 2006 Sheet 55 of 55


AC_BAT_SYS
+VCORE
(35A)
+3VS
+5VS
19,70 CPUPWR_GD
5 CPU_VID0
5 CPU_VID1
5 CPU_VID2
5 CPU_VID3
5 CPU_VID4
5 CPU_VID5
PR6122 close to PL6101
MAX8760ETL PU6101
5 CPU_VDD_FB
5 CPU_VDD_FB#
19 CPU_VRON
67 CPU_VRON_PWR
CPU_PSI#
OAIN+
OAIN-
3/8 emi issue
5/26 VDS issue
REF = 300kHz,
VREF = 2V
SKIP#>2.7V , TWO PHASE PWM MODE
2.3V>SKIP#>1.2V , TWO PHASE PFM MODE
SKIP#<0.8V , SINGLE PHASE PFM MODE
CPU_PSI#:HIGH, SKIP#=5V
CPU_PSI#:LOW, SKIP#=1.74V
5/10 change to change OCP >40A 6/14 EE change
PQ6101 FDS6298
PQ6102 FDS6298
PQ6103 FDS6676S
PQ6104 FDS6676S
PQ6105 FDS6298
PQ6106 FDS6298
PQ6107 FDS6676S
PQ6108 FDS6676S
PD6101 EC31QS04
PD6102 EC31QS04
PL6101 0.56UH
PL6102 0.56UH
PR6142 0Ohm
PR6143 0Ohm
PR6124 1Ohm
PR6112 1Ohm
PR6102 1mOhm
PR6109 1.82KOhm
PR6128 1.82KOhm
PC6104 0.1UF/50V
PC6106 0.22UF/25V
PC6111 0.22UF/25V
PC6107 1000PF/50V
PC6108 4.7UF/16V
PC6112 0.1UF/50V
PC6113 470PF/50V
PC6114 100PF/50V
PC6116 4.7UF/16V
PC6117 0.01UF/50V
PC6118 0.01UF/50V
PC6119 0.1UF/50V
PC6121 0.22UF/10V
PC6122 0.1UF/50V
PR6139 100KOhm 1%
PR6140 100KOhm
PR6144 53.6KOhm 1%
PR6141 470KOhm
PR6132 121KOhm
PR6133 200KOhm
PR6136 200KOhm
PR6135 30.1KOhm
PR6122 10KOHM
PR6123 1MOhm
PR6121 470Ohm
PR6126 1KOhm
PR6127 10Ohm
PR6129 10Ohm
PR6130 10Ohm
PR6125 1KOhm
PR6131 0Ohm
PC6115 150PF/50V
PC6120 100PF/50V
PC6109 1000PF/50V
PC6101 1000PF/50V
PC6615 1UF/25V
PC6616 15UF/25V
PC6617 330UF/2V
PC6618 330UF/2V
PC6611 330UF/2V
PC6102 1000PF/50V
PC6103 1UF/25V
PC6612 15UF/25V
PC6613 15UF/25V
PC6105 0.1UF/25V
PC6614 330UF/2V
PT6104 TPC28T
PT6105 TPC28T
PT6102 TPC28T
PT6103 TPC28T
PT6106 TPC28T
PT6107 TPC28T
PT6108 TPC28T
PT6109 TPC28T
PT6110 TPC28T
PT6111 TPC28T
PT6112 TPC28T
PT6113 TPC28T
PT6114 TPC28T
PT6115 TPC28T
PT6116 TPC28T
PT6101 TPC28T
PT6117 TPC28T
PT6118 TPC28T
PT6119 TPC28T
PT6120 TPC28T
PT6122 TPC28T
PT6123 TPC28T
PT6124 TPC28T
PT6125 TPC28T
PT6126 TPC28T
PT6127 TPC28T
PT6128 TPC28T
PT6129 TPC28T
PT6130 TPC28T
PT6131 TPC28T
PT6132 TPC28T
PT6133 TPC28T
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPUPWR_GD
CPU_VDD_FB
CPU_VDD_FB#
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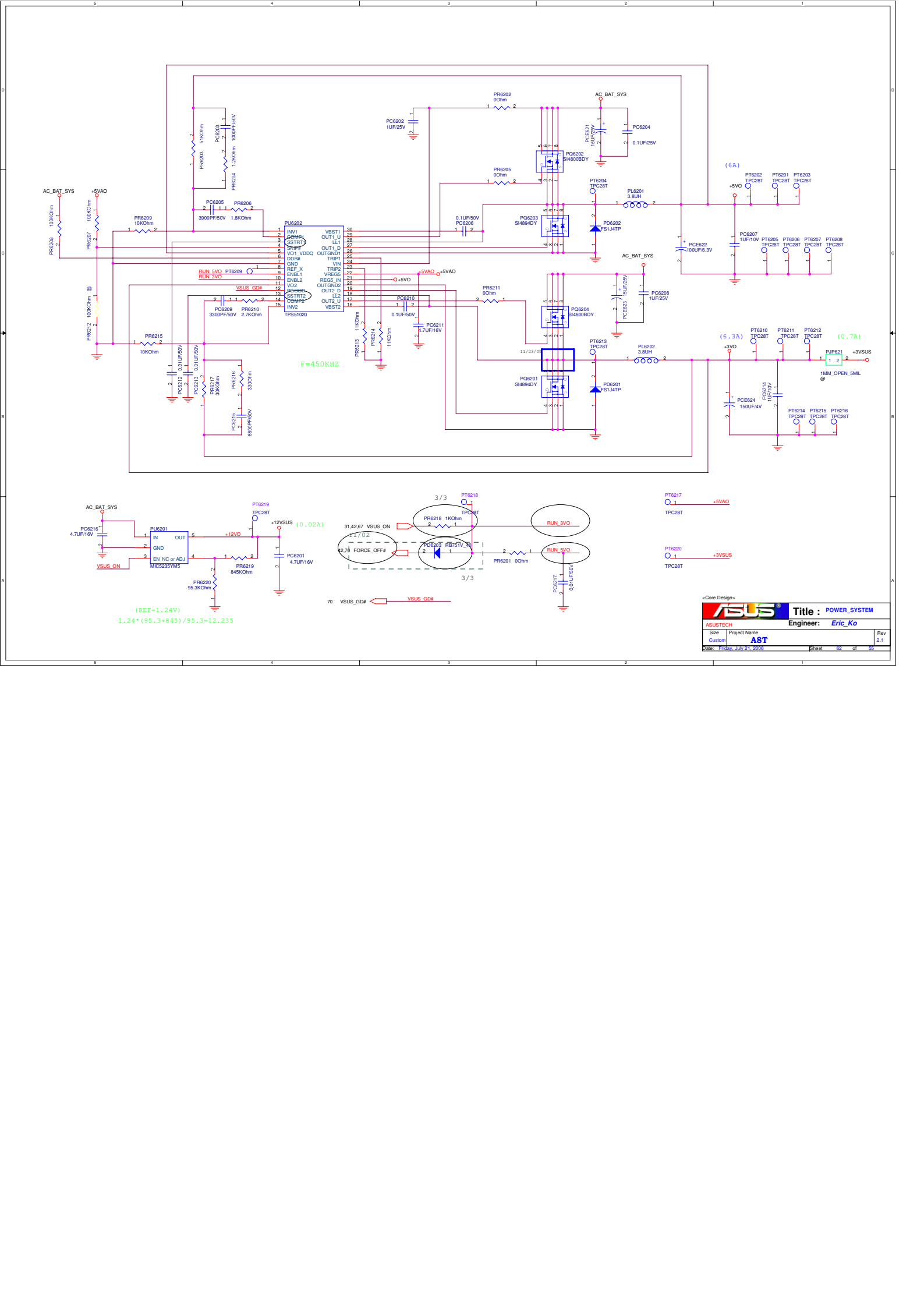
Title : POWER_VCORE
Engineer: Eric_Ko
ASUSTek
Size Custom
Project Name A8T
Rev 2.1
Date: Friday, July 21, 2006
Sheet 61 of 55


AC_BAT_SYS
+5VAO
PR6208 100KOhm
PR6207 100KOhm
PR6212 100KOhm @
PR6209 10KOhm
PR6215 10KOhm
PR6203 51KOhm
PC6203 1000PF/50V
PR6204 1.2KOhm
PC6205 3900PF/50V
PR6206 1.8KOhm
PC6209 3300PF/50V
PR6210 2.7KOhm
PC6212 0.01UF/50V
PC6213 0.01UF/50V
PR6217 30KOhm
PR6216 330Ohm
PC6215 6800PF/50V
PU6202
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
TPS51020
F=450KHZ
RUN_5VO
RUN_3VO
PT6209
VSUS_GD#
PR6202 0Ohm
PR6205 0Ohm
PC6202 1UF/25V
PC6206 0.1UF/50V
PC6210 0.1UF/50V
PC6211 4.7UF/16V
PR6211 0Ohm
PR6213 11KOhm
PR6214 11KOhm
PQ6202 SI4800BDY
PQ6203 SI4894DY
PQ6204 SI4800BDY
PQ6201 SI4894DY
PC6201 15UF/25V
PC6204 0.1UF/25V
PC6208 1UF/25V
PC6223 15UF/25V
PT6204 TPC28T
PT6213 TPC28T
PL6201 3.8UH
PL6202 3.8UH
PD6202 FS1J4TP
PD6201 FS1J4TP
(6A)
(6.3A)
(0.7A)
+5VO
+3VO
PT6202 TPC28T
PT6201 TPC28T
PT6203 TPC28T
PT6210 TPC28T
PT6211 TPC28T
PT6212 TPC28T
PJP621
+3VSUS
1MM_OPEN_5MIL @
PC6207 1UF/10V
PC6222 100UF/6.3V
PC6214 1UF/10V
PCE624 150UF/4V
PT6205 TPC28T
PT6206 TPC28T
PT6207 TPC28T
PT6208 TPC28T
PT6214 TPC28T
PT6215 TPC28T
PT6216 TPC28T
PU6201
IN
OUT
GND
EN NC or ADJ
MIC5235YM5
VSUS_ON
PC6216 4.7UF/16V
PT6219 TPC28T
+12VSUS
(0.02A)
+12VO
PR6219 845KOhm
PR6220 95.3KOhm
PC6201 4.7UF/16V
(REF=1.24V)
1.24*(95.3+845)/95.3=12.235
3/3
PT6218 TPC28T
PR6218 1KOhm
PD6203 RB751V_40
PR6201 0Ohm
PC6217 0.01UF/50V
31,42,67 VSUS_ON
42,78 FORCE_OFF#
RUN_3VO
RUN_5VO
70 VSUS_GD#
PT6217 TPC28T
+5VAO
PT6220 TPC28T
+3VSUS
<Core Design>
Title : POWER_SYSTEM
ASUSTECH
Engineer: Eric_Ko
Size Custom
Project Name A8T
Rev 2.1
Date: Friday, July 21, 2006
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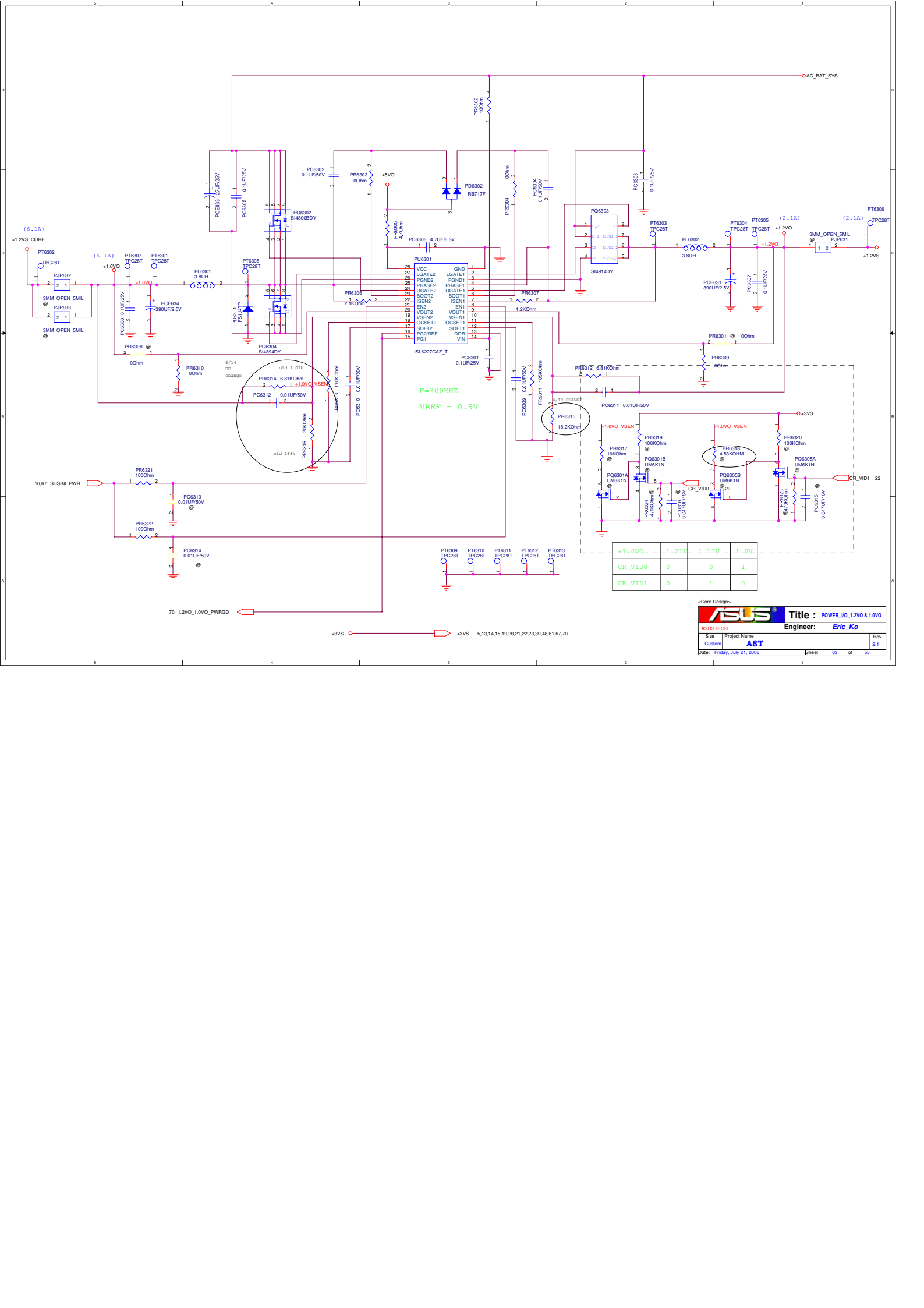
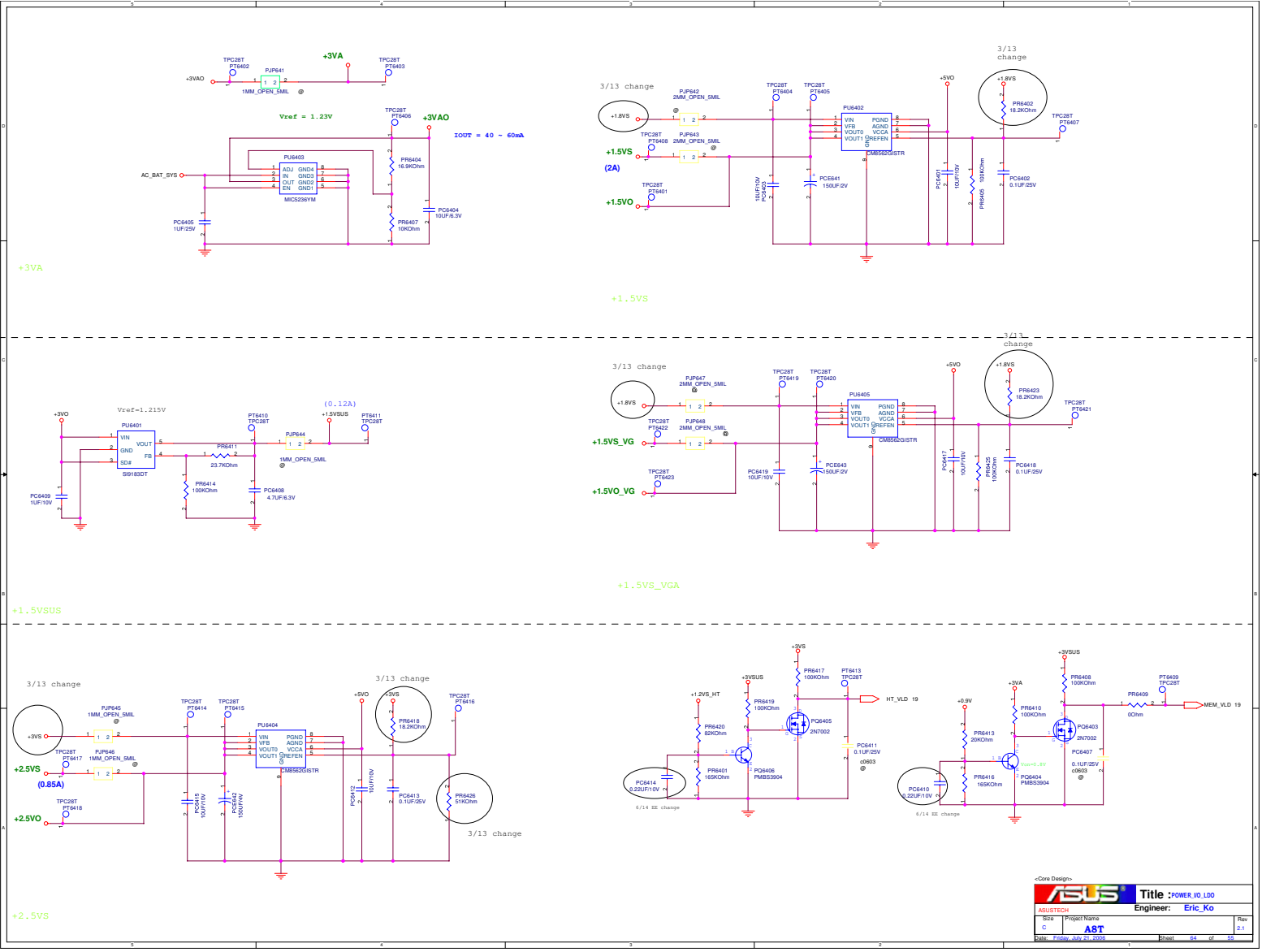


+1.02V	1.21V	1.11V	1.0V
CR_VID0	0	0	1
CR_VID1	0	1	0


+3VA
Vref = 1.23V
IOUT = 40 ~ 60mA
AC_BAT_SYS
MIC5236YM
3/13 change
+1.8VS
+5VO
+1.5VS
(2A)
+1.5VO
CMB522GISTR
+3VA
+1.5VS
Vref=1.215V
(0.12A)
+1.5VSUS
SI9183DT
+1.5VS_VG
+1.5VO_VG
+1.5VSUS
+1.5VS_VGA
+2.5VS
(0.85A)
+2.5VO
+1.2VS_HT
HT_VLD 19
MEM_VLD 19
+0.9V
+3VSUS
6/14 EE change
<Core Design>
ASUSTeK
Title : POWER_IO_LDO
Engineer: Eric_Ko
Size: C
Project Name: A8T
Rev: 2.1
Date: Friday, July 21, 2006
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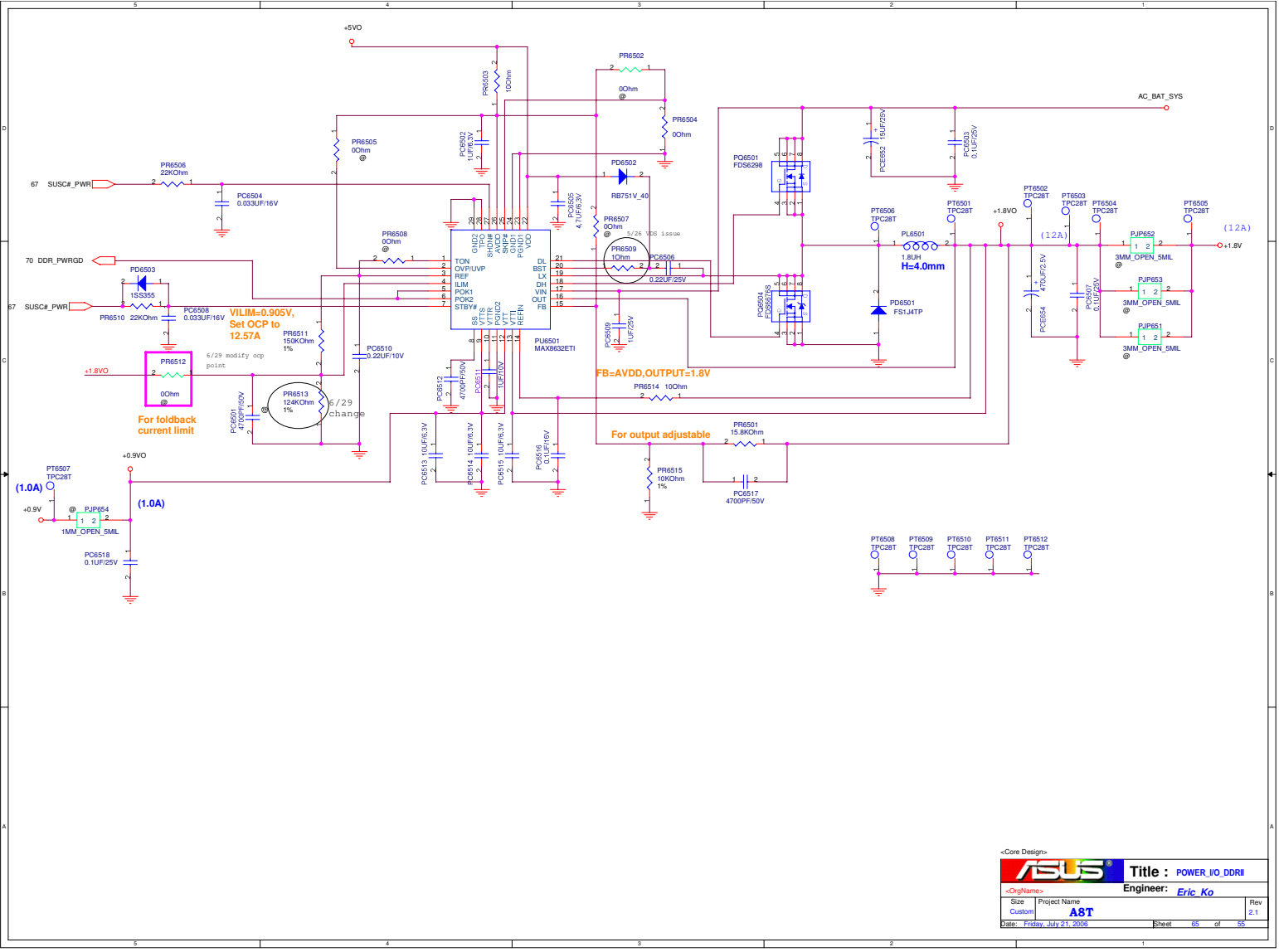

<Core Design>

Title : POWER_I/O_DDRII

<OrgName>

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

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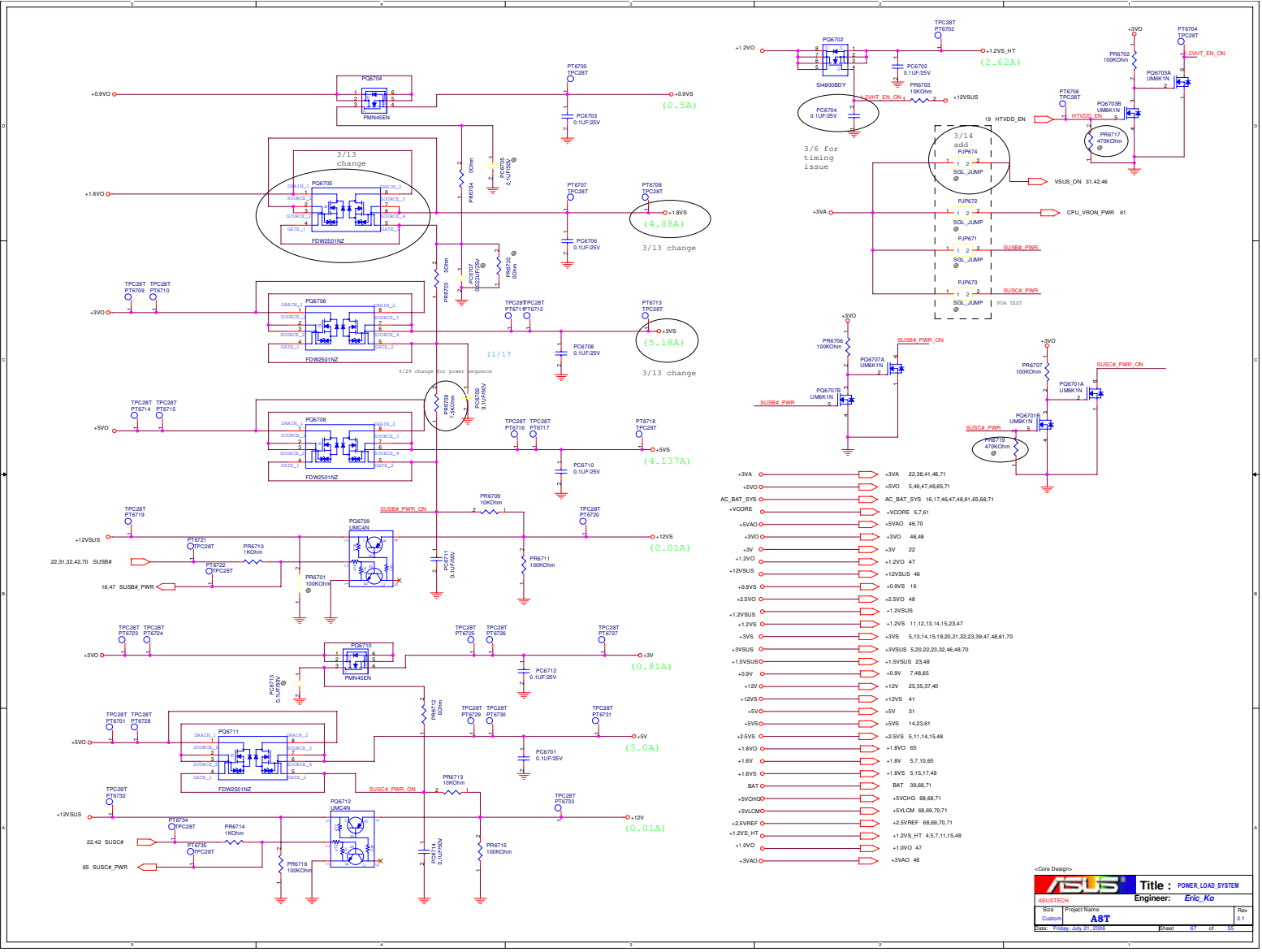
+0.9VO
PQ6704
PMN45EN
PT6705 TPC28T
PC6703 0.1UF/25V
+0.9VS
(0.5A)
3/13 change
+1.8VO
PQ6705
FDW2501NZ
PR6704 0Ohm
PC6705 0.1UF/25V
PT6707 TPC28T
PC6706 0.1UF/25V
PT6708 TPC28T
+1.8VS
(4.08A)
3/13 change
PR6705 0Ohm
PC6707 0.01UF/50V
PR6720 0Ohm
+3VO
TPC28T PT6709
TPC28T PT6710
PQ6706
FDW2501NZ
TPC28T PT6711
TPC28T PT6712
PC6708 0.1UF/25V
PT6713 TPC28T
+3VS
(5.18A)
11/17
6/29 change for power sequence
3/13 change
PR6708 1.5KOhm
PC6709 0.1UF/50V
+5VO
TPC28T PT6714
TPC28T PT6715
PQ6708
FDW2501NZ
TPC28T PT6716
TPC28T PT6717
PT6718 TPC28T
+5VS
(4.137A)
PC6710 0.1UF/25V
PR6709 10KOhm
SUSB#_PWR_ON
+12VSUS
TPC28T PT6719
PT6721 TPC28T
PR6710 1KOhm
22,31,32,42,70 SUSB#
PT6722 TPC28T
16,47 SUSB#_PWR
PR6701 100KOhm
PQ6709 UMC4N
PC6711 0.1UF/50V
PR6711 100KOhm
TPC28T PT6720
+12VS
(0.01A)
+3VO
TPC28T PT6723
TPC28T PT6724
PQ6710
PMN45EN
PC6713 0.1UF/50V
TPC28T PT6725
TPC28T PT6726
PC6712 0.1UF/25V
TPC28T PT6727
+3V
(0.81A)
PR6702 100KOhm
TPC28T PT6729
TPC28T PT6730
PC6701 0.1UF/25V
TPC28T PT6731
+5V
(3.0A)
+5VO
TPC28T PT6701
TPC28T PT6728
PQ6711
FDW2501NZ
SUSC#_PWR_ON
PR6713 10KOhm
+12VSUS
TPC28T PT6732
PT6734 TPC28T
PR6714 1KOhm
22,42 SUSC#
PT6735 TPC28T
65 SUSC#_PWR
PQ6712 UMC4N
PR6715 100KOhm
PC6714 0.1UF/50V
PR6716 100KOhm
TPC28T PT6733
+12V
(0.01A)
+1.2VO
PQ6702
SI4800BDY
TPC28T PT6702
+1.2VS_HT
(2.62A)
PC6702 0.1UF/25V
PR6703 10KOhm
+12VSUS
+1.2VHT_EN_ON
PC6704 0.1UF/25V
3/6 for timing issue
19 HTVDD_EN
3/14 add
PJP674
SGL_JUMP
VSUS_ON 31,42,46
PJP672
SGL_JUMP
CPU_VRON_PWR 61
+3VA
PJP671
SGL_JUMP
SUSB#_PWR
PJP673
SGL_JUMP
FOR TEST
SUSC#_PWR
+3VO
PT6704 TPC28T
+1.2VHT_EN_ON
PR6702 100KOhm
PQ6703A UMBK1N
PT6706 TPC28T
HTVDD_EN
PQ6703B UMBK1N
PR6717 470KOhm
+3VO
PR6706 100KOhm
SUSB#_PWR_ON
PQ6707A UMBK1N
PQ6707B UMBK1N
SUSB#_PWR
+3VO
PR6707 100KOhm
SUSC#_PWR_ON
PQ6701A UMBK1N
PQ6701B UMBK1N
SUSC#_PWR
PR6719 470KOhm
+3VA 22,38,41,48,71
+5VO 5,46,47,48,65,71
AC_BAT_SYS 16,17,46,47,48,61,65,68,71
+VCORE +VCORE 5,7,61
+5VAO 46,70
+3VO 46,48
+3V 22
+1.2VO 47
+12VSUS 46
+0.9VS 16
+2.5VO 48
+1.2VSUS
+1.2VS 11,12,13,14,15,23,47
+3VS 5,13,14,15,19,20,21,22,23,39,47,48,61,70
+3VSUS 5,20,22,23,32,46,48,70
+1.5VSUS 23,48
+0.9V 7,48,65
+12V 25,35,37,40
+12VS 41
+5V 31
+5VS 14,23,61
+2.5VS 5,11,14,15,48
+1.8VO 65
+1.8V 5,7,10,65
+1.8VS 5,15,17,48
BAT 39,68,71
+5VCHG 68,69,71
+5VLCM 68,69,70,71
+2.5VREF 68,69,70,71
+1.2VS_HT 4,5,7,11,15,48
+1.0VO 47
+3VAO 48
<Core Design>
Title : POWER_LOAD_SYSTEM
ASUSTECH
Engineer: Eric_Ko
Size Custom
Project Name A8T
Rev 2.1
Date: Friday, July 21, 2006
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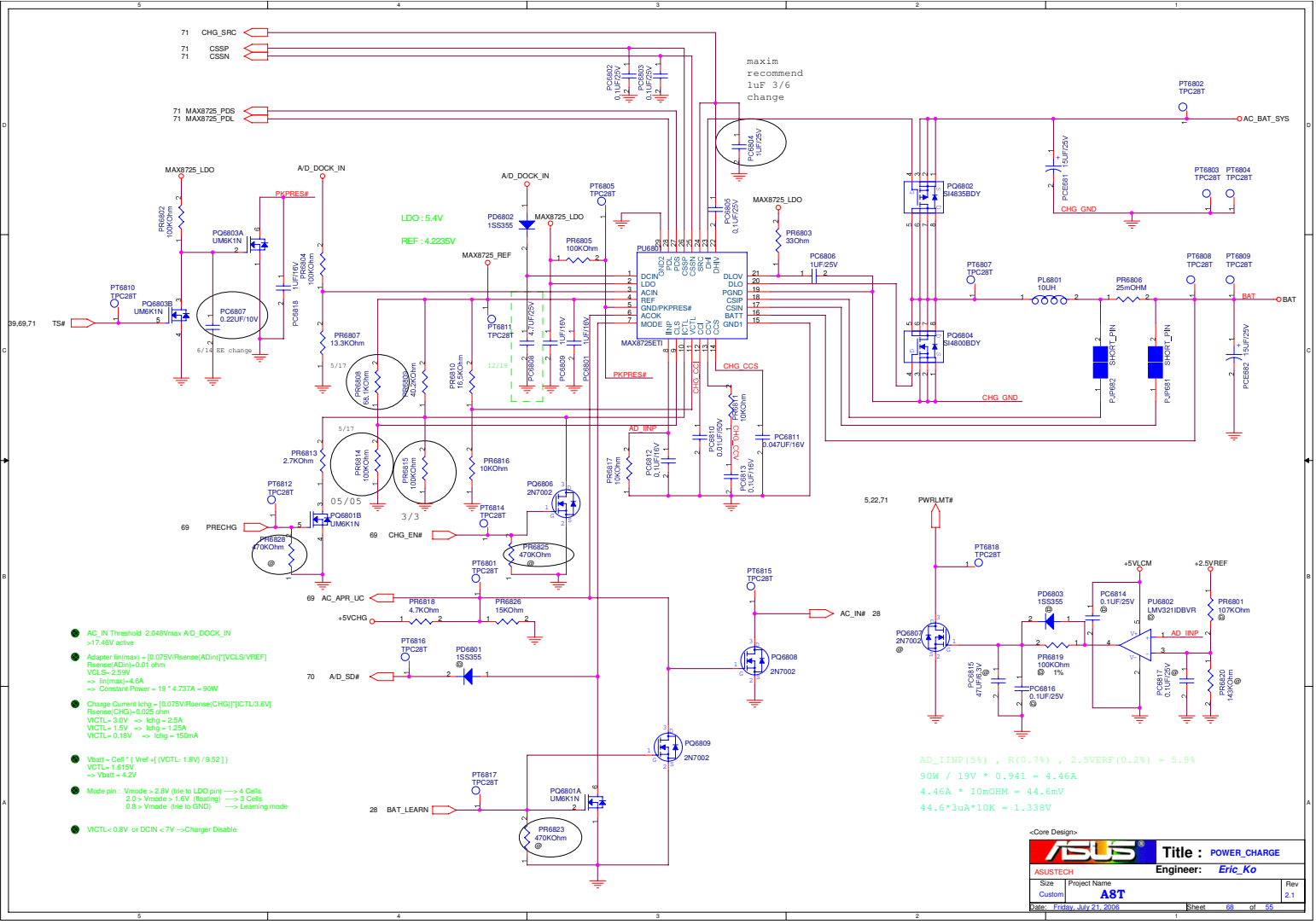
71 CHG_SRC
71 CSSP
71 CSSN
71 MAX8725_PDS
71 MAX8725_PDL
maxim recommend 1uF 3/6 change
AC_BAT_SYS
MAX8725_LDO
A/D_DOCK_IN
PKPRES#
LDO : 5.4V
REF : 4.2235V
MAX8725_REF
PU6801
MAX8725ETI
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
PQ6802 SI4835BDY
PQ6804 SI4800BDY
CHG_GND
PL6801 10UH
PR6806 25mOHM
BAT
SHORT_PIN
PJP681
PJP682
PC6862 15UF/25V
39,69,71 TS#
PQ6803B UM6K1N
PQ6803A UM6K1N
PC6807 0.22UF/10V
PR6807 13.3KOhm
PR6808 68.1KOhm
PR6809 40.2KOhm
PR6810 16.5KOhm
PC6808
PC6809
PC6801
CHG_CCS
CHG_CCI
AD_IINP
PC6810 0.01UF/50V
PC6811 0.047UF/16V
PC6812 0.1UF/16V
PC6813 0.1UF/16V
PR6817 10KOhm
PR6813 2.7KOhm
PR6814 100KOhm
PR6815 100KOhm
PR6816 10KOhm
PQ6806 2N7002
69 PRECHG
PQ6801B UM6K1N
PR6826 470KOhm
69 CHG_EN#
PR6825 470KOhm
69 AC_APR_UC
PR6818 4.7KOhm
PR6826 15KOhm
+5VCHG
70 A/D_SD#
PD6801 1SS355
PQ6809 2N7002
28 BAT_LEARN
PQ6801A UM6K1N
PR6823 470KOhm
AC_IN# 28
PQ6808 2N7002
5,22,71 PWRLMT#
PQ6807 2N7002
PD6803 1SS355
PC6814 0.1UF/25V
PU6802 LMV321IDBVR
PR6819 100KOhm 1%
PC6816 0.1UF/25V
PC6815 47UF/6.3V
PC6817 0.1UF/25V
PR6820 140KOhm
PR6801 107KOhm
+5VLCM
+2.5VREF
AD_IINP(5%) , R(0.7%) , 2.5VERF(0.2%) = 5.9%
90W / 19V * 0.941 = 4.46A
4.46A * 10mOHM = 44.6mV
44.6*3uA*10K = 1.338V
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.46V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm
VCLS= 2.59V
=> Iin(max)=4.6A
=> Constant Power = 19 * 4.737A = 90W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.0V => Ichg = 2.5A
VICTL= 1.5V => Ichg = 1.25A
VICTL= 0.18V => Ichg = 150mA
Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.615V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
<Core Design>
ASUSTECH
Title : POWER_CHARGE
Engineer: Eric_Ko
Size: Custom
Project Name: A8T
Rev: 2.1
Date: Friday, July 21, 2006
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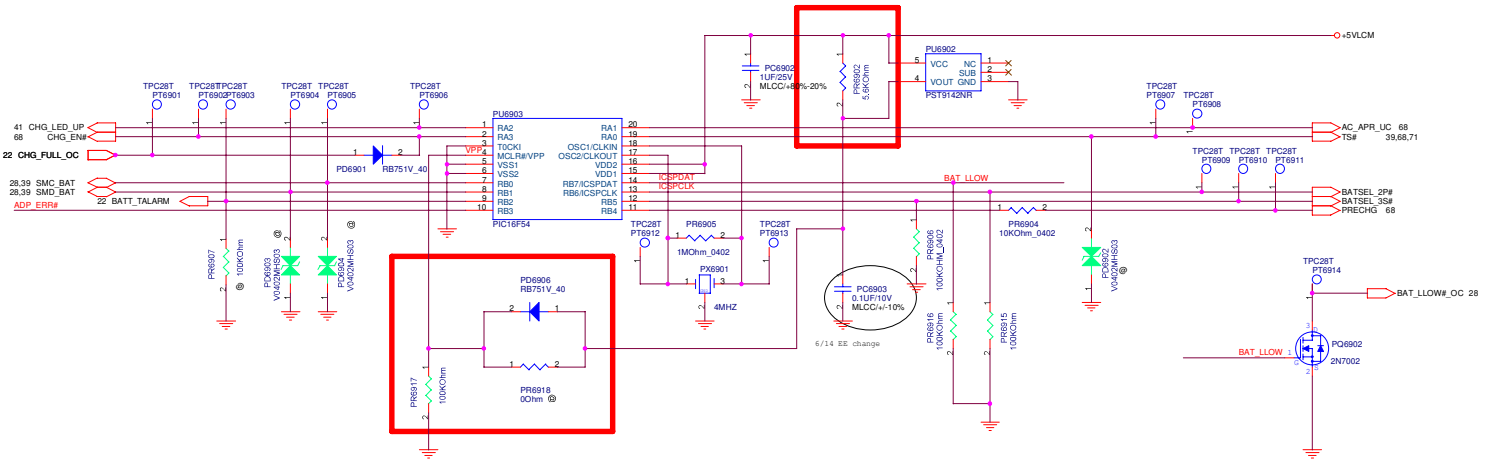
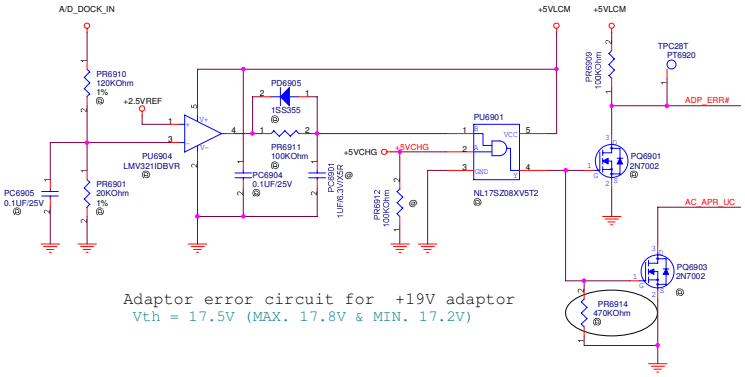
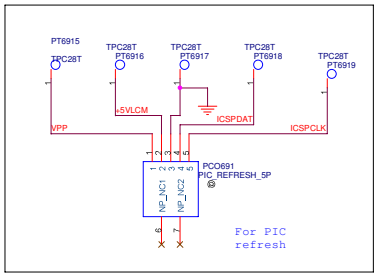
PIC16F54



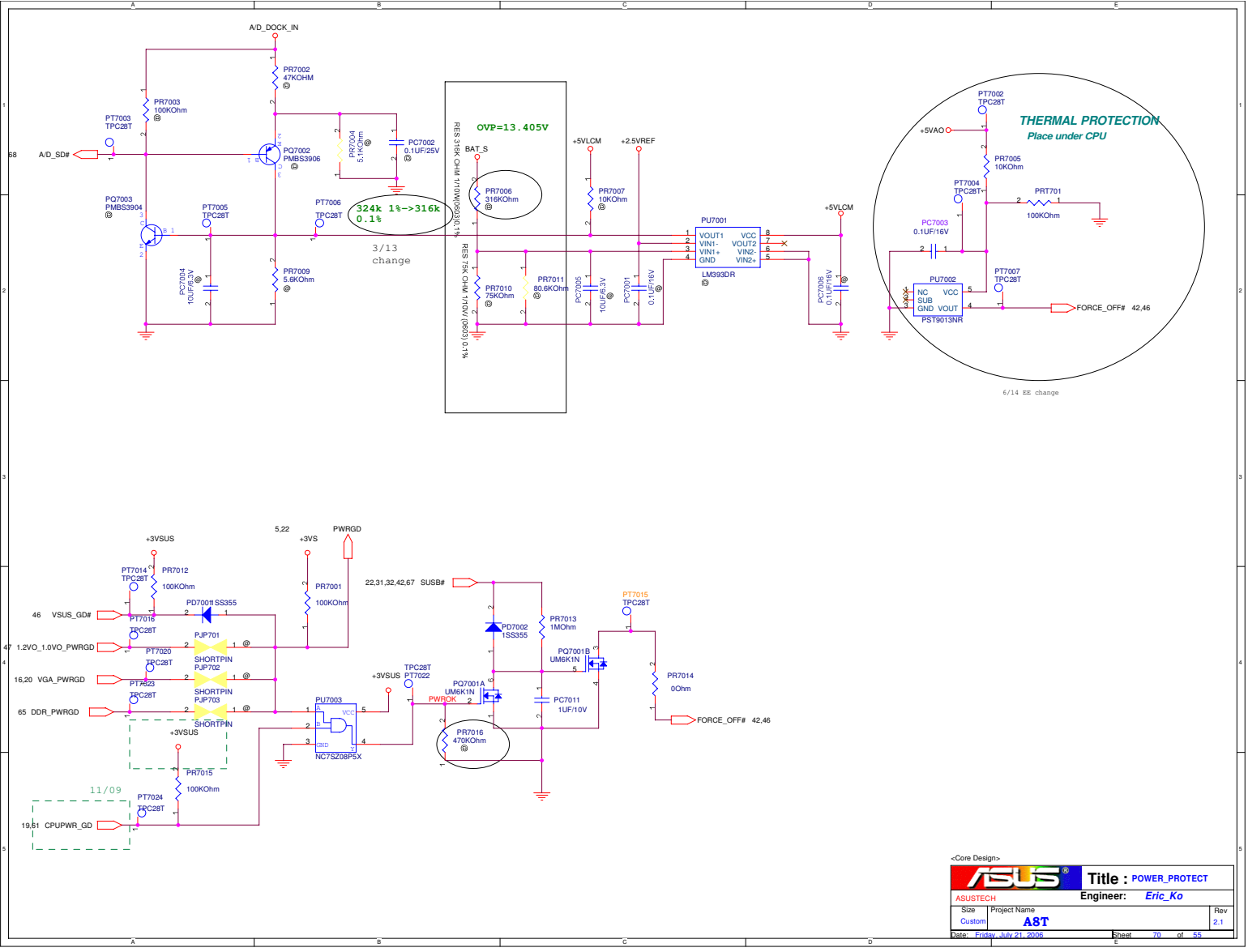


Adaptor error circuit for +19V adaptor
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)



<Core Design>

<OrgName>	Title : POWER_PIC	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 69 of 55	



<Core Design>

ASUSTECH

Title : POWER_PROTECT

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

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