Compal Confidential

QCL40 MB Schematic Document

LA-8221P

Rev: 0.2

2011.09.28

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Cover Sheet		
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QCL40

ZZZ1
PCB-MB
PCB P/N for Load BOM

NV N13P-GL
(N13M-GE1)
Page 20 ~ 28

PEG 16X

Mobile
Ivy Bridge
Processor
rPGA 988B Socket
Page 4 ~ 9
+VCC_CORE, +VCCP,
+VCC_GFXCORE_AVG, +1.5V_CPU_VDDQ,
+1.8VS, _VCCSA

DDR3 1333/1600MHz 1.5V
Dual Channel

DDR3-SO-DIMM X 2
BANK 0, 1, 2, 3
+1.5V, +0.75VS
Page 10, 11

FDI x8
(UMA)
100MHz
2.7GT/s

DMI x4
100MHz
5GB/s

LCD conn
Page 30
LVDS, EDID, DISPOFF#, PWM

CRT Conn
Page 30
RGB, HV Sync, DDC

HDMI
Page 35
HDMI, DDC

Intel
PANTHER-POINT
PCH

HM77

FCBGA 989 Balls
Page 12 ~ 19

+1.05VS, +1.8VS, +3VS,
+3V_PCH, +5V_PCH, +RTCVCC,
+VCCAFDI_VRM

USB2.0

port 4
USB conn x1
USB Board Page 33

port 8
Camera
Page 30

port 10
Card Reader
RTS5137
Page 34

Memory Card Slot
SD/MMC
Page 34

port 9
MiniCard-2
Page 40

USB3.0

port 0,1
port 1,2
USB3.0 conn x2
Page 36

Azalia

Realtek
ALC269
Page 33

Audio Jack (HP)
Page 33

Audio Jack (MIC)
Page 33

Speaker Connector
Page 33

SATA

port 0
2.5" SATA HDD Connector
Page 31

port 2
SATA ODD Connector
Page 31

SPI

SPI ROM
4MB+2MB
Page 12

PCI-e

port 1
LAN/CRT Board
10/100/1000 LAN
Realtek GbE
RTL8111F
Page 32

port 2
Mini Card-1
WLAN
Bluetooth
Page 40

LPC BUS

Touch Pad CONN.
Page 38

ENE KB9012QF
Reserve KB930F
+3VLP/+3VALW
page 39

Int. KBD
Page 38

SPI ROM
256KB
Page 39

External board

DC/DC Interface CKT.
Page 29,41

LS-4221P
USB/B
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Fan Control
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Title: Block Diagram

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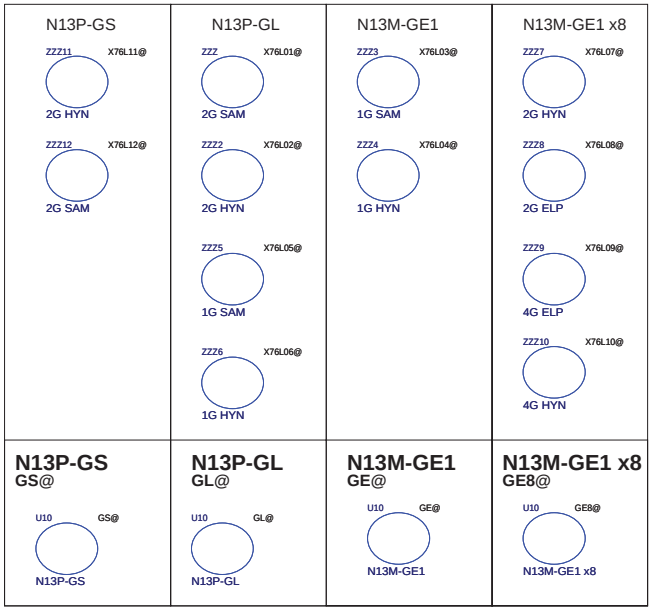
X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GEL@: N13P-GL or N13M-GE1
GSL@: N13P-GL or N13P-GS
GS@: N13P-GS

9012@: EC(ENE 9012 chip)

930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

	USB3 PORT	DESTINATION
PCH	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

	USB2 PORT	DESTINATION
PCH	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 51ON power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

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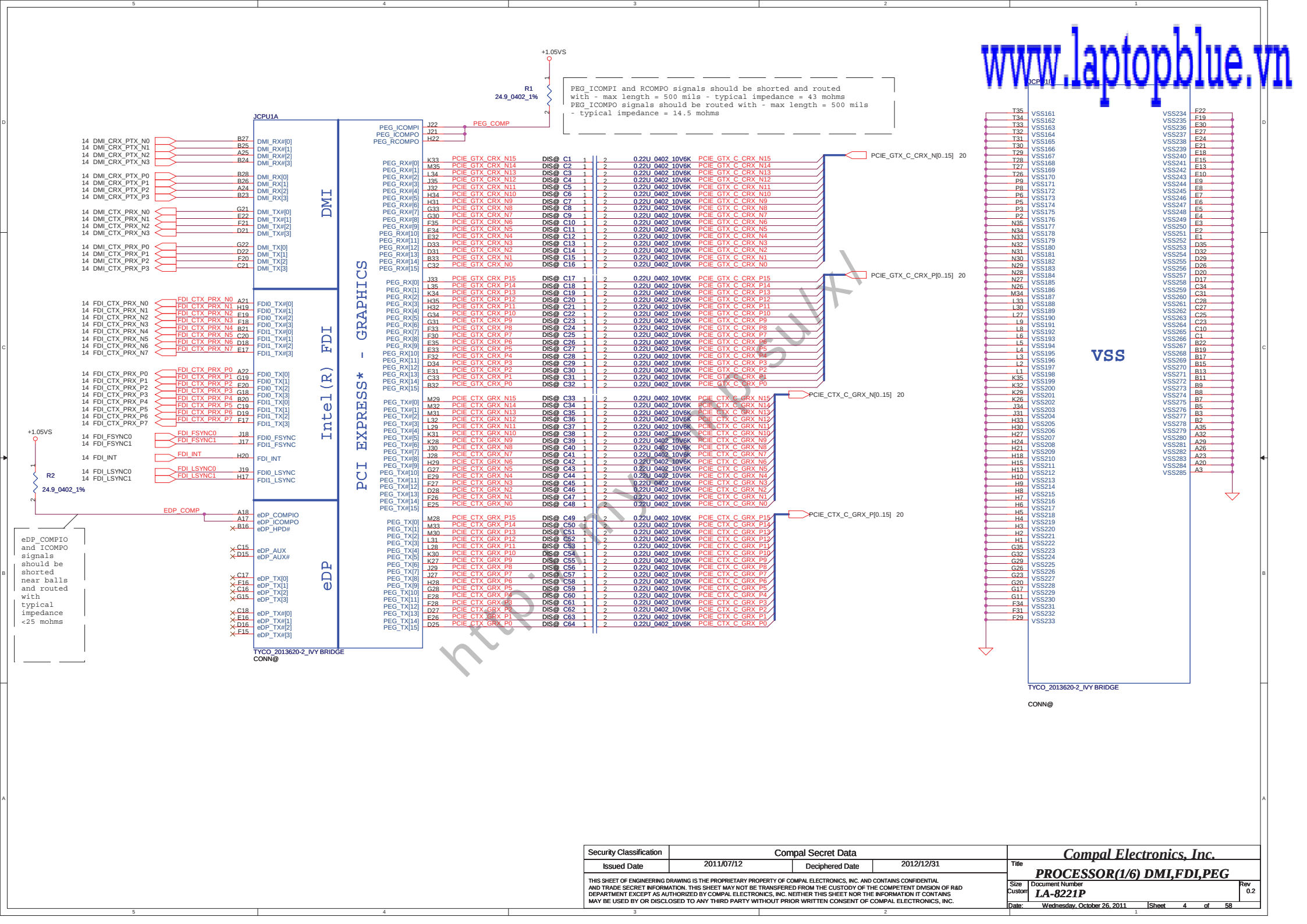

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Title: PROCESSOR(1/6) DMI,FDI,PEG

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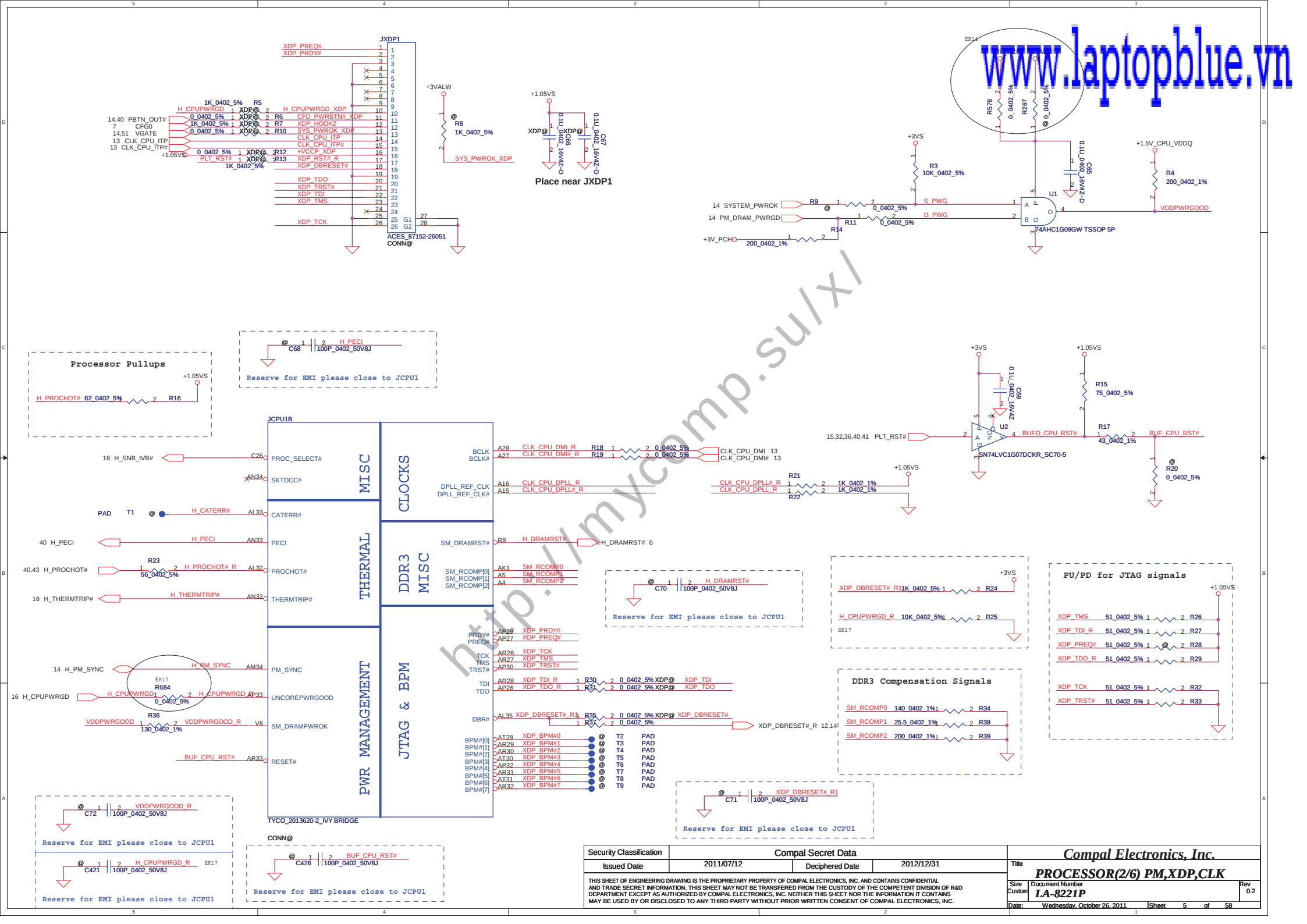

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Compal Electronics, Inc.

Title: PROCESSOR(2/6) PM,XDP,CLK

Size	Document Number	Rev
Custom	LA-8221P	0.2

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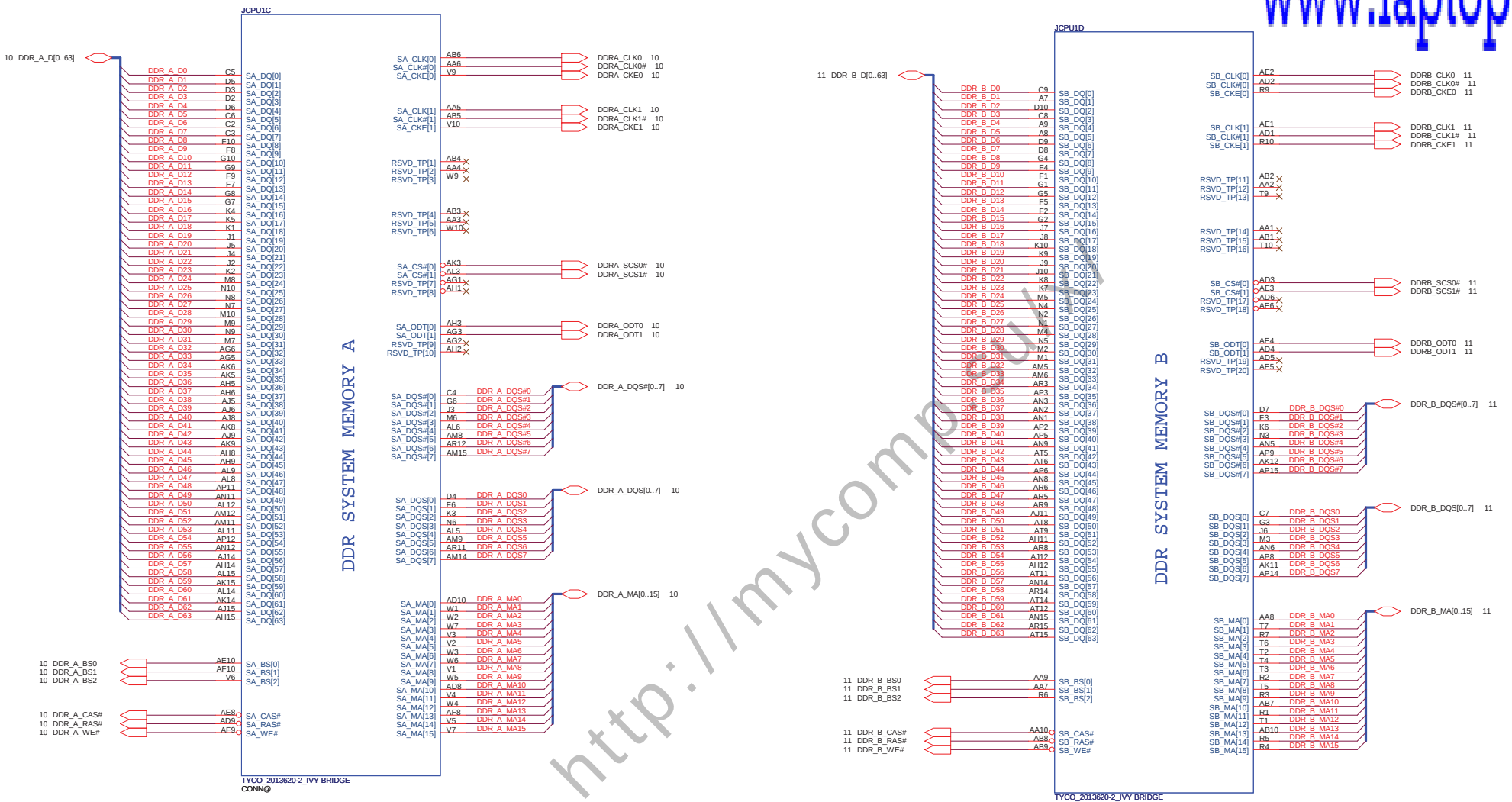

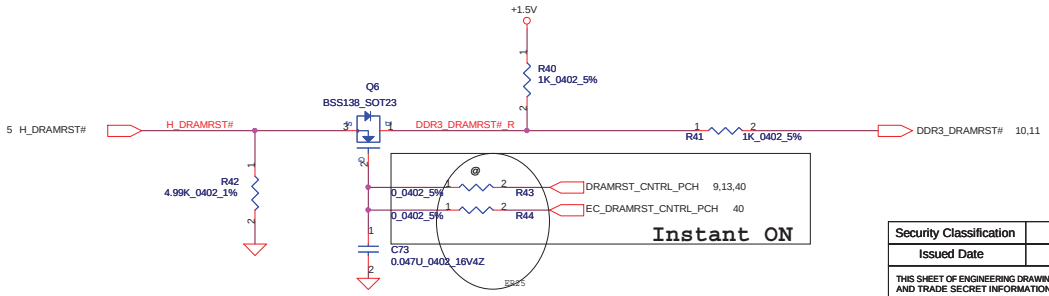

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Compal Electronics, Inc.

Title: PROCESSOR(3/6) DDRIII

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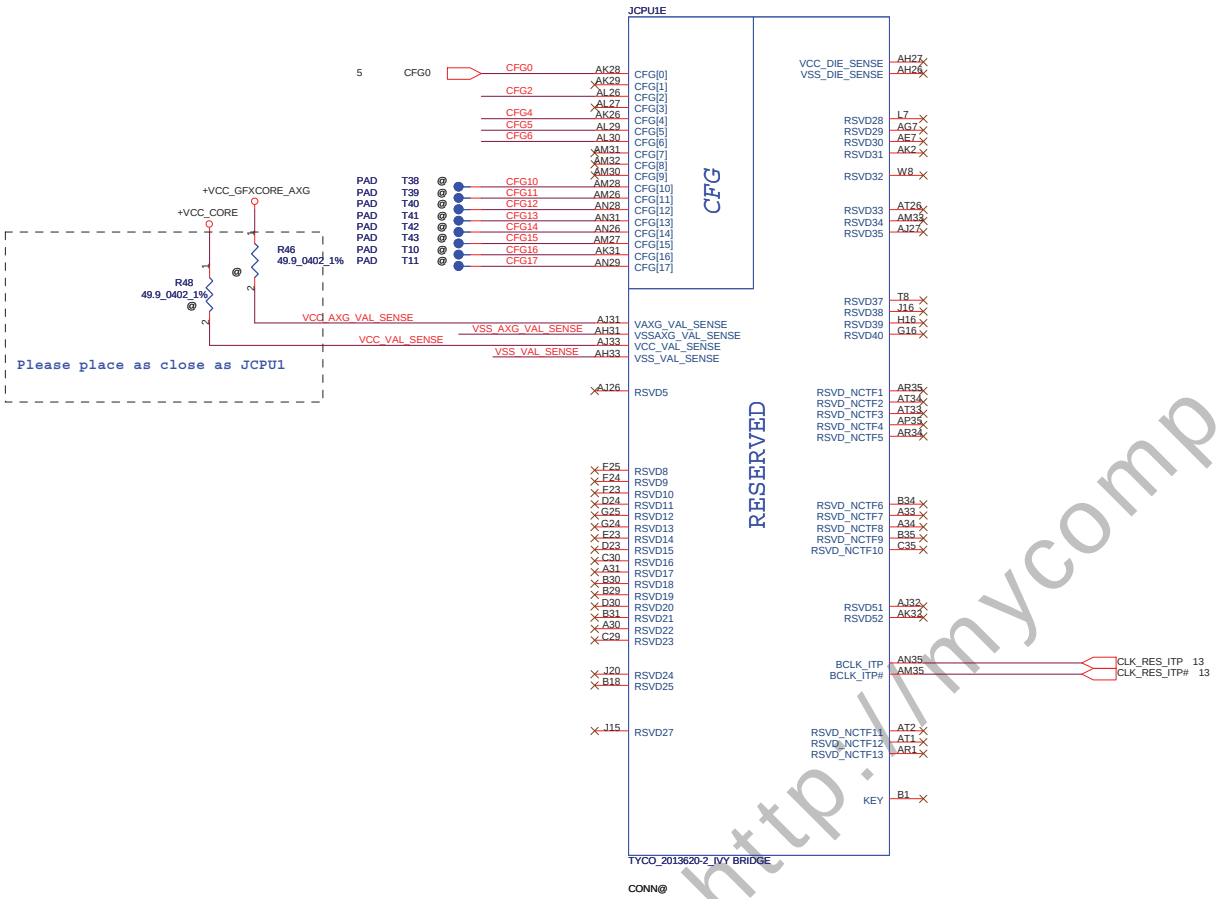
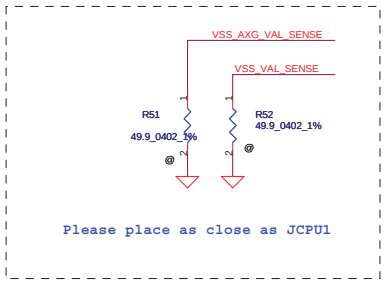
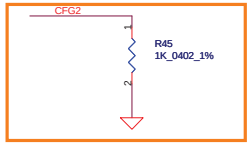
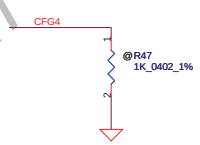
CFG Straps for Processor



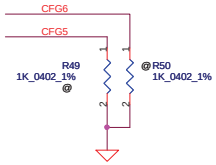




PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: PROCESSOR(4/6) RSVD,CFG

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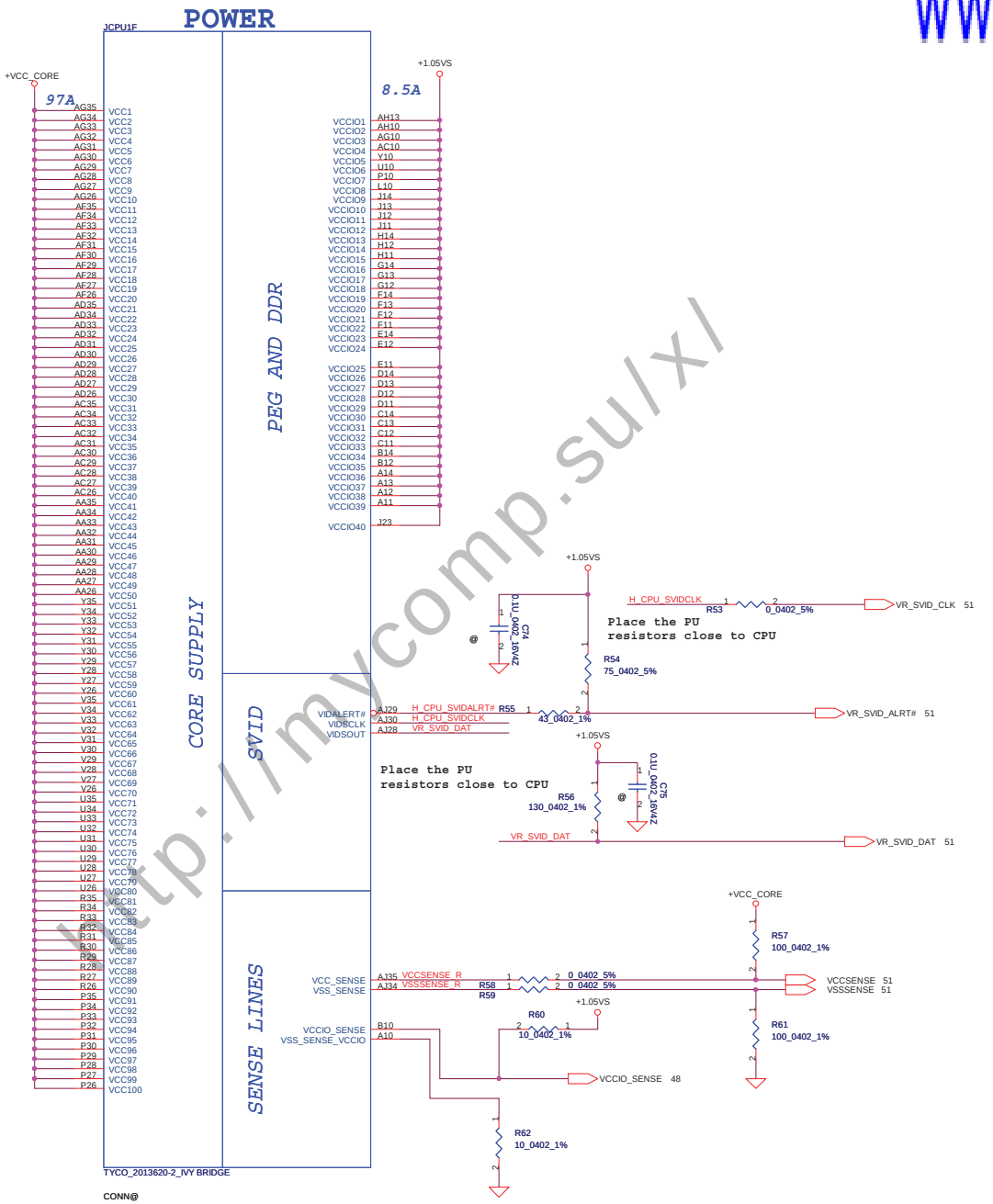

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Title: PROCESSOR(5/6) PWR,BYPASS

Size	Document Number	Rev
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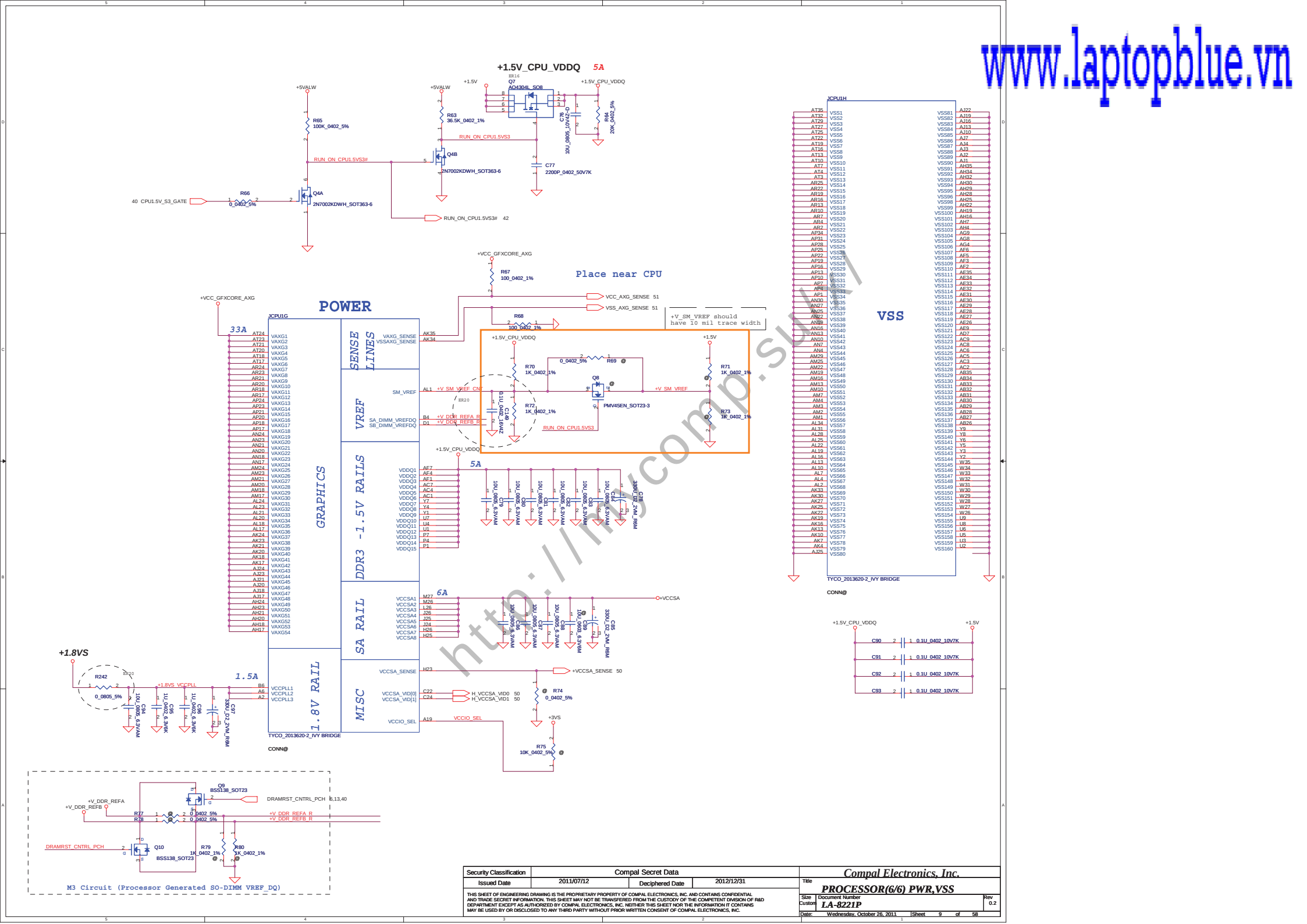

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Title: PROCESSOR(6/6) PWR,VSS

Size	Document Number	Rev
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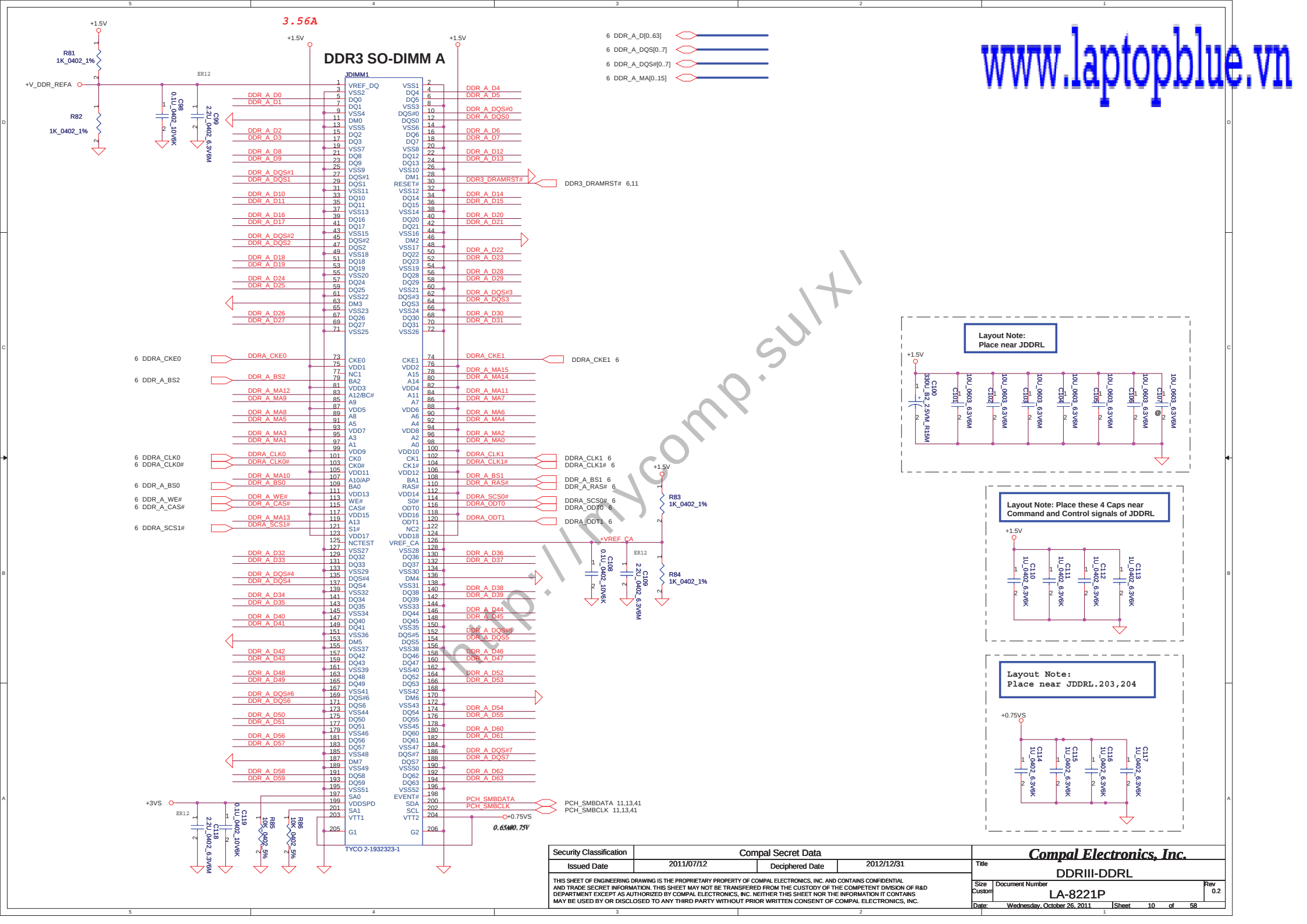

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Compal Electronics, Inc.

Title: DDRIII-DDRL

Size	Document Number	Rev
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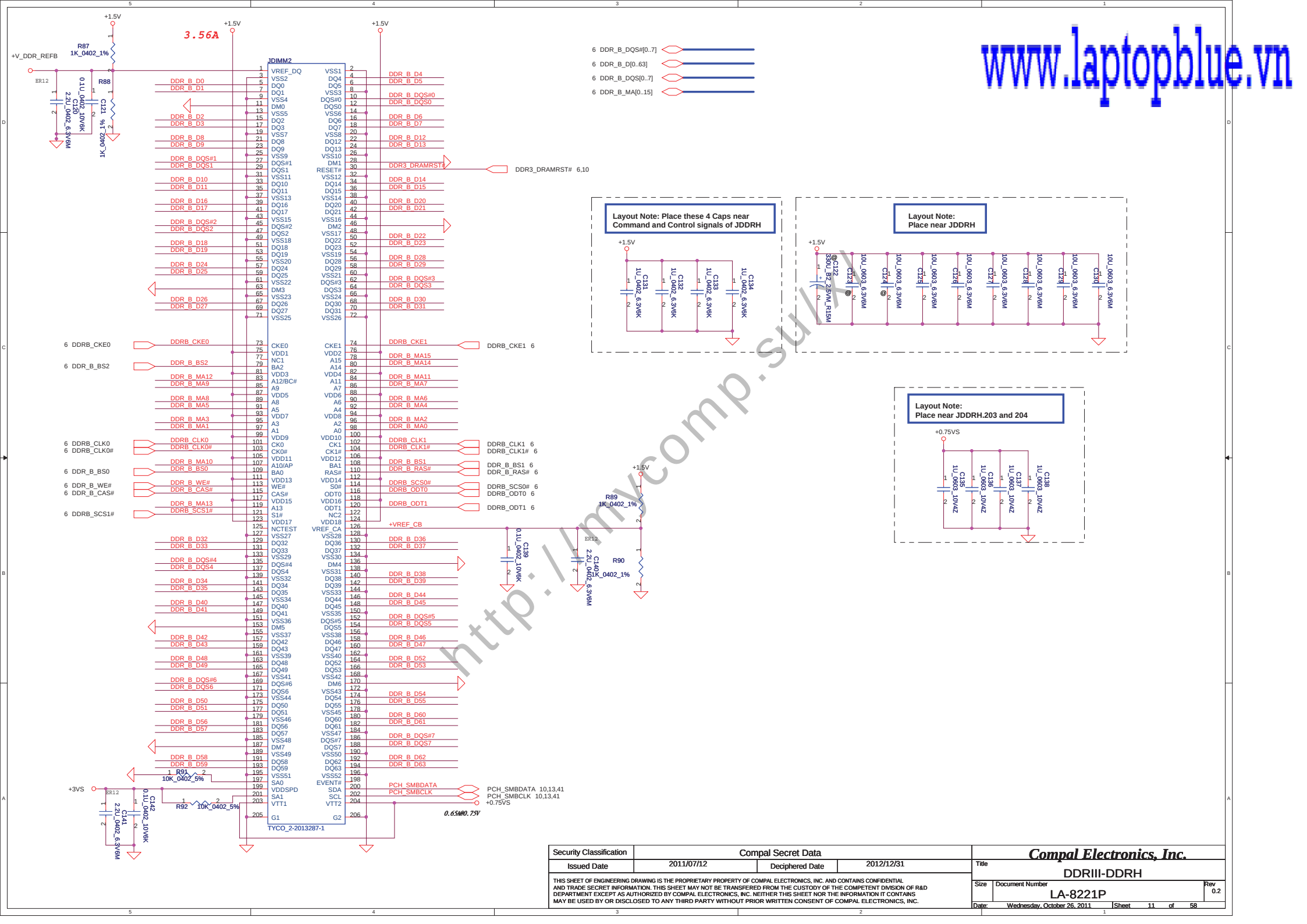

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Title	DDRIII-DDRH		
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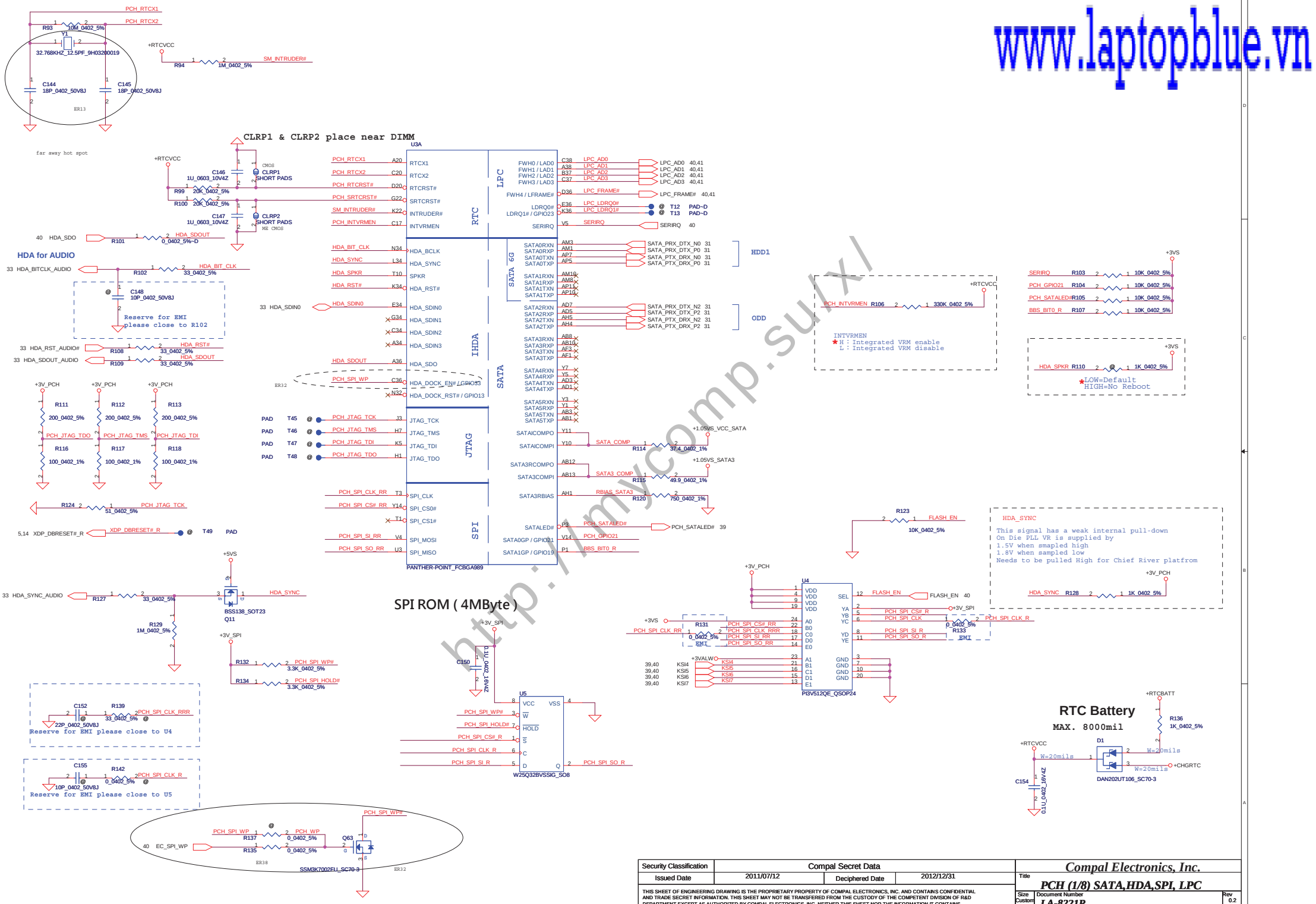

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Title: PCH (1/8) SATA,HDA,SPI, LPC

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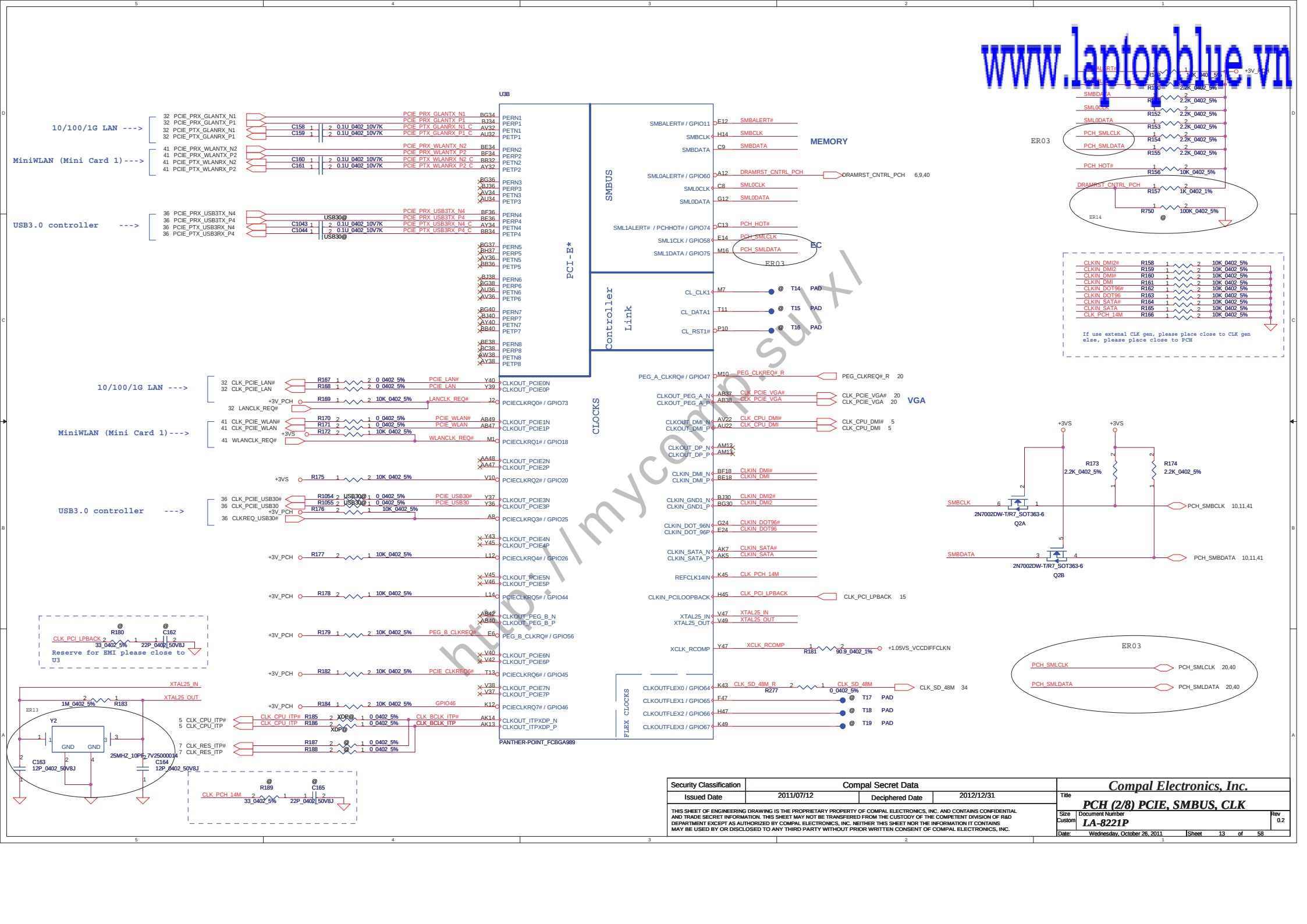

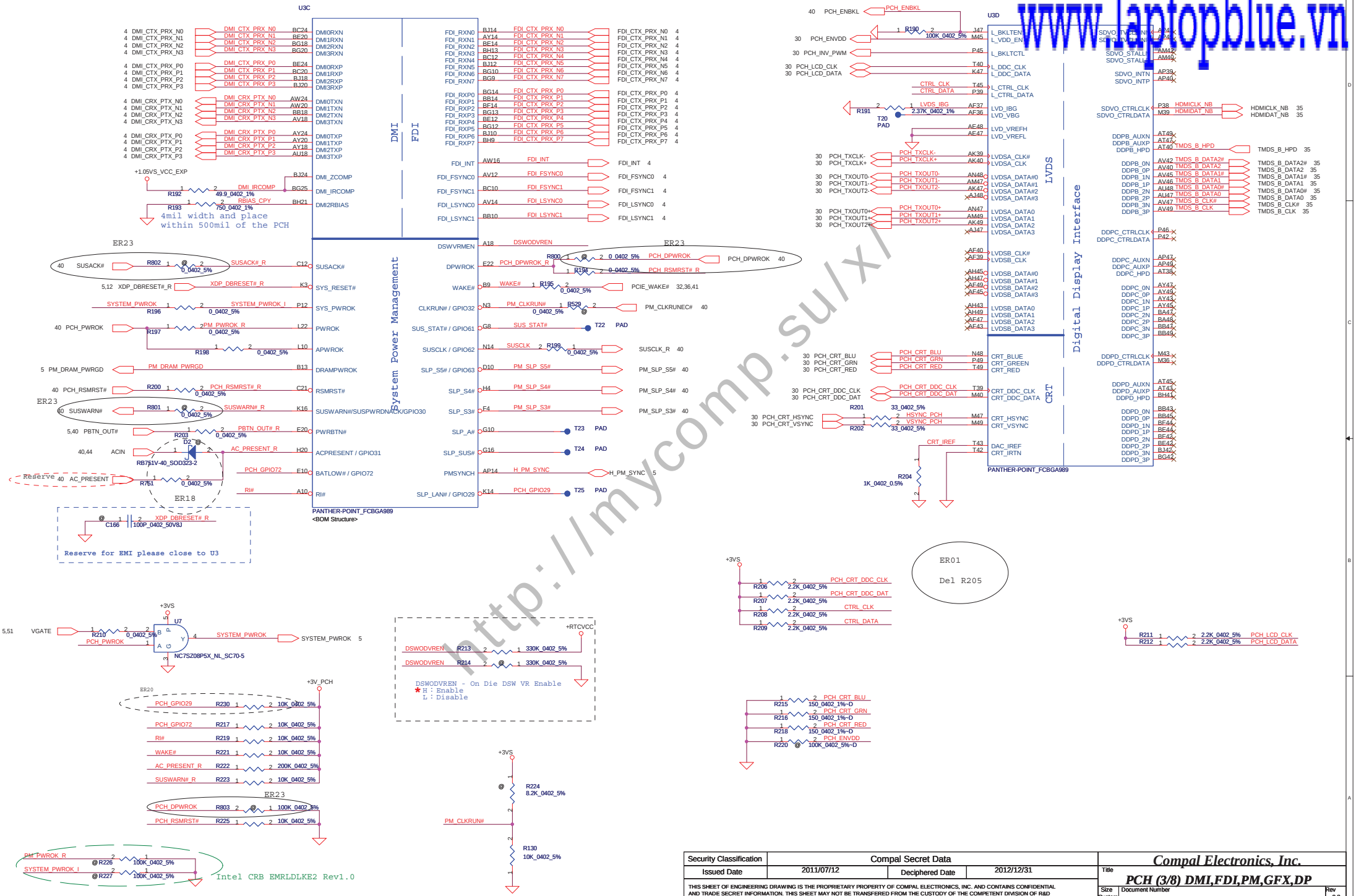

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Title: PCH (3/8) DMI,FDI,PM,GFX,DP

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GPIO19 => [illegible]
GPIO51 => [illegible]

Boot BIOS Strap

BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI *

Intel Anti-Theft Techonlogy

NV_ALE	High=Endabled Low=Disable(floating) *

+1.8VS
NV_ALE @R228 1 2 1K_0402_5%

Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

U3E

RSVD
RSVD1 AY7
RSVD2 AV7
RSVD3 AU3
RSVD4 BG4
RSVD5 AT10
RSVD6 BC8
RSVD7 AU2
RSVD8 AT4
RSVD9 AT3
RSVD10 AT1
RSVD11 AY3
RSVD12 AT5
RSVD13 AV3
RSVD14 AV1
RSVD15 BB1
RSVD16 BA3
RSVD17 BB5
RSVD18 BB3
RSVD19 BB7
RSVD20 BE8
RSVD21 BD4
RSVD22 BF6
RSVD23 AV5 NV_ALE
RSVD24 AV10
RSVD25 AT8
RSVD26 AY5
RSVD27 BA2
RSVD28 AT12
RSVD29 BF3

TP1 BG26
TP2 BJ26
TP3 BH25
TP4 BJ16
TP5 BG16
TP6 AH38
TP7 AH37
TP8 AK43
TP9 AK45
TP10 C18
TP11 N30
TP12 H3
TP13 AH12
TP14 AM4
TP15 AM5
TP16 Y13
TP17 K24
TP18 L24
TP19 AB46
TP20 AB45
TP21 B21
TP22 M20
TP23 AY16
TP24 BG46

USB3
USB3Rn1 BE28
USB3Rn2 BC30
USB3Rn3 BE32
USB3Rn4 BJ32
USB3Rp1 BC28
USB3Rp2 BE30
USB3Rp3 BF32
USB3Rp4 BG32
USB3Tn1 AY26
USB3Tn2 BB26
USB3Tn3 AU28
USB3Tn4 AY30
USB3Tp1 AU26
USB3Tp2 AY26
USB3Tp3 AV28
USB3Tp4 AW30

37 USB3_RX1_N
37 USB3_RX2_N
37 USB3_RX1_P
37 USB3_RX2_P
37 USB3_TX1_N
37 USB3_TX2_N
37 USB3_TX1_P
37 USB3_TX2_P

USB
USBP0N C24 USB20_N0 — USB20_N0 37
USBP0P A24 USB20_P0 — USB20_P0 37 — USB2/3 port 1
USBP1N C25 USB20_N1 — USB20_N1 37
USBP1P B25 USB20_P1 — USB20_P1 37 — USB2/3 port 2
USBP2N C26
USBP2P A26
USBP3N K28
USBP3P H28
USBP4N E28 USB20_N4 — USB20_N4 41
USBP4P D28 USB20_P4 — USB20_P4 41 — Mini Card(WLAN) Bluetooth
USBP5N C28
USBP5P A28
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
HM76 not Support USB Port6,7
USBP8N L30 USB20_N8 — USB20_N8 30
USBP8P K30 USB20_P8 — USB20_P8 30 — Camera
USBP9N G30 USB20_N9 — USB20_N9 33
USBP9P E30 USB20_P9 — USB20_P9 33 — USB2 Conn. R
USBP10N C30 USB20_N10 — USB20_N10 34
USBP10P A30 USB20_P10 — USB20_P10 34 — Card Reader
USBP11N L32
USBP11P K32
USBP12N G32
USBP12P E32
USBP13N C32
USBP13P A32
USBRBIAS# C33 USBRBIAS
USBRBIAS B33

Within 500 mils
R231 22.6_0402_1%

PCI
PCI_PIRQA# K40 PIRQA#
PCI_PIRQB# K38 PIRQB#
PCI_PIRQC# H38 PIRQC#
PCI_PIRQD# G38 PIRQD#
DGPU_HOLD_RST# C46 REQ1# / GPIO50
PCH_GPIO52 C44 REQ2# / GPIO52
20,29,54 DGPU_PWR_EN DGPU_PWR_EN E40 REQ3# / GPIO54
D47 GNT1# / GPIO51
41 PCH_WAN_RADIO_OFF# PCH_WAN_RADIO_OFF# F46 GNT2# / GPIO53
E42 GNT3# / GPIO55
PCH_GPIO2 G42 PIRQE# / GPIO2
31 ODD_DA# ODD_DA# G40 PIRQF# / GPIO3
PCH_GPIO4 C42 PIRQG# / GPIO4
PCH_GPIO5 D44 PIRQH# / GPIO5
PAD T26 @ K10 PME#
PCH_PLTRST# C6 PLTRST#

C167 @ 1 2 0.1U_0402_16V4Z~D ODD_DA#
Reserve for EMI please close to U3

13 CLK_PCI_LPBACK CLK_PCI_LPBACK R232 2 1 22_0402_5% CLK_PCI0
40 CLK_PCI_LPC CLK_PCI_LPC R233 1 2 22_0402_5% CLK_PCI1
41 CLK_LPC_DEBUG1 CLK_LPC_DEBUG1 R234 1 2 22_0402_5% CLK_PCI3
CLKOUT_PCI0 H49
CLKOUT_PCI1 H43
CLKOUT_PCI2 J48
CLKOUT_PCI3 K42
CLKOUT_PCI4 H40

OC0# / GPIO59 A14 USB_OC0# — USB_OC0# 37 (For USB Port0, 1)
OC1# / GPIO40 K20 USB_OC1#
OC2# / GPIO41 B17 USB_OC2#
OC3# / GPIO42 C16 USB_OC3#
OC4# / GPIO43 L16 USB_OC4# — USB_OC4# 37 (For USB Port9)
OC5# / GPIO9 A16 USB_OC5#
OC6# / GPIO10 D14 USB_OC6#
OC7# / GPIO14 C14 USB_OC7#

PANTHER-POINT_FCBGA989

ER11
+3V_PCH
USB_OC0# 10K_0402_5% R776
USB_OC2# 10K_0402_5% R777
USB_OC7# 10K_0402_5% R778
USB_OC5# 10K_0402_5% R779
USB_OC6# 10K_0402_5% R780
USB_OC4# 10K_0402_5% R781
USB_OC3# 10K_0402_5% R782
USB_OC1# 10K_0402_5% R783

Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13

ER11
+3VS
PCH_GPIO4 8.2K_0402_5% R784
PCI_PIRQB# 8.2K_0402_5% R785
PCI_PIRQD# 8.2K_0402_5% R786
PCI_PIRQC# 8.2K_0402_5% R787
PCH_WAN_RADIO_OFF# 8.2K_0402_5% R788
PCI_PIRQA# 8.2K_0402_5% R789
ODD_DA# 8.2K_0402_5% R790
PCH_GPIO5 8.2K_0402_5% R791
PCH_GPIO52 8.2K_0402_5% R792
PCH_GPIO2 8.2K_0402_5% R793
DGPU_HOLD_RST# R244 10K_0402_5%
DGPU_PWR_EN R288 10K_0402_5%
@
ER20

+3VS
@ R238 10K_0402_5%
5,32,36,40,41 PLT_RST#
U8
VCC IN1 OUT IN2 GND
MC74VHC1G08DFT2G_SC70-5
R235 @ 1 2 0_0402_5%
C168 1 2 0.1U_0402_16V4Z~D
PCH_PLTRST#
R243 100K_0402_5%

R236 @ 1 2 0_0402_5%
C169 DIS@ 1 2 0.1U_0402_16V4Z~D
U9
VCC B PCH_PLTRST#
Y A DGPU_HOLD_RST#
GND
NC7SZ08P5X_NL_SC70-5
20 DGPU_RST#
DIS@ R240 1 2 100_0402_5%
R241 100K_0402_5% DIS@

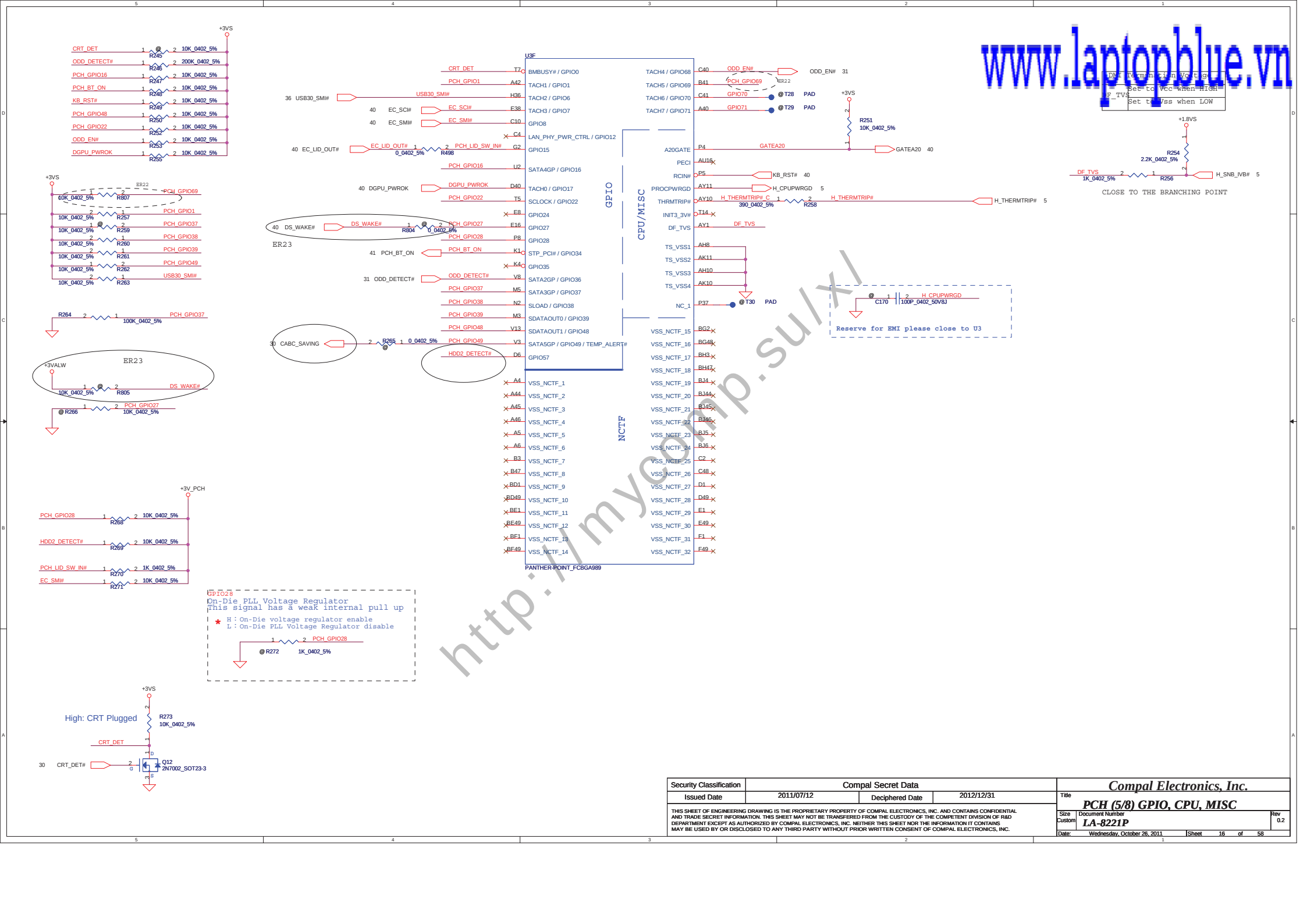
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 15 of 58



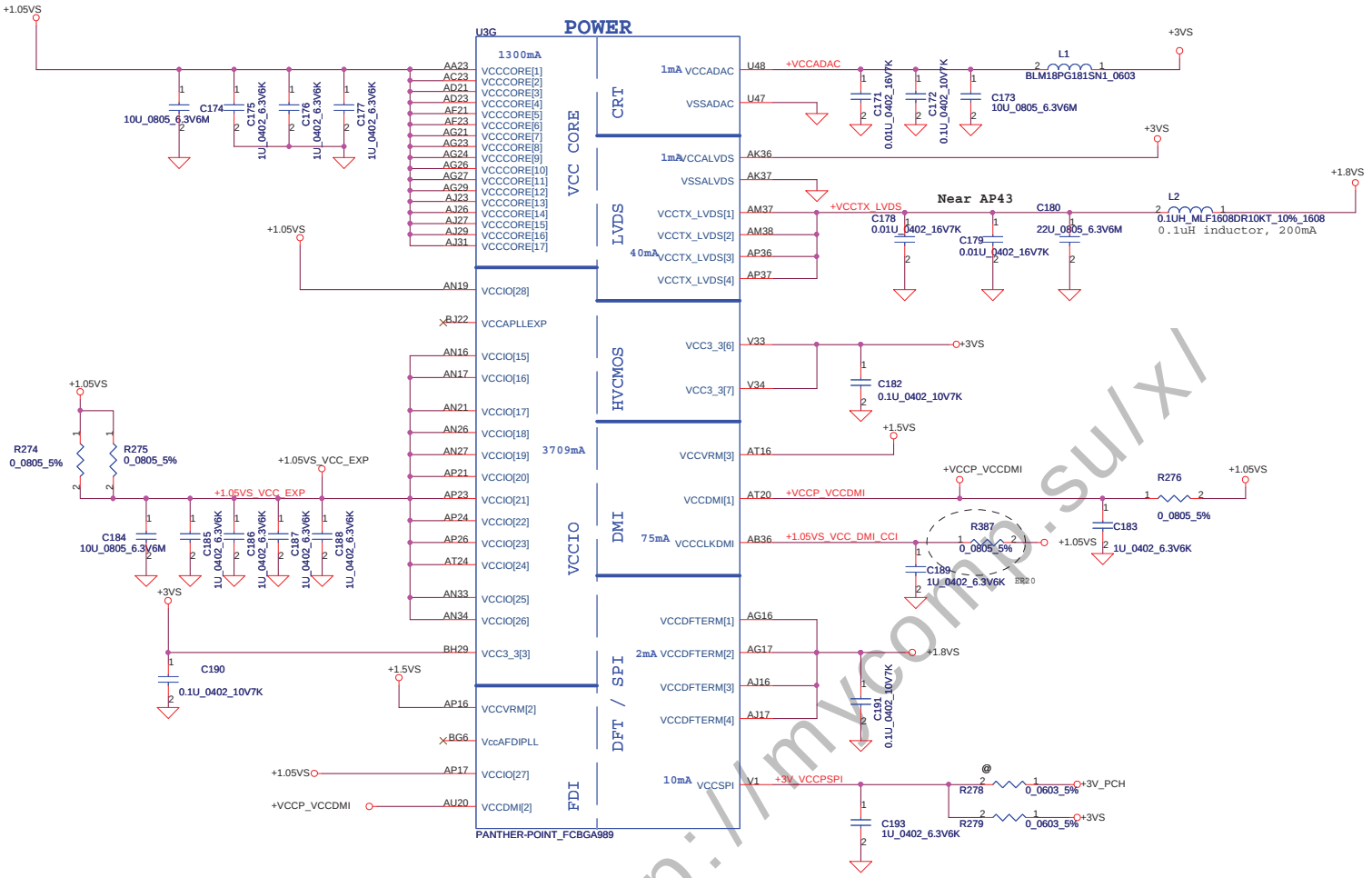
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 16 of 58



PCH Power Rail Table Refer to CPU EDS V1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

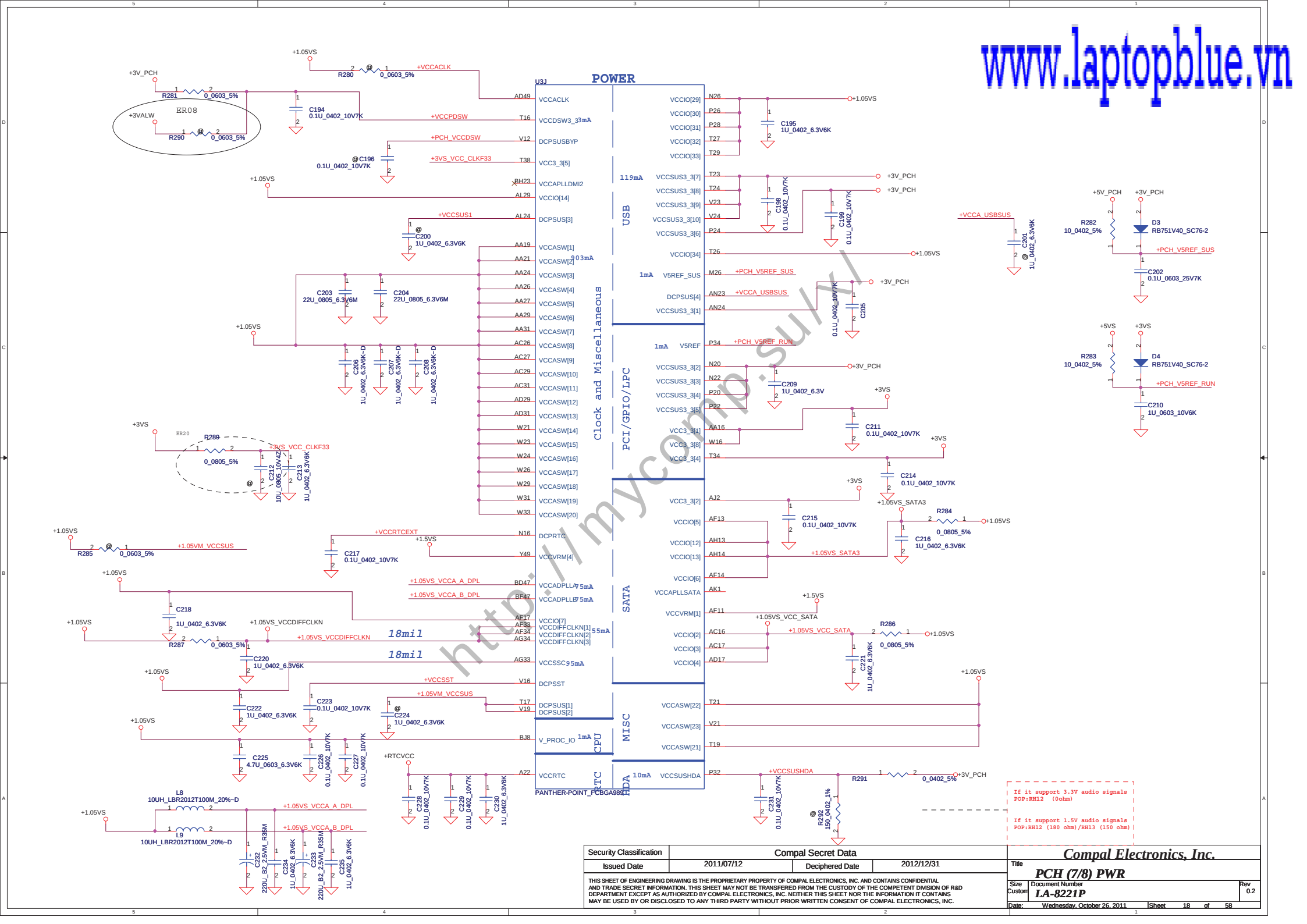
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: Custom | Document Number: LA-8221P | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 17 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

If it support 3.3V audio signals
POP:RH12 (0ohm)

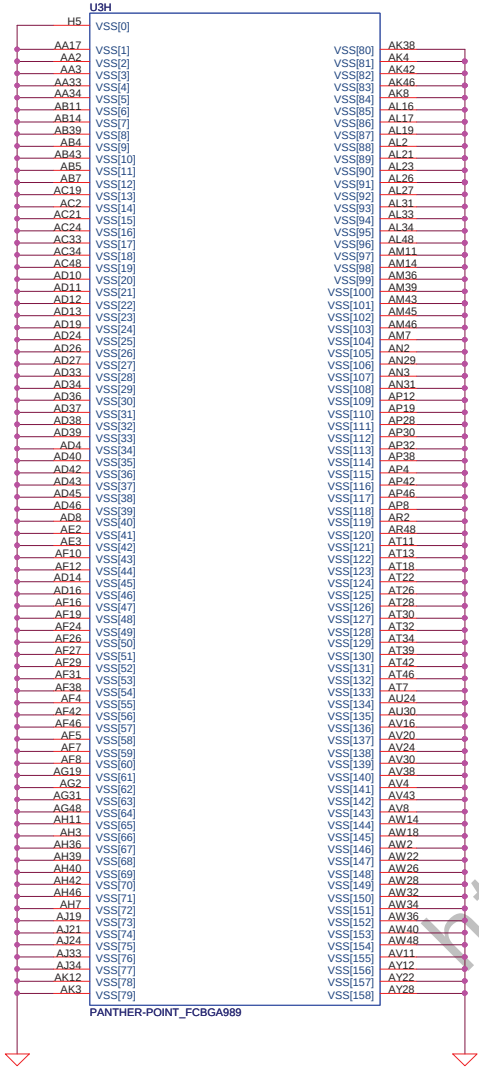
If it support 1.5V audio signals
POP:RH12 (180 ohm)/RH13 (150 ohm)

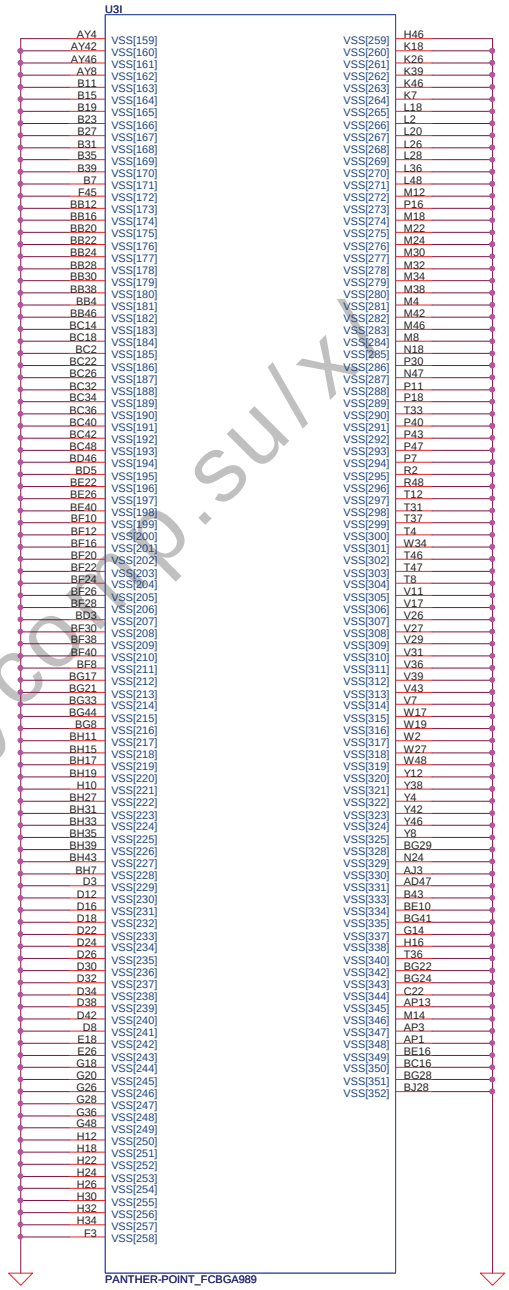
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 18 of 58





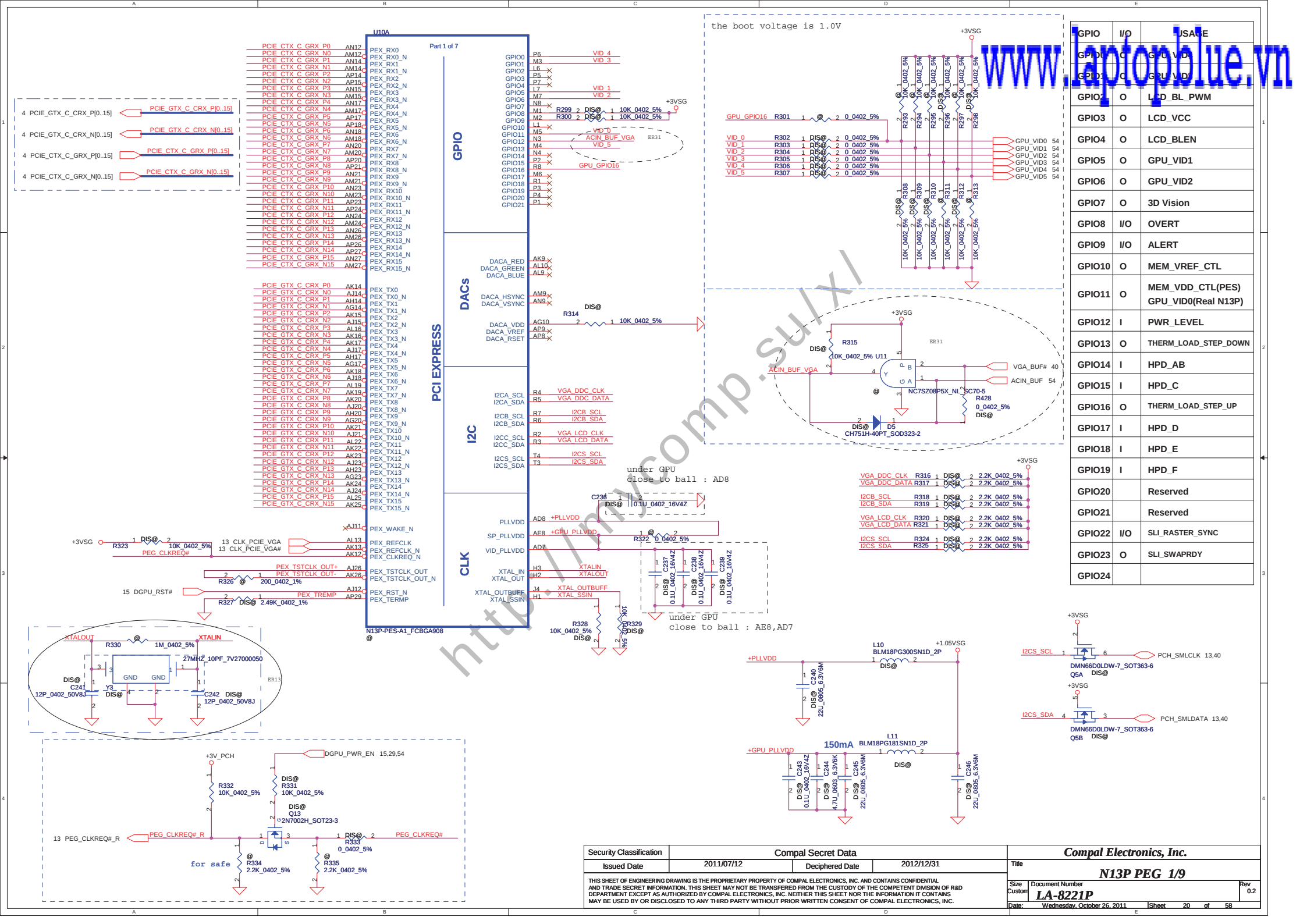
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (8/8) VSS

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 19 of 58



GPIO	I/O	USAGE
GPIO0	O	GPU_VID
GPIO1	O	GPU_VID
GPIO2	O	GPU_VID
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	N13P PEG 1/9
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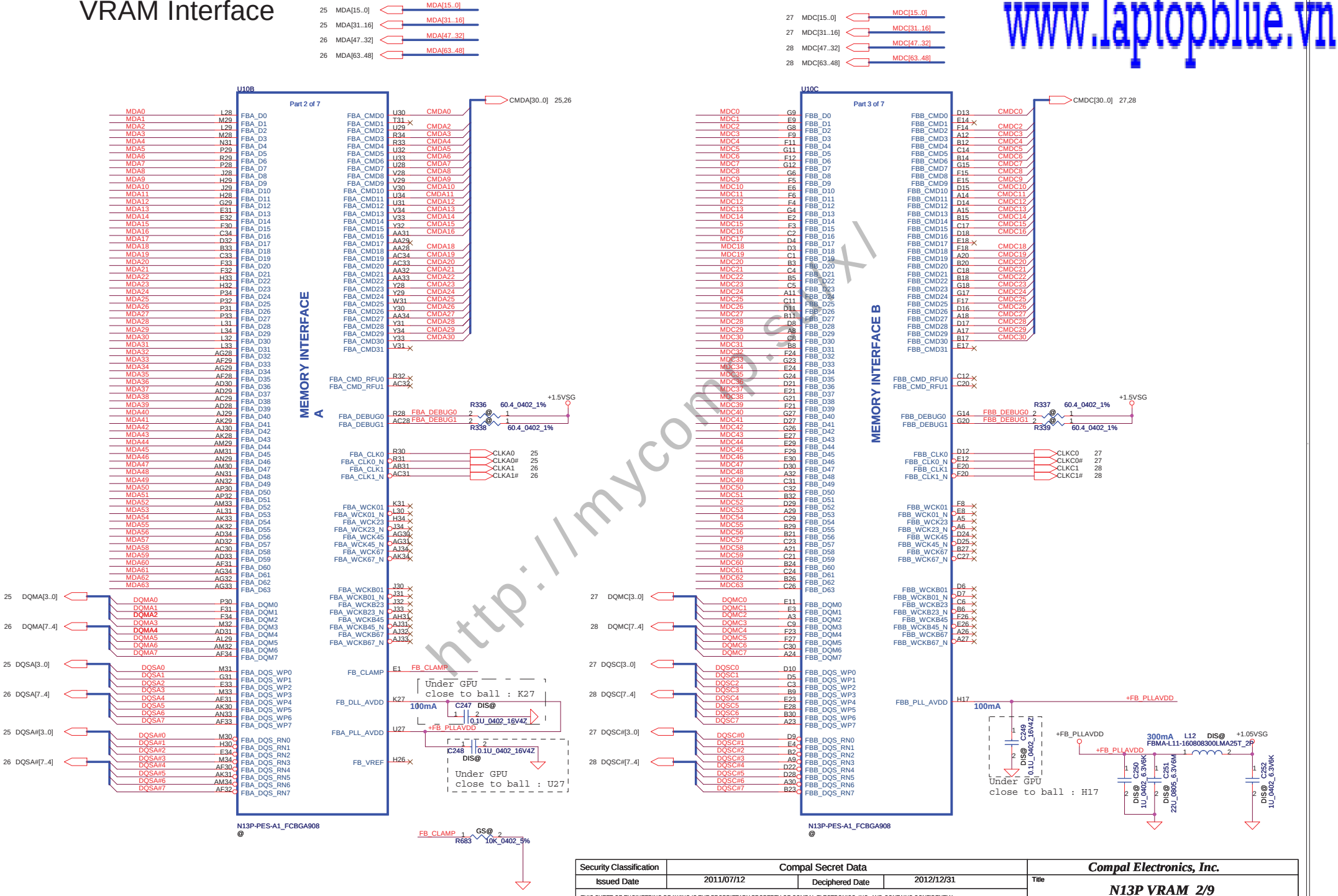
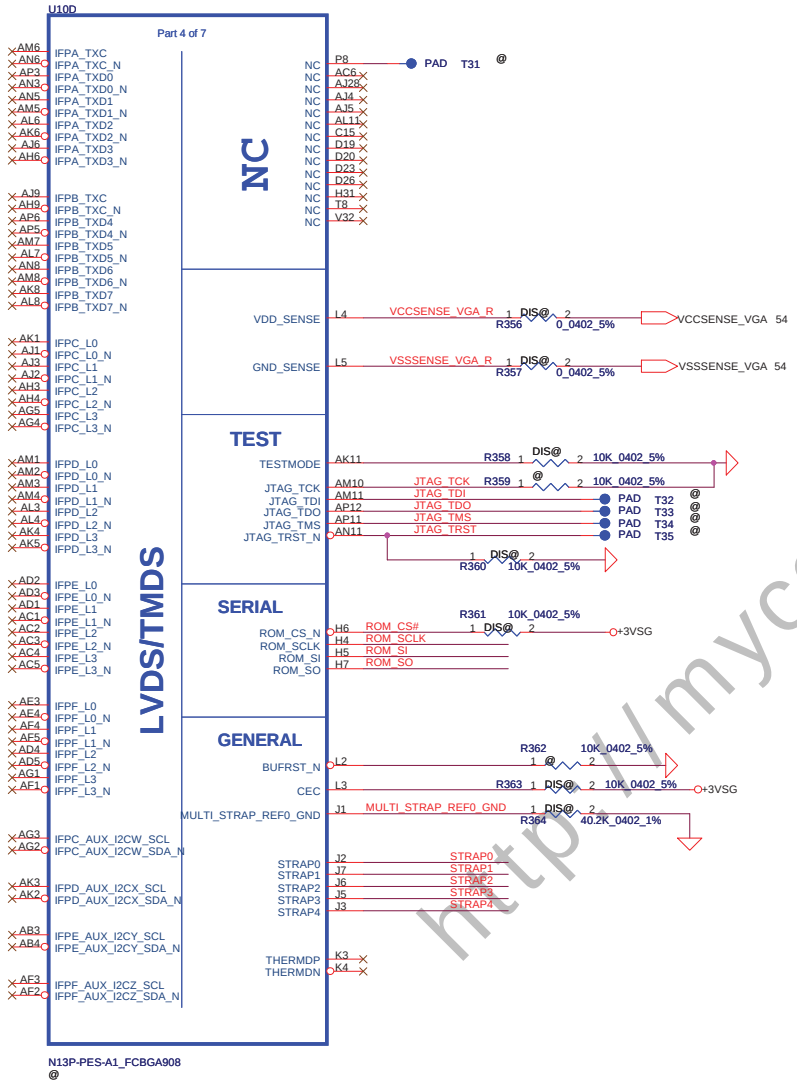
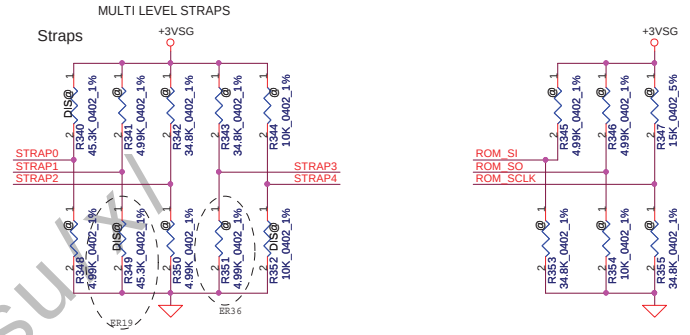
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	N13P VRAM 2/9		
Size: Custom	Document Number: LA-8221P		Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 21 of 58		





Need check with NVIDIA

10/12 nVidia Keven
Strap1
10/17 nVidia Keven N13P-GS
ER36 Strap2 / Strap3

For N13P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 45K	R PD 30K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 35K	R PD 30K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 20K	R PD 30K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 15K	R PD 30K	R PD 15K

For N13M-GE1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M* 16* 4 1GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 45K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	128M* 16* 4 1GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 35K	R PD 30K	R PU 5K

For N13M-GE1 GB1b-64 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	256M* 8* 8 2GB	ELPIDA SA000056P00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	256M* 8* 8 2GB	Hynix SA000056Q00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	512M* 8* 8 4GB	HYNIX SA00005BL00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 15K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	512M* 8* 8 4GB	ELPIDA SA00005AA00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 20K	R PD 30K	R PU 5K

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P LVDS 3/9**

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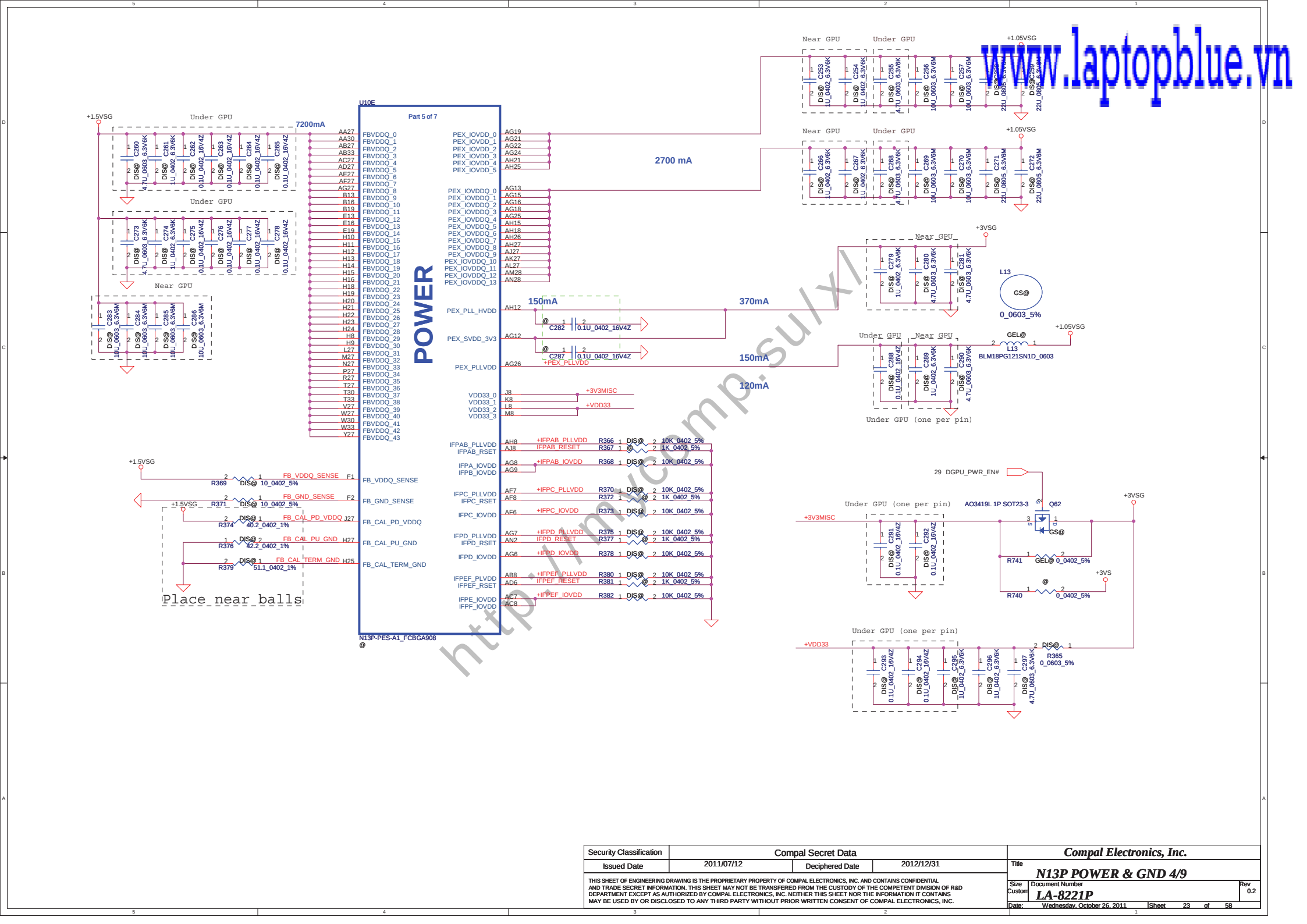

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P POWER & GND 4/9**

Size	Document Number	Rev
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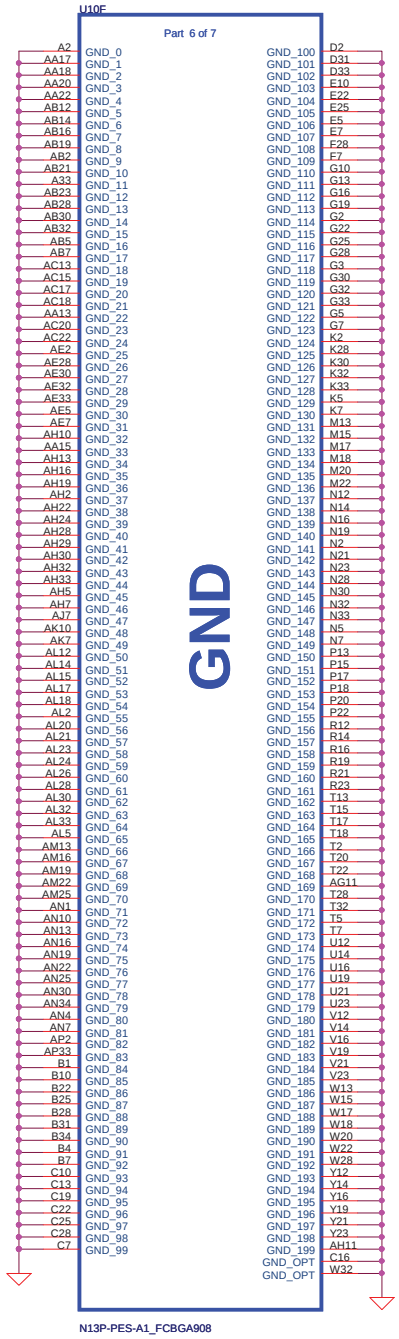
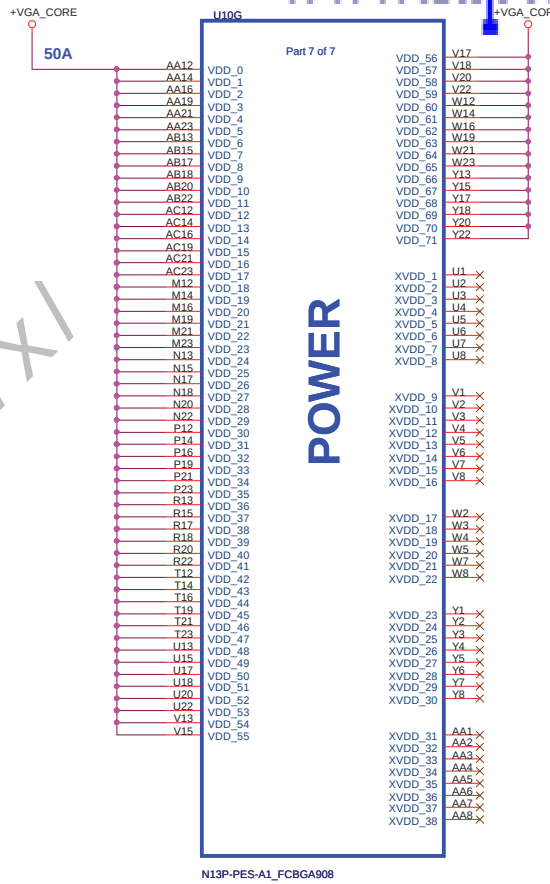




Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

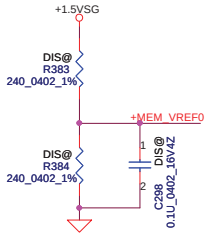
Title: **N13P POWER & GND 5/9**

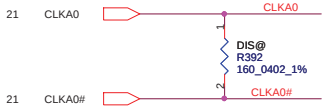
Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 24 of 58

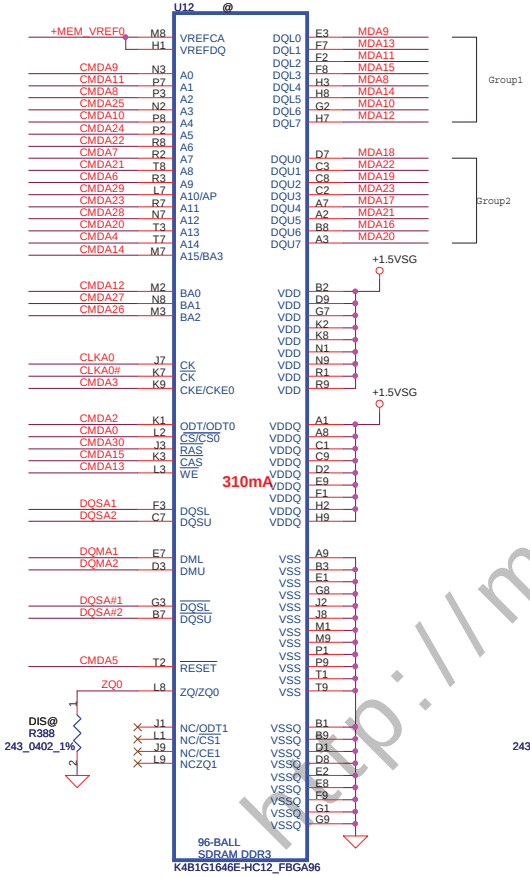
VRAM DDR3 chips (1GB)

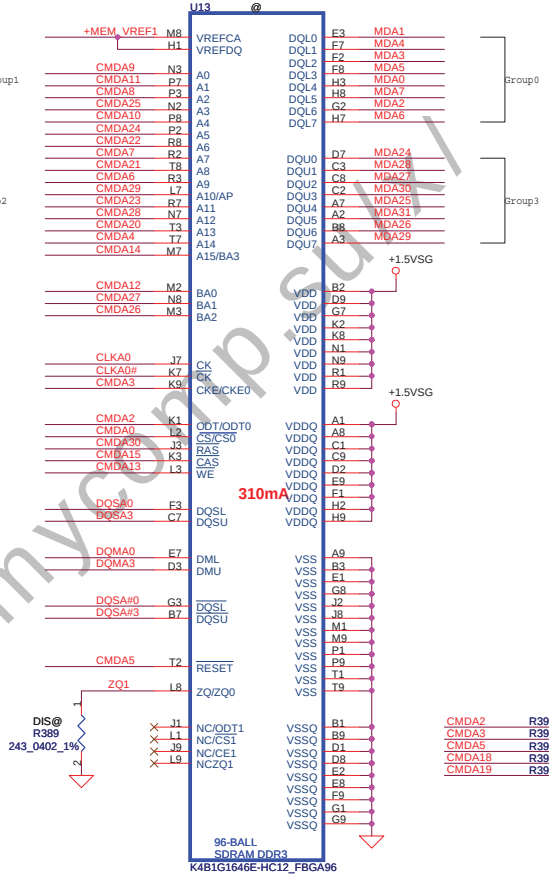
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



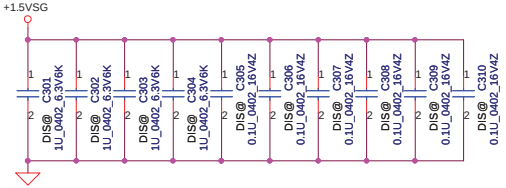


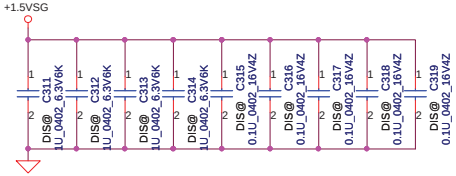
NV recommand 0720





	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Mode		
Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date 2012/12/31

Compal Electronics, Inc.

Title: **N13P DDR3 6/9**

Size: Custom | Document Number: **LA-8221P** | Rev: 0.2

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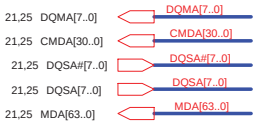
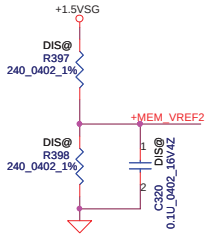
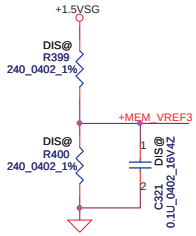
VRAM DDR3 chips (1GB)

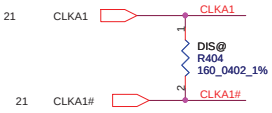
64Mx16 DDR3 *8==>1GB

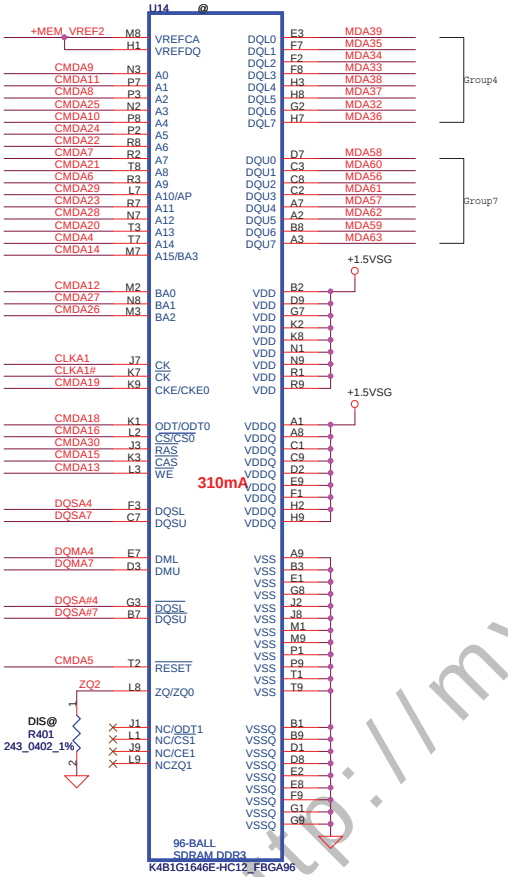
128Mx16 DDR3 *8==>2GB

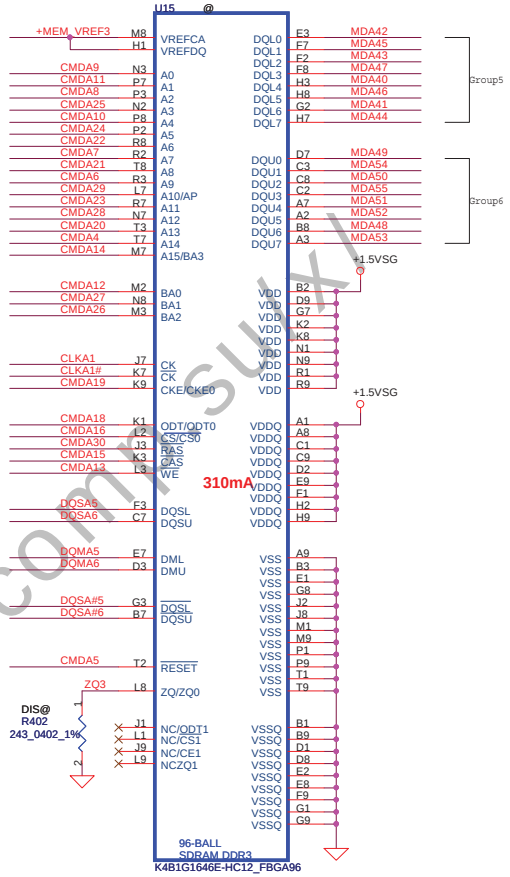


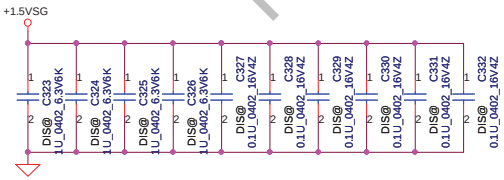


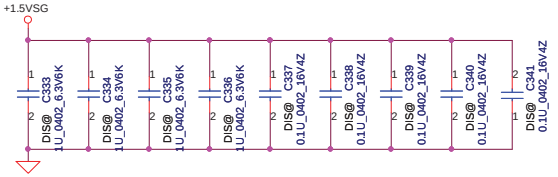












Mode	Address	
	BA2	BA2
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

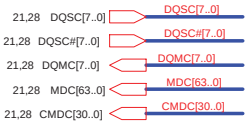
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

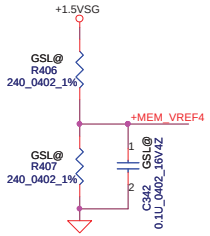
Compal Electronics, Inc.		
Title: N13P DDR3 7/9		
Size: Custom	Document Number: LA-8221P	Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 26 of 58	

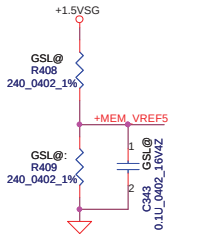
VRAM DDR3 chips (1GB)

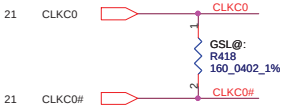
64Mx16 DDR3 *8==>1GB

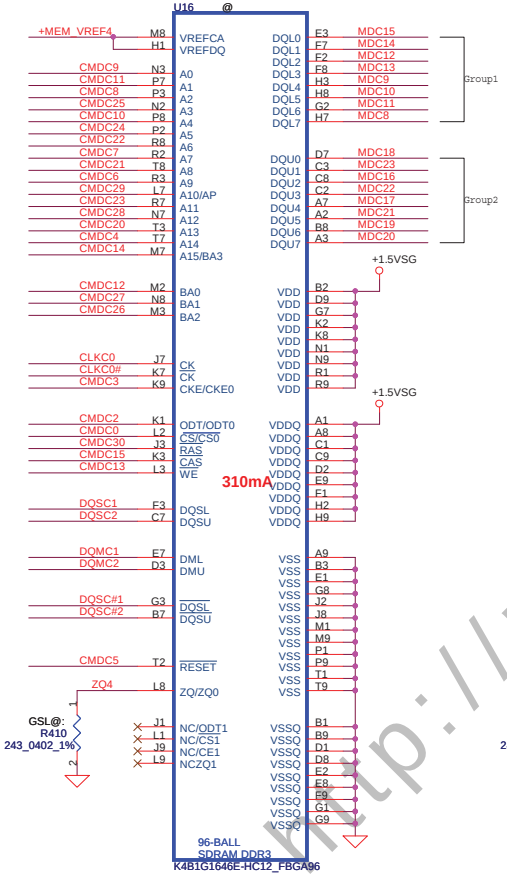
128Mx16 DDR3 *8==>2GB

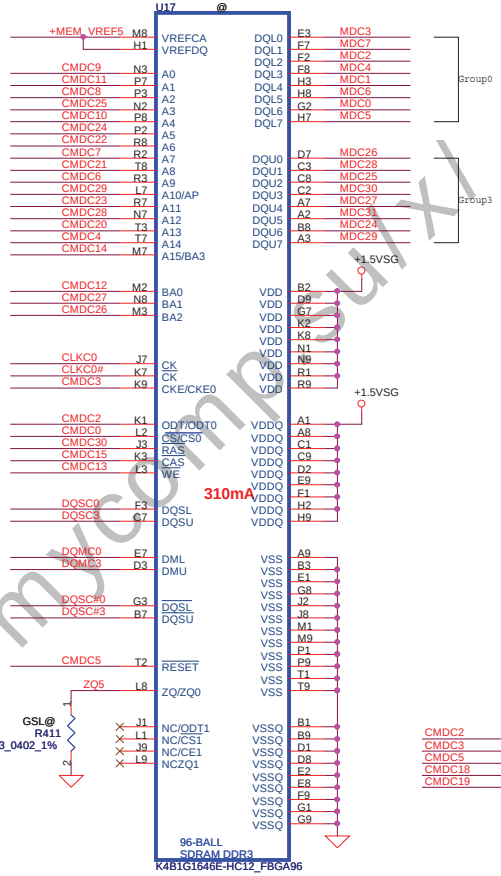


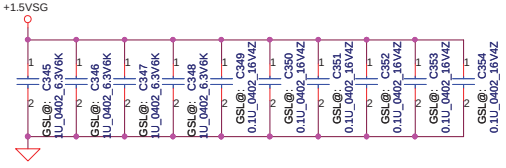


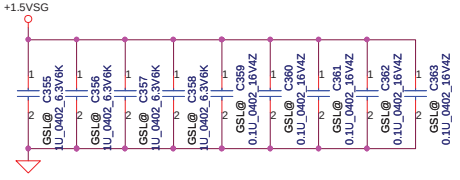












	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

	LOW	HIGH
CMD0		
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date 2012/12/31

Compal Electronics, Inc.

Title: N13P DDR3 8/9

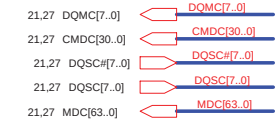
Size: Custom | Document Number: LA-8221P | Rev: 0.2

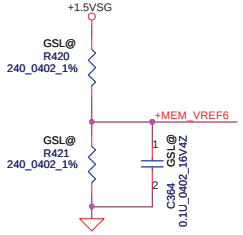
Date: Wednesday, October 26, 2011 | Sheet 27 of 58

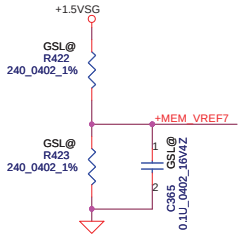
VRAM DDR3 chips (1GB)

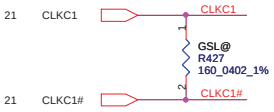
64Mx16 DDR3 *8==>1GB

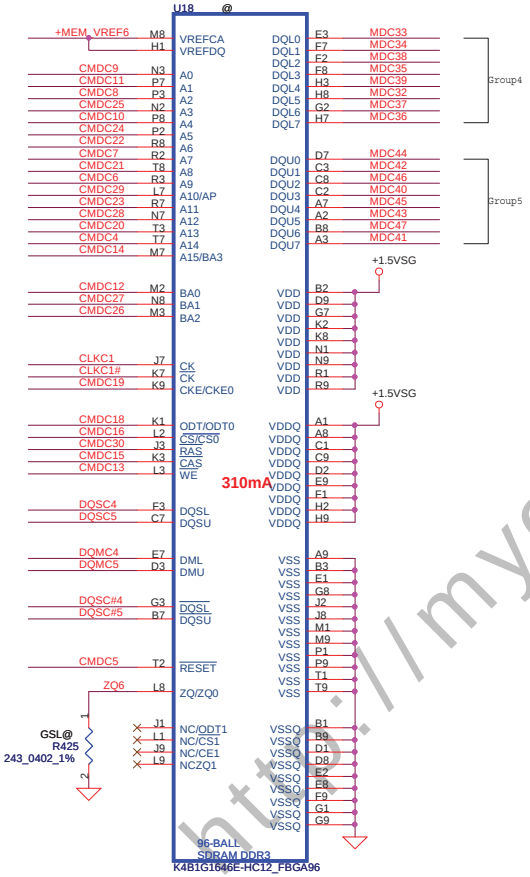
128Mx16 DDR3 *8==>2GB

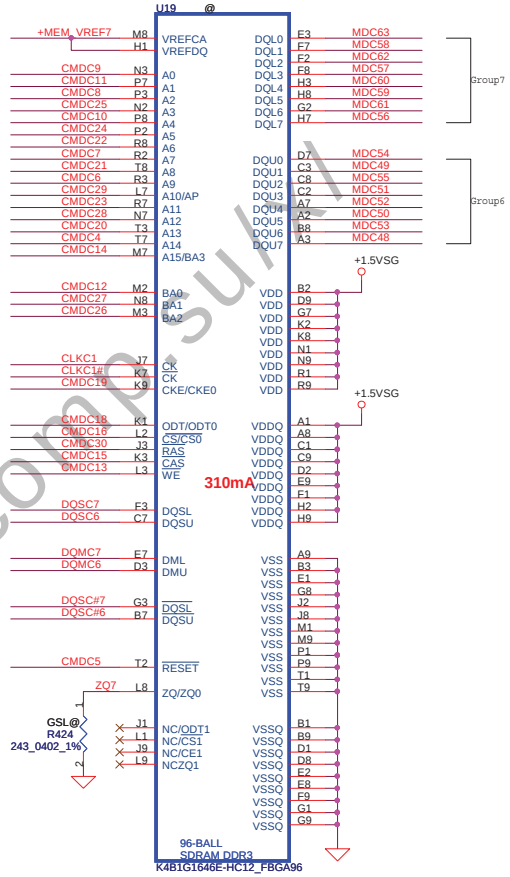


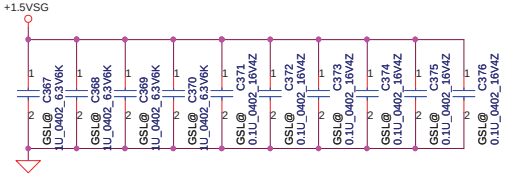


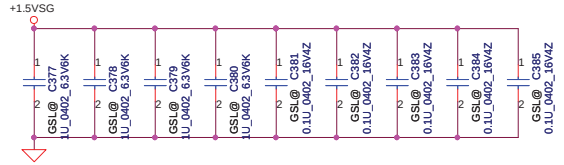












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P DDR3 9/9

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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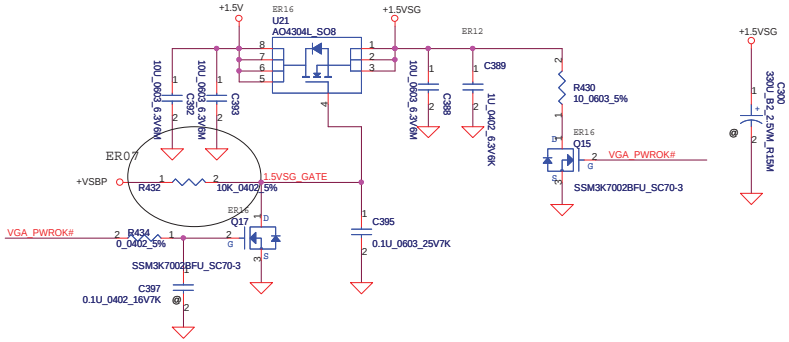
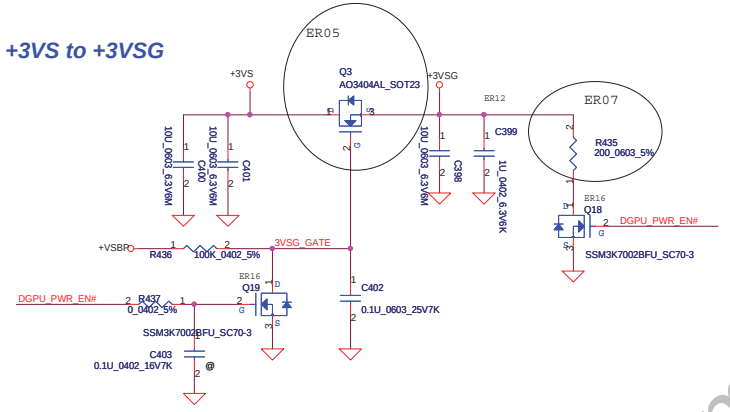
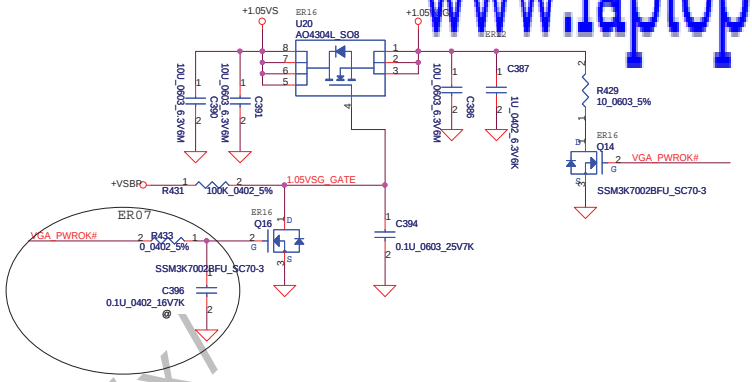
+1.5V to +1.5VSG

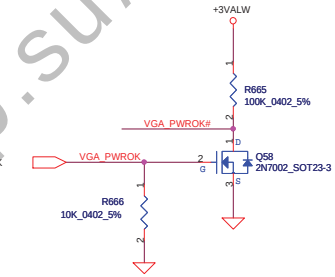


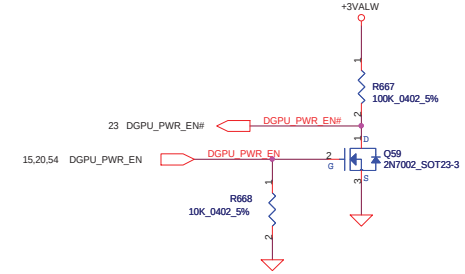
+3VS to +3VSG



+VCCP to +1.05VSG







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
Custom	LA-8221P	0.2

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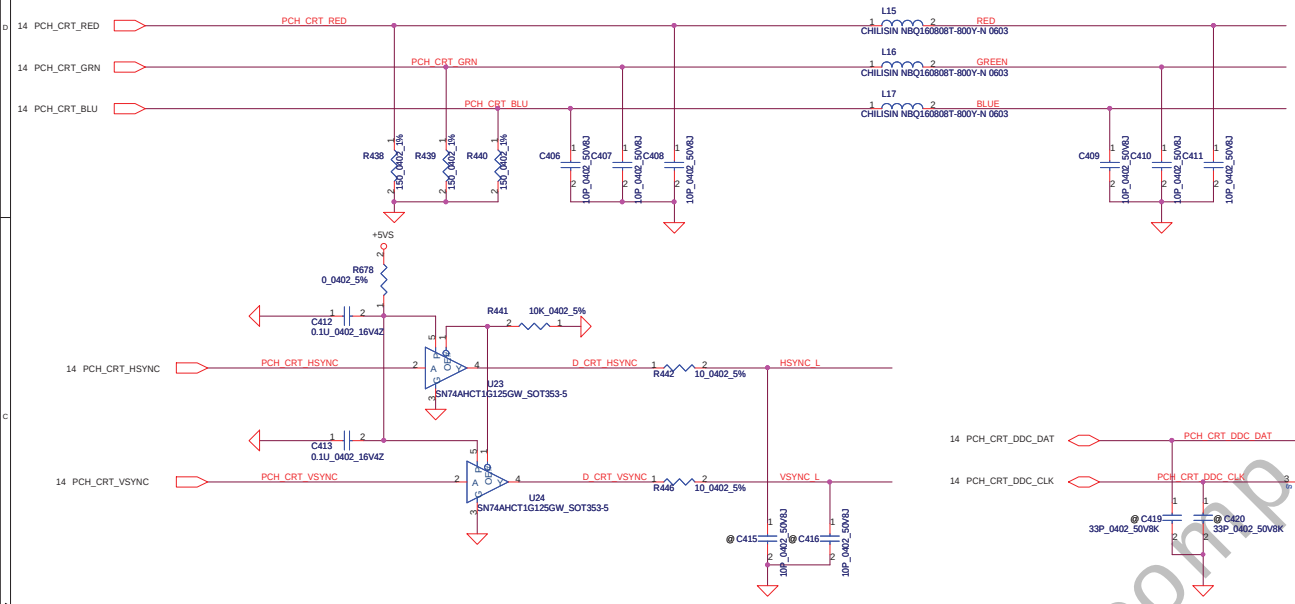
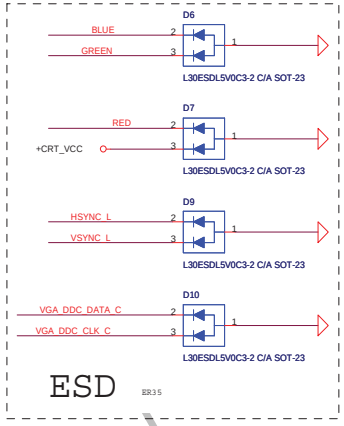
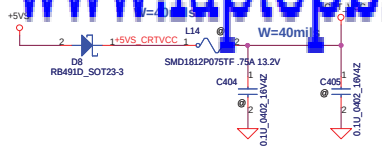
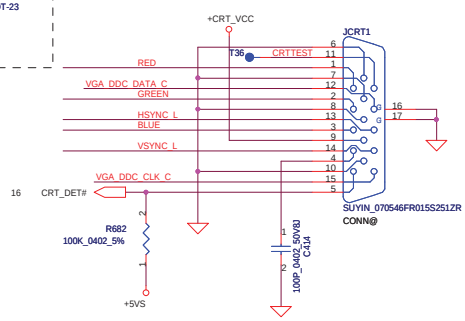
CRT

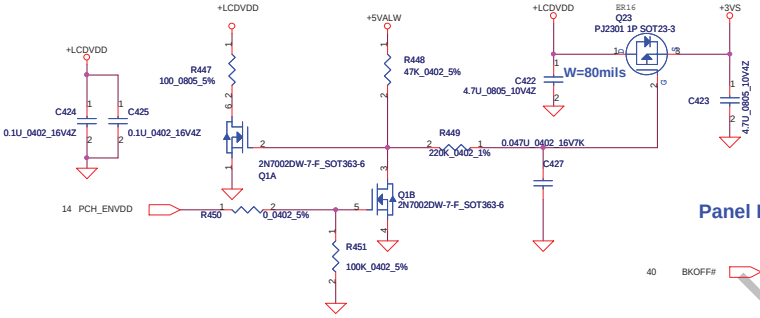




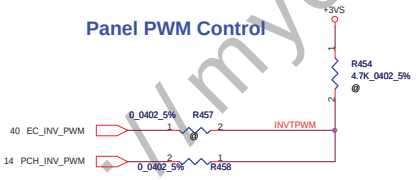




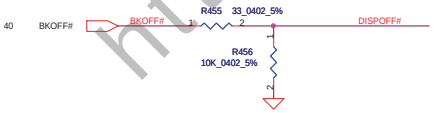
LCD POWER CIRCUIT

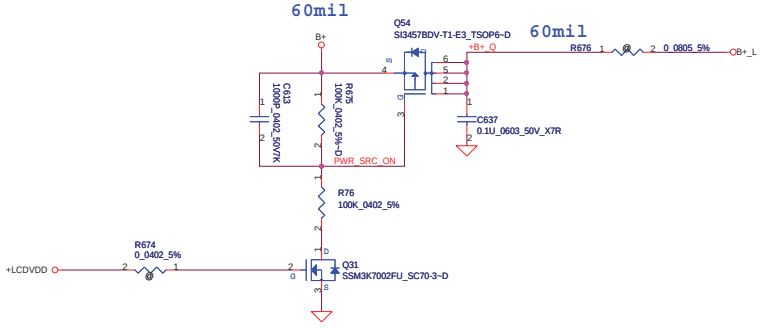


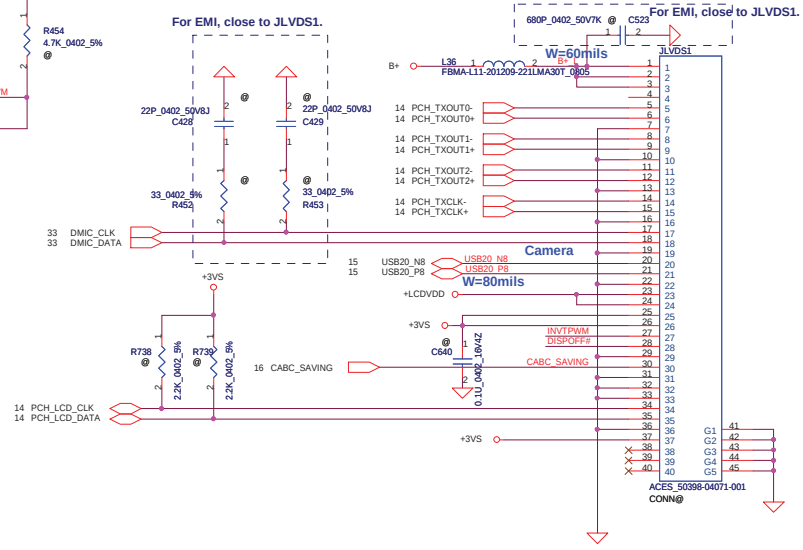
Panel PWM Control



Panel Backlight Control







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LVDS/CRT CONN

Size	Document Number	Rev
C	LA-8221P	0.2

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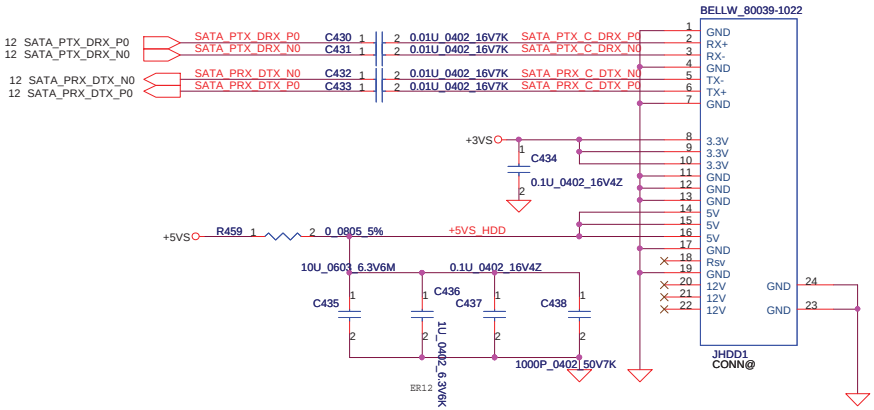
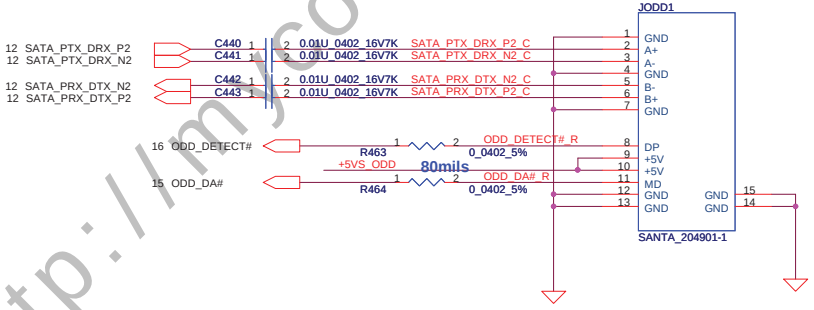
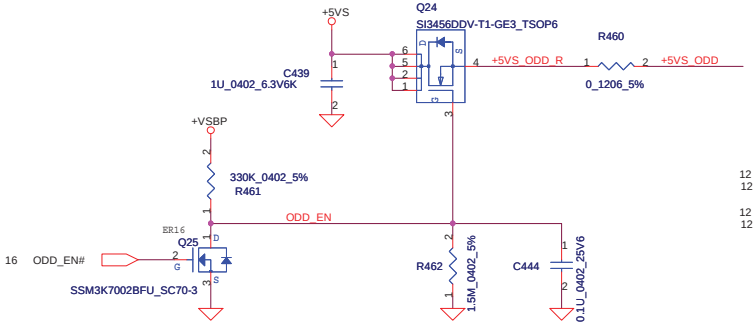
SATA HDD Conn.

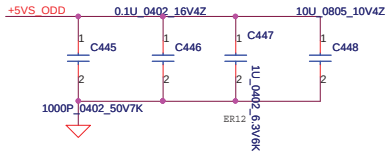


SATA ODD Conn.





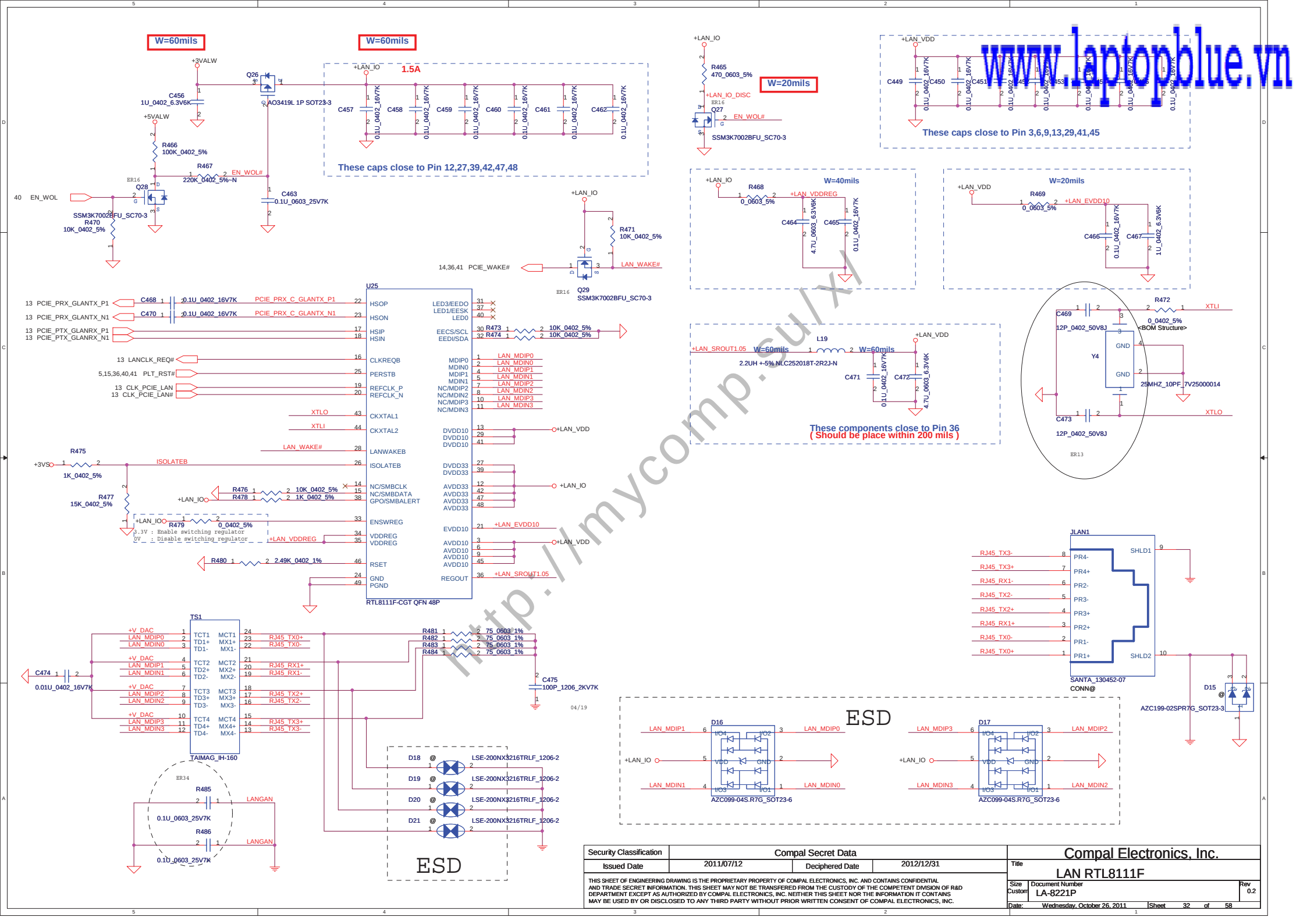
Placea caps. near ODD CONN.



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title	HDD & ODD CONN	
Size B	Document Number LA-8221P	Rev 0.2
Date: Wednesday, October 26, 2011	Sheet 31 of 58	



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LAN RTL8111F

Size	Document Number	Rev
Custom	LA-8221P	0.2

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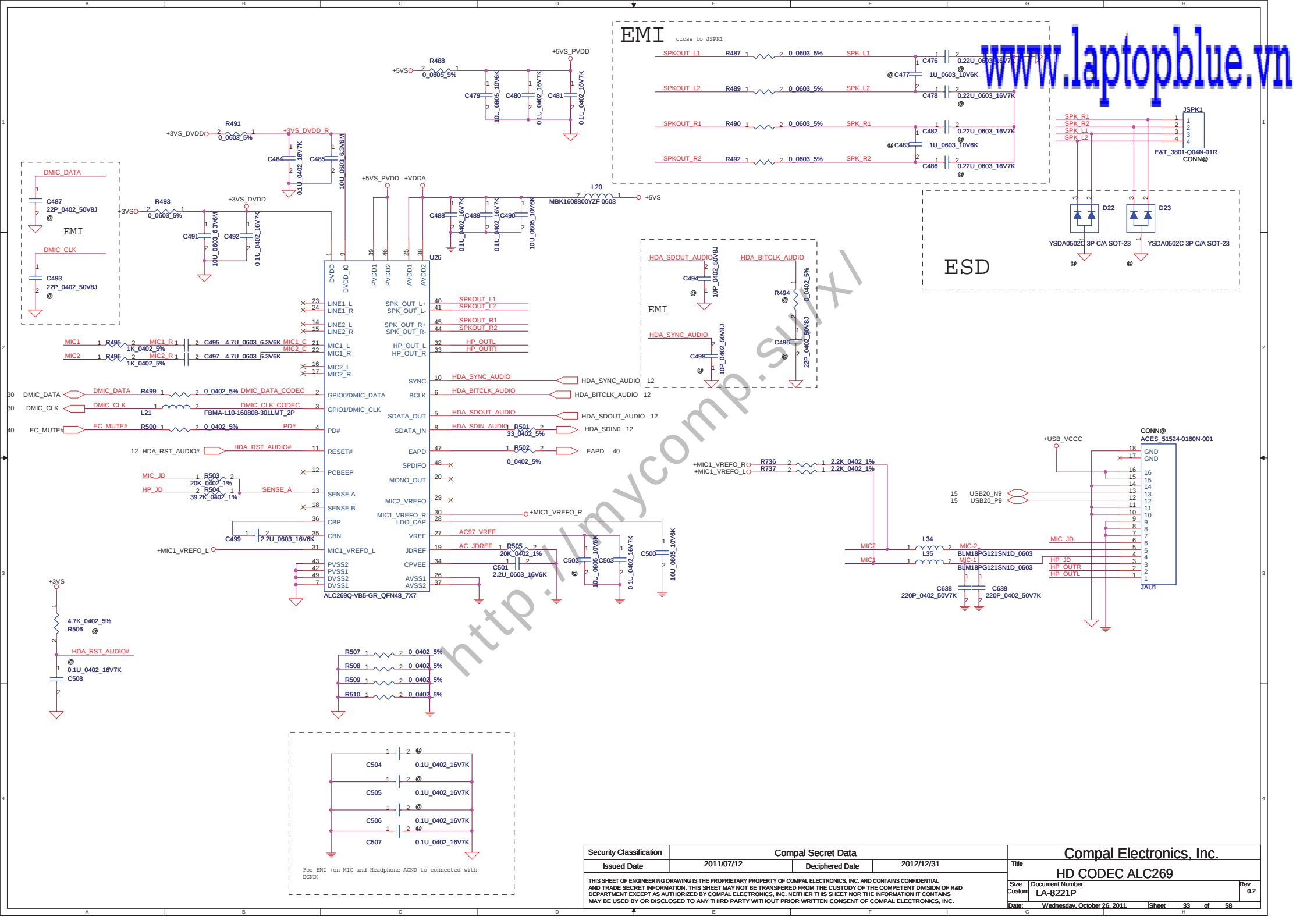

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: HD CODEC ALC269

Size	Document Number	Rev
Custom	LA-8221P	0.2

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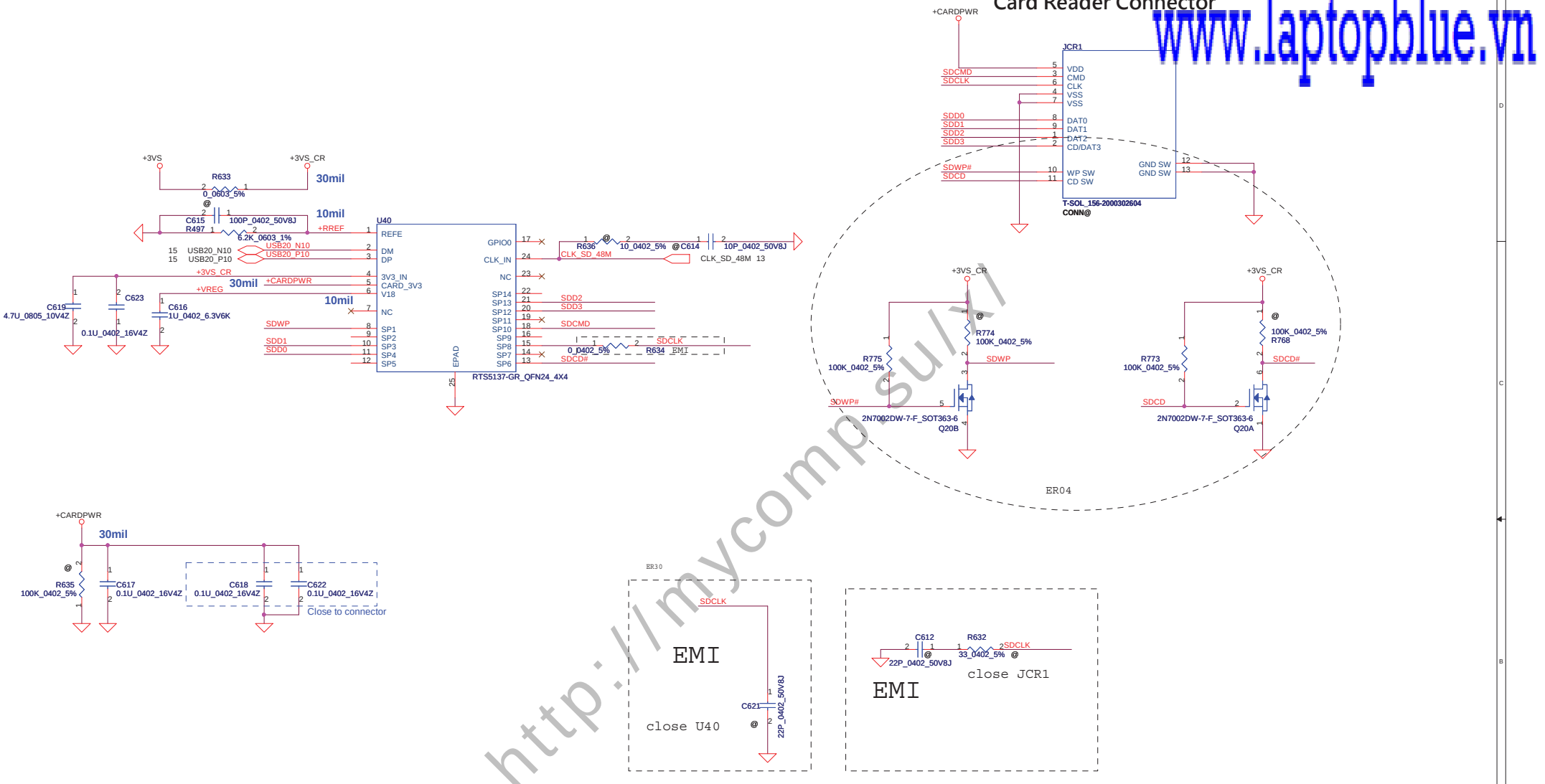
Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	LA-8221P	0.2

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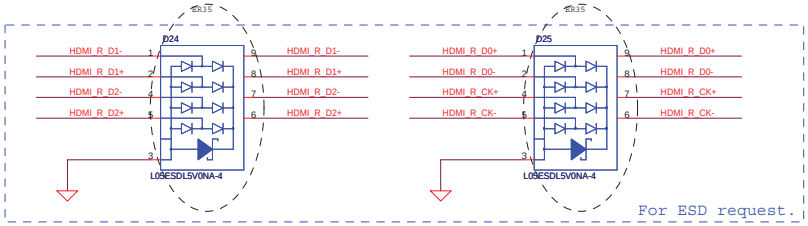

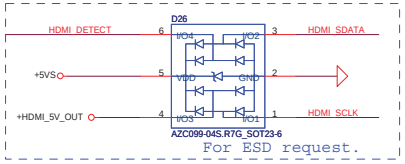

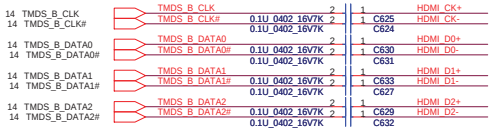

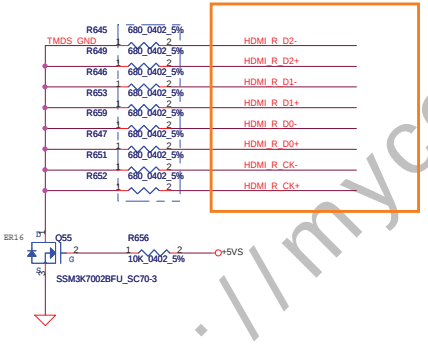

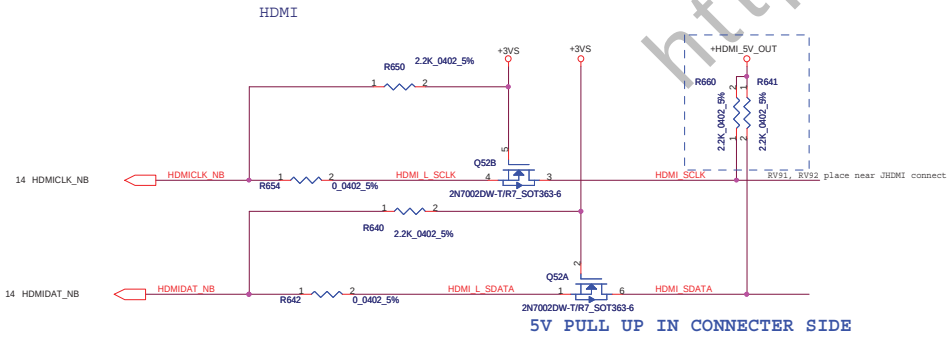

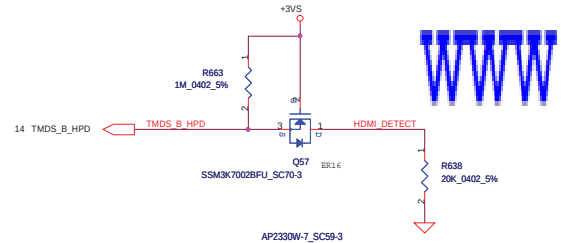

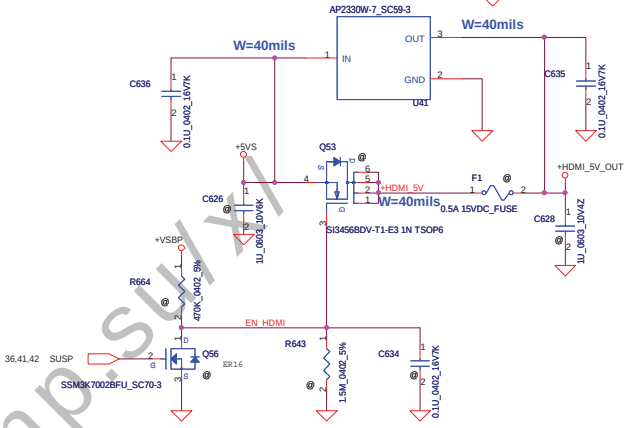

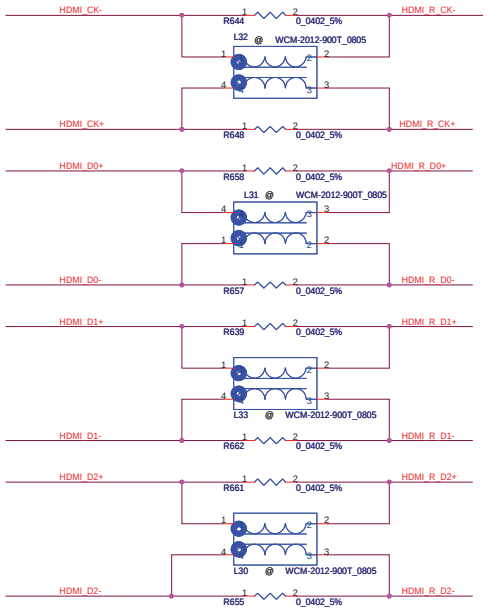

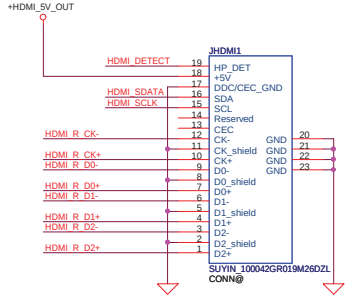

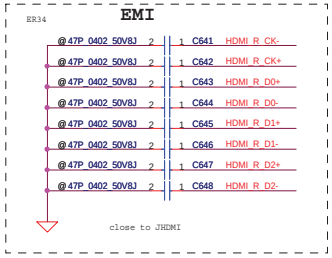

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
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Date: Wednesday, October 26, 2011 | Sheet 35 of 58

ER02 Add USB3.0 (ASM1042)

	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

For WAKE Function

USB_PEPWRDET

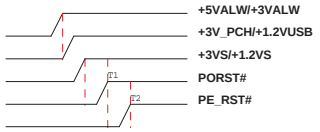
	R1034	R1022
S1	Mount	@
* S3	@	Mount

USB_PESEL

	R1033
* Other applaction	@
Express Card/Mini Card	Mount

Power Sequence

ASM1042



T1: 2~80ms
T2: >200ms

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: USB3.0 controller

Size	Document Number	Rev
Custom	LA-8221P	0.2

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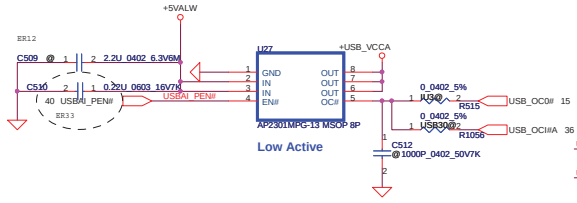
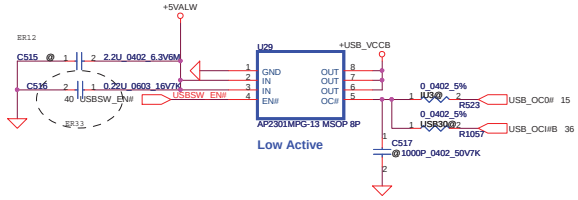
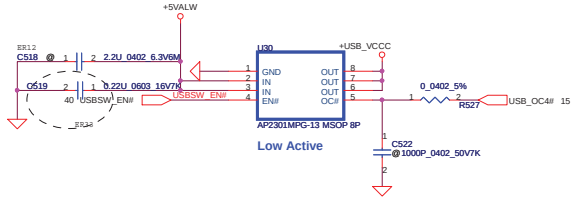
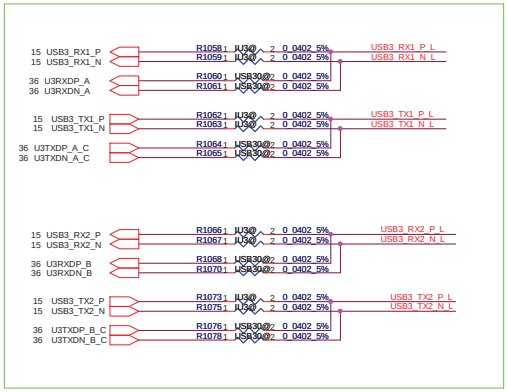
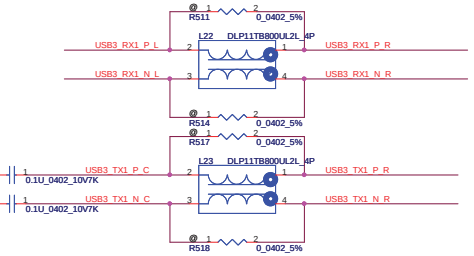
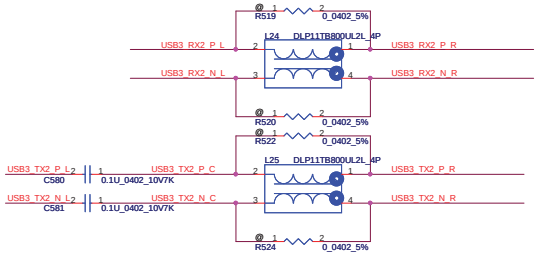


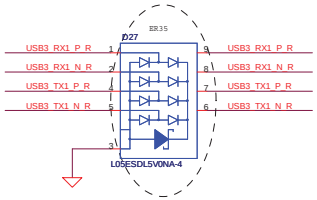


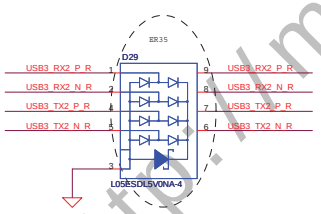


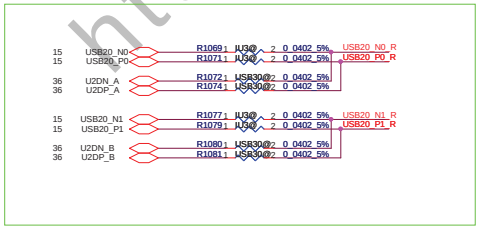


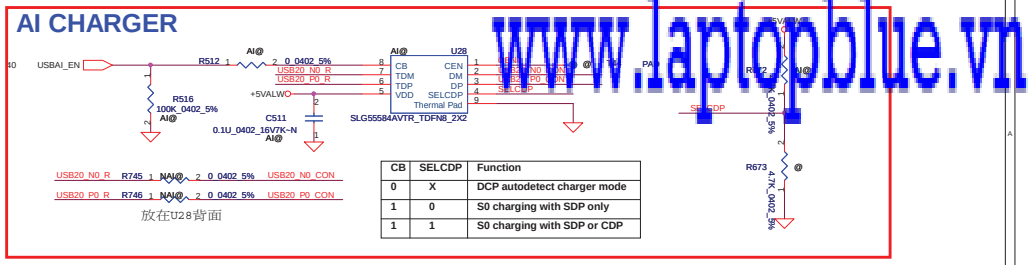


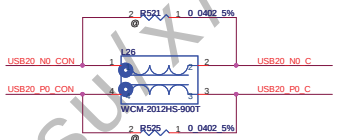


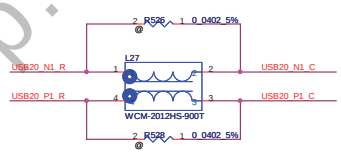


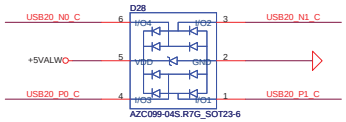




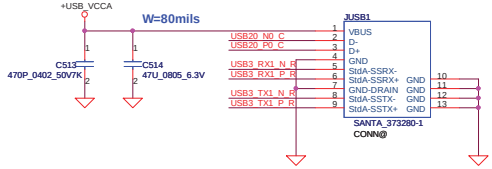


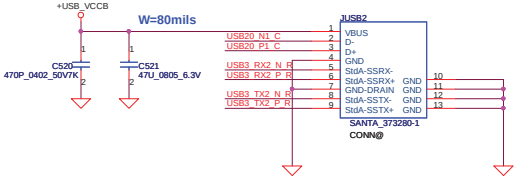






charger port: left side & near user





ER02 Add USB3.0 (ASM1042)

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: USB2.0/USB3.0 CONN

Size	Document Number	Rev
Custom	LA-8221P	0.2

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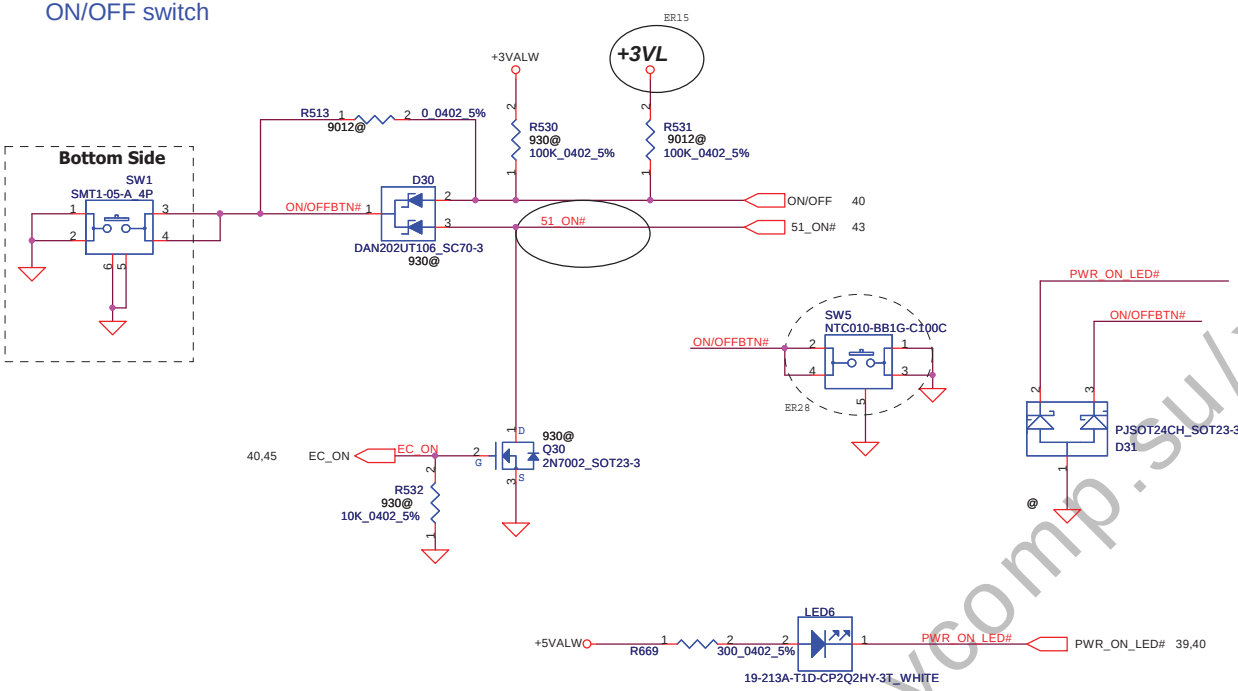
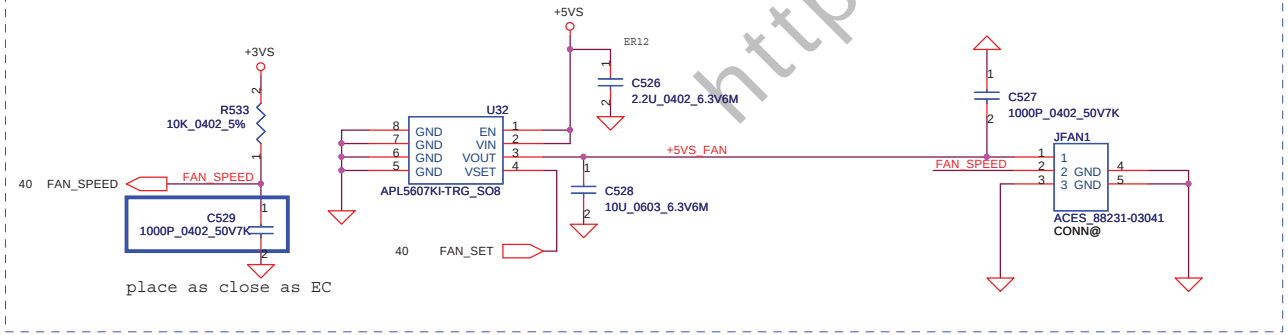
Power Button

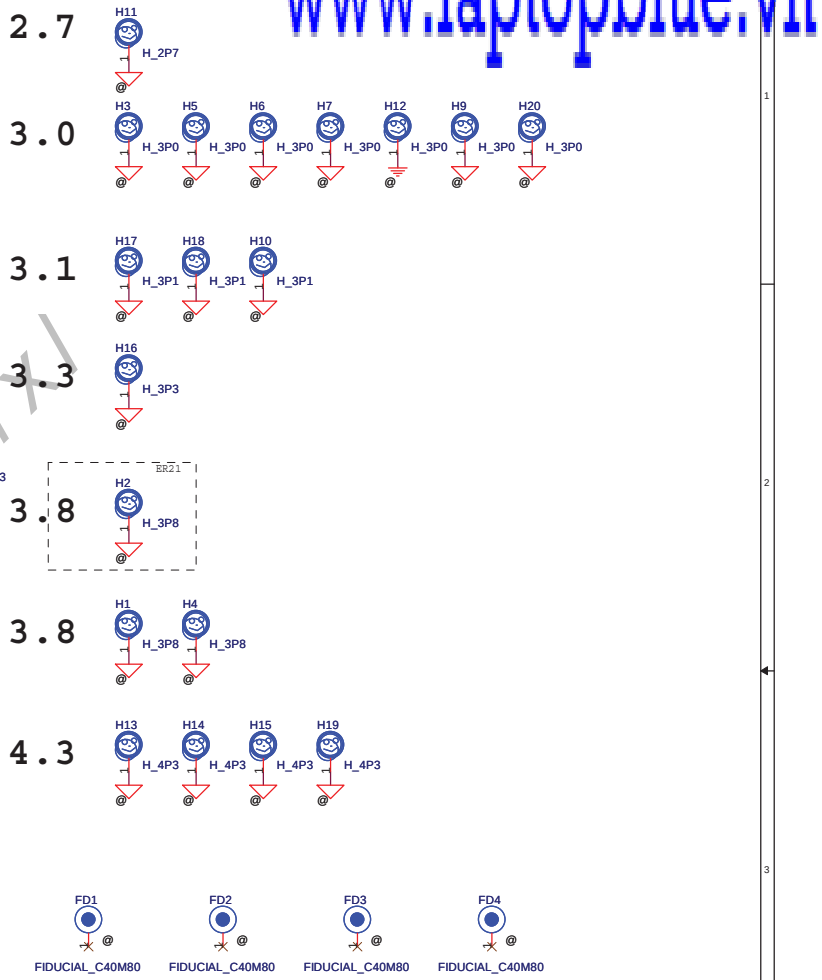
ON/OFF switch



Fan Control Circuit



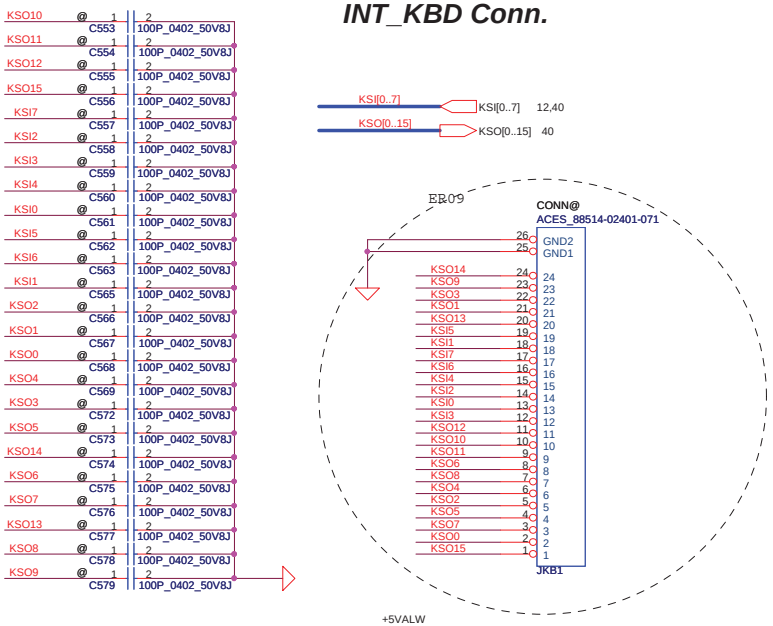
Screw Hole



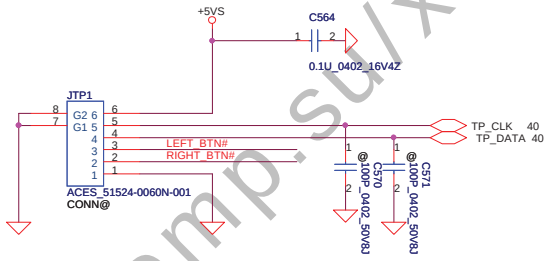
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

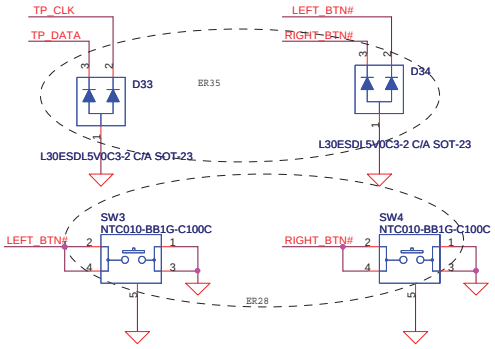
Compal Electronics, Inc.			
Title: PWRBTN/ FAN / Screws			
Size: Custom	Document Number: LA-8221P		Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 38 of 58		

INT_KBD Conn.

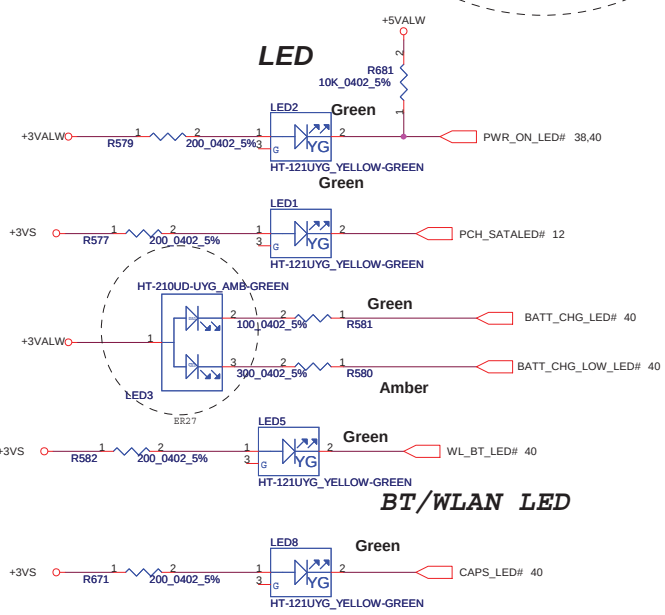


Touch/B Connector

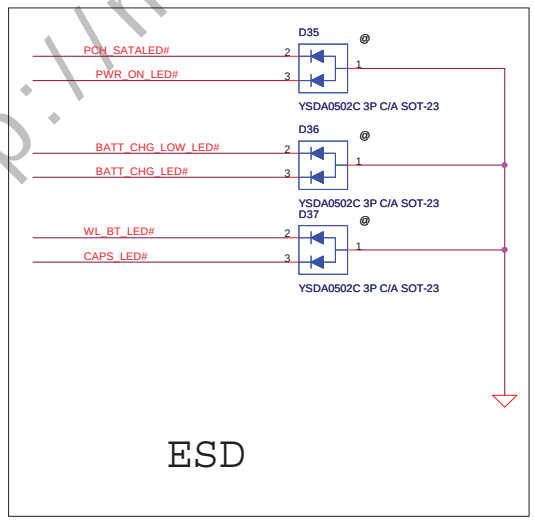




LED

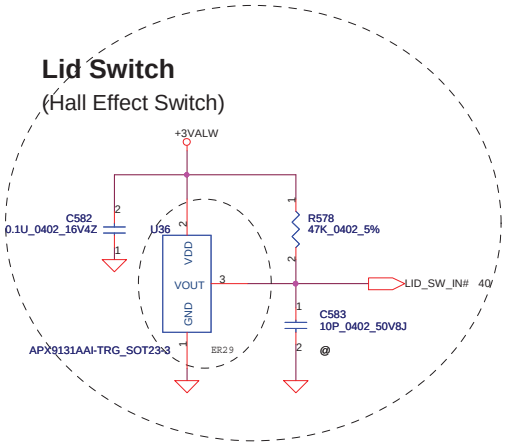


BT/WLAN LED



Lid Switch

(Hall Effect Switch)



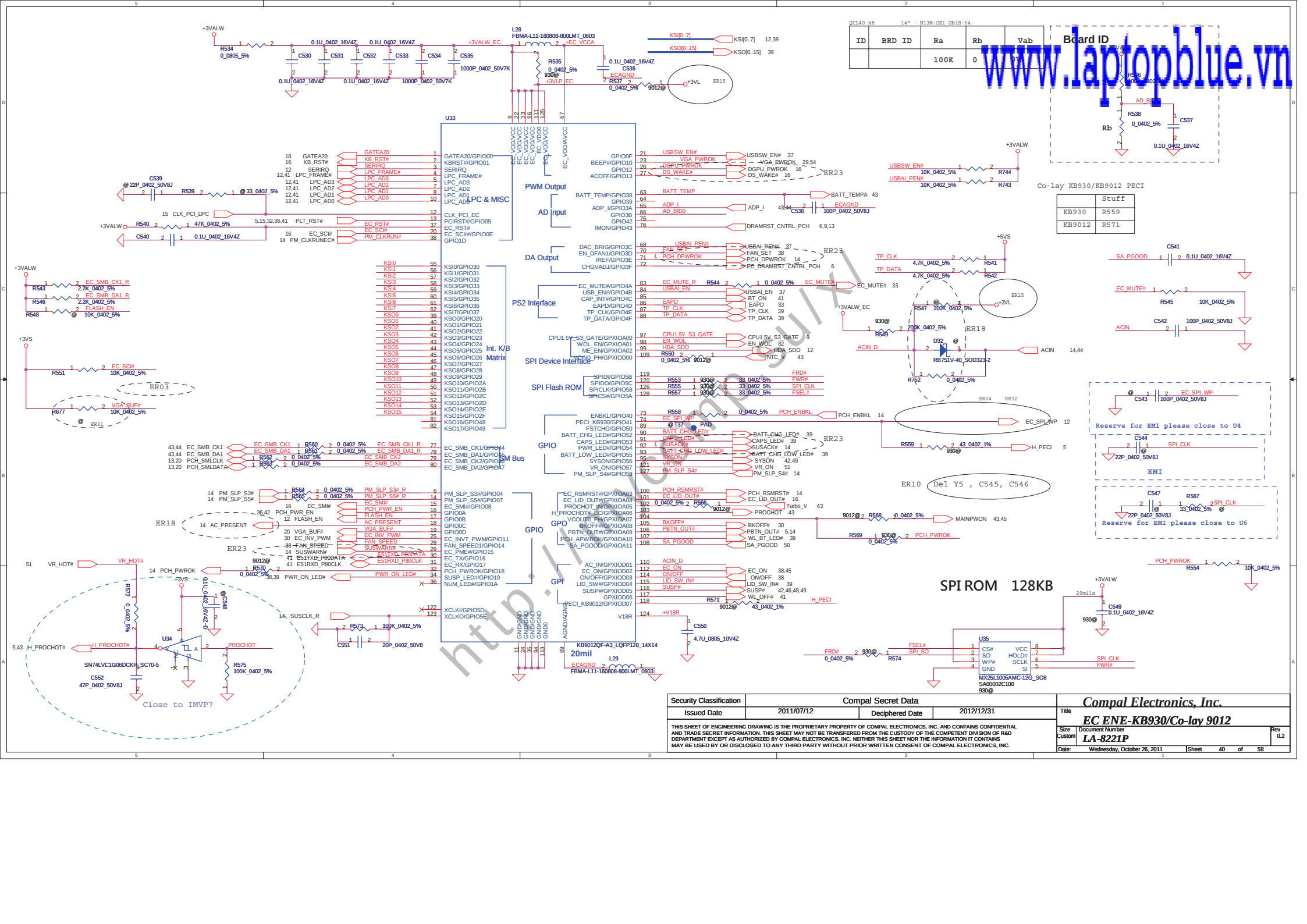
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: KB/EC ROM/TP/FUN/LED

Size	Document Number	Rev
B	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 39 of 58



ID	BRD ID	Ra	Rb	Vab
		100K	0	0

	Stuff
KB930	R559
KB9012	R571

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

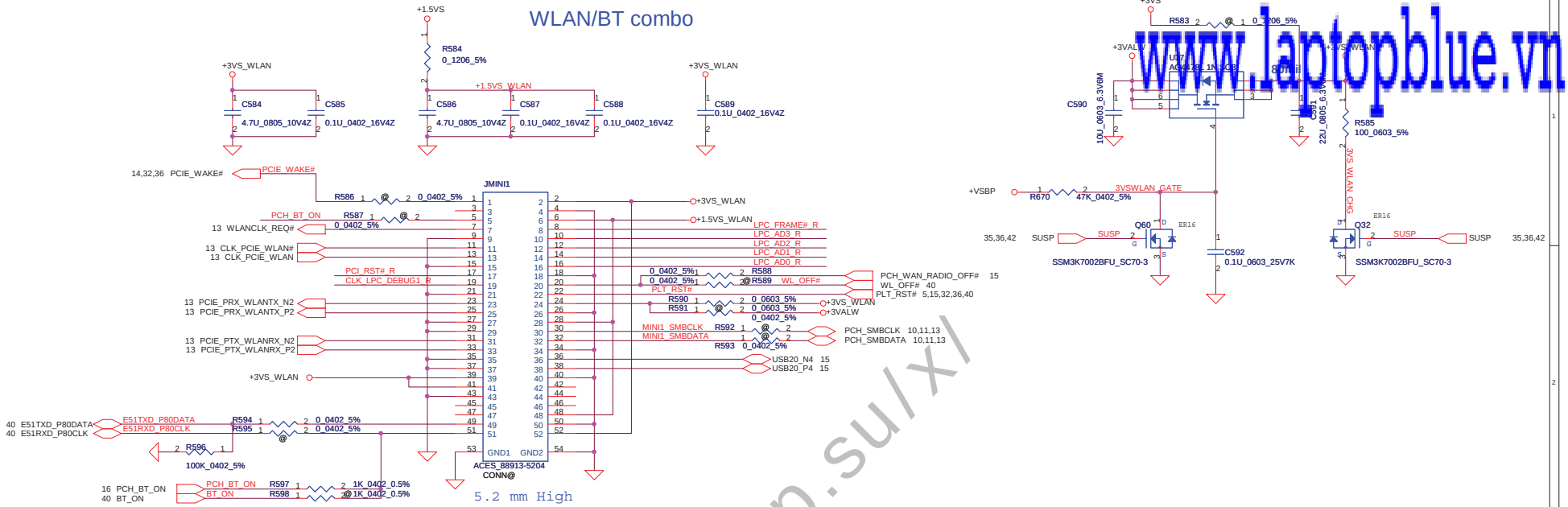
Compal Electronics, Inc.

Title: EC ENE-KB930/Co-lay 9012

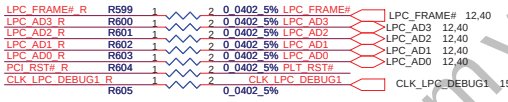
Size: Custom | Document Number: LA-8221P | Rev: 0.2

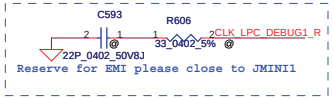
Date: Wednesday, October 26, 2011 | Sheet 40 of 58

WLAN/BT combo



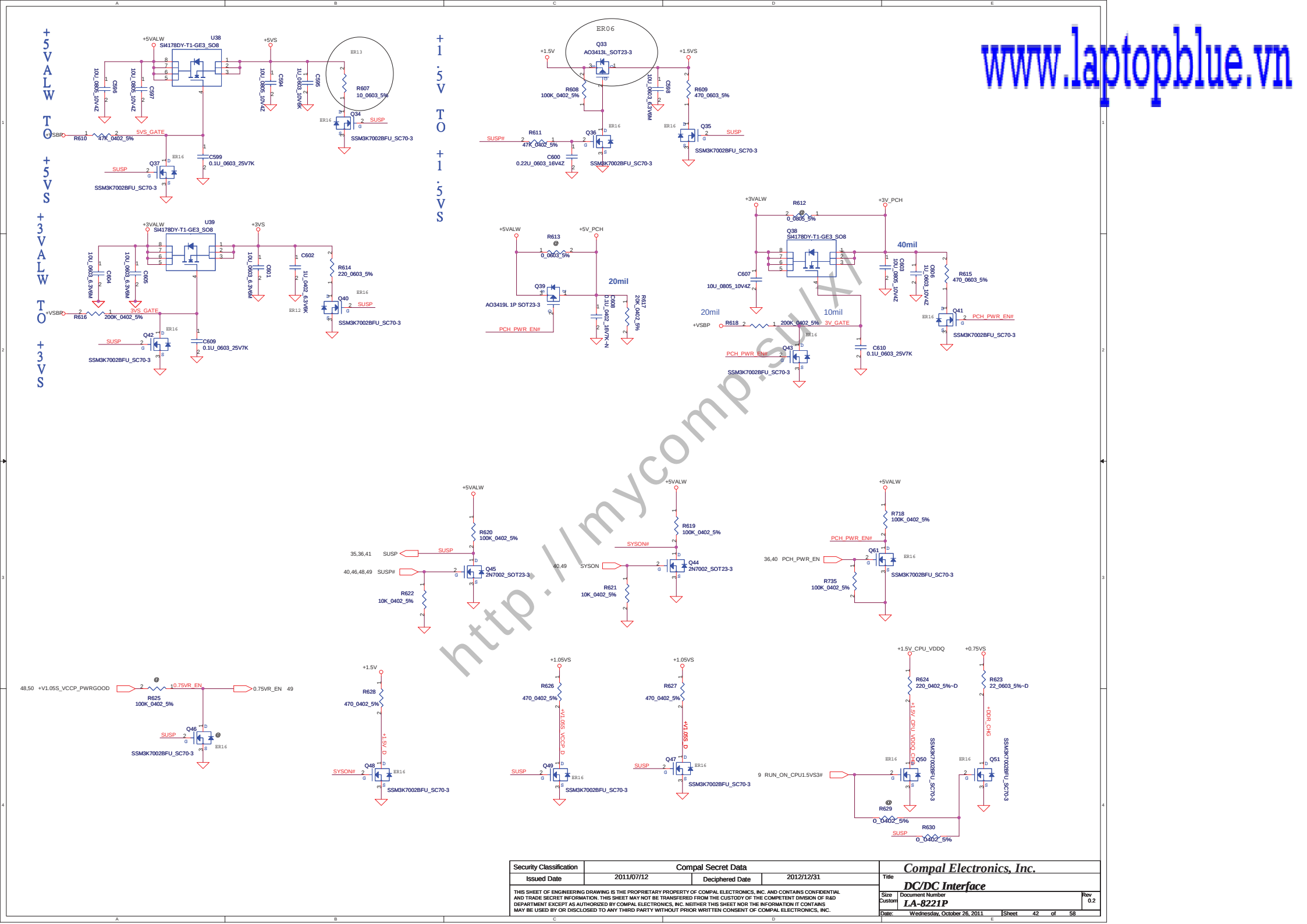
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: WLAN/ WWAN/ m-SATA			
Size: Custom	Document Number: LA-8221P		Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 41 of 58		



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: DC/DC Interface

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 42 of 58

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

PJPDC1
@SINGA_SDC2003-004111F
PL1 HCB2012KF-121T50_0805
PL2 HCB2012KF-121T50_0805
ADPIN
VIN
PC1 1000P_0402_50V7K
PC2 100P_0402_50V8J
PC3 1000P_0402_50V7K
PC5 100P_0402_50V8J

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit but keep PR56
PH1, PR2, PQ1, PR7,PC15,PR73,PR56

VL
+3VS
PC4 @0.1U_0603_16V7K
PU1 @G718TM1U_SOT23-8
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
PR5 @100K_0402_1%
PQ1 @SSM3K7002FU_SC70-3
5,40 H_PROCHOT#
ADP_OCP_1
OTP_N_003
PR73 @0_0402_5%
40 PROCHOT
PR9 @0_0402_5%
MAINPWON 40,45
40,44 ADP_I
PR2 1K_0402_1%
+3VL
PR56 12.1K_0402_1%
PR3 @21.5K_0402_1%
NTC_V
OTP_N_002
Turbo_V
PR6 @29.4K_0402_1%
ADP_OCP_2
PR7 20K_0402_1%
PR4 @10K_0402_1%
PH1 100K_0402_1%_NCP15WF104F03RC
40

PJP2
@SUYIN_200045GR009G28DZR
EC_SMCA
EC_SMDA
TS_A
GND
GND
PD1 @PJSOT24CW_SOT323-3
PL3 HCB2012KF-121T50_0805
PL4 HCB2012KF-121T50_0805
VMB
BATT+
PR27 1K_0402_1%
PC6 1000P_0402_50V7K
PC128 10U_0805_25V6K
PC7 0.01U_0402_25V7K
PD2 @PJSOT24CW_SOT323-3
PR28 100_0402_1%
EC_SMB_CK1 40,44
PR31 100_0402_1%
EC_SMB_DA1 40,44
PR29 100K_0402_5%
+3VALW
PR30 1K_0402_1%
BATT_TEMPA 40

B+
+VSBP
PR13 100K_0402_1%
PC8 0.22U_0603_25V7K
PQ3 TP0610K-T1-E3_SOT23-3
PC9 0.1U_0603_25V7K
VL
PR14 22K_0402_1%
VSB_N_001
PR16 100K_0402_1%
PR18 0_0402_5%
VSB_N_003
VSB_N_002
45 POK
PQ4 SSM3K7002FU_SC70-3
PC10 .1U_0402_16V7K
+3VL
+CHGRTC
PJ3 JUMP_43X39

RTC Battery
PBJ1
@LOTES_AAA-BAT-054-K01
+RTCBATT

VIN
PD3 RLS4148_LL34-2
VS_N_001
BATT+
PD4 LL4148_LL34-2
PQ5 TP0610K-T1-E3_SOT23-3
PR19 68_1206_5%
PR20 68_1206_5%
N1
VS
PR23 100K_0402_1%
PC11 0.22U_0603_25V7K
PC12 0.1U_0603_25V7K
38 51_ON#
PR24 22K_0402_1%
VS_N_002

For KB9012 --> Remove all 51_ON# circuit

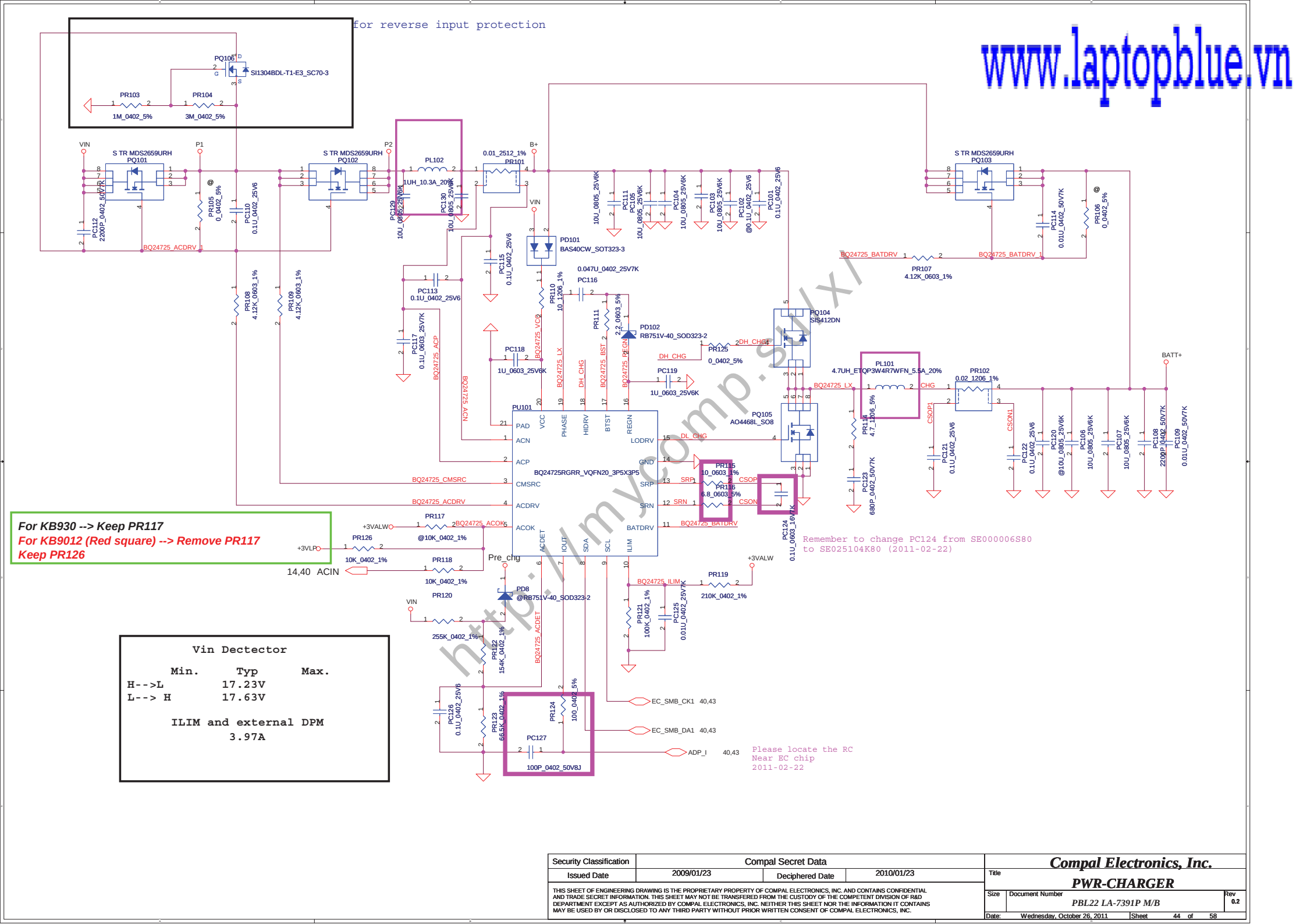
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

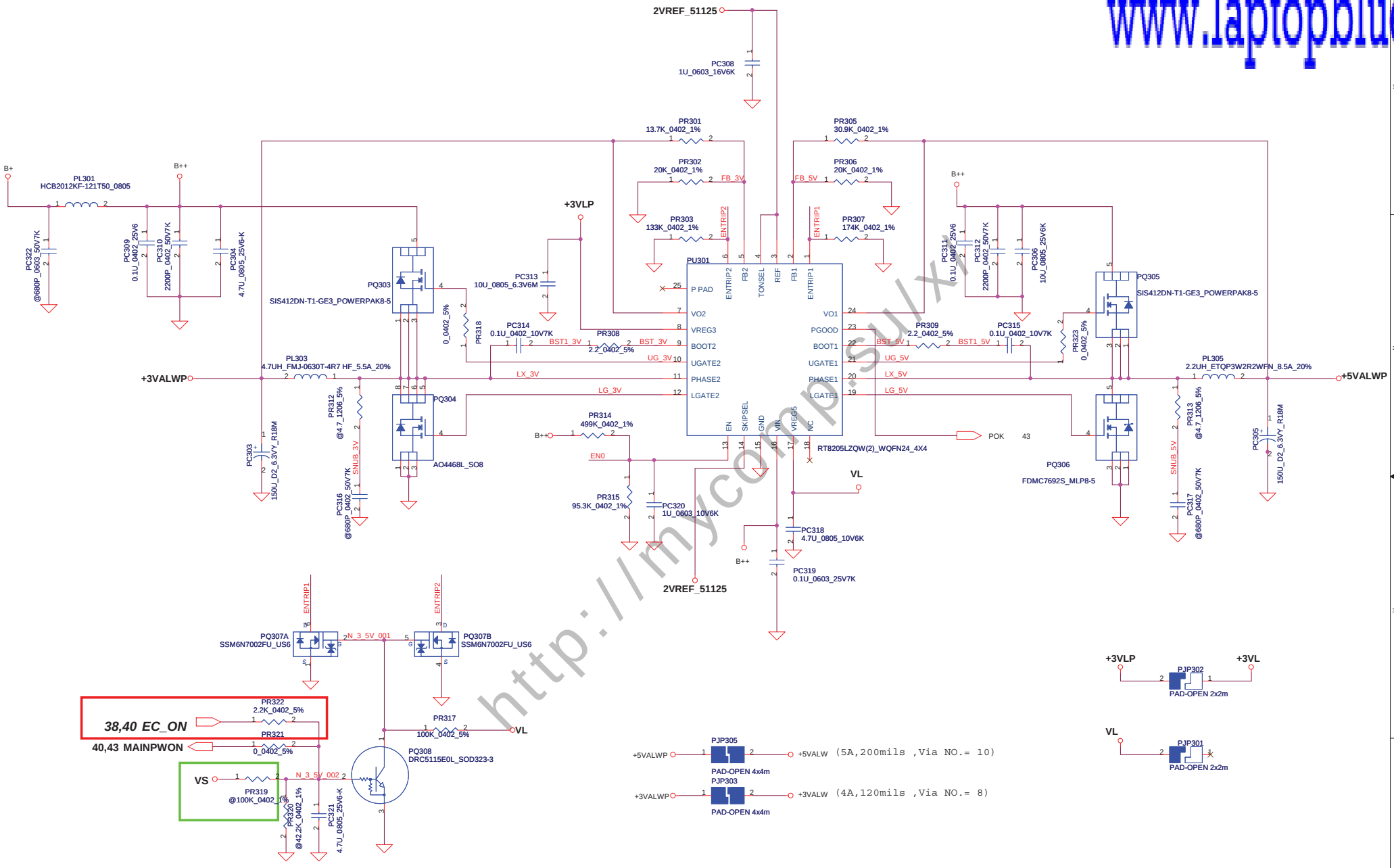
Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 43 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PWR-CHARGER		
Size	Document Number	PBL22 LA-7391P M/B	Rev 0.2
Date: Wednesday, October 26, 2011	Sheet 44 of 58		



For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

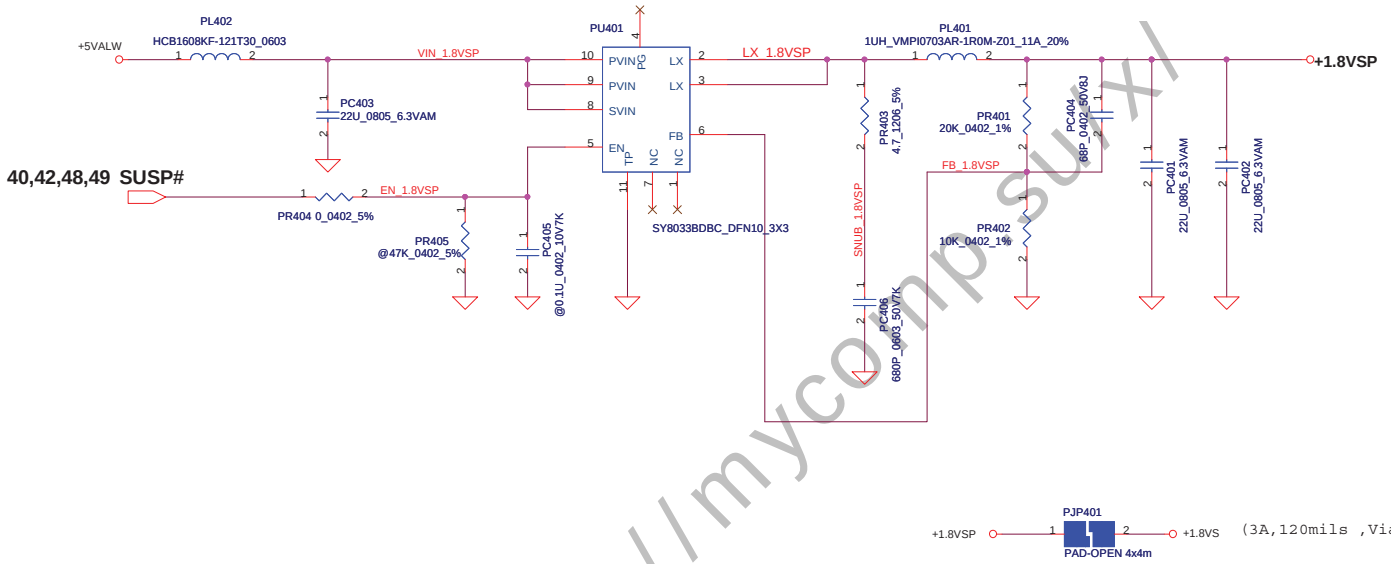
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 45 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PWR-1.8VSP**

Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 46 of 58

(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

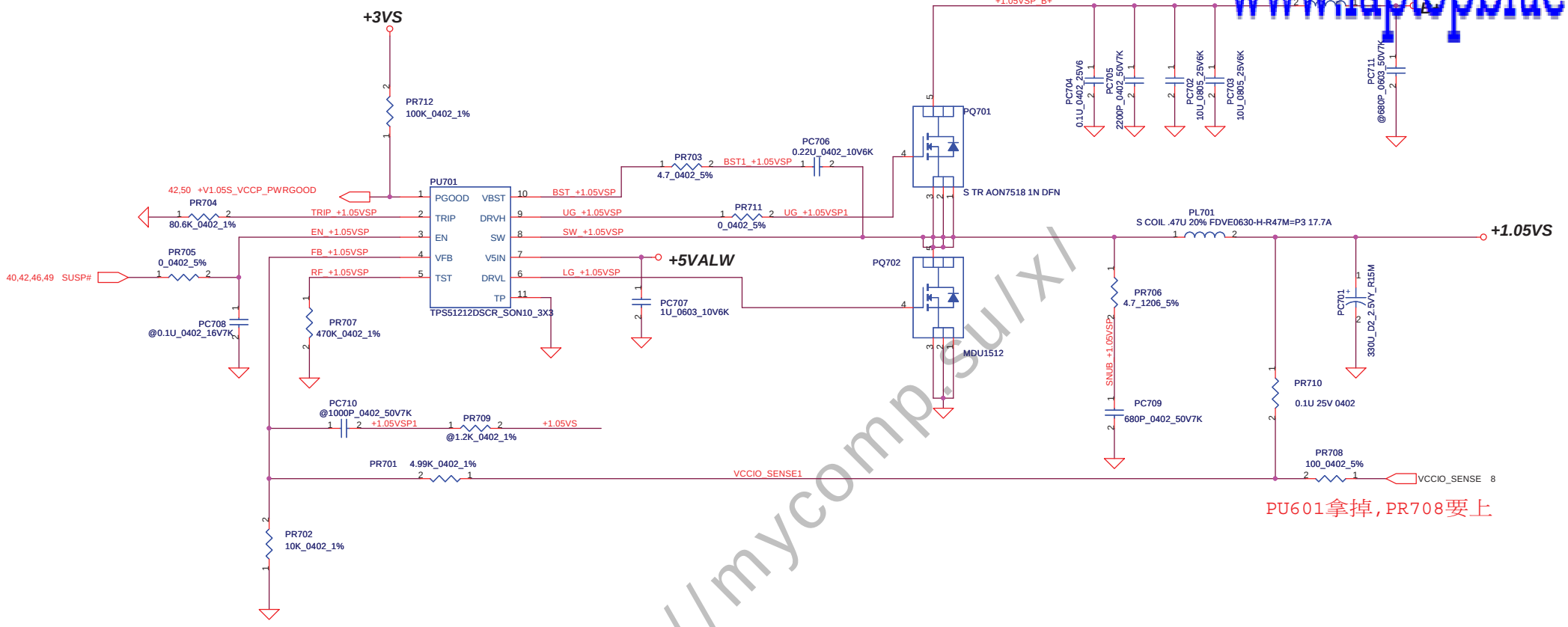
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PWR-V1.05S_VCCP**

Size: Custom | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 47 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

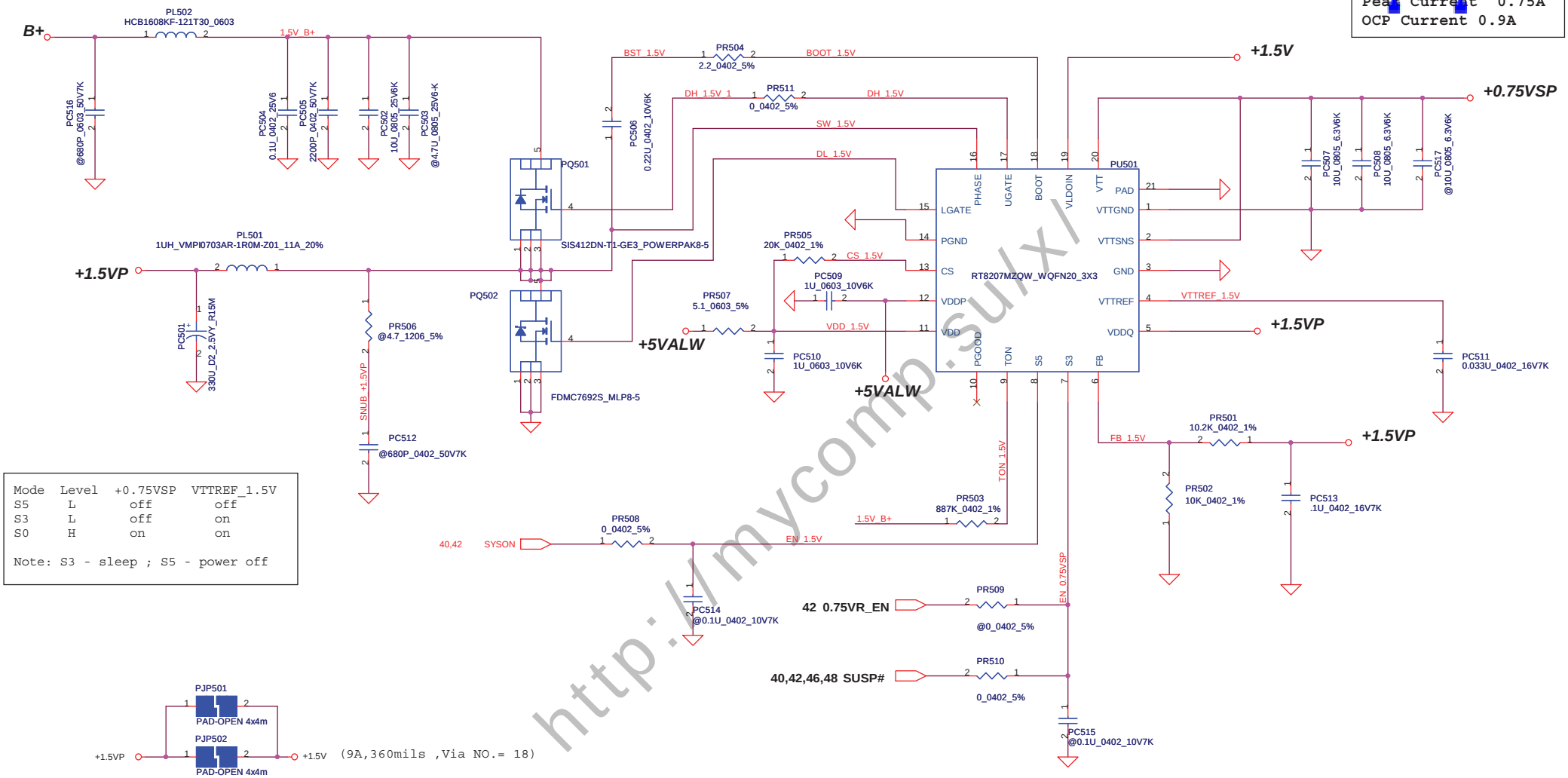
Compal Electronics, Inc.

Title: **PWR-V1.05SP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 48 of 58

0.75VOUT +/- 5%
Iout 0.25A
Peak Current 0.75A
OCP Current 0.9A



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

Size: Custom | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

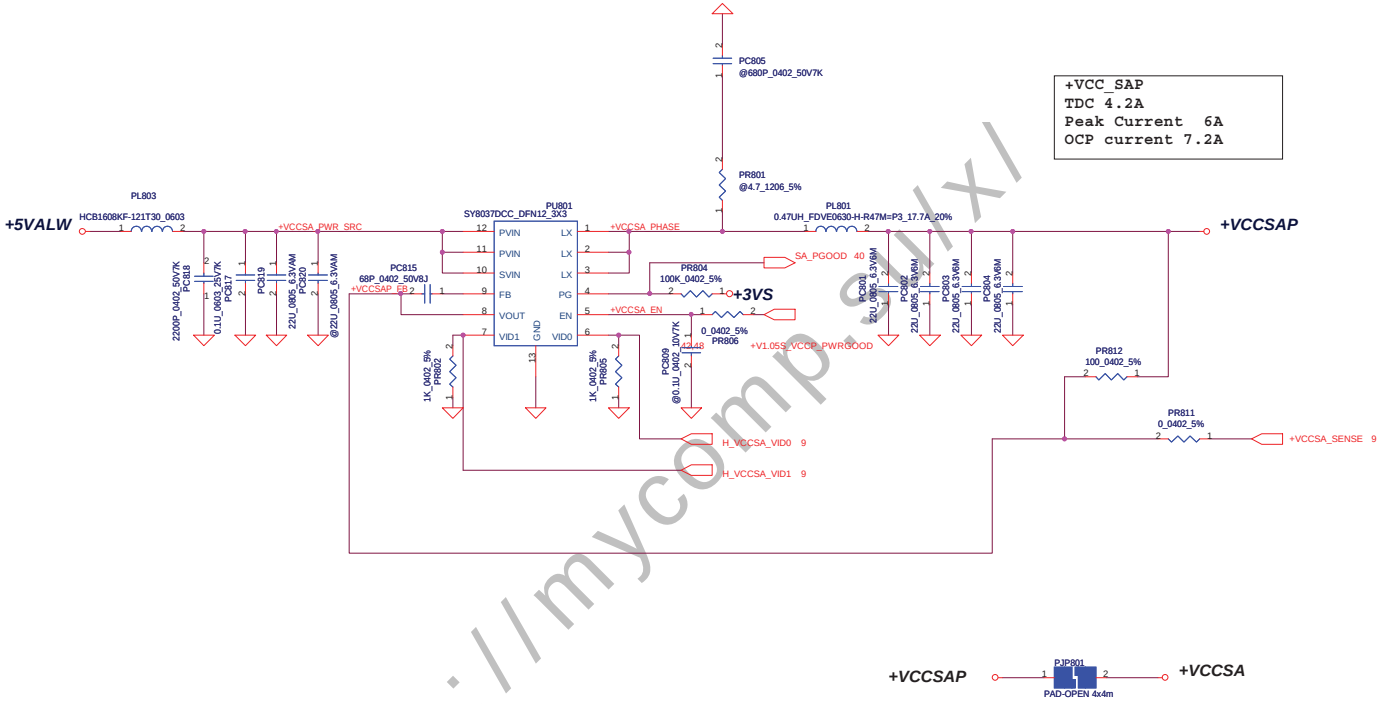
Date: Wednesday, October 26, 2011 | Sheet 49 of 58

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



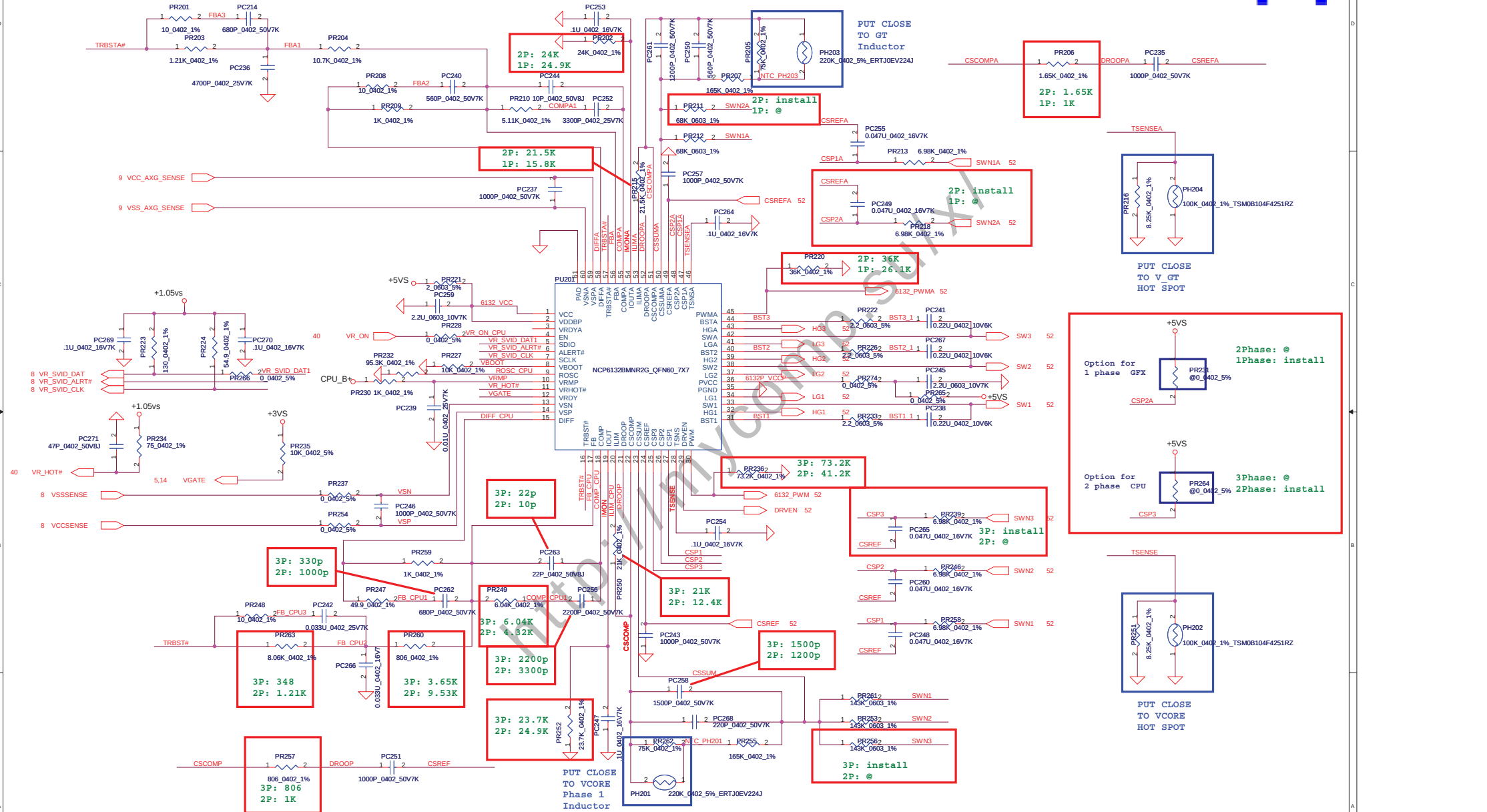
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size	Document Number	Rev
C	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 50 of 58



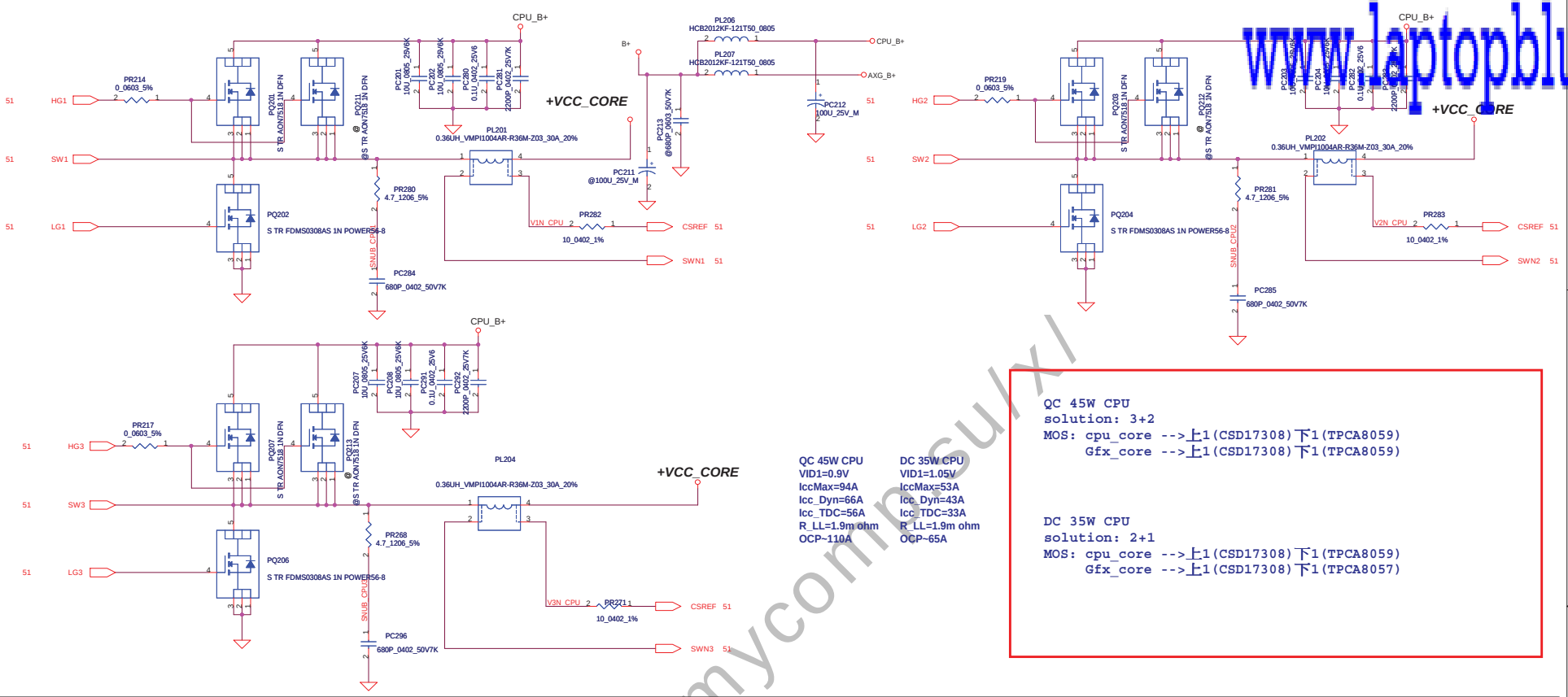
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 51 of 58

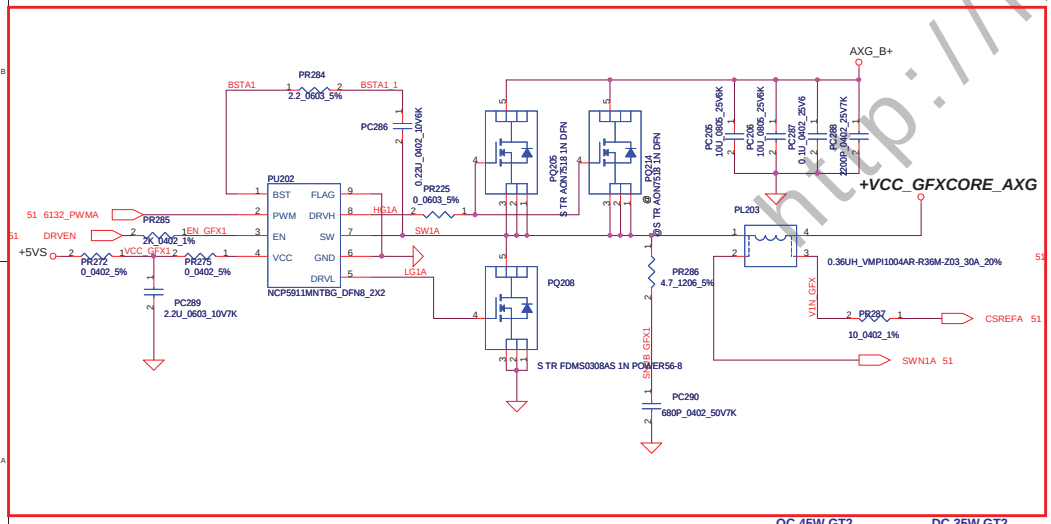


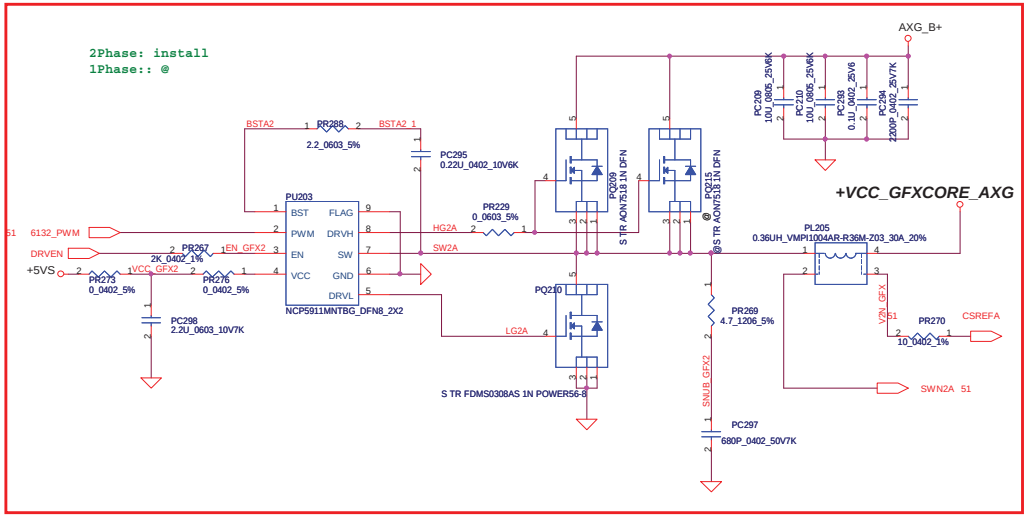
QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=56A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=33A
R_LL=1.9m ohm
OCP~65A

QC 45W CPU
solution: 3+2
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8057)





QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
C	PBL22 LA-7391P M/B	0.2

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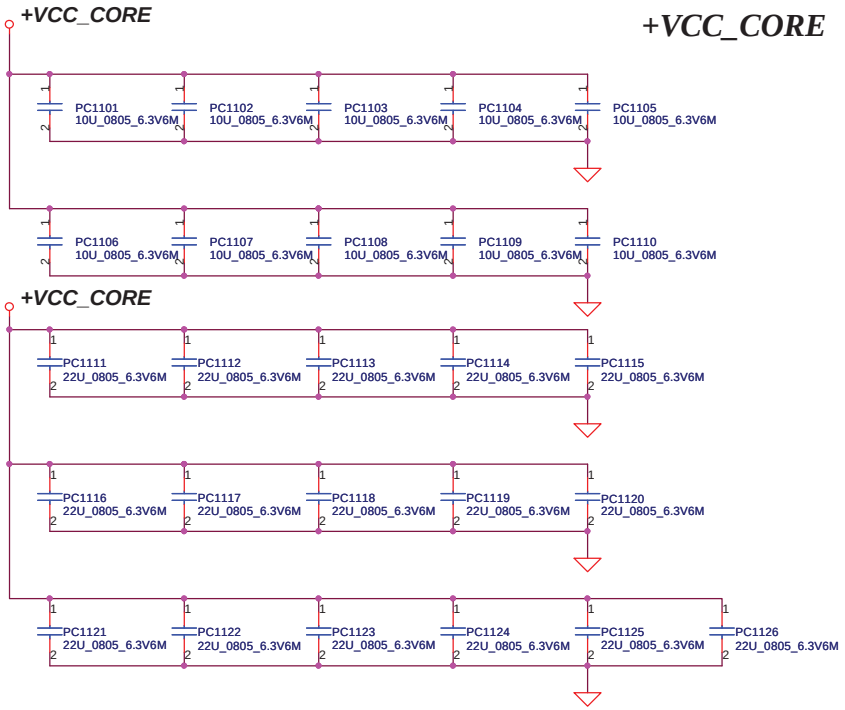
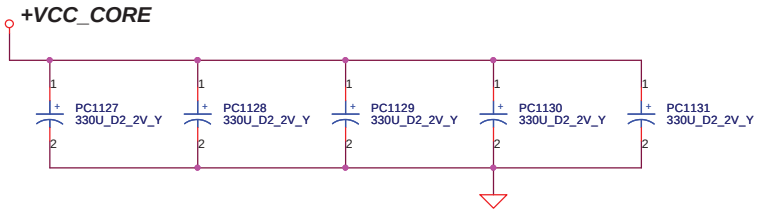
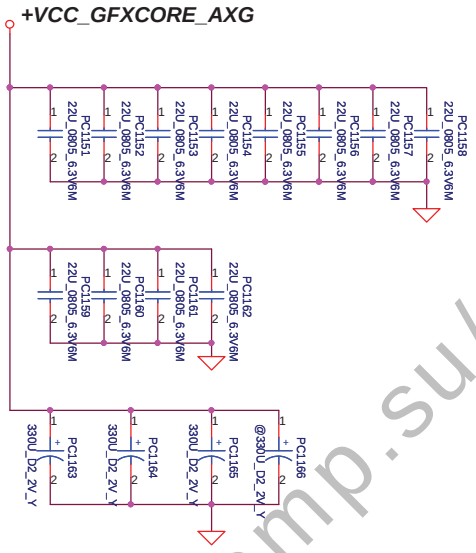
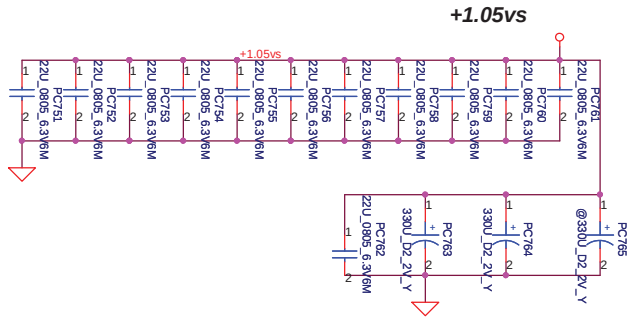
Below is 45[illegible]DDG[illegible]

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites









Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-8221P	0.2

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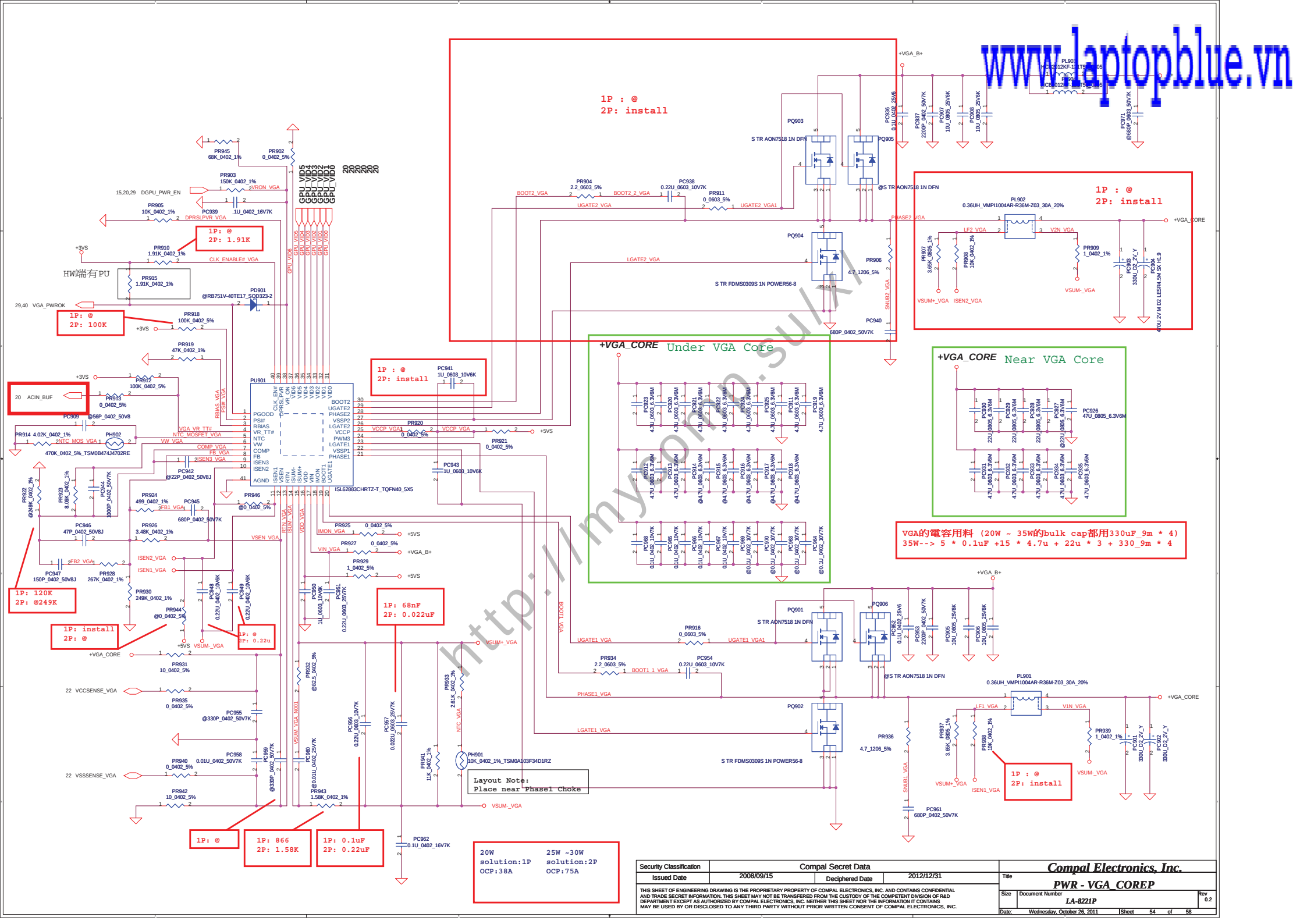

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PWR - VGA_COREP		
Size	Document Number		Rev
	LA-8221P		0.2
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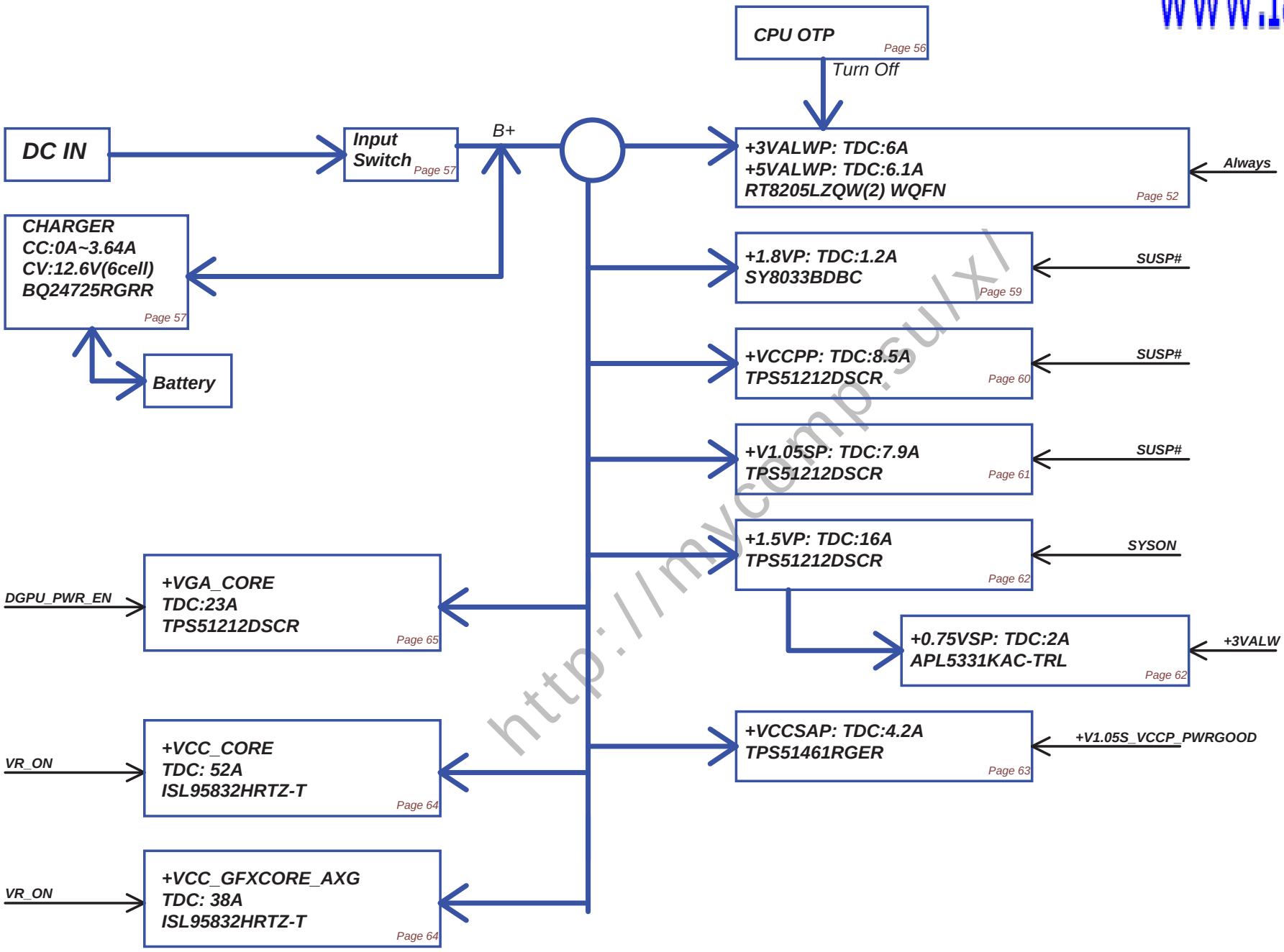
Power block



Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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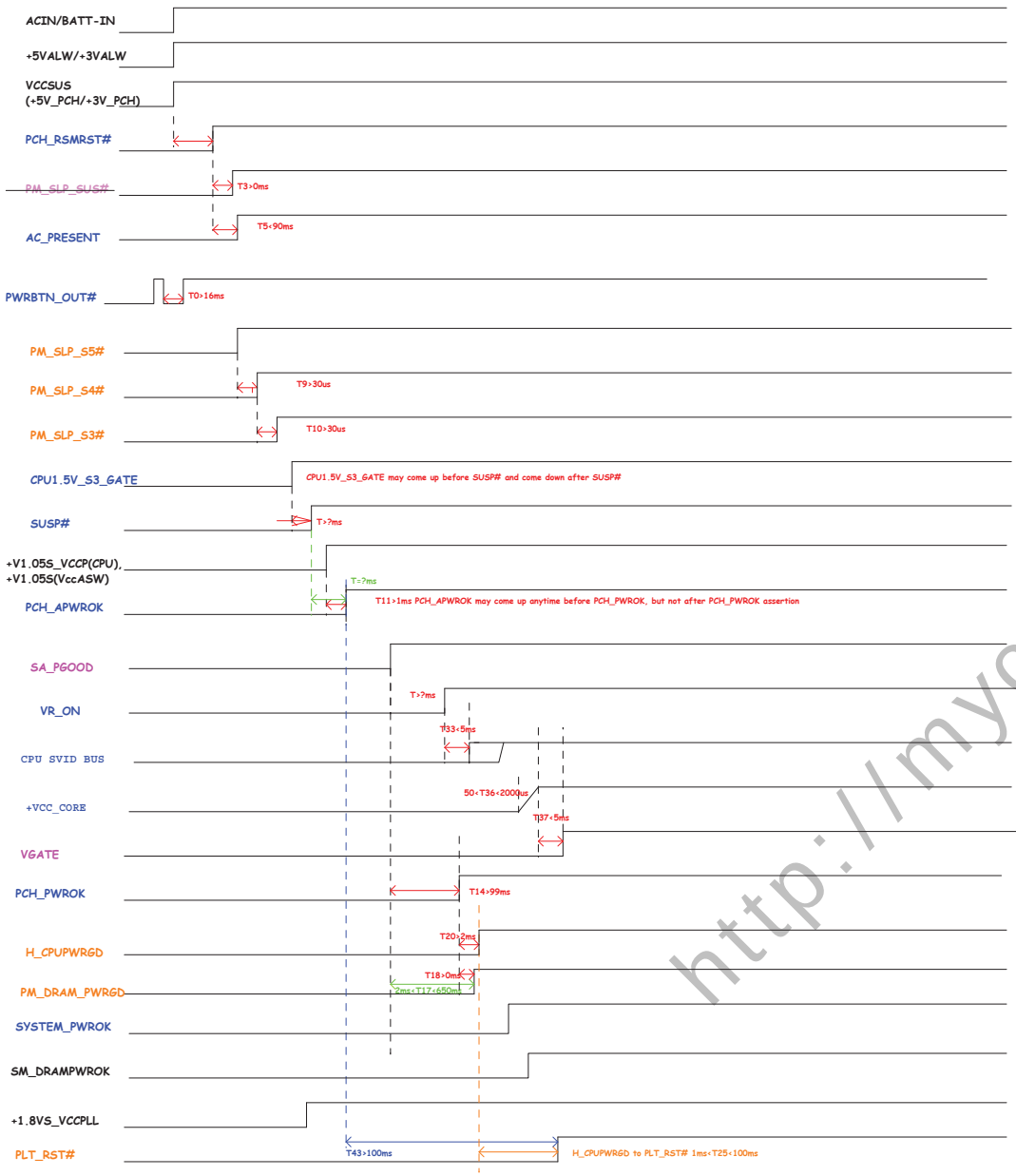
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Security Classification	Compal Secret Data		
Issued Date	2009/12/05	Deciphered Date	2011/12/31

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Title: Power Sequence

Size: A3 | Document Number: LA-8221P | Rev: 0.4

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Version Change List (P. I. R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		Add USB3.0(ASM1042) & non AI co-lay	0.2	36 37	Add ASM1042 co-lay AI parts change to AI@	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13 40	Delete Q3. (connect pin S & D) remove R135, R137 Del R552, R556	09/21	
ER04		Design change for card reader	0.2	34	Add Q20,R773,R775 Reserve R768,R774. Change Net name at Card reader Conn	09/21	
ER05		HW Design (PURC demand)	0.2	29	Change to Q3(AO3404L) from U22(AO4430L)	09/21	
ER06		HW Design (PURC demand)	0.2	42	Change Q33 to AO3413L from AP2301GN	09/21	
ER07		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER08		HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER09	KB connector reverse	HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER10		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER11		HW Design (PURC demand)	0.2	15	Del R229,R230 (10K) Add R776~R783 (10K) Del R237,R239,R242 (8.2K) Add R784~R793 (8.2K)	09/30	
ER12		HW Design (PURC demand)	0.2	29,31 37,38 10,11	Change P/N C387,C389,C399,C436,C447,C602 Change P/N C509,C515,C518,C526.(0402) Change P/N C99,C109,C118,C120,C140,C141.(0402)	10/03	
ER13		HW Design(XTAL fine-tune)	0.2	42,12 13,32 20,36	Change R607 to 10 ohm Change Y3,C241,C242. Change Y1,C144,C145 Change Y4,C469,C473. Change Y2,C163,C164 Change Y9	10/07	
ER14		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER15		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
ER16		HW Design (PURC demand)	0.2		Change P/N Q7,U20,U21. Change P/N Q14~Q19,Q25,Q27~Q29,Q32,Q34~Q37,Q40~Q43, Q46~Q51,Q55~Q57,Q60,Q61,Q902,Q903,Q905. Change P/N Q23	10/14	
ER17		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER18		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER19		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	
ER20		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R242 Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER21		Modify H2 size	0.2	38	Modify H2 size	10/17	

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title	EE-PIR-1		
Size: Custom	Document Number: LA-8221P		Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 58 of 58		

Version Change List (P. I. R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER22		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER23		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER24		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER25		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER26		For EMI request	0.2	36	Reserve R1082 , C1045	10/19	
ER27		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER28		For PRUC request	0.2	38 39	Change SW3,SW4,SW5 P/N	10/20	
ER29		For PRUC request	0.2	39	Change U36 P/N	10/20	
ER30		For EMI request (without MS_CLK)	0.2	34	Remove R637,C611,R631,C620.	10/20	
ER31		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER32		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER33		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER34		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641~C648	10/20	
ER35		For ESD request	0.2	37,35 30,39	Change D27,D29,D24,D25. Change D6,D7,D9,D10,D33,D34.	10/20	
ER36		Modify X76 table (N13P-GS)	0.2	22	update X76 table (Strap1,Strap2,Strap3)	10/24	
ER37		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 ~ZZZ12 for N13P-GS & N13M-GE1 x8) & update P/N	10/25	
ER38		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	

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Title: EE-PIR-2
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