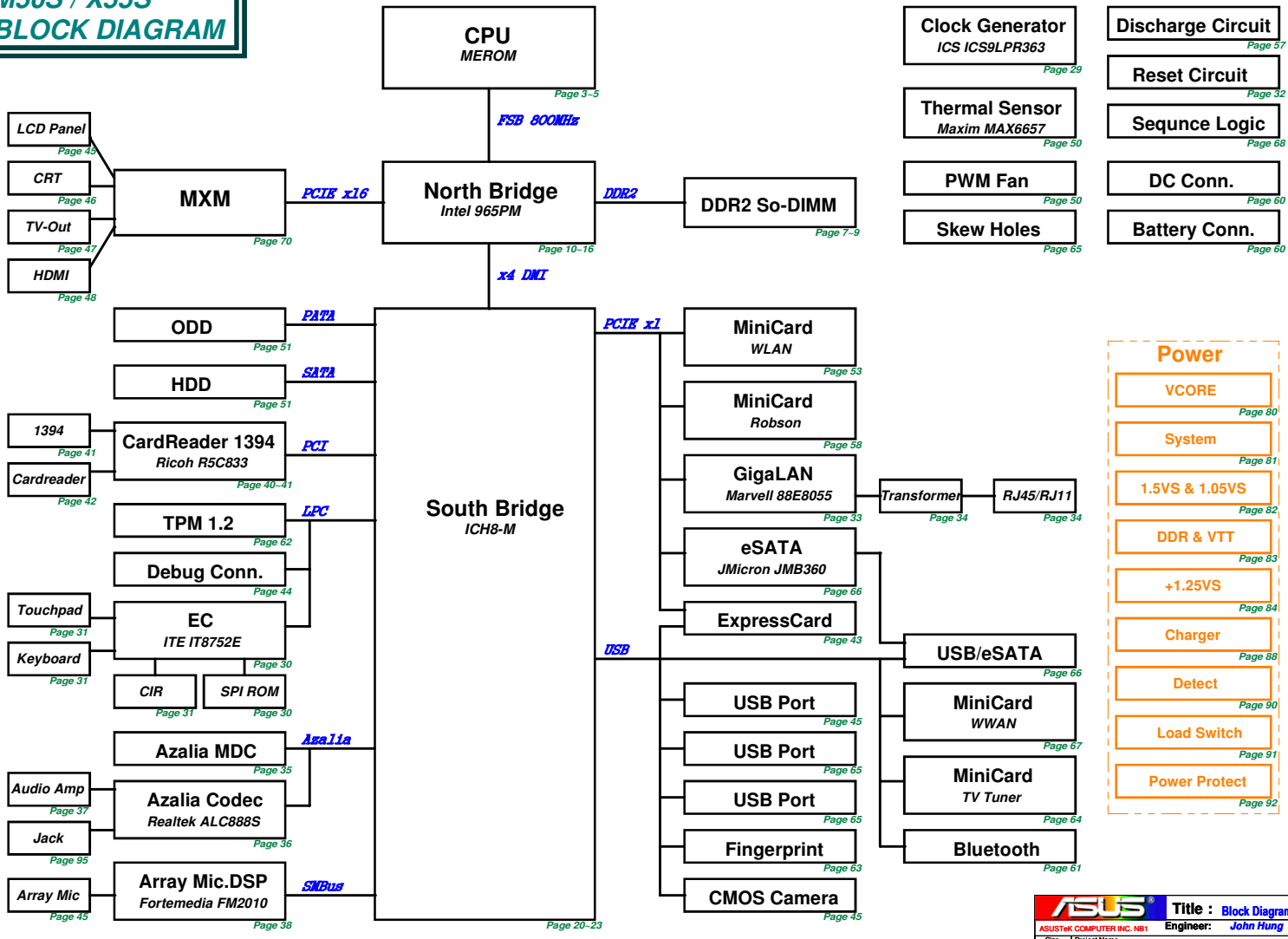


M50S / X55S BLOCK DIAGRAM



ASUS		Title : Block Diagram	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	1 of 88

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIROF#/GPIO3	PCI_INTF#	I/OD
F12	PIROG#/GPIO4	PCI_INTG#	I/OD
B3	PIROH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLG_GPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLG_GPIO2/GPIO14		
AE20	STP_PC#/GPIO15	STP_PC#	I/O
AJ14	DPRSLVPR/GPIO16	PM_DPRSLVPR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0/GPIO21		
AG10	SCLK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLG_GPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8752E GPIO SETTING

Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
32	PWM1/GPA1	CHG_LED_UP#	O
29	PWM2/GPA2		
33	PWM3/GPA3		
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
36	PWM6/GPA6		
38	PWM7/GPA7		
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
139	CTX0/GPB2		
124	SMCLK0/GPB3	SMB0_CLK	I/O
125	SMDAT0/GPB4	SMB0_DAT	I/O
42	GA20/GPB5	A20GATE	O
4	KBRST#/GPB6	RC_IN#	O
126	GPB7	PM_RSMRST#	O
133	CRX0/GPC0	CRX0	I
129	SMCLK1/GPC1	SMB1_CLK	I/O
130	SMDAT1/GPC2	SMB1_DAT	I/O
64	GPC3	PM_PWRBTN#	O
136	WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	WUI3/GPC6	BAT1_IN_OC#	I
20	GPC7	RFON_SW#	I
22	WUI0/GPD0	PWRLIMIT#	I
25	WUI1/GPD1	PM_SUSC#	I
26	WUI4/GPD2	BUF_PLT_RST#	I
27	ECSCI#/GPD3	EXT_SCI#	O
19	GPD4	GPC7	O
37	GPD5	LCD_BACKOFF#	O
53	TACH0 / GPD6	FANO_TACH	I
54	GPD7		
23	GPE0	VSUS_ON	O
94	GPE1	SUSC_EC#	O
95	GPE2	SUSB_EC#	O
96	GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	GPE6	LID_SW#	I
24	GPE7	INSTANT_ON#	I
97	PS2LK0/GPF0		
98	PS2DAT0/GPF1	COLOREN#	I
99	PS2CLK1/GPF2	MARATHON#	I
100	PS2DAT1/GPF3	DISSTP#	I
101	PS2CLK2/GPF4	TP_CLK	I/O
102	PS2DAT2/GPF5	TP_DAT	I/O
131	SMCLK2/GPF6	THRO_CPU	O
132	SMDAT2/GPF7	TP_LED	O
118	WUI7/GPG0		
121	GPG1	PM_SUSB#	I
112	GPG2		
116	GPG6		

965GM/PM co-layout option:

965PM

Change:
U1001 to 965PM, U3601 to ALC888S
R1213-R1219 to 0ohm
C1406, C1501-C1504, C1506-C1507, C1510, C1514 to 0ohm

Mount:
D4801-D4803
F4801
J4801, J7001
H7001-H7004
Q4801
R1112-R1117, R1203-R1212, R1502, R2910, R3618-R3620, R4801-R4804
RX2901-RX2902, RX4801-RX4810
CX1201-CX1232

Un-mount:
R1202, R1401-R1403, R1501, R1503-R1505, R2909, R3621, R7001-R7008
RN7001-RN7011
RNX1201, RNX2901, RNX2915
L1501-L1505
C1404-C1405, C1407-C1409, C1505, C1509, C1511-C1513
CE1404, CE1501-CE1503

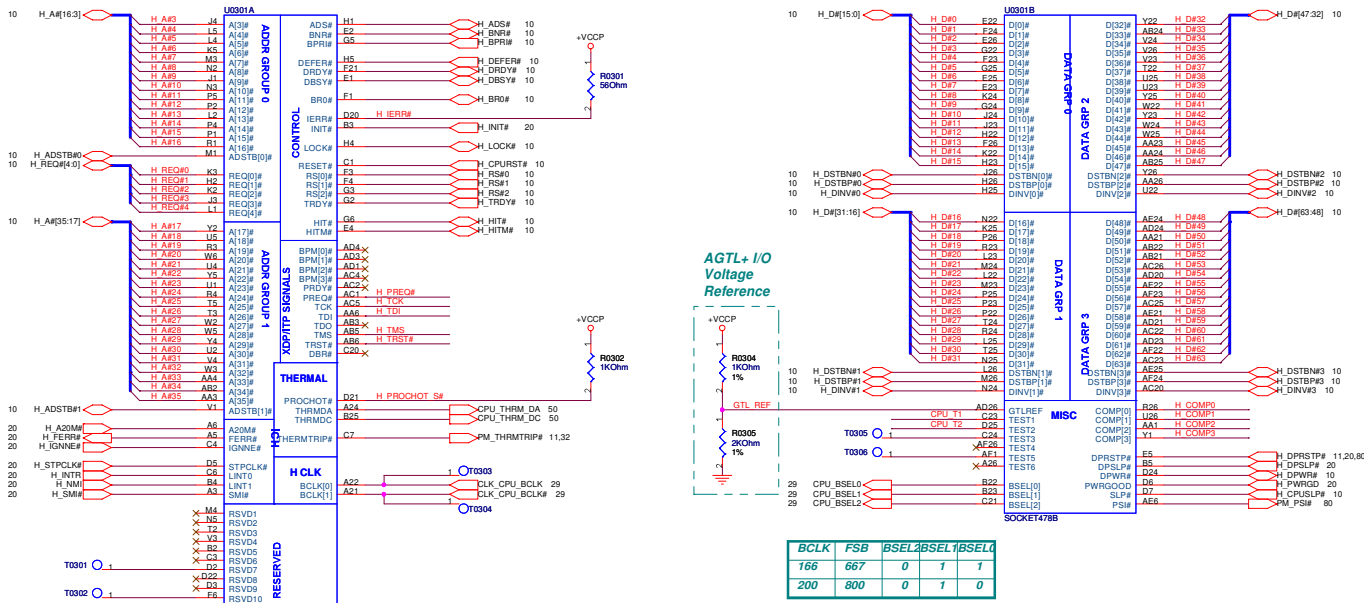
965GM

Change:
U1001 to 965GM
R1213-R1218 to 150ohm
R1219 to 1.3Kohm

Un-mount:
D4801-D4803
F4801
J4801, J7001
H7001-H7004
G4801
R1112-R1117, R1203-R1212, R1502, R2910, R3618-R3620, R4801-R4804
RX2901-RX2902, RX4801-RX4810
CX1201-CX1232

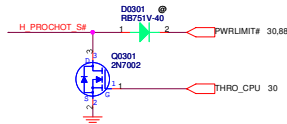
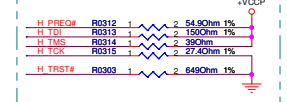
Mount:
R1202, R1401-R1403, R1501, R1503-R1505, R2909, R3621, R7001-R7008
RN7001-RN7011
RNX1201, RNX2901, RNX2915
L1501-L1505
C1404-C1409, C1501-C1507, C1509-C1514
CE1404, CE1501-CE1503

		Title : System Setting	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet 2 of 55	

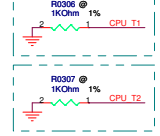


BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0

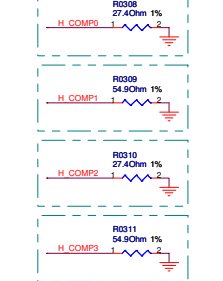
Default Strapping When XDP/ITP Not Used



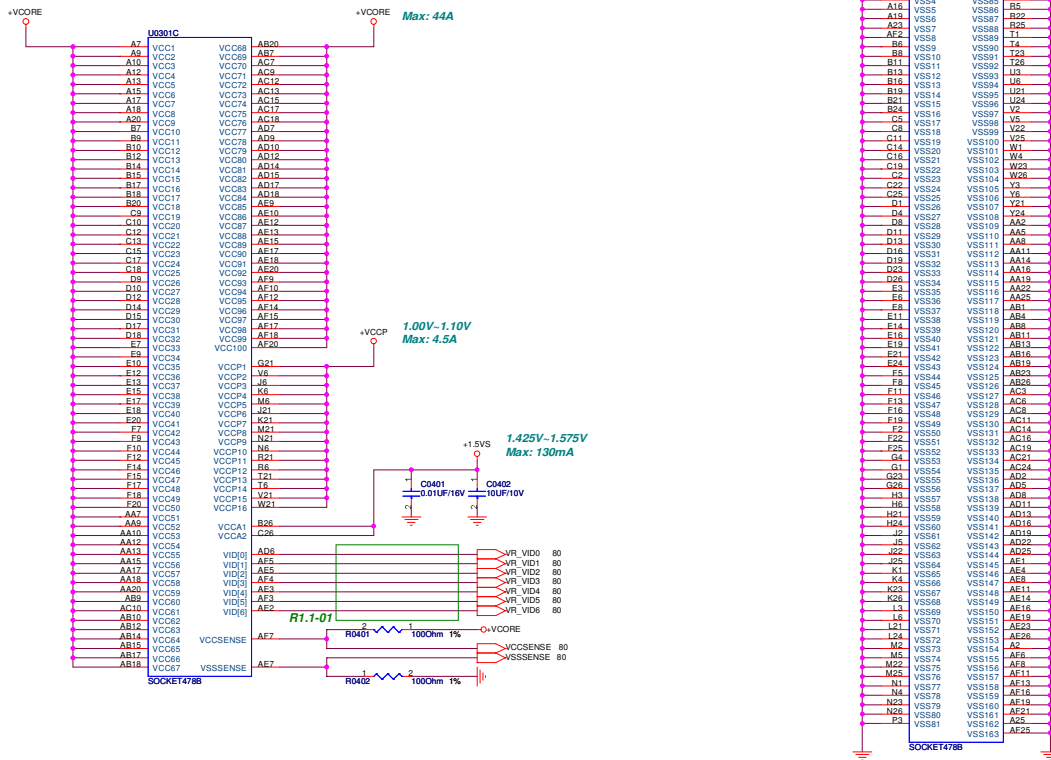
CPU Test Pin



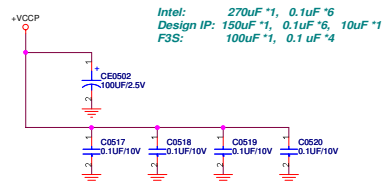
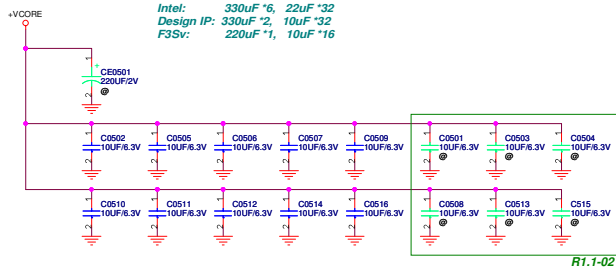
AGTL+ I/O Buffer Compensation



ASUS Title : CPU_Merom(Host)
ASUSTeK COMPUTER INC. NBI Engineer: John Hung
 Size: Project Name: M50S/X55S Rev: 2.0
 Date: Monday, September 03, 2007 Sheet: 3 of 88

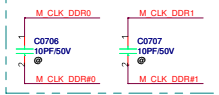


ASUS Title : CPU_Merom(PWR)
 ASUSTek COMPUTER INC. NBI Engineer: John Hung
 Sub Project Name
 Custom M50S/X55S
 Date: Monday, September 03, 2007 Sheet 4 of 55

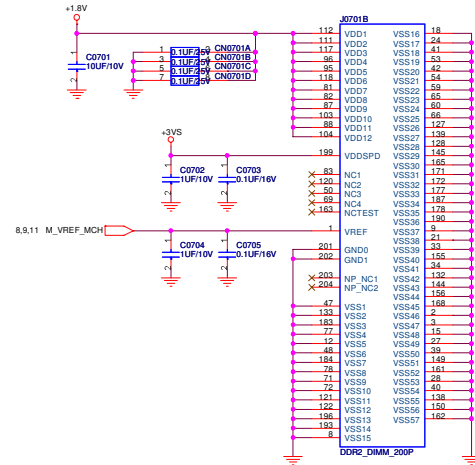
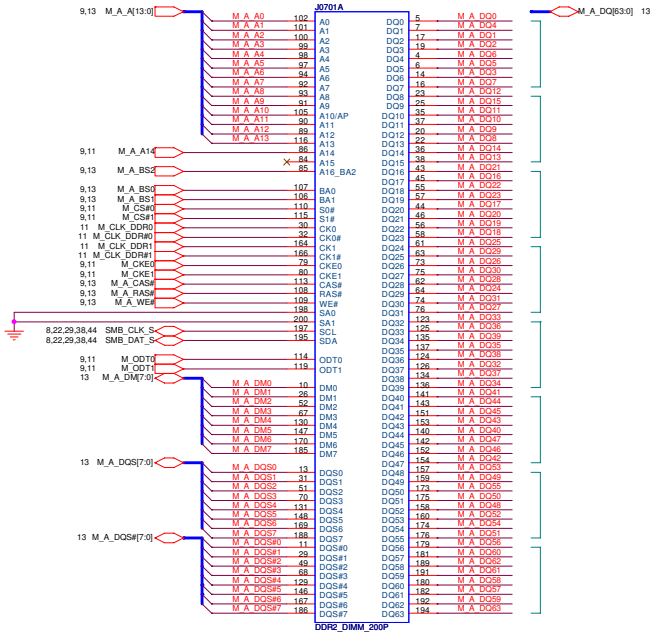


		Title : CPU_Capacitors	
ASUSTeK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	5 of 88

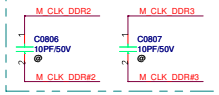
Reserved for 3G



Reverse Type
H = 9.2 mm

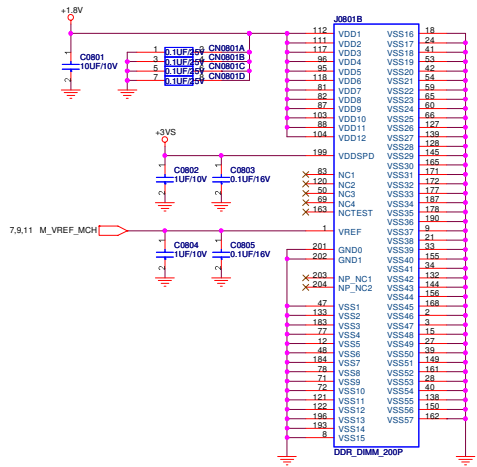
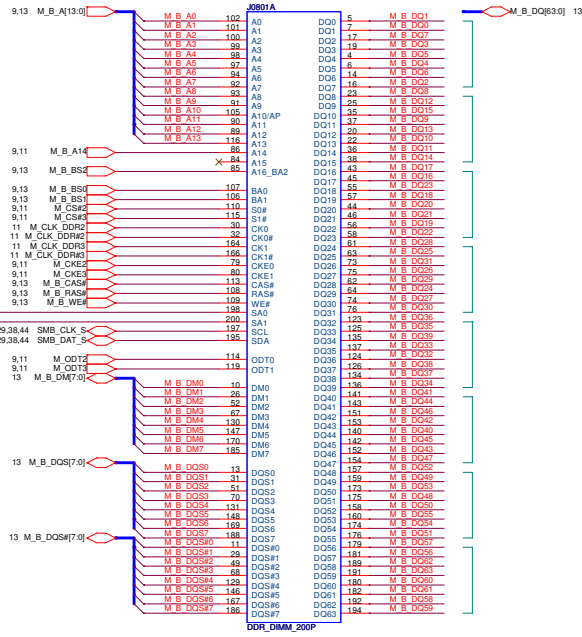


Reserved for 3G

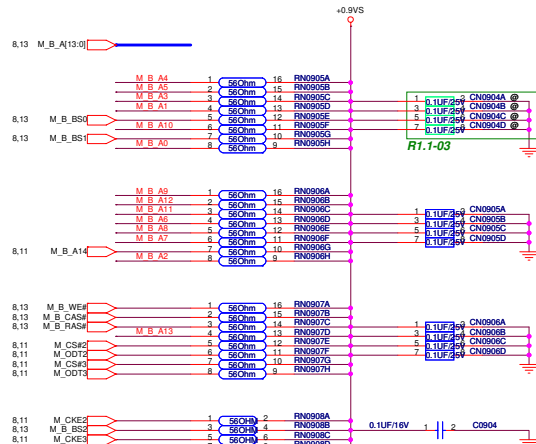
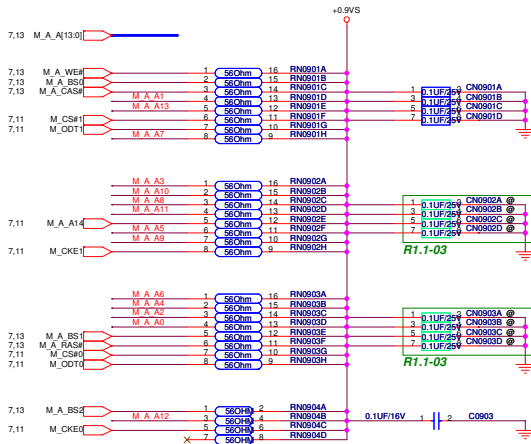
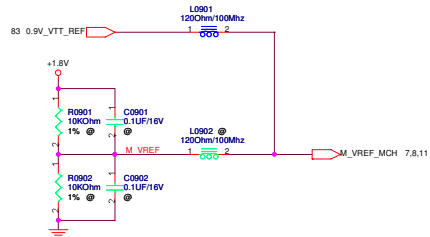


Reverse Type

H = 4.0 mm

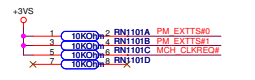
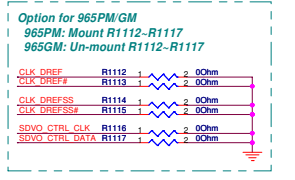
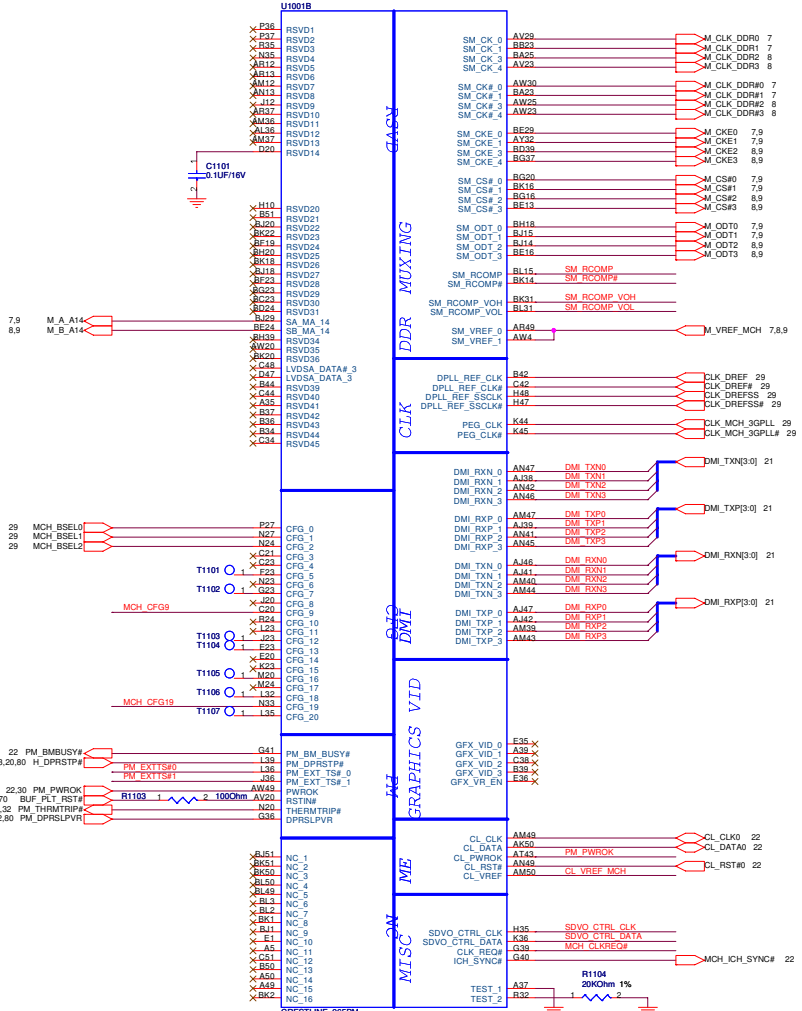


ASUS Title : DIM So-DIMM 1
 ASUSTEK COMPUTER INC. (NBI) Engineer: John Hung
 Project Name: M50S/X55S Rev: 2.0
 Date: Monday, September 03, 2007 Sheet: 8 of 88



ASUS Title : DIM_DDR2 Termination
 ASUSTek COMPUTER INC. NBI Engineer: John Hung
 Project Name: M50S/X55S
 Date: Monday, September 03, 2007 Sheet 9 of 88

- CFG5 : DMI Strap**
 0 = DMI x2
 1 = DMI x4 (D)
- CFG7 : CPU Strap**
 0 = Reserved
 1 = Mobile CPU (D)
- CFG9 : PCIe Graphic Lane**
 0 = Reverse Lane
 1 = Normal Operation (D)
- CFG13:12 : GMCH Test Mode**
 00 = Partial CLK Gating Disable
 01 = XOR Mode Enable
 10 = All Z Mode Enable
 11 = Normal Operation (D)
- CFG16 : FSB Dynamic ODT**
 0 = Dynamic ODT Disable
 1 = Dynamic ODT Enable (D)
- CFG18 : Core Voltage**
 0 = 1.05V (D)
 1 = 1.5V
- CFG19 : DMI Lane Reversal**
 0 = Normal Operation (D)
 1 = Lanes Reversed
- CFG20 : Concurrent SDVO / PCIe**
 0 = Only one is operational (D)
 1 = operate simultaneous

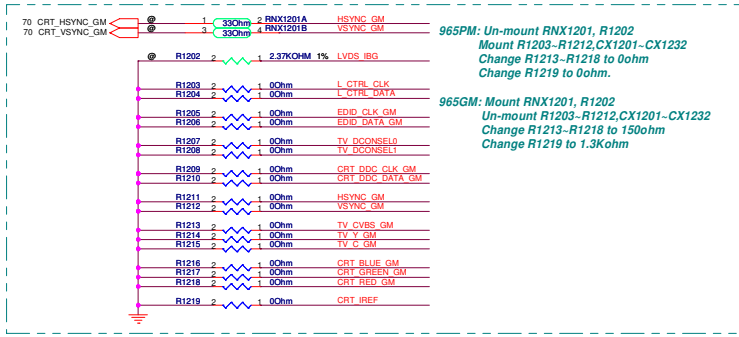
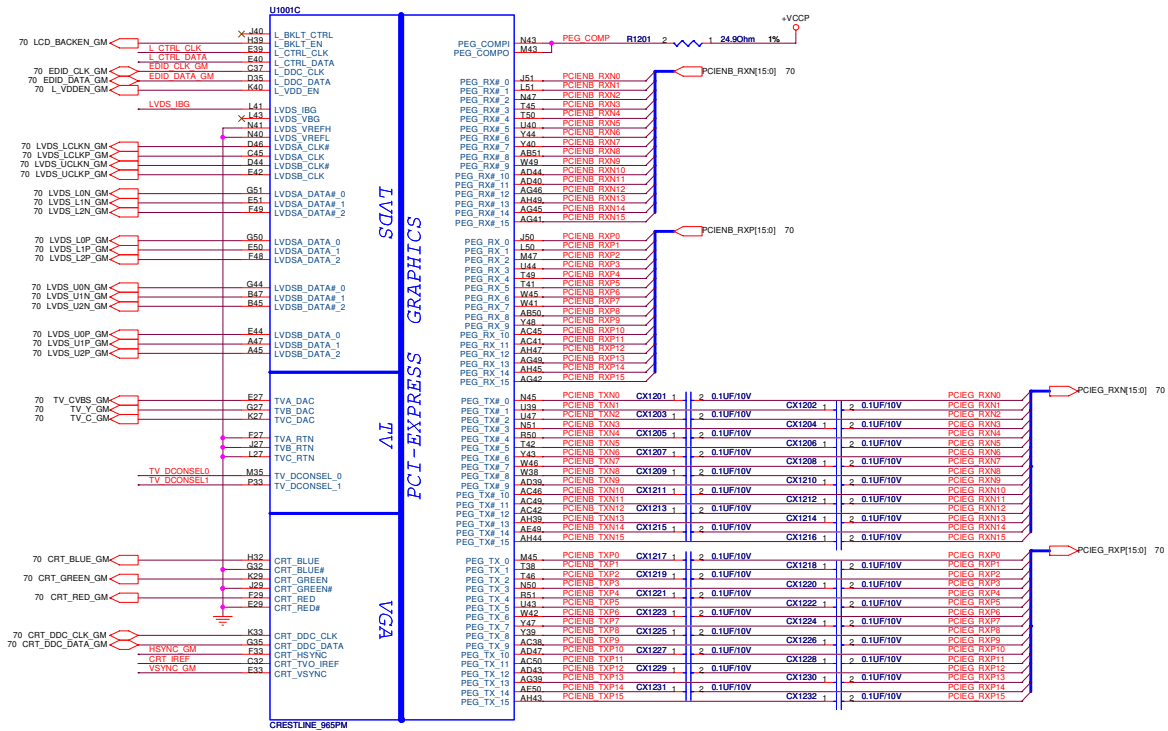


ASUS Title : NB_965PM(DM/CFG)

ASUSTek COMPUTER INC. NBI Engineer: John Hung

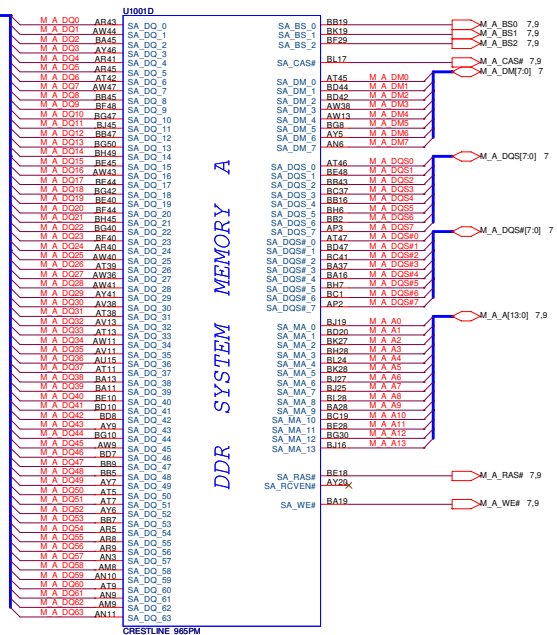
Size Project Name M50S/X55S Rev 2.0

Date: Monday, September 03, 2007 Sheet 11 of 85

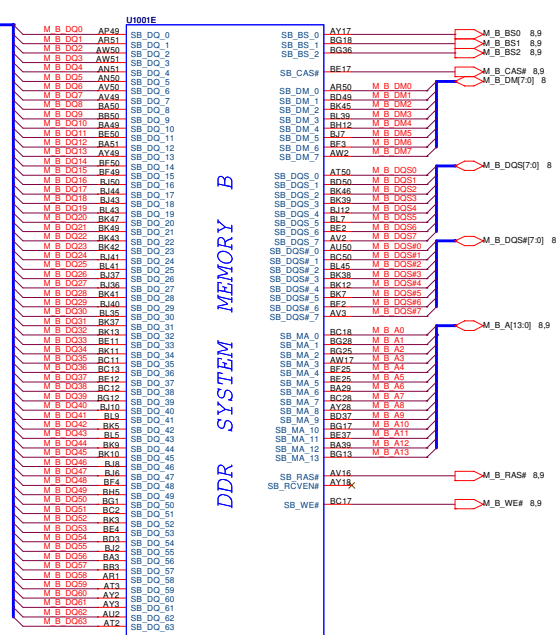


ASUS Title : NB_965PM(GFX)
 ASUSTek COMPUTER INC. NBI Engineer: John Hung
 Size Project Name
 Custom M50S/X55S Rev 2.0
 Date: Monday, September 03, 2007 Sheet 12 of 88

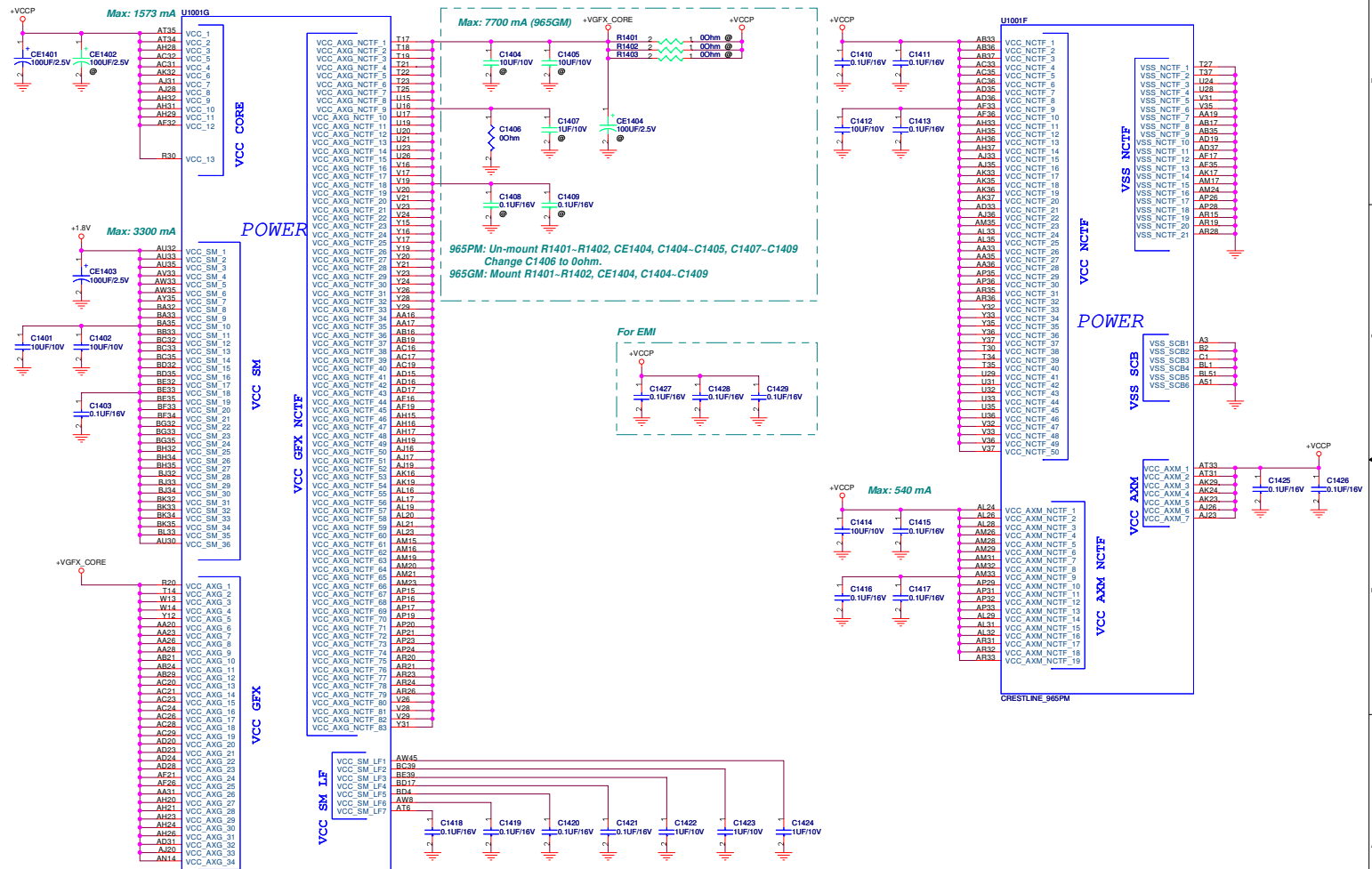
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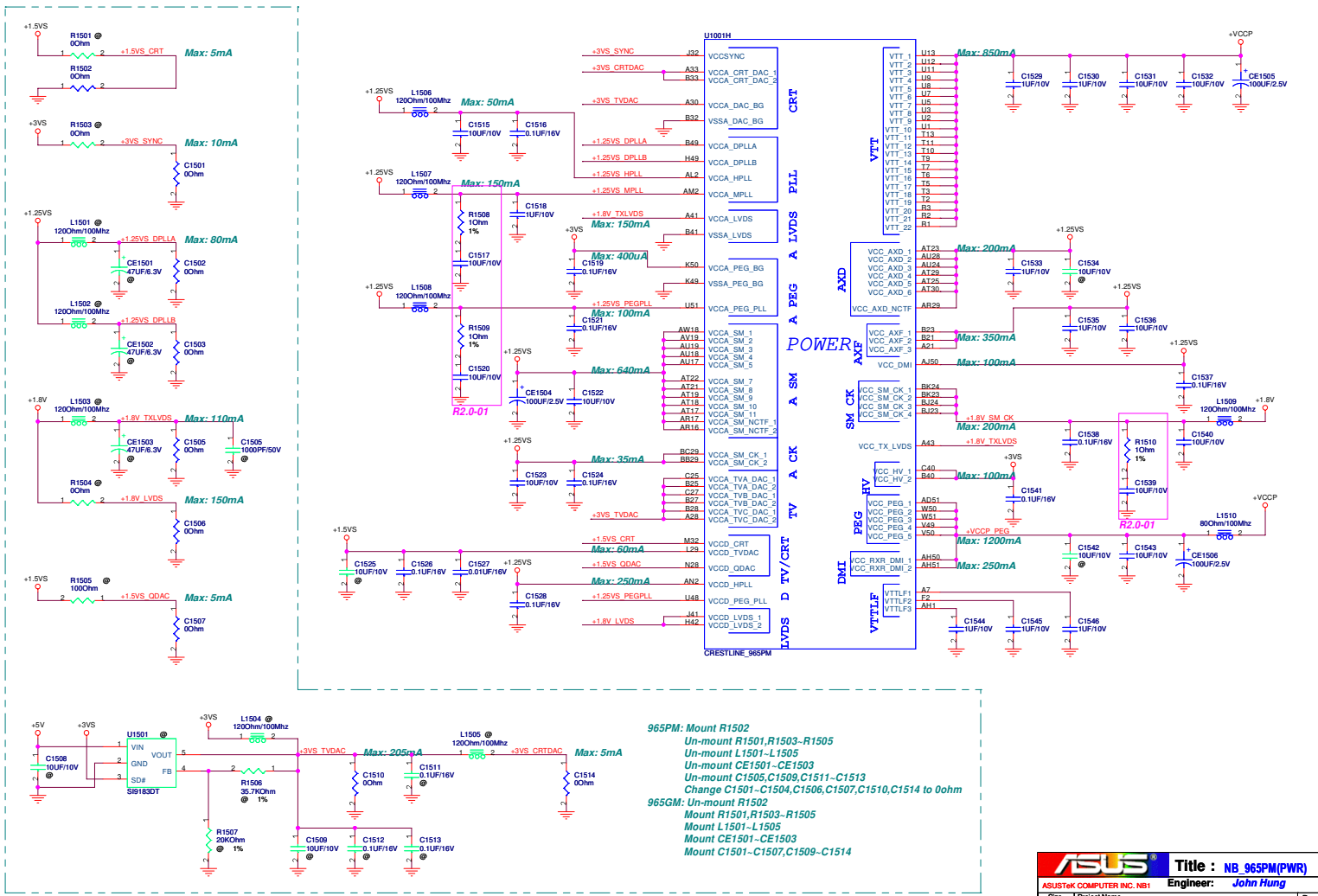
8 M_B_DQ[63:0]



ASUS Title : NB_965PM(DDR2)
 ASUSTEK COMPUTER INC. NBI Engineer: John Hung
 Sub Project Name
 Custom M50S/X55S
 Date: Monday, September 03, 2007 Sheet 13 of 35



ASUS		Title : NB_965PM(PWR)
ASUSTek COMPUTER INC. NB1	Project Name	Engineer: John Hung
Custom	Project Name	M50S/X55S
Date: Tuesday, September 04, 2007	Sheet	14 of 85



U1001J		AW24	
A13	VSS_1	VSS_100	AW24
A15	VSS_2	VSS_101	AW25
A17	VSS_3	VSS_102	AW26
A21	VSS_4	VSS_103	AW5
AA24	VSS_5	VSS_104	AW7
AA24	VSS_6	VSS_105	AV10
AB21	VSS_7	VSS_106	AV37
AB21	VSS_8	VSS_107	AV42
AB21	VSS_9	VSS_108	AV43
AB21	VSS_10	VSS_109	AV44
AB21	VSS_11	VSS_110	AV45
AB21	VSS_12	VSS_111	AV47
AC10	VSS_13	VSS_112	AV50
AC10	VSS_14	VSS_113	BL10
AC3	VSS_15	VSS_114	BL20
AC38	VSS_16	VSS_115	BL24
AD1	VSS_17	VSS_116	BL30
AD1	VSS_18	VSS_117	BL31
AD21	VSS_19	VSS_118	BL38
AD21	VSS_20	VSS_119	BL42
AD21	VSS_21	VSS_120	BL43
AD41	VSS_22	VSS_121	BL46
AD41	VSS_23	VSS_122	BL5
AD45	VSS_24	VSS_123	BL8
AD45	VSS_25	VSS_124	BL11
AD45	VSS_26	VSS_125	BL12
AD45	VSS_27	VSS_126	BL15
AD50	VSS_28	VSS_127	BL22
AD50	VSS_29	VSS_128	BL24
AD50	VSS_30	VSS_129	BL25
AE5	VSS_31	VSS_130	BL40
AE5	VSS_32	VSS_131	BL44
AF20	VSS_33	VSS_132	BL45
AF24	VSS_34	VSS_133	BL46
AF24	VSS_35	VSS_134	BL8
AF31	VSS_36	VSS_135	BL13
AG2	VSS_37	VSS_136	BL24
AG38	VSS_38	VSS_137	BL25
AG41	VSS_39	VSS_138	BL29
AG47	VSS_40	VSS_139	BL40
AG50	VSS_41	VSS_140	BL43
AH3	VSS_42	VSS_141	BL46
AH40	VSS_43	VSS_142	BL46
AH41	VSS_44	VSS_143	BL46
AH4	VSS_45	VSS_144	BL46
AH5	VSS_46	VSS_145	BL5
AH11	VSS_47	VSS_146	BL19
AH11	VSS_48	VSS_147	BL25
AH11	VSS_49	VSS_148	BL29
AH2	VSS_50	VSS_149	BL42
AH2	VSS_51	VSS_150	BL42
AH2	VSS_52	VSS_151	BL42
AH3	VSS_53	VSS_152	BL8
AH3	VSS_54	VSS_153	BL12
AH3	VSS_55	VSS_154	BL16
AK21	VSS_56	VSS_155	BL36
AK28	VSS_57	VSS_156	BL36
AK28	VSS_58	VSS_157	BL32
AK31	VSS_59	VSS_158	BL36
AK31	VSS_60	VSS_159	BL29
AK31	VSS_61	VSS_160	BL29
AL1	VSS_62	VSS_161	BL39
AM1	VSS_63	VSS_162	BL46
AM13	VSS_64	VSS_163	BL5
AM3	VSS_65	VSS_164	BL5
AM4	VSS_66	VSS_165	BL17
AM41	VSS_67	VSS_166	BL30
AM45	VSS_68	VSS_167	BL44
AN1	VSS_69	VSS_168	BL46
AN38	VSS_70	VSS_169	BL11
AN38	VSS_71	VSS_170	BL13
AN38	VSS_72	VSS_171	BL38
AN3	VSS_73	VSS_172	BL38
AN3	VSS_74	VSS_173	BL4
AP4	VSS_75	VSS_174	BL42
AP48	VSS_76	VSS_175	BL46
AP50	VSS_77	VSS_176	BL15
AR1	VSS_78	VSS_177	BL17
AR2	VSS_79	VSS_178	BL25
AR28	VSS_80	VSS_179	BL30
AR44	VSS_81	VSS_180	BL36
AR47	VSS_82	VSS_181	BL40
AR7	VSS_83	VSS_182	BL44
AT10	VSS_84	VSS_183	BL6
AT14	VSS_85	VSS_184	BL6
AT41	VSS_86	VSS_185	BL11
AT48	VSS_87	VSS_186	BL13
AU1	VSS_88	VSS_187	BL19
AU21	VSS_89	VSS_188	BL22
AU28	VSS_90	VSS_189	BL37
AU2	VSS_91	VSS_190	BL47
AU32	VSS_92	VSS_191	CL12
AU49	VSS_93	VSS_192	CL16
AU51	VSS_94	VSS_193	CL28
AV38	VSS_95	VSS_194	CL28
AV48	VSS_96	VSS_195	CL28
AW1	VSS_97	VSS_196	CL30
AW12	VSS_98	VSS_197	CL36
AW18	VSS_99	VSS_198	CL41

VSS

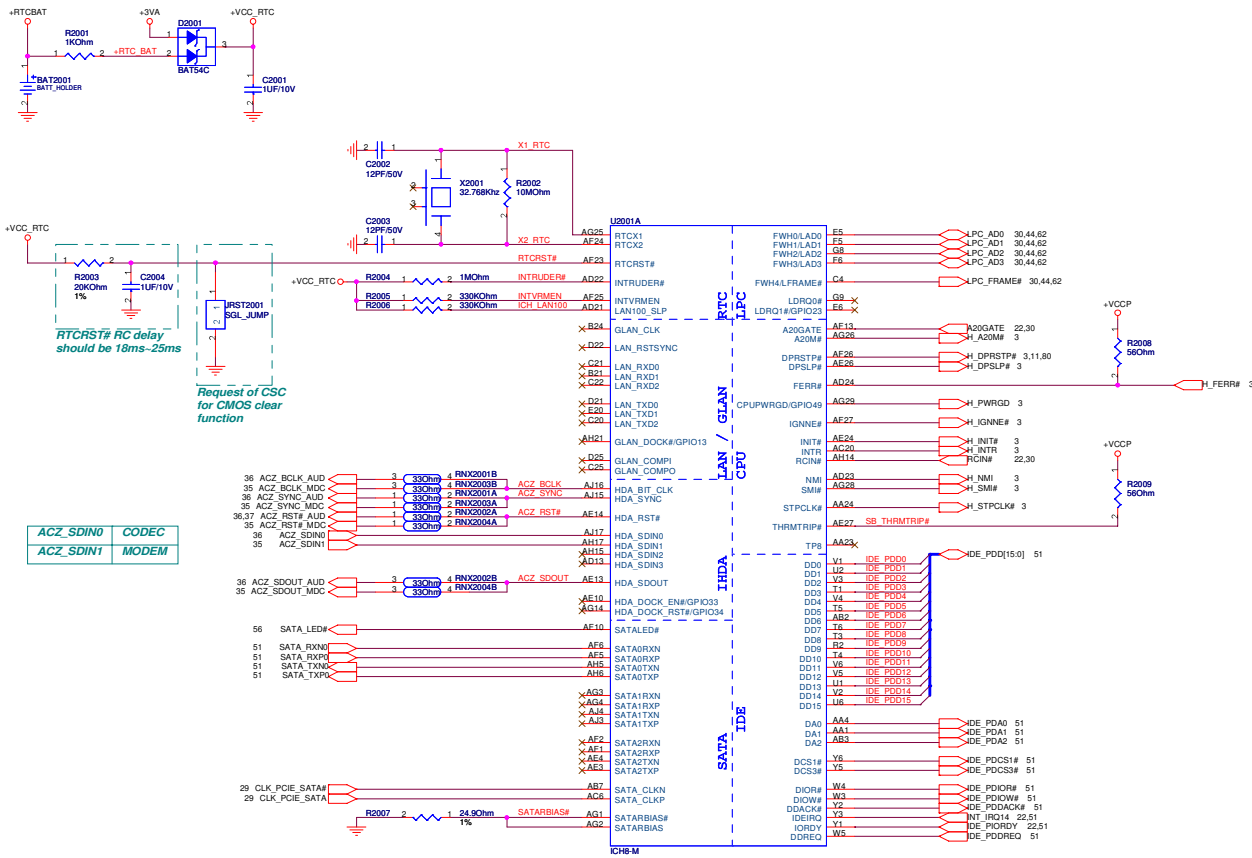
CRESTLINE_965PM

U1001J		W11	
C4	VSS_199	VSS_287	W39
C20	VSS_200	VSS_288	W39
C7	VSS_201	VSS_289	W43
D14	VSS_202	VSS_290	W47
D24	VSS_203	VSS_291	W5
D3	VSS_204	VSS_292	W7
D32	VSS_205	VSS_293	Y13
D38	VSS_206	VSS_294	Y2
D46	VSS_207	VSS_295	Y2
D48	VSS_208	VSS_296	Y41
E10	VSS_209	VSS_297	Y45
E16	VSS_210	VSS_298	Y49
E24	VSS_211	VSS_299	Y5
E28	VSS_212	VSS_300	Y50
E47	VSS_213	VSS_301	Y11
E50	VSS_214	VSS_302	Y28
F19	VSS_215	VSS_303	Y28
F4	VSS_216	VSS_304	T31
F49	VSS_217	VSS_305	T53
F50	VSS_218	VSS_306	R28
G13	VSS_219	VSS_307	AA32
G1	VSS_220	VSS_308	AB32
G16	VSS_221	VSS_309	AC32
G18	VSS_222	VSS_310	AF28
G24	VSS_223	VSS_311	AF29
G28	VSS_224	VSS_312	AV25
G32	VSS_225	VSS_313	HS0
G38	VSS_226		
G33	VSS_227		
G42	VSS_228		
G45	VSS_229		
G48	VSS_230		
G8	VSS_231		
H24	VSS_232		
H38	VSS_233		
H4	VSS_234		
H45	VSS_235		
J11	VSS_236		
J16	VSS_237		
J2	VSS_238		
J24	VSS_239		
J28	VSS_240		
J33	VSS_241		
J35	VSS_242		
J39	VSS_243		
K12	VSS_245		
K47	VSS_246		
L1	VSS_247		
L11	VSS_248		
L17	VSS_249		
L20	VSS_250		
L24	VSS_251		
L28	VSS_252		
L3	VSS_253		
L48	VSS_254		
L49	VSS_255		
M28	VSS_256		
M42	VSS_257		
M46	VSS_258		
M49	VSS_259		
M5	VSS_260		
M50	VSS_261		
M9	VSS_262		
N11	VSS_263		
N14	VSS_264		
N17	VSS_265		
N29	VSS_266		
N30	VSS_267		
N36	VSS_268		
N39	VSS_269		
N44	VSS_270		
N49	VSS_271		
N7	VSS_272		
P19	VSS_273		
P2	VSS_274		
P23	VSS_275		
P3	VSS_276		
P50	VSS_277		
P49	VSS_278		
T30	VSS_279		
T43	VSS_280		
T47	VSS_281		
U41	VSS_282		
U45	VSS_283		
U50	VSS_284		
V2	VSS_285		
V3	VSS_286		

VSS

CRESTLINE_965PM

ASUS		Title : NB_965PM(GND)	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	16	of 85

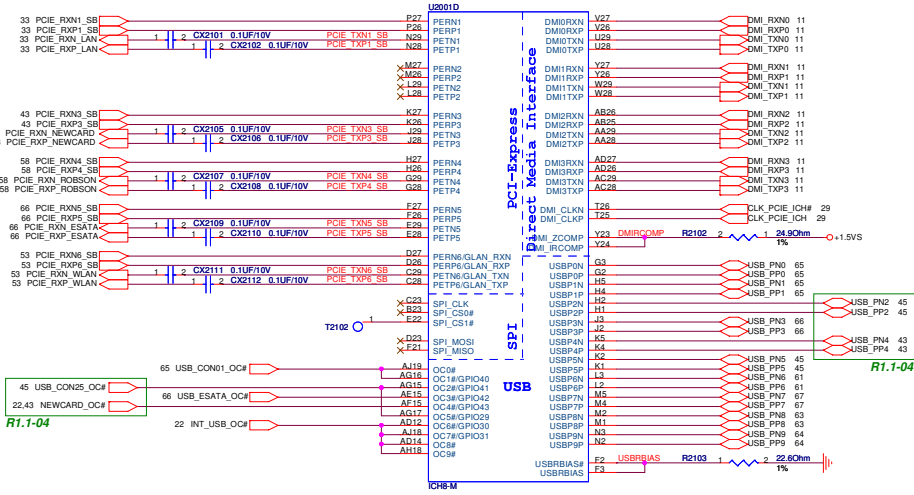
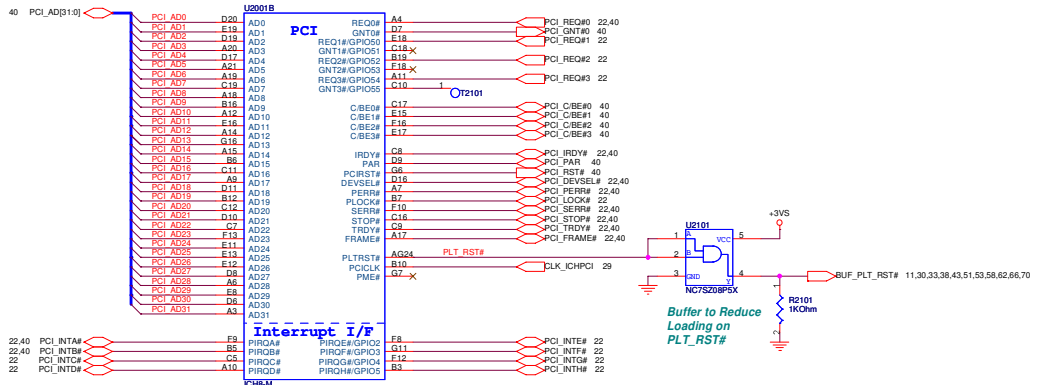


ICH_TP3, ACZ_SDOOUT : XOR Chain Entrance Strap
 00 = Reserved
 01 = Enter XOR Chain
 10 = Normal Operation (D)
 11 = Set PCIe Port Config Bit 1

GNT0#, SPI_CS1 : ICH8 Boot BIOS Select
 01 = SPI
 10 = PCI
 11 = LPC (D)

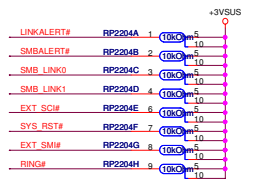
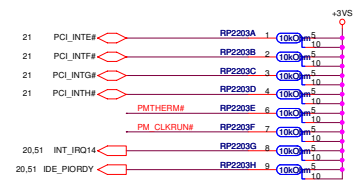
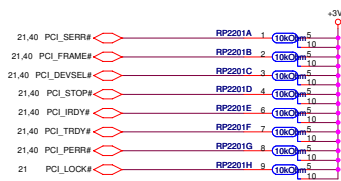
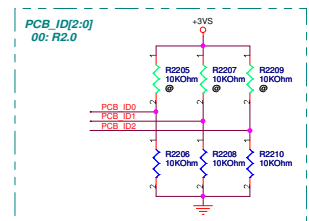
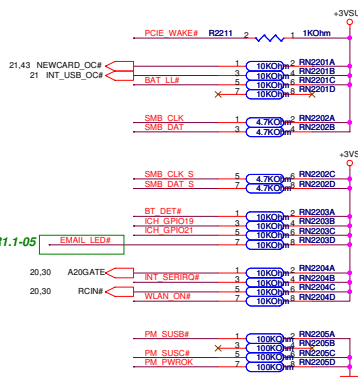
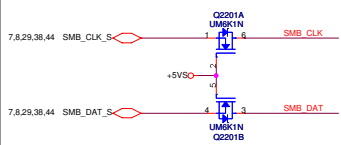
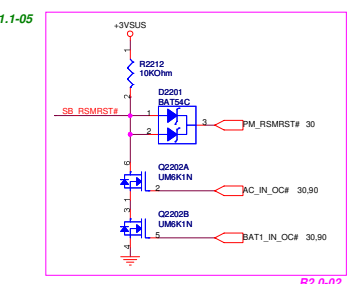
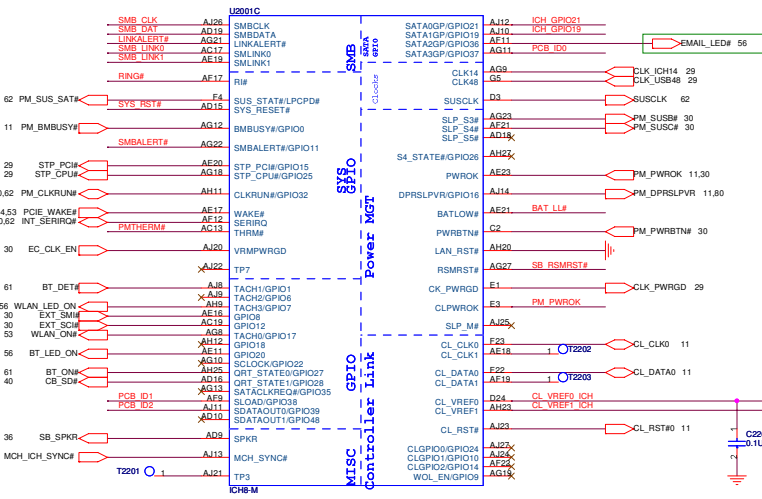
GNT2# : PCIe Port Configuration 2(Port 5/6)
 0 = Port 5 (x2)
 1 = Port 5 (x1), Port 6(x1) (D)

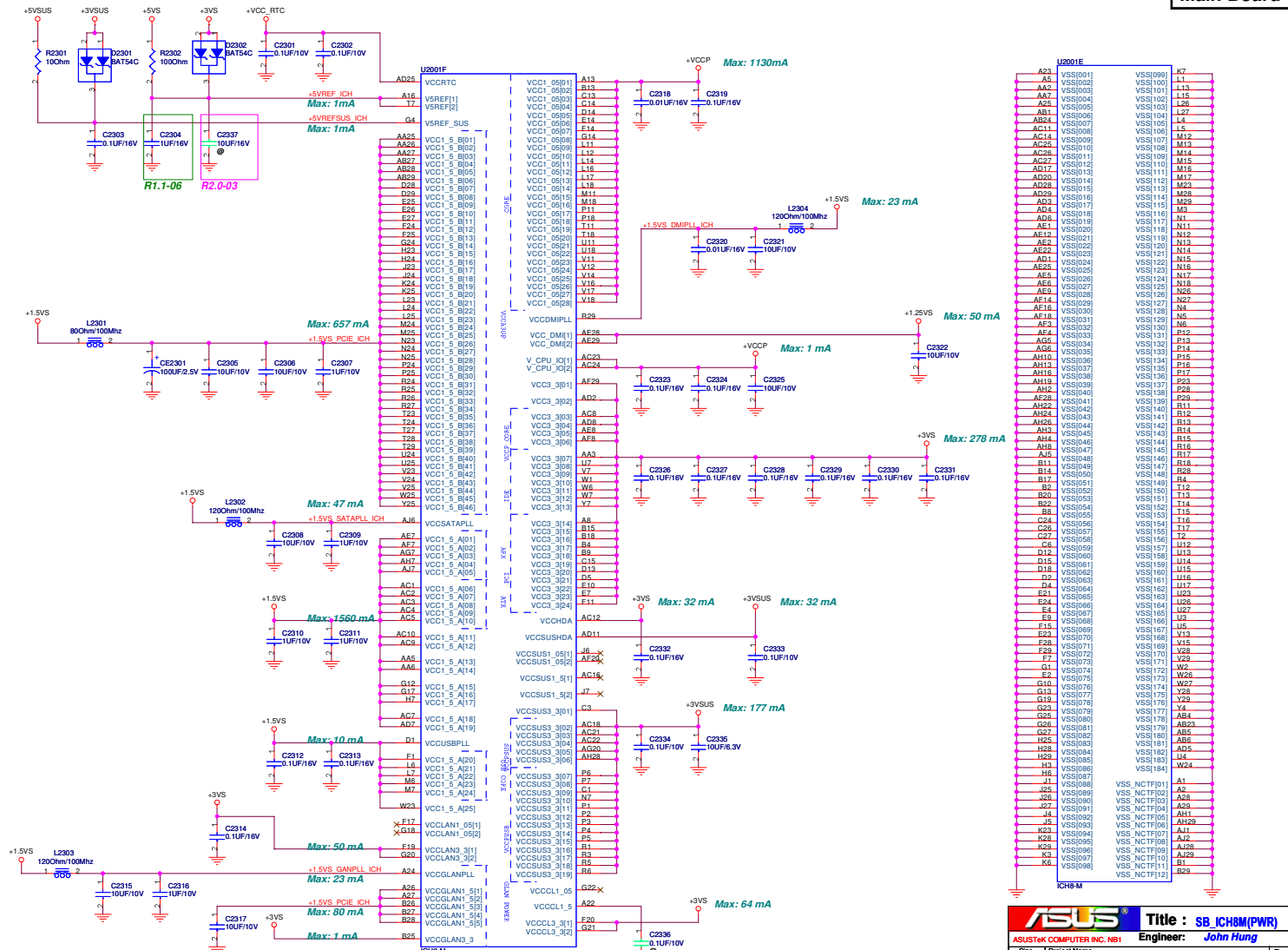
GNT3# : A16 Swap override strip
 0 = Enable
 1 = Default (D)



- USB 0 USB Conn.
- USB 1 USB Conn.
- USB 2 USB Conn.
- USB 3 eSATA/USB
- USB 4 NewCard
- USB 5 Camera
- USB 6 Bluetooth
- USB 7 3G Card
- USB 8 Fingerprint
- USB 9 TV Tuner

ASUS Title : SB_ICH8M(2)
 ASUSTek COMPUTER INC. NBI Engineer: John Hung
 Site: Project Name: M50S/X55S
 Date: Monday, September 03, 2007 Sheet 21 of 55





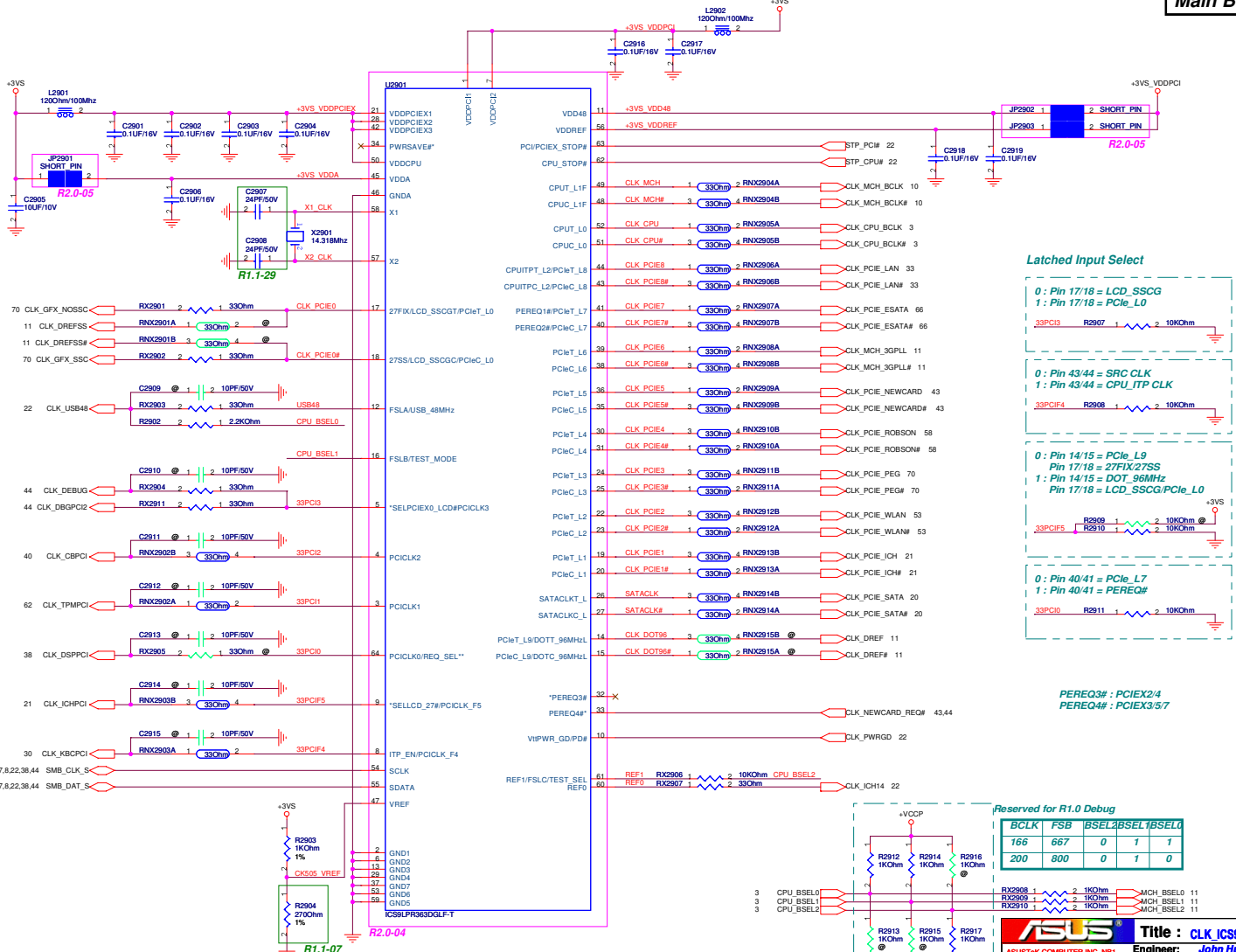
ASUS Title : SB_ICH8M(PWR)

ASUSTeK COMPUTER INC. NE1 Engineer: John Hung

Size: _____ Project Name: _____

Customer: M50S/X55S

Date: Monday, September 03, 2007 Sheet: 23 of 35



Latched Input Select

0 : Pin 17/18 = LCD_SSCG
 1 : Pin 17/18 = PCIe_L0

0 : Pin 43/44 = SRC CLK
 1 : Pin 43/44 = CPU_I7P CLK

0 : Pin 14/15 = PCIe_L9
 1 : Pin 17/18 = 27FX/27SS
 1 : Pin 14/15 = DOT_96MHz
 1 : Pin 17/18 = LCD_SSCG/PCIe_L0

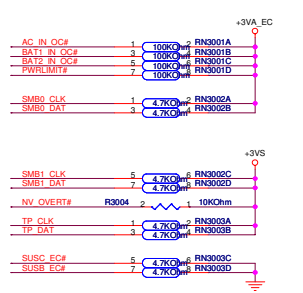
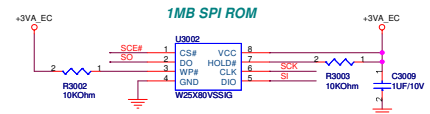
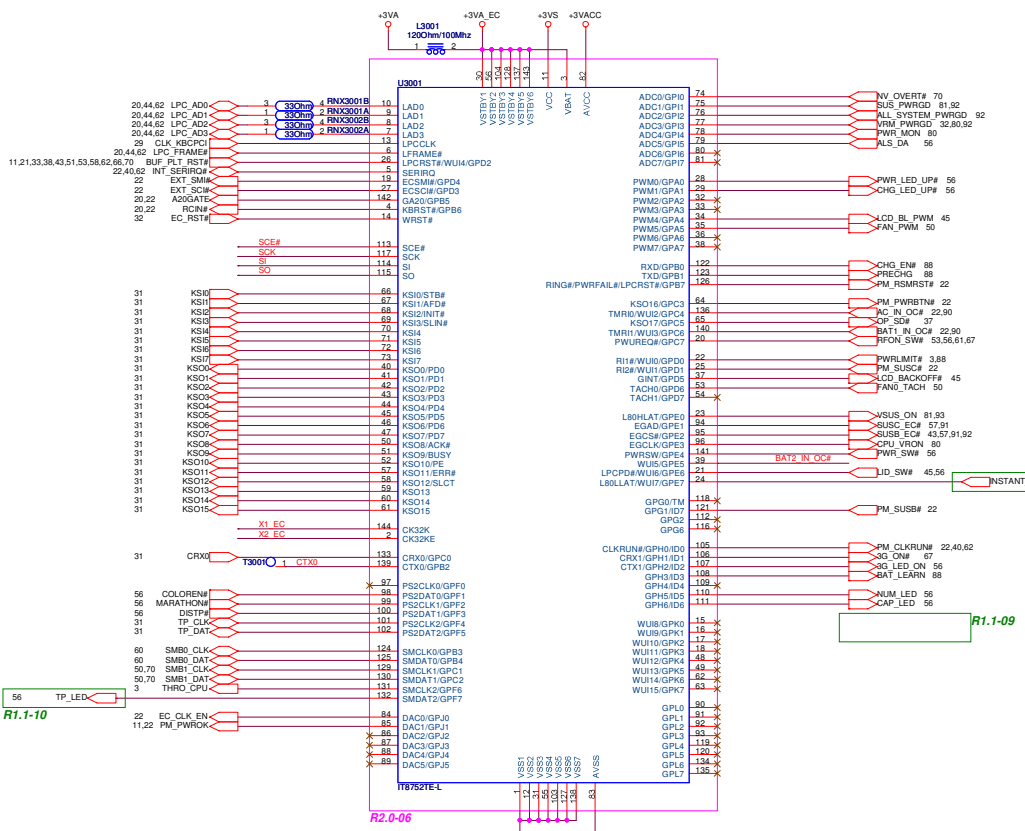
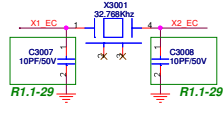
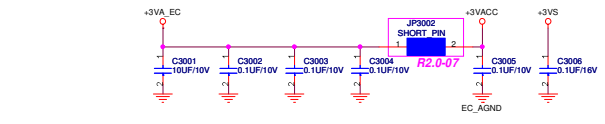
PEREQ3# : PCIEX2/4
 PEREQ4# : PCIEX3/5/7

Reserved for R1.0 Debug

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0

RX2908 1 2 1KOhm MCH_BSEL0 11
 RX2909 1 2 1KOhm MCH_BSEL1 11
 RX2910 1 2 1KOhm MCH_BSEL2 11

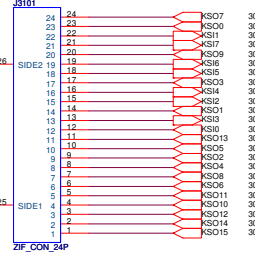
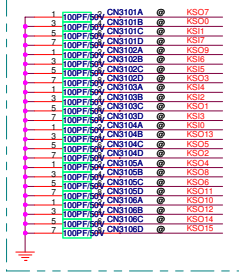
RX2913 1 1KOhm
 RX2915 1 1KOhm
 RX2917 1 1KOhm



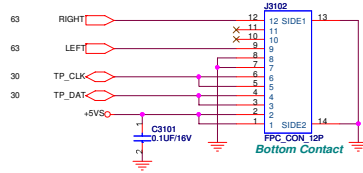
ASUS Title : KBC_IT8752
 ASUSTeK COMPUTER INC. NBI Engineer: John Hung
 Size Project Name M50S/X55S Rev
 Custom Date: Monday, September 03, 2007 Sheet 30 of 55

Keyboard

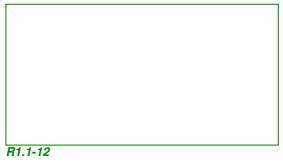
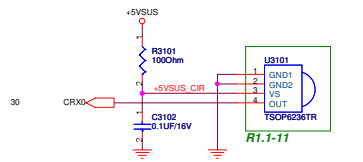
EMI

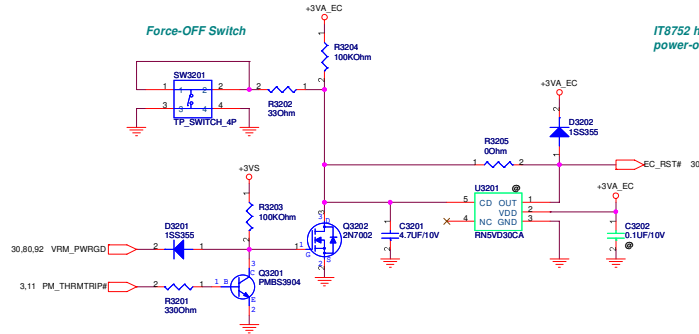


Touchpad

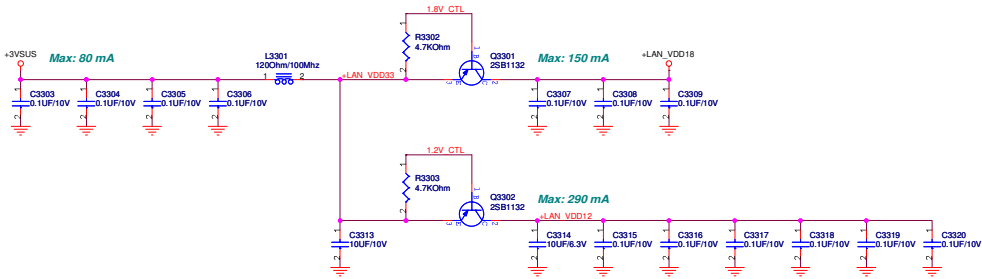
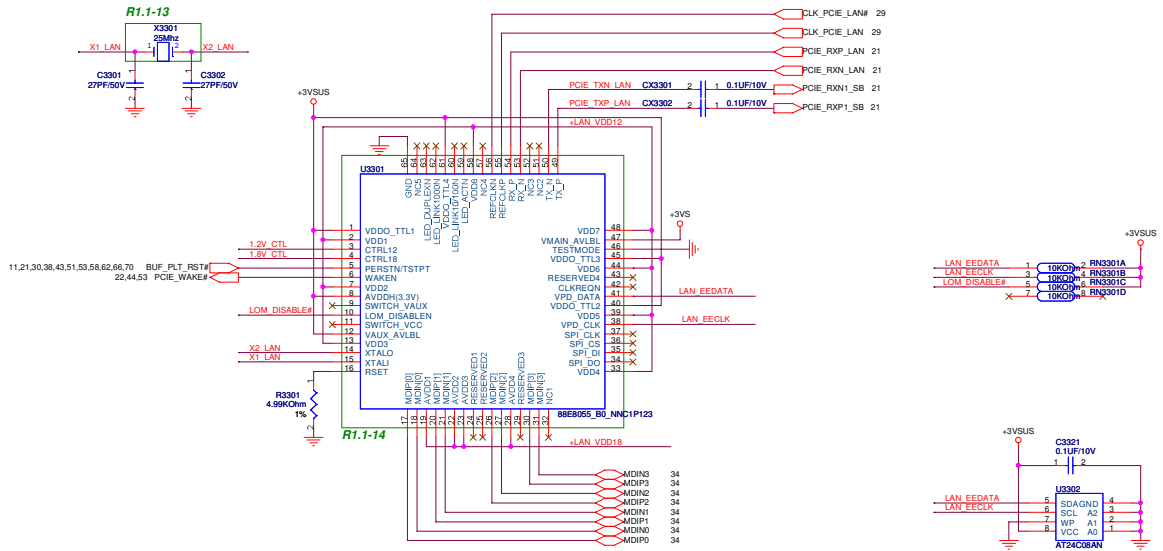


CIR

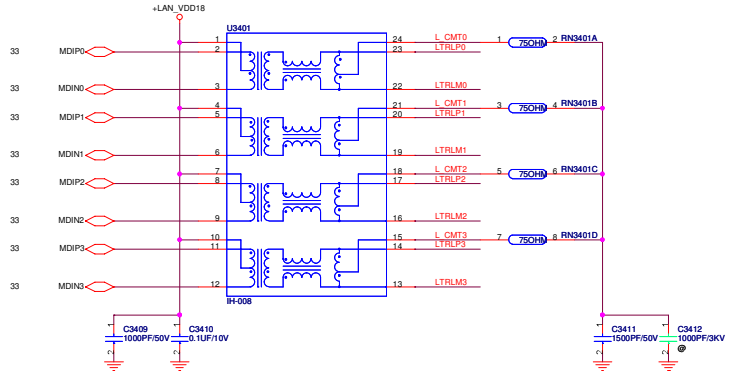
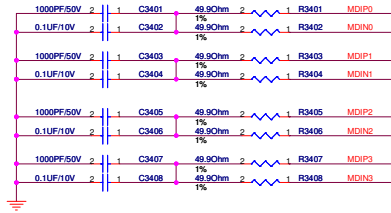




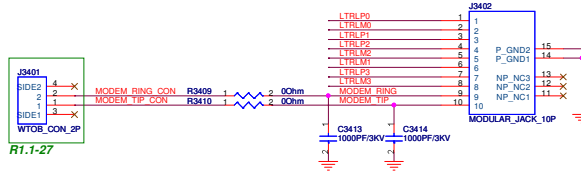
		Title : RST_Reset Circuit	
ASUSTeK COMPUTER INC. NBI		Engineer: <i>John Hung</i>	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	32	of 88



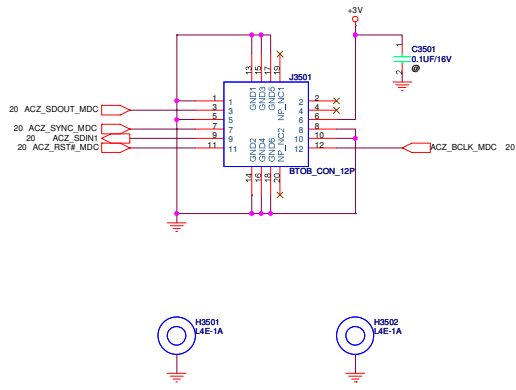
ASUS		Title : LAN_88E8055	
ASUSTek COMPUTER INC. NBI			
Engineer: John Hung			
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	33	of 88



R1.1-28
R2.0-08

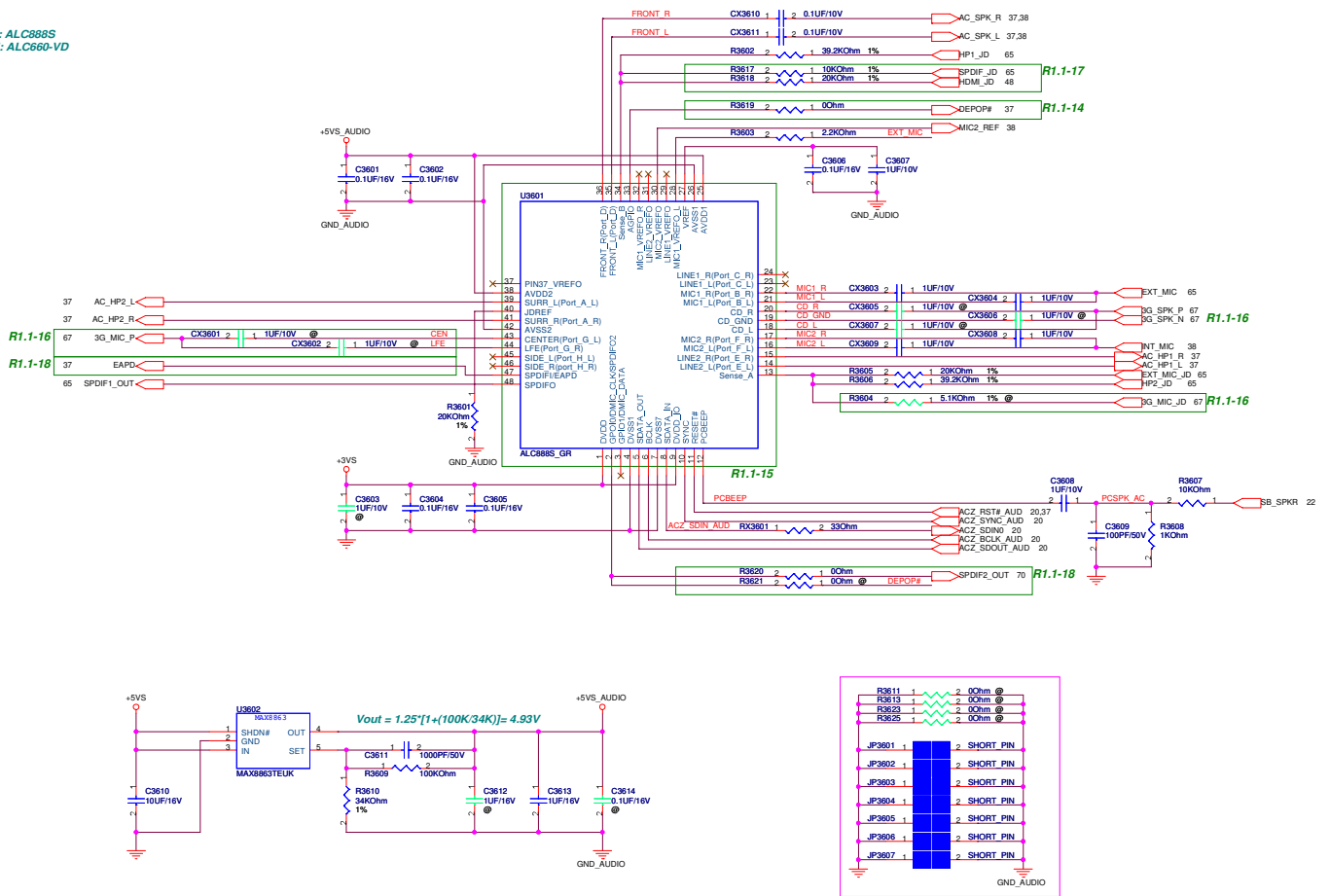


ASUS		Title : LAN RJ45 & RJ11	
ASUSTEK COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	34	of 88



		Title : LAN_MDC	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	35 of 35

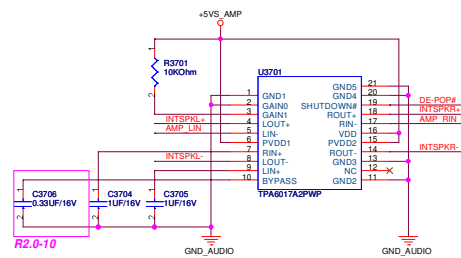
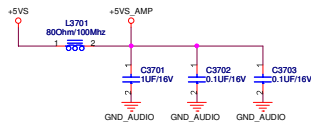
PM: ALC888S
GM: ALC660-VD



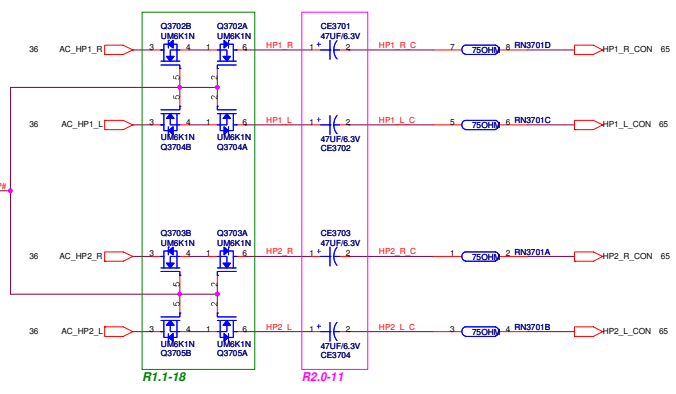
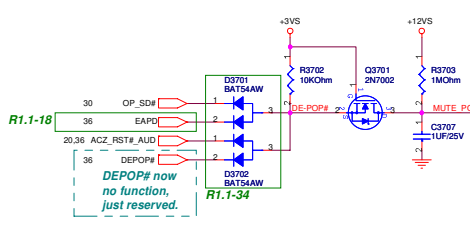
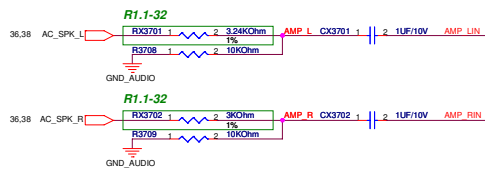
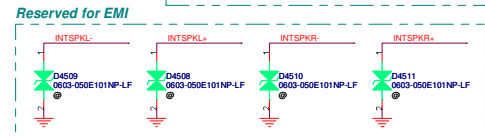
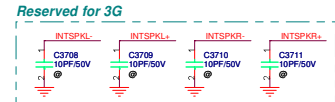
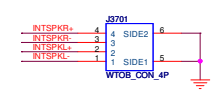
R1.1-28
R2.0-09

R3611	1	2	0Ohm	@
R3613	1	2	0Ohm	@
R3623	1	2	0Ohm	@
R3625	1	2	0Ohm	@
JP3601	1	2	SHORT PIN	
JP3602	1	2	SHORT PIN	
JP3603	1	2	SHORT PIN	
JP3604	1	2	SHORT PIN	
JP3605	1	2	SHORT PIN	
JP3606	1	2	SHORT PIN	
JP3607	1	2	SHORT PIN	

ASUS		Title : AUD_ALC888S
ASUSTek COMPUTER INC. NBI		Engineer: John Hung
Size	Project Name	Rev
Custom	M50S/X55S	2.0
Date: Monday, September 03, 2007	Sheet	36 of 55

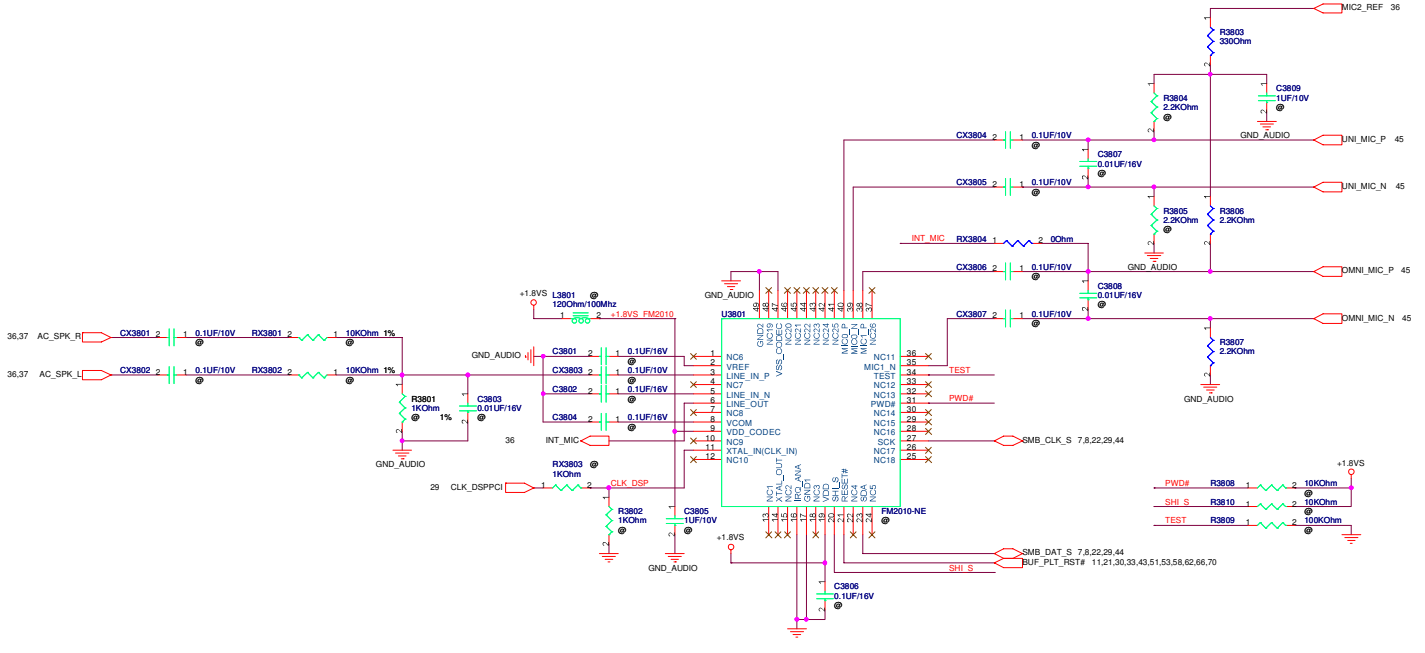


Internal Speaker Conn.

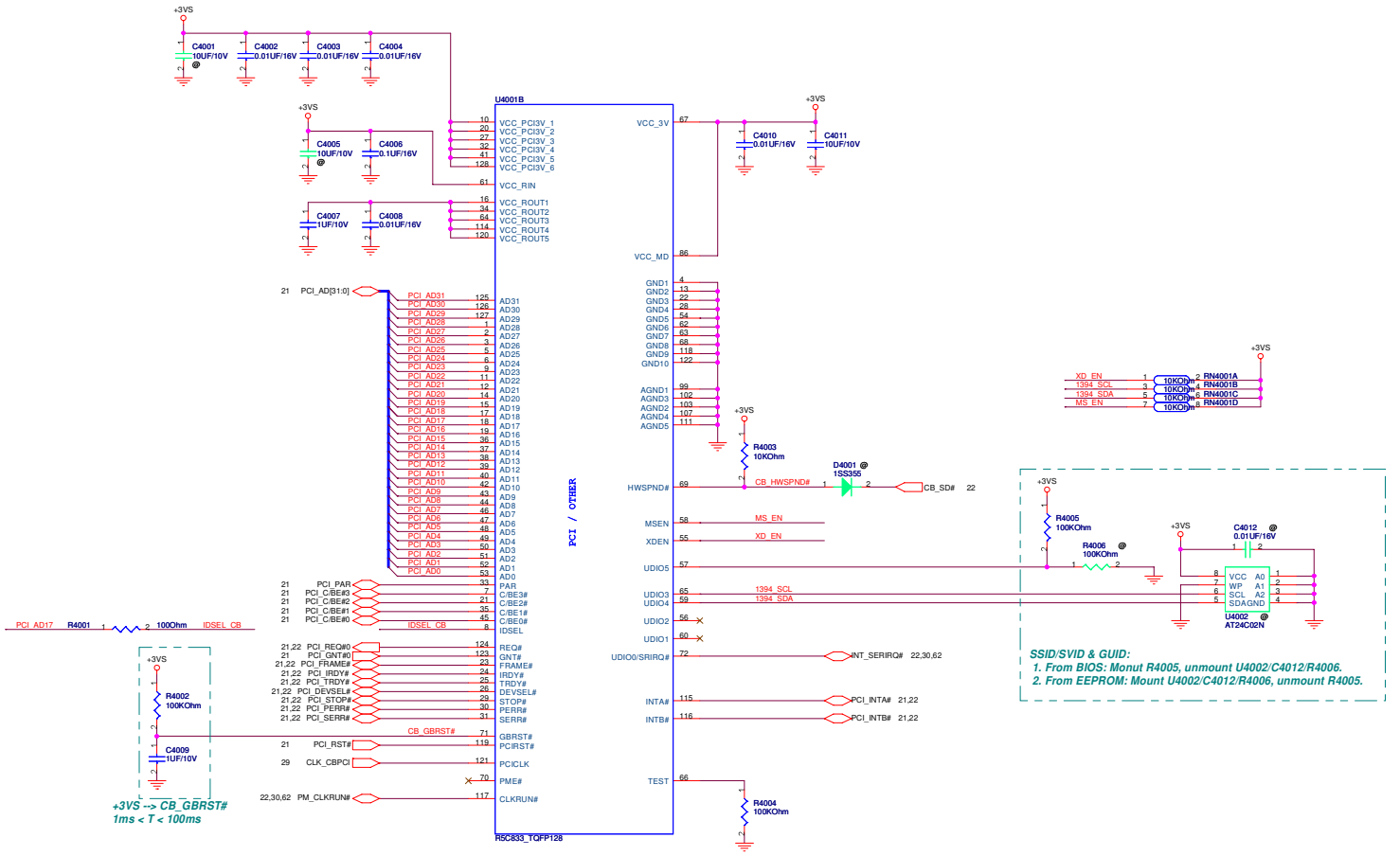


R1.1-18
DEPOP# now no function, just reserved.

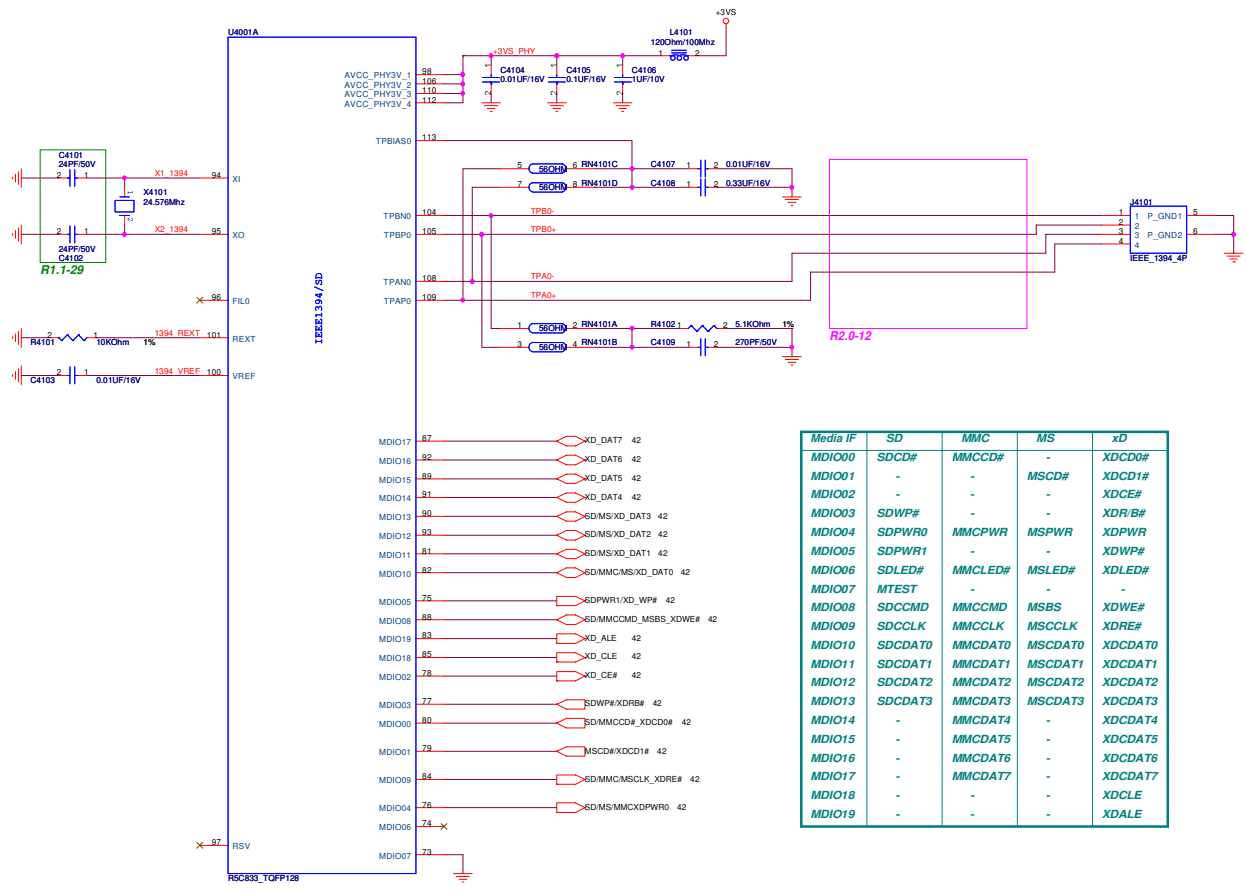
ASUS		Title : AUD_Amp & Jack
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung
Size	Project Name	Rev
Custom	M50S/X55S	2.0
Date: Wednesday, September 05, 2017	Sheet	37 of 38



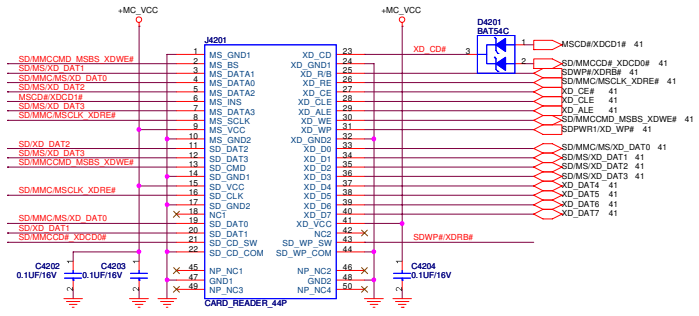
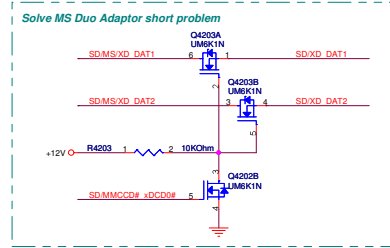
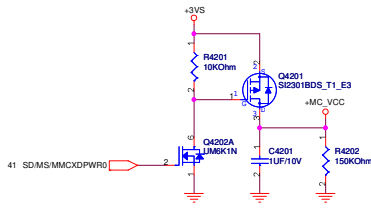
		Title : AUD_FM2010
ASUSTEK COMPUTER INC. NB1		Engineer: John Hung
Size	Project Name	Rev
Custom	M50S/X55S	2.0
Date: Tuesday, September 04, 2007	Sheet	38 of 88

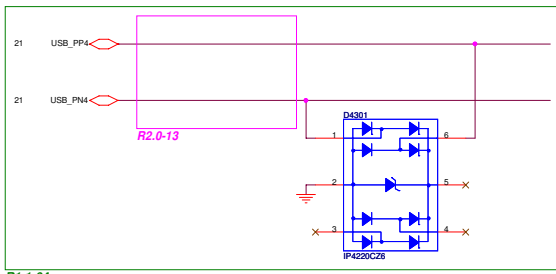


ASUS		Title : CB_R5C833
ASUSTEK COMPUTER INC. NB1		Engineer: John Hung
Size	Project Name	Rev
Custom	M50S/X55S	2.0
Date: Monday, September 03, 2007	Sheet	40 of 88

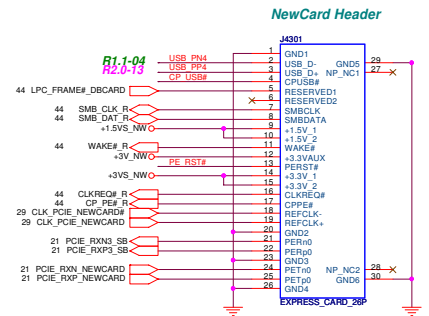
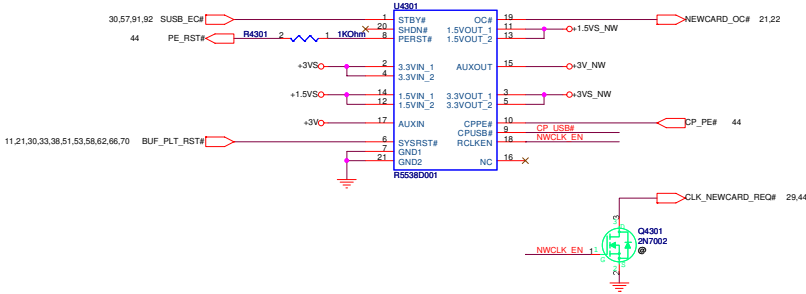


ASUS Title : CB_R5C833
 ASUSTek COMPUTER INC. NE1 Engineer: John Hung
 Project Name: M50S/X55S
 Date: Monday, September 03, 2007 Sheet 41 of 88

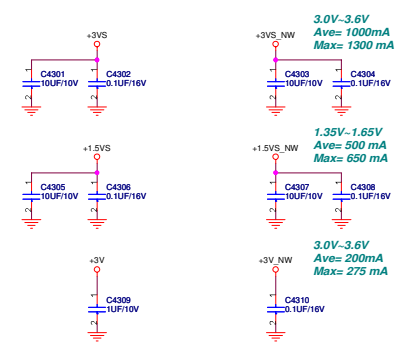
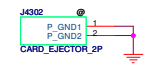




R1.1-04

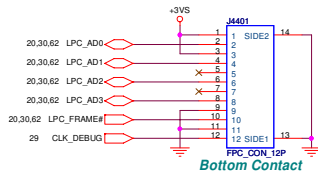


NewCard Ejector

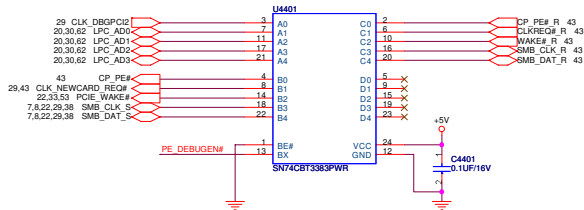


ASUS		Title : CB_NewCard	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	1.0	
Date: Monday, September 03, 2007	Sheet	43	of 88

LPC Debug Port

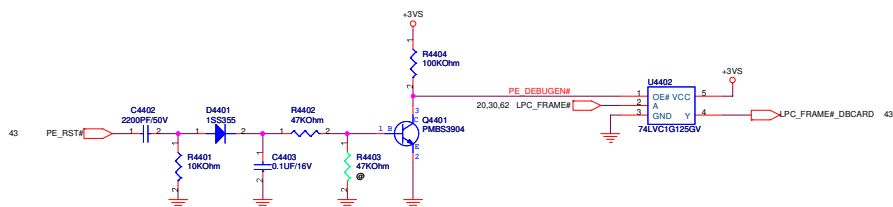


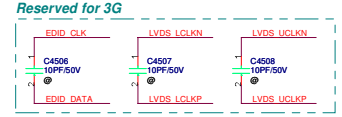
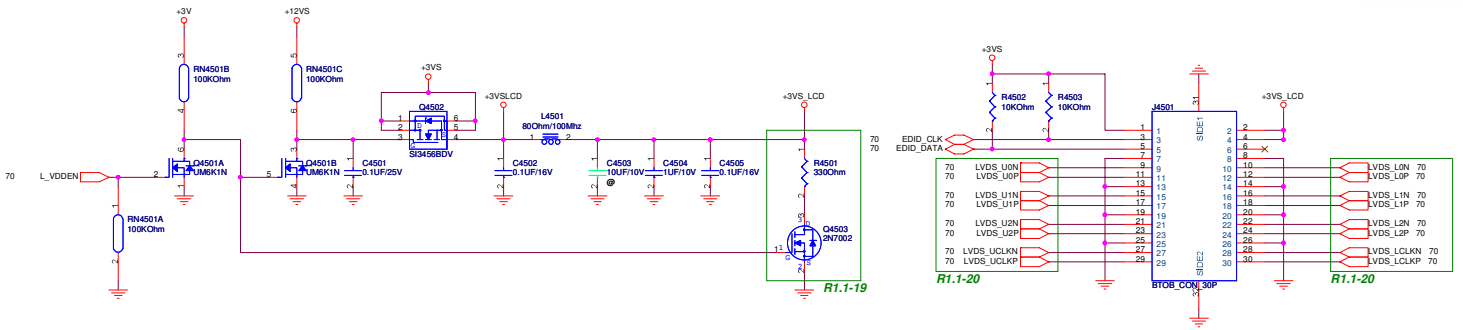
For NewCard Debug Card



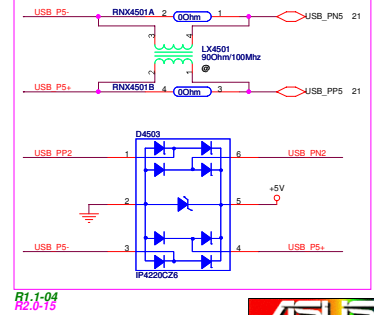
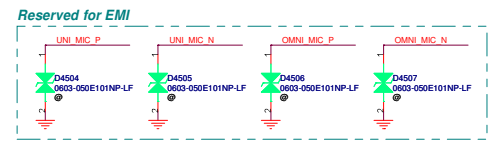
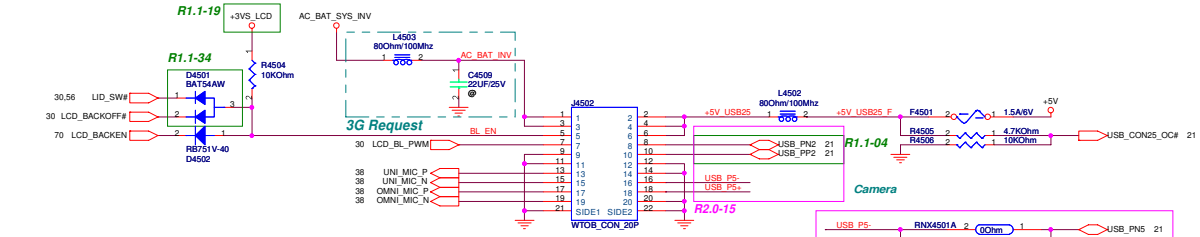
CP_PE#	@ 00hm	2	1	R4405	CP_PE# R
CLK_NEWCARD_REQ#	@ 00hm	4	4	R4401B	CLK_REQ# R
PCIE_WAKE#	@ 00hm	1	2	R4401A	WAKE# R
SMB_DAT# S	@ 00hm	4	4	R4402B	SMB_DAT# R
SMB_CLK# S	@ 00hm	2	2	R4402A	SMB_CLK# R

R2.0-14



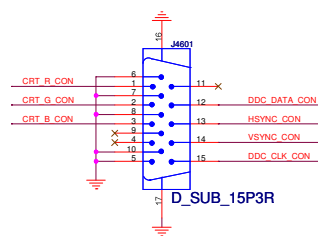
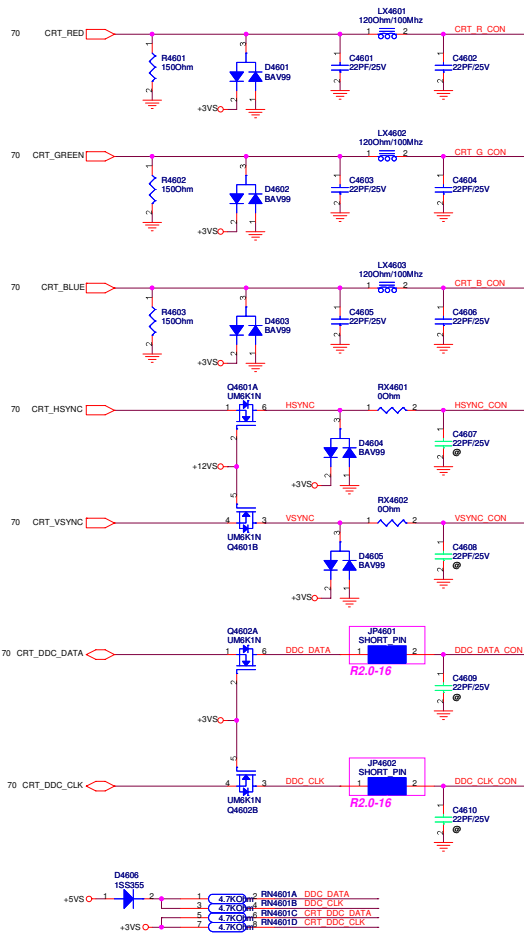


X 7 100K Ohm RN4501D

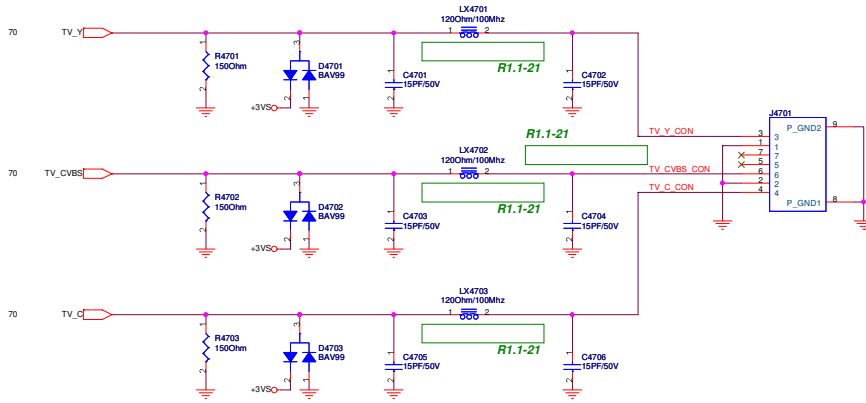


R1.1-04
R2.0-15

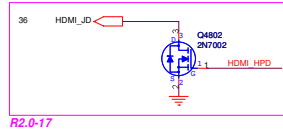
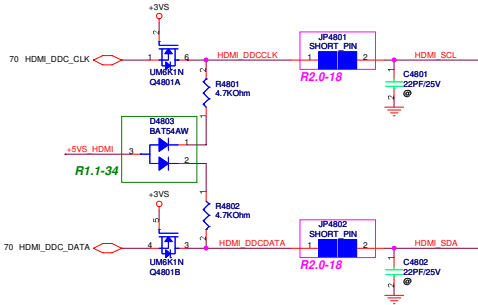
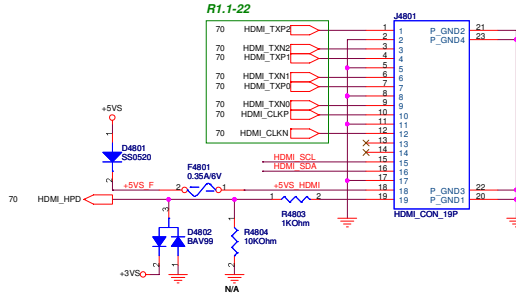
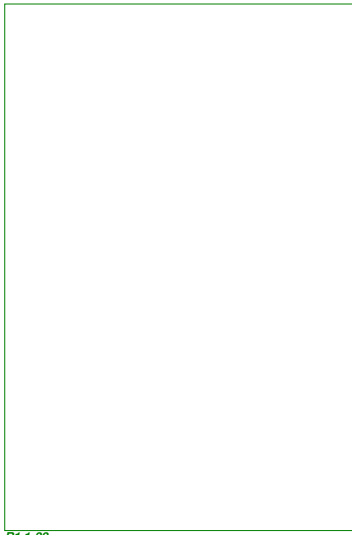
ASUS		Title : CRT_LCD Panel	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	45 of 85



ASUS		Title : CRT_D-Sub	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	46	of 88

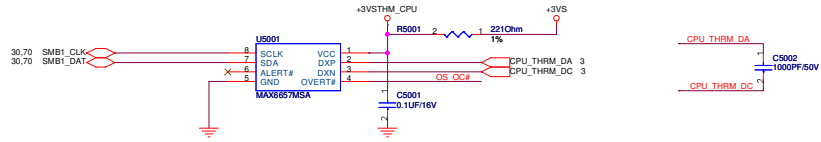


ASUS		Title : TV_TV-Out	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet 47 of 88	

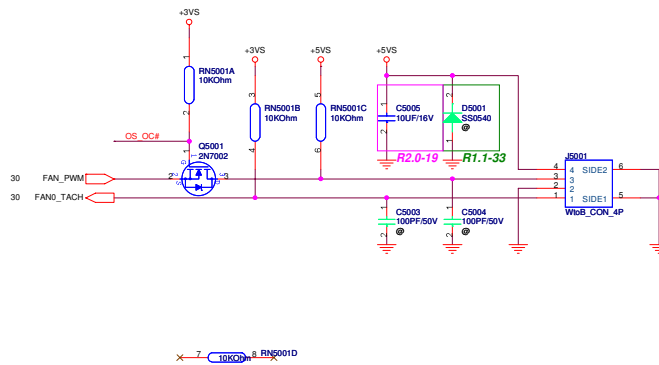


ASUS		Title : CRT_HDMI	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	48	of 88

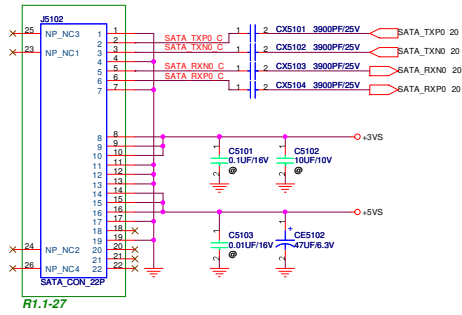
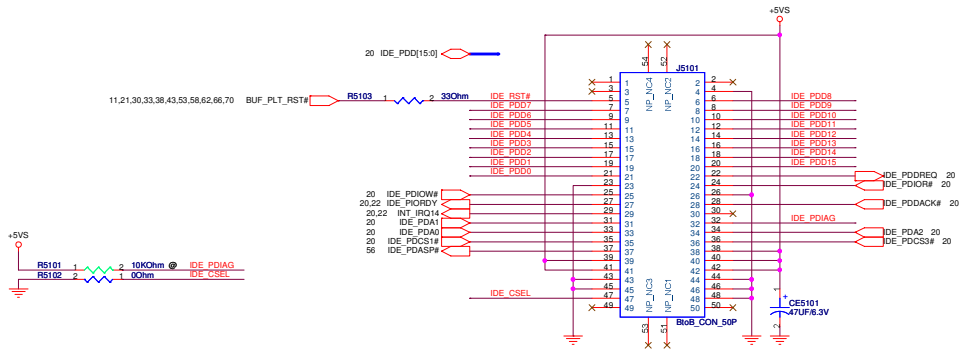
CPU Thermal Sensor



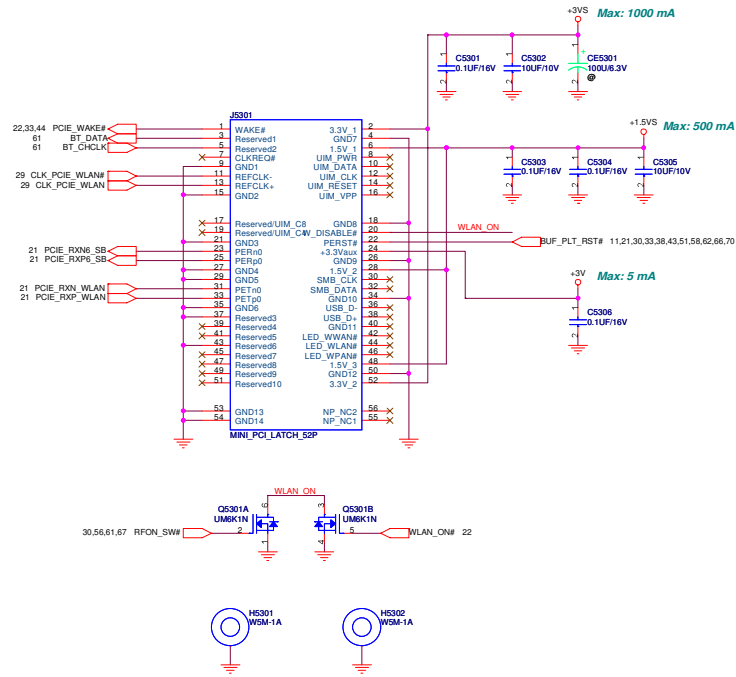
PWM Fan



ASUS		Title : FAN_Fan & Sensor	
ASUSTeK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007	Sheet	50	of 55



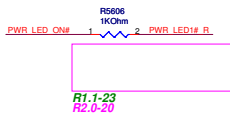
ASUS		Title : XDD_HDD & ODD	
ASUSTeK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	2.0
Custom	M50S/X55S	Date:	Monday, September 03, 2007
		Sheet	51 of 88



ASUS		Title : PCI WLAN	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Tuesday, September 04, 2017	Sheet	53	of 85

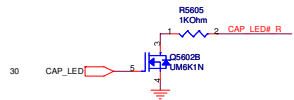
		Title : SIO ****	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	55 of 55

Power LED

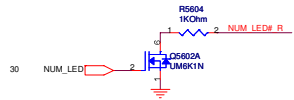


R1.1-23
R2.0-20

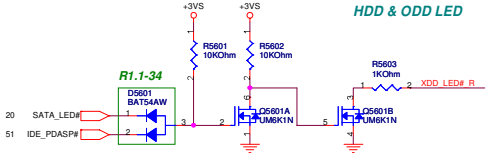
Cap Lock LED



Num Lock LED

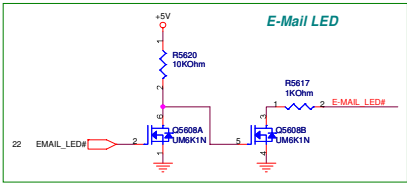


HDD & ODD LED



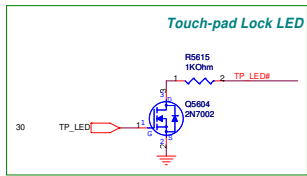
R1.1-34

E-Mail LED

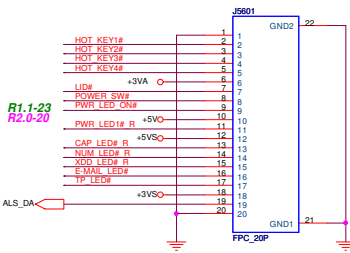


R1.1-03

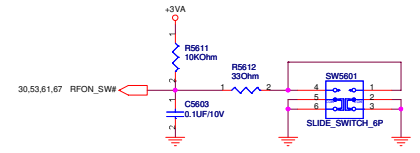
Touch-pad Lock LED



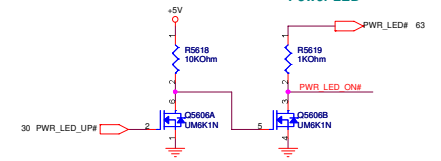
R1.1-08



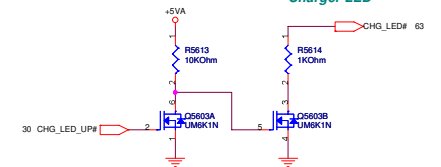
R1.1-23
R2.0-20



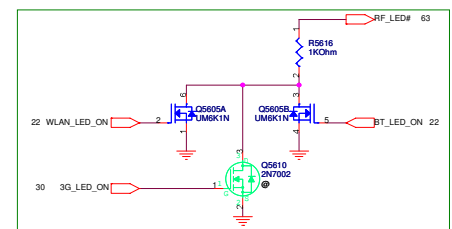
Power LED



Charger LED

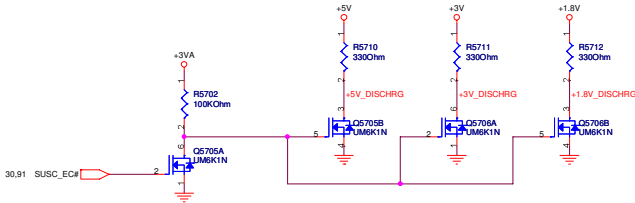
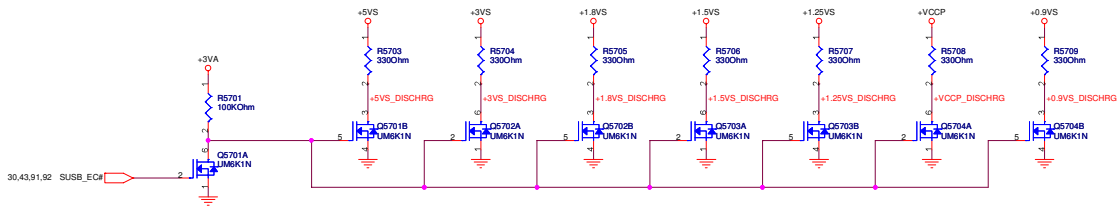


WLAN LED

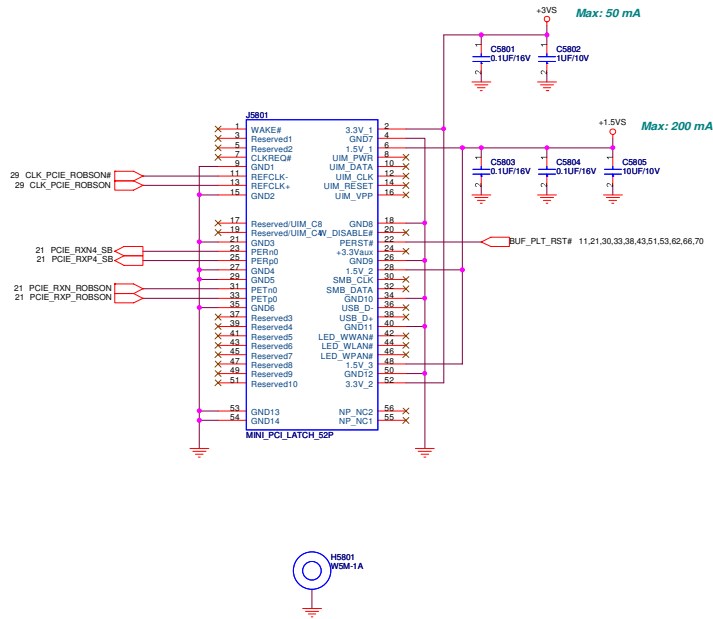


R1.1-24

ASUS		Title : LED Indicator	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X555	2.0	
Date: Tuesday, September 04, 2007	Sheet	56	of 88

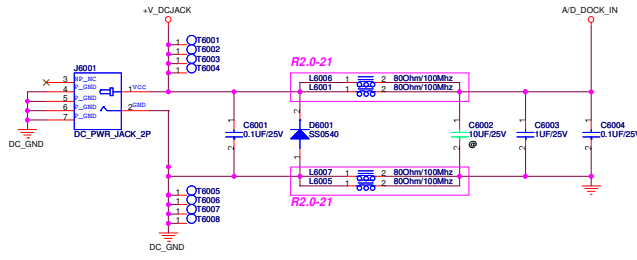


		Title : DSG Discharge	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	57 of 88

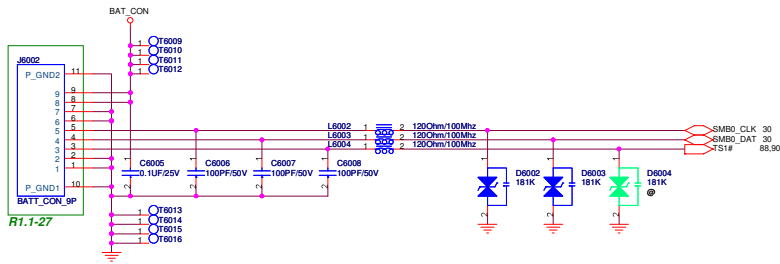


ASUS		Title : ROB_Robson	
ASUSTEK COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	58 of 88

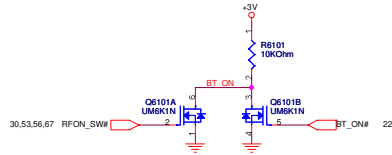
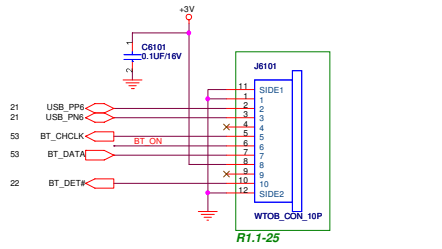
DC Jack



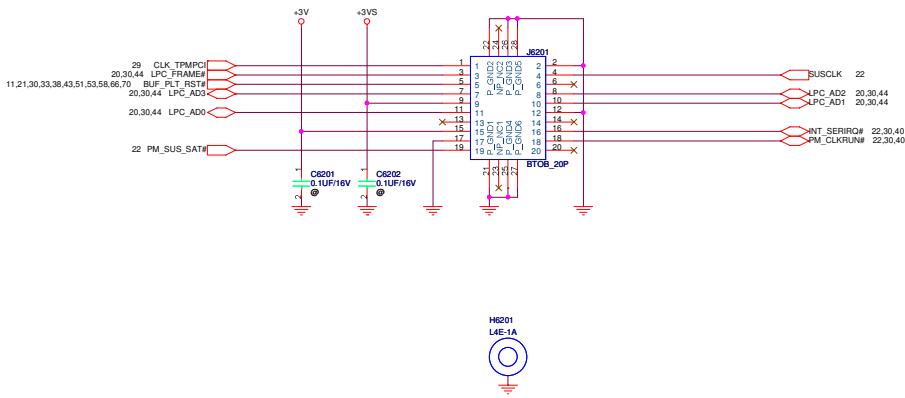
Battery Connector



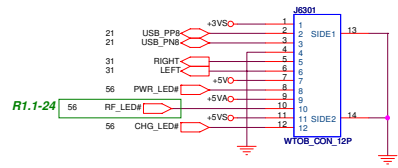
ASUS		Title : DC_DC & BAT Conn.	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	60	of 88



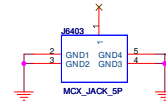
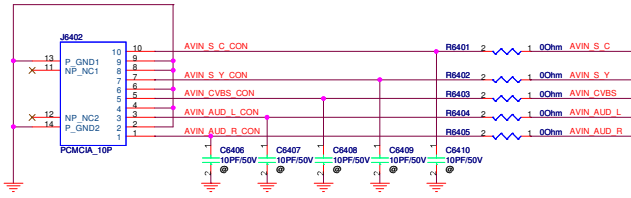
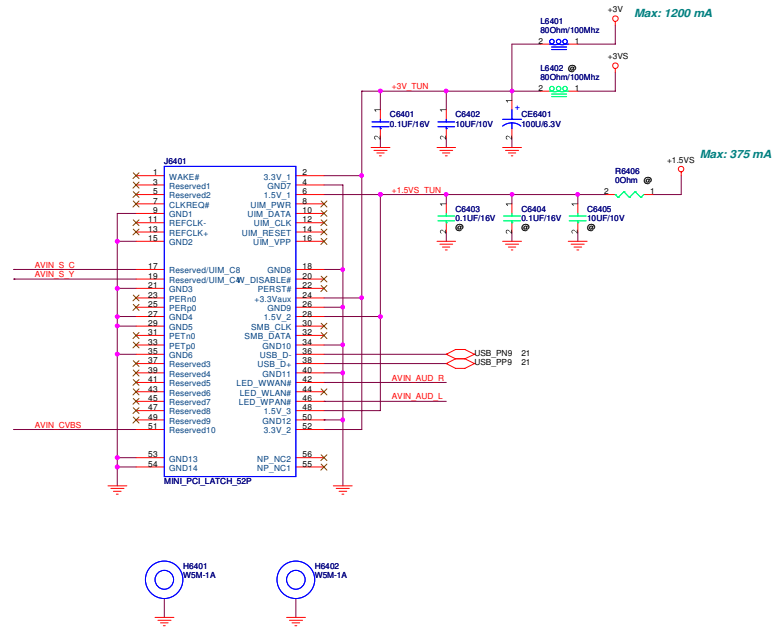
ASUS		Title : BT Bluetooth	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	61	of 88

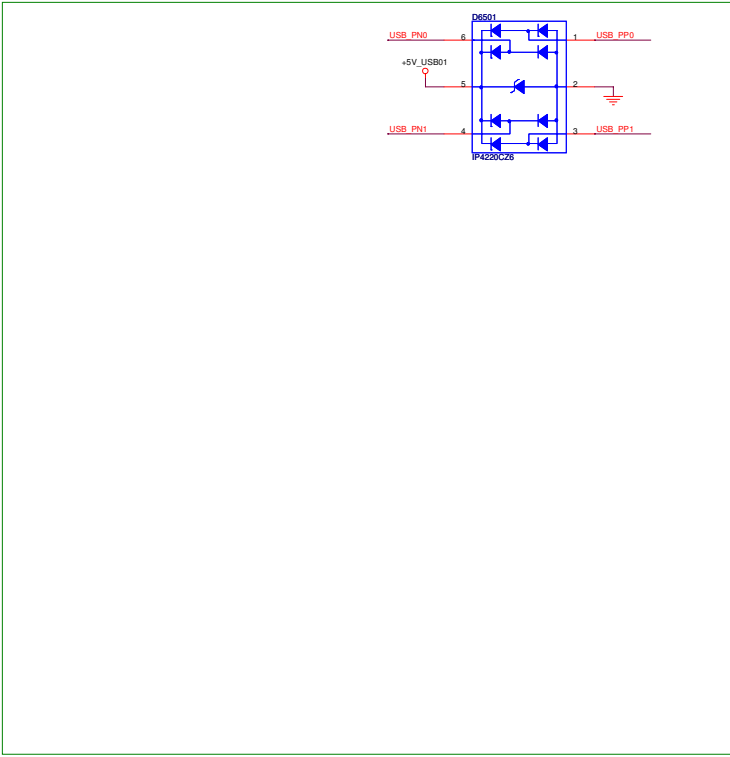
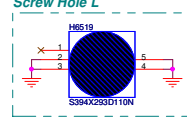
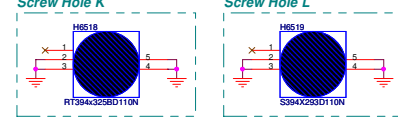
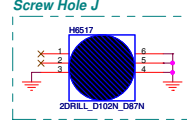
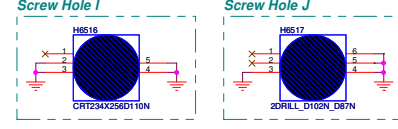
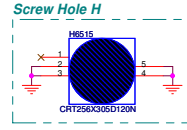
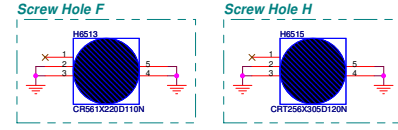
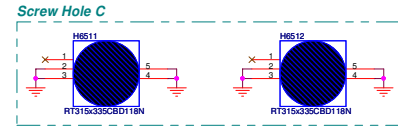
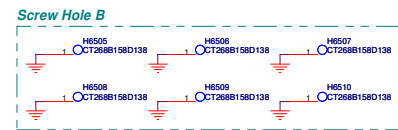
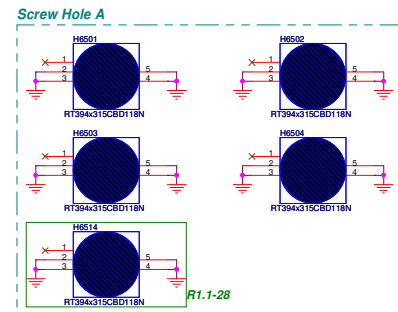
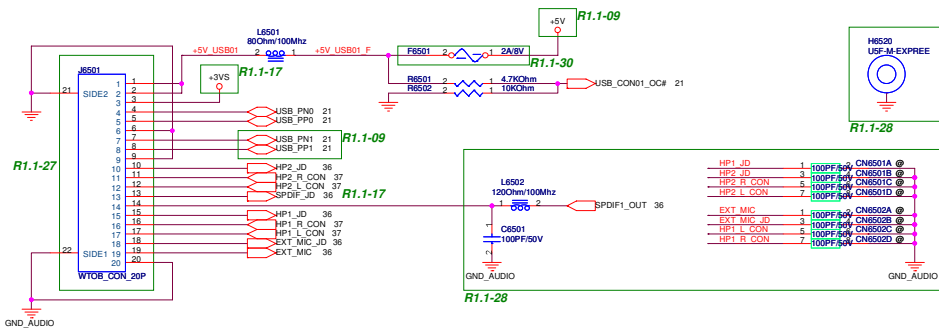


		Title : TPM TPM 1.2	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	62	of 88

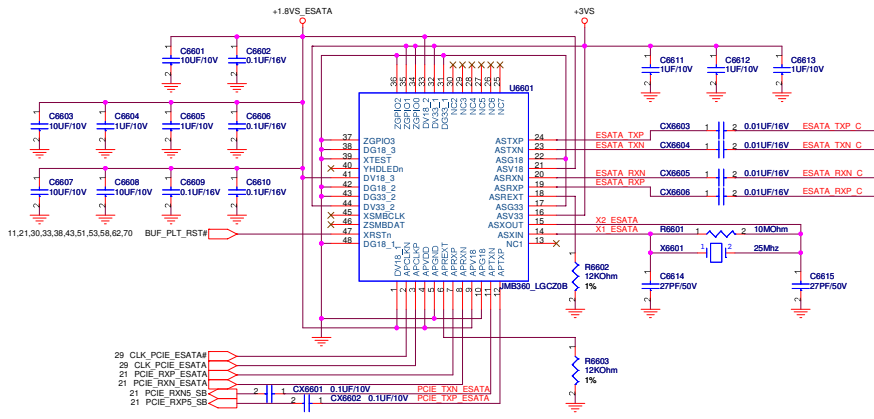


		Title : FP Fingerprint Conn.	
ASUSTEK COMPUTER INC. NB1		Engineer: John Hung	
Site	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	63 of 88

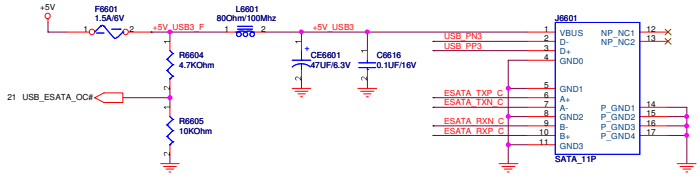
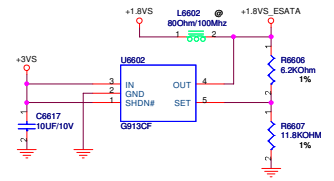
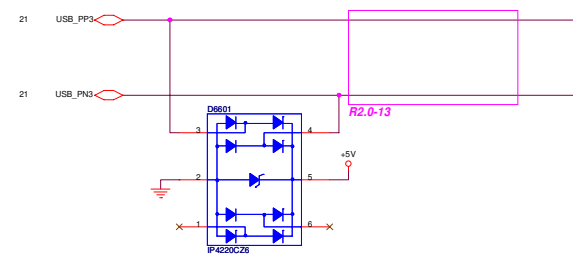




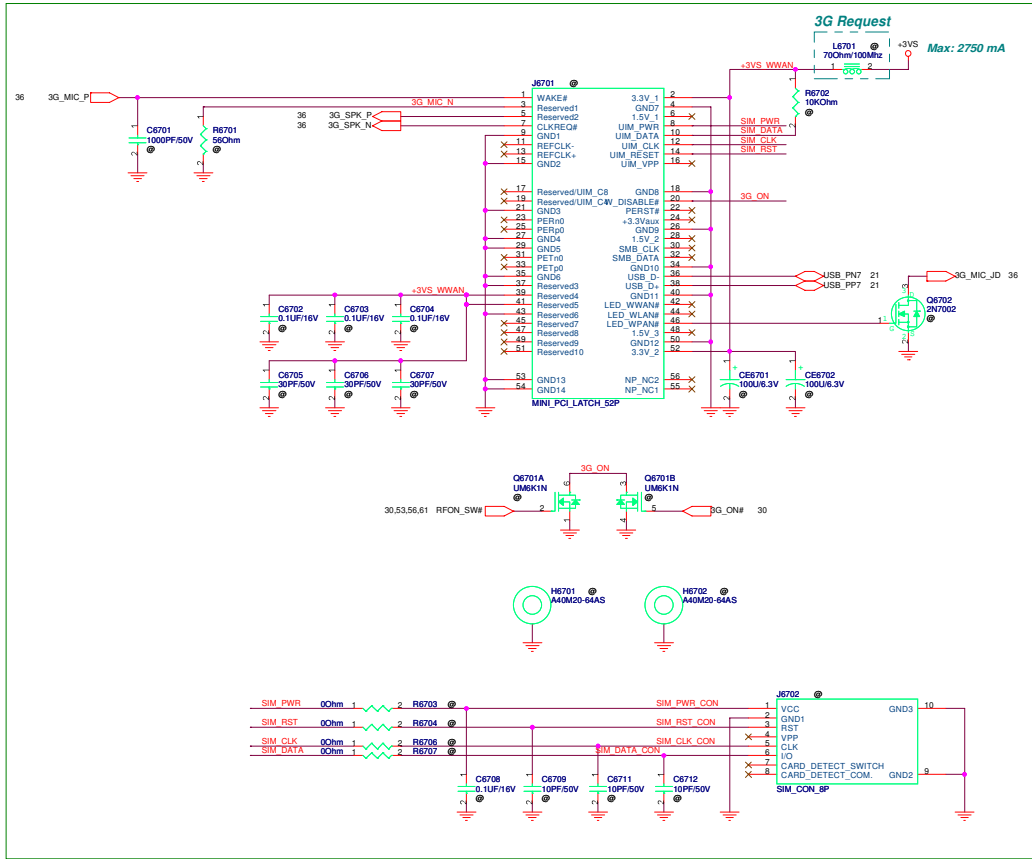
ASUS Title : ME_Conn & Screw Holes
 ASUSTEK COMPUTER INC. NBI Engineer: John Hung
 Project Name: M50S/X55S
 Date: Monday, September 03, 2007 Sheet: 65 of 85



- ZGPIO : Clock Type of PCI Express
0 = 25MHz Oscillator (D)
1 = 100MHz from PCI Express Finger
- ZGPIO1 : Clock Source of SATA II
0 = from Internal Clock Source (D)
1 = from ASXIN & ASXOUT
- ZGPIO2 : Interface to Debug Registers
0 = SMBus I/F (D)
1 = Reserved
- ZGPIO3 : SMBus ID Address
0 = 8'h44 (D)
1 = 8'h4A

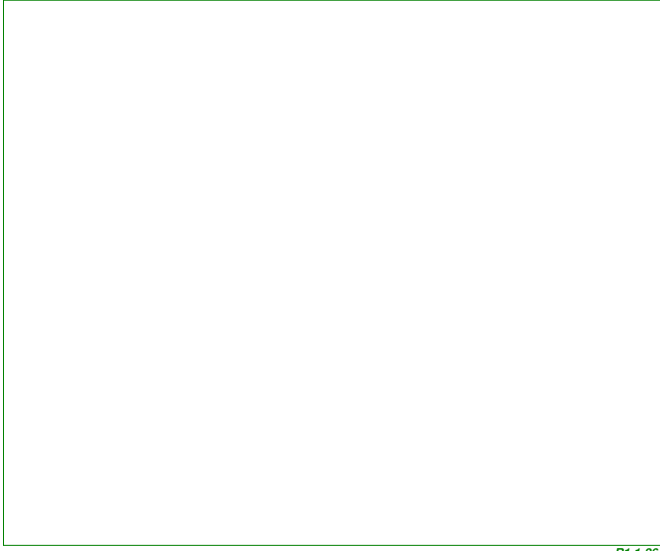


ASUS		Title : ESA_JMB360	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	2.0
Custom	M50S/X55S	Date	Monday, September 03, 2007
		Sheet	66 of 88



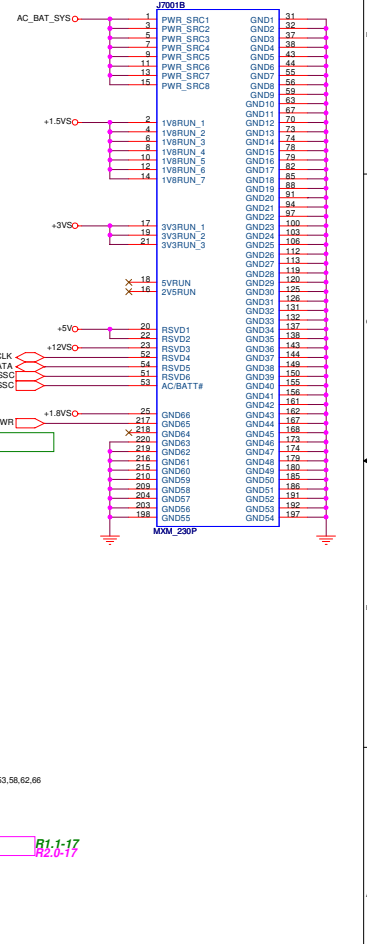
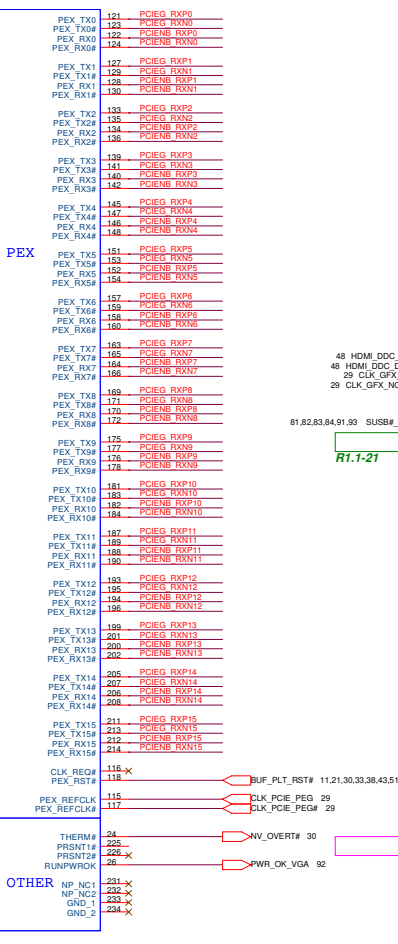
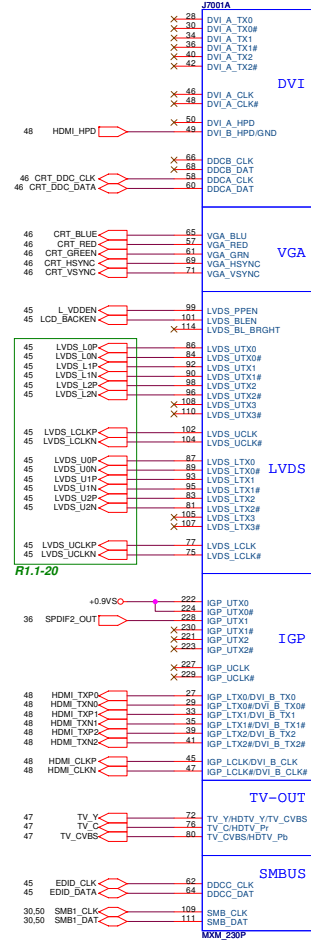
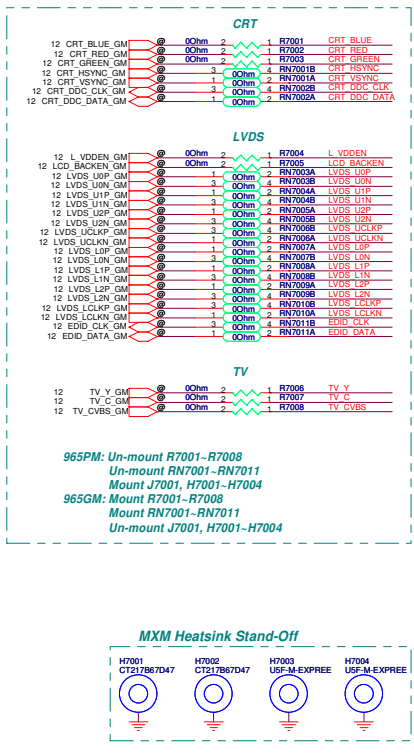
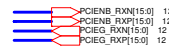
R1.1-16

ASUS		Title : WAN_WWAN	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	67	of 88

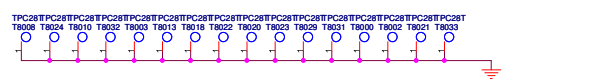
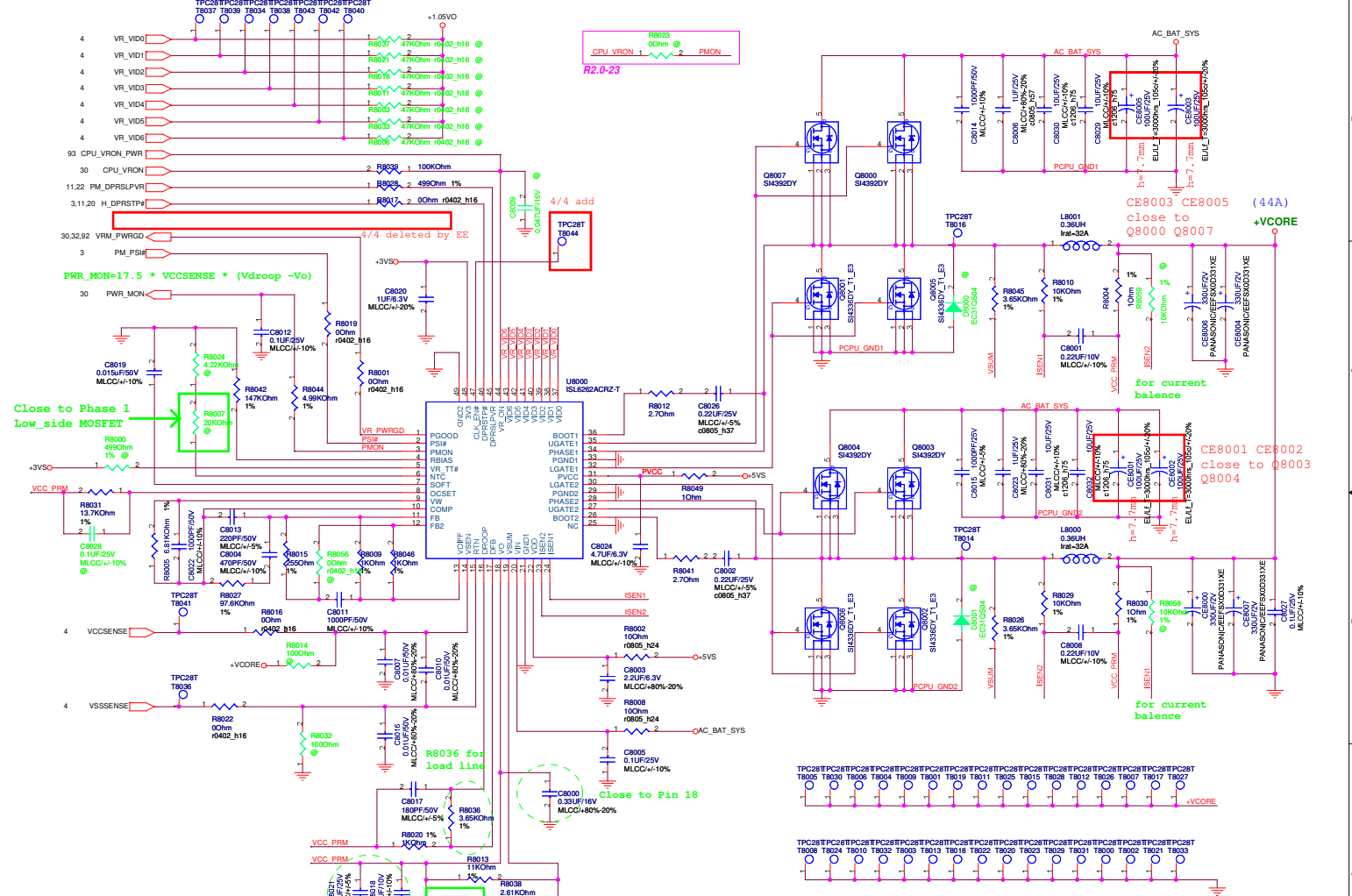


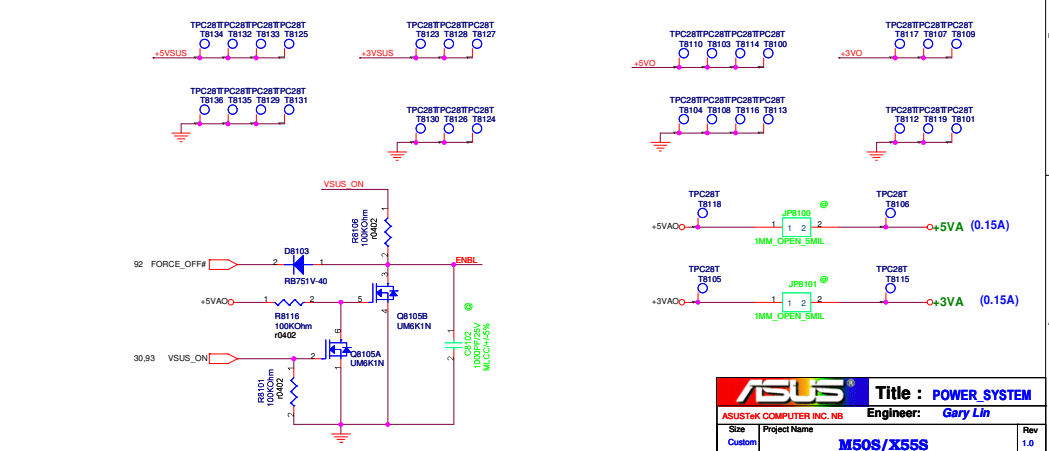
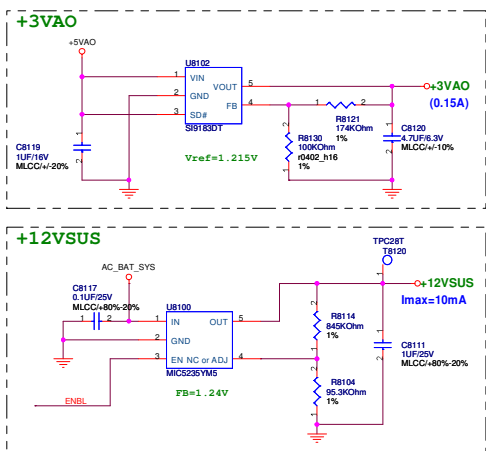
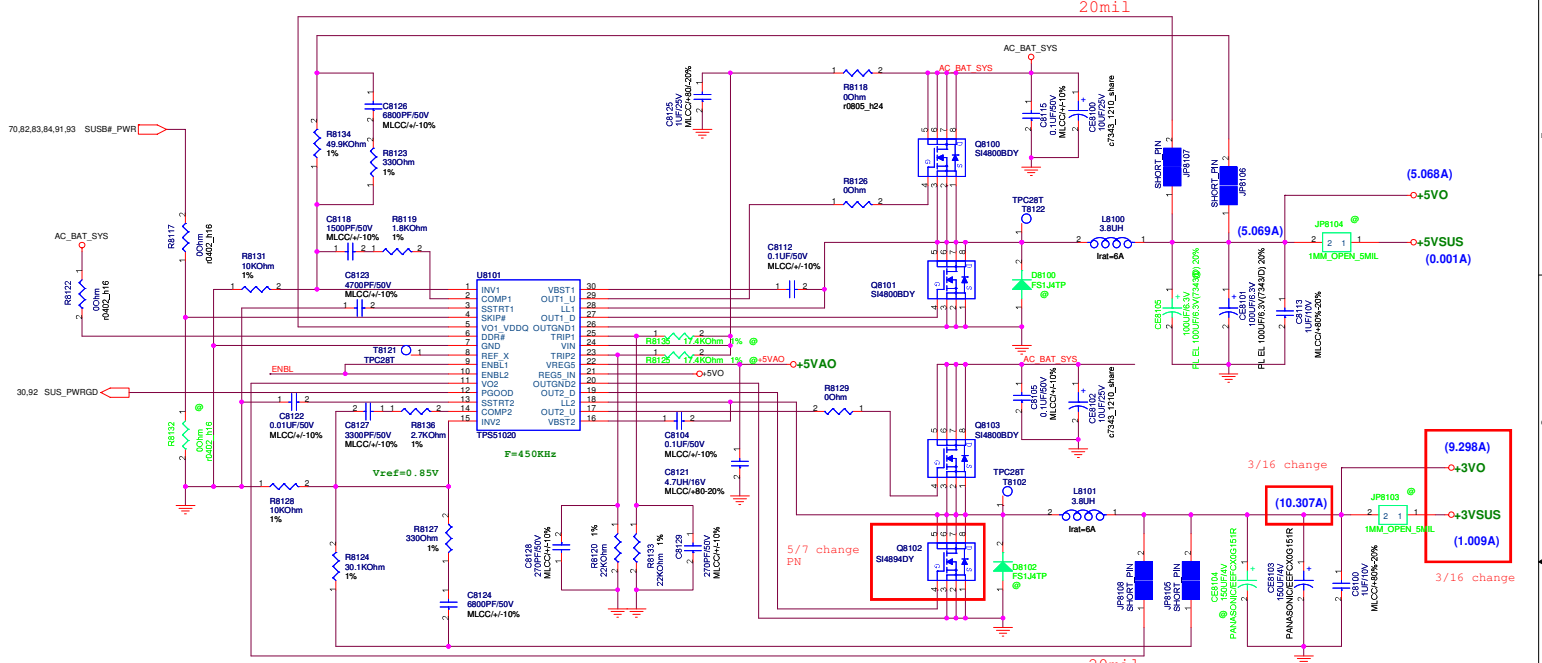
R1.1-26

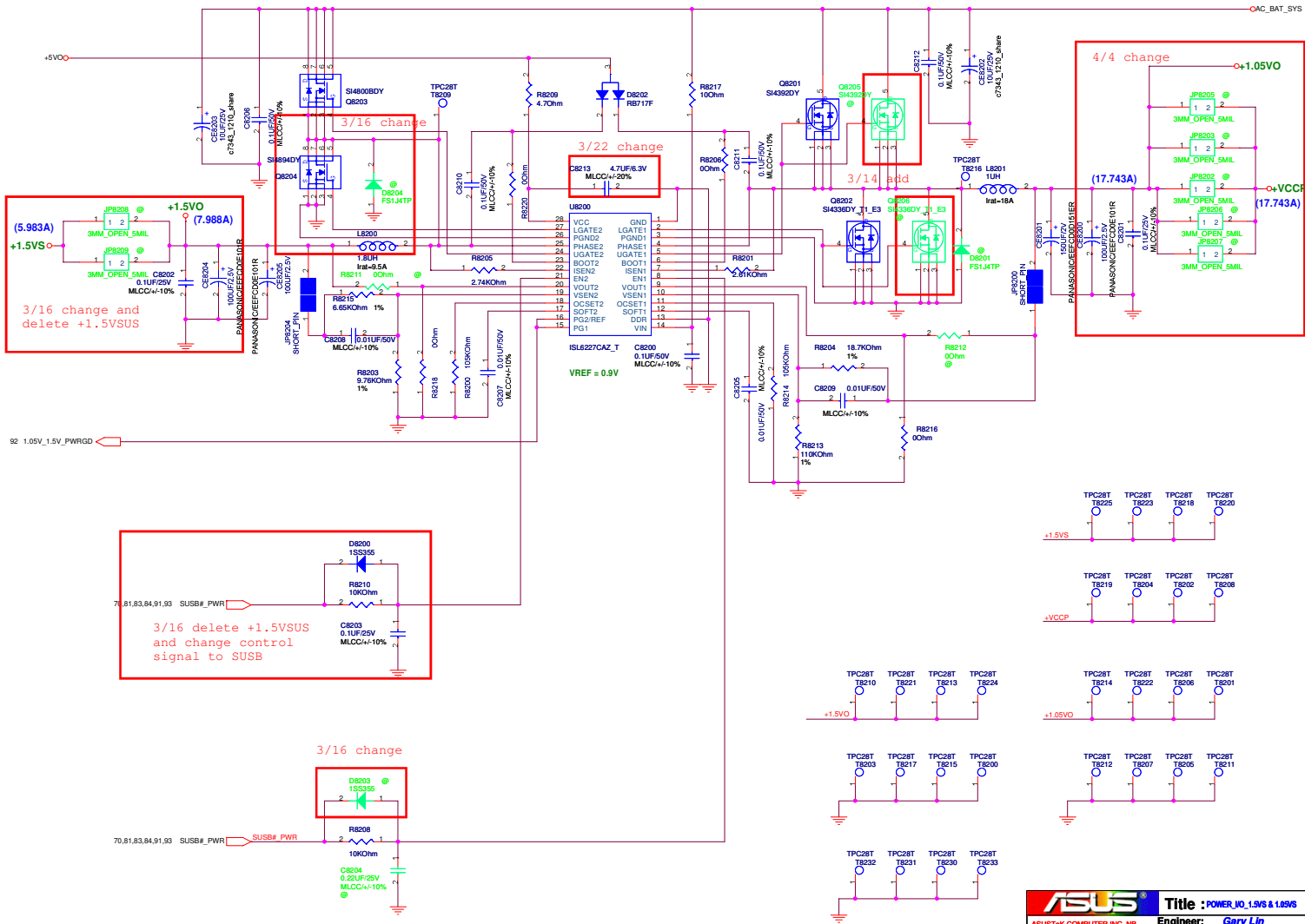
		Title : OTH_****	
ASUSTEK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	68 of 88

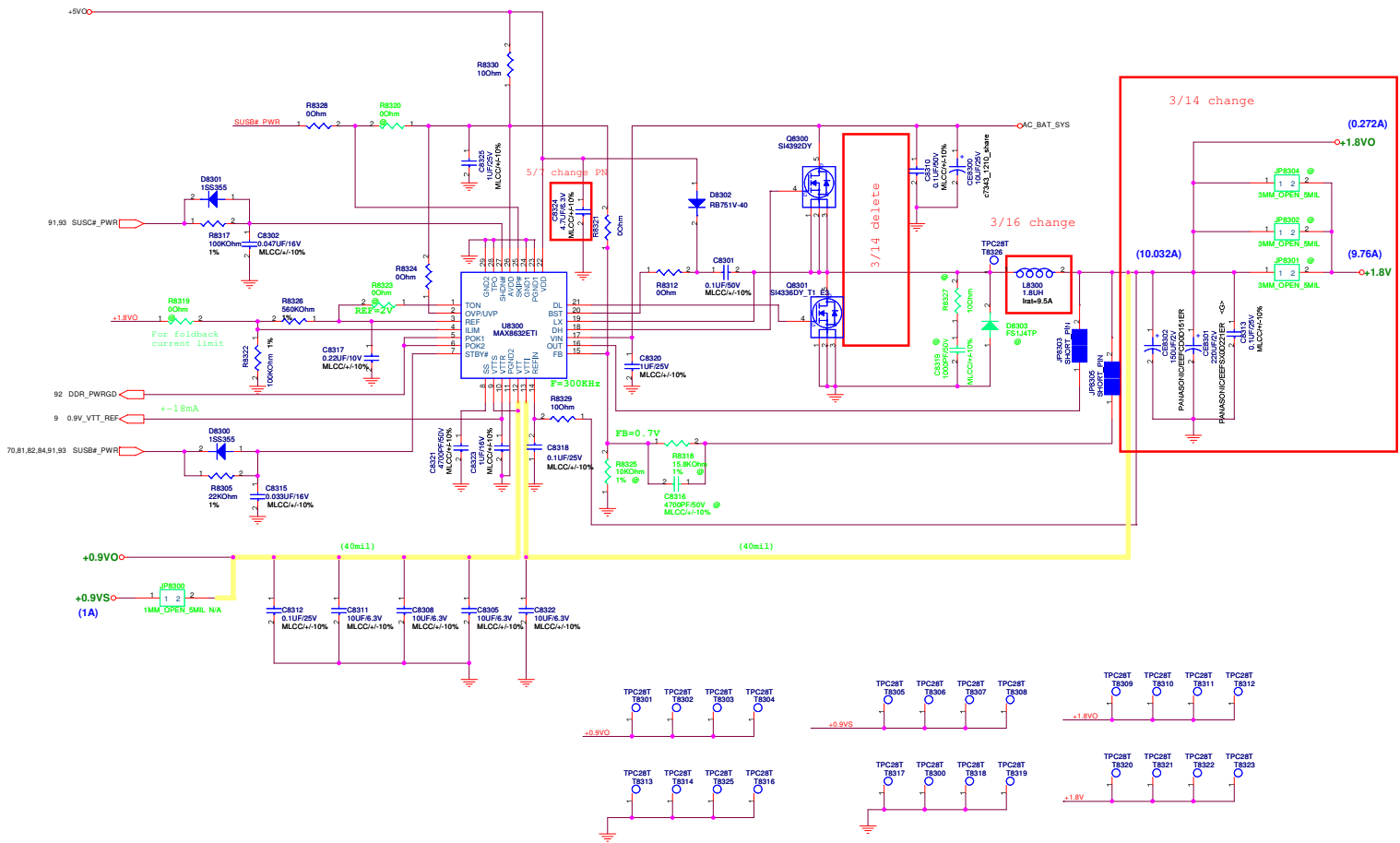


ASUS Logo | Title : VGA_MXM | ASUSTek COMPUTER INC. H61 | Engineer: John Hung | Project Name: M50S/X55S | Date: Monday, September 03, 2007 | Sheet: 70 of 85

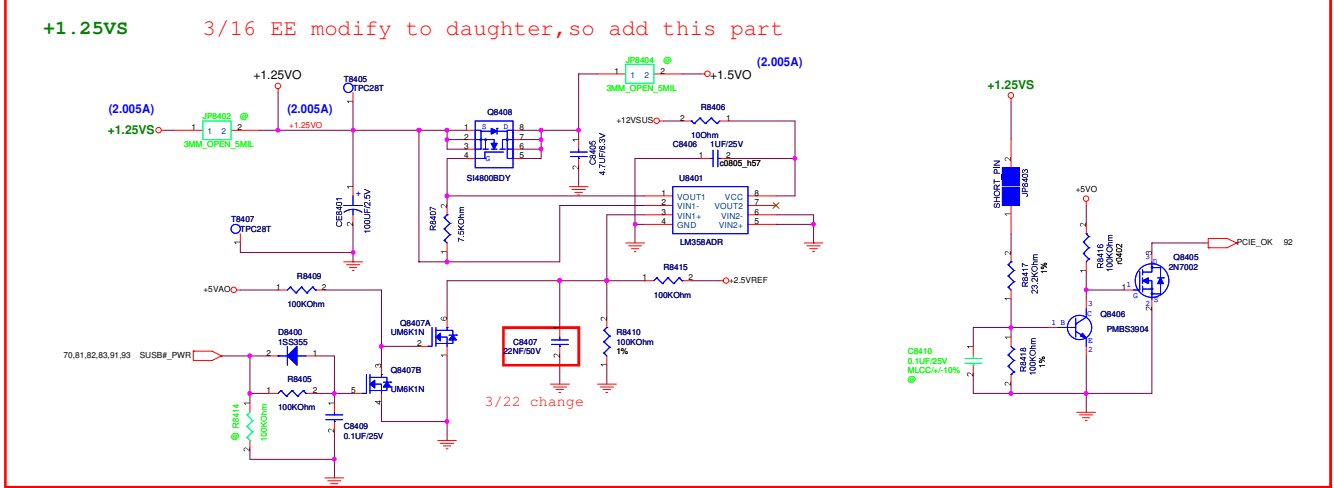








ASUS		Title : POWER_IO_DDR & VTT	
ASUSTEK COMPUTER INC. NB		Engineer: Gary Lin	
Size	Project Name	Rev	1.0
Custom	M50S/X55S	Date	Monday, September 03, 2007
		Sheet	83 of 89



3/16 delete +2.5VSUS

3/14 EE modify to daughter,so delete this page

		Title : N/A	
ASUSTEK COMPUTER INC. NB		Engineer: Gary Lin	
Site	Project Name		Rev
Custom	M50S/X55S		1.0
Date: Monday, September 03, 2007		Sheet 05 of 05	

POWER PATH & BAT_LEARN

90 WATT

● AC_IN Threshold > 0.048Vms AD_DOCK_IN
 > 17.44V active
 Adapter (In/ma) = [0.075V/Rsense/Adm]/[VCLS.VREF]
 ResenseAdm=0.075ms
 VCLS=2.534V
 => In/ma=4.5A
 => Constant Power = 13.145 + 85.5W
 => RST to 200/257/15330K
 Charge Current Ichg = [0.075V/Rsense/CHG]/[VCTL3.VV]
 ResenseCHG=0.075ms
 VCTL3.VV => Ichg = 2.5A
 VCTL3.VV => Ichg = 1.4A
 Vbat = Cell1 [Vbat - (VCTL - 1.5V) / 9.52]
 VCTL = 1.58V
 => Vbat = 4.2V
 Mode pin: Vinode > 2.5V (96 to LDO pin) => 4 Cells
 2.0 Vinode > 1.8V (Booting) => 3 Cells
 0.8 Vinode (96 to DCIN) => Learning mode
 VICT < 0.8V or DCIN < 7V => Charger Disable
 Precharge current=150mA

3/6 change for 3S2P/3S3P only 4/4 deleted

3/16 change
 3/16 change colayout
 4/4 deleted by EE

4/4 deleted

4/17 DELETE BAT_S WITHOUT SHUTDOWN FUNCTION

AC_BAT_SYS_INV to Inverter connect,
 Power Issue =>Email (mail)
 Put JP8805 close to Q8800

MAX8725 LDO
 REF: 4.2235V

MAX8725 REF

MAX8725 LDO

MAX8725 LDO

MAX8725 LDO

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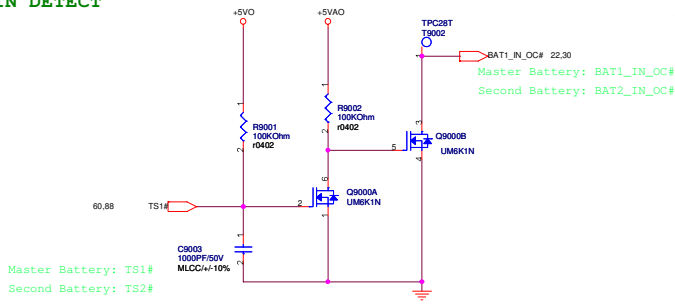
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MAX8725 LDO

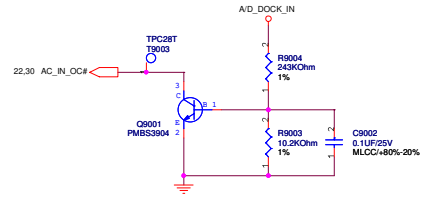
MAX8725 LDO

MAX8725 LDO

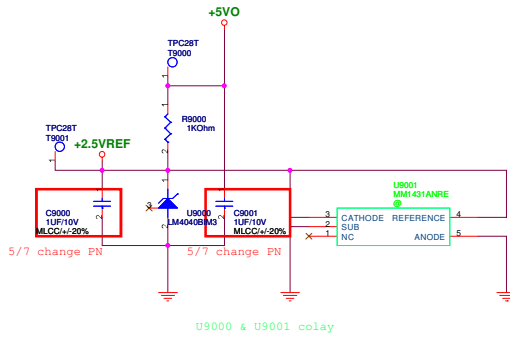
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF

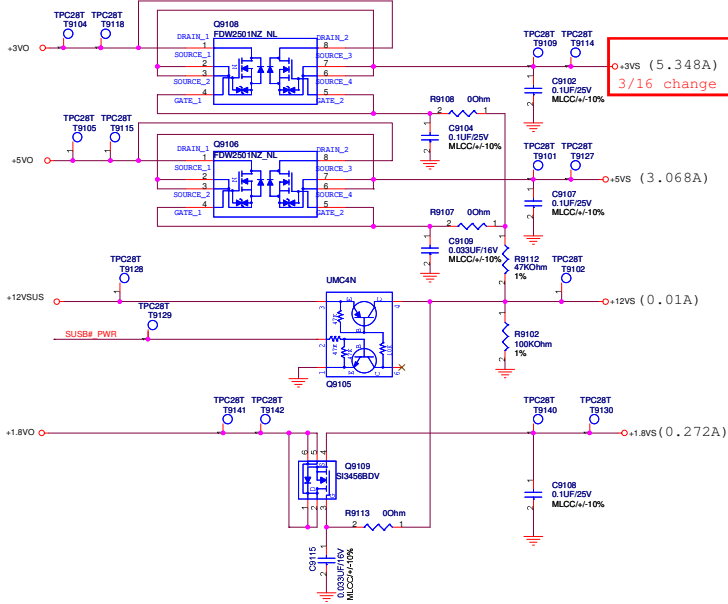


ASUS		Title : POWER_DETECT	
ASUSTEK COMPUTER INC. NB		Engineer: Gary Lin	
Size	Project Name	Rev	
Custom	M50S/X55S	1.0	
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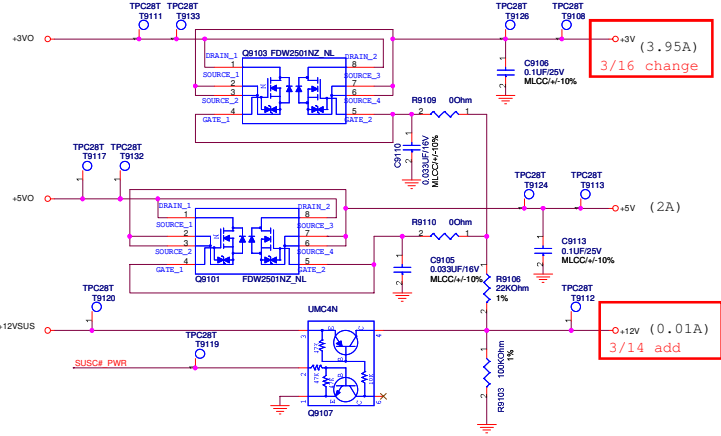
SUSB#_PWR POWER

3/16 delete +1.5VS from load switch

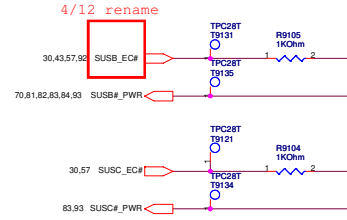
3/14 delete +VRAM



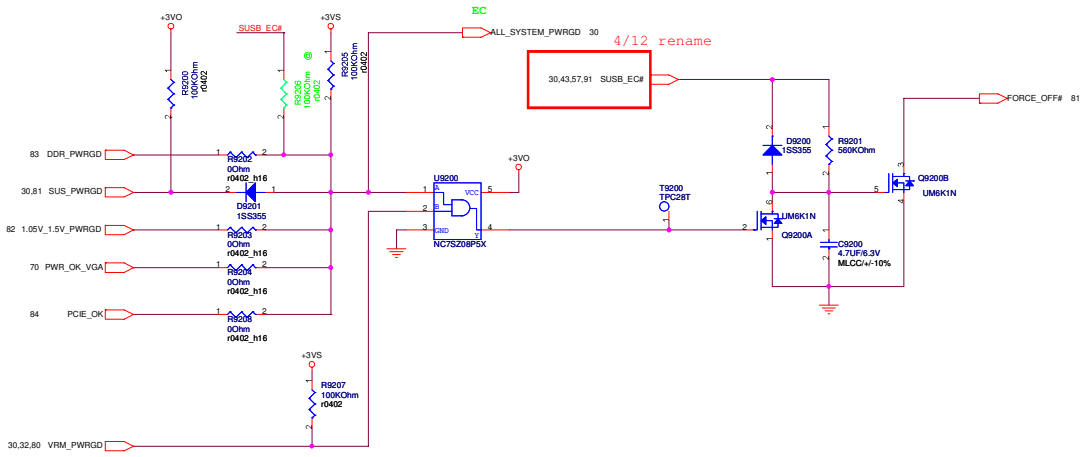
SUSC#_PWR POWER



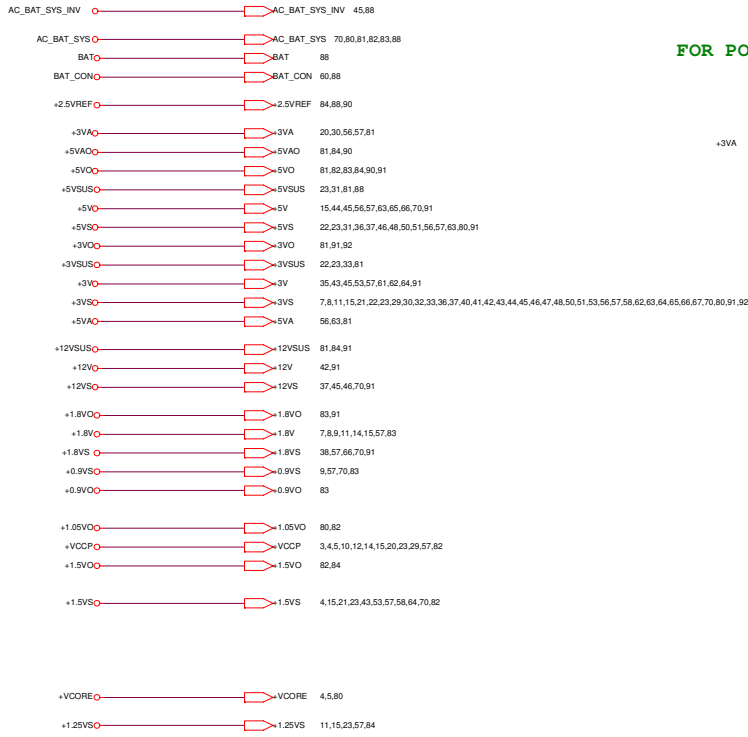
3/16 delete +1.5V



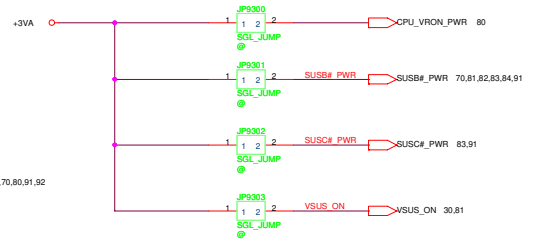
POWER GOOD DETECTOR

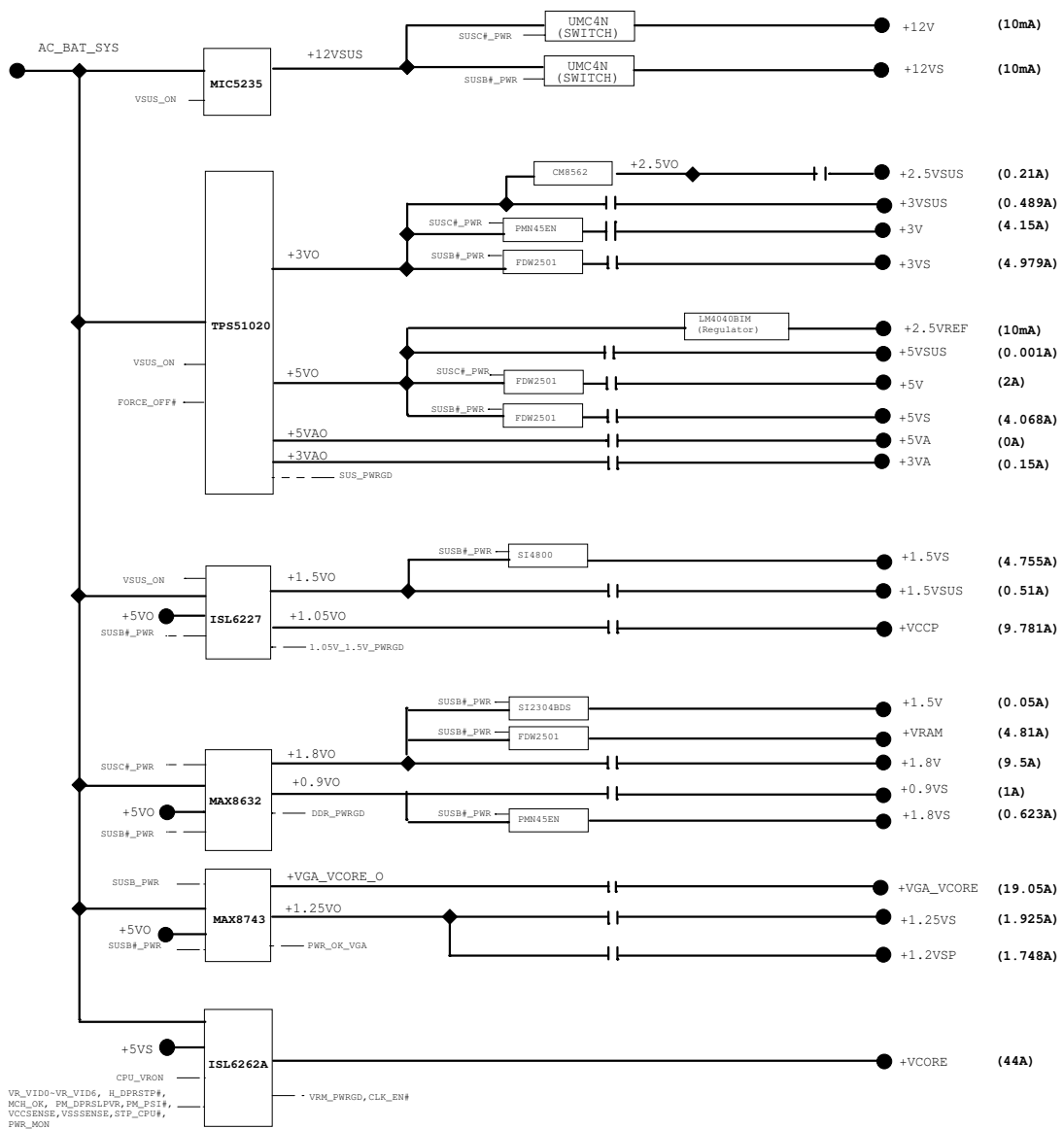


ASUS		Title : POWER_PROTECT	
ASUSTEK COMPUTER INC. NB		Engineer: Gary Lin	
Size	Project Name		Rev
Custom	M50S/X55S		1.0
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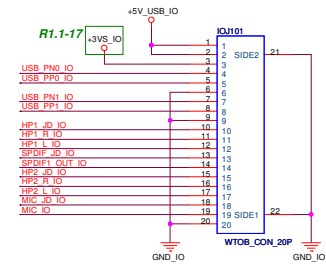


FOR POWER TEST

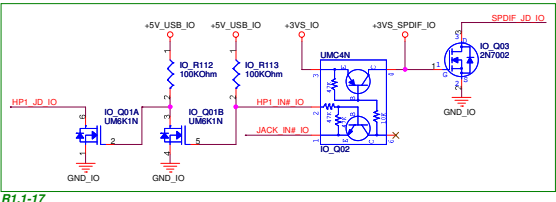
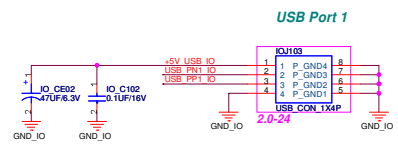
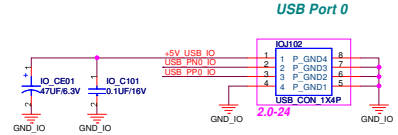




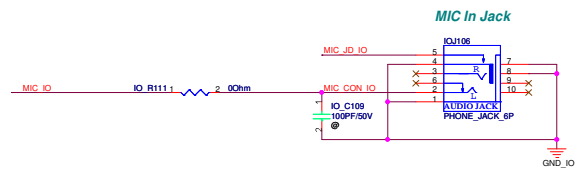
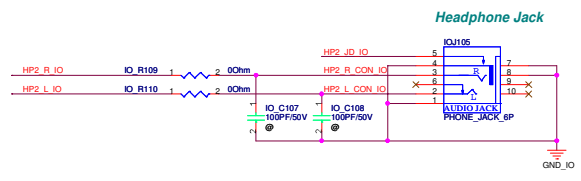
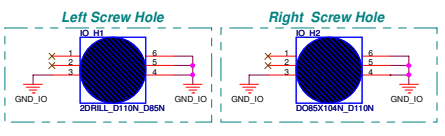
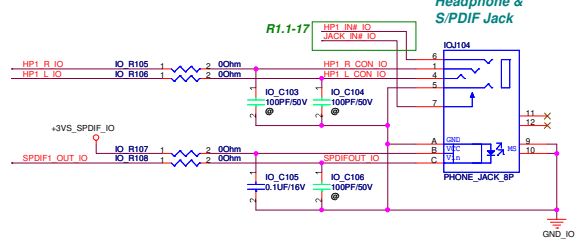
VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRS1PVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON



R1.1-31



R1.1-17



		Title : USB & Audio Jack	
		ASUSTek COMPUTER INC. NBI	Engineer: Wenchi Shen
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet: 85	of 88	

Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		<p>** Merge IO board into main board PCB. Page 95.</p> <p>01.Remove VR_VID[6:0] testing series 0 Ohm. Page 4.</p> <p>02.Change 6pcs +VCCORE capacitors to No-Stuff for cost down. Page 5.</p> <p>03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9.</p> <p>04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45.</p> <p>05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56.</p> <p>06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23.</p> <p>07.Follow R1E to change R2904 to 270ohm. Page 29.</p> <p>08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30.</p> <p>09.PM REquest: Remove USB port charger function. Page 30,65.</p> <p>10.PM change WWAN LED to touch-pad lock LED. Page 30,56.</p> <p>11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31.</p> <p>12.Remove testing 2nd CIR design. Page 31.</p> <p>13.Change X3301 to 49S type for cost down. Page 33.</p> <p>14.LAN chip version change. Page 33.</p> <p>15.Audio codec chip change version. Page 36.</p> <p>16.N1Sv/X55 will not supprot 3G function. Page 36,67.</p> <p>17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95.</p> <p>18.Modify audio de-pop circuit. Page 36,37.</p> <p>19.Modify LVDS power sequence failed bug. Page 45.</p> <p>20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70.</p> <p>21.Remove HDIV support function. Page 47,70.</p> <p>22.Remove HDMI EMI filter design. Page 48.</p> <p>23.X55 need two pwer LEDs. Page 56.</p> <p>24.PM change WLAN LED to RF LED. Page 56,63.</p> <p>25.Bluetooth pin define error. Page 61.</p> <p>26.Remove co-layout sequence logic control circuit. Page 68.</p> <p>27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65.</p> <p>28.EMI modification. Page 34,36,65.</p> <p>29.Crystal accuracy fine-tune. Page</p> <p>30.USB droop test fail. Page 65.</p> <p>31.Remove IO board USB common choke design. Page 95.</p> <p>32.Speaker fine-tune. Page 37.</p> <p>33.Cost down for 4-wire PWM fan. Page 50.</p> <p>34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.</p>
R2.0 Pink Block		<p>01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15.</p> <p>02.Add CMOS crack protection circuit. Page 22.</p> <p>03.Reserve C2337 (10UF/16V) for +5VREF_ICH. Page 23.</p> <p>04.Change ICS9LPR363 version from D to E for SATA clock jitter improve. Page 29.</p> <p>05.With EMI's confirmation, replace R2901, R2905, R2906 with short-pad JP2901, JP2902, JP2903. Page 29.</p> <p>06.With EC's confirmation, change ITE8752 P/N to 06G042016011. Page 30.</p> <p>07.With EMI's confirmation, replace R3001 with short-pad JP3002. Page 30.</p> <p>08.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34.</p> <p>09.With EMI's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624, R3626 to short-pad JP3601-JP3607. And change R3611, R3613, R3623, R3625 to No-Stuff. Page 36.</p> <p>10.Post wave sounds abnormal when audio amplifier use GMT G1431. Change C3706 to 0.33UF to shorten audio amplifier start-up time. Page 37.</p>

Rev	Date	Description
		<p>11.For cost down, change CE3701-CE3704 to 47UF. And after EA test, these can pass Vista audio criteria. Page 37.</p> <p>12.With EMI's confirmation, remove reserved 1394 common choke circuit. Page 41.</p> <p>13.With EMI's confirmation, remove reserved NewCard USB common choke circuit. Page 43.</p> <p>14.Add NewCard debug card co-layout circuit. Page 44.</p> <p>15.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45.</p> <p>16.With EMI's confirmation, replace RX4603, RX4604 with JP4601, JP4602. Page 46.</p> <p>17.HDMI jack detection modification. Page 48,70.</p> <p>18.With EMI's confirmation, replace RX4809, RX4810 with JP4801, JP4802. Page 48.</p> <p>19.Change PWM FAN capacitors to 10UF. Page 50.</p> <p>20.Modify X55S power LED design. Page 56.</p> <p>21.Modify DC_IN bead for 120W design. Page 60.</p> <p>22.With EMI's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 66.</p> <p>23.Reserve R8023 for shortage issue of ISL6262A. Page 80.</p> <p>24.QTR USB plug test failed, change USB connector. Page 95.</p>

		Title : Revision History	
ASUSTek COMPUTER INC. NBI		Engineer: John Hung	
Site	Project Name	Rev	
Custom	M50S/X55S	1.0	
Date: Wednesday, September 05, 2007		Sheet	98 of 98