

K23

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

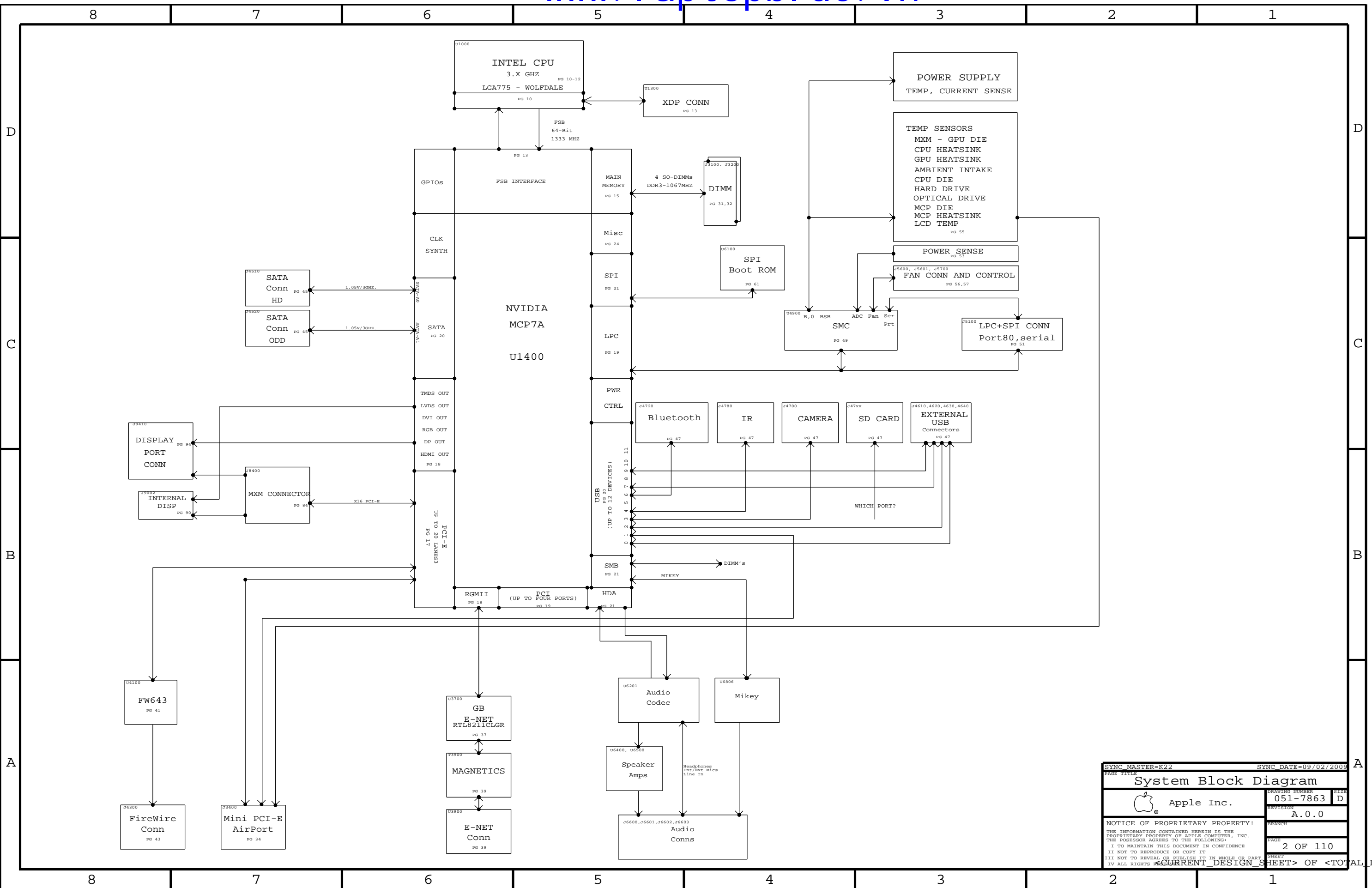
REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0000774489	PRODUCTION RELEASED		2009-08-20

LAST_MODIFIED=Wed Sep 2 16:45:56 2009

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DRAWING TITLE		SCH, K23, MLB	
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System Block Diagram

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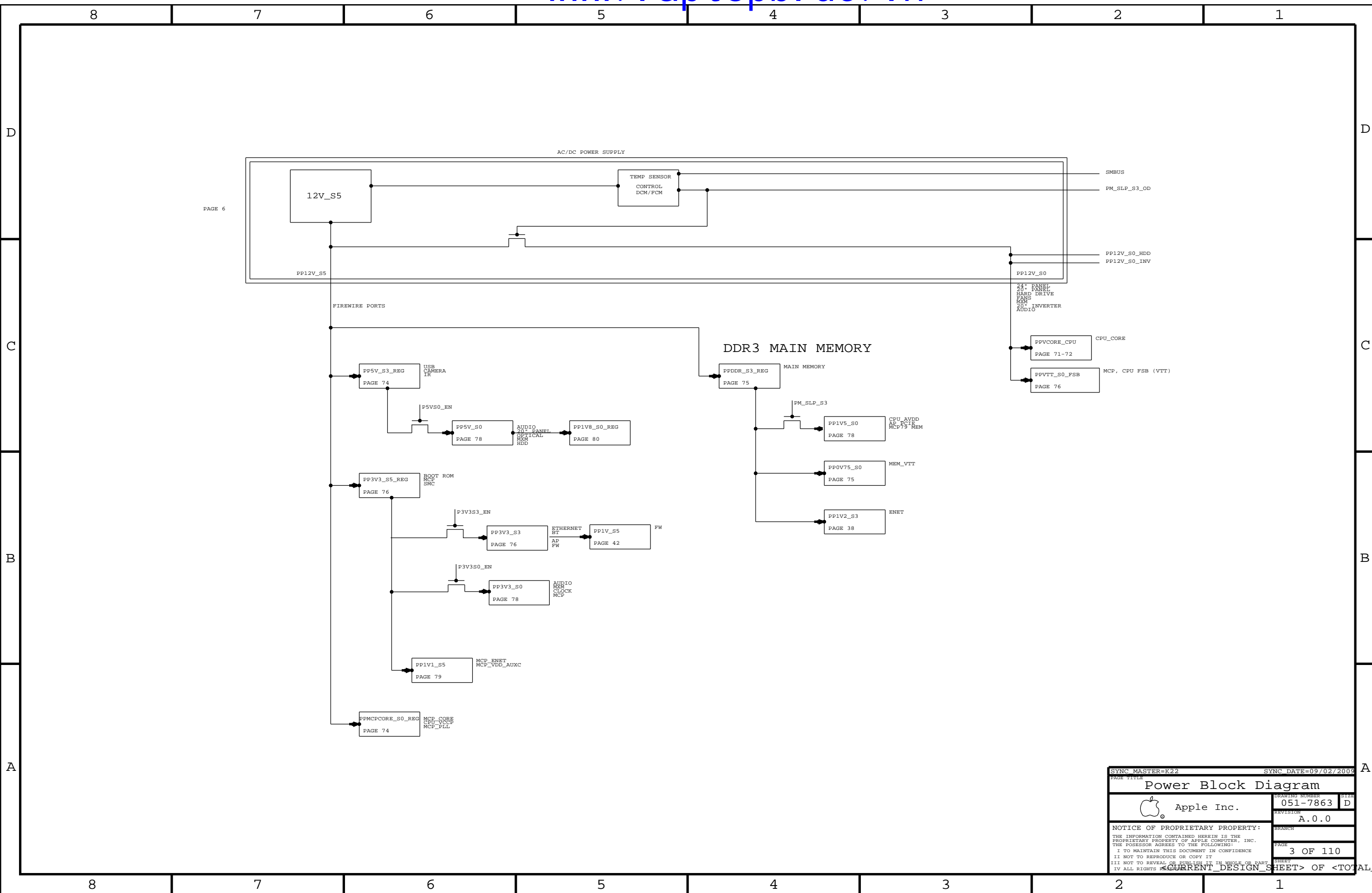
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Power Block Diagram			
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9879	PCBA,MLB,BETTER,K23	K23,2P80GHZ_CPU,BASIC,MXM,K23_MXM
639-0394	PCBA,MLB,2.80 GHZ-2M,K23	K23,2P80GHZ_2M_CPU,BASIC,MXM,K23_MXM
639-0185	PCBA,MLB,2.93 GHZ,K23	K23,2P93GHZ_CPU,BASIC,MXM,K23_MXM
630-9983	PCBA,MLB,BEST,K23	K23,3P0GHZ_CPU,BASIC,MXM,K23_MXM
639-0509	PCBA,MLB,3.06 GHZ,K23	K23,3P06GHZ_CPU,BASIC,MXM,K23_MXM
639-0109	PCBA,MLB,3.16 GHZ,K23(INVESTIGATION)	K23,3P16GHZ_CPU,BASIC,MXM,K23_MXM
630-9880	PCBA,MLB,ULTIMATE,K23	K23,3P33GHZ_CPU,BASIC,MXM,K23_MXM
607-4427	PCBA,MLB,DEV,K23	DEVELOPMENT,DEV_GROUP

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0731	1	IC,GMCP,MCP7A-JA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	IG
338S0732	1	IC,MCP,MCP7A-DA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	MXM
341T0170	1	IC,EFI BOOTROM,K22/K23	U6100	CRITICAL	
338S0765	1	IC,XI02211ZAY,1394B,167BGA	U4100	CRITICAL	
338S0694	1	IC,RTL8251CA,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

MCP -J SKU HAS INTEGRATED GPU
MCP -D SKU DOES NOT

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3745	1	WLF,QXXX,QS,2.80G,65W,1066,RO,3M,LGA	CPU	CRITICAL	2P80GHZ_CPU
337S3742	1	WLF,SL89J,PRO,2.83G,65W,1333,EO,6M,LGA	CPU	CRITICAL	2P83GHZ_CPU
337S3726	1	WLF,SL89J,PRO,3.0G,65W,1333,EO,6M,LGA	CPU	CRITICAL	3P0GHZ_CPU
337S3715	1	WLF,SL89K,PRO,3.16G,65W,1333,EO,6M,LGA	CPU	CRITICAL	3P16GHZ_CPU
337S3727	1	WLF,SL89L,PRO,3.33G,65W,1333,EO,6M,LGA	CPU	CRITICAL	3P33GHZ_CPU
337S3807	1	WLF,SL89L,PRO,2.93G,65W,1333,EO,6M,LGA	CPU	CRITICAL	2P93GHZ_CPU
337S3766	1	WLF,SL89L,PRO,3.06G,65W,1333,EO,6M,LGA	CPU	CRITICAL	3P06GHZ_CPU
337S3804	1	WLF,SL899,PRO,2.80G,65W,1066,RO,2M,LGA	CPU	CRITICAL	2P80GHZ_2M_CPU

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP7A,XDP,BETTER,MCP_ISL9563A,PRODUCTION
MCP7A	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP
DEV_GROUP	XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE,MCP_CPU_TDIODE,PECI_SMB,MOJOMUX


K23 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7863	1	SCH,K23,MLB	SCH1		K23
820-2507	1	PCBF,K23,MLB	MLB1		K23
(338S0489 - BLNK) 341T0169	1	IC,SMC,K23	U4900	CRITICAL	K23

ALTERNATES


BOARD STACK-UP

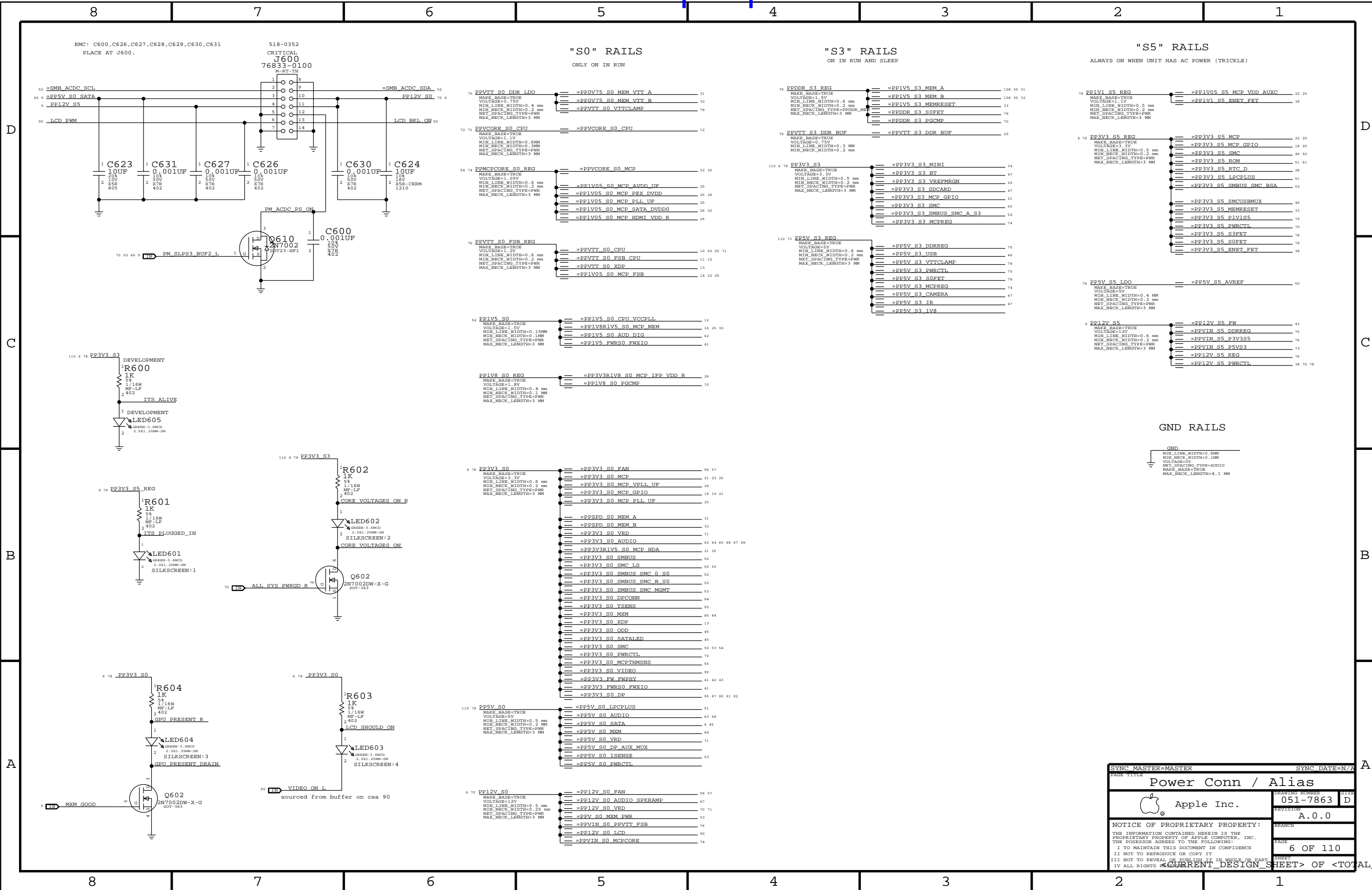
TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

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BOM Configuration			
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EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TR

"S0" RAILS
ONLY ON IN RUN

"S3" RAILS
ON IN RUN AND SLEEP

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

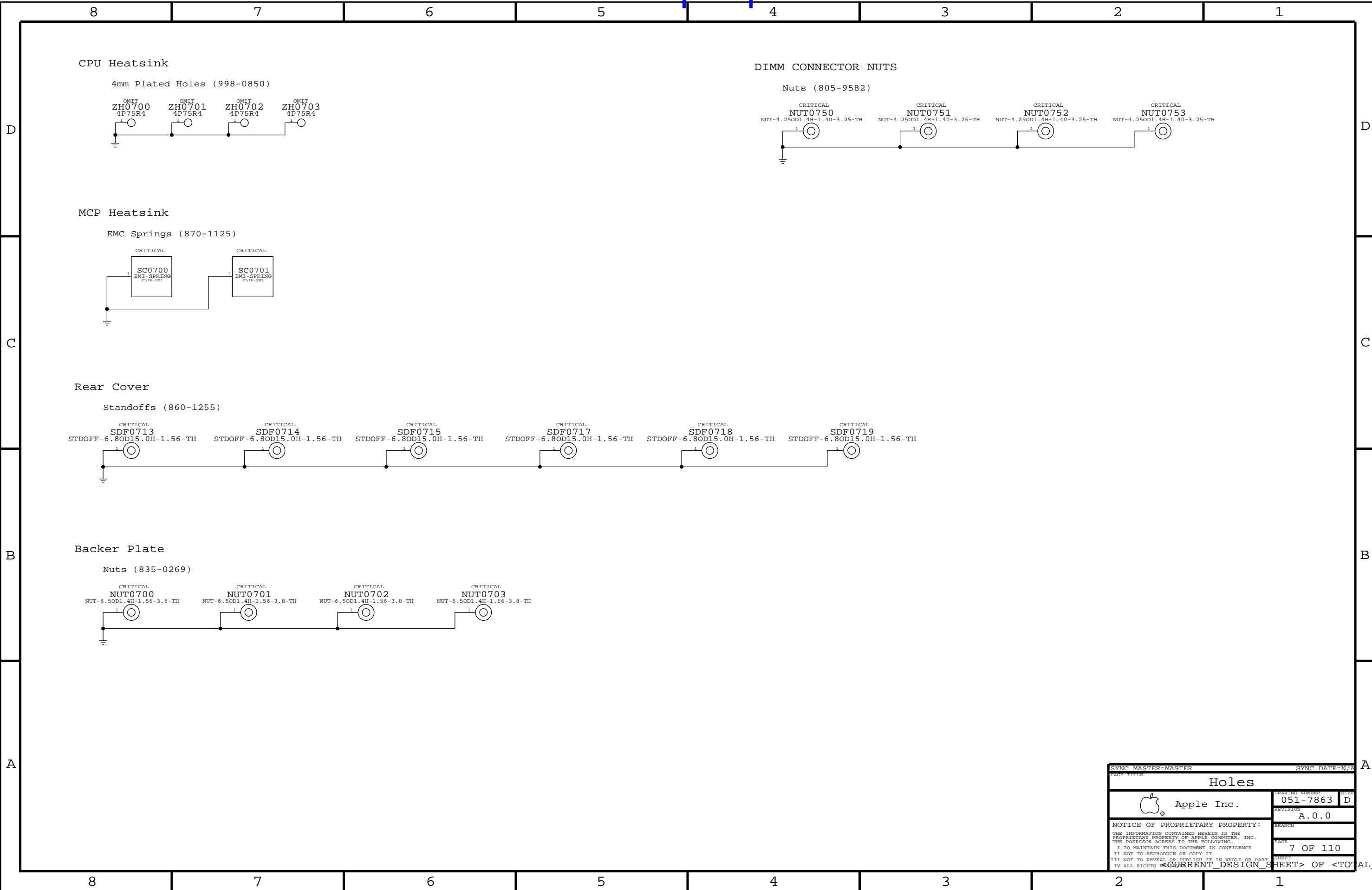
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Power Conn / Alias

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Holes			
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NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	==	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_TV_DAC_VREF	==	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	==	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	==	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_R_C_PR	==	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_G_Y_Y	==	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	==	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_HSYNC	==	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_VSYNC	==	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	==	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	==	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_AD<31..15>	==	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_IRDY_L	==	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_C_BE_L<1..0>	==	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_SERR_L	==	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_DEVSEL_L	==	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_PERR_L	==	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_LPC_DRQ0_L	==	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	==	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_ENET_INTR_L	==	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	==	NC_ENET_PWRDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	==	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_GPIO_18	==	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	==	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_C_BE_L<3>	==	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_CLK0	==	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_CLK1	==	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_FRAME_L	==	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_GNT0_L	==	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_GNT1_L	==	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_INTW_L	==	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_INTX_L	==	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_INTY_L	==	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_INTZ_L	==	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_PAR	==	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_RESET1_L	==	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_STOP_L	==	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_TRDY_L	==	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	==	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	==	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	==	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	==	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	==	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	==	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_PRSNL_L	==	NC_PCIE_EXCARD_PRSNL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	==	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_PRSNL_L	==	NC_PE4_PRSNL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_SB_A20GATE	==	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10N	==	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10P	==	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_N	==	NC_USB_MINI_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_P	==	NC_USB_MINI_P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_N	==	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_P	==	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
21	ODD_PWR_EN_L	==	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	==	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	==	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	EXCARD_CLKREQ_L	==	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_AD<12..10>	==	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_PCI_AD<8>	==	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE

17	TP_PCIE_PE4_R2D_CP	==	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	==	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	==	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	==	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	==	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	==	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	==	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	==	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_N	==	NC_USB_TPAD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_P	==	NC_USB_TPAD_P	MAKE_BASE=TRUE	NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	==	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_A_CLK2N	==	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5P	==	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5N	==	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2P	==	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2N	==	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5P	==	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5N	==	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	==	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	GMUX_JTAG_TDO	==	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE
18	GMUX_JTAG_TDI	==	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE
18	GMUX_JTAG_TMS	==	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE

SYNC MASTER=K22 SYNC DATE=09/02/2009

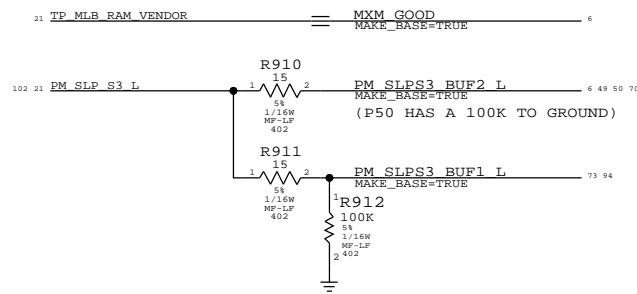
UNUSED SIGNAL ALIAS

Apple Inc.	051-7863	D
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PAGE	8 OF 110	
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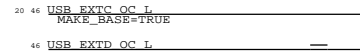
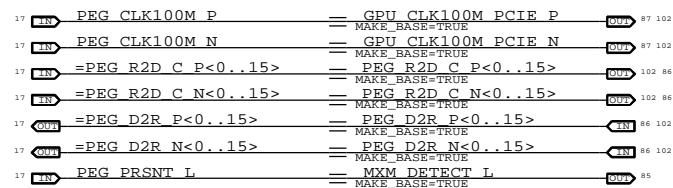
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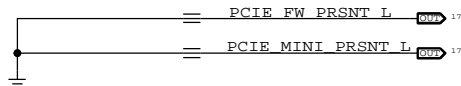
SIGNAL ALIAS



PEG Slot Support

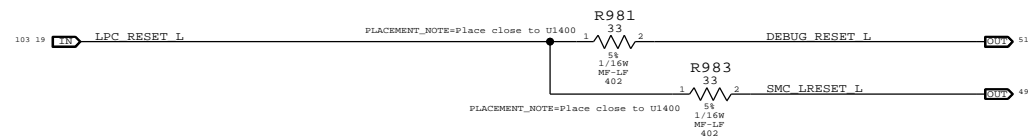


K22/K23 Use one GPIO for both ports 2&3 OC
USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

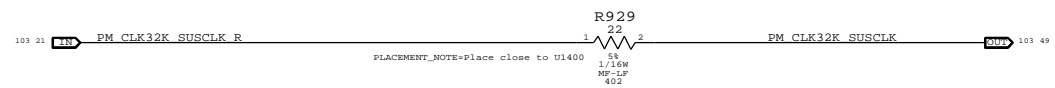
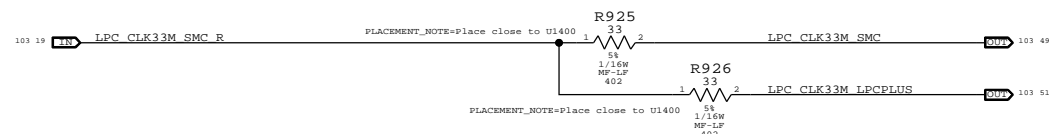
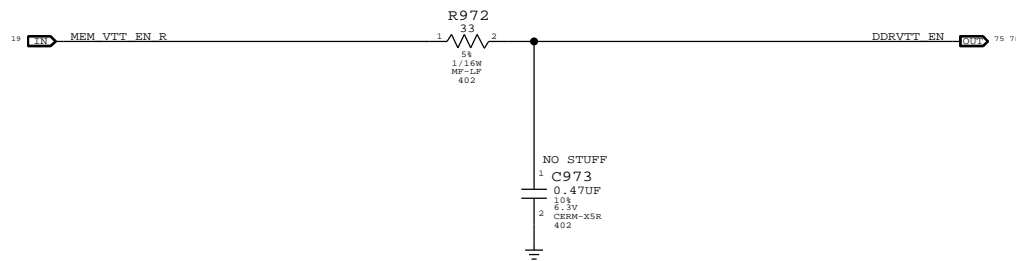
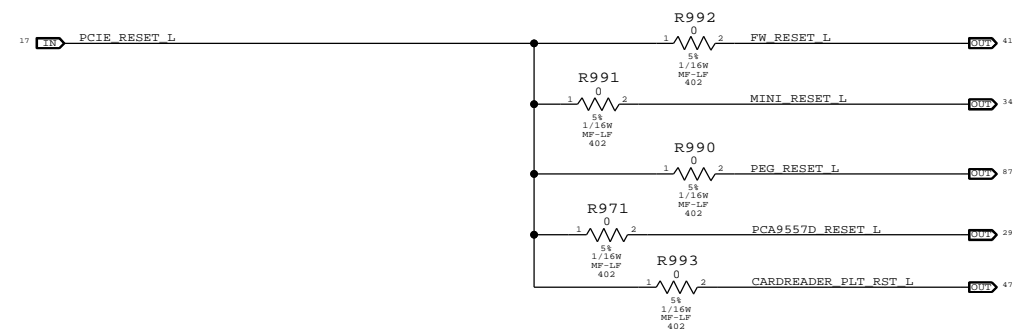


Platform Reset Connections

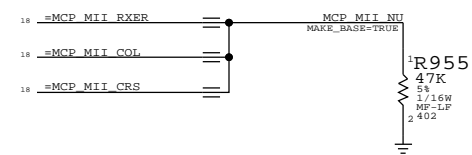
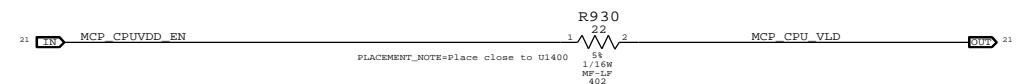
LPC Reset (Unbuffered)



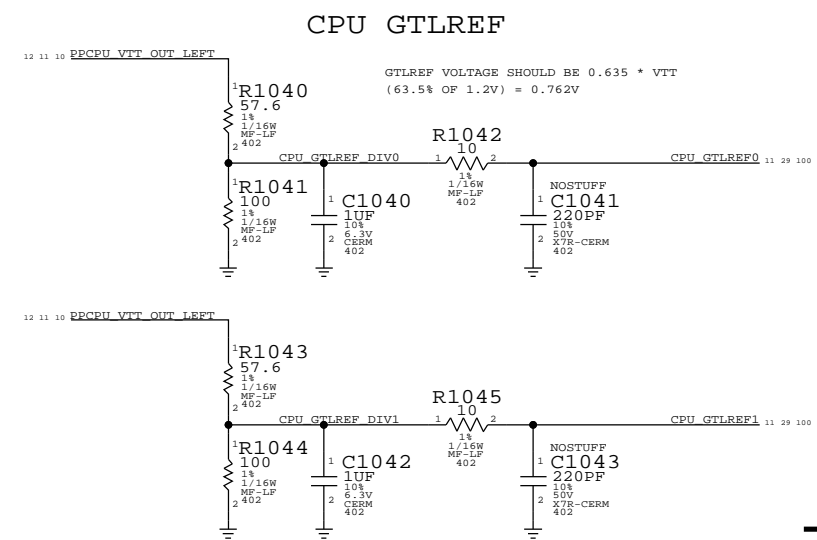
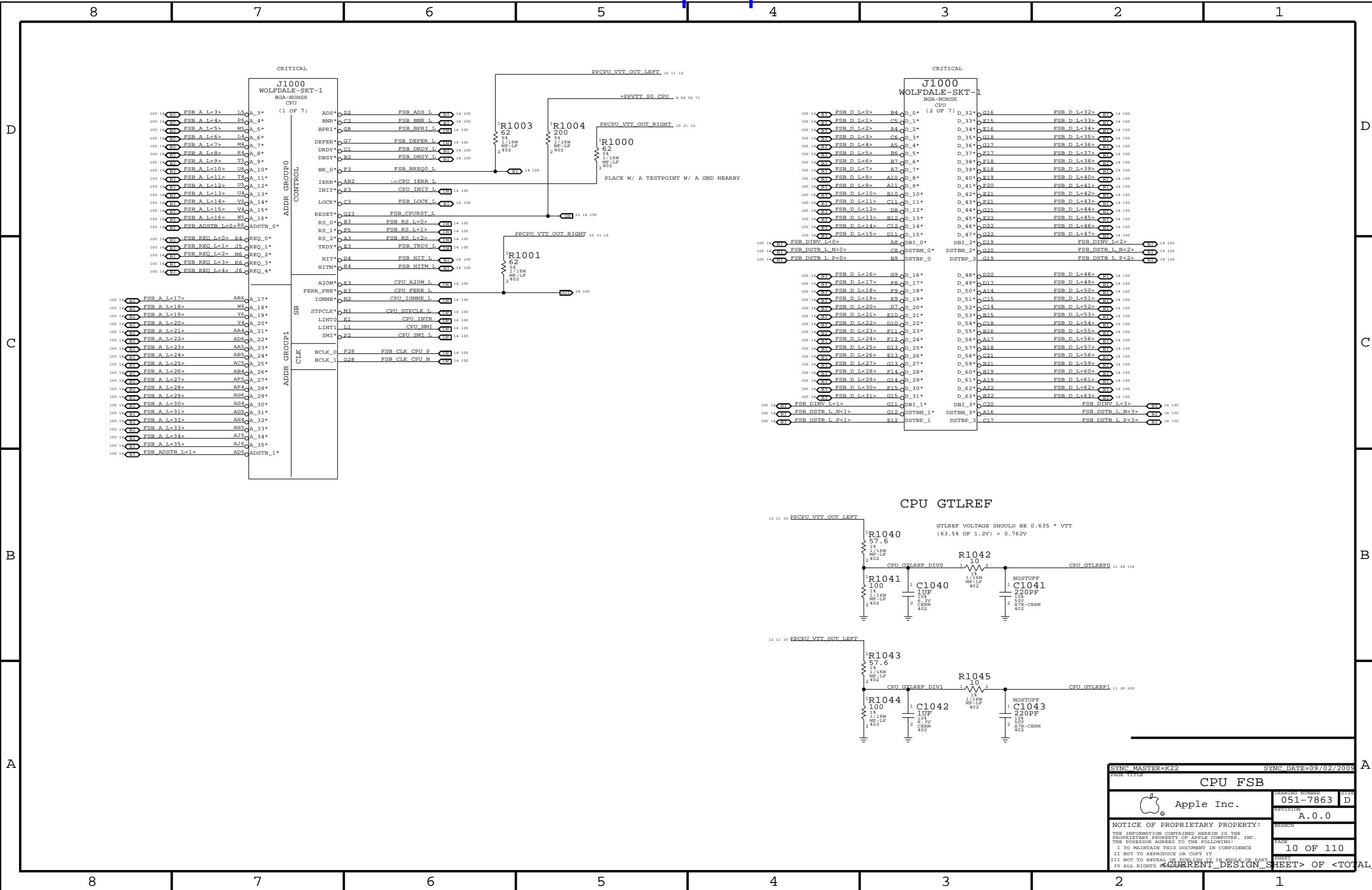
PCIE Reset (Unbuffered)



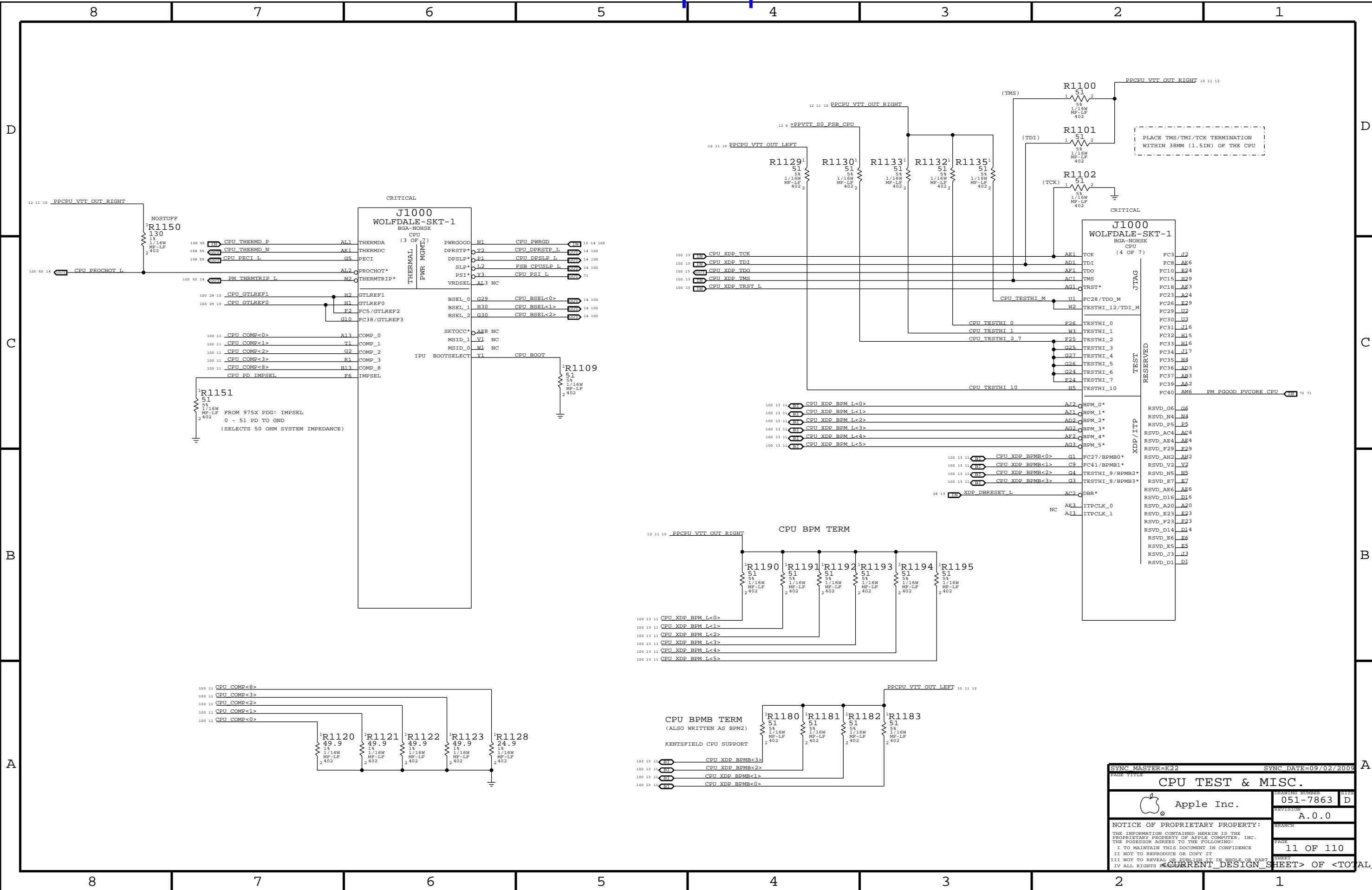
MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP



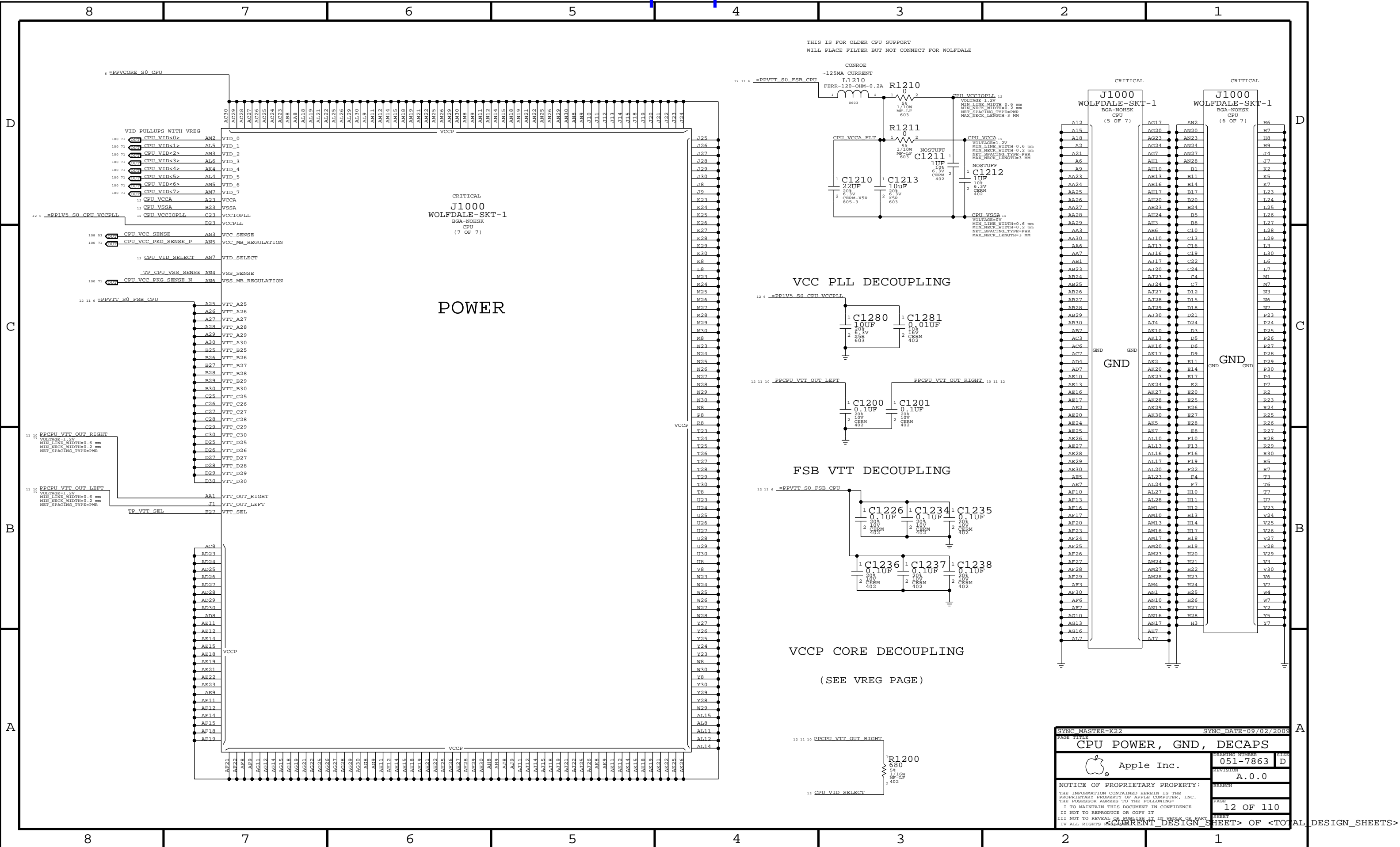
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Signal Aliases			
Apple Inc.		DRAWING NUMBER	SIZE
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CPU FSB			
Apple Inc.		DRAWING NUMBER	051-7863 D
		REVISION	A.0.0
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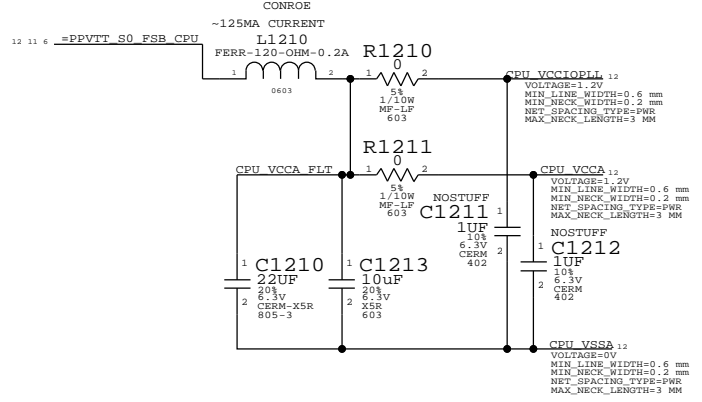
SYNC MASTER=K22		SYNC DATE=09/02/2009	
CPU TEST & MISC.			
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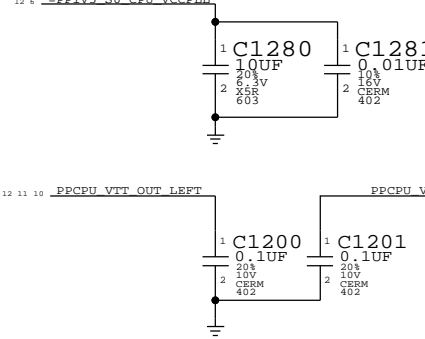
CRITICAL
J1000
 WOLFDAL-SKT-1
 BGA-NOHSK
 CPU
 (7 OF 7)

POWER

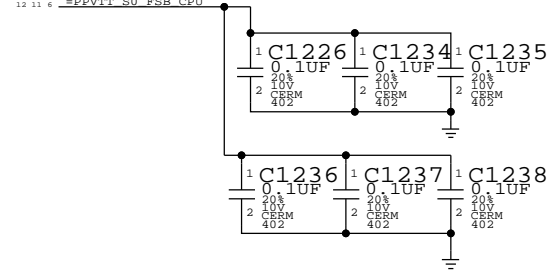
THIS IS FOR OLDER CPU SUPPORT
 WILL PLACE FILTER BUT NOT CONNECT FOR WOLFDAL



VCC PLL DECOUPLING

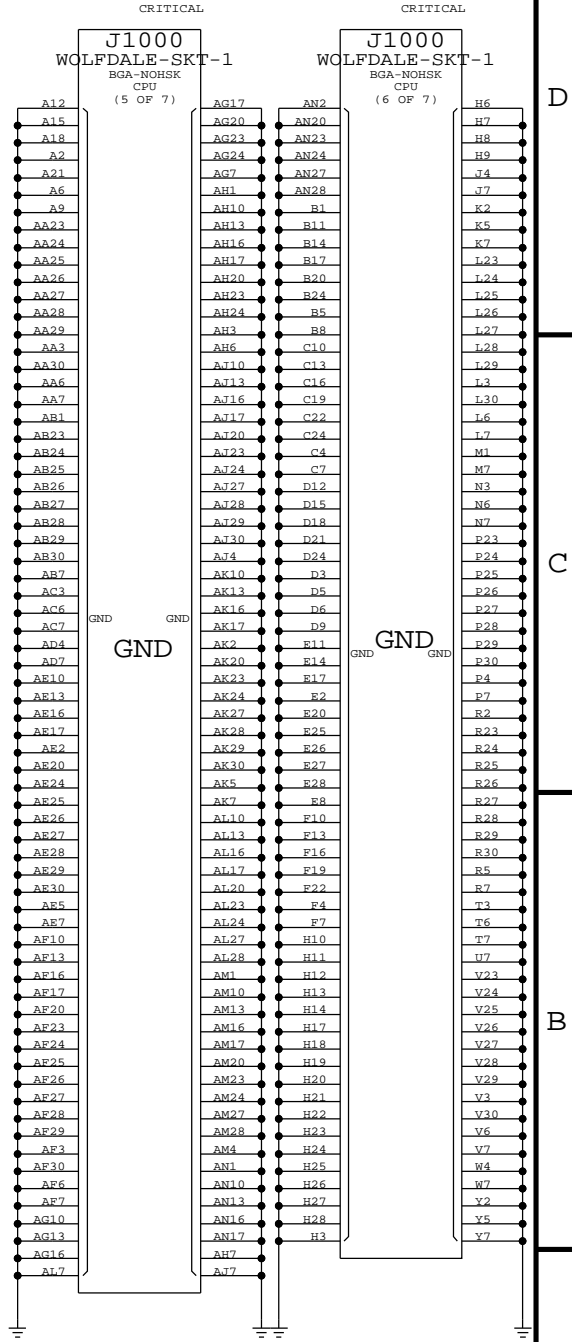


FSB VTT DECOUPLING

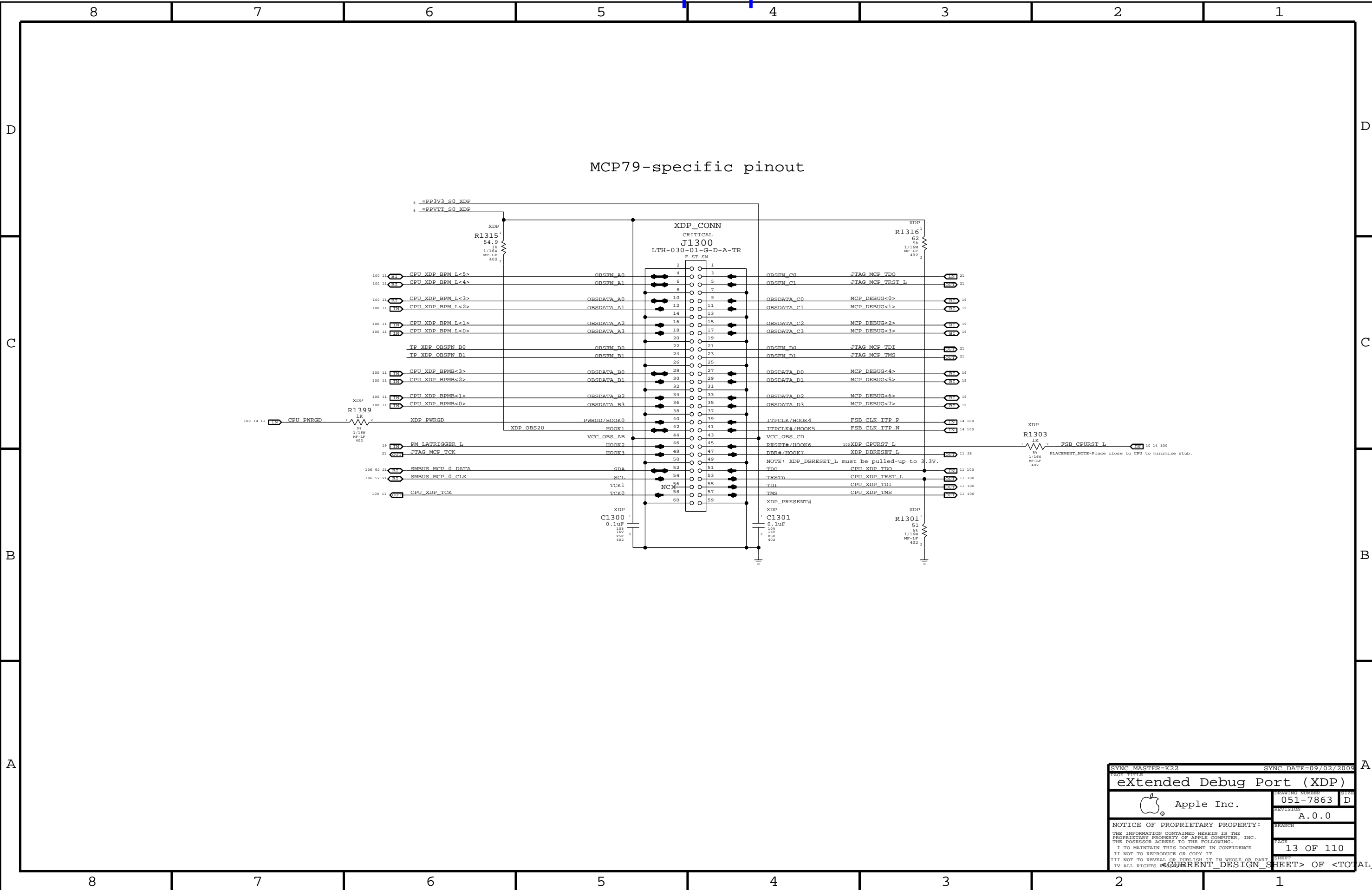



VCCP CORE DECOUPLING

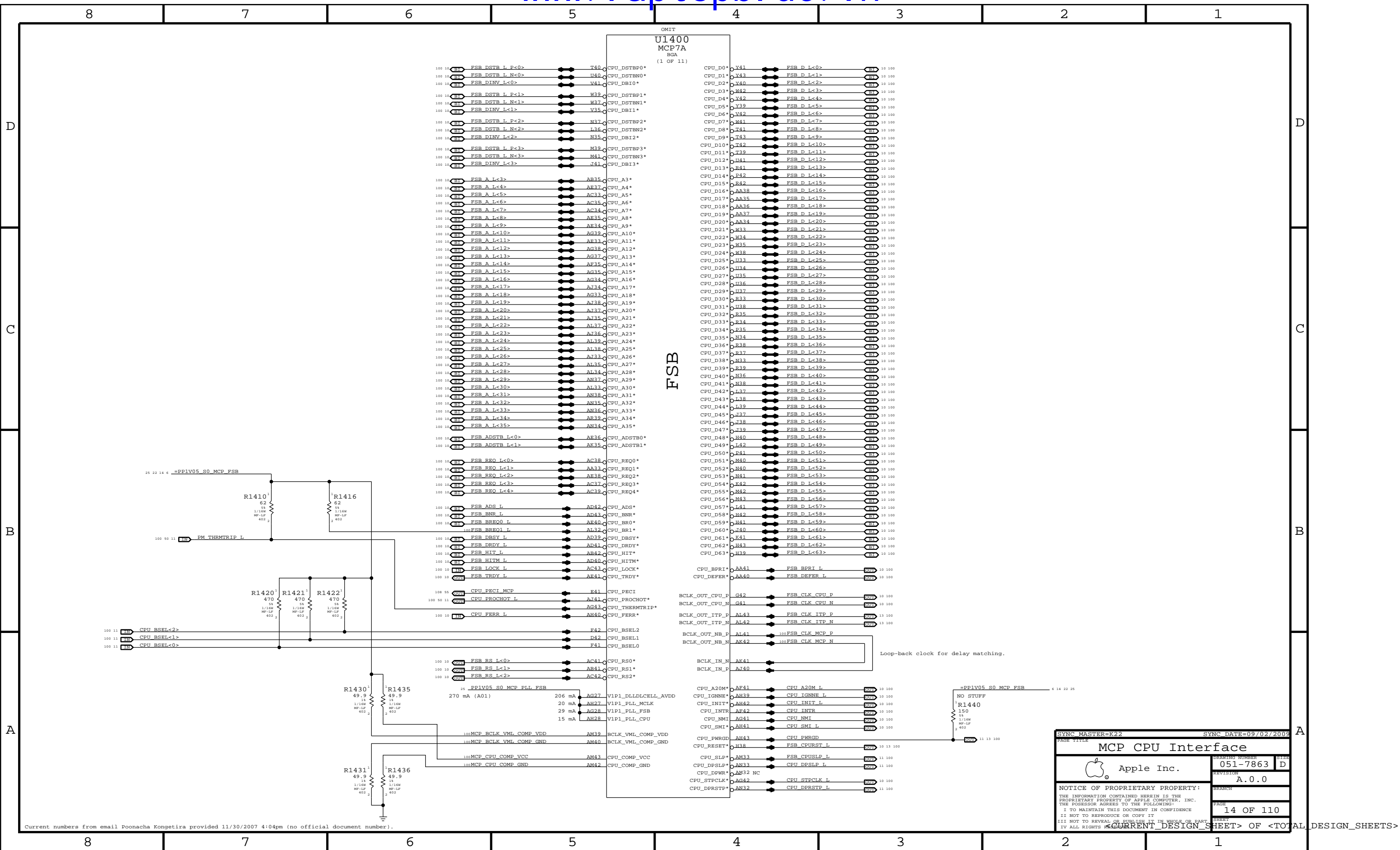
(SEE VREG PAGE)



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CPU POWER, GND, DECAPS			
Apple Inc.		DRAWING NUMBER 051-7863	REVISION D
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eXtended Debug Port (XDP)					
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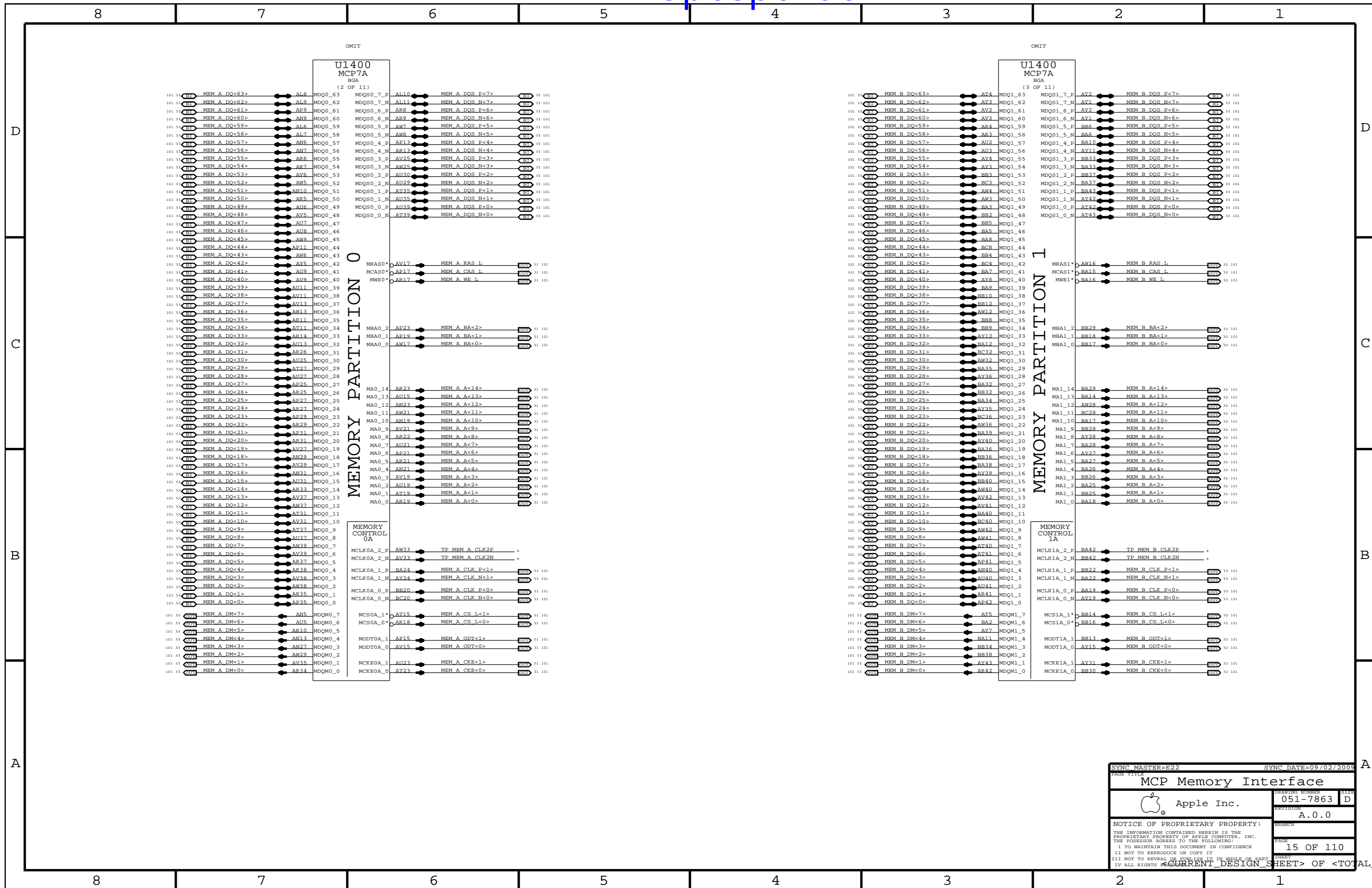
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MCP Memory Interface

Apple Inc.

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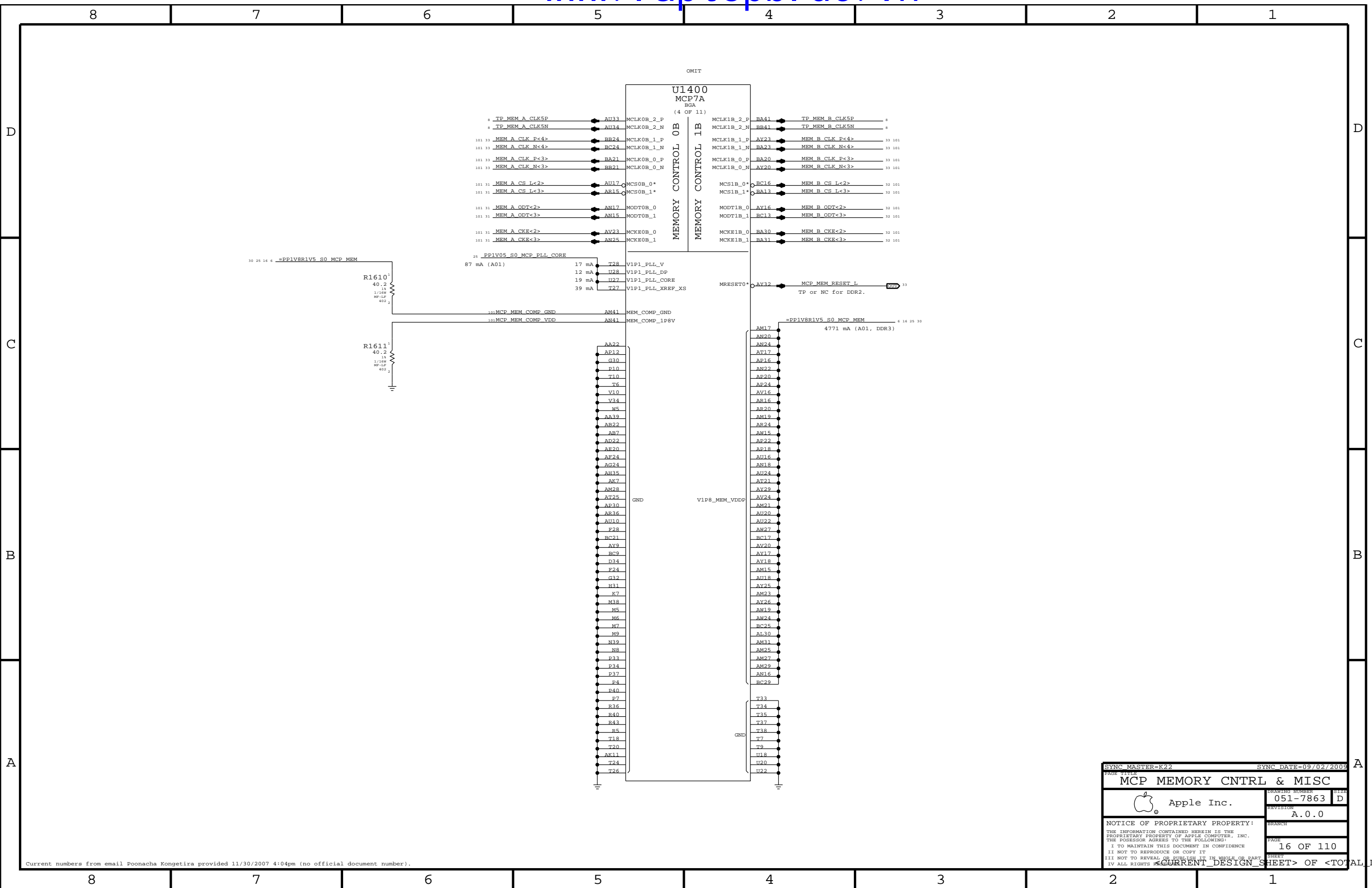
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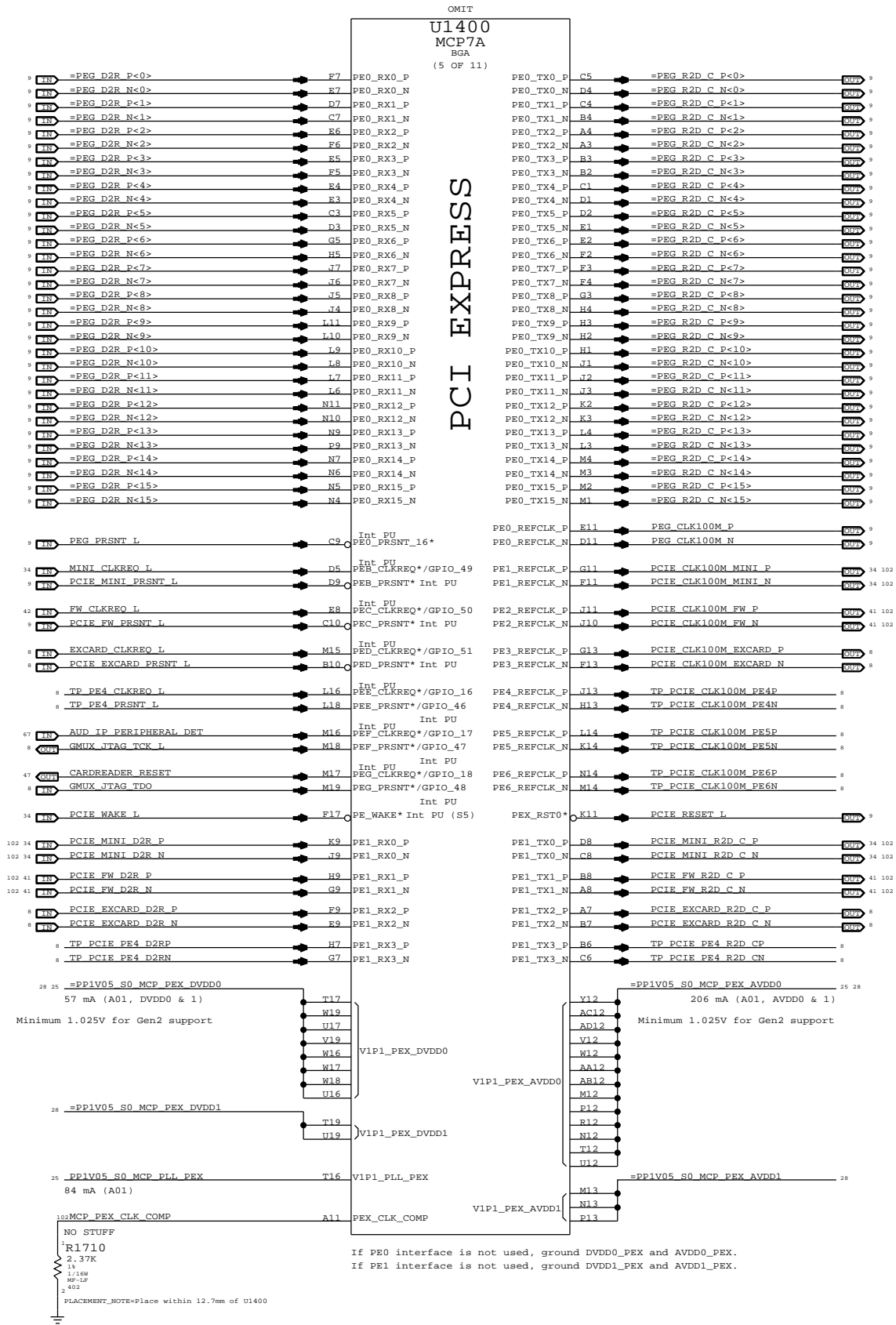
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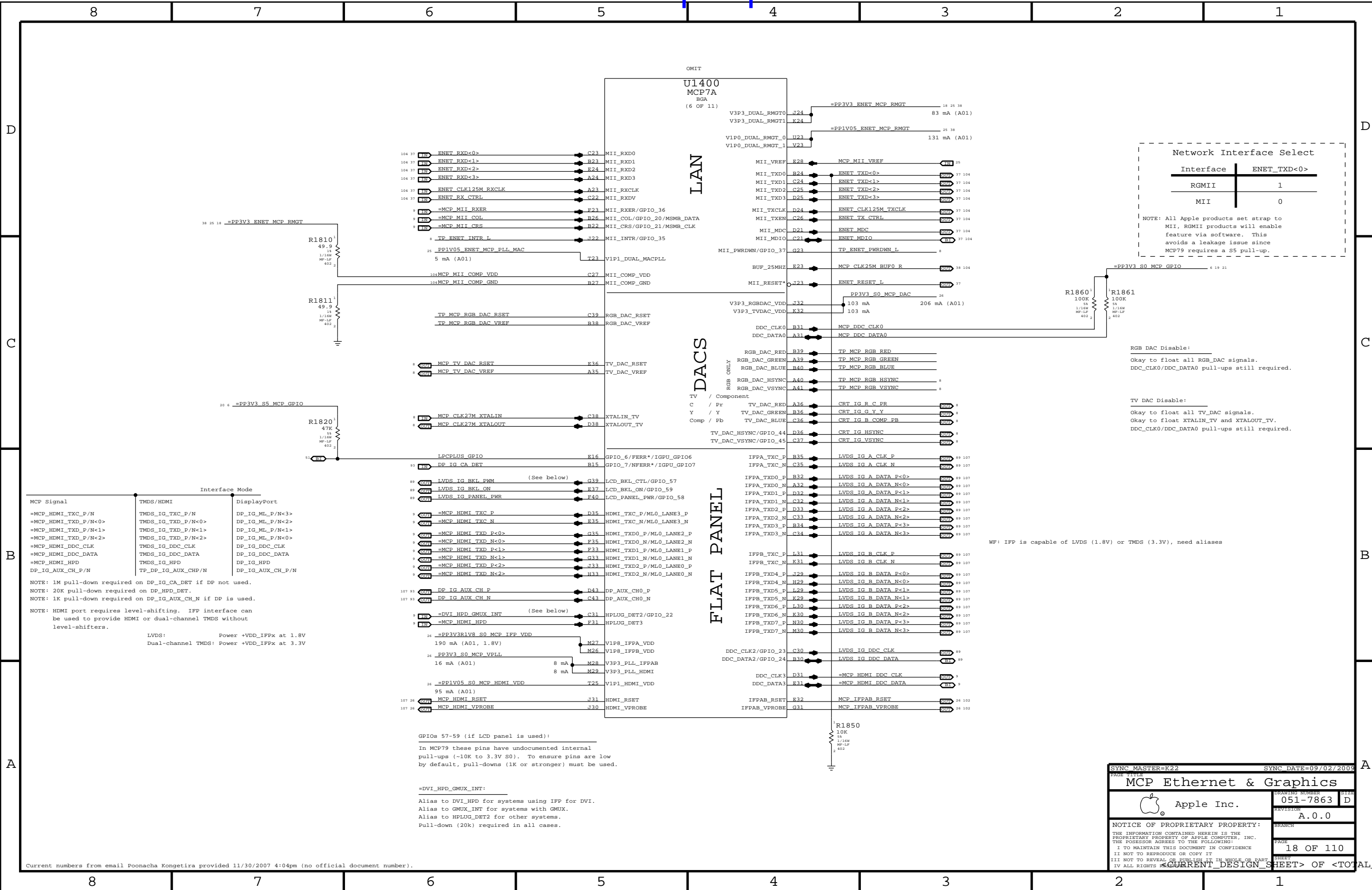
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MCP MEMORY CNTRL & MISC			
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MCP PCIe Interfaces			
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Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
 Okay to float all TV_DAC signals.
 Okay to float XTALIN_TV and XTALOUT_TV.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HPD_DET.
 NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
 Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
 Alias to DVI_HPD for systems using IFP for DVI.
 Alias to GMUX_INT for systems with GMUX.
 Alias to HPLUG_DET2 for other systems.
 Pull-down (20k) required in all cases.

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MCP Ethernet & Graphics

Apple Inc.

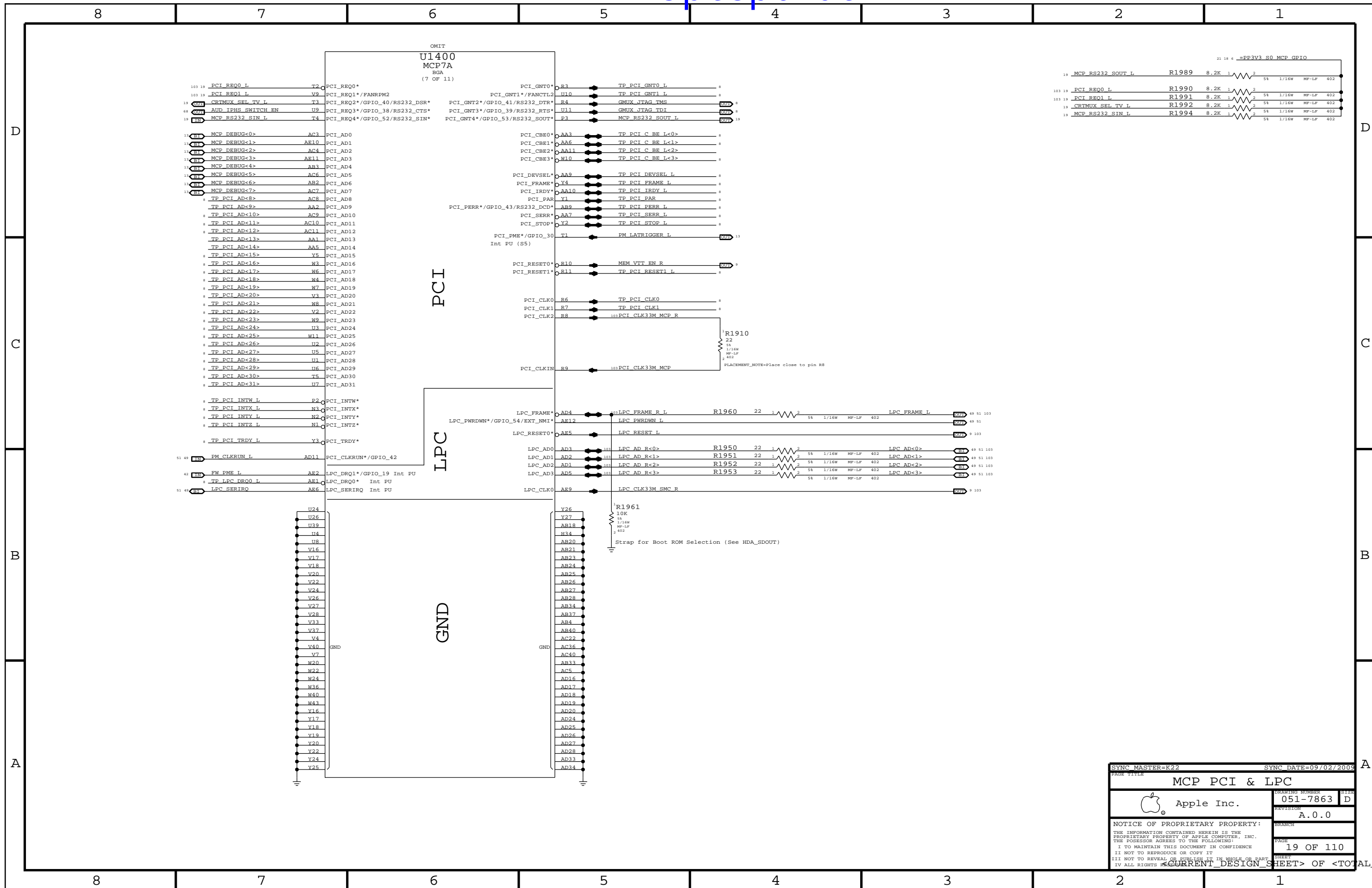
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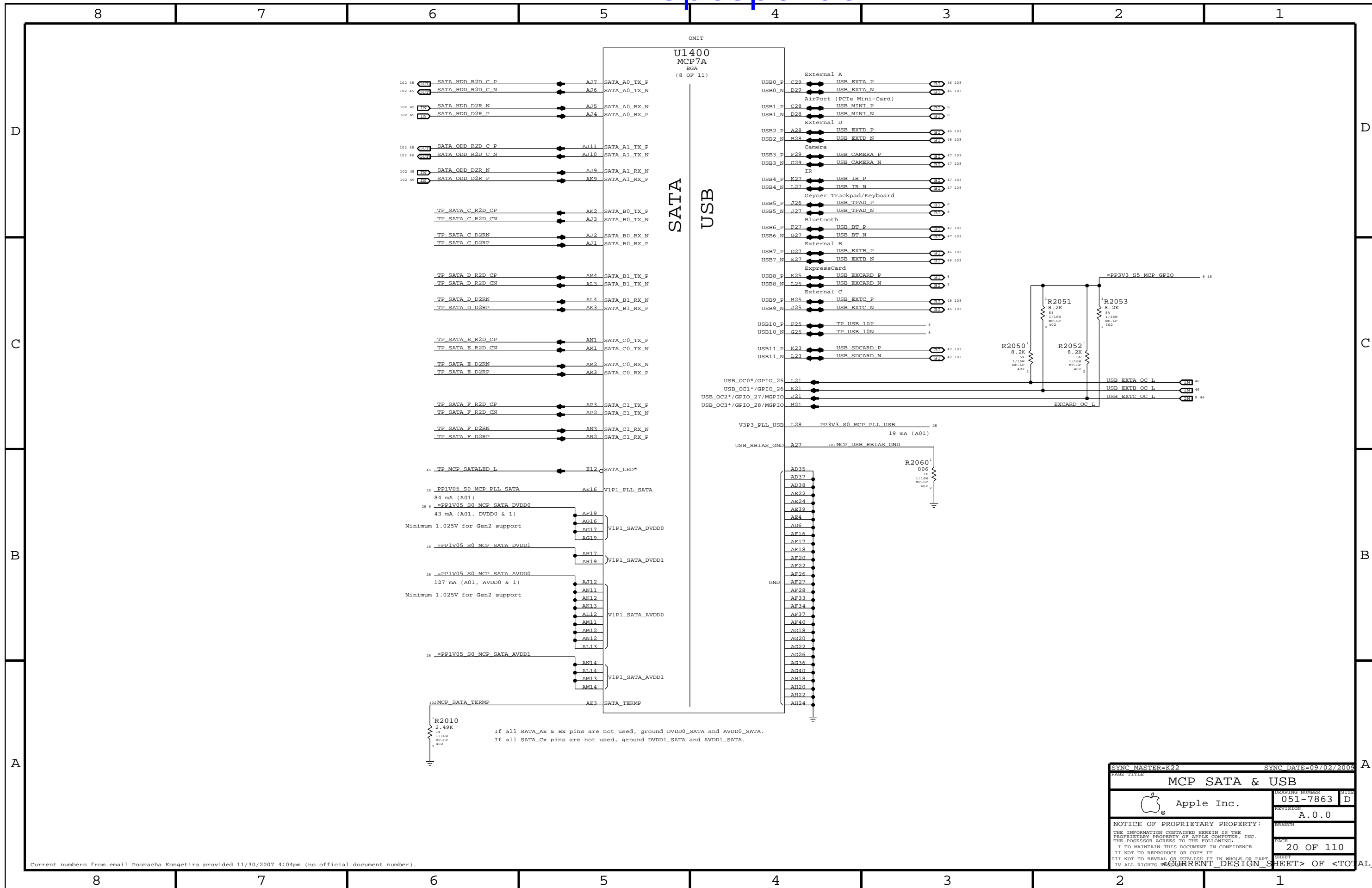
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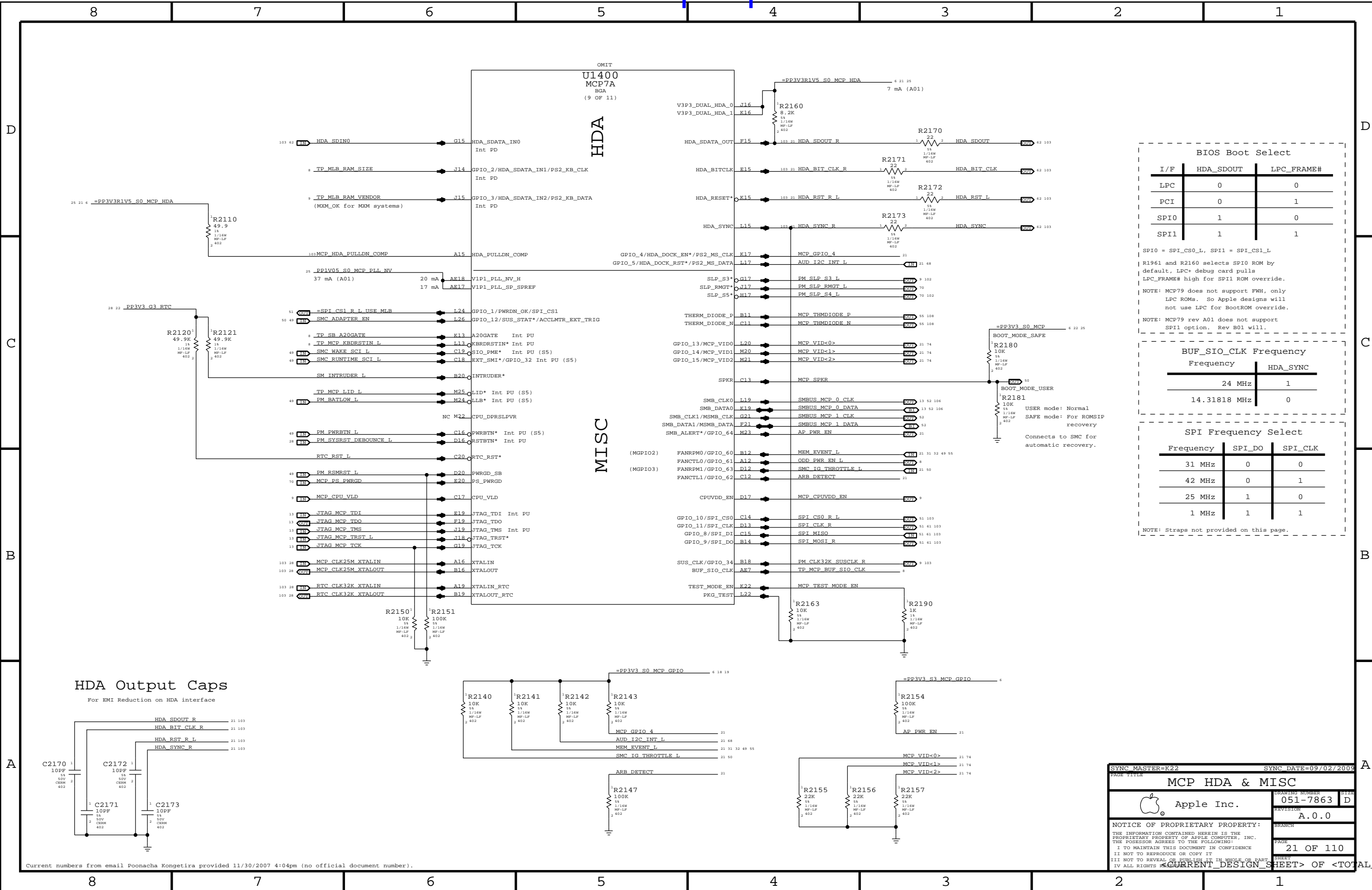
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MCP PCI & LPC			
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MCP SATA & USB			
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		PAGE	20 OF 110



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

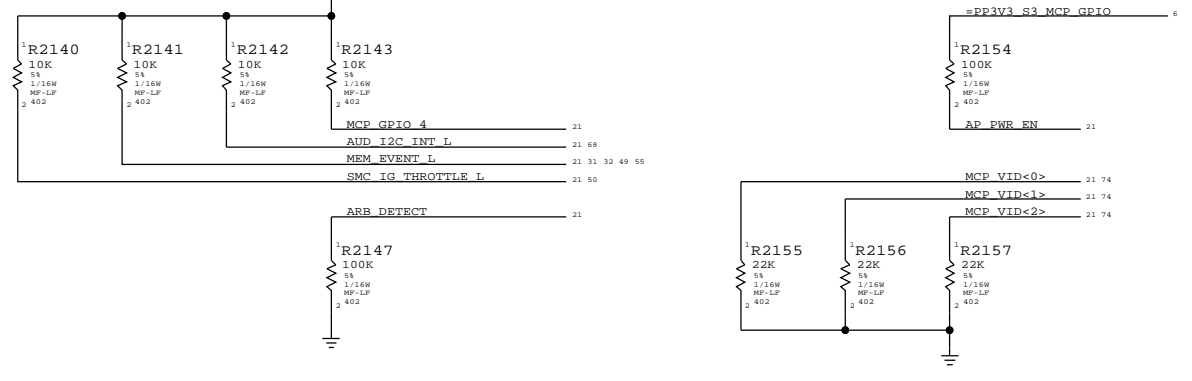
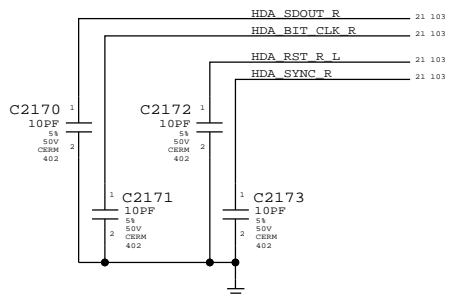
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



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MCP HDA & MISC

Apple Inc.

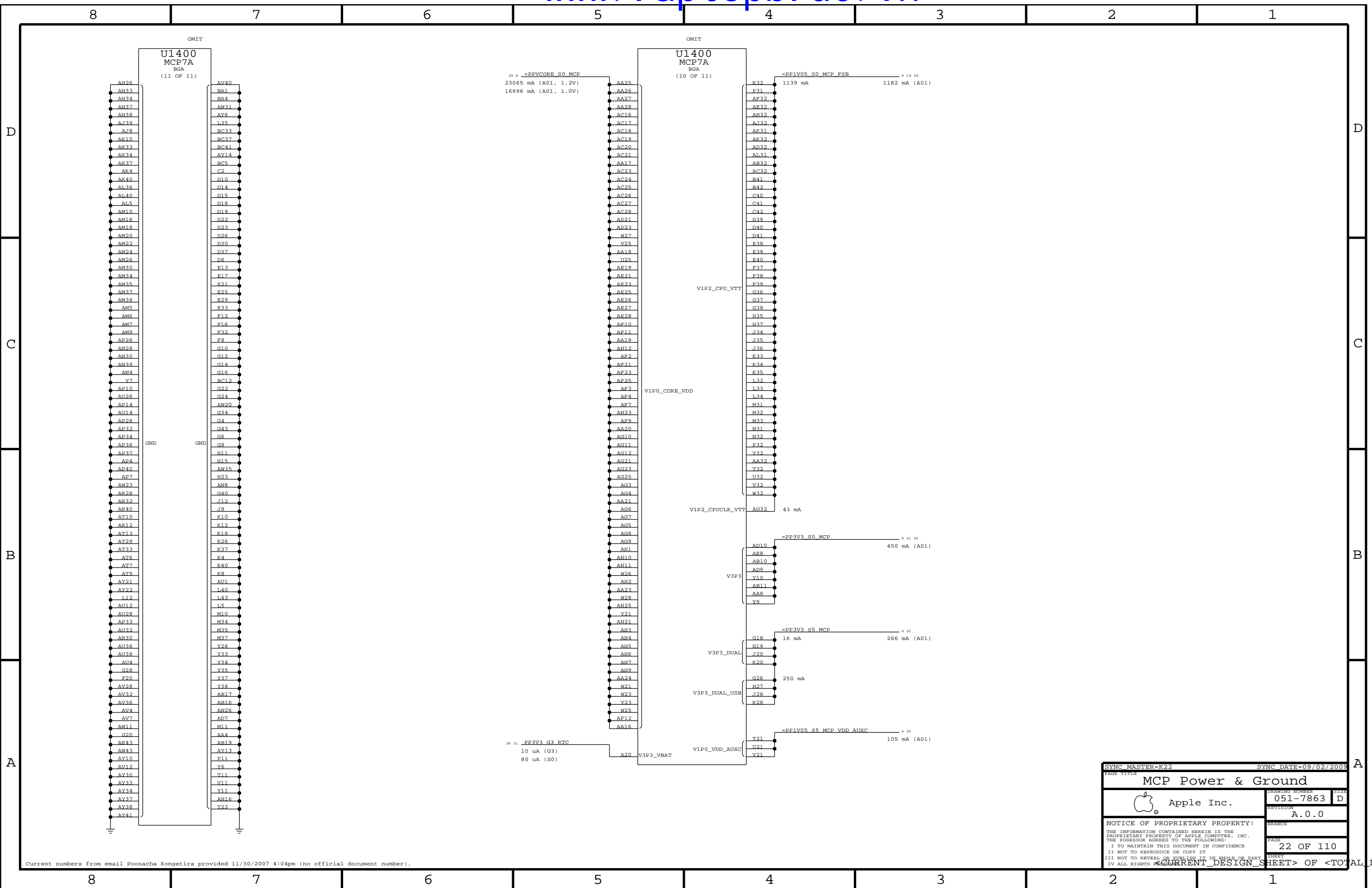
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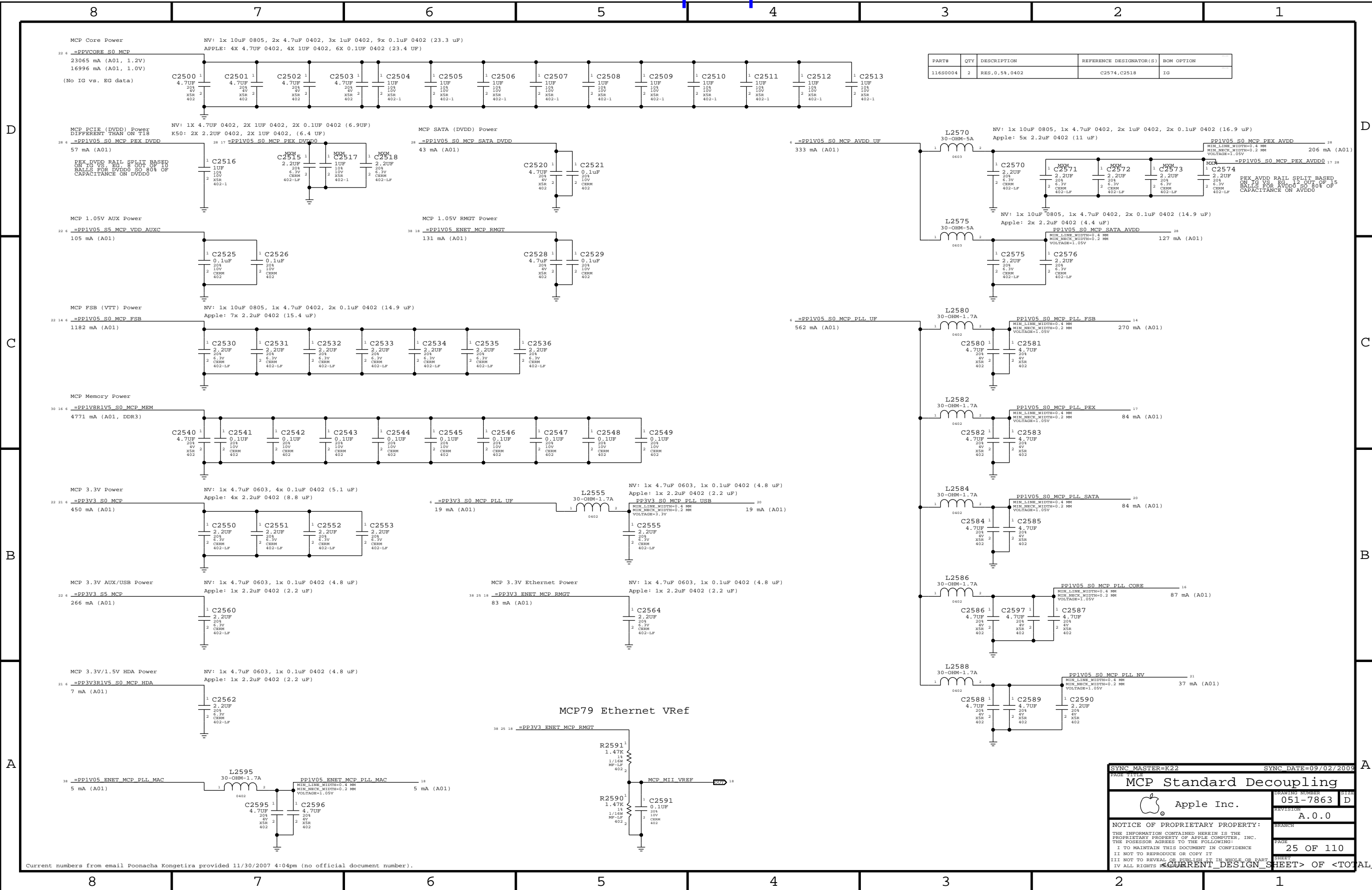
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C									C
B									B
A									A
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C									C
B									B
A									A
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0.5%,0402	C2574,C2518	IG

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MCP Standard Decoupling

Apple Inc.

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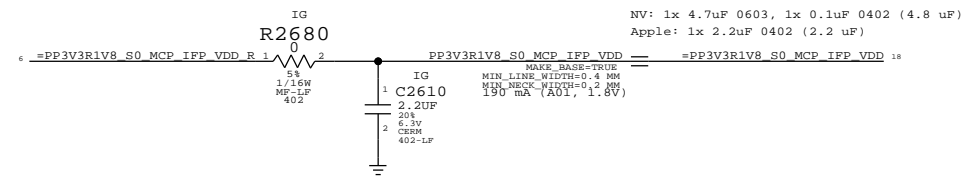
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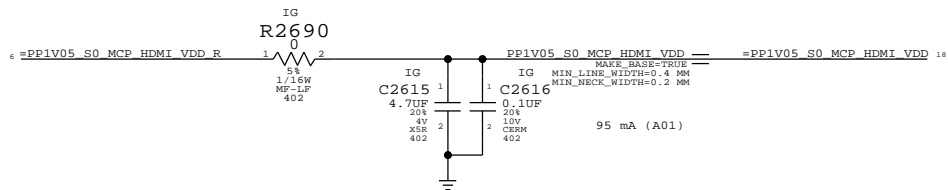
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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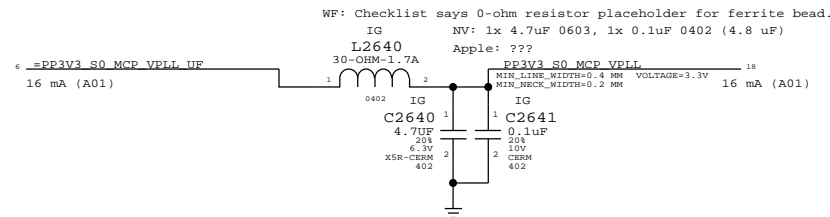
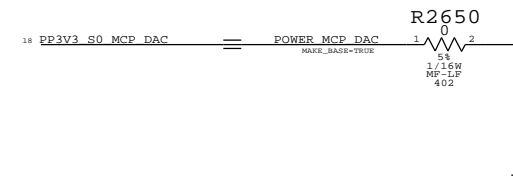
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2616		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2641		MXM

SYNC MASTER=K22 SYNC DATE=09/02/2009

MCP Graphics Support

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051-7863 D

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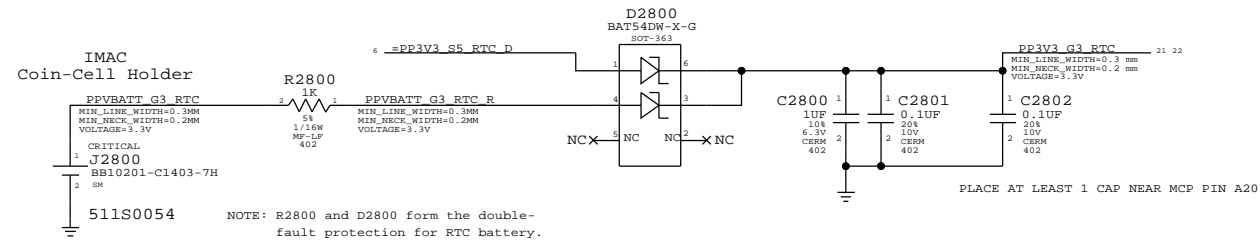
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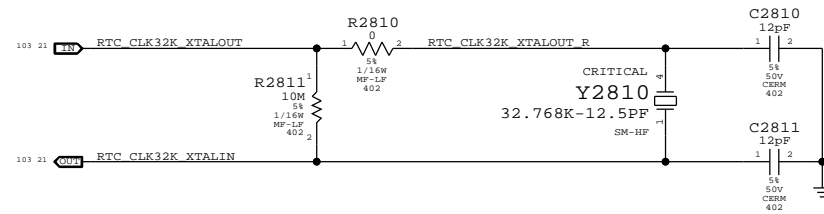
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C									C
B									B
A									A
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SYNC MASTER=K22		SYNC DATE=09/02/2009	
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			PAGE 27 OF 110
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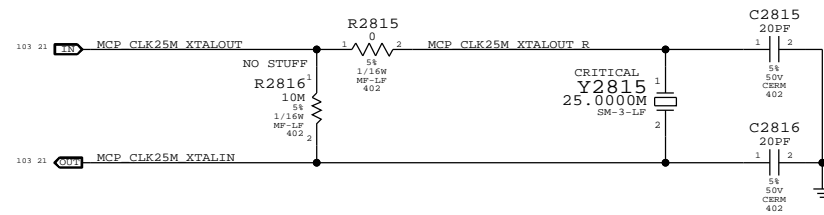
RTC Power Sources



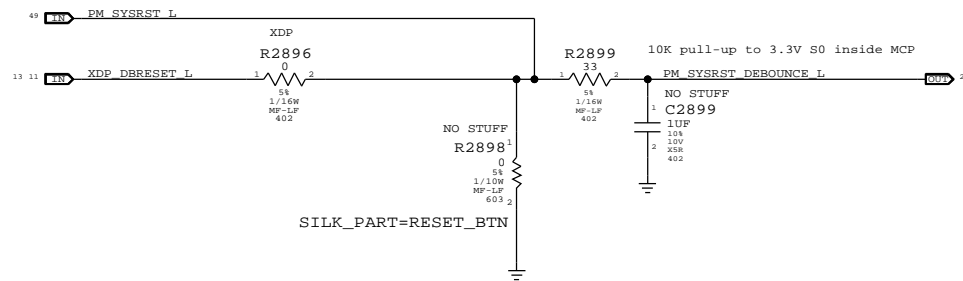
RTC Crystal



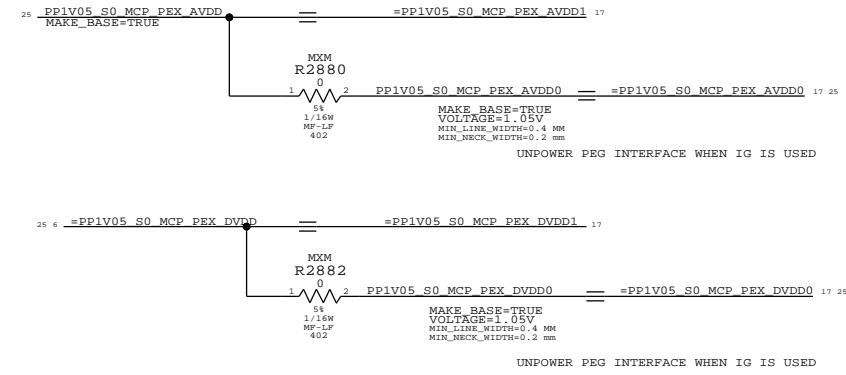
MCP 25MHz Crystal



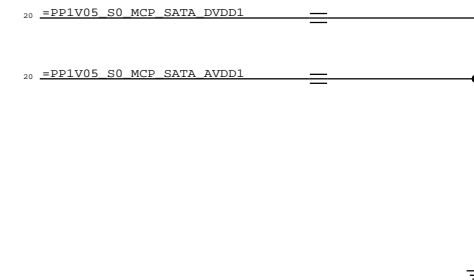
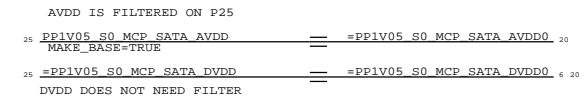
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



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SB Misc			
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CURRENT DESIGN SHEET		PAGE	28 OF 110
SHEET			

Page Notes

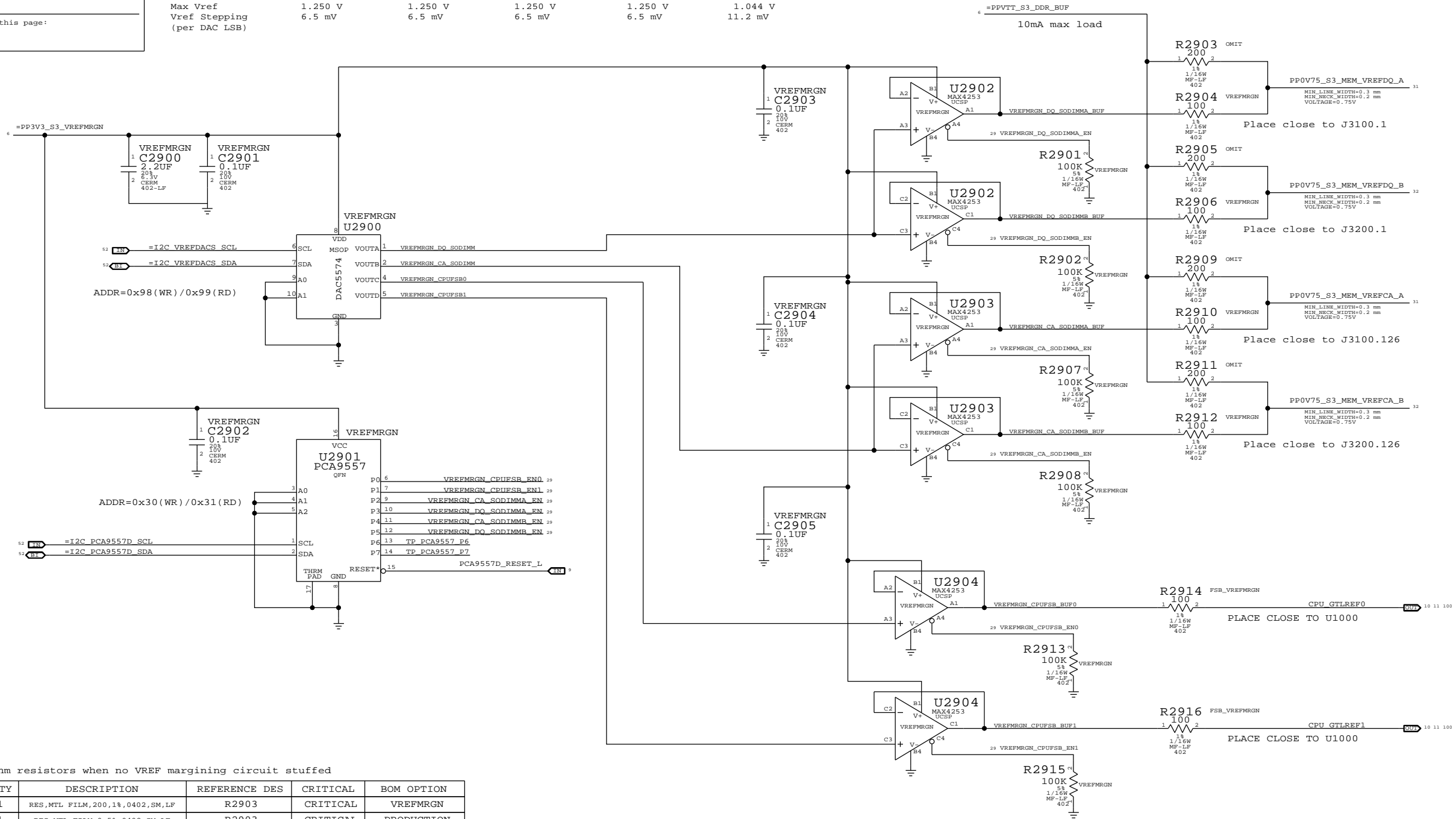
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN
 PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



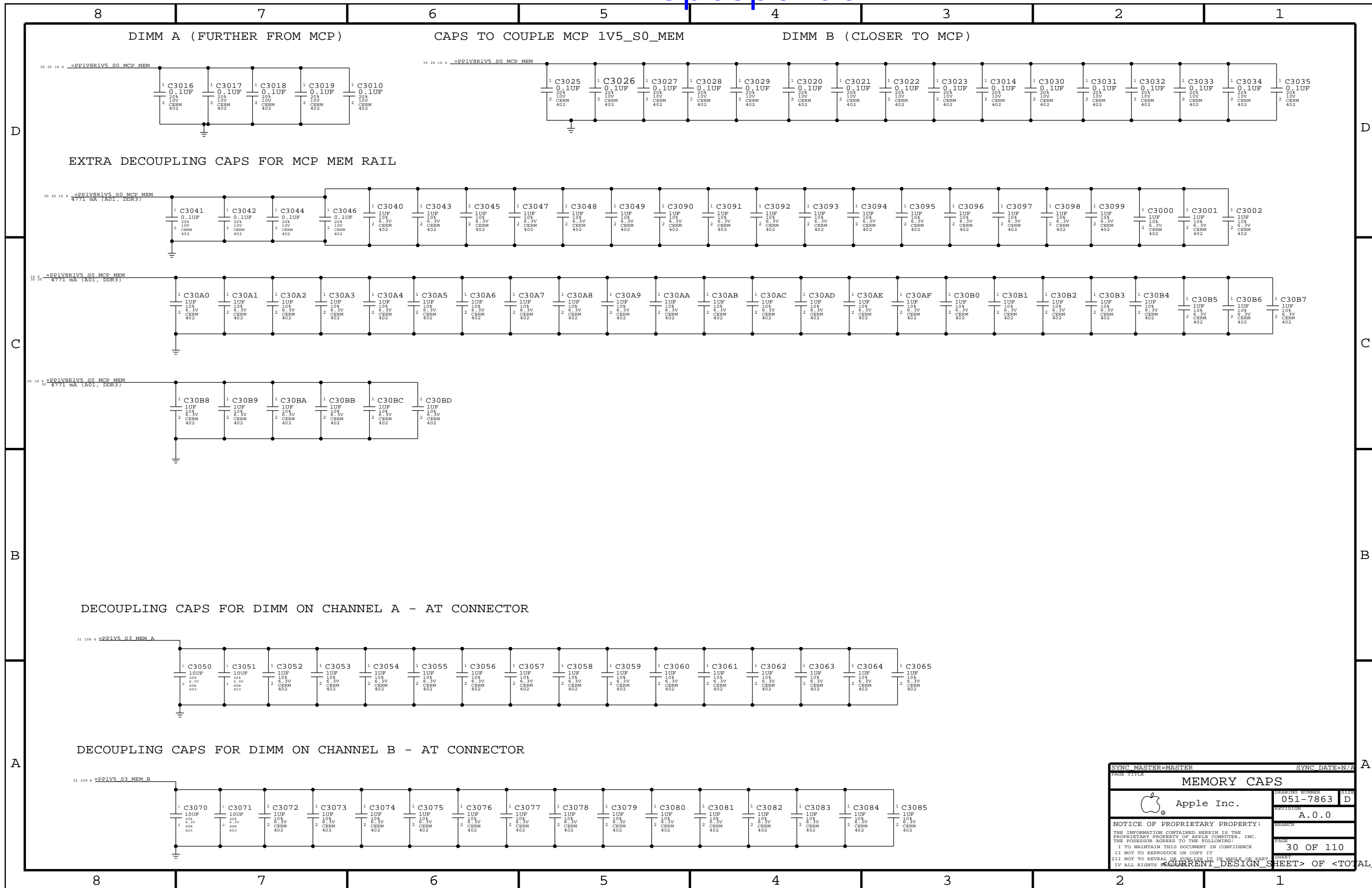
Required zero ohm resistors when no VREF margining circuit stuffed


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

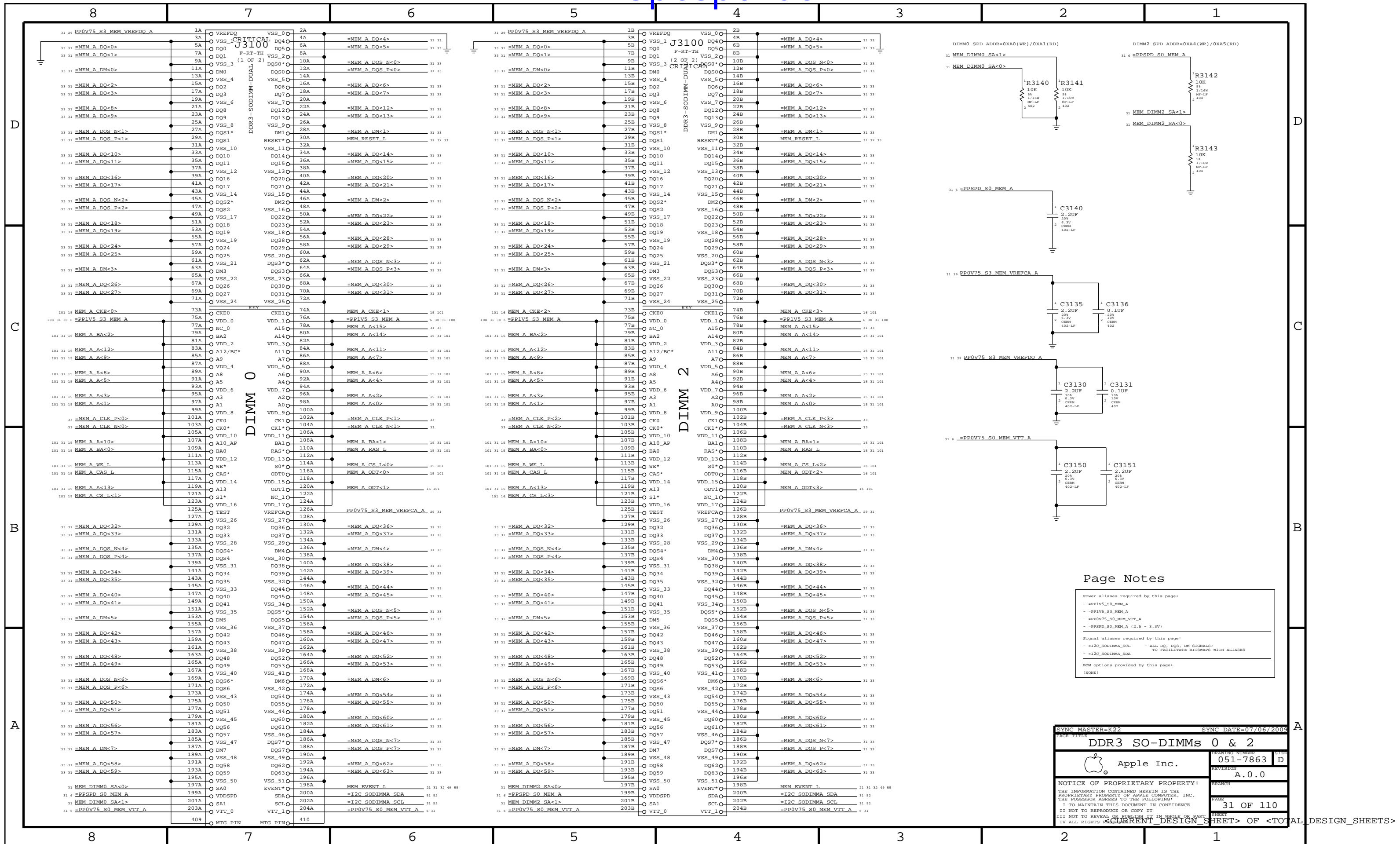
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FSB/DDR3 Vref Margining

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PAGE TITLE			
MEMORY CAPS			
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		BRANCH	
		PAGE 30 OF 110	
		SHEET	
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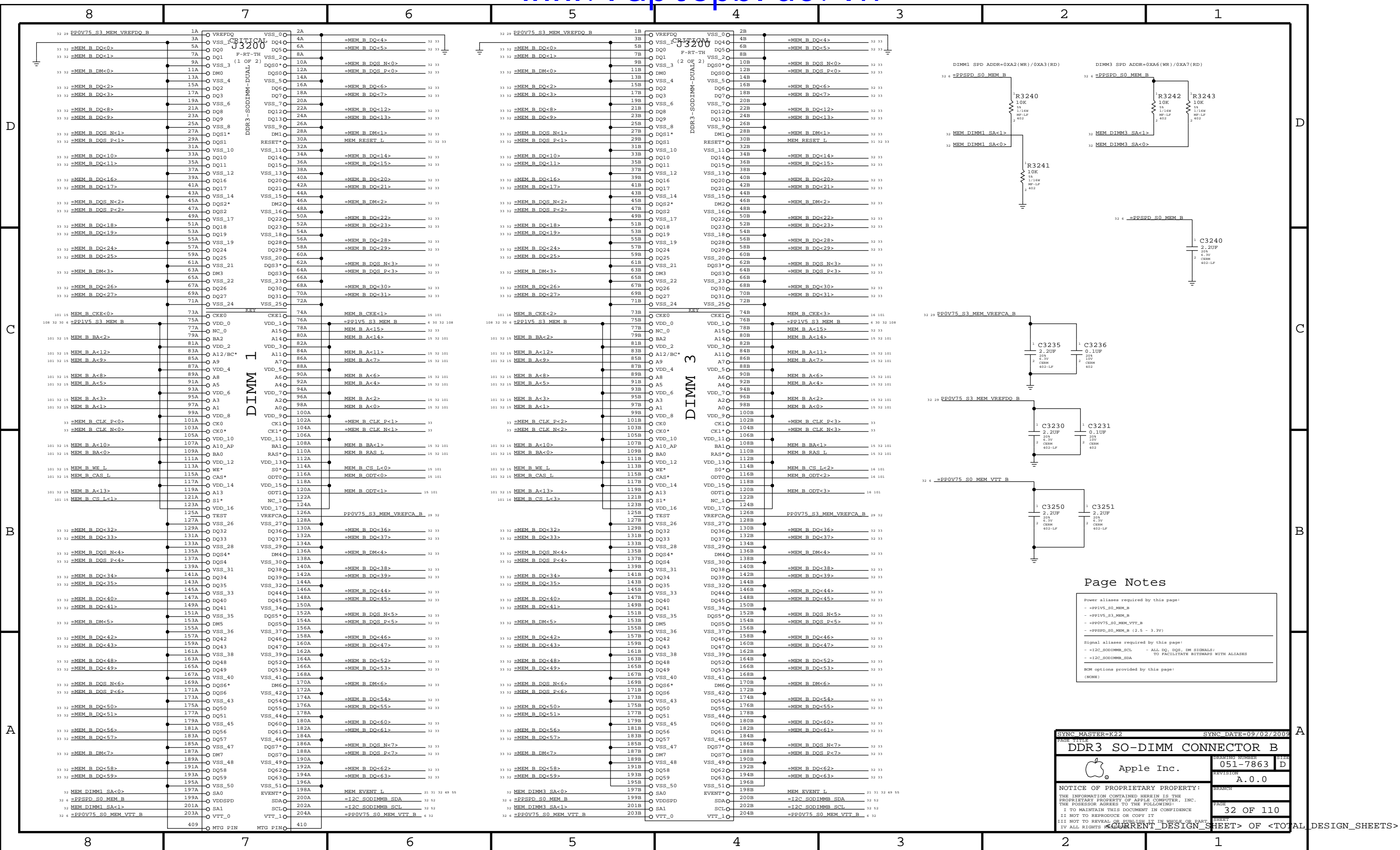
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL - ALL DQ, DQS, DM SIGNALS/ TO FACILITATE BITSTREAMS WITH ALIASES
- =I2C_SODIMMA_SDA

NOM options provided by this page:
(NONE)

SYNC MASTER=K22 SYNC DATE=07/06/2009
DDR3 SO-DIMMs 0 & 2
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31 OF 110
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Page Notes

- Power aliases required by this page:
 - =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)
- Signal aliases required by this page:
 - =I2C_SODIMMB_SCL - ALL DQ, DQS, DM SIGNALS/ TO FACILITATE BITWANGS WITH ALIASES
 - =I2C_SODIMMB_SDA
- NCM options provided by this page:
 - (NONE)

SYNC MASTER=K22 SYNC DATE=09/02/2009

DDR3 SO-DIMM CONNECTOR B

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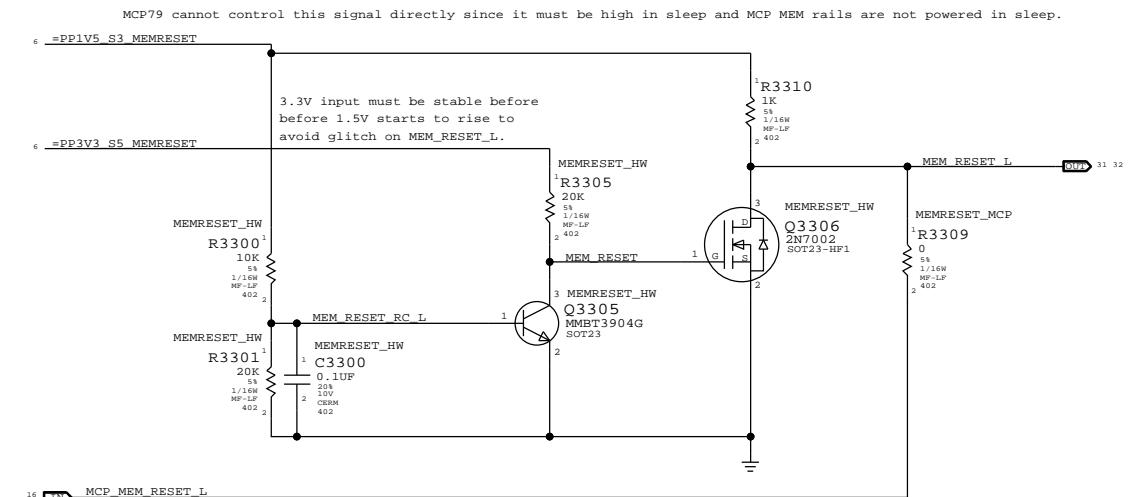
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SHEET

DDR3 RESET Support



MCP MEMORY CLOCK ALIASING

MEM A CLK P<0>	MAKE_BASE=TRUE	MEM A CLK P<0>
MEM A CLK N<0>	MAKE_BASE=TRUE	MEM A CLK N<0>
MEM A CLK P<1>	MAKE_BASE=TRUE	MEM A CLK P<1>
MEM A CLK N<1>	MAKE_BASE=TRUE	MEM A CLK N<1>
MEM A CLK P<2>	MAKE_BASE=TRUE	MEM A CLK P<2>
MEM A CLK N<2>	MAKE_BASE=TRUE	MEM A CLK N<2>
MEM A CLK P<3>	MAKE_BASE=TRUE	MEM A CLK P<3>
MEM A CLK N<3>	MAKE_BASE=TRUE	MEM A CLK N<3>
MEM A CLK P<4>	MAKE_BASE=TRUE	MEM A CLK P<4>
MEM A CLK N<4>	MAKE_BASE=TRUE	MEM A CLK N<4>
MEM B CLK P<0>	MAKE_BASE=TRUE	MEM B CLK P<0>
MEM B CLK N<0>	MAKE_BASE=TRUE	MEM B CLK N<0>
MEM B CLK P<1>	MAKE_BASE=TRUE	MEM B CLK P<1>
MEM B CLK N<1>	MAKE_BASE=TRUE	MEM B CLK N<1>
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MEM B CLK N<2>	MAKE_BASE=TRUE	MEM B CLK N<2>
MEM B CLK P<3>	MAKE_BASE=TRUE	MEM B CLK P<3>
MEM B CLK N<3>	MAKE_BASE=TRUE	MEM B CLK N<3>
MEM B CLK P<4>	MAKE_BASE=TRUE	MEM B CLK P<4>
MEM B CLK N<4>	MAKE_BASE=TRUE	MEM B CLK N<4>

MCP MEMORY TEST POINT ALIASING

TP MEM A A<15>	MAKE_BASE=TRUE	MEM A A<15>
TP MEM B A<15>	MAKE_BASE=TRUE	MEM B A<15>

SYNC MASTER=MASTER SYNC DATE=N/A

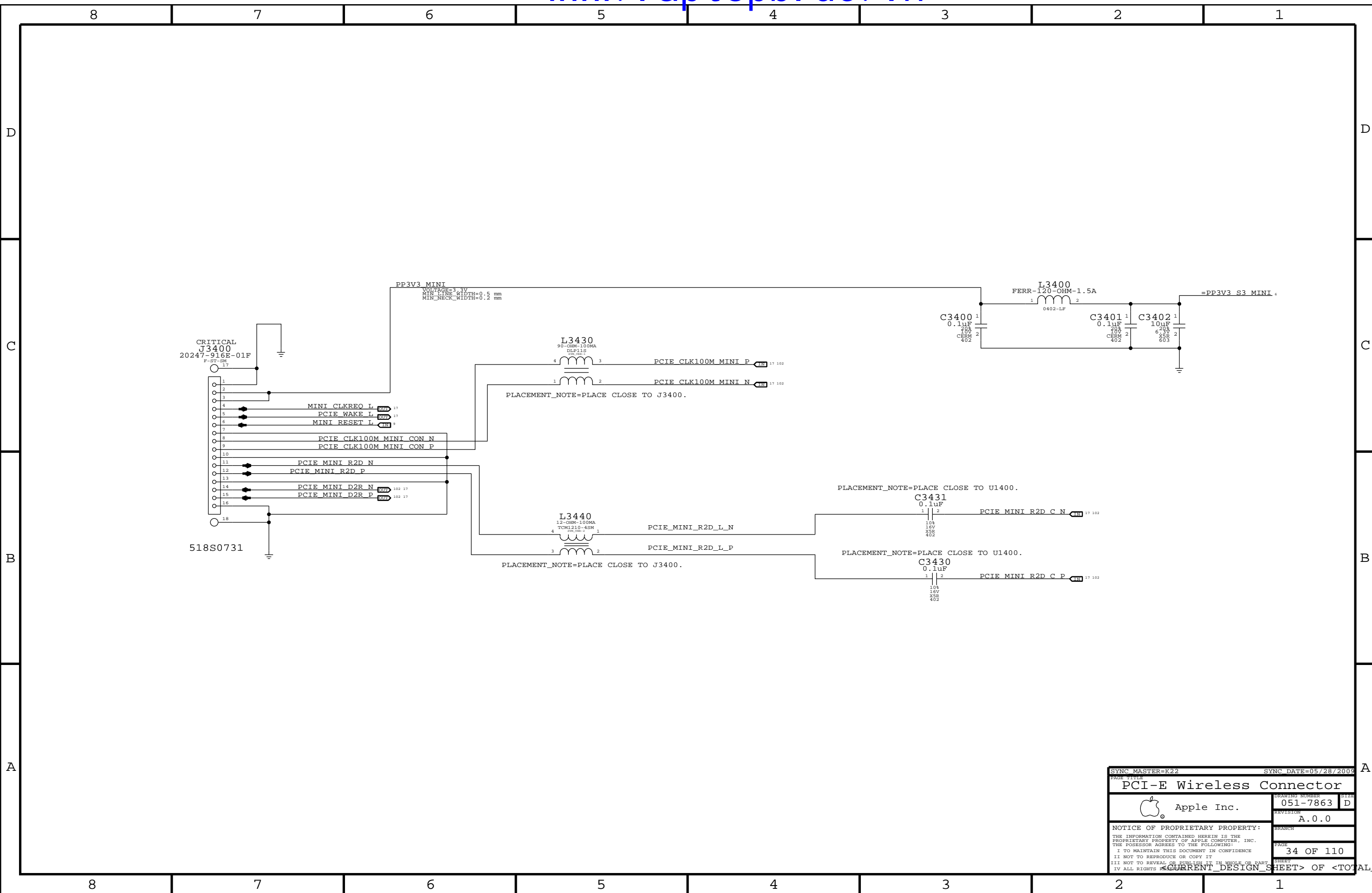
DDR3 SUPPORT AND BITSWAPS

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PAGE: 33 OF 110
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8	7	6	5	4	3	2	1
MCP CHANNEL A DQS 0 -> DIMM A DQS 0	MCP CHANNEL A DQS 1 -> DIMM A DQS 1	MCP CHANNEL A DQS 2 -> DIMM A DQS 2	MCP CHANNEL A DQS 3 -> DIMM A DQS 3	MCP CHANNEL A DQS 4 -> DIMM A DQS 4	MCP CHANNEL A DQS 5 -> DIMM A DQS 5	MCP CHANNEL A DQS 6 -> DIMM A DQS 6	MCP CHANNEL A DQS 7 -> DIMM A DQS 7
MCP CHANNEL B DQS 0 -> DIMM B DQS 0	MCP CHANNEL B DQS 1 -> DIMM B DQS 1	MCP CHANNEL B DQS 2 -> DIMM B DQS 2	MCP CHANNEL B DQS 3 -> DIMM B DQS 3	MCP CHANNEL B DQS 4 -> DIMM B DQS 4	MCP CHANNEL B DQS 5 -> DIMM B DQS 5	MCP CHANNEL B DQS 6 -> DIMM B DQS 6	MCP CHANNEL B DQS 7 -> DIMM B DQS 7
MCP CHANNEL A DQS 8 -> DIMM A DQS 8	MCP CHANNEL A DQS 9 -> DIMM A DQS 9	MCP CHANNEL A DQS 10 -> DIMM A DQS 10	MCP CHANNEL A DQS 11 -> DIMM A DQS 11	MCP CHANNEL A DQS 12 -> DIMM A DQS 12	MCP CHANNEL A DQS 13 -> DIMM A DQS 13	MCP CHANNEL A DQS 14 -> DIMM A DQS 14	MCP CHANNEL A DQS 15 -> DIMM A DQS 15
MCP CHANNEL B DQS 8 -> DIMM B DQS 8	MCP CHANNEL B DQS 9 -> DIMM B DQS 9	MCP CHANNEL B DQS 10 -> DIMM B DQS 10	MCP CHANNEL B DQS 11 -> DIMM B DQS 11	MCP CHANNEL B DQS 12 -> DIMM B DQS 12	MCP CHANNEL B DQS 13 -> DIMM B DQS 13	MCP CHANNEL B DQS 14 -> DIMM B DQS 14	MCP CHANNEL B DQS 15 -> DIMM B DQS 15




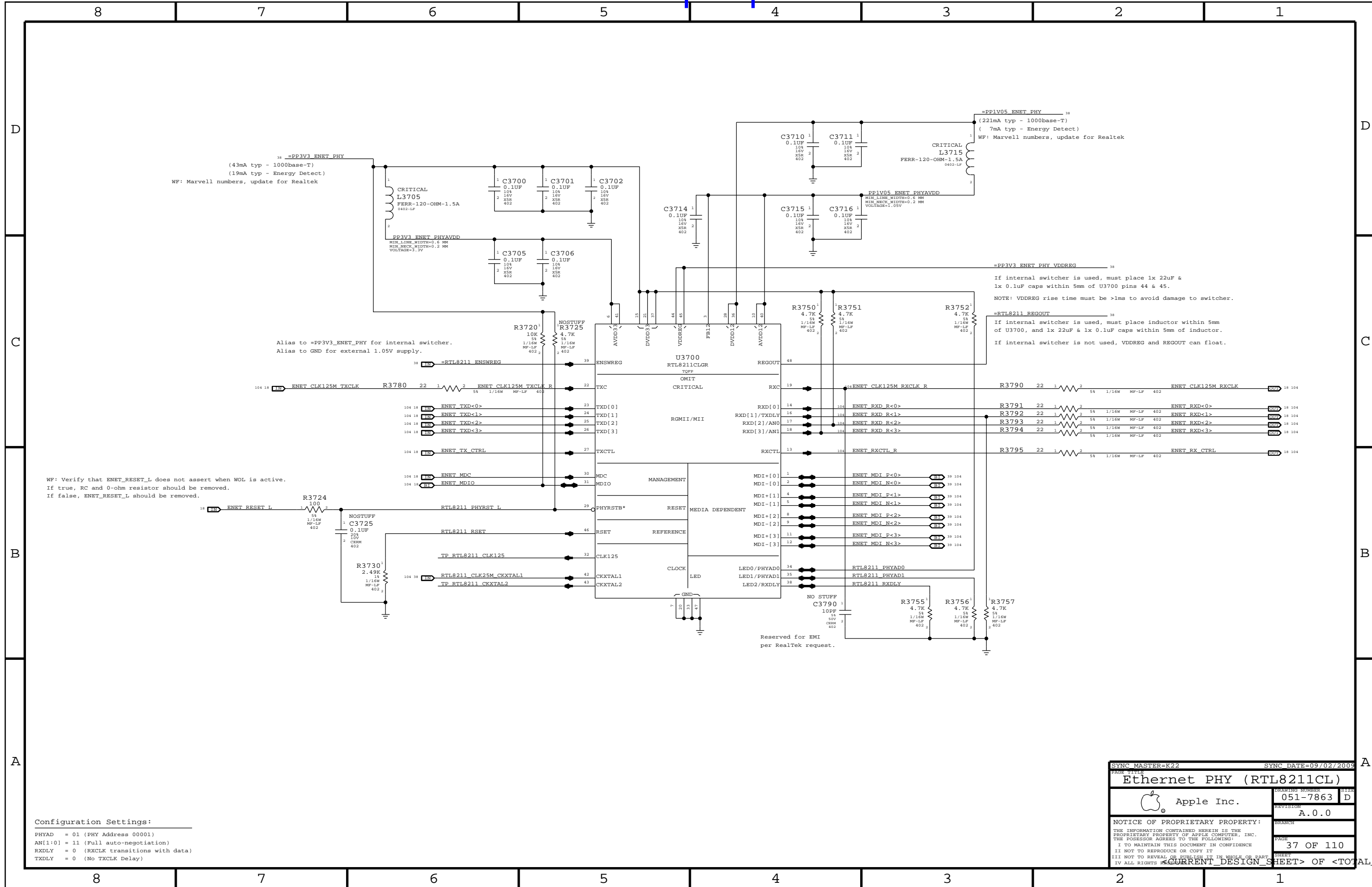
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		PAGE 34 OF 110	SHEET
		SHEET <CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>	

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		SHEET 35 OF 110	

	8	7	6	5	4	3	2	1	
D									D
C									C
B									B
A									A
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PP3V3_ENET_PHY (43mA typ - 1000base-T) (19mA typ - Energy Detect) WF: Marvell numbers, update for Realtek

PP1V05_ENET_PHY (221mA typ - 1000base-T) (7mA typ - Energy Detect) WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher. Alias to GND for external 1.05V supply.

PP3V3_ENET_PHY_VDDREG If internal switcher is used, must place 1x 22uF & 1x 0.1uF caps within 5mm of U3700 pins 44 & 45. NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

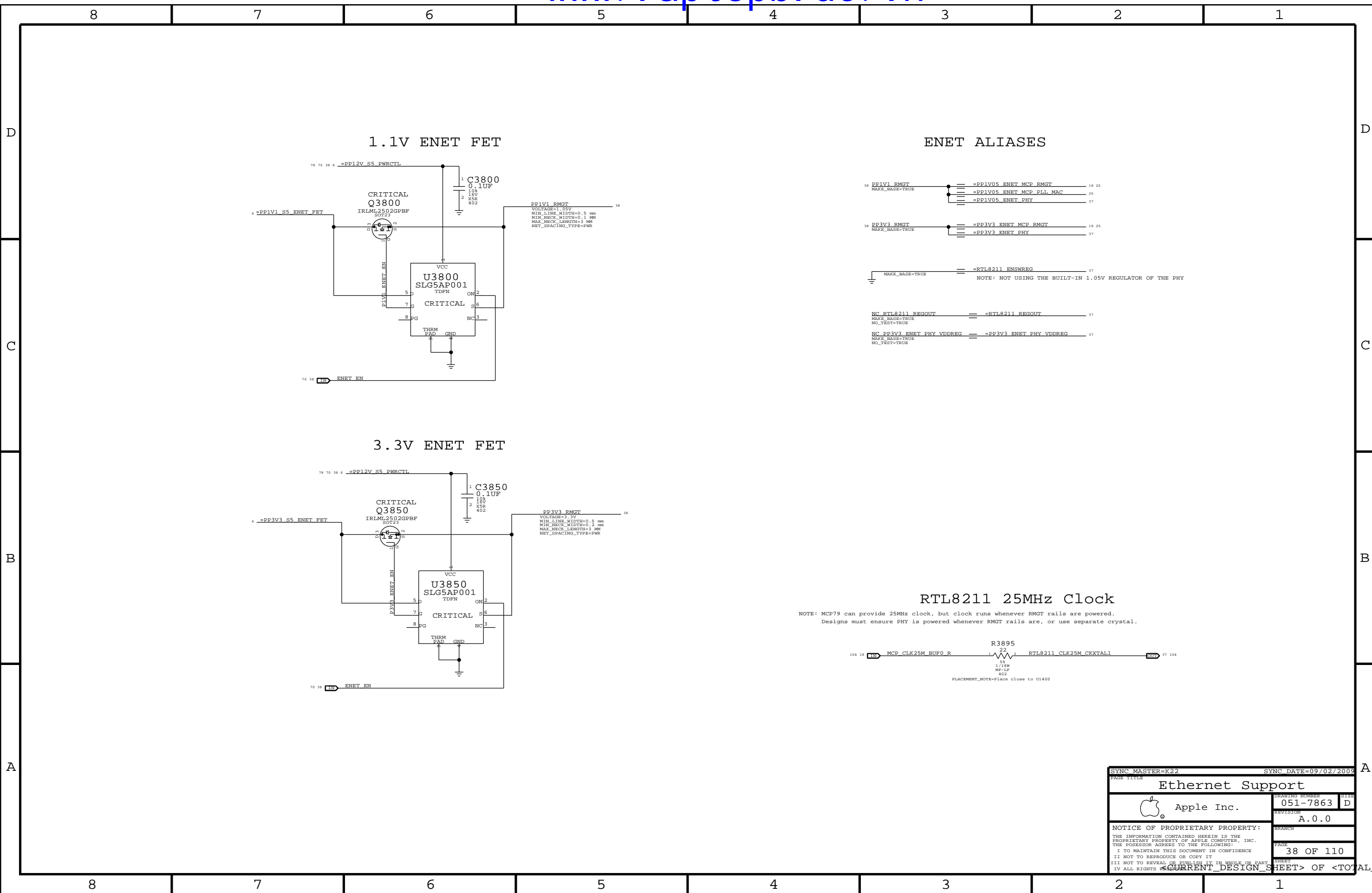
RTL8211_REGOUT If internal switcher is used, must place inductor within 5mm of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor. If internal switcher is not used, VDDREG and REGOUT can float.


WF: Verify that ENET_RESET_L does not assert when WOL is active. If true, RC and 0-ohm resistor should be removed. If false, ENET_RESET_L should be removed.

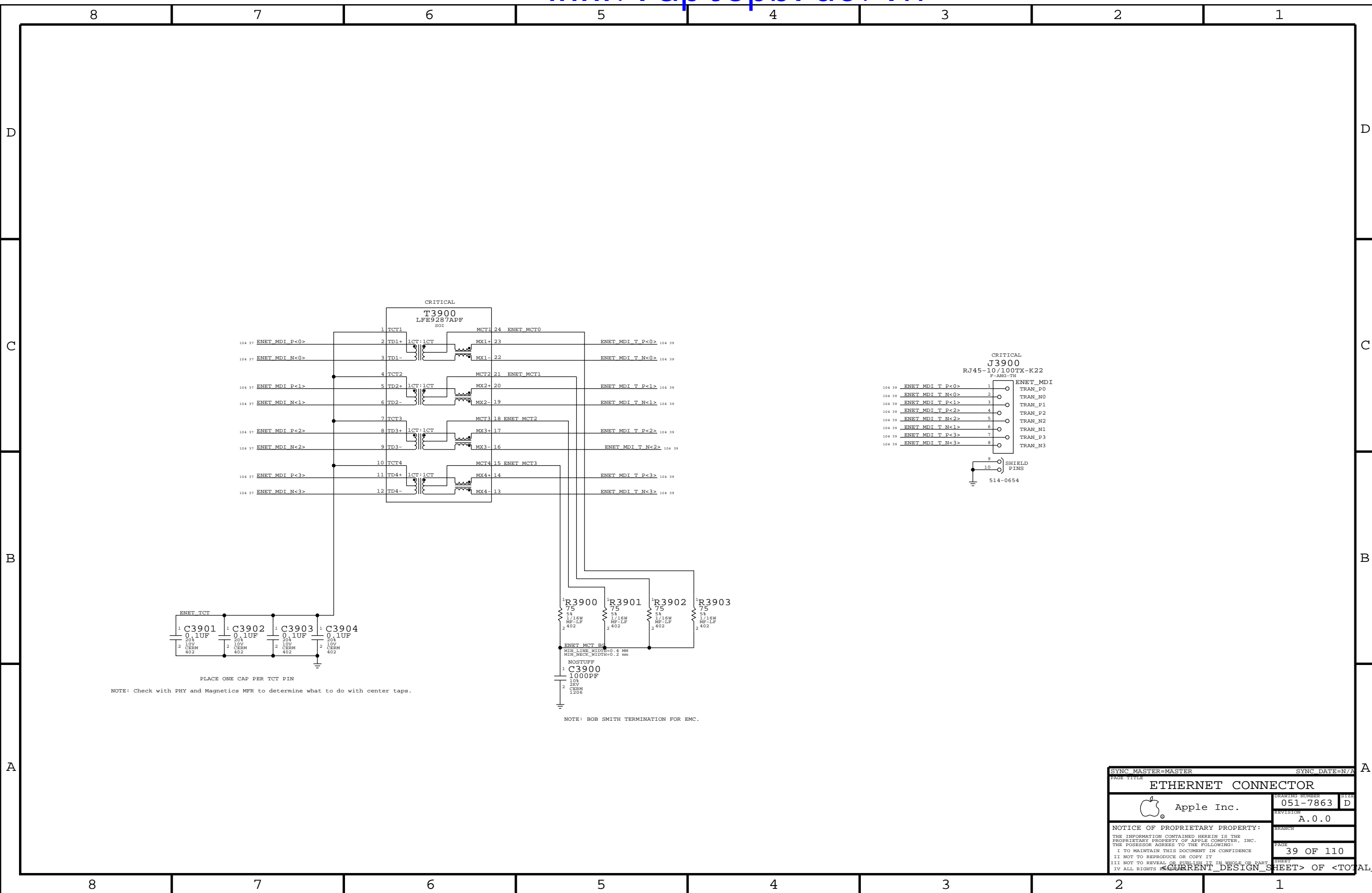
Reserved for EMI per RealTek request.

Configuration Settings: PHYAD = 01 (PHY Address 00001) AN[1:0] = 11 (Full auto-negotiation) RXDLY = 0 (RXCLK transitions with data) TXDLY = 0 (No TXCLK Delay)

Metadata block containing: SYNC MASTER=K22, SYNC DATE=09/02/2009, Ethernet PHY (RTL8211CL), Apple Inc. logo, drawing number 051-7863, revision A.0.0, and a notice of proprietary property. It also includes a page number 37 OF 110 and a sheet number CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS.




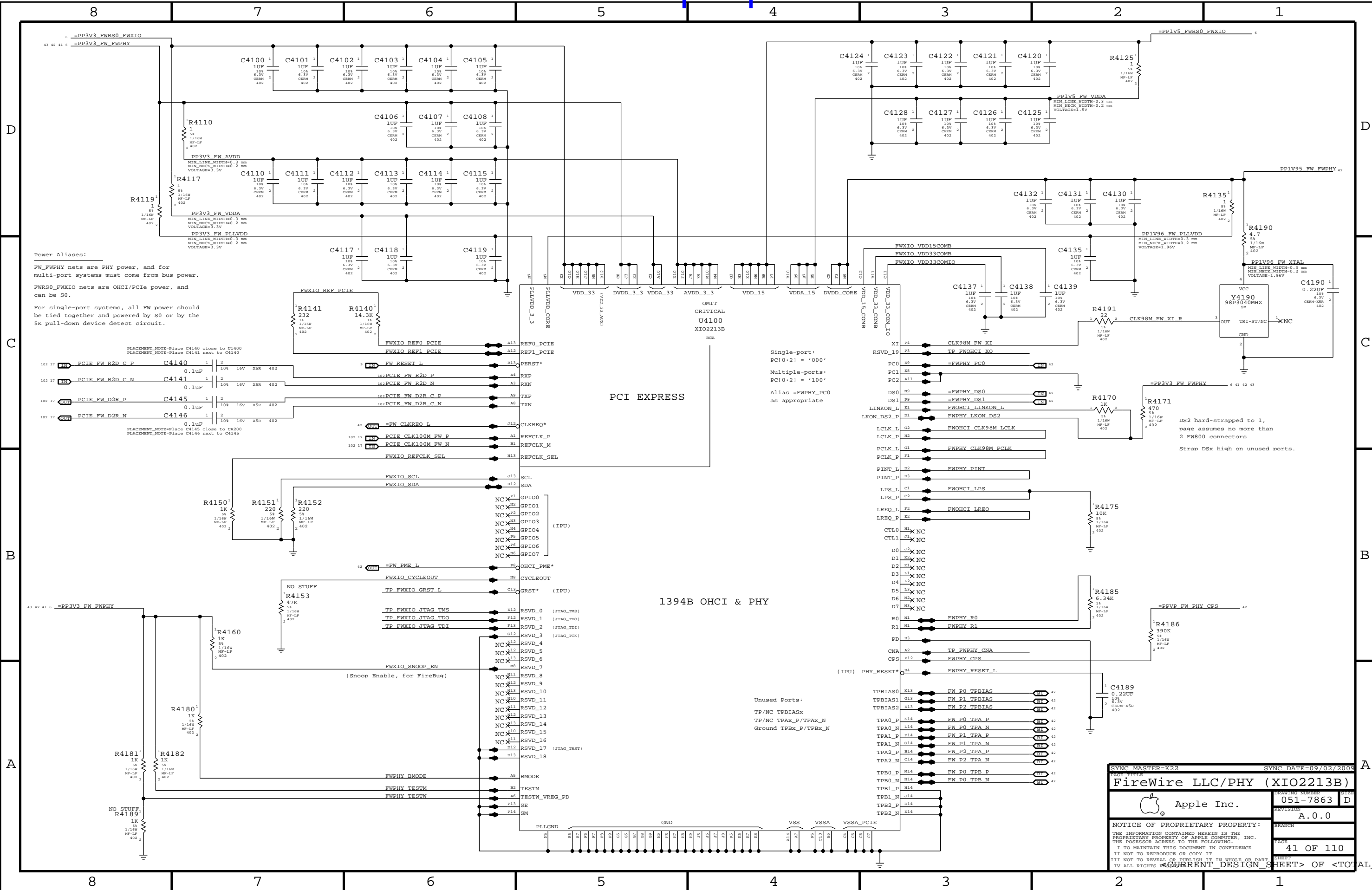
SYNC MASTER=K22		SYNC DATE=09/02/2009	
Ethernet Support			
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PAGE TITLE ETHERNET CONNECTOR			
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CURRENT DESIGN SHEET		SHEET OF <TOTAL DESIGN SHEETS>	

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D									D
C									C
B									B
A									A
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			PAGE 40 OF 110
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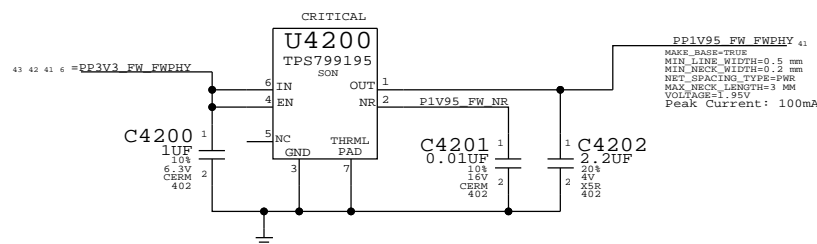
Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWKIO nets are OHCI/PCIE power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0 as appropriate

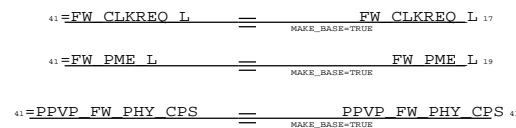
DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors.
Strap DSx high on unused ports.

SYNC MASTER=K22 SYNC DATE=09/02/2009
PAGE TITLE
FireWire LLC/PHY (XIO2213B)
Apple Inc.
DRAWING NUMBER 051-7863 D
REVISION A.0.0
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PAGE 41 OF 110
SHEET
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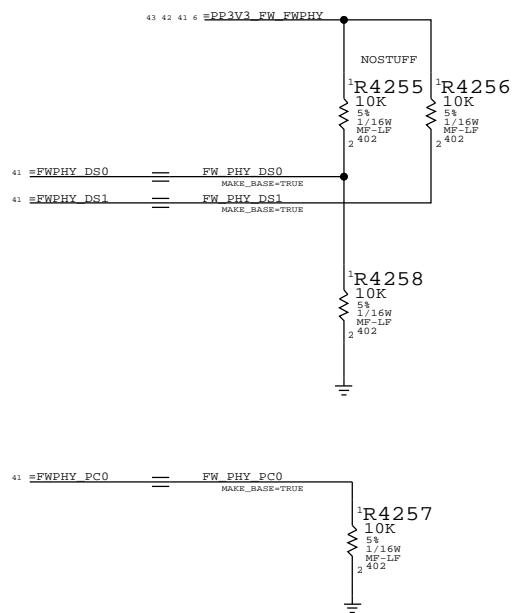
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity

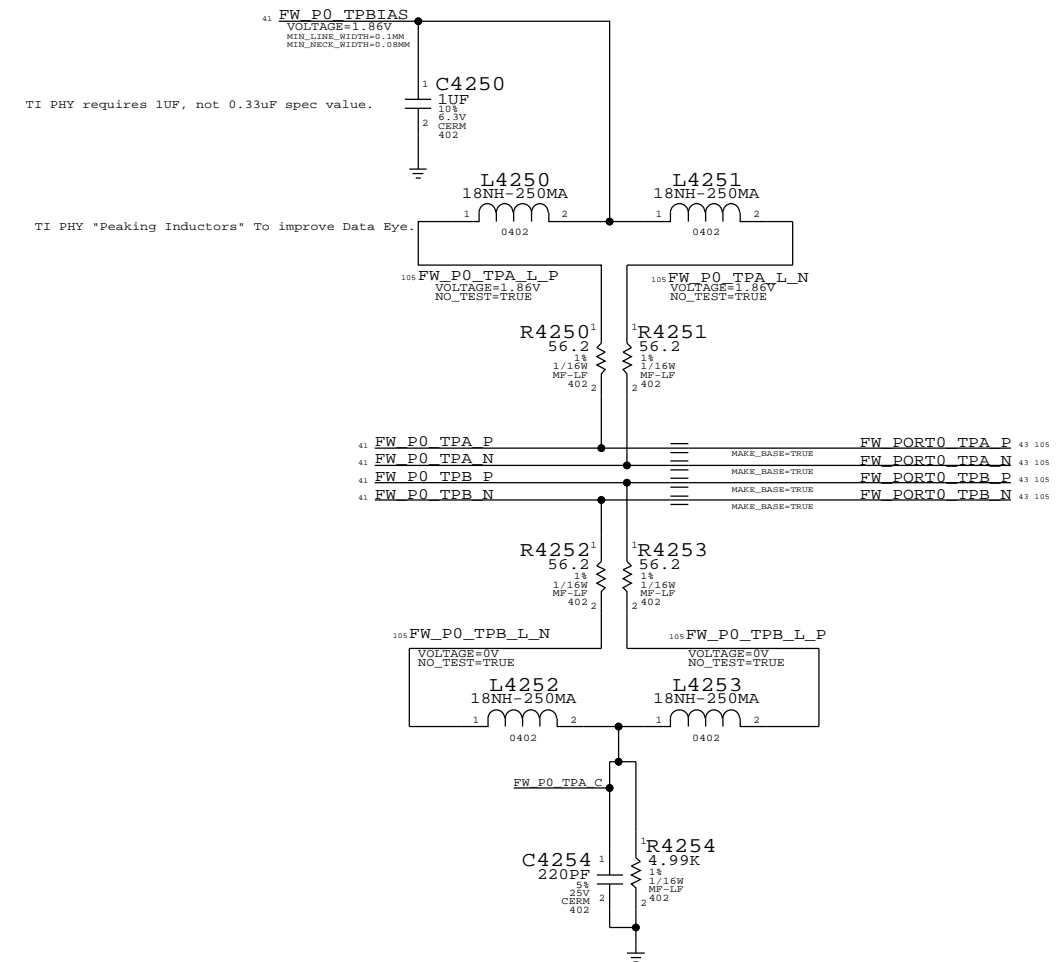


1394 PHY STRAPPING OPTIONS

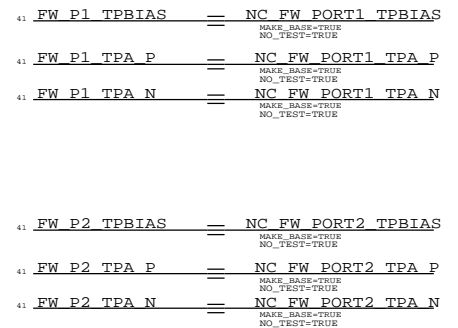


Termination

Place close to FireWire PHY




2ND & 3RD TPA/TPB PAIR UNUSED

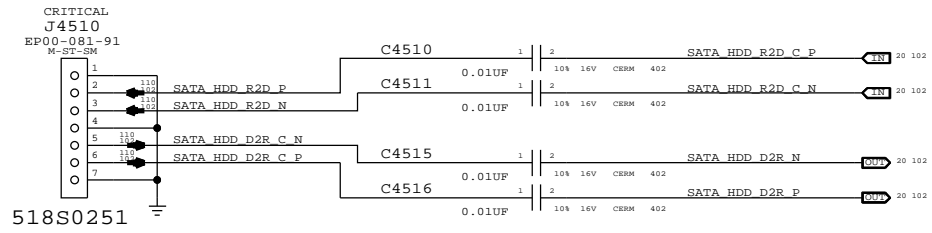


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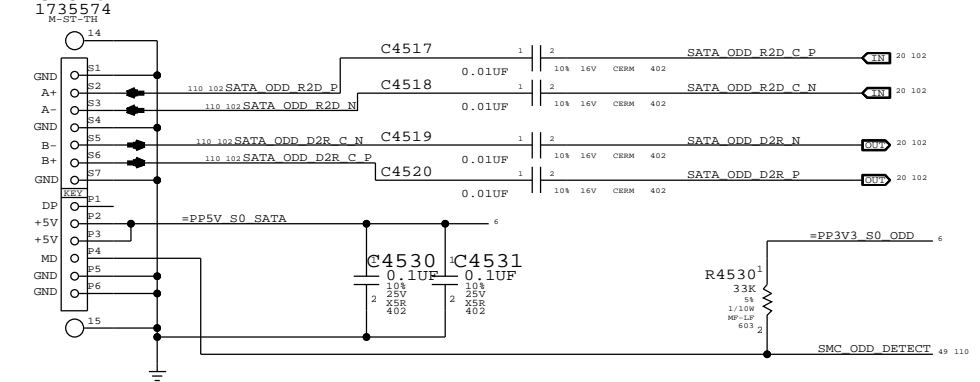
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			PAGE 44 OF 110
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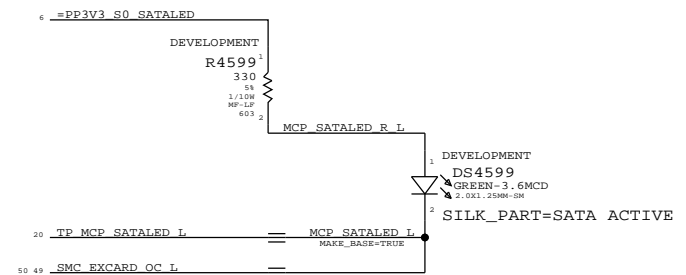
SATA PORT A0 FOR HDD




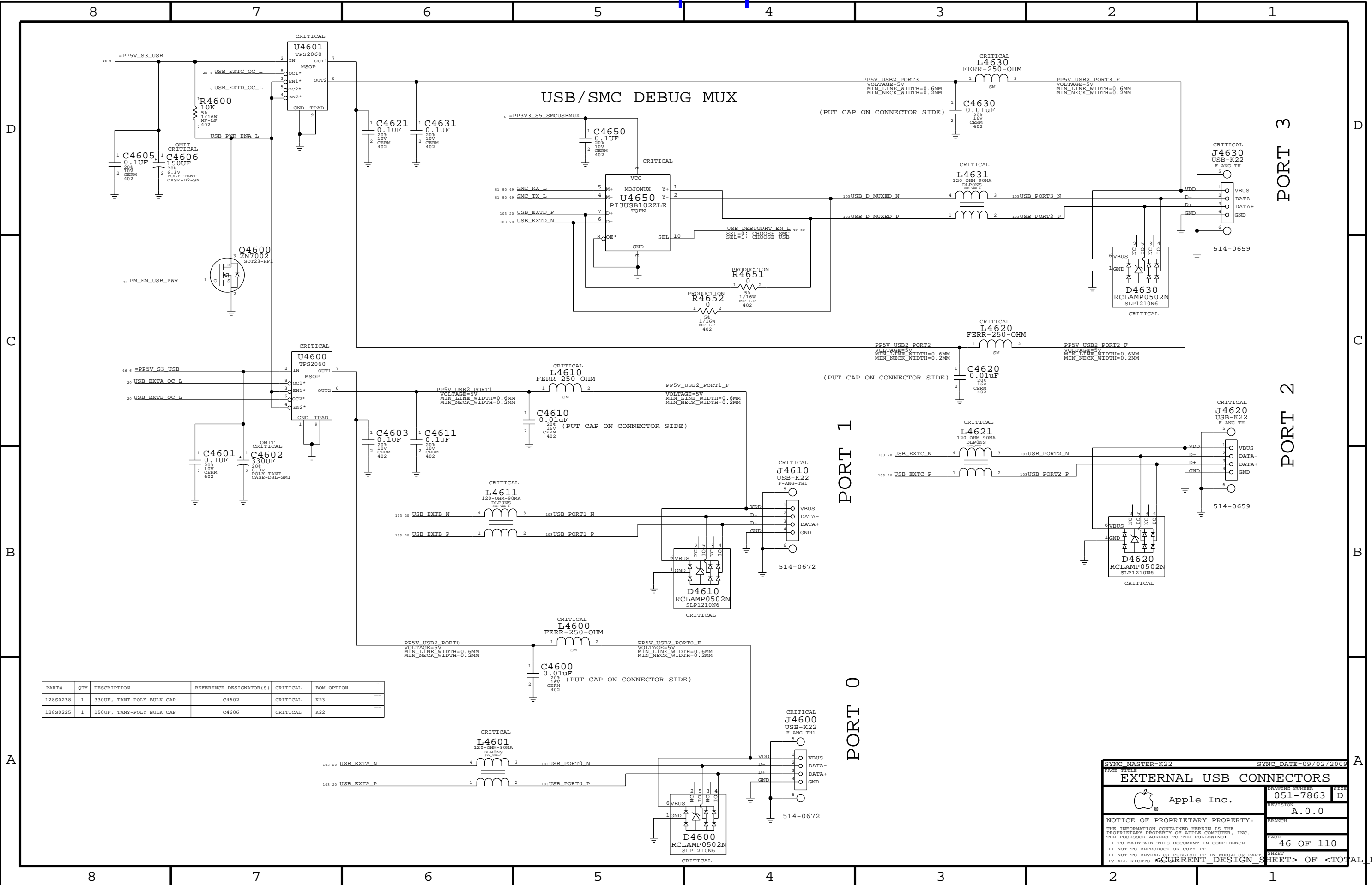
SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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SATA Connectors			
 Apple Inc.		DRAWING NUMBER	051-7863 D
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		PAGE	45 OF 110
		SHEET	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0238	1	330UF, TANT-POLY BULK CAP	C4602	CRITICAL	K23
128S0225	1	150UF, TANT-POLY BULK CAP	C4606	CRITICAL	K22

SYNC MASTER=K22 SYNC DATE=09/02/2009

EXTERNAL USB CONNECTORS

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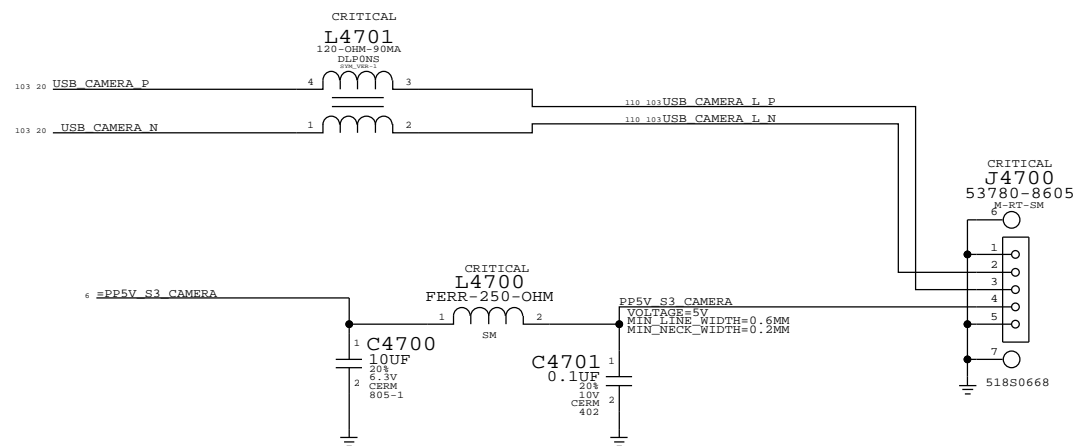
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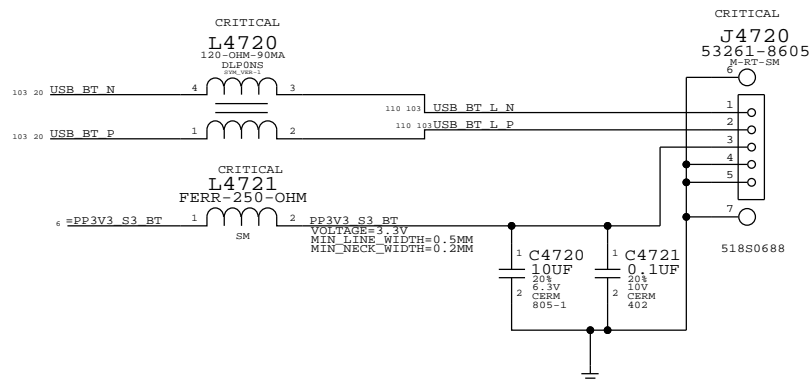
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CAMERA CONNECTOR & FILTER

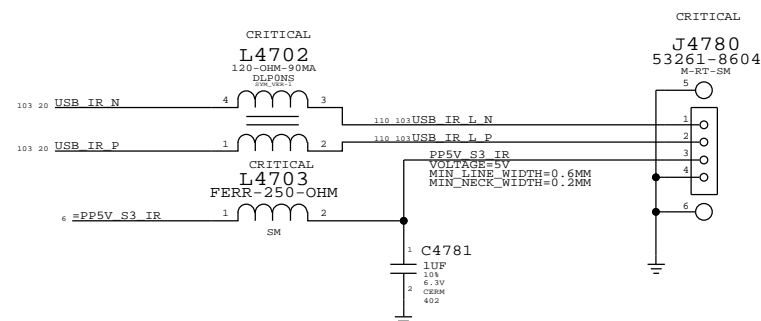


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

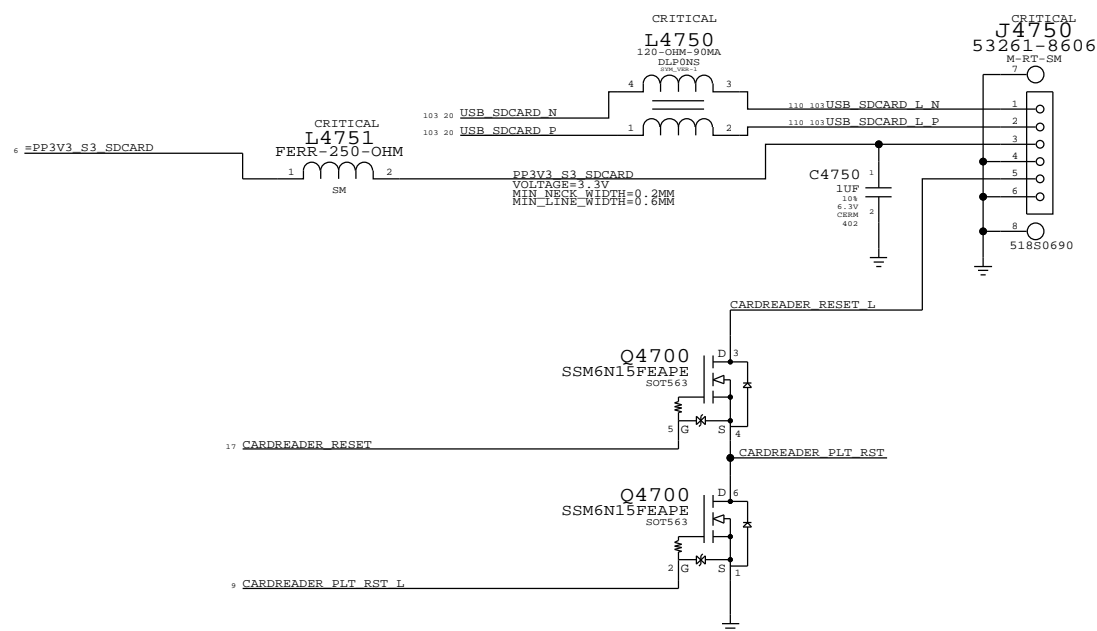
K37L (BLUETOOTH) CONNECTOR



IR RECEIVER CONNECTOR




SD Card Reader Board Connector

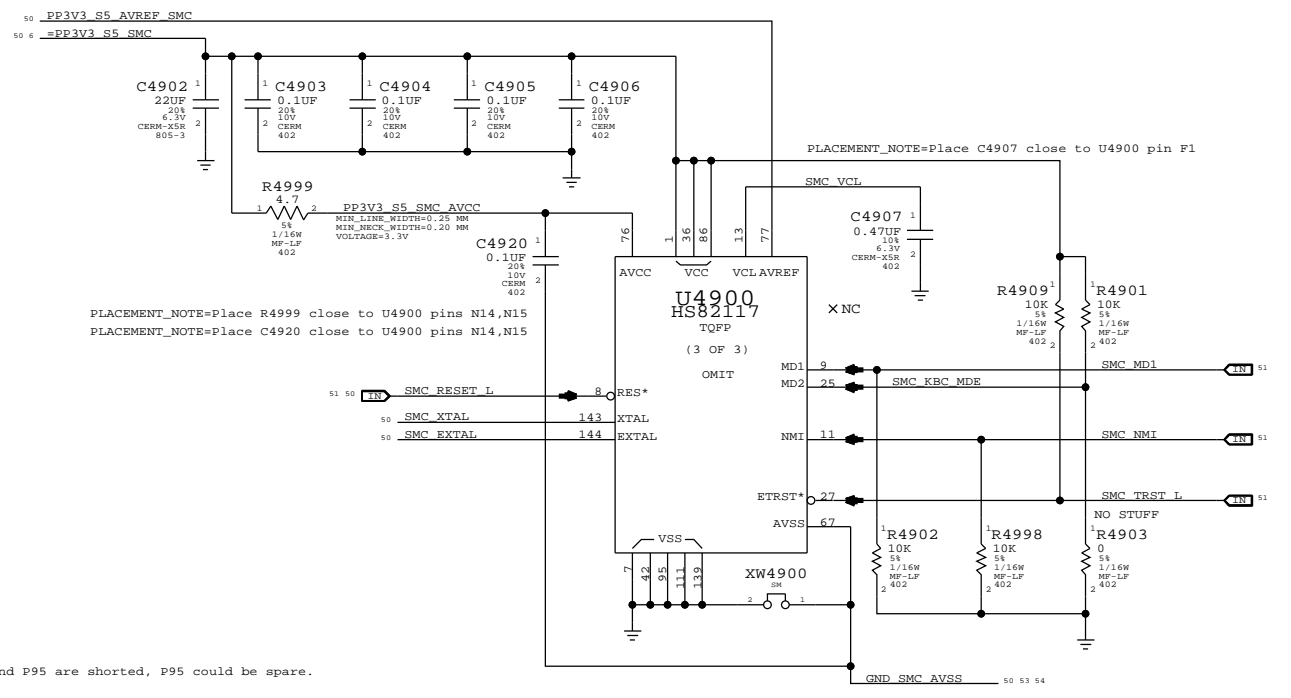
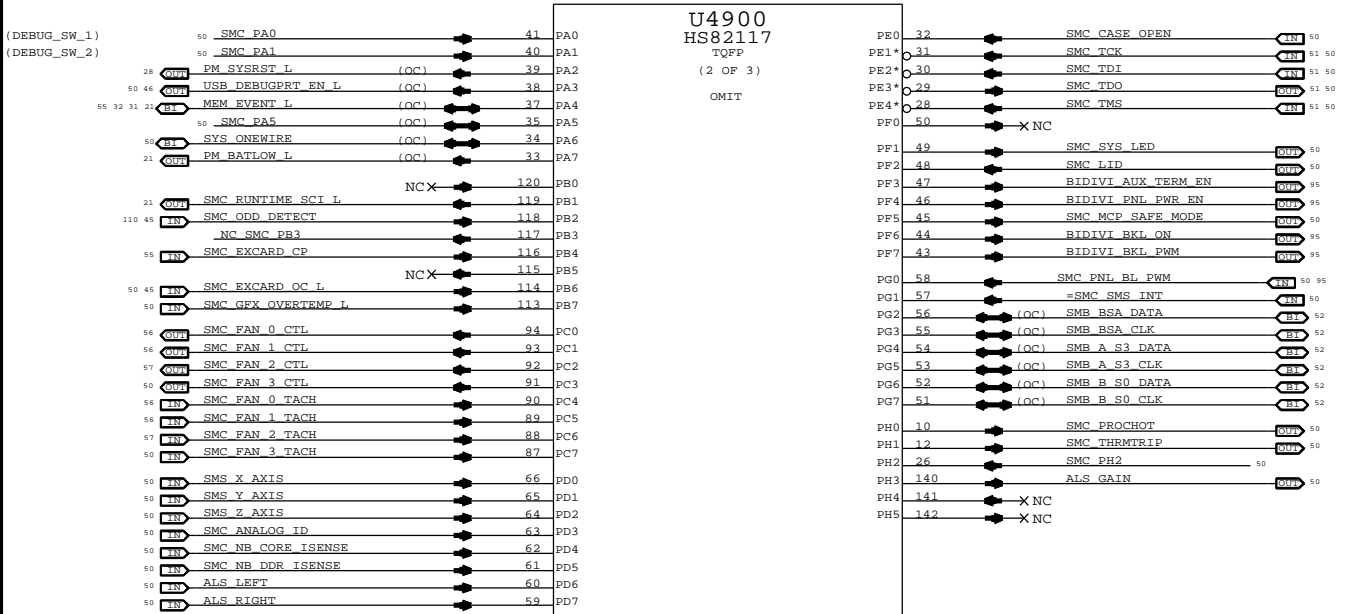
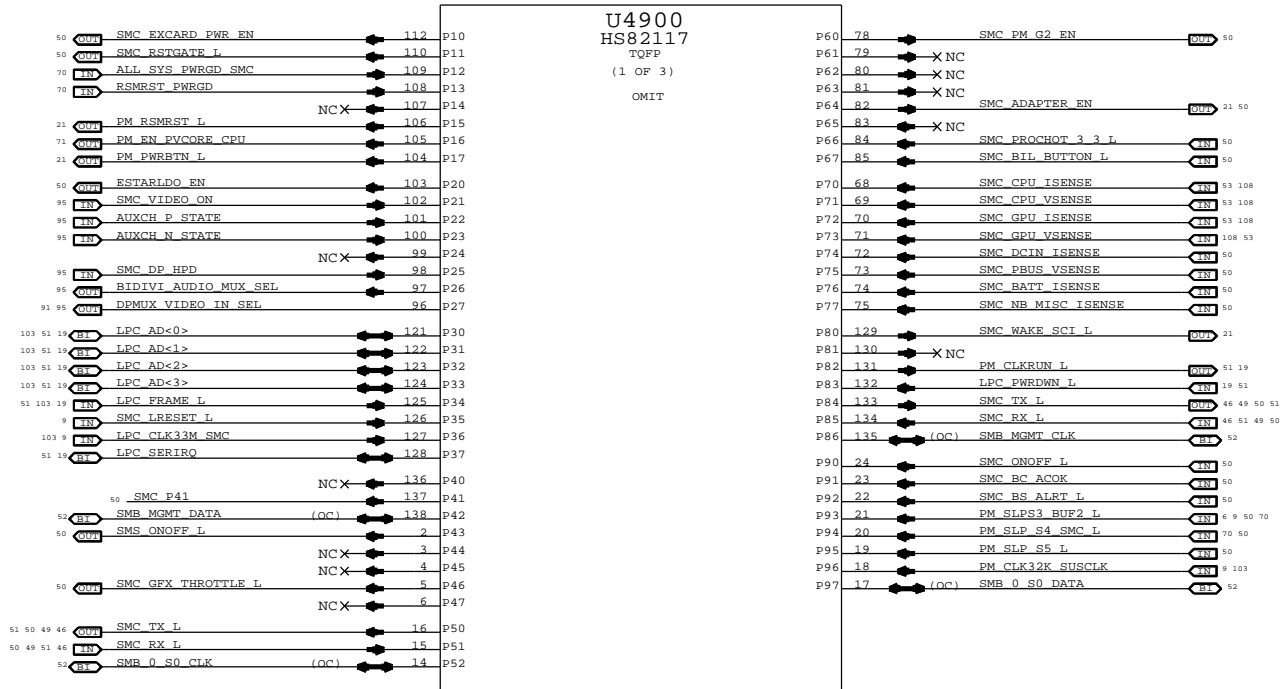


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Internal USB Connections			
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		SHEET 48 OF 110	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2009

SMC Apple Inc.

051-7863 D

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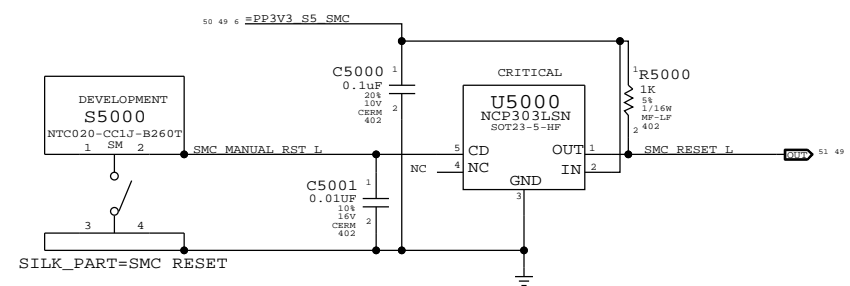
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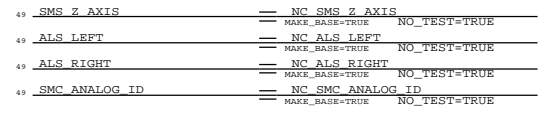
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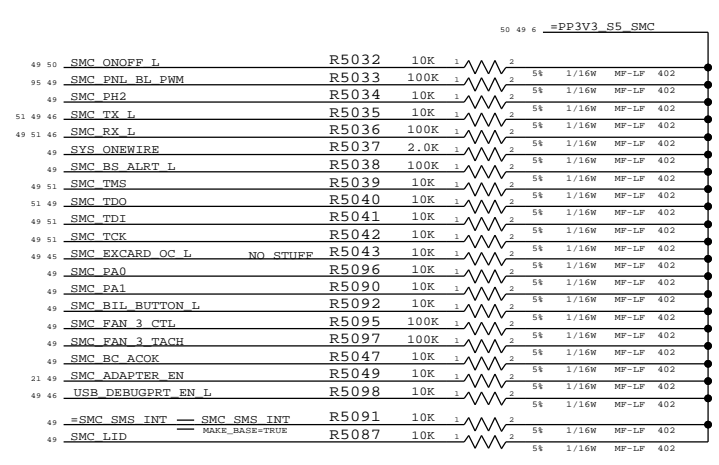
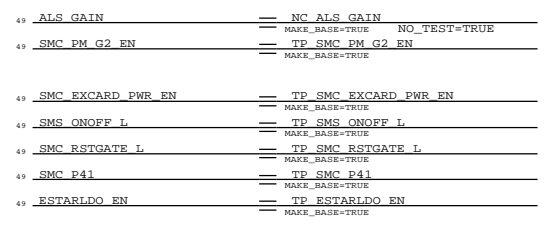
SMC Reset Button / Brownout Detect



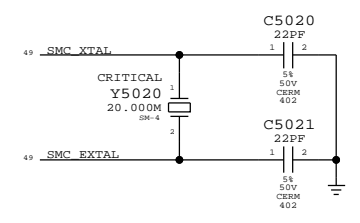
UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS



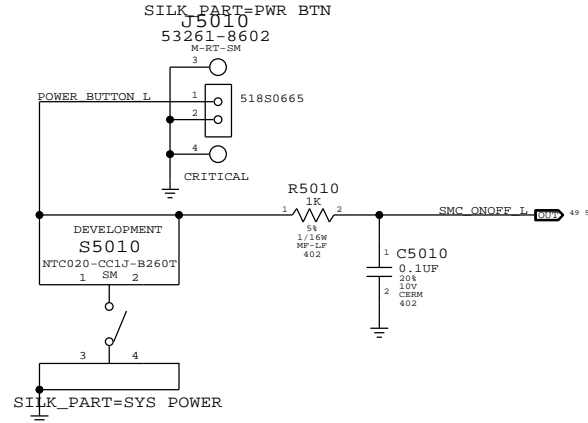
UNUSED TP/NC ALIASES



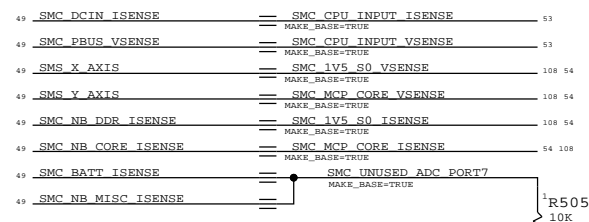
SMC Crystal Circuit



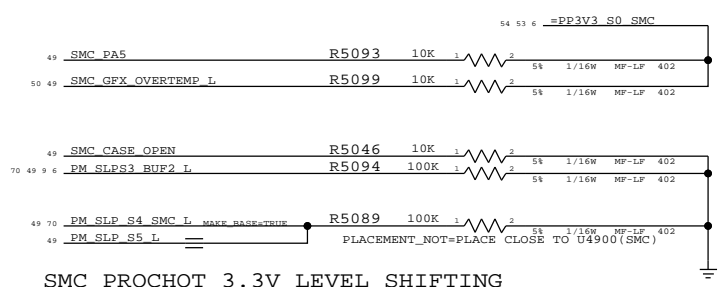
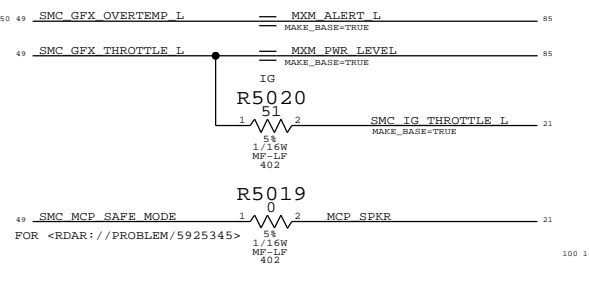
POWER BUTTON



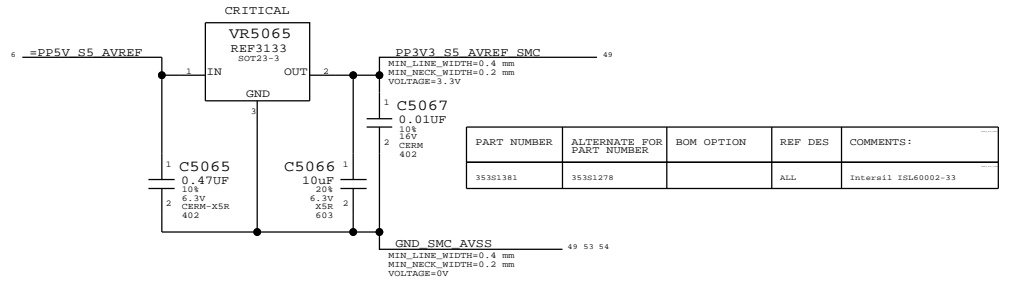
ANALOG SENSORS



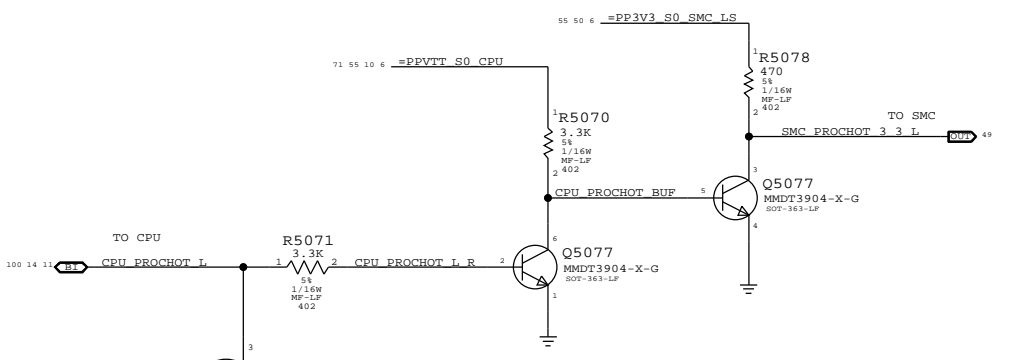
MISC. SIGNAL ALIASES



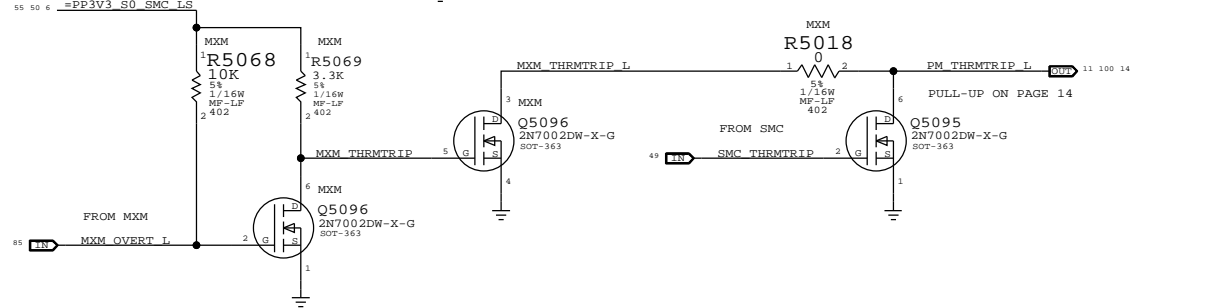
SMC AVREF Supply



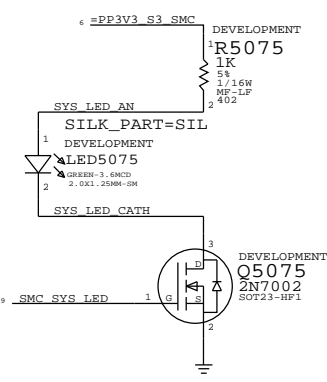
SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



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SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2009

SMC Support	
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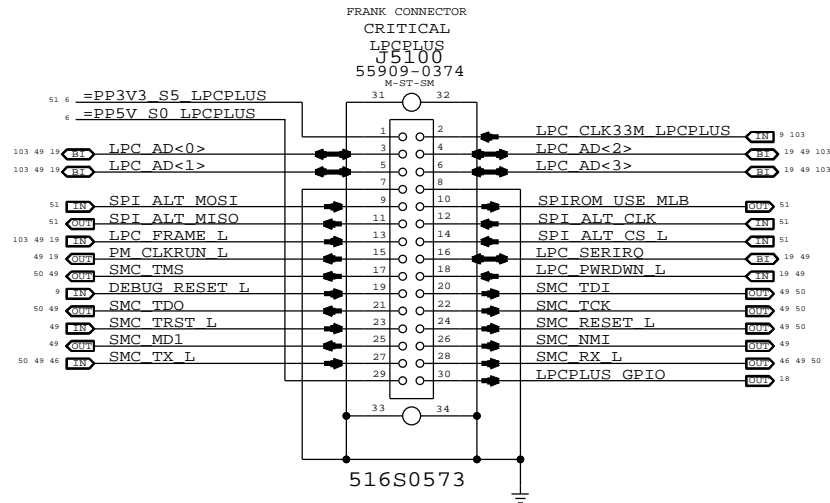
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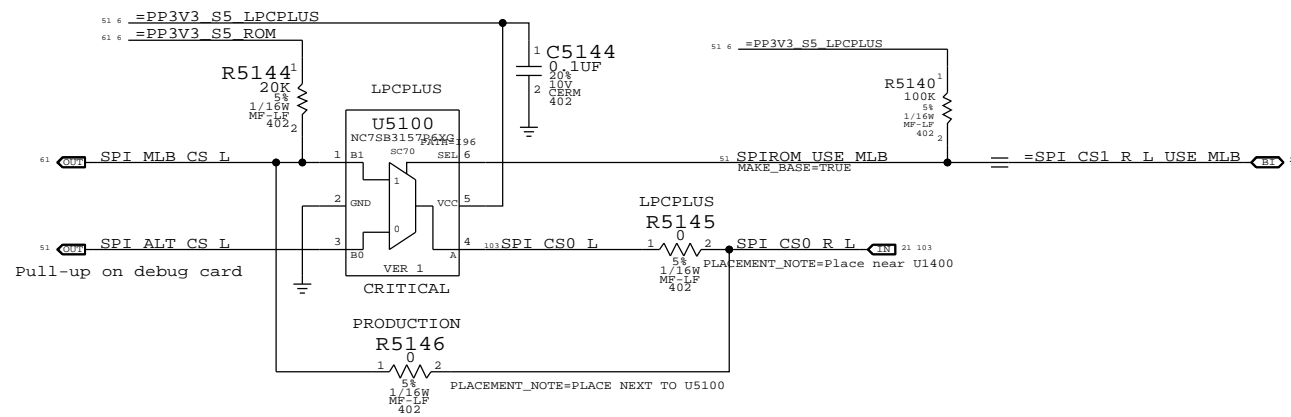
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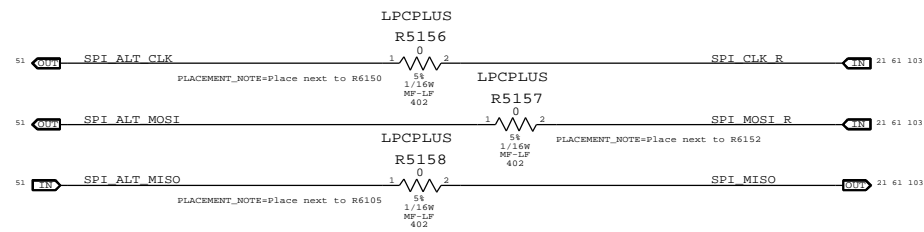
LPC+SPI Connector



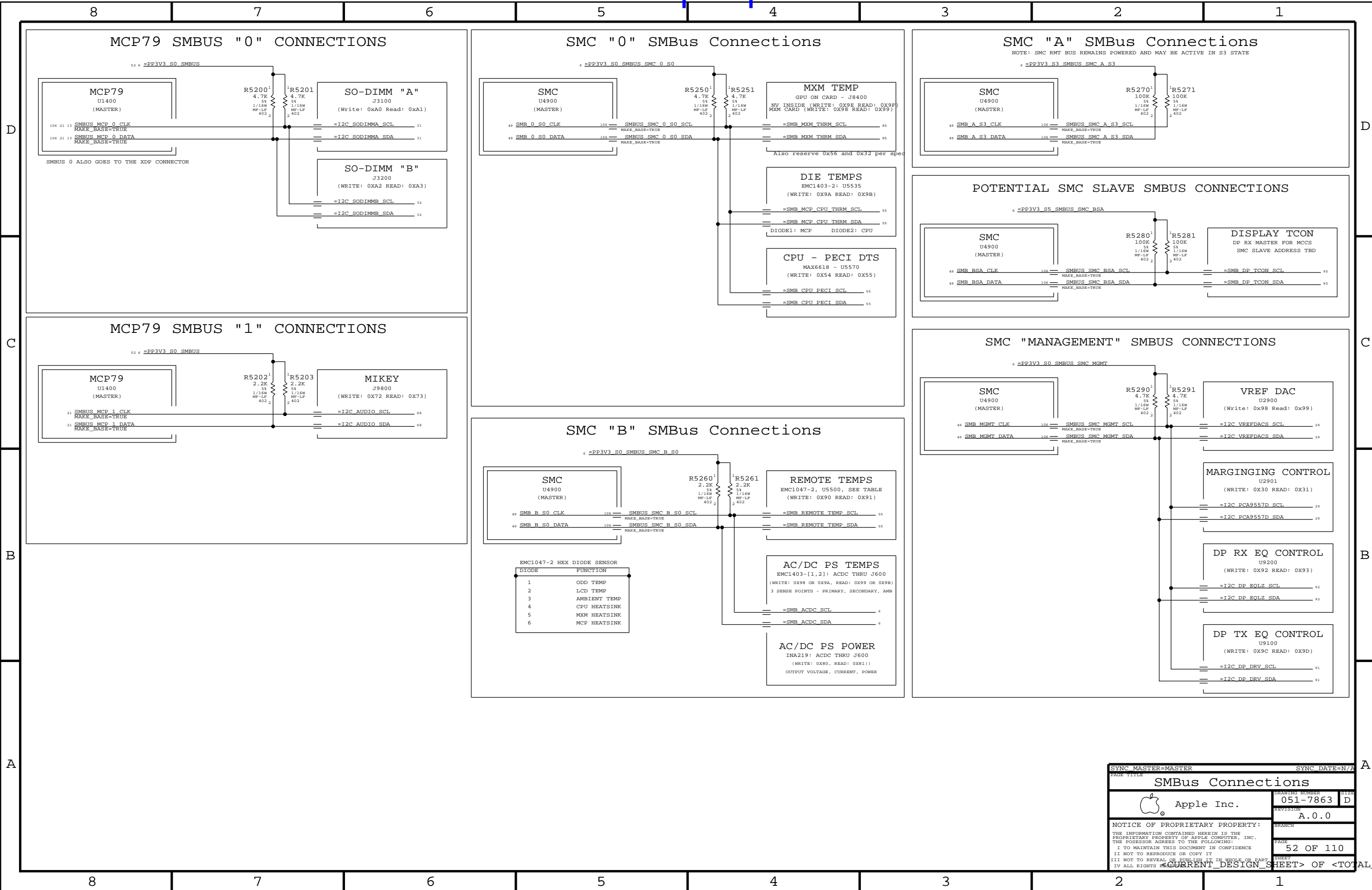
Alternate SPI ROM Support



SPI Bus Series Resistance Option



PAGE TITLE		SYNC DATE=09/02/2009	
LPC+SPI Debug Connector			
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051-7863		051-7863	
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SMBus Connections

Apple Inc.

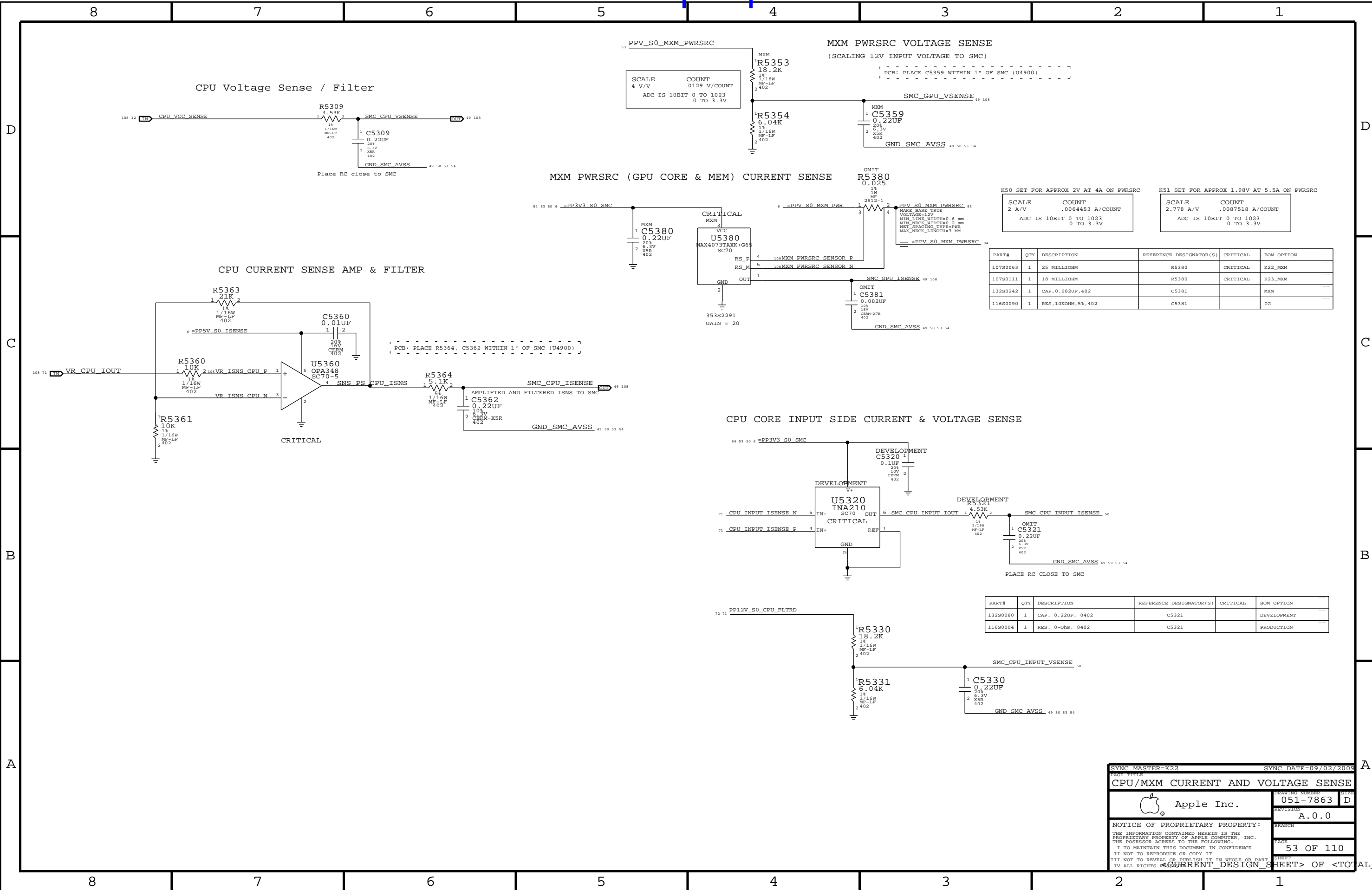
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K50 SET FOR APPROX 2V AT 4A ON PWSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT
ADC IS 10BIT 0 TO 1023 0 TO 3.3V	

K51 SET FOR APPROX 1.98V AT 5.5A ON PWSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT
ADC IS 10BIT 0 TO 1023 0 TO 3.3V	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP, 0.082UF, 402	C5381		MXM
116S0090	1	RES, 10KOHM, 54, 402	C5381		IG

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5321		DEVELOPMENT
116S0004	1	RES, 0-Ohm, 0402	C5321		PRODUCTION

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PAGE TITLE: CPU/MXM CURRENT AND VOLTAGE SENSE

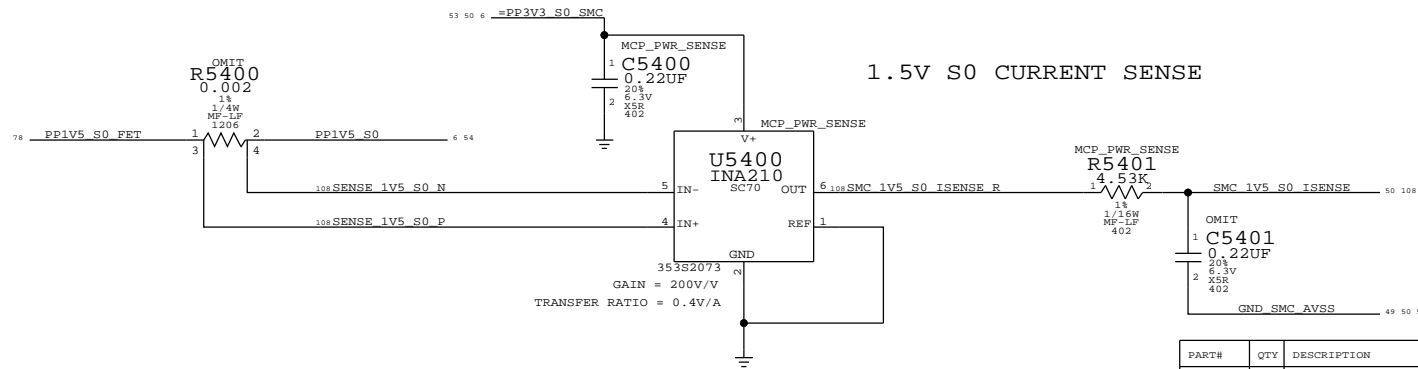
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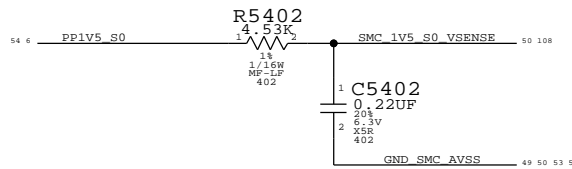


1.5V S0 CURRENT SENSE

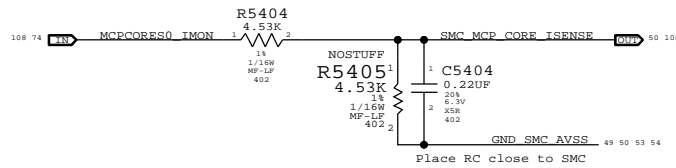
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10480018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
10180414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP, 0.22UF, 0402	C5401		MCP_PWR_SENSE
11680004	1	RES, 0 OHM, 0402	C5401		PRODUCTION

1.5V S0 VOLTAGE SENSE

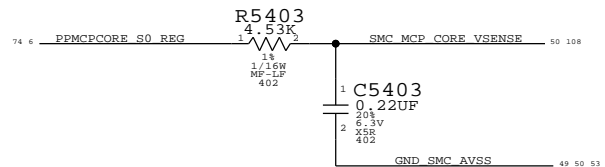


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

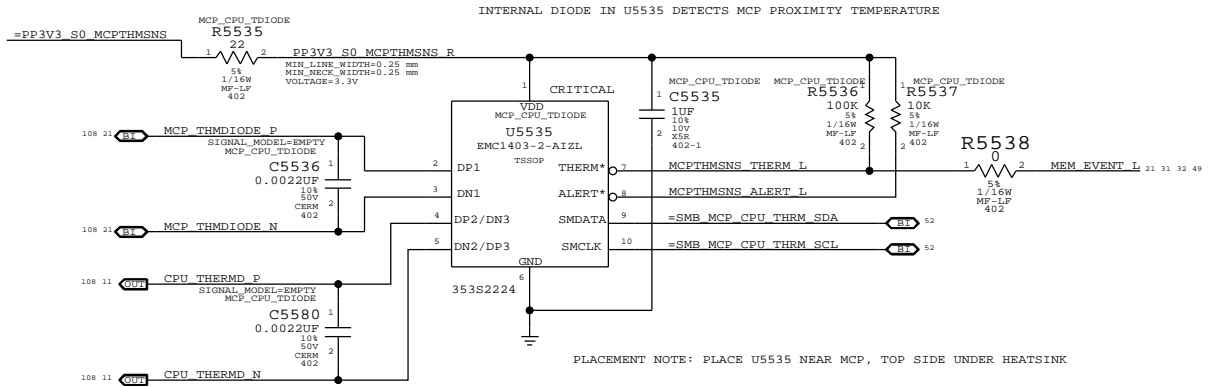
MCP CORE VOLTAGE SENSE



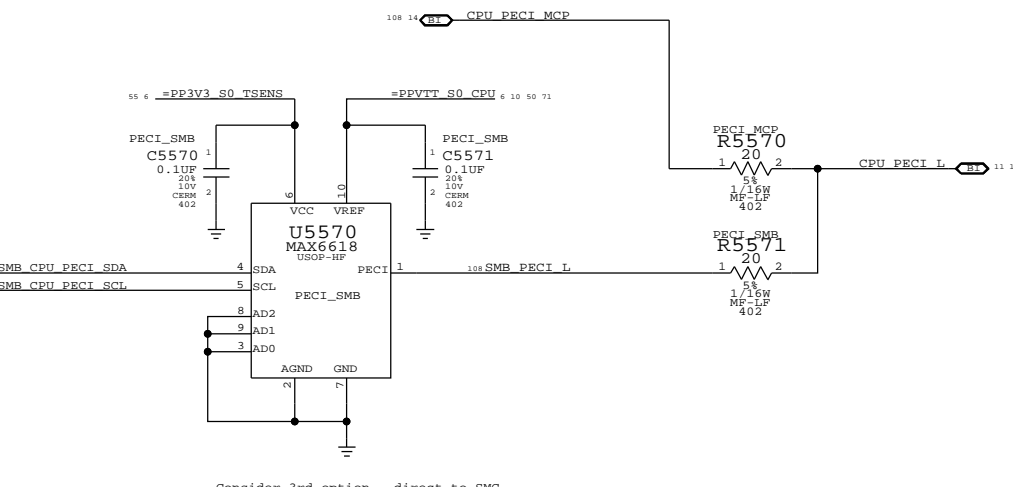
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MCP CURRENT AND VOLTAGE SENSE			
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REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

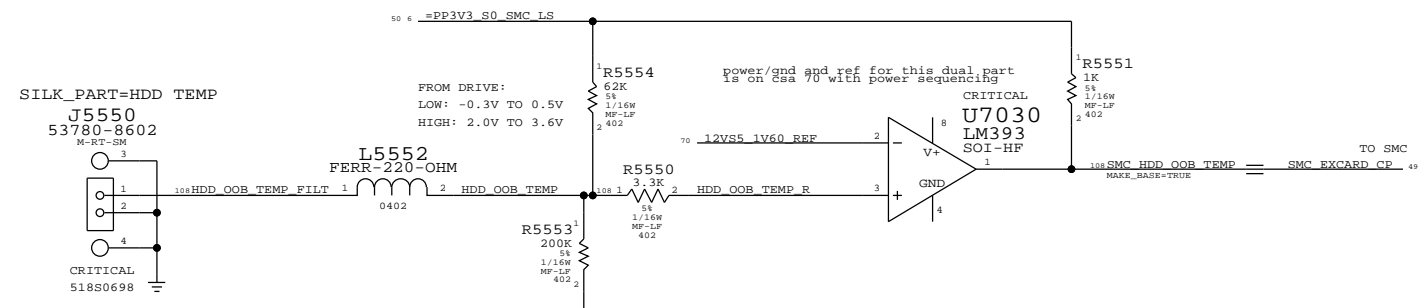
MCP & CPU T-Diode Thermal Sensor



CPU PECCI DTS OPTIONS



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



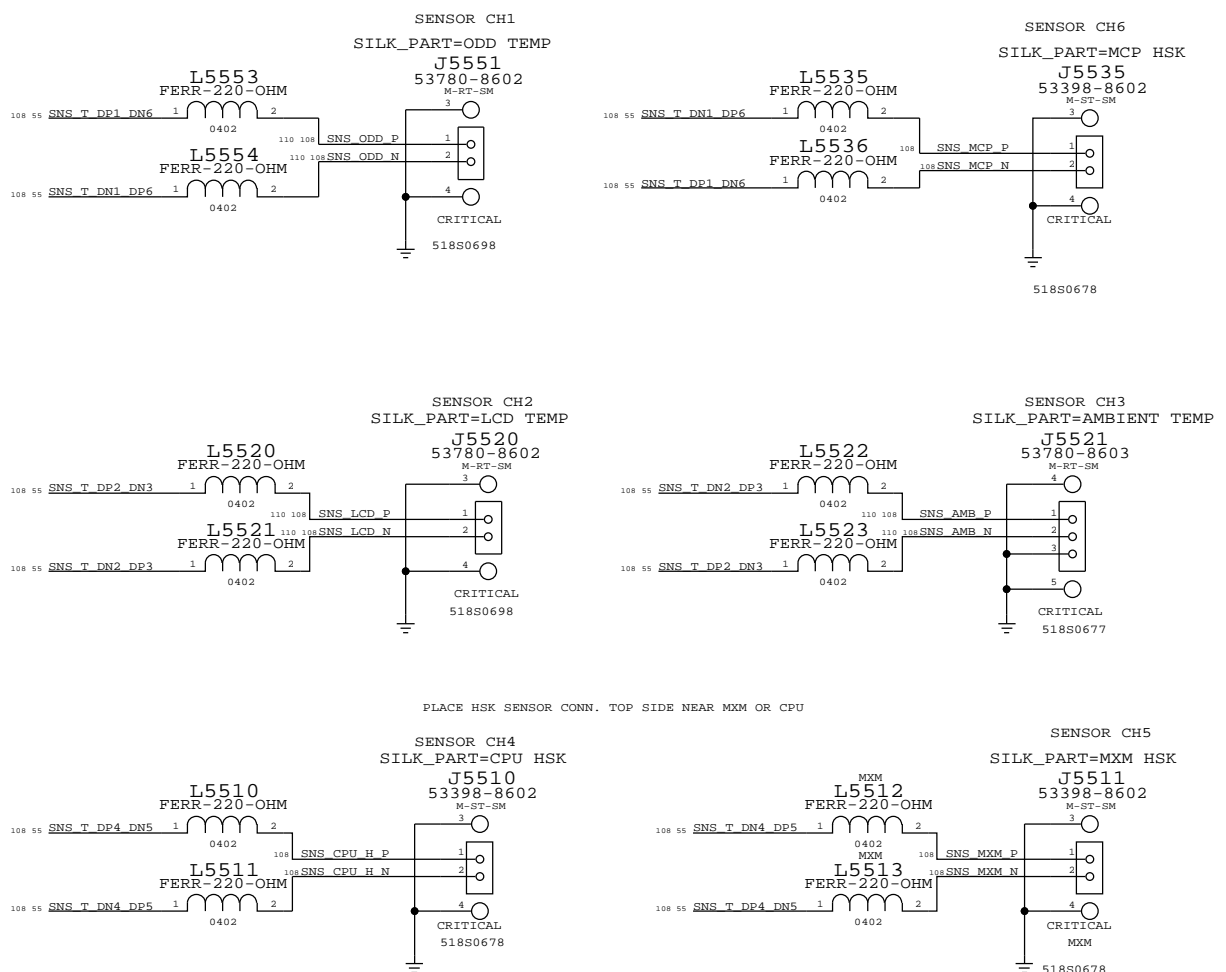
Drive active = valid signal, Drive asleep = HDO drives HDO OOB TEMP low, Drive disconnected = pulled high. Must pull high to 2.5V for compatibility with all drives. Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA.

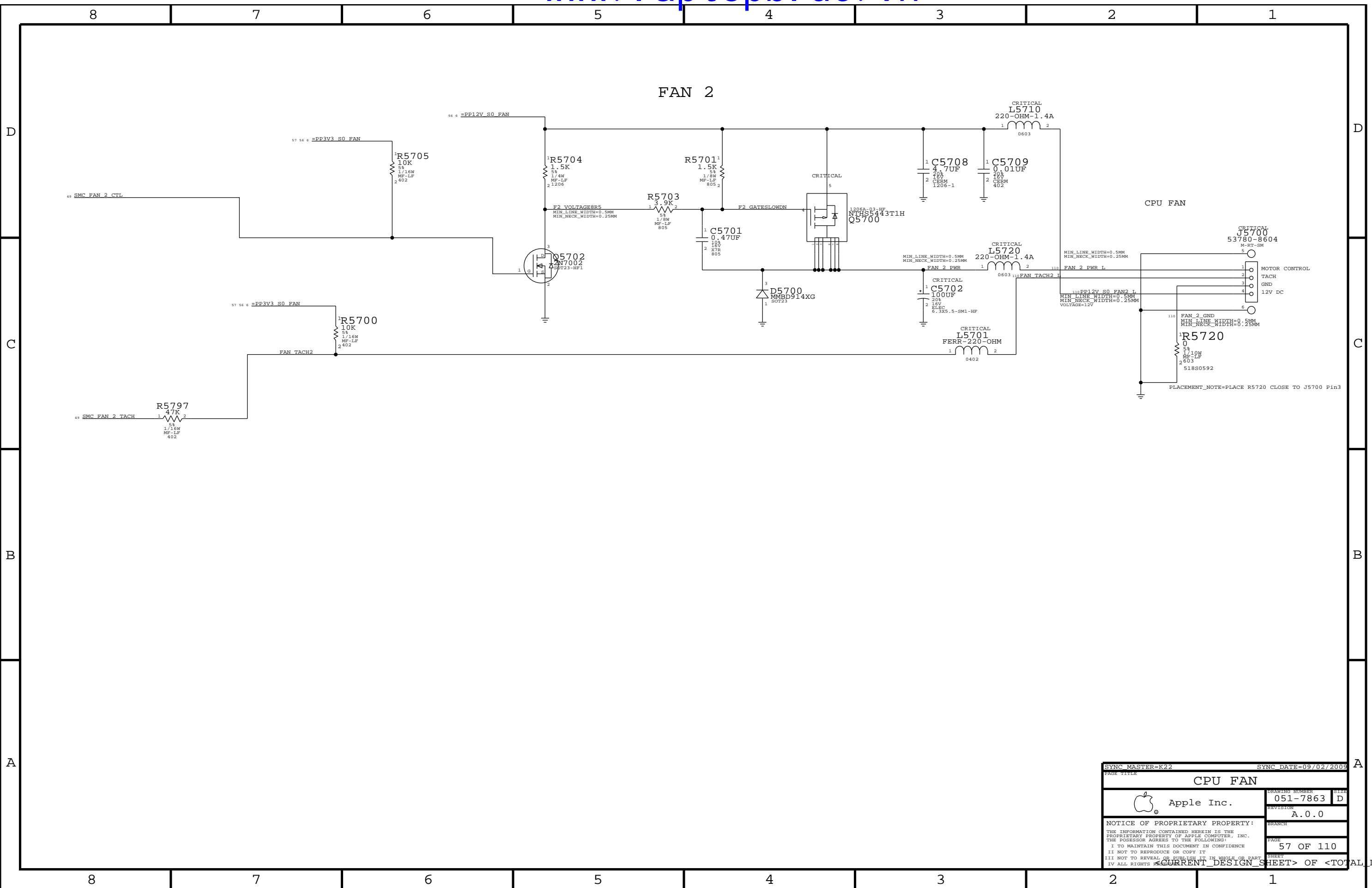
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REMOTE THERMAL SENSORS (HEATSINKS AND ODD)






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CPU FAN			
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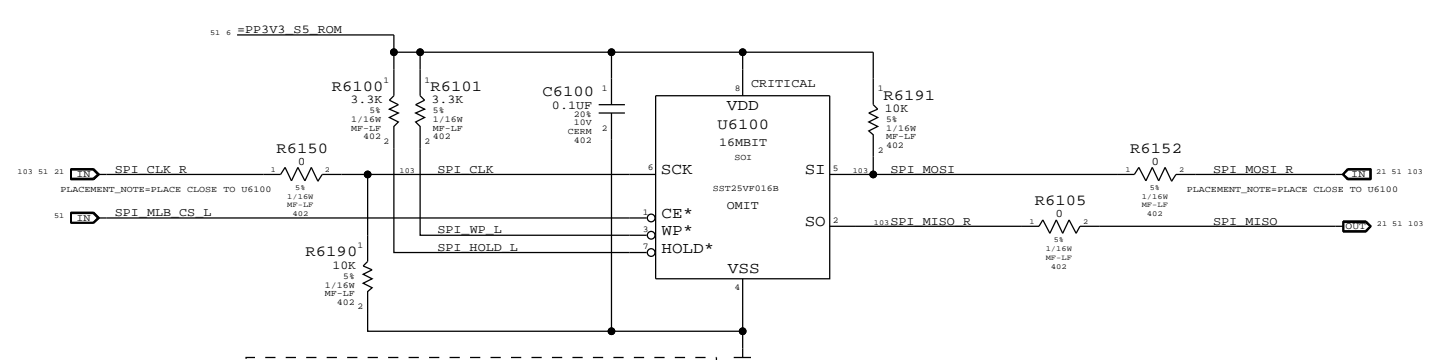
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		SHEET 60 OF 110	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.
SST25VF016B max speed for READ command is 25MHz.

SYNC MASTER=K22 SYNC DATE=09/02/2009

SPI ROM

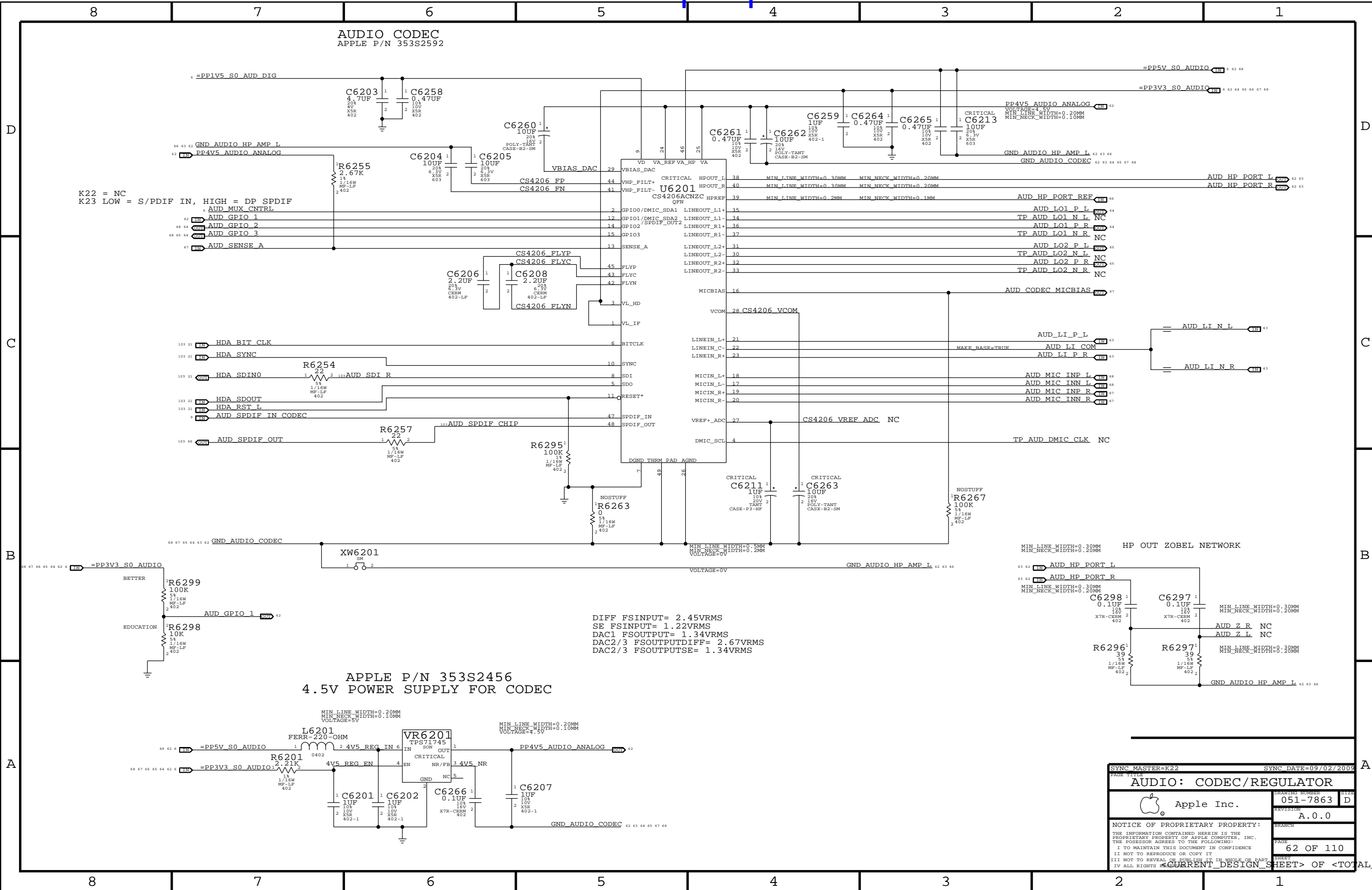
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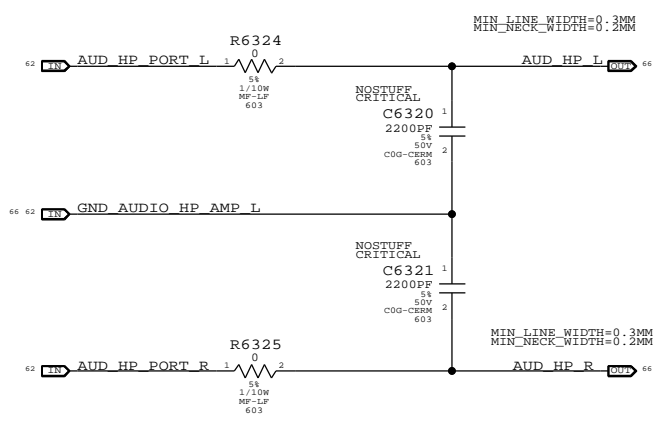
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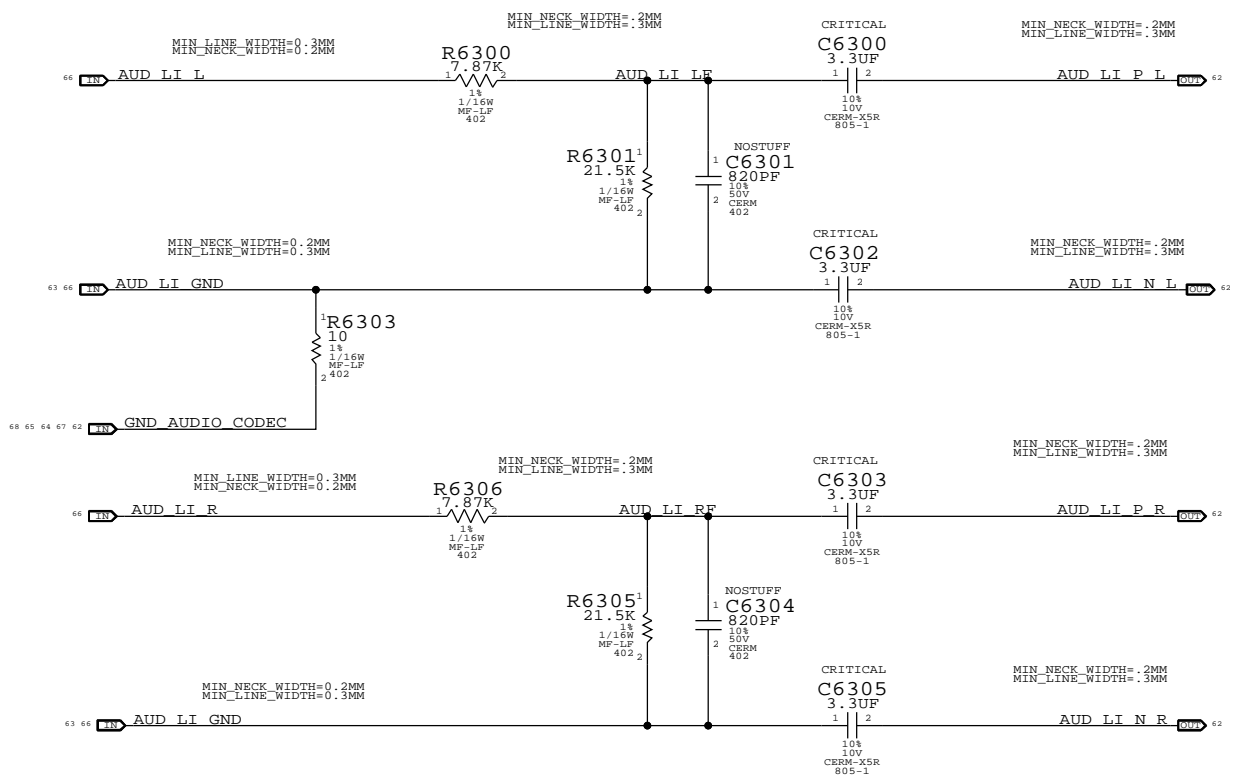


PAGE TITLE		SYNC DATE=09/02/2009	
AUDIO: CODEC/REGULATOR			
Apple Inc.		DESIGN NUMBER	051-7863 D
		REVISION	A.0.0
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1ST ORDER DAC FILTER PLACEHOLDER



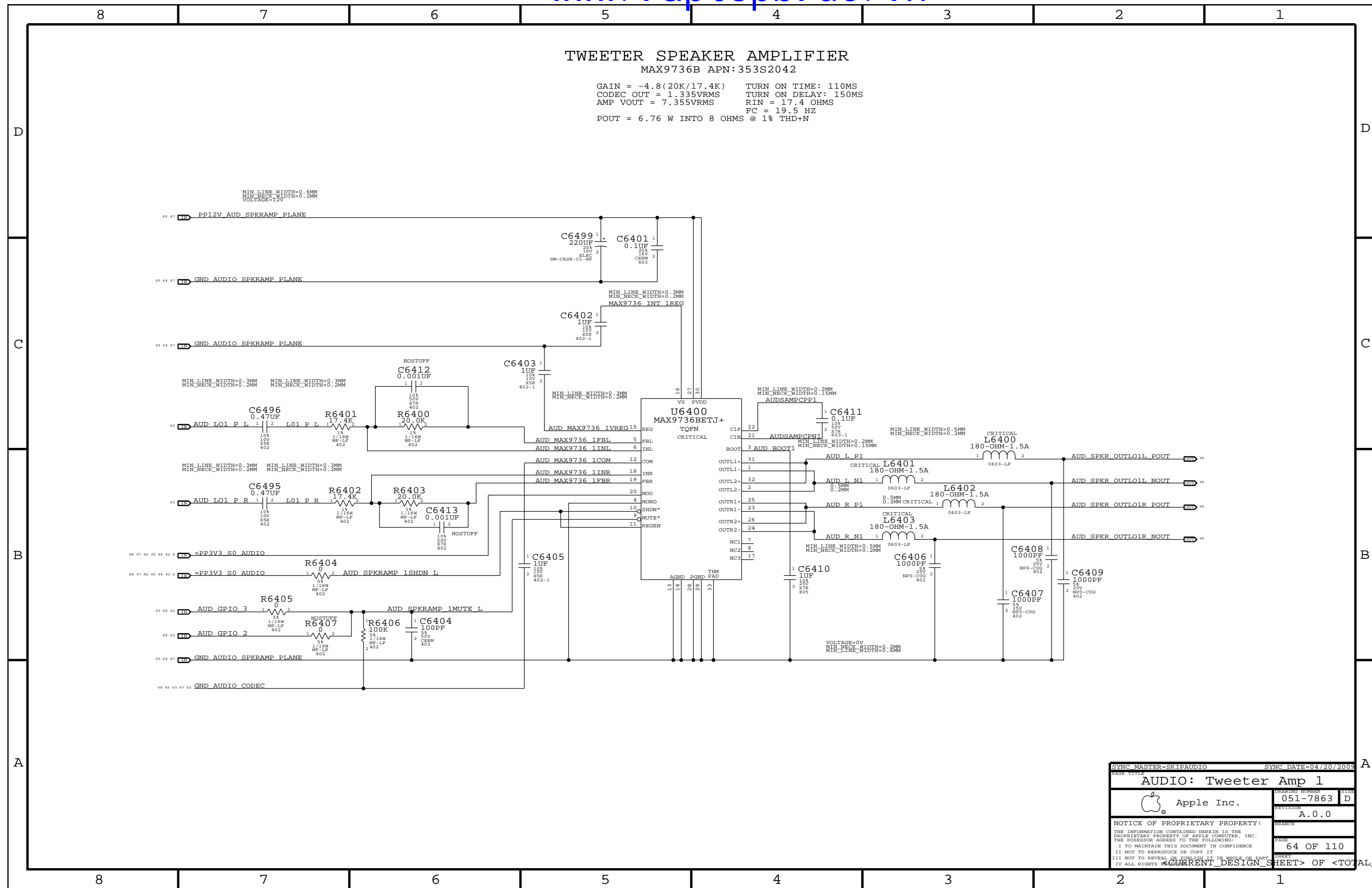
CODEC Nom SE RIN = 20K OHMS
 FC = 5 HZ Max
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS
 NET RIN = 18K OHMS



SYNC MASTER=SKIPAUDIO		SYNC DATE=04/20/2009	
PAGE TITLE			
AUDIO: FILTER/BUFFER			
Apple Inc.		DRAWING NUMBER	051-7863 D
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TWEETER SPEAKER AMPLIFIER
MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K) TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS RIN = 17.4 OHMS
FC = 19.5 HZ
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

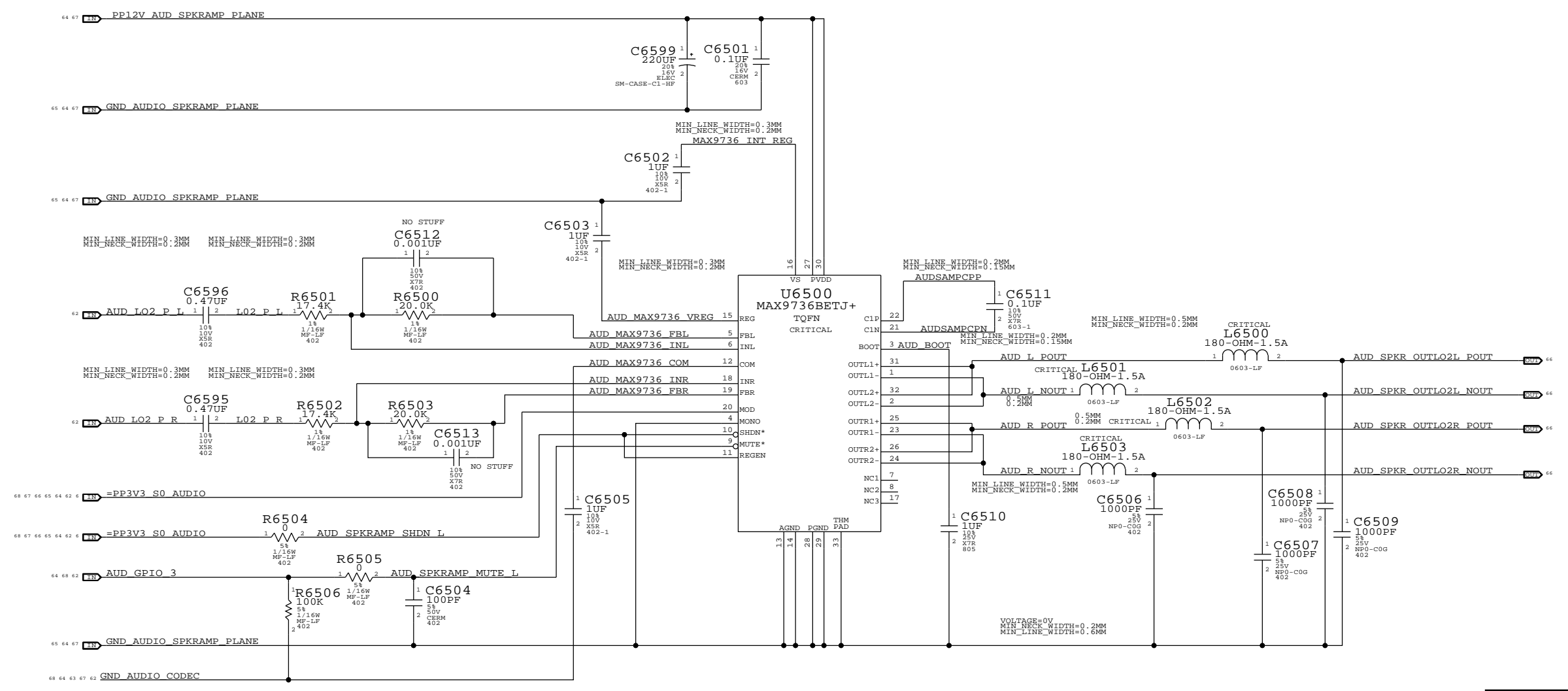


SYNC MASTER=SKIPAUDIO		SYNC DATE=04/20/2009	
PAGE TITLE AUDIO: Tweeter Amp 1			
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WOOFER SPEAKER AMPLIFIER MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K) TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS RIN = 17.4 OHMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N FC = 19.5 HZ

MIN LINE WIDTH=0.5MM
MIN NECK WIDTH=0.2MM
VOLTAGE=12V

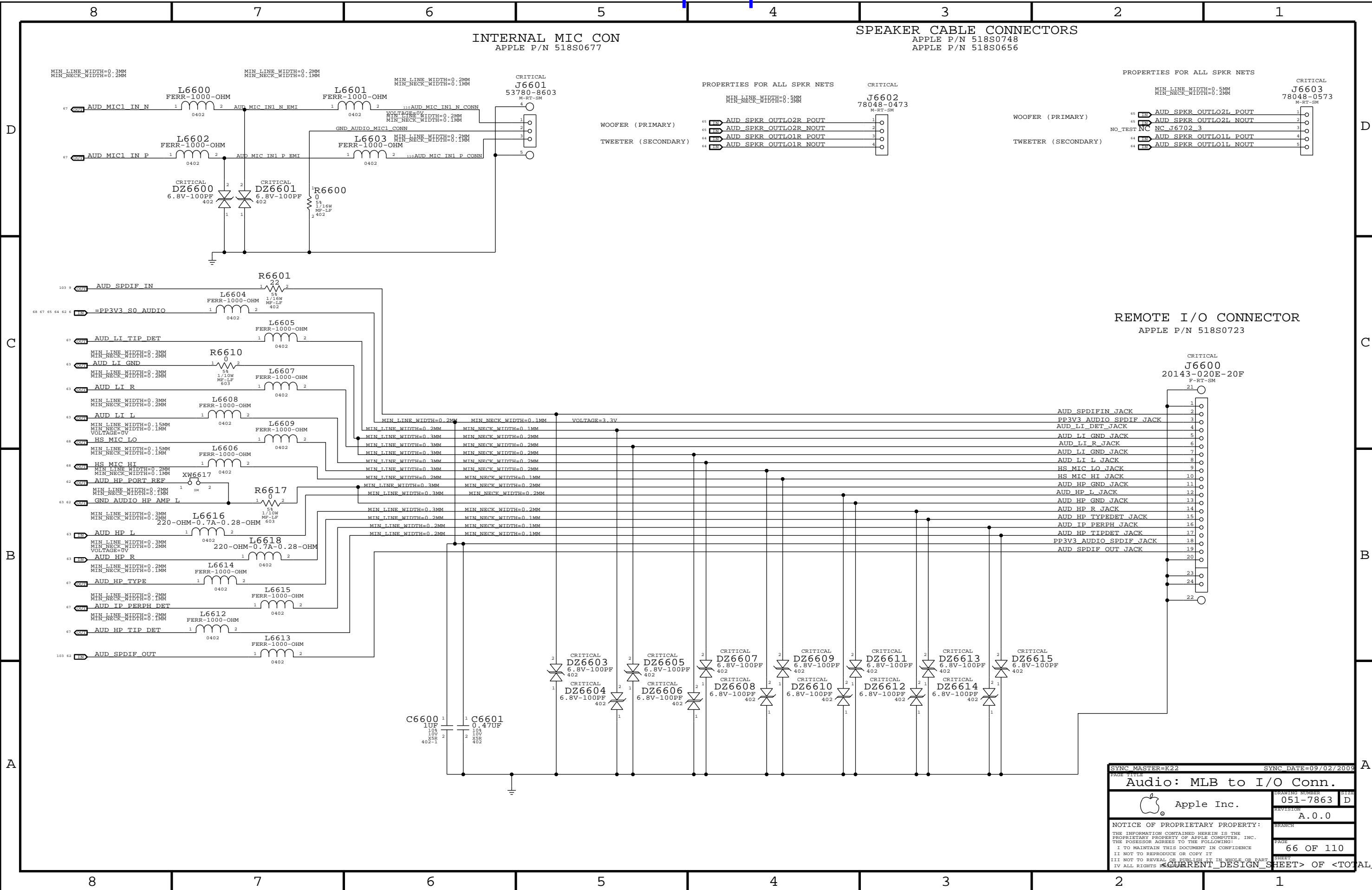


SYNC MASTER=SKIPAUDIO SYNC DATE=04/20/2009

AUDIO: Woofer Amp

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SHEET: 1 OF 1



SYNC MASTER=K22 SYNC DATE=09/02/2009

Audio: MLB to I/O Conn.

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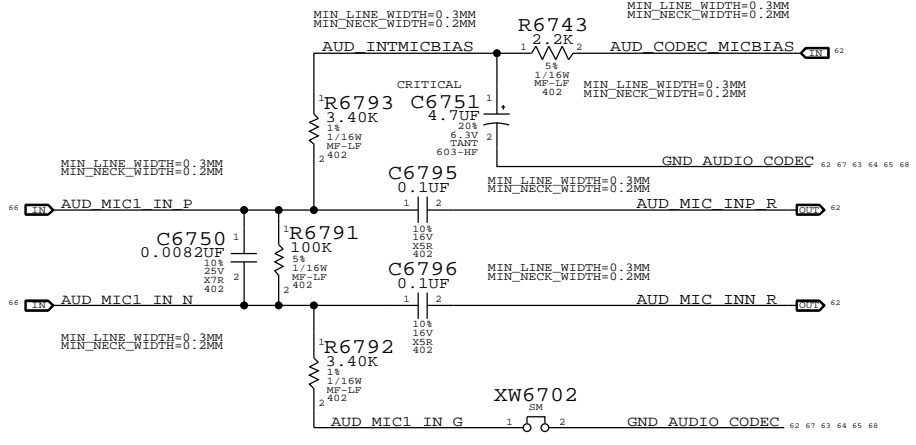
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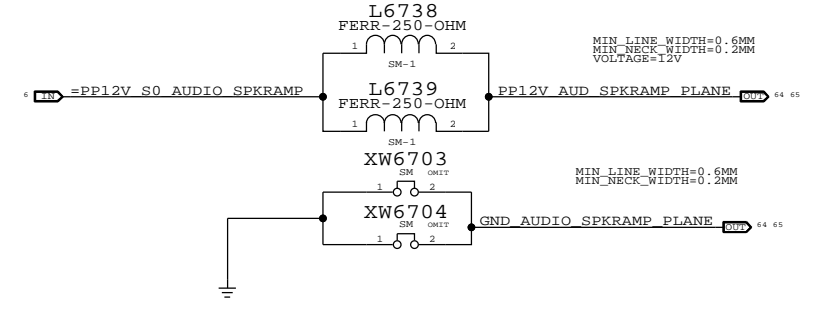
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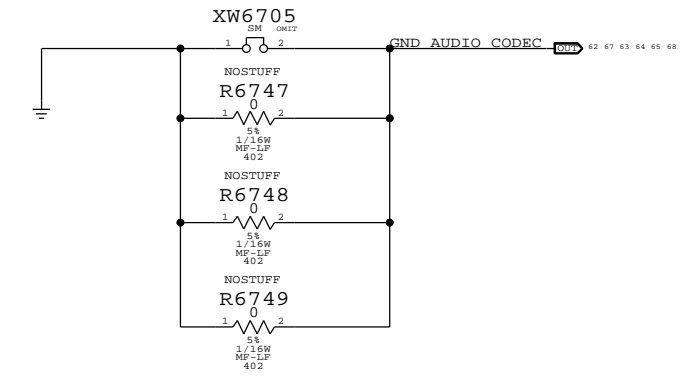
Internal Microphone Impedance Matching



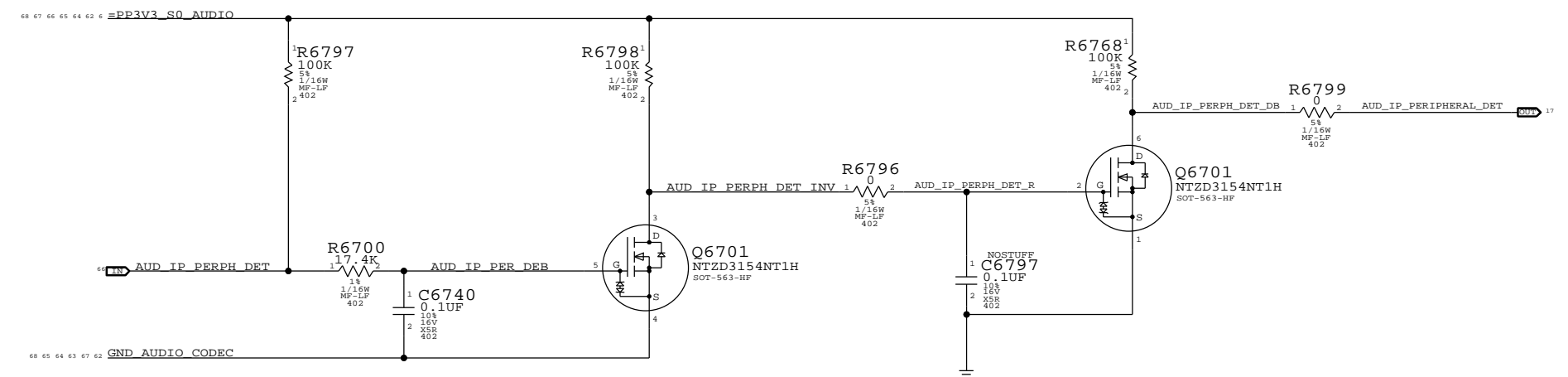
Place Across Ground Split



Audio Ground Returns



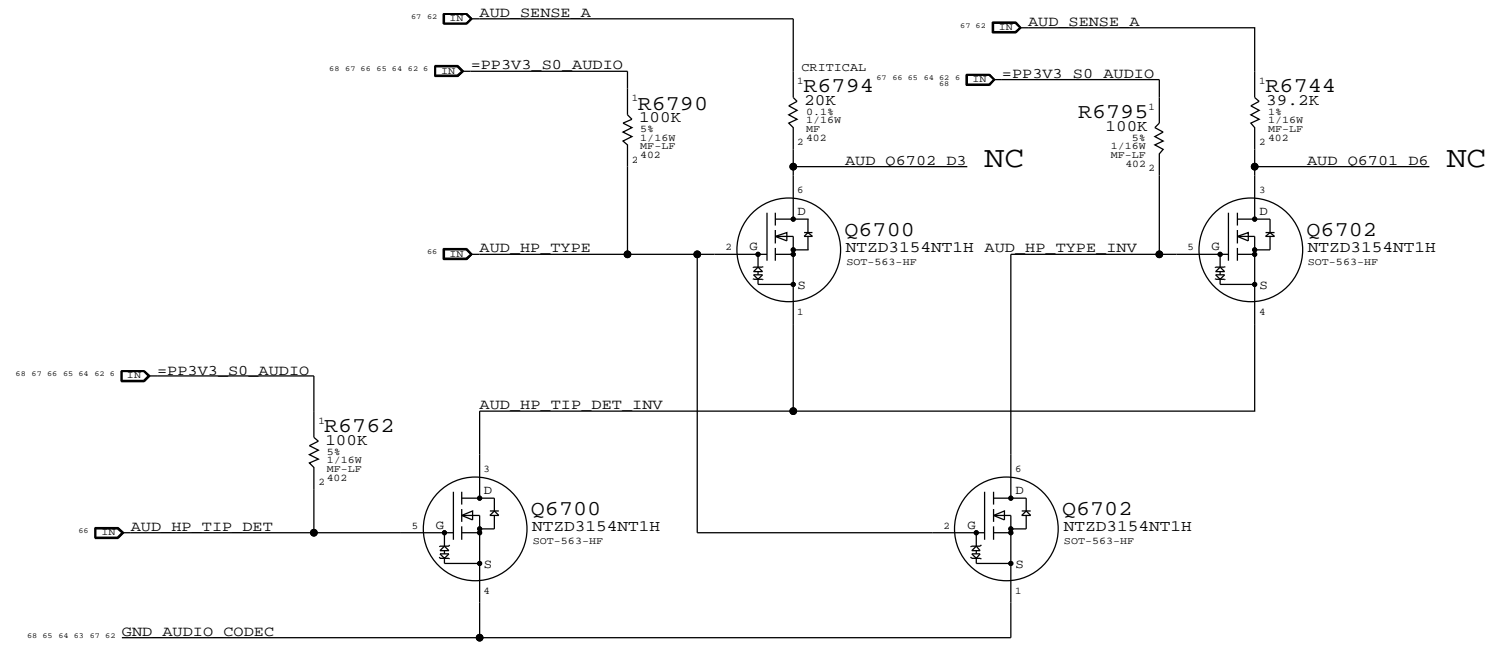
IPHS HS Detect Debounce CKT



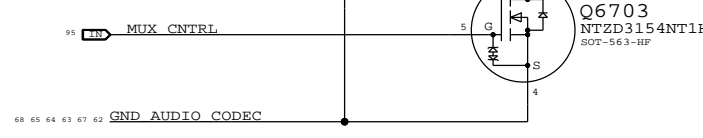
Digital Out

Headphone Out

LI Insert Detect



DP Audio Enable

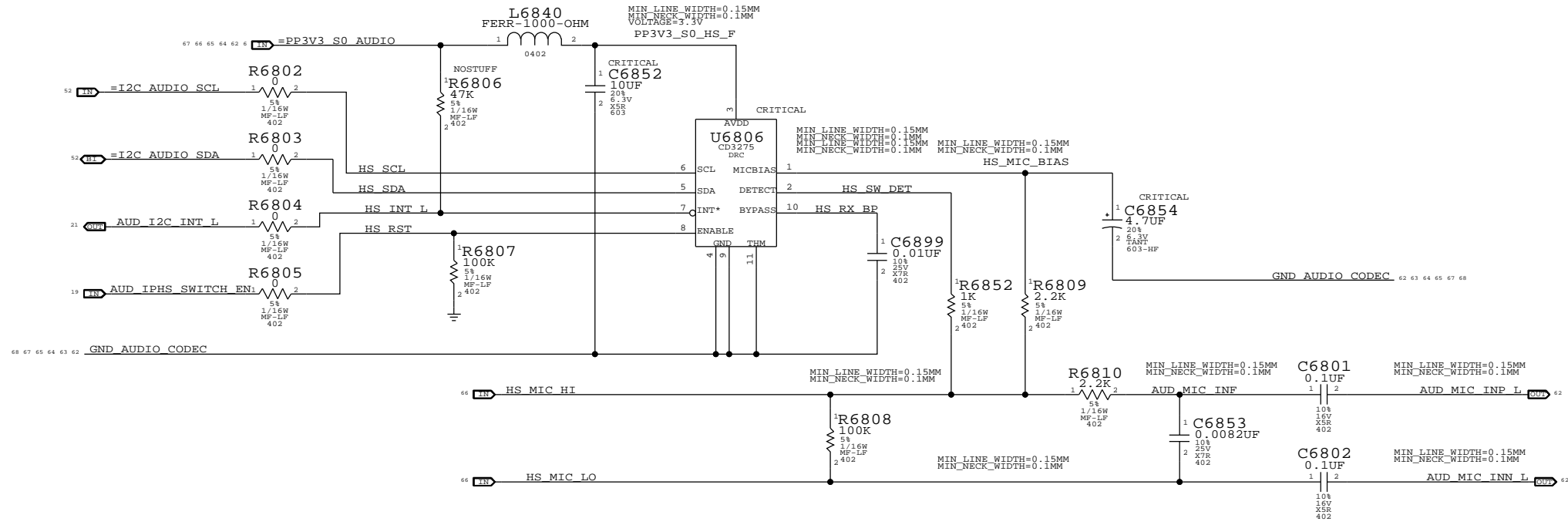


SYNC MASTER=SKIPAUDIO		SYNC DATE=04/20/2009	
AUDIO: Detects/Grounding			
Apple Inc.		CREATING NUMBER	051-7863 D
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		OF TOTAL DESIGN SHEETS	

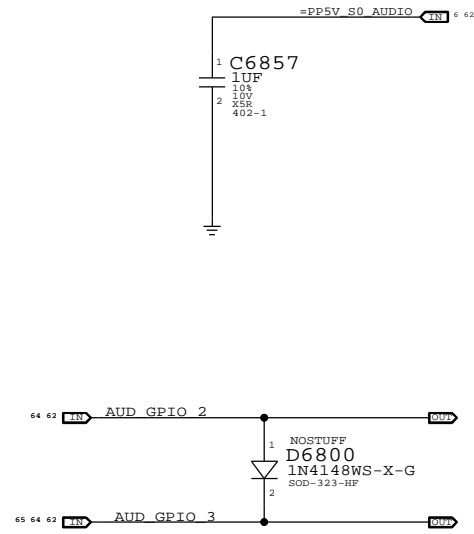
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/ INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

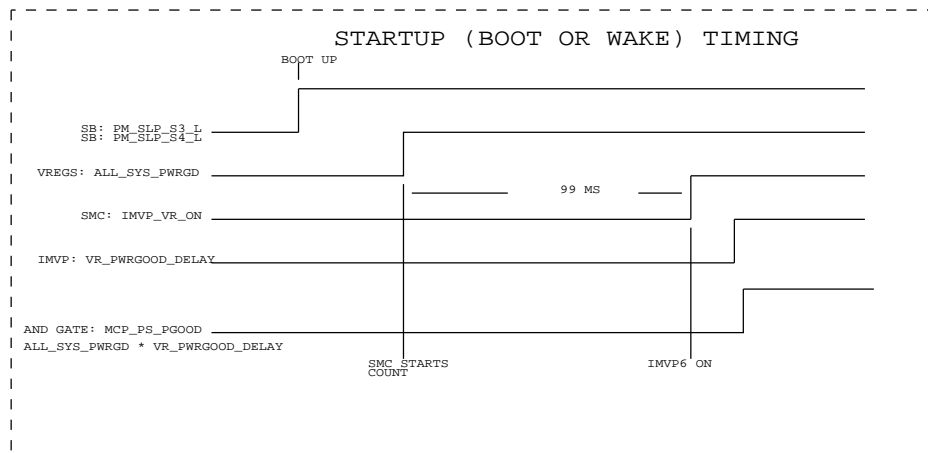
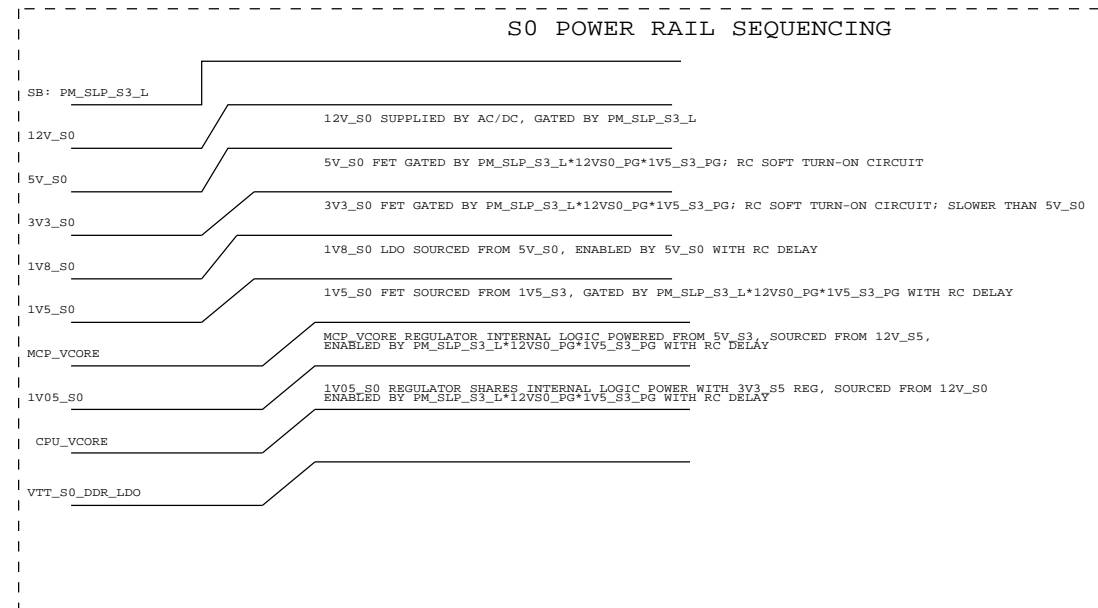
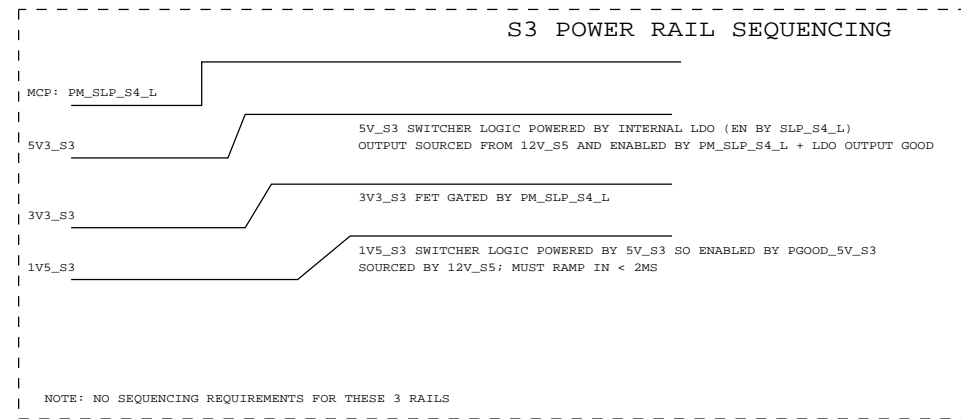
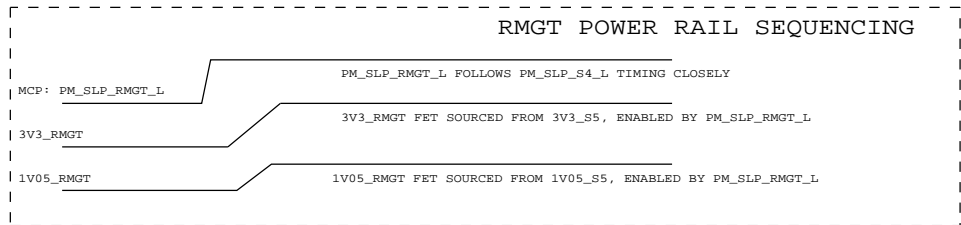
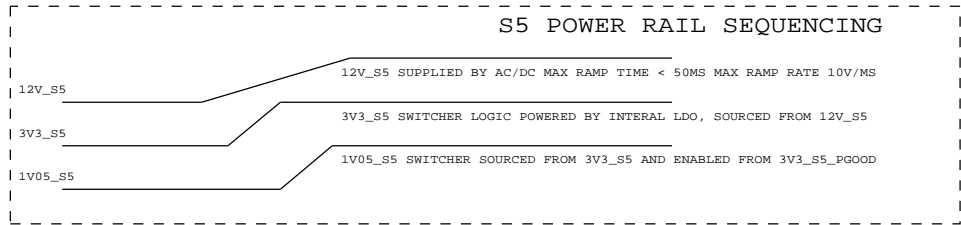


FLP = 8.82 KHZ
FHP = 80 HZ

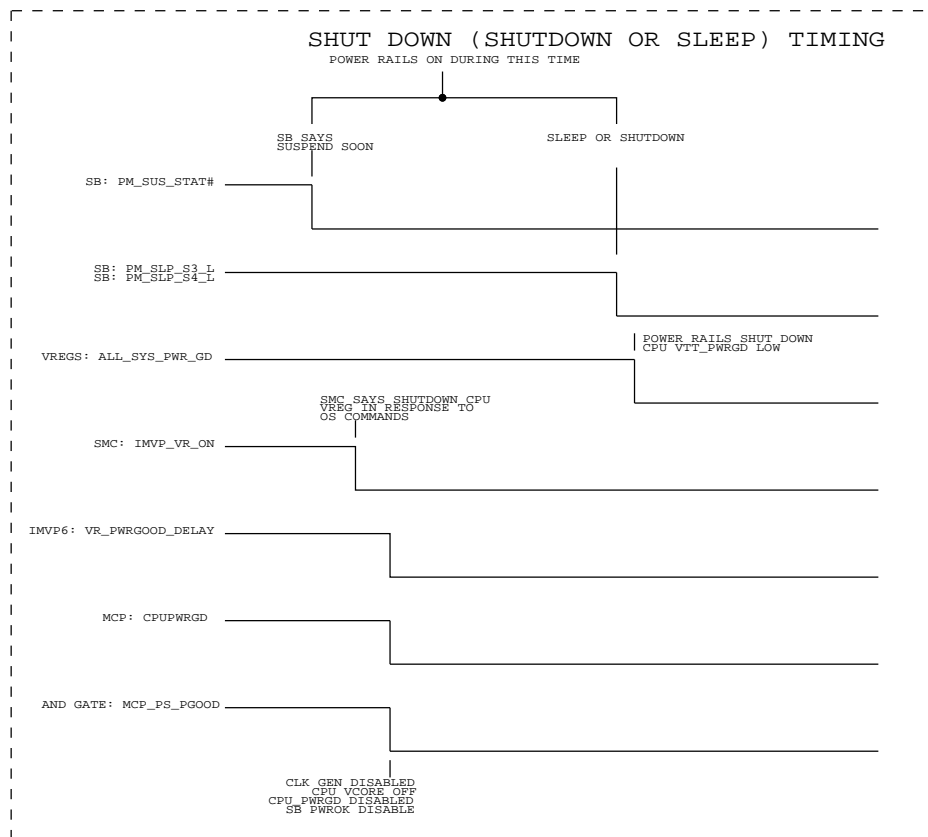


SYNC MASTER=K22		SYNC DATE=09/02/2009	
AUDIO: Mikey			
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8 7 6 5 4 3 2 1



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	off	1	1	0	1	0
Soft-Off (S5/M-Off)	off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0



SYNC MASTER=K22 SYNC DATE=09/02/2009

POWER SEQUENCING BLOCK DIAGRAM

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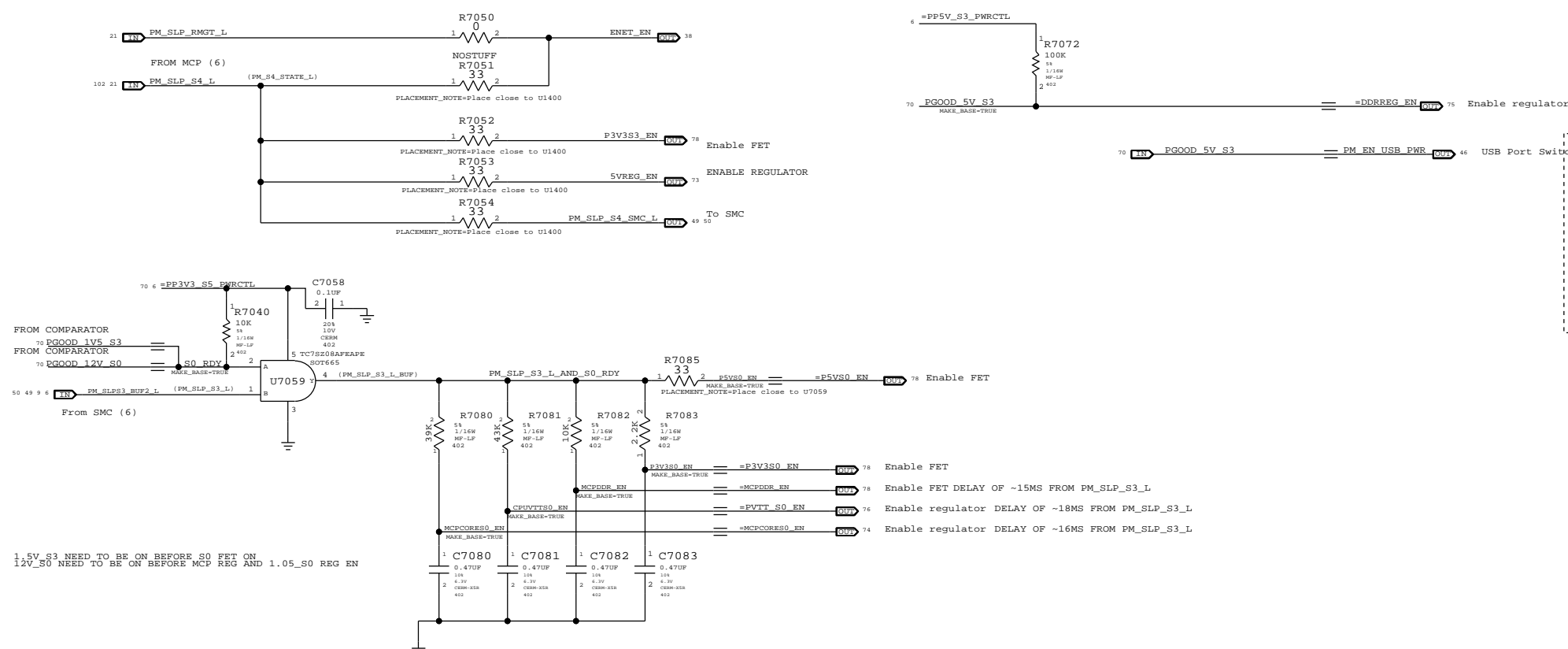
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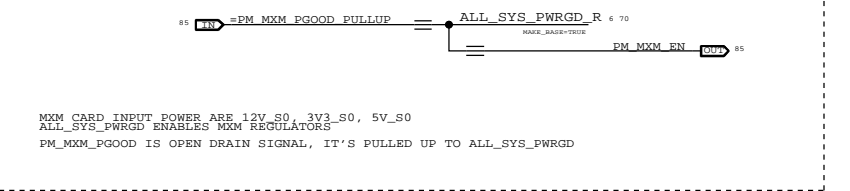
8 7 6 5 4 3 2 1

Power Control Signals
3.3V, 5V S3 enable

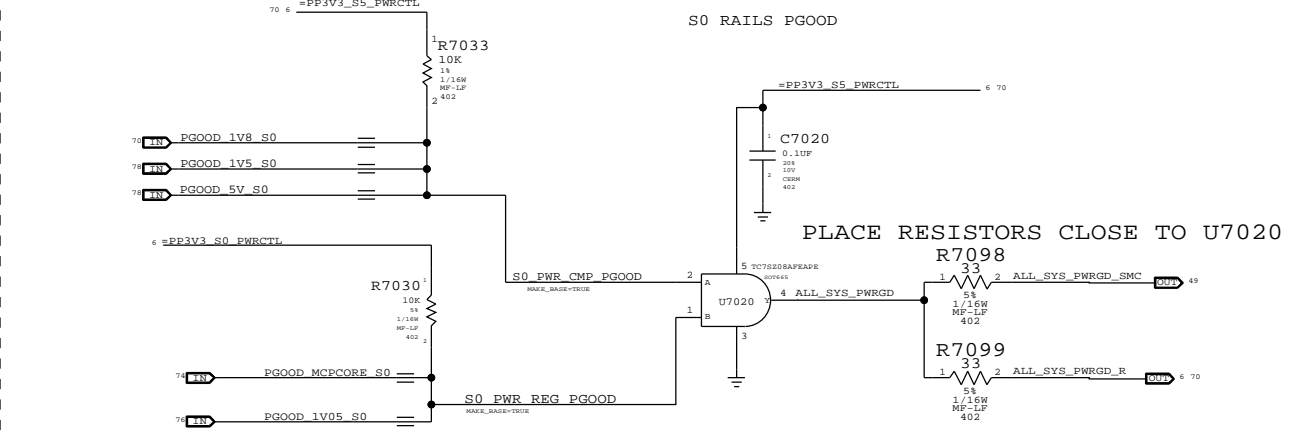
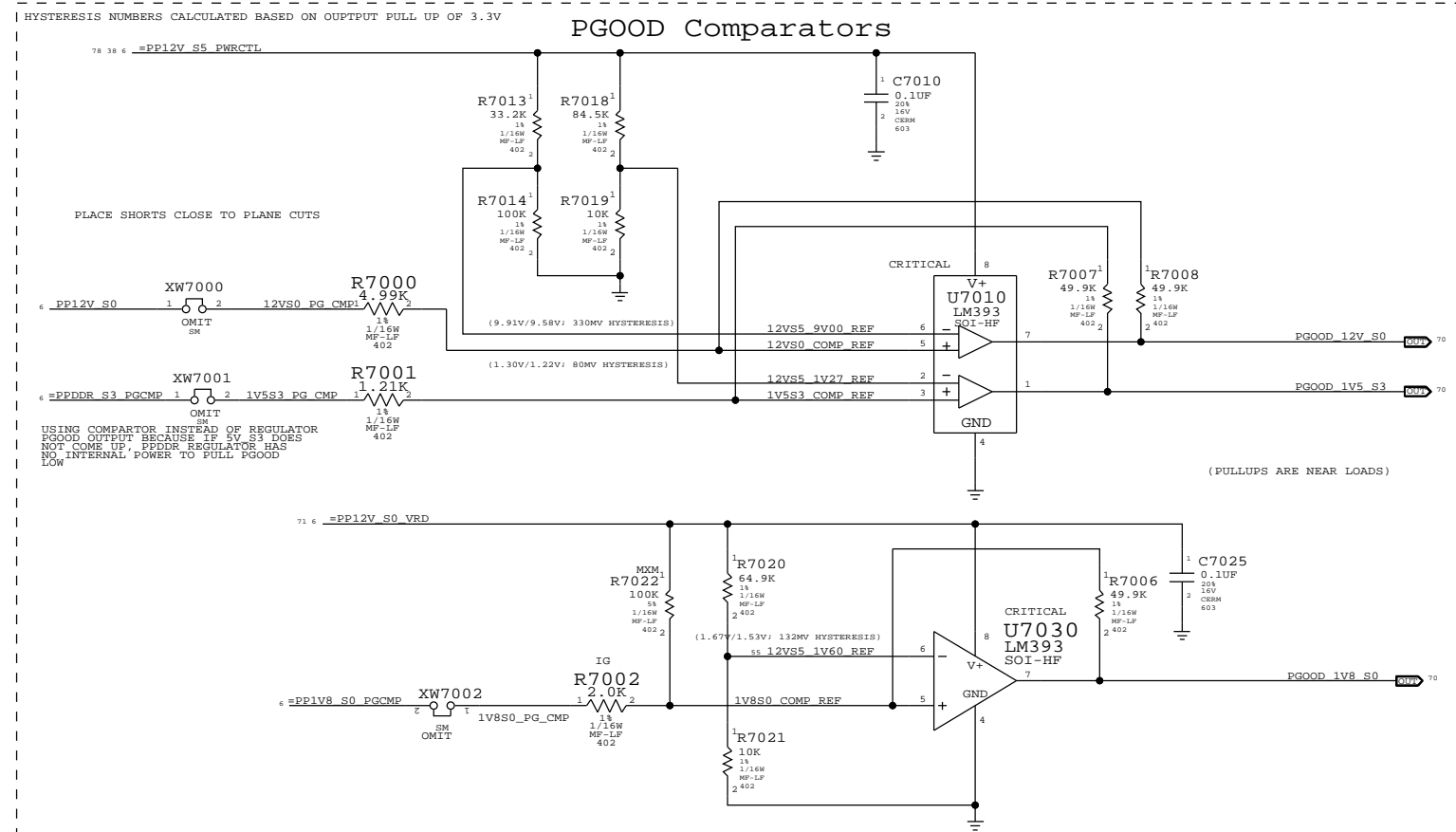


State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Def (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

MXM POWER SEQUENCE



MXM CARD INPUT POWER ARE 1.2V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD



Part	Value	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
PDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

SYNC MASTER=K22 SYNC DATE=09/02/2009

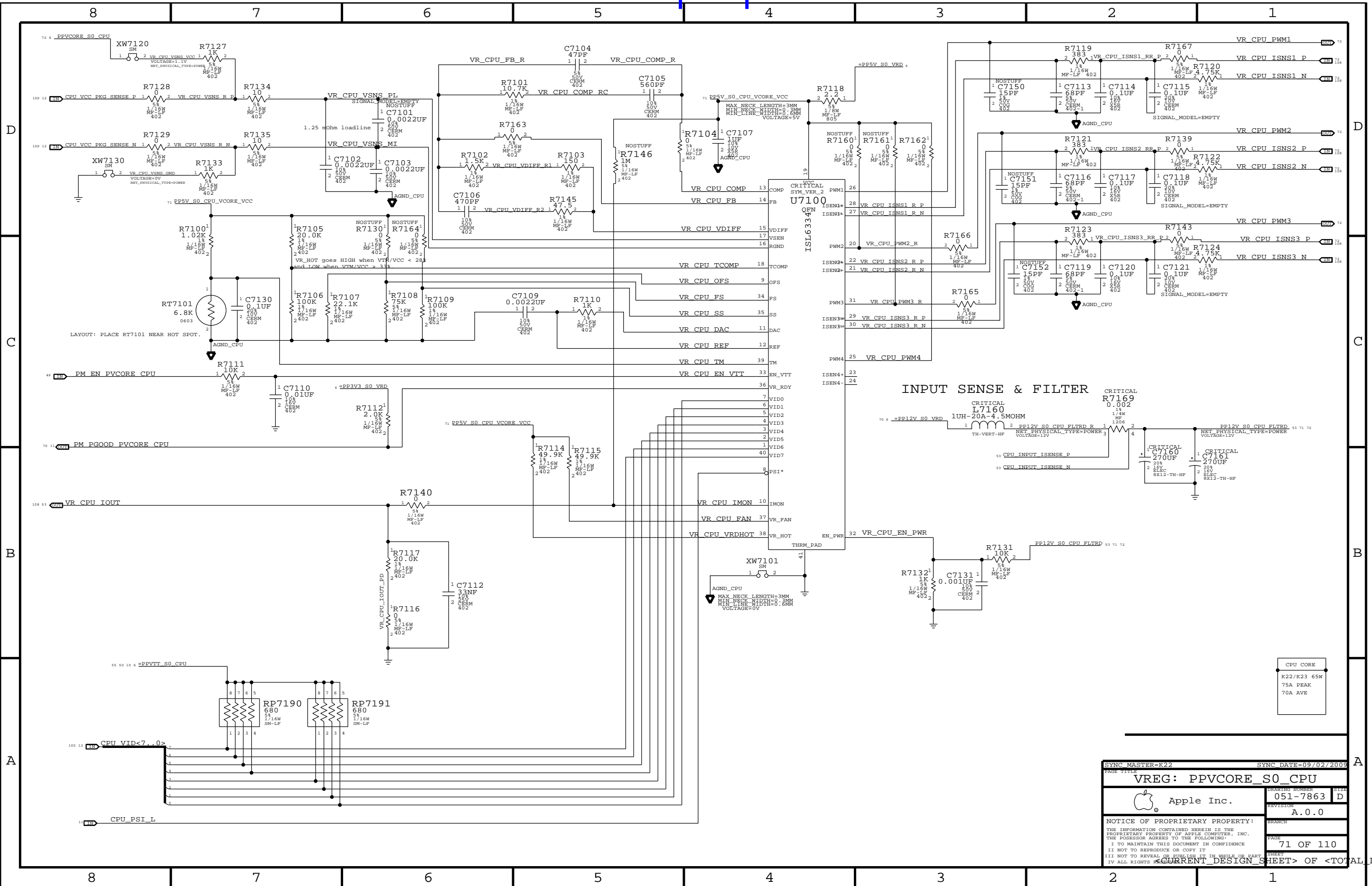
PGOOD and Power Sequencing

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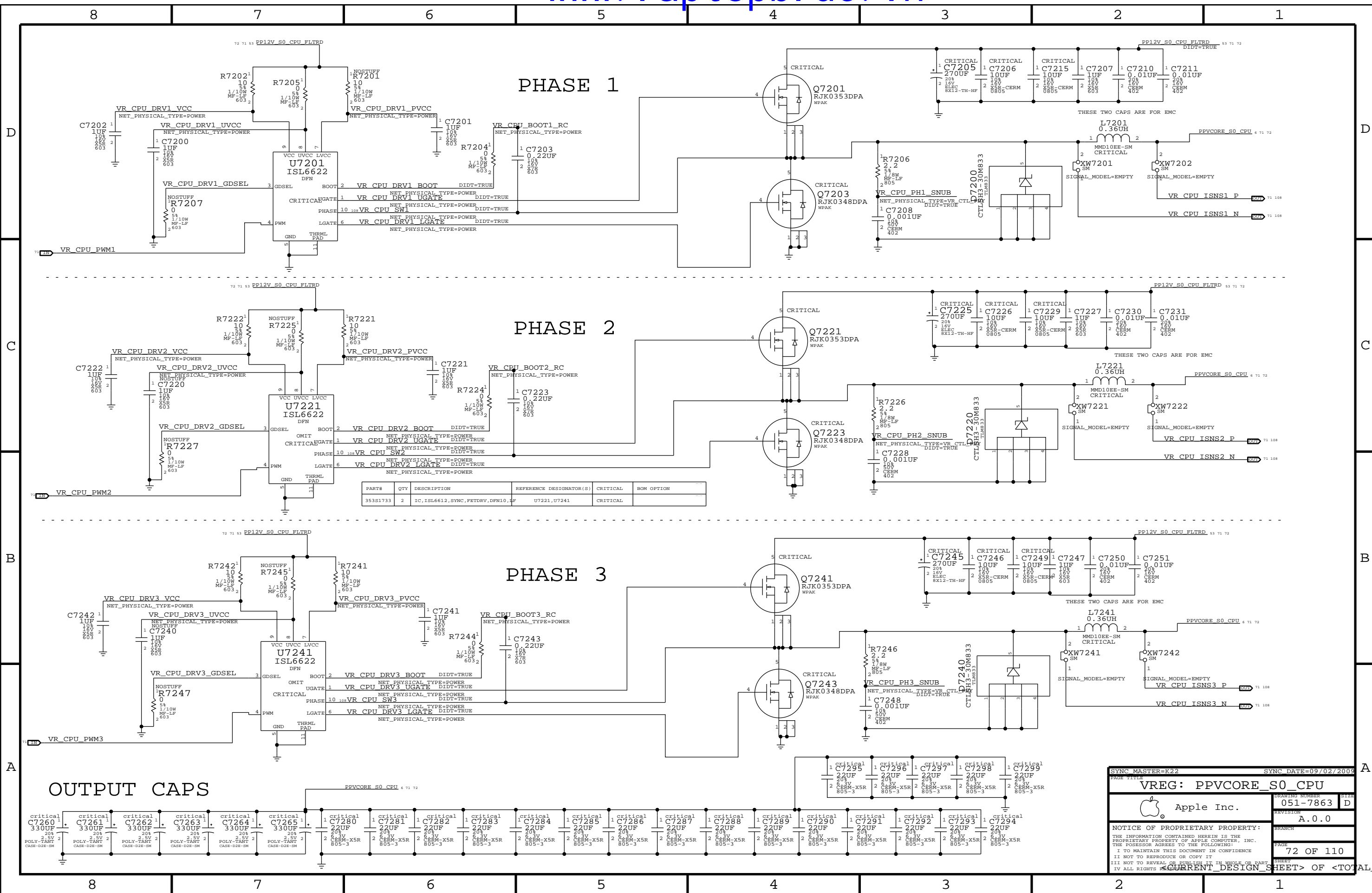
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ALL SYS_PWRGD IS ALSO AN INPUT TO THIS AND GATE BY THE FACT THAT PM_MXM_PGOOD IS PULLED UP TO IT



CPU CORE
K22/K23 65W
75A PEAK
70A AVE

SYNC MASTER=K22		SYNC DATE=09/02/2009	
PAGE TITLE VREG: PPVCORE_S0_CPU			
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35351733	2	IC, ISL6612, SYNC, FETDRV, DFN10, 4P	U7221, U7241	CRITICAL	

SYNC MASTER=K22 SYNC DATE=09/02/2009

VREG: PPVCORE_S0_CPU

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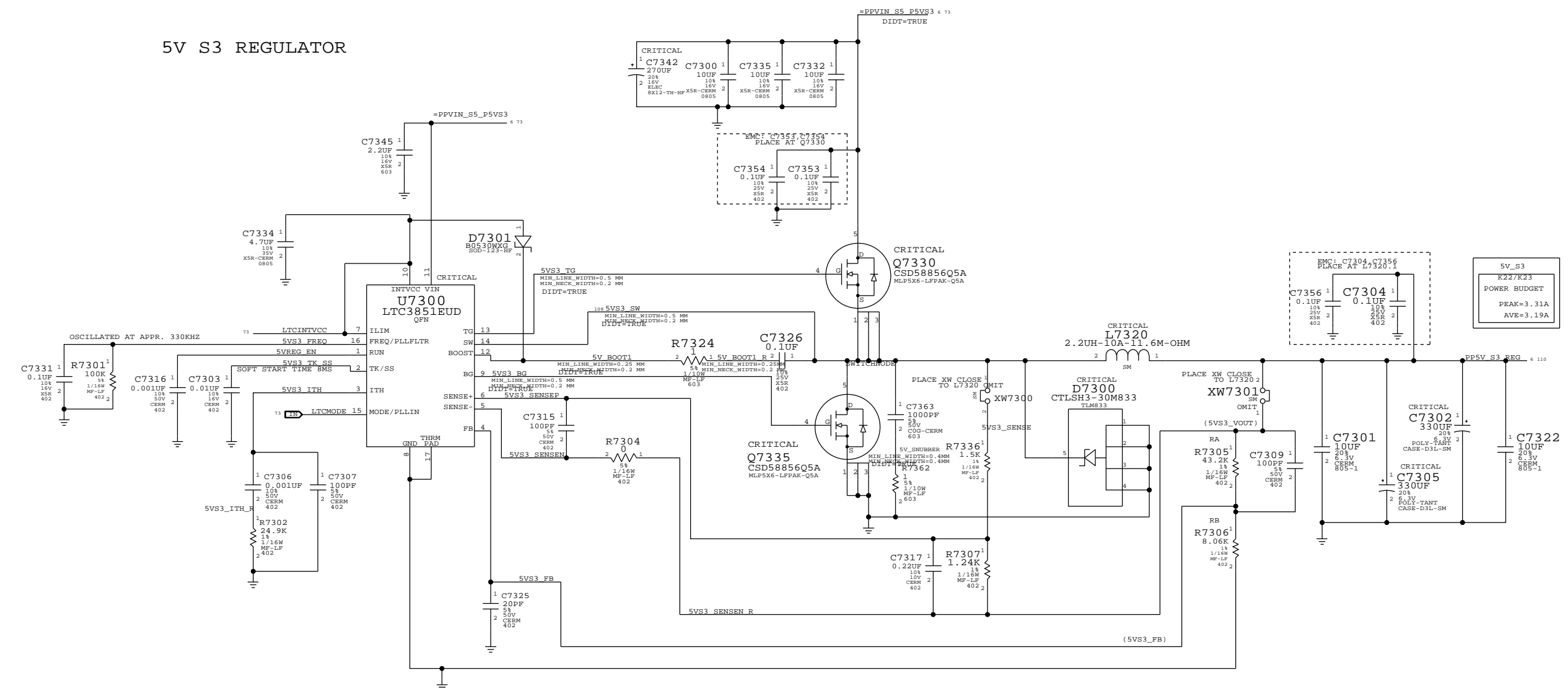
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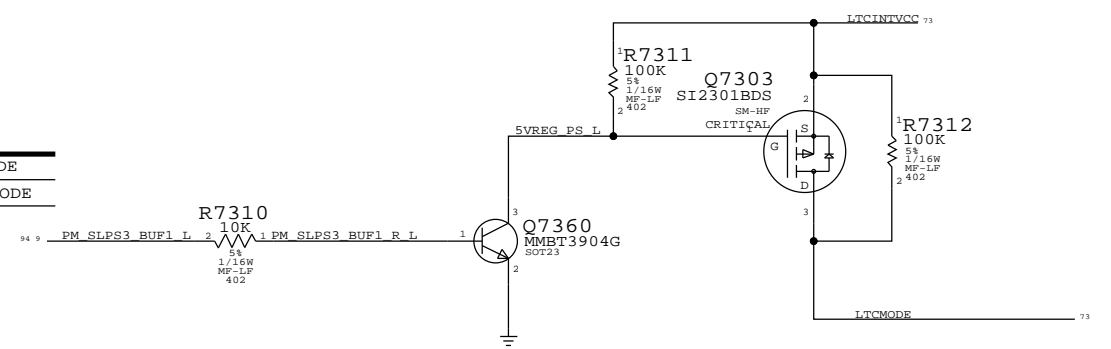
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5V S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE



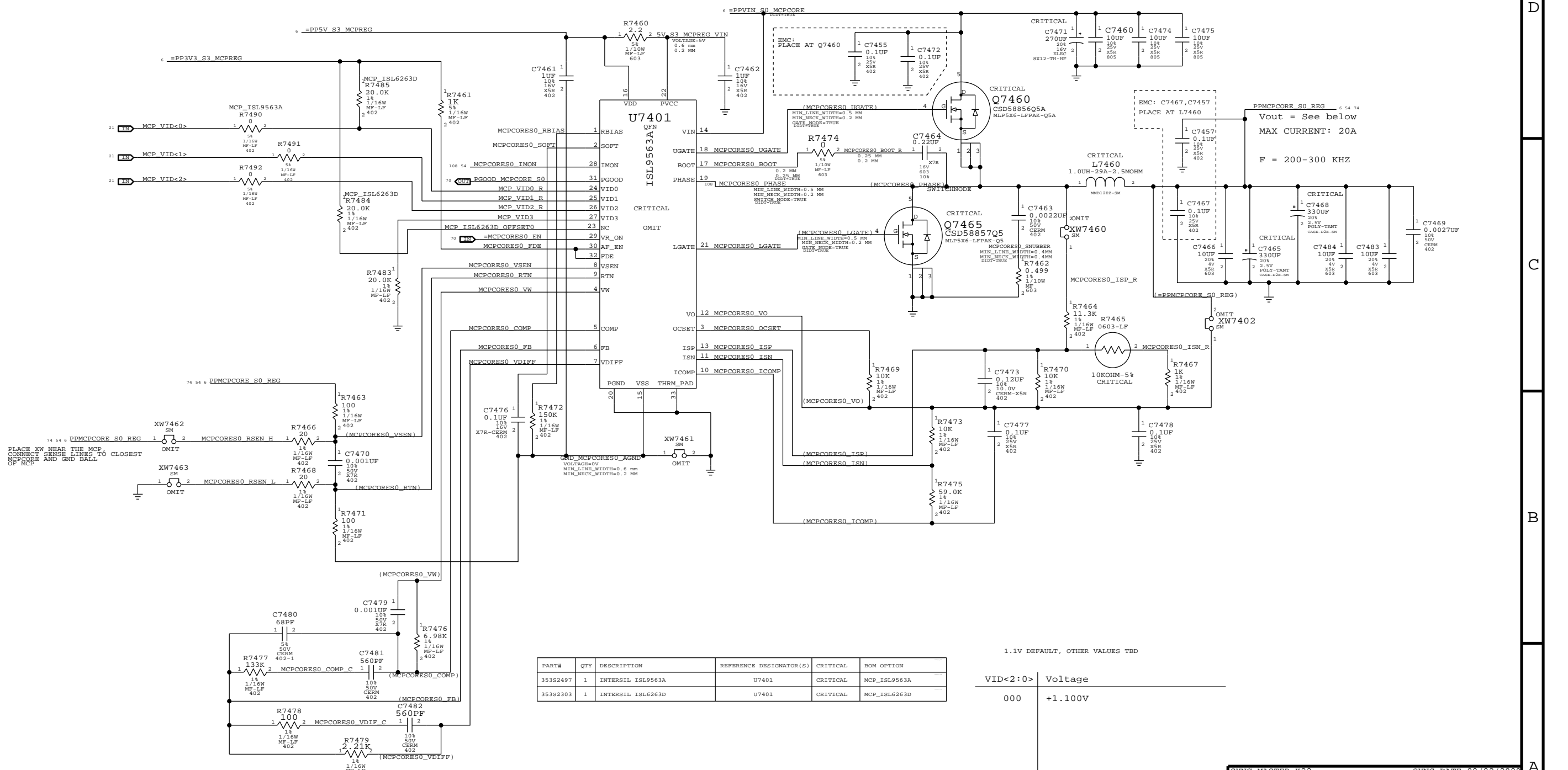
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5V_S3 REGULATOR	
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<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

MCP CORE



PARTS	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC MASTER=K22 SYNC DATE=09/02/2009

MCP CORE REGULATOR

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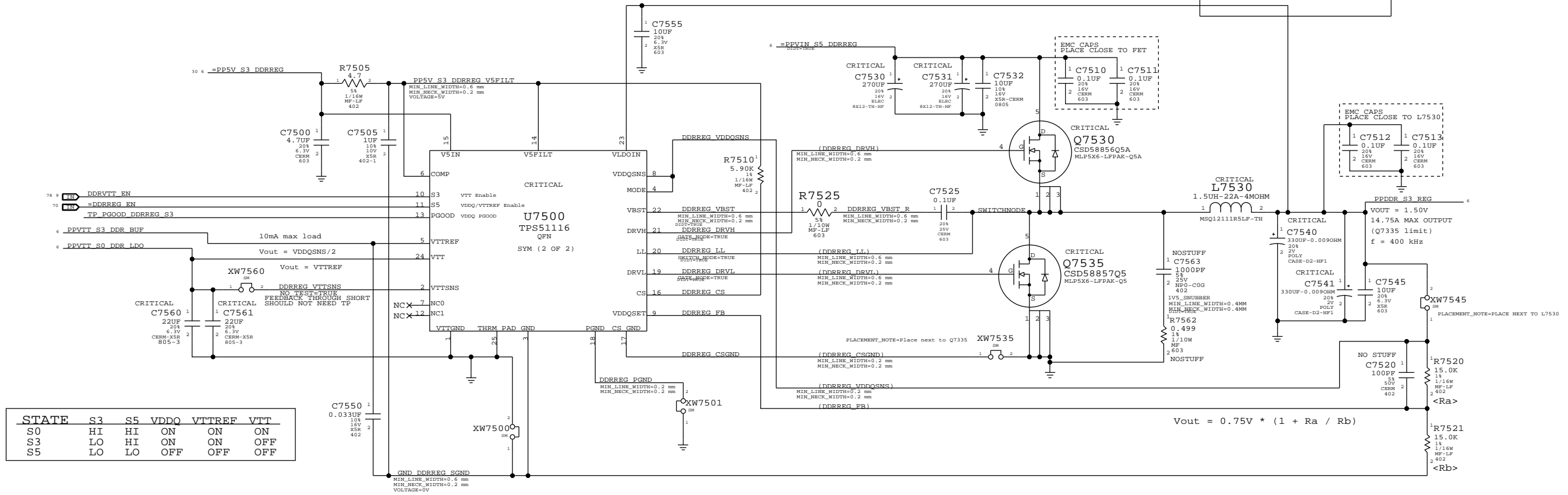
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1.5 V DDR SUPPLY

PPDDR_S3_REG
 VOUT = 1.5V
 PEAK = 11.28A
 AVG = 6.72A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC MASTER=K22 SYNC DATE=09/02/2009

1.5V DDR SUPPLY

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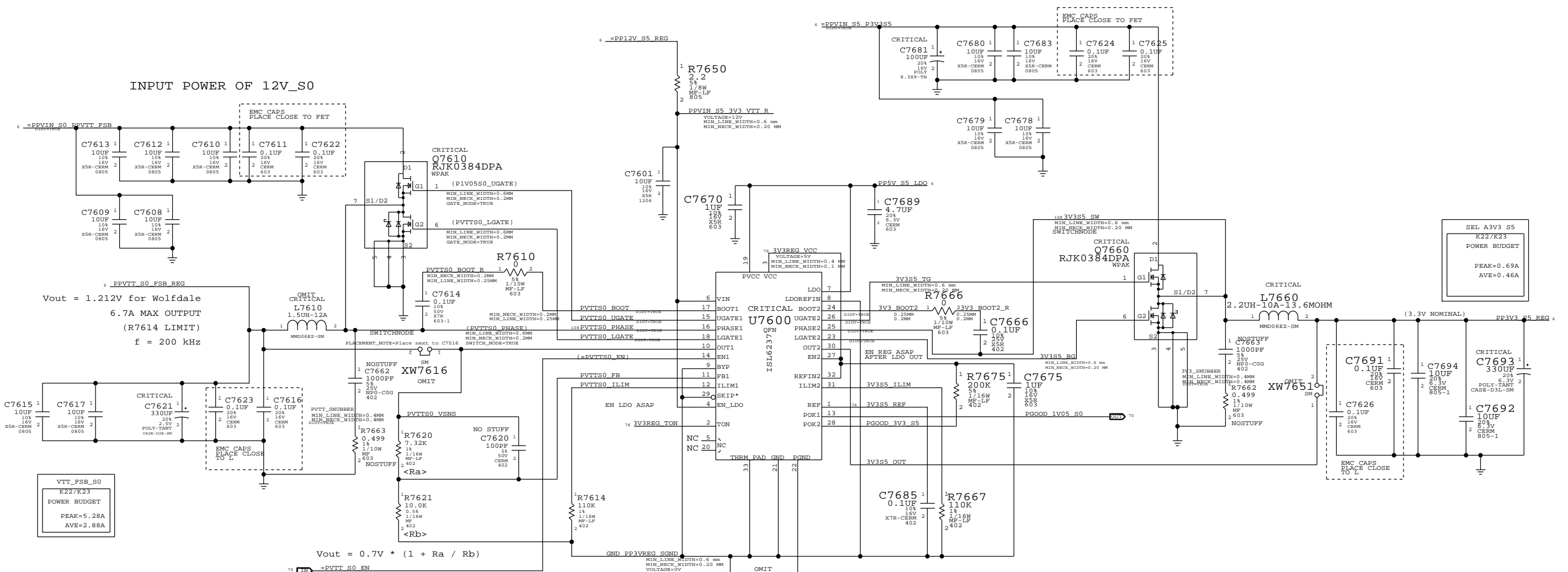
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FSB VTT AND 3.3V S5 RAILS

INPUT POWER OF 12V_S5

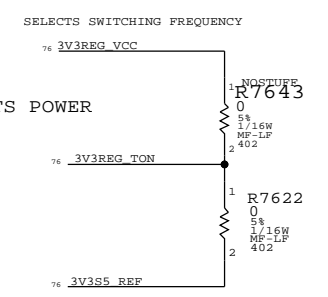
INPUT POWER OF 12V_S0



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15281078	1	IND, PWR, 1.5UH, 20A, 9A, 12mOHM	L7610	CRITICAL	

EN_LDO TIED TO 12V_S5 TO EN_LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
 EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
 TIED EXTERNALLY TO LDO_OUT, SO REGULATOR IS ENABLED
 AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY




SYNC MASTER=K22 SYNC DATE=09/02/2009

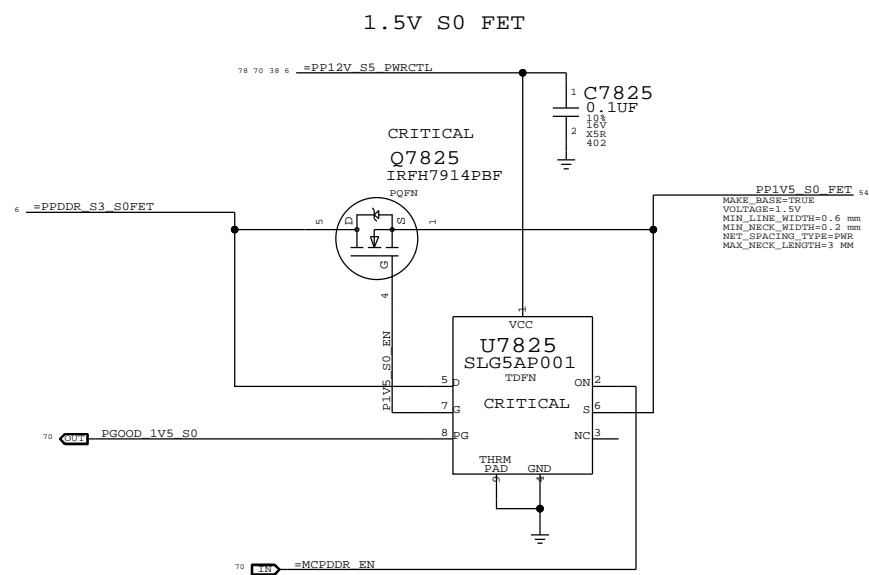
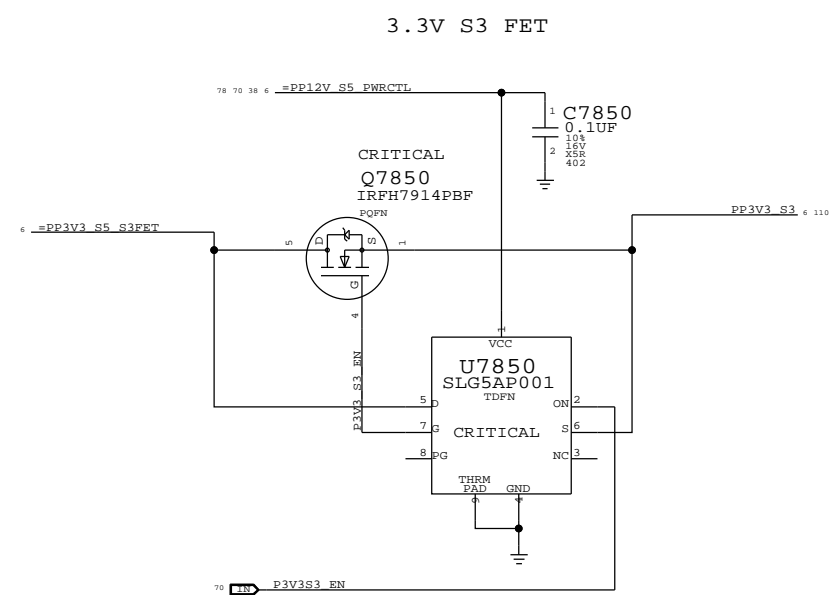
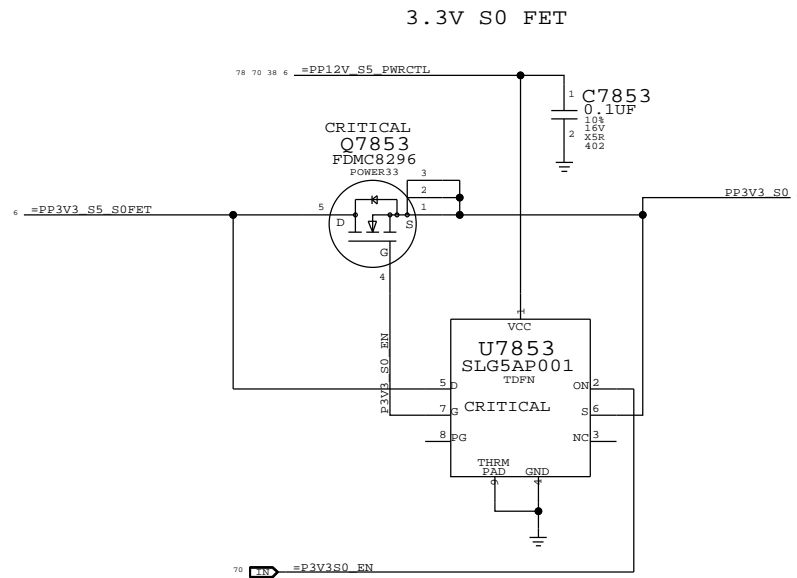
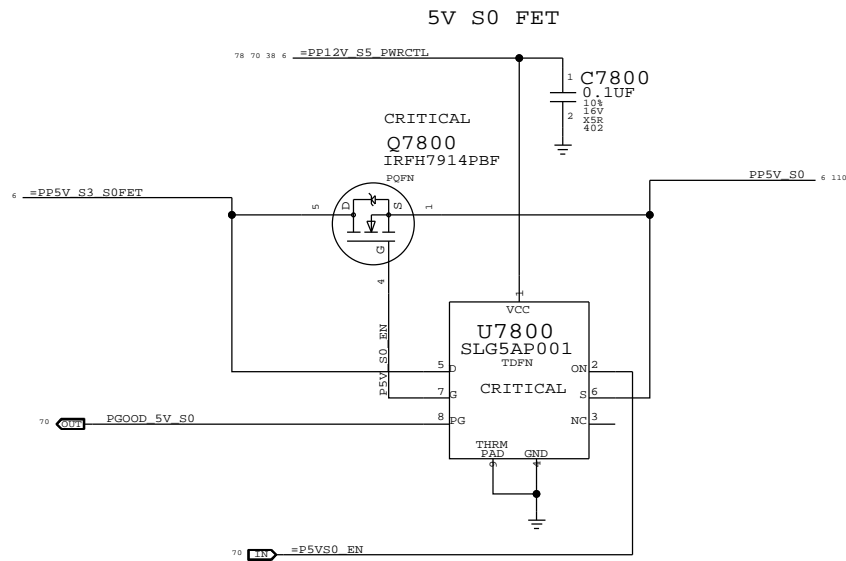
FSB VTT/3.3V S5 SUPPLIES

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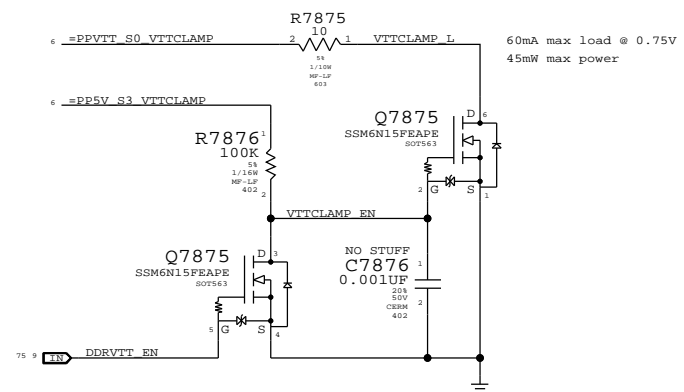
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 Apple Inc.	DRAWING NUMBER	051-7863	SIZE D
	REVISION	A.0.0	
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			PAGE 77 OF 110
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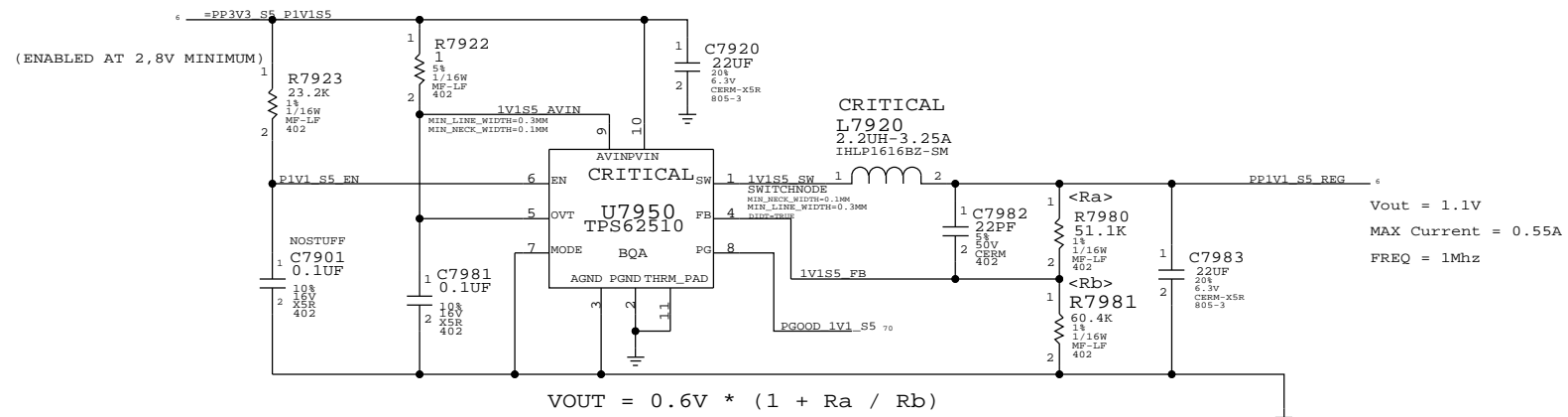
MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.




PAGE TITLE		SYNC MASTER=K22		SYNC DATE=09/02/2009	
S3 & S0 FETs					
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		PAGE	78 OF 110		

MCP 1.1V_S5 AUXC SUPPLY




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PAGE TITLE			
1V1 S5 POWER SUPPLY			
DRAWING NUMBER		REV	
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SHEET		PAGE	
79 OF 110		79 OF 110	
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		SHEET SHEET	


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		SHEET 82 OF 110	

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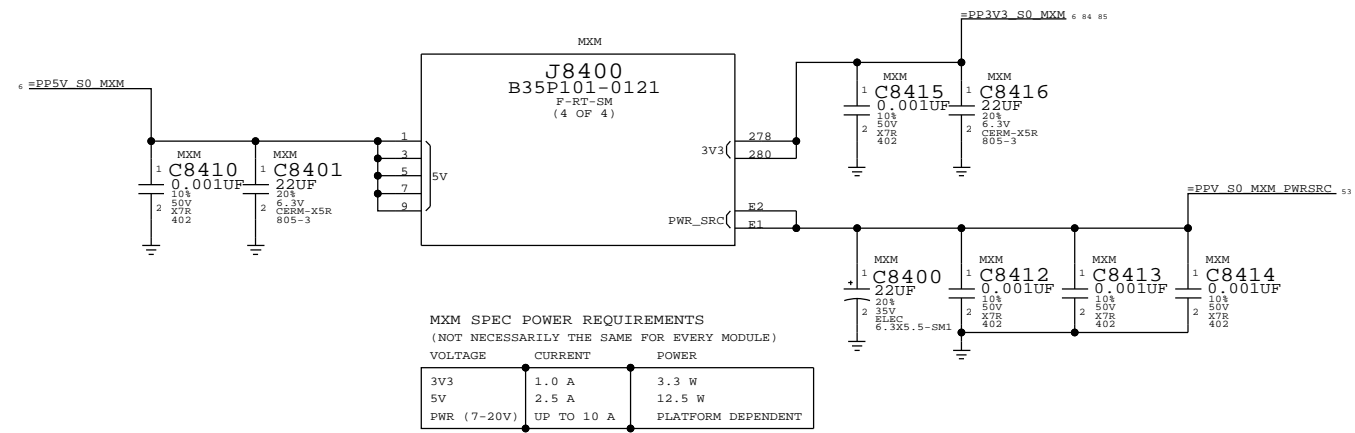
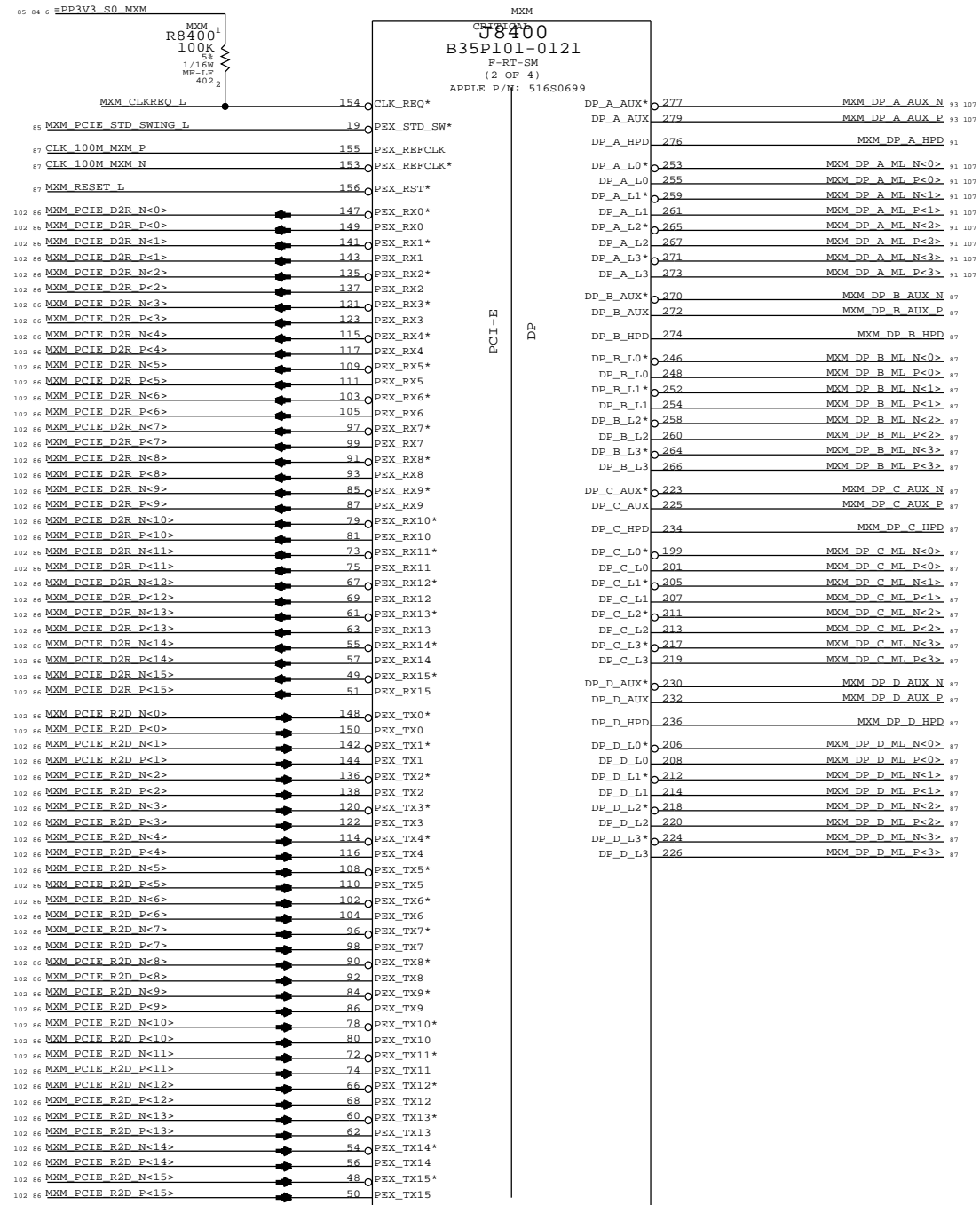
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		SHEET 83 OF 110	

Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM
 - =PP5V_S0_MXM
 - =PPV_S0_MXM_PWSRSC

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - MXM



MXM SPEC POWER REQUIREMENTS
 (NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K22 SYNC DATE=09/02/2009

MXM PCIe, DP & Power

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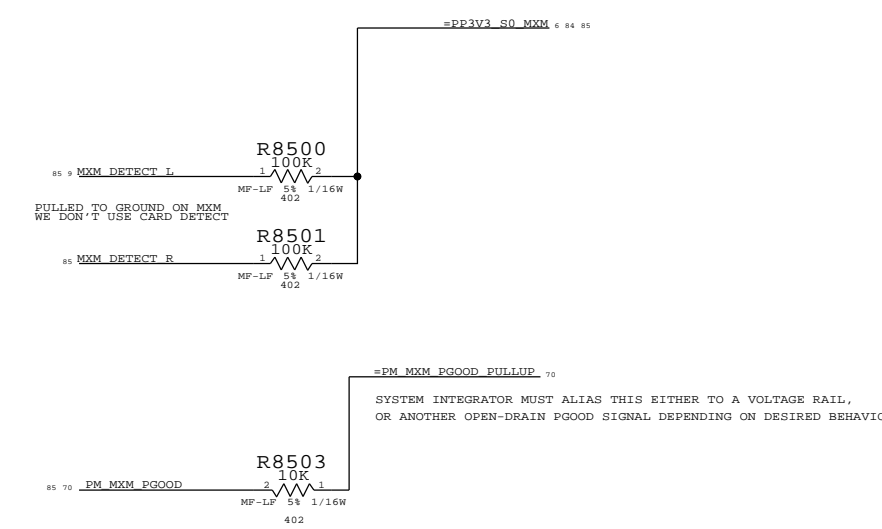
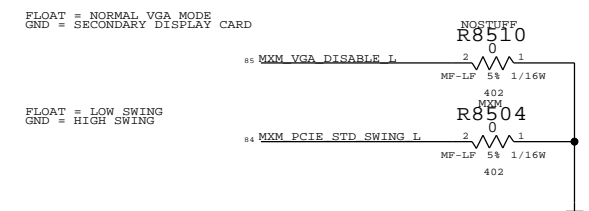
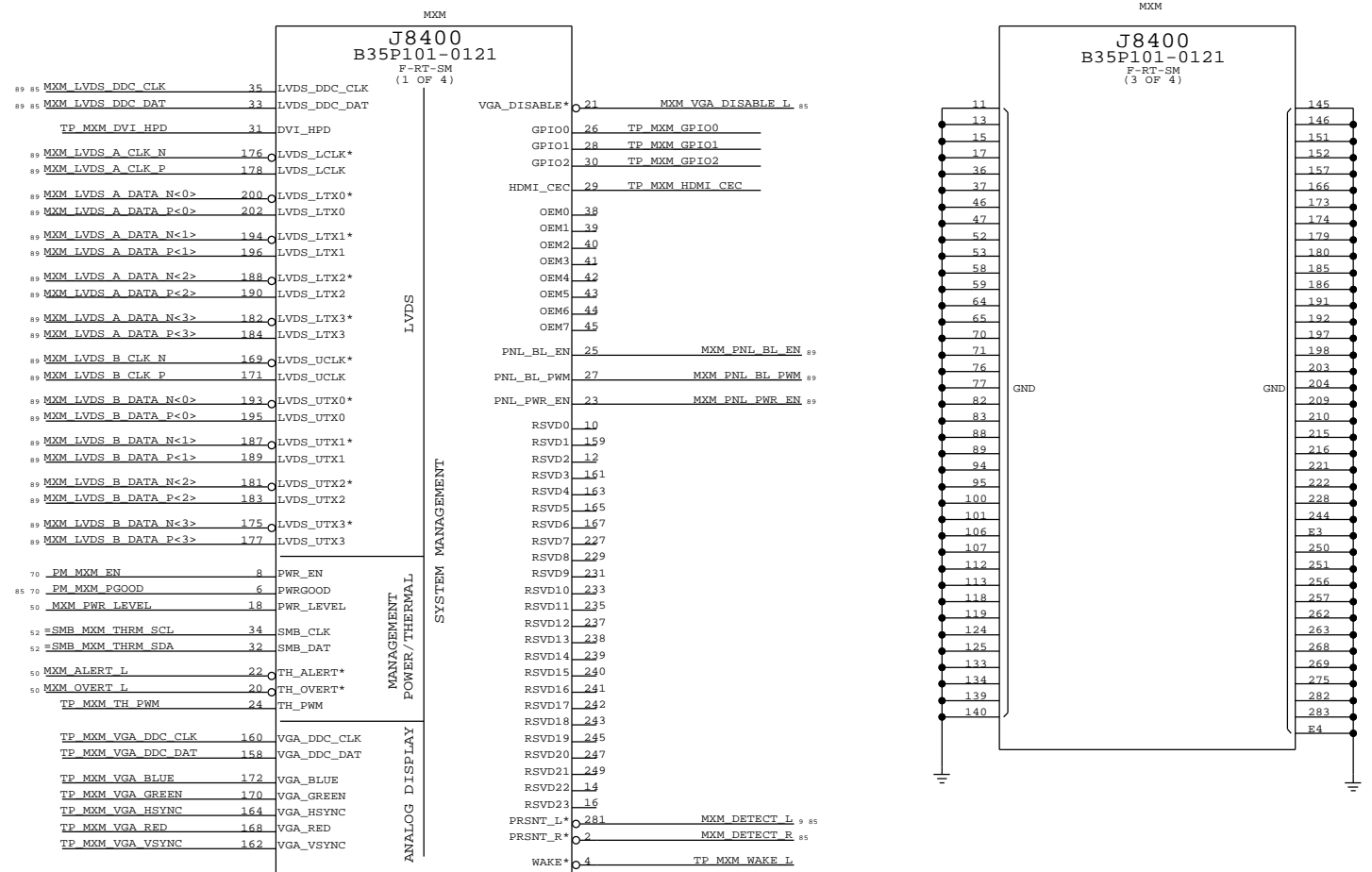
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 - =PP3V3_S0_MXM

Signal aliases required by this page:
 - =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
 - =SMB_MXM_THRM_CLK

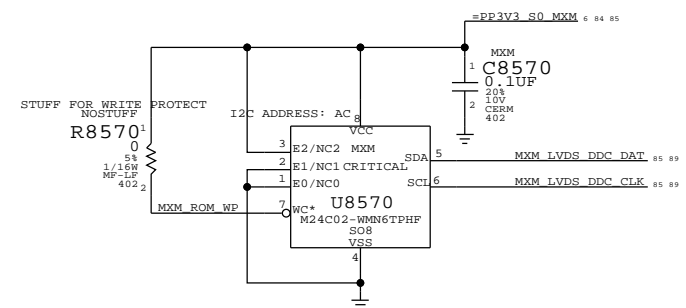
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



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PAGE TITLE: MXM I/O

DRAWING NUMBER: 051-7863 D

REVISION: A.0.0

BRANCH:

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SHEET:

MXM TX CAPS

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MXM RX CAPS

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PAGE TITLE

MXM PCIE CAPS

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Page Notes

Power aliases required by this page:
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Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

MCP Connections

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Unused MXM Interfaces

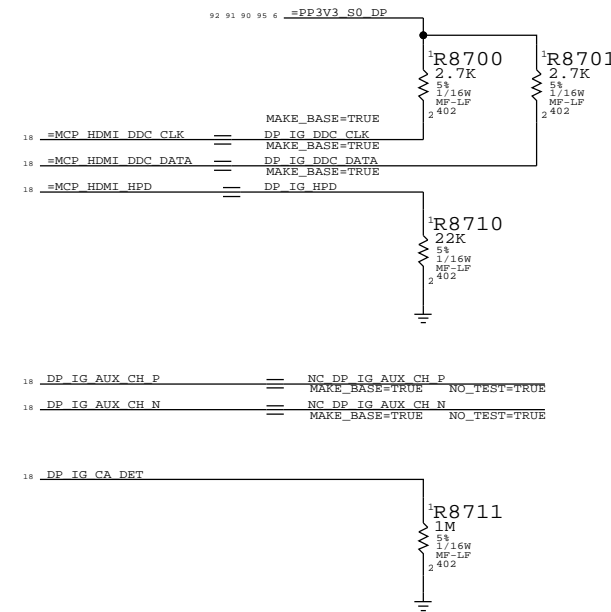
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85	MXM LVDS A DATA N<0>	==	NC MXM LVDS A DATA N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA P<0>	==	NC MXM LVDS A DATA P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA N<1>	==	NC MXM LVDS A DATA N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA P<1>	==	NC MXM LVDS A DATA P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA N<2>	==	NC MXM LVDS A DATA N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA P<2>	==	NC MXM LVDS A DATA P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA N<3>	==	NC MXM LVDS A DATA N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS A DATA P<3>	==	NC MXM LVDS A DATA P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B CLK N	==	NC MXM LVDS B CLK N	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B CLK P	==	NC MXM LVDS B CLK P	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA N<0>	==	NC MXM LVDS B DATA N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA P<0>	==	NC MXM LVDS B DATA P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA N<1>	==	NC MXM LVDS B DATA N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA P<1>	==	NC MXM LVDS B DATA P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA N<2>	==	NC MXM LVDS B DATA N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA P<2>	==	NC MXM LVDS B DATA P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA N<3>	==	NC MXM LVDS B DATA N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
85	MXM LVDS B DATA P<3>	==	NC MXM LVDS B DATA P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MXM DP Interfaces

84	MXM DP B MI P<0..3>	==	NC MXM DP B MI P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP B MI N<0..3>	==	NC MXM DP B MI N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP B AUX P	==	NC MXM DP B AUX P	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP B AUX N	==	NC MXM DP B AUX N	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP B HPD	==	NC MXM DP B HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP D MI P<0..3>	==	NC MXM DP D MI P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP D MI N<0..3>	==	NC MXM DP D MI N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP D AUX P	==	NC MXM DP D AUX P	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP D AUX N	==	NC MXM DP D AUX N	MAKE_BASE=TRUE	NO_TEST=TRUE
84	MXM DP D HPD	==	NC MXM DP D HPD	MAKE_BASE=TRUE	NO_TEST=TRUE


Unused MCP Interfaces

18	LVDS IG BKL ON	==	NC LVDS IG BKL ON	MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS IG BKL PWM	==	NC LVDS IG BKL PWM	MAKE_BASE=TRUE	NO_TEST=TRUE
18	LVDS IG PANEL PWR	==	NC LVDS IG PANEL PWR	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP HDMI TXD P<0..2>	==	NC MCP HDMI TXD P<0..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP HDMI TXD N<0..2>	==	NC MCP HDMI TXD N<0..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP HDMI TXC P	==	NC MCP HDMI TXC P	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP HDMI TXC N	==	NC MCP HDMI TXC N	MAKE_BASE=TRUE	NO_TEST=TRUE




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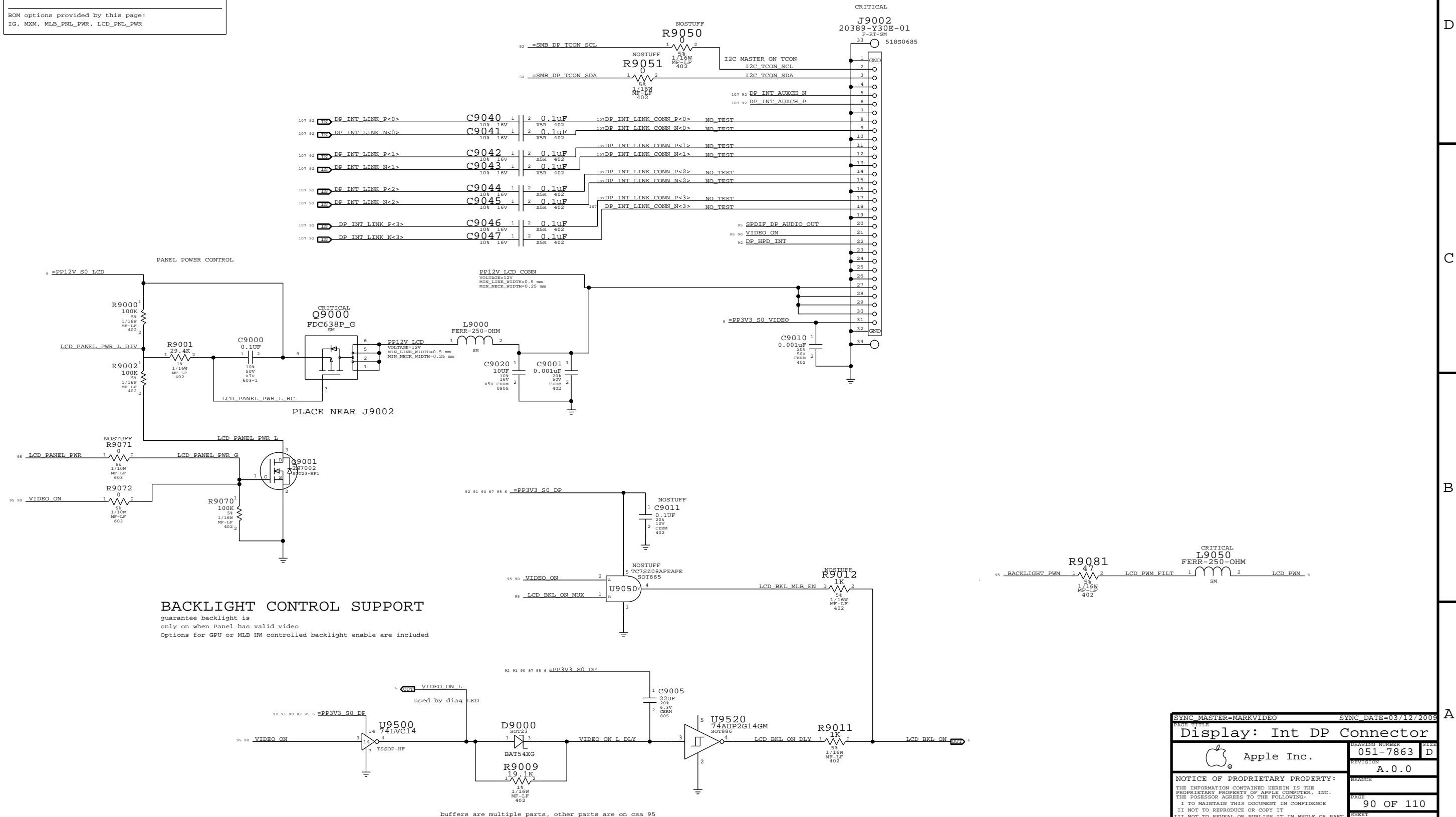
Page Notes

Power aliases required by this page:
 - =PP12V_S0_LCD
 - =PP3V3_S0_VIDEO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

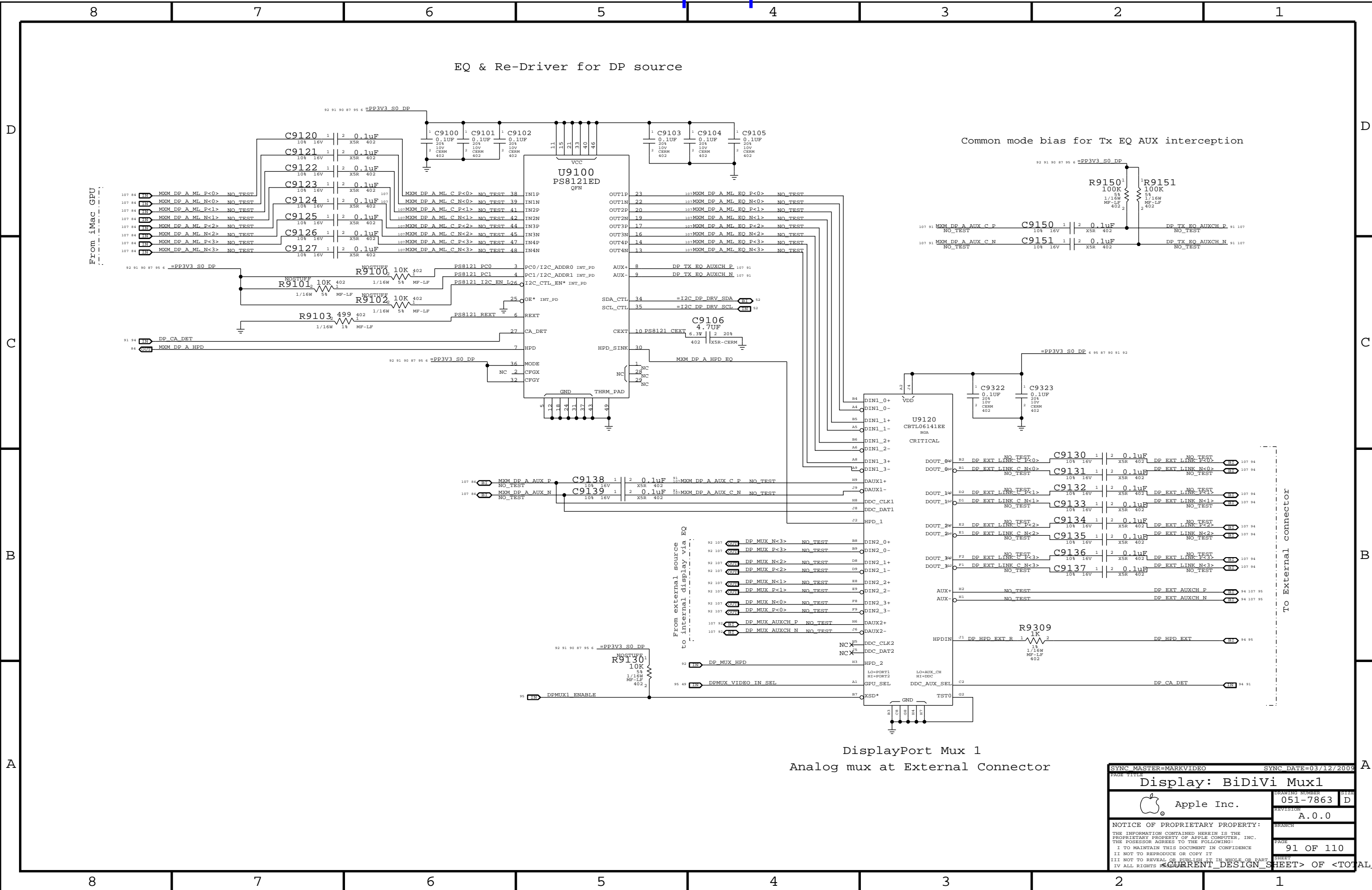


BACKLIGHT CONTROL SUPPORT

guarantee backlight is only on when Panel has valid video
 Options for GPU or MLB HW controlled backlight enable are included

buffers are multiple parts, other parts are on csa 95

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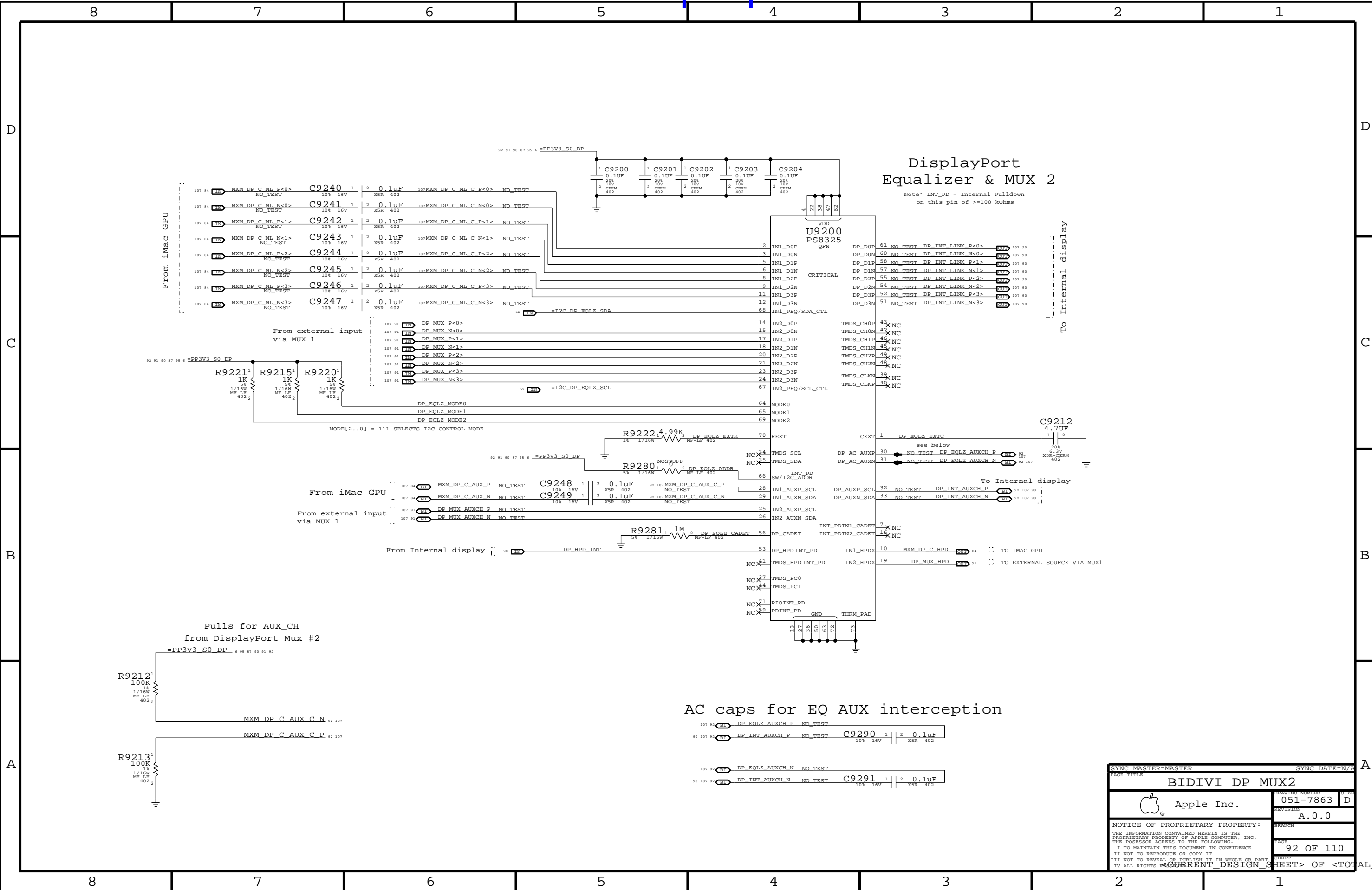


EQ & Re-Driver for DP source

Common mode bias for Tx EQ AUX interception

DisplayPort Mux 1
Analog mux at External Connector

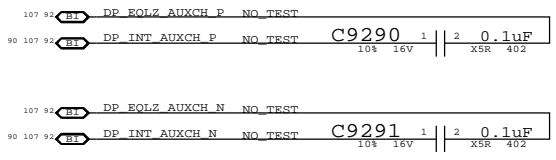
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DisplayPort Equalizer & MUX 2

Note: INT_PD = Internal Pulldown on this pin of >=100 kohms

AC caps for EQ AUX interception



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BIDIVI DP MUX2


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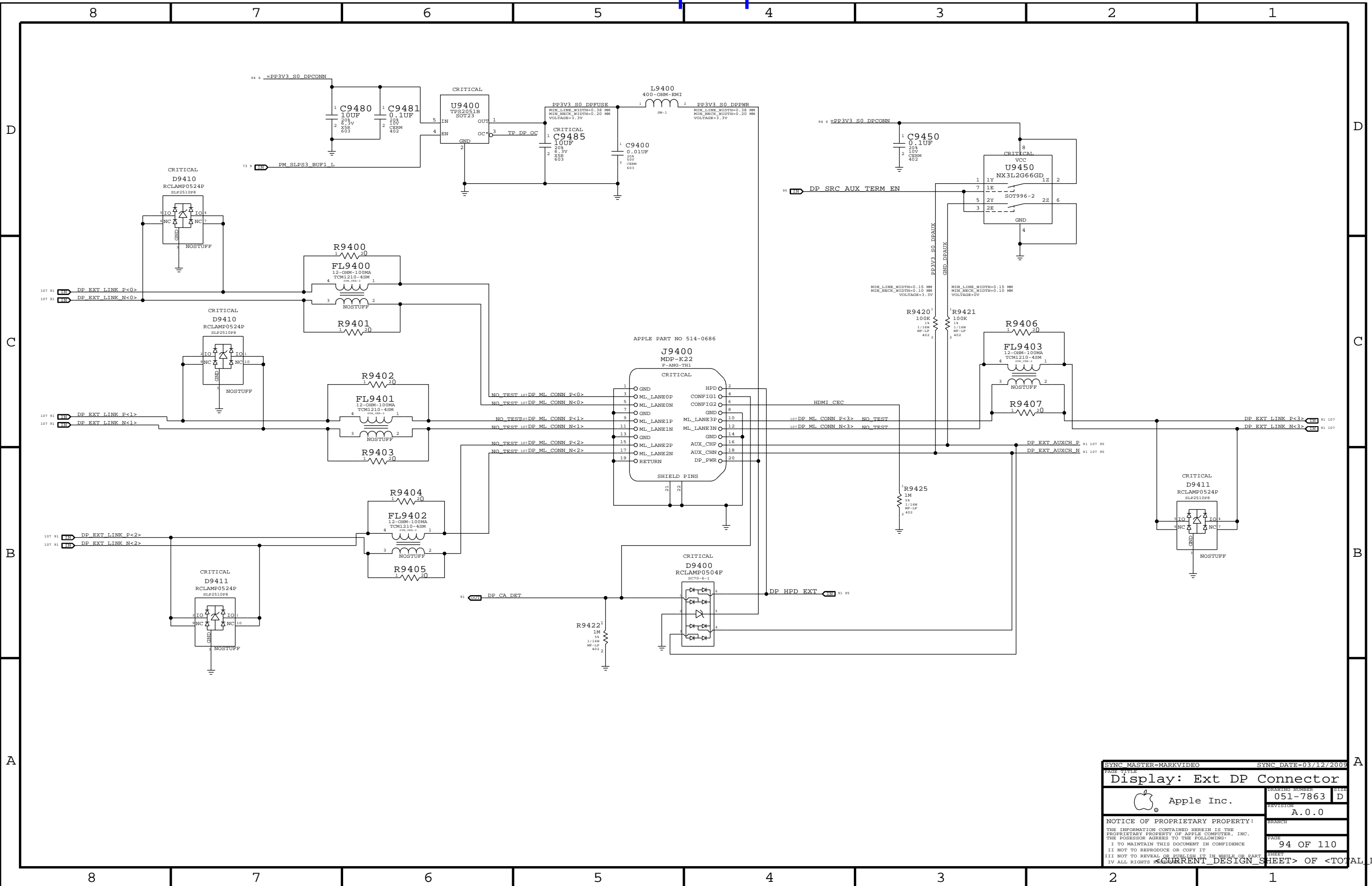
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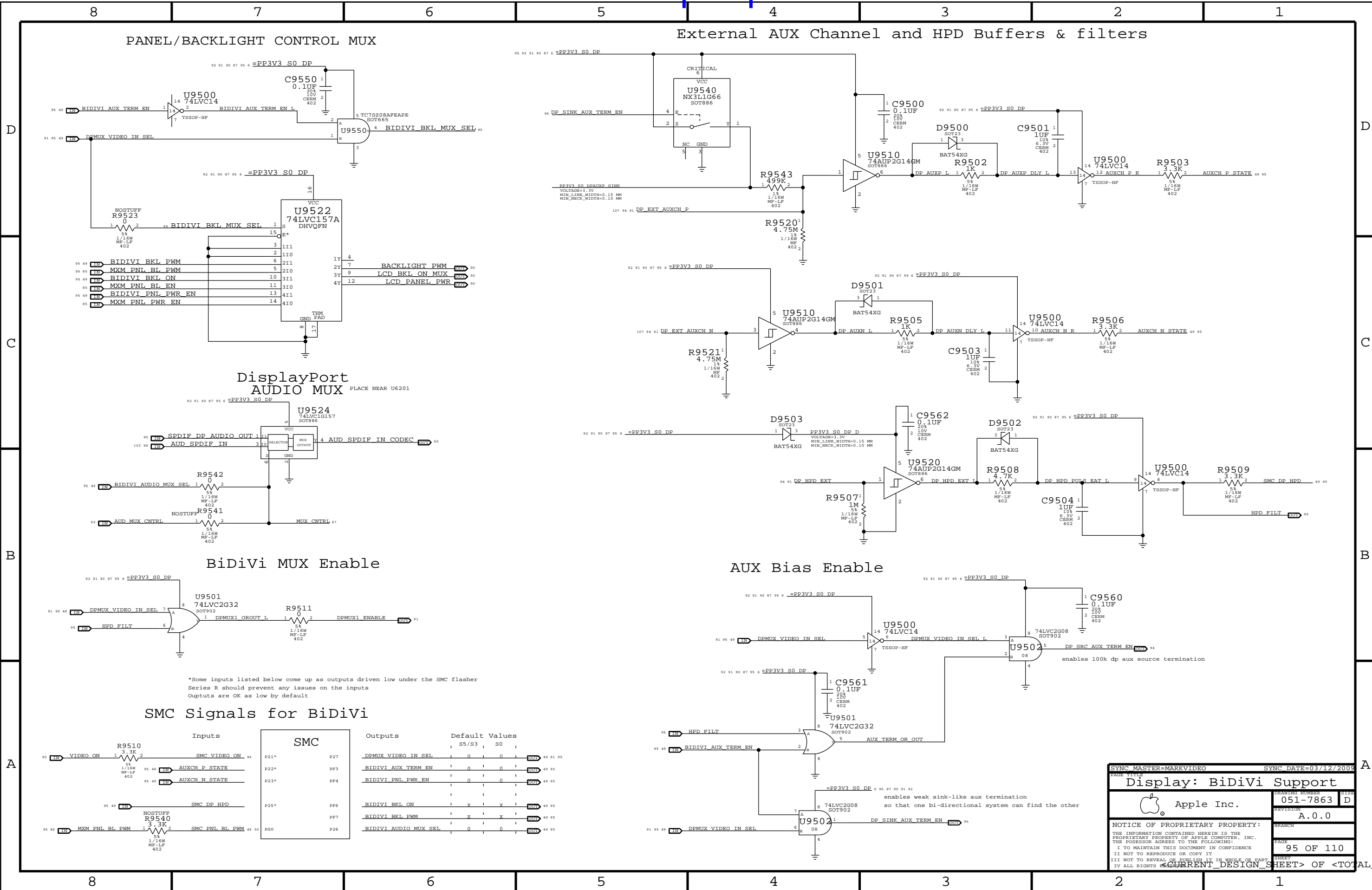
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PANEL/BACKLIGHT CONTROL MUX

External AUX Channel and HPD Buffers & filters

DisplayPort AUDIO MUX

BiDiVi MUX Enable

AUX Bias Enable

SMC Signals for BiDiVi

*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Outputs are OK as low by default


Inputs	SMC	Outputs	Default Values
VIDEO GN	P21*	DPMUX VIDEO IN SEL	0 0 0
AUXCH_P_STATE	P22*	BIDIVI AUX TERM EN	0 0 0
AUXCH_N_STATE	P23*	BIDIVI PNL PWR EN	0 0 0
SMC_DP_HPDP	P25*	BIDIVI BKL ON	x x x
SMC_PNL_BL_PWM	P26	BIDIVI BKL PWM	x x x
		BIDIVI AUDIO MUX SEL	0 0 0

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Display: BiDiVi Support


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FSB (Front-Side Bus) Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include FSB_50S, FSB_42S, FSB_DSTR_42S.

Two tables side-by-side for spacing rules. Left table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Right table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include FSB_DATA, FSB_DSTR, FSB_ADDR, FSB_ADSTR, FSB_1X.

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended. All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4x signals / groups shown in signal table on right. Signals within each 4x group should be matched within 5 ps of strobe. DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighter than MCP79) Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2x signals / groups shown in signal table on right. Signals within each 2x group should be matched within 20 ps. ADTBS#s should be matched +/- 300 ps. Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1x signals shown in signal table on right. Signals within each 1x group should be matched to CPU clock, +0/-1000 mils. Design Guide recommends each strobe/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened. SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2 SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include CPU_50S, CPU_27P4S.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Two tables side-by-side for CPU spacing rules. Left table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Right table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include CPU_AGTL, CPU_SMIL, CPU_COMP, CPU_GTLREF, CPU_ITP, CPU_VCCSENSE.

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED. Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2 SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes MCP_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes MCP_FSB_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes CLK_FSB_100D.

Two tables side-by-side for FSB clock spacing rules. Left table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Right table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes CLK_FSB.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

Large table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. It lists various signal groups (Group 0, Group 1, Group 2, Group 3) and individual signals like FSB_42S, FSB_50S, CPU_50S, CPU_27P4S, CLK_FSB_100D, MCP_50S, CPU_GTLREF, CPU_COMP, CPU_ITP, CPU_XDP_TDI, CPU_XDP_TDO, CPU_XDP_TMS, CPU_XDP_TCK, CPU_XDP_TRST_L, CPU_XDP_BFM_L<5..0>, CPU_XDP_BFMB<3..0>, XDP_CPUREST_L, CPU_VID<7..0>, CPU_VCCSENSE_P, CPU_VCCSENSE_N, VR_CPU_VSNS_E_P, VR_CPU_VSNS_E_N.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 5 ps of CLK pairs.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM A CLK P<1..0>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM A CLK N<1..0>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM A CLK P<4..3>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM A CLK N<4..3>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM A CKE<3..0>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM A CS I<3..0>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM A ODT<3..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM A A<14..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM A BA<2..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM A RAS L
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM A CAS L
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM A WE L
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<7..0>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<0>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<15..8>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<1>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<23..16>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<2>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<31..24>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<3>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<39..32>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<4>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<47..40>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<5>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<55..48>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<6>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DQ<63..56>
MEM_40S	MEM_DATA	MEM_DATA	MEM A DM<7>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<0>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<0>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<1>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<1>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<2>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<2>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<3>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<3>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<4>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<4>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<5>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<5>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<6>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<6>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS P<7>
MEM_70D	MEM_DQS	MEM_DQS	MEM A DQS N<7>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM B CLK P<1..0>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM B CLK N<1..0>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM B CLK P<4..3>
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM B CLK N<4..3>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM B CKE<3..0>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM B CS I<3..0>
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM B ODT<3..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM B A<14..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM B BA<2..0>
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM B RAS L
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM B CAS L
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM B WE L
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<7..0>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<0>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<15..8>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<1>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<23..16>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<2>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<31..24>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<3>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<39..32>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<4>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<47..40>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<5>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<55..48>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<6>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DQ<63..56>
MEM_40S	MEM_DATA	MEM_DATA	MEM B DM<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<0>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<0>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<1>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<1>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<2>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<2>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<3>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<3>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<4>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<4>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<5>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<5>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<6>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<6>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS P<7>
MEM_70D	MEM_DQS	MEM_DQS	MEM B DQS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

SYNC MASTER=K22 SYNC DATE=09/02/2009

Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?				
MCP_PEX_COMP	*	0.2 MM	?				

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?	SATA	TOP,BOTTOM	=3X_DIELECTRIC	?
SATA_TERM	*	0.2 MM	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCIe GRAPHICS				
	PCIE_90D	PCIE	PEG R2D C P<15..0>	9 86
	PCIE_90D	PCIE	PEG R2D C N<15..0>	9 86
	PCIE_90D	PCIE	PEG D2R P<15..0>	9 86
	PCIE_90D	PCIE	PEG D2R N<15..0>	9 86
	PCIE_90D	PCIE	MMX PCIE R2D P<15..0>	84 86
	PCIE_90D	PCIE	MMX PCIE R2D N<15..0>	84 86
	PCIE_90D	PCIE	MMX PCIE D2R P<15..0>	84 86
	PCIE_90D	PCIE	MMX PCIE D2R N<15..0>	84 86
PCIe I/O				
	PCIE_90D	PCIE	PCIE MINI R2D P	34
	PCIE_90D	PCIE	PCIE MINI R2D N	34
	PCIE_90D	PCIE	PCIE MINI R2D C P	17 34
	PCIE_90D	PCIE	PCIE MINI R2D C N	17 34
	PCIE_90D	PCIE	PCIE MINI R2D L P	34
	PCIE_90D	PCIE	PCIE MINI R2D L N	34
	PCIE_90D	PCIE	PCIE MINI D2R P	17 34
	PCIE_90D	PCIE	PCIE MINI D2R N	17 34
	PCIE_90D	PCIE	PCIE FW R2D P	41
	PCIE_90D	PCIE	PCIE FW R2D N	41
	PCIE_90D	PCIE	PCIE FW R2D C P	17 41
	PCIE_90D	PCIE	PCIE FW R2D C N	17 41
	PCIE_90D	PCIE	PCIE FW D2R P	17 41
	PCIE_90D	PCIE	PCIE FW D2R N	17 41
	PCIE_90D	PCIE	PCIE FW D2R C P	41
	PCIE_90D	PCIE	PCIE FW D2R C N	41
PCIe REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU CLK100M PCIE P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU CLK100M PCIE N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CON P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CON N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N	17 41
SATA				
	SATA_100D	SATA	SATA HDD R2D C P	20 45
	SATA_100D	SATA	SATA HDD R2D C N	20 45
	SATA_100D	SATA	SATA HDD R2D P	45 110
	SATA_100D	SATA	SATA HDD R2D N	45 110
	SATA_100D	SATA	SATA HDD D2R P	20 45
	SATA_100D	SATA	SATA HDD D2R N	20 45
	SATA_100D	SATA	SATA HDD D2R C P	45 110
	SATA_100D	SATA	SATA HDD D2R C N	45 110
	SATA_100D	SATA	SATA ODD R2D C P	20 45
	SATA_100D	SATA	SATA ODD R2D C N	20 45
	SATA_100D	SATA	SATA ODD R2D P	45 110
	SATA_100D	SATA	SATA ODD R2D N	45 110
	SATA_100D	SATA	SATA ODD D2R P	20 45
	SATA_100D	SATA	SATA ODD D2R N	20 45
	SATA_100D	SATA	SATA ODD D2R C P	45 110
	SATA_100D	SATA	SATA ODD D2R C N	45 110
	MCP_50G	SATA_TERM	MCP SATA TERM	20
MISC				
	MCP_50G	MCP_PEX_COMP	MCP PEX CLK COMP	17
	MCP_PEX_COMP	MCP_PEX_COMP	MCP IFPAB RSET	18 26
	MCP_50G	MCP_PEX_COMP	MCP IFPAB VPROBE	18 26
			PM SLP S3 L	9 21
			PM SLP S4 L	21 70

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MCP Constraints 1

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
			PCI REQ0 L	19
			PCI REQ1 L	19
			PCI_CLK33M MCP_R	19
			PCI_CLK33M MCP	19
			LPC AD<3..0>	19 49 51
			LPC AD R<3..0>	19
			LPC FRAME L	19 49 51
			LPC FRAME R L	19
			LPC RESET L	9 19
			LPC_CLK33M SMC_R	9 19
			LPC_CLK33M SMC	9 49
			LPC_CLK33M LPCPLUS	9 51
			PM_CLK32K SUSCLK_R	9 21
			PM_CLK32K SUSCLK	9 49
			MCP_USB_RBIAS	20
			MCP_USB_RBIAS_GND	20
			USB_EXT_A_P	20 46
			USB_EXT_A_N	20 46
			USB_PORT0_P	46
			USB_PORT0_N	46
			USB_EXT_B_P	20 46
			USB_EXT_B_N	20 46
			USB_PORT1_P	46
			USB_PORT1_N	46
			USB_EXT_C_P	20 46
			USB_EXT_C_N	20 46
			USB_PORT2_P	46
			USB_PORT2_N	46
			USB_EXT_D_P	20 46
			USB_EXT_D_N	20 46
			USB_D_MIXED_P	46
			USB_D_MIXED_N	46
			USB_PORT3_P	46
			USB_PORT3_N	46
			USB_CAMERA_P	20 47
			USB_CAMERA_N	20 47
			USB_CAMERA_L_P	47 110
			USB_CAMERA_L_N	47 110
			USB_BT_P	20 47
			USB_BT_N	20 47
			USB_BT_L_P	47 110
			USB_BT_L_N	47 110
			USB_IR_P	20 47
			USB_IR_N	20 47
			USB_IR_L_P	47 110
			USB_IR_L_N	47 110
			USB_SDCARD_P	20 47
			USB_SDCARD_N	20 47
			USB_SDCARD_L_P	47 110
			USB_SDCARD_L_N	47 110
			SPI_CLK_R	21 51 61
			SPI_CLK	61
			SPI_MOSI_R	21 51 61
			SPI_MOSI	61
			SPI_MISO	21 51 61
			SPI_MISO_R	61
			SPI_CS0_R_L	21 51
			SPI_CS0_L	51
			HDA_BIT_CLK	21 62
			MCP_HDA_PULLDN_COMP	21
			HDA_BIT_CLK_R	21
			HDA_RST_L	21 62
			HDA_RST_R_L	21
			HDA_SDOUT	21 62
			HDA_SDOUT_R	21
			HDA_SYNC	21 62
			HDA_SYNC_R	21
			HDA_SDIN0	21 62
			AUD_SDI_R	62
			AUD_SPDIF_IN	6 66
			AUD_SPDIF_OUT	62 66
			AUD_SPDIF_CHIP	62
			MCP_CLK25M_XTALOUT	21 28
			MCP_CLK25M_XTALIN	21 28
			RTC_CLK32K_XTALOUT	21 28
			RTC_CLK32K_XTALIN	21 28

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
	MCP_MII_COMP		MCP_MII_COMP_GND 18
ENET_MII_558	MCP_BUF0_CLK		MCP_CLK25M_BUF0_R 18 38
	MCP_BUF0_CLK		RTL8211_CLK25M_CKXTAL1 37 38
ENET_MII_558	ENET_MII		ENET_MDIO 18 37
	ENET_MII		ENET_MDC 18 37
ENET_MII_558	ENET_MII		ENET_CLK125M_RXCLK 18 37
	ENET_MII		ENET_CLK125M_RXCLK_R 37
ENET_MII_558	ENET_MII		ENET_RXD<0> 18 37
	ENET_MII		ENET_RXD_R<0> 37
ENET_MII_558	ENET_MII		ENET_RXD<3..1> 18 37
	ENET_MII		ENET_RXD_R<3..1> 37
ENET_MII_558	ENET_MII		ENET_RX_CTRL 18 37
	ENET_MII		ENET_RXCTL_R 37
ENET_MII_558	ENET_MII		ENET_CLK125M_TXCLK 18 37
	ENET_MII		ENET_TXD<0> 18 37
ENET_MII_558	ENET_MII		ENET_TXD<3..1> 18 37
	ENET_MII		ENET_TX_CTRL 18 37
ENET_MDI_100D	ENET_MDI		ENET_MDI_P<3..0> 37 39
	ENET_MDI		ENET_MDI_N<3..0> 37 39
ENET_MDI_100D	ENET_MDI		ENET_MDI_T_P<3..0> 39
	ENET_MDI		ENET_MDI_T_N<3..0> 39

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Ethernet Constraints

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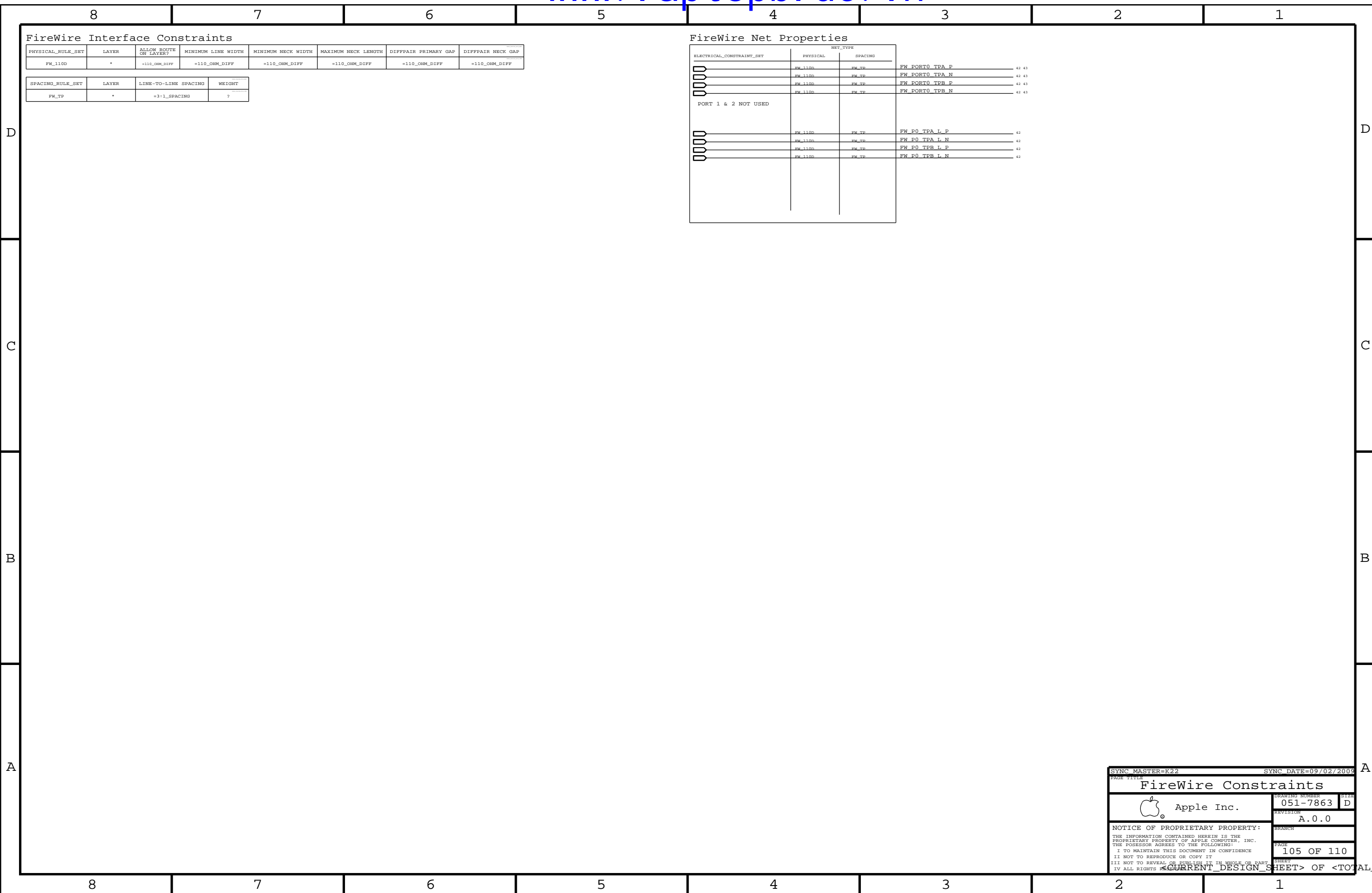
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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	FW_110D	FW_TP	FW_PORT0_TPA_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPA_N	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_N	42 43
	PORT 1 & 2 NOT USED			
	FW_110D	FW_TP	FW_P0_TPA_L_P	42
	FW_110D	FW_TP	FW_P0_TPA_L_N	42
	FW_110D	FW_TP	FW_P0_TPB_L_P	42
	FW_110D	FW_TP	FW_P0_TPB_L_N	42

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FireWire Constraints

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SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	smb_558	smb	SMBUS SMC A S3_SCL 52
	smb_558	smb	SMBUS SMC A S3_SDA 52
	smb_558	smb	SMBUS SMC B S0_SCL 52
	smb_558	smb	SMBUS SMC B S0_SDA 52
	smb_558	smb	SMBUS SMC 0 S0_SCL 52
	smb_558	smb	SMBUS SMC 0 S0_SDA 52
	smb_558	smb	SMBUS SMC BSA_SCL 52
	smb_558	smb	SMBUS SMC BSA_SDA 52
	smb_558	smb	SMBUS SMC MGMT_SCL 52 106
	smb_558	smb	SMBUS SMC MGMT_SDA 52 106
	smb_558	smb	SMBUS SMC MGMT_SCL 52 106
	smb_558	smb	SMBUS SMC MGMT_SDA 52 106
	smb_558	smb	SMBUS MCP 0_CLK 13 21 52
	smb_558	smb	SMBUS MCP 0_DATA 13 21 52

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP_BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	3:1_SPACING
DISPLAYPORT	POWER	*	PWR_P2MM
DISPLAYPORT	GND	*	GND_P2MM

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET ASSIGNED IN CONT. MGR.	NET_TYPE			
	PHYSICAL	SPACING		
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML P<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML N<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML C P<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML C N<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML EQ P<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A ML EQ N<3..0>	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A AUX P	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A AUX N	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A AUX C P	04 91
DP_100D	DP_100D	DISPLAYPORT	MXM DP A AUX C N	04 91
DP_100D	DP_100D	DISPLAYPORT	DP EXT LINK P<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	DP EXT LINK N<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	DP EXT LINK C P<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	DP EXT LINK C N<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	DP EXT AUXCH P	04 94 95
DP_100D	DP_100D	DISPLAYPORT	DP EXT AUXCH N	04 94 95
DP_100D	DP_100D	DISPLAYPORT	DP ML CONN P<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	DP ML CONN N<3..0>	04 94
DP_100D	DP_100D	DISPLAYPORT	MXM DP C ML P<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C ML N<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C ML C P<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C ML C N<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C AUX P	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C AUX N	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C AUX C P	04 92
DP_100D	DP_100D	DISPLAYPORT	MXM DP C AUX C N	04 92
DP_100D	DP_100D	DISPLAYPORT	DP INT LINK P<3..0>	04 90
DP_100D	DP_100D	DISPLAYPORT	DP INT LINK N<3..0>	04 90
DP_100D	DP_100D	DISPLAYPORT	DP INT LINK CONN P<3..0>	04 90
DP_100D	DP_100D	DISPLAYPORT	DP INT LINK CONN N<3..0>	04 90
DP_100D	DP_100D	DISPLAYPORT	DP INT AUXCH P	04 90
DP_100D	DP_100D	DISPLAYPORT	DP INT AUXCH N	04 90
DP_100D	DP_100D	DISPLAYPORT	DP MUX P<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	DP MUX N<3..0>	04 92
DP_100D	DP_100D	DISPLAYPORT	DP MUX AUXCH P	04 92 107
DP_100D	DP_100D	DISPLAYPORT	DP MUX AUXCH N	04 92 107
DP_100D	DP_100D	DISPLAYPORT	DP MUX AUXCH P	04 92 107
DP_100D	DP_100D	DISPLAYPORT	DP MUX AUXCH N	04 92 107
DP_100D	DP_100D	DISPLAYPORT	DP TX EQ AUXCH P	04 91
DP_100D	DP_100D	DISPLAYPORT	DP TX EQ AUXCH N	04 91
DP_100D	DP_100D	DISPLAYPORT	DP EQIZ AUXCH P	04 92
DP_100D	DP_100D	DISPLAYPORT	DP EQIZ AUXCH N	04 92
MCP_DV_COMP			MCP HDMI RSET	18 26
MCP_DV_COMP			MCP HDMI VPROBE	18 26

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Graphics Constraints

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
PSB_DSTR	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP	OVERRIDE	OVERRIDE	0.1 MM	600 MIL	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP	OVERRIDE	OVERRIDE	0.1 MM	600 MIL	OVERRIDE	OVERRIDE
MEM_70D	TOP	OVERRIDE	OVERRIDE	0.1 MM	600 MIL	OVERRIDE	OVERRIDE
PCIE_90D	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
USB_90D	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
MCP_M11_COMP	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
MCP_USB_KBIAS	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
MCP_DV_COMP	OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM	250 MIL	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM	OVERRIDE	OVERRIDE	0.23 MM	100 MIL	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
		PPDDR_MEM	=PP1V5 S3 MEM A	6 30 31
		PPDDR_MEM	=PP1V5 S3 MEM B	6 30 32
		SWITCHNODE	VR_CPU SW1	72
		SWITCHNODE	VR_CPU SW2	72
		SWITCHNODE	VR_CPU SW3	72
		SWITCHNODE	1V8_SW	80
		SWITCHNODE	1V185_SW	79
		SWITCHNODE	PVTT50 PHASE	74
		SWITCHNODE	3V3S5_SW	74
		SWITCHNODE	5V33_SW	73
		SWITCHNODE	MPCORE50 PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1 DN6	55
	THERM_DIFF	THERMAL	SNS_T_DP1 DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2 DN3	55
	THERM_DIFF	THERMAL	SNS_T_DP2 DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4 DN5	55
	THERM_DIFF	THERMAL	SNS_T_DP4 DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 110
	THERM_DIFF	THERMAL	SNS_LCD_N	55 110
	THERM_DIFF	THERMAL	SNS_ODD_P	55 110
	THERM_DIFF	THERMAL	SNS_ODD_N	55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 110
	THERM_DIFF	THERMAL	SNS_AMB_N	55 110
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU ISNS1_P	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS1_N	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU ISNS2_P	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS2_N	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU ISNS3_P	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS3_N	71 72
	SNS_DIFF	THERMAL	VR_CPU ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU ISNS3_R_N	71
		THERMAL	SMC_CPU_ISENSE	49 53
		THERMAL	VR_CPU_IOUT	53 71
		THERMAL	VR_ISNS_CPU_P	53
		THERMAL	VR_ISNS_CPU_N	53
		THERMAL	SNS_PS_CPU_ISNS	53
		THERMAL	SMC_CPU_VSENSE	49 53
		THERMAL	CPU_VCC_SENSE	12 53
		THERMAL	SMC_GPU_VSENSE	49 53
		THERMAL	SMC_GPU_ISENSE	49 53
		THERMAL	SMC_1V5_S0_ISENSE	50 54
		THERMAL	SMC_1V5_S0_ISENSE_R	54
		THERMAL	SMC_1V5_S0_VSENSE	50 54
		THERMAL	SMC_MCP_CORE_ISENSE	50 54
		THERMAL	SMC_MCP_CORE_VSENSE	50 54
		THERMAL	MPCORE50_IMON	54 74
		THERMAL	CPU_PECI_L	11 55
		THERMAL	SMB_PECI_L	55
		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
		THERMAL	HDD_OOB_TEMP	55
		THERMAL	HDD_OOB_TEMP_R	55
		THERMAL	SMC_HDD_OOB_TEMP	55

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K22/K23 SPECIFIC CONSTRAINTS

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP, BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

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K22/K23 RULE DEFINITIONS

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CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI, LPC, SMB, HDA, SPI, RGMII, SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA
 103 47 USB_CAMERA_I_P FUNC_TEST=TRUP
 103 47 USB_CAMERA_I_N FUNC_TEST=TRUP
 1 PP5V_S3_REG Testpoint near J4700
 2 Ground Testpoints near J4700

J4750 USB CARD READER
 103 47 USB_SDCARD_I_P FUNC_TEST=TRUP
 103 47 USB_SDCARD_I_N FUNC_TEST=TRUP
 1 PP3V3_S3 Testpoint near J4750
 2 Ground Testpoints near J4750

J4720 USB BLUETOOTH
 103 47 USB_BT_I_P FUNC_TEST=TRUP
 103 47 USB_BT_I_N FUNC_TEST=TRUP
 1 PP3V3_S3 Testpoint near J4720
 2 Ground Testpoints near J4720

J4780 IR BOARD
 103 47 USB_IR_I_P FUNC_TEST=TRUP
 103 47 USB_IR_I_N FUNC_TEST=TRUP
 1 PP5V_S3_REG Testpoint near J4780
 2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)
 102 45 SATA_ODD_R2D_P FUNC_TEST=TRUP
 102 45 SATA_ODD_R2D_N FUNC_TEST=TRUP
 102 45 SATA_ODD_D2R_C_N FUNC_TEST=TRUP
 102 45 SATA_ODD_D2R_C_P FUNC_TEST=TRUP
 49 45 SMC_ODD_DETECT FUNC_TEST=TRUP
 1 PP5V_S0 Testpoint near J4520
 5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)
 102 45 SATA_HDD_R2D_P FUNC_TEST=TRUP
 102 45 SATA_HDD_R2D_N FUNC_TEST=TRUP
 102 45 SATA_HDD_D2R_C_N FUNC_TEST=TRUP
 102 45 SATA_HDD_D2R_C_P FUNC_TEST=TRUP
 3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR
 108 55 SNS_LCD_P FUNC_TEST=TRUP
 108 55 SNS_LCD_N FUNC_TEST=TRUP

J5521 AMBIENT TEMP SENSOR
 108 55 SNS_AMB_P FUNC_TEST=TRUP
 108 55 SNS_AMB_N FUNC_TEST=TRUP

J5551 ODD TEMP SENSOR
 108 55 SNS_ODD_P FUNC_TEST=TRUP
 108 55 SNS_ODD_N FUNC_TEST=TRUP

J5600 ODD FAN
 56 FAN_0_PWR_L FUNC_TEST=TRUP
 56 FAN_TACH0_L FUNC_TEST=TRUP
 56 PP12V_S0_FAN0_L FUNC_TEST=TRUP
 56 FAN_0_GND FUNC_TEST=TRUP

J5700 CPU FAN
 57 FAN_2_PWR_L FUNC_TEST=TRUP
 57 FAN_TACH2_L FUNC_TEST=TRUP
 57 PP12V_S0_FAN2_L FUNC_TEST=TRUP
 57 FAN_2_GND FUNC_TEST=TRUP

J5601 HD FAN
 56 FAN_1_PWR_L FUNC_TEST=TRUP
 56 FAN_TACH1_L FUNC_TEST=TRUP
 56 PP12V_S0_FAN1_L FUNC_TEST=TRUP
 56 FAN_1_GND FUNC_TEST=TRUP

J6601 AUDIO MICROPHONE
 66 AUD_MIC_IN1_N_CONN FUNC_TEST=TRUP
 66 GND_AUDIO_MIC1_CONN FUNC_TEST=TRUP
 66 AUD_MIC_IN1_P_CONN FUNC_TEST=TRUP
 1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER
 66 AUD_SPKR_OUTLO2R_P FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO2R_N FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO1R_P FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO1R_N FUNC_TEST=TRUP

J6603 AUDIO LEFT SPEAKER
 66 AUD_SPKR_OUTLO2L_P FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO2L_N FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO1L_P FUNC_TEST=TRUP
 66 AUD_SPKR_OUTLO1L_N FUNC_TEST=TRUP

GND 16 TP45 FUNC_TEST=TRUP
 MIN_ALLOWED_TPS16 1

PP3V3_S3 2 TP46 FUNC_TEST=TRUP
 MIN_ALLOWED_TPS2 2

PP5V_S3_REG 2 TP48 FUNC_TEST=TRUP
 MIN_ALLOWED_TPS2 2

PP5V_S0 FUNC_TEST=TRUP
 MIN_ALLOWED_TPS1 1

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