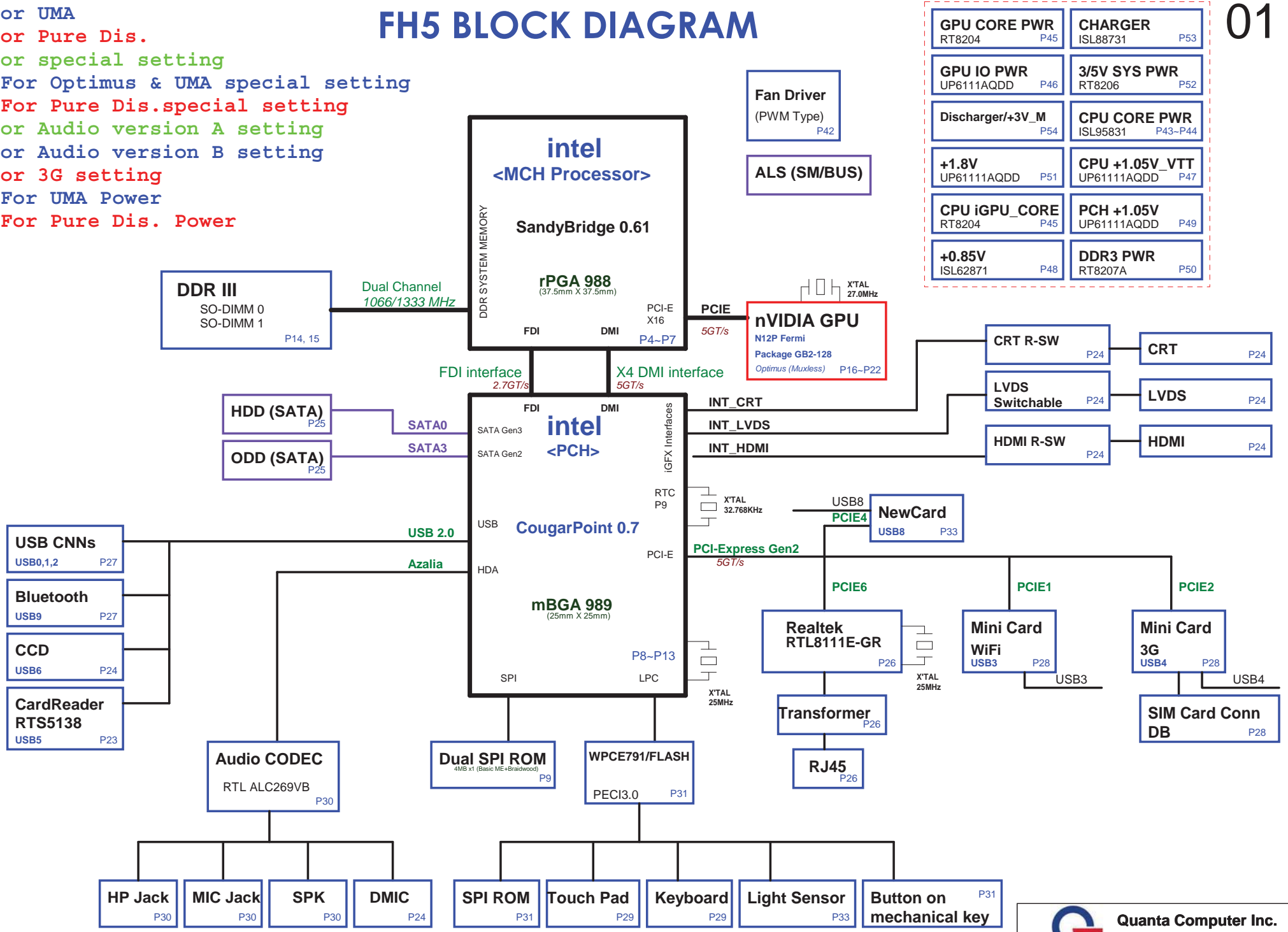


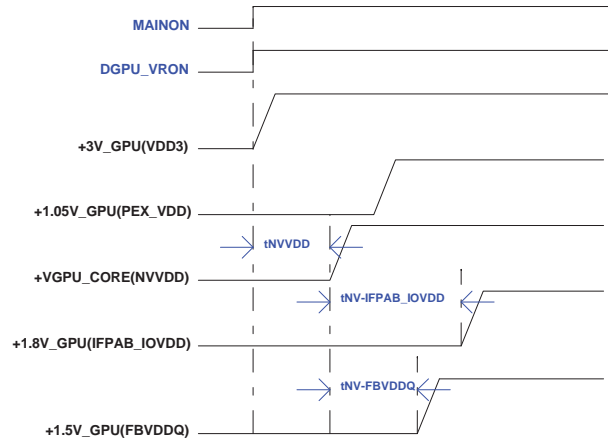
FH5 BLOCK DIAGRAM

IV@ For UMA
 EV@ For Pure Dis.
 SP@ For special setting
 SPI@ For Optimus & UMA special setting
 SPE@ For Pure Dis.special setting
 VA@ For Audio version A setting
 VB@ For Audio version B setting
 @3G For 3G setting
 PIV@ For UMA Power
 PEV@ For Pure Dis. Power



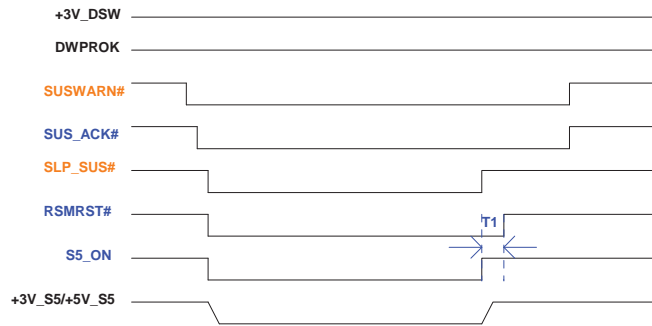
Note:
 HM65 does not support USB 6 & 7
 HM65 does not support SATA 2 & 3

N12P-GE Power Up Sequence



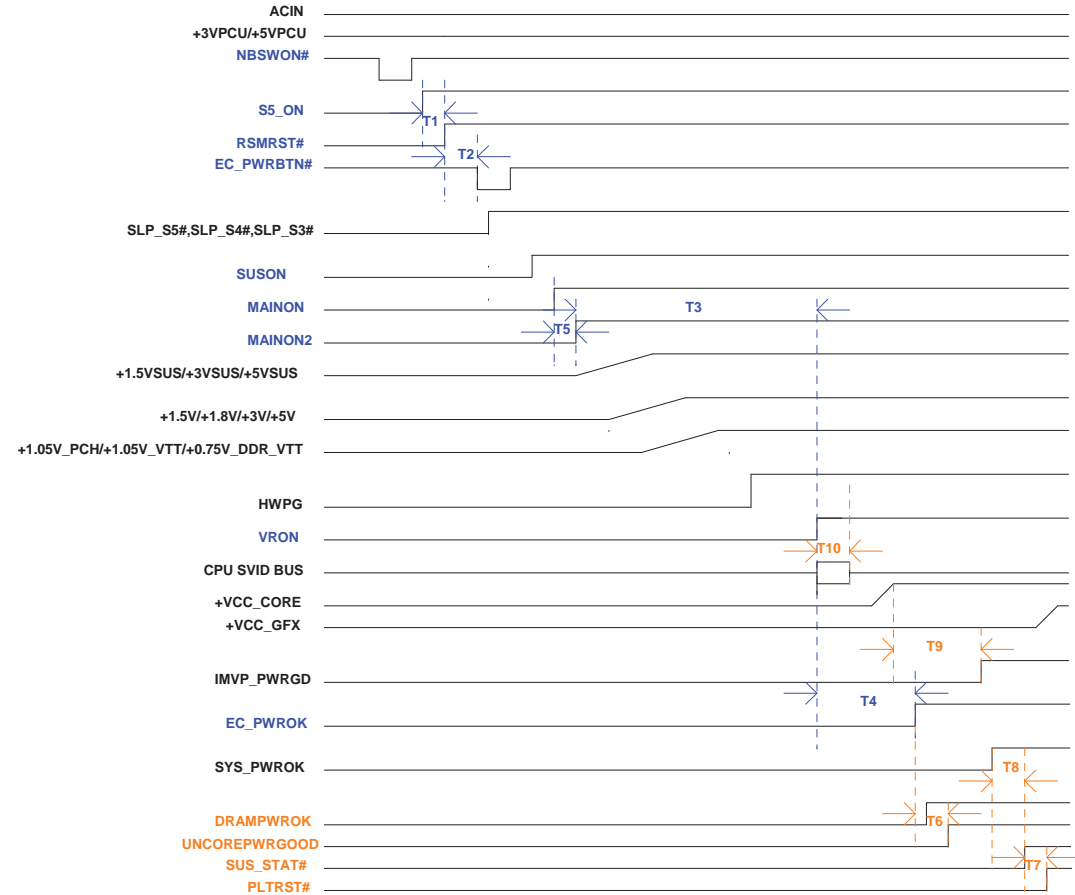
N12P-GE Power up Sequence
 tINVDD>0
 tINV-IFPAB_IOVDD>0
 tINV-FBVDDQ>0

Deep S4/S5 off-on Sequence

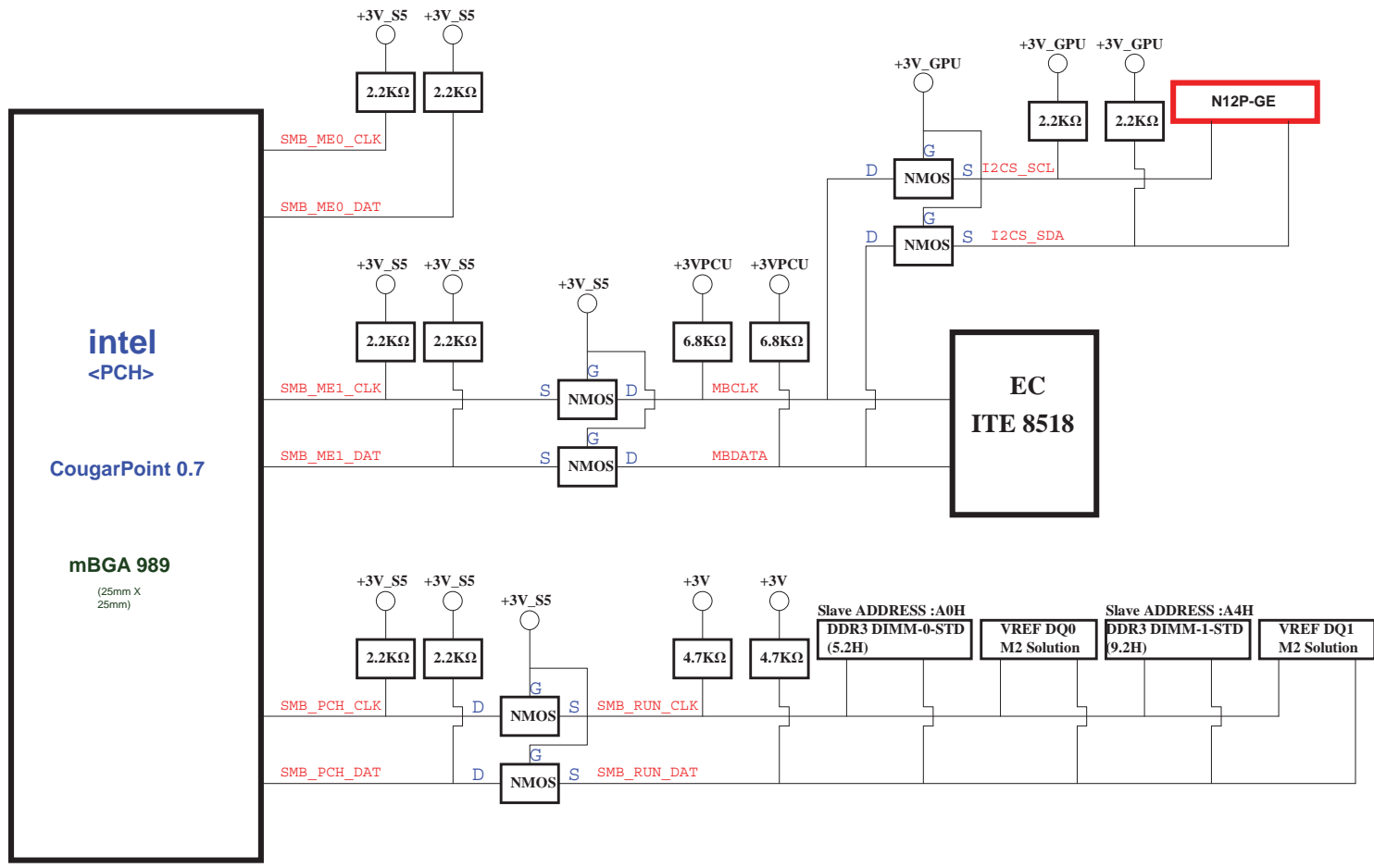


Deep S4/S5 Sequence
 T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence

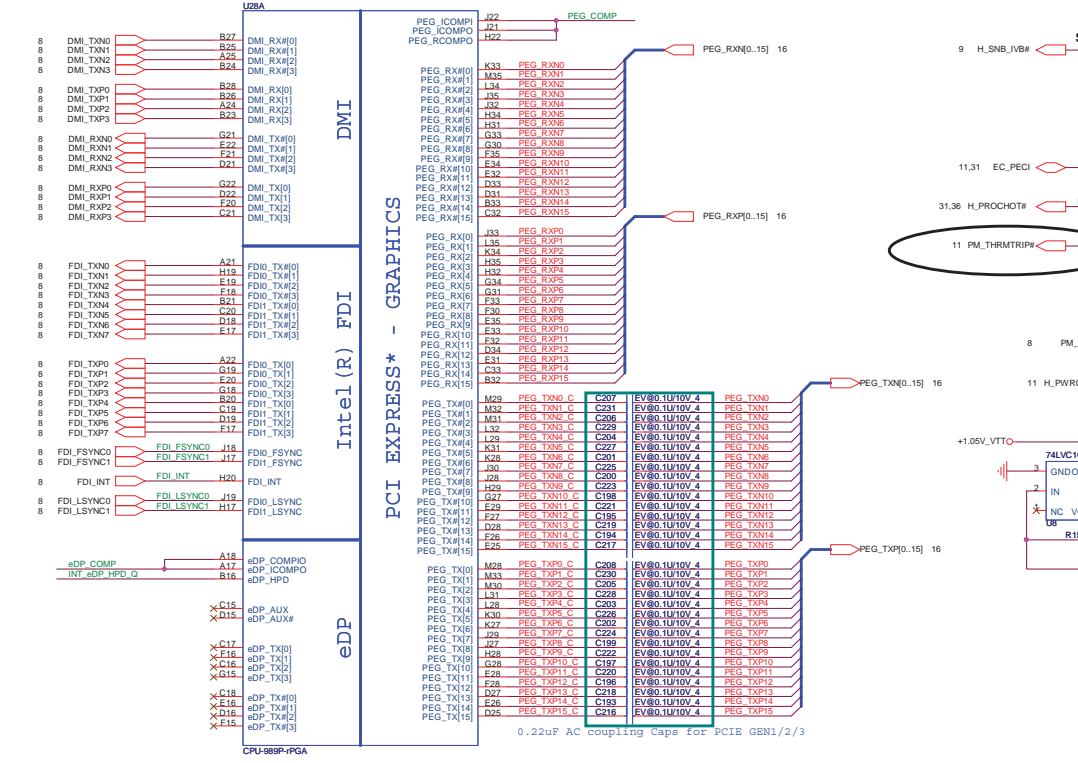


System Power Sequence
 T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
 T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
 T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
 T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
 T5: MAINON TO MAINON2 = 500us
 T6: EC_PWROK to UNCOREPWROK = 2ms(Min)
 T7: SUS_STAT# to PLTRST# = 60us(Min)
 T8: SYS_PWROK to SUS_STAT# = 1ms(Min)
 T9: +VCC_CORE to IMVP_PWRGD = 5ms(Max)
 T10: VRON to accept SVID command. = 5ms(Max)

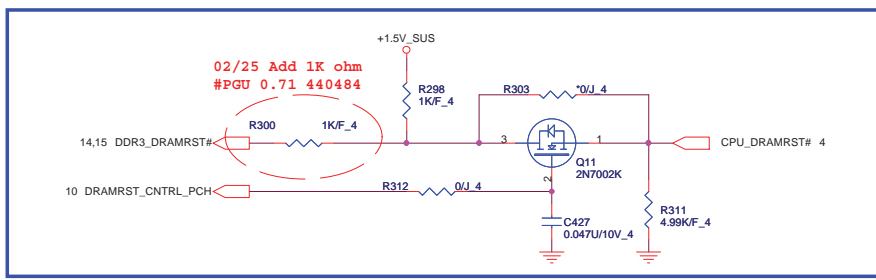
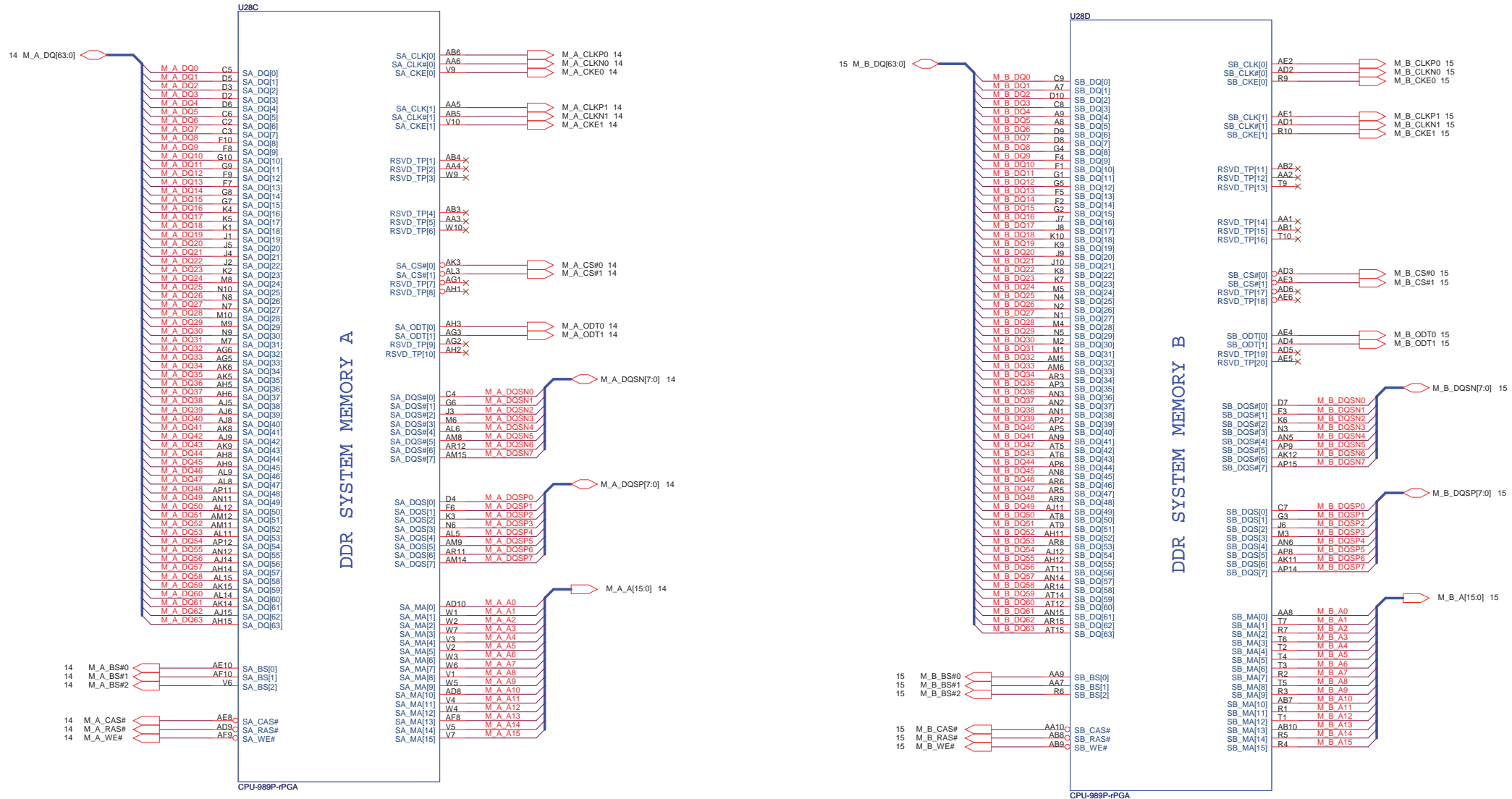


Sandy Bridge Processor (DMI, PEG, FDI)

Sandy Bridge Processor (CLK, MISC, JTAG)



Sandy Bridge Processor (DDR3)



Quanta Computer Inc.
PROJECT : FHS

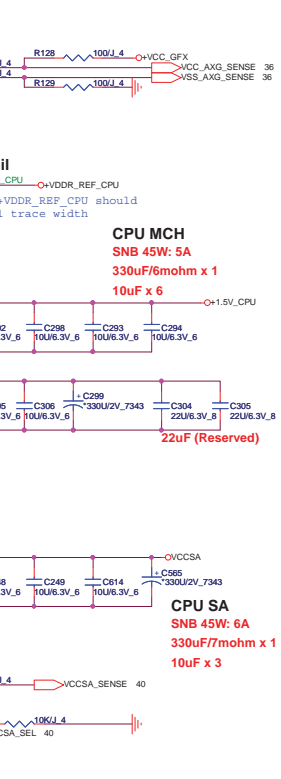
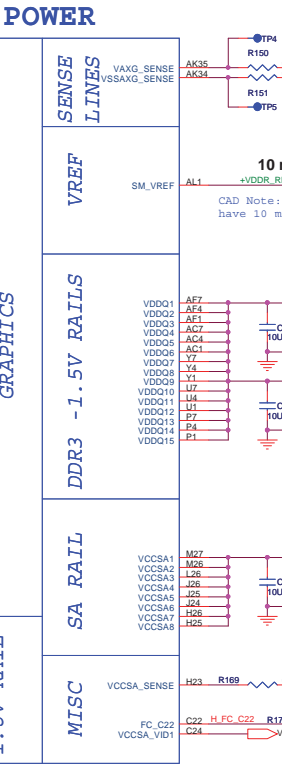
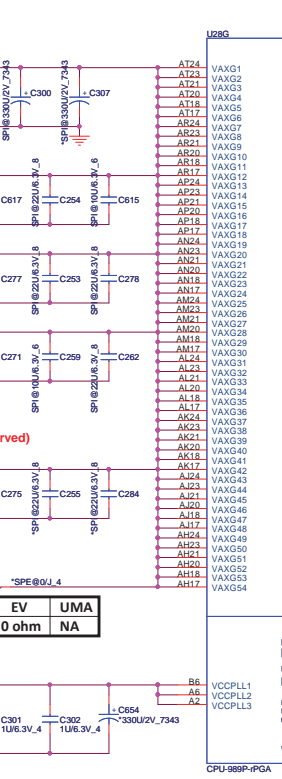
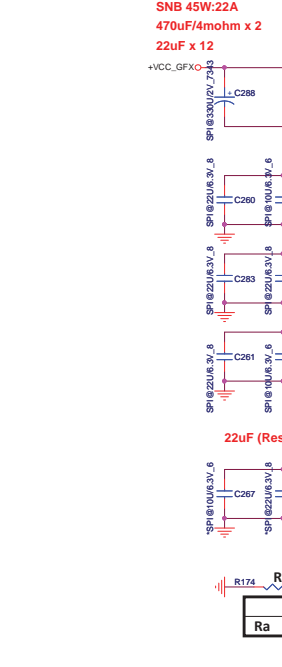
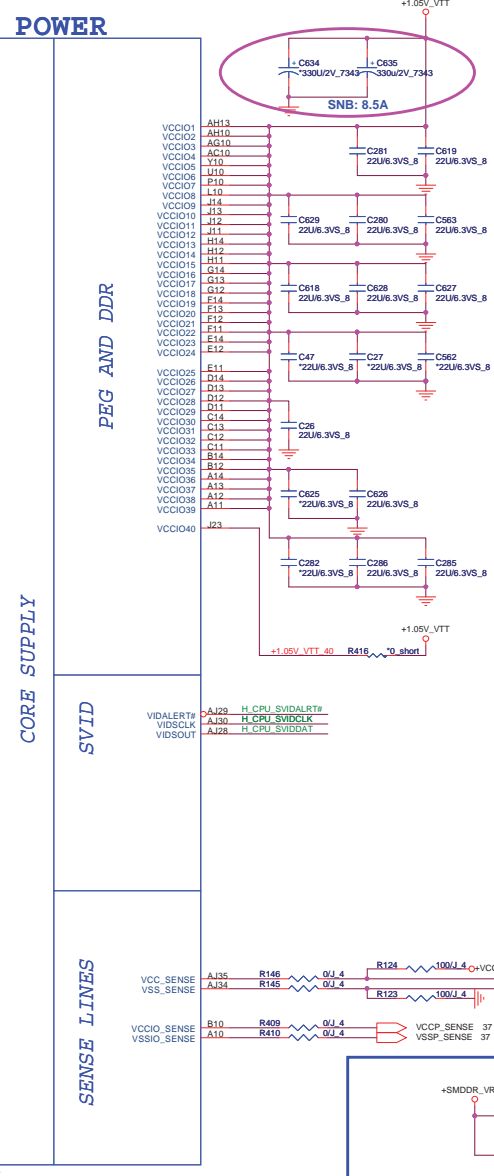
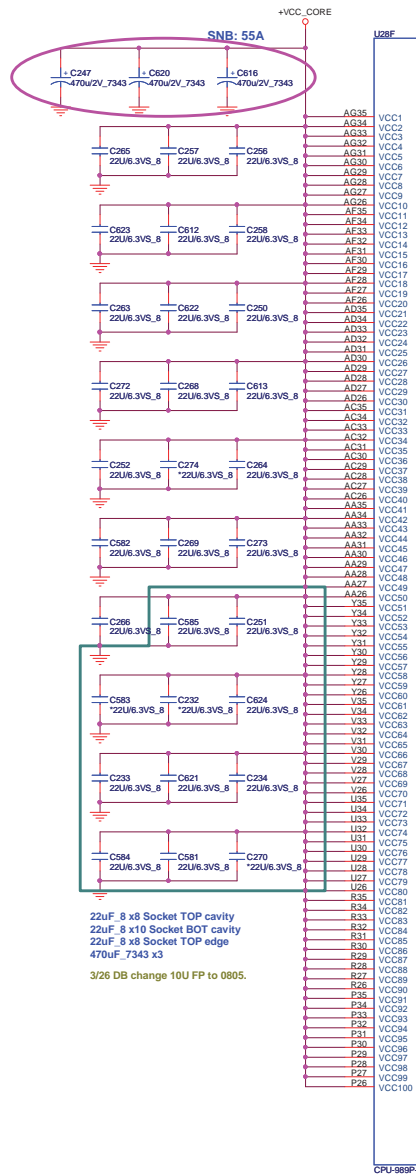
Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date:	Monday, September 27, 2010	Sheet 5 of 41

22uF 8 x7 Socket TOP cavity
22uF 8 x5 Socket BOT cavity
22uF 8 x2 Socket TOP cavity (no stuff)
22uF 8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

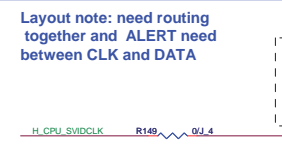
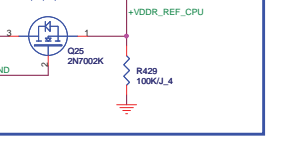
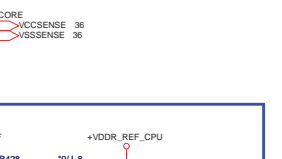
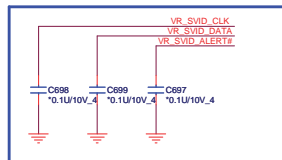
SPI@ For Optimus & UMA
SPE@ For Pure Dis.
SP@ For special setting

Sandy Bridge Processor (POWER)

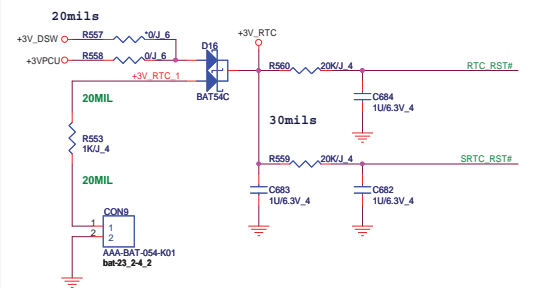
Sandy Bridge Processor (GRAPHIC POWER)



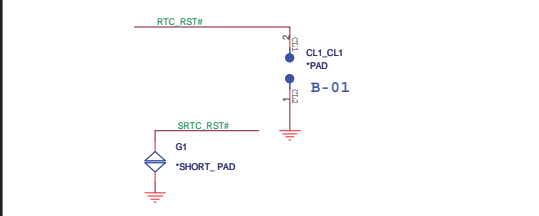
22uF 8 x8 Socket TOP cavity
22uF 8 x10 Socket BOT cavity
22uF 8 x8 Socket TOP edge
470uF_7343 x3
3/26 DB change 10U FP to 0805.



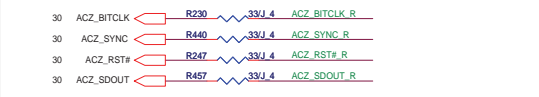
RTC Circuitry(RTC)



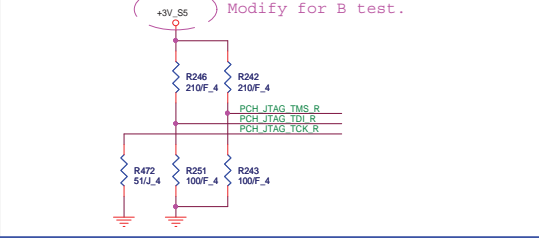
RESET JUMP (Near ROOM DOOR)



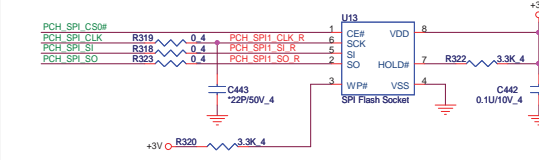
HDA Bus(CLG)



PCH JTAG Debug (CLG)

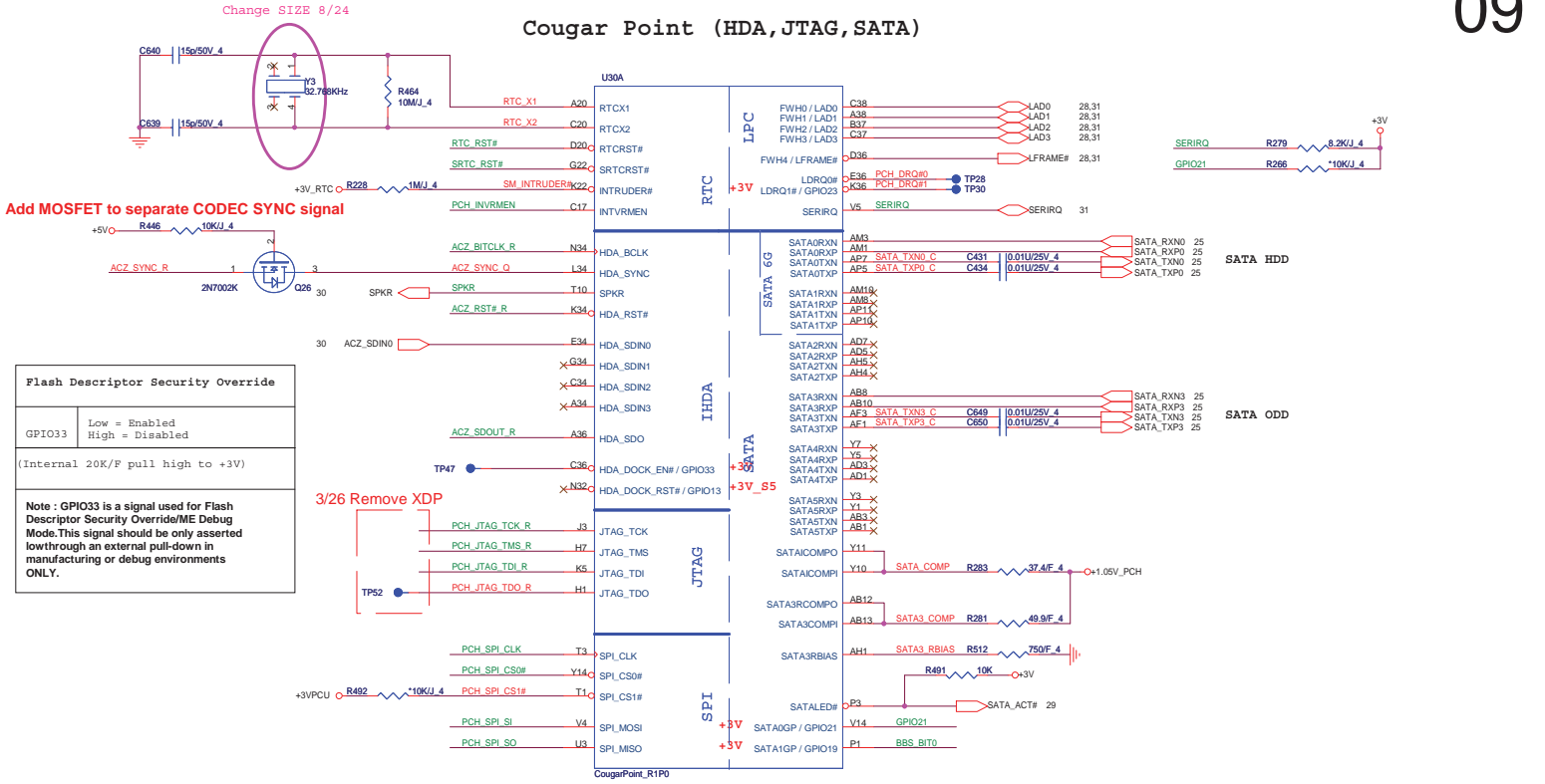


PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH2 (CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting internal PD	PWROK	0 = Default (weak pull-down) 1 = Setting to No-Reboot mode	+3V₀ - R508 *1KJ_4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override internal PU	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R237 *1KJ_4 PCI_GNT3# 10									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R195 *330KJ_4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1] internal PU	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	+3V₀ - R465 *1KJ_4 R475 *1KJ_4
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0] internal PU	PWROK		R468 *1KJ_4 R489 *1KJ_4 BBS_BIT0 10									
HDA_SDO	Flash Descriptor Security internal PD	RSMRST	0 = Default (weak pull-up 20K) 1 = Override	+3V₀ - R441 *1KJ_4 ACZ_SDOUT_R 31 ME_WTR# R436 *0.4									
DF_TVS	DMI/FDI Termination voltage internal PD	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-up 20K)	R522 2.2KJ_4 +0.18V R523 *1KJ_4 DF_TVS 11 H_SNB_IVB# 4									
GPIO28	On-die PLL Voltage Regulator internal PU	RSMRST#	0 = Disable 1 = Enable (Default)	R270 *1KJ_4 PLL_OVR_EN 11									
HDA_SYNC	On-Die PLL VR Voltage Select internal PD	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R434 *1KJ_4 ACZ_SYNC_Q Need check schematic									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Intel ME TLS with no confidentiality 1 = Intel ME TLS with confidentiality	+3V_S5 - R241 *1K_4 PCH_GPIO15 11									

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

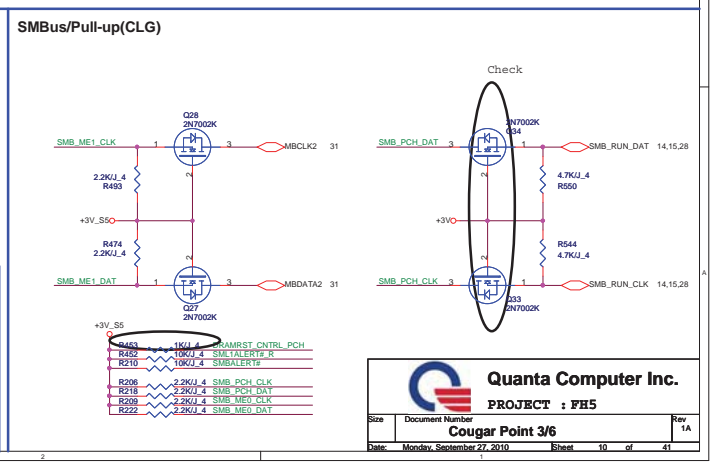
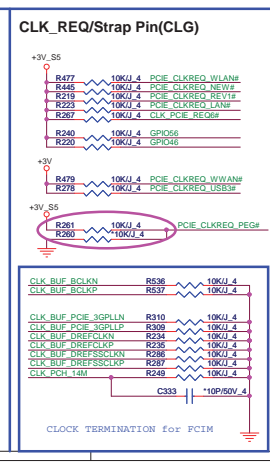
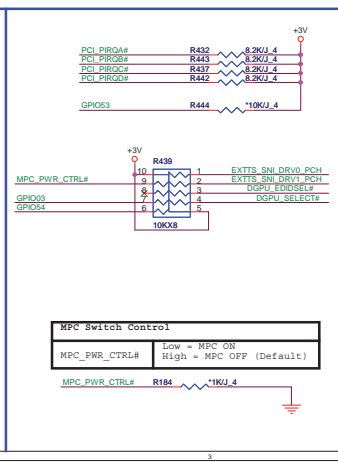
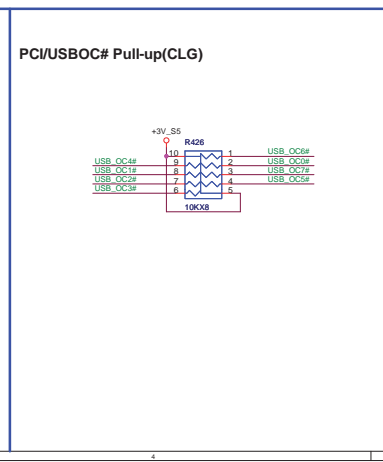
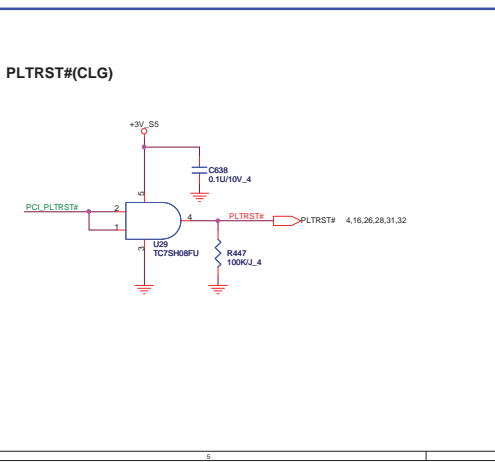
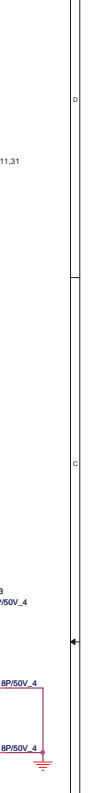
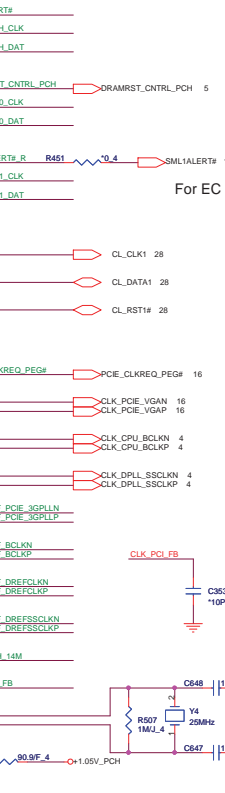
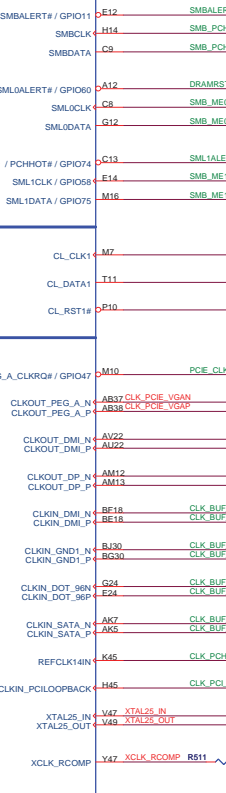
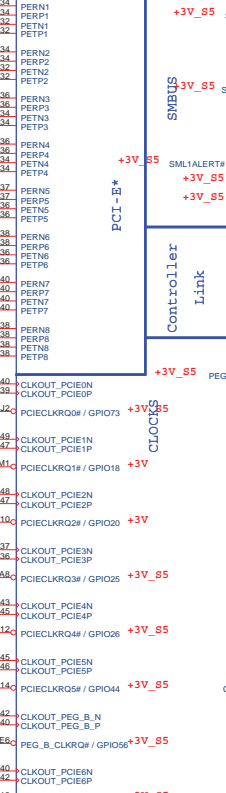
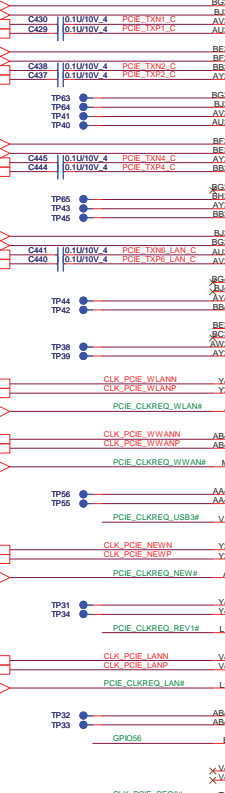
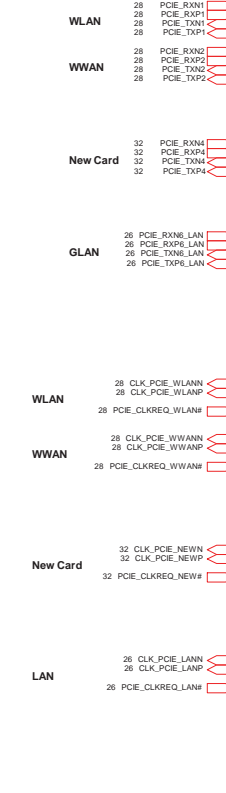
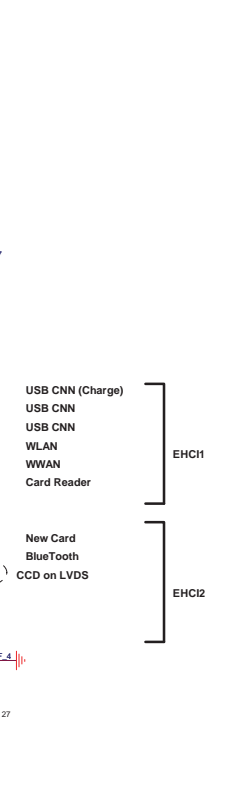
GNT[3:0]# functionality is not available on Mobile. Used as GPIO only.

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

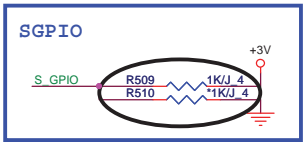
R8361 change to 1K ohm follow Dg1.0 and chklst 1.0
It needs to be connected to PROC_SELECT with a 1k±5% pull-up resistor to PCH VCCPND rail and a 4.7k±5% series resistor.

New Add in CPT EDS Rev1.0 at 0316
, Needs to be pulled High for Huron River platform.

Cougar Point-M (PCI,USB,NVRAM)

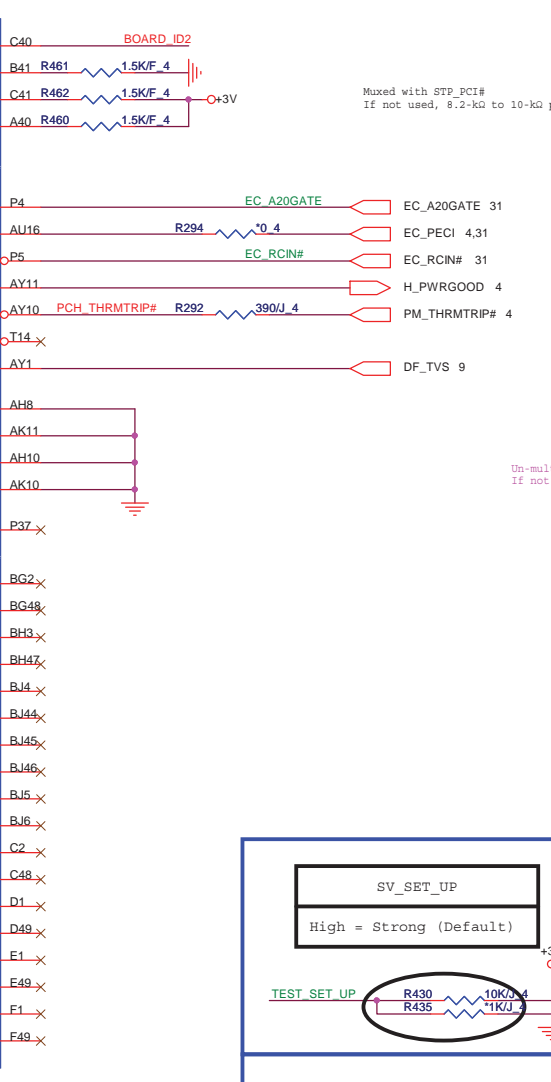
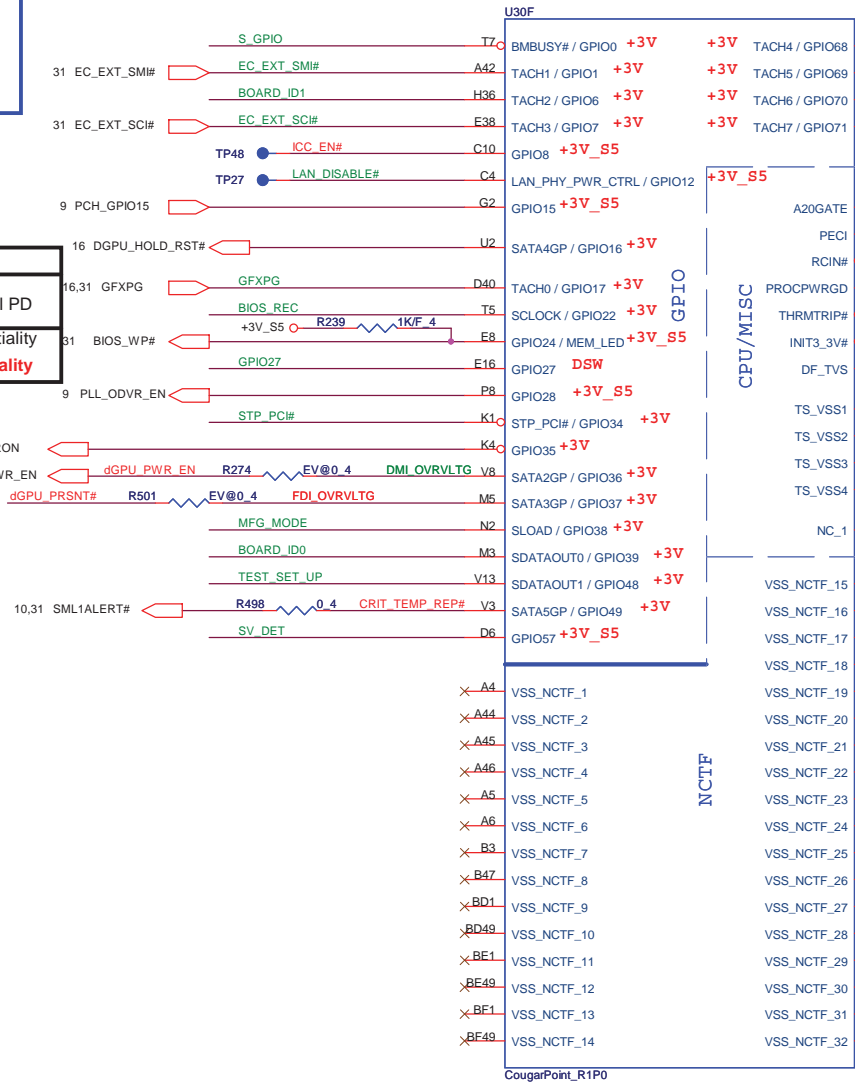


Cougar Point (GPIO, VSS_NCTF, RSVD)

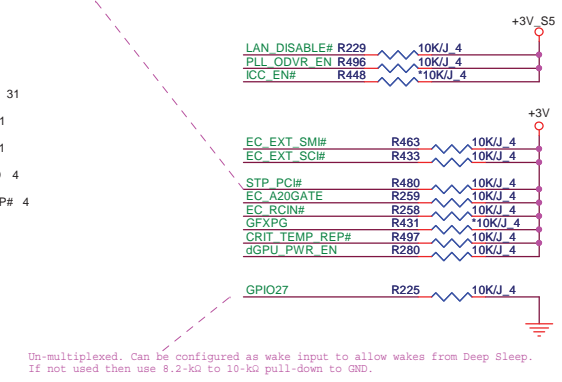


GPIO15
Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD
0 = Intel ME TLS with no confidentiality
1 = Intel ME TLS with confidentiality

GPUCORE_ON 31,39,41 dGPU_VRON
GPU_PWR_ON 41 dGPU_PWR_EN

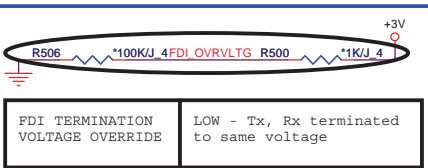


GPIO Pull-up/Pull-down(CLG)

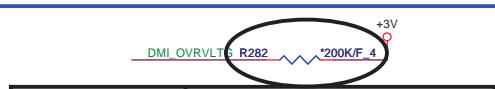


Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep. If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

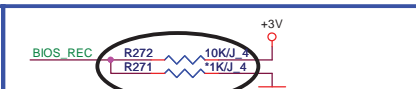
SATA[3:2]GP/GPIO[37:36] internal Pull-down 20K
SATA2GP/GPIO36 (FDI_OVRVLTG) & SATA3GP/GPIO37 (DMI_OVRVLTG)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled



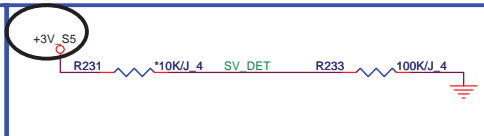
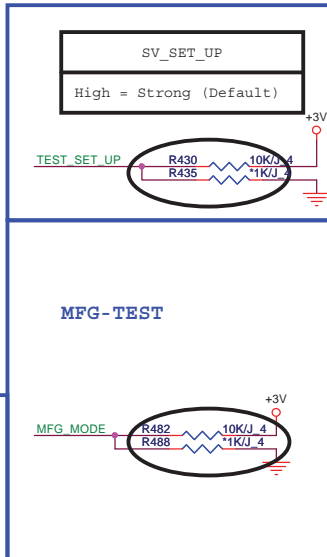
FDI TERMINATION VOLTAGE OVERRIDE
Low - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

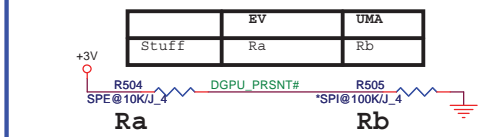
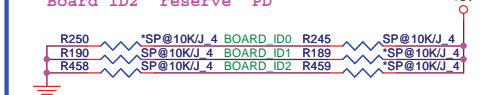


BIOS RECOVERY
High = Disable (Default)
Low = Enable



[ID0:D1]	0:0	0:1	1:0	1:1
Fuction	UMA	Optimus (Hynix)	Optimus (Samsung)	Rev.

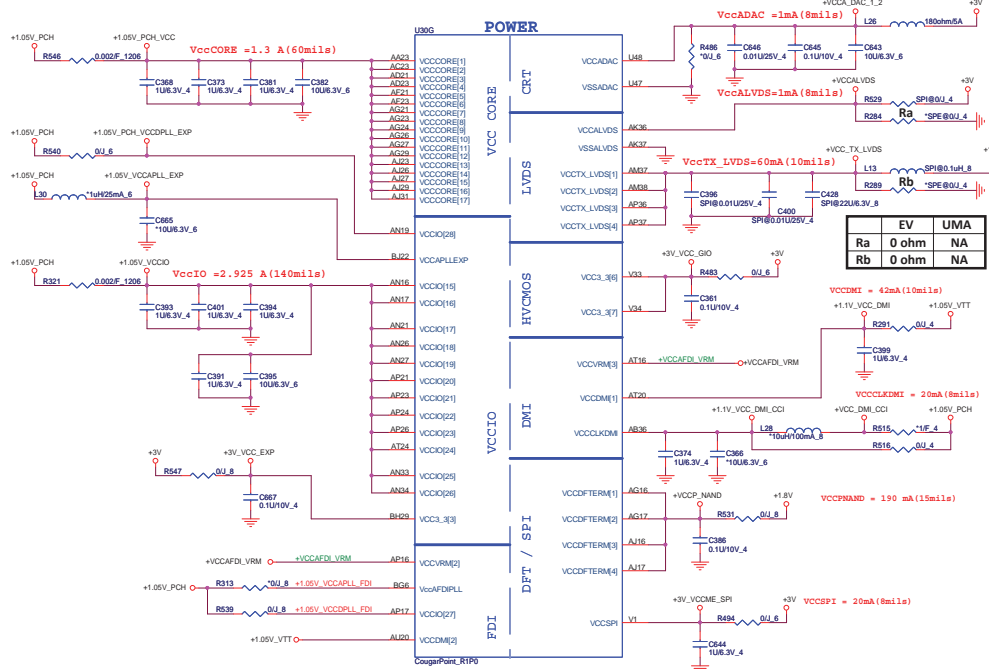
Board ID2 reserve PD



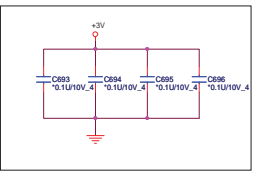
	EV	UMA
Stuff	Ra	Rb

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PROJECT : FH5

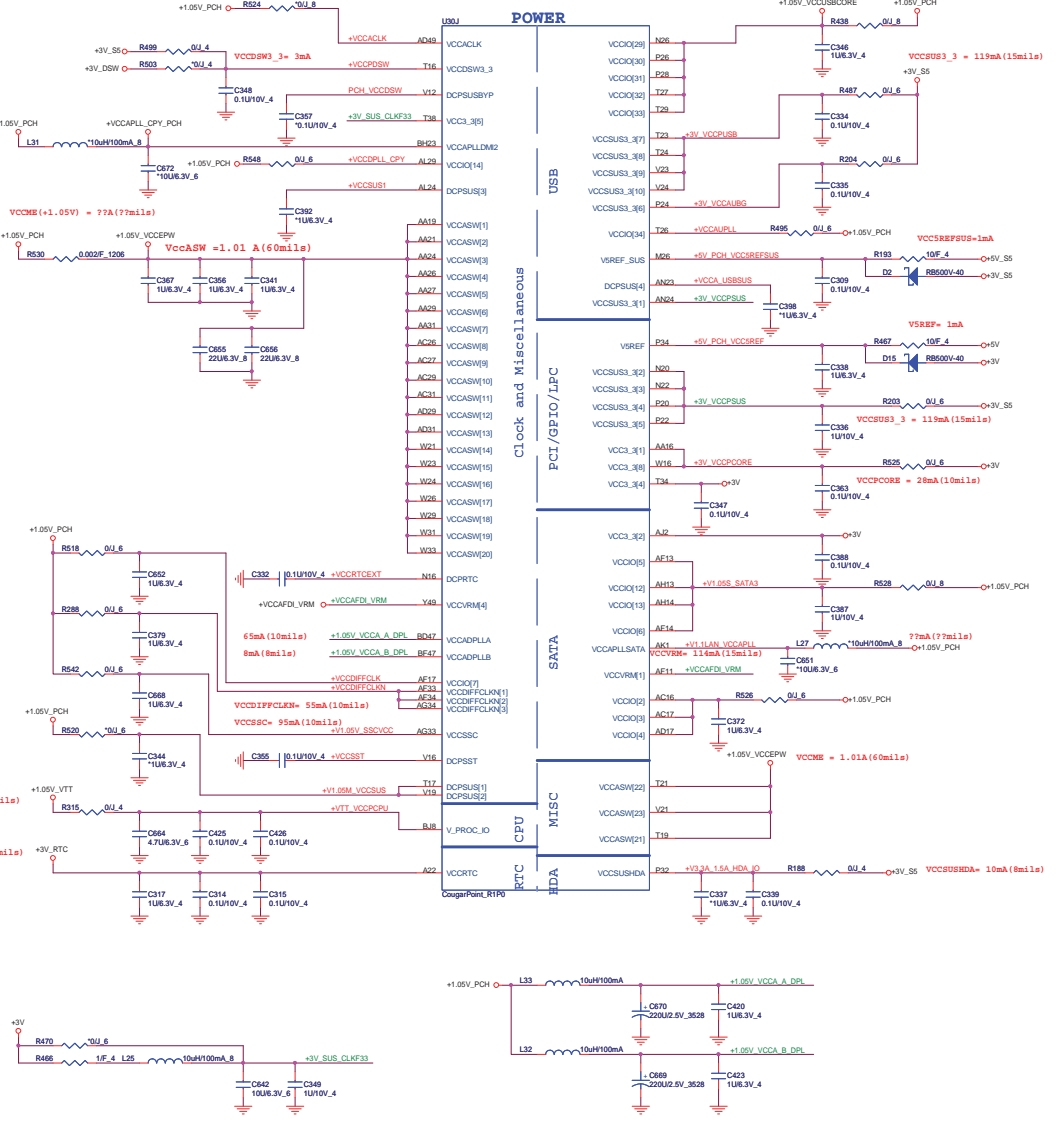
COUGAR POINT (POWER)



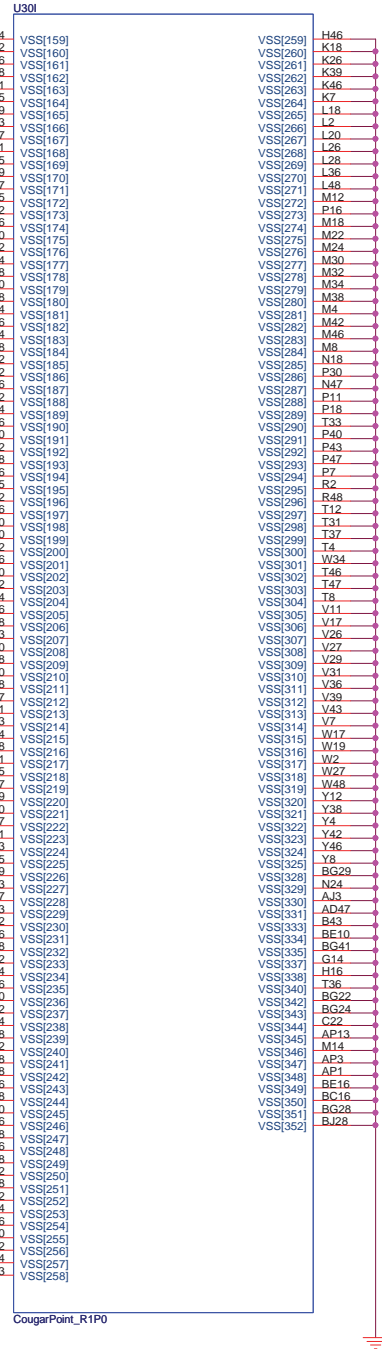
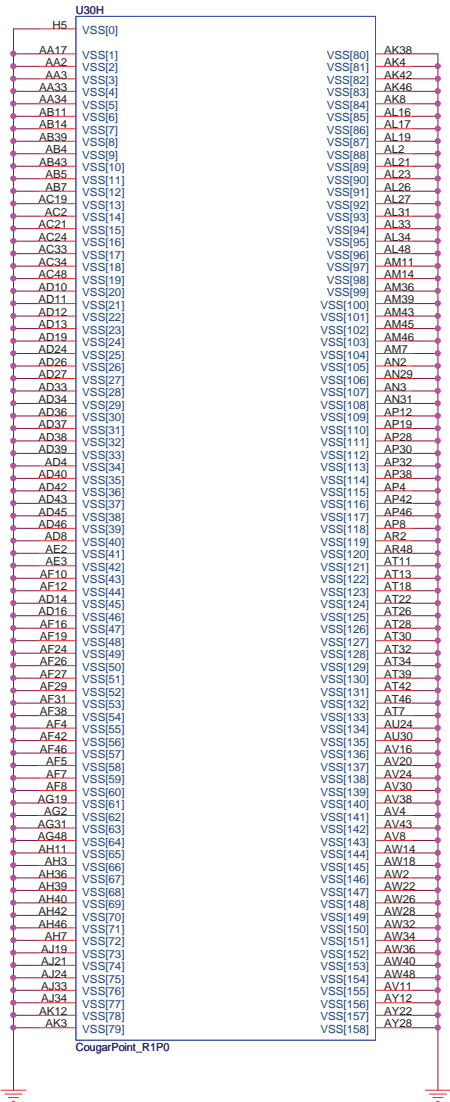
VCCVRM: 1.6V (Desktop) 0.720 del for Pre-B51
1.5V (Mobile)



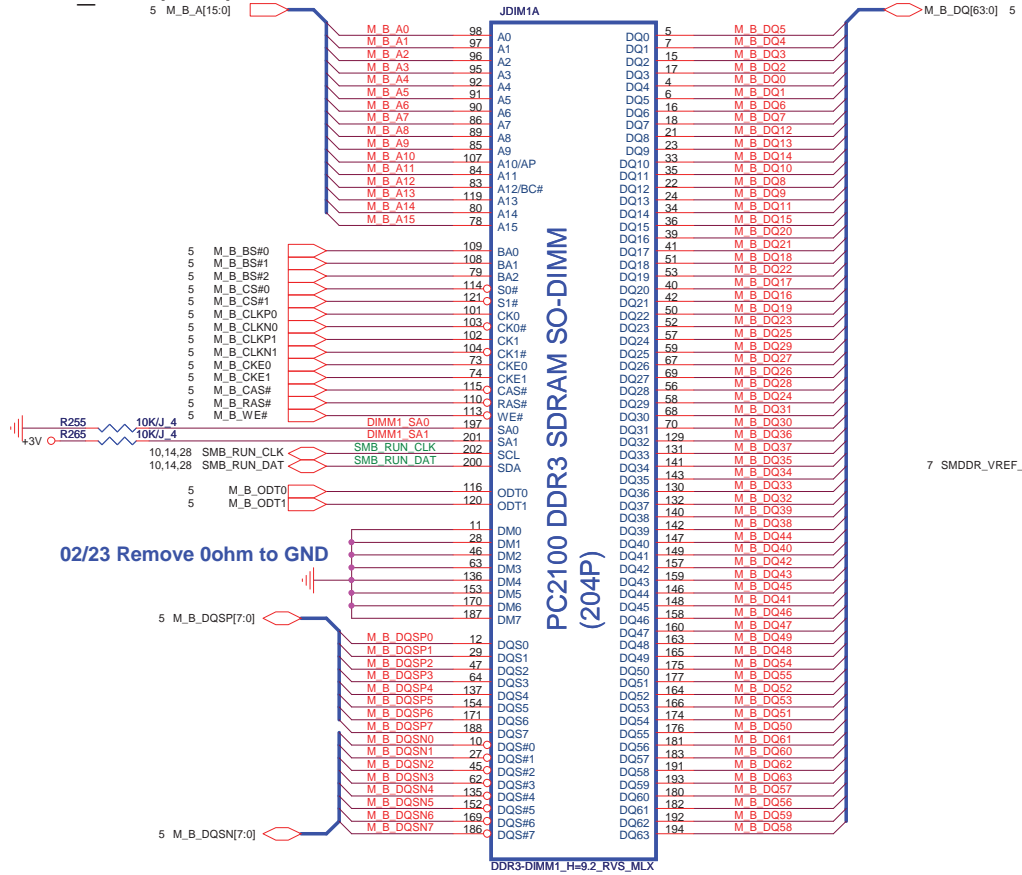
Cougar Point-M (POWER)



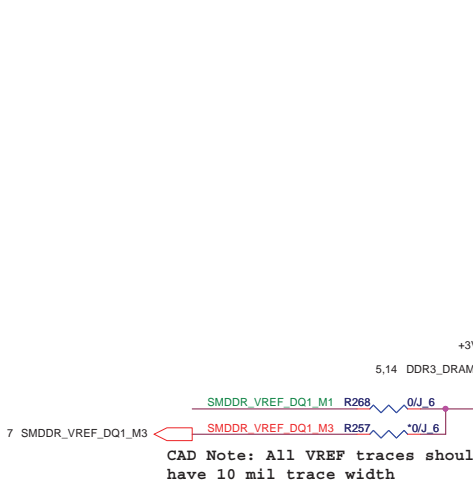
IBEX PEAK-M (GND)



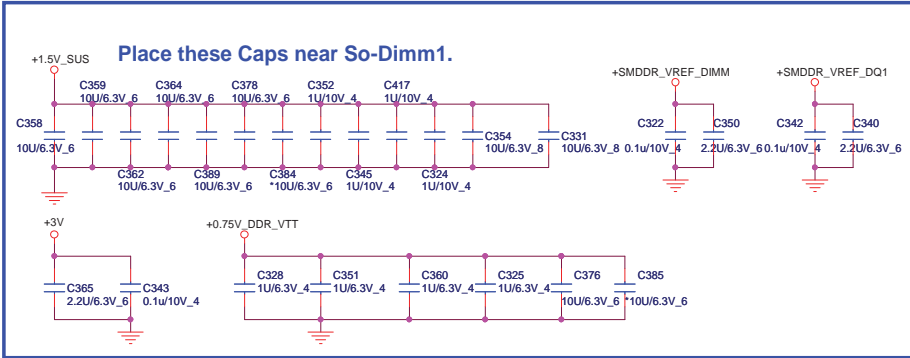
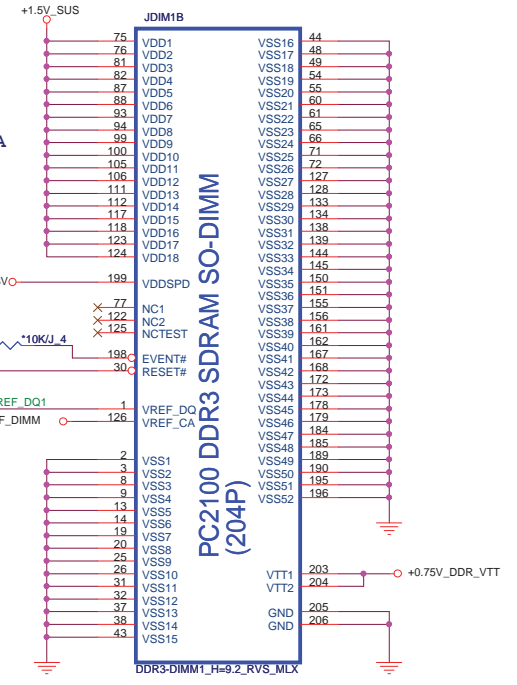
DDR_RVS (DDR)



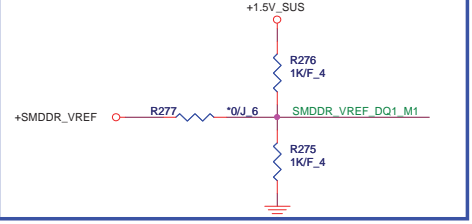
02/23 Remove 0ohm to GND



2.48A



VREF DQ1 M1 Solution



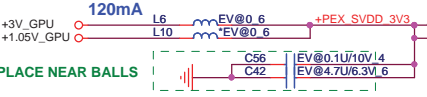
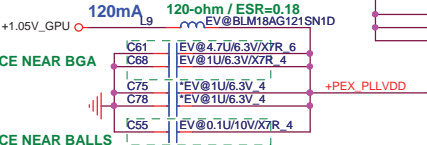
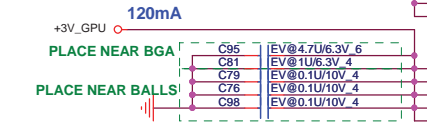
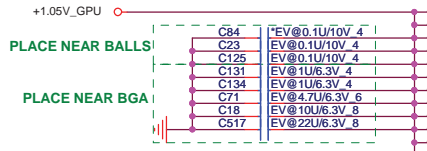
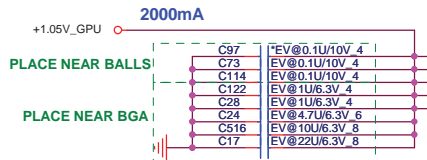
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

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PROJECT : FH5

Size	Document Number	Rev
	DDR3 SO-DIMM-1	1A
Date:	Monday, September 27, 2010	Sheet 15 of 41

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A



U23A
fcbg973-rvidia-n12p-ge
COMMON

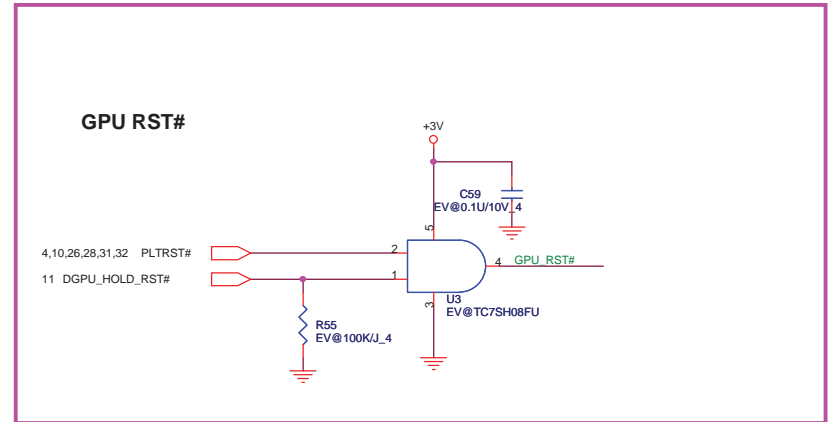
PEX_IOVDD_1	AK16
PEX_IOVDD_2	AK17
PEX_IOVDD_3	AK21
PEX_IOVDD_4	AK24
PEX_IOVDD_5	AK27
PEX_IOVDDQ_1	AG11
PEX_IOVDDQ_2	AG12
PEX_IOVDDQ_3	AG13
PEX_IOVDDQ_4	AG15
PEX_IOVDDQ_5	AG16
PEX_IOVDDQ_6	AG17
PEX_IOVDDQ_7	AG18
PEX_IOVDDQ_8	AG22
PEX_IOVDDQ_9	AG23
PEX_IOVDDQ_10	AG24
PEX_IOVDDQ_11	AG25
PEX_IOVDDQ_12	AG26
PEX_IOVDDQ_13	AJ14
PEX_IOVDDQ_14	AJ15
PEX_IOVDDQ_15	AJ19
PEX_IOVDDQ_16	AJ21
PEX_IOVDDQ_17	AJ22
PEX_IOVDDQ_18	AJ25
PEX_IOVDDQ_19	AJ27
PEX_IOVDDQ_20	AK18
PEX_IOVDDQ_21	AK20
PEX_IOVDDQ_22	AK23
PEX_IOVDDQ_23	AK28
PEX_IOVDDQ_24	AL16
PEX_IOVDDQ_25	AL16

PCI EXPRESS

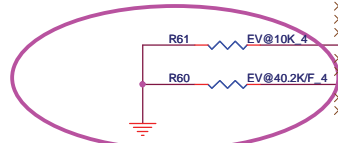
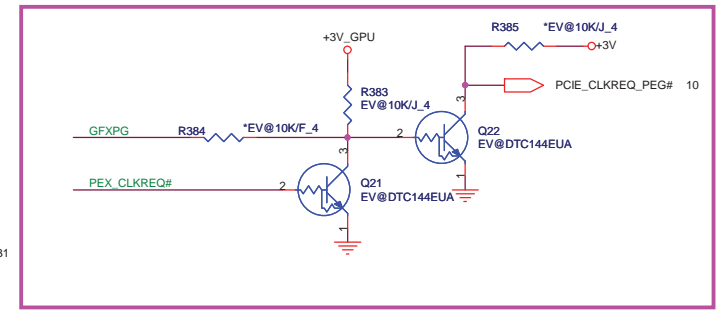
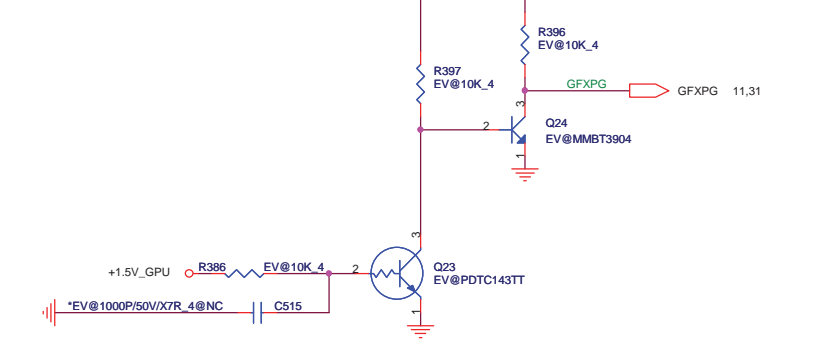
PEX_TX0	AL17	PEG RXP15 C	C80	EV@0.1U/10V_4	PEG_RXP15_4
PEX_TX0	AM17	PEG RXN15 C	C89	EV@0.1U/10V_4	PEG_RXN15_4
PEX_TX1	AM18	PEG RXP14 C	C109	EV@0.1U/10V_4	PEG_RXP14_4
PEX_TX1	AM19	PEG RXN14 C	C102	EV@0.1U/10V_4	PEG_RXN14_4
PEX_TX2	AK19	PEG RXP13 C	C113	EV@0.1U/10V_4	PEG_RXP13_4
PEX_TX2	AK19	PEG RXN13 C	C108	EV@0.1U/10V_4	PEG_RXN13_4
PEX_TX3	AL20	PEG RXP12 C	C106	EV@0.1U/10V_4	PEG_RXP12_4
PEX_TX3	AM20	PEG RXN12 C	C112	EV@0.1U/10V_4	PEG_RXN12_4
PEX_TX4	AM21	PEG RXP11 C	C120	EV@0.1U/10V_4	PEG_RXP11_4
PEX_TX4	AM22	PEG RXN11 C	C123	EV@0.1U/10V_4	PEG_RXN11_4
PEX_TX5	AK22	PEG RXP10 C	C124	EV@0.1U/10V_4	PEG_RXP10_4
PEX_TX5	AK22	PEG RXN10 C	C127	EV@0.1U/10V_4	PEG_RXN10_4
PEX_TX6	AL23	PEG RXP9 C	C129	EV@0.1U/10V_4	PEG_RXP9_4
PEX_TX6	AM23	PEG RXN9 C	C137	EV@0.1U/10V_4	PEG_RXN9_4
PEX_TX7	AM24	PEG RXP8 C	C128	EV@0.1U/10V_4	PEG_RXP8_4
PEX_TX7	AM25	PEG RXN8 C	C136	EV@0.1U/10V_4	PEG_RXN8_4
PEX_TX8	AL25	PEG RXP7 C	C130	EV@0.1U/10V_4	PEG_RXP7_4
PEX_TX8	AK25	PEG RXN7 C	C138	EV@0.1U/10V_4	PEG_RXN7_4
PEX_TX9	AL26	PEG RXP6 C	C143	EV@0.1U/10V_4	PEG_RXP6_4
PEX_TX9	AM26	PEG RXN6 C	C145	EV@0.1U/10V_4	PEG_RXN6_4
PEX_TX10	AM27	PEG RXP5 C	C144	EV@0.1U/10V_4	PEG_RXP5_4
PEX_TX10	AM28	PEG RXN5 C	C147	EV@0.1U/10V_4	PEG_RXN5_4
PEX_TX11	AL28	PEG RXP4 C	C160	EV@0.1U/10V_4	PEG_RXP4_4
PEX_TX11	AK28	PEG RXN4 C	C153	EV@0.1U/10V_4	PEG_RXN4_4
PEX_TX12	AK29	PEG RXP3 C	C162	EV@0.1U/10V_4	PEG_RXP3_4
PEX_TX12	AL29	PEG RXN3 C	C157	EV@0.1U/10V_4	PEG_RXN3_4
PEX_TX13	AM29	PEG RXP2 C	C165	EV@0.1U/10V_4	PEG_RXP2_4
PEX_TX13	AM30	PEG RXN2 C	C168	EV@0.1U/10V_4	PEG_RXN2_4
PEX_TX14	AM31	PEG RXP1 C	C167	EV@0.1U/10V_4	PEG_RXP1_4
PEX_TX14	AM32	PEG RXN1 C	C170	EV@0.1U/10V_4	PEG_RXN1_4
PEX_TX15	AN32	PEG RXP0 C	C171	EV@0.1U/10V_4	PEG_RXP0_4
PEX_TX15	AP32	PEG RXN0 C	C173	EV@0.1U/10V_4	PEG_RXN0_4

AG20	PEX_CAL_PU_GND/NC
A2	NC_1
AB7	NC_2
AD6	NC_3
AE5	NC_4
AG6	NC_5
AJ5	NC_6
AK15	NC_7
AL7	NC_8
E7	NC_11
H32	NC_13
M7	NC_14
P6	NC_15
U7	NC_18
V6	NC_19

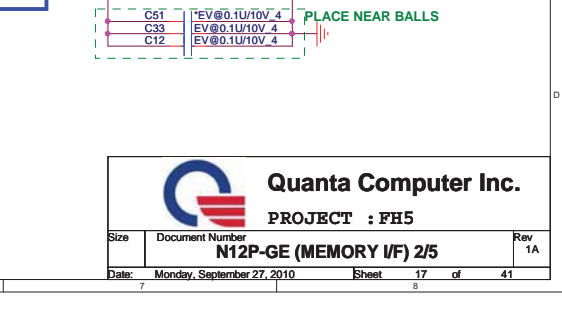
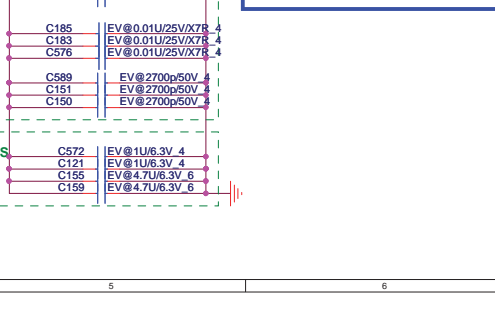
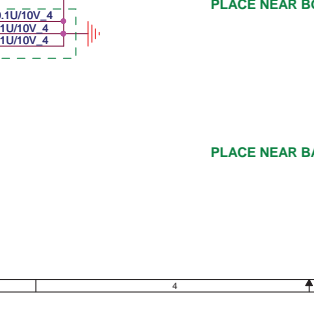
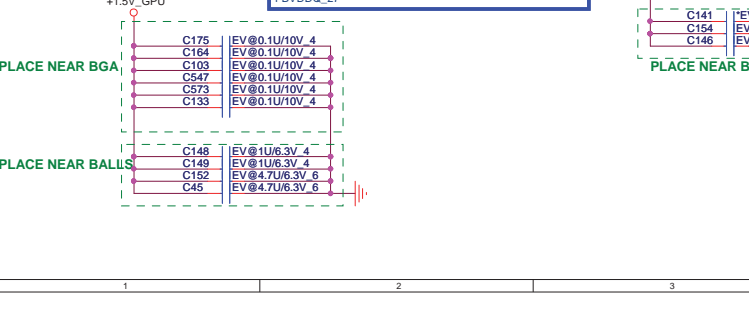
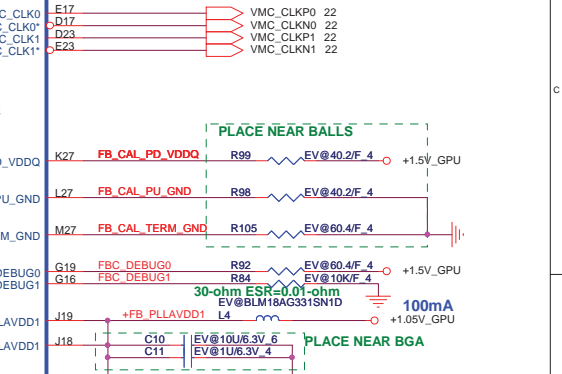
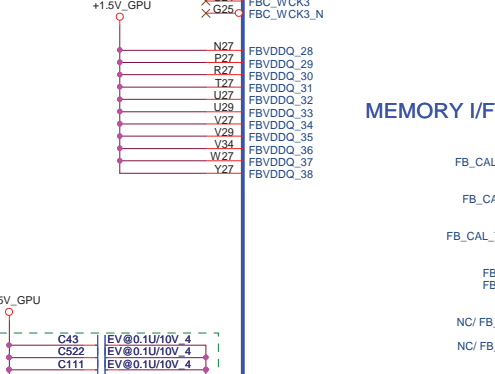
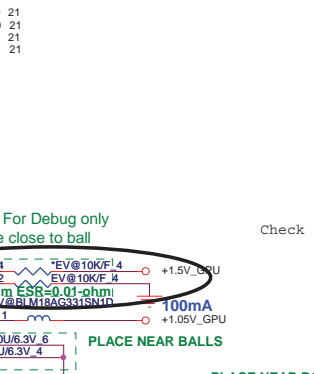
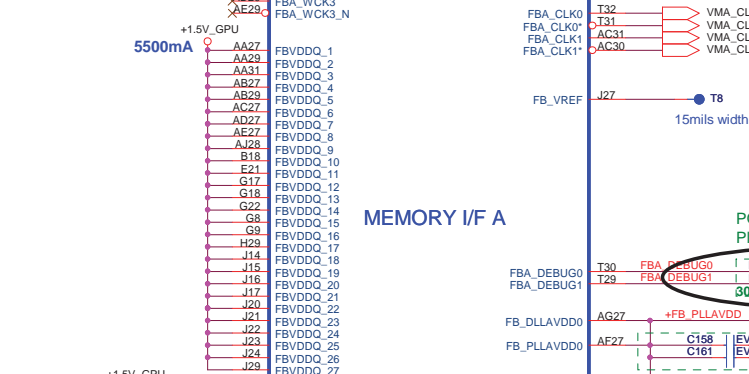
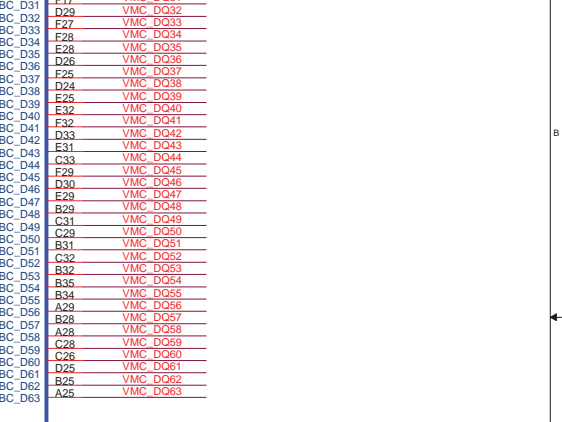
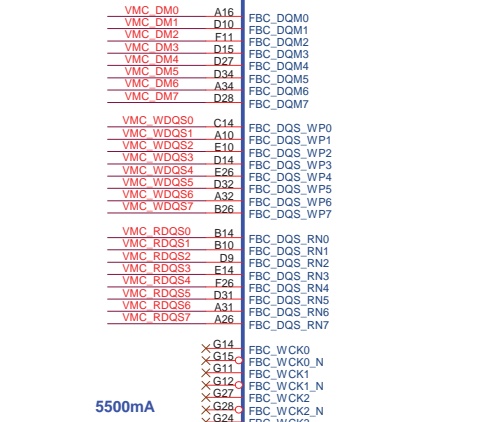
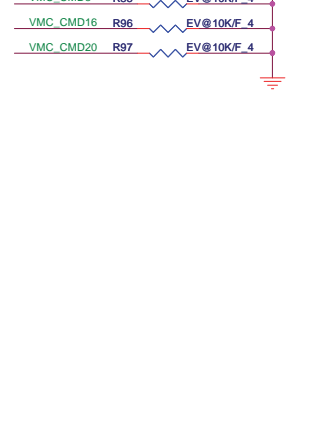
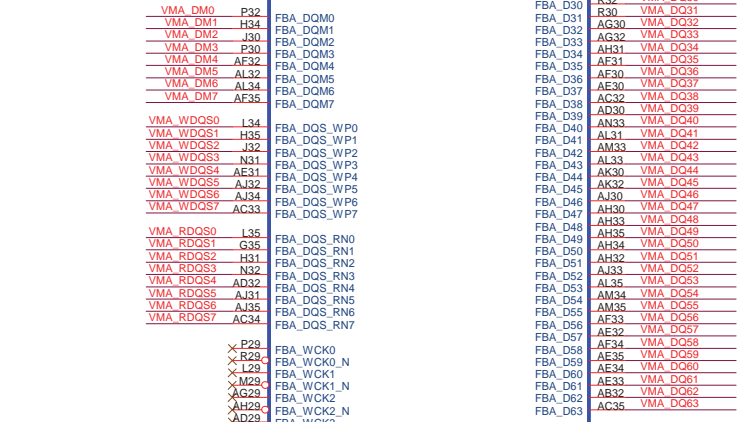
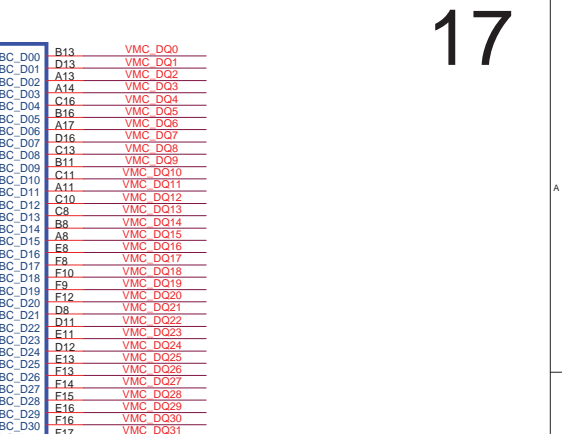
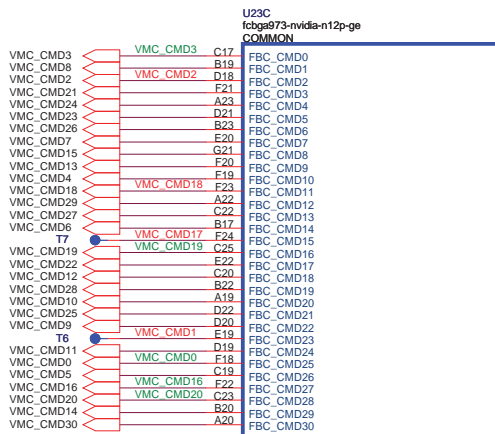
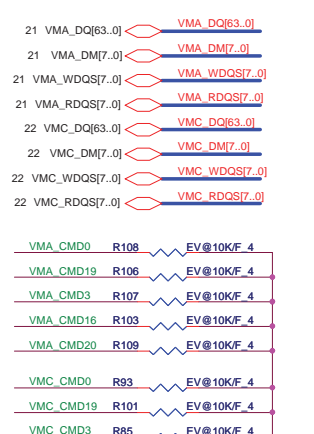
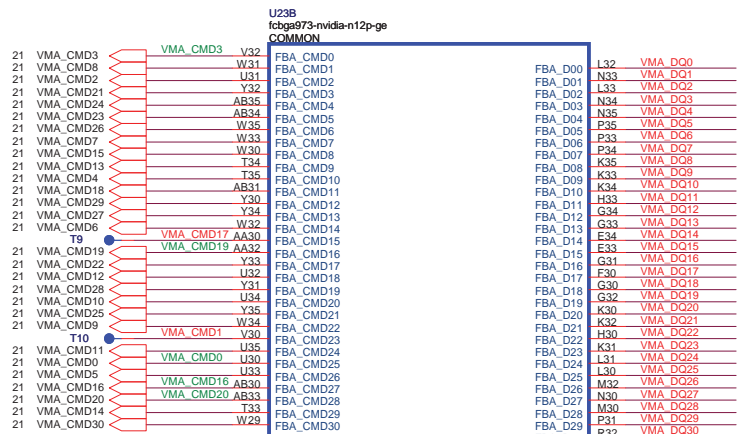
AR16	CLK_PCIE_VGAP	10
AR17	CLK_PCIE_VGAN	10
AJ17	PEX_TSTCLK	R89
AJ18	PEX_TSTCLK#	EV@200K/J_4
AM16	VGA_RST#	R87
AR13	PEX_CLKREQ#	R401
AG21	PEX_TERM	R94
AP35	TESTMODE	R110



GPU all PWROK



Ffor N12P-GE, they can be unstuffed by default



POP For Debug only
Place close to ball

30-ohm ESR=0.01-ohm
EV@BL18AG331SN1D

MEMORY I/F C

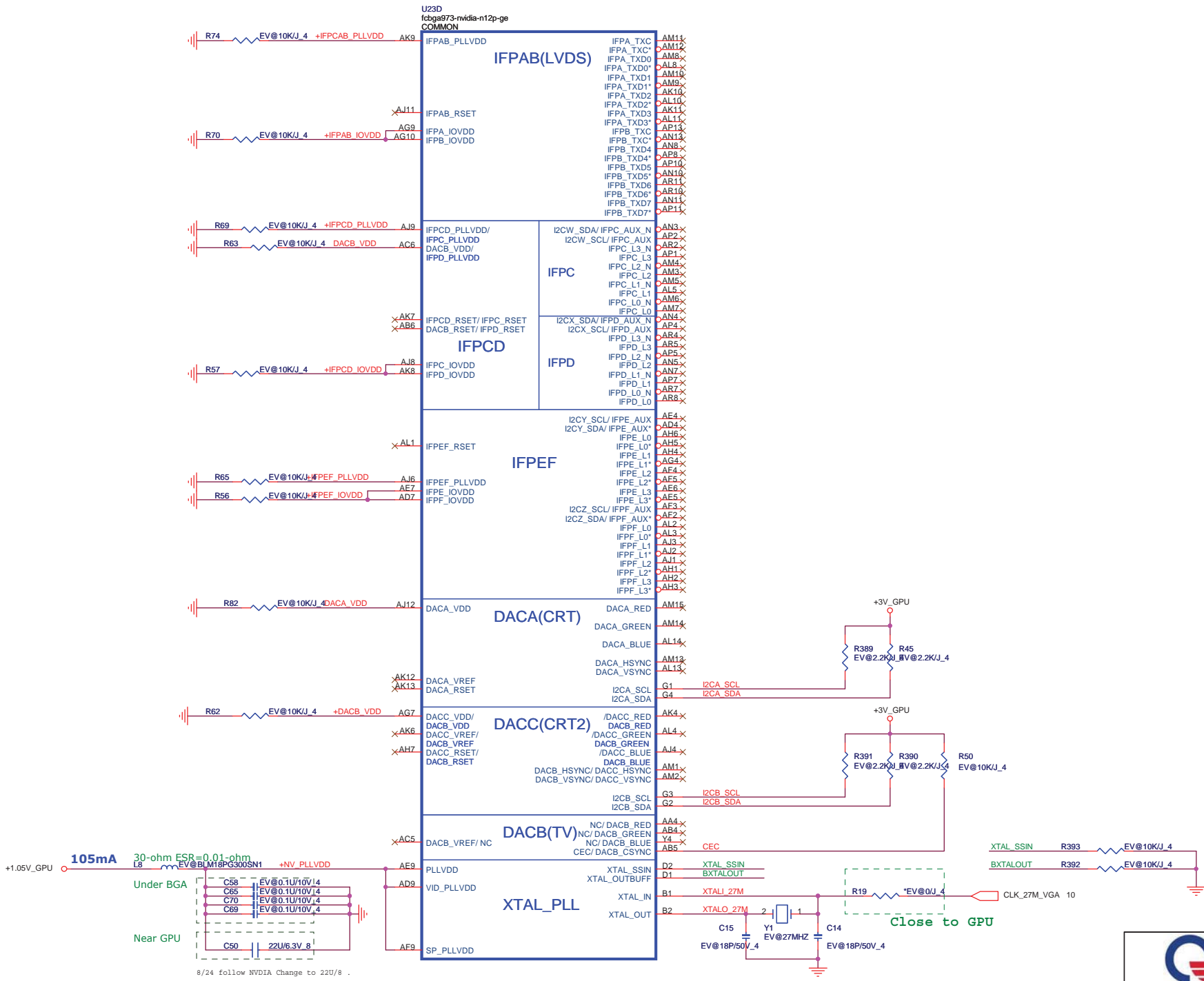
PLACE NEAR BALLS

PLACE NEAR BGA

PLACE NEAR BALLS

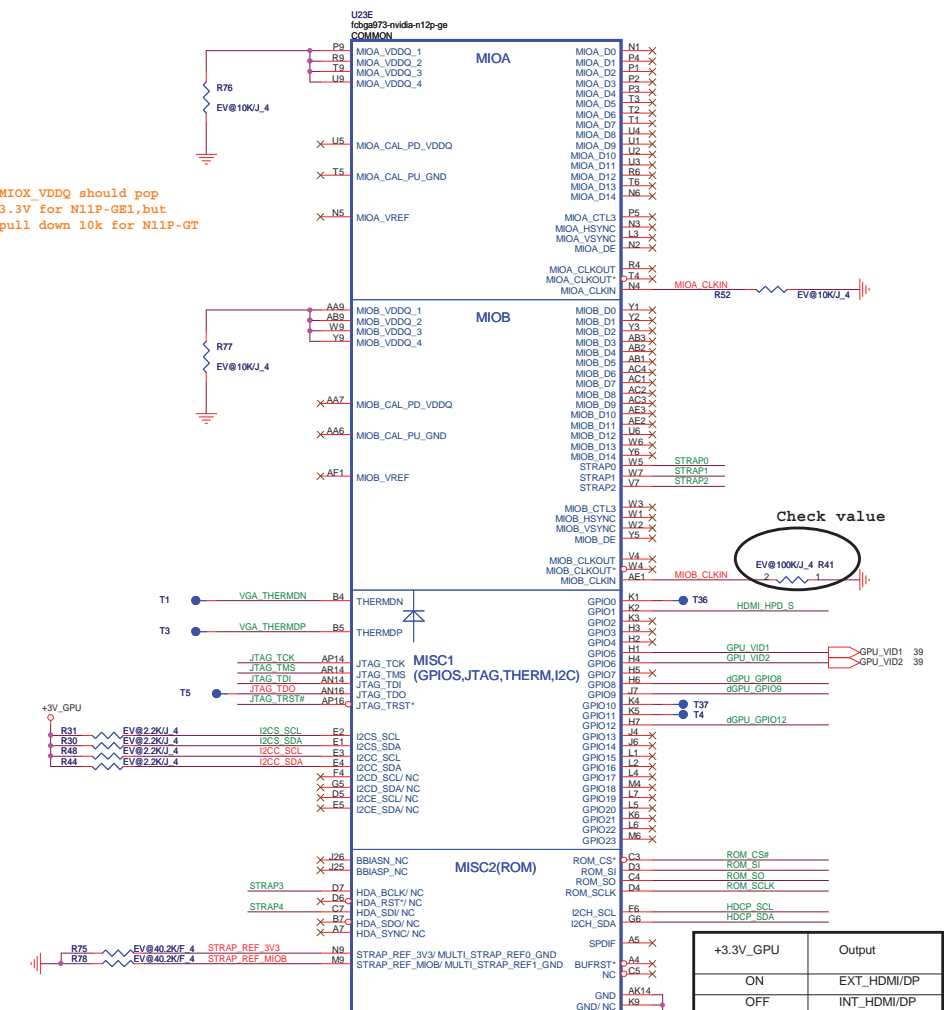
Quanta Computer Inc.
PROJECT : FH5
N12P-GE (MEMORY I/F) 2/5
Rev 1A

Size: Document Number: N12P-GE (MEMORY I/F) 2/5
Date: Monday, September 27, 2010 Sheet 17 of 41



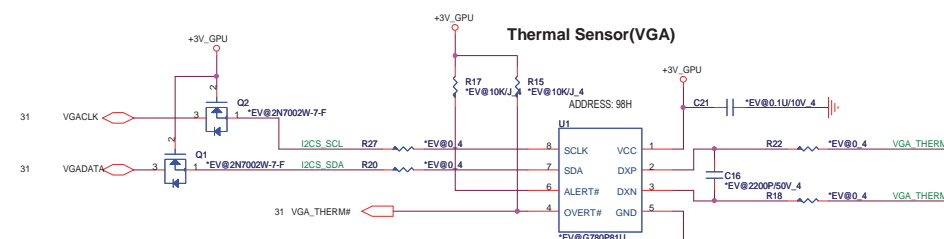
Quanta Computer Inc.
PROJECT : FH5

Size	Document Number	Rev
	N12P-GE (DISPLAY) 3/5	1A
Date:	Monday, September 27, 2010	Sheet 18 of 41



MIOX_VDDQ should pop 3.3V for N11P-GE1, but pull down 10k for N11P-GT

Check value EV@10KJ_4 R41 2 1



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0011
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVIDE[3]	PCI_DEVIDE[2]	PCI_DEVIDE[1]	PCI_DEVIDE[0]	0101
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	TBD
STRAP4	Reserve	Reserve	PCI_MAX_SPEED	DP_PLL_VDD3	TBD

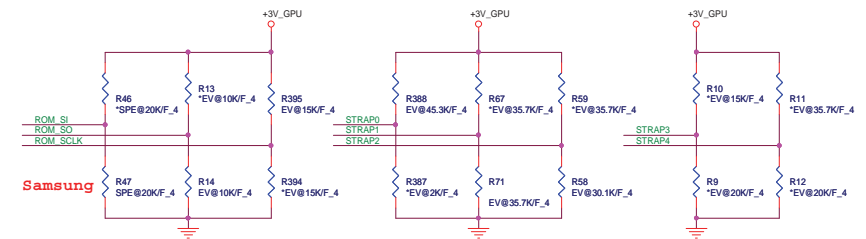
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKDSLGH500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKDSLZWTW01	AKDSLZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT502	K4W2G1646E-HC12

4.99K/F_4 ==> CS24992FB26
 10K/F_4 ==> CS31002FB26
 15K/F_4 ==> CS31502FB24
 20K/F_4 ==> CS32002FB29
 30.1K/F_4 ==> CS33012FB18
 35.7K/F_4 ==> CS33572FB13
 45.3K/F_4 ==> CS34532FB18

ROM_SI Strap Bit for RAM Mapping



N11P-GE1 DevID is 0x0DFE, so pull up ROM_SCLK with 15Kohm and STRAP2 pull up 35Kohm

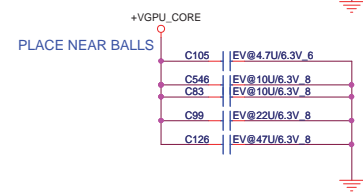
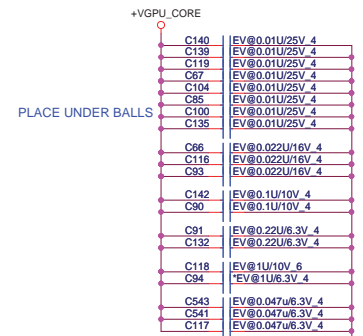
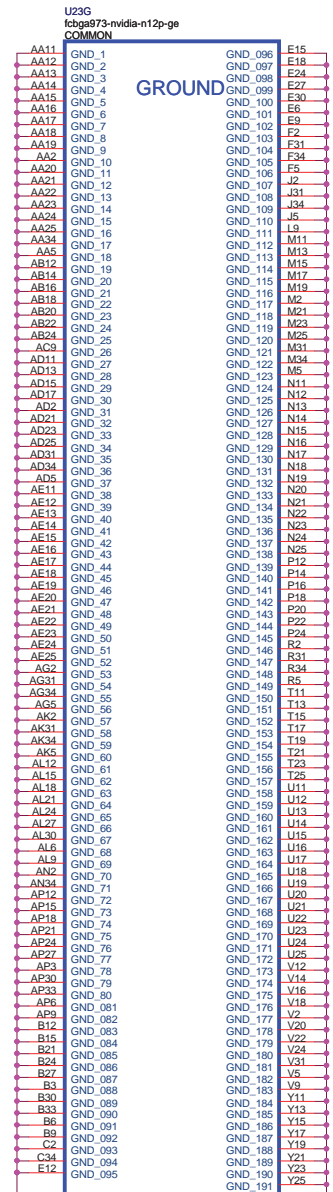
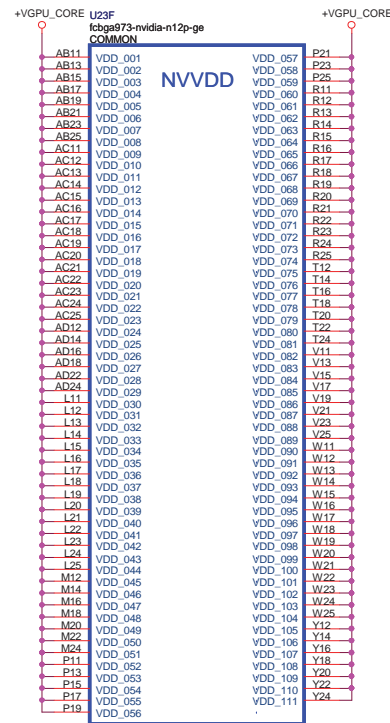
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVRT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

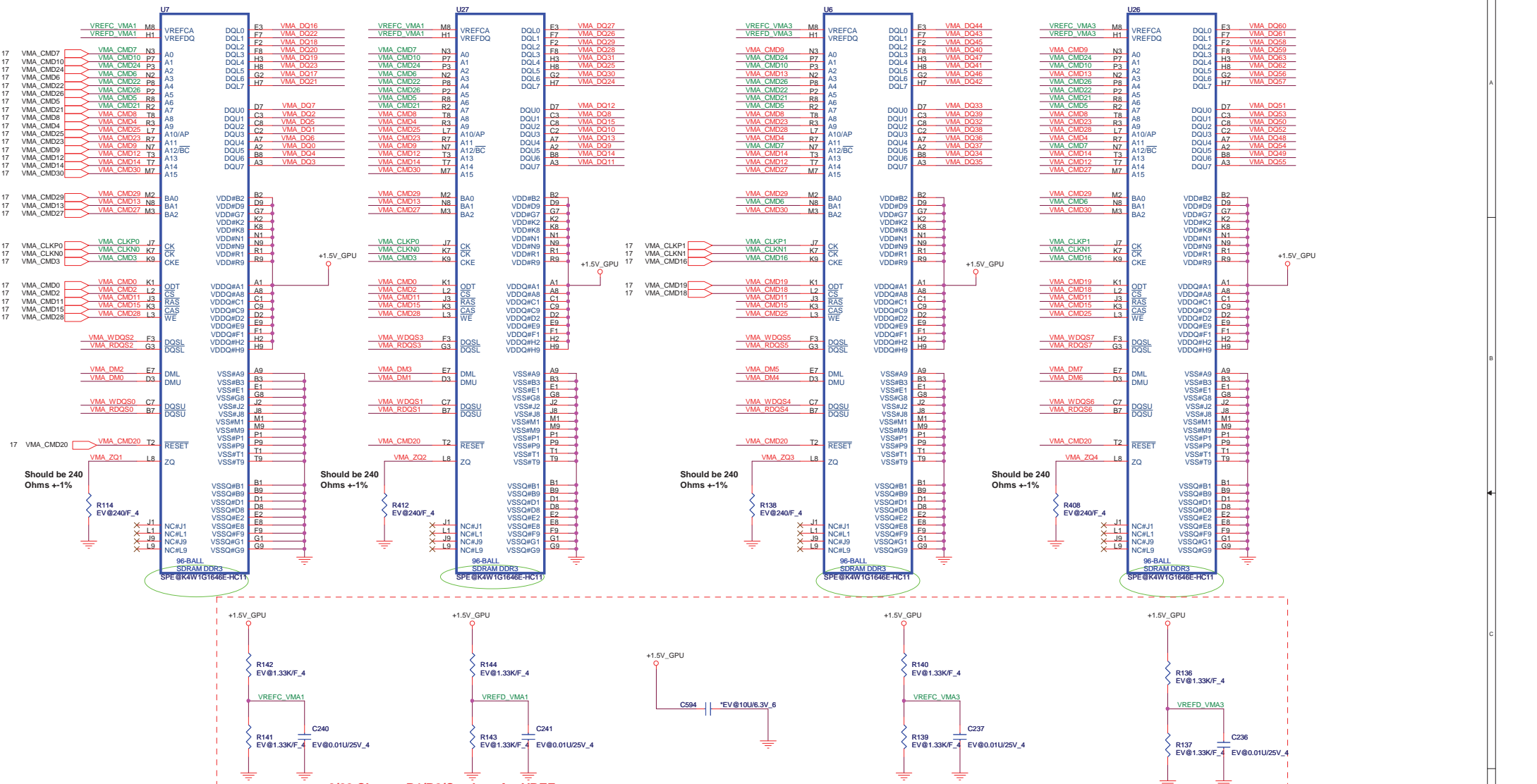
NV VID Table for N12P-GE

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	0.825V
1	0	0.9V
0	1	0.95V
1	1	TBD

Modify 8/18

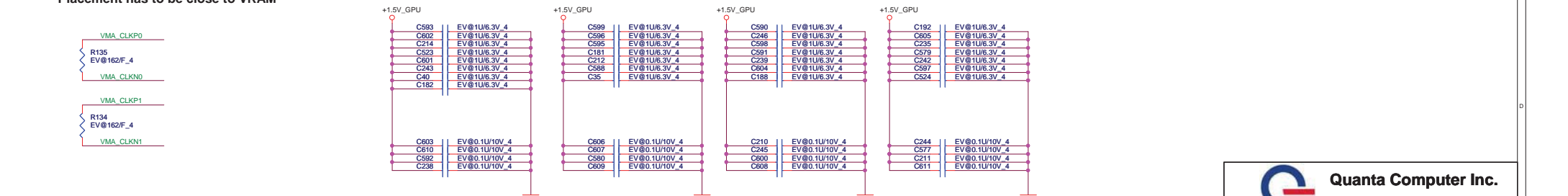


CHANNEL A: 512MB/1024MB DDR3



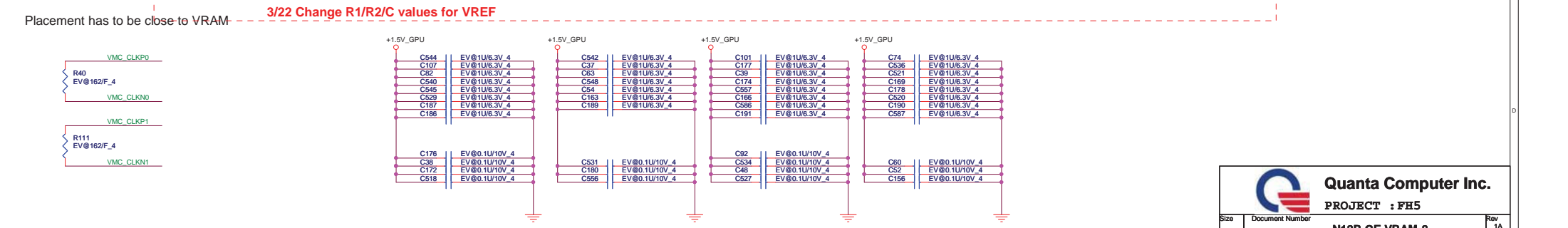
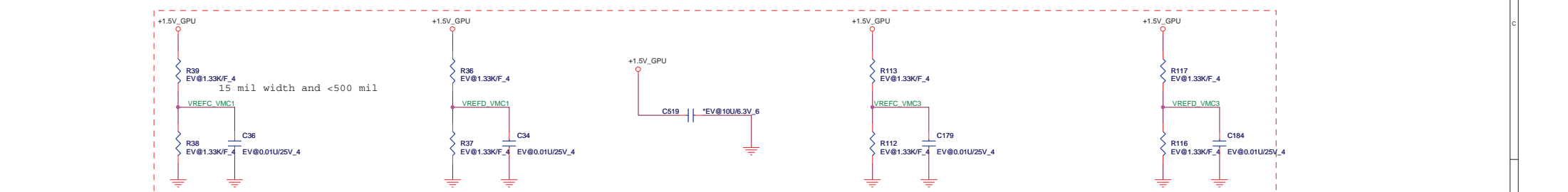
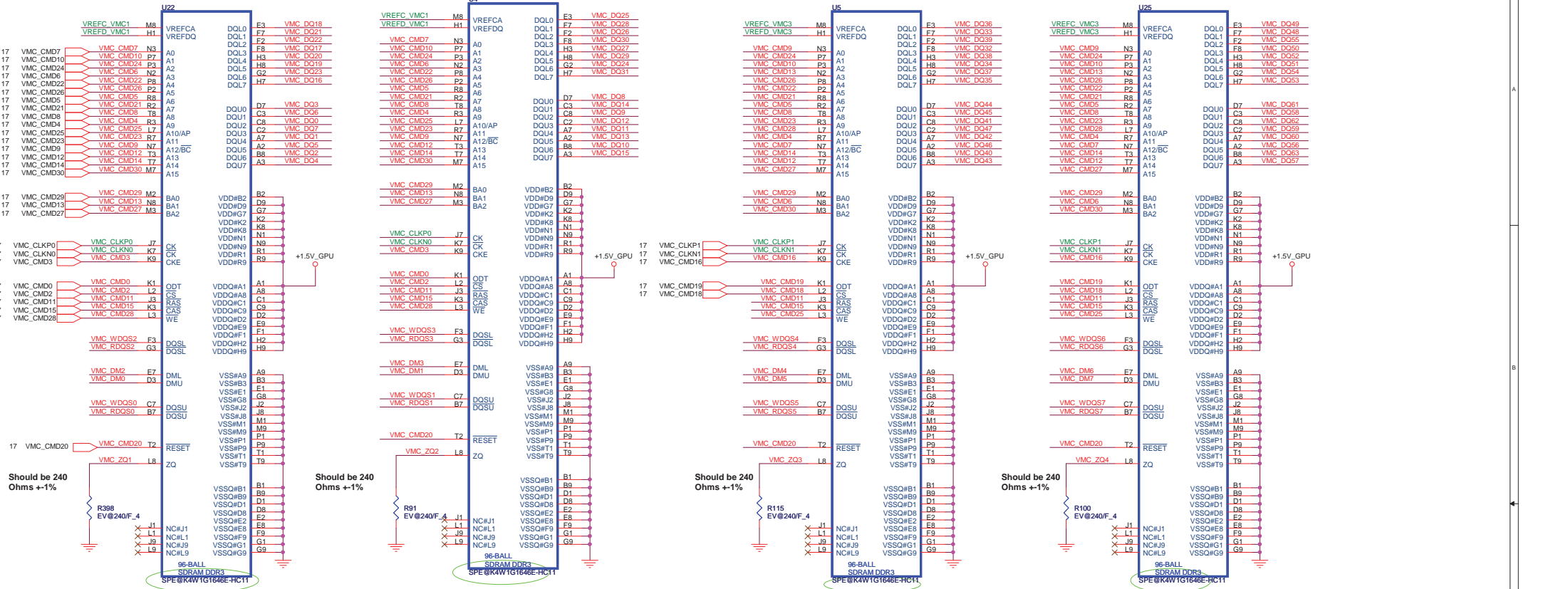
Placement has to be close to VRAM

3/22 Change R1/R2/C values for VREF



GE1 FOR 243 BUT GT/E REQUIRE CHECK FAE

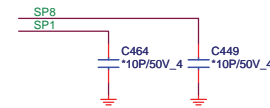
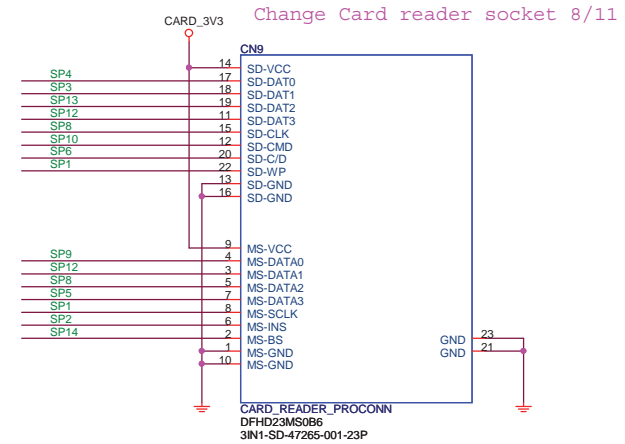
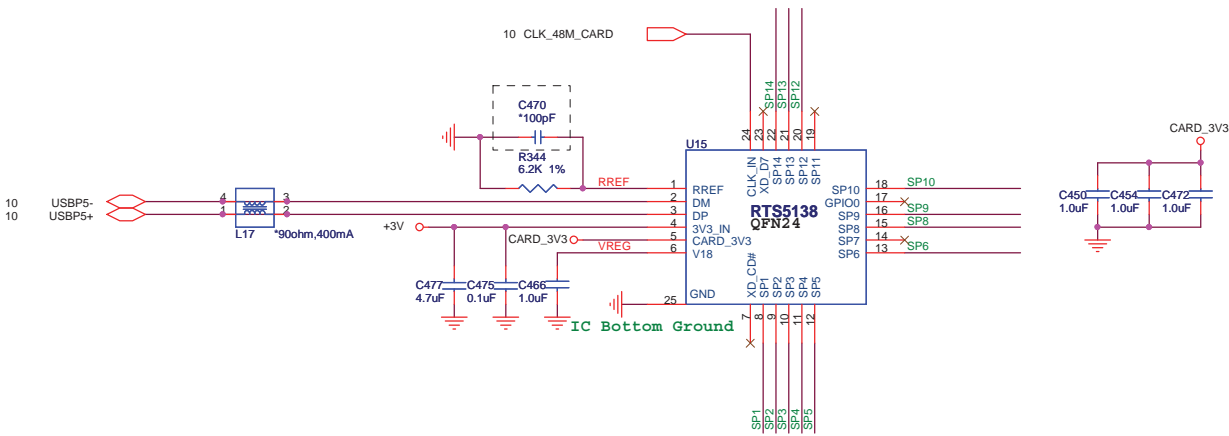
CHANNEL B: 512MB/1024MB DDR3



RST5138 SIDO

SD/SDHC CARD READER

SD/MS CONNDETOR

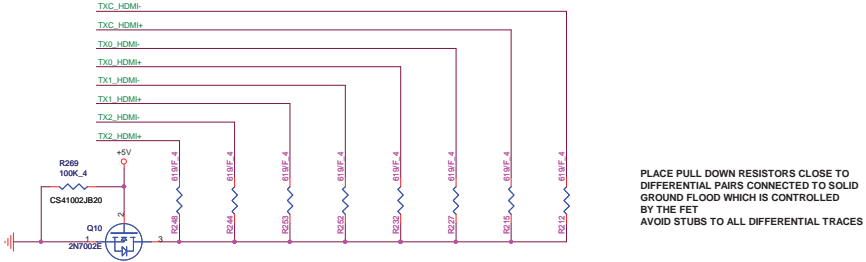
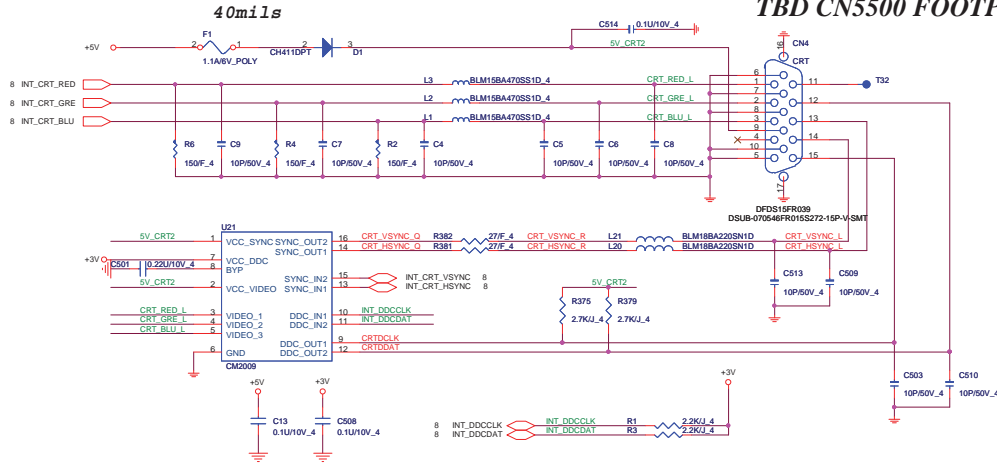


Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	

CRT CONN/DDC LEVEL SHIFT

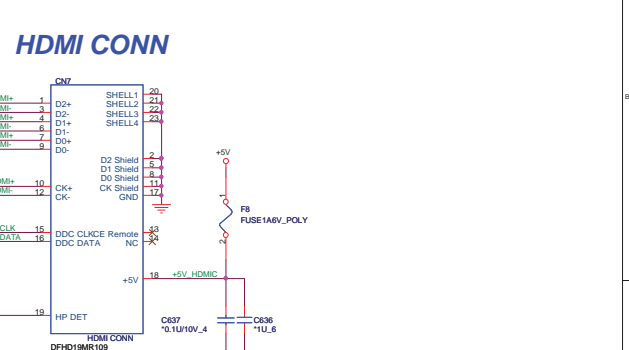
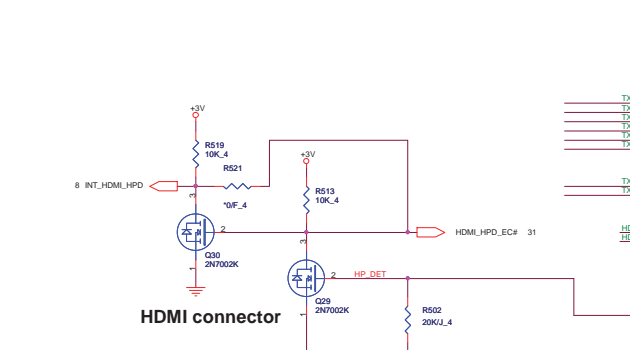
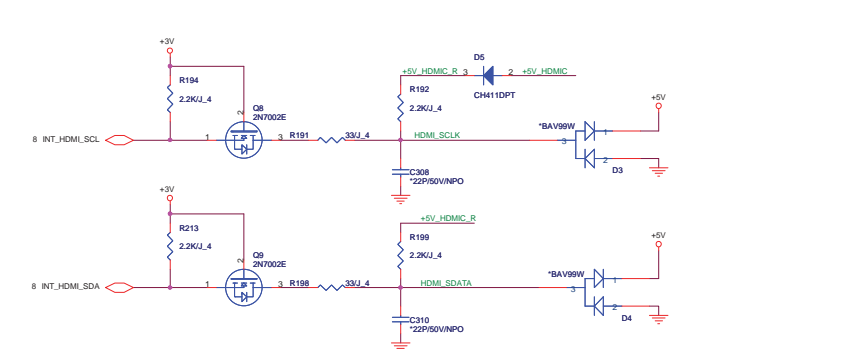
TBD CN5500 FOOTPRINT



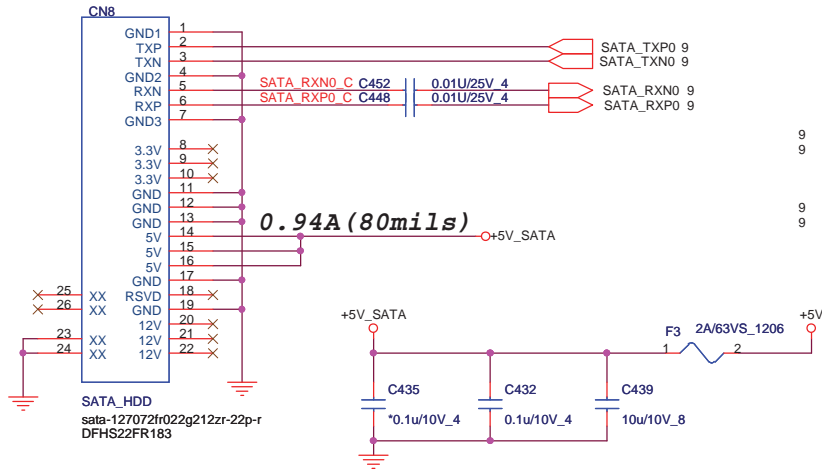
INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR

8 INT_HDMI_TXCN	INT_HDMI_TXCN	C311	0.1u/10V_4	TXC_HDMI+
8 INT_HDMI_TXCP	INT_HDMI_TXCP	C312	0.1u/10V_4	TXC_HDMI-
8 INT_HDMI_TXDN0	INT_HDMI_TXDN0	C327	0.1u/10V_4	TX0_HDMI+
8 INT_HDMI_TXDP0	INT_HDMI_TXDP0	C329	0.1u/10V_4	TX0_HDMI-
8 INT_HDMI_TXDN1	INT_HDMI_TXDN1	C313	0.1u/10V_4	TX1_HDMI+
8 INT_HDMI_TXDP1	INT_HDMI_TXDP1	C318	0.1u/10V_4	TX1_HDMI-
8 INT_HDMI_TXDN2	INT_HDMI_TXDN2	C320	0.1u/10V_4	TX2_HDMI+
8 INT_HDMI_TXDP2	INT_HDMI_TXDP2	C323	0.1u/10V_4	TX2_HDMI-



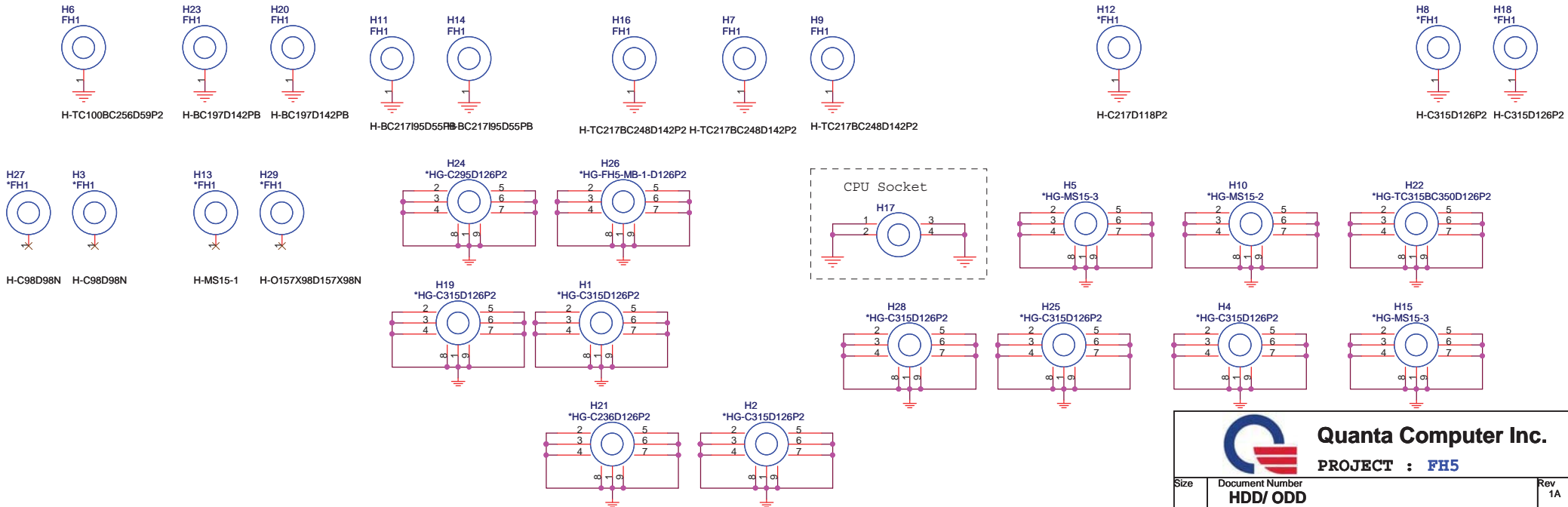
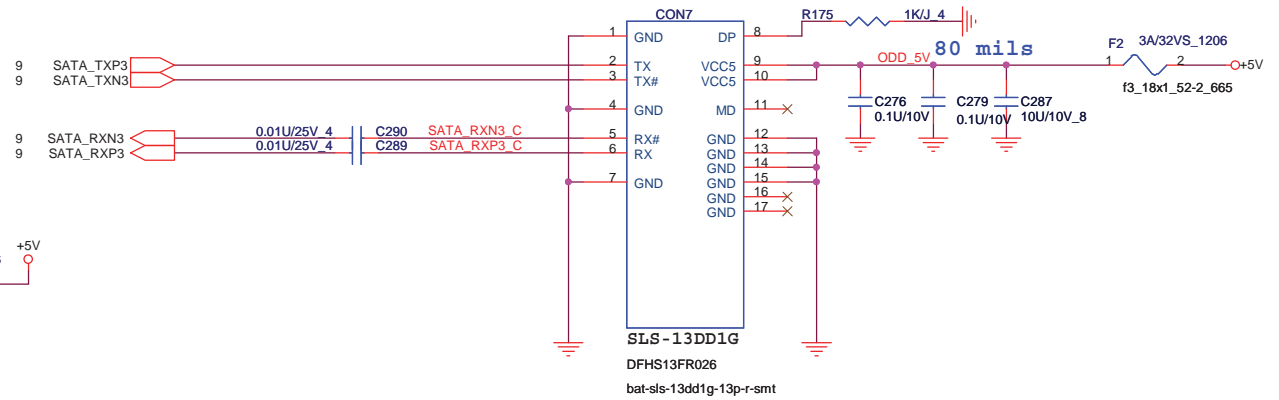
2.5" SATA HDD



SATA ODD

25

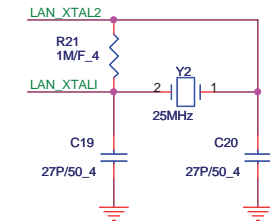
ODD CONN



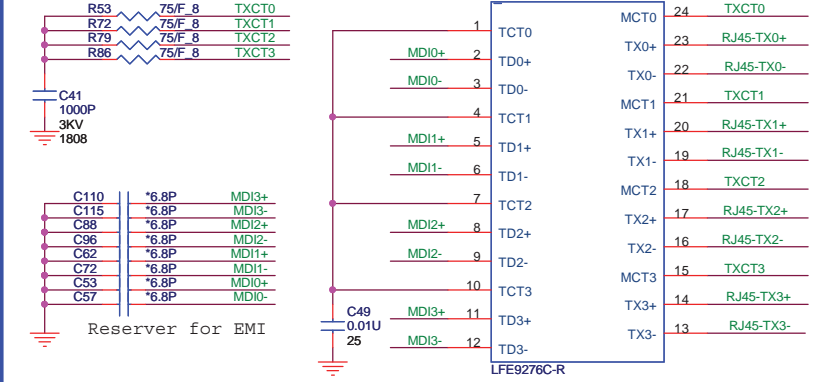
Quanta Computer Inc. PROJECT : FH5		Size	Document Number	Rev
		HDD/ ODD		1A
Date:	Monday, September 27, 2010	Sheet	25 of 41	

LAN EEPROM(DEL)

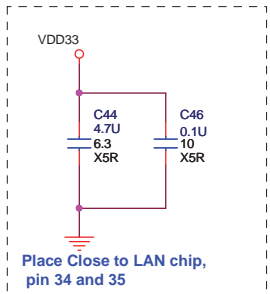
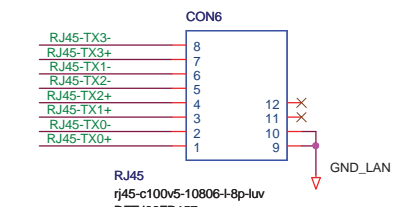
X'tal 25MHz



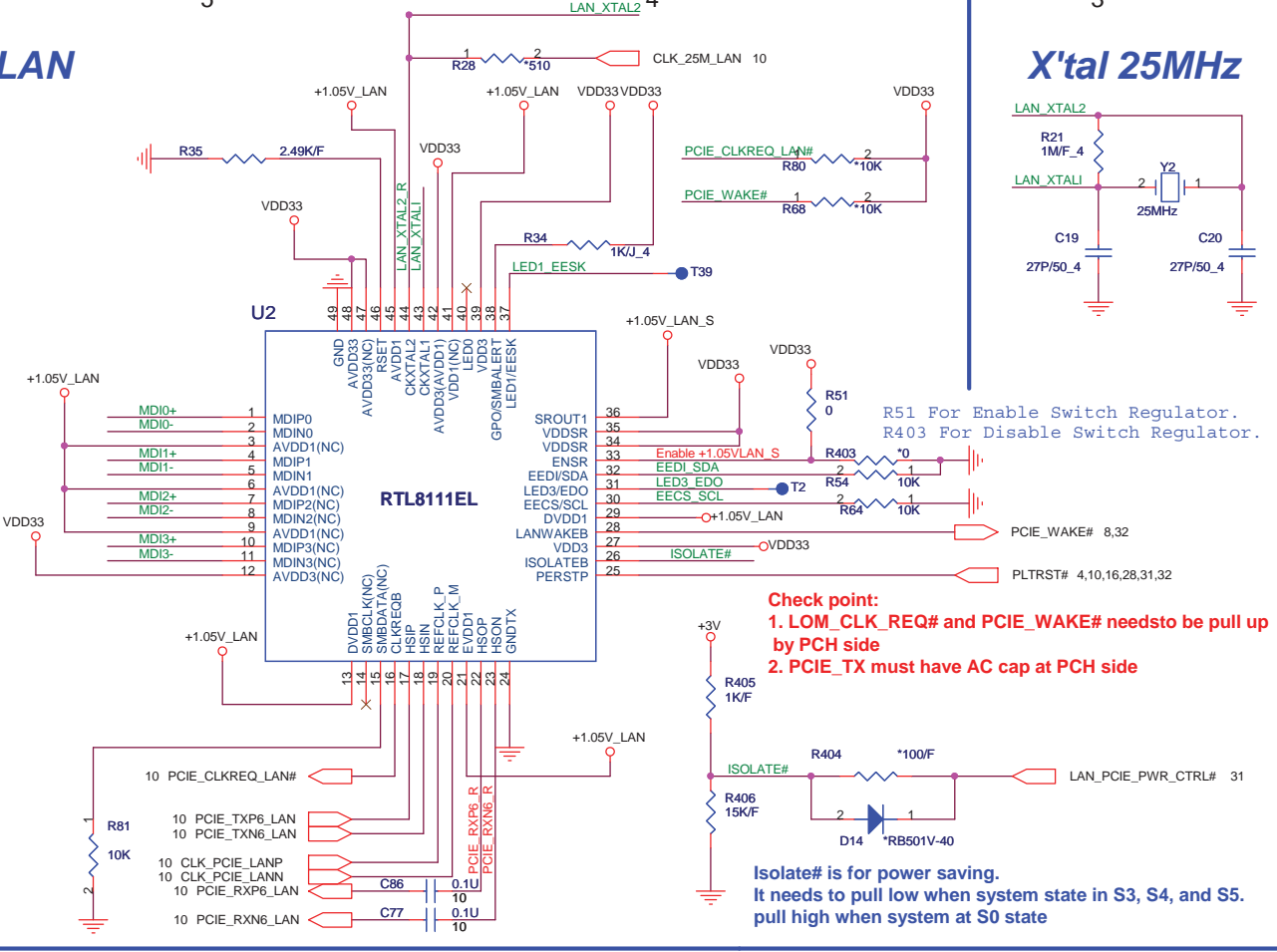
Transformer



RJ45



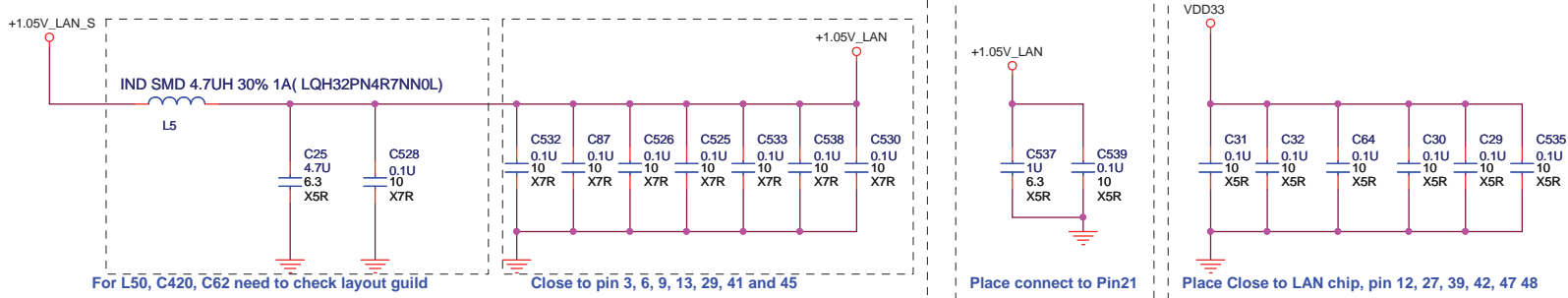
LAN



Check point:
 1. LOM_CLK_REQ# and PCIE_WAKE# need to be pull up by PCH side
 2. PCIE_TX must have AC cap at PCH side

Isolate# is for power saving.
 It needs to pull low when system state in S3, S4, and S5. pull high when system at S0 state

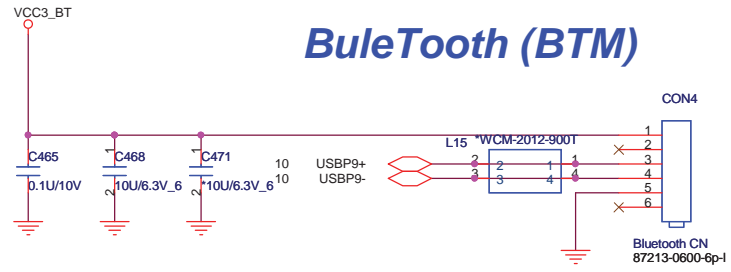
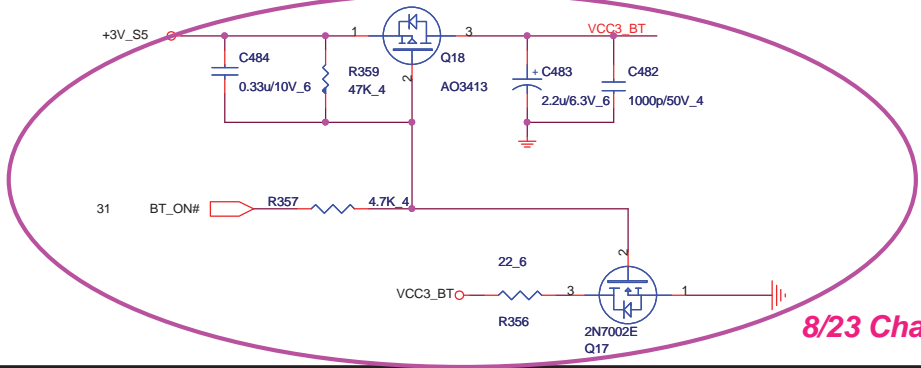
LAN Power



For L50, C420, C62 need to check layout guid
 Close to pin 3, 6, 9, 13, 29, 41 and 45
 Place connect to Pin21
 Place Close to LAN chip, pin 12, 27, 39, 42, 47 48

REQ by layout

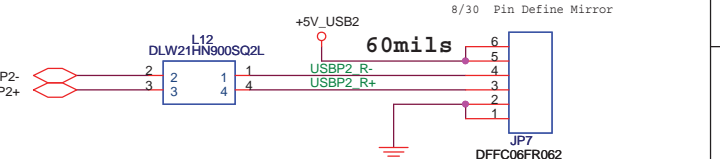
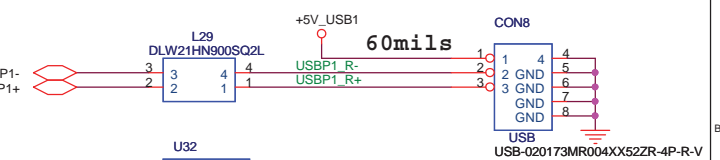
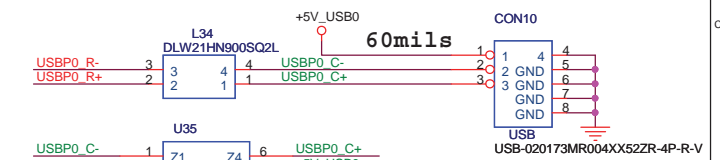
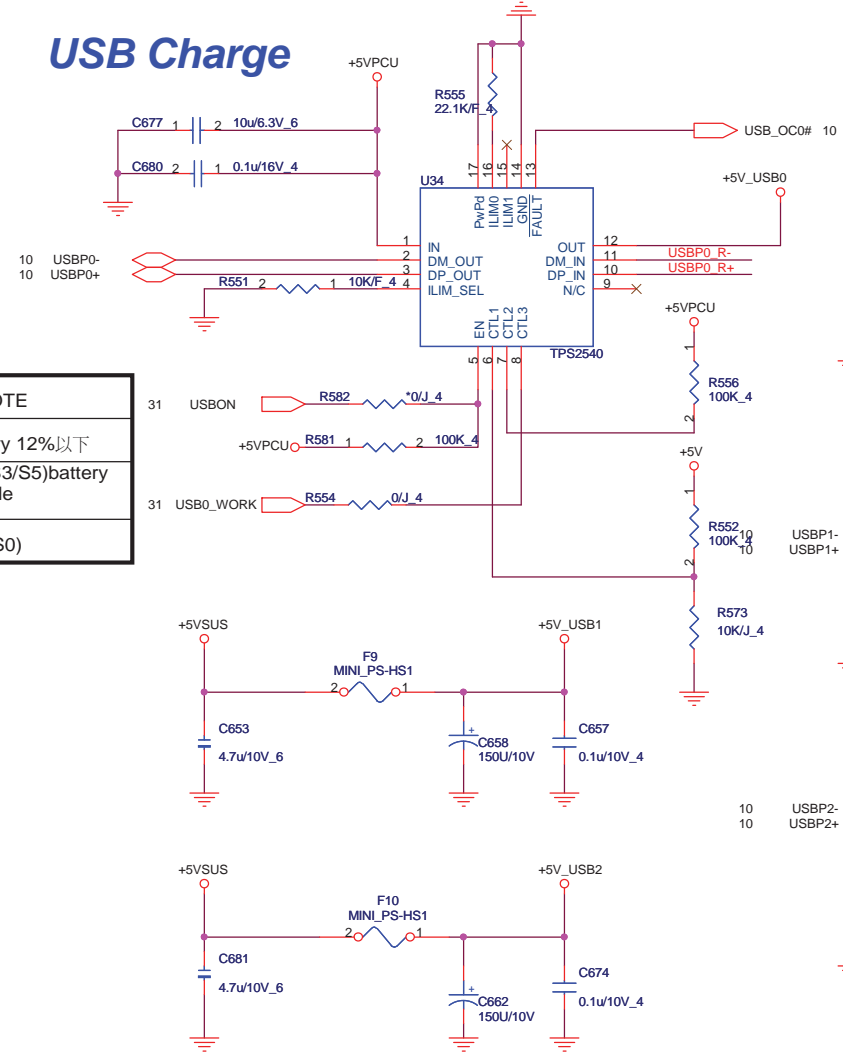
Quanta Computer Inc.
 PROJECT : FH5
 LAN_RTL8111E-GR/RJ45
 Rev 1A



8/23 Change BT on circuit.

USB Connector

USB Charge



	CTL1	CTL2	CTL3	NOTE
ES(PG1.1)	0	1	0	SDP(S3/S5)battery 12%以下
	0	1	1	DCP, Auto-detect(S3/S5)battery 12%以上 or AC mode
	1	1	0	SDP(S0)

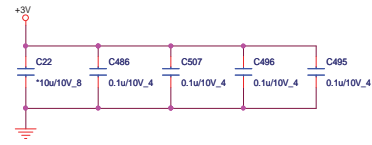
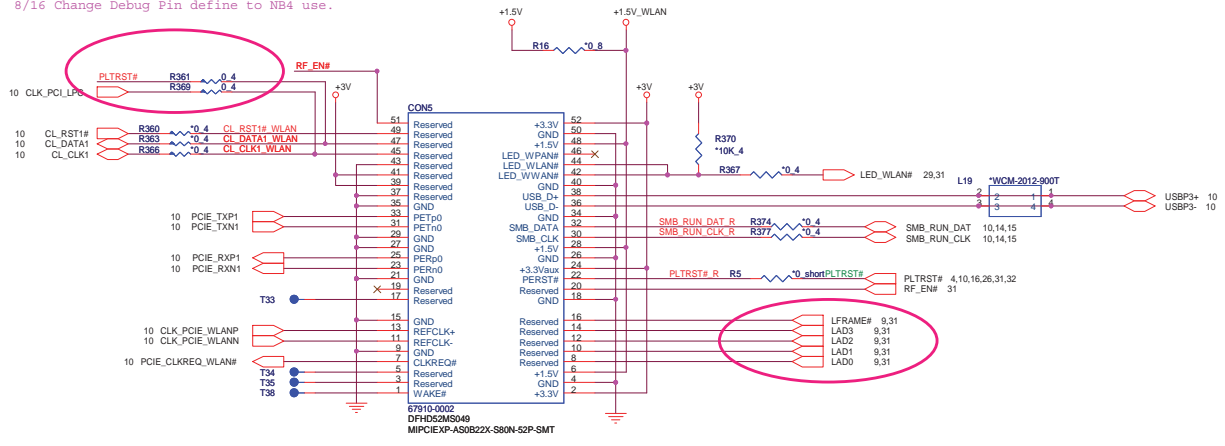
USB0_WORK	Mode
Low - S5 - 1.8A	DCP, Auto-detect
High - S0/S3 - 1.5A USB wake up with S3	CDP, BC Spec 1.1 == PCH HOST

	R321	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

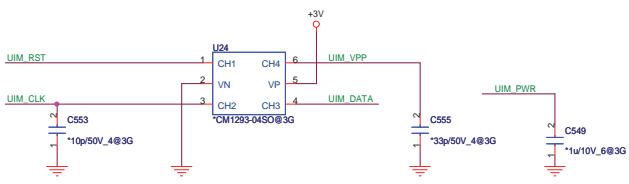
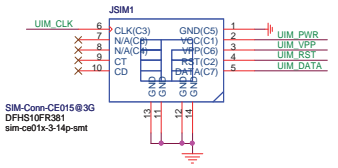
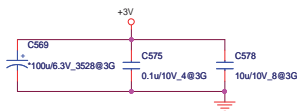
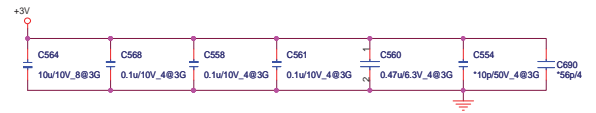
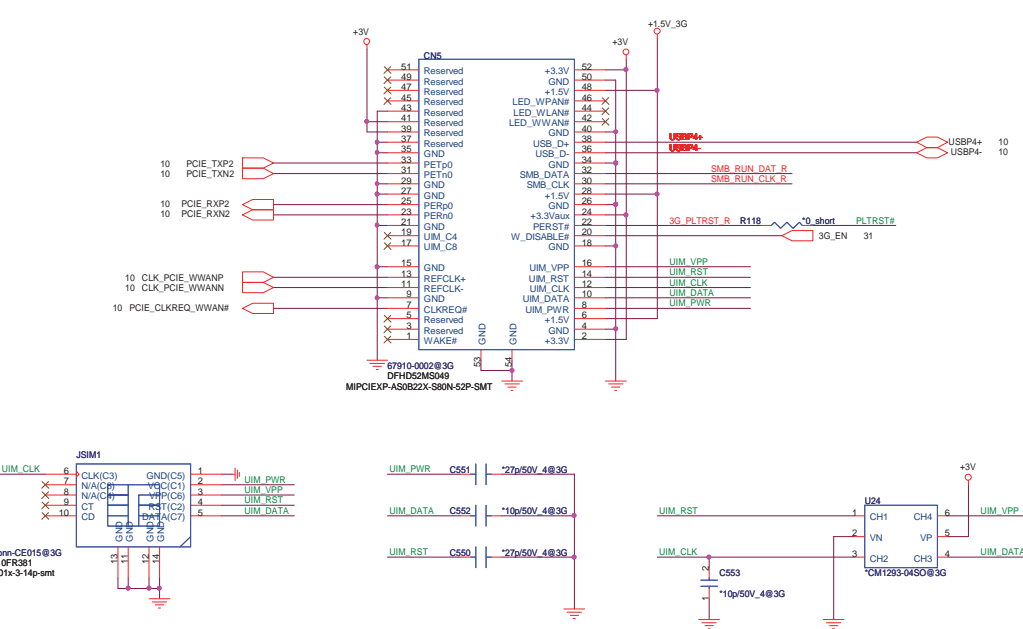
Applied Now

MINI CARD (WLAN)

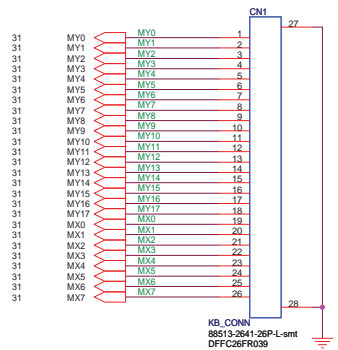
8/16 Change Debug Pin define to NB4 use.



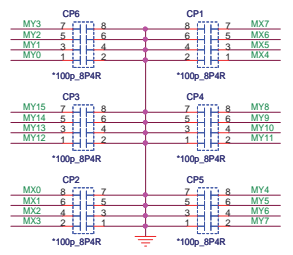
Mini Card2-3G(MNC)



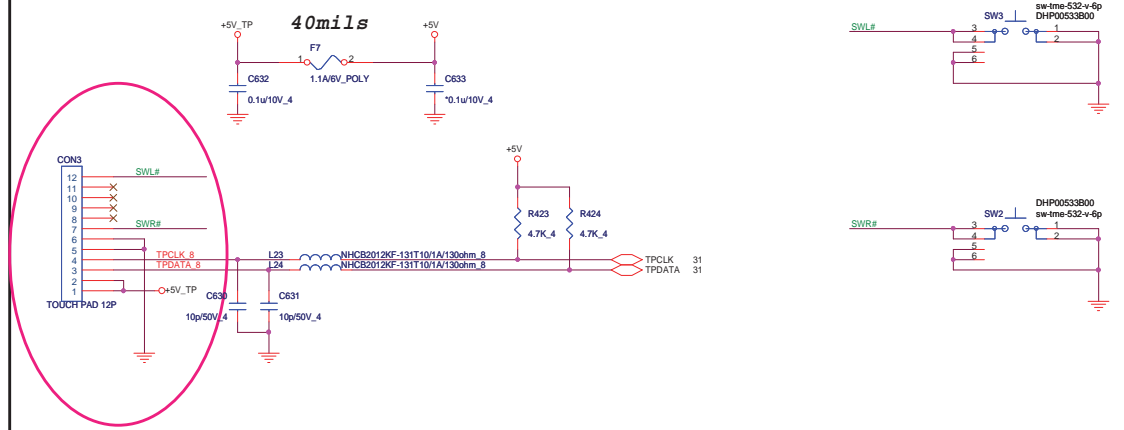
Keyboard(KBC)



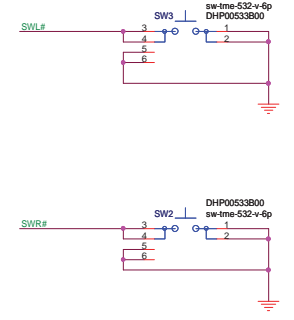
For EMI Reserve Caps for debug



Touch Pad

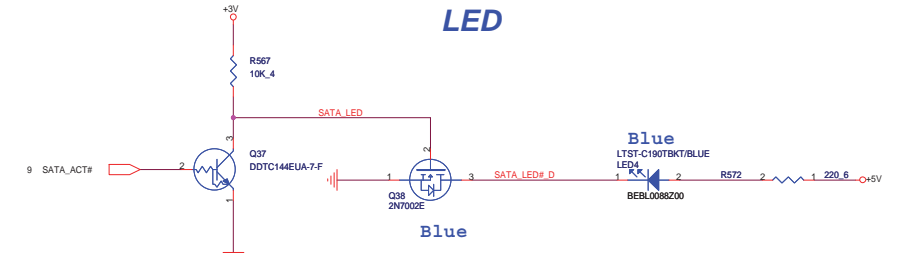


8/23 Change TP to 12 pin conn.



LED

HDD/ODD



CAPS LED



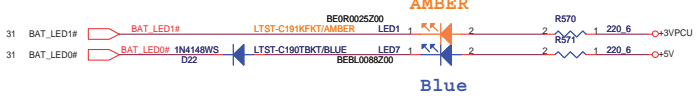
NUM LED



WLAN

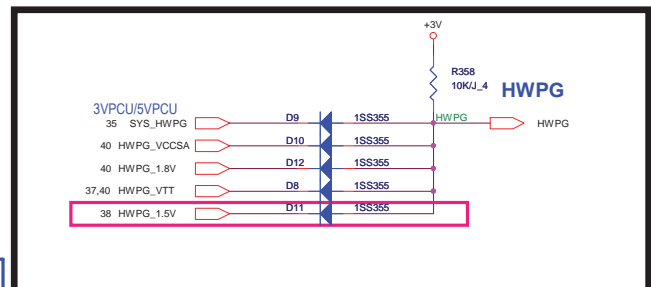
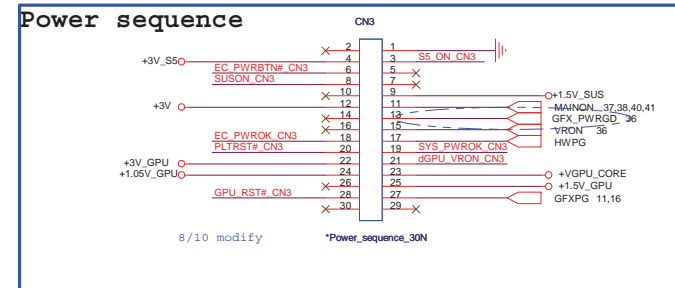
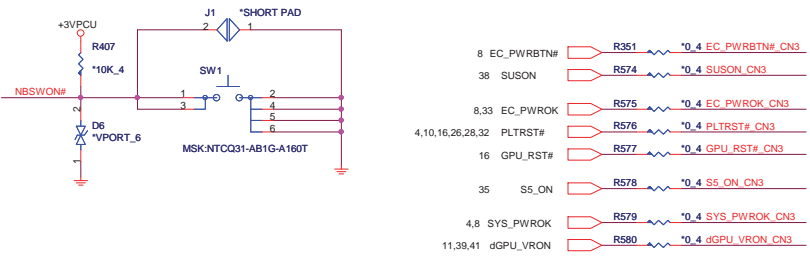
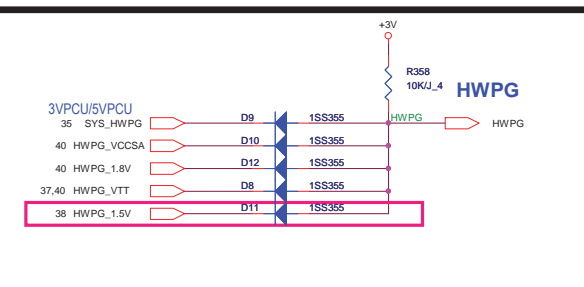
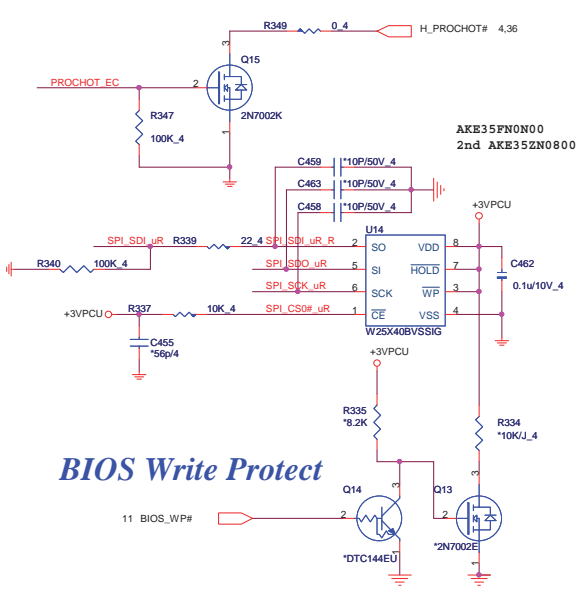
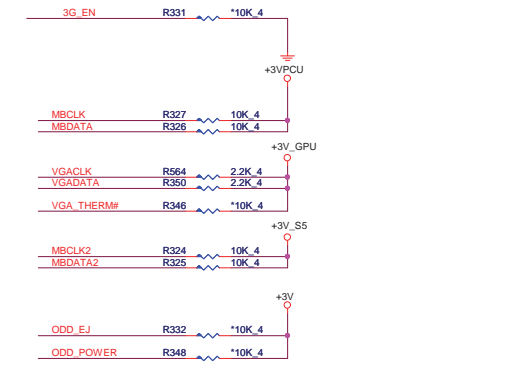
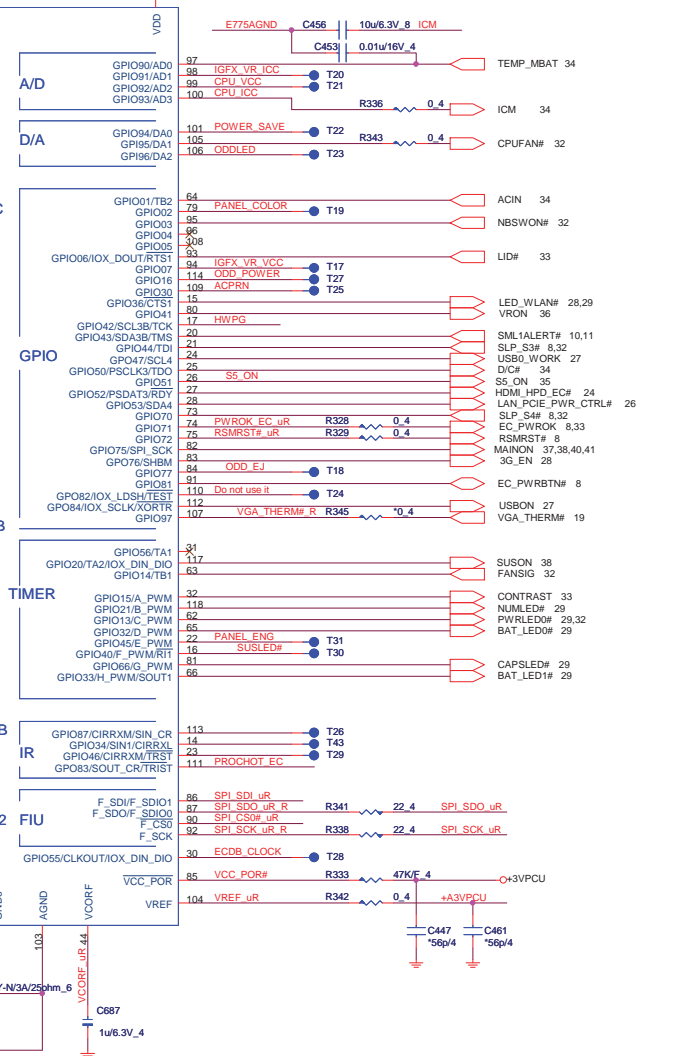
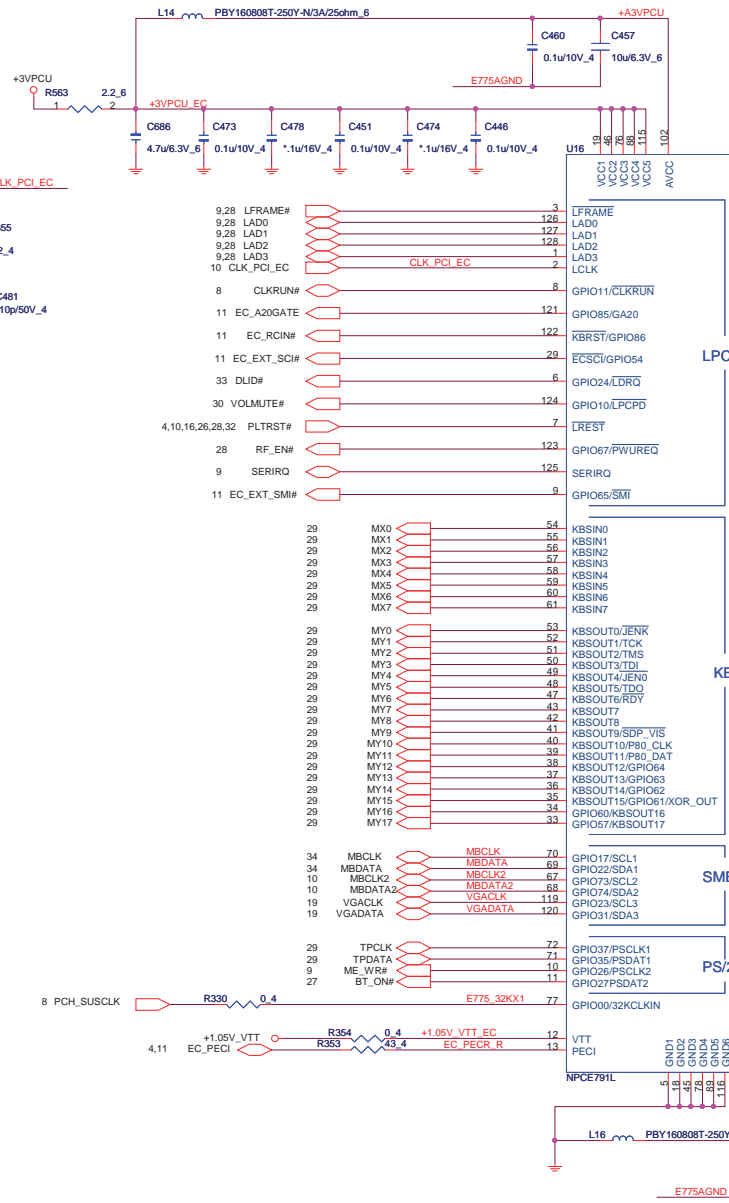


Battery



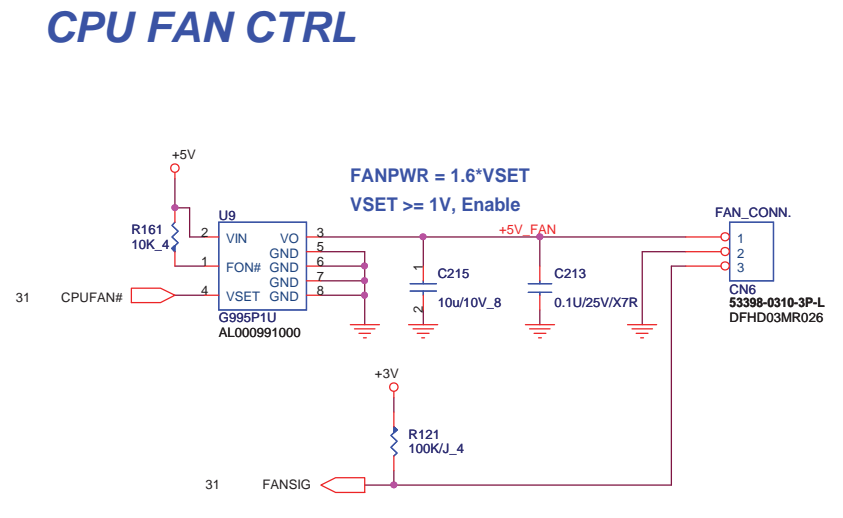
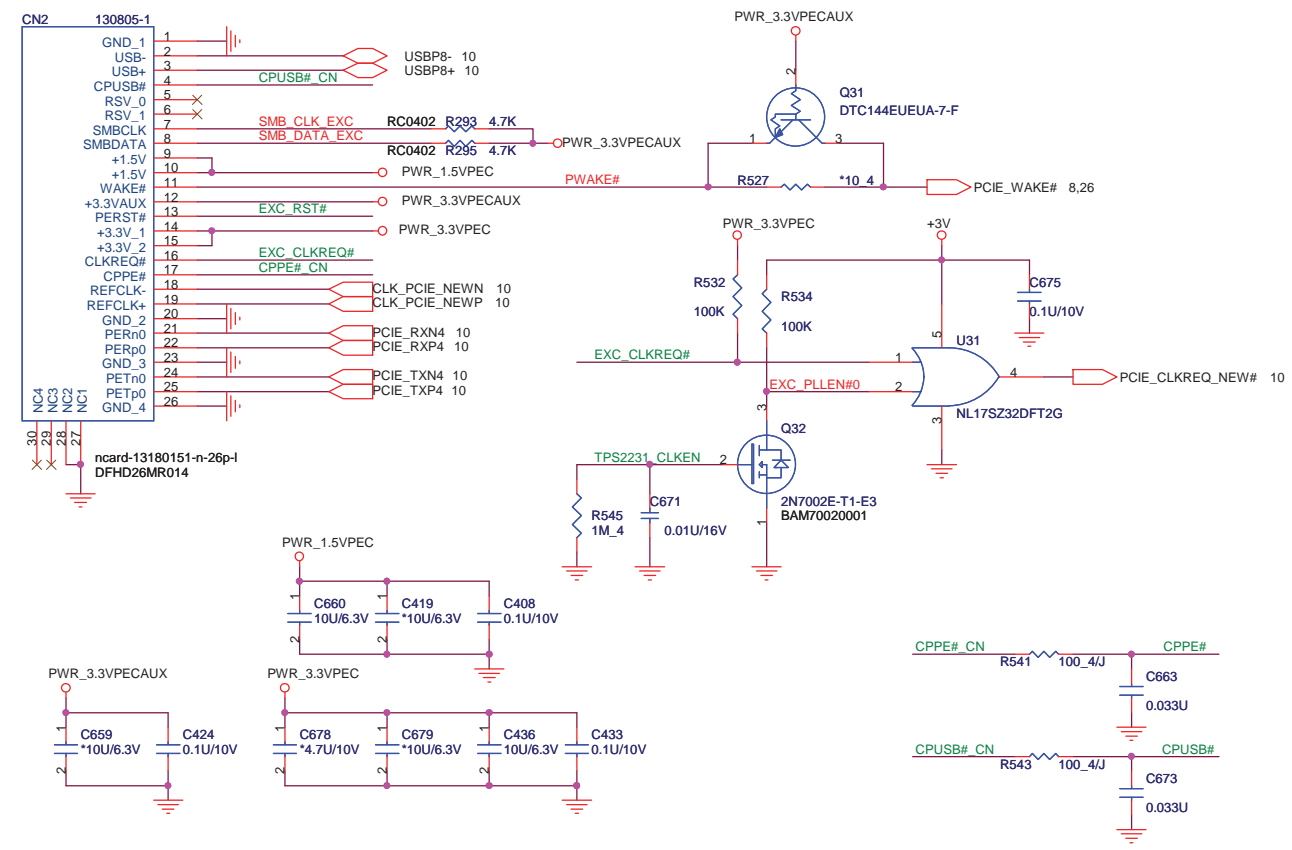
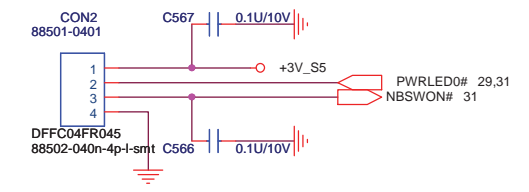
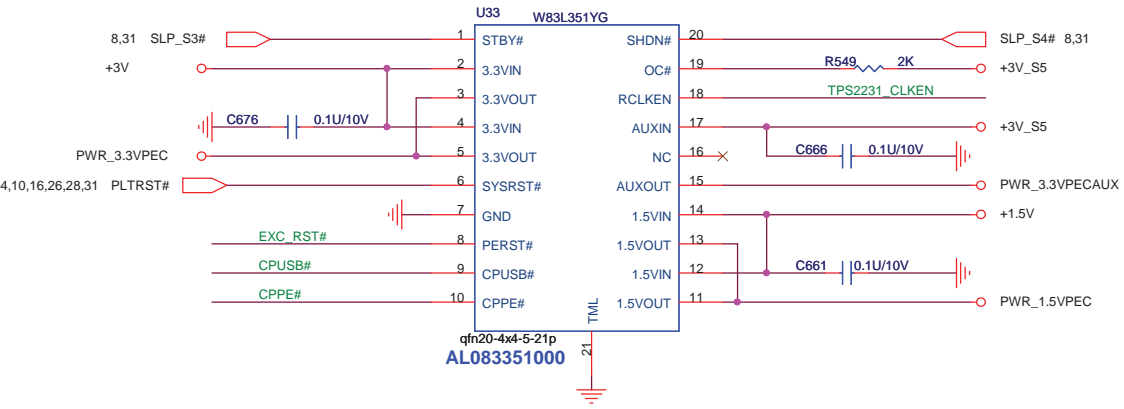
Power Status





NEW CARD

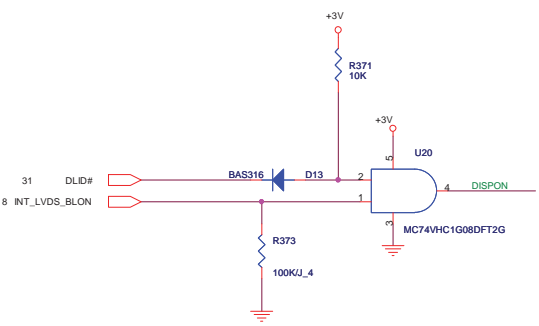
PW BOARD CON



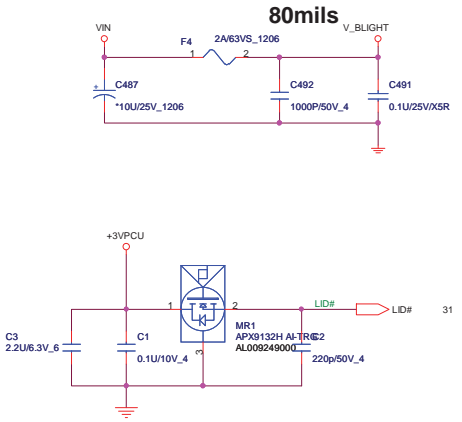
Quanta Computer Inc.
PROJECT : FH5

Size	Document Number	Rev
	FAN/SW/NEWCARD	1A
Date:	Monday, September 27, 2010	Sheet 32 of 41

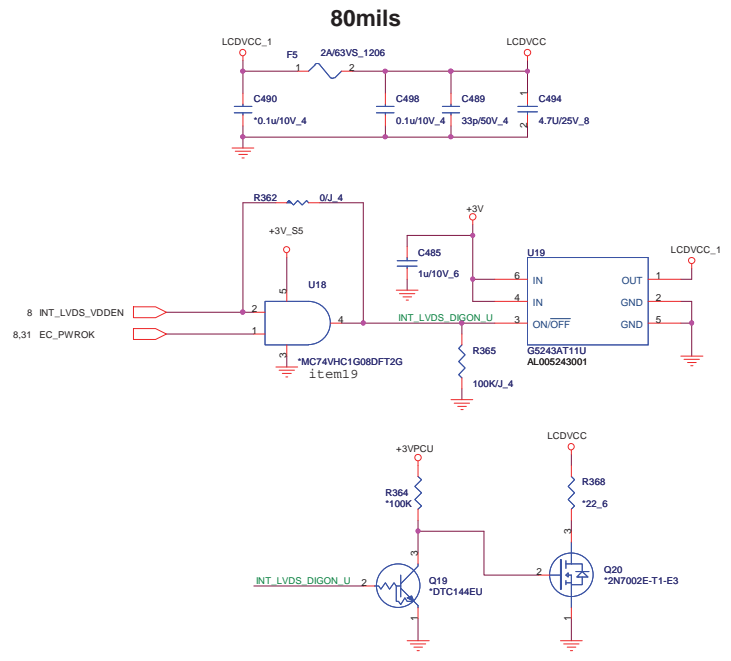
BACKLIGHT Control(LVDS)



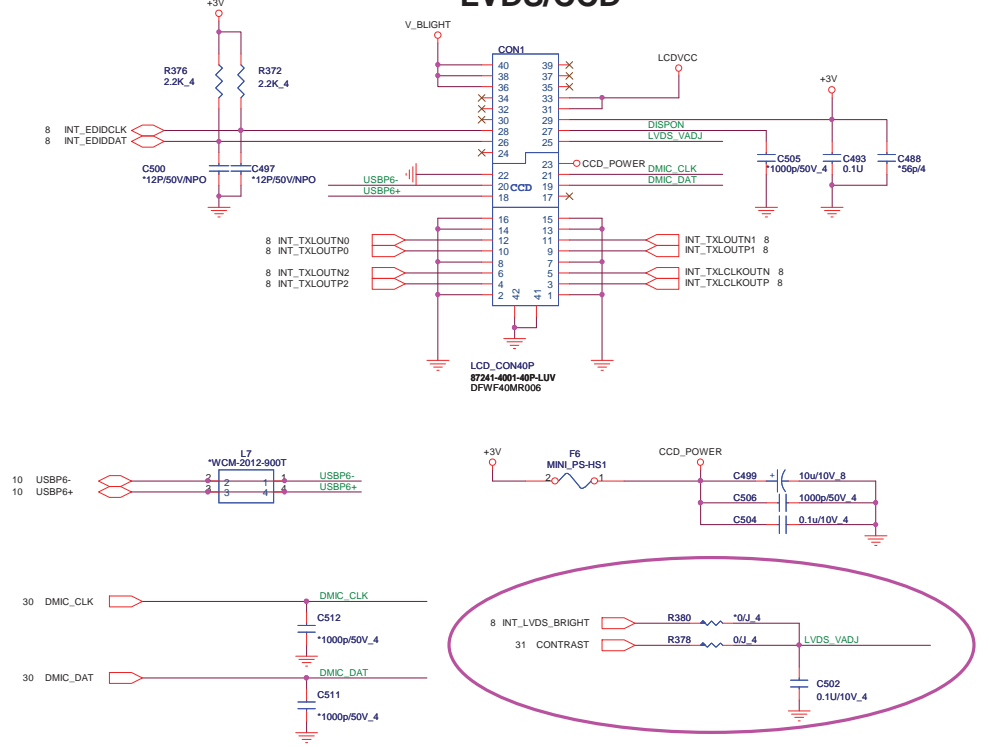
BACKLIGHT POWER

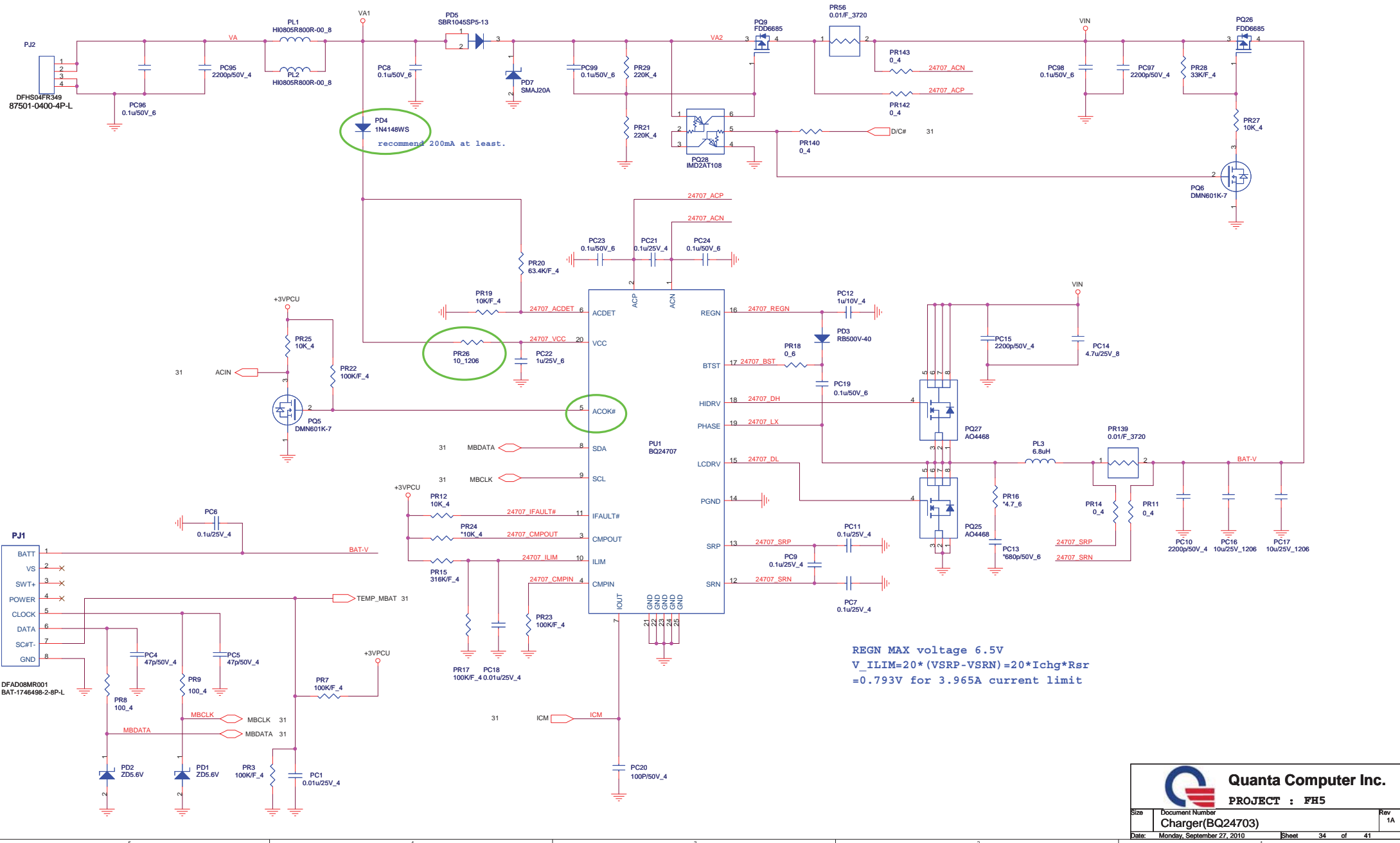


LED Panel POWER SWITCH(LVDS)



LVDS/CCD






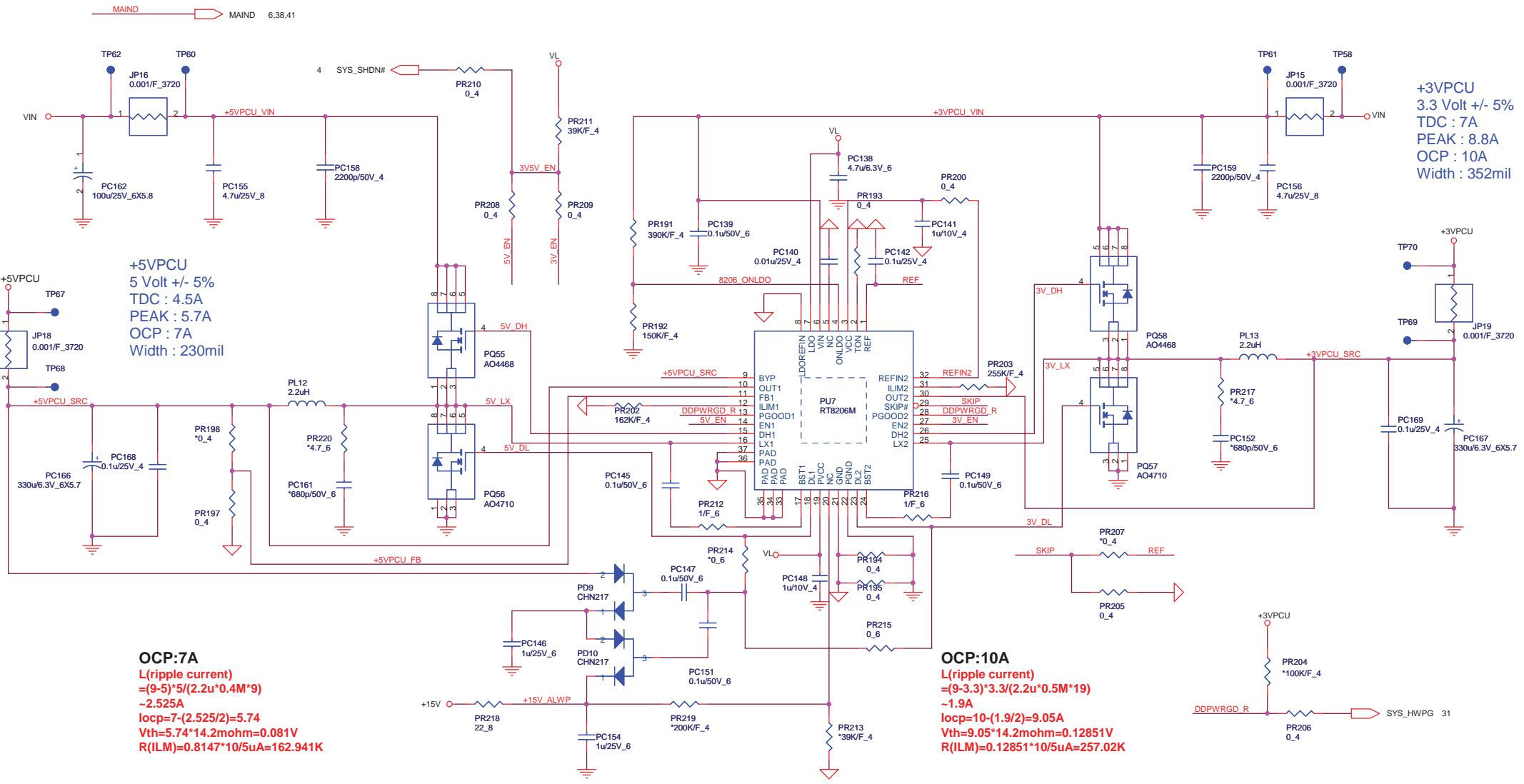
PD4
1N4148WS
recommend 200mA at least.

PR26
10_1206

ACOK#

REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$
 $= 0.793V$ for 3.965A current limit

 Quanta Computer Inc. PROJECT : FH5		
Size	Document Number	Rev
	Charger(BQ24703)	1A
Date:	Monday, September 27, 2010	Sheet 34 of 41

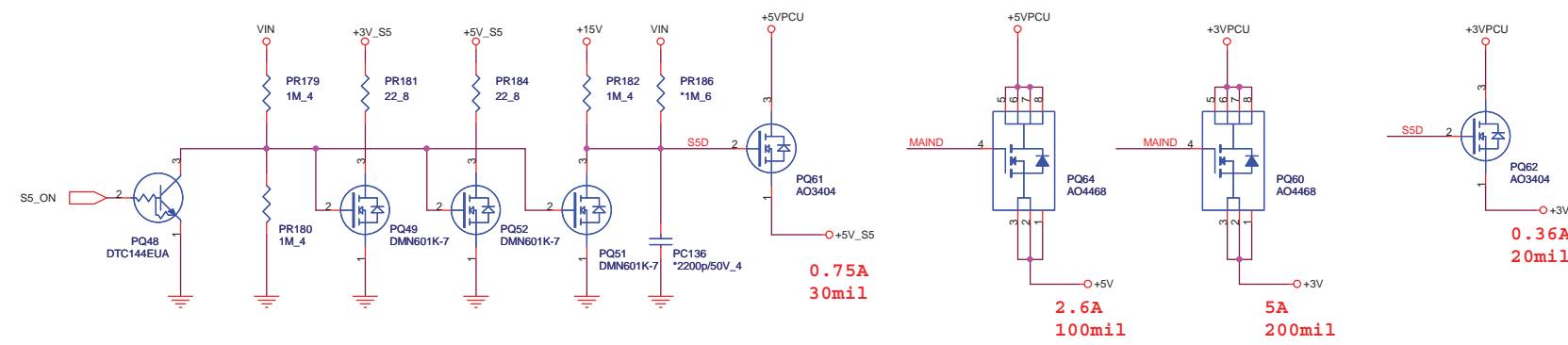


+5VPCU
 5 Volt +/- 5%
 TDC : 4.5A
 PEAK : 5.7A
 OCP : 7A
 Width : 230mil

+3VPCU
 3.3 Volt +/- 5%
 TDC : 7A
 PEAK : 8.8A
 OCP : 10A
 Width : 352mil

OCP:7A
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9) \approx 2.525 \text{A}$
 $I_{\text{ocp}} = 7 - (2.525/2) = 5.74$
 $V_{\text{th}} = 5.74 \cdot 14.2 \text{mohm} = 0.081 \text{V}$
 $R(\text{ILM}) = 0.8147 \cdot 10 / 5 \mu \text{A} = 162.941 \text{K}$

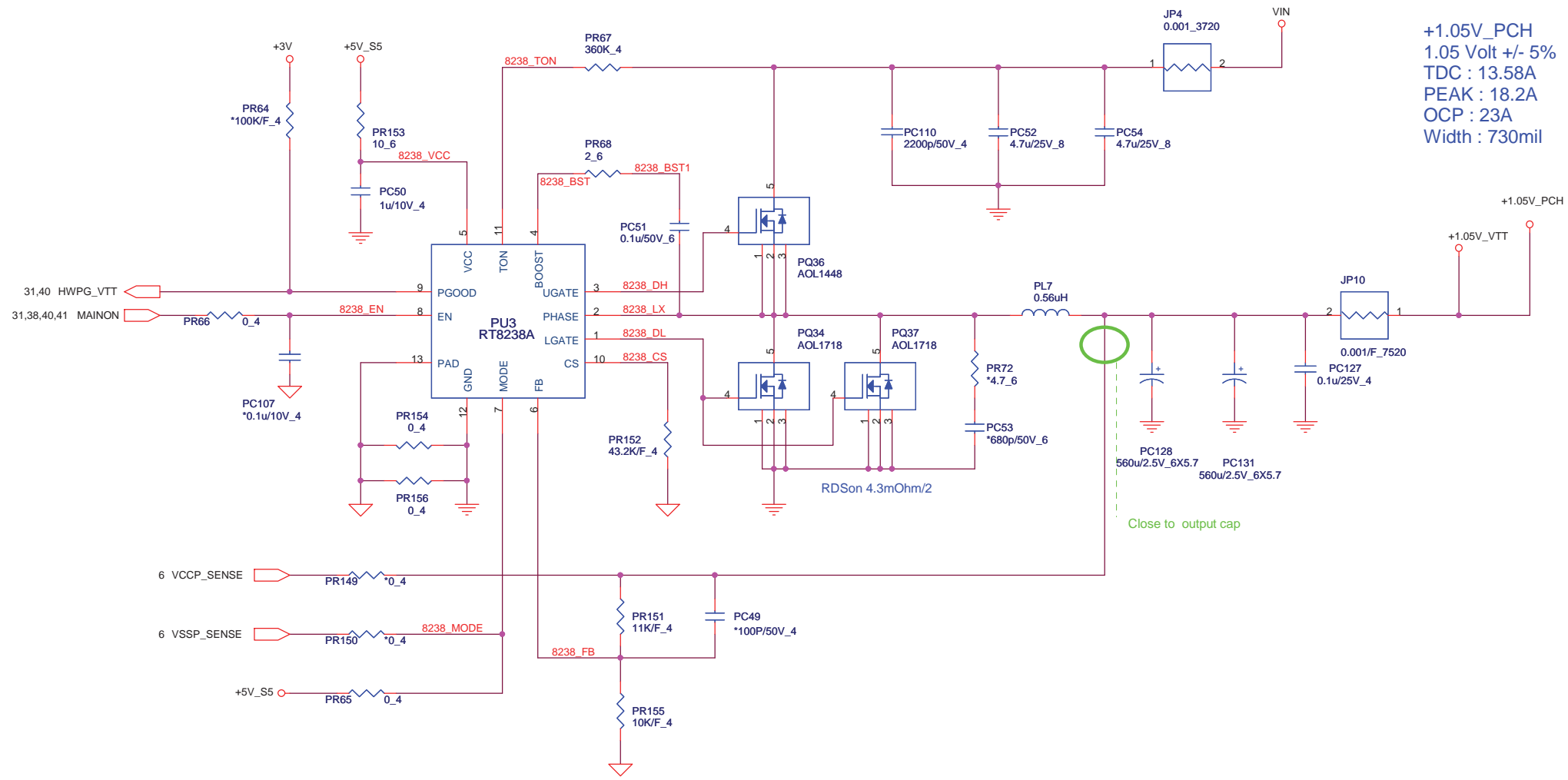
OCP:10A
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 19) \approx 1.9 \text{A}$
 $I_{\text{ocp}} = 10 - (1.9/2) = 9.05 \text{A}$
 $V_{\text{th}} = 9.05 \cdot 14.2 \text{mohm} = 0.12851 \text{V}$
 $R(\text{ILM}) = 0.12851 \cdot 10 / 5 \mu \text{A} = 257.02 \text{K}$



Quanta Computer Inc.
PROJECT : FH5

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A


Date: Monday, September 27, 2010 Sheet 35 of 41

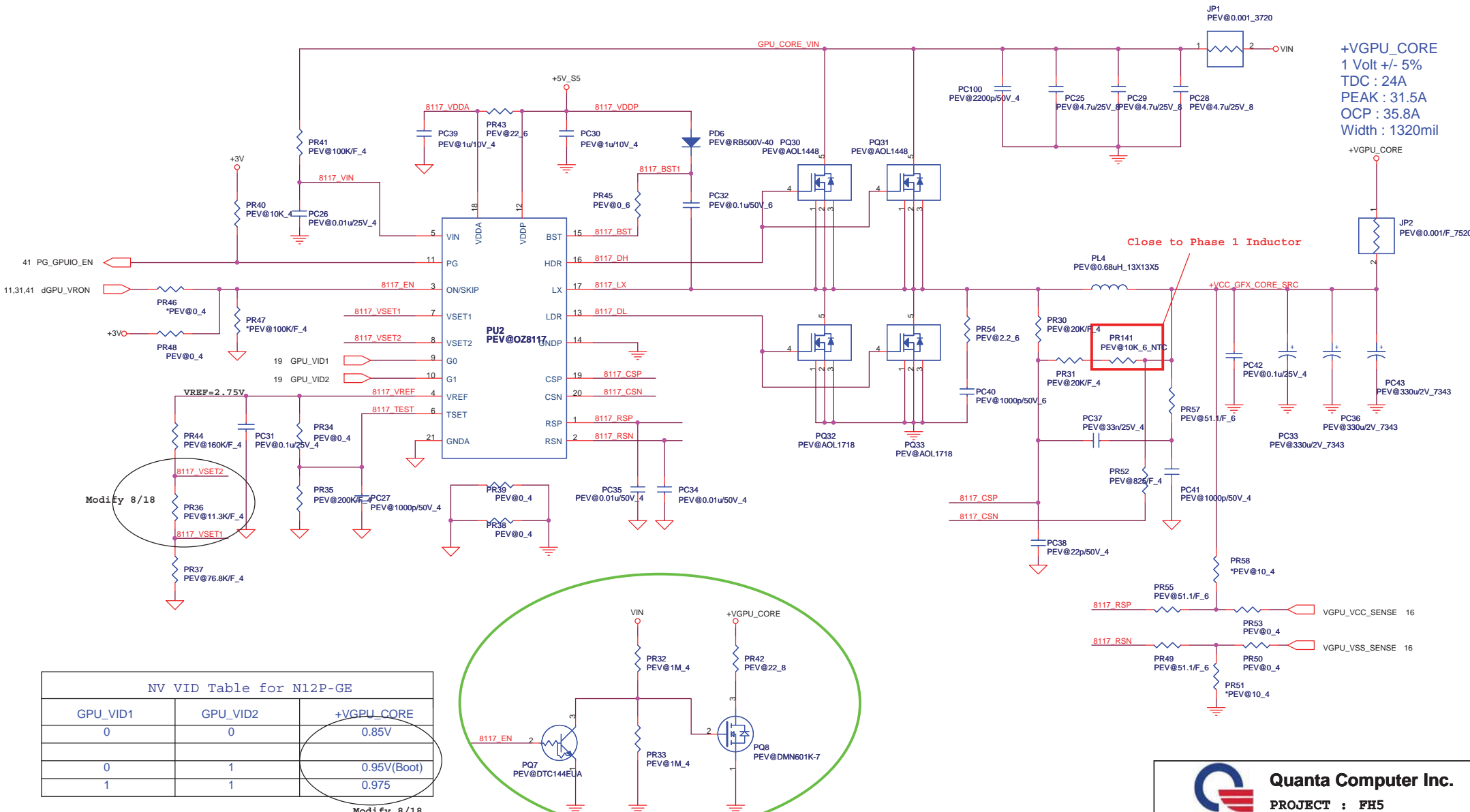


+1.05V_PCH
 1.05 Volt +/- 5%
 TDC : 13.58A
 PEAK : 18.2A
 OCP : 23A
 Width : 730mil

Current limit = 10uA * Rth / RDson

$$VOUT = (1 + R1/R2) * 0.5$$

 Quanta Computer Inc. PROJECT : FH5		Size	Document Number	Rev
			+PCH&VTT (RT8238A)	1A
Date:	Monday, September 27, 2010	Sheet	37	of 41

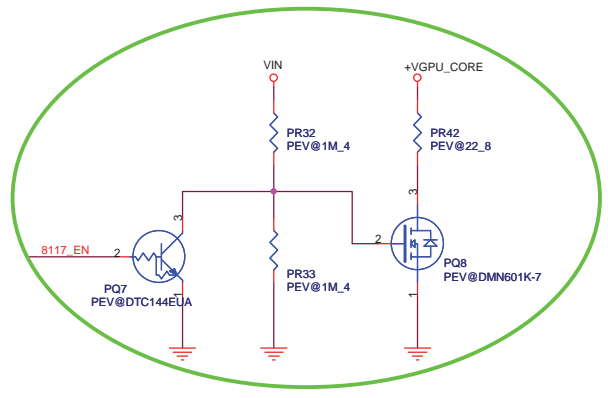


+VGPU_CORE
 1 Volt +/- 5%
 TDC : 24A
 PEAK : 31.5A
 OCP : 35.8A
 Width : 1320mil

Modify 8/18

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	0.85V
0	1	0.95V(Boot)
1	1	0.975

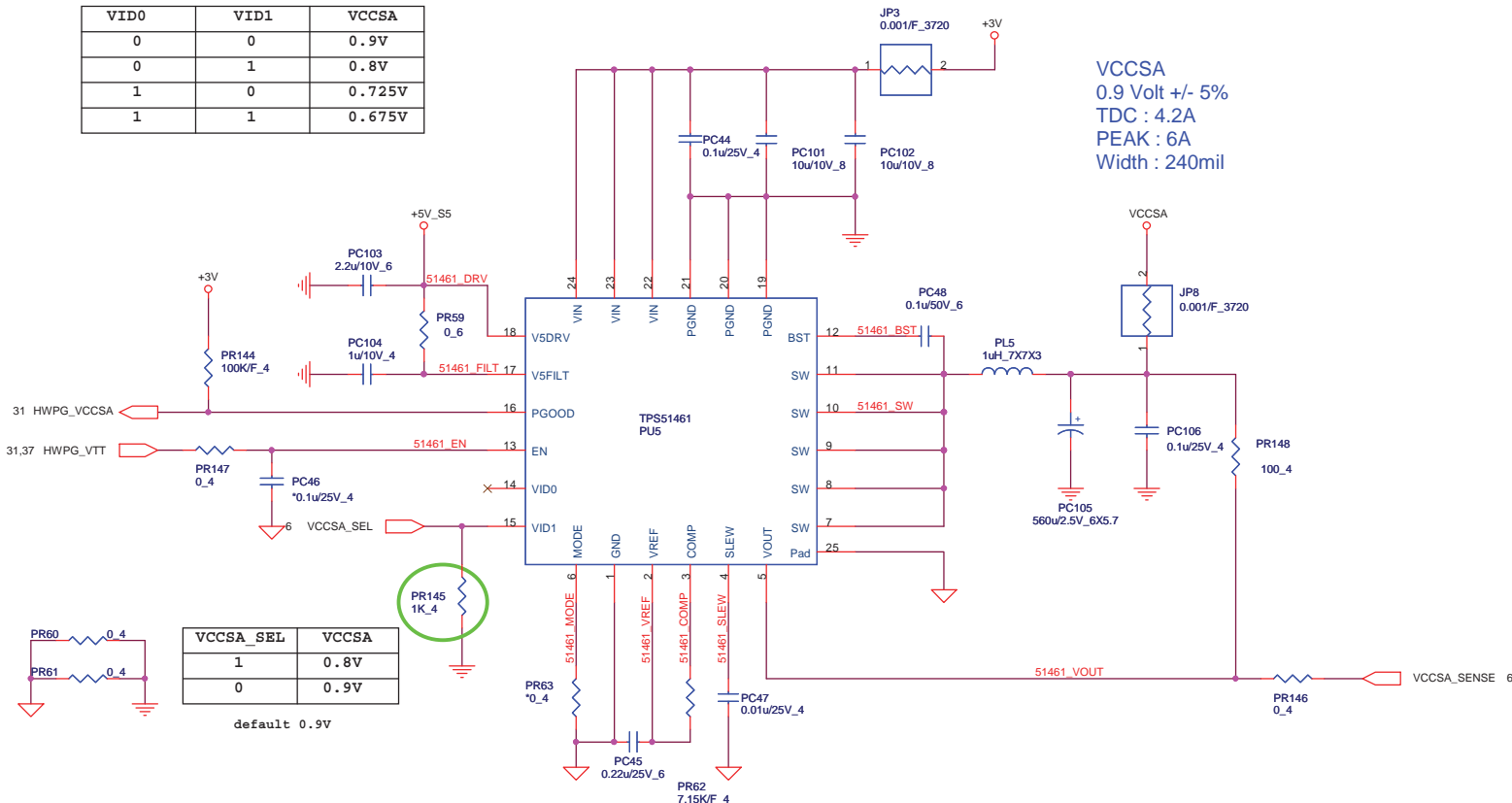
Modify 8/18



Quanta Computer Inc.
 PROJECT : FH5

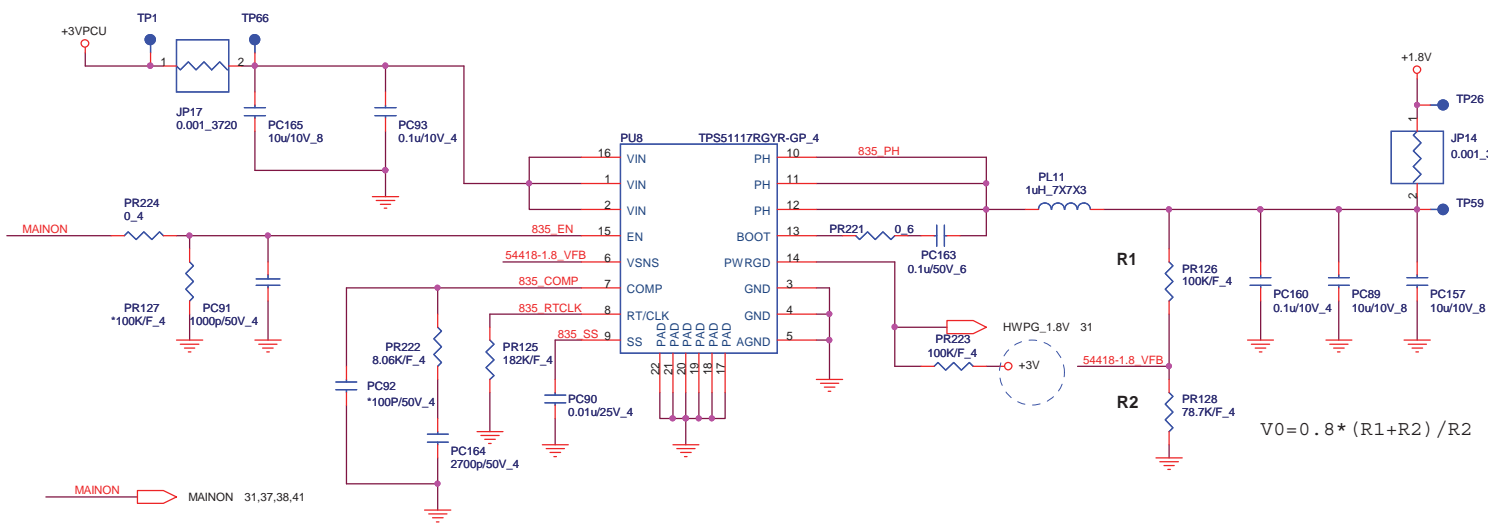
Size	Document Number	Rev
	GPU CORE(OZ8117)	1A
Date:	Monday, September 27, 2010	Sheet 39 of 41

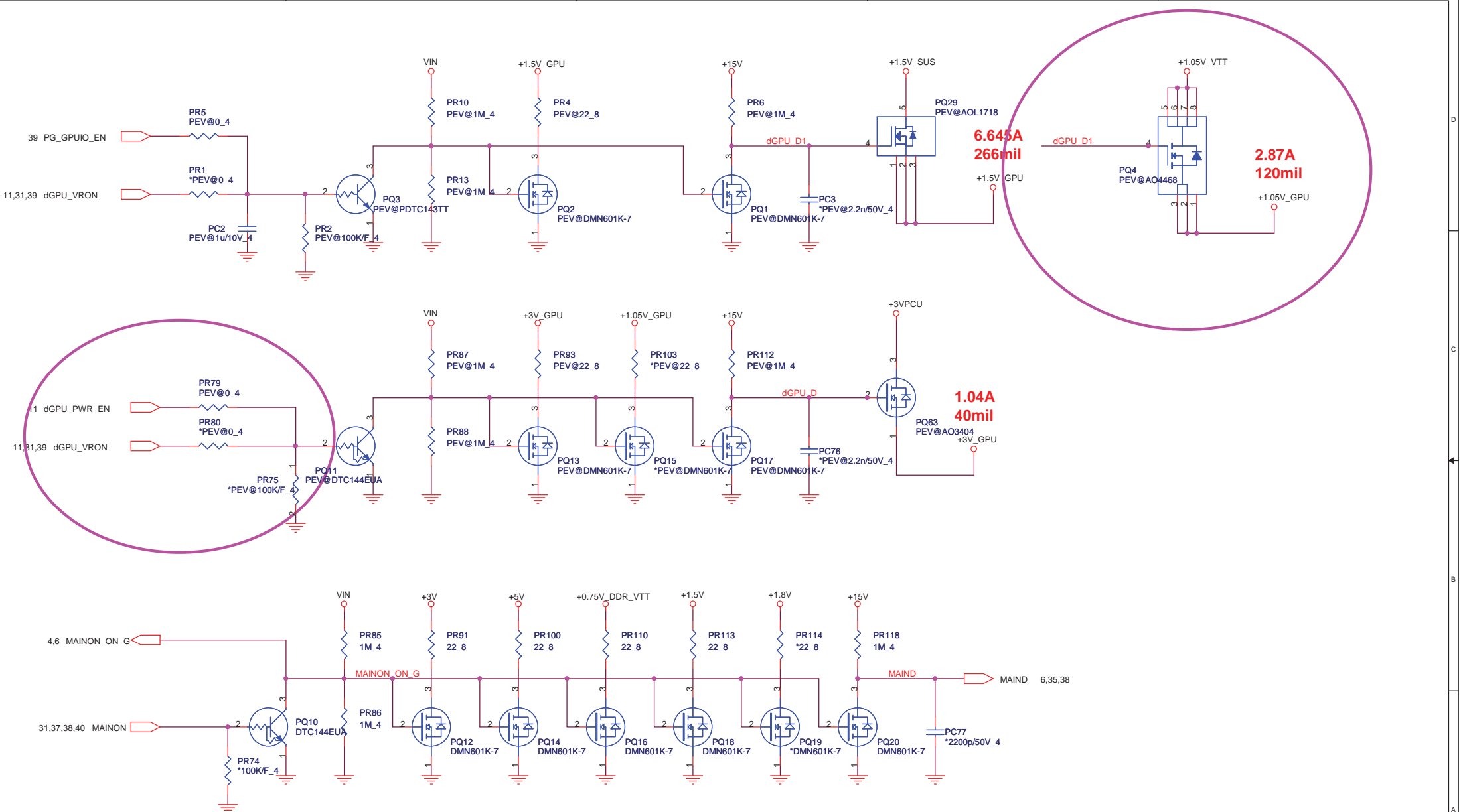
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V




VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V






Quanta Computer Inc.
PROJECT : FH5

Size	Document Number	Rev
	Discharger	1A
Date:	Monday, September 27, 2010	Sheet 41 of 41

Model

FH5 MB

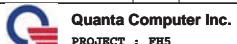
REV

CHANGE LIST

B

	<p>page 33: Change +VIN to VIN.</p> <p>2010/09/20 page 30 : Del Q16 ,R351. page 10 : Add Q27 and Q28. page 26 : Change CON6 RJ45 Conn to DFTJ08FR157.</p>
	<p>2010/09/22 page 10: Change USB port6 ot port10.</p>
	<p>2010/09/22 page 31 : Del CN3 Netname ,NBSWON#, SLP_S3# ,+VCC_GFX,+VCC_CORE,H_PWRGOOD, RSMRST#, SLP_S4# ,SUS_STATE#. page 31 : Reserve R351 ,R574-R580 for Power sequence resistor. page 31 : Reserve C692 for H_PWRGOOD. page 9: Change JTAG VCC +3VPCU to +3V_S5.</p>
	<p>2010/09/23 page 31 : Change CON2 VCC from +3V to +3V_S5.</p> <p>page 12 : Reserve C693,C694,C695,C696 for BSD. Page36 : PC61 - PC63 change value from *1000p/50V_4 (CH21006JB10) to *0.1u/50V_6 (CH41006K911) Page36 : PC62 - PC112 - PC116 - PC119 change value from 1000p/50V_4 (CH21006JB10) to 0.1u/50V_6 (CH41006K911) Page36 : PC72 change value from *PIV01000p/50V_4 (CH21006JB10) to * PIV00.1u/50V_6 (CH41006K911) Page36 : PC74 - PC122 - PC125 change value from PIV01000p/50V_4 (CH21006JB10) to PIV00.1u/50V_6 (CH41006K911) Page38 : PR190 changes value from 620K/F_4 (CS46202FB00) to 750K/F_4 (CS47502FB14) Page39 : PR44 changes value from PEV0169K/F_4 (CS41692FB12) to PEV0160K/F_4 (CS41602FB00) Page39 : PR36 changes value from PEV021.5K/F_4 (CS32152FB17) to PEV011.3K/F_4 (CS31132FB07) Page39 : PR37 changes value from PEV082K/F_4 (CS38202FB14) to PEV076.8K/F_4 (CS37682FB00)</p> <p>page36 :PL6 - PL8 - PL9 change footprint from CHOKE-BTQP4LR36WFC-4P-SMT to CHOKE-PCMB104T-R45MN-4P-SMT page06 Reserve C697,C698,C699 for VID.</p>
	<p>2010/09/24 page06 Del R28 , add R21,C19,C20,Y2 , use crystal to provide 25M CLK. page36 Del PC57,PC58 ,ADD PC170,171,PC78,PC73,PC55 for C state issue. page38 Change PR199 to 7.32K_4(CS27322FB12), change 1.5V_SUS OCP value.</p>
	<p>2010/09/27 Page39 : PL4 change P/B from CV+68*0M200 to DC+68Z0M001 Page24 : C4,C5,C6,C7,C8,C9 change from2.2P/50V_4 to 10P/50V_4(CH01006JB08). page 27 : Change U34 Ctrl1 1 ->3 behavior,add R554 , R581,del R582.</p>

3C



DOC NO.	PROJECT MODEL :	FH5	APPROVED BY:	DATE:	2010/09/20
	PART NUMBER:		DRAWING BY:	REVISION:	1A

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