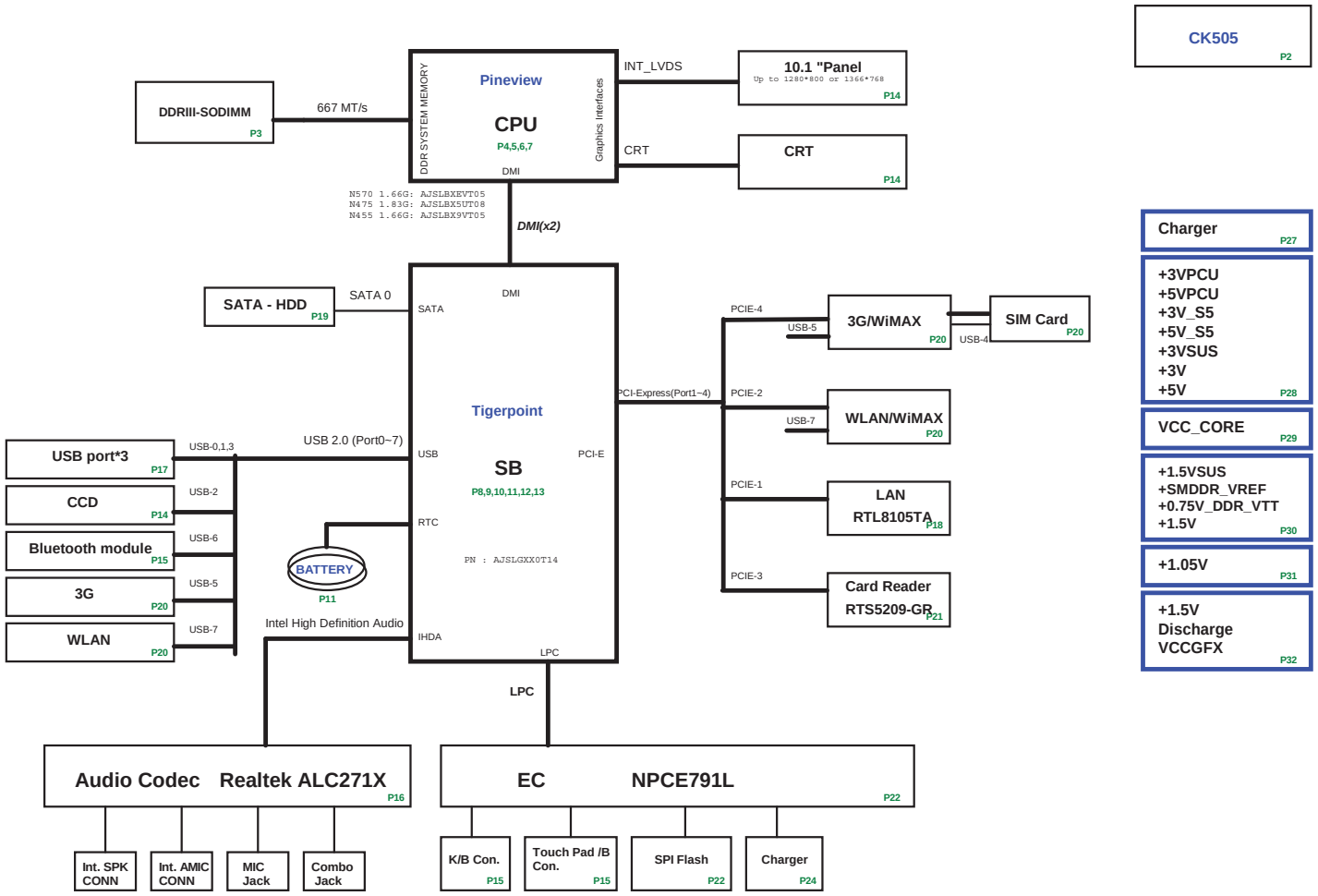
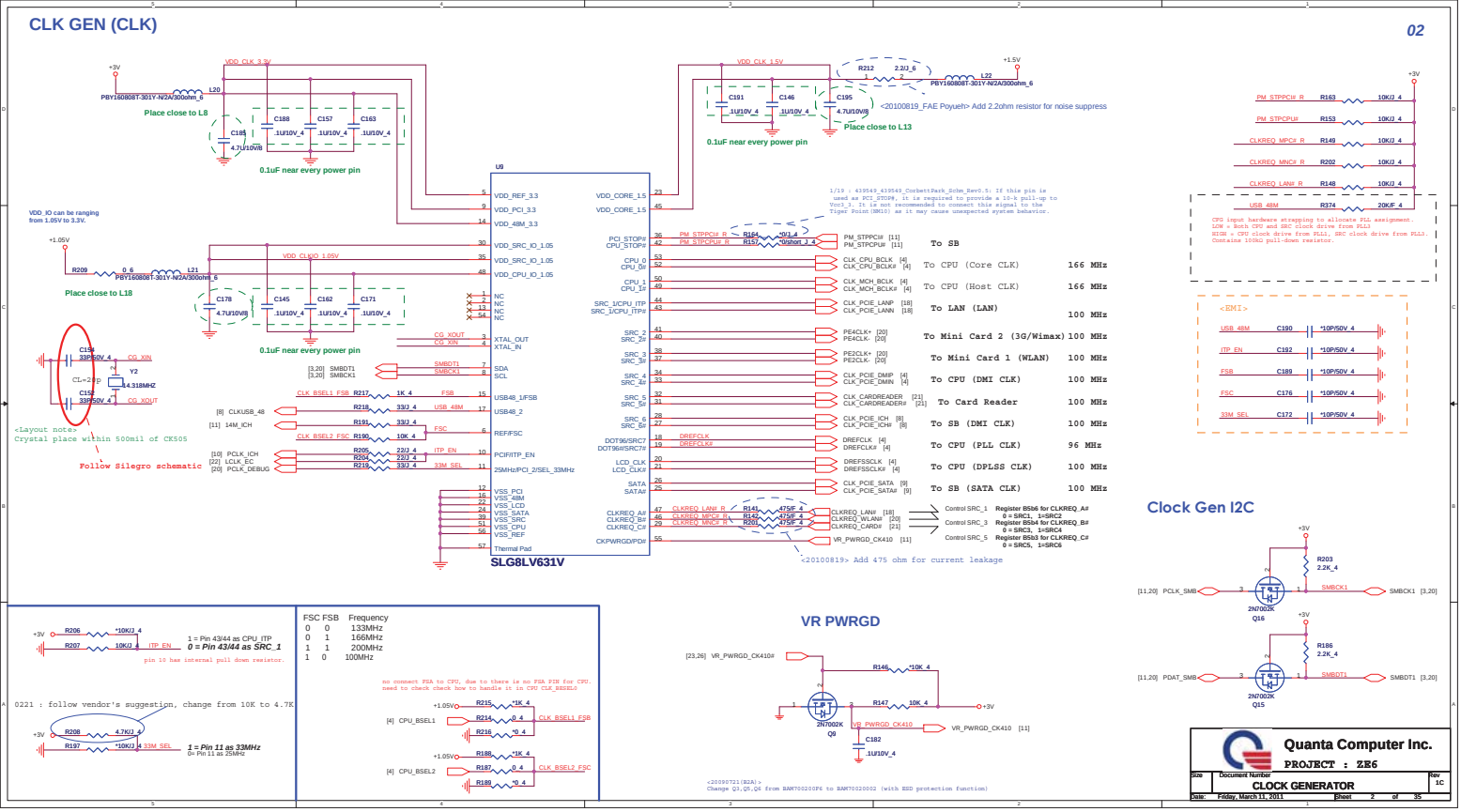
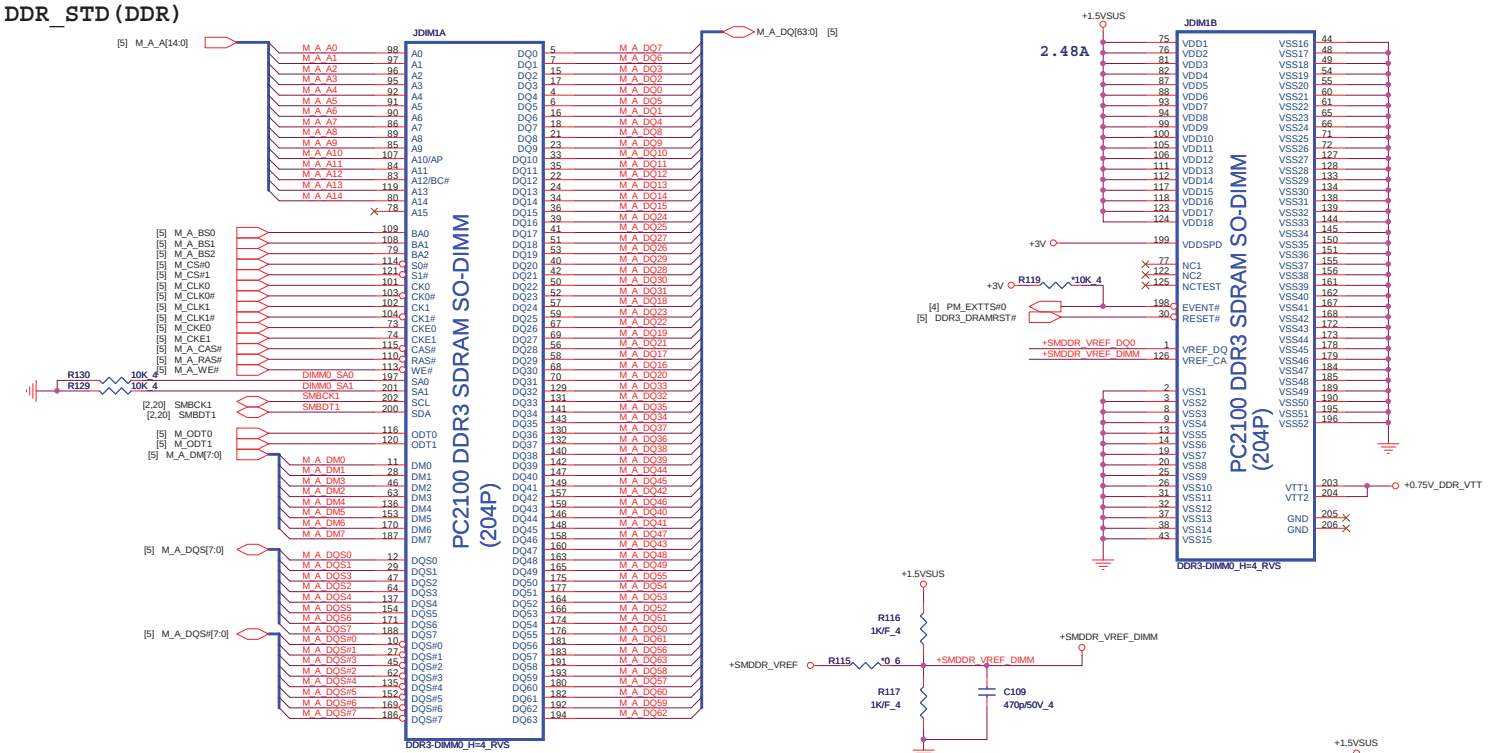
ZE6 Block Diagram



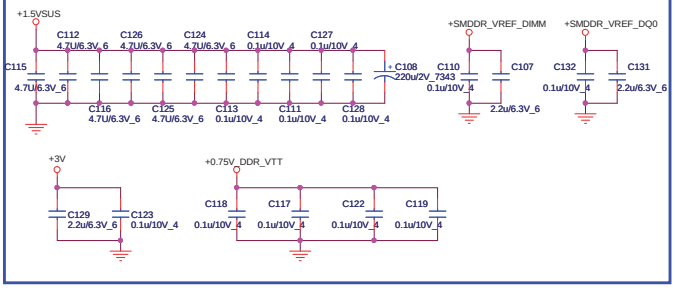
Quanta Computer Inc.
PROJECT : ZE6
Size | Document Number | Rev 1B
Block Diagram
Date: Friday, March 11, 2011 | Sheet 1 of 35



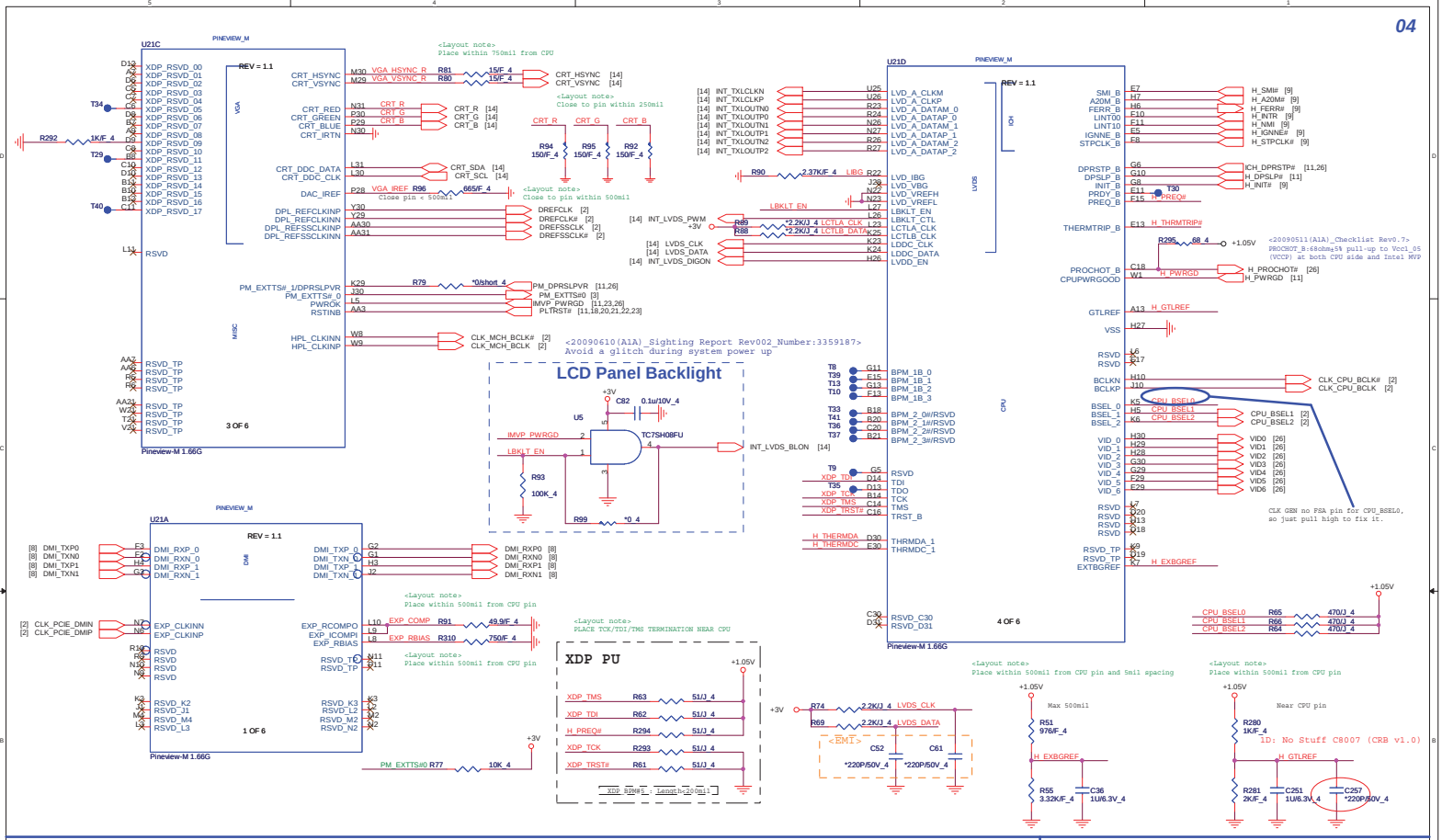
DDR_STD(DDR)

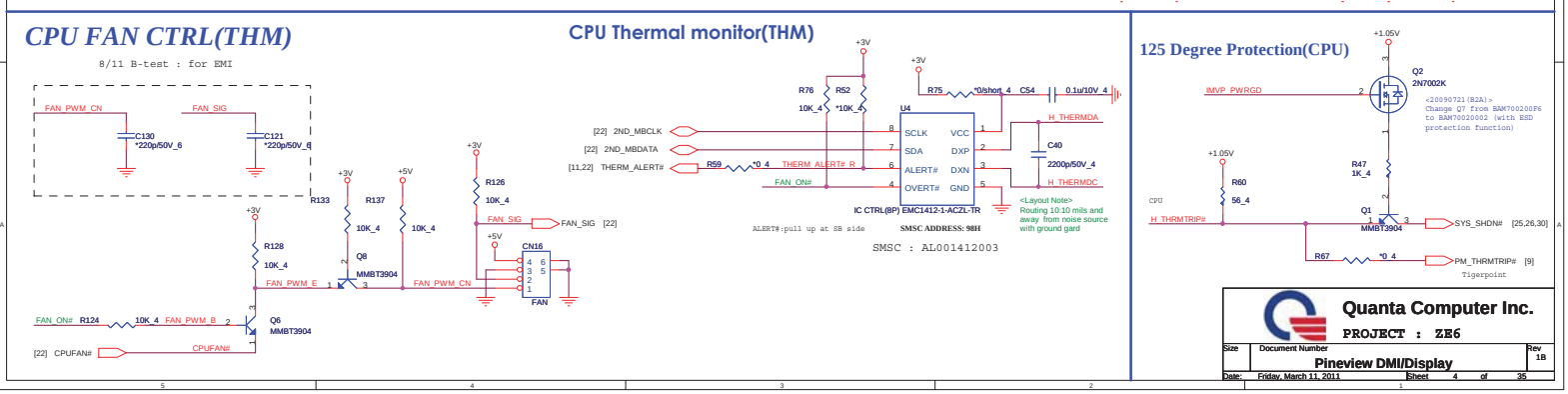


Place these Caps near So-Dimm0.

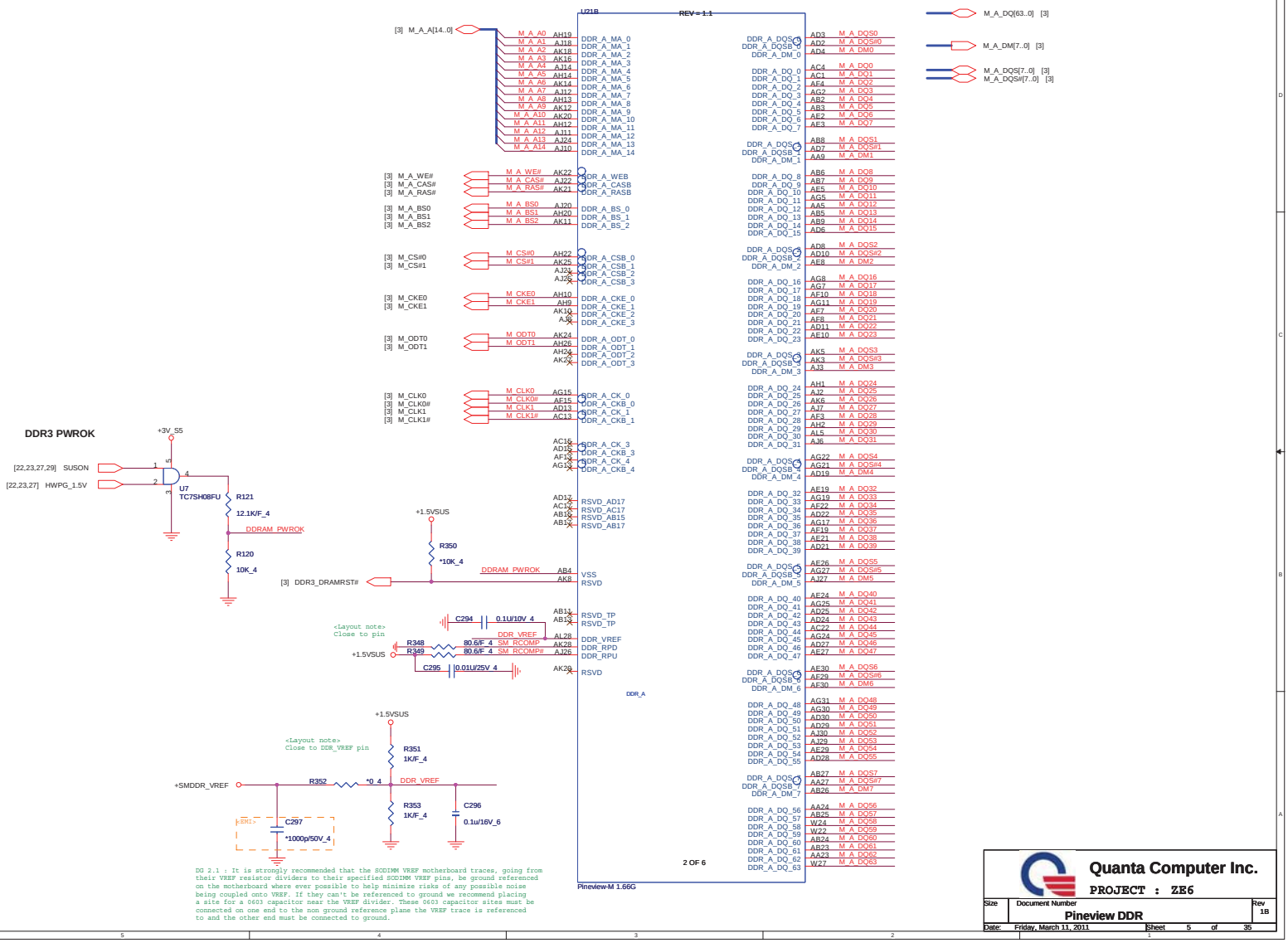


Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Friday, March 11, 2011	Sheet 3 of 35	

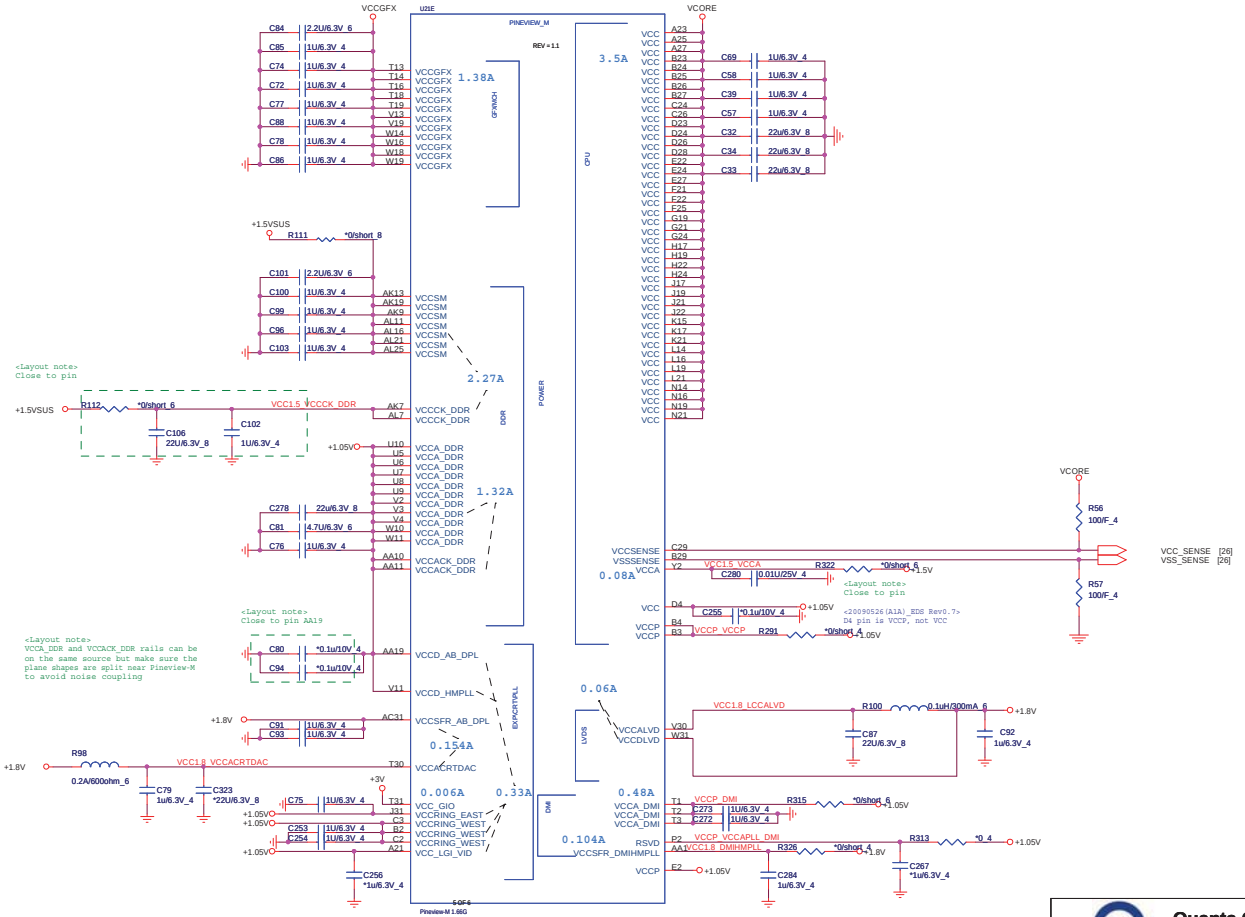




Quanta Computer Inc.
PROJECT : ZE6
Size | Document Number | Rev 1B
Pineview DMI/Display
Date: Friday, March 11, 2011 | Sheet 4 of 35



Quanta Computer Inc.	PROJECT : ZE6	
Size	Document Number: Pineview DDR	Rev: 1B
Date: Friday, March 11, 2011	Sheet 5 of 35	

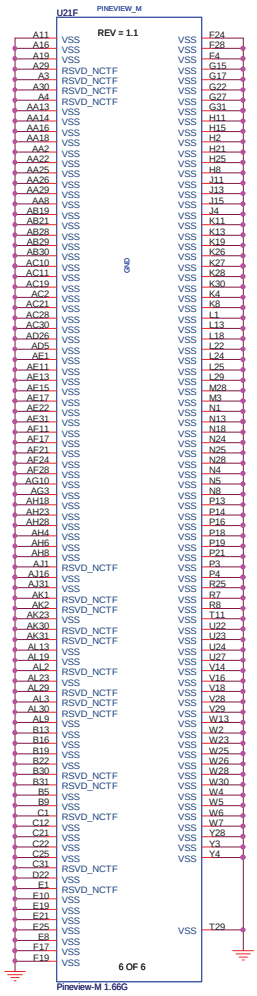


Quanta Computer Inc.

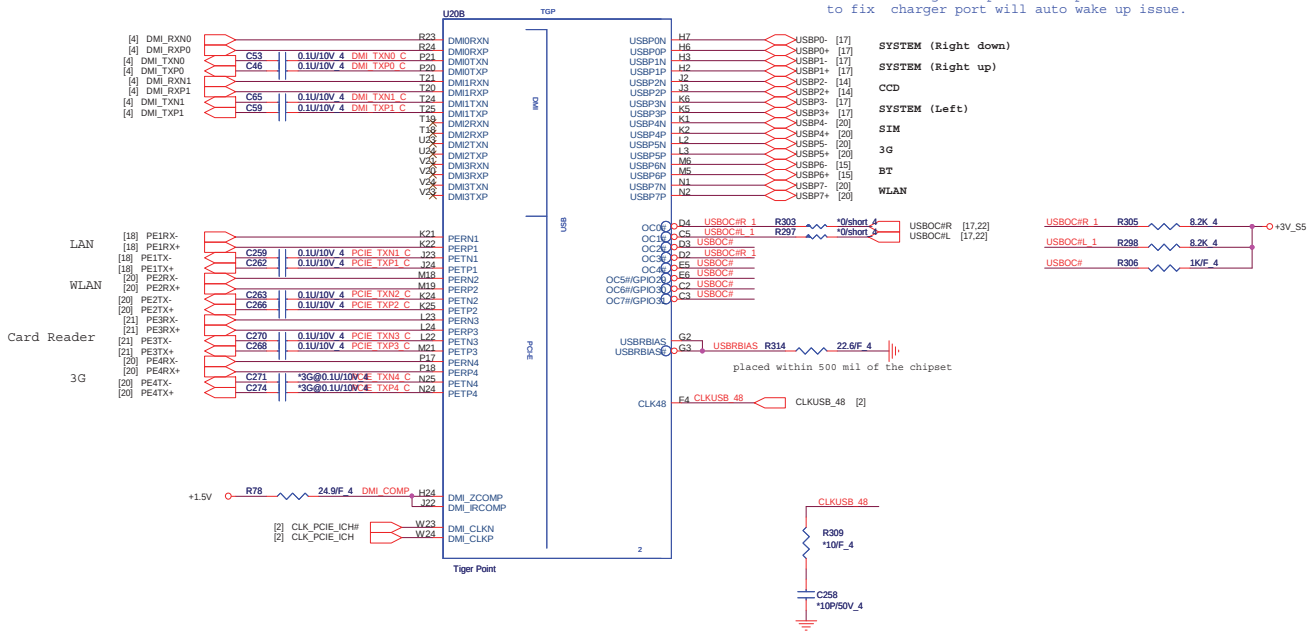
PROJECT : ZE6

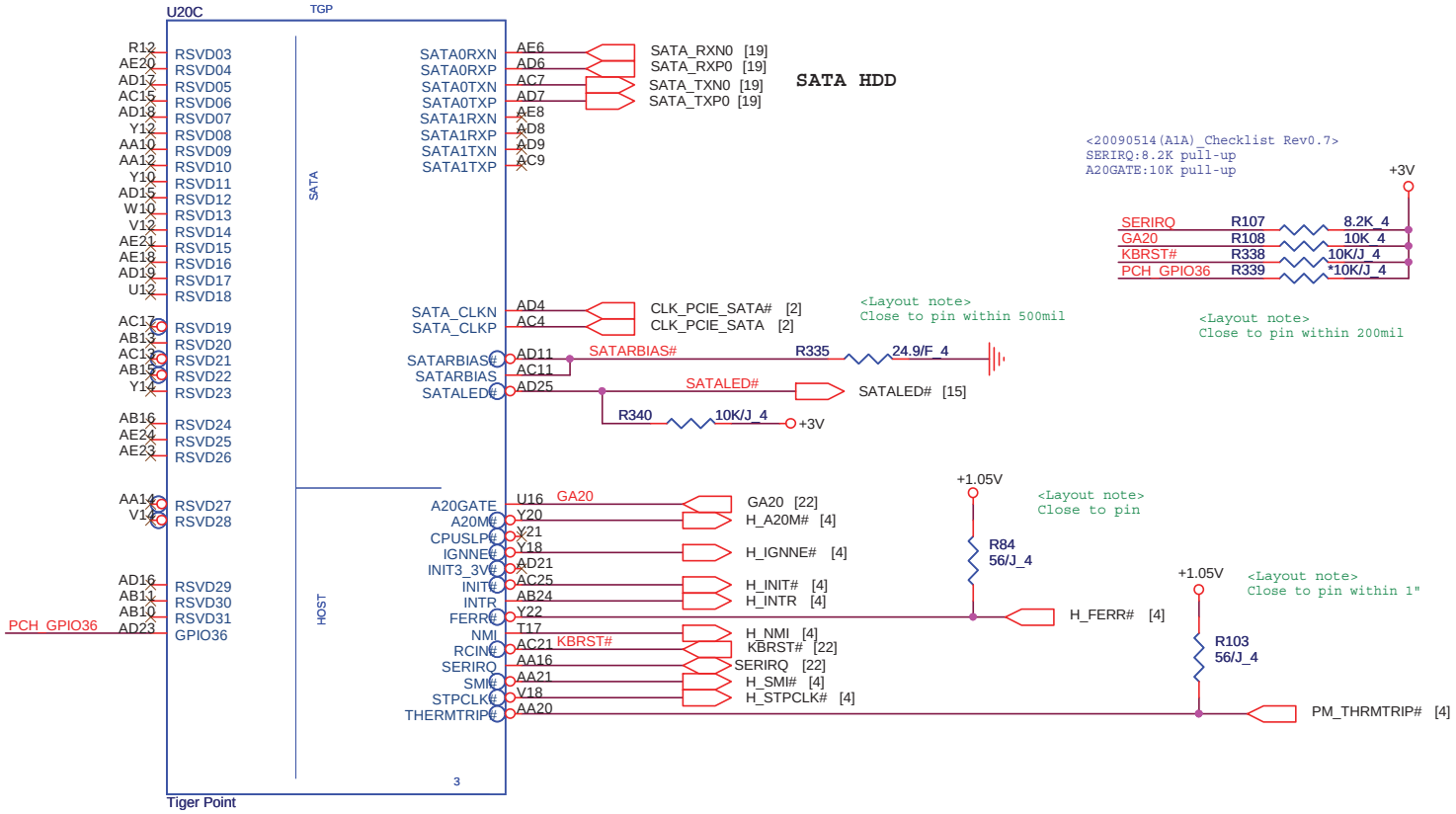
Size	Document Number	Rev
	Pineview Power	1B

Date: Friday, March 11, 2011 Sheet 6 of 35



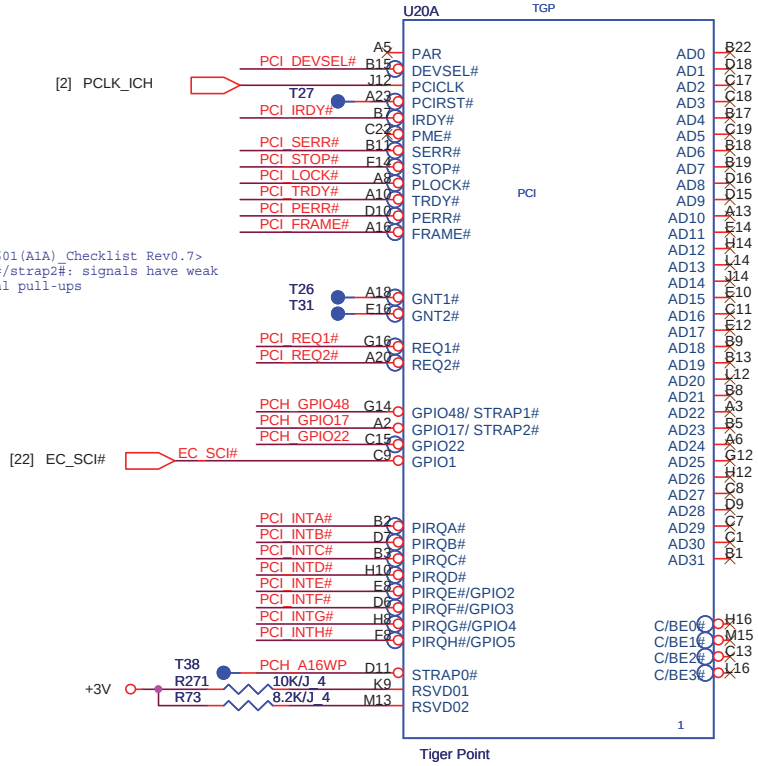
Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number	Rev
	Pineview GND	1B
Date: Friday, March 11, 2011	Sheet 7 of 35	





NOTE :
1. CPUSLP# is supported only on nettop platforms.

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: Tiger Point Sata/Host	Rev 1B
Date: Friday, March 11, 2011	Sheet 9 of 35	

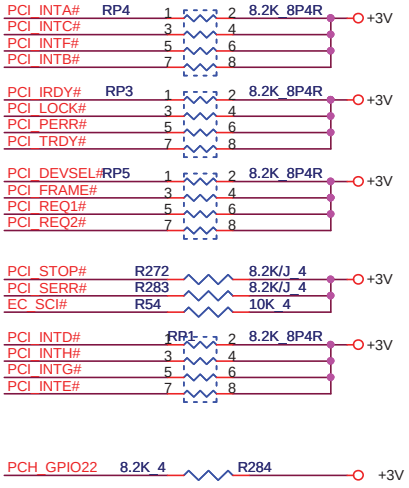


ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default



IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

Quanta Computer Inc.

PROJECT : ZE6

Size	Document Number	Rev
	TigerPoint PCI(3/6)	1B
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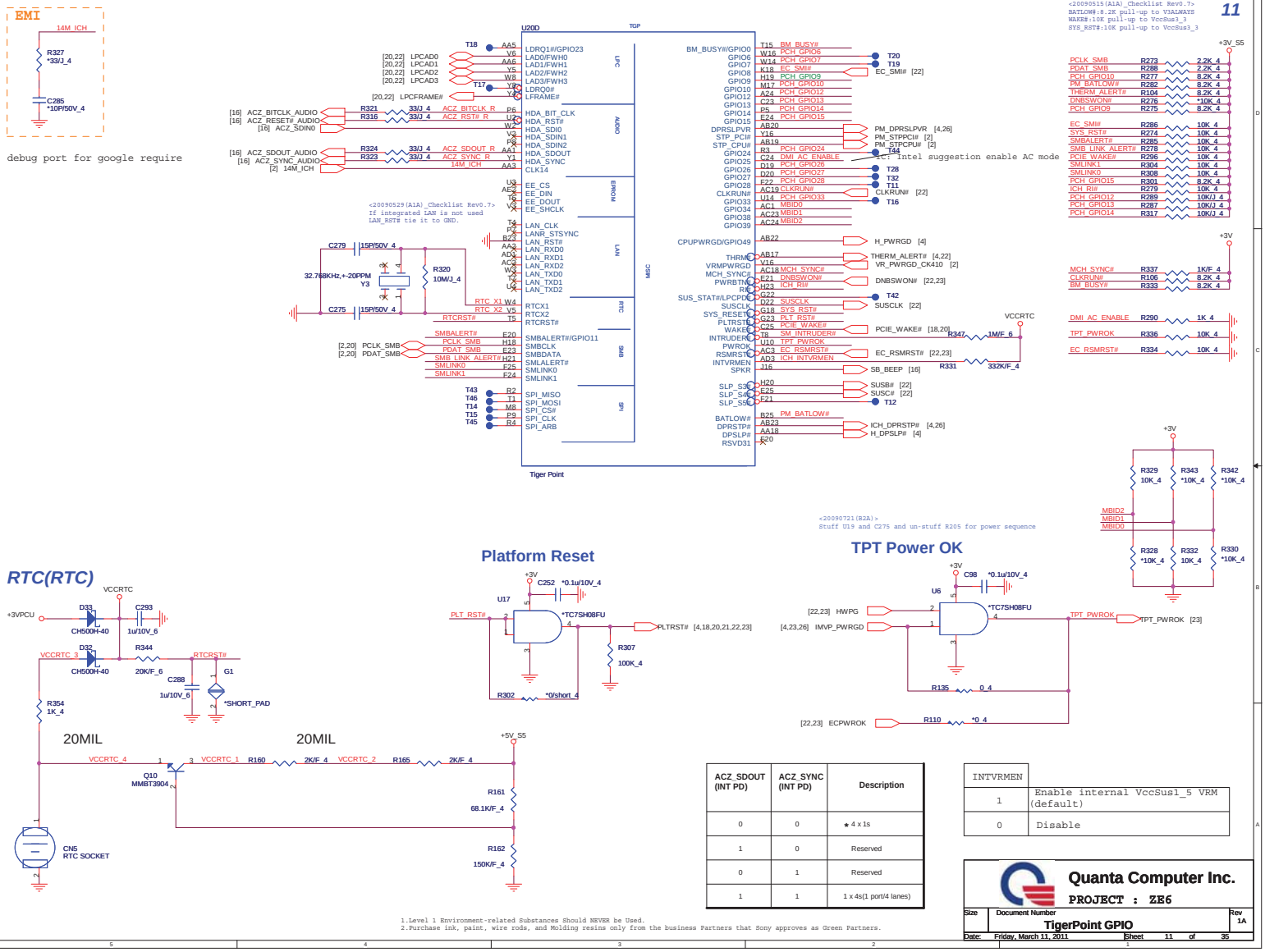


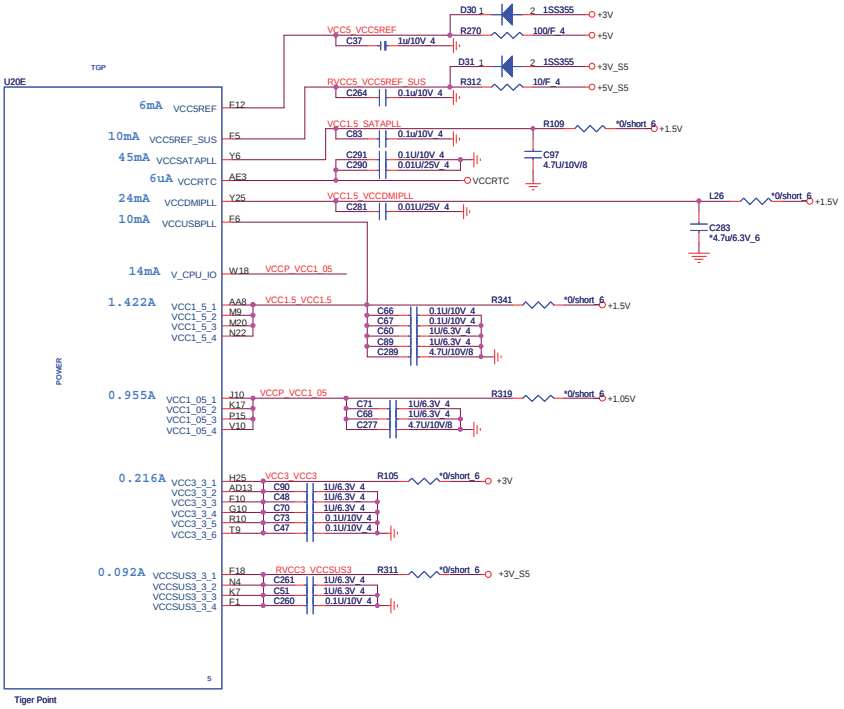
ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	★ 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6
Size: Document Number: TigerPoint GPIO Rev: 1A
Date: Friday, March 11, 2011 Sheet 11 of 35

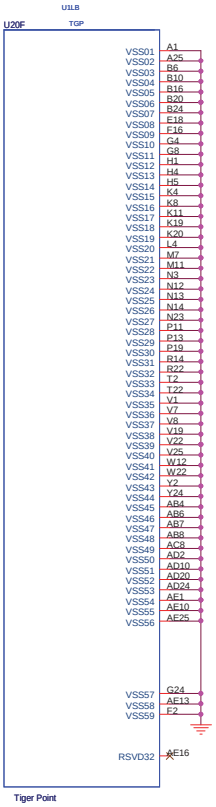
<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	TigerPoint Power	1B
Date: Friday, March 11, 2011	Sheet 12 of 35	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	TigerPoint GND	1B

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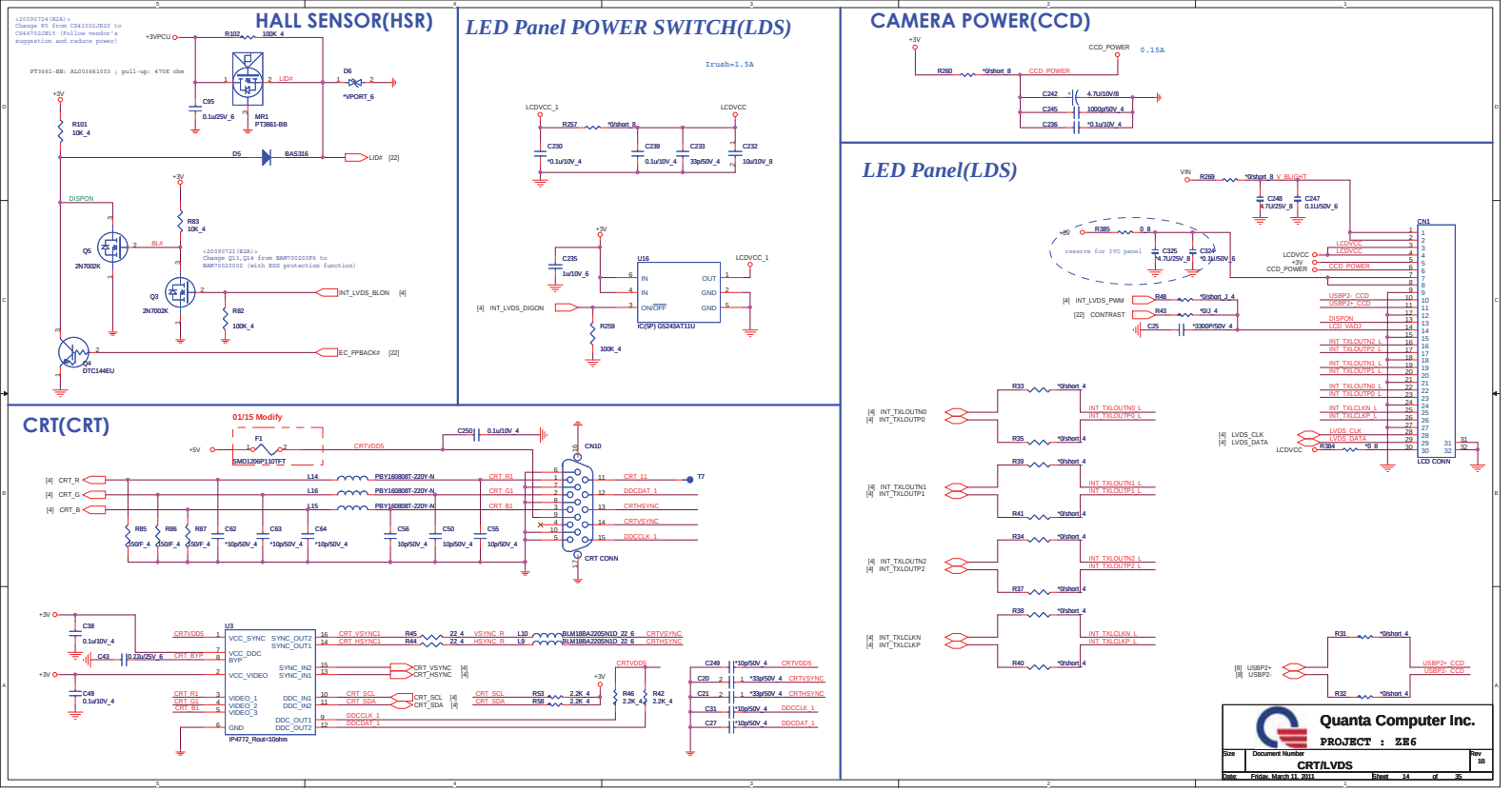
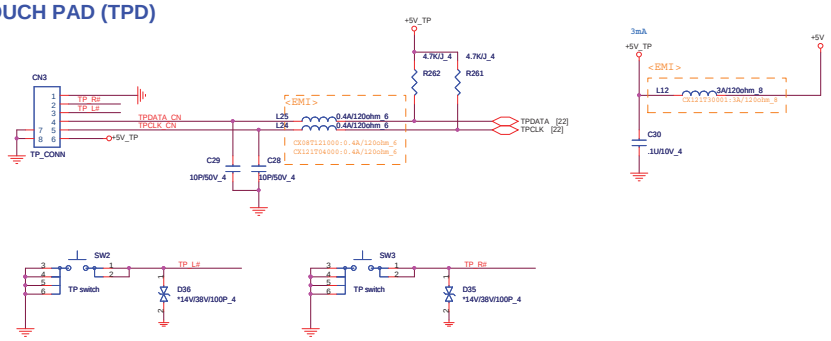
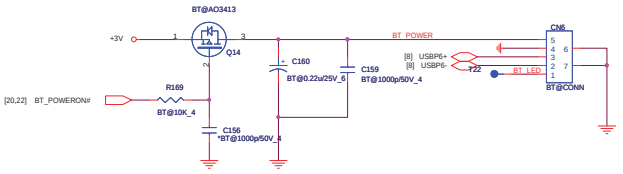


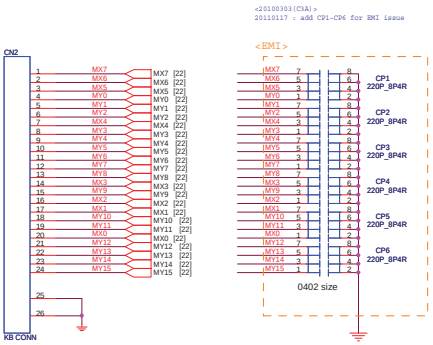
TOUCH PAD (TPD)



BLUETOOTH(BTM)

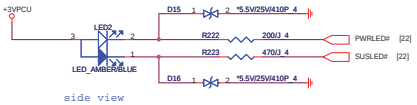


KEYBOARD (KBC)



LED/SW (UIF)

PWR LED / SUS LED

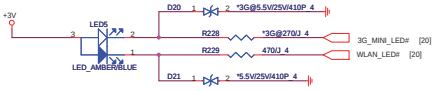


side view

FULL LED / CHG LED

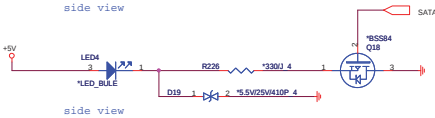
side view

3G LED / WLAN LED



side view

HDD LED

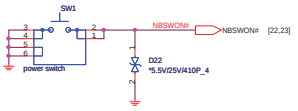


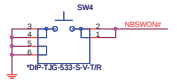
side view

PWR: Blue Vf: 2.55~3.15V, If=20mA
SUS: Orange Vf=1.6~2.0V, If=20mA

PWR indicator

PWR Button





W/O 3G: use BE0R0083Z00
W 3G: use BEB00023ZA0

<20090609(A1A)_Checklist Rev1.0>
Need the buffer for LED driving capability since the IOL is 6mA only.

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: KB/BT/TP/LED/Power Connector	Rev 1B
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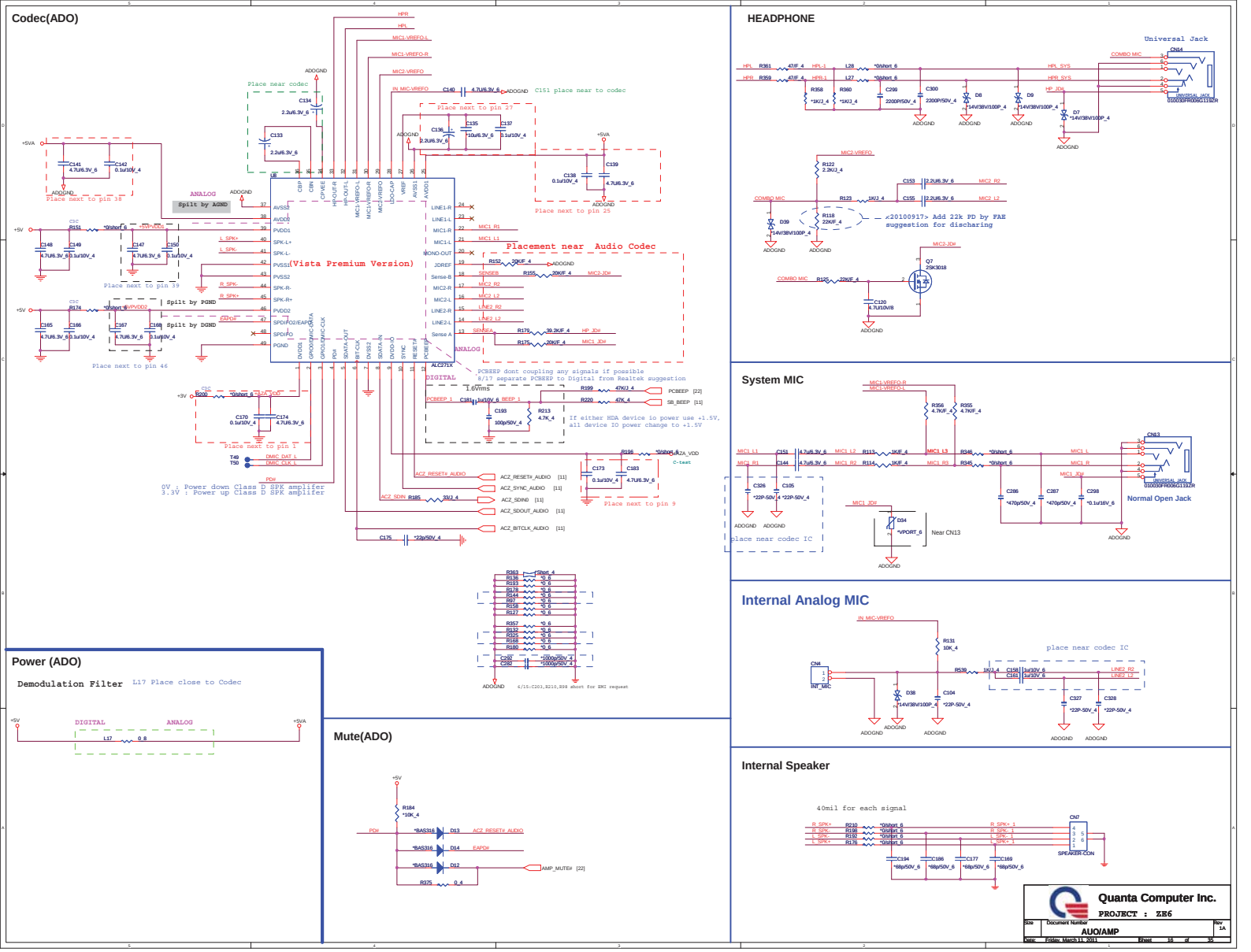
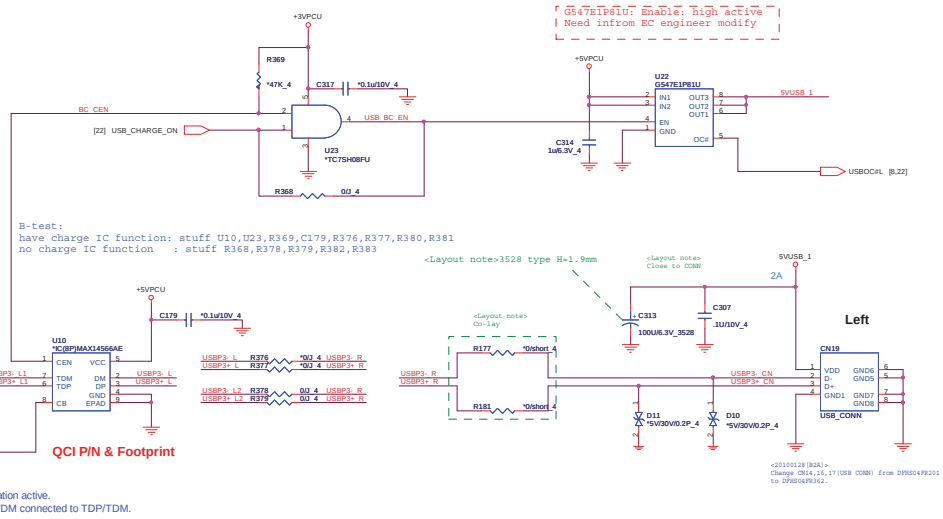


USB for iPod charge (USB)

Enable USB Charger						
	AC		DC(Battery > Setting%)		DC(Battery < Setting%)	
	S3	S4/S5	S3	S4/S5	S3	S4/S5
Charge Feature	O	O	O	O	△ (Note 2)	X
Wake Feature	X		X		X	

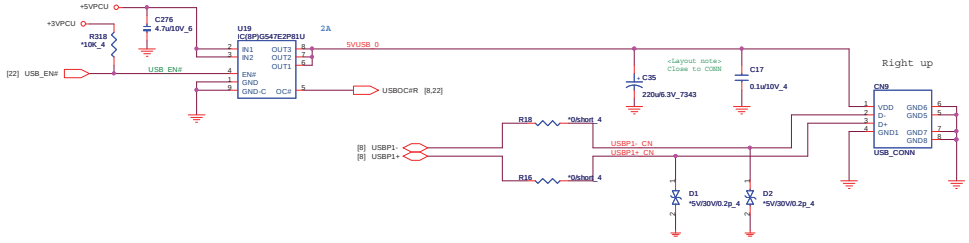
Disable USB Charger						
	AC		DC(Battery > Setting%)		DC(Battery < Setting%)	
	S3	S4/S5	S3	S4/S5	S3	S4/S5
Charge Feature	△ (Note 2)	X	△ (Note 2)	X	△ (Note 2)	X
Wake Feature	O		O		O	

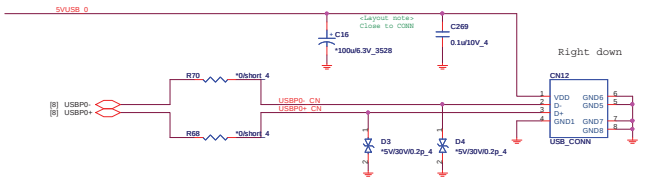
Note.1 Devices can be charged or not should same as other USB ports



System Status: .
> Lo: AM, autodetection charger identification active.
> HI: PM, pass-through mode active, DP/DM connected to TDP/TDM.

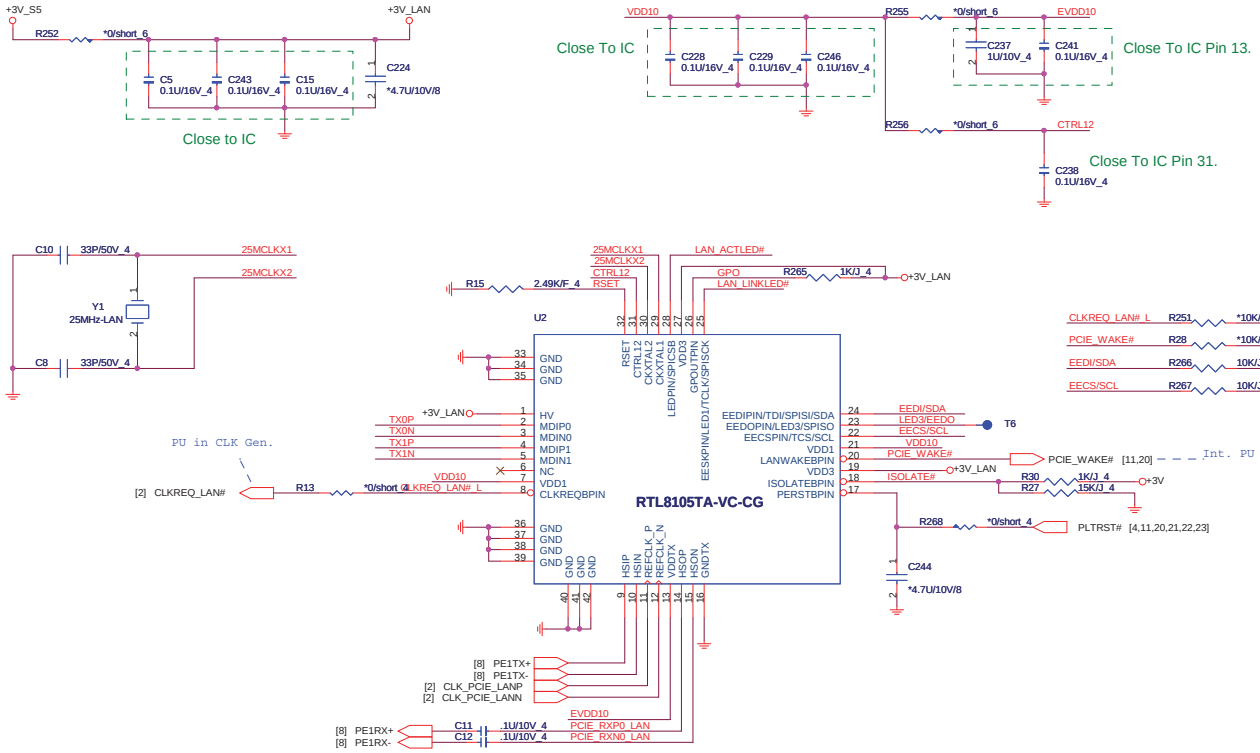
USB(USB)



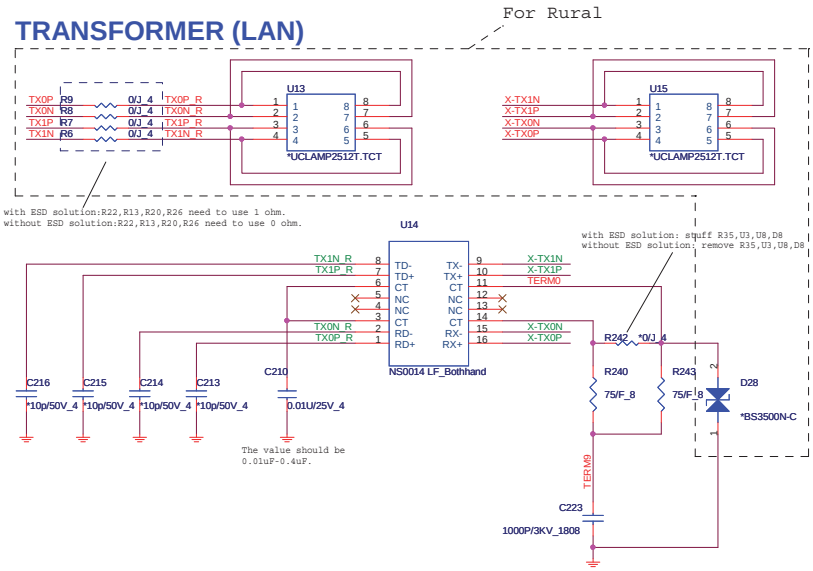


Quanta Computer Inc.
PROJECT : ZE6
Size | Document Number: USB on Board/LED/SW/HOLE | Rev: 1B
Date: Friday, March 11, 2011 | Sheet 17 of 35

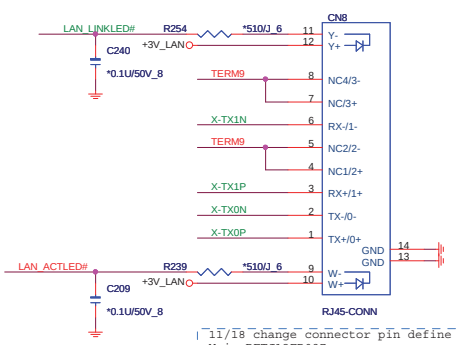
LAN (LAN)



TRANSFORMER (LAN)



RJ45 Connector (LAN)



Quanta Computer Inc.

PROJECT : ZE6

Size	Document Number	Rev
	LAN RTL8105TA-VC-CG	1B

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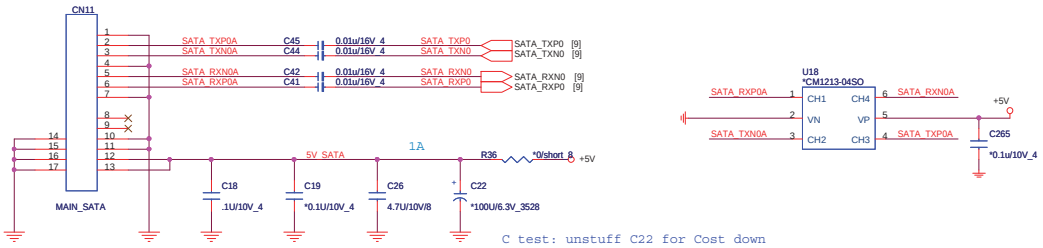

Quanta Computer Inc.

PROJECT : ZE6

Size	Document Number	Rev
	SATA-HDD	1B

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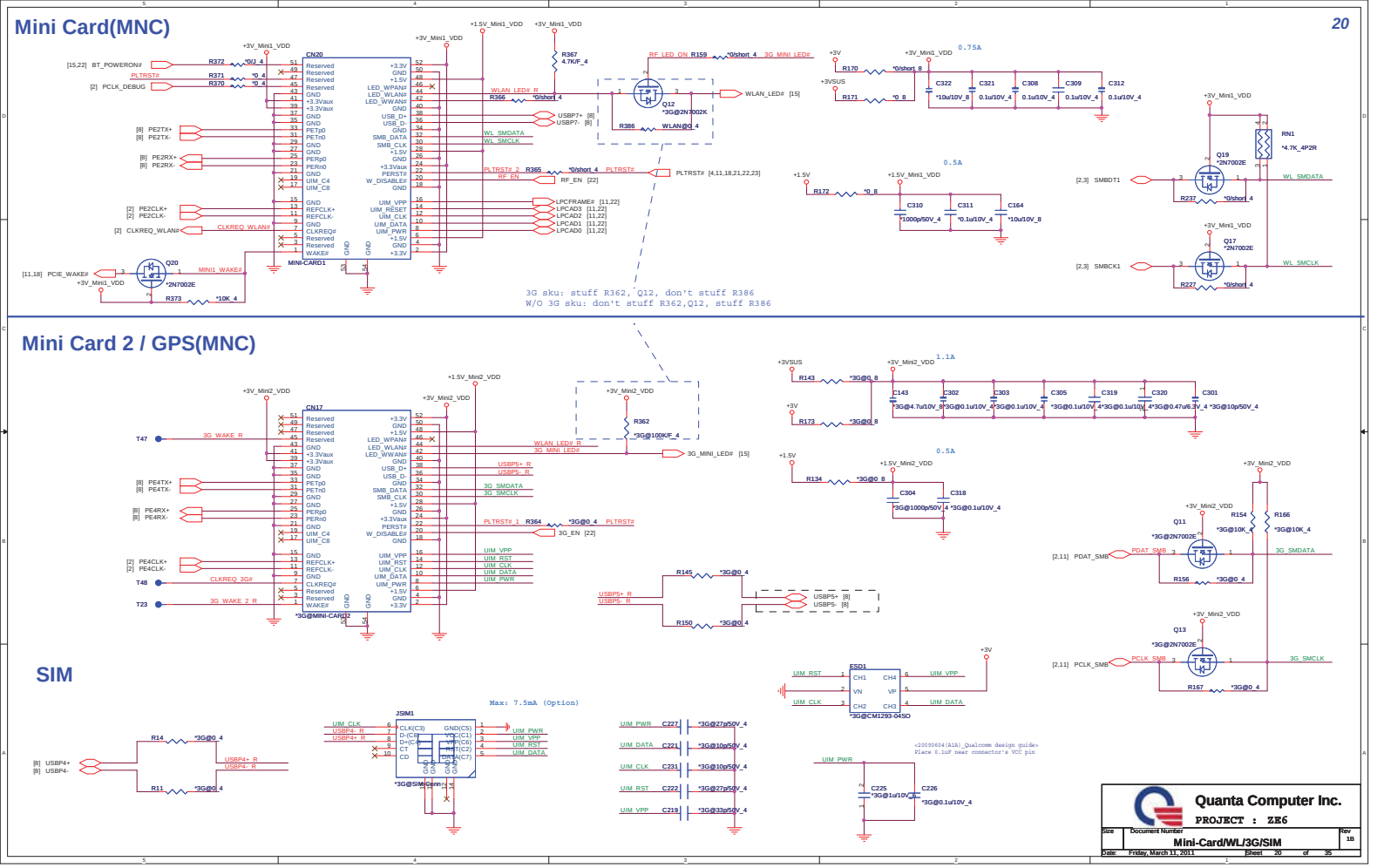
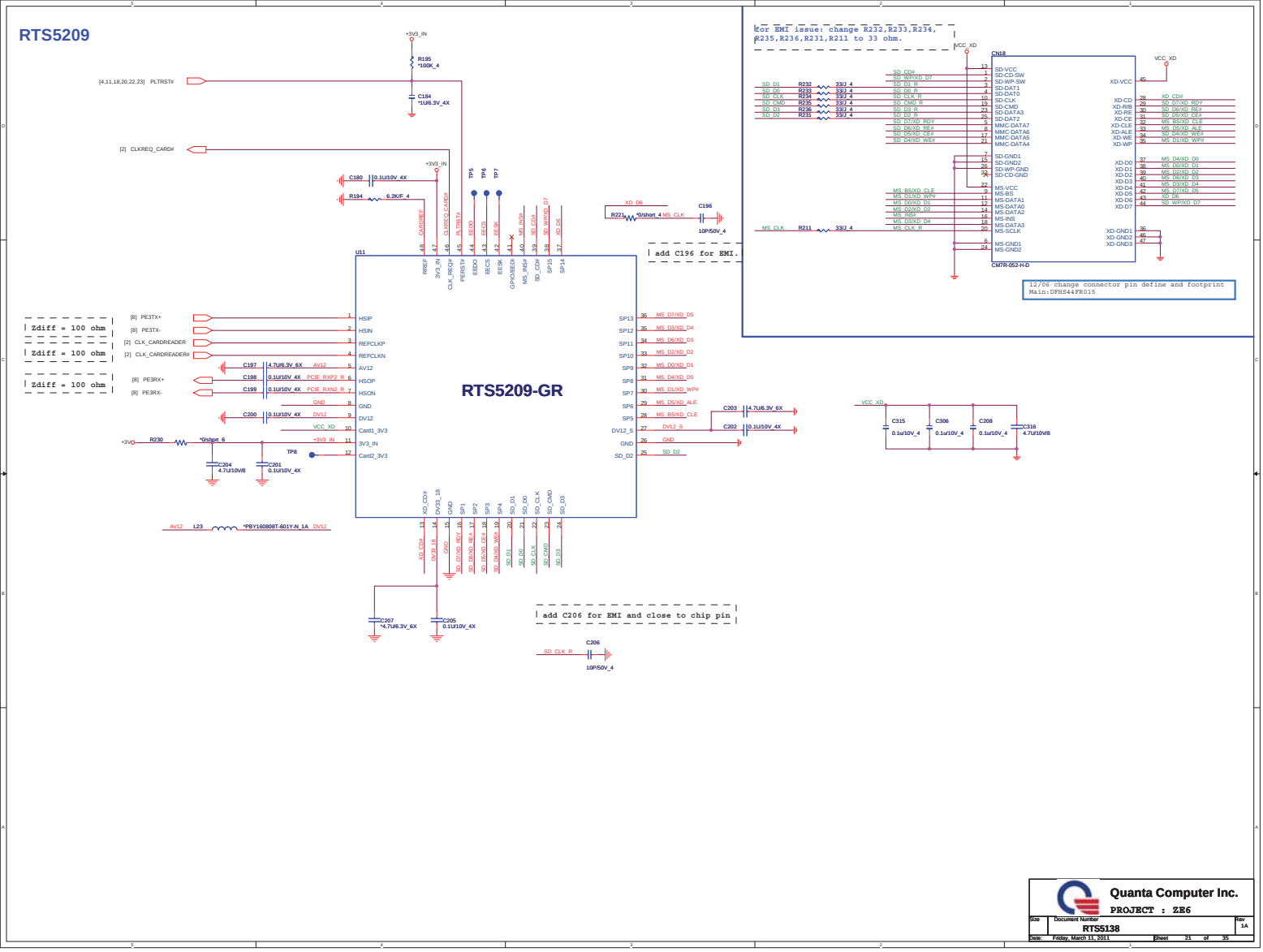
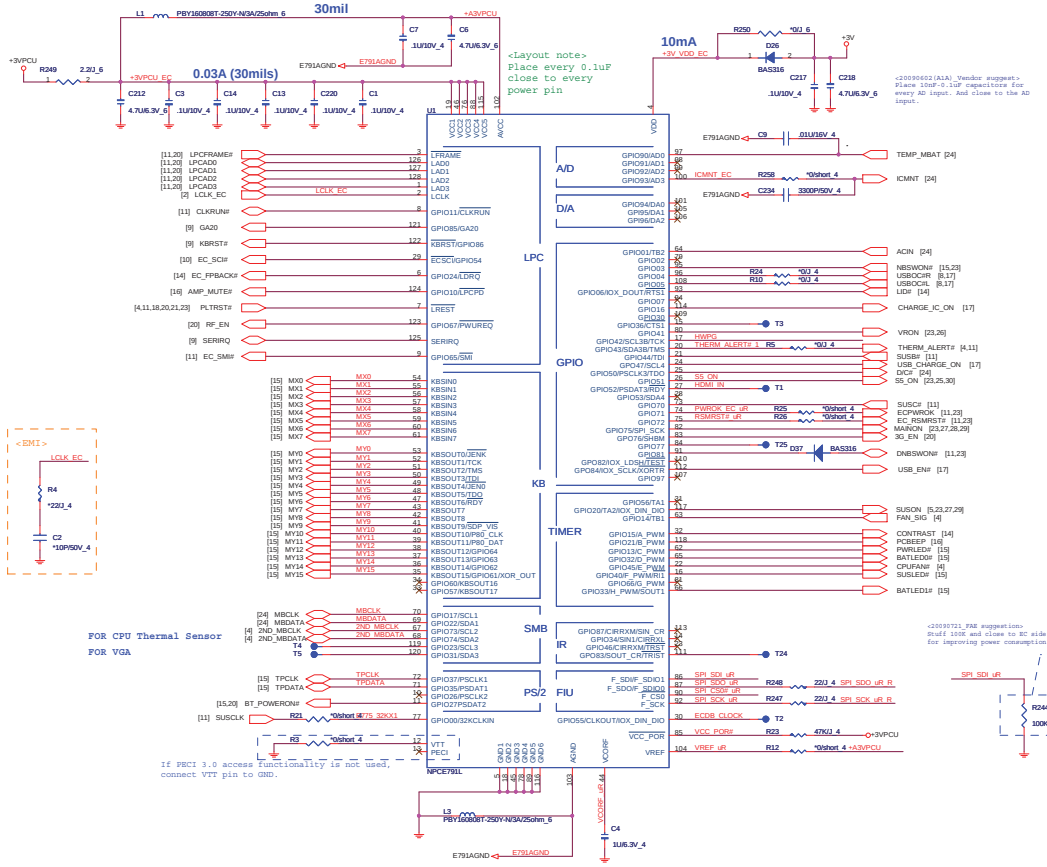
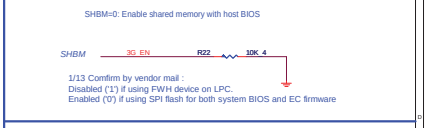


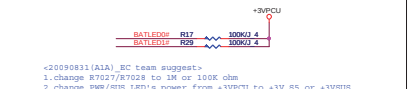


EC (KBC)



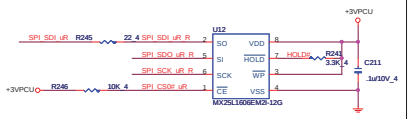
I/O ADDRESS SETTING(KBC)



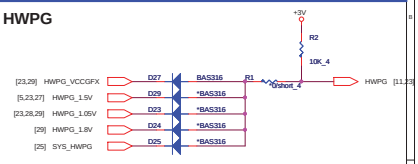


SM BUS PU(KBC)

SPI FLASH(KBC)



HWPG



INTERNAL KEYBOARD STRIP SET (KBC)

SM BUS ARRANGEMENT TABLE

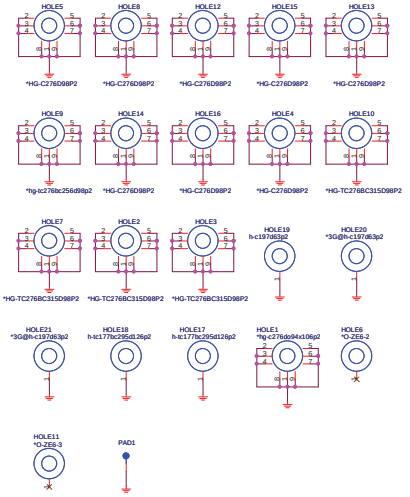
SM Bus 1	Battery
SM Bus 2	CPU thermal sensor

INTERNAL KEYBOARD STRIP SET(KBC)

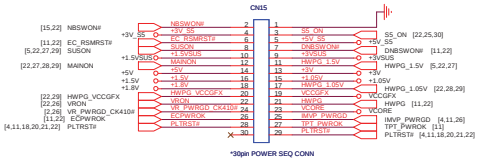
Quanta Computer Inc.			
PROJECT : ZE6			
Size	Document Number		Rev
	WPCE781 & FLASH		1A
Date: Friday, March 11, 2011		Sheet 22 of 35	

EMI

Hole



Power Sequence Connector 30pin (CPU)



1	GND	11	HWPG_1.5V	21	HWPG
2	NBSWON#	12	MAINON	22	VRON
3	S5_ON	13	+3V	23	VCORE
4	+3V_S5	14	+5V	24	VR_PWRGD_CK410#
5	+5V_S5	15	+1.05V	25	IMVP_PWRGD
6	EC_RSMRST#	16	+1.5V	26	ECPWROK
7	DNBSWON#	17	HWPG_1.05V	27	TPT_PWROK
8	SUSON	18	+1.8V	28	H_PWRGD
9	+3VSUS	19	VCCGFX	29	PLTRST#
10	+1.5VSUS	20	HWPG_VCCGFX	30	RESERVE

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	HDMI(1/2)	1A

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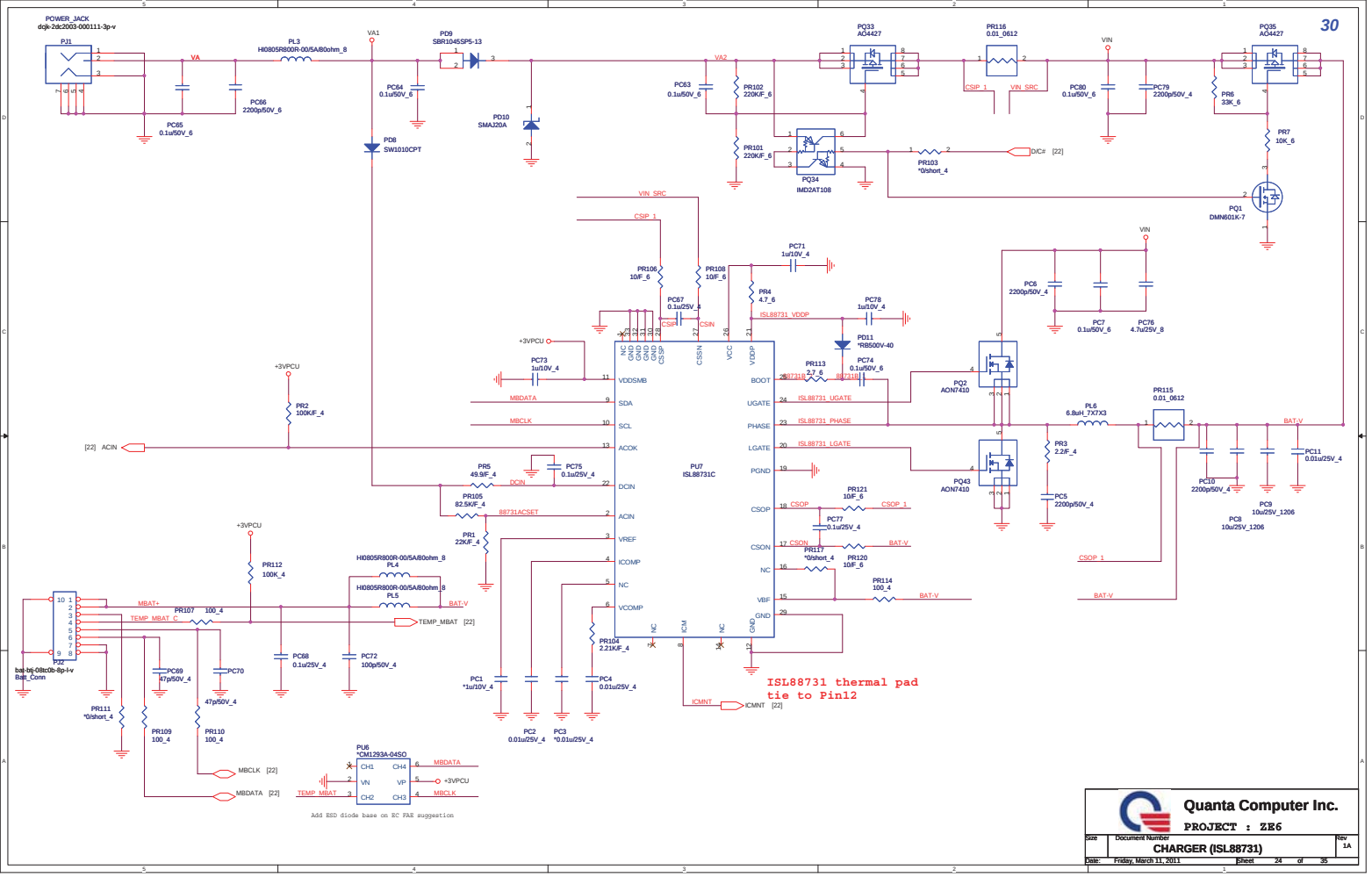
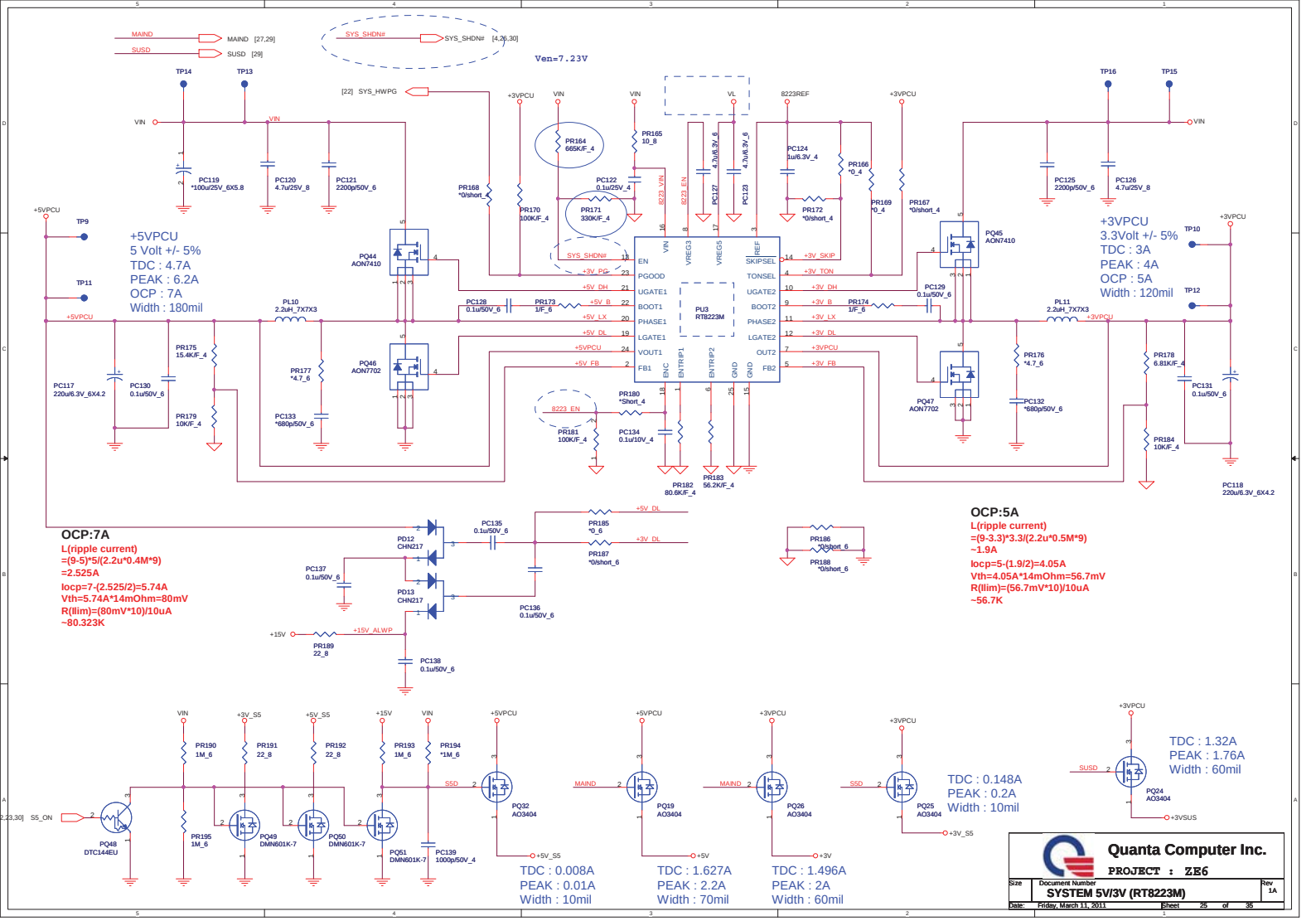
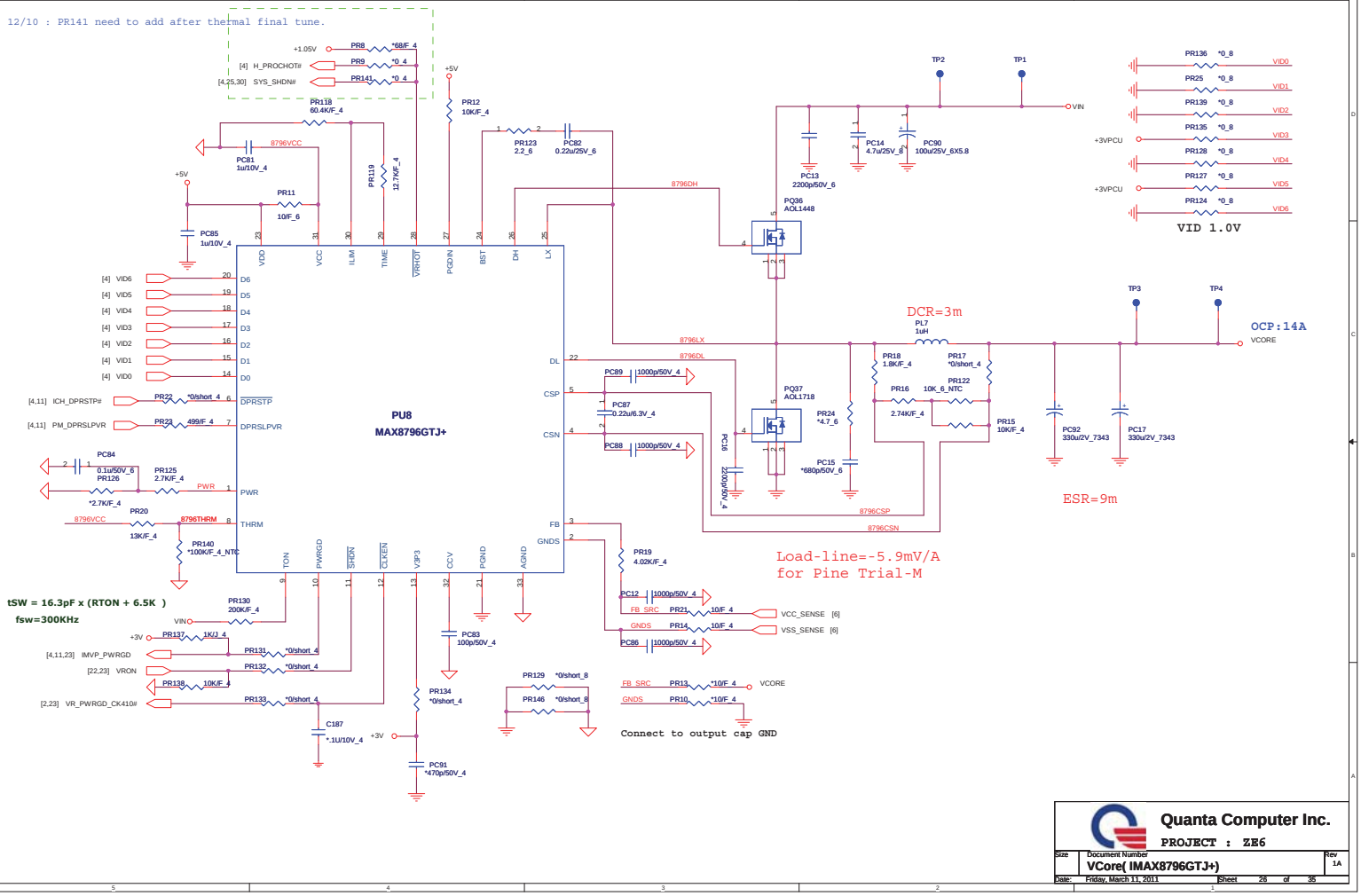
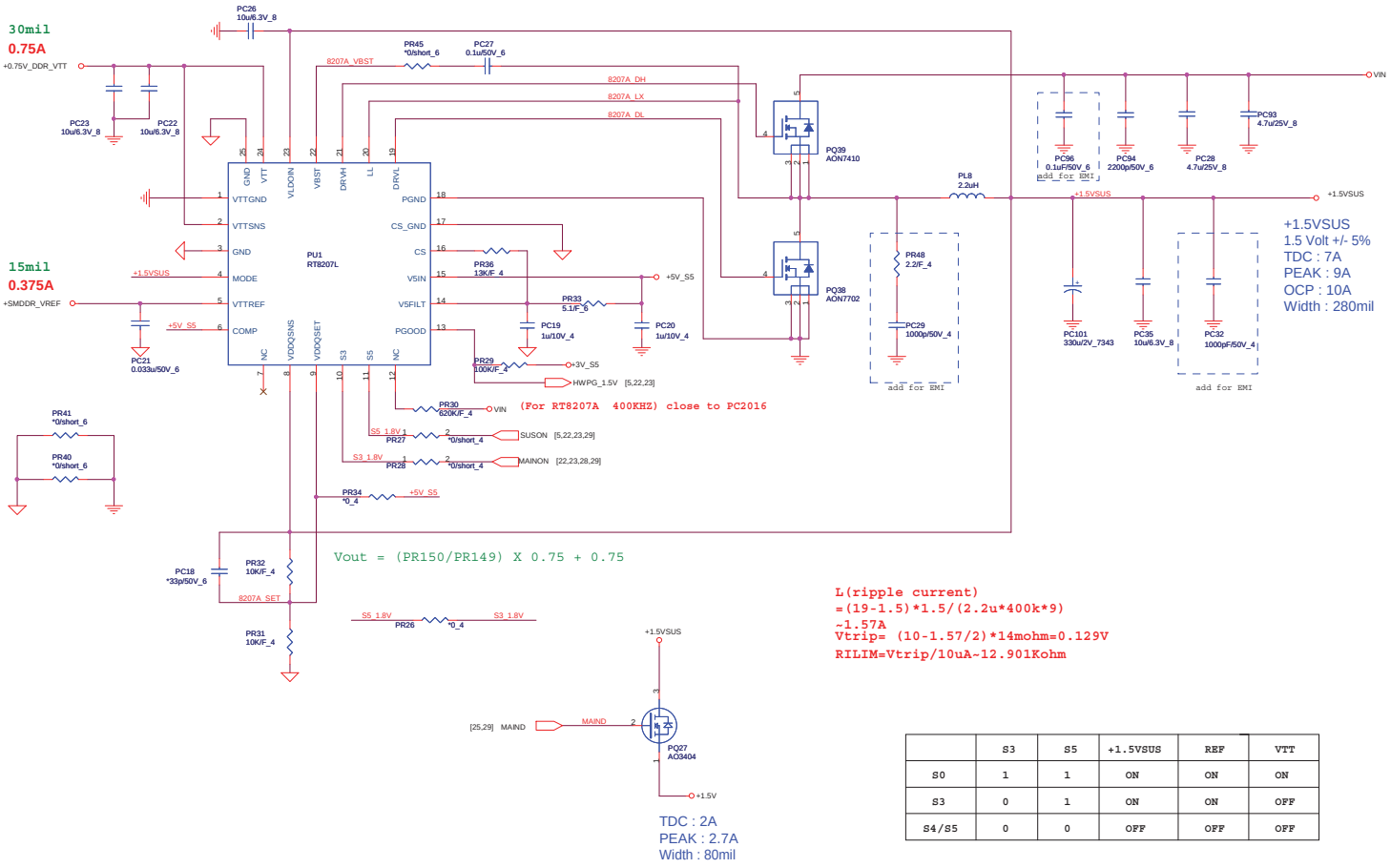






[PWM]



L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*9)
~1.57A
Vtrip= (10-1.57/2)*14mohm=0.129V
RILIM=Vtrip/10uA~12.901Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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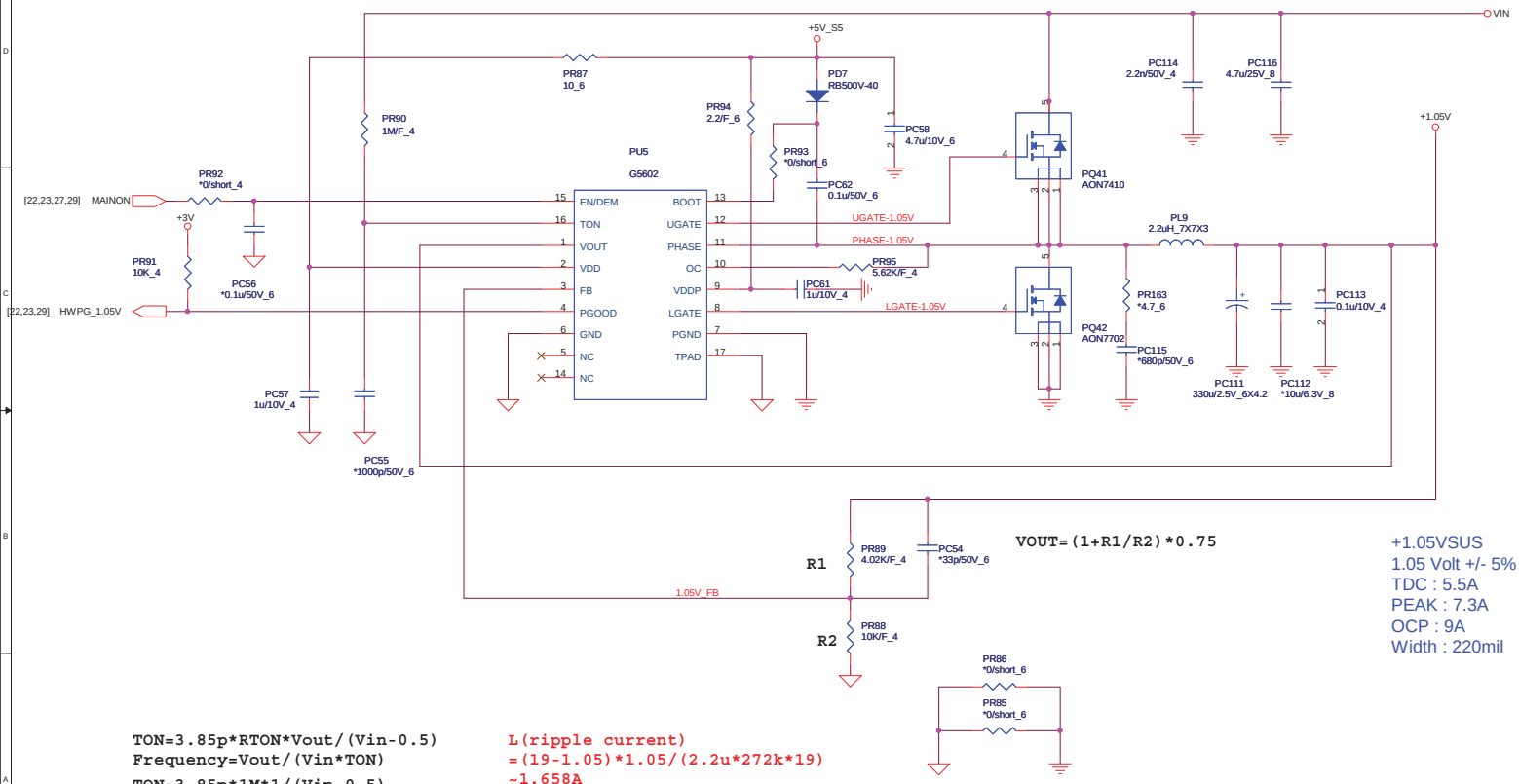

VOUT=(1+R1/R2)*0.75

+1.05VSUS
1.05 Volt +/- 5%
TDC : 5.5A
PEAK : 7.3A
OCP : 9A
Width : 220mil

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.658A
Rth=14m*(9-0.829)/20uA
RILIM=5.719Kohm

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	+1.05V(G5602)	1A
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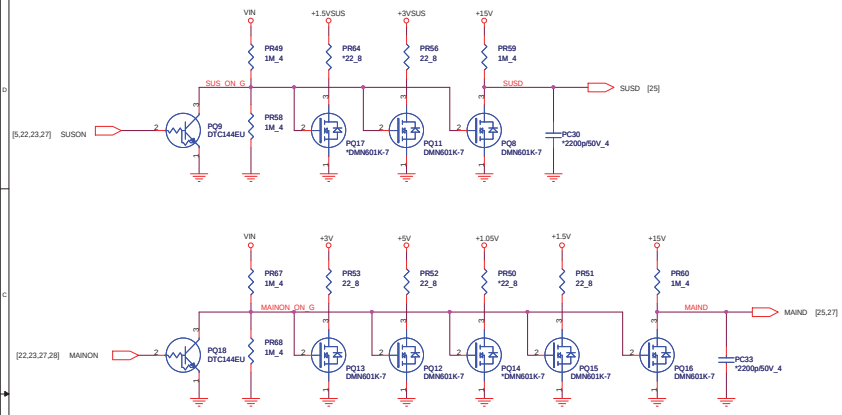
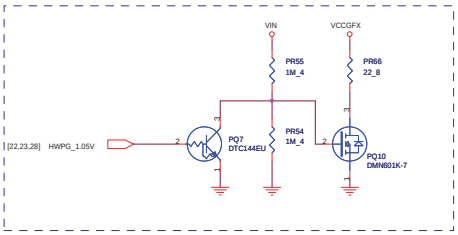
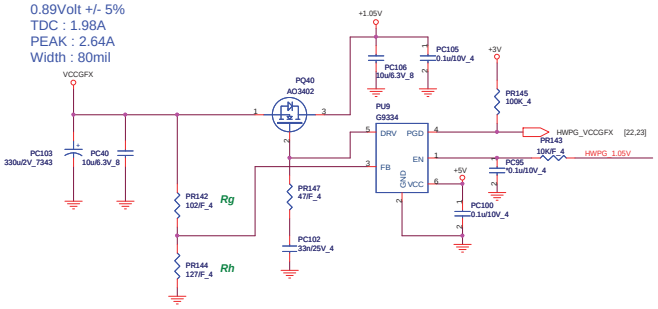
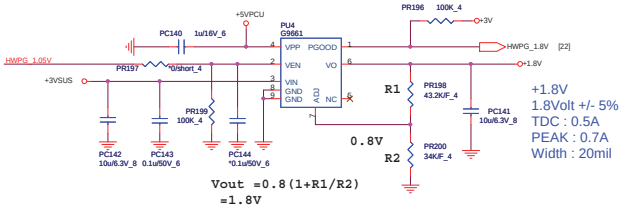




VCCGFX
0.89Volt +/- 5%
TDC : 1.98A
PEAK : 2.64A
Width : 80mil



*Vout1 = (1+Rg/Rh)*0.5*



Vout =0.8(1+R1/R2)
=1.8V

+1.8V
1.8Volt +/- 5%
TDC : 0.5A
PEAK : 0.7A
Width : 20mil

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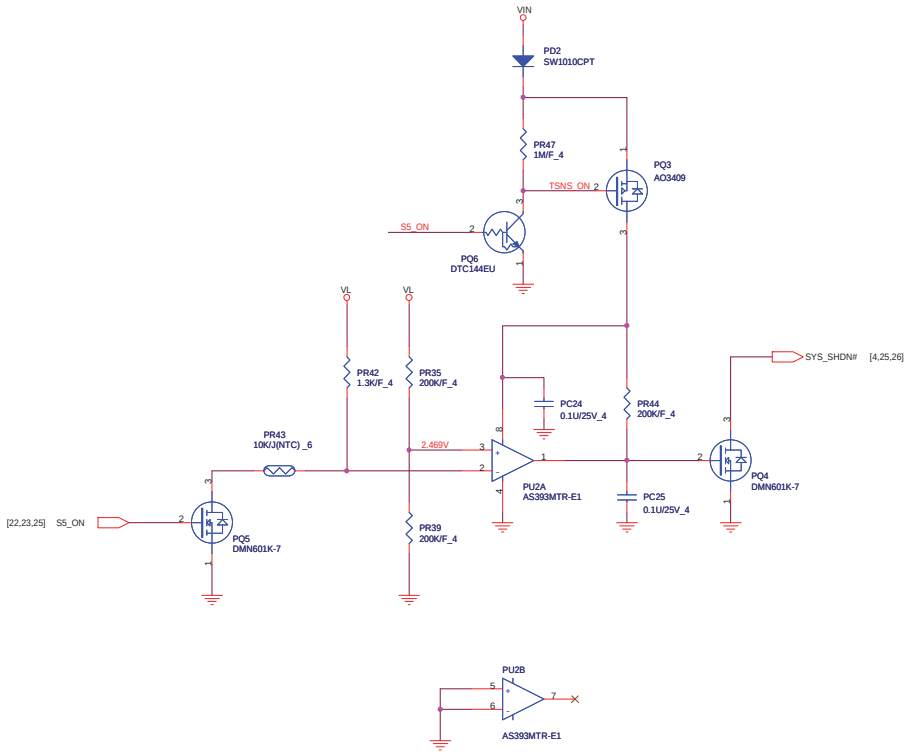
Thermal Protection (DCD)



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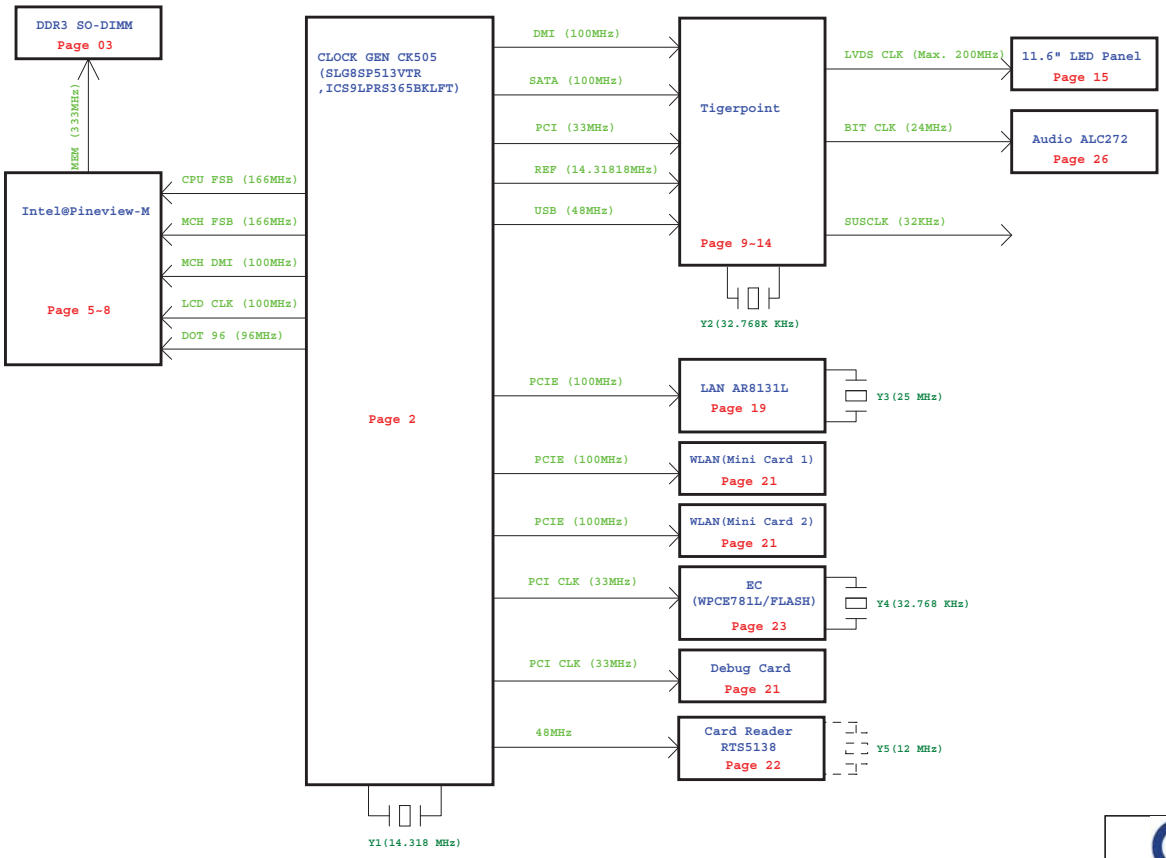

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Size	Document Number	Rev
	Clock Distribution Diagram	1B

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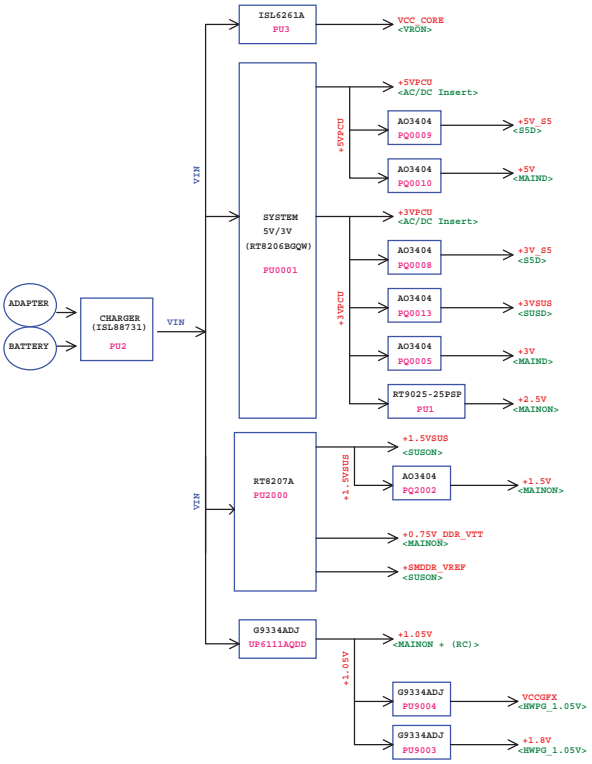

POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connecter
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

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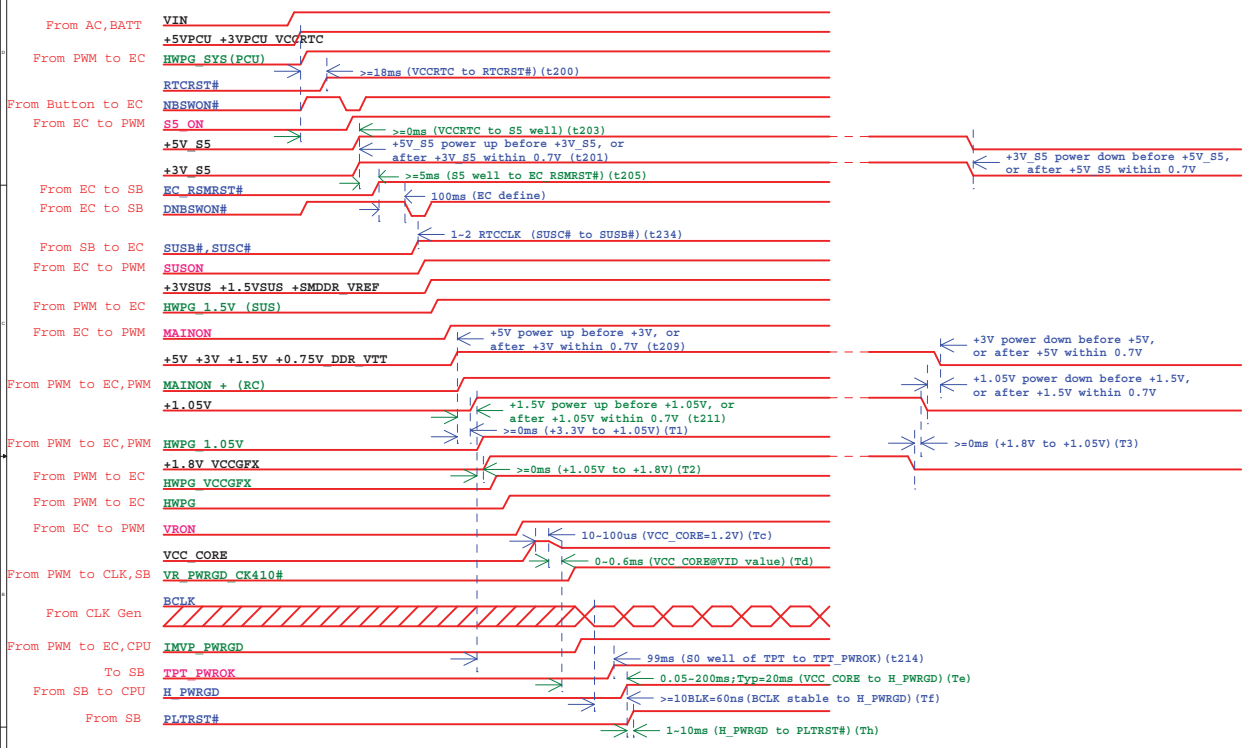
PROJECT : XE6
Power Tree

ZGA Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			
Power Plane	+3VPCU	+3V	
MOS CKT (Level shift)	X	X	

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SYSTEM INFORMATION
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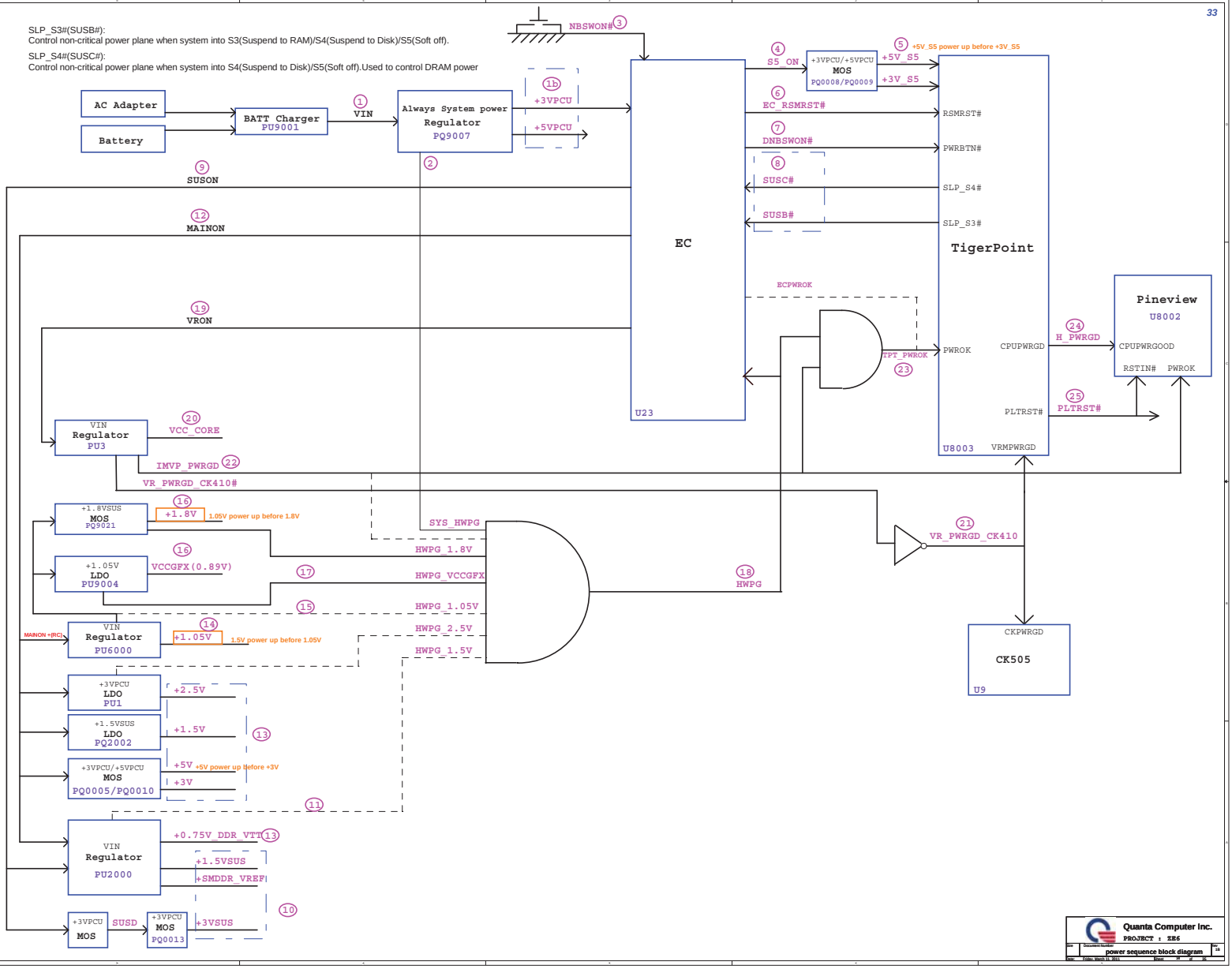
SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



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PROJECT : ZE6
power sequence block diagram

Model	REV	CHANGE LIST	MODEL	ZE6 FROM	ZE6 To
ZE6 MB	A1	FIRST RELEASED: (PCB:A)		X	1A
	B	Page 2 : add R374 for CLK GEN change version			
		Page 11 : change RTC connector type from SMT to holder.			
		Page 15 : modify TP connector pin define			
		Page 16 : modify audio and mic connector pin define.			
		Page 17 : modify USB charger IC circuit to support or not support charger function.			
		Page 29 : modify 1.8V IC enable signal to HWPG_1.05V			
		20110117 Page 15 : add CP1-CP6 for EMI issue			
		20110117 Page 15 : for EMI issue: change R232,R233,R234,R235,R236,R231,R211 to bead CX5BB121001			
		20110118 Page 27 : for EMI issue: add PC96 ,PC32 and stuff PR48, PC29			
		20110118 Page 30 : Thermal temperature setting at 75C, change PR42 from 1.54K/F to 1.3K/F			
	B	20110131 Page 14 : add 5V into LCD connector for IVO panel to use.			
	1D				

DOC NO.					
PROJECT MODEL :	11.6	APPROVED BY:		DATE:	2009/12/05
PART NUMBER:		DRAWING BY:		REVISON:	1B

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Size | Document Number: Change list | Rev 1B
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