

MODEL NAME : *PLW00*

PCB NO : *LA-7451P*

BOM P/N : *TBD*
TBD

Dell/Compal Confidential

Schematic Document

Breitling (Huron River)

Sandy Bridge (BGA) + Cougar Point (standard)

DISCRETE VGA N12P-GV-S-A1 (optimus)

2011-07-12

Rev: 1.0

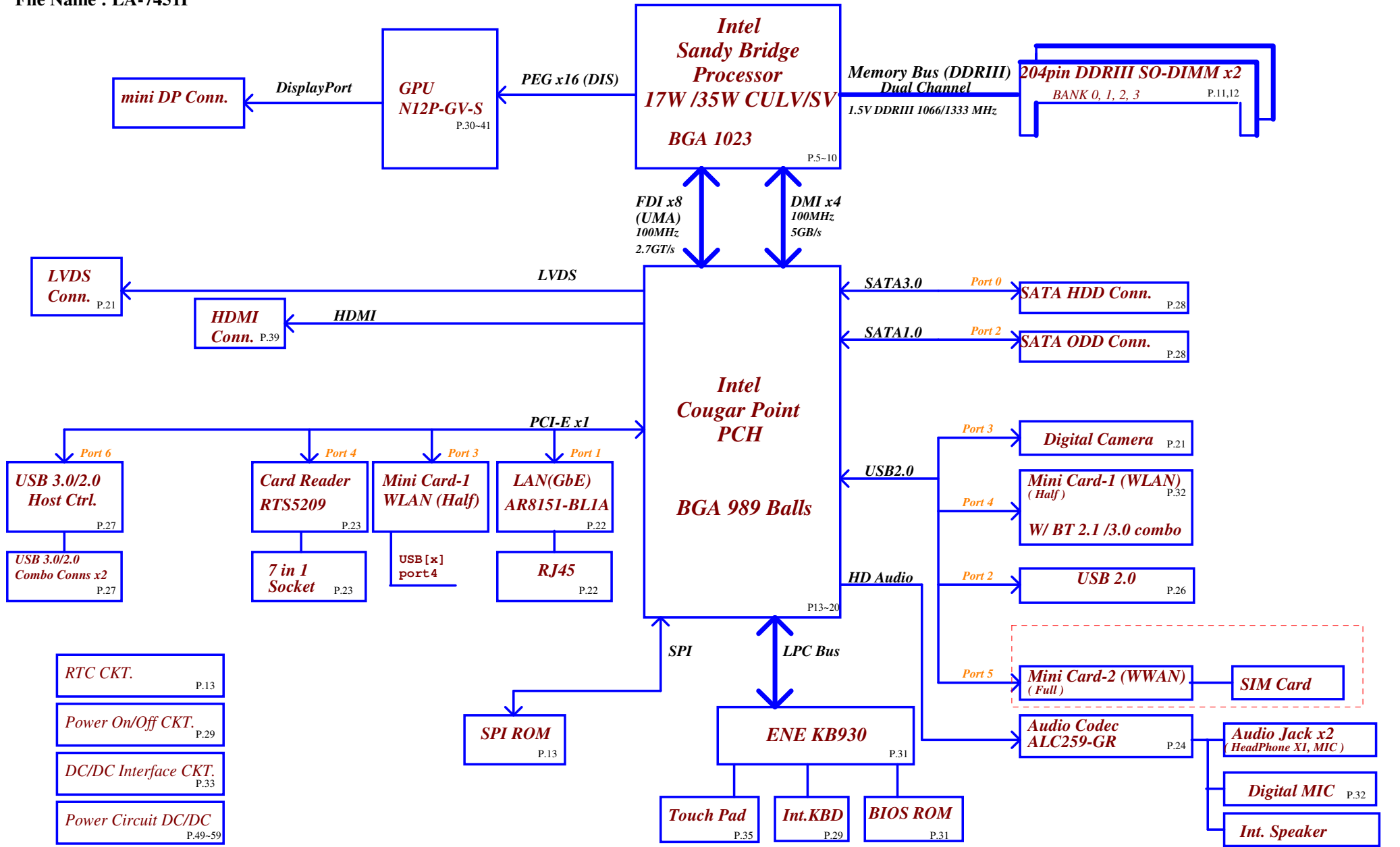
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	<i>Cover Page</i>	
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Project Code : PLW00

File Name : LA-7451P

FFS P.28 Fan Control P.30 CPU XDP Conn. P.6

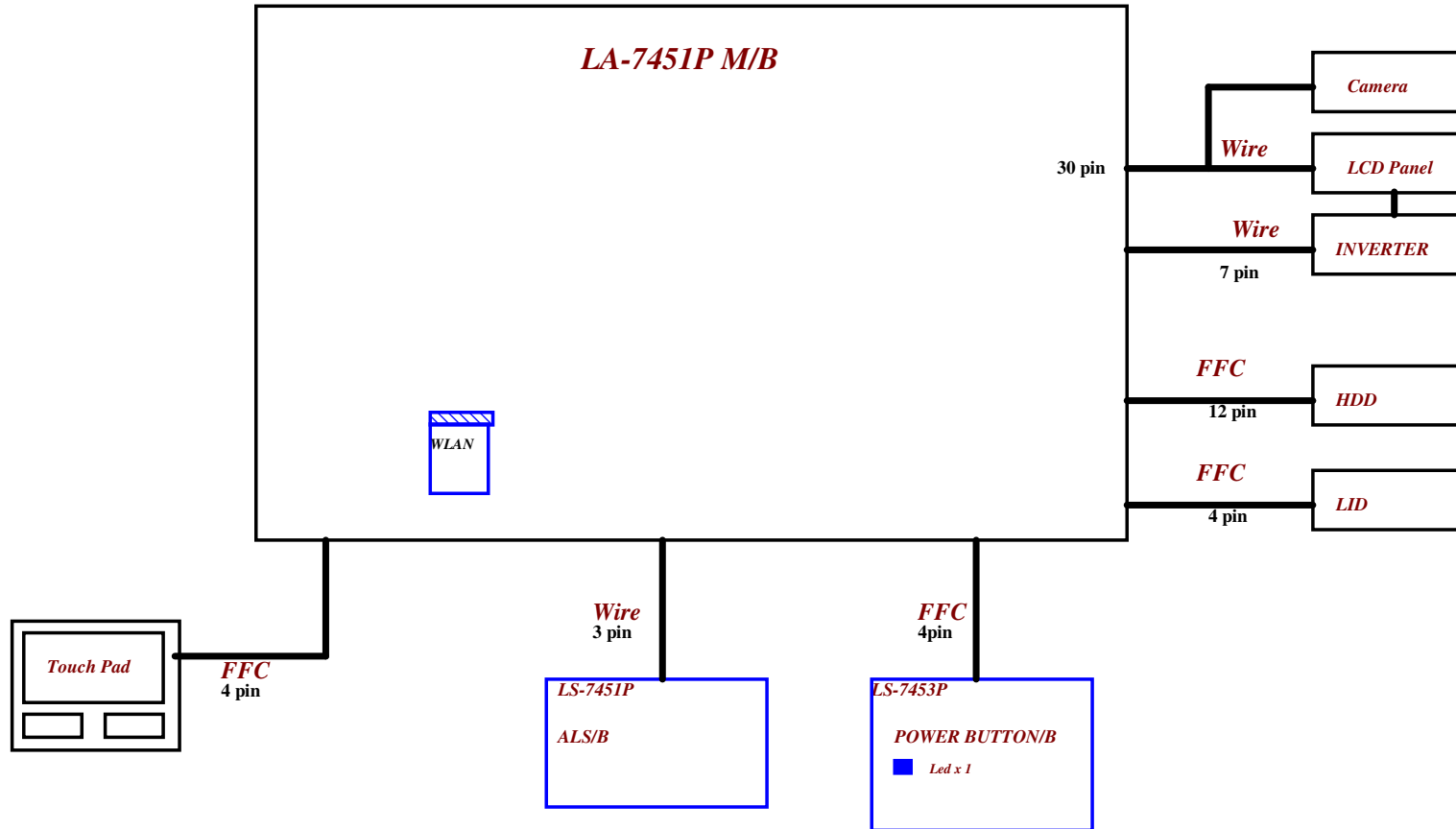


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Board ID Table for AD channel

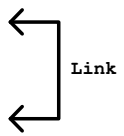
Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	BATT	SODIMM	SODIMM	FFS	VGA Thermal Sensor	XDP	Charger
EC_SMB_CK1 EC_SMB_DAI	KB930	V						
EC_SMB_CK2 EC_SMB_DAI2	KB930							
PCH_SML0CLK PCH_SML0DATA	PCH							
PCH_SML1CLK PCH_SML1DATA	PCH						V	
MEM_SMBCLK MEM_SMBDATA	PCH		V	V	V			V



PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (2.0 Ext UP Side)
	2	None
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN)
	6	None
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
13	None	

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

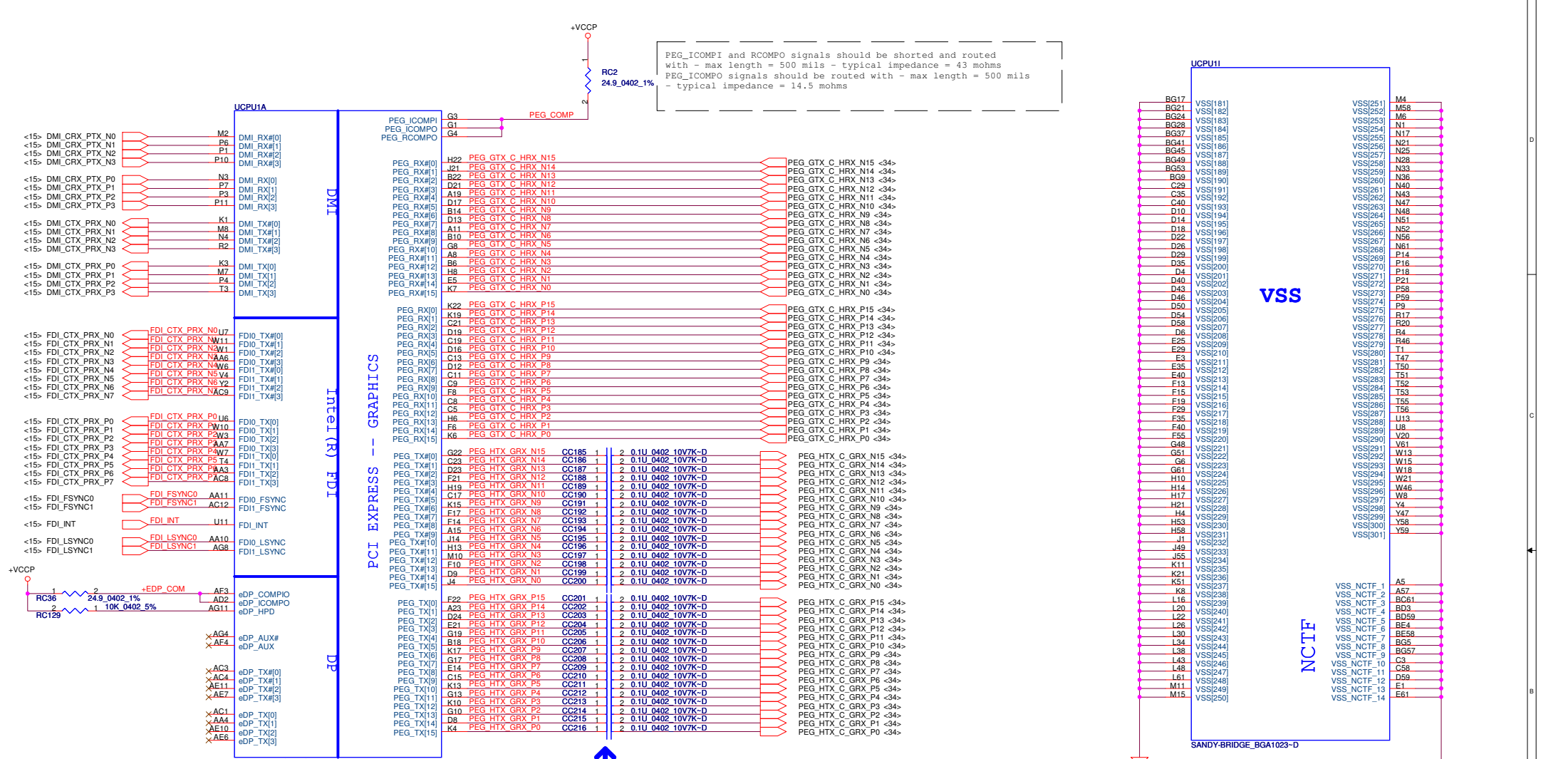
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None			

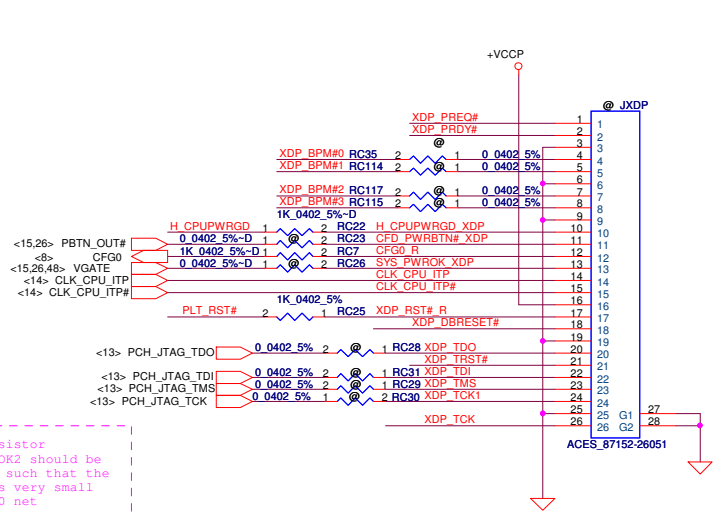
Symbol Note :



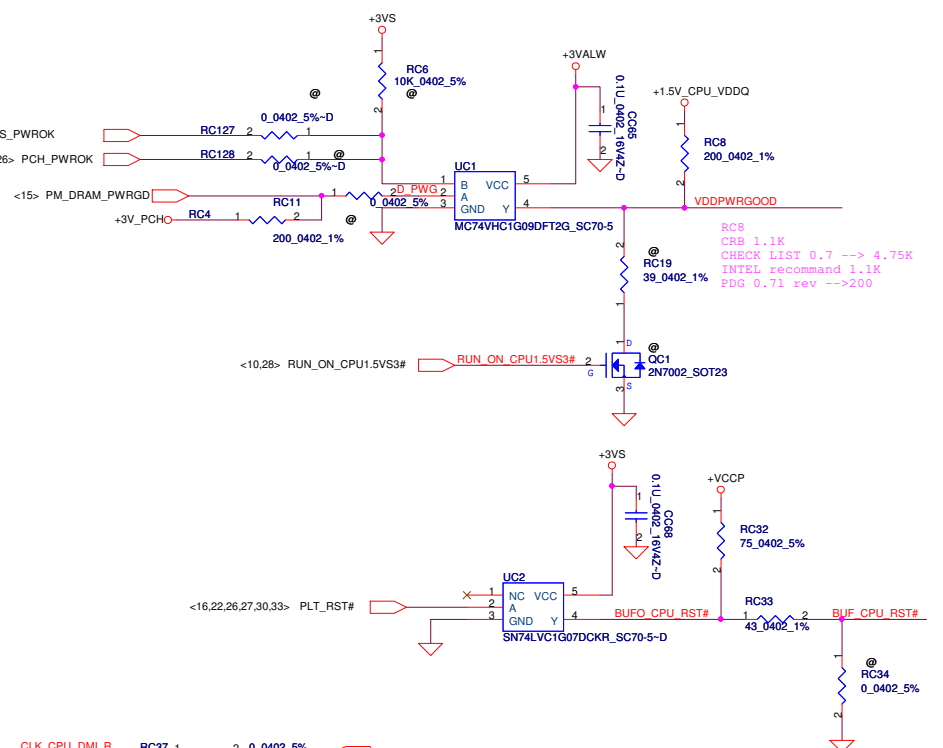
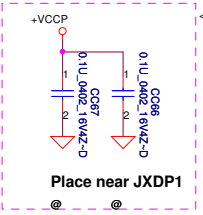


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Issued Date	2010/12/20	Deciphered Date	2011/12/20	PROCESSOR(1/6) DMI, FDI, PEG	
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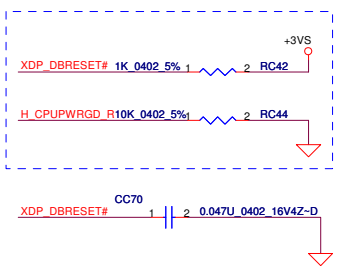
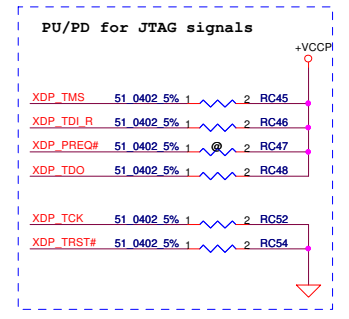
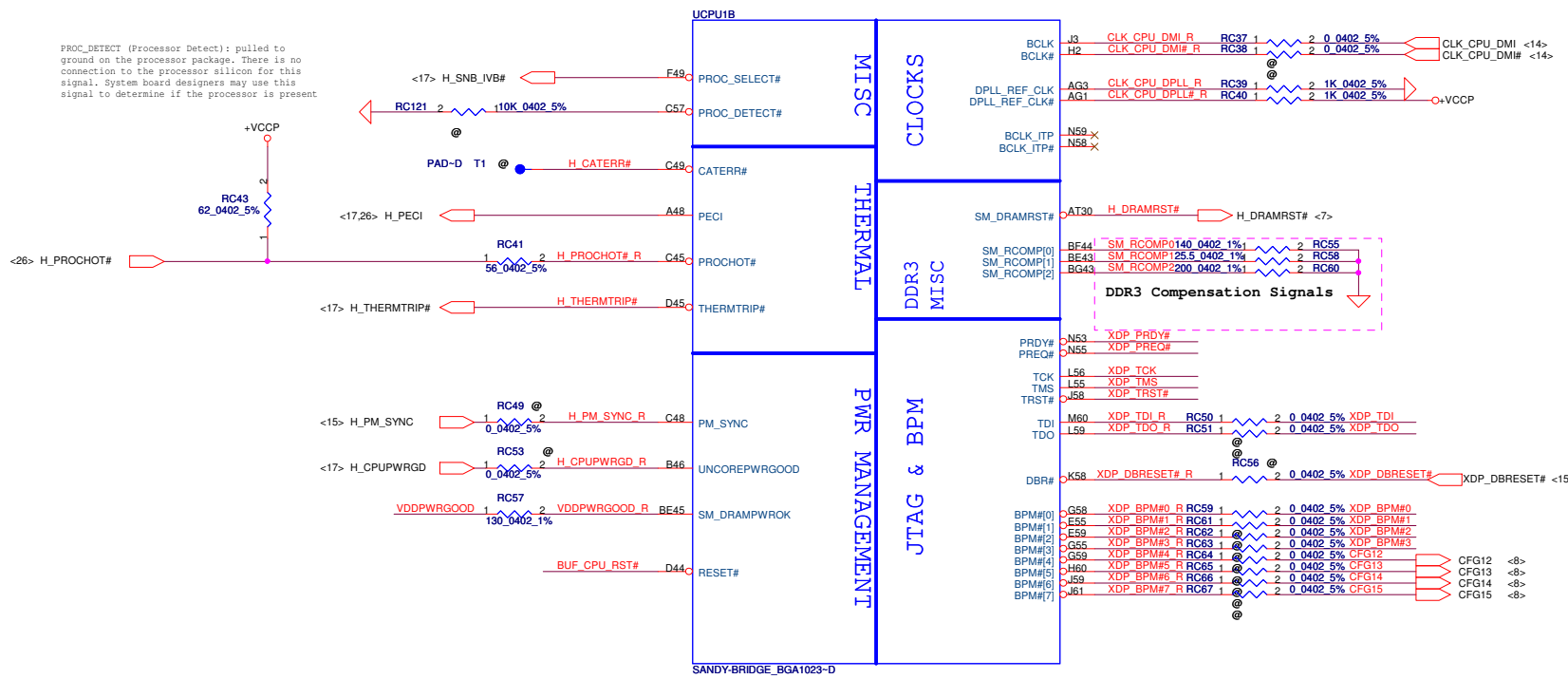
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)



The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net



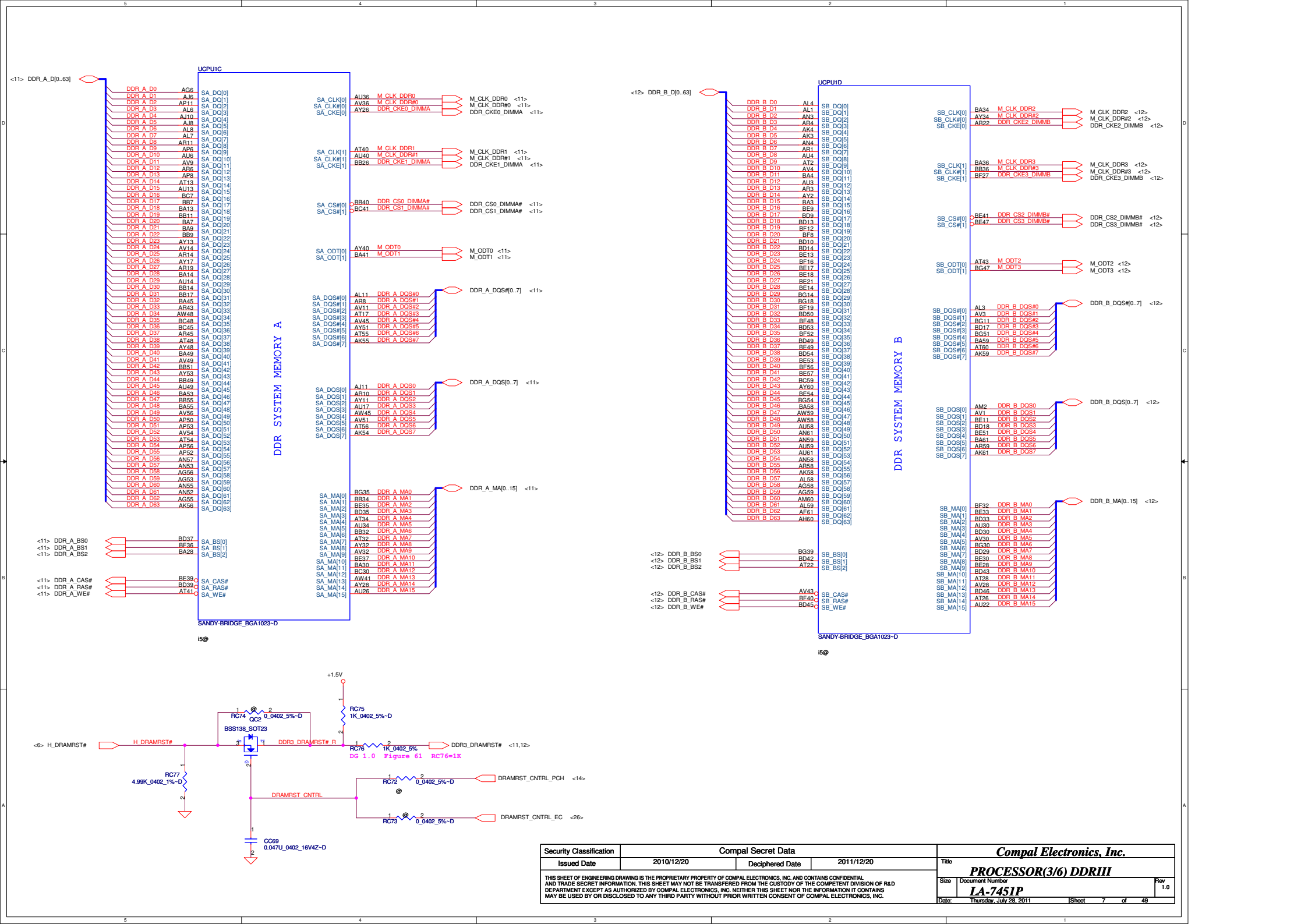
PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present



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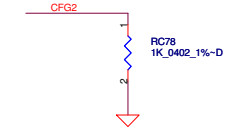
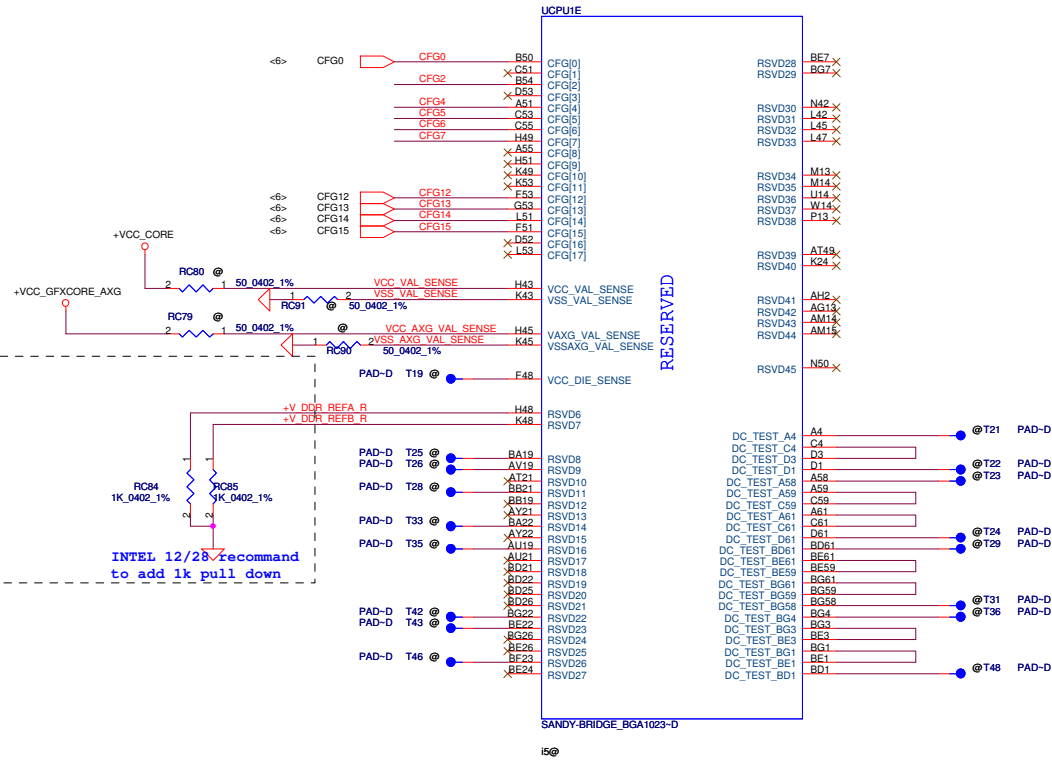
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PROCESSOR(2/6) PM,XDP,CLK		
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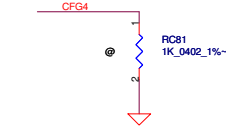


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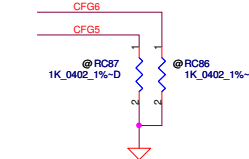
CFG Straps for Processor



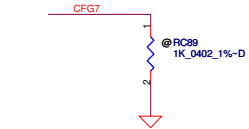
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



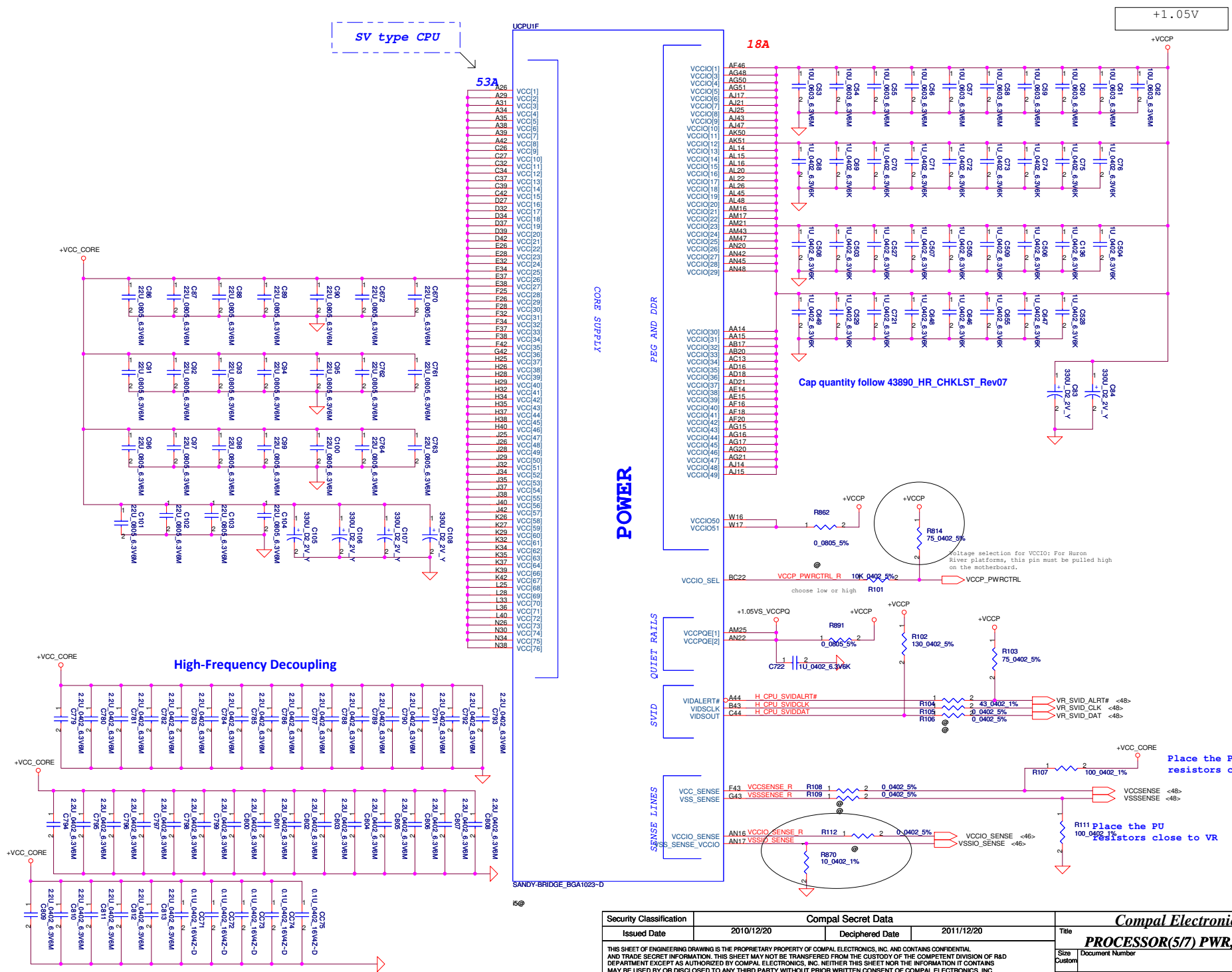
Display Port Presence Strap	
CFG4	*1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SV type CPU

+1.05V

POWER

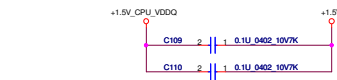
Cap quantity follow 43890_HR_CHKLIST_Rev07

High-Frequency Decoupling

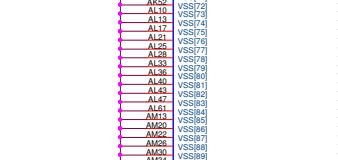
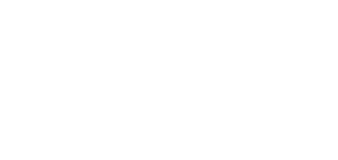
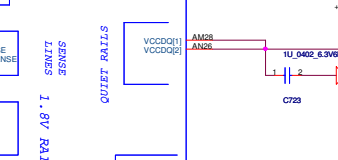
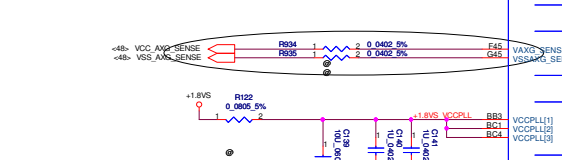
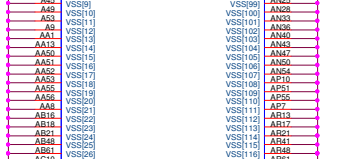
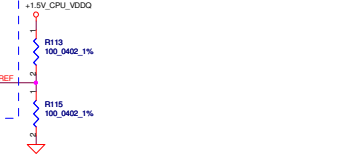
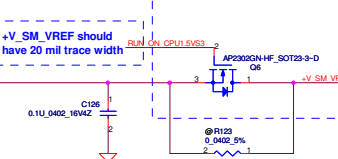
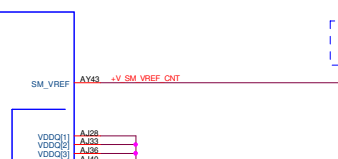
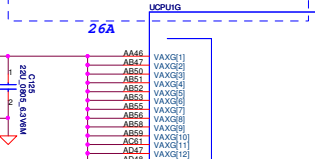
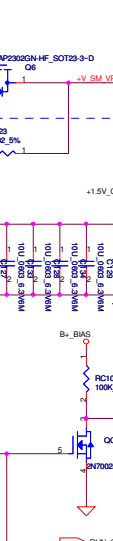
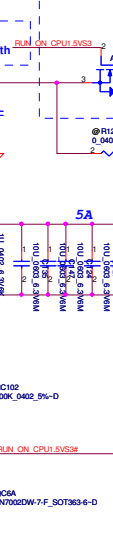
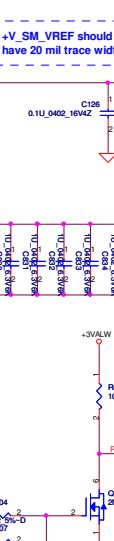
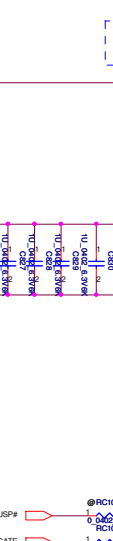
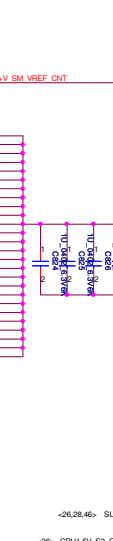
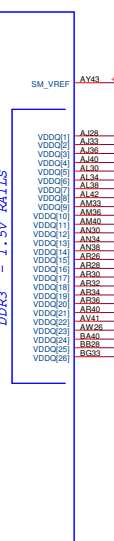
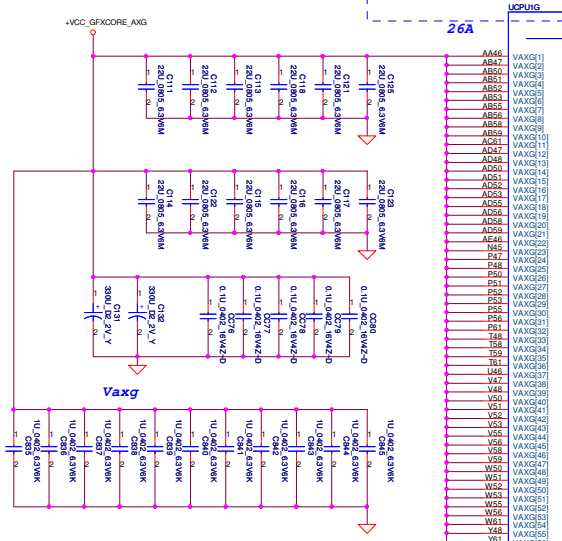
Place the PU resistors close to CPU

Place the PU resistors close to VR

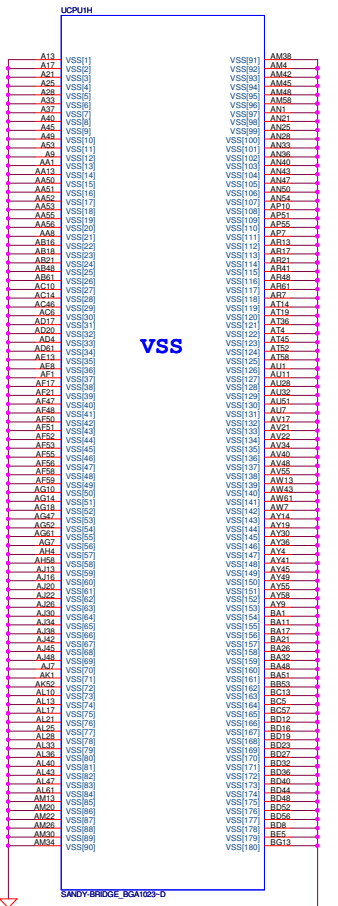
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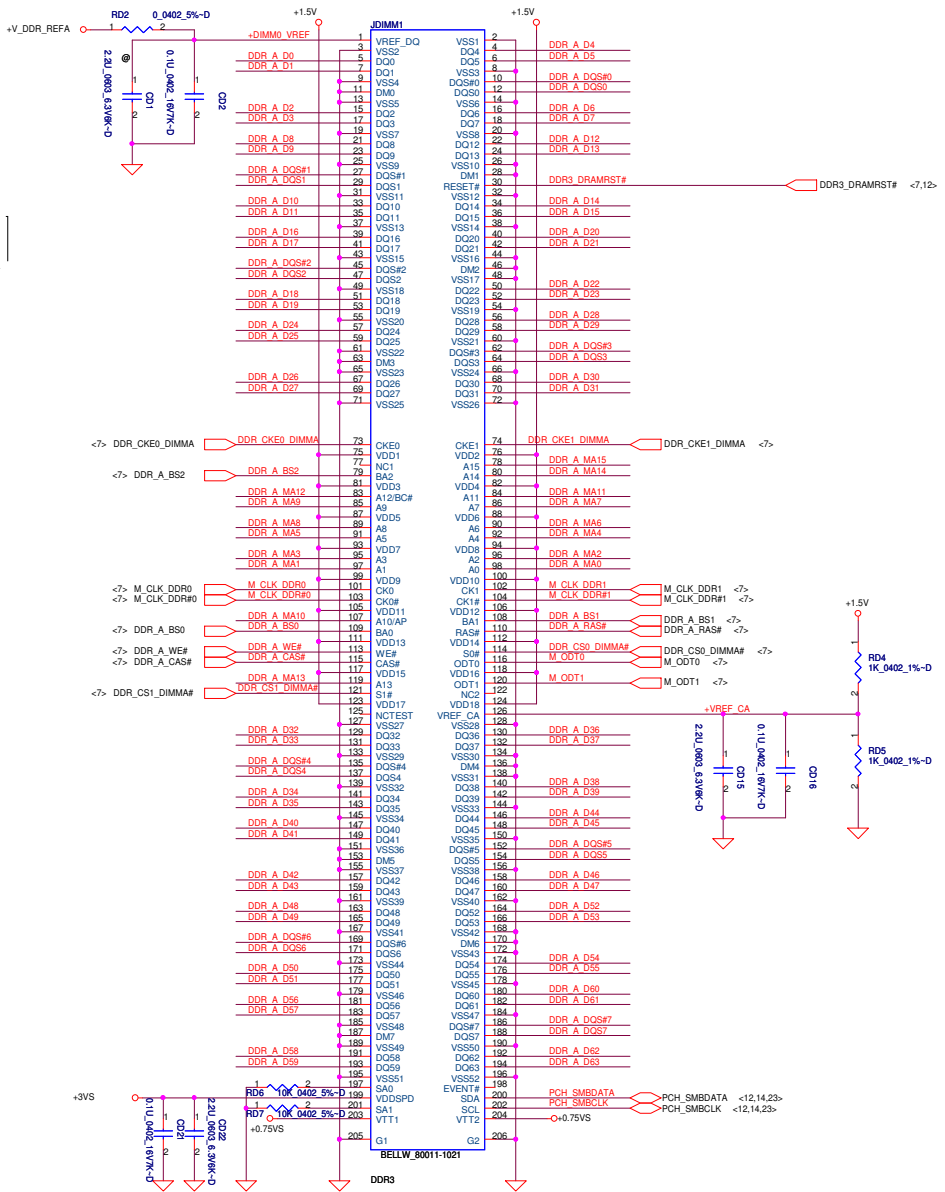
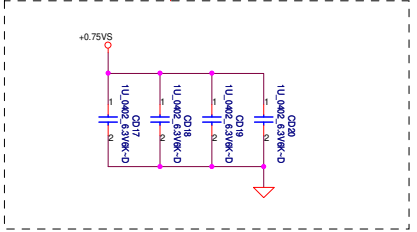
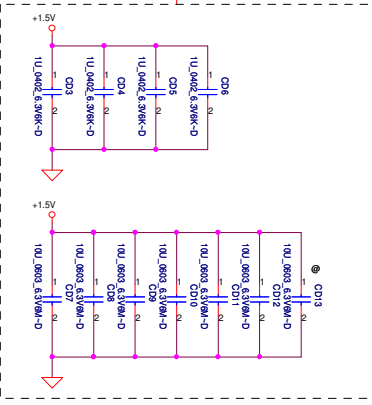
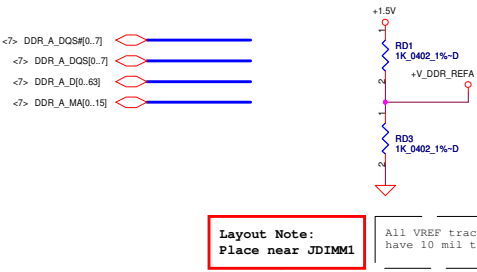


- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design.
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



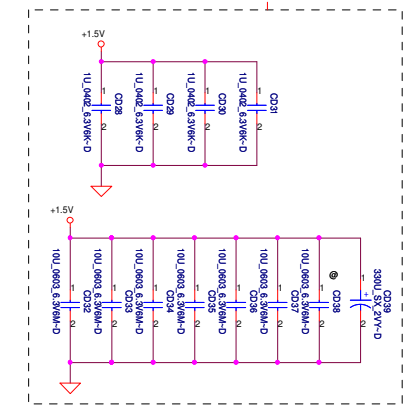
VDD[0]	VDD[1]	VDD[2]	VDD[3]
0	0	0.30 V	Yes
1	1	0.30 V	Yes
2	2	0.30 V	Yes
3	3	0.30 V	Yes



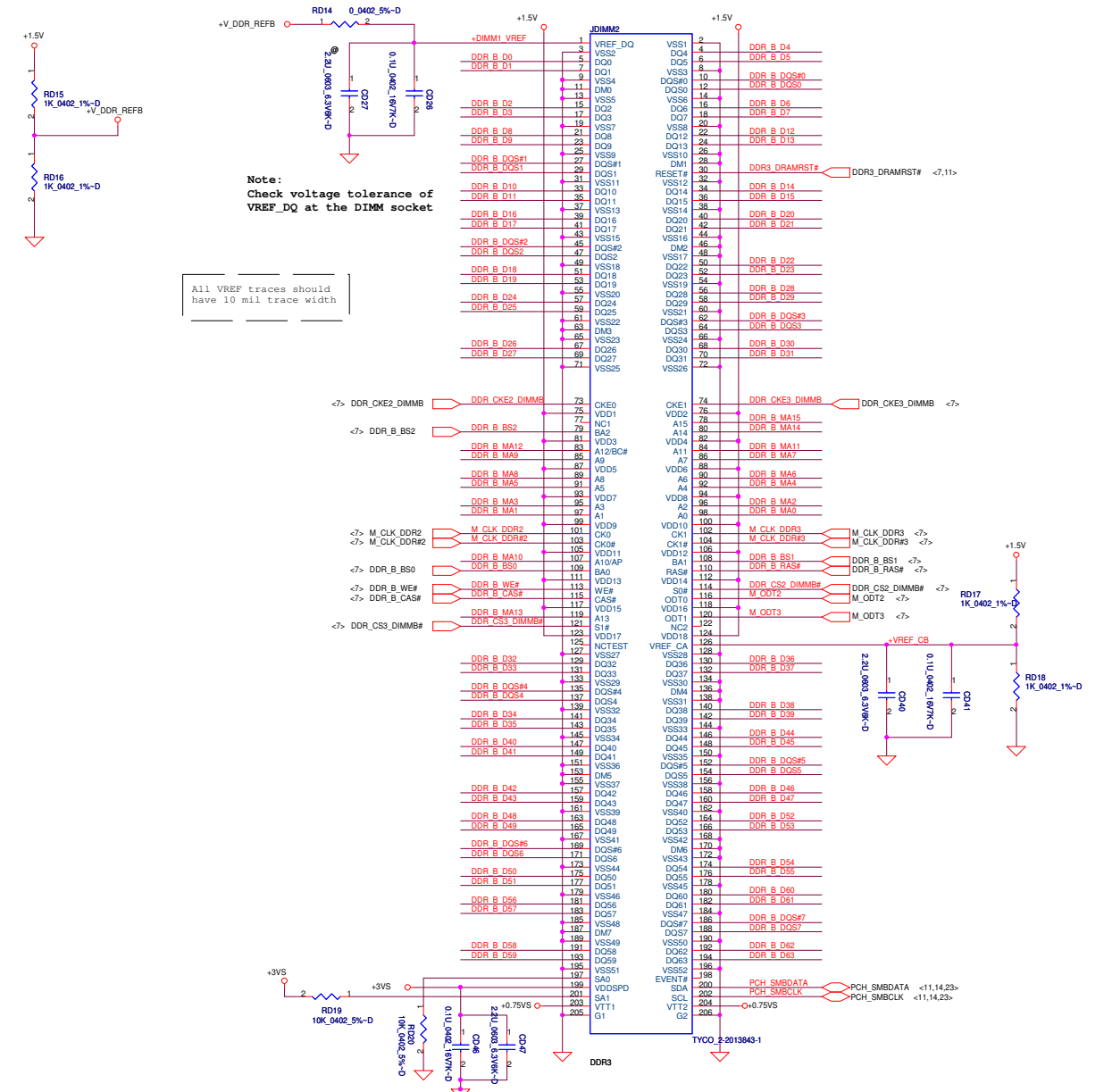
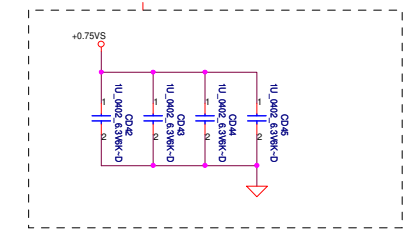


- <-> DDR_B_DQS#[0..7]
- <-> DDR_B_DQS#[0..7]
- <-> DDR_B_DQ[0..63]
- <-> DDR_B_MA[0..15]

Layout Note:
Place near JDIMMB



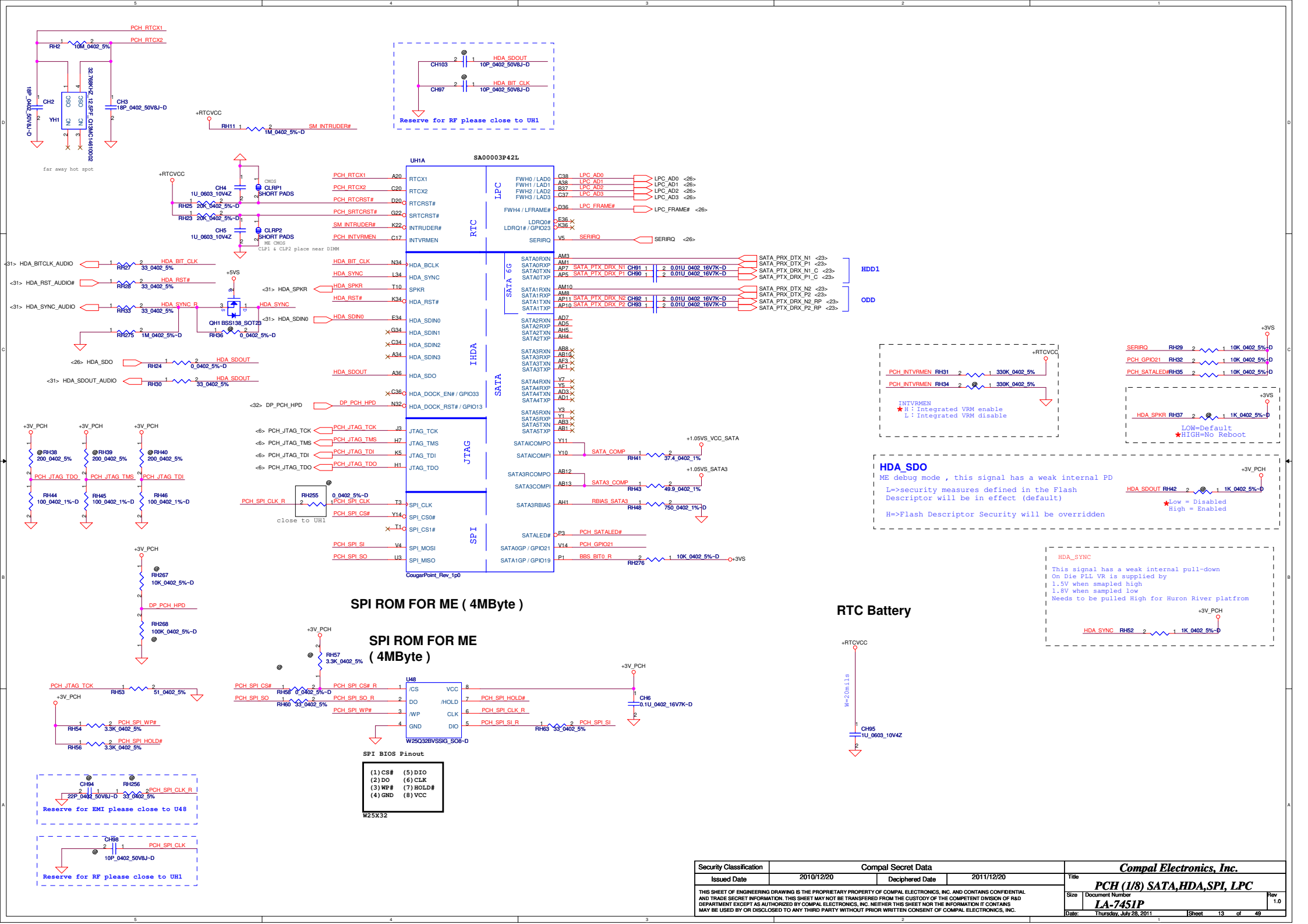
Layout Note:
Place near JDIMMB.203,204



Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

All VREF traces should have 10 mil trace width

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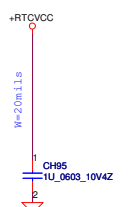
SPI ROM FOR ME (4MByte)

SPI ROM FOR ME (4MByte)

SPI BIOS Pinout

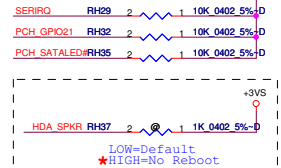
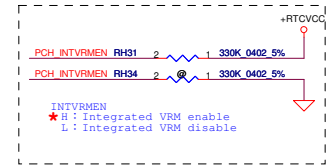
(1) CS#	(5) DIO
(2) DO	(6) CLK
(3) WP#	(7) HOLD#
(4) GND	(8) VCC

RTC Battery

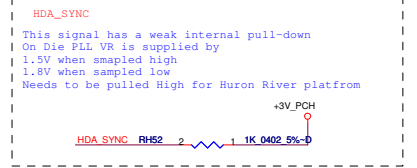


HDA_SDO

ME debug mode, this signal has a weak internal PD
 L=>security measures defined in the Flash Descriptor will be in effect (default)
 H=>Flash Descriptor Security will be overridden

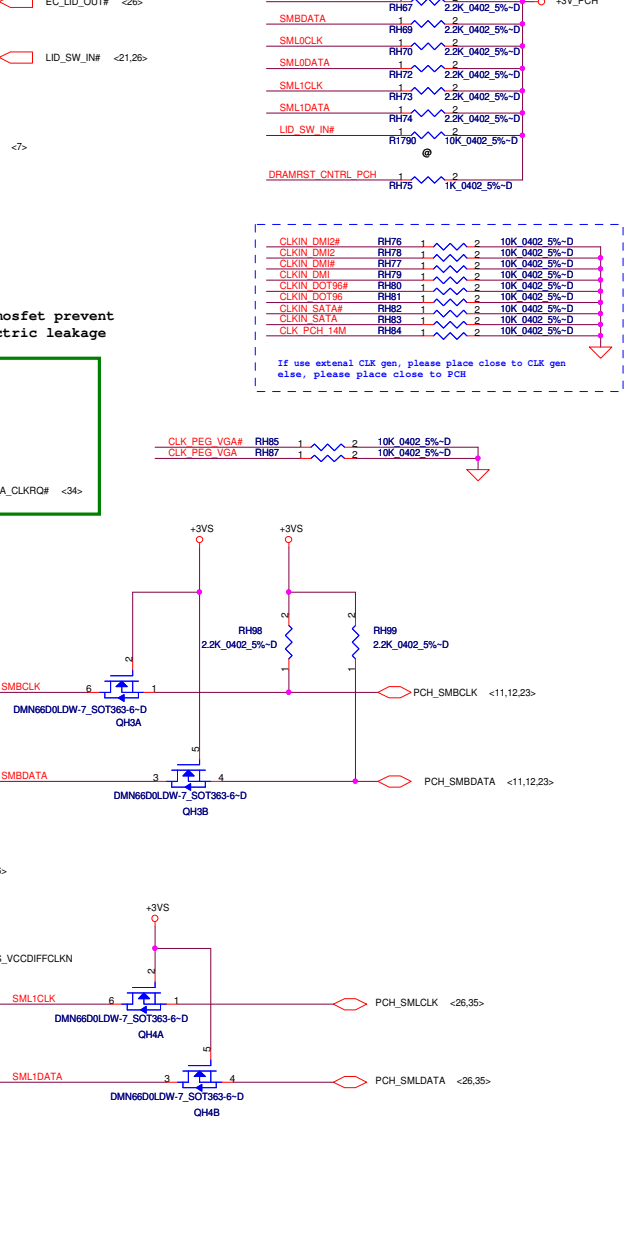
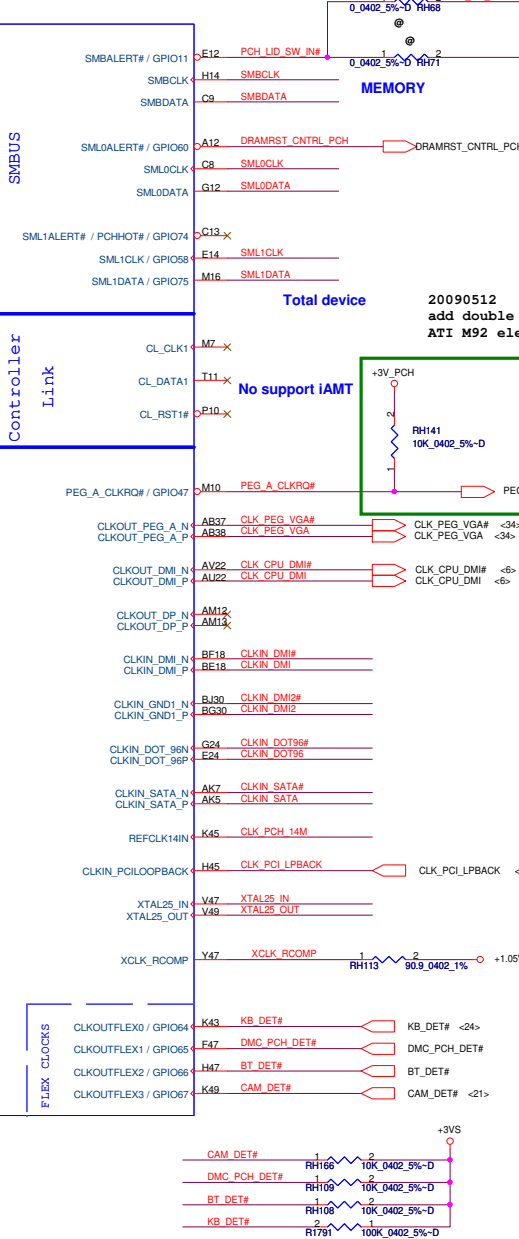
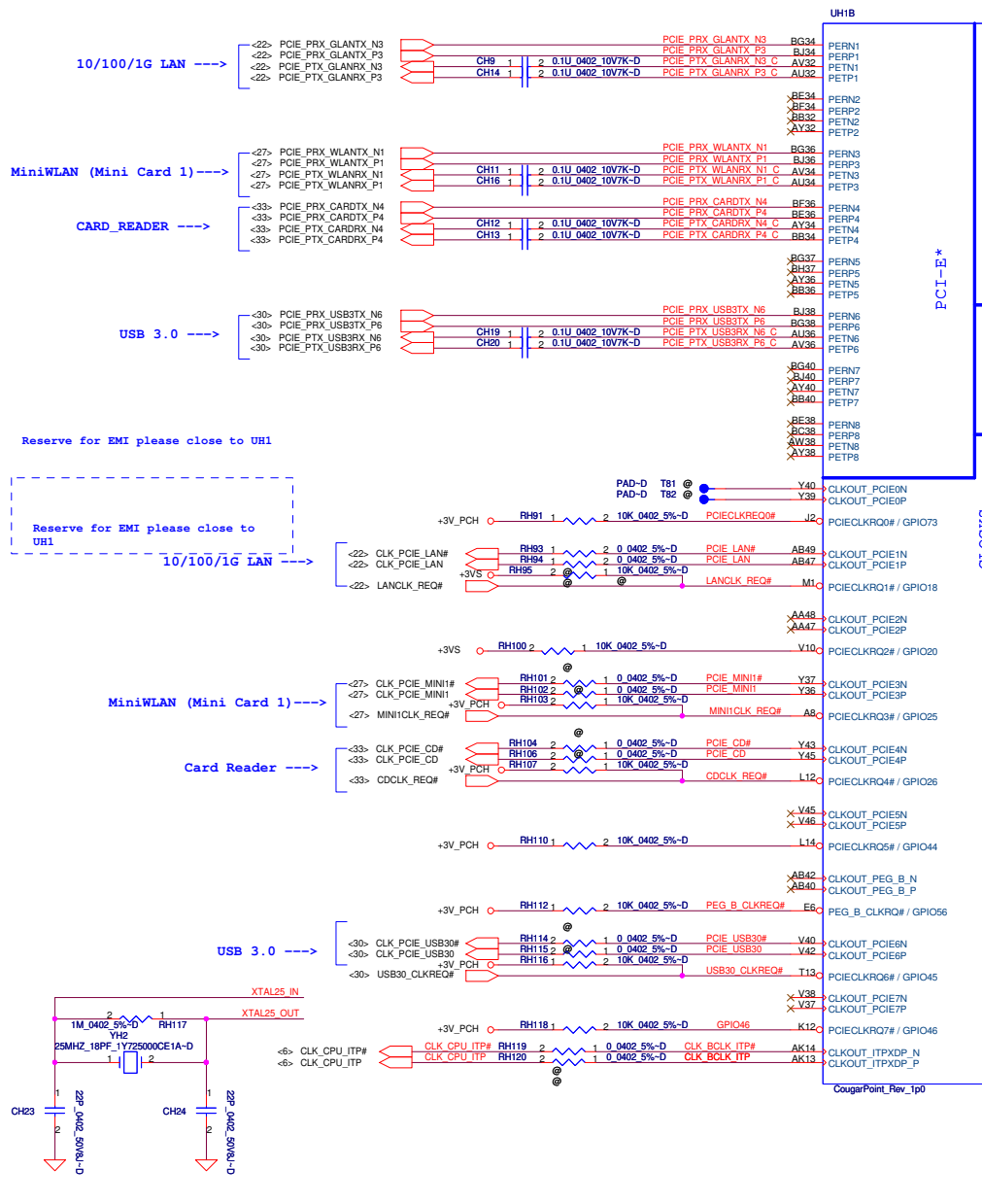


LOW=Default
 *HIGH=No Reboot

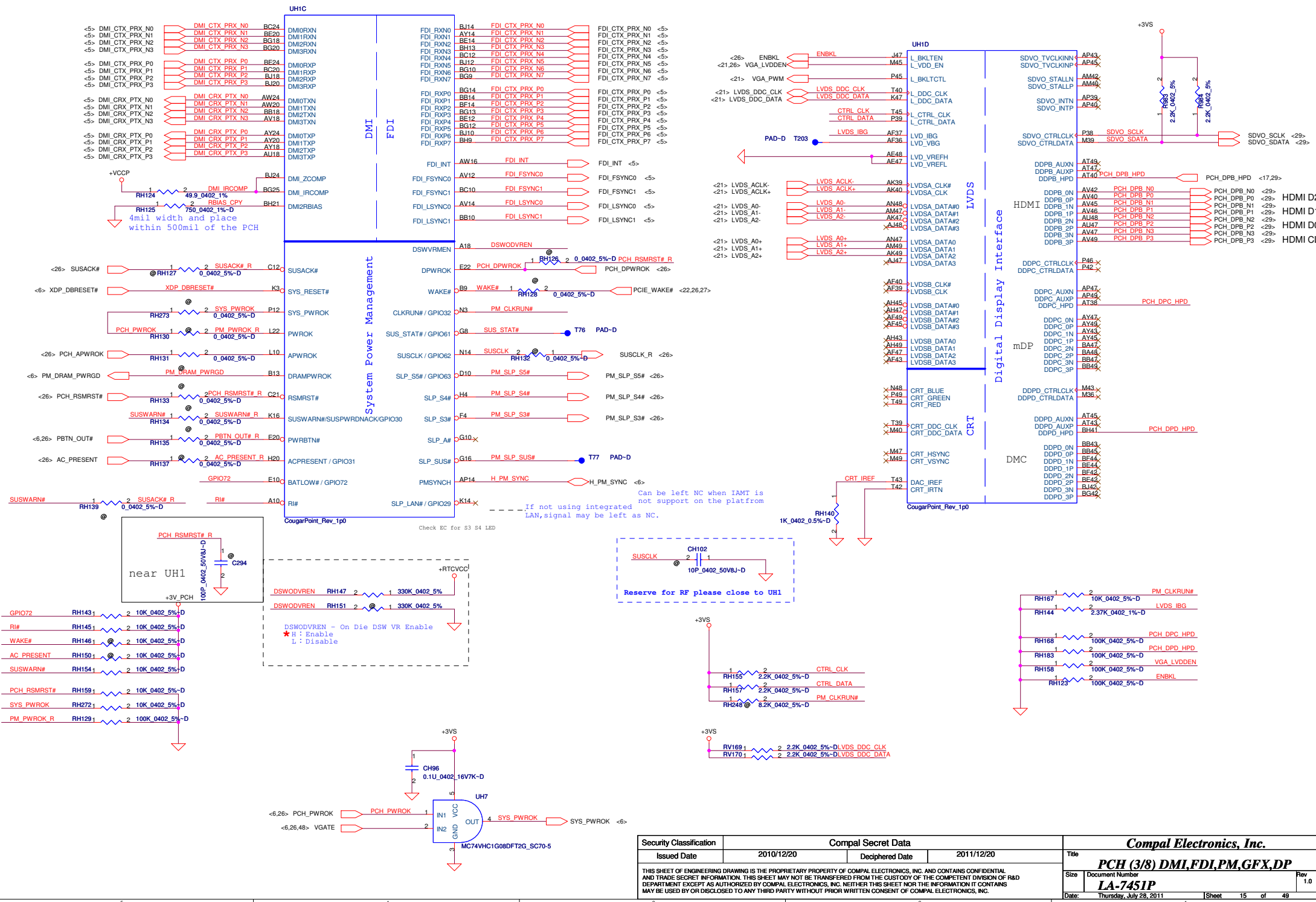


This signal has a weak internal pull-down
 On Die PLL VR is supplied by 1.8V when sampled low
 Needs to be pulled High for Huron River platform

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				LA-7451P	Rev 1.0
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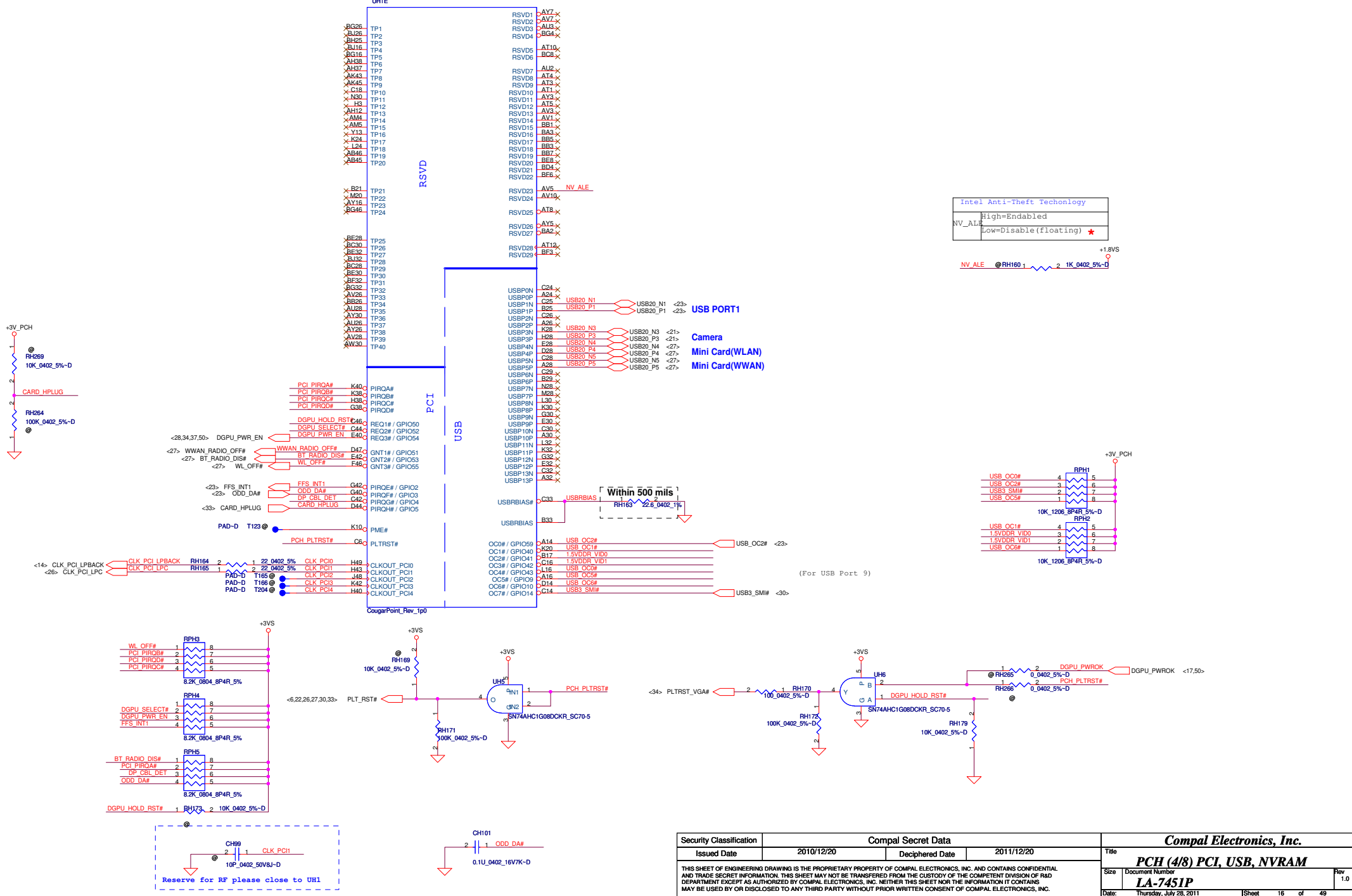


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Size	Document Number	Date		Rev	
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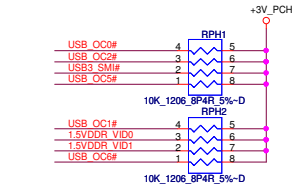
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Issued Date	2010/12/20	Deciphered Date	2011/12/20
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Compal Electronics, Inc.			
Title: PCH (3/8) DMI, FDI, PM, GFX, DP			
Size	Document Number	Rev	
	LA-7451P	1.0	
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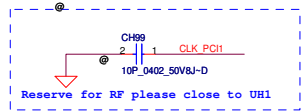


Intel Anti-Theft Technology	
NV_ALE	High=Enabled
	Low=Disable (floating) *

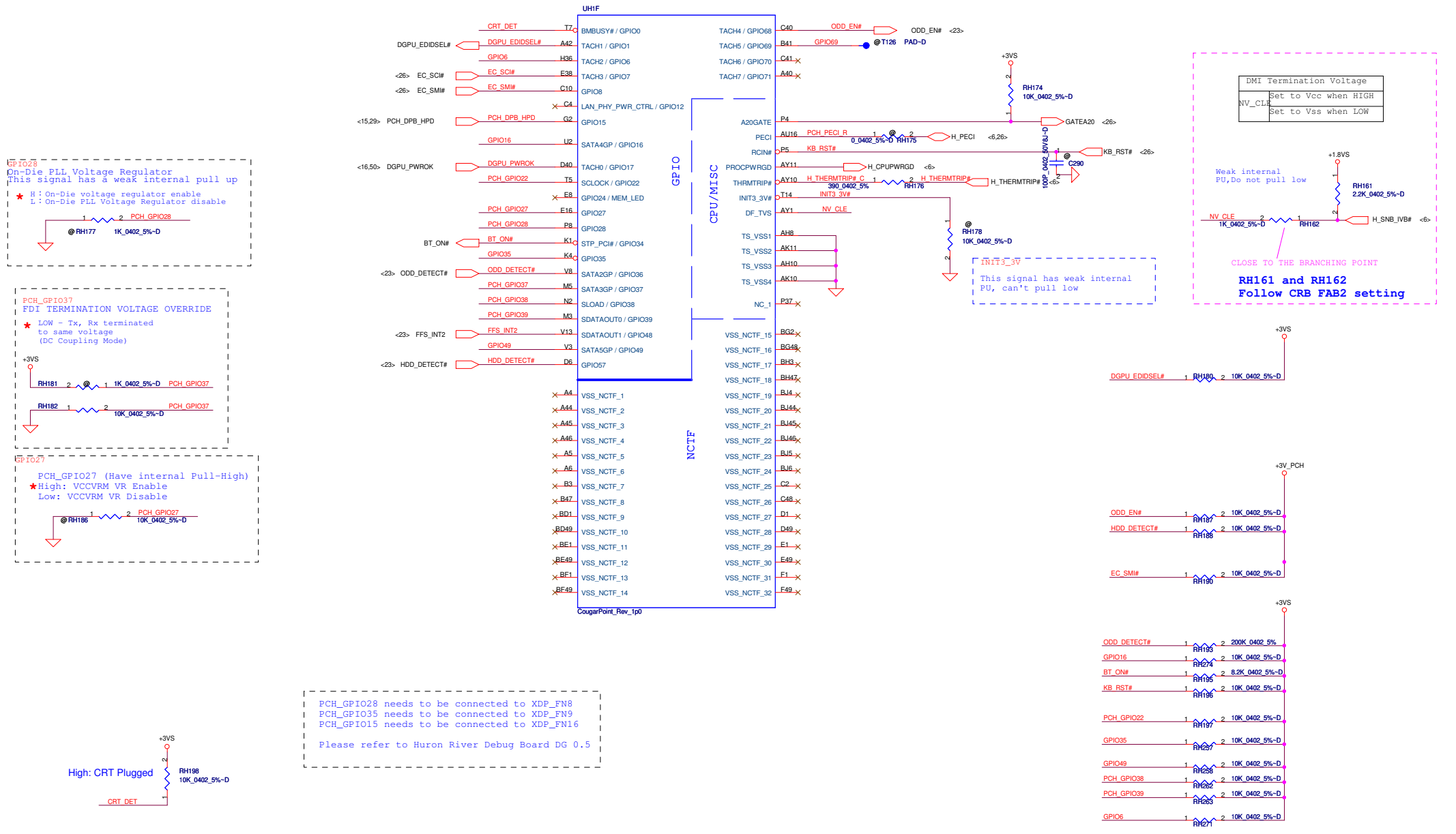
`NV_ALE @ RH160 1 100K 0.402 5%-D`



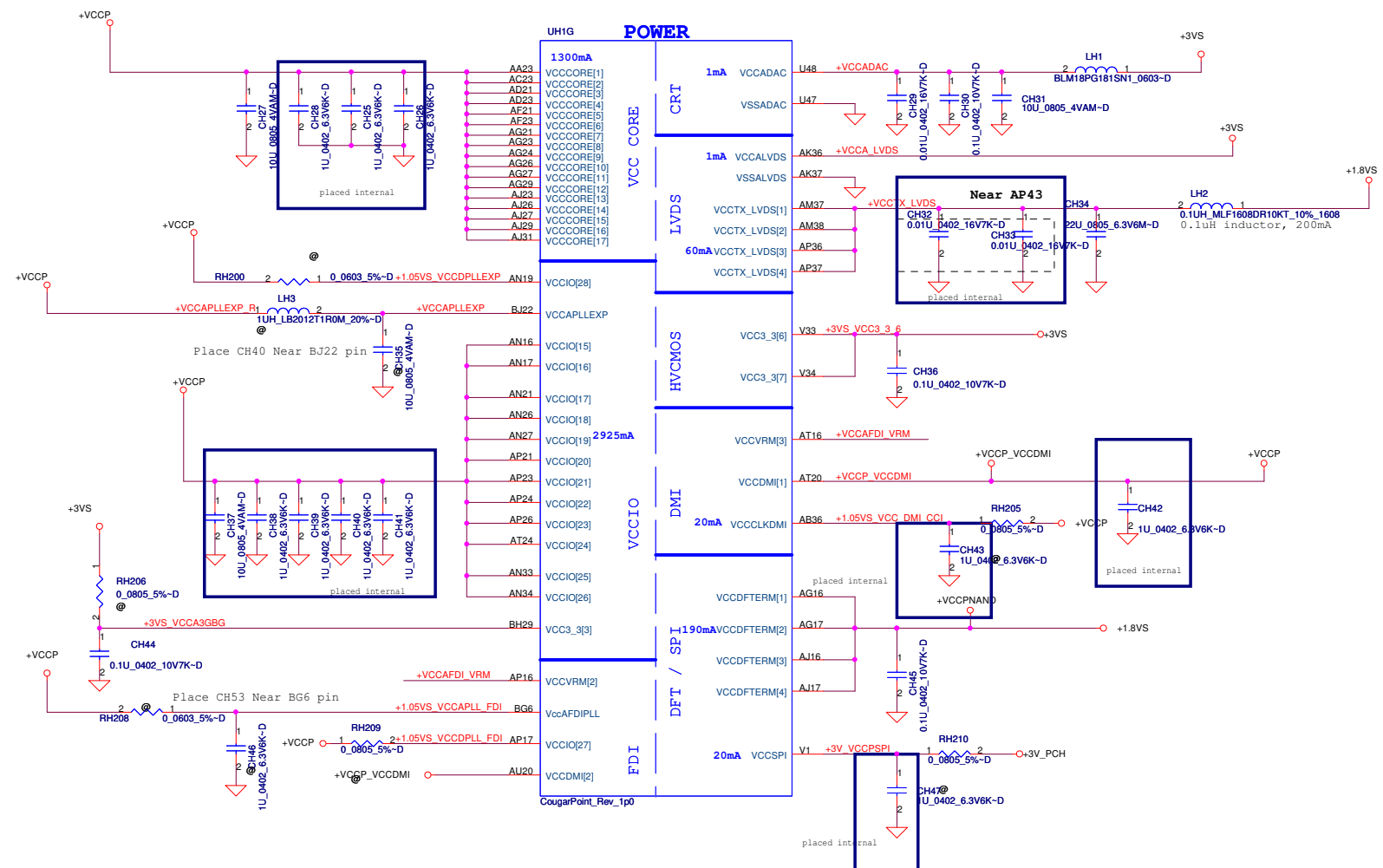
(For USB Port 9)



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				LA-7451P		1.0	
Date: Thursday, July 28, 2011				Sheet		16 of 49	

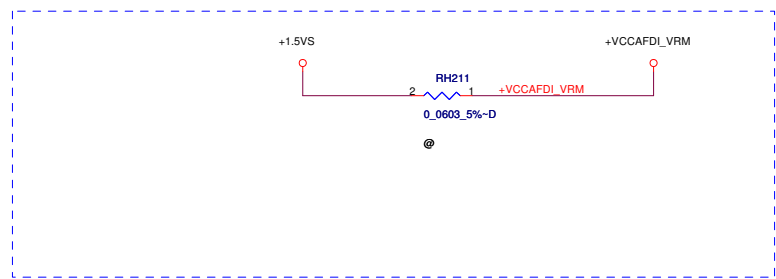


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Issued Date	2010/12/20	Deciphered Date	2011/12/20	PCH (5/8) GPIO, CPU, MISC
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Date			Sheet	of
			17	49

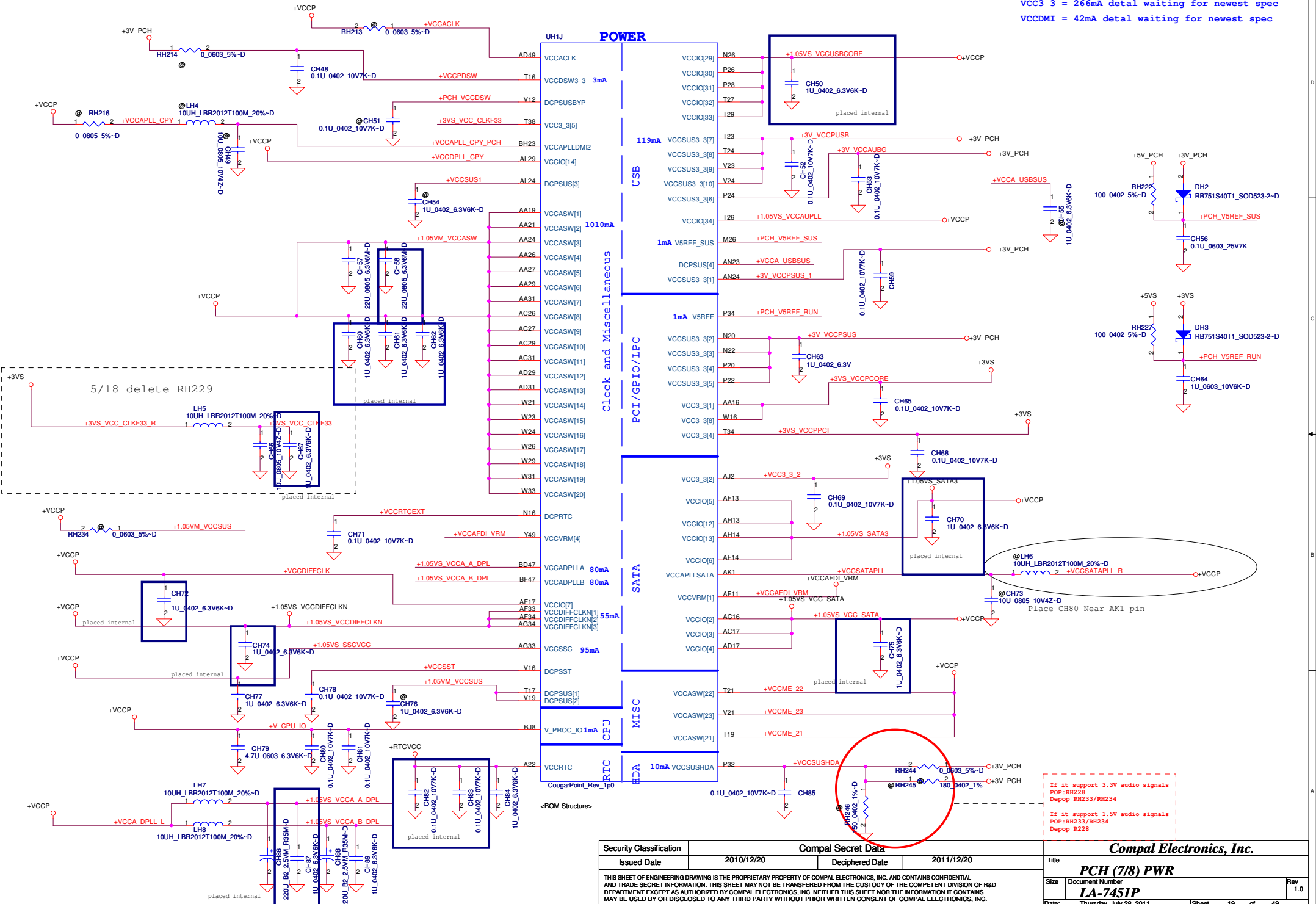


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec



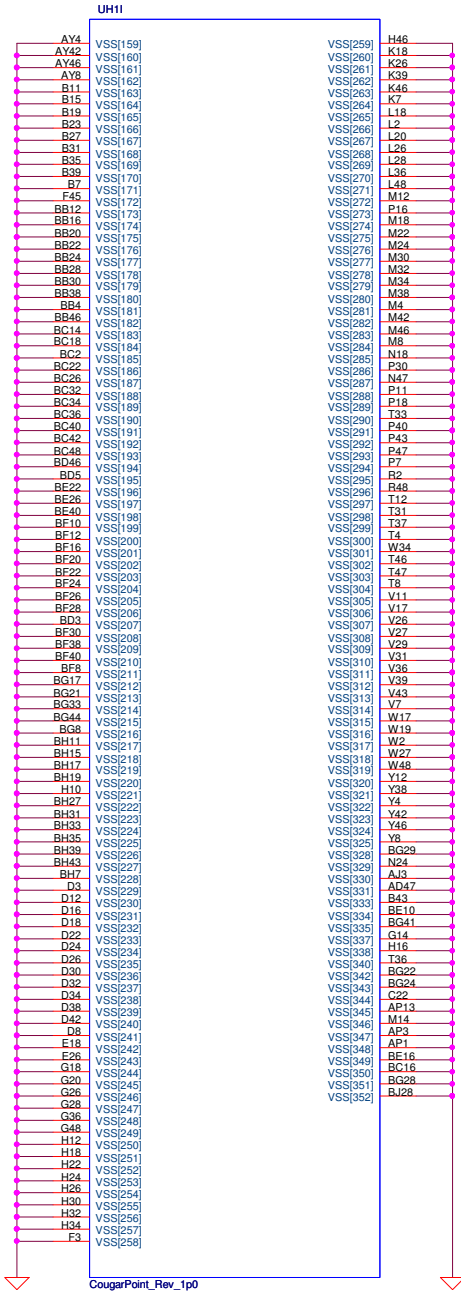
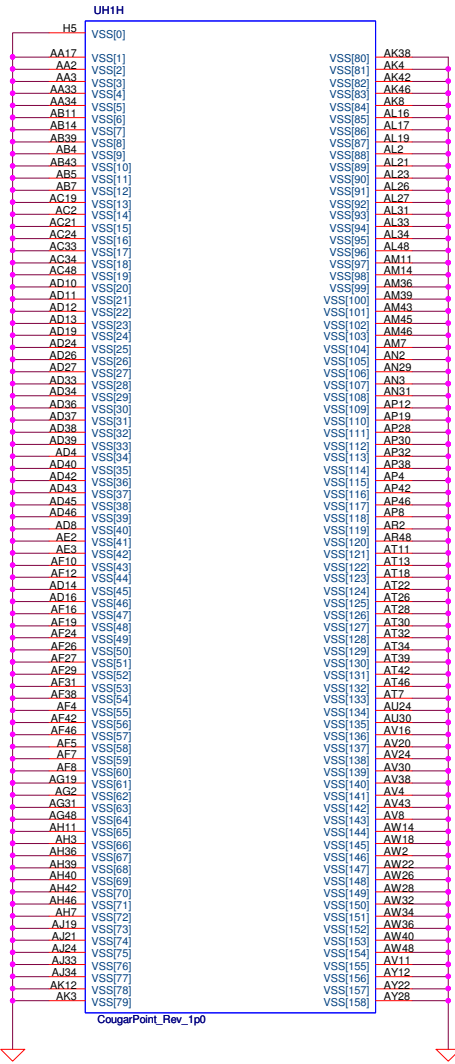
VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec



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PCH (7/8) PWR		
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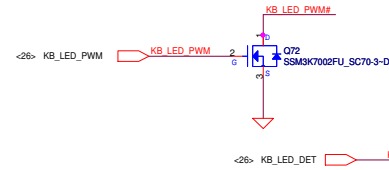
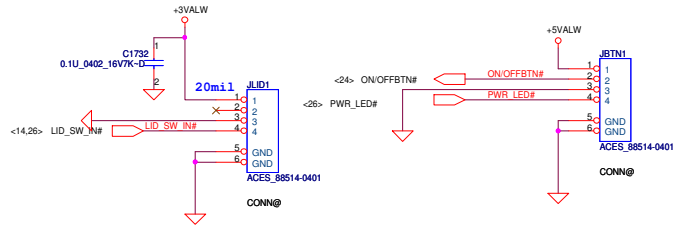


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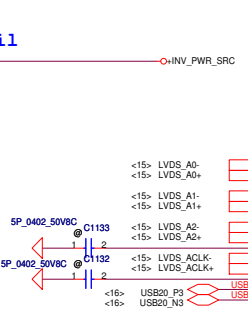
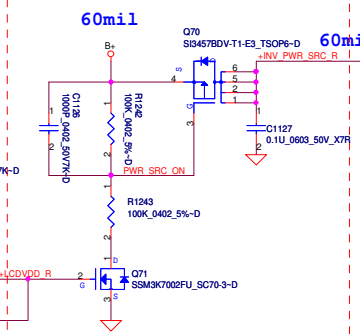
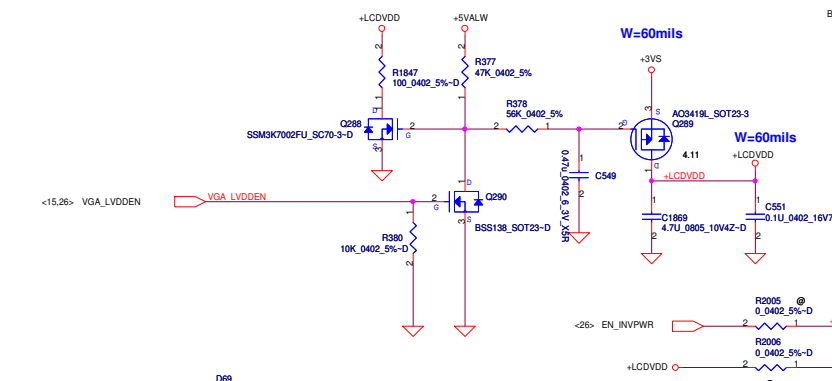
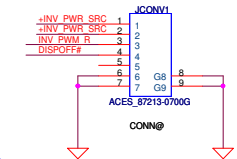
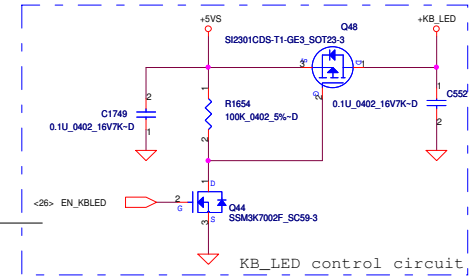
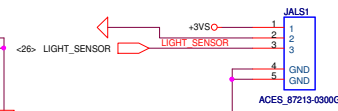
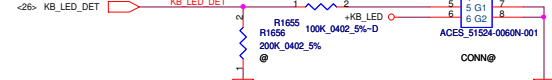
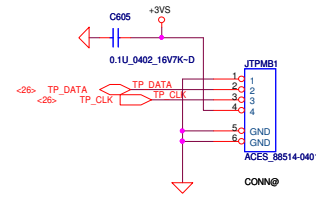
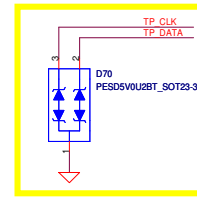
LOGO Board CONN

PWR BTN Board CONN

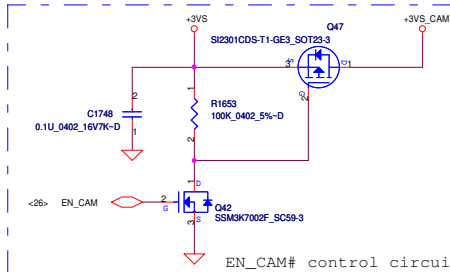
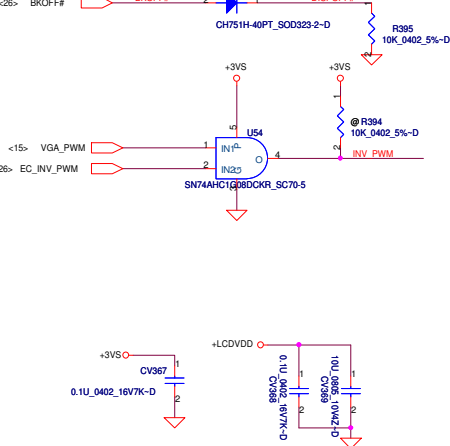
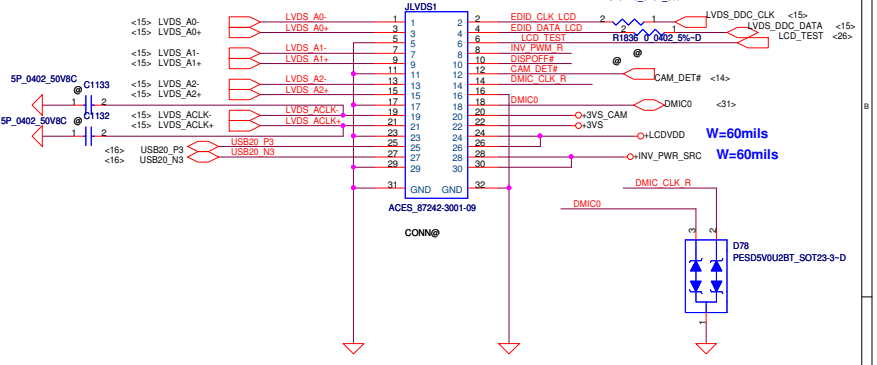
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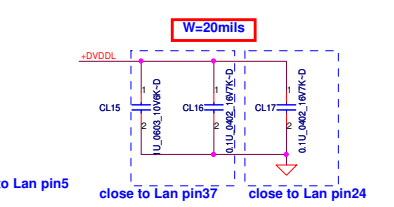
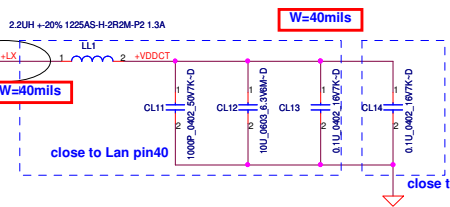
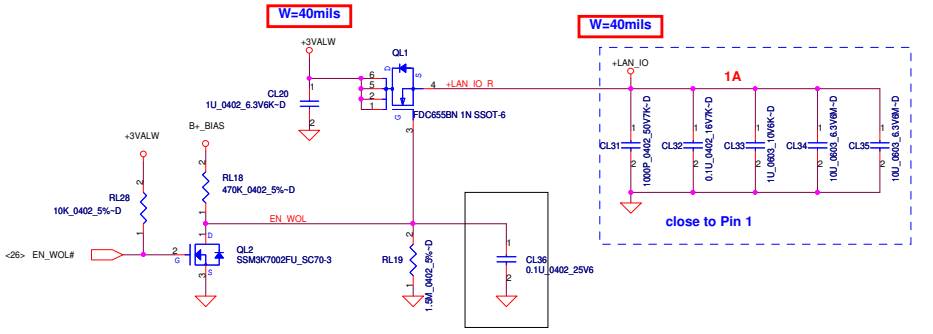
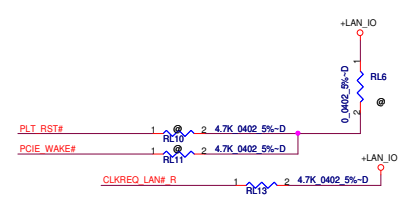
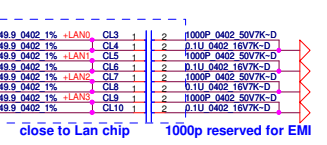
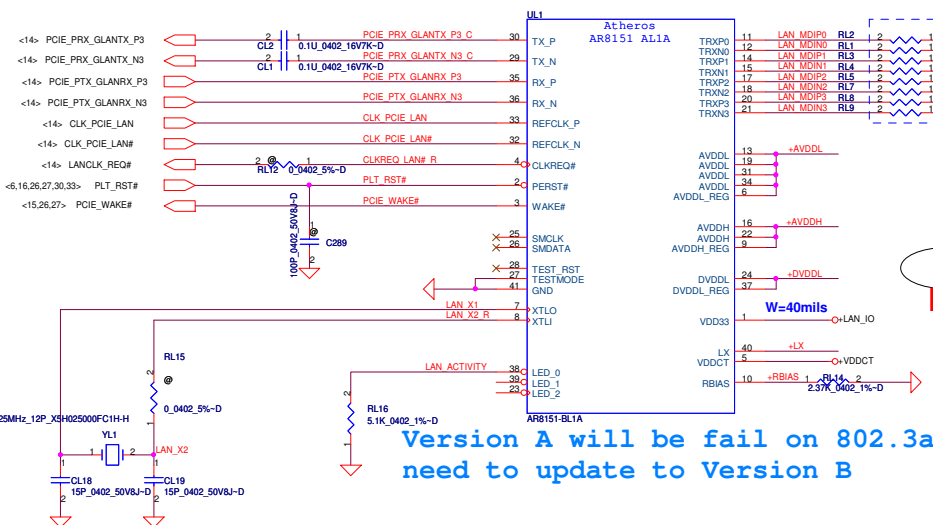
close to JTFMB 7/26



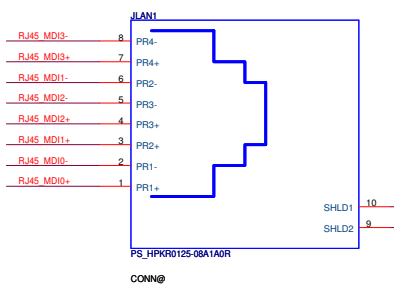
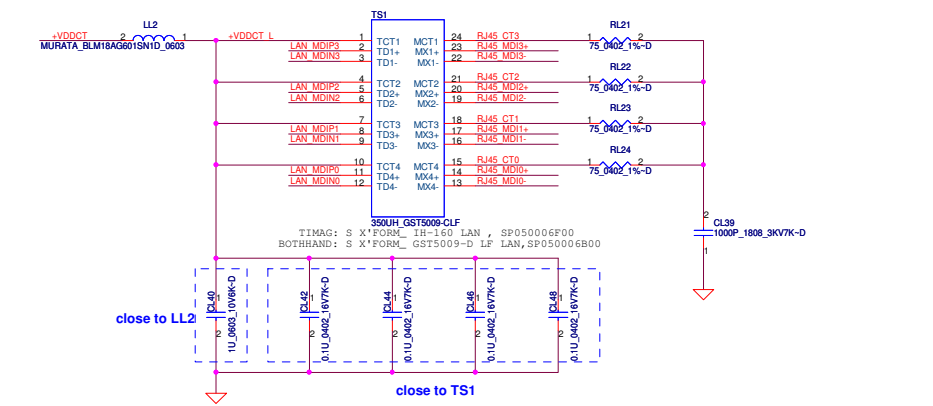
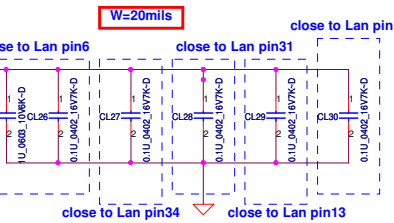
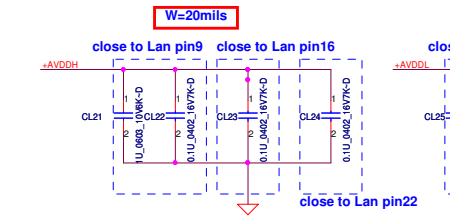
LVDS Conn.



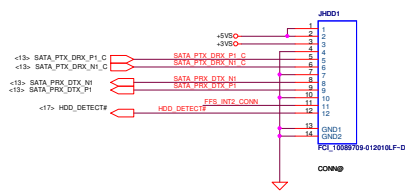
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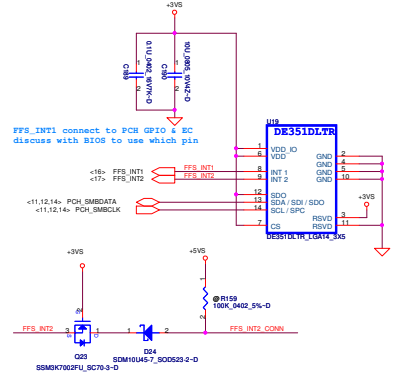
Version A will be fail on 802.3a
need to update to Version B



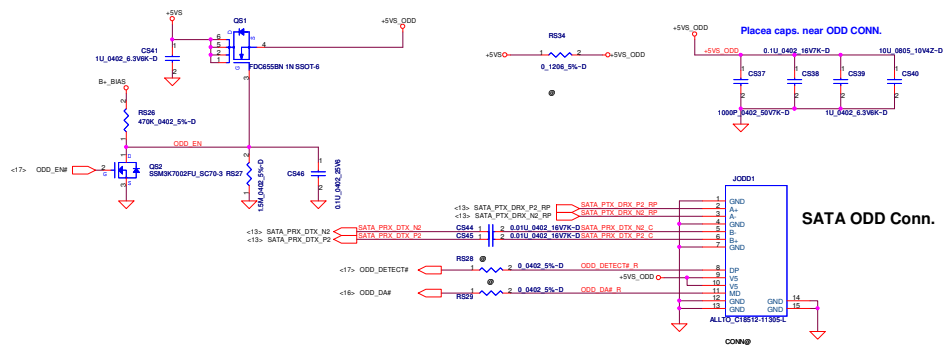
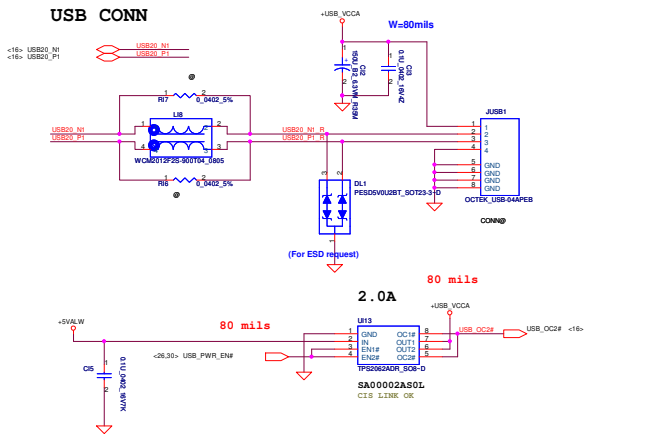
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Free Fall Sensor



USB CONN

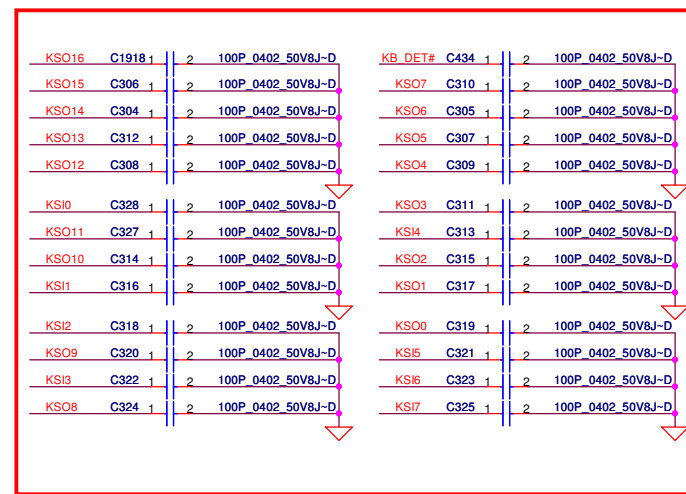
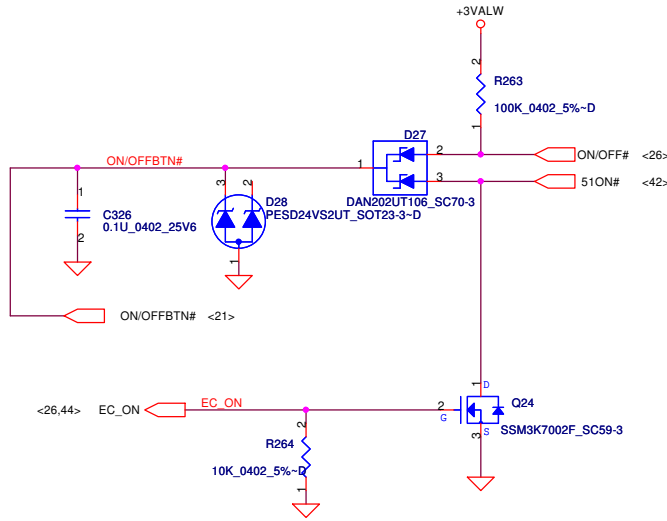


SATA ODD Conn.

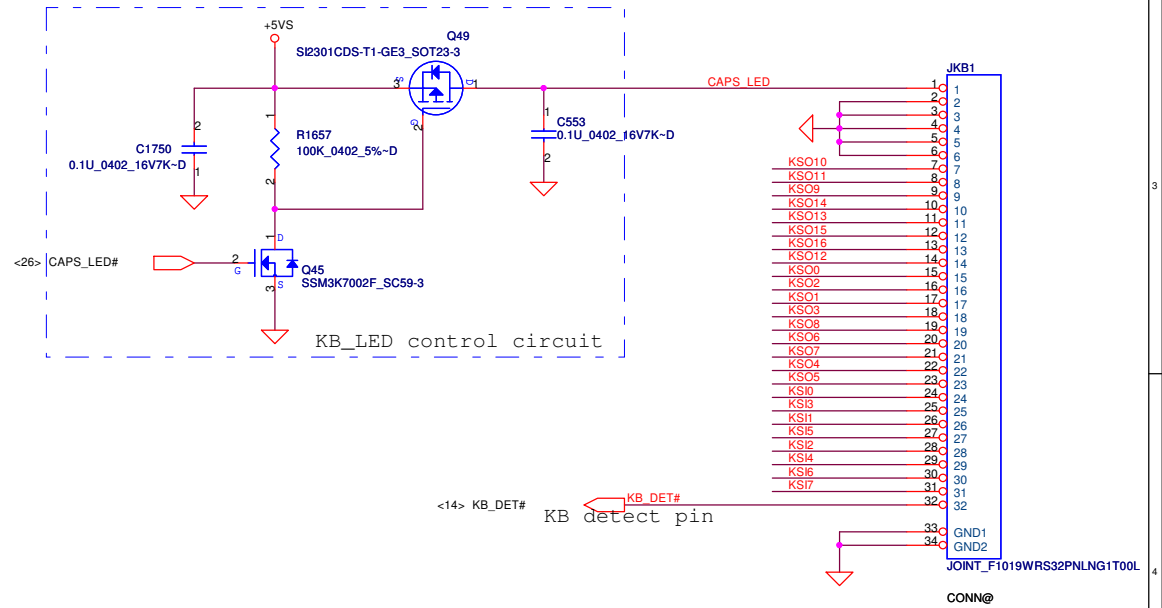
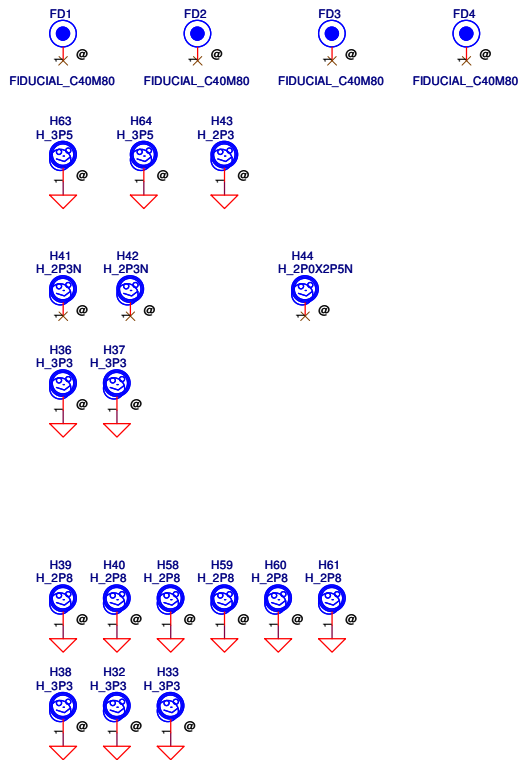
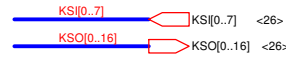
ON/OFF switch

Power Button

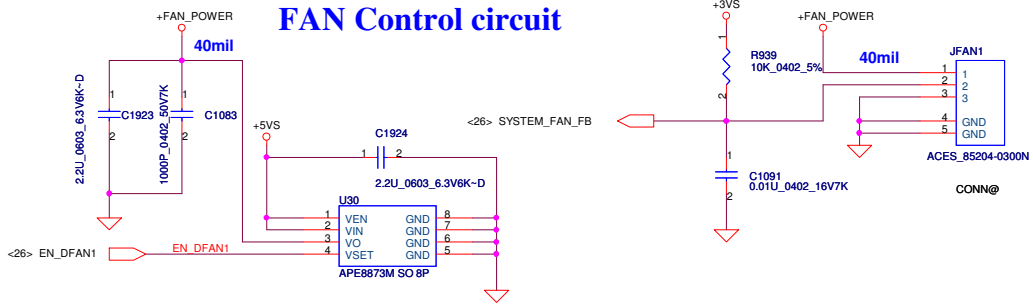
TOP Side
Bottom Side
Test Only



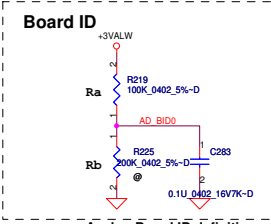
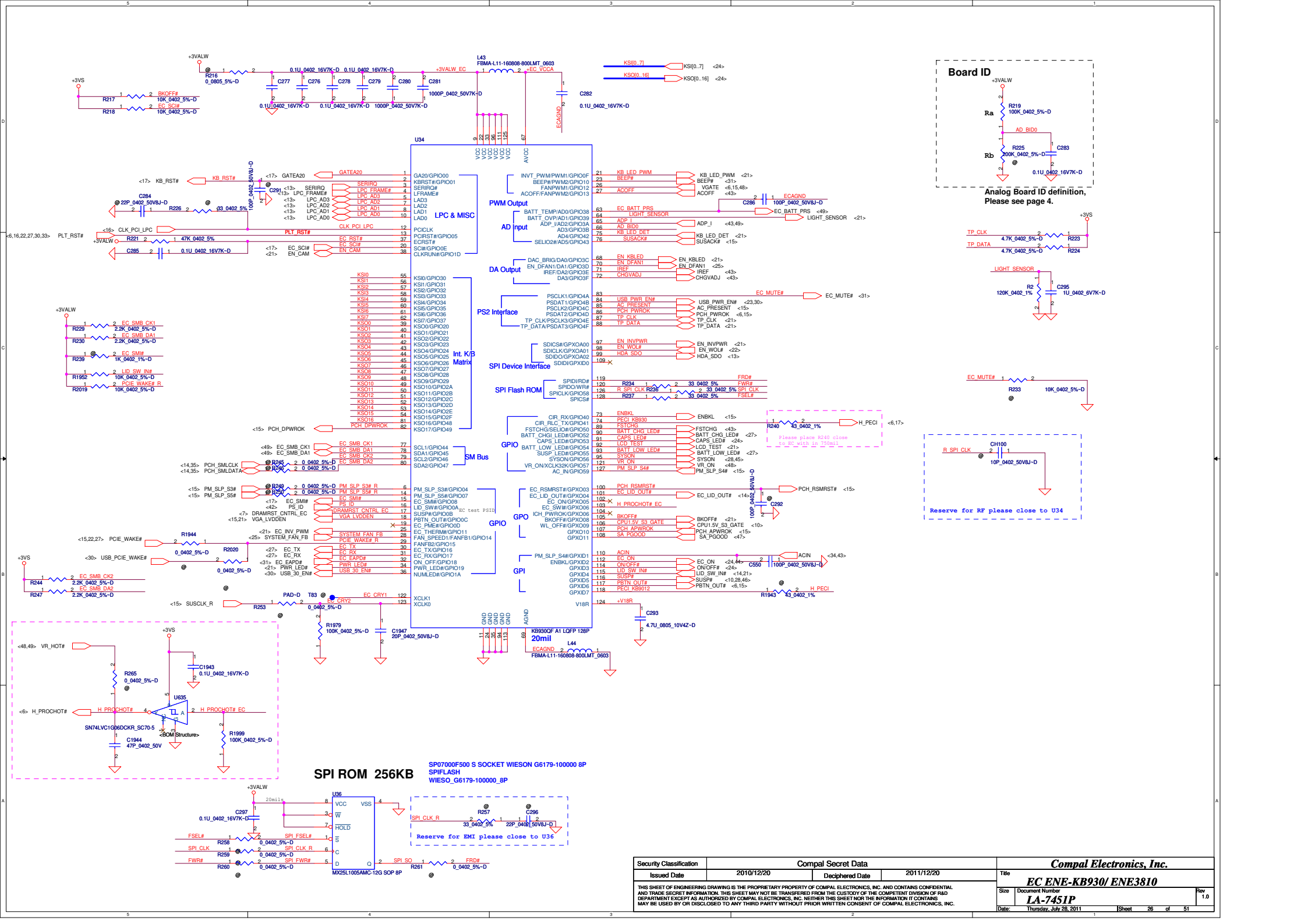
INT_KBD Conn.



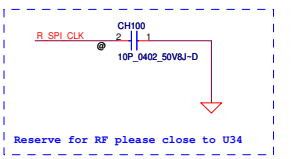
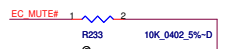
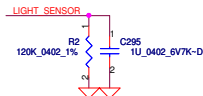
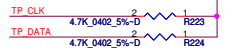
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				Date	Thursday, July 28, 2011
				Sheet	25 of 51

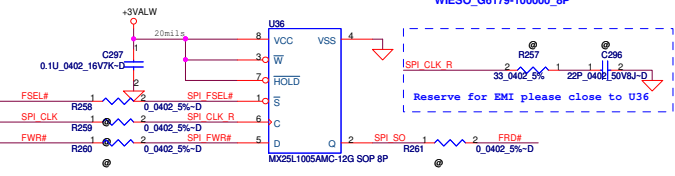


Analog Board ID definition, Please see page 4.

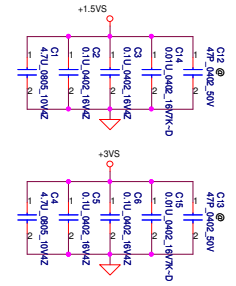
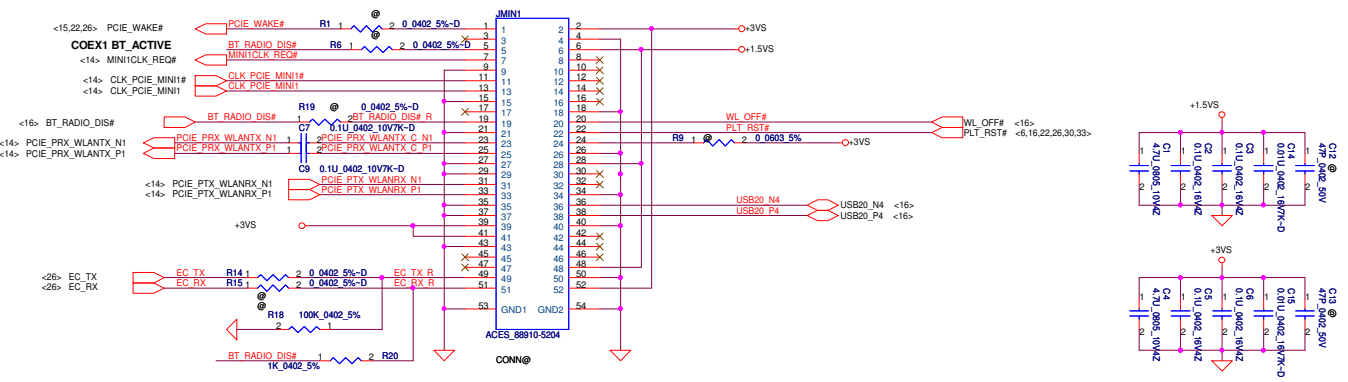


SPI ROM 256KB

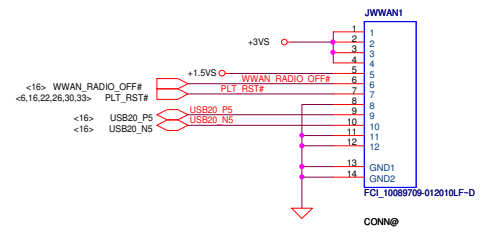
SP07000F50 S SOCKET WIESON G6179-10000 8P
SPIFLASH
WIESO_G6179-10000_8P



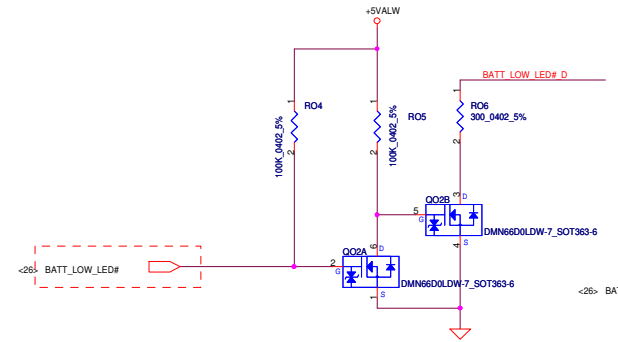
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title
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				EC ENE-KB930/ ENE3810
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				1.0
				Date
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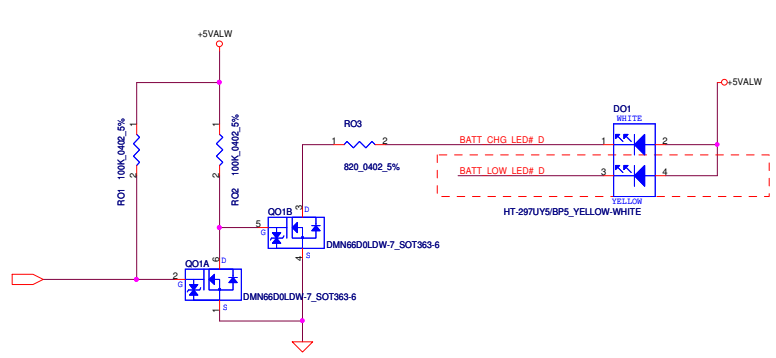
TO WWAN BOARD



BATT LOW

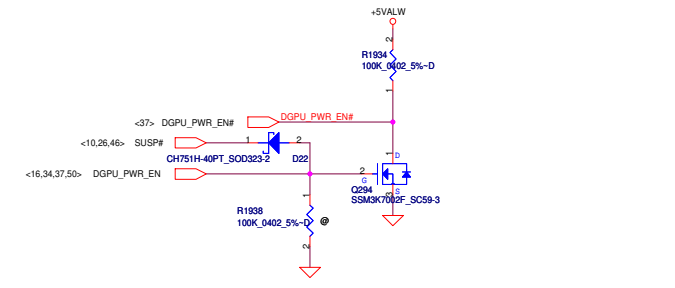
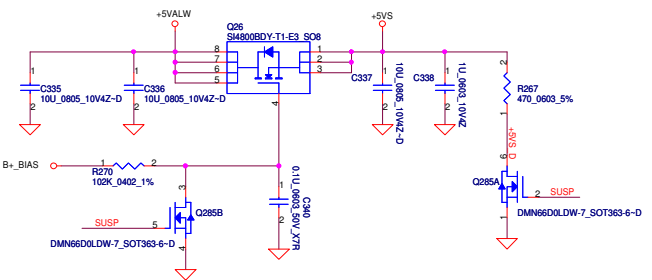


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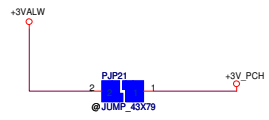
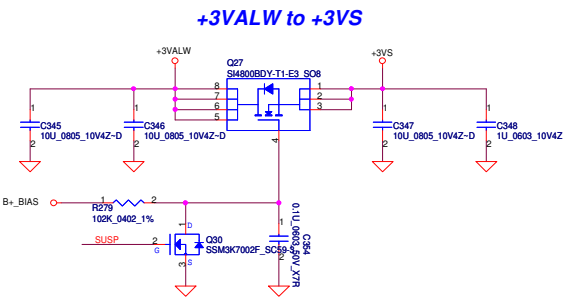


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Size	Document Number	Rev		
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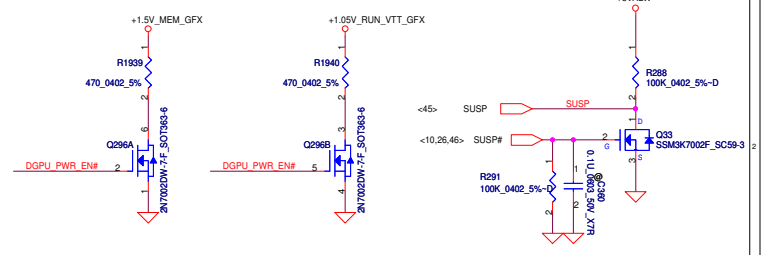
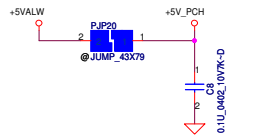
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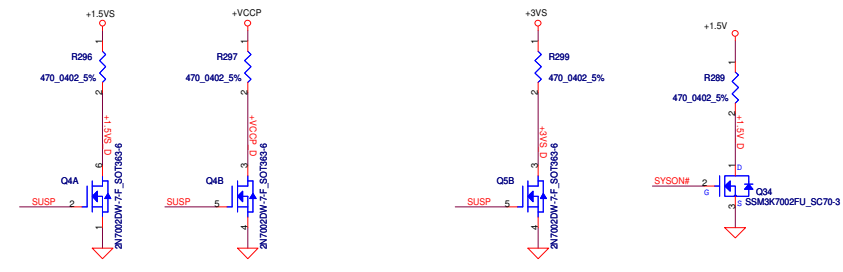
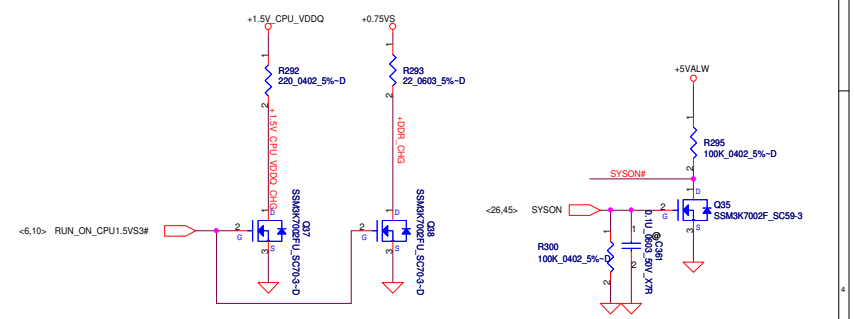
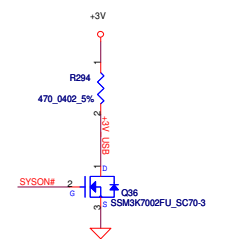
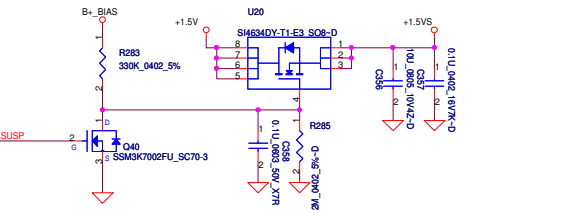
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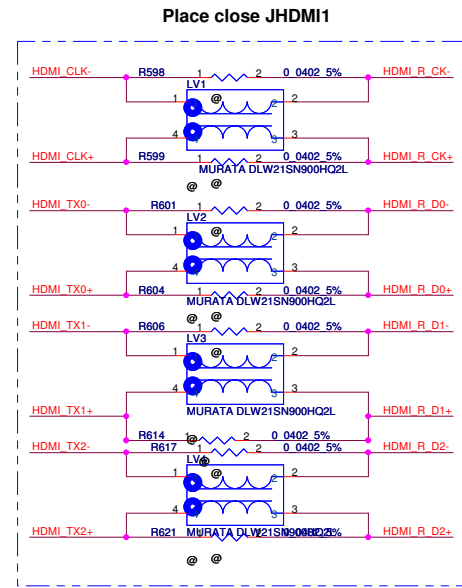
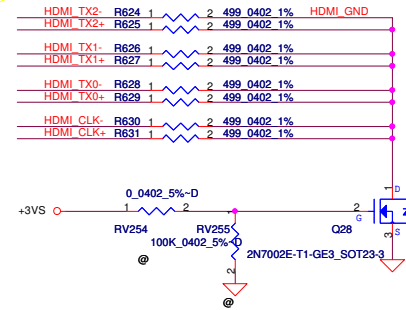
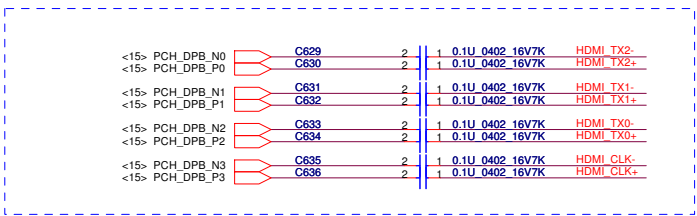
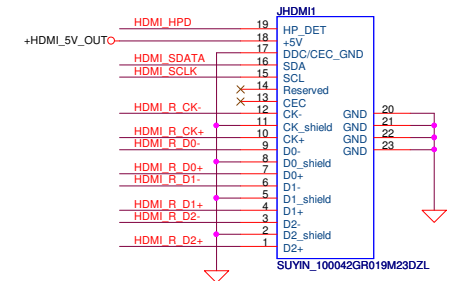
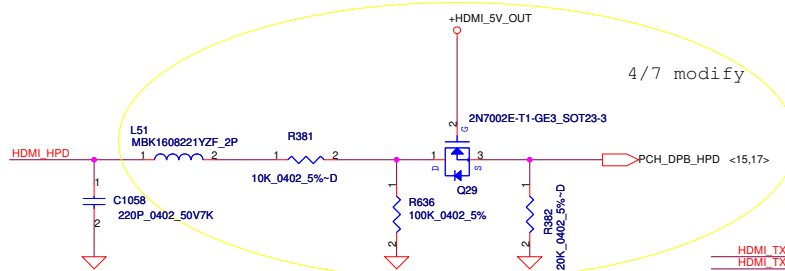
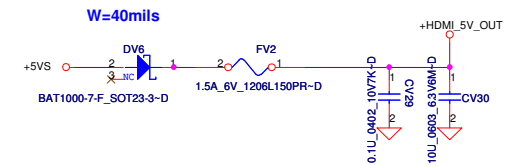
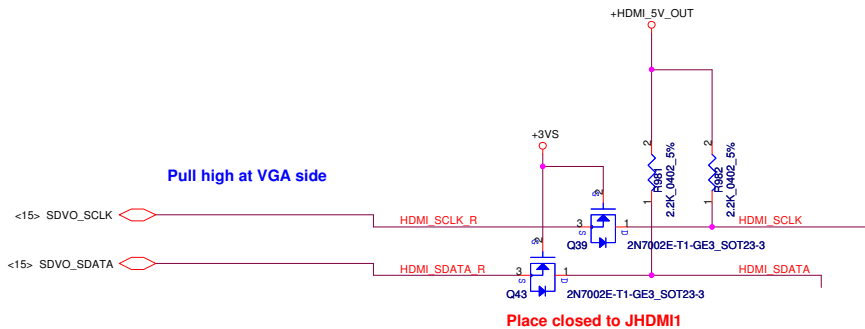
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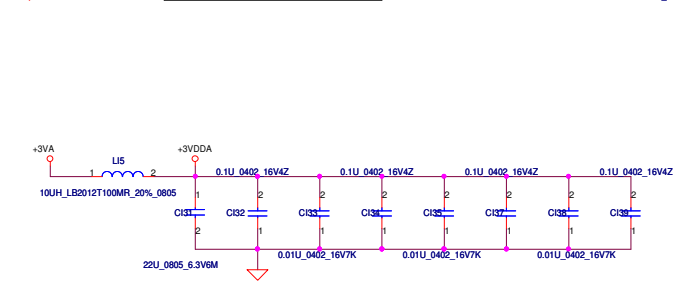
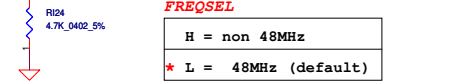
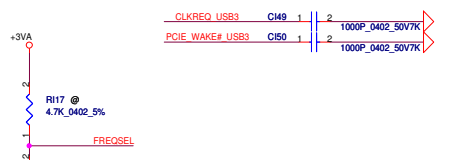
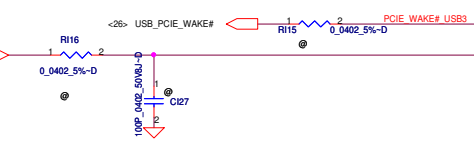
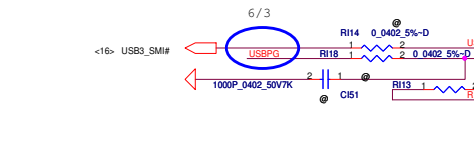
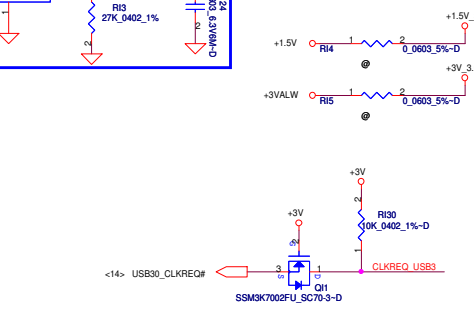
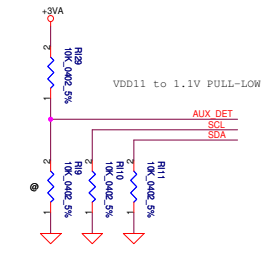
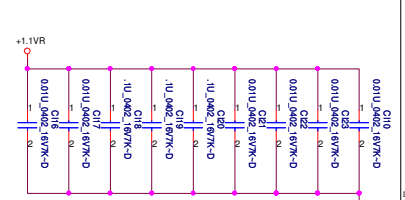
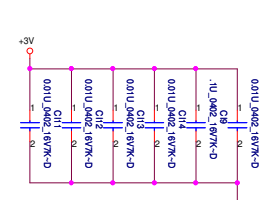
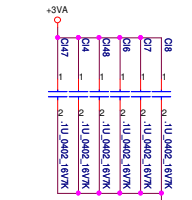
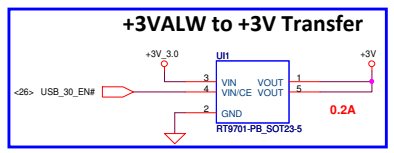
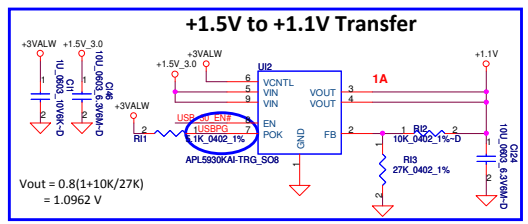
+1.5V To +1.5VS



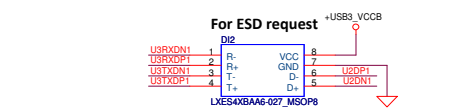
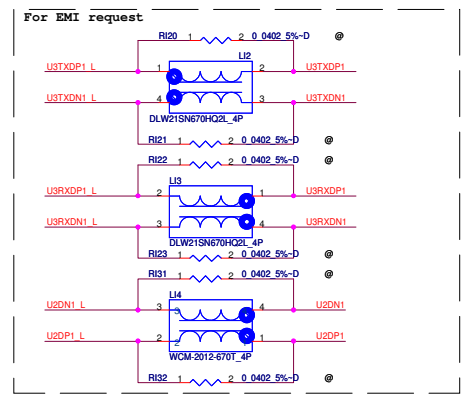
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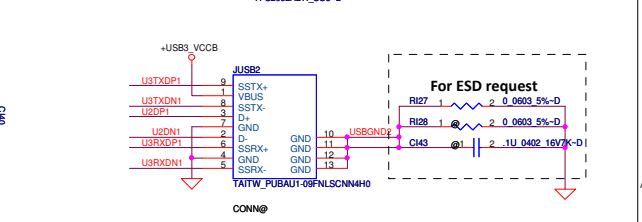
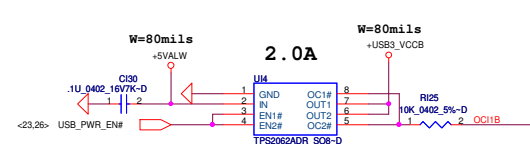
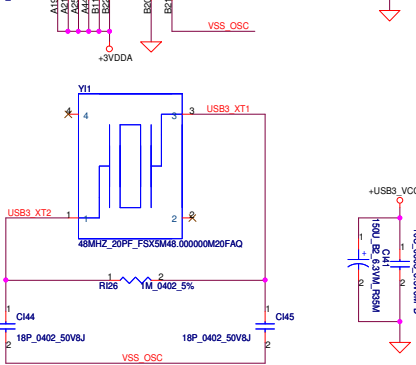
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title
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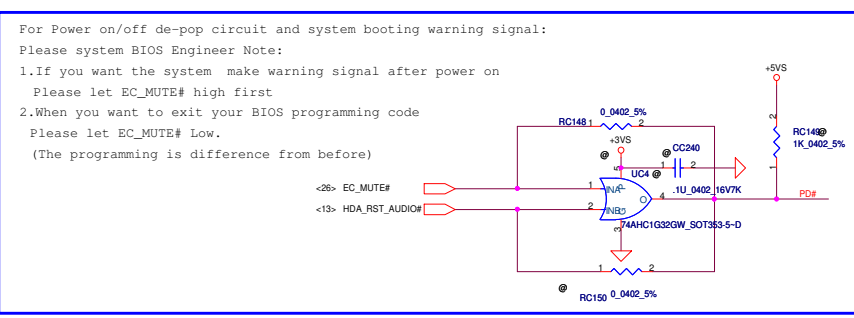
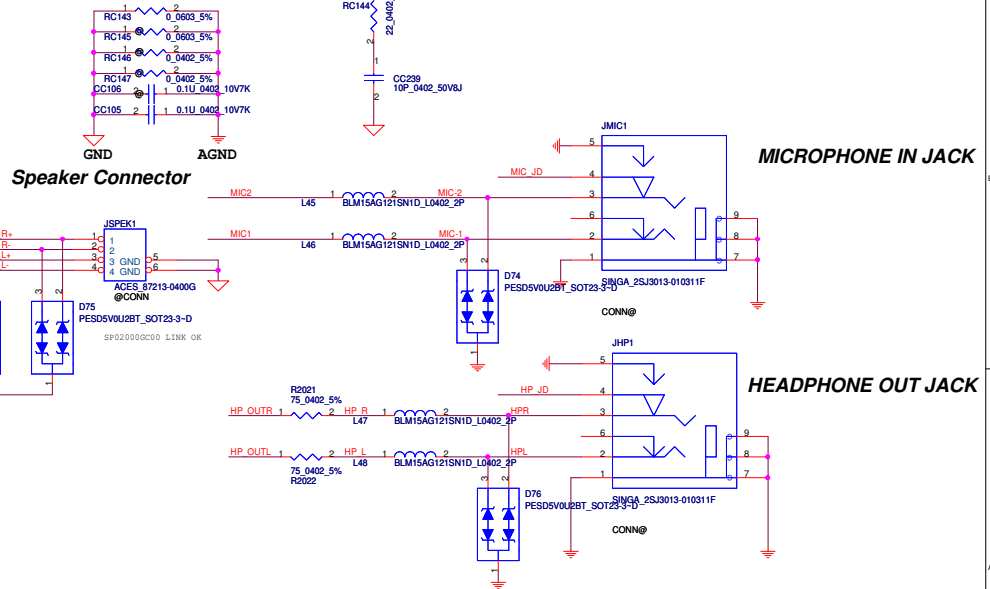
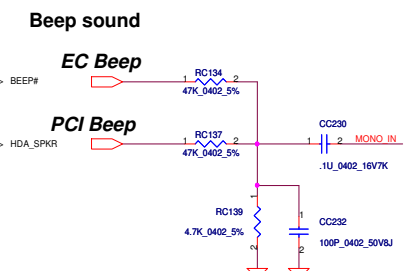
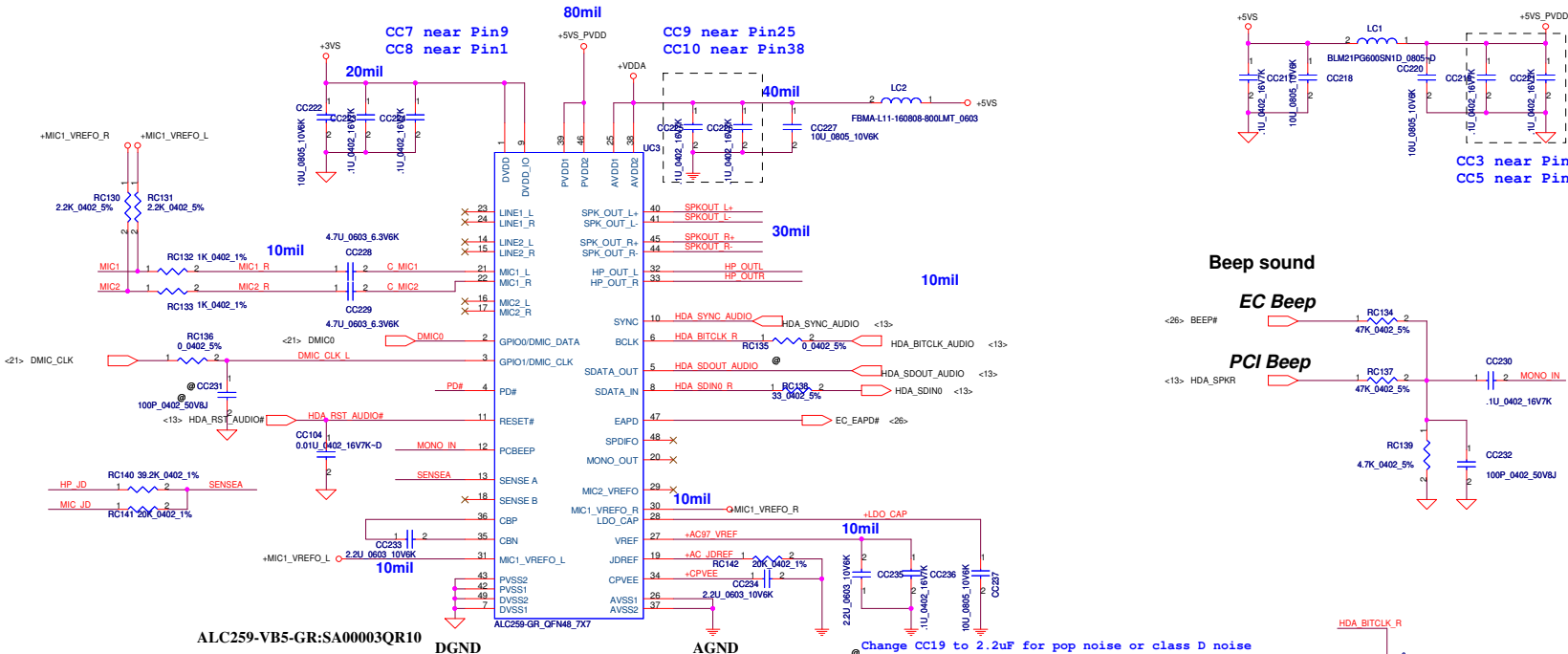


7K for customer request, can use other kind of capacitor, like Y5V.



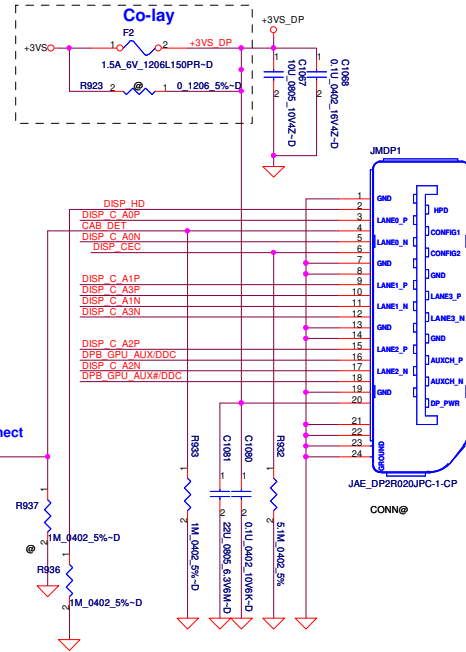
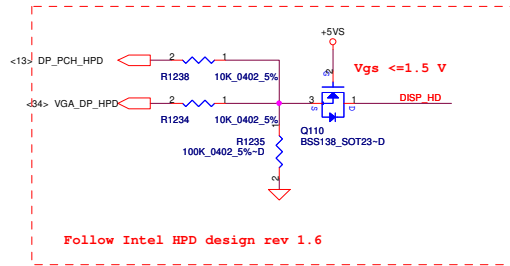
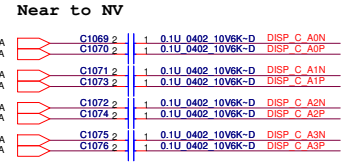
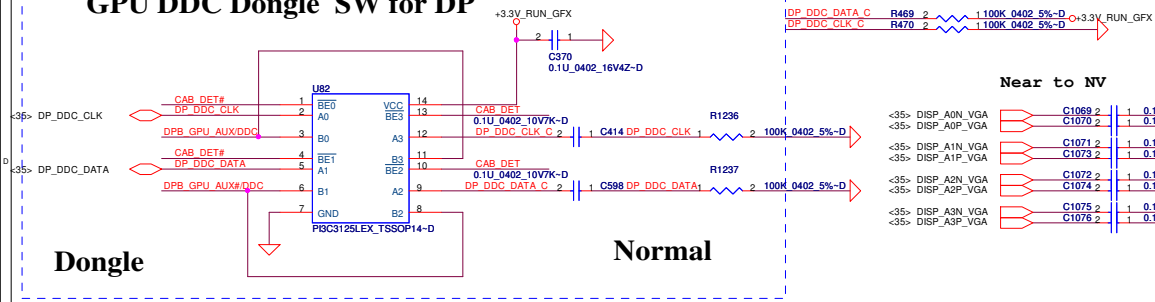
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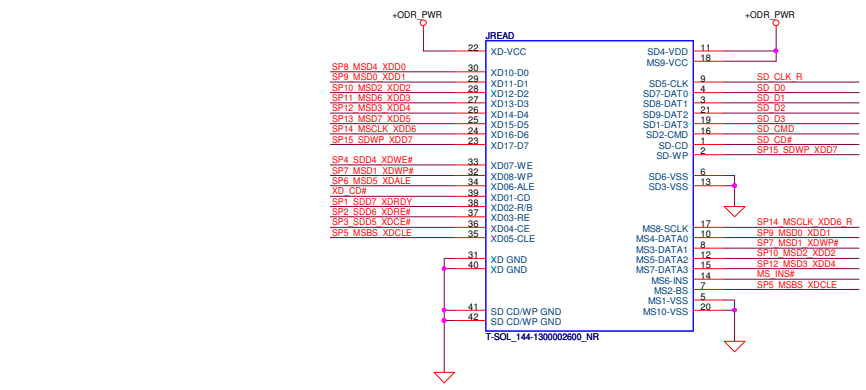
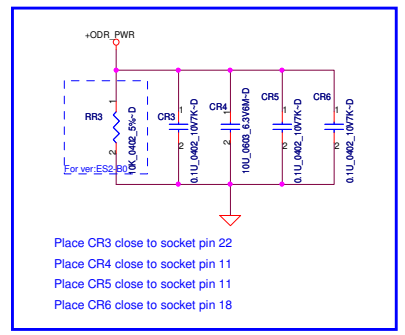
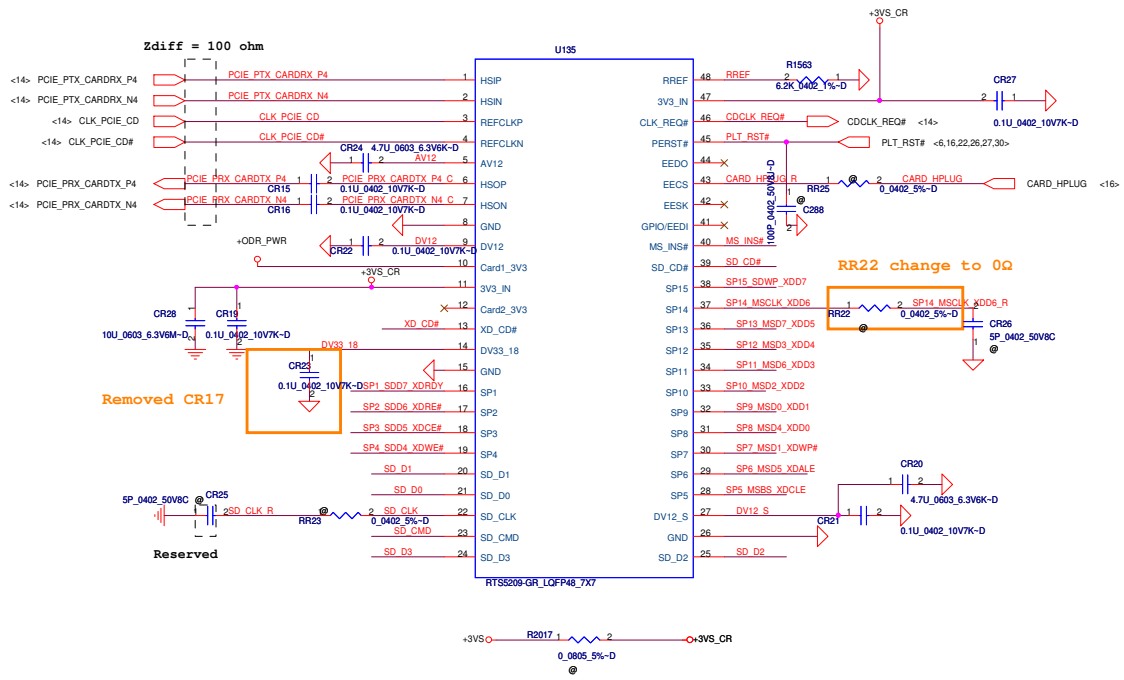
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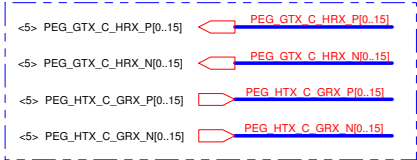
GPU DDC Dongle SW for DP



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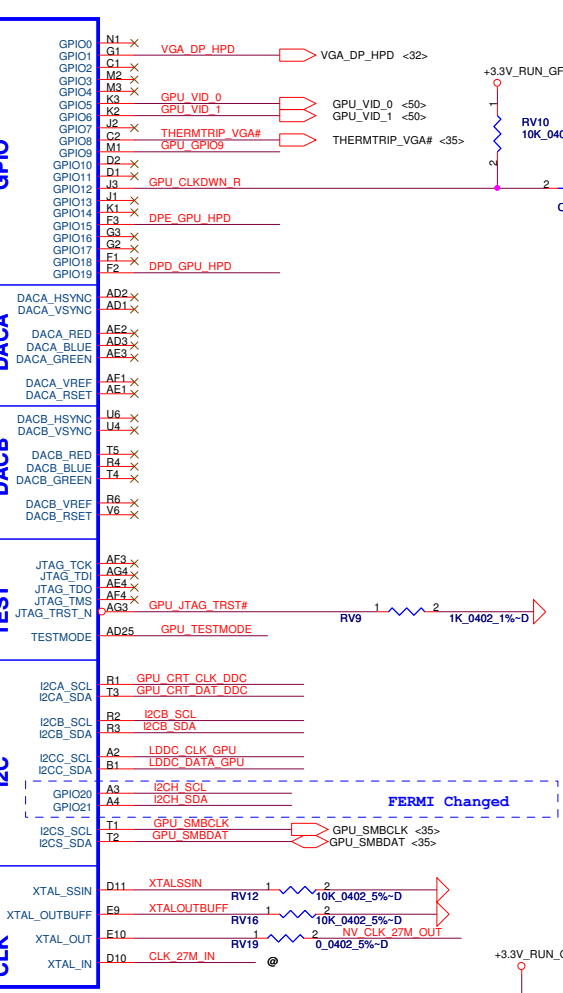
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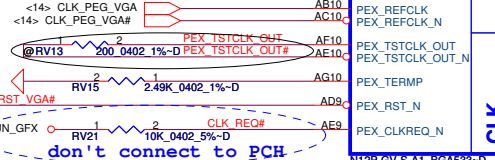


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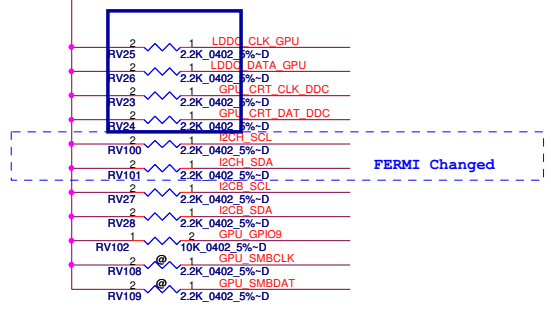
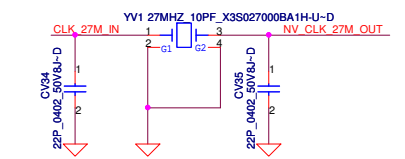
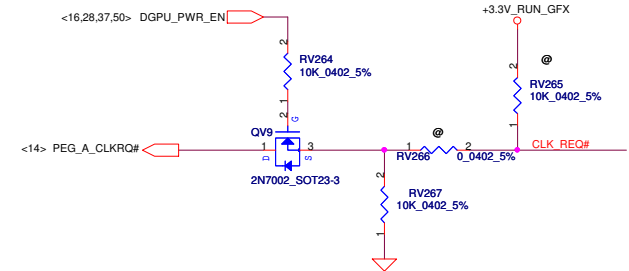
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Differential signal



CHANGE 0325



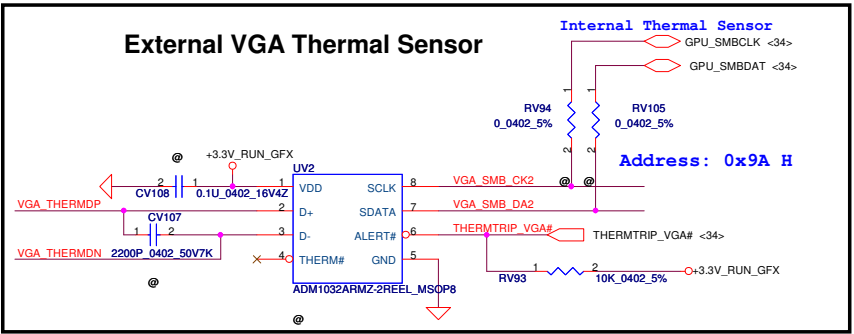
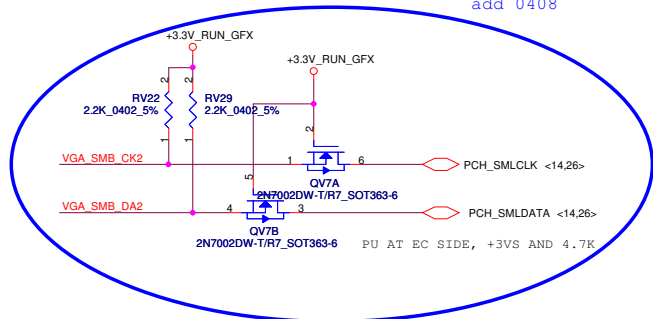
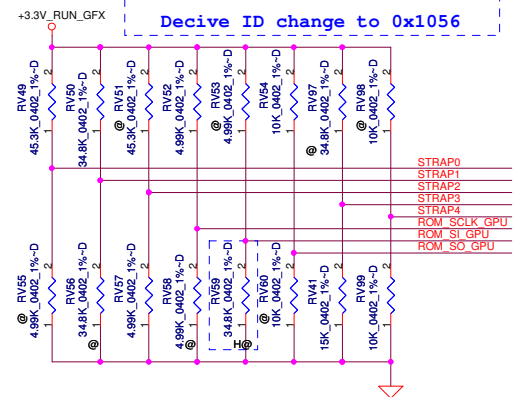
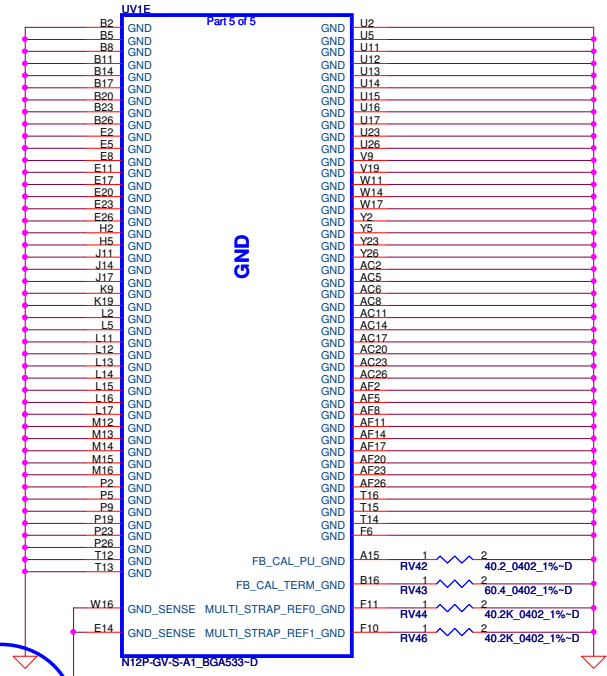
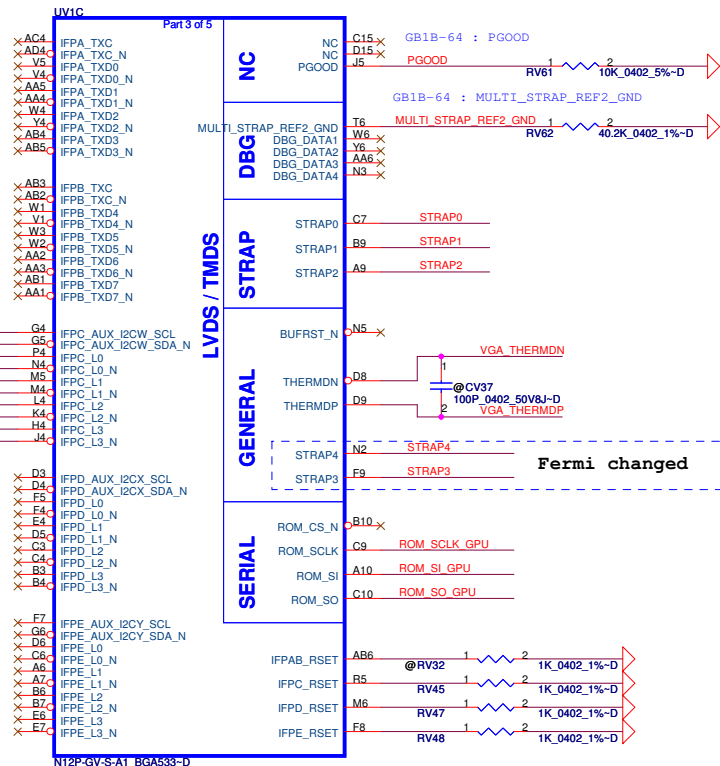
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Compal Electronics, Inc.

N12P PCIe,I2C,DAC,GPIO

LA-7451P

Date: Thursday, July 28, 2011 Sheet 34 of 51



**** Hynix 64Mx16 DDR3 part stuff RV59=15K**
Samsung 64Mx16 DDR3 part stuff RV59=20K
Hynix 128Mx16 DDR3 part stuff RV59=35K
Samsung 128Mx16 DDR3 part stuff RV59=45.3K

Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

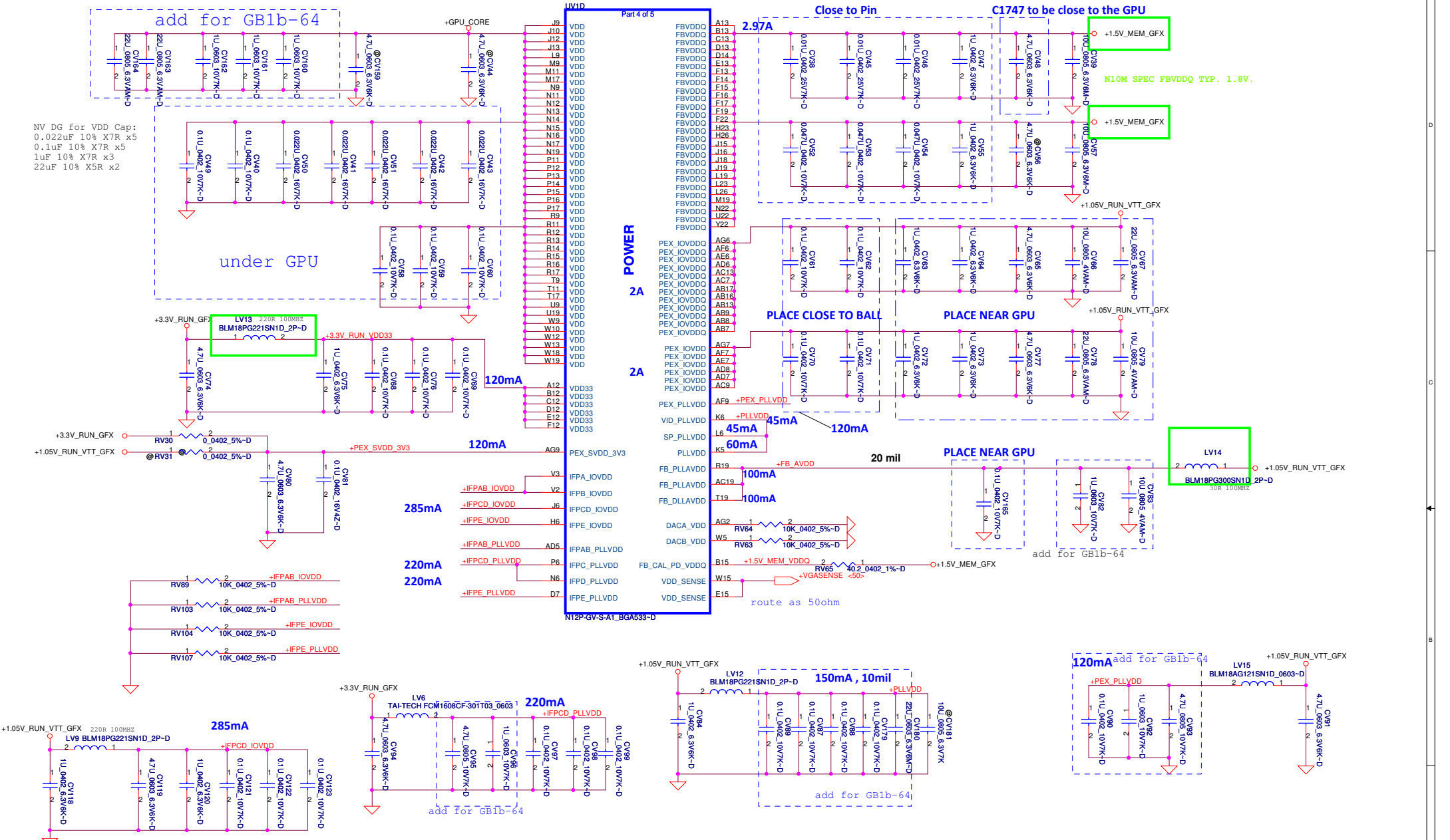
ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

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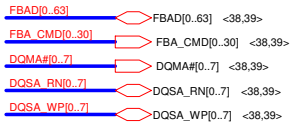


Compaq Electronics, Inc.
 Title: **N12P DP, STRAP, GND**
 Size: **LA-7451P**
 Date: Thursday, July 28, 2011
 Sheet: 35 of 51
 Rev: 1.0

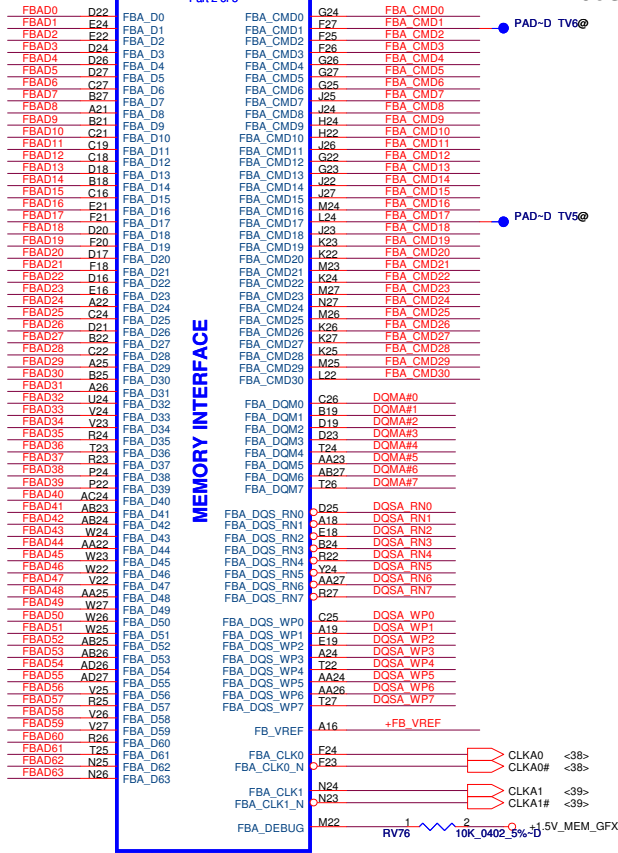


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	Compal Electronics, Inc.	
	N12P Power	
Title LA-7451P	Document Number LA-7451P	Rev 1.0
Date Thursday, July 28, 2011	Sheet 36 of 51	



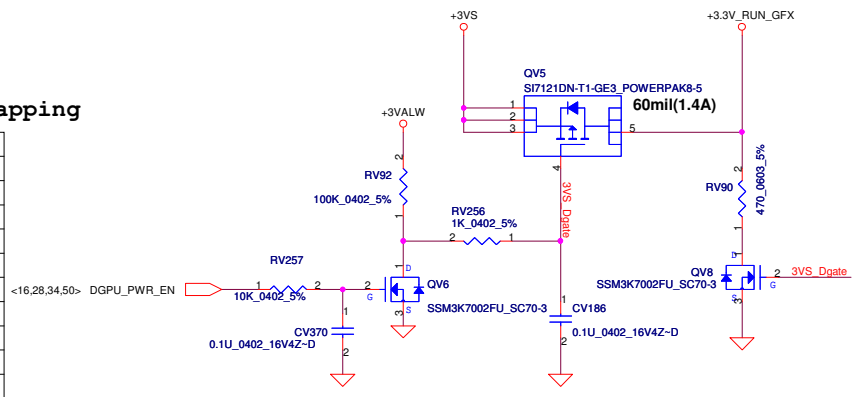
UV18 Part 2 of 5



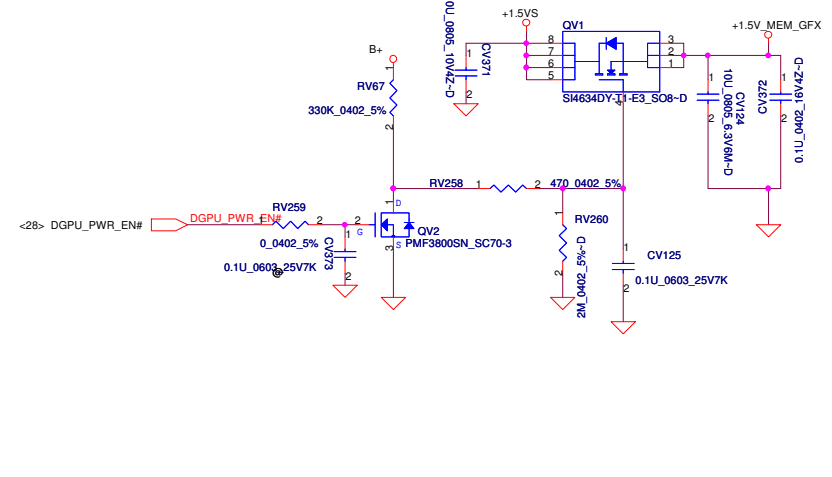
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

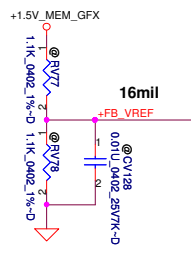
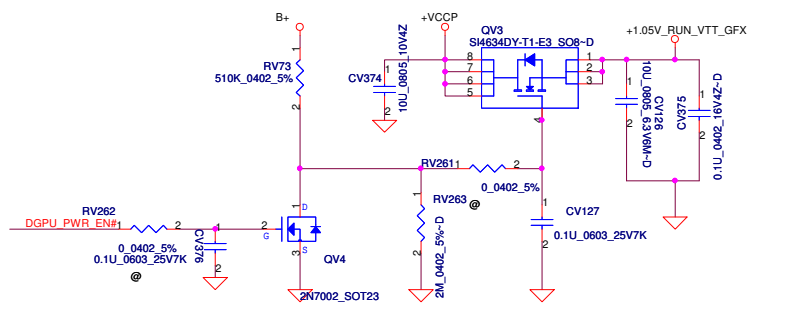
+3.3V_RUN_GFX Source



+1.5V_MEM_GFX Source



+1.05V_RUN_VTT_GFX Source



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Compal Electronics, Inc.

Title: **N12P Memory**

Size: **LA-7451P**

Date: Thursday, July 28, 2011

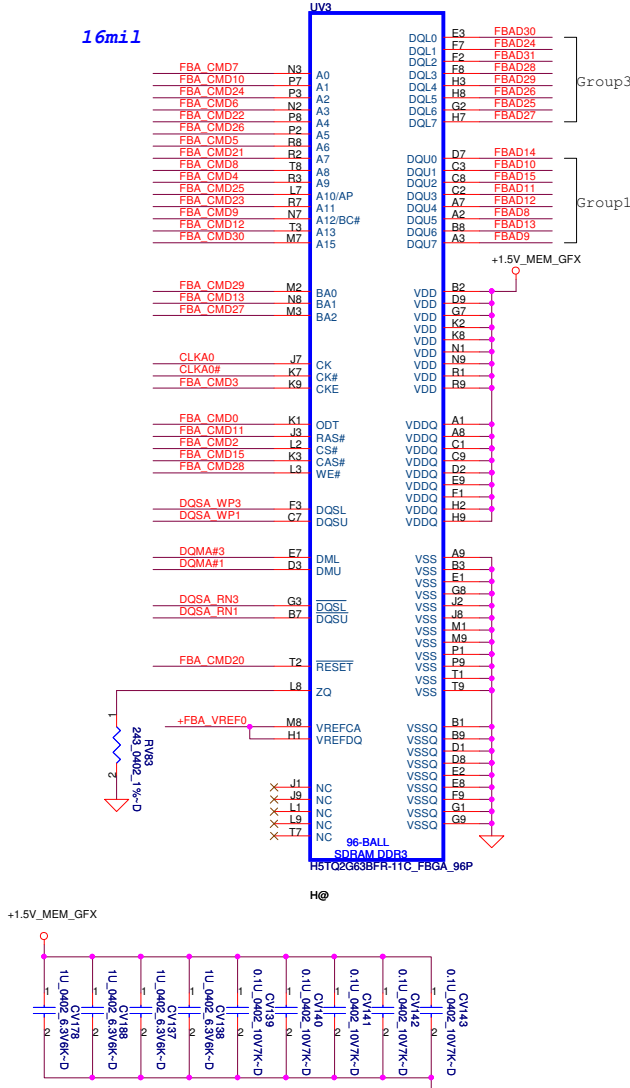
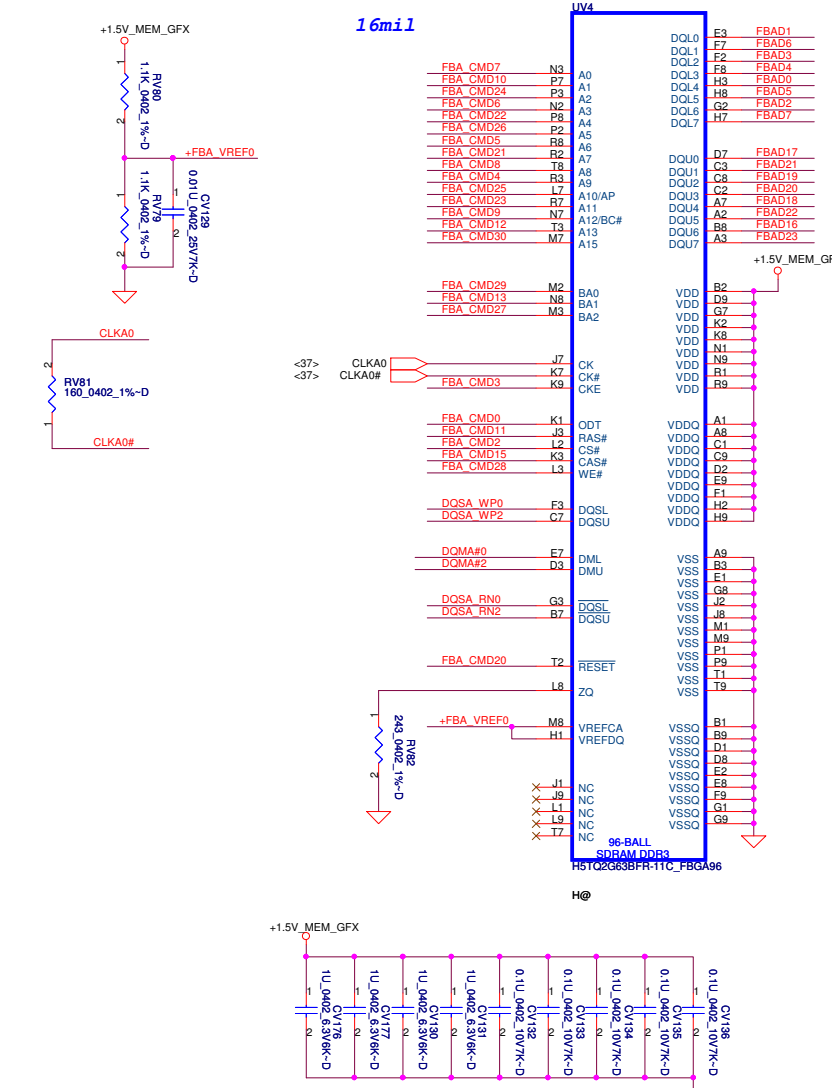
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Rev 1.0

Memory Partition A - Lower 32 bits

change to Hxix

- FBA_CMD[0..30] FBA_CMD[0..30] <37..39>
- FBAD[0..63] FBAD[0..63] <37..39>
- DOMA# [0..7] DOMA# [0..7] <37..39>
- DQSA_RN [0..7] DQSA_RN [0..7] <37..39>
- DQSA_WP [0..7] DQSA_WP [0..7] <37..39>



Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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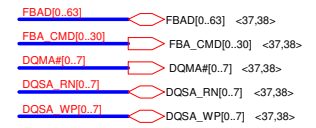
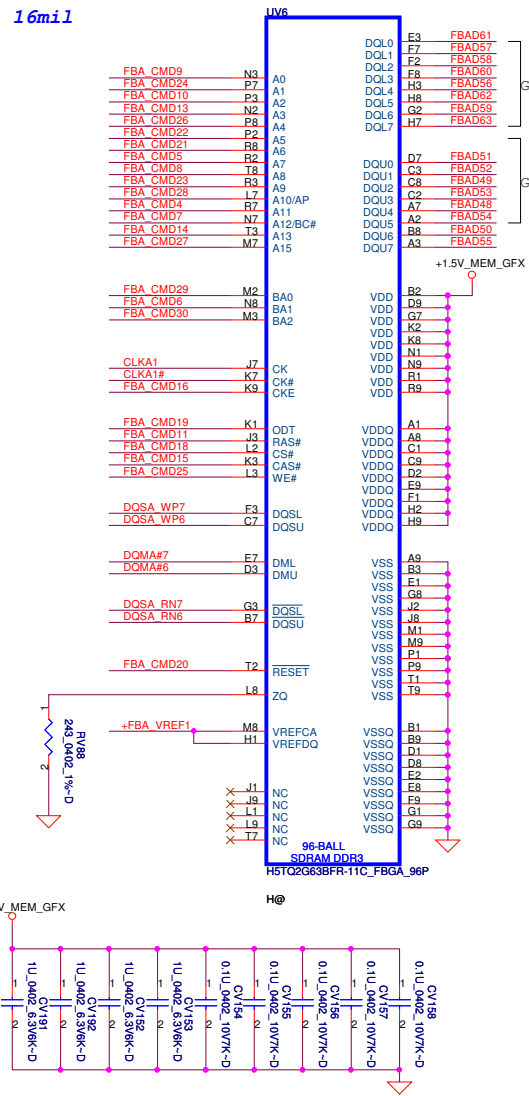
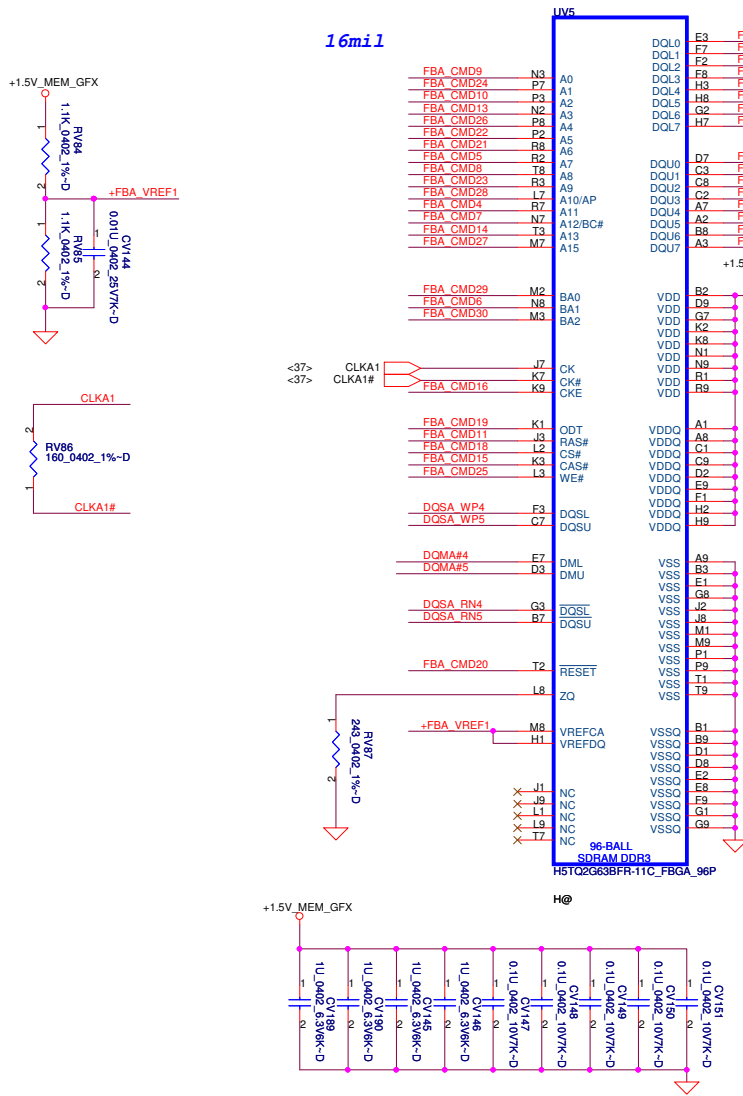
Compal Electronics, Inc.

VRAM A Lower

LA-7451P

Date:	Thursday, July 28, 2011	Sheet:	38 of 51
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Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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Compal Electronics, Inc.

Title: **VRAM A Upper**

Size: **LA-7451P**

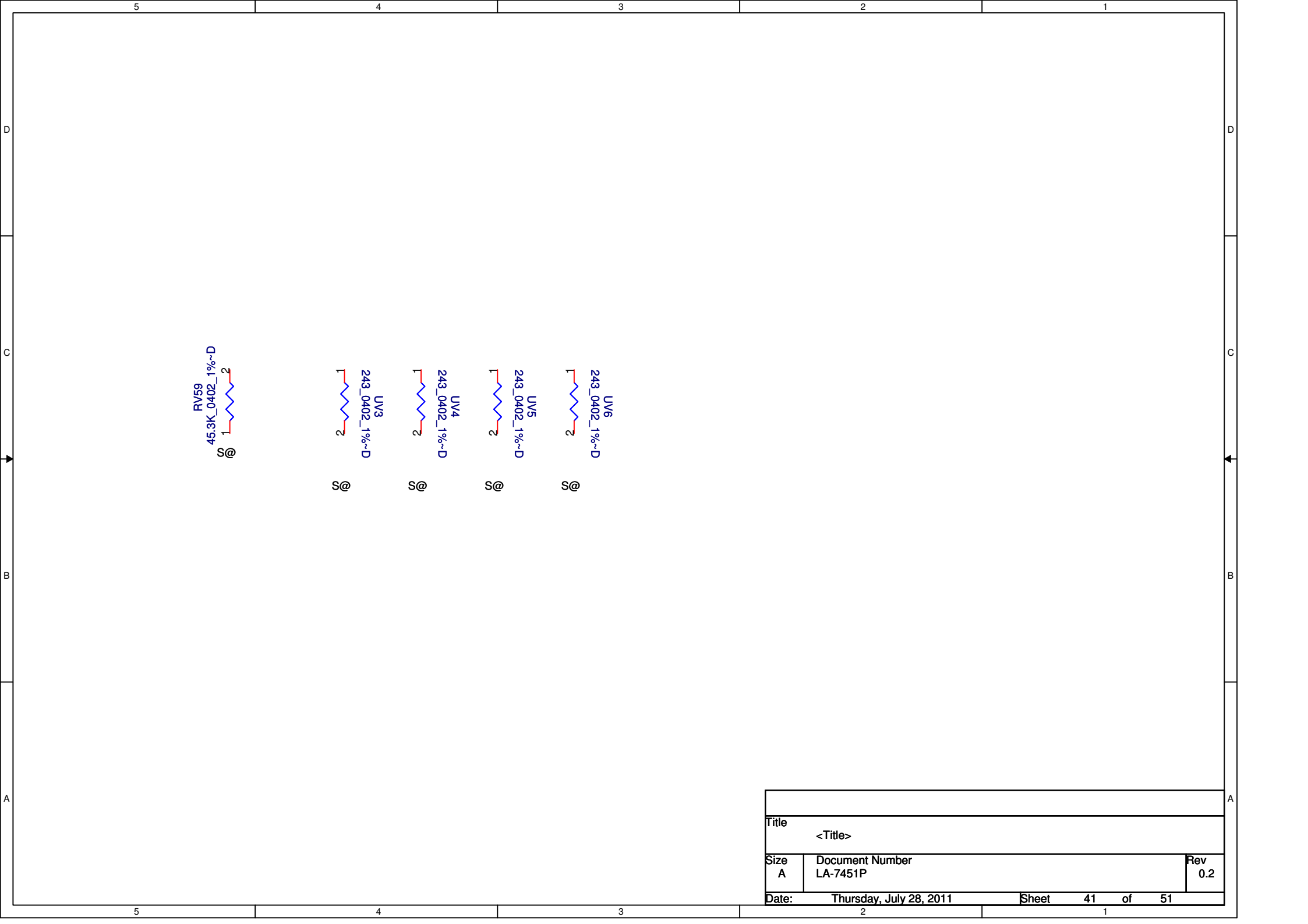
Date: Thursday, July 28, 2011

Document Number	Rev
1	1.0

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Item	Reason for change	PG#	Modify List	Date	Phase
1	SMBus signal Pull HIGH	15	Add R983,R984	2011/04/07	PT
2	SMBus signal Pull HIGH	25	Add RV22, RV29, QV7	2011/04/07	PT
3	vss pull low	35	Add RV106	2011/04/07	PT
4	hdmi HPD	29	Add R636	2011/04/07	PT
5	GPU_CLKDOWN_R PULL HIGH	34	Add RV10	2011/04/07	PT
6	PEG_A_CLKRQ# CONTROL	34	Add RV264, RV265, RV266, RV267, QV9	2011/04/07	PT
7	sounds too small	31	Change RC134, RC137 from 47K to 560ohm	2010/10/15	PT
8	protect HDMI plug in noise	29	add CV101	2010/10/15	PT
9	Modify USB3.0 Solution	30		2010/10/15	PT
10	change Lan symbol	22	JLAN1	2010/10/15	PT
11	Power LED no light when S3	21	Change JBTN1 Pin1 from +5VS to +5VALW net	2010/10/15	PT
12	ESD request		Add CC70	2010/10/15	PT
13	ESD request		Add CHI01	2010/10/17	PT
14	ESD request		Add CC71-CC75	2010/10/17	PT
15	ESD request		Add CC76-CC80	2010/10/17	PT
16	ESD request		Del CF61,3,8,9,10,11,16,17	2010/10/20	PT
17	USB 3.0 Wake Issue	30	Del RI19, Add CI51	2010/10/20	PT
18	USB 3.0 Wake Issue	30	Change RI18 Pin1 to UI2 pin7	2010/10/22	PT
19	T		Change BOM UV2, CV107, CV108, RV108, RV109 to remove	2010/10/22	ST
20	LCD timing		Change BOM C549 to SEI24474R80	2010/10/22	ST
21			Change BOM U48 to SA00003R80	2010/10/22	ST
22			Change BOM UV1 to SA00004Q40L	2010/10/22	ST
23				2010/10/24	PT
24				2010/10/24	PT
25				2010/10/26	PT
26				2010/12/1	ST
27				2010/12/1	ST
28				2010/12/1	ST
29				2010/12/1	ST
30				2010/12/1	ST
31				2010/12/6	ST
32				2010/12/6	ST
33				2010/12/6	ST
34				2010/12/6	ST
35				2010/12/8	ST
36				2010/12/8	ST
37				2010/12/8	ST
38				2010/12/8	ST
39				2010/12/9	ST
40					
41					
42					
43					
44					
45					
46					
47					
48					
49					
50					
51					
52					
53					
54					

Security Classification		Compal Secret Data		Compal Electronics, Inc. HW Changed-List History-1		
Issued Date	2009/07/25	Deciphered Date	2010/07/25			
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					LA-6961P	1.0
				Date:	Thursday, July 28, 2011	Sheet 40 of 51



RV59
45.3K_0402_K3:597
1 2

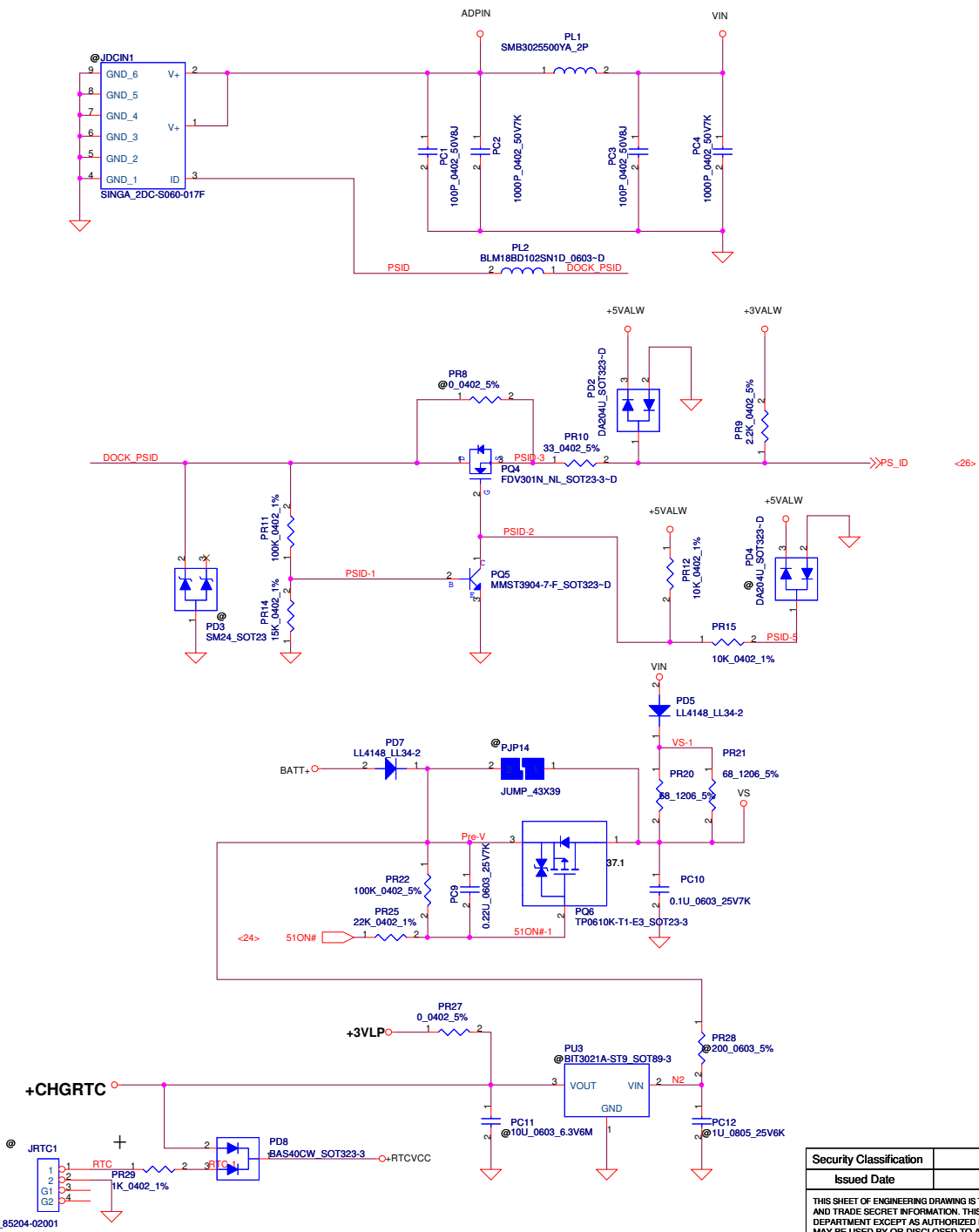
UV3
243_0402_1%~D
1 2
S

UV4
243_0402_1%~D
1 2
S

UV5
243_0402_1%~D
1 2
S

UV6
243_0402_1%~D
1 2
S

Title		
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Size	Document Number	Rev
A	LA-7451P	0.2
Date:	Thursday, July 28, 2011	Sheet 41 of 51



Security Classification	Compal Secret Data	
Issued Date	2010/12/24	Deciphered Date
		2011/12/24

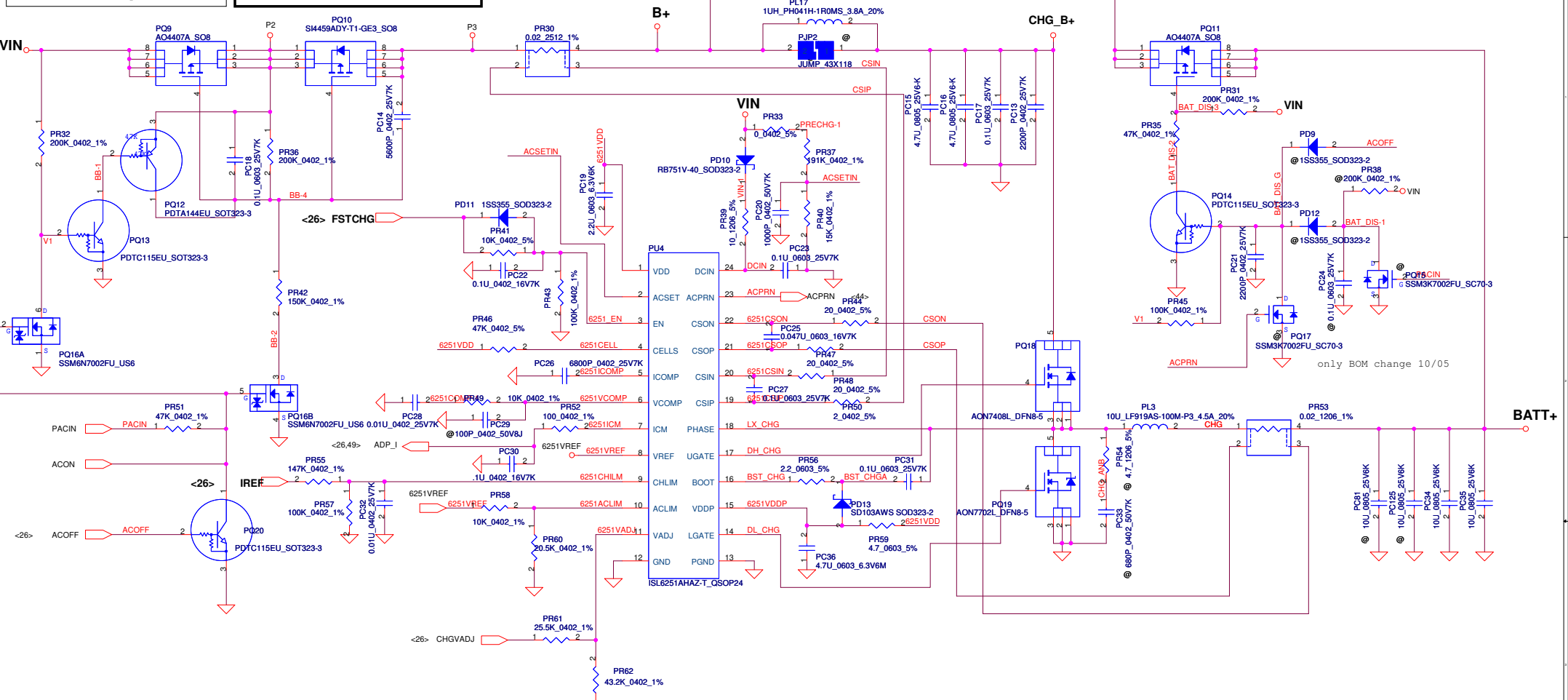
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Compal Electronics, Inc.		
PWR-DCIN / Vin Detector		
Size	Document Number	Rev
Custom		1.0
Date:	Thursday, July 28, 2011	Sheet 42 of 51

Iada=0~4.615A (90W/19.5V=4.615A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 4.15A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 $V_{ac1m} = 2.39 * ((20.5K / 152K) / ((10K / 152K) + (20.5K / 152K)))$

CC=2.8A
IREF=1*Icharge
IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

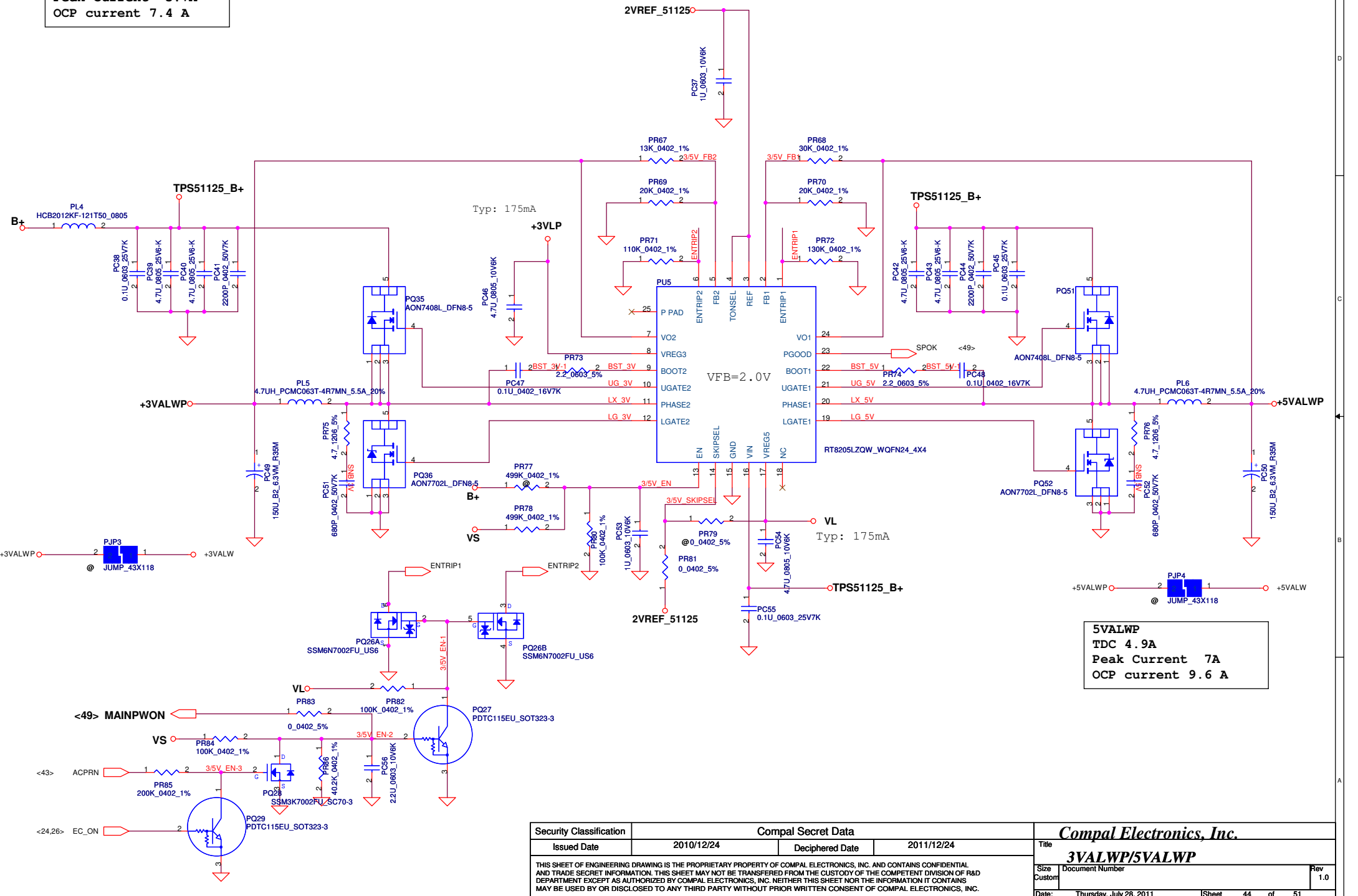
BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

Security Classification	Compal Secret Data	
Issued Date	2010/12/24	Deciphered Date
		2011/12/24

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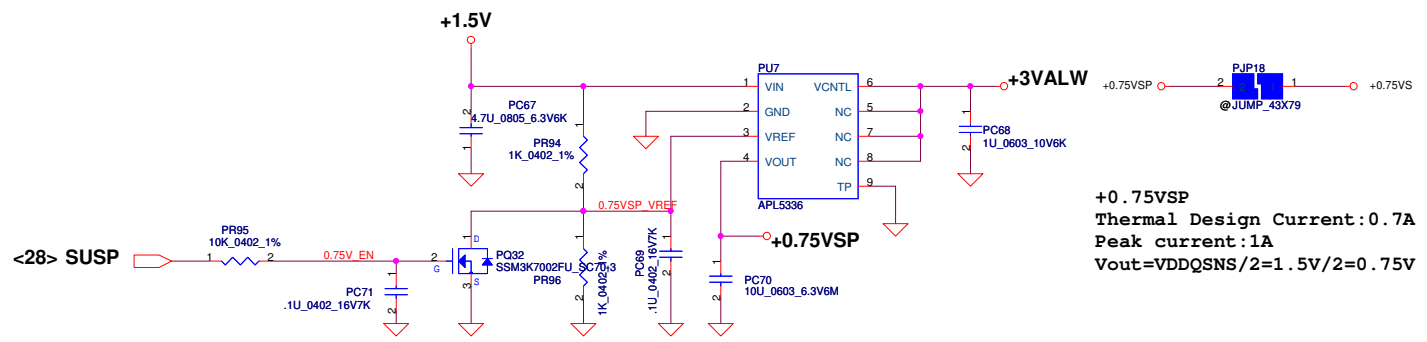
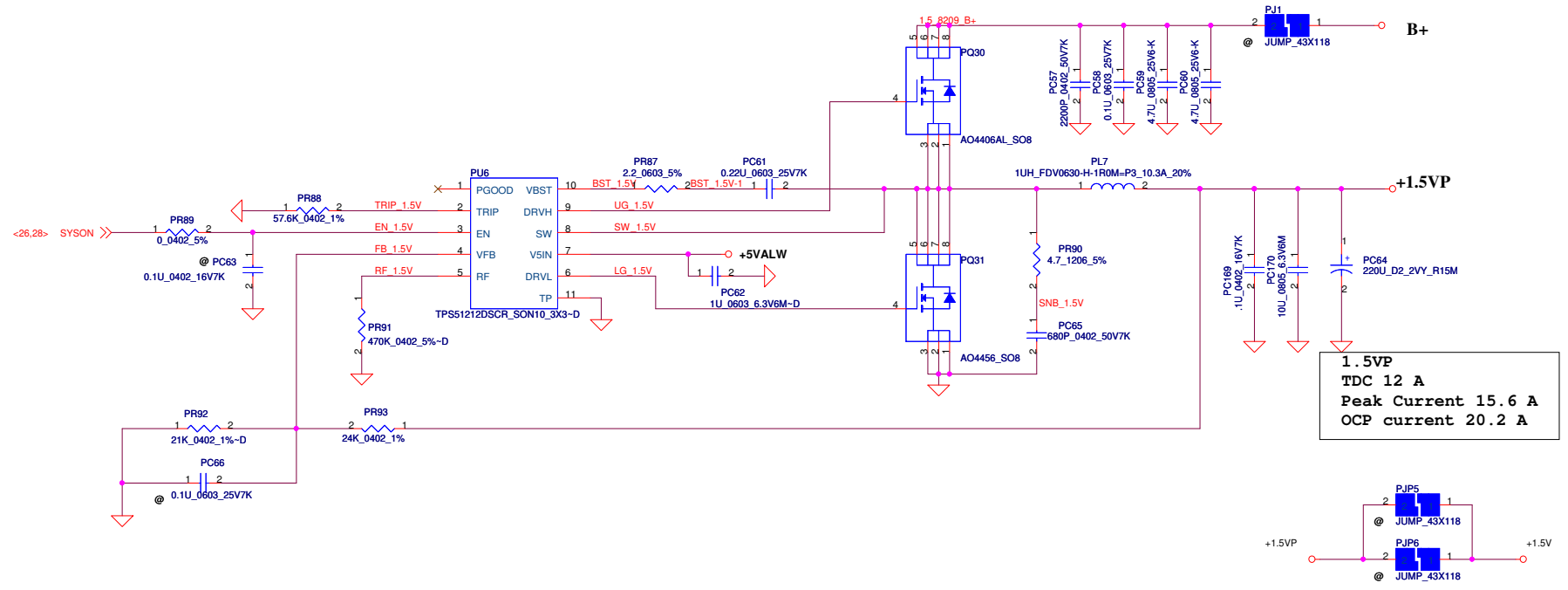
3.3VALWP
 TDC 4.02 A
 Peak Current 5.7A
 OCP current 7.4 A

5VALWP
 TDC 4.9A
 Peak Current 7A
 OCP current 9.6 A

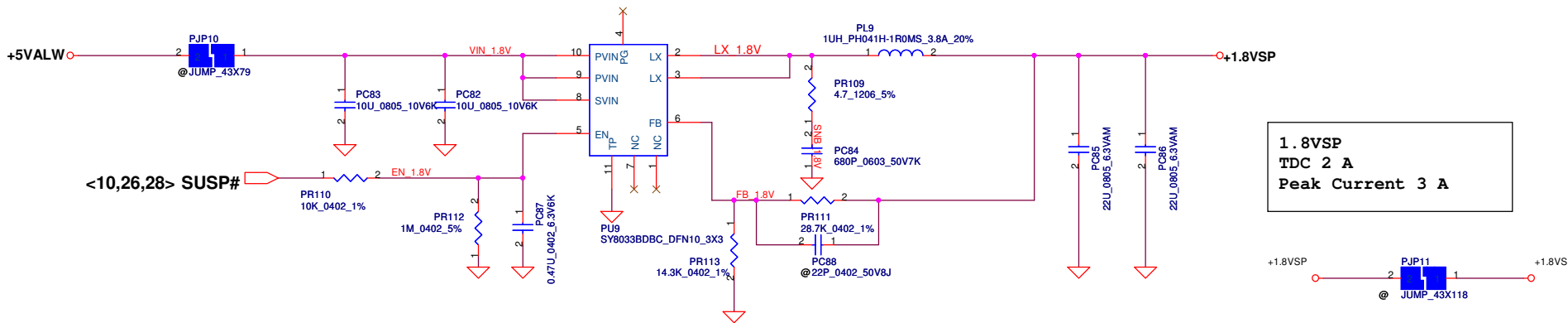
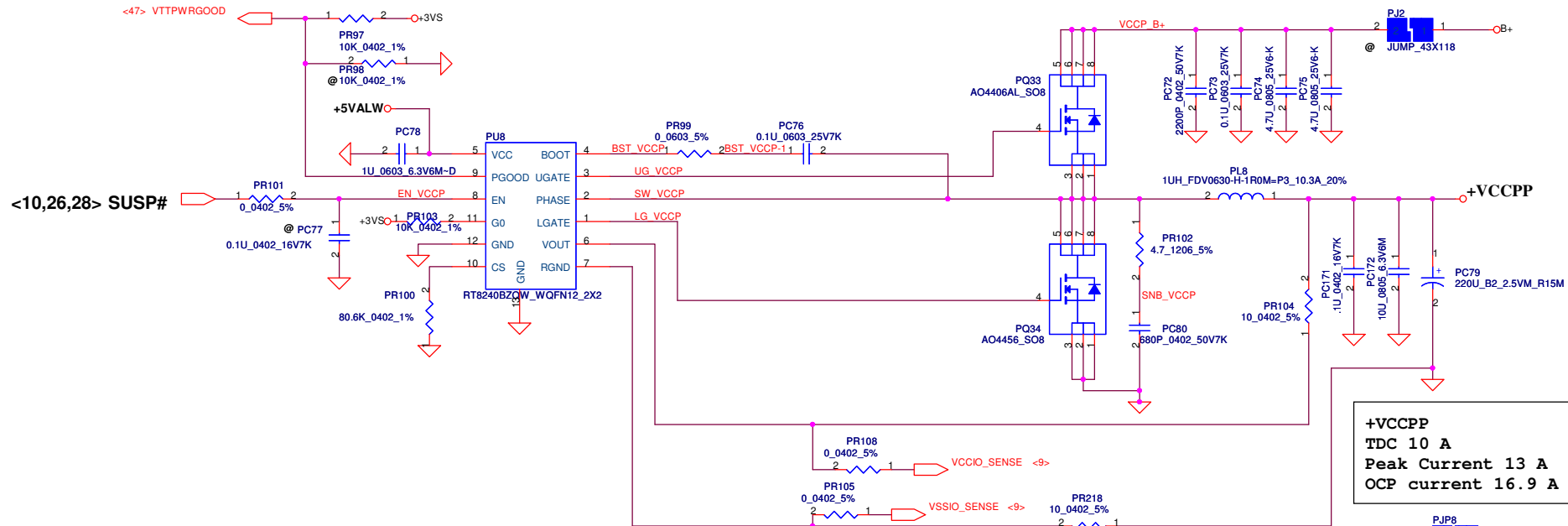


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Issued Date	2010/12/24	Deciphered Date	2011/12/24	3VALWP/5VALWP	
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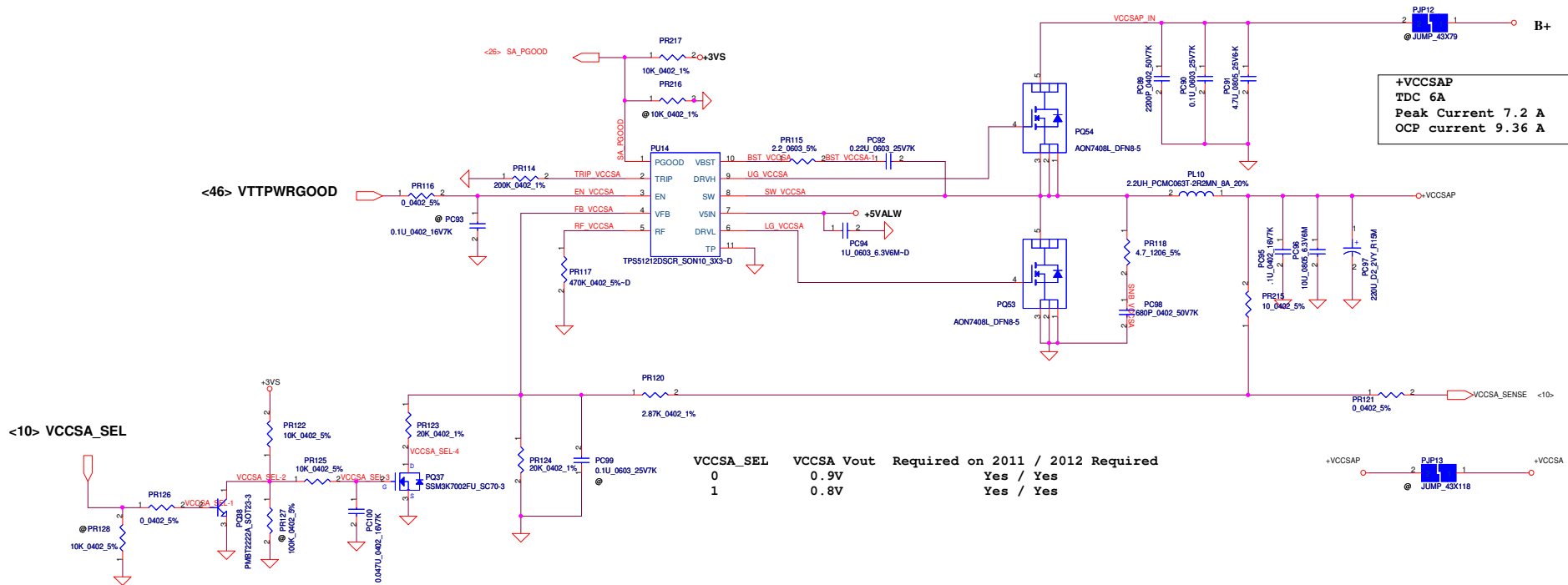
Compal Electronics, Inc.
 Document Number
 Rev 1.0



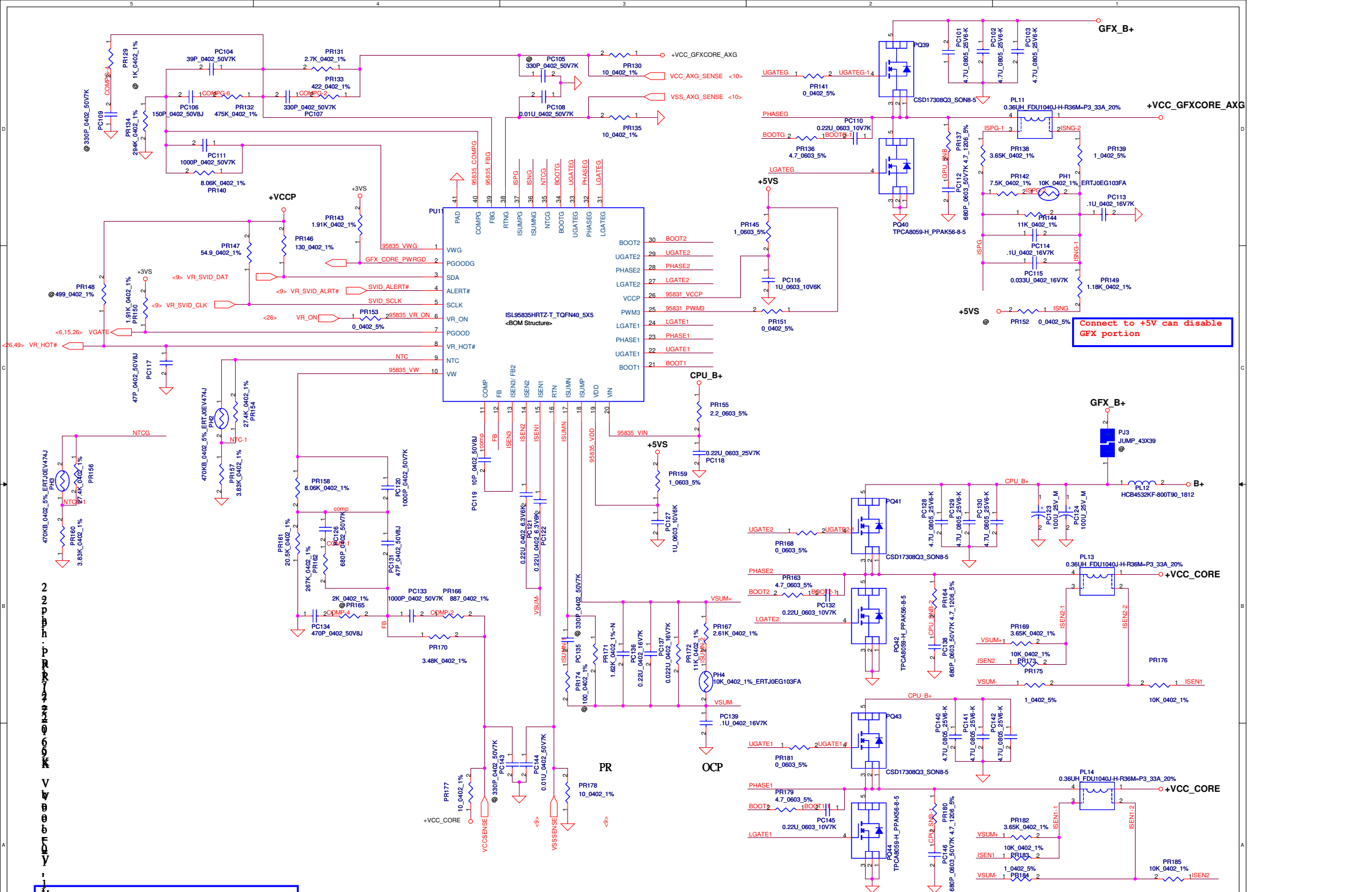
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+0.75V
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Size	Document Number				Rev
Custom					1.0
Date:	Thursday, July 28, 2011	Sheet	45	of	51



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Issued Date	2010/12/24	Deciphered Date	2011/12/24	Title	+VCCPP/+1.8VSP
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+VCCSAP
TDC 6A
Peak Current 7.2 A
OCF current 9.36 A



+CPU_CORE
 I_{ocp}=70A, I_{ccMAX}=53A
 Load line=1.9mohm
 DCR=1.1mohm

+GFX_CORE
 I_{ocp}=40A, I_{ccMAX}=24A
 Load line=3.9mohm
 DCR=1.1mohm

Security Classification	Compal Secret Data	
Issued Date	2010/12/24	Deciphered Date
		2011/12/24

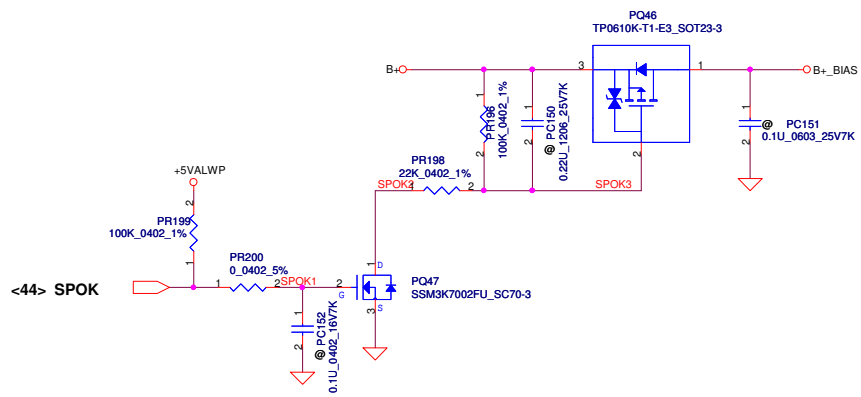
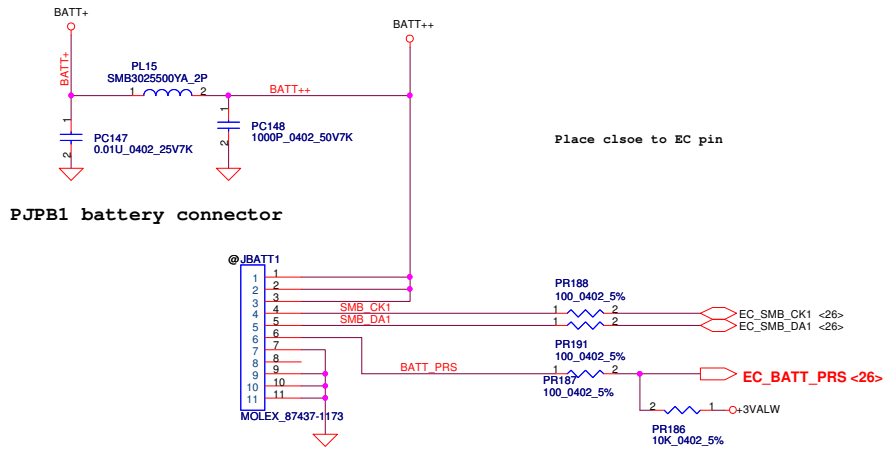
Compal Electronics, Inc.

Title: CPU_CORE/GFX

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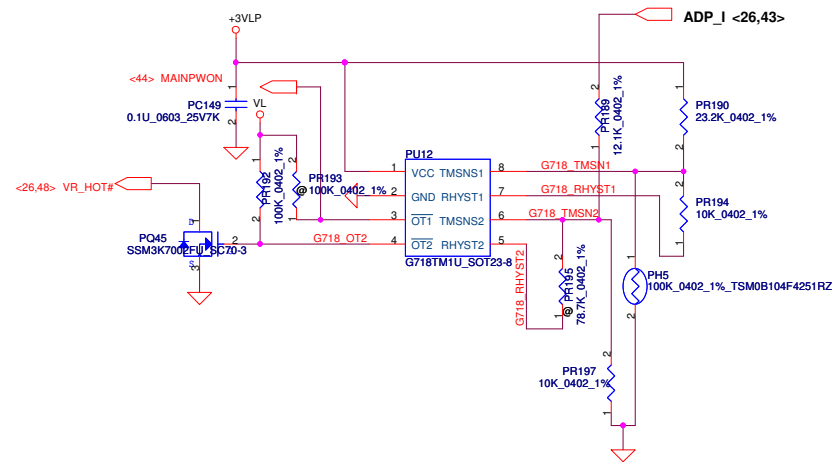
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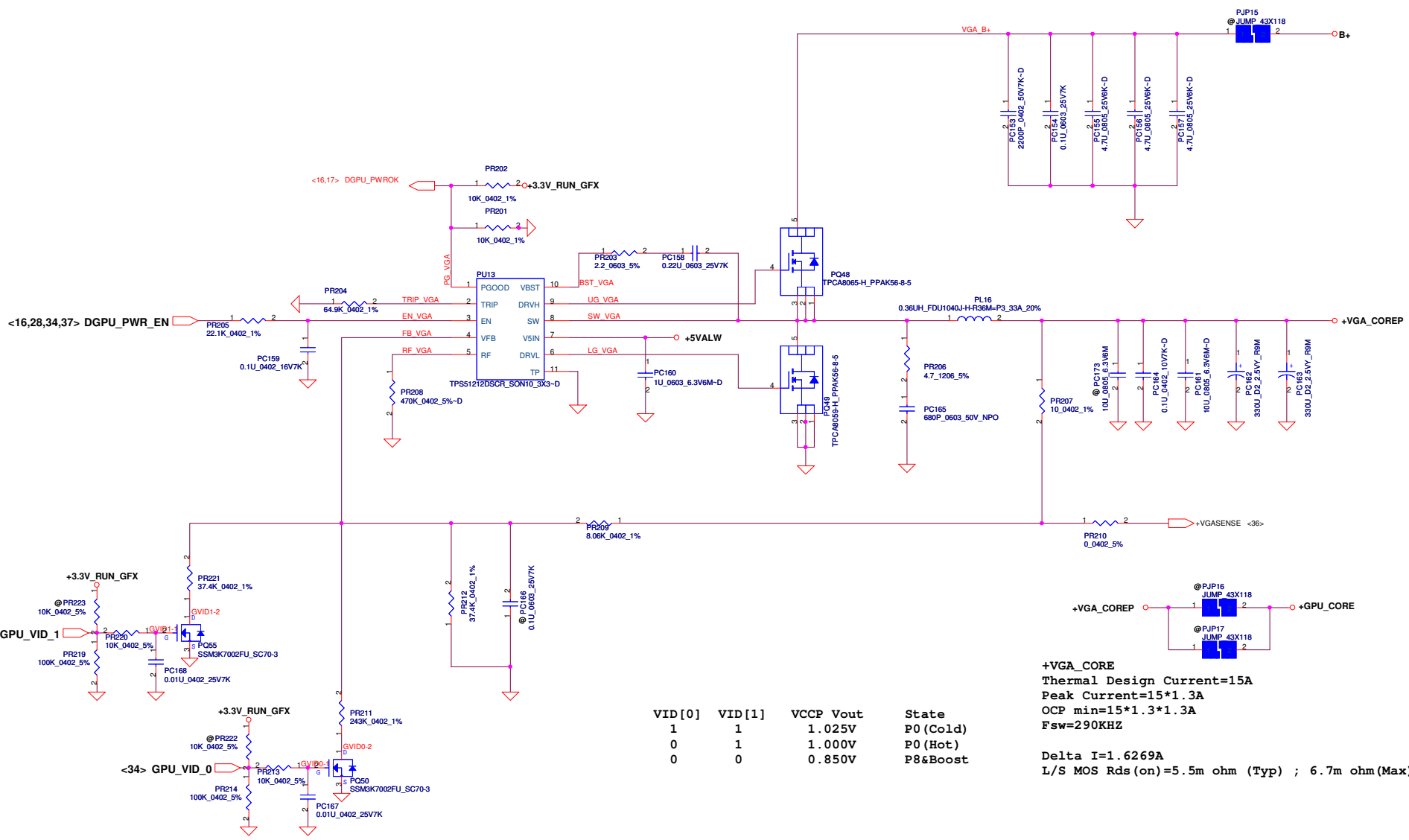


Battery Connect/OTP

PH3 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



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VID[0]	VID[1]	VCCP Vout	State
1	1	1.025V	P0 (Cold)
0	1	1.000V	P0 (Hot)
0	0	0.850V	P8&Boost

+VGA_CORE
 Thermal Design Current=15A
 Peak Current=15*1.3A
 OCP min=15*1.3*1.3A
 Fsw=290KHZ
 Delta I=1.6269A
 L/S MOS Rds(on)=5.5m ohm (Typ) ; 6.7m ohm (Max)

Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	modify Vcore and GFX boost resistance		P48	change PR136,PR163,PR179 to 2.2 +-5% 0603.	2011.2.10	before SSI
2	modify VGA FB resistance		P50	change PR211 to 243K +-1% 0402. PR221 to 37.4K +-1% 0402.	2011.3.24	SSI
3	modify 1.5V Enable signal		P45	change PR81 connect to SYSON.	2011.3.24	SSI
4	modify ADP_I protection		P49	change PR189 to 12.1k +-5% 0402.	2011.3.24	SSI
5	integrate mosfet		P45	change PQ53 PQ54 to AON7408L		
6	modify Vcore and GFX's loadline and OCP		P48	change PR171 to 1.62K +-1% 0402 change PR170 to 3.48K +-1% 0402 change PR149 to 1.18K +-1% 0402 change PR131 to 2.7K +-1% 0402 change PC115 to .033U 16V K X7R 0402		
7	modify VGA for HW team suggest item		P50	add PR219 100K +-5% 0402 remove PR223 10K +-5% 0402 change PR205 to 22.1K +-1% 0402		
8	integrate mosfet		P45 P47	change PQ32 to SSM3K7002FU 1N SC70-3 change PQ37 to SSM3K7002FU 1N SC70-3		
9	add capacitance for RF team suggest item		P43 P45 P46 P50	change PC81 PC125 to 10U 25V K X5R 0805 H1.25 change PC169 to .1U 16V K X7R 0402 change PC170 to 10U 6.3V M X5R 0805 H1.25 change PC171 to .1U 16V K X7R 0402 change PC172 to 10U 6.3V M X5R 0805 H1.25 change PC173 to 10U 6.3V M X5R 0805 H1.25		
10	modify 1.5V OCP resistance		P45	change PR88 to 57.6K +-1% 0402		
11	modify VCCP OCP resistance		P46	change PR100 to 80.6K +-1% 0402		
12	modify choke footprint for DFX requirement			change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P		
13	modify PQ11 Vgs resistance		P43	change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402		
14	modify the net name of SPOK-'		P49	change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3		
15	modify PU12 vcc power from +3VALW to +3VLP		P49	change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP		
16	modify OTP resistance		P49	change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402		
17	modify VCORE VCCP resistance		P48	change PR145 to 1 +-5% 0603		

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