MODEL NAME : *QLM00*
PCB NO : *LA-7841P (DA**********)*
BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Chief River)

Ivy Bridge ULV(BGA1023) + Panther Point

DISCRETE VGA N13P-GV(optimus)

2012-01-19

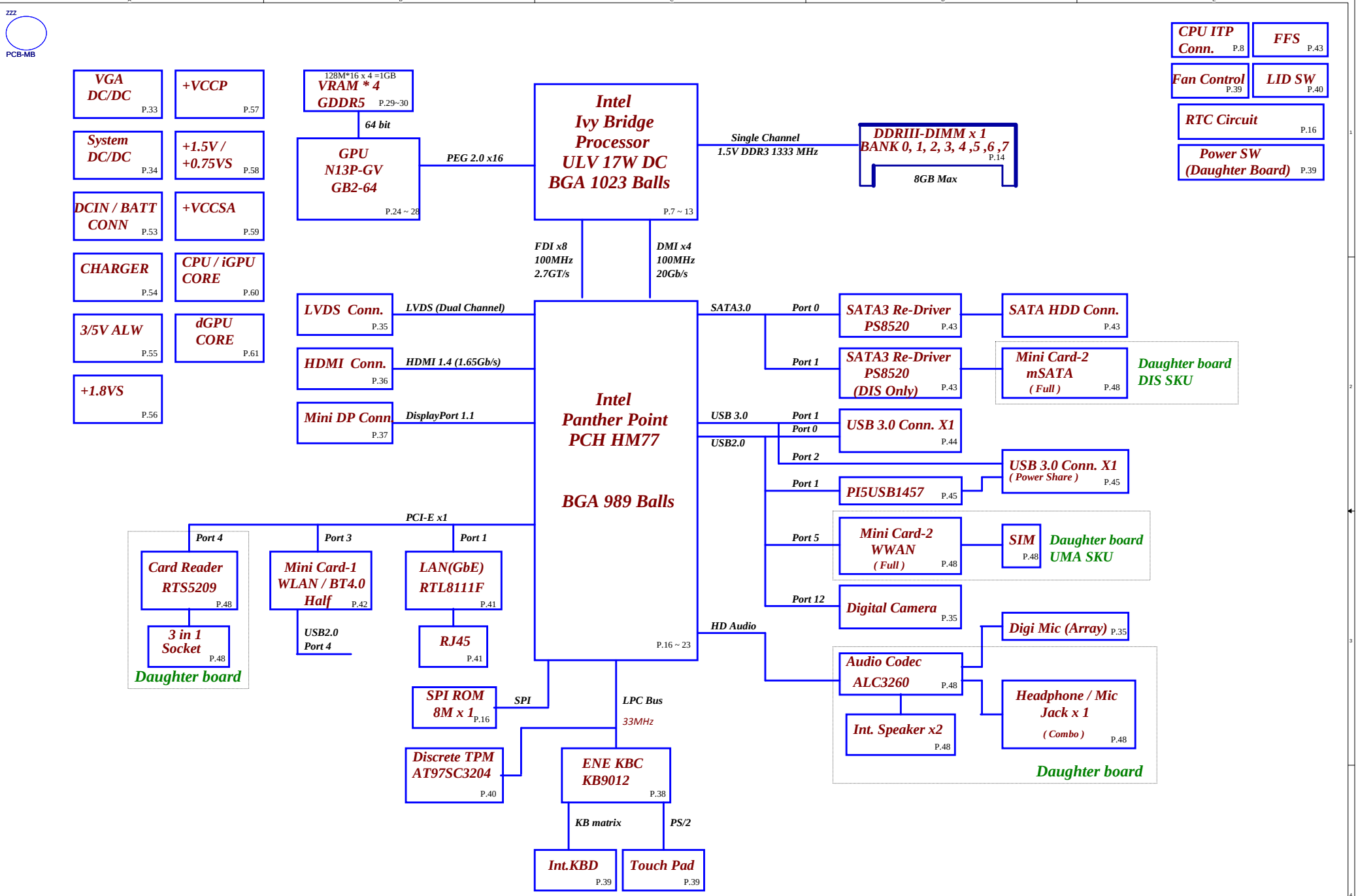
Rev: 1.0 (X04)

@ : Nopop Component
CONN@ : Connector Component
DIS@ : pop when DIS configuration
UMA@ : pop when UMA configuration

MB Type	BOM P/N	
TPM	4319EJ31L01	
TCM	4319EJ31L02	2@ 4@
TPM DIS/ TCM DIS		2@ 3@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Title	Cover Page		
Size	Document Number		Rev
	LA-7841P		0.3
Date:	Tuesday, February 07, 2012	Sheet 1 of 65	

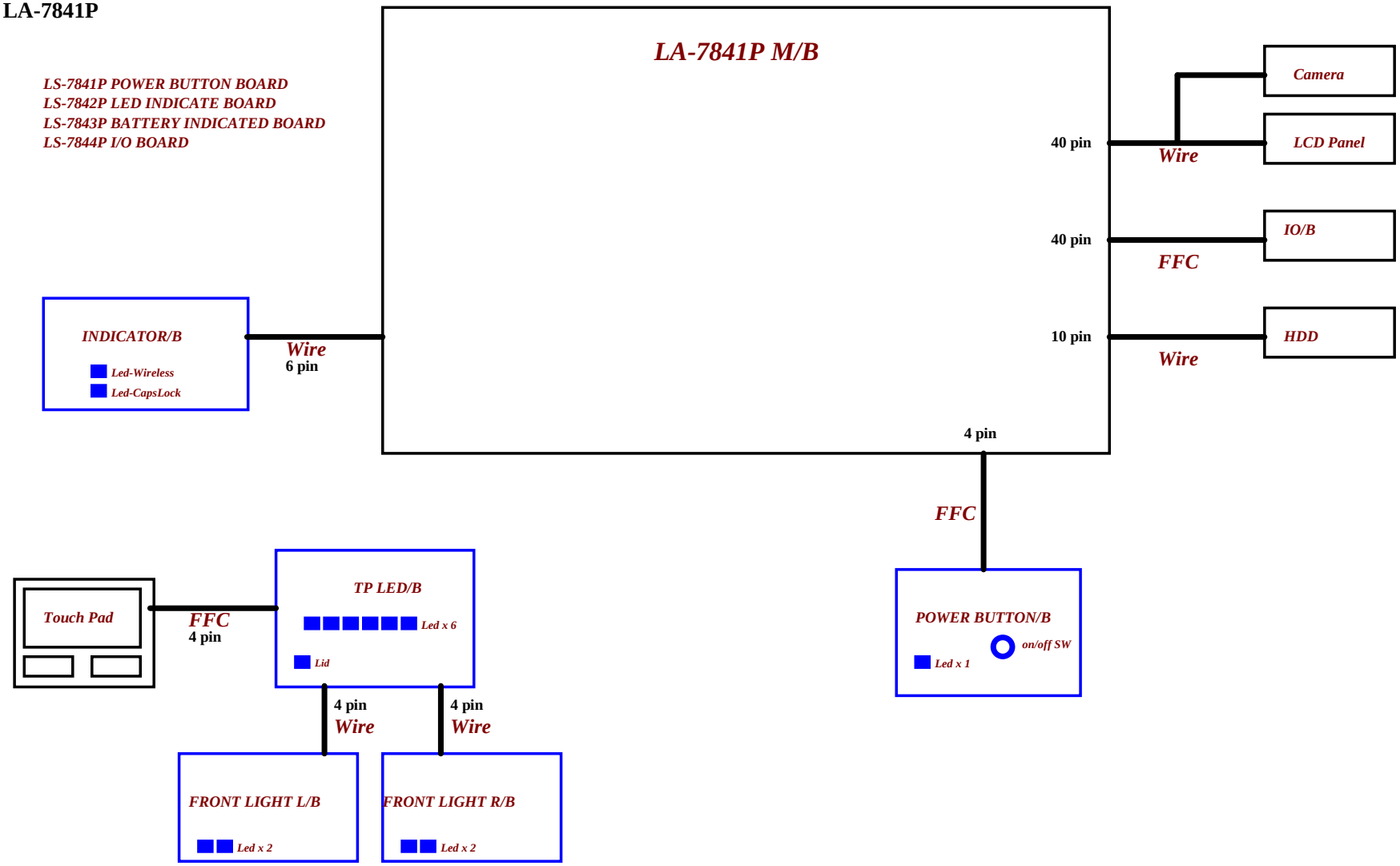


Security Classification	Compal Secret Data		Compal Electronics,Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Title			
Size C	Document Number		Rev 0.3
Date: Tuesday, February 07, 2012		Sheet 2 of 65	

Compal Confidential

Project Code : QLM00
File Name : LA-7841P



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Title	Block Diagram		
Size	Document Number		Rev 0.3
Date: Tuesday, February 07, 2012	Sheet 3	of 65	

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (2.0 Ext Left Side)
	2	Bluetooth
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN/DMC)
	6	ELC 8051
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
	13	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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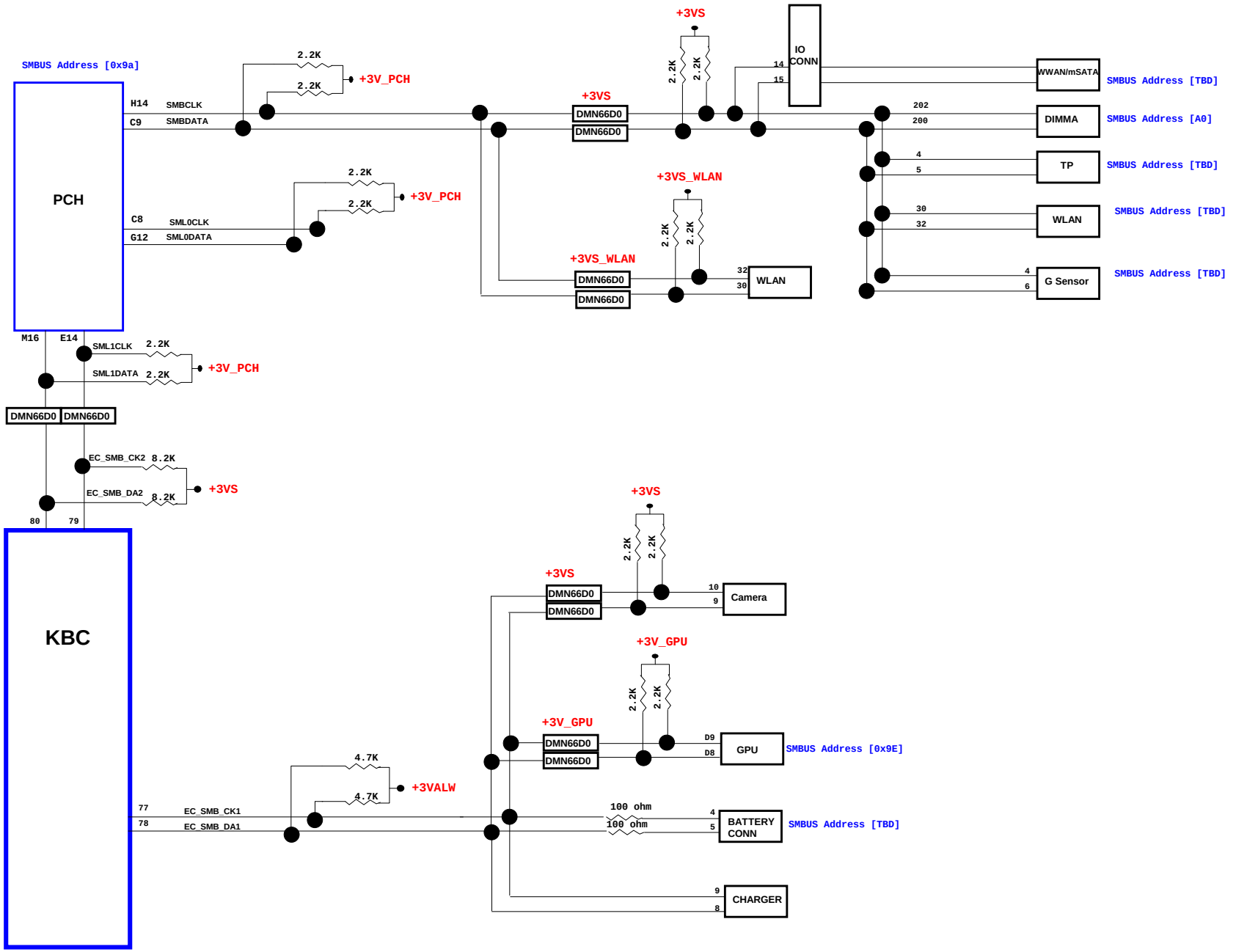
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 4 of 65



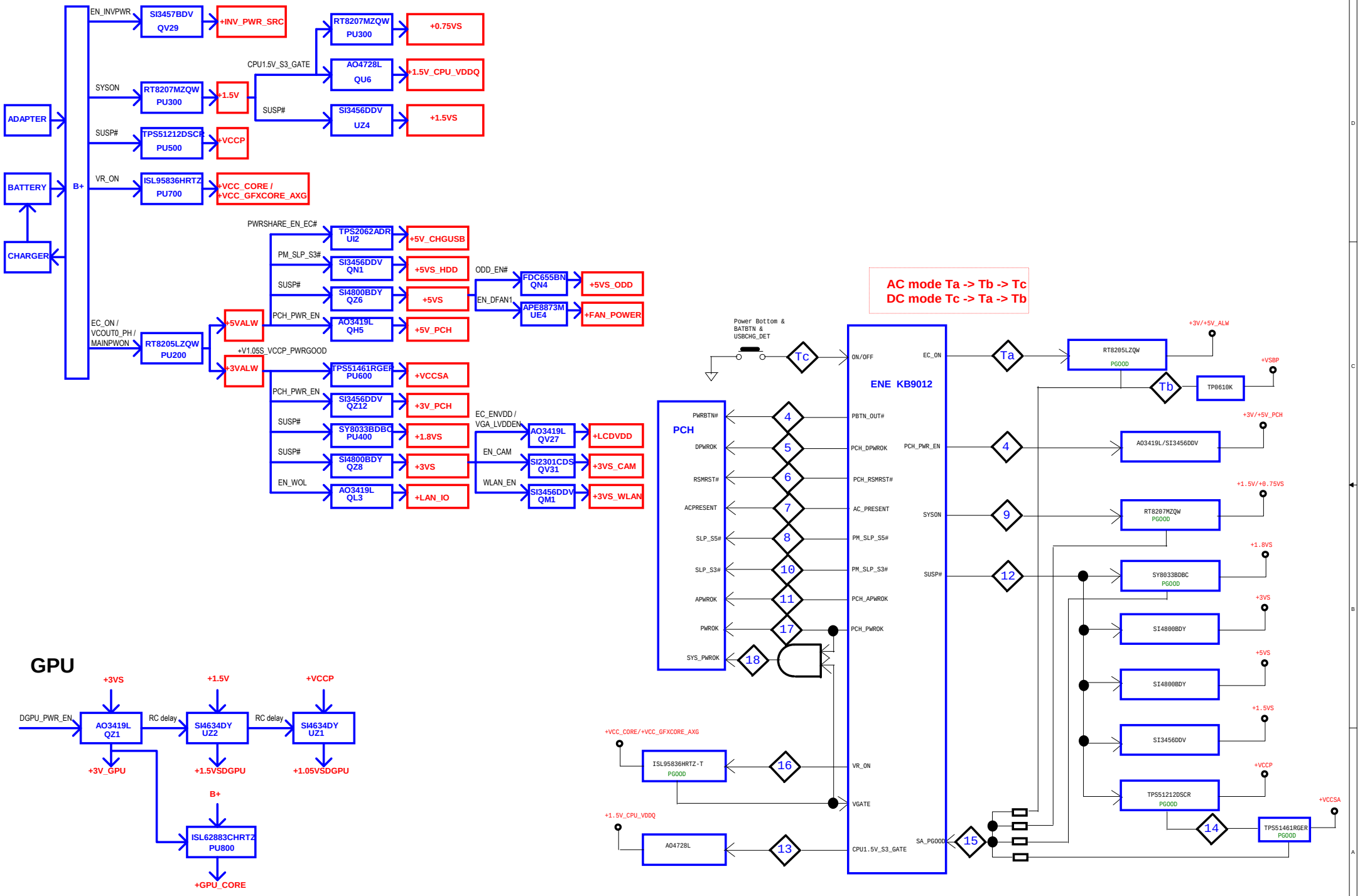
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom		0.3

Date: Tuesday, February 07, 2012 Sheet 5 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **Power Diagram**

Size	Document Number	Rev
		0.3

Date: Tuesday, February 07, 2012 Sheet 6 of 65

PEG_RCOMPO (G4) — R_COMP place close to CPU
PEG_ICOMPI (G3) — width 4 mils — VCC_IO
PEG_ICOMPO (G1) — width 12 mils — R_COMP

Trace length Max is 500 mils

PEG_ICOMPI and RCOMPO signals should be shorted and routed with max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with max length = 500 mils
- typical impedance = 14.5 mohms

U2A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
eDP

<18> DMI_CRX_PTX_N0 M2 DMI_RX#[0]
<18> DMI_CRX_PTX_N1 P6 DMI_RX#[1]
<18> DMI_CRX_PTX_N2 P1 DMI_RX#[2]
<18> DMI_CRX_PTX_N3 P10 DMI_RX#[3]
<18> DMI_CRX_PTX_P0 N3 DMI_RX[0]
<18> DMI_CRX_PTX_P1 P7 DMI_RX[1]
<18> DMI_CRX_PTX_P2 P3 DMI_RX[2]
<18> DMI_CRX_PTX_P3 P11 DMI_RX[3]
<18> DMI_CTX_PRX_N0 K1 DMI_TX#[0]
<18> DMI_CTX_PRX_N1 M8 DMI_TX#[1]
<18> DMI_CTX_PRX_N2 N4 DMI_TX#[2]
<18> DMI_CTX_PRX_N3 R2 DMI_TX#[3]
<18> DMI_CTX_PRX_P0 K3 DMI_TX[0]
<18> DMI_CTX_PRX_P1 M7 DMI_TX[1]
<18> DMI_CTX_PRX_P2 P4 DMI_TX[2]
<18> DMI_CTX_PRX_P3 T3 DMI_TX[3]

U7
<18> FDI_CTX_PRX_N0 W11 FDI0_TX#[0]
<18> FDI_CTX_PRX_N1 W1 FDI0_TX#[1]
<18> FDI_CTX_PRX_N2 AA6 FDI0_TX#[2]
<18> FDI_CTX_PRX_N3 W6 FDI0_TX#[3]
<18> FDI_CTX_PRX_N4 V4 FDI1_TX#[0]
<18> FDI_CTX_PRX_N5 Y2 FDI1_TX#[1]
<18> FDI_CTX_PRX_N6 AC9 FDI1_TX#[2]
<18> FDI_CTX_PRX_N7 FDI1_TX#[3]

U6
<18> FDI_CTX_PRX_P0 W10 FDI0_TX[0]
<18> FDI_CTX_PRX_P1 W3 FDI0_TX[1]
<18> FDI_CTX_PRX_P2 AA7 FDI0_TX[2]
<18> FDI_CTX_PRX_P3 W7 FDI0_TX[3]
<18> FDI_CTX_PRX_P4 T4 FDI1_TX[0]
<18> FDI_CTX_PRX_P5 AA3 FDI1_TX[1]
<18> FDI_CTX_PRX_P6 AC8 FDI1_TX[2]
<18> FDI_CTX_PRX_P7 FDI1_TX[3]

<18> FDI_FSYNC0 AA11 FDI0_FSYNC
<18> FDI_FSYNC1 AC12 FDI1_FSYNC
<18> FDI_INT U11 FDI_INT
<18> FDI_LSYNC0 AA10 FDI0_LSYNC
<18> FDI_LSYNC1 AG8 FDI1_LSYNC

+VCCP — RU2 (1, 2) — 24.9_0402_1%
EDP_COMP AF3 eDP_COMPIO
AD2 eDP_ICOMPO
AG11 eDP_HPD#
AG4 eDP_AUX#
AF4 eDP_AUX
AC3 eDP_TX[0]
AC4 eDP_TX[1]
AE11 eDP_TX[2]
AE7 eDP_TX[3]
AC1 eDP_TX[0]
AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

IVY-BRIDGE_BGA1023-D
@

PEG_ICOMPI G3
PEG_ICOMPO G1
PEG_RCOMPO G4
PEG_COMP — RU1 (2, 1) — +VCCP — 24.9_0402_1%

PEG_RX#[0] H22 PEG_GTX_C_HRX_N15
PEG_RX#[1] J21 PEG_GTX_C_HRX_N14
PEG_RX#[2] B22 PEG_GTX_C_HRX_N13
PEG_RX#[3] D21 PEG_GTX_C_HRX_N12
PEG_RX#[4] A19 PEG_GTX_C_HRX_N11
PEG_RX#[5] D17 PEG_GTX_C_HRX_N10
PEG_RX#[6] B14 PEG_GTX_C_HRX_N9
PEG_RX#[7] D13 PEG_GTX_C_HRX_N8
PEG_RX#[8] A11 PEG_GTX_C_HRX_N7
PEG_RX#[9] B10 PEG_GTX_C_HRX_N6
PEG_RX#[10] G8 PEG_GTX_C_HRX_N5
PEG_RX#[11] A8 PEG_GTX_C_HRX_N4
PEG_RX#[12] B6 PEG_GTX_C_HRX_N3
PEG_RX#[13] H8 PEG_GTX_C_HRX_N2
PEG_RX#[14] E5 PEG_GTX_C_HRX_N1
PEG_RX#[15] K7 PEG_GTX_C_HRX_N0

PEG_RX[0] K22 PEG_GTX_C_HRX_P15
PEG_RX[1] K19 PEG_GTX_C_HRX_P14
PEG_RX[2] C21 PEG_GTX_C_HRX_P13
PEG_RX[3] D19 PEG_GTX_C_HRX_P12
PEG_RX[4] C19 PEG_GTX_C_HRX_P11
PEG_RX[5] D16 PEG_GTX_C_HRX_P10
PEG_RX[6] C13 PEG_GTX_C_HRX_P9
PEG_RX[7] D12 PEG_GTX_C_HRX_P8
PEG_RX[8] C11 PEG_GTX_C_HRX_P7
PEG_RX[9] C9 PEG_GTX_C_HRX_P6
PEG_RX[10] F8 PEG_GTX_C_HRX_P5
PEG_RX[11] C8 PEG_GTX_C_HRX_P4
PEG_RX[12] C5 PEG_GTX_C_HRX_P3
PEG_RX[13] H6 PEG_GTX_C_HRX_P2
PEG_RX[14] F6 PEG_GTX_C_HRX_P1
PEG_RX[15] K6 PEG_GTX_C_HRX_P0

PEG_TX#[0] G22 PEG_HTX_C_GRX_N15
PEG_TX#[1] C23 PEG_HTX_C_GRX_N14
PEG_TX#[2] D23 PEG_HTX_C_GRX_N13
PEG_TX#[3] F21 PEG_HTX_C_GRX_N12
PEG_TX#[4] H19 PEG_HTX_C_GRX_N11
PEG_TX#[5] C17 PEG_HTX_C_GRX_N10
PEG_TX#[6] K15 PEG_HTX_C_GRX_N9
PEG_TX#[7] F17 PEG_HTX_C_GRX_N8
PEG_TX#[8] F14 PEG_HTX_C_GRX_N7
PEG_TX#[9] A15 PEG_HTX_C_GRX_N6
PEG_TX#[10] J14 PEG_HTX_C_GRX_N5
PEG_TX#[11] H13 PEG_HTX_C_GRX_N4
PEG_TX#[12] M10 PEG_HTX_C_GRX_N3
PEG_TX#[13] F10 PEG_HTX_C_GRX_N2
PEG_TX#[14] D9 PEG_HTX_C_GRX_N1
PEG_TX#[15] J4 PEG_HTX_C_GRX_N0

PEG_TX[0] F22 PEG_HTX_C_GRX_P15
PEG_TX[1] A23 PEG_HTX_C_GRX_P14
PEG_TX[2] D24 PEG_HTX_C_GRX_P13
PEG_TX[3] E21 PEG_HTX_C_GRX_P12
PEG_TX[4] G19 PEG_HTX_C_GRX_P11
PEG_TX[5] B18 PEG_HTX_C_GRX_P10
PEG_TX[6] K17 PEG_HTX_C_GRX_P9
PEG_TX[7] G17 PEG_HTX_C_GRX_P8
PEG_TX[8] E14 PEG_HTX_C_GRX_P7
PEG_TX[9] C15 PEG_HTX_C_GRX_P6
PEG_TX[10] K13 PEG_HTX_C_GRX_P5
PEG_TX[11] G13 PEG_HTX_C_GRX_P4
PEG_TX[12] K10 PEG_HTX_C_GRX_P3
PEG_TX[13] G10 PEG_HTX_C_GRX_P2
PEG_TX[14] D8 PEG_HTX_C_GRX_P1
PEG_TX[15] K4 PEG_HTX_C_GRX_P0

PT
CU1 CU2 CU3 CU4 CU5 CU6 CU7 CU8 CU9 CU10 CU11 CU12 CU13 CU14 CU15 CU16 — 1 — 2 @ — 0.22U_0402_16V7K-D
CU17 CU18 CU19 CU20 CU21 CU22 CU23 CU24 — 1 — 2 @ — 0.22U_0402_16V7K-D
CU25 CU26 CU27 CU28 CU29 CU30 CU31 CU32 — 1 — 2 DIS@ — 0.22U_0402_16V7K-D
SSI2

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

PEG_GTX_C_HRX_N[0..15] — PEG_GTX_C_HRX_N[0..15] <24>
PEG_GTX_C_HRX_P[0..15] — PEG_GTX_C_HRX_P[0..15] <24>
PEG_HTX_C_GRX_N[0..15] — PEG_HTX_C_GRX_N[0..15] <24>
PEG_HTX_C_GRX_P[0..15] — PEG_HTX_C_GRX_P[0..15] <24>

PT
CPU Option
Sandy Bridge 1.6G
U2
SNB1.6G
CPU_SNB1.6G@
Ivy Bridge 1.5G
U2
IVB1.5G
CPU_IVB1.5G@
Ivy Bridge 1.7G
U2
IVB1.7G
CPU_IVB1.7G@

Trace length Max is 500 mils

R_COMP place close to CPU
eDP_COMPIO (AF3) — width 4 mils — VCC_IO
eDP_ICOMPO (AD2) — width 12 mils — R_COMP

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.
Title: PROCESSOR(1/7) DMI,FDI,PEG
Size: Custom | Document Number | Rev: 0.3
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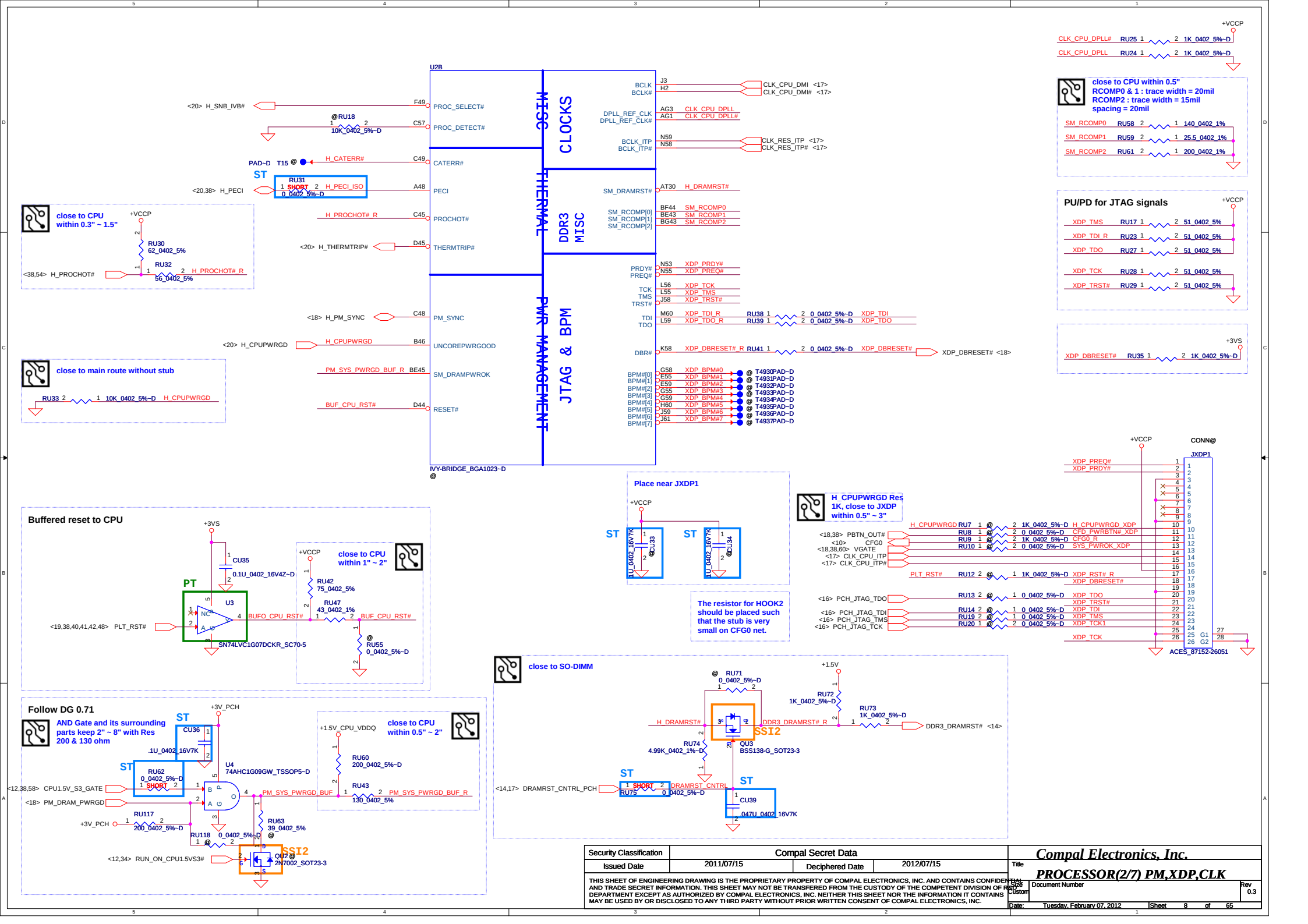


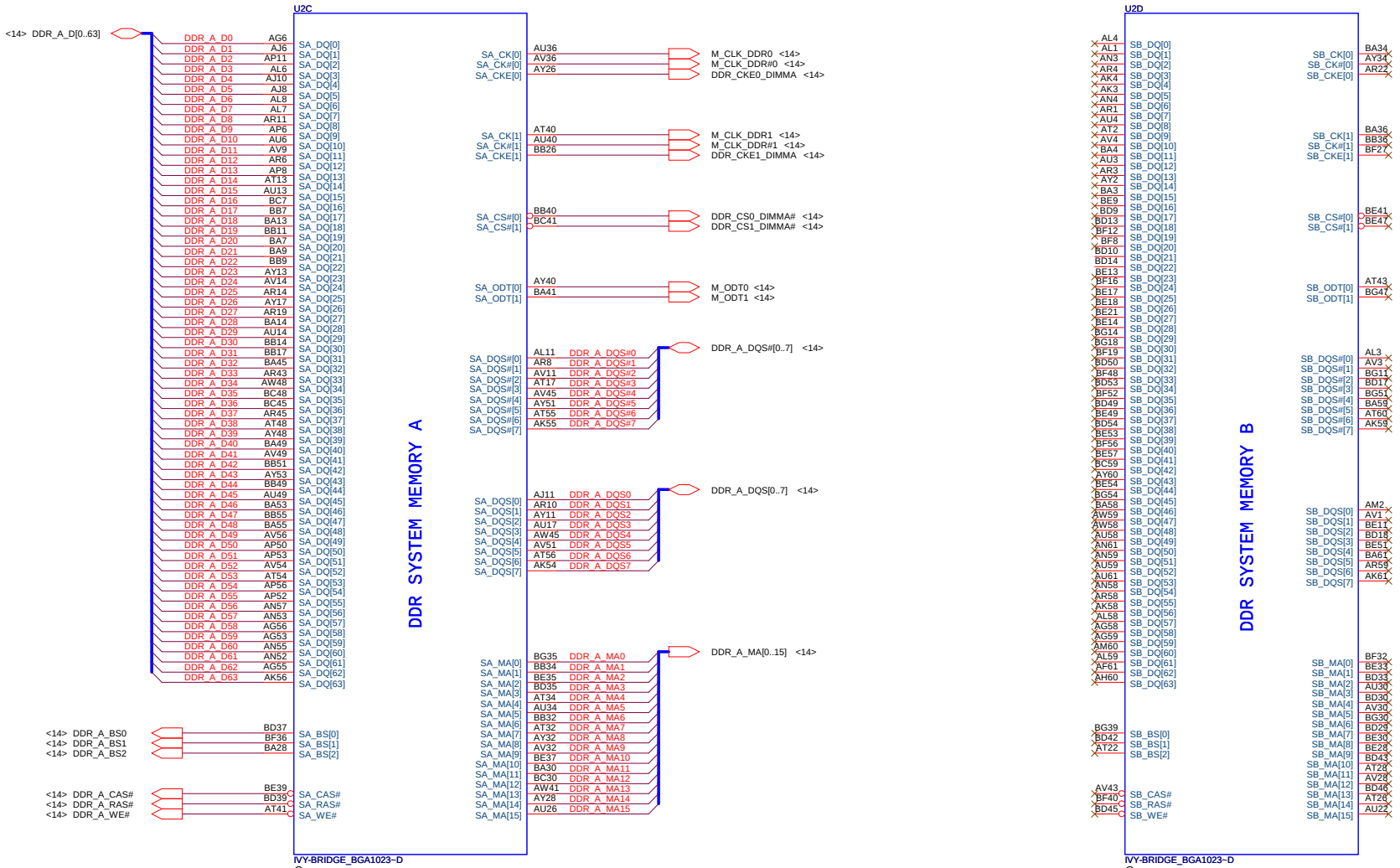
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom		0.3

Date: Tuesday, February 07, 2012 Sheet 8 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom		0.3

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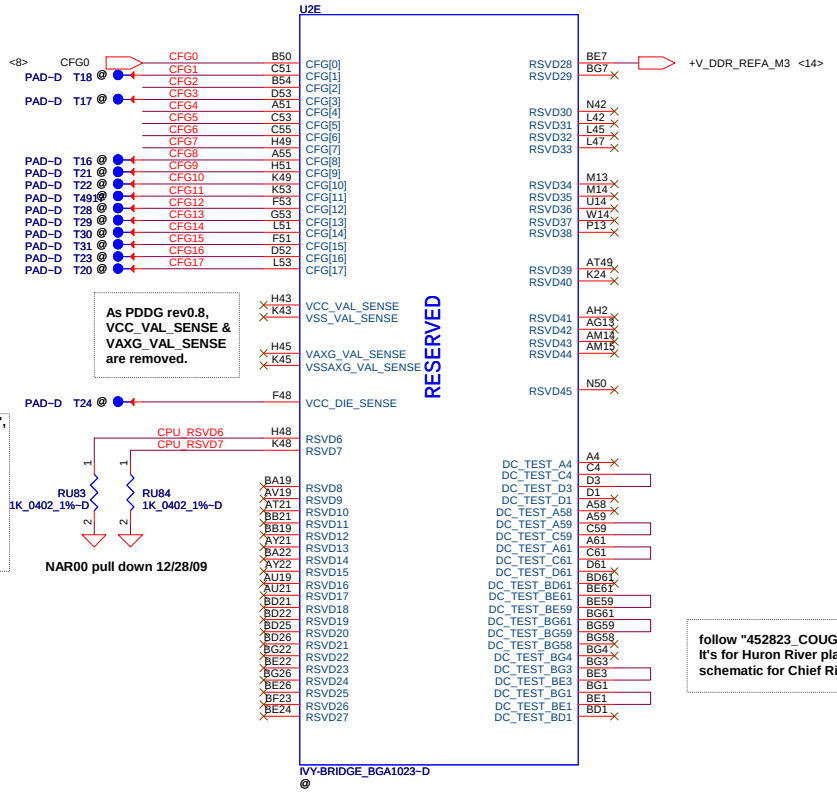


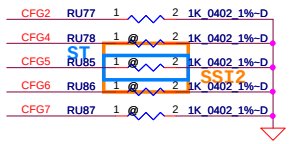
As PDDG rev0.8, VCC_VAL_SENSE & VAXG_VAL_SENSE are removed.

follow "458544_CR_PDDG_rev_0.8", section "2.2.1", Intel recommends providing accessibility to the pins F48 & G48 for debug purpose. The pins should be via through to the backside of the board to allow backside probing with no connection to other rails/components on the platform.

NAR00 pull down 12/28/09

follow "452823_COUGAR_CANYON(BGA1023)_Customer_Ready_Schematic". It's for Huron River platform, since can't find CPU Ivy bridge BGA1023 schematic for Chief River at this moment.

CFG Straps for Processor



		1 (Default value)	0
PCI Express* Static x16 Lane Numbering Reversal	CFG2	Normal operation (match socket pin map)	Lane numbers reversed
PCI Express* Static x4 Lane Numbering Reversal	CFG3	Normal operation (match socket pin map)	Lane numbers reversed
eDP enable	CFG4	Disable	Enable
PEG DEFER TRAINING	CFG7	PEG Train immediately following RESETB de-assertion	PEG Wait for BIOS for training

PCI Express Bifurcation (x16 Lane)	CFG[6:5]	11	1 x16 PCI Express (Default value)
		10	2 x8 PCI Express
		01	reserved
		00	1 x8, 2 x4 PCI Express

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 10 of 65

POWER

+VCC_CORE decoupling Cap. in Page 62.

+VCCP decoupling Cap. in Page 62.

U2F

+VCC_CORE

33A

ULV 17W , Max Current in Turbo Mode or HFM

CORE SUPPLY

A26	VCC[1]
A29	VCC[2]
A31	VCC[3]
A34	VCC[4]
A35	VCC[5]
A38	VCC[6]
A39	VCC[7]
A42	VCC[8]
C26	VCC[9]
C27	VCC[10]
C32	VCC[11]
C34	VCC[12]
C37	VCC[13]
C39	VCC[14]
C42	VCC[15]
D27	VCC[16]
D32	VCC[17]
D34	VCC[18]
D37	VCC[19]
D39	VCC[20]
D42	VCC[21]
E26	VCC[22]
E28	VCC[23]
E32	VCC[24]
E34	VCC[25]
E37	VCC[26]
E38	VCC[27]
F25	VCC[28]
F26	VCC[29]
F28	VCC[30]
F32	VCC[31]
F34	VCC[32]
F37	VCC[33]
F38	VCC[34]
F42	VCC[35]
G42	VCC[36]
H25	VCC[37]
H26	VCC[38]
H28	VCC[39]
H29	VCC[40]
H32	VCC[41]
H34	VCC[42]
H35	VCC[43]
H37	VCC[44]
H38	VCC[45]
H40	VCC[46]
J25	VCC[47]
J26	VCC[48]
J28	VCC[49]
J29	VCC[50]
J32	VCC[51]
J34	VCC[52]
J35	VCC[53]
J37	VCC[54]
J38	VCC[55]
J40	VCC[56]
J42	VCC[57]
K26	VCC[58]
K27	VCC[59]
K29	VCC[60]
K32	VCC[61]
K34	VCC[62]
K35	VCC[63]
K37	VCC[64]
K39	VCC[66]
K42	VCC[67]
L25	VCC[68]
L28	VCC[69]
L33	VCC[70]
L36	VCC[71]
L40	VCC[72]
N26	VCC[73]
N30	VCC[74]
N34	VCC[75]
N38	VCC[76]

PEG IO AND DDR IO

+VCCP

8.5A

AF46	VCCIO[1]
AG48	VCCIO[3]
AG50	VCCIO[4]
AG51	VCCIO[5]
AJ17	VCCIO[6]
AJ21	VCCIO[7]
AJ25	VCCIO[8]
AJ43	VCCIO[9]
AJ47	VCCIO[10]
AK50	VCCIO[11]
AK51	VCCIO[12]
AL14	VCCIO[13]
AL15	VCCIO[14]
AL16	VCCIO[15]
AL20	VCCIO[16]
AL22	VCCIO[17]
AL26	VCCIO[18]
AL45	VCCIO[19]
AL48	VCCIO[20]
AM16	VCCIO[21]
AM17	VCCIO[22]
AM21	VCCIO[23]
AM43	VCCIO[24]
AM47	VCCIO[25]
AN20	VCCIO[26]
AN42	VCCIO[27]
AN45	VCCIO[28]
AN48	VCCIO[29]
AA14	VCCIO[30]
AA15	VCCIO[31]
AB17	VCCIO[32]
AB20	VCCIO[33]
AC13	VCCIO[34]
AD16	VCCIO[35]
AD18	VCCIO[36]
AD21	VCCIO[37]
AE14	VCCIO[38]
AE15	VCCIO[39]
AF16	VCCIO[40]
AF18	VCCIO[41]
AF20	VCCIO[42]
AG15	VCCIO[43]
AG16	VCCIO[44]
AG17	VCCIO[45]
AG20	VCCIO[46]
AG21	VCCIO[47]
AJ14	VCCIO[48]
AJ15	VCCIO[49]

+VCCP

W16 VCCIO50
W17 VCCIO51

CU40 1U_0402_6.3V6K~D

VCCIO_SEL BC22 @ T25 PAD~D

As 473716_Ivy_Bridge_EDS(1 of 2)_Mobile_rev1.5, Page 92, VCCIO_SEL, "For Chief River platforms this pin should not be used"

QUIET RAILS

+VCCP

VCCPQE[1] AM25
VCCPQE[2] AN22

CU94 1U_0402_6.3V6K~D

close to CPU within 0.3" ~ 1.5"

+VCCP

RU93 75_0402_5%

SVID

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43
VIDSOUT C44

RU94 1 2 43_0402_1%

VR_SVID_ALRT# <60>
VR_SVID_CLK <60>
VR_SVID_DAT <60>

RU92 2 1 130_0402_5% +VCCP

close to CPU within 0.3" ~ 1.5"

SENSE LINES

+VCC_CORE

RU97 100_0402_1%~D

close to CPU within 2"

VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R

VCCSENSE <60>
VSSSENSE <60>

RU102 100_0402_1%~D

RU100 1 2 10_0402_1%~D +VCCP

VCCIO_SENSE AN16 VCCIO_SENSE_R
VSS_SENSE_VCCIO AN17 VSS_SENSE_VCCIO

VCCIO_SENSE <57>
VSSIO_SENSE <57>

RU103 10_0402_1%~D

close to CPU within 2"

IVY-BRIDGE_BGA1023~D
@

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom	Document Number	Rev: 0.3
Date: Tuesday, February 07, 2012	Sheet 11 of 65	

POWER

+VCC_GFXCORE_AXG decoupling Cap. in Page 62.

33A

ULV GT2 , Max Current in Turbo Mode

U2G

GRAPHICS | VREF | DDR3 - 1.5V RAILS | SENSE LINES | QUIET RAILS | 1.8V RAIL | SENSE LINES | SA RAIL | VCCSA VID lines

VAXG[1..56] — AA46, AB47, AB50, AB51, AB52, AB53, AB55, AB56, AB58, AB59, AC61, AD47, AD48, AD50, AD51, AD52, AD53, AD55, AD56, AD58, AD59, AE46, N45, P47, P48, P50, P51, P52, P53, P55, P56, P61, T48, T58, T59, T61, U46, V47, V48, V50, V51, V52, V53, V55, V56, V58, V59, W50, W51, W52, W53, W55, W56, W61, Y48, Y61

SM_VREF — AY43

+SM_VREF — RU105 1K_0402_1%~D, RU107 1K_0402_1%~D, CU97 .1U_0402_16V7K

RU120 0_0402_5%~D — +0.75VS

+V_DDR_REFA — @RU104 0_0402_5%~D

RU121 100K_0402_5%~D @ — @QU4 AP2302GN-HF_SOT23-3 — RUN_ON_CPU1.5VS3

VREF traces should have 20 mil trace width & spacing to other signals

VDDQ[1..26] — AJ28, AJ33, AJ36, AJ40, AL30, AL34, AL38, AL42, AM33, AM36, AM40, AN30, AN34, AN38, AR26, AR28, AR30, AR32, AR34, AR36, AR40, AV41, AW26, BA40, BB28, BG33

5A

+1.5V_CPU_VDDQ — CU98–CU107 1U_0402_6.3V6K~D; CU108–CU117 10U_0603_6.3V6M~D, 330U_D2_2V_Y

+1.5V_CPU_VDDQ — CU95–CU154 0.1U_0402_10V7K

Intel PDDG rev0.8 :
330uF x 1 - Bottom CPU edge
10uF x 8 - Bottom CPU edge
1uF x 10 - Under CPU

close to CPU within 2"

+VCC_GFXCORE_AXG — RU114 100_0402_1%~D

<60> VCC_AXG_SENSE — RU122 SHORT 0_0402_5%~D — VCC_AXG_SENSE_R — F45 VAXG_SENSE

<60> VSS_AXG_SENSE — RU123 SHORT 0_0402_5%~D — VSS_AXG_SENSE_R — G45 VSSAXG_SENSE

RU115 100_0402_1%~D

+1.8VS — RU116 0_0805_5%~D SHORT

Intel PDDG rev0.8 :
330uF x 1 - Bottom CPU edge
1uF x 2 - Top CPU edge

1.5A

+1.8VS_VCCPLL — CU138 330U_D2_25VY_R8M~D; CU140, CU141 1U_0402_6.3V6K~D

VCCPLL[1..3] — BB3, BC1, BC4

6A

+VCCSA — CU142 330U_D2_2V_Y; CU143–CU150 10U_0603_6.3V6M~D; CU146–CU152 1U_0402_6.3V6K~D

VCCSA[1..16] — L17, L21, N16, N20, N22, P17, P20, R16, R18, R21, U15, V16, V17, V18, V21, W20

Intel PDDG rev0.8 :
330uF x 1 - Bottom CPU edge
10uF x 5 - Bottom CPU edge
1uF x 5 - Under CPU

VCCQ[1..2] — AM28, AN26

+1.5V_VCCDQ — RU125 0_0603_5%~D — CU137 1U_0402_6.3V6K~D

VDDQ_SENSE — BC43

VSS_SENSE_VDDQ — BA43

VCCSA_SENSE — U10 — VCCSA_SENSE <59>

VCCSA_VID[0] — D48 — VCCSA_VID0 <59>

VCCSA_VID[1] — D49 — VCCSA_VID1 <59>

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.85 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

+1.5V_CPU_VDDQ Source

+1.5V — QU5 AO4728L_SO8 — +1.5V_CPU_VDDQ

+VSBP — RU108 100K_0402_5%~D — RUN_ON_CPU1.5VS3 — QU6B 2N7002DWH_SOT363-6 — RU111 330K_0402_5% — CU136 0.1U_0402_25V6K~D

+3VALW — RU110 100K_0402_5%~D

RU112 0_0402_5%~D — <8,38,58> CPU1.5V_S3_GATE

@RU113 0_0402_5%~D — <34,38,56,57,58> SUSP#

QU6A 2N7002DWH_SOT363-6 — RUN_ON_CPU1.5VS3# <8,34>

CU155 .1U_0402_16V7K @

IVY-BRIDGE_BGA1023~D

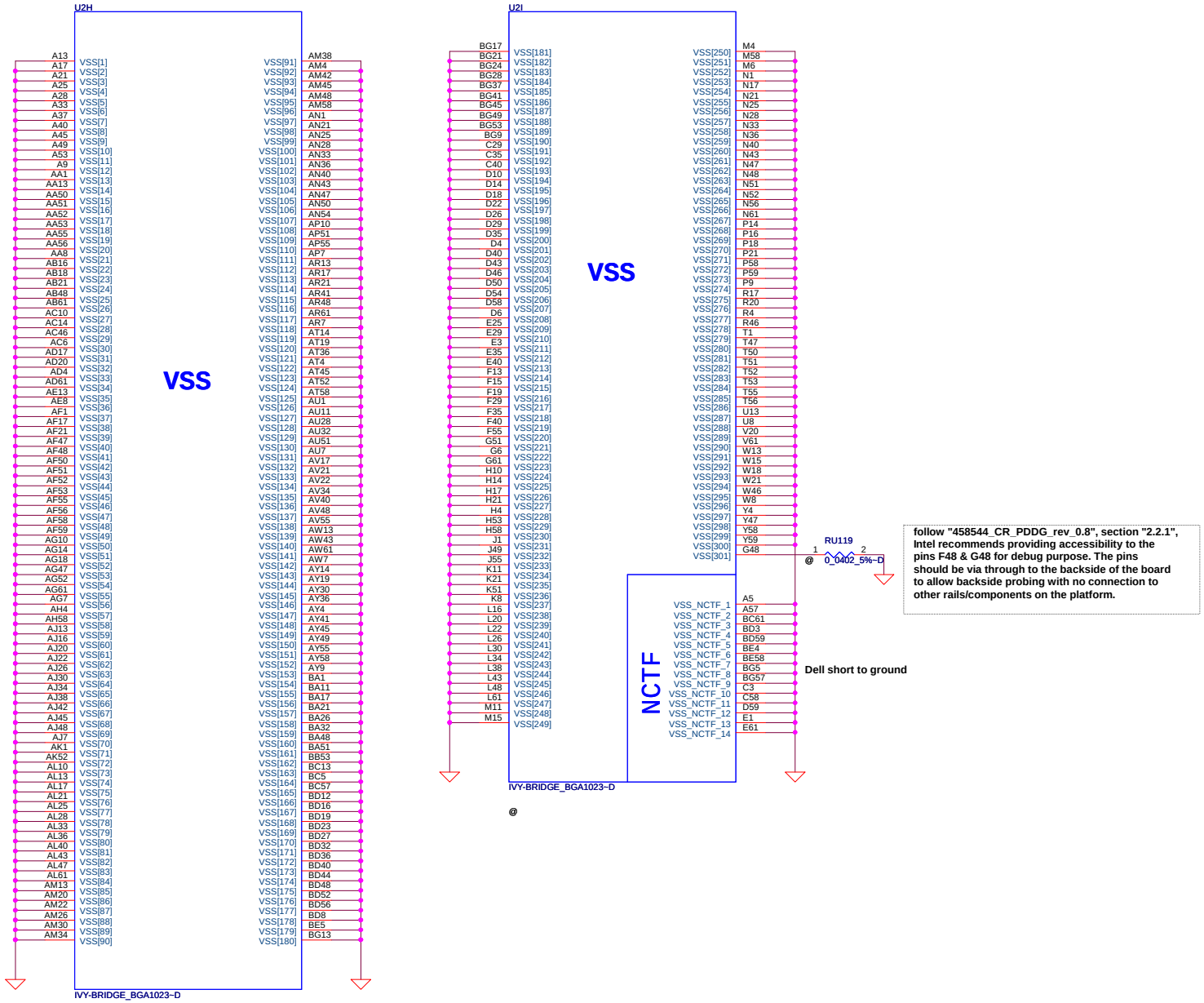
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 12 of 65



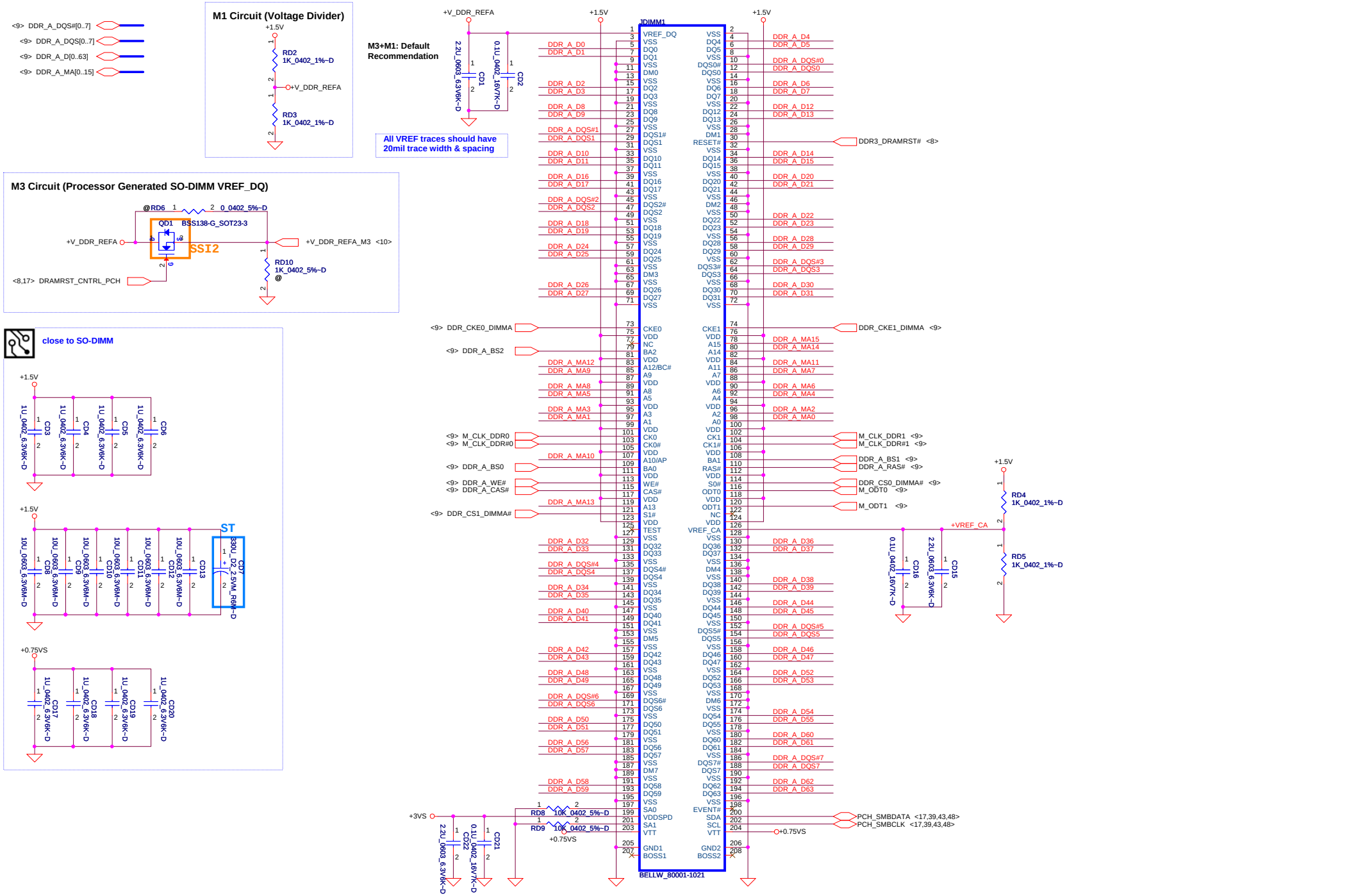
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 13 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size	Document Number	Rev
	LA-7841P	0.3

Date: Tuesday, February 07, 2012 | Sheet 14 of 65

intent to blank

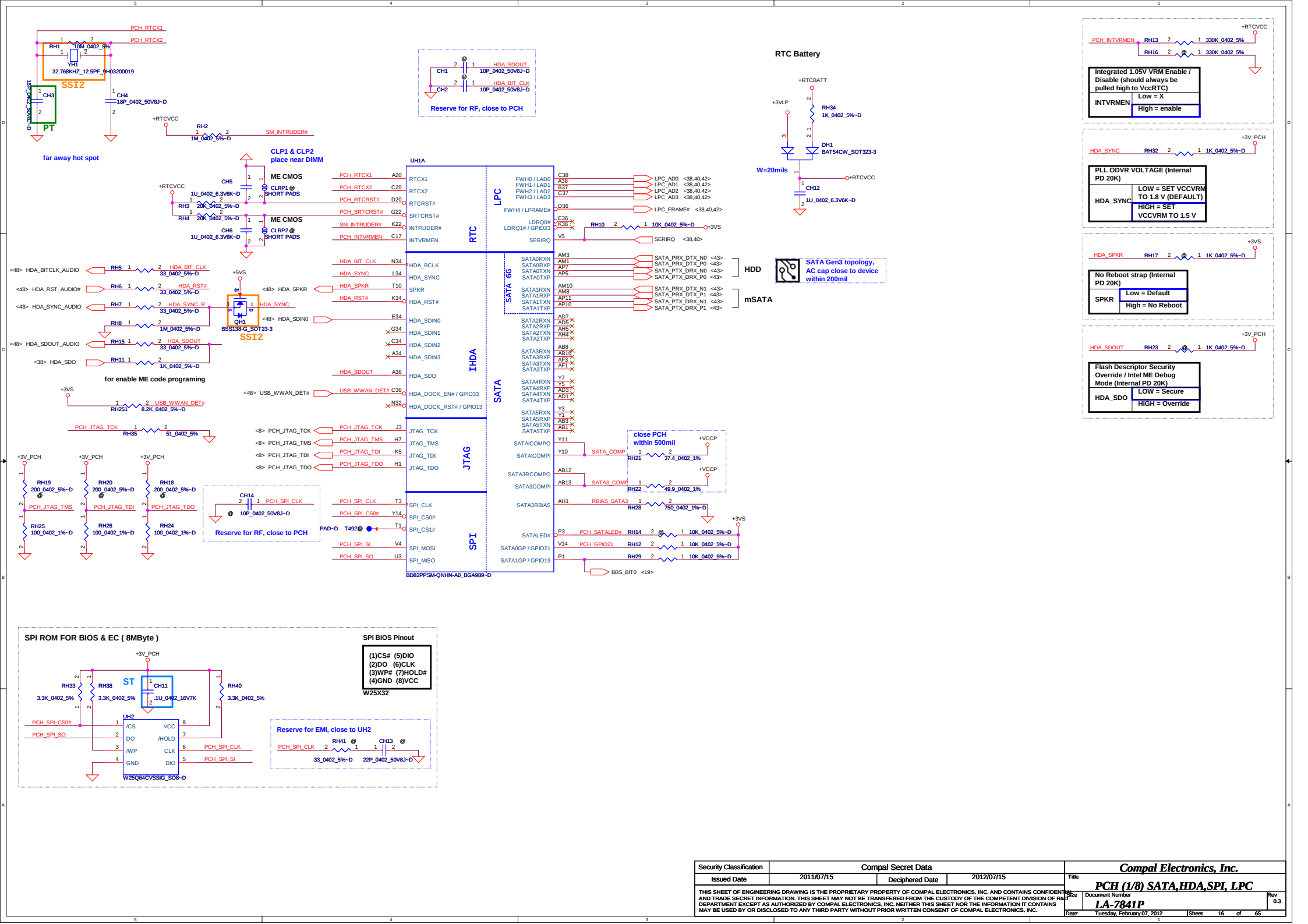
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

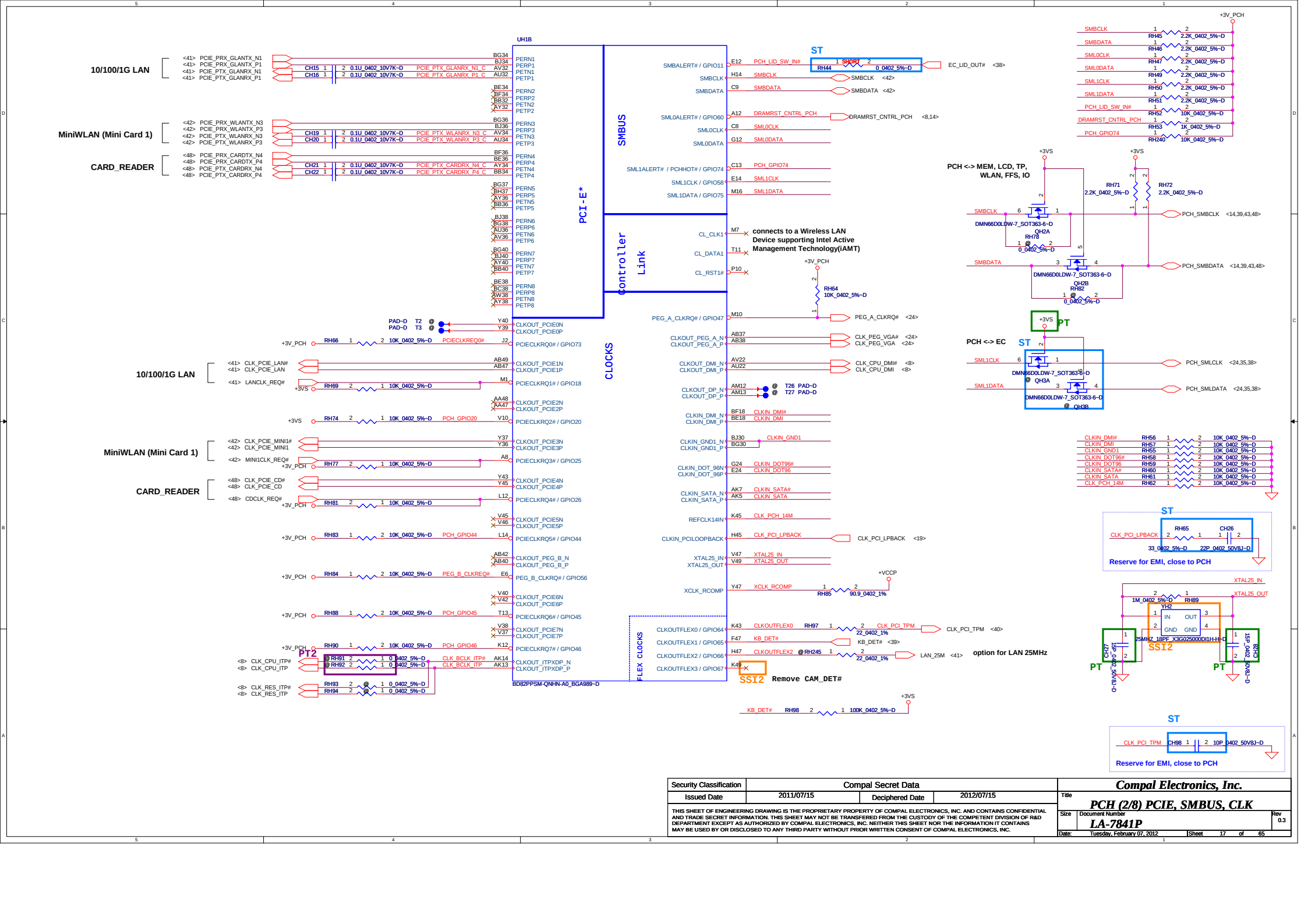
Size | Document Number: **LA-7841P** | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 15 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.	
Title	PCH (1/8) SATA,HDA,SPI, LPC
Size	Document Number: LA-7841P
Rev	0.3
Date: Tuesday, February 07, 2012	Sheet 16 of 65



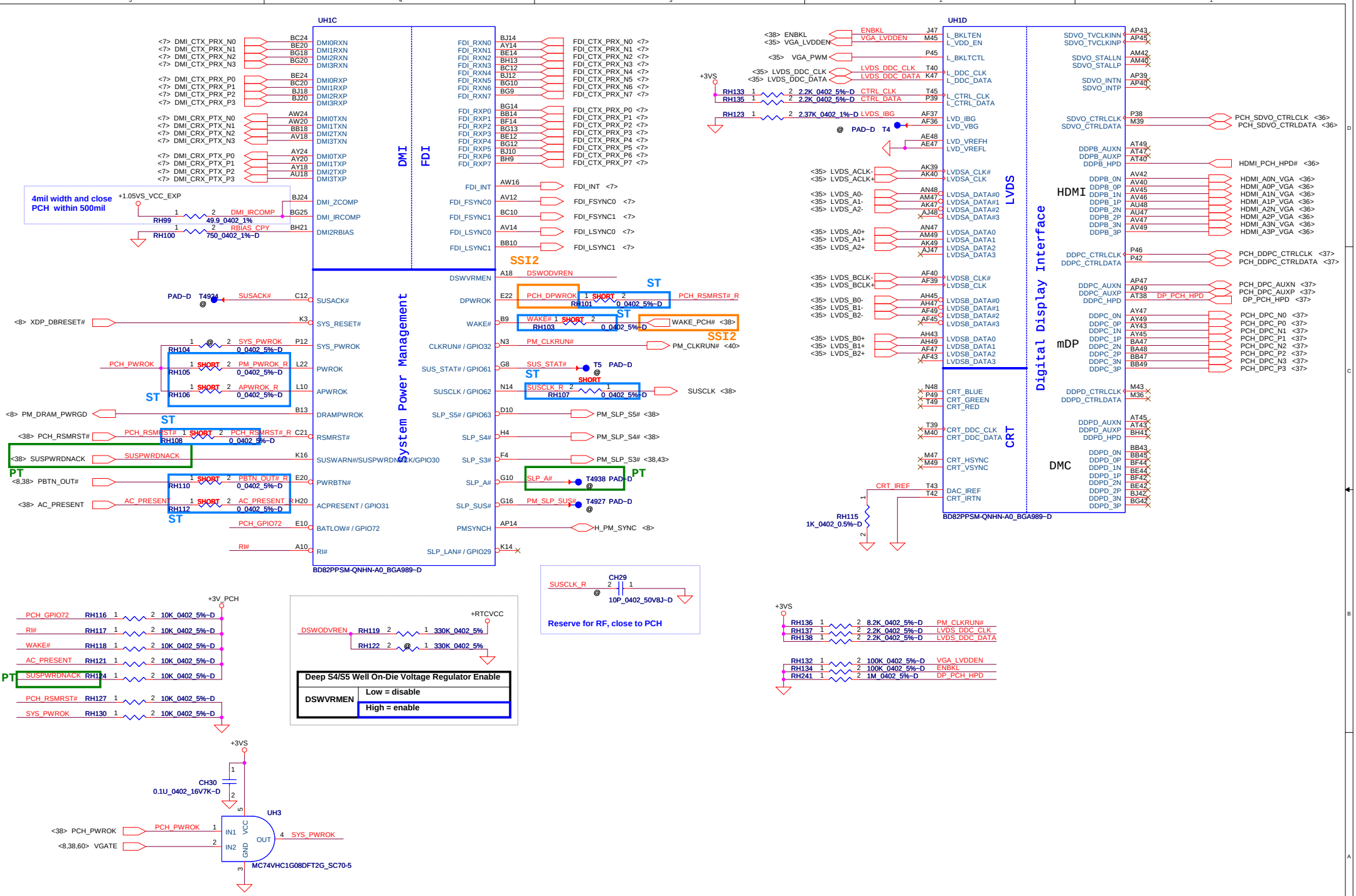
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
	LA-7841P	0.3

Date: Tuesday, February 07, 2012 | Sheet 17 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 18 of 65

RH242 1 @ 2 1K_0402_5%~D BBS_BIT0 <16>
RH244 1 @ 2 BBS_BIT1 1K_0402_5%~D

Boot BIOS Strap (Both internal PU 20K)		
BIT 1	BIT 0	Boot BIOS Location
GNT1#	SATA1GP	
0	0	LPC
0	1	Reserved
1	0	PCI(non-mobile)
1	1	SPI

RH243 1 @ 2 WL_OFF# 1K_0402_5%~D

A16 Top-Block Swap Override (Internal PU 20K)	
GNT3#	Low = swap enabled
	High = Default

UH1E

RSVD1 AY7
RSVD2 AV7
RSVD3 AU3
RSVD4 BG4
RSVD5 AT10
RSVD6 BC8
RSVD7 AU2
RSVD8 AT4
RSVD9 AT3
RSVD10 AT1
RSVD11 AY3
RSVD12 AT5
RSVD13 AV3
RSVD14 AV1
RSVD15 BB1
RSVD16 BA3
RSVD17 BB5
RSVD18 BB3
RSVD19 BB7
RSVD20 BB8
RSVD21 BD4
RSVD22 BF6
RSVD23 AV5 NV_ALE
RSVD24 AV10
RSVD25 AT8
RSVD26 AY5
RSVD27 BA2
RSVD28 AT12
RSVD29 BF3

BG26 TP1
BJ26 TP2
BH25 TP3
BJ16 TP4
BG16 TP5
AH38 TP6
AH37 TP7
AK43 TP8
AK45 TP9
C18 TP10
N30 TP11
H3 TP12
AH12 TP13
AM4 TP14
AM5 TP15
Y13 TP16
K24 TP17
L24 TP18
AB46 TP19
AB45 TP20
B21 TP21
M20 TP22
AY16 TP23
BG46 TP24

RH139 1 @ 2 1K_0402_5%~D +1.8VS

Intel Anti-Theft Techonlogy	
NV_ALE	Low = disable
	High = enable

+3VS

RPH1
8 1 PCI_PIRQA#
7 2 PCI_PIRQB#
6 3 PCI_PIRQD#
5 4 PCI_PIRQC#
8.2K_0804_8P4R_5%

RPH2
8 1 DGPU_HOLD_RST#
7 2 PCH_GPIO52
6 3 DGPU_PWR_EN#
5 4 WL_OFF#
8.2K_0804_8P4R_5%

RPH3
8 1 FFS_INT1
7 2 ODD_DA#
6 3 PCH_GPIO5
5 4
8.2K_0804_8P4R_5%

USB Conn 1
USB Conn 2 (Power Share)

<44> USB3RN1 BE28 USB3Rn1
<45> USB3RN2 BC30 USB3Rn2
BE32 USB3Rn3
BJ32 USB3Rn4
<44> USB3RP1 BC28 USB3Rp1
<45> USB3RP2 BE30 USB3Rp2
BF32 USB3Rp3
BG32 USB3Rp4
<44> USB3TN1 AV26 USB3Tn1
<45> USB3TN2 BB26 USB3Tn2
AU28 USB3Tn3
AY30 USB3Tn4
<44> USB3TP1 AU26 USB3TP1
<45> USB3TP2 AY26 USB3Tp2
AV28 USB3Tp3
AW30 USB3Tp4

USBP0N C24 USB20_N0 <44>
USBP0P A24 USB20_P0 <44>
USBP1N C25 USB20_N1 <45>
USBP1P B25 USB20_P1 <45>
USB Conn 1
USB Conn 2 (Power Share)
USBP2N C26
USBP2P A26
USBP3N K28
USBP3P H28
USBP4N E28
USBP4P D28 USB20_N4 <42>
USBP5N C28 USB20_P4 <42>
USBP5P A28 USB20_N5 <48>
USBP5P C29 USB20_P5 <48>
Mini Card(WLAN)
Mini Card(WWAN)
USBP6N B29
USBP6P N28
USBP7N M28
USBP7P L30
USBP8N K30
USBP8P G30
USBP9N E30
USBP9P C30
USBP10N A30
USBP10P L32
USBP11N K32
USBP11P G32
USBP12N E32 USB20_N12 <35>
USBP12P C32 USB20_P12 <35>
USBP13N A32
Camera
USBRBIAS# C33 USBRBIAS
USBRBIAS B33

Within 500 mils
RH143 1 2 22.6_0402_1%

PCI_PIRQA# K40 PIRQA#
PCI_PIRQB# K38 PIRQB#
PCI_PIRQC# H38 PIRQC#
PCI_PIRQD# G38 PIRQD#
DGPU_HOLD_RST# C46
PCH_GPIO52 C44 REQ1# / GPIO50
DGPU_PWR_EN# E40 REQ2# / GPIO52
REQ3# / GPIO54
REQ[1:3]# & GNT[1:3]# are used as GPIO on Mobile
GNT[1:3]# have internal weak PU, and disable after PLTRST# deassert
BBS_BIT1 D47 GNT1# / GPIO51
EN_CAM E42 GNT2# / GPIO53
<35> EN_CAM
<42> WL_OFF# WL_OFF# F46 GNT3# / GPIO55
<43> FFS_INT1 FFS_INT1 G42 PIRQE# / GPIO2
ODD_DA# G40 PIRQF# / GPIO3
<37> DP_CBL_DET C42 PIRQG# / GPIO4
PCH_GPIO5 D44 PIRQH# / GPIO5
PAD~D T6 @ K10 PME#
PCH_PLTRST# C6 PLTRST#

OC0# / GPIO59 A14 USB_OC0#
OC1# / GPIO40 K20 USB_OC1#
OC2# / GPIO41 B17 USB_OC2#
OC3# / GPIO42 C16 USB_OC3#
OC4# / GPIO43 L16 USB_OC4#
OC5# / GPIO9 A16 USB_OC5#
OC6# / GPIO10 D14 USB_OC6#
OC7# / GPIO14 C14 USB_OC7#
USB_OC0# <44>
USB_OC1# <45>

RPH4
USB_OC0# 4 5
USB_OC1# 3 6
USB_OC2# 2 7
USB_OC3# 1 8
10K_1206_8P4R_5%~D
RPH5
USB_OC4# 4 5
USB_OC5# 3 6
USB_OC6# 2 7
USB_OC7# 1 8
10K_1206_8P4R_5%~D

<17> CLK_PCI_LPBACK RH144 2 1 22_0402_5% CLK_PCI0 H49 CLKOUT_PCI0
<38> CLK_PCI_LPC RH145 1 2 22_0402_5% CLK_PCI1 H43 CLKOUT_PCI1
<42> CLK_LPC_DEBUG RH252 1 2 22_0402_5% CLK_LPC_DEBUG H48 CLKOUT_PCI2
PAD~D T8 @ CLK_PCI3 K42 CLKOUT_PCI3
PAD~D T9 @ CLK_PCI4 H40 CLKOUT_PCI4

BD82PPSM-QNHN-A0_BGA989~D

+3VS
RH247 2 1 10K_0402_5%~D DIS@
<33,61> DGPU_PWR_EN
CH99 0.01U_0402_16V7K~D DIS@
SSI2
DGPU_PWR_EN#
QH6 DIS@ ME2N7002D-G_SOT23-3
ST

ST CH31 2 1 10P_0402_50V8J~D CLK_PCI1
Reserve for RF, close to PCH

CH100 1 2 CLK_LPC_DEBUG
@ 27P_0402_50V8J

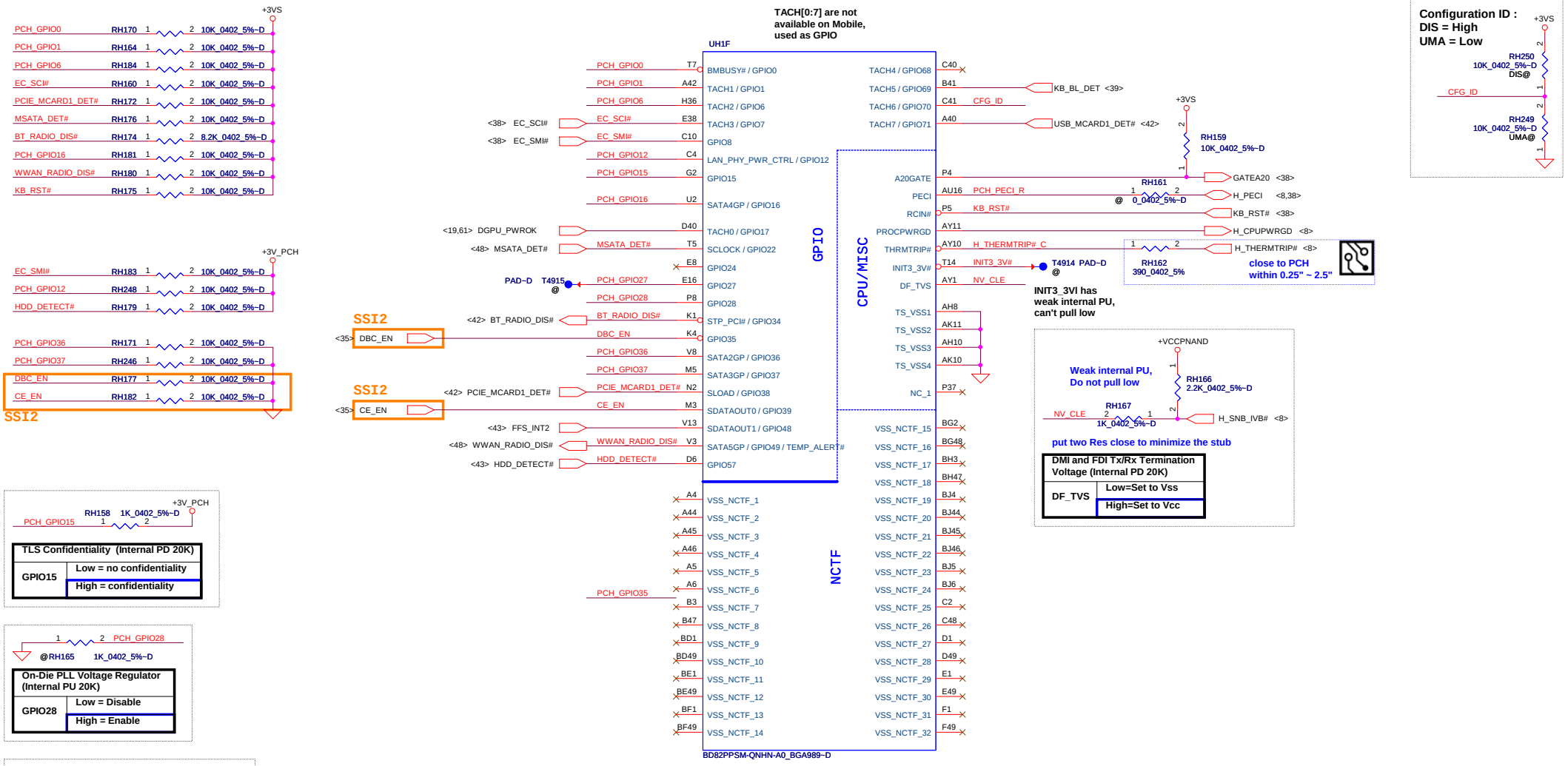
+3V_PCH

RH148 1 @ 2 0_0402_5%~D
+3V_GPU
RH149 1 @ 2 0_0402_5%~D
+3VS
<24> PLTRST_VGA#
<8,38,40,41,42,48> PLT_RST#
PCH_PLTRST#
RH155 100K_0402_5%~D
UH5 SN74AHC1G08DCKR_SC70-5
RH157 @ 10K_0402_5%~D
UH4 DIS@ SN74AHC1G08DCKR_SC70-5
RH154 DIS@ 100K_0402_5%~D
PT
RH151 @ 0_0402_5%~D DGPU_PWROK <20,61>
RH152 DIS@ 0_0402_5%~D PCH_PLTRST#
RH156 DIS@ 100K_0402_5%~D DGPU_HOLD_RST#
PT

Switchable Graphics

Signal	GPIO	Type	DuringReset	After Reset	Usage	Description
DGPU_PWR_EN#	GPIO54	Output	High	High	Must have	Driven by Switchable Graphics Driver to turn on/off the discrete graphics power. 0 = dGPU power switch turned on 1 = Power switch turned off
DGPU_PWROK	GPIO17	Input	-	-	Must have	Driven by dGPU VR to indicate the power status to PCH. Used to enable clocks to dGPU. 0 = dGPU power is not stable. Keep clock disabled & reset asserted. 1 = dGPU power is stable. Clock can be enabled; reset can be deasserted If DGPU_PRSNT# is 1, in-order to get regular discrete GFX cards working, program DGPU_PWROK as GPO and assert a high value (1) on the pin.
DGPU_HOLD_RST#	GPIO50	Output	Low	Low	Must have	Discrete Graphics Enable signal. Controlled by Switchable Graphics Driver and driven by PCH GPIO. Used to gate with Platform Reset to enable the Reset for dGPU. 0 = Keep dGPU in reset. 1 = Reset is released. This action taken 100 ms after DGPU_PWROK to ensure clock is stable.

Compal Electronics, Inc.
Title: PCH (4/8) PCI, USB, NVRAM
Size: Document Number: LA-7841P Rev: 0.3
Date: Tuesday, February 07, 2012 Sheet 19 of 65

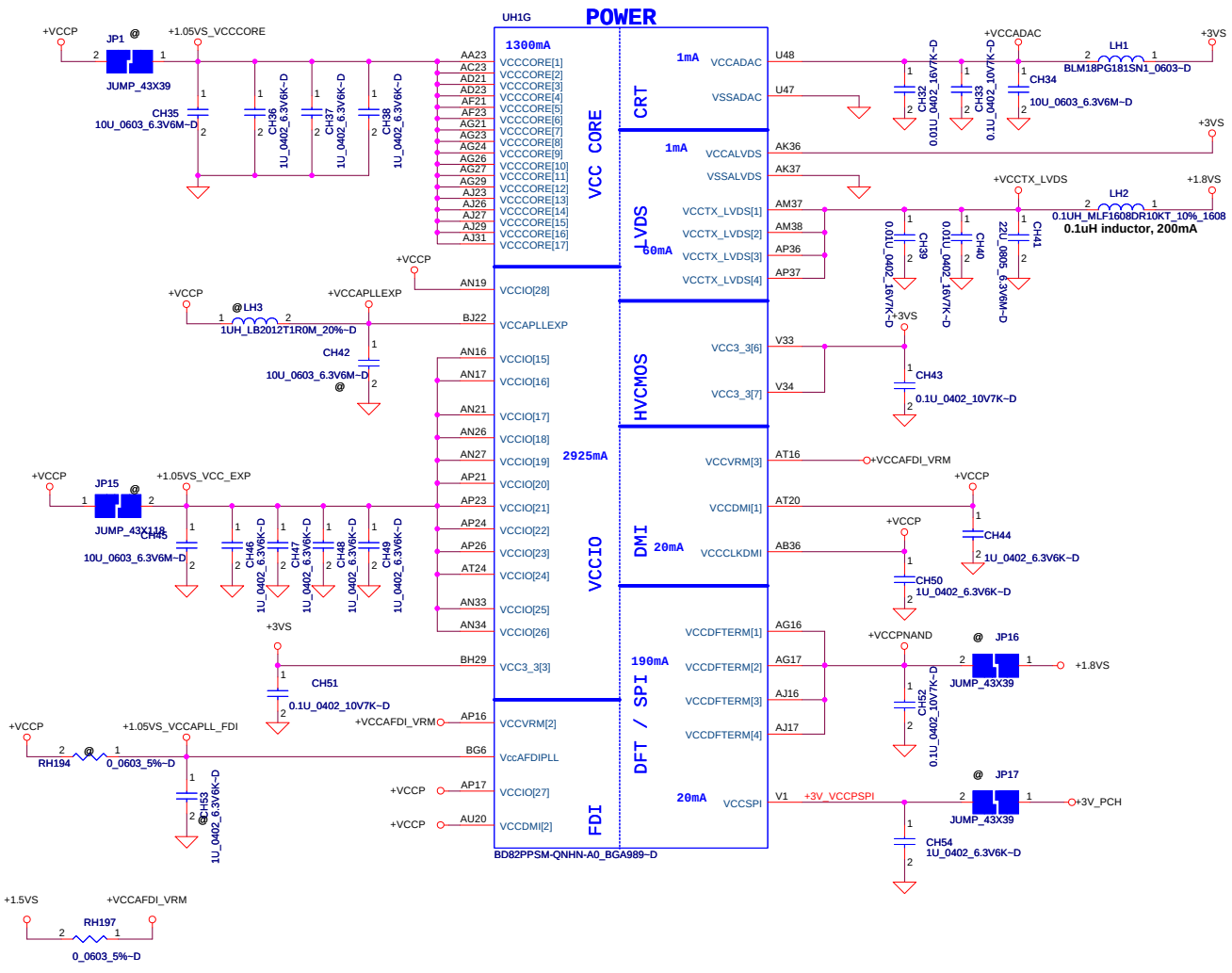


Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 20 of 65



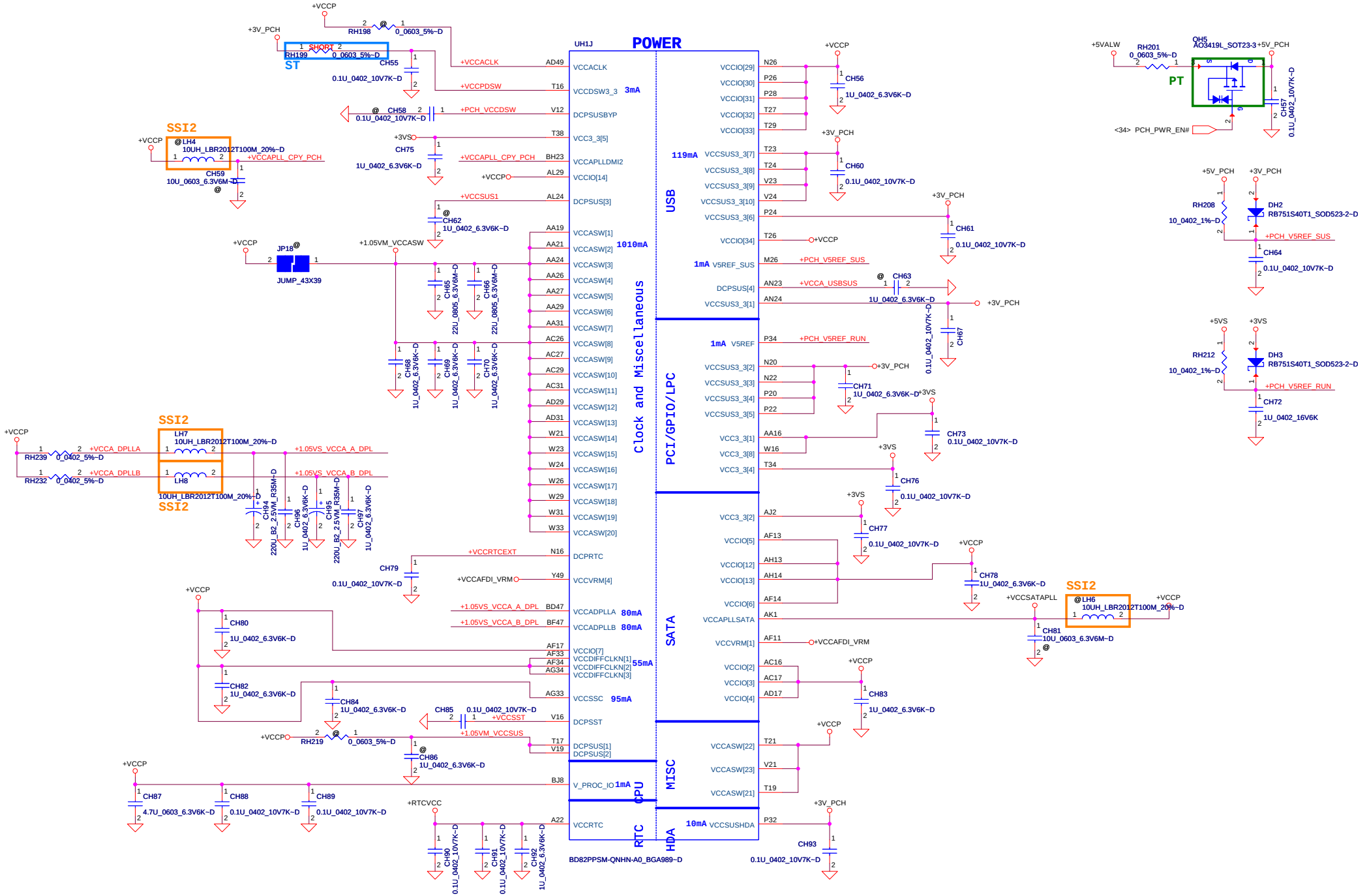
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 21 of 65



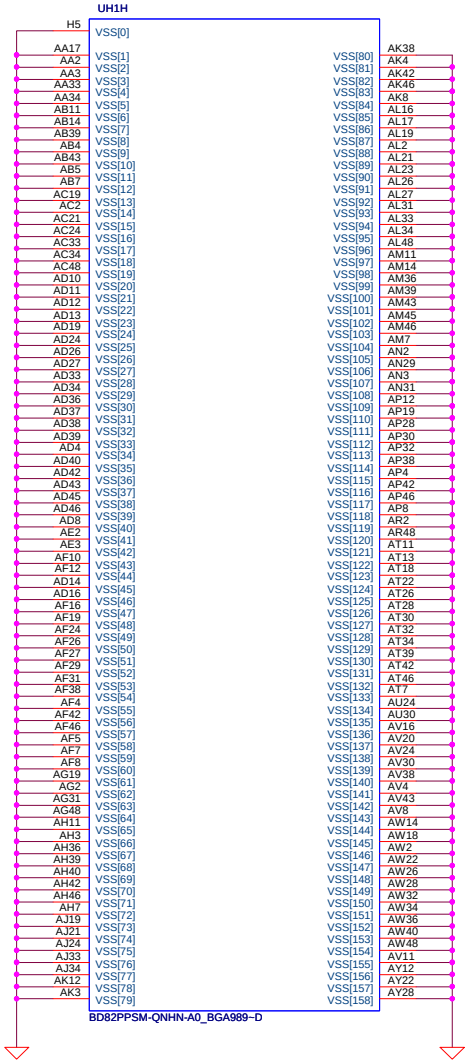
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

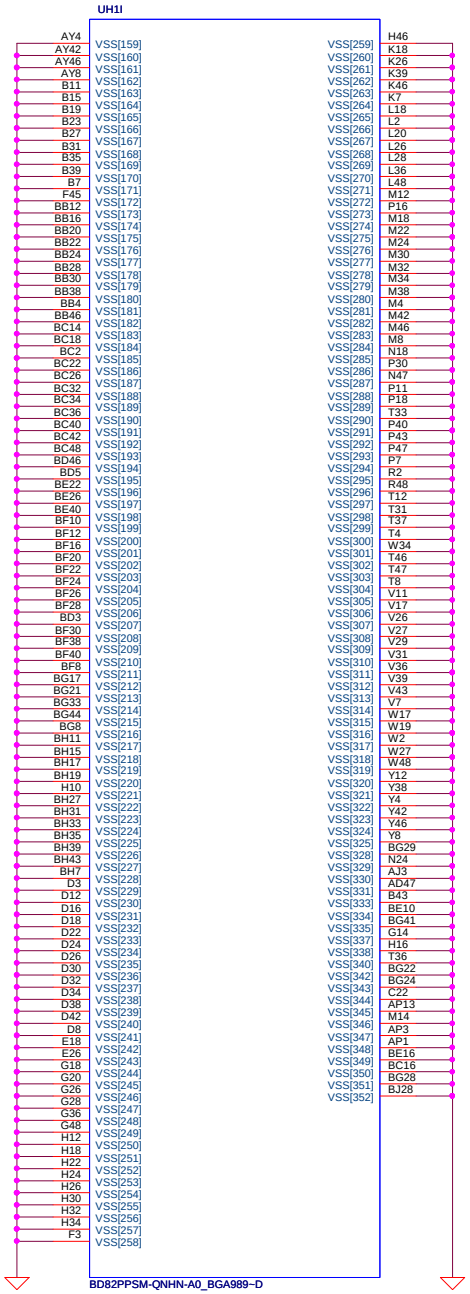
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size	Document Number	Rev
	LA-7841P	0.3

Date: Tuesday, February 07, 2012 Sheet 22 of 65





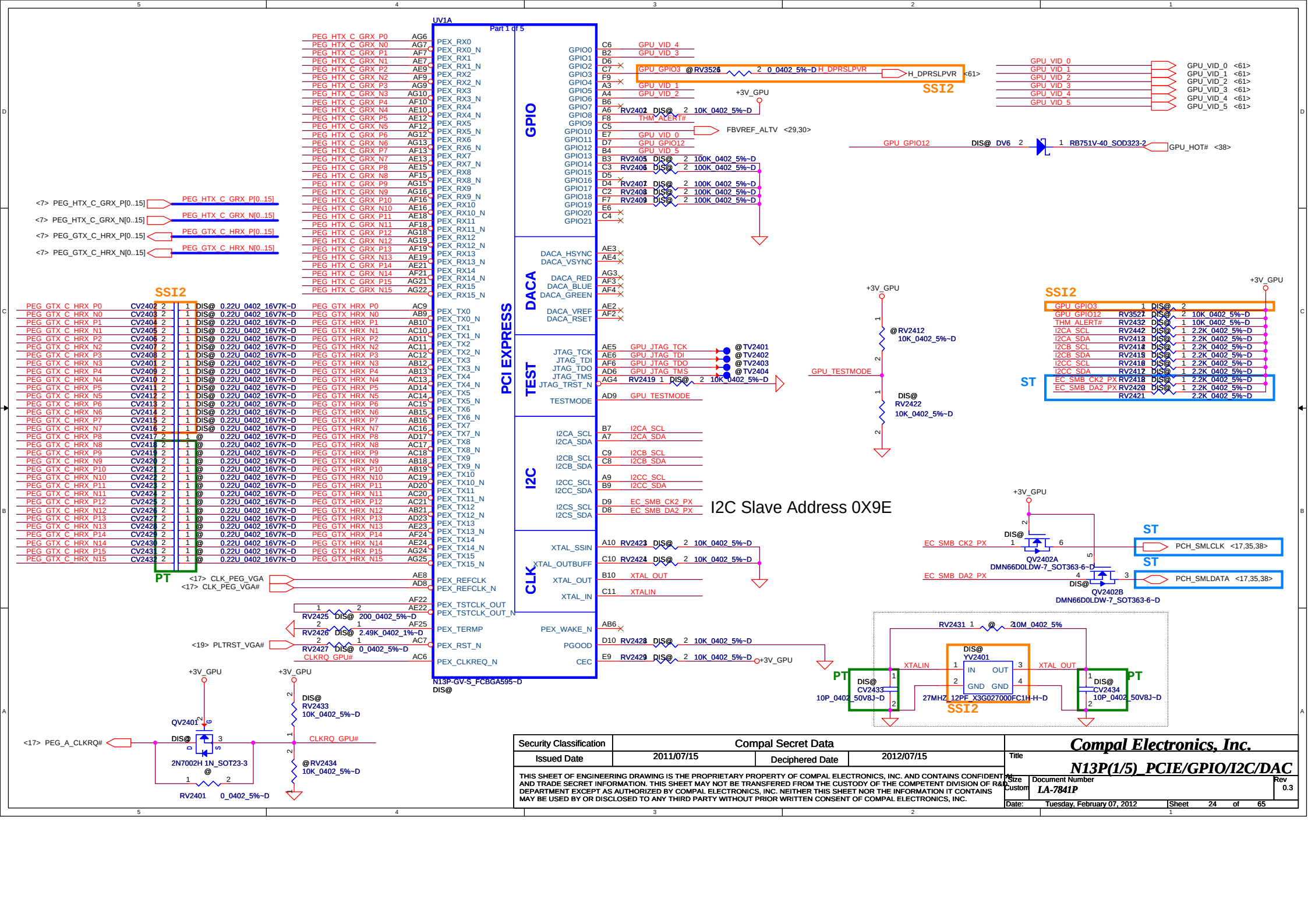
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size | Document Number: **LA-7841P** | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 23 of 65



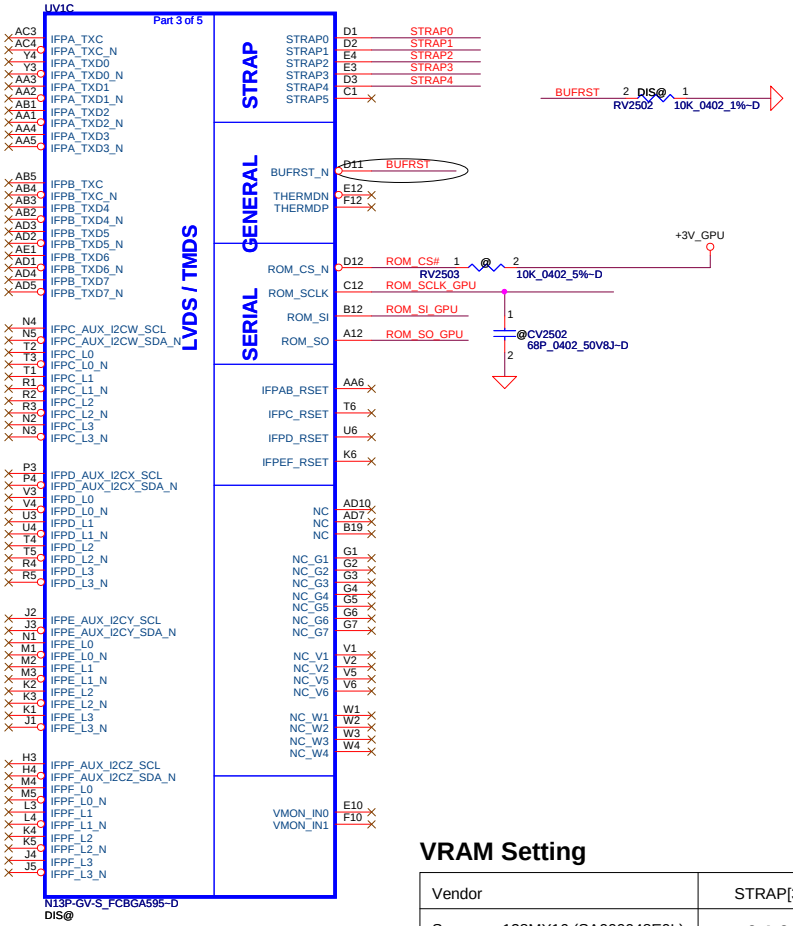
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **N13P(1/5)_PCIE/GPIO/I2C/DAC**

Size	Document Number	Rev
Custom	LA-7841P	0.3

Date: Tuesday, February 07, 2012 | Sheet 24 of 65



VRAM Setting

Vendor	STRAP[3:0]
Samsung 128MX16 (SA000048E0L)	**0 1 0 1**
Hynix 128MX16 (SA00004GD0L)	**0 1 0 0**

PT

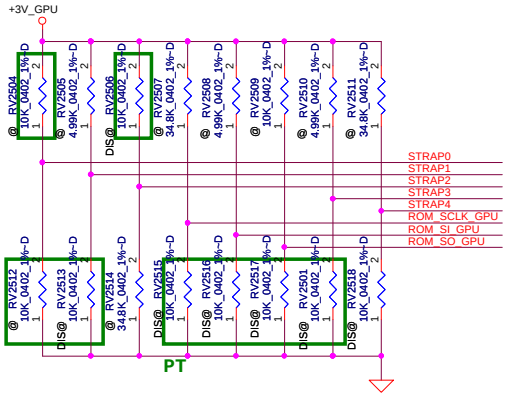
SAMSUNG RV2504 10K_0402_1%~D X76_SAM@

HYNIX RV2512 10K_0402_1%~D X76_HYN@

GPU BIOS Device ID

N13P-GV-S-A2	**0x1140**

PT



Binary Mode Straps

STRAP Pin Name	STRAP Mapping	Resistance	Polarity
STRAP0	RAM_CFG[0]	10K Ohm	For Hynix Pull-down 10K ohm to GND, Samsung pull-high 10K ohm to 3.3V
STRAP1	RAM_CFG[1]	10K Ohm	Pull-down 10K ohm to GND
STRAP2	RAM_CFG[2]	10K Ohm	Pull-up 10K ohm to +3V_GPU
STRAP3	RAM_CFG[3]	10K Ohm	Pull-down 10K ohm to GND
STRAP4	PCIE_MAX_SPEED	10K Ohm	Pull-down 10K ohm to GND
ROM_SCLK	SMB_ALT_ADDR	10K Ohm	Pull-down 10K ohm to GND
ROM_SI	SUB_VENDOR	10K Ohm	Pull-down 10K ohm to GND
ROM_SO	VGA_DEVICE	10K Ohm	Pull-down 10K ohm to GND

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: N13P(2/5)_LVDS/HDMI/DP/STRP

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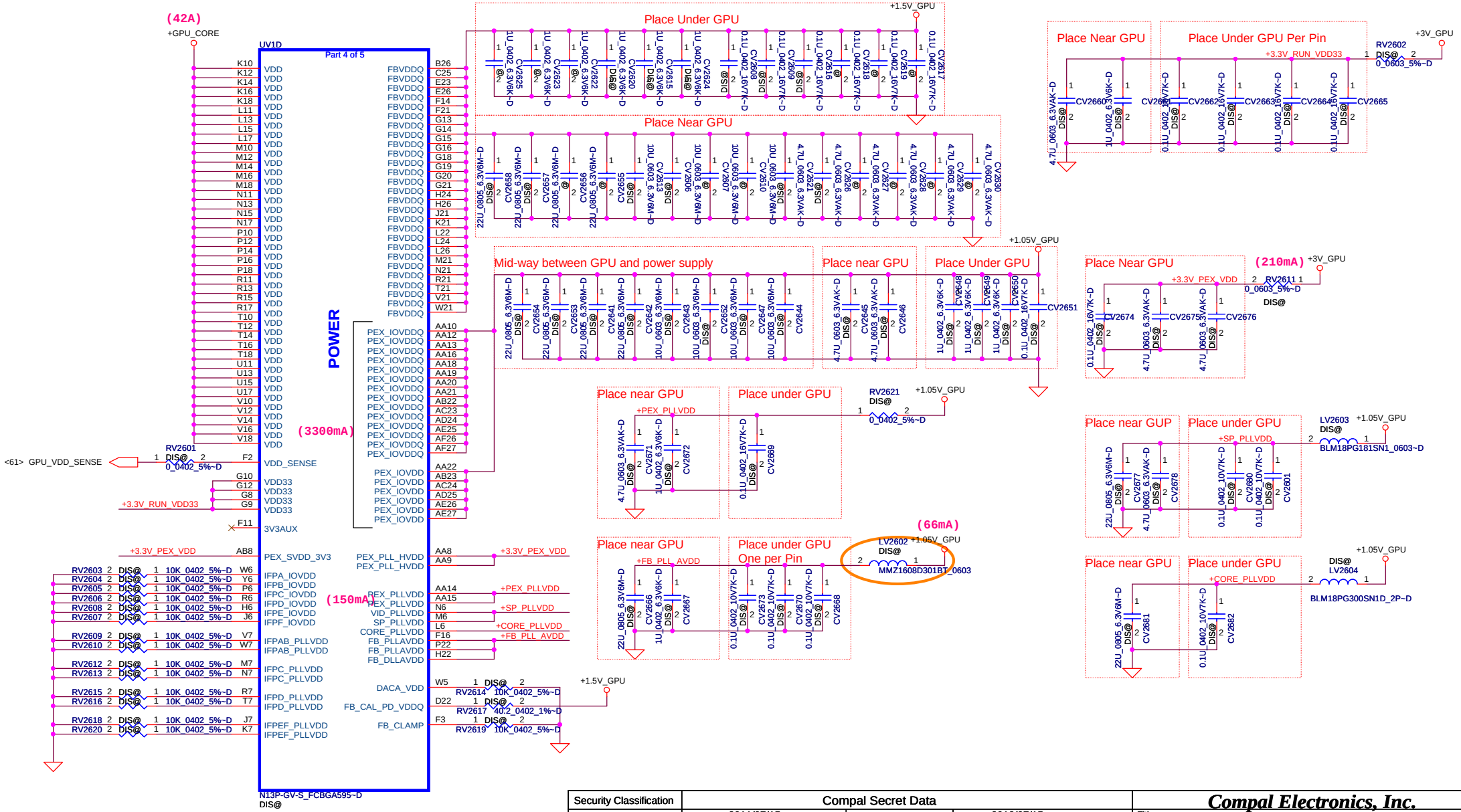
(42A)
+GPU_CORE
UV1D
Part 4 of 5
POWER
(3300mA)
(150mA)
N13P-GV-S_FCBGA595~D
DIS@
Place Under GPU
Place Near GPU
Place Under GPU Per Pin
Mid-way between GPU and power supply
Place near GPU
Place Under GPU
Place near GUP
Place under GPU
Place under GPU One per Pin
(66mA)
(210mA)
+1.5V_GPU
+3V_GPU
+1.05V_GPU
+3.3V_RUN_VDD33
+3.3V_PEX_VDD
+PEX_PLLVDD
+SP_PLLVDD
+CORE_PLLVDD
+FB_PLL_AVDD
<61> GPU_VDD_SENSE
VDD_SENSE
3V3AUX
RV2601
RV2602
RV2603
RV2604
RV2605
RV2606
RV2608
RV2607
RV2609
RV2610
RV2612
RV2613
RV2615
RV2616
RV2618
RV2620
RV2614
RV2617
RV2619
RV2621
RV2611
LV2602
LV2603
LV2604
MMZ1608D301BT_0603
BLM18PG181SN1_0603~D
BLM18PG300SN1D_2P~D
Security Classification
Compal Secret Data
Issued Date
2011/07/15
Deciphered Date
2012/07/15
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Title
N13P(3/5)_POWER
Size
Custom
Document Number
LA-7841P
Rev
0.3
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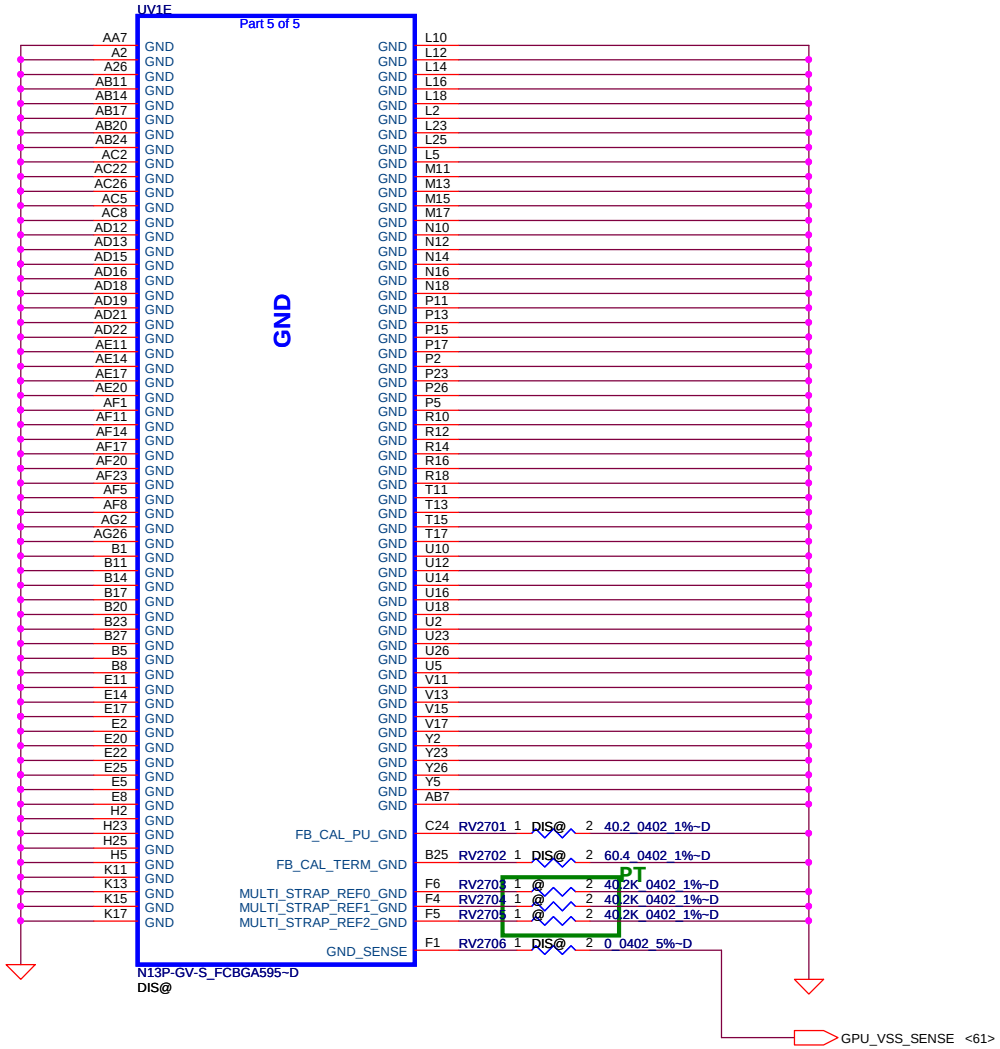

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Compal Electronics, Inc.

Title: **N13P(4/5)_GND**

Size	Document Number	Rev
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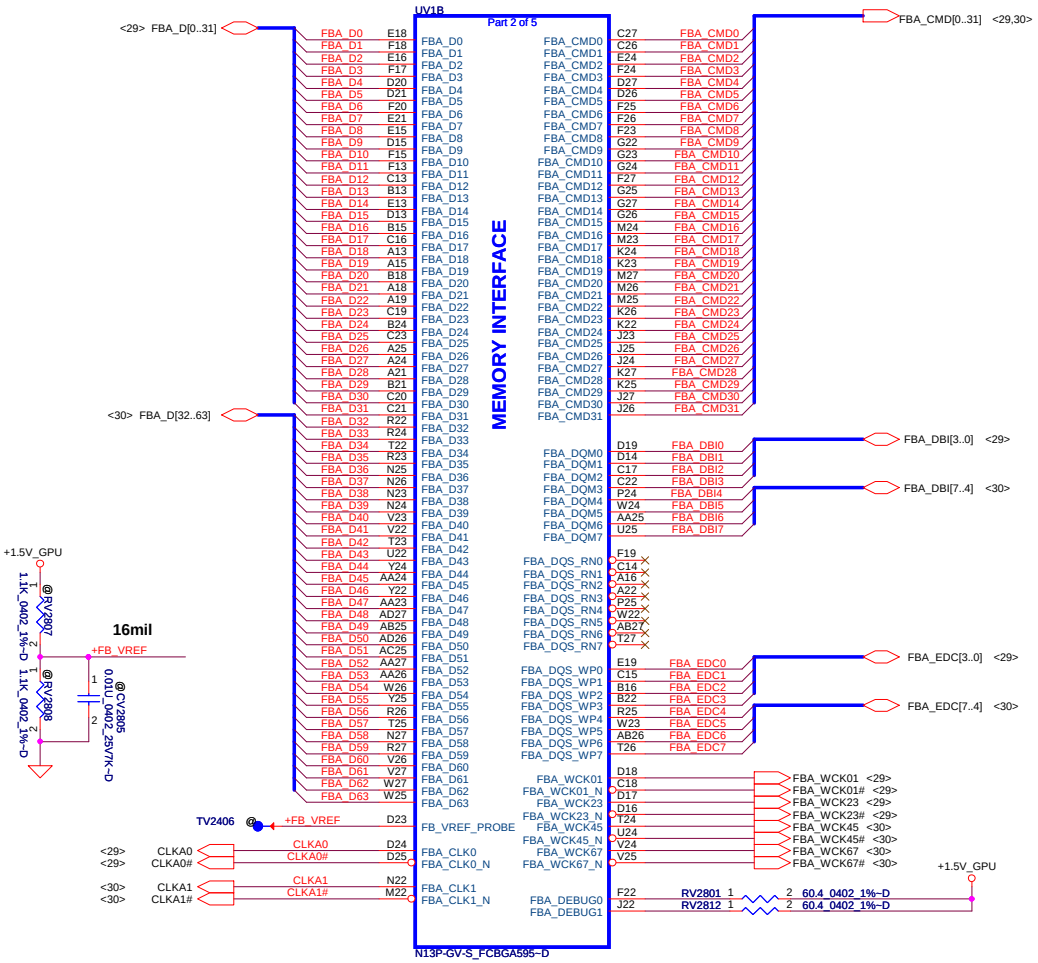

Mode H - Command Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS#	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

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Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: N13P(5/5)_MEMORY INTERFACE

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Memory Partition A - Lower 32 bits

128X16 GDDR5

NORMAL

MIRROR

PT

SAMSUNG

HYNIX

PCB-MB X76_SAM@

PCB-MB X76_HYN@

One Per pin

PLACE 0.1uF CAPS CLOSEST TO THE MEMORY DEVICES
PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

GDDR5 Mode H Mapping	
GB2-64	Channel 0 0...31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	ABI#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#

DELL CONFIDENTIAL/PROPRIETARY

	123
Title	VRAM A Lower
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Memory Partition A - Upper 32 bits

MIRROR

NORMAL

PT

PT

GDDR5 Mode H Mapping	
GB2-64	Channel 0 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	ABI#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

SAMSUNG

UV7 PCB-MB X76_SAM@

UV6 PCB-MB X76_SAM@

HYNIX

UV7 PCB-MB X76_HYN@

UV6 PCB-MB X76_HYN@

123			
Title: VRAM A Upper			
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Compal Electronics, Inc.

Title: **Block Diagram**

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Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

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Title: **Block Diagram**

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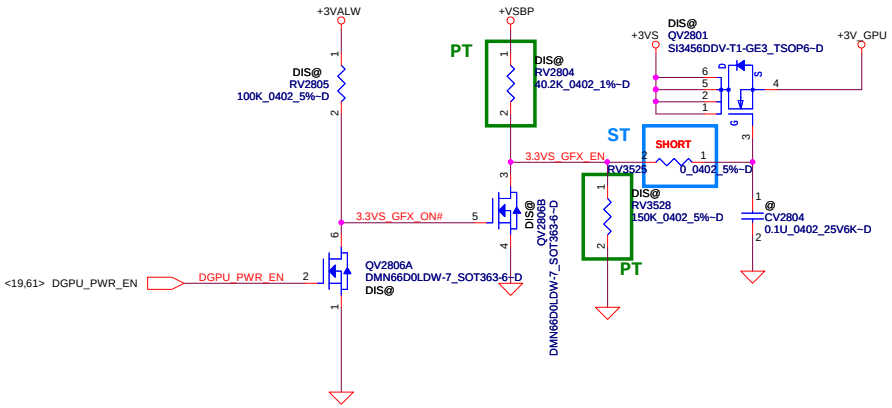
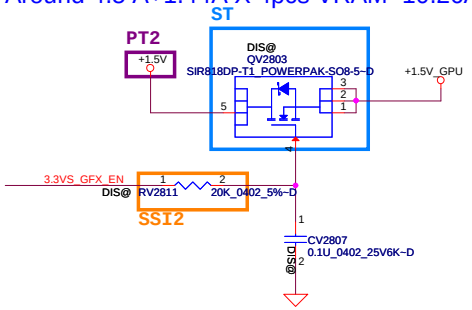
+3VS to +3V_GPU

Around 1.4 A



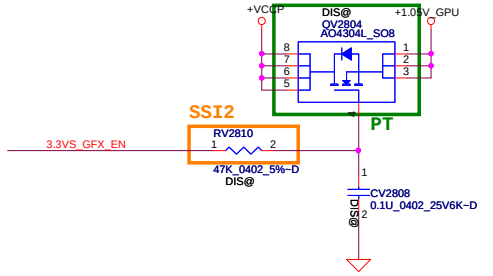
+1.5VS to +1.5V_GPU

Around 4.5 A+1.44A X 4pcs VRAM=10.26A

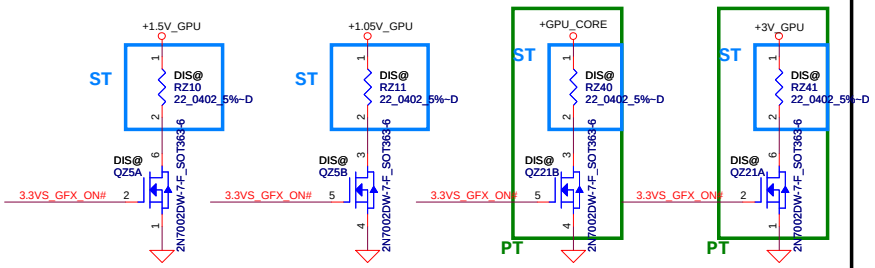


+1.05VS to +1.05V_GPU

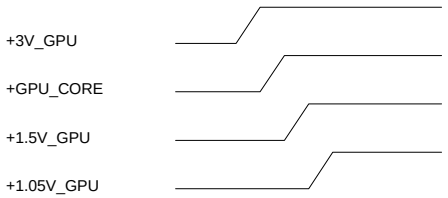
Around 3 A



GPU Power Discharge Path

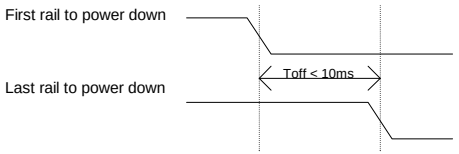


GPU Power Up Power Rail Sequence

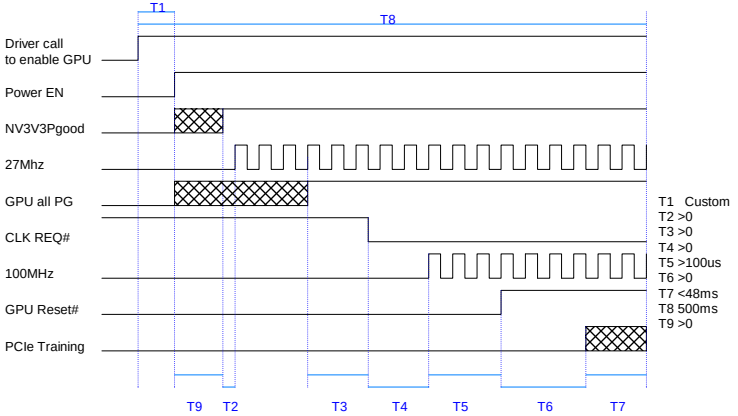


The ramp time for any rail must be more than 40us.

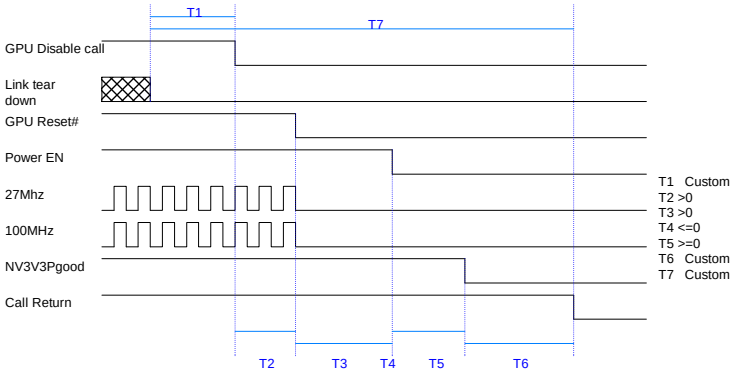
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

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Title: **Block Diagram**

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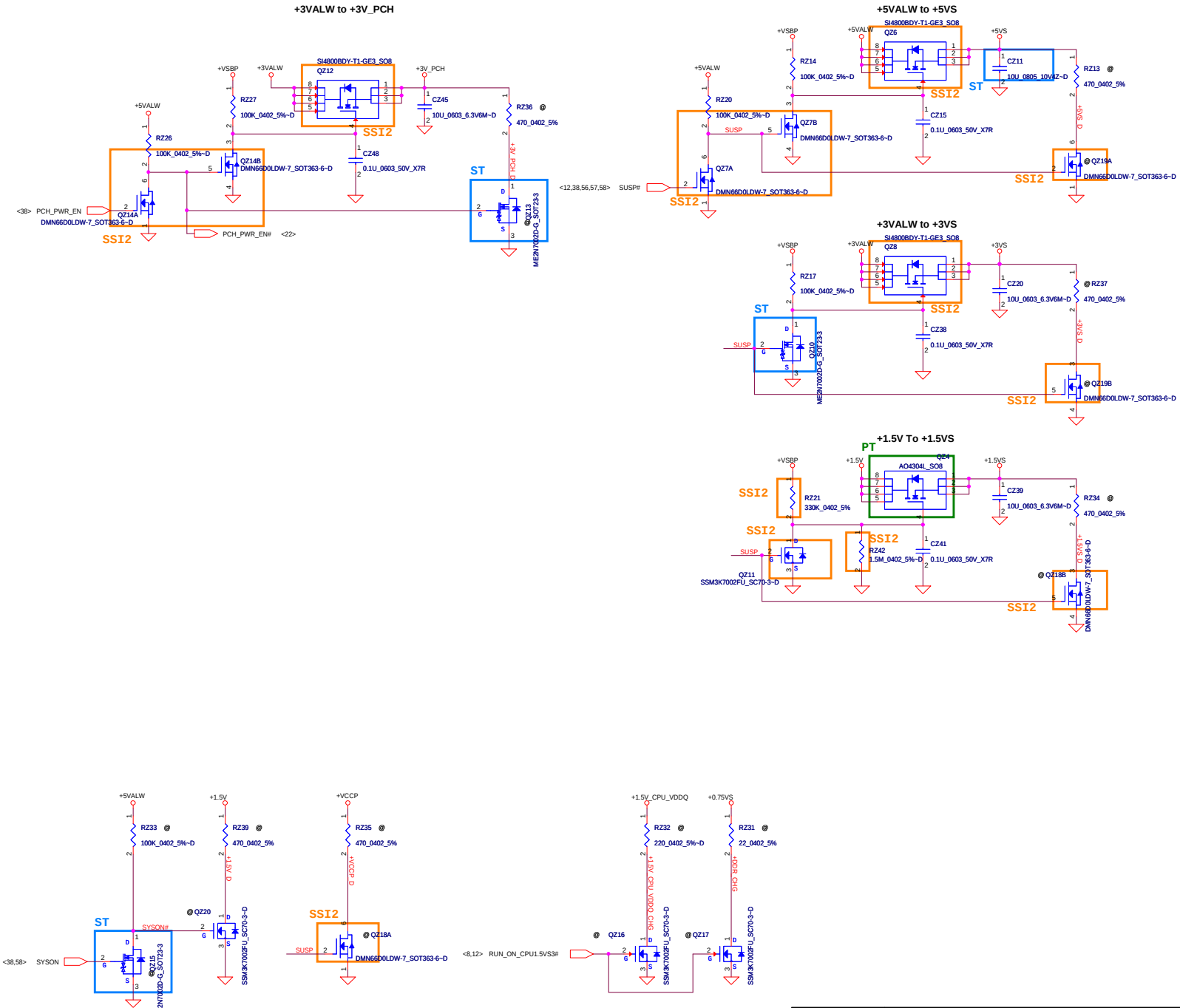

Compal Electronics, Inc.

Title: DC/DC Interface

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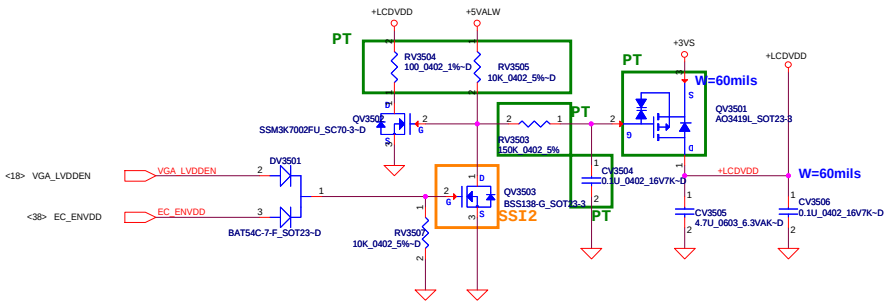
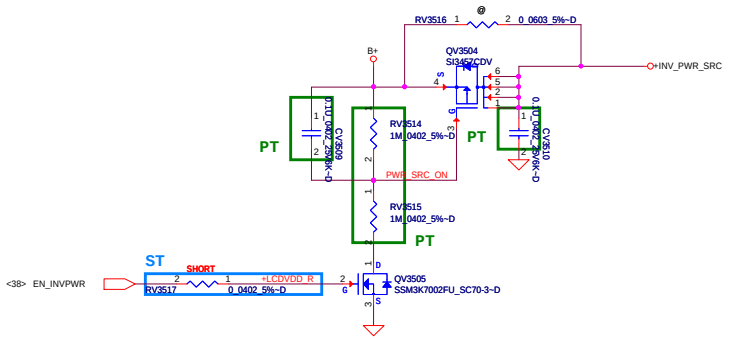
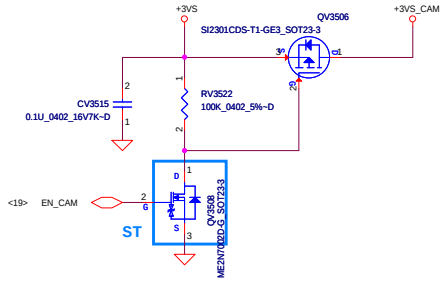
LCD PWR CTRL



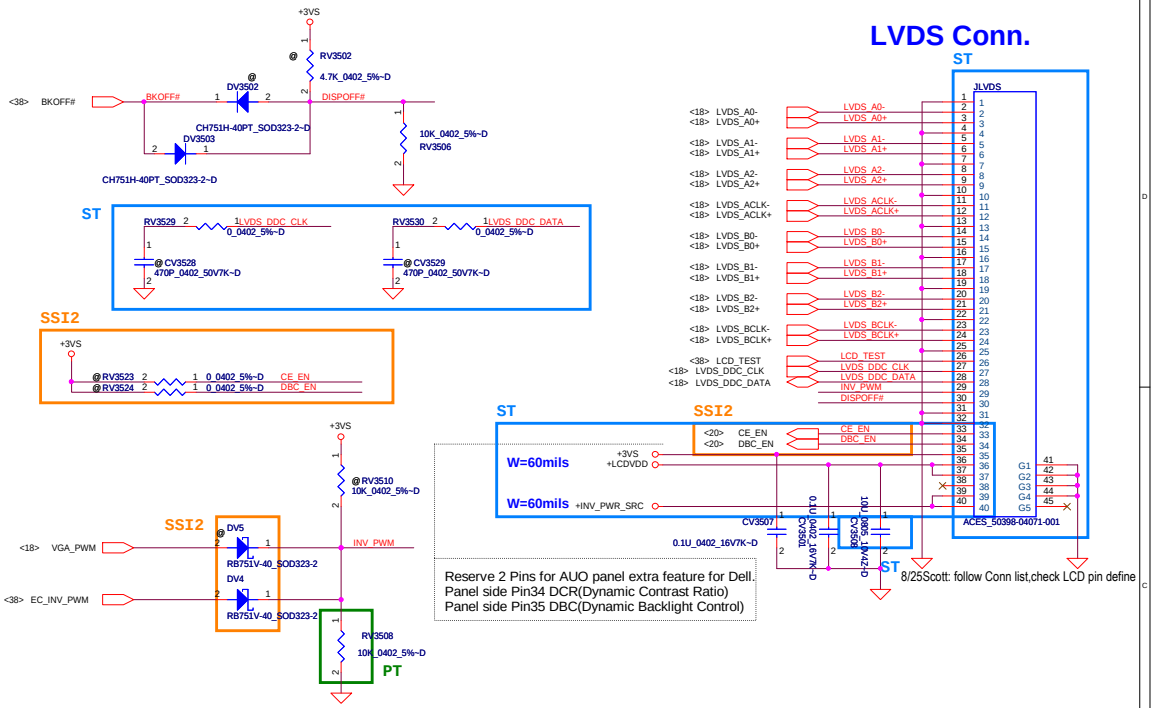
LCD backlight PWR CTRL



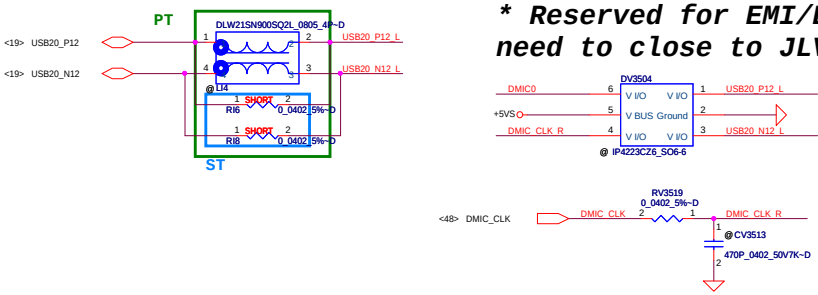
Webcam PWR CTRL



LVDS Conn.

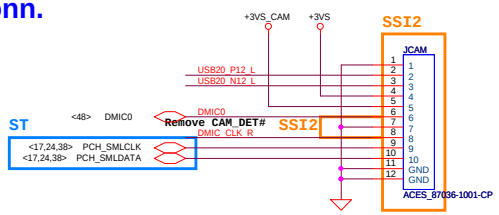


Reserve 2 Pins for AUO panel extra feature for Dell.
Panel side Pin34 DCR(Dynamic Contrast Ratio)
Panel side Pin35 DBC(Dynamic Backlight Control)

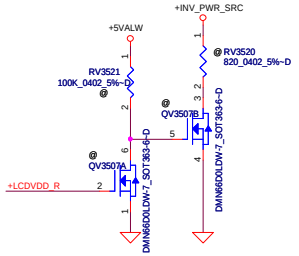


*** Reserved for EMI/ESD/RF need to close to JLVDS**

Webcam Conn.



*** Reserved for LCD sequence tuning**



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **LVDS /camera conn.**

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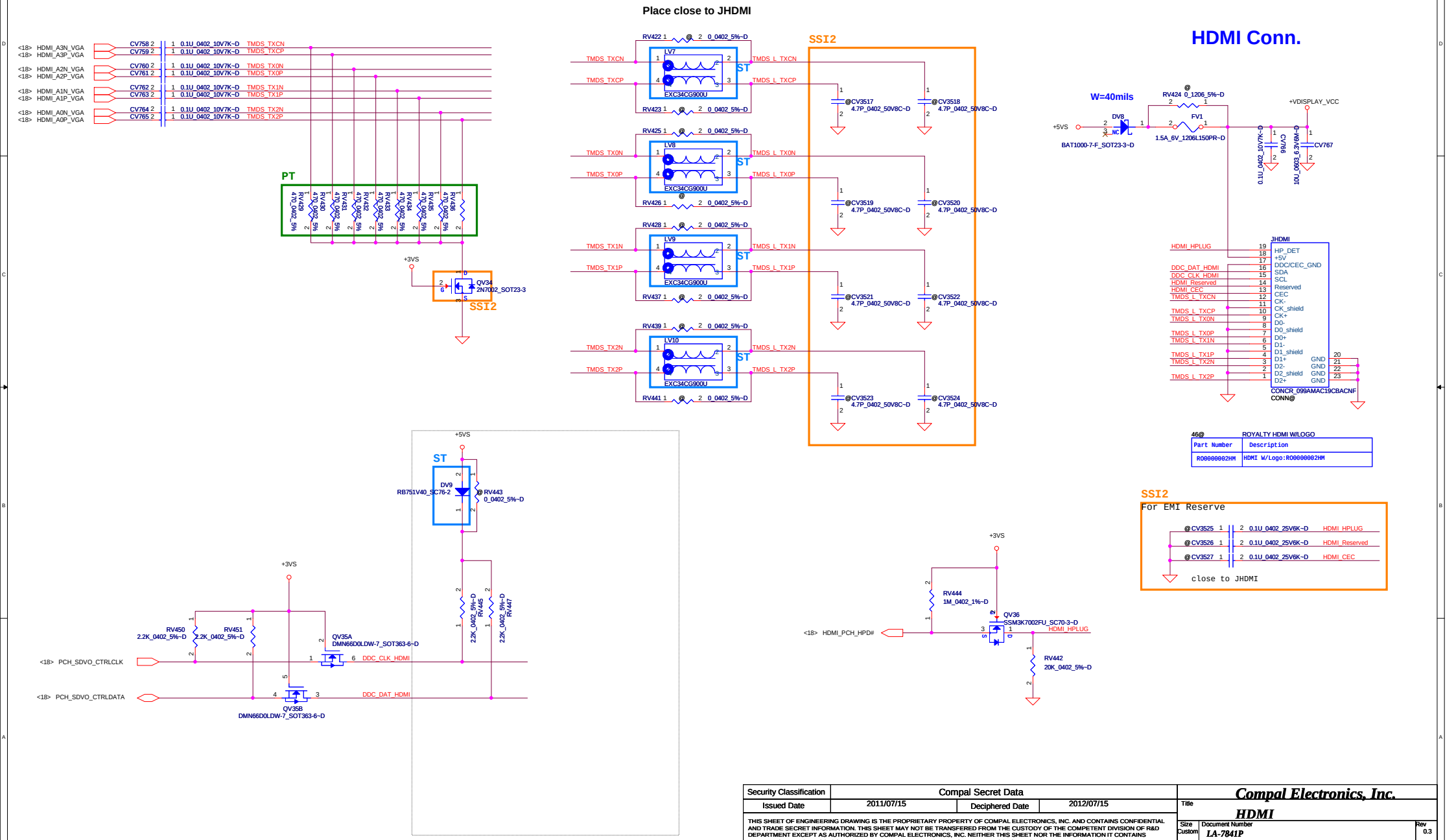

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
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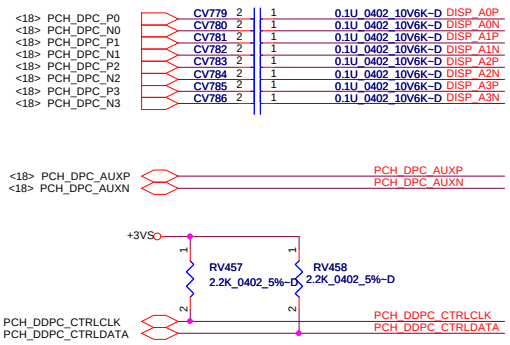
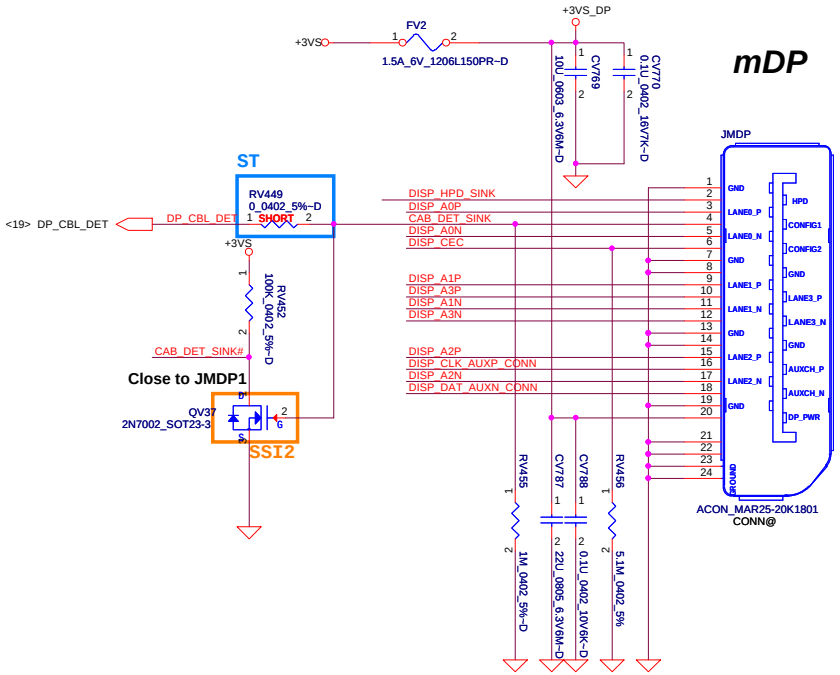
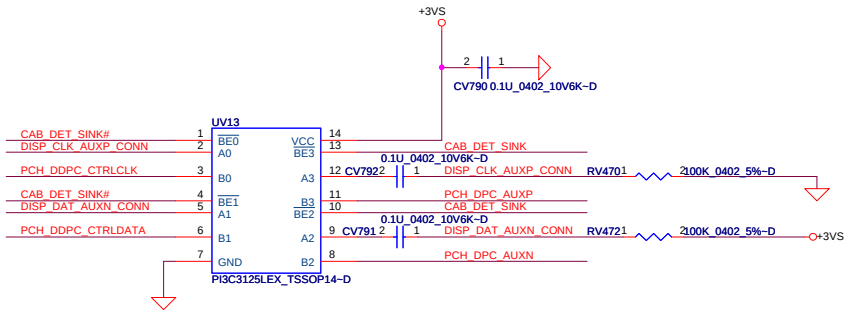
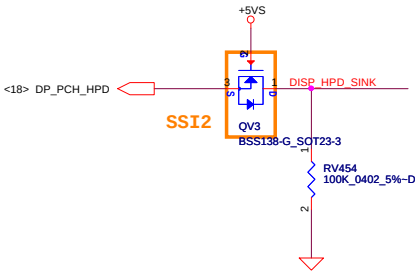




DDC Dongle SW for DP



DP HPD to PCH (iGPU)



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Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title: DP/FAN/HDD			
Size: Custom	Document Number: LA-7841P		Rev: 0.3
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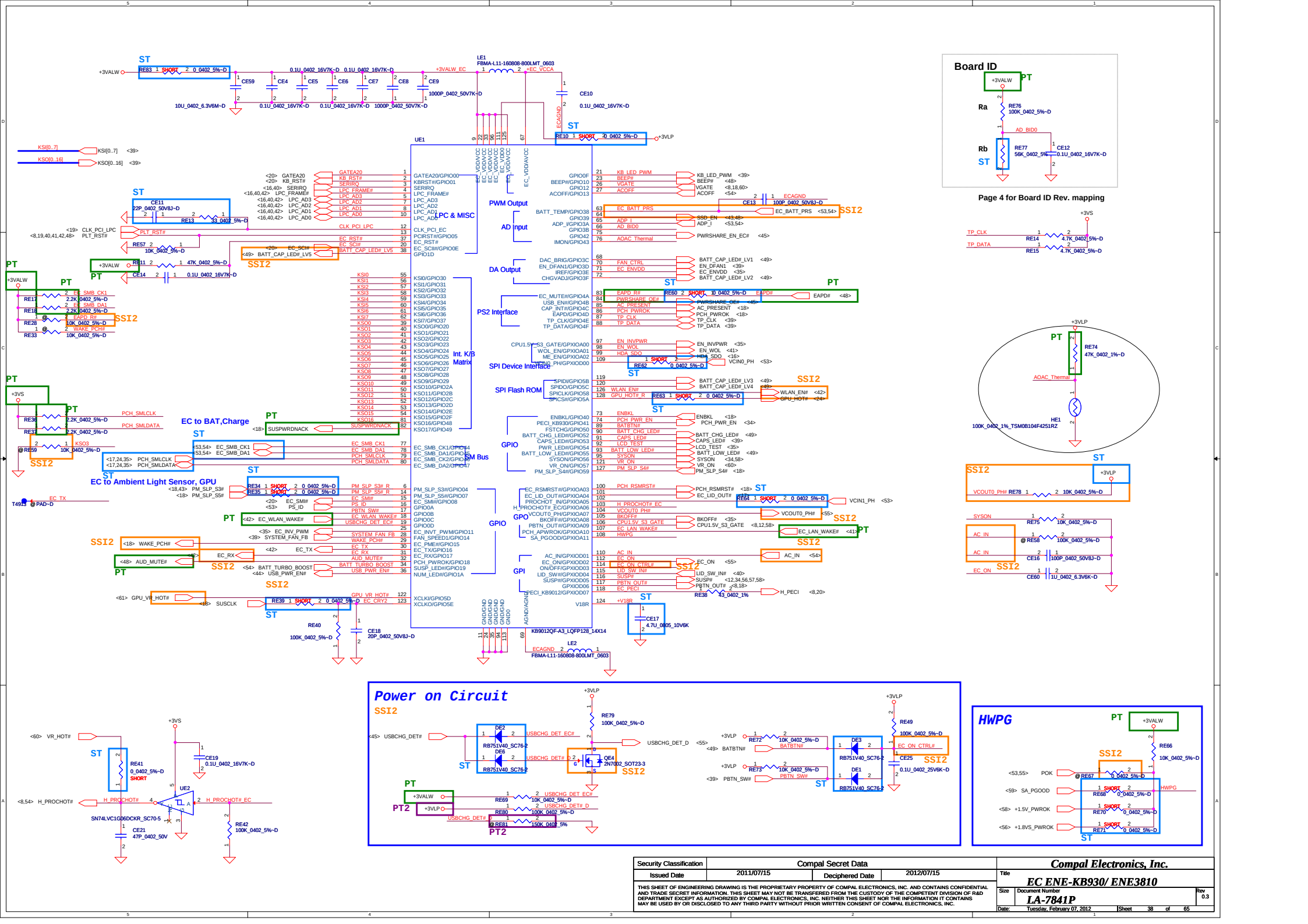

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Title: **EC ENE-KB930/ ENE3810**

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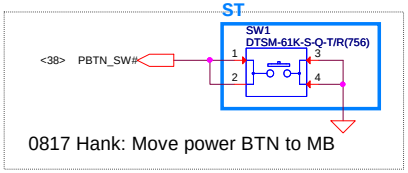
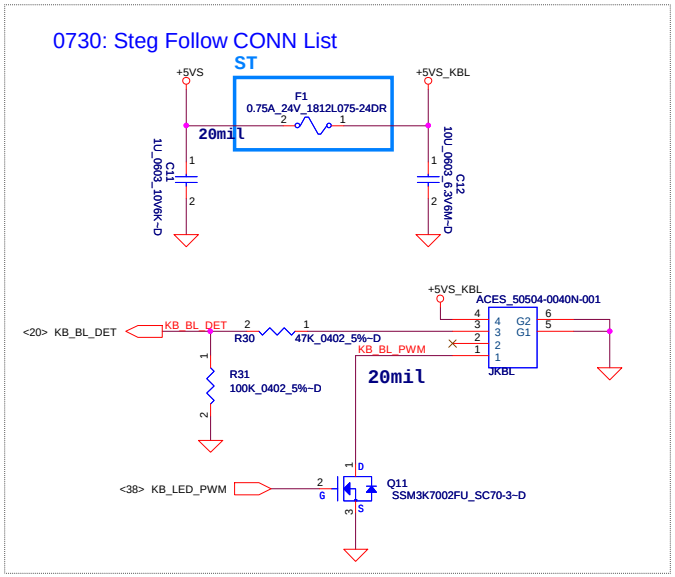
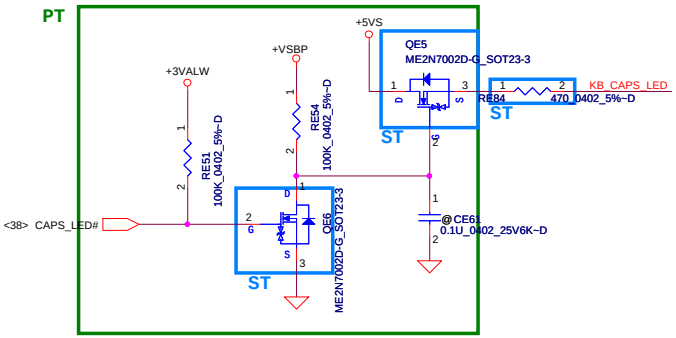
Power ON Circuit - PWR/Button Board

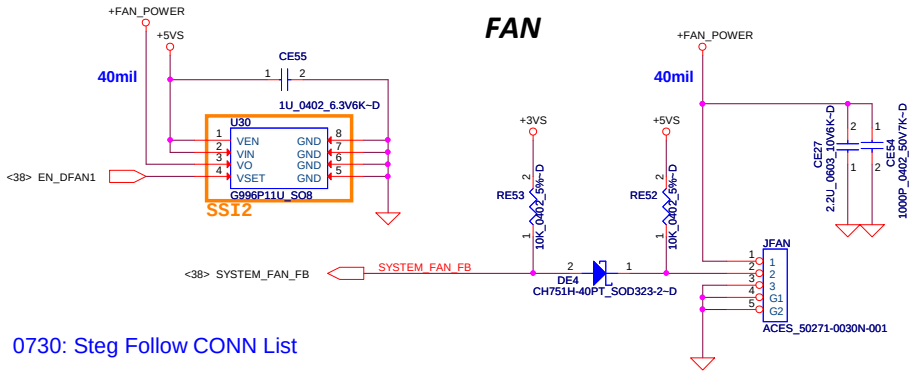


Keyboard back light

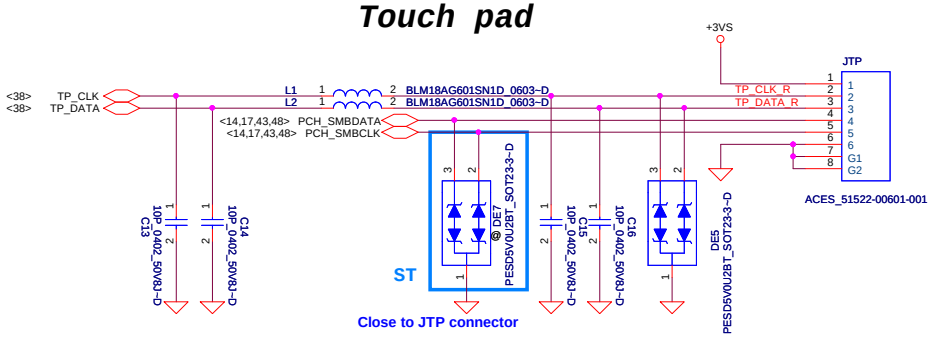




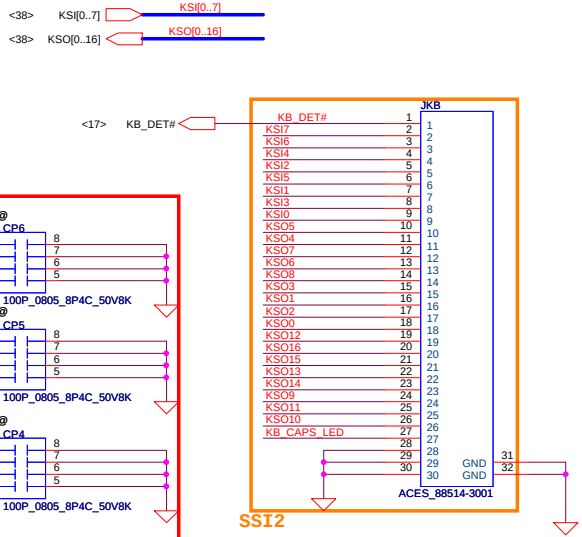
FAN Control circuit

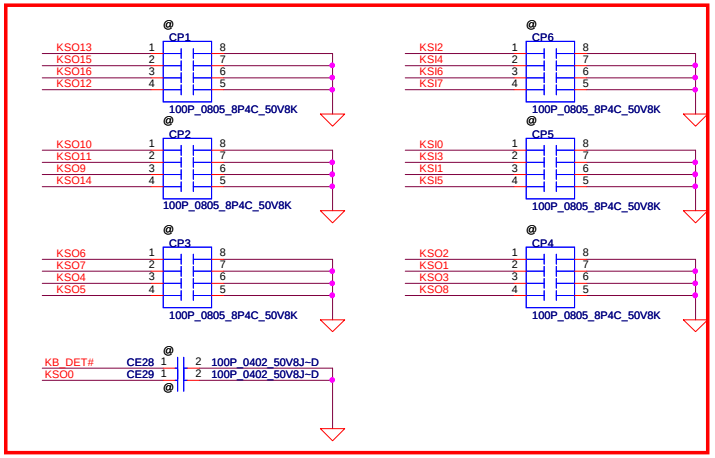


Touch pad



INT_KBD Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: SW/TP/SCREW

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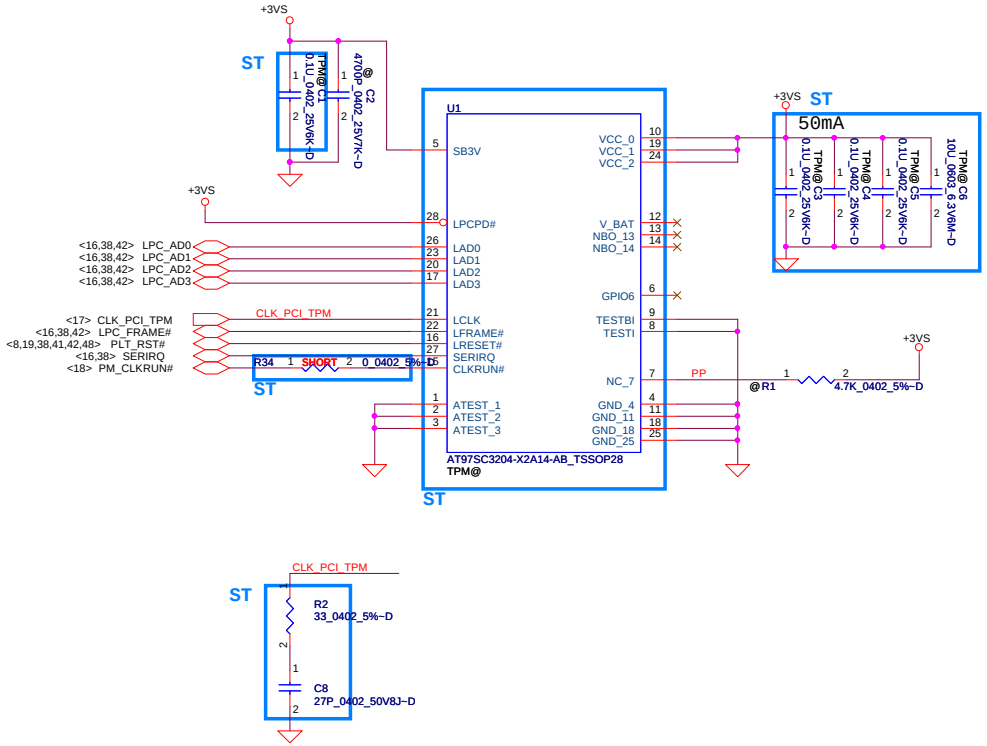
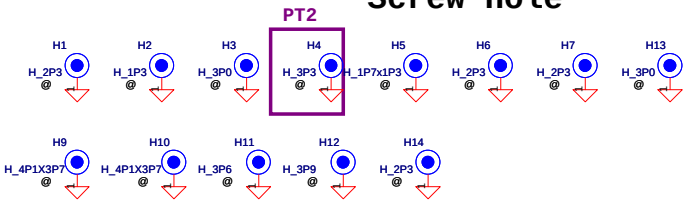
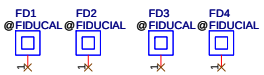
ATMEL TPM for XPS

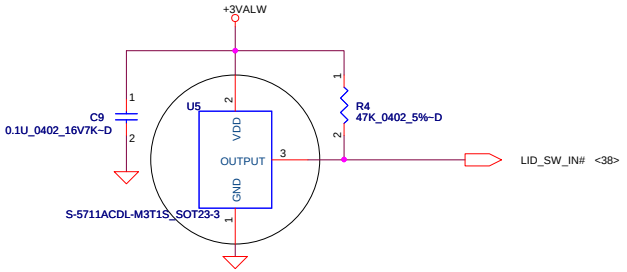


Screw Hole





Lid Switch



No CIS Symbol, Change PN to SA00003GI00 as ME recommand.

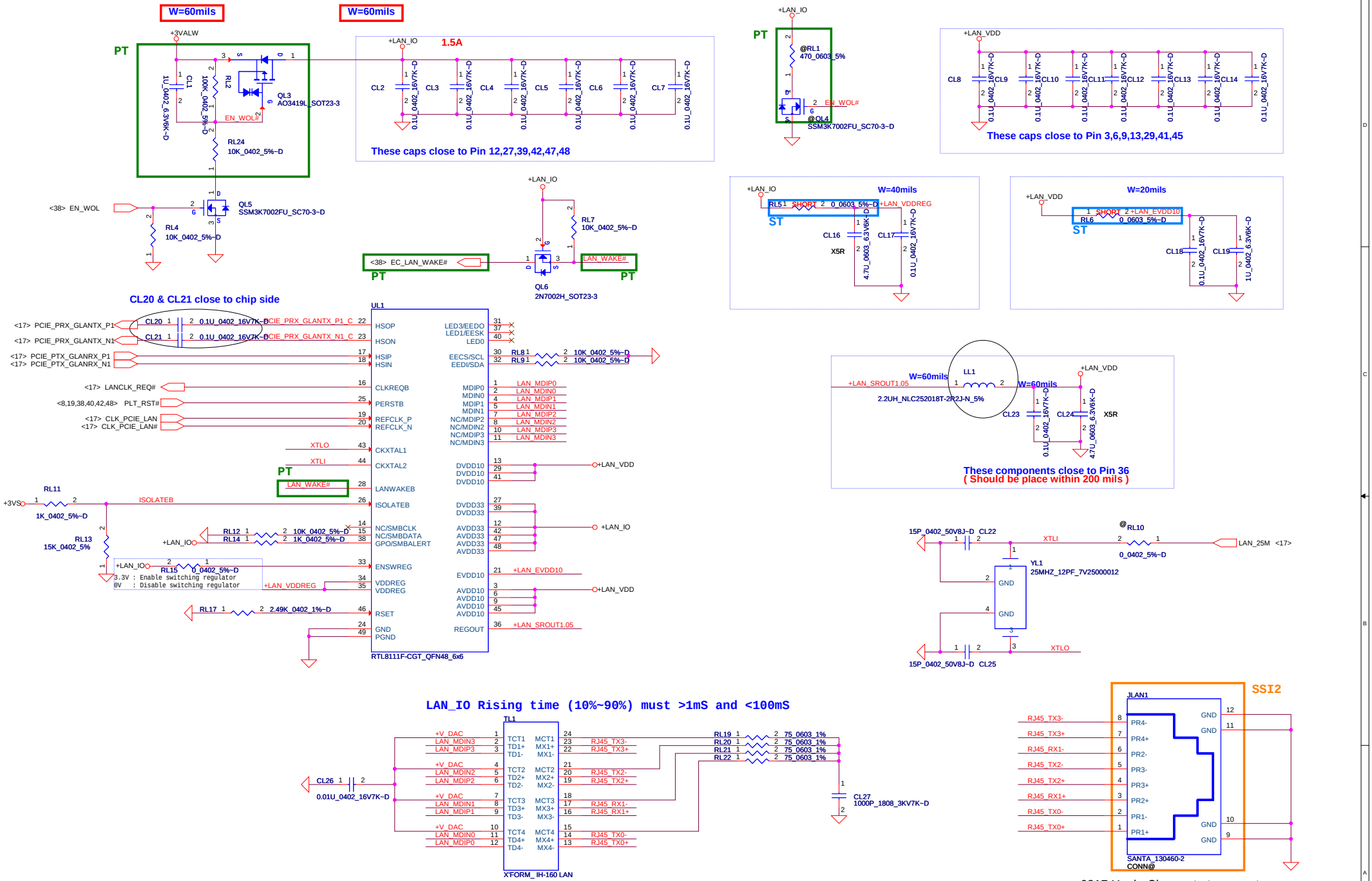
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: CONN & LID

Size | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 40 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

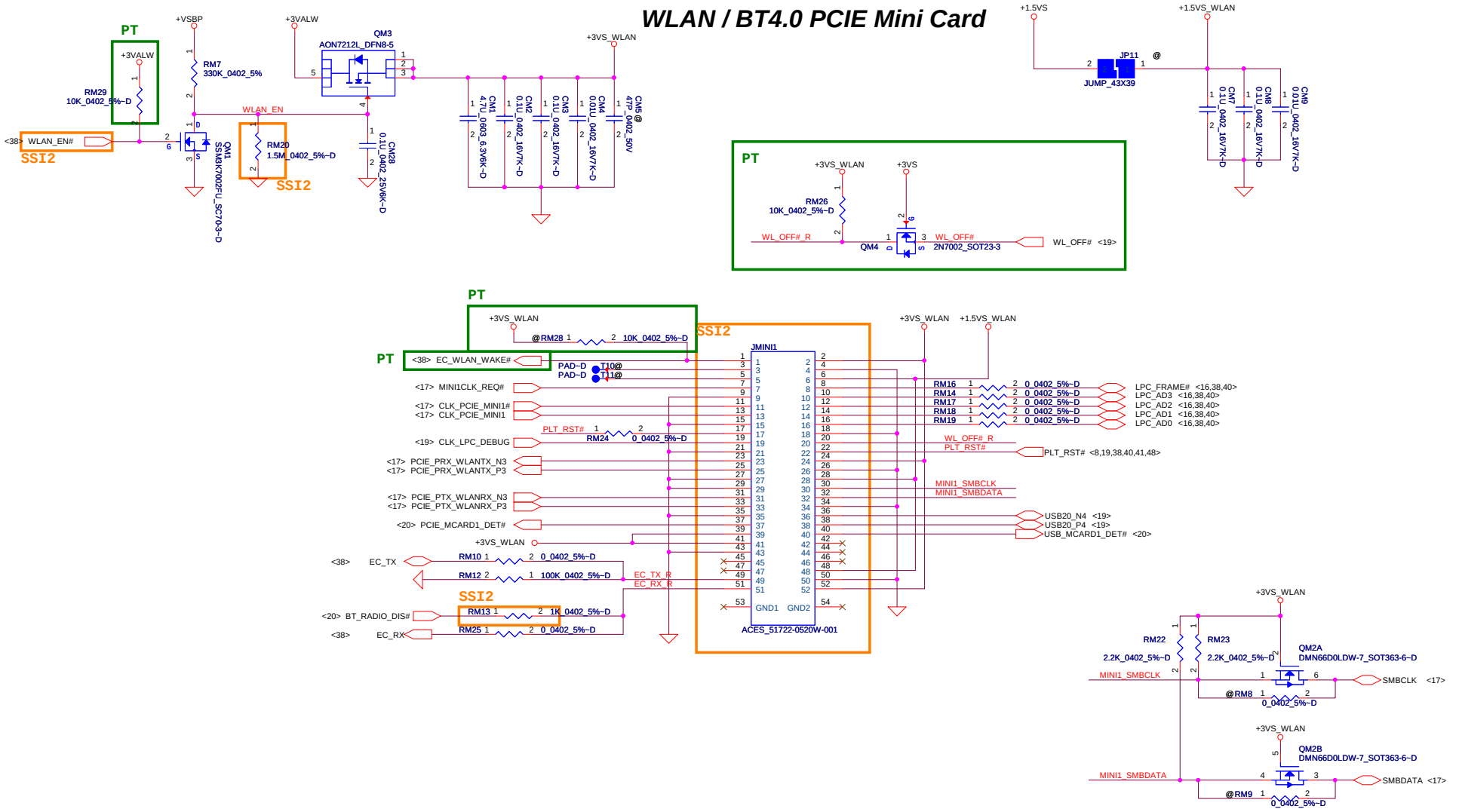
Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size	Document Number	Rev
Custom	LA-7841P	0.3

Date: Tuesday, February 07, 2012 Sheet 41 of 65

WLAN / BT4.0 PCIE Mini Card



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **WLAN/WWAN/SIM/BT**

Size	Document Number	Rev
Custom	LA-7841P	0.3

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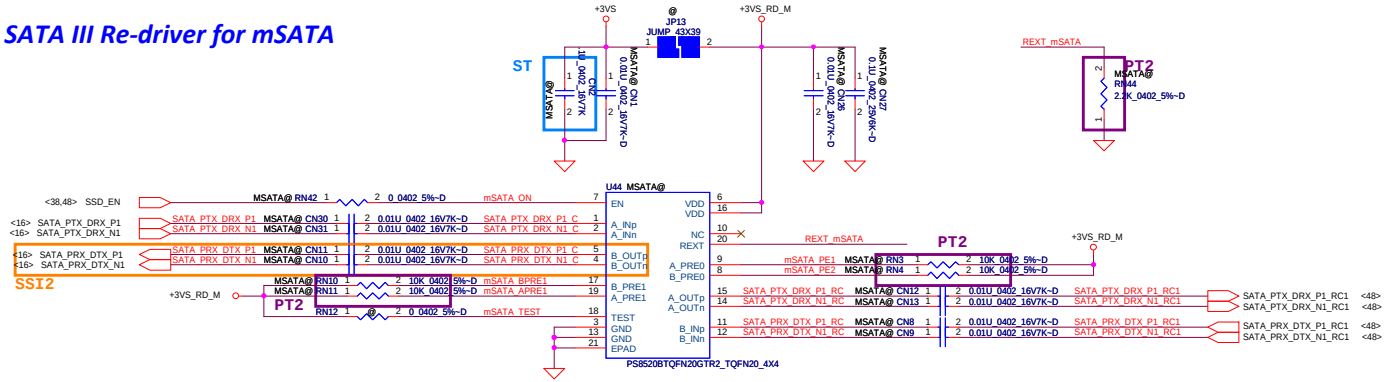
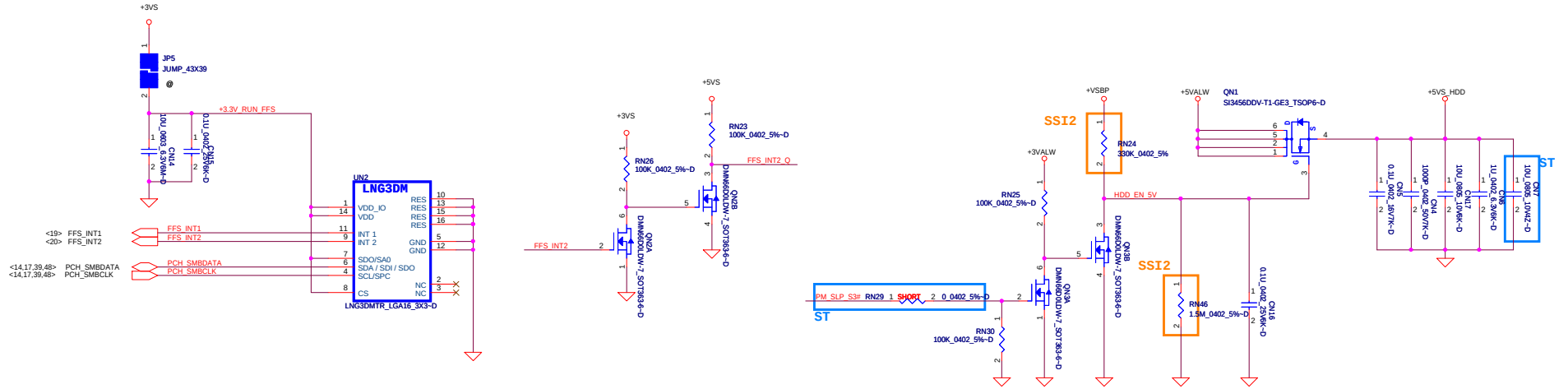
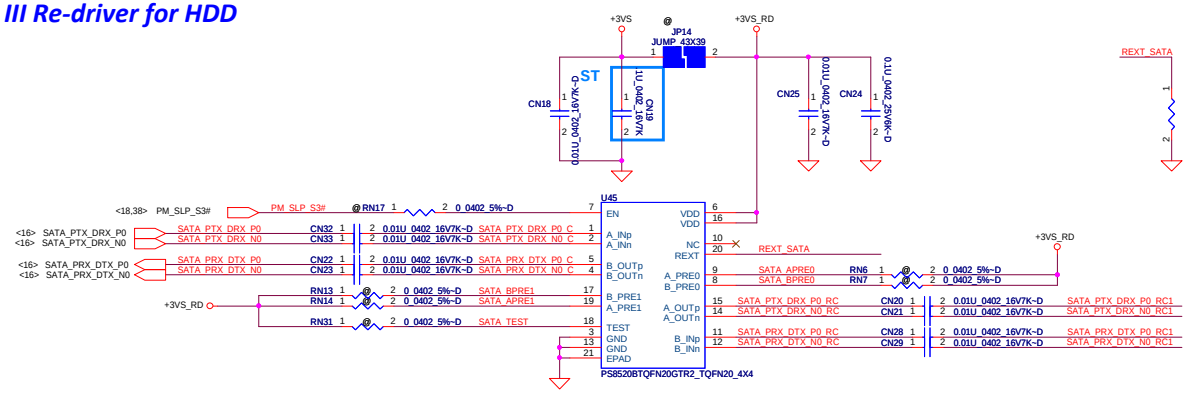
SATA III Re-driver for mSATA

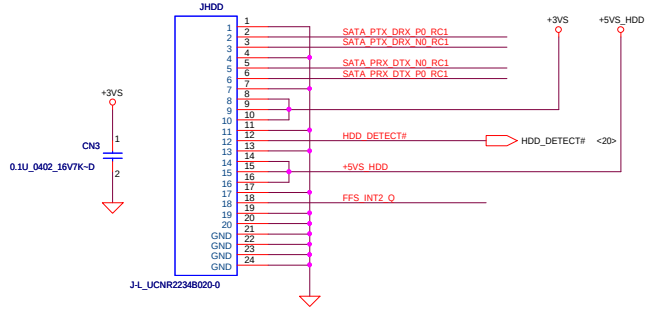




SATA III Re-driver for HDD



HDD CONN



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

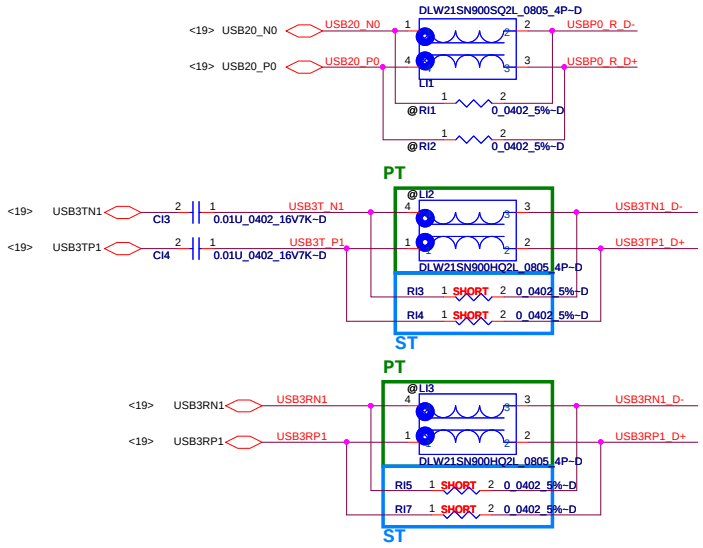
Compal Electronics, Inc.

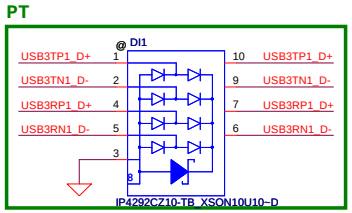
Title: HDD / FFS

Size	Document Number	Rev
C	LA-7841P	0.3

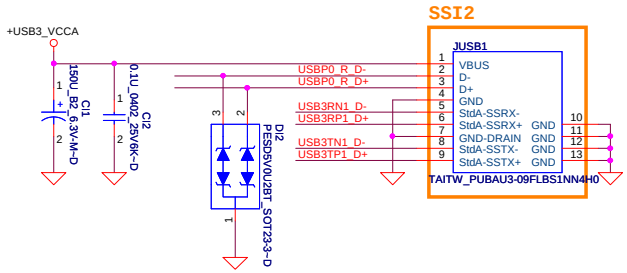
Date: Tuesday, February 07, 2012 | Sheet 43 of 65

USB3.0 / USB2.0

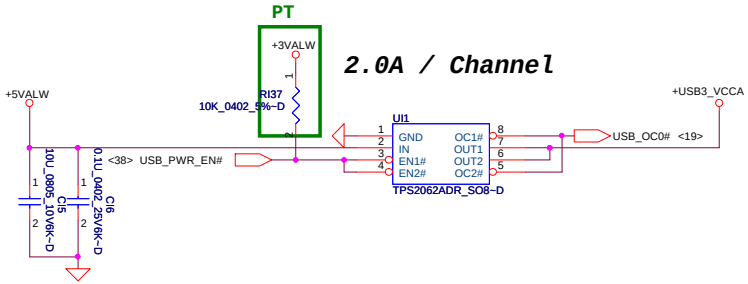




Place close to JUSB1



0816 Hank: Change USB connector to DC233009W00

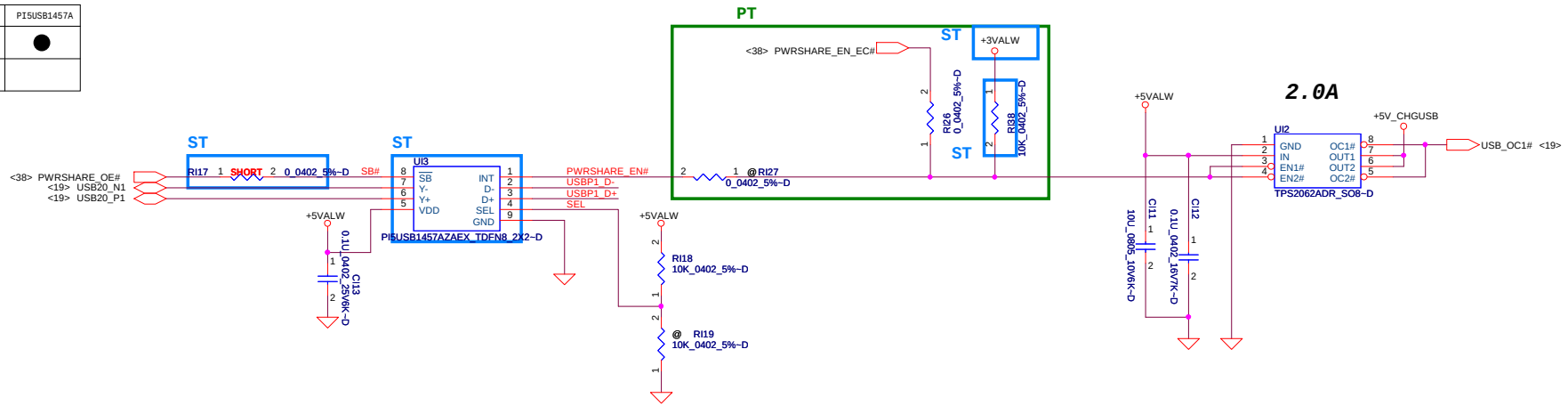


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date 2012/07/15	Title: USB conn.
			Size: Document Number: LA-7841P Rev: 0.3
			Date: Tuesday, February 07, 2012 Sheet 44 of 65

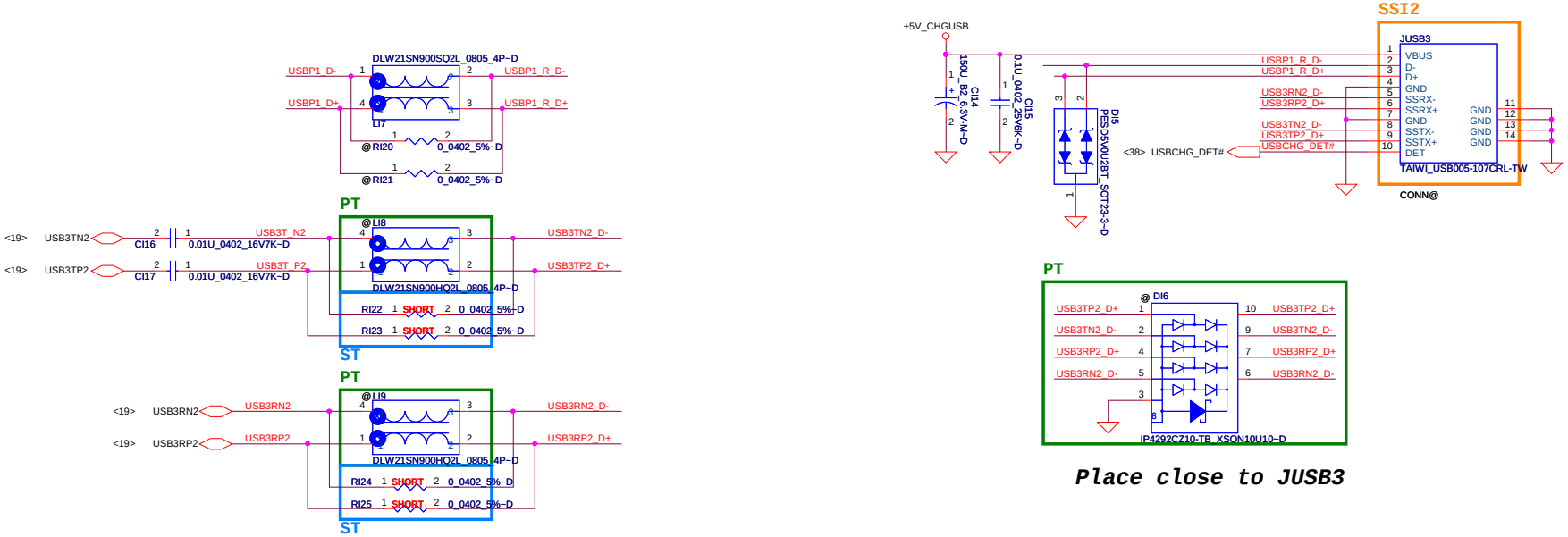
USB Powershare

	PI5USB1457	PI5USB1457A
INT		●
$\overline{INT}$	●	

USB Power Switch



USB3.0 / USB2.0



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date 2012/07/15	Title: USB conn.
			Size: Document Number: LA-7841P Rev: 0.3
			Date: Tuesday, February 07, 2012 Sheet 45 of 65

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **HD Audio ALC275/Audio Jack**

Size	Document Number	Rev
Custom		

Date: Tuesday, February 07, 2012 Sheet 46 of 65

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

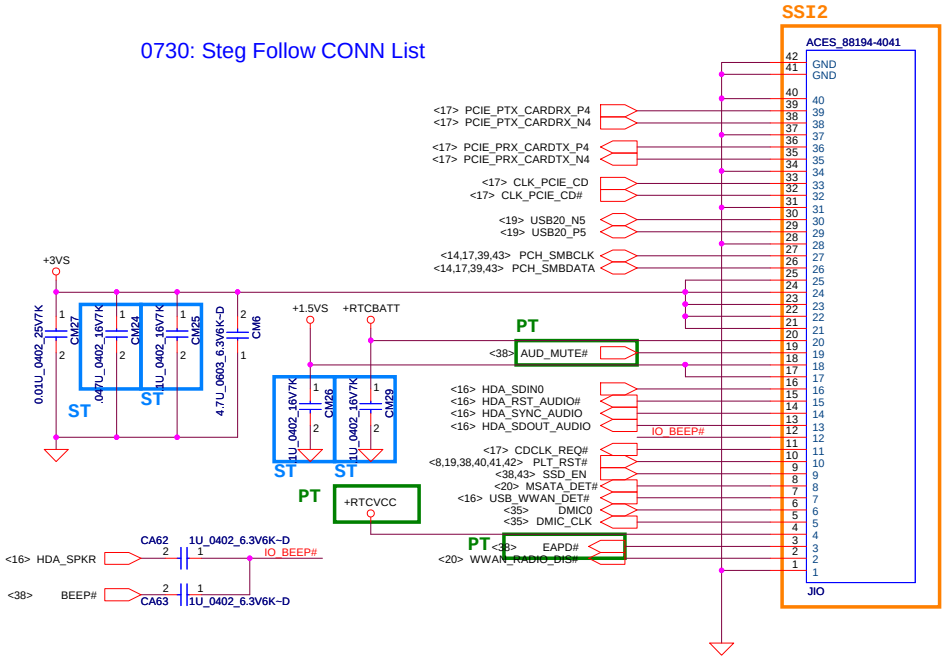
Title: Speaker/Audio Jack

Size	Document Number	Rev
Custom	LA-7841P	0.3

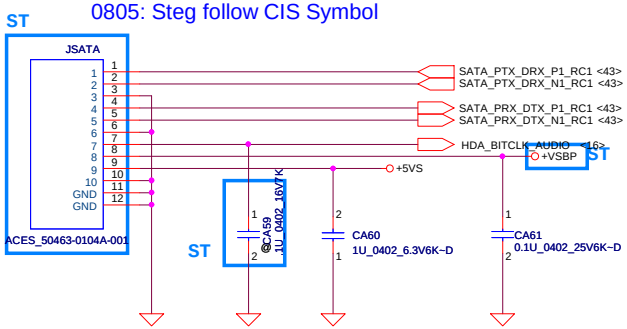
Date: Tuesday, February 07, 2012 Sheet 47 of 65

IO BOARD Connector

0730: Steg Follow CONN List



0805: Steg follow CIS Symbol



0816 Hank: P/N Correct, footprint Correct, but not CIS.

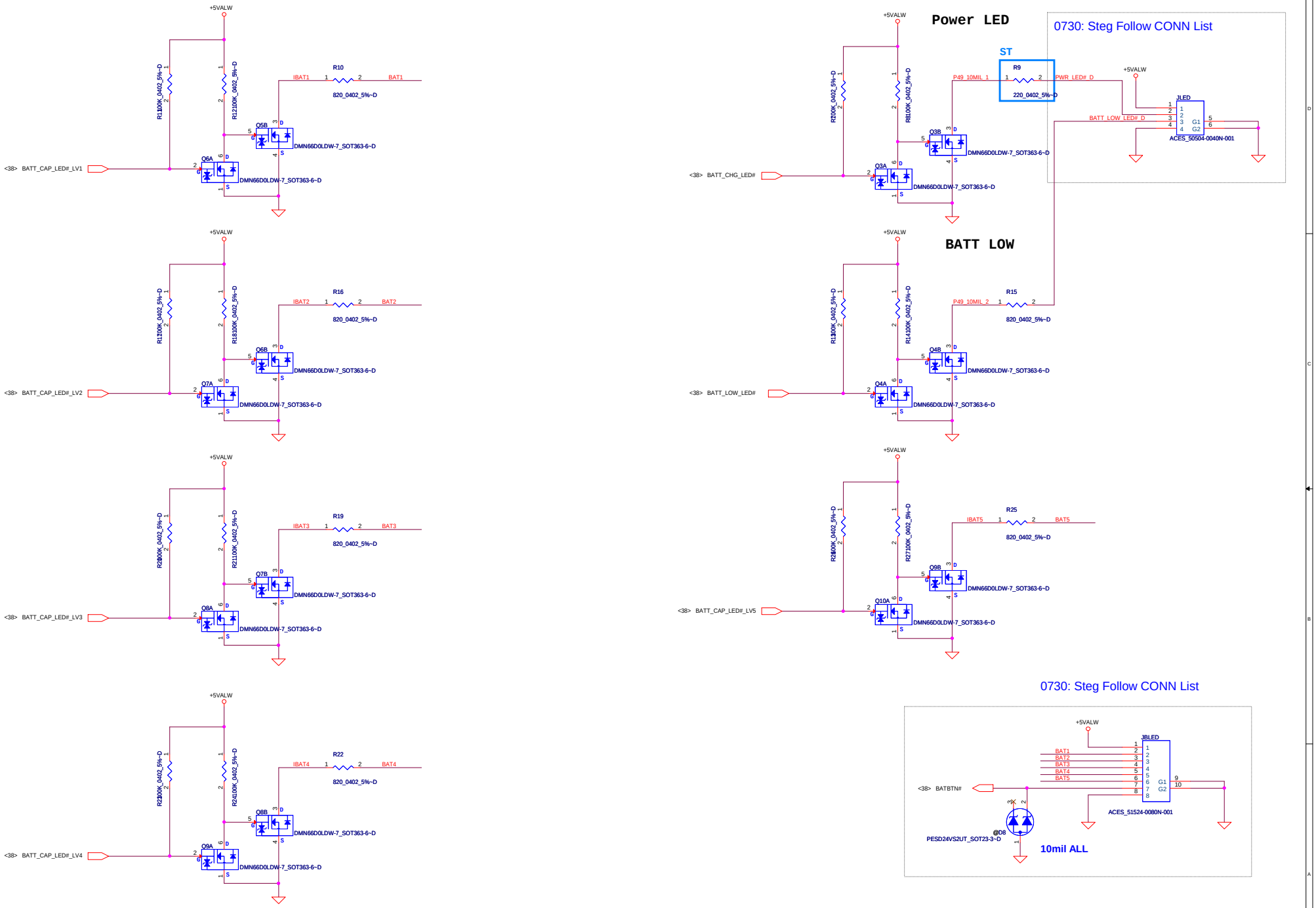
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: Card Reader RTS5209

Size | Document Number: LA-7841P | Rev: 0.3

Date: Tuesday, February 07, 2012 | Sheet 48 of 65



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Title	Speaker/Audio Jack		
Size C	Document Number LA-7841P		Rev 0.3
Date: Tuesday, February 07, 2012		Sheet 49 of 65	

Version change list (P.I.R. List)

EE section

Item	Reason for change	PG#	Modify List	Date	Phase
1	GRST delay to 2ms	P04-USB3.0	DEL POK to GRST , ADD RC , R62,C154		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Compal Electronics, Inc.	
Title	Block Diagram
Size	Document Number
Rev	0.3
Date:	Tuesday, February 07, 2012
Sheet	50 of 65

Title	<Title>
Size: A	Document Number: <Doc>
Rev	0.3
Date:	Tuesday, February 07, 2012
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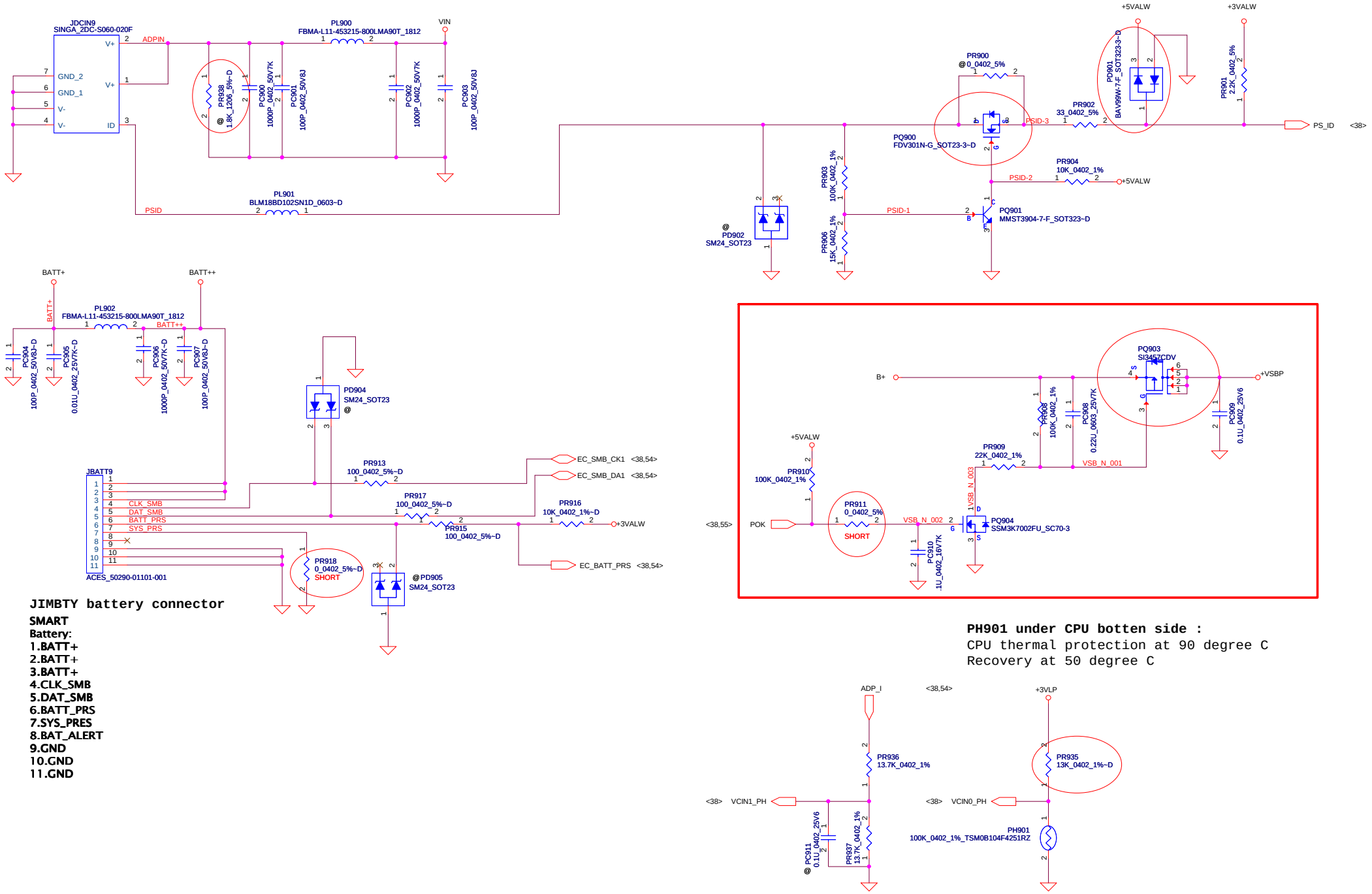
Title	<Title>
Size: A	Document Number: <Doc>
Rev: 0.3	
Date: Tuesday, February 07, 2012	Sheet 52 of 65



JIMBTY battery connector

SMART Battery:

1.BATT+
2.BATT+
3.BATT+
4.CLK_SMB
5.DAT_SMB
6.BATT_PRS
7.SYS_PRES
8.BAT_ALERT
9.GND
10.GND
11.GND

PH901 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C

Compal Electronics, Inc.
Title: PWR-DCIN / BATT CONN / OTP
Size: Document Number: XPS14
Rev: 0.1
Date: Tuesday, February 07, 2012
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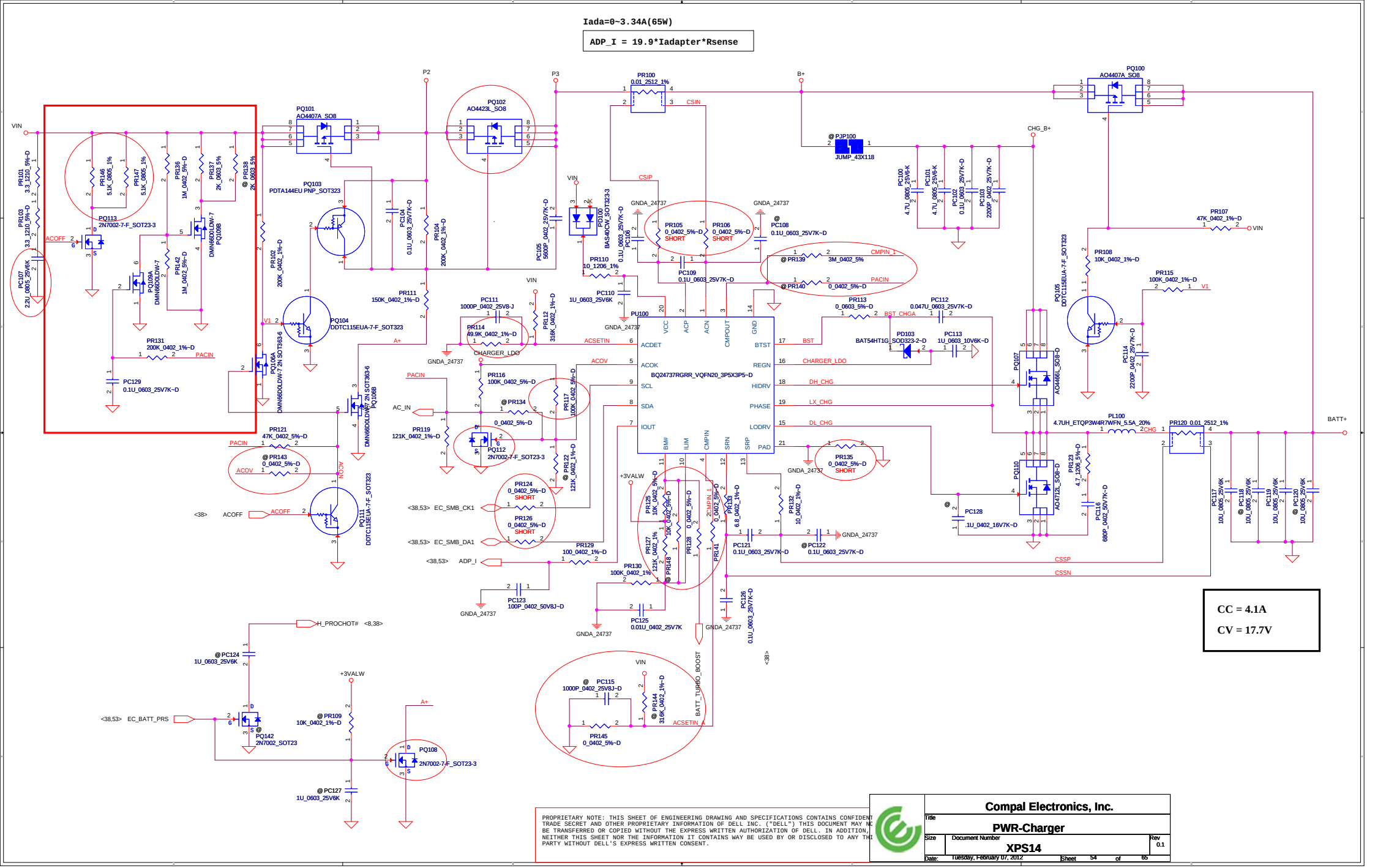
Iada=0~3.34A(65W)

ADP_I = 19.9*Iadapter*Rsense

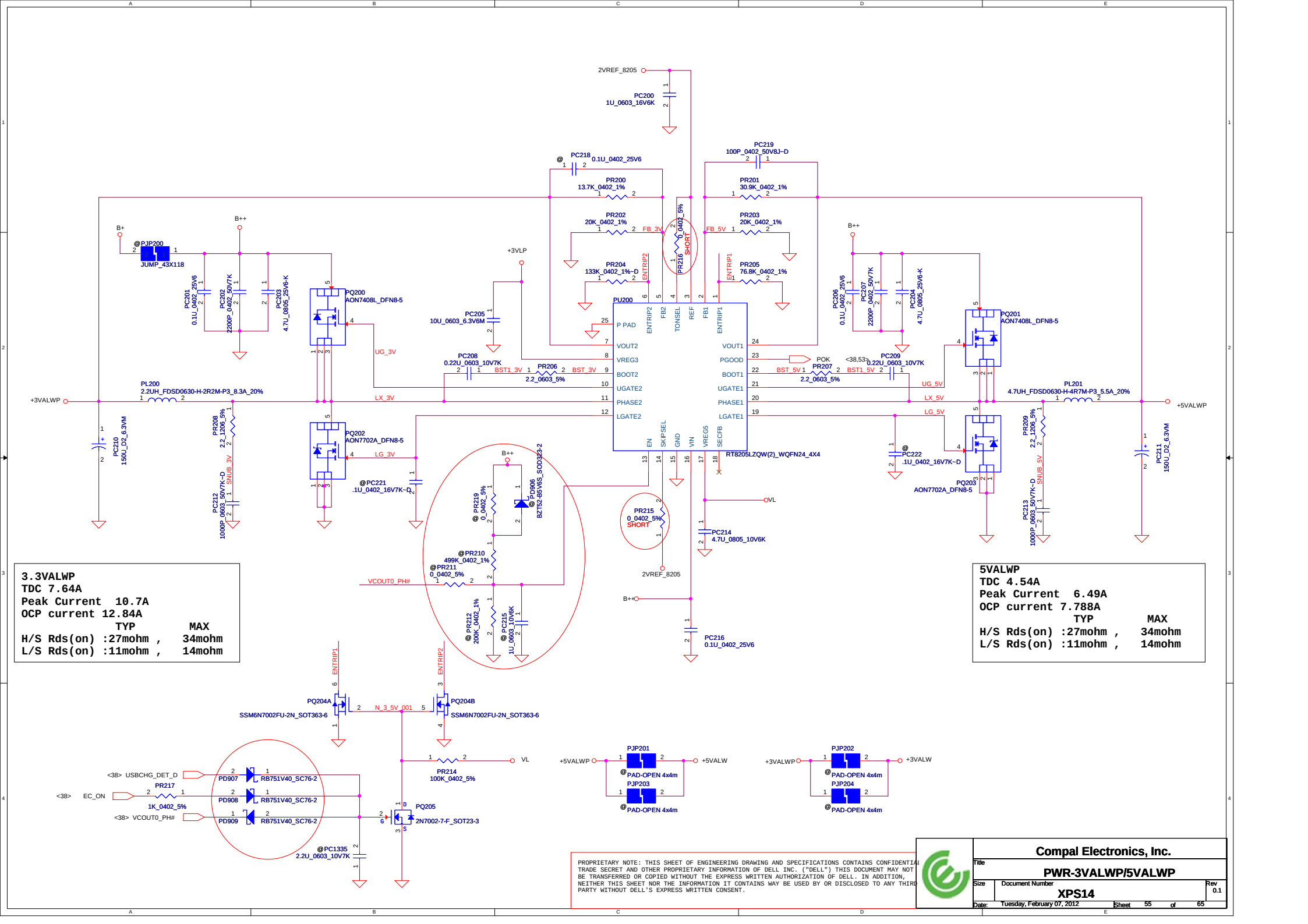


Compal Electronics, Inc.

Title: PWR-Charger

Size | Document Number: XPS14 | Rev: 0.1

Date: Tuesday, February 07, 2012 | Sheet 54 of 65


3.3VALWP
TDC 7.64A
Peak Current 10.7A
OCP current 12.84A
TYP MAX
H/S Rds(on) :27mohm , 34mohm
L/S Rds(on) :11mohm , 14mohm
5VALWP
TDC 4.54A
Peak Current 6.49A
OCP current 7.788A
TYP MAX
H/S Rds(on) :27mohm , 34mohm
L/S Rds(on) :11mohm , 14mohm
RT8205LZQW(2)_WQFN24_4X4
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Compal Electronics, Inc.
Title
PWR-3VALWP/5VALWP
Size
Document Number
XPS14
Rev
0.1
Date: Tuesday, February 07, 2012
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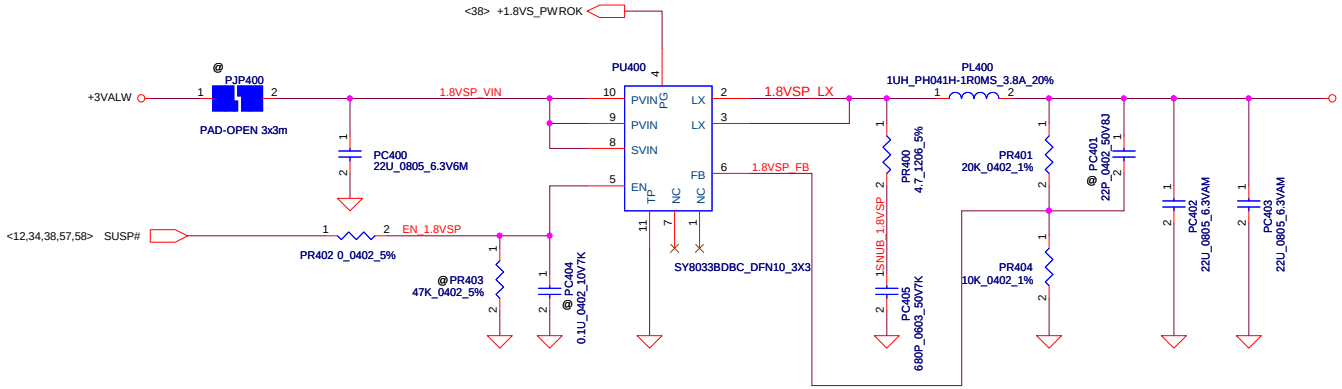
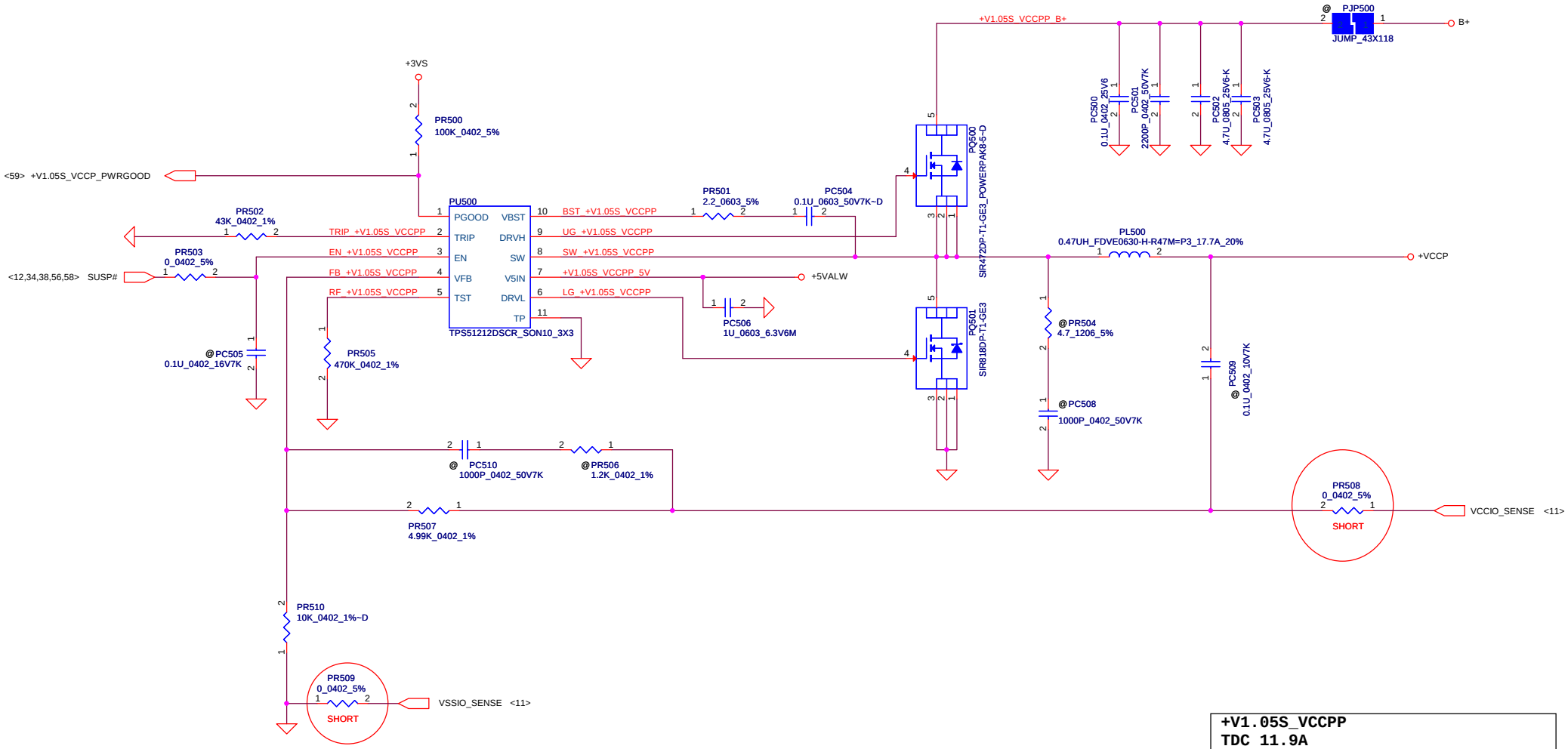


<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR404)=0.6*(1+20K/10K)=1.8V

+1.8VSP
TDC 1.092A
Peak Current 1.56A

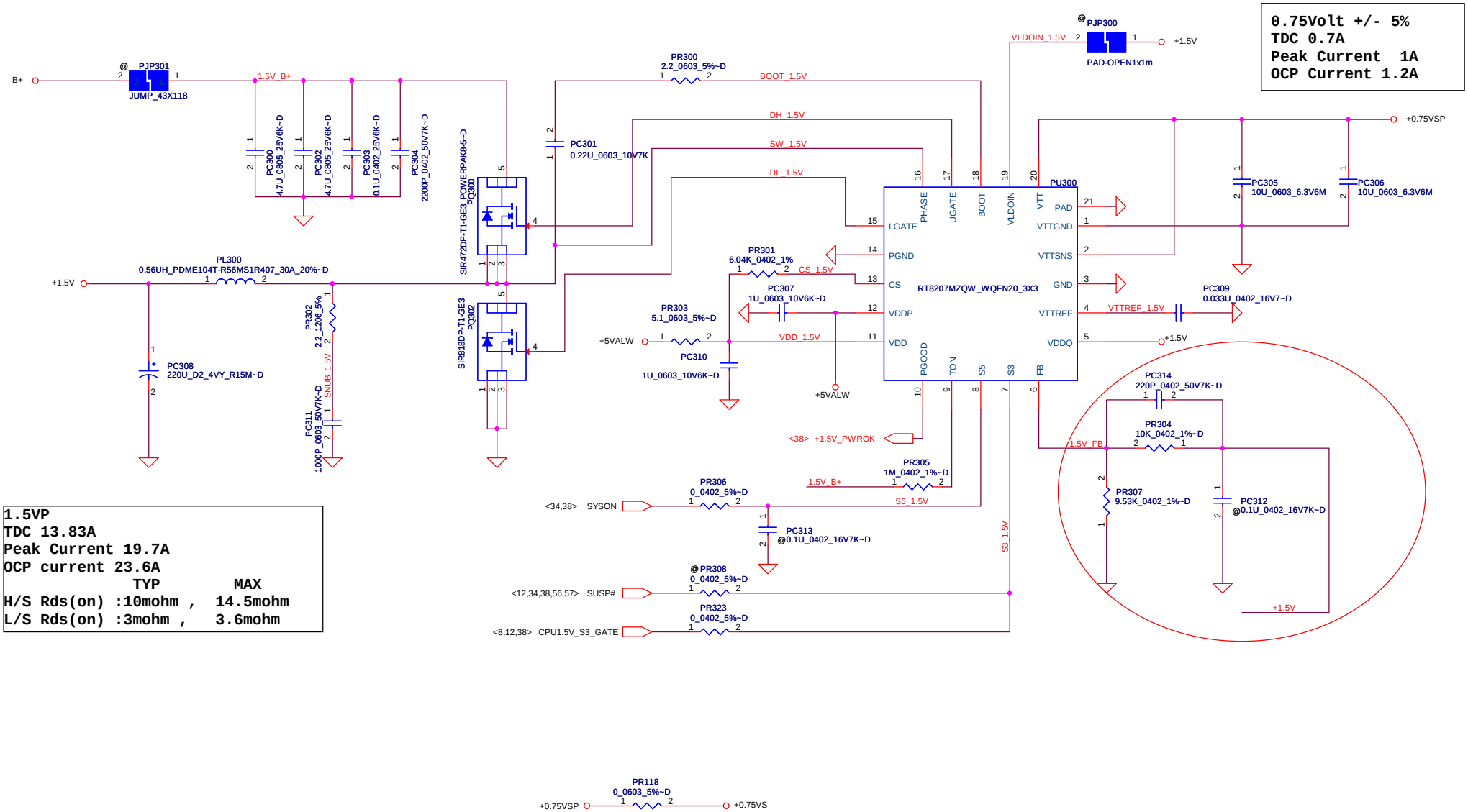


+V1.05S_VCCPP
TDC 11.9A
Peak Current 17A
OCP current 20.4A

	TYP	MAX
H/S Rds(on) :	10mohm ,	14.5mohm
L/S Rds(on) :	3mohm ,	3.6mohm

Compal Electronics, Inc.

Title	PWR-V1.05S_VCCPP	
Size	Document Number: XPS14	Rev: 0.1
Date: Tuesday, February 07, 2012	Sheet 57 of 65	


0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A
1.5VP
TDC 13.83A
Peak Current 19.7A
OCP current 23.6A
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
PJP301
JUMP_43X118
PJP300
PAD-OPEN1x1m
PL300
0.56UH_PDME104T-R56MS1R407_30A_20%~D
PU300
RT8207MZQW_WQFN20_3X3
PR300
PR301
PR302
PR303
PR304
PR305
PR306
PR307
PR308
PR310
PR323
PR118
PC301
PC303
PC304
PC305
PC306
PC307
PC308
PC309
PC310
PC311
PC312
PC313
PC314
PQ300
PQ302
SIR472DP-T1-GE3_POWERPAK8-5-D
SIR818DP-T1-GE3
BOOT_1.5V
DH_1.5V
SW_1.5V
DL_1.5V
CS_1.5V
VDD_1.5V
SNUB_1.5V
VTTREF_1.5V
1.5V_FB
S5_1.5V
S3_1.5V
+5VALW
+1.5V_PWROK
SYSON
SUSP#
CPU1.5V_S3_GATE
+0.75VSP
+0.75VS
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Compal Electronics, Inc.
Title
PWR-1.5VP/0.75VSP
Size
Document Number
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Rev
0.1
Date: Tuesday, February 07, 2012
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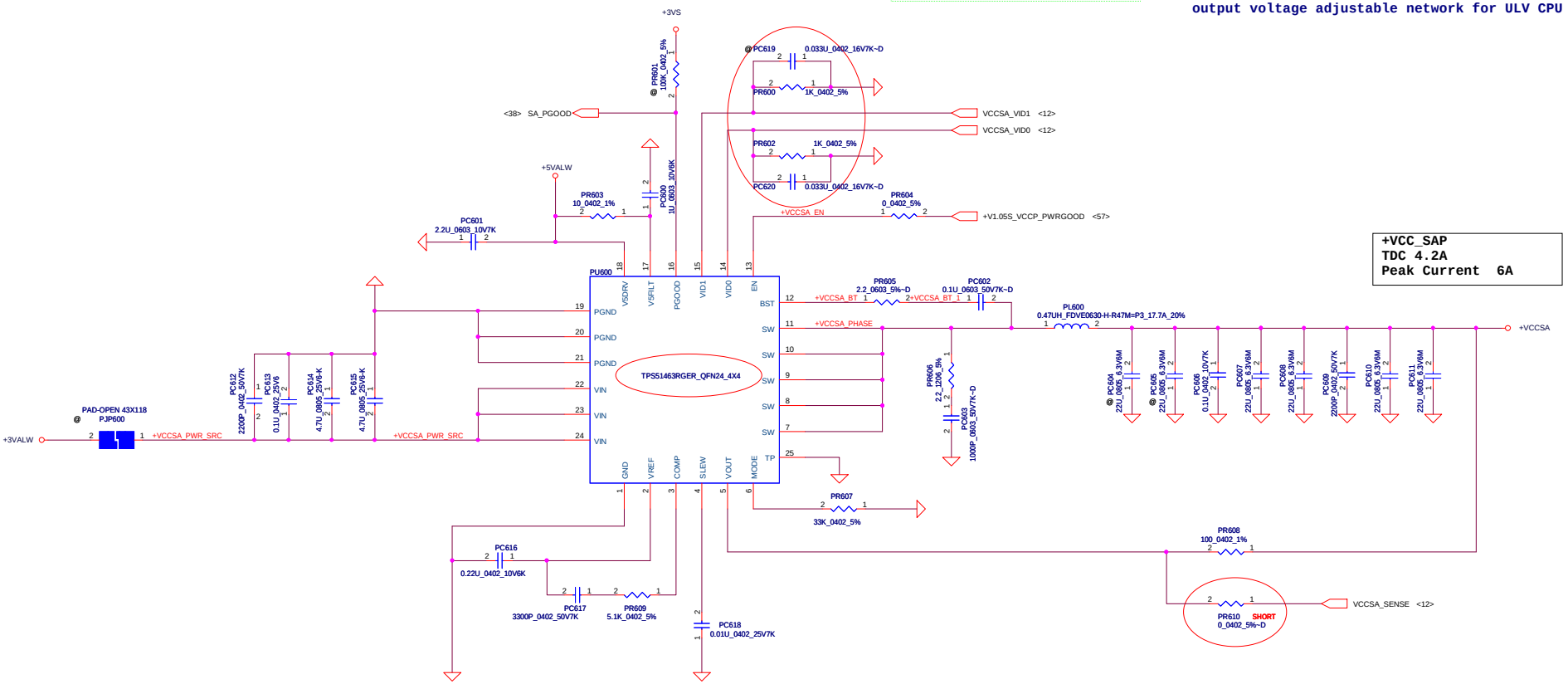
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

output voltage adjustable network for ULV CPU

+VCC_SAP
TDC 4.2A
Peak Current 6A



Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size | Document Number: XPS14 | Rev: 0.1

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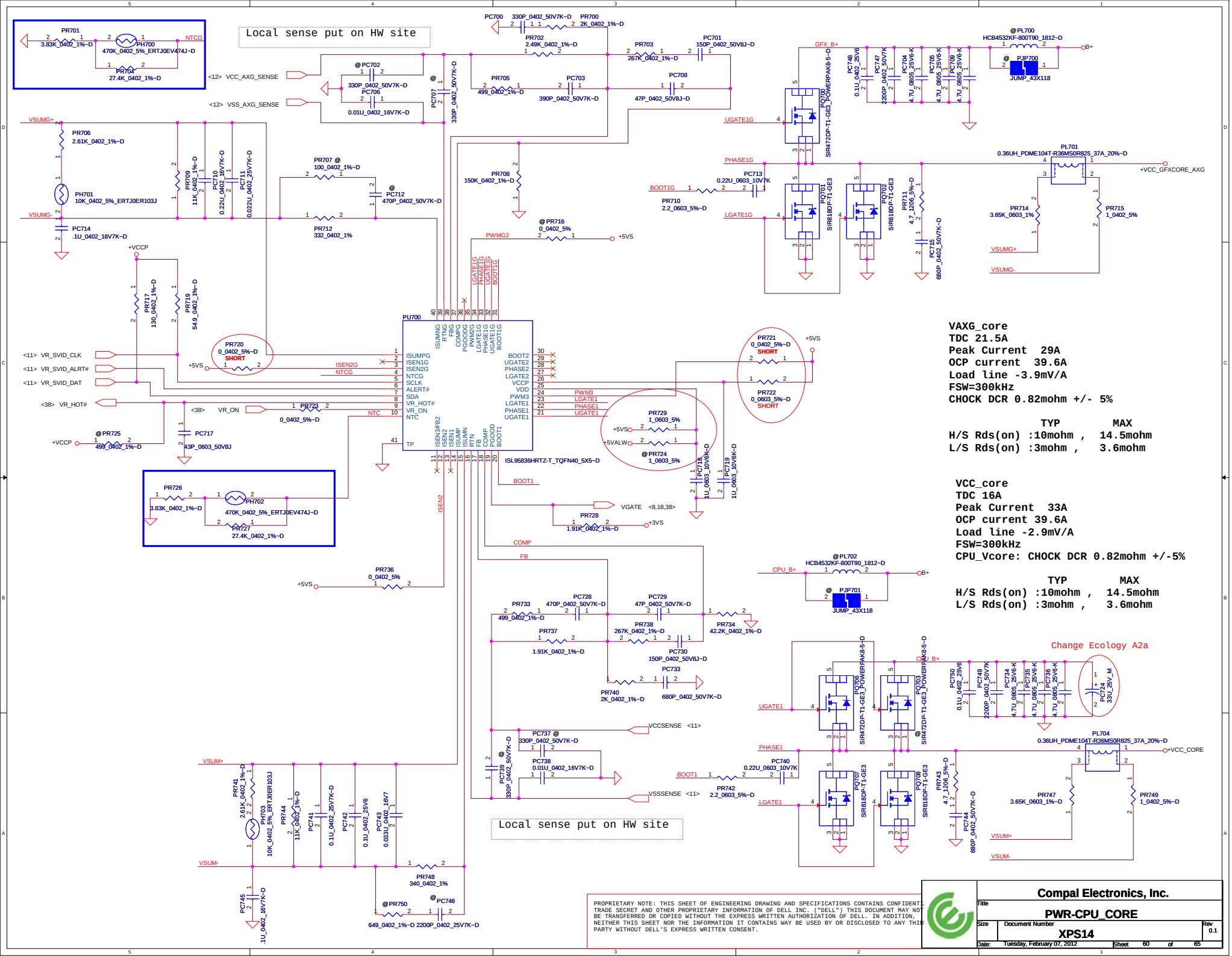
Local sense put on HW site
Local sense put on HW site
PU700
ISL95836HRTZ-T_TQFN40_5X5~D
VAXG_core
TDC 21.5A
Peak Current 29A
OCP current 39.6A
Load line -3.9mV/A
FSW=300kHz
CHOCK DCR 0.82mohm +/- 5%
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
VCC_core
TDC 16A
Peak Current 33A
OCP current 39.6A
Load line -2.9mV/A
FSW=300kHz
CPU_Vcore: CHOCK DCR 0.82mohm +/-5%
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
Change Ecology A2a
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Compal Electronics, Inc.
Title
PWR-CPU_CORE
Size
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Date: Tuesday, February 07, 2012
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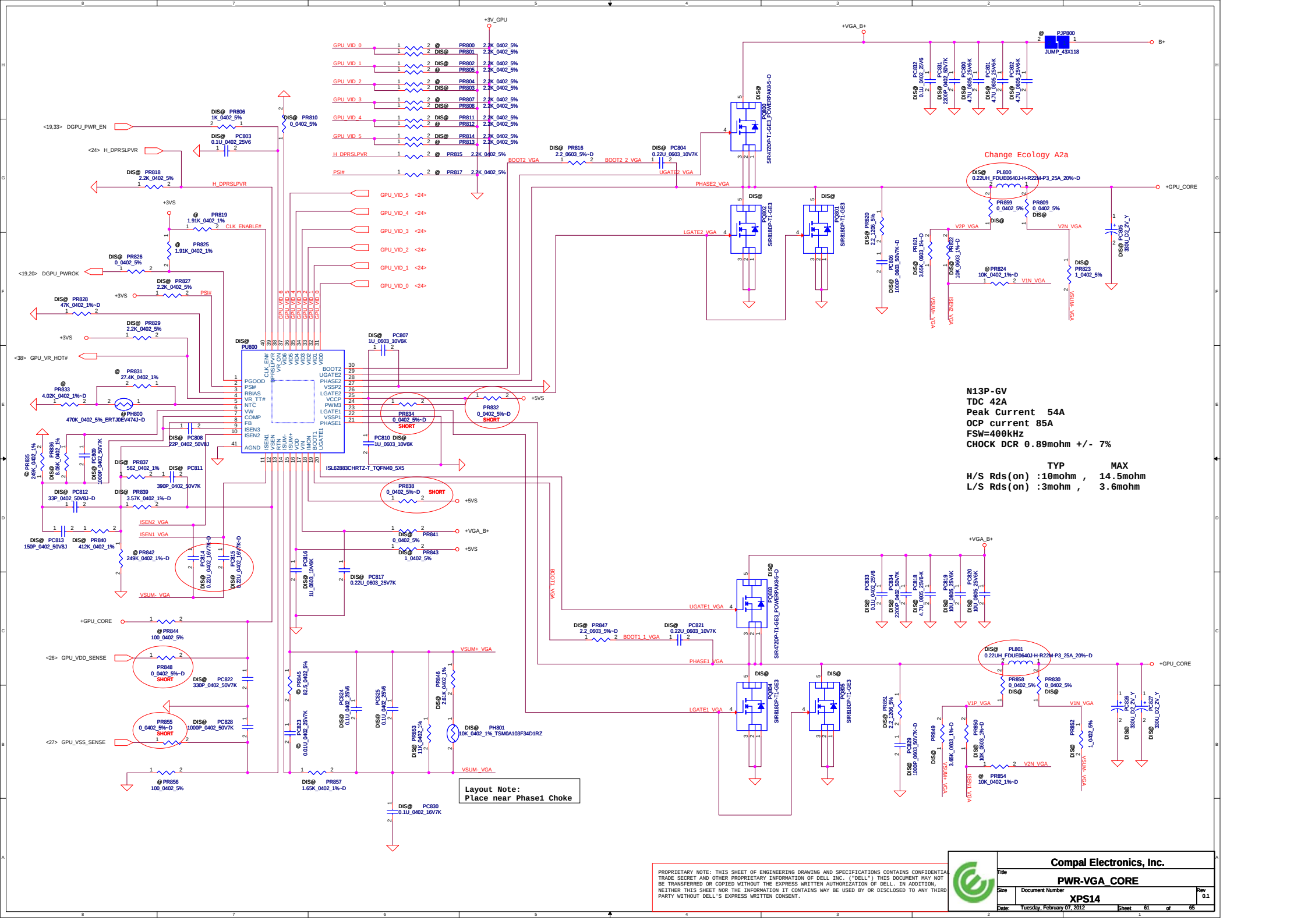
N13P-GV
TDC 42A
Peak Current 54A
OCP current 85A
FSW=400kHz
CHOCK DCR 0.89mohm +/- 7%
TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm
Change Ecology A2a
Layout Note:
Place near Phase1 Choke
ISL62883CHRTZ-T_TQFN40_5X5
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Compal Electronics, Inc.
Title
PWR-VGA_CORE
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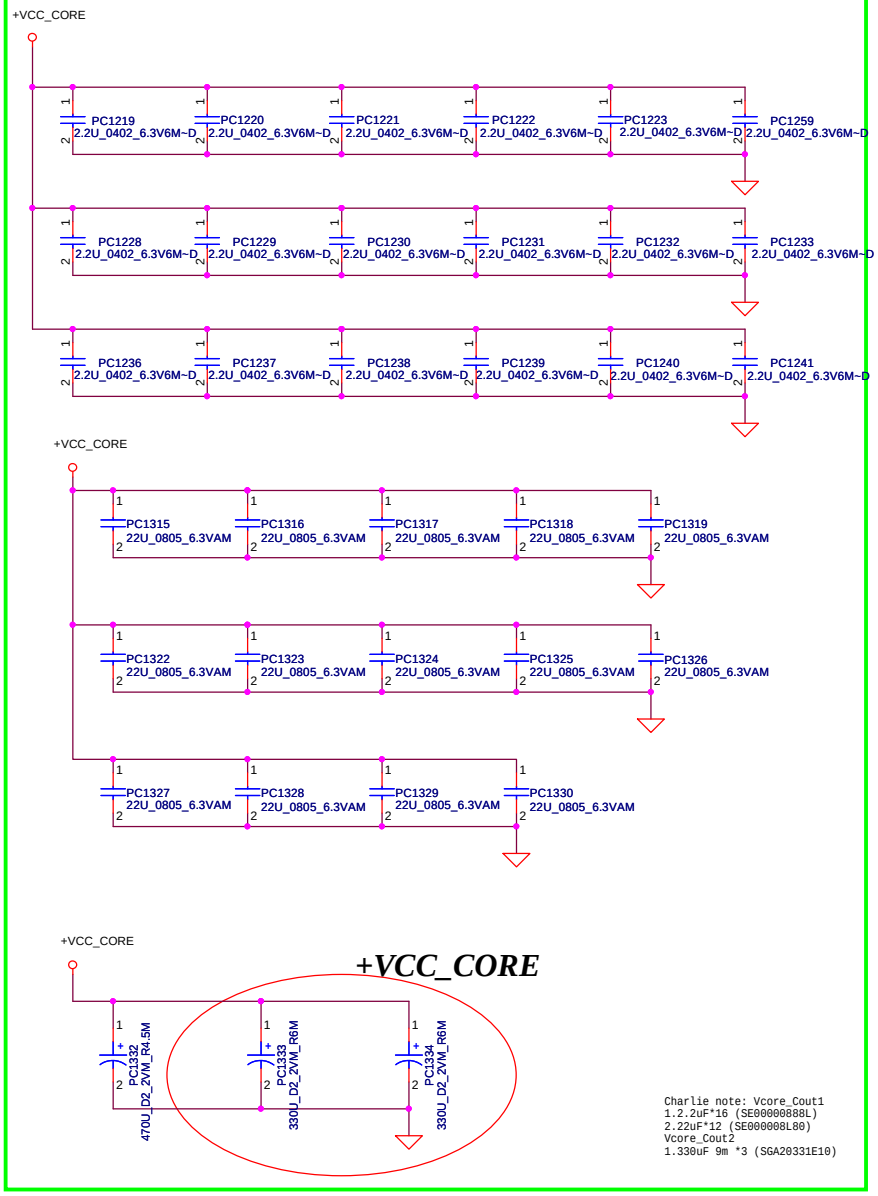
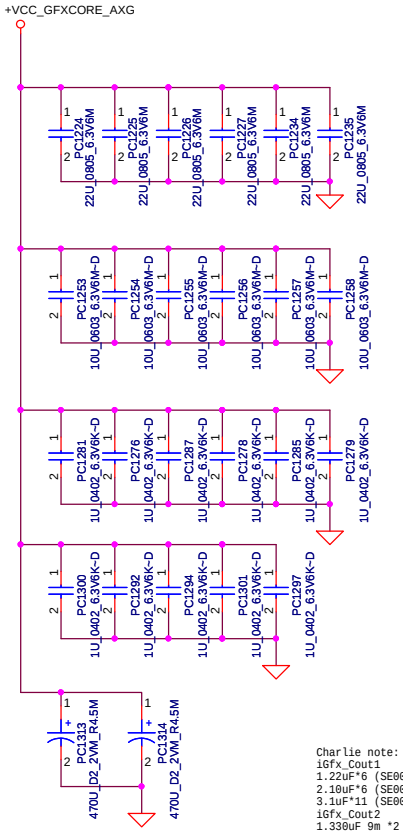
+VCC_CORE



+VCC_CORE

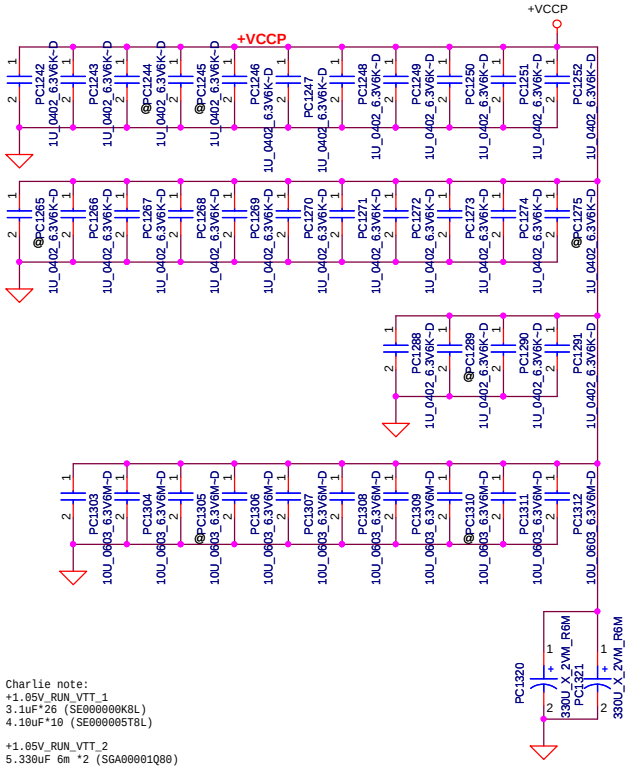
Charlie note: Vcore_Cout1
1.2.2uF*16 (SE00000888L)
2.22uF*12 (SE000008L80)
Vcore_Cout2
1.330uF 9m *3 (SGA20331E10)

+VCC_GFXCORE_AXG



Charlie note:
iGfx_Cout1
1.22uF*6 (SE000000I10)
2.10uF*6 (SE000005T8L)
3.1uF*11 (SE000000K8L)
iGfx_Cout2
1.330uF 9m *2 (SGA20331E10)

+VCCP

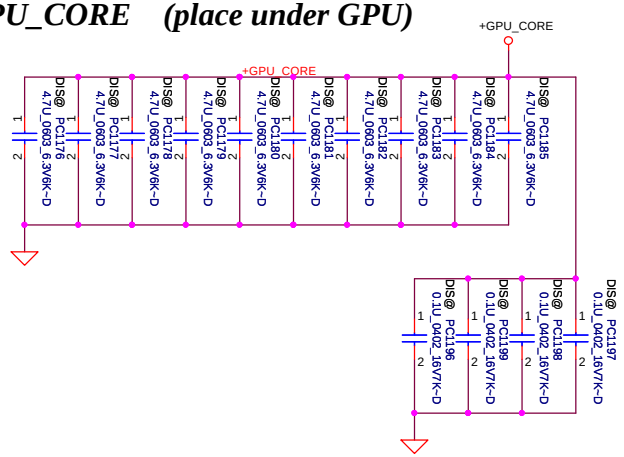


Charlie note:
+1.05V_RUN_VTT_1
3.1uF*26 (SE000000K8L)
4.10uF*10 (SE000005T8L)

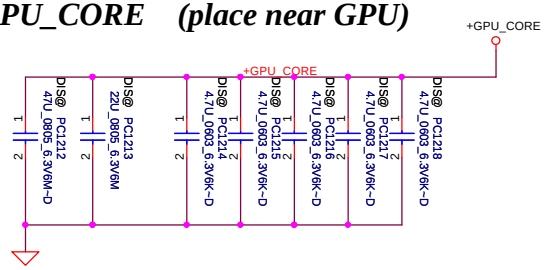
+1.05V_RUN_VTT_2
5.330uF 6m *2 (SGA00001Q80)

Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
Size	Document Number: XPS14	Rev: 0.1
Date: Tuesday, February 07, 2012	Sheet 62 of 65	

+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



Compal Electronics, Inc.		
Title: GPU DECOUPLING		
Size	Document Number: XPS14	Rev: 0.1
Date: Tuesday, February 07, 2012	Sheet 63 of 65	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	X01

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
QLM00	1	38	01/12			1.0	PCB REV change to 1.0	Change RE77 to 56K
	2	24	01/12			1.0	Change EC_SMB_CK2_PX/EC_SMB_DA2_PX pull up resistor as design guide	Change RV2420,RV2421 to 2.2K
	3	39	01/12			1.0	Adjust CAPS_LED brightness	Change RE84 to 470ohm
	4	45	01/12			1.0	Sync up with XPS 15" for pull up power rail	RI38 pull up from +5VALW to +3VALW
	5	17,24,35	01/12			1.0	Solve adaptor detect issue	Depop QH3; change GPU SMBus/Ambient Light Sensor connect to PCH_SMLDATA and PCH_SMLCLK
	6	45	01/12			1.0	Purchase recommand	Change UI3 to high active parts
	7	40	01/12			1.0	BOM structure control	ADD TPM@ for TPM circuit
	8	38	01/12			1.0	For USBCHG_DET_D can't turn on 3V/5V issue	Change RE78 pull up to +3VLP
	9	45	01/12			1.0	Vendor recommand	UI2 EN pin pull up resistor RI38 change to 10K
	10	35	01/12			1.0	Change JLVDS connector PN and footprint as assembly issue	Change JLVDS connector PN to SP01001BT00, footprint to ACES_59003-04006-001_40P
	11	39	01/12			1.0	ME change	SW1 PN change to SN100005100
	12	33	01/16			1.0	Solve 1.5V voltage drop issue	Change QV2803 to SB00000SJ0L to lower Rds on
	13		01/16			1.0	Remove 0 ohm to short pad for MP	RI22,RI23,RI24,RI25,RI17,RI3,RI4,RI5,RI7,RN29,RM10,RM25,RL25,RL6,R34,RE83, RE10,RE34,RE35,RE39, RE68,RE70,RE71,RE60,RE62,RE63,RE64,RV449, RV3519,RV3517,RI6,RI8,RV3525,RH199,RH105,RH106,RH108,RH110,RH112,RH101, RH103,RH107,RH44,RU125,RU122,RU123,RU116,RU131,RU75,RU62
	14	10	01/17			1.0	Change setting for Ivy Bridge support 1x16 PCI Epress and Sandy Bridge only UMA Config	Depop RU85
	15	49	01/17			1.0	ME requirement for LED brightness tunning	R9 Change to 220ohm for Power LED(White)
	16	39	01/18			1.0	EMI requirement	Add DE7 on TP SMBus
	17	38,35,39	01/19			1.0	Thailand flood disaster, original material shortage	Change DE1,DE2,DE3,DE6 PN to SCS00002G00; QE5,QE6,QV3508,QZ10,QZ13,QZ15 to SB00000M700; DV9 to SCS00002G00
	18	35	01/19			1.0	JLVDS pin define change for opertion risk	JLVDS Pin38 NC and up shift to Pin33
	19	33	01/20			1.0	Change HF part	Change RZ10,RZ11,RZ40,RZ41 PN to SD028220A8L
	20	48	01/20			1.0	Manufacture highlight change	Change JSATA footprint to ACES_50463-0104A-001_10P-T
	21	17,19,40	01/20			1.0	EMI requirement	Populate PCI CLK reserved parts RH65,CH26,CH31,R2,C8
	22	36	01/20			1.0	EMI requirement for LVDS	Change LV7,LV8,LV9,LV10 to SM070002S00
	23	39	01/30			1.0	Change HF part	Change F1 to SP040003200
	24	48,53	01/30			1.0	Solve audio power consumption issue	Change PQ903 PN to SB93457001L, JSATA pin8 B+ change to +VSBP
	25	17,38	01/30			1.0	EMI requirement	Populate CH98,CE11,RE13
	26	14	02/01			1.0	1.5V power rail reach up to 1.614V, change for derating concern	CD7 capacitor change from 2V to 2.5V
	27	15	02/02			1.0	EMI requirement	Add RV3529,RV3530,CV3528,CV3529
	28		02/02			1.0	Customer concern Y5V MLCC performance	Change CA59 to SE076104K80; CE17 to SE064475KL0;CN2,CH11,CN19,CM25,CM26, CM29,CU33,CU34,CU35,CU36,CU97,CU155 to SE076104K80; CM24,CU39 change to SE076473K80; CN7,CZ11,CV3508 change to SE064106M8L
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Title: **Change List**

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