PWA : Y507R
PWB : Y509R
SCH : Y510R

Calpella Intel Discrete Block Diagram

VER : D3A

SYSTEM POWER

PCH REGULATOR +1.05V_PCH PG 49	**SYS VR** +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 51	**VGA Core** +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
DDR3 VR +1.5V_SUS/+0.75V_DDR_VTT PG 47	**CPU VR** +1.1V_VTT PG 48	**REGULATOR** +1.8V_RUN PG 46
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/ +3.3V_RUN/+1.5V_RUN/ +1.5V_GDDR PG 54	**VCC Core** +VCC_CORE PG 50	**VGA VDDCI** +VDDCI PG 53

POWER
- AC/BATT CONNECTOR PG 55
- BATT CHARGER PG 45

CLOCK SLG8SP585V (QFN-64) PG 15

FAN & THERMAL EMC1422 (8P TSSOP) PG 37

Clarksfield (Qual Core) (989 PGA) PG 3,4,5,6

DDR3-SODIMM1 PG 13 — 800 / 1066 MHZ DDR III

DDR3-SODIMM2 PG 14 — 800 / 1066 MHZ DDR III

PCIEx16

AMD M96XT PCI EXPRESS GFX (962 FCBGA) PG 17,18,19,20

- HDMI → **HDMI CONN.** PG 23
- DP → **DISPLAYPORT** PG 23
- LVDS → **Panel Connector** PG 24
- VGA → **CRT CONN.** PG 25

DDR3 x 8 (1G, 64Mx16 bit) (100P FBGA) PG 21,22

GPU THERMAL ANALOG DEVICES ADM1032 (8 MSOP) 3 x 3 mm PG 20

DMI x 4

Ibex Peak-M PG 7,8,9,10,11,12

IHDA

AUDIO IDT 92HD73C (56 LQFP) 9 x 9 mm PG 38

- **Subwoofer CONN** PG 40 ← **Subwoofer AMP MAXIM MAX9759** (16 Pin TQFN) PG 40
- **MIC**
- **Internal Speaker** ← **Amplifier TI TPA6040A4** (32 Pin QFN) PG 39
- **HP2**
- **HP1** ← **Amplifier TI TPA4411MRTJR** (20 Pin QFN) PG 39
- **Camera + D-MIC** PG 35 — USB2.0 [11]
- **TV CONN** PG 33 — USB2.0 [9]
- **USB CONN** — USB2.0 x 2 [0:1]
- **USB/eSATA Combo** PG 33 & eSATA board — USB2.0 [8]
- **SATA-ODD** PG 34 — SATA2 [A5]
- **SATA-HDD** PG 34 — SATA2 [A1]
- SATA2 [A0]
- PCIE [5] → **PC Card/1394 RICOH R5U230** (48 Pin QFN) 6 x 6 mm PG 26
- **1394 CONN** PG 27
- **CardReader CONN** PG 27

PCIE [1] / USB2.0 [5] → **WWAN MINI-CARD** PG 32

PCIE [2] / USB2.0 [4] → **WLAN Half MINI-CARD** PG 31

PCIE [3] / USB2.0 [6] → **UWB/BT MINI-CARD** PG 32

PCIE [4] / USB2.0 [7] → **Express Card** PG 28 → **Express Switch RICOH R5538D001** (20 QFN) 4 x 4 mm PG 28

PCIE [6] → **LAN Broadcom BCM5784M** (68P QFN) PG 41 → **Magnetic** PG 42 → **RJ45** PG 42

LPC

SIO ITE ITE8512E (128 Pin LQFP) 16 x 16 mm PG 29

- SPI → **SPI ROM 2MB** (8 Pin SO8W) PG 30
- **Keyboard** PG 35
- **CIR** PG 30
- **Touchpad**
- SMBus [2] → **Media Button**
- PS/2

LED PG 36

RTC PG 30

PAD & SCREW & SPRING PG 44

System Reset Circuit PG 43

To IO Board (USB*2/ MIC/ HP2/ HP1/ LED) PG 40

To Daughter Board (Power Button/Speaker/ KB LED/Touch PAD/ Media Button) PG 35

RM5 MB PCB (rev D)

QUANTA COMPUTER

Title	BLOCK DIAGRAM	
Size	Document Number: Calpella	Rev: 3A
Date: Thursday, August 20, 2009	Sheet 1 of 61	

Table of Contents

Power States

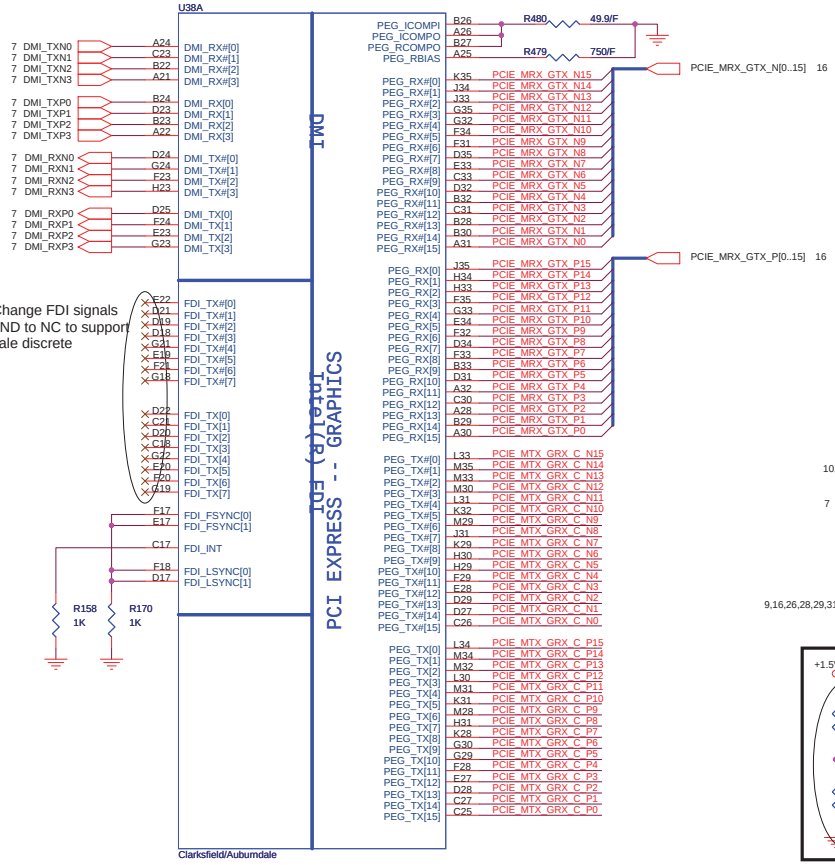
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48, 49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31, 32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
AGND	38,39,40	
AGND_DC/DC	51	
AGND_VCORE	50	
GND	ALL	

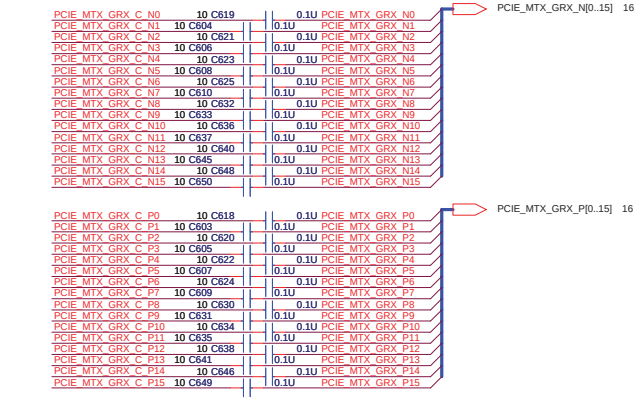
QUANTA COMPUTER

Title	FRONTPAGE	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 2 of 61	

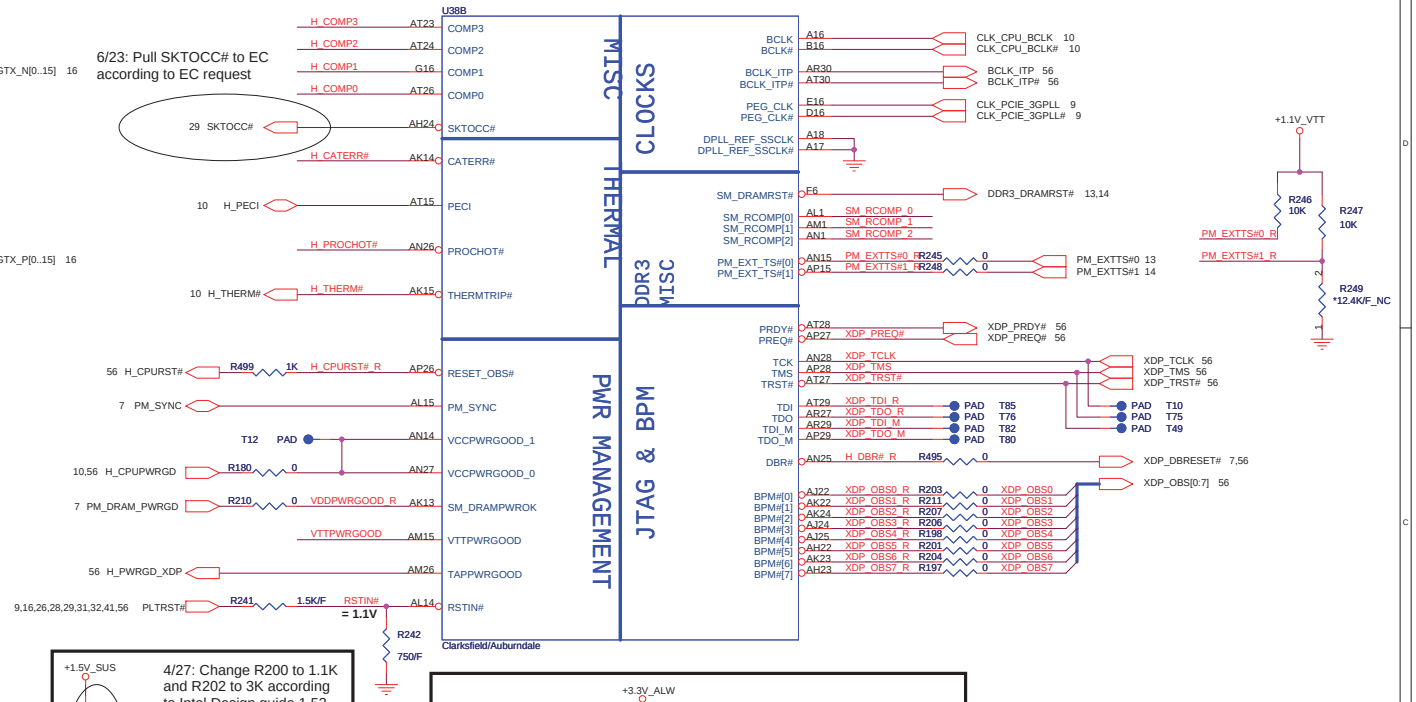
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



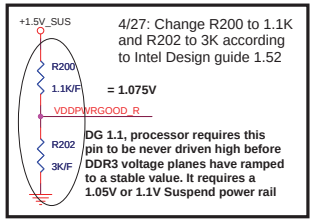
5/14: Change FDI signals from GND to NC to support Arrandale discrete

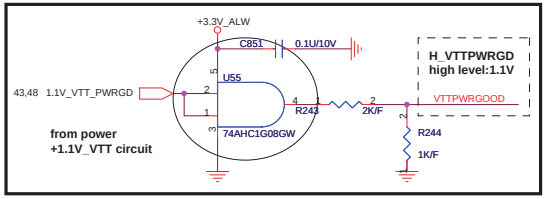


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

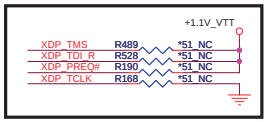


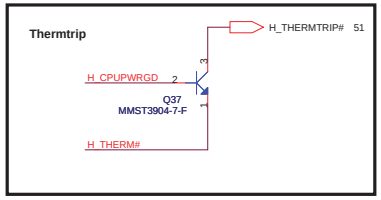
6/23: Pull SKTOCC# to EC according to EC request

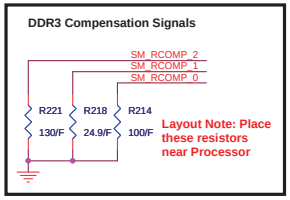


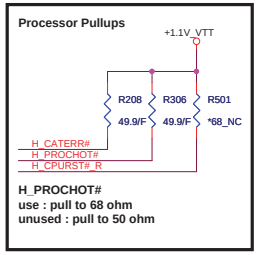


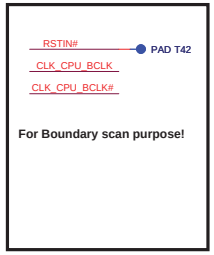
5/3: Added buffer to prevent power good voltage to fluctuate

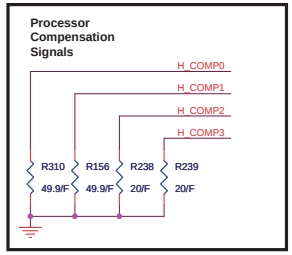


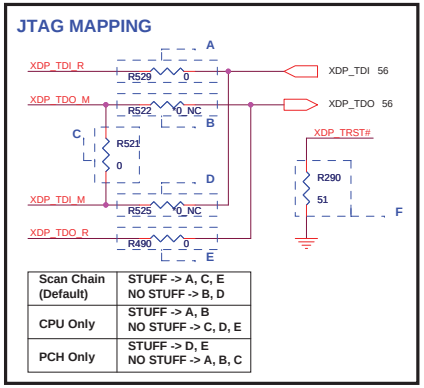








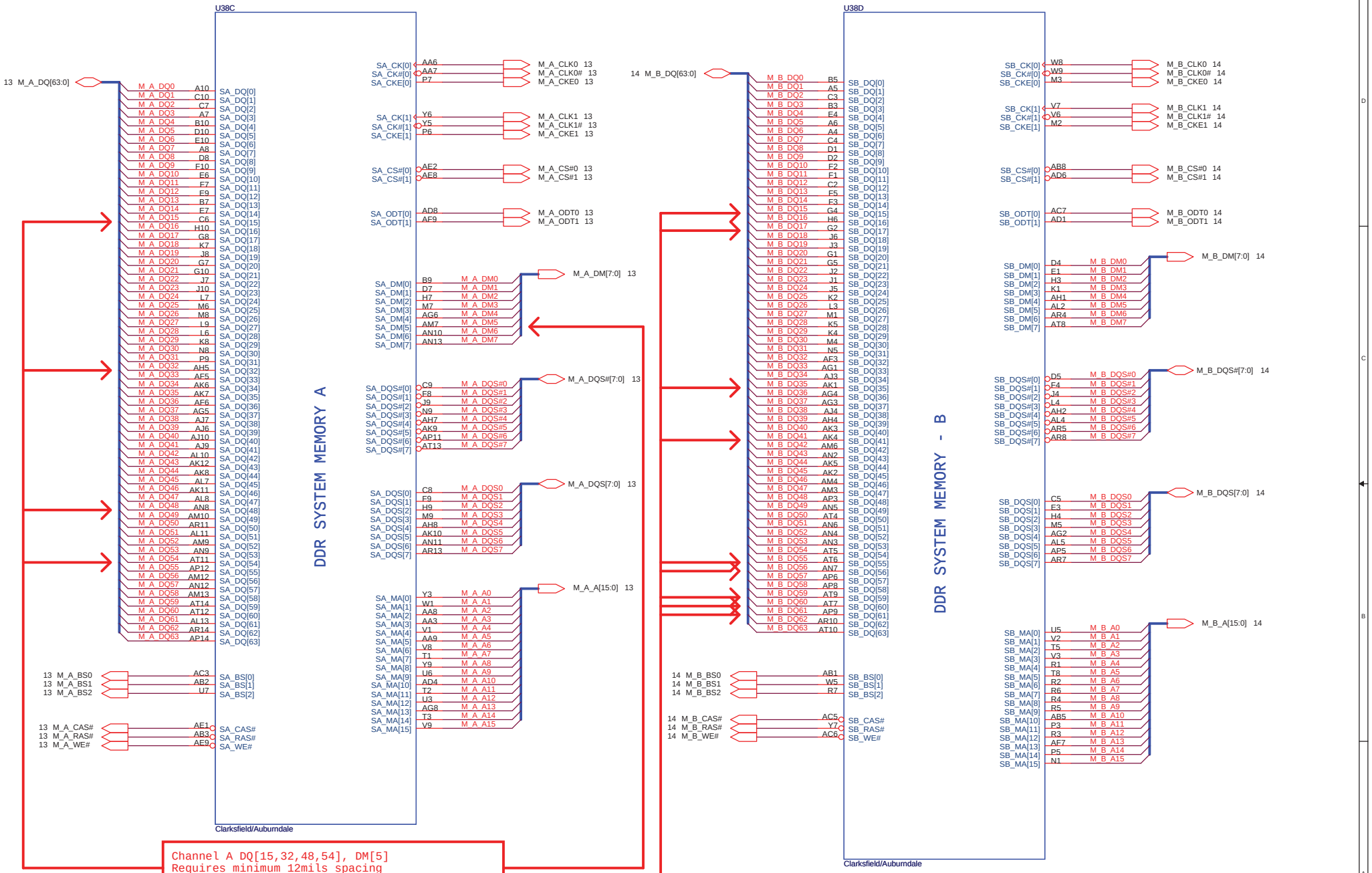




QUANTA COMPUTER

Title	CPU 1/4(PEG/DMI)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 3 of 61	

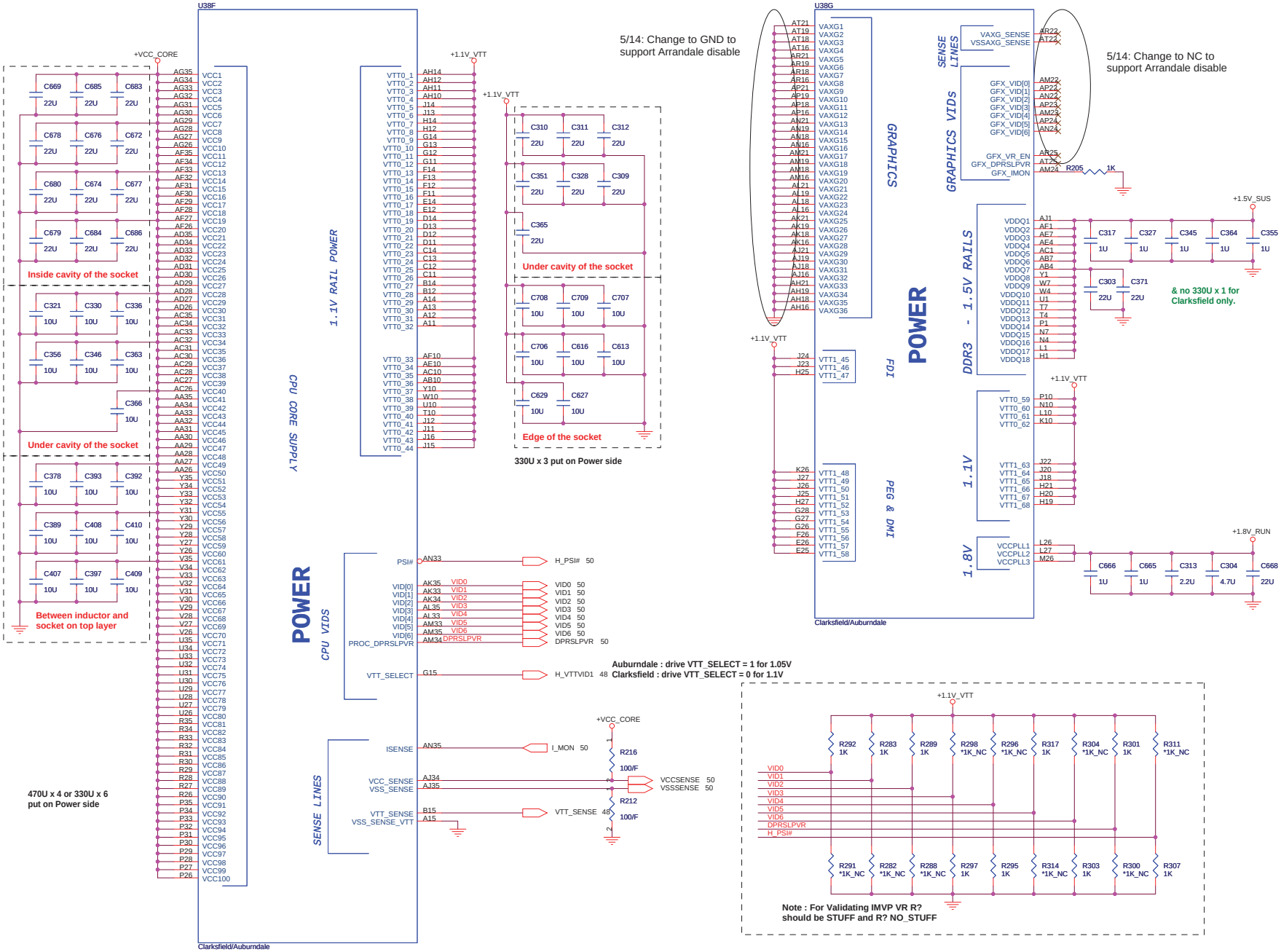
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



QUANTA COMPUTER

Title	CPU 2/4(DDR)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 4 of 61	

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



5/14: Change to GND to support Arrandale disable

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

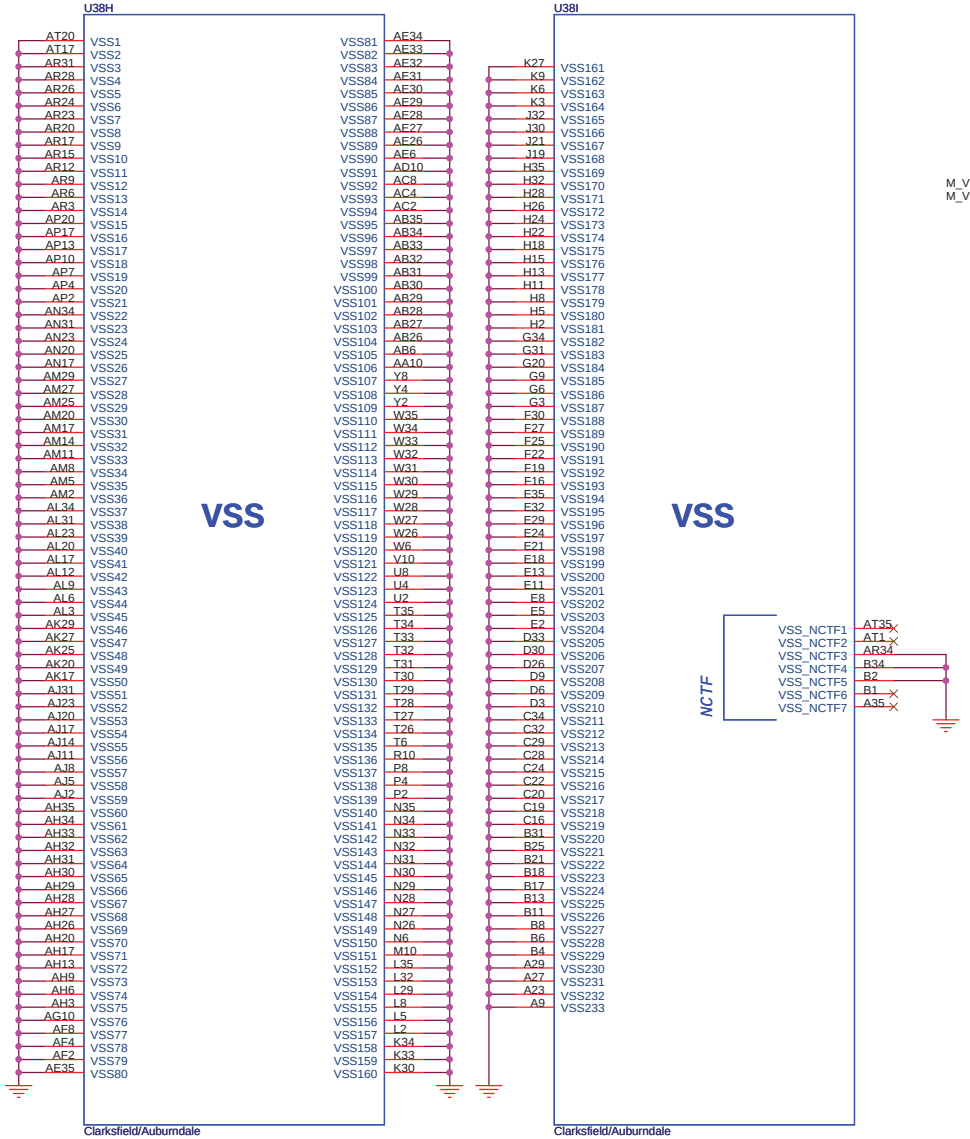
5/14: Change to NC to support Arrandale disable

Auburndale : drive VTT_SELECT = 1 for 1.05V
Clarksfield : drive VTT_SELECT = 0 for 1.1V

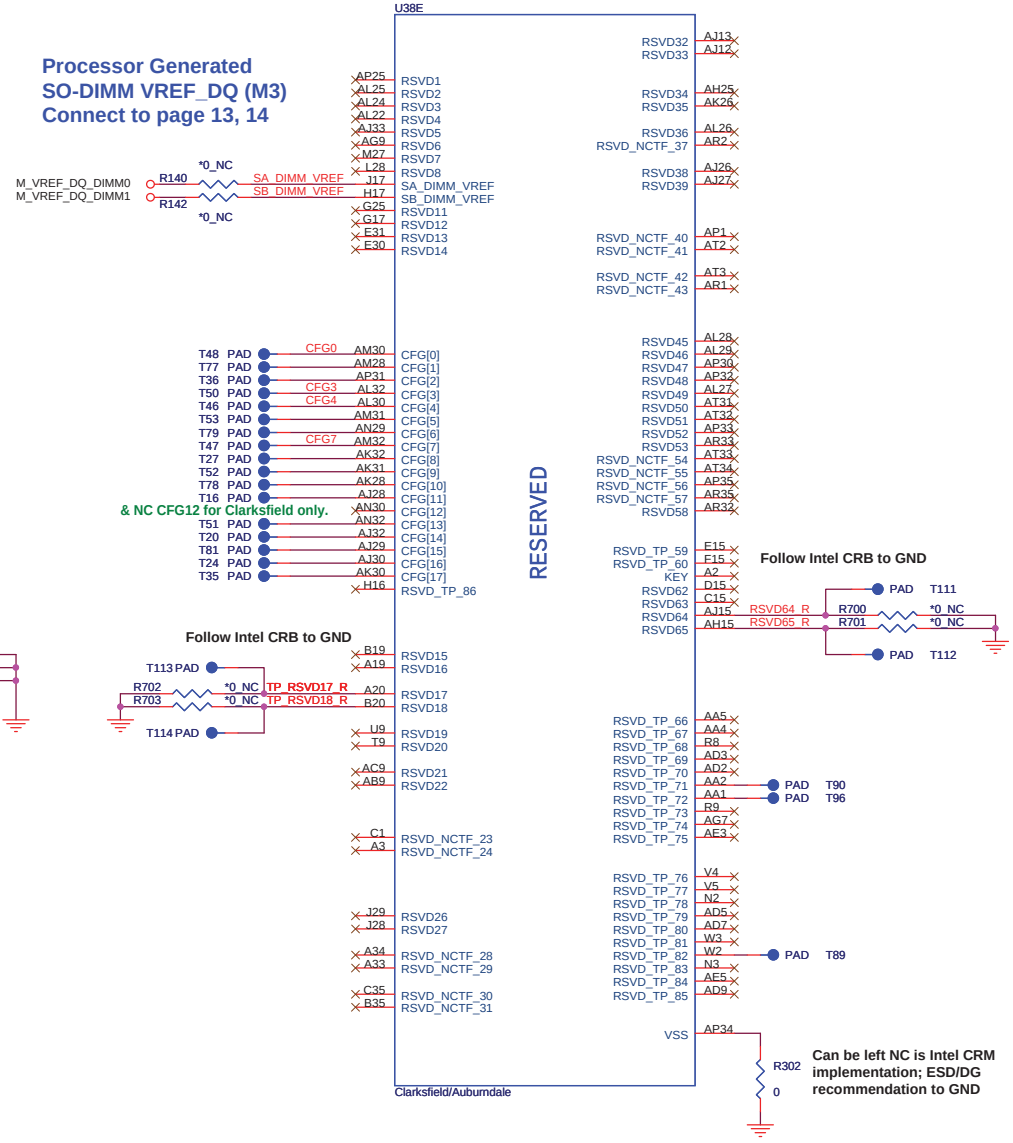
Title	CPU 3/4(POWER)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 5 of 61	

QUANTA COMPUTER

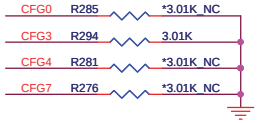
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Scott_0630:Change R294 footprint from RC0402-C to RC0402



The Clarksfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

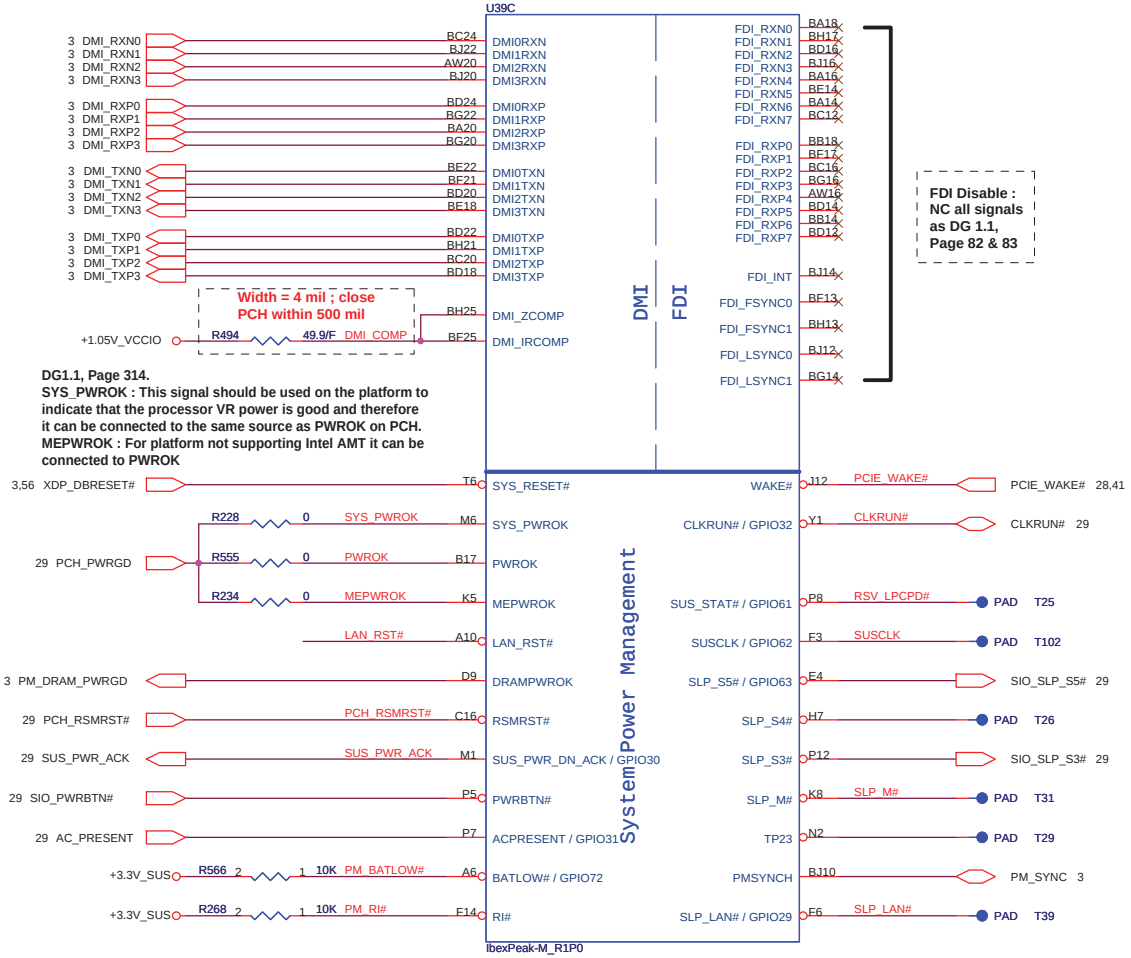
	1	0
CFG0 (PCI-Epress Configuration Select)	**Single PEG (Default)**	**Bifurcation enabled**
CFG3 (PCI-Epress Static Lane Reversal)	**Normal Operation (Default)**	**Lane Numbers Reversed**
CFG4 (Display Port Presence)	**Disabled; No Physical Display Port attached to Embedded Diplay Port (Default)**	**Enabled; An external Display port device is connected to the Embedded Display port**
CFG7 Clarksfield (only for early samples pre-ES1)	**Common motherboard design**	**For early samples pre-ES1 CFD (Default)**

Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

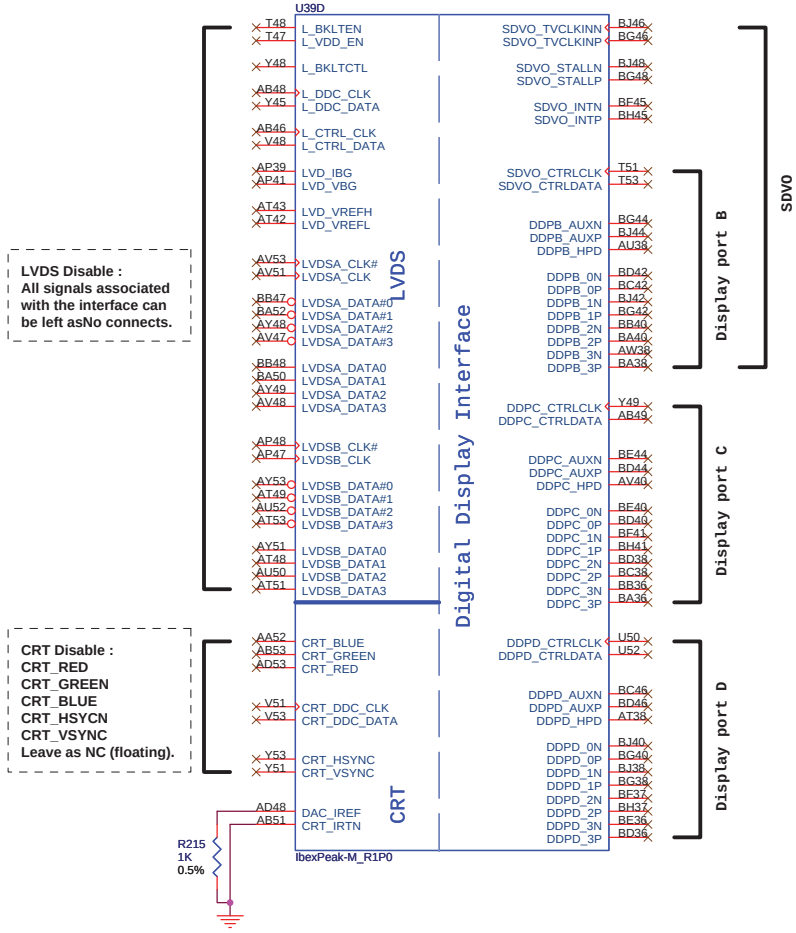
QUANTA COMPUTER

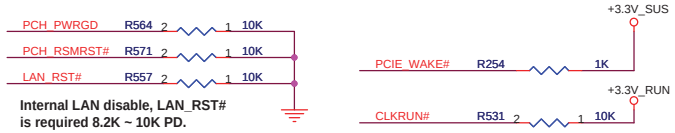
Title	CPU 4/4(GND_RESV)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 6 of 61	

IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)





Title	PCH 1/6(DMI_VIDEO)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 7 of 61	

IBEX PEAK-M (HDA,JTAG,SATA)

+RTC_CELL
R570 1M
R568 20K
R574 20K
C700 1U/10V
C699 1U/10V

Cap values depend on Xtal
C701 15P/50V
C696 15P/50V
Y3 32.768KHZ
R552 10M
RTC_X1
RTC_X2

INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

38 ICH_AZ_CODEC_BITCLK — R562 33 — ACZ_BIT_CLK
C703 *27P/50V_NC
38 ICH_AZ_CODEC_SYNC — R273 33 — ACZ_SYNC
29,38 ICH_AZ_CODEC_RST# — R561 33 — ACZ_RST#
38 ICH_AZ_CODEC_SDOUT — R573 33 — ACZ_SDOUT

Place all series terms close to PCH (within 500 mil) except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

+3.3V_RUN — R545 *1K_NC — SPKR

Scott_0630:Change R545 footprint from RC0402-C to RC0402.

R261 *1K_NC GPIO33

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K_NC to 1K_NC according to Intel design guide 1.51

U39A

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0 / LAD0 D33, FWH1 / LAD1 B33, FWH2 / LAD2 C32, FWH3 / LAD3 A32, FWH4 / LFRAME# C34, LDRQ0# A34, LDRQ1# / GPIO23 F34, SERIRQ AB9
IHDA: HDA_BCLK A30, HDA_SYNC D29, SPKR P1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29, HDA_DOCK_EN# / GPIO33 H32, HDA_DOCK_RST# / GPIO13 J30
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1
SATA: SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9, SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8, SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6, SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AE3, SATA3TXP AE1, SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5, SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO AF16, SATAICOMPI AF15, SATALED# T3, SATA0GP / GPIO21 Y9, SATA1GP / GPIO19 V1

IbexPeak-M_R1P0

LPC_LAD0 29,32 / LPC_LAD1 29,32 / LPC_LAD2 29,32 / LPC_LAD3 29,32
LPC_LFRAME# 29,32
PAD T92 / PAD T34
IRQ_SERIRQ 29

HDD: SATA_RX0- 34, SATA_RX0+ 34, SATA_TX0-_C 34, SATA_TX0+_C 34
ODD: SATA_RX1- 34, SATA_RX1+ 34, SATA_TX1-_C 34, SATA_TX1+_C 34
E-SATA: SATA_RX5- 33, SATA_RX5+ 33, SATA_TX5-_C 33, SATA_TX5+_C 33

Notes : Put AC Coupling Cap. near device side. As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

Notes : FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

within 500 mils of the PCH
SATA_COMP R213 37.4/F +1.05V_PCH

PU 10K to +3.3V_RUN at Page 38
SATA_ACT# 36
R188 10K
R537 10K +3.3V_RUN

6/2: NC JTAG resistors as PCH is in QT stage

+3.3V_SUS
Res. of TDI near PCH
R236 *200_NC, R251 *200_NC, R263 *200_NC, R259 *20K_NC
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R546 *100_NC, R547 *100_NC, R549 *100_NC, R548 *10K_NC

Scott_0707: Reserver PCH_JTAG_RST# circuit as review.

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

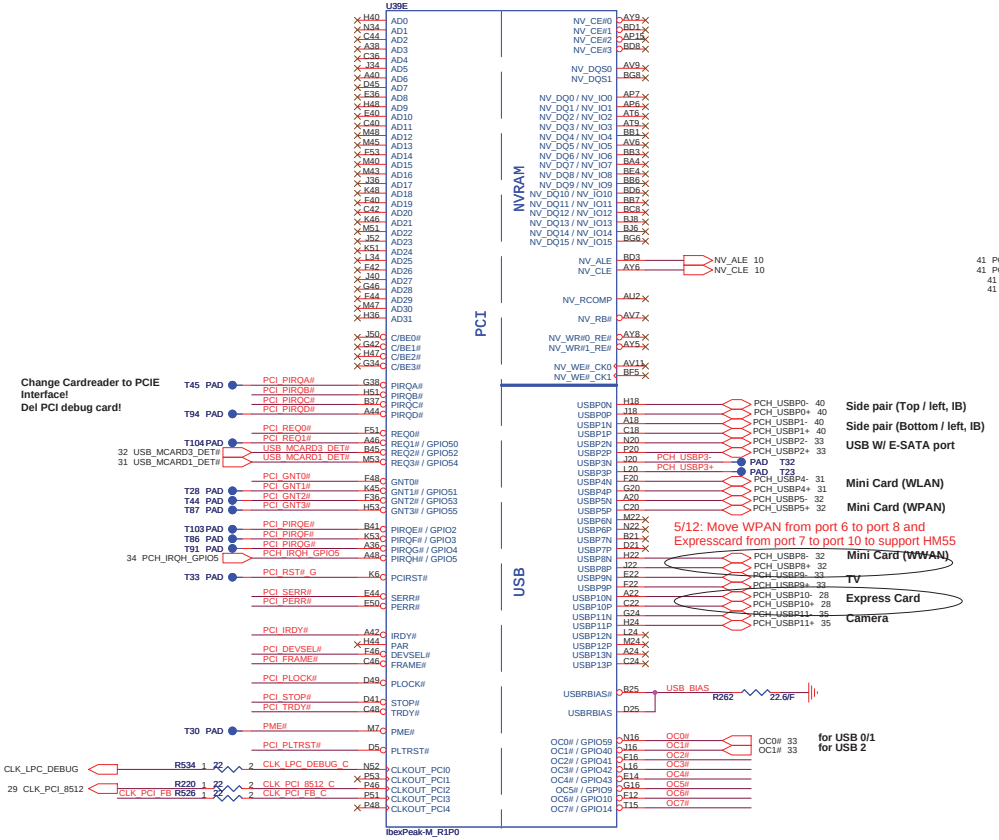
Scott_0703 : Note : Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)

PCH_JTAG_TCK_BUF
R544 51

QUANTA COMPUTER

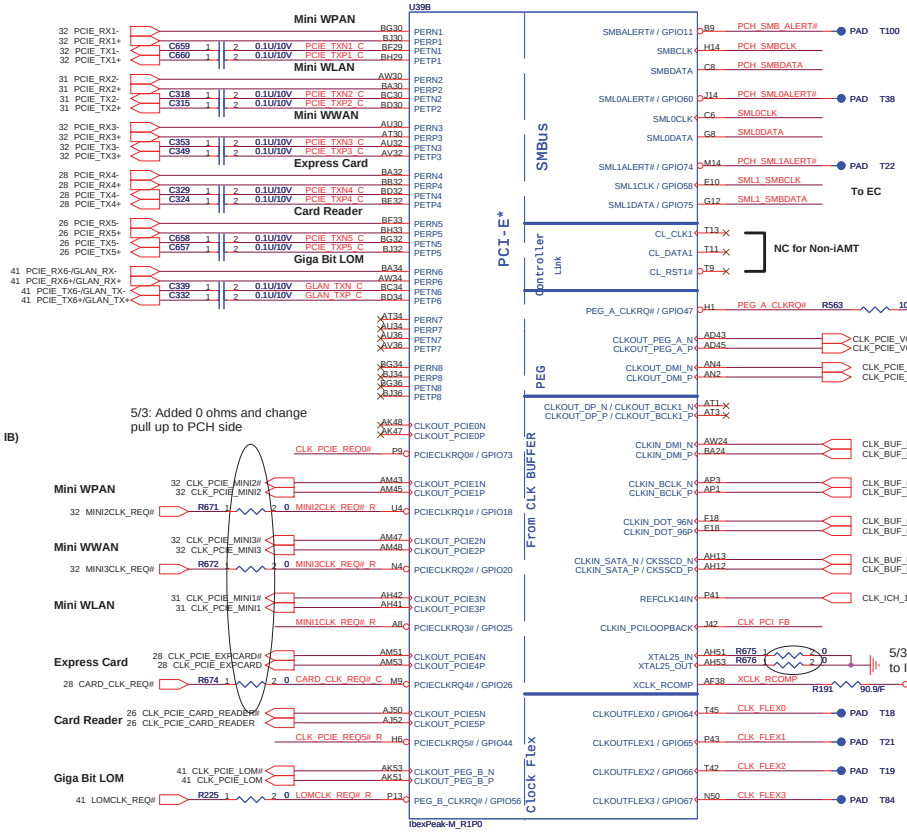
Title	PCH 2/6(SATA_SPI)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 8 of 61	

IBEX PEAK-M (PCI,USB,NVRAM)



5/12: Move WPAN from port 6 to port 8 and Expresscard from port 7 to port 10 to support HM55

IBEX PEAK-M (PCI-E,SMBUS,CLK)



5/3: Added 0 ohms and change pull up to PCH side

5/3: Added 0 ohms to GND according to Intel reccomandation

5/13: Added MOSFET Q81 to prevent leakage from 3.3V_SUS to cardreader during S3

5/4: Added MOSFET Q80 to prevent leakage from 3.3V_SUS to cardreader during S3

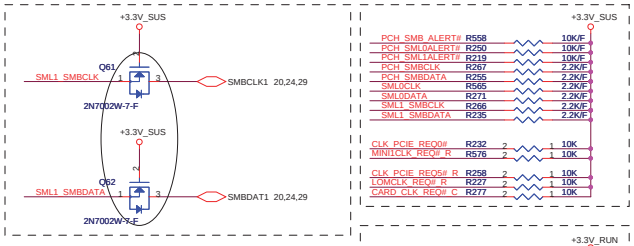
5/12: Depop R226 and R229 as BIOS decided to boot from SPI ROM connected to PCH

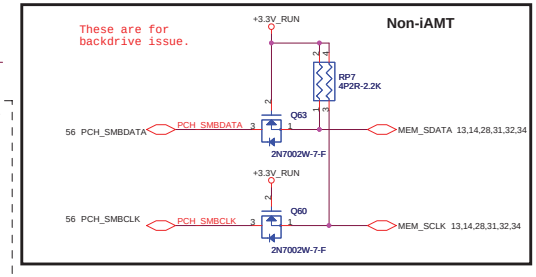
5/19: Update BIOS strap table

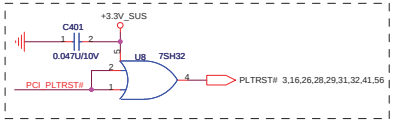
Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

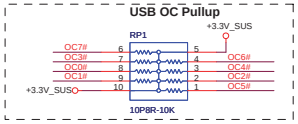
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	0 = A16 swap override/Top-Block Swap Override enabled 1 = Default

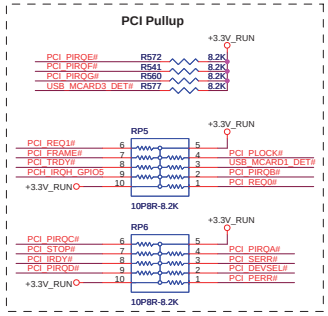
4/28: Change polarity to prevent leakage

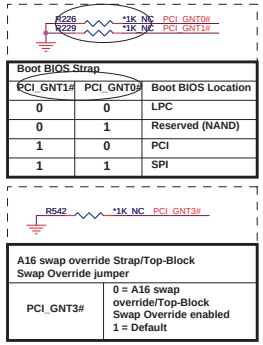








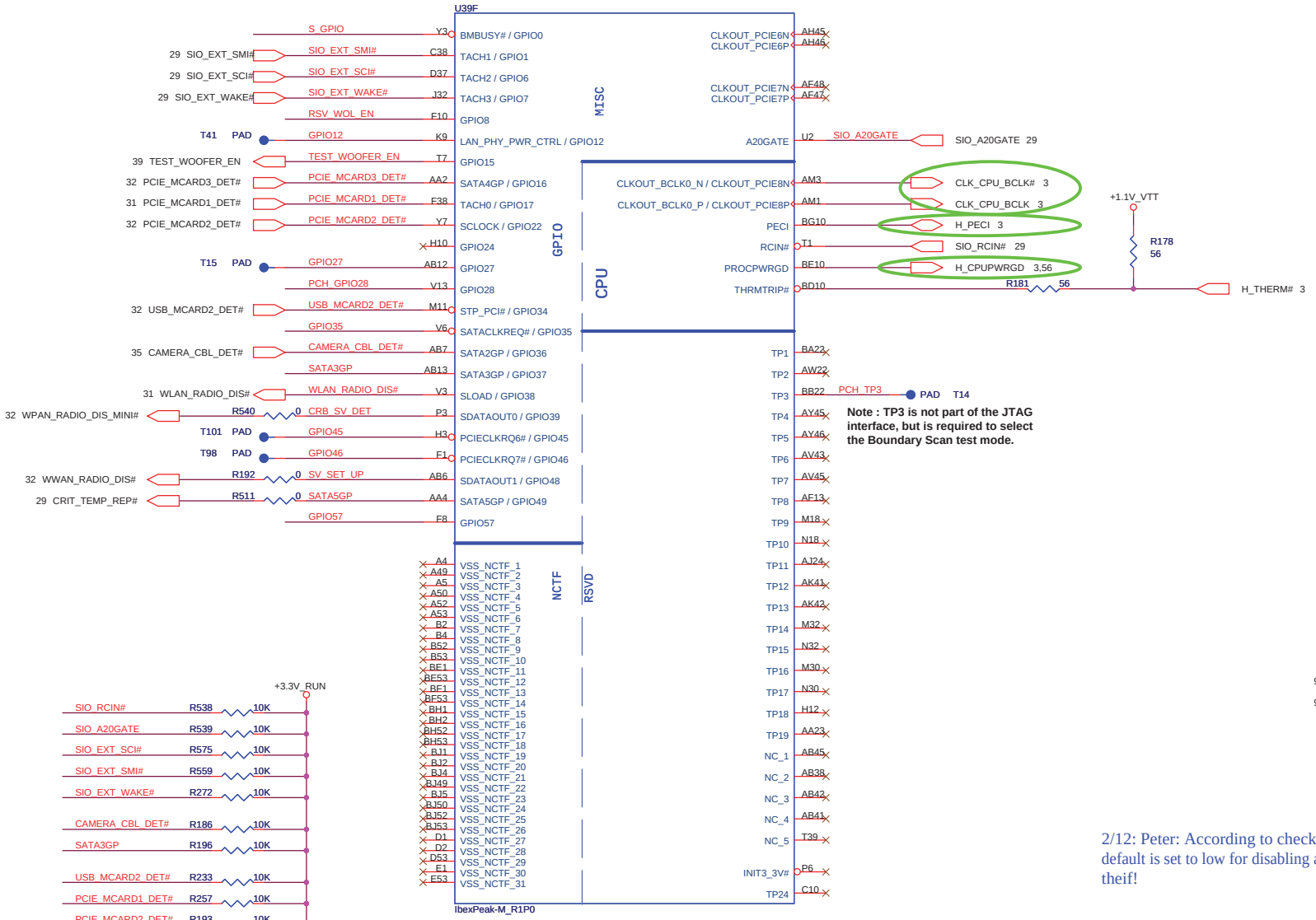


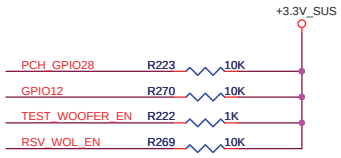


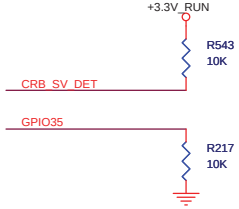
Title	PCH 3/6(PCI_SMBUS_CLK)
Size	Document Number RM5 — Rev 3A
Date: Thursday, August 20, 2009	Sheet 9 of 61

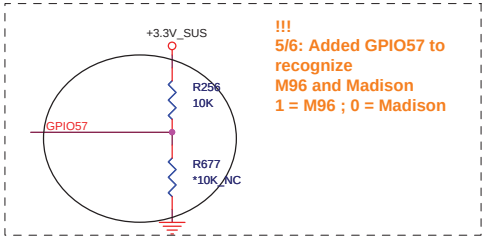
QUANTA COMPUTER

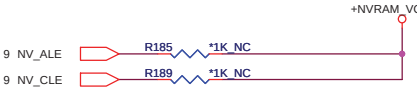
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)







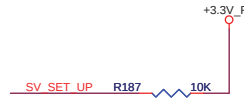




DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Anti-Thief Enabled	
NV_ALE	High = Enable (Default) Low = Disable

2/12: Peter: According to checklist, default is set to low for disabling anti - theif!

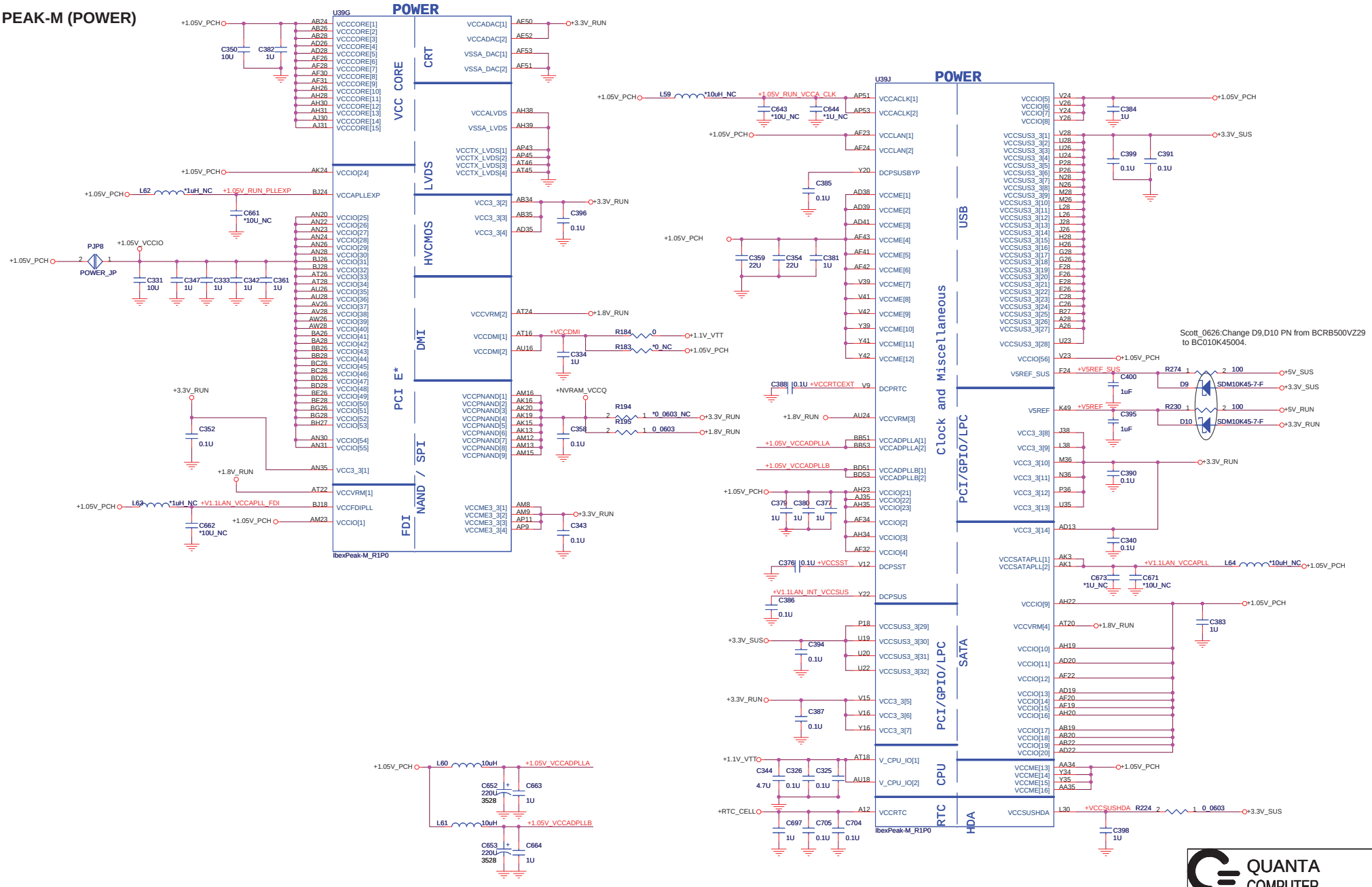


SV_SET_UP	1-X High = Strong (Default)

QUANTA COMPUTER

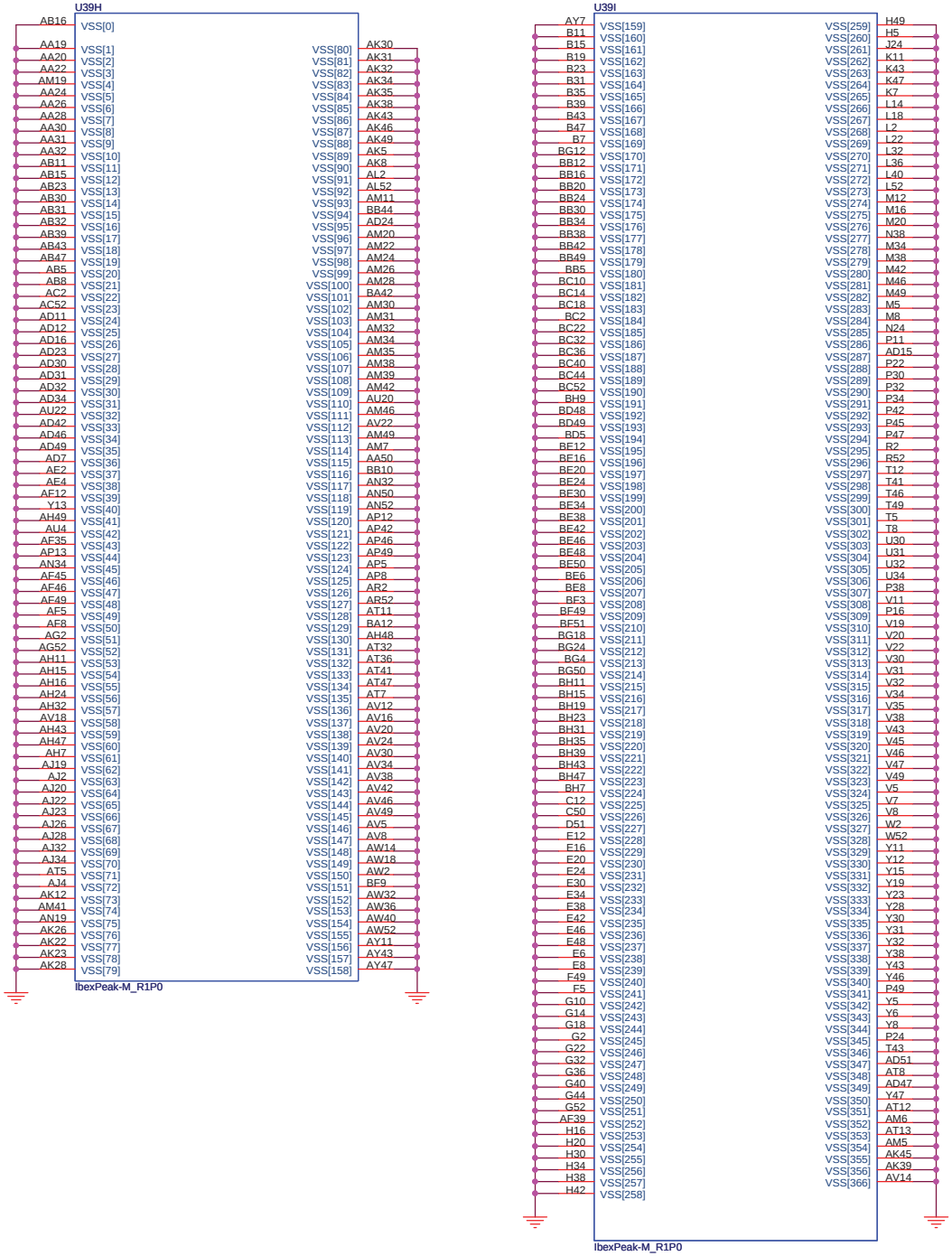
Title	PCH 4/6(GPIO)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 10 of 61	

IBEX PEAK-M (POWER)



Title	PCH 5/6(POWER)
Size	Document Number RM5
Rev	3A
Date:	Thursday, August 20, 2009
Sheet	11 of 61

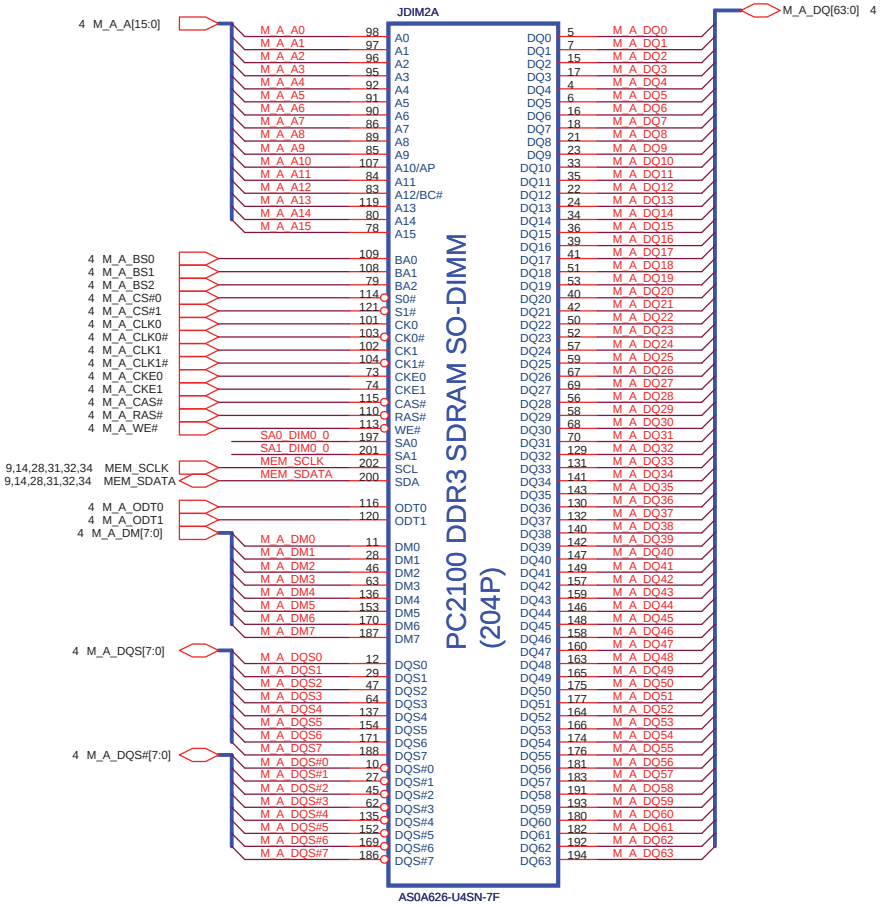
IBEX PEAK-M (GND)



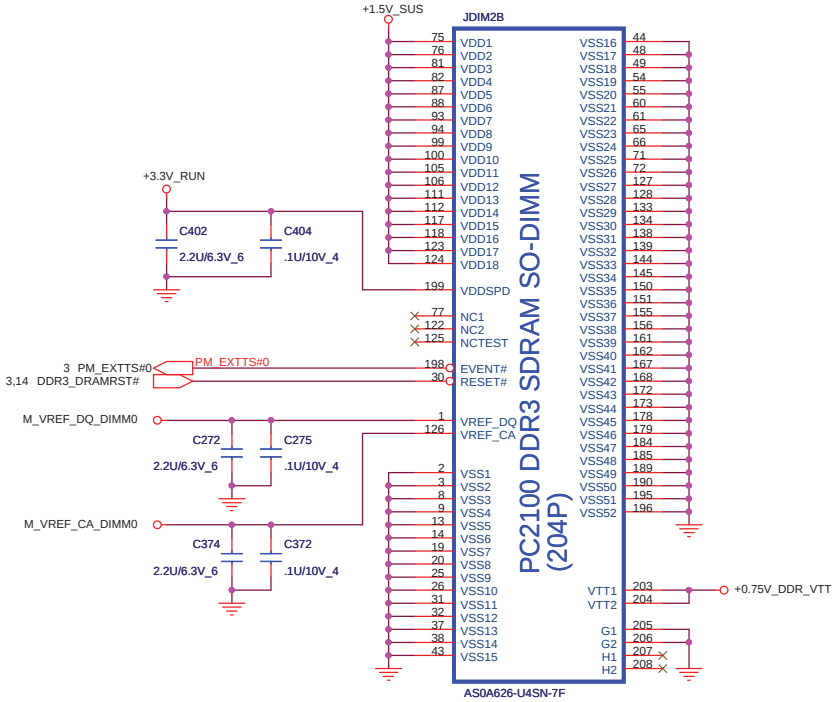
QUANTA COMPUTER

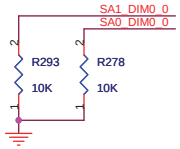
Title	PCH 6/6(GND)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 12 of 61	

5/13: Change connector from Tyco to Foxconn to avoid shortage



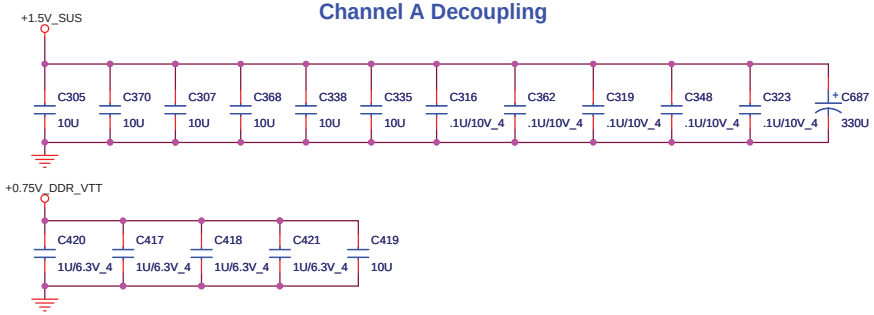
Channel A





Note:
If SA1_DIM0 = 0, SA0_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA1_DIM0 = 0, SA0_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Channel A Decoupling



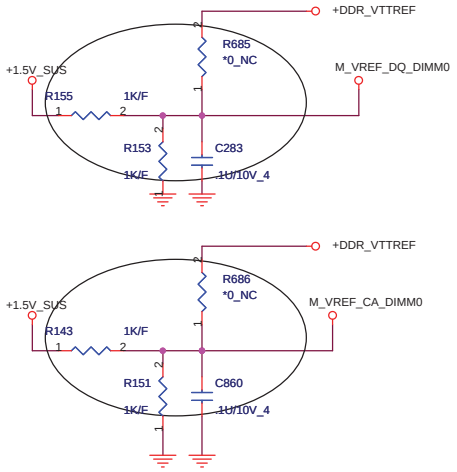
For CH A SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM0 and M_VREF_CA_DIMM0 to follow Intel CRB design

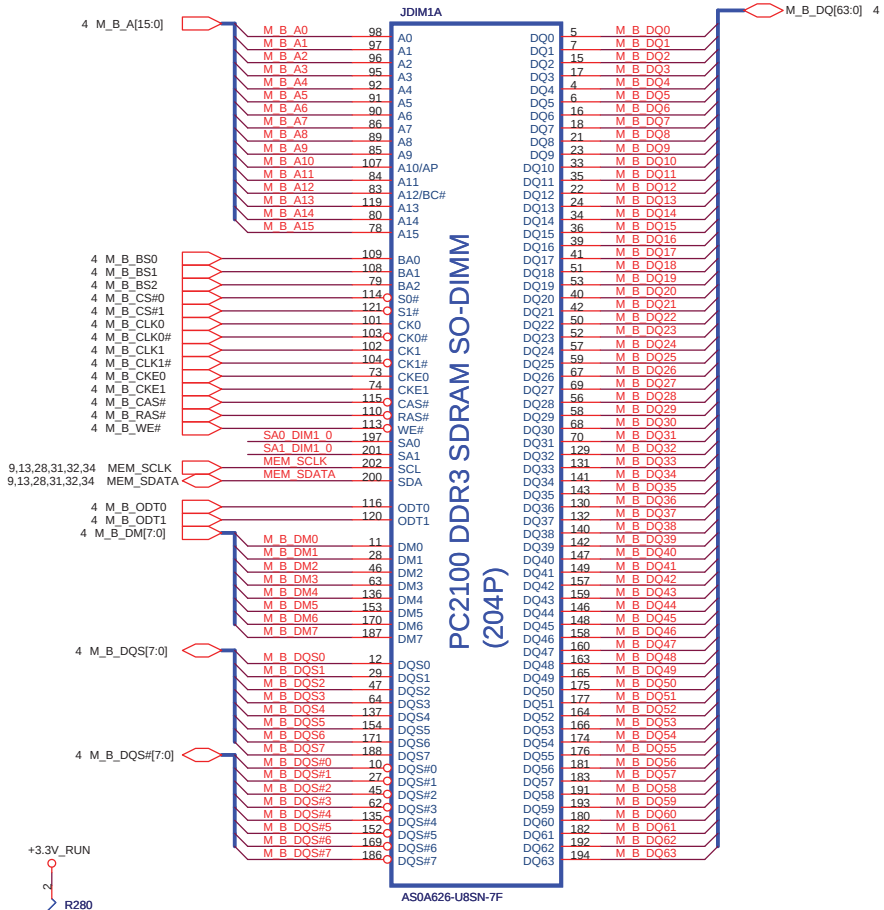
6/02: Change M1 from voltage regulator to voltage divider

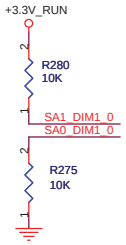


QUANTA COMPUTER

Title	DDR3 DIMM-A	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 13 of 61	

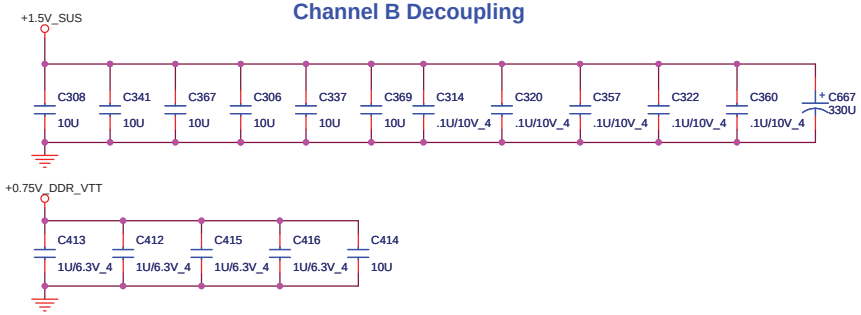
5/13: Change connector from Tyco to Foxconn to avoid shortage



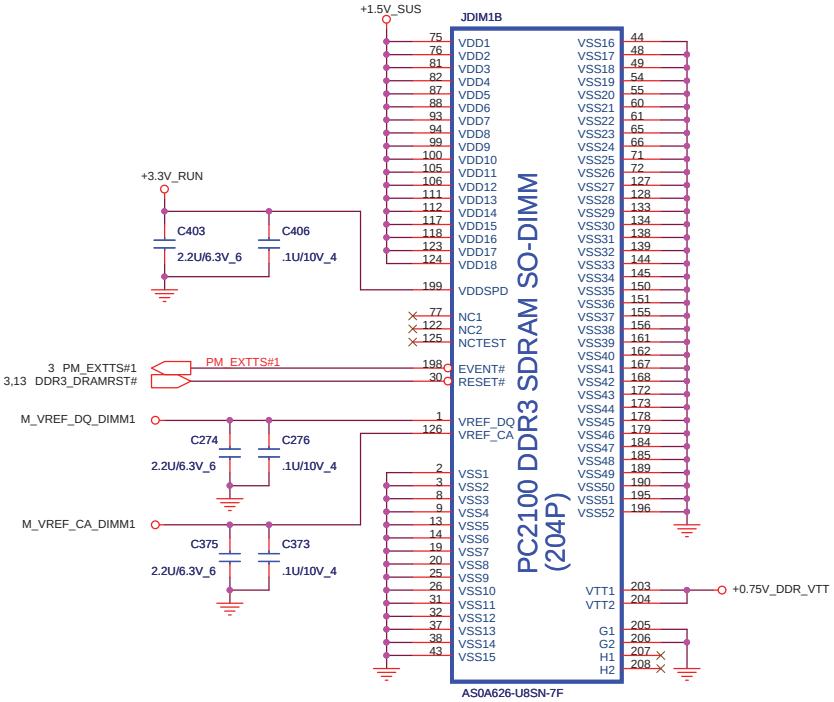


Note:
If SA1_DIM1 = 1, SA0_DIM1 = 0
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34
If SA1_DIM1 = 1, SA0_DIM1 = 1
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36

Channel B Decoupling



Channel B



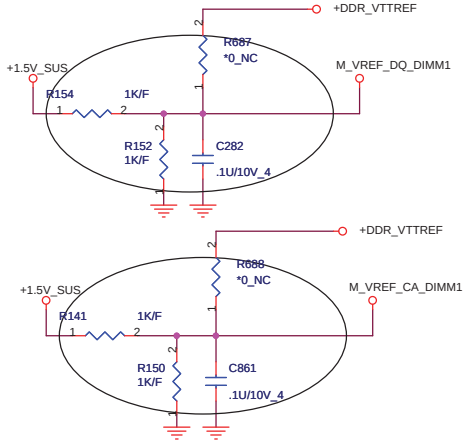
For CH B SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

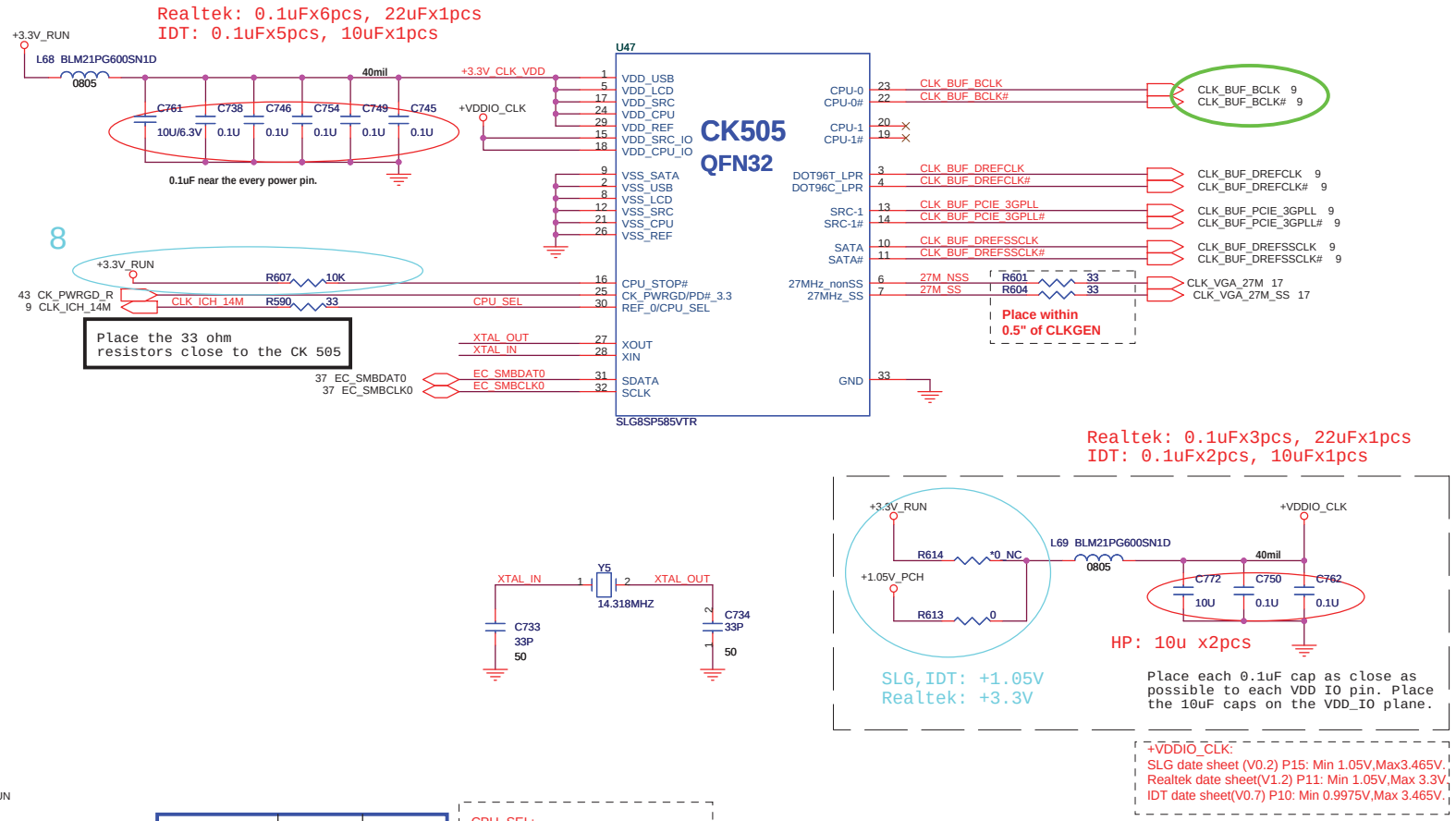
5/18: Separate voltage divider for M_VREF_DQ_DIMM1 and M_VREF_CA_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider



QUANTA COMPUTER

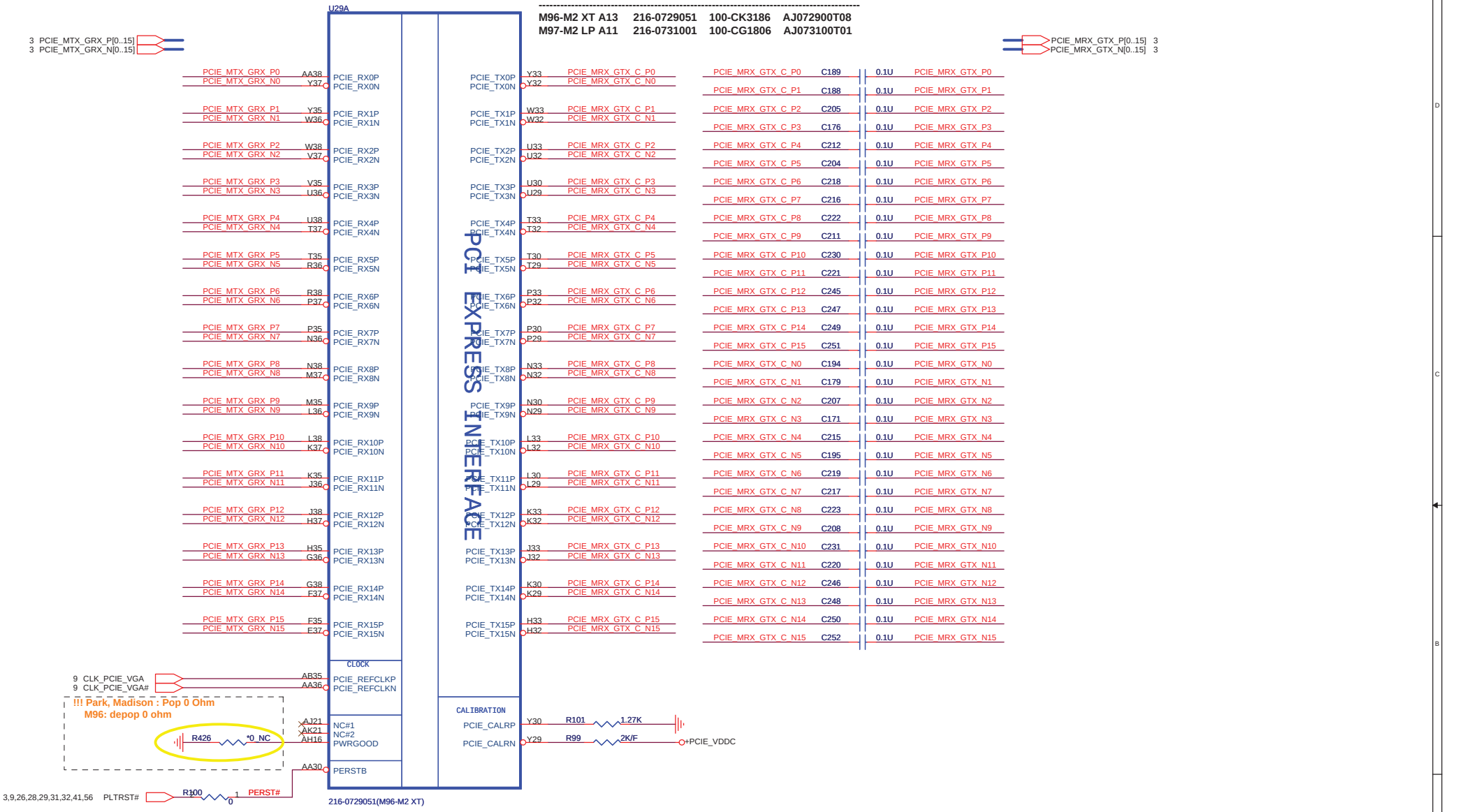
Title	DDR3 DIMM-B	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 14 of 61	



QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 15 of 61	

ASIC	PN	100-CK	QCI P/N
M96-M2 XT A13	216-0729051	100-CK3186	AJ072900T08
M97-M2 LP A11	216-0731001	100-CG1806	AJ073100T01



Title	M96XT_PCIE		
Size	Document Number RM5		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 16 of 61	

Memory Straps		RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
800 MHz 512MB(32M*16) Hynix_Tiva die	H5TQ5163MFR-12	1	1	1	1
reserve for Qimonda		1	1	1	0
reserve for Samsung		1	1	0	1
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	1	0	1	1
800 MHz 1GB(64M*16) Qimonda_A1 die	IDGH1G-04A1F1C-16X	1	0	1	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	1	0	0	1

Note : Required Frequency = 800 MHz

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

VRAM TYPE

APERTURE SIZE

!!! NC when M92-M2

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

(1.8V @ 70mA AVDD)

(1.8V @ 45mA VDD1DI)

(1.8V @ 40mA VDD2DI)

(1.8V @ 20mA A2VDDQ)

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

!!! (1.1V @ 150mA DPLL_VDDC) (1.0V @ 150mA DPLL_VDDC for M97)

(1.8V @ 20mA TSVDD)

Reserve 0 ohm for Dual mode DDC/AUX

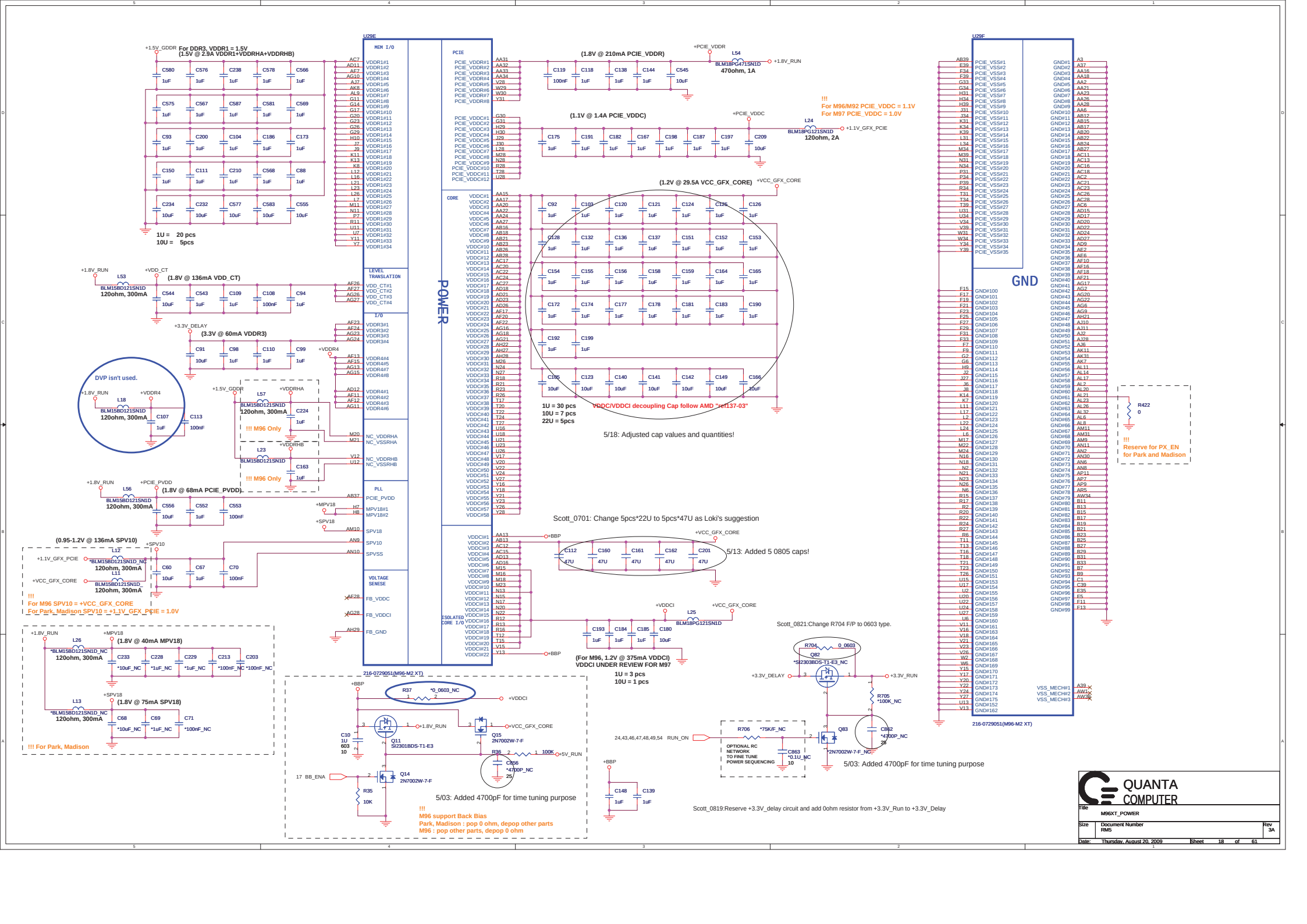
!!! NC when M92-M2

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

Scott_0703:Delete Spread Spectrum XTAL circuit as placement required of thermal issue.

216-0729051(M96-M2 XT)

Title	M96XT_IO & STRAP		
Size	Document Number RM5		Rev 3A
Date: Thursday, August 20, 2009	Sheet 17 of 61		


U29E
MEM I/O
PCIE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
CORE
ISOLATED CORE I/O
+1.5V_GDDR
For DDR3, VDDR1 = 1.5V
(1.5V @ 2.9A VDDR1+VDDRHA+VDDRHB)
1U = 20 pcs
10U = 5pcs
(1.8V @ 210mA PCIE_VDDR)
BLM18PG471SN1D
470ohm, 1A
+1.8V_RUN
+PCIE_VDDR
(1.1V @ 1.4A PCIE_VDDC)
BLM18PG121SN1D
120ohm, 2A
+1.1V_GFX_PCIE
+PCIE_VDDC
!!!
For M96/M92 PCIE_VDDC = 1.1V
For M97 PCIE_VDDC = 1.0V
(1.2V @ 29.5A VCC_GFX_CORE)
+VCC_GFX_CORE
VDDC/VDDCI decoupling Cap follow AMD "rel137-03"
1U = 30 pcs
10U = 7 pcs
22U = 5pcs
5/18: Adjusted cap values and quantities!
(1.8V @ 136mA VDD_CT)
BLM15BD121SN1D
120ohm, 300mA
+1.8V_RUN
+VDD_CT
(3.3V @ 60mA VDDR3)
+3.3V_DELAY
+VDDR4
DVP isn't used.
(1.8V @ 68mA PCIE_PVDD)
+PCIE_PVDD
(0.95-1.2V @ 136mA SPV10)
+SPV10
+1.1V_GFX_PCIE
+VCC_GFX_CORE
!!!
For M96 SPV10 = +VCC_GFX_CORE
For Park, Madison SPV10 = +1.1V_GFX_PCIE = 1.0V
(1.8V @ 40mA MPV18)
+MPV18
(1.8V @ 75mA SPV18)
+SPV18
!!! For Park, Madison
+VDDRHA
+VDDRHB
!!! M96 Only
BLM15BD121SN1D_NC
*BLM15BD121SN1D_NC
120ohm, 300mA
Scott_0701: Change 5pcs*22U to 5pcs*47U as Loki's suggestion
5/13: Added 5 0805 caps!
+BBP
(For M96, 1.2V @ 375mA VDDCI)
VDDCI UNDER REVIEW FOR M97
1U = 3 pcs
10U = 1 pcs
+VDDCI
Scott_0821:Change R704 F/P to 0603 type.
R704
0_0603
Q82
*SI2303BDS-T1-E3_NC
R705
*100K_NC
Q83
*2N7002W-7-F_NC
R706
*75K/F_NC
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
C863
*0.1U_NC
24,43,46,47,48,49,54 RUN_ON
5/03: Added 4700pF for time tuning purpose
Scott_0819:Reserve +3.3V_delay circuit and add 0ohm resistor from +3.3V_Run to +3.3V_Delay
216-0729051(M96-M2 XT)
R37
*0_0603_NC
Q11
SI2301BDS-T1-E3
Q15
2N7002W-7-F
Q14
2N7002W-7-F
R36
100K
C856
*4700P_NC
R35
10K
17 BB_ENA
+5V_RUN
!!!
M96 support Back Bias
Park, Madison : pop 0 ohm, depop other parts
M96 : pop other parts, depop 0 ohm
U29F
GND
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
R422
0
!!!
Reserve for PX_EN
for Park and Madison
QUANTA COMPUTER
Title
M96XT_POWER
Size
Document Number
RM5
Rev
3A
Date: Thursday, August 20, 2009
Sheet 18 of 61

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

DPC & DPD aren't used.

U29H

DP C/D POWER | DP A/B POWER

+DPC_VDD18
AP20 DPC_VDD18#1
AP21 DPC_VDD18#2
+1.1V_GFX_PCIE
AP13 DPC_VDD10#1
AT13 DPC_VDD10#2
C55 *100nF_NC
AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5
+DPD_VDD18
AP22 DPD_VDD18#1
AP23 DPD_VDD18#2
+1.1V_GFX_PCIE
AP14 DPD_VDD10#1
AP15 DPD_VDD10#2
C57 *100nF_NC
AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5

DPA_VDD18#1 AN24
DPA_VDD18#2 AP24
+DPA_VDD18
DPA_VDD10#1 AP31
DPA_VDD10#2 AP32
+DPA_VDD10
(1.1V @ 200mA DPA_VDD10)
L48 BLM15BD121SN1D 120ohm, 300mA
C519 100nF C520 1uF C521 10uF
+1.1V_GFX_PCIE
DPA for HDMI
DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26

DPB_VDD18#1 AP25
DPB_VDD18#2 AP26
+DPB_VDD18
DPB_VDD10#1 AN33
DPB_VDD10#2 AP33
+DPB_VDD10
(1.1V @ 200mA DPB_VDD10)
L16 BLM15BD121SN1D 120ohm, 300mA
C78 100nF C77 1uF C83 10uF
+1.1V_GFX_PCIE
DPB for DP
DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32

!!! For M97 Only

+DPA_VDD18
(1.8V @ 110mA DPA_VDD18)
L15 *BLM15BD121SN1D_NC 120ohm, 300mA
+1.8V_RUN
C80 *100nF_NC C74 *1uF_NC C73 *10uF_NC

+DPB_VDD18
(1.8V @ 110mA DPB_VDD18)
L14 *BLM15BD121SN1D_NC 120ohm, 300mA
+1.8V_RUN
C79 *100nF_NC C75 *1uF_NC C72 *10uF_NC

+DPC_VDD18
R59 1 *0_NC 2 +1.8V_RUN
C82 *100nF_NC

+DPD_VDD18
R58 1 *0_NC 2 +1.8V_RUN
C81 *100nF_NC

(1.8V @ 400mA DPE_VDD18;
200mA for DPE/DPF respectively)
+DPE_VDD18
+1.8V_RUN
L19 BLM18PG600SN1D 60ohm, 500mA
C97 10uF C95 1uF C96 100nF

0504: Change L19 for low DCR
0.1ohm as AMD suggest.

150/F R425 AW18
DPCD_CALR
DPAB_CALR
AW28 R424 150/F

DP E/F POWER | DP PLL POWER

DPE_VDD18#1 AH34
DPE_VDD18#2 AJ34
+DPE_VDD10
DPE_VDD10#1 AL33
DPE_VDD10#2 AM33

DPA_PVDD AU28
DPA_PVSS AV27
+DPA_PVDD
(1.8V @ 20 mA DPA_PVDD)
L49 BLM15BD121SN1D 120ohm, 300mA
+1.8V_RUN
C534 100nF C532 1uF C529 10uF

DPB_PVDD AV29
DPB_PVSS AR28
+DPB_PVDD
(1.8V @ 20 mA DPB_PVDD)
L50 BLM15BD121SN1D 120ohm, 300mA
+1.8V_RUN
C537 100nF C533 1uF C531 10uF

DPE & DPF for LVDS

DPE_VSSR#1 AN34
DPE_VSSR#2 AP39
DPE_VSSR#3 AR39
DPE_VSSR#4 AU37
DPE_VSSR#5 AW35

DPC & DPD aren't used.
+1.8V_RUN
C535 *100nF_NC
C536 *100nF_NC

DPC_PVDD AU18
DPC_PVSS AV17
DPD_PVDD AV19
DPD_PVSS AR18

+DPE_VDD18
DPF_VDD18#1 AE34
DPF_VDD18#2 AG34

(1.1V @ 200mA DPE_VDD10;
100mA for DPE/DPF respectively)
+DPE_VDD10
+1.1V_GFX_PCIE
L17 BLM15BD121SN1D 120ohm, 300mA
C86 10uF C84 1uF C85 100nF

DPF_VDD10#1 AK33
DPF_VDD10#2 AK34

DPE_PVDD AM37
DPE_PVSS AN38
+DPE_PVDD
(1.8V @ 40mA DPE_PVDD; 20mA
for DPE/DPF respectively)
L55 BLM15BD121SN1D 120ohm, 300mA
+1.8V_RUN
C549 100nF C548 1uF C547 10uF

NC_DPF_PVDD AL38
NC_DPF_PVSS AM35

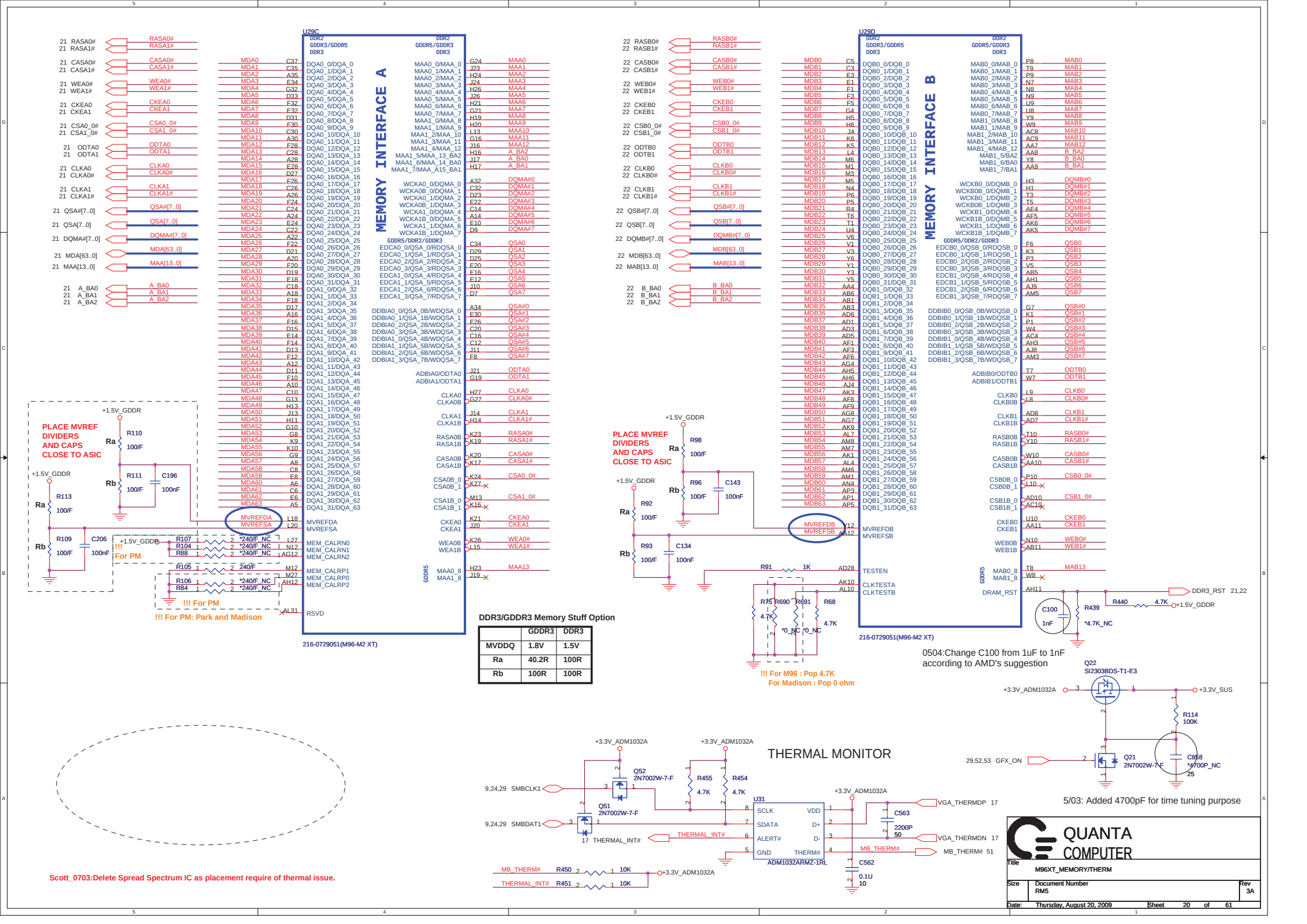
DPF_VSSR#1 AF39
DPF_VSSR#2 AH39
DPF_VSSR#3 AK39
DPF_VSSR#4 AL34
DPF_VSSR#5 AM34

150/F R438 AM39
DPEF_CALR

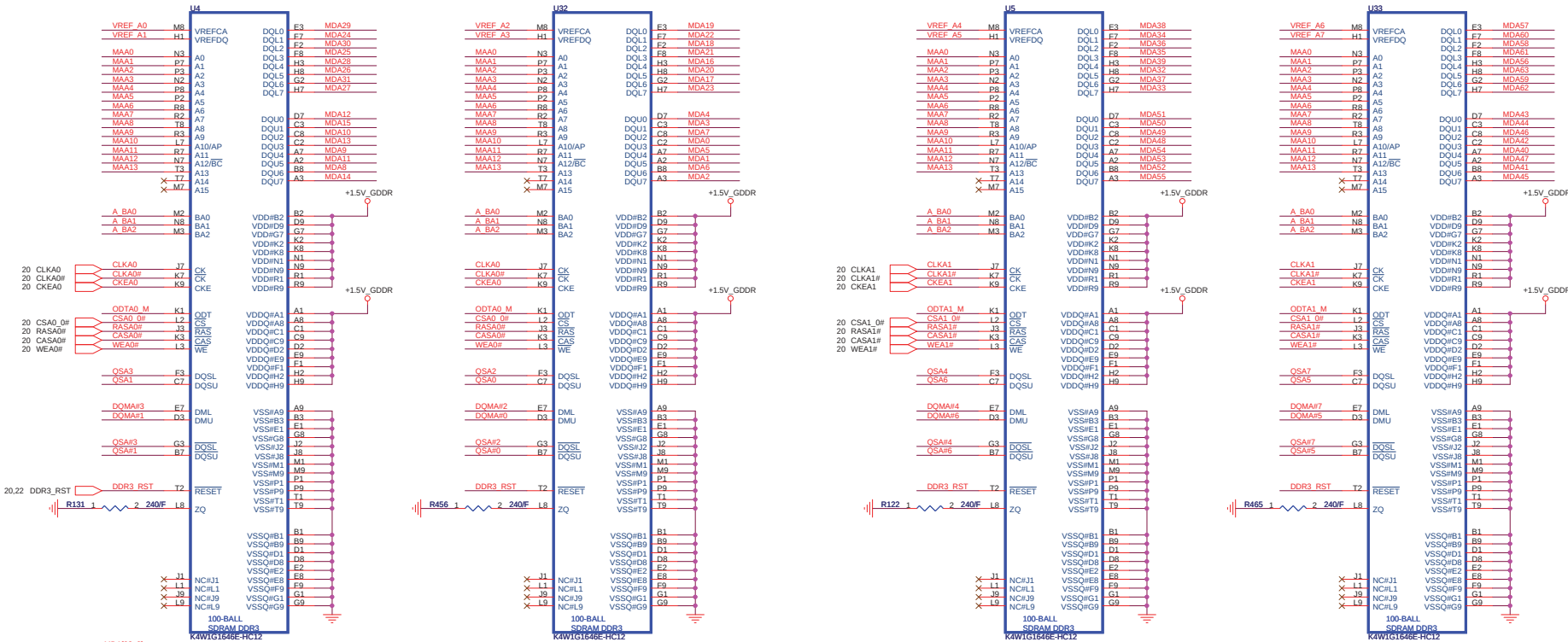
216-0729051(M96-M2 XT)

QUANTA COMPUTER

Title	M96XT_DP POWER	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 19 of 61	

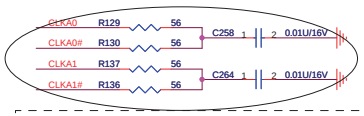

U29C
MEMORY INTERFACE A
DDR2
GDDR3/GDDR5
DDR3
DDR2
GDDR5/GDDR3
DDR3
GDDR5/DDR2/GDDR3
216-0729051(M96-M2 XT)
U29D
MEMORY INTERFACE B
216-0729051(M96-M2 XT)
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+1.5V_GDDR
!!! For PM
!!! For PM: Park and Madison
!!! For M96 : Pop 4.7K
For Madison : Pop 0 ohm
DDR3/GDDR3 Memory Stuff Option
GDDR3
DDR3
MVDDQ 1.8V 1.5V
Ra 40.2R 100R
Rb 100R 100R
0504:Change C100 from 1uF to 1nF
according to AMD's suggestion
5/03: Added 4700pF for time tuning purpose
THERMAL MONITOR
ADM1032ARMZ-1RL
Scott_0703:Delete Spread Spectrum IC as placement require of thermal issue.
QUANTA COMPUTER
Title M96XT_MEMORY/THERM
Size Document Number RM5 Rev 3A
Date: Thursday, August 20, 2009 Sheet 20 of 61

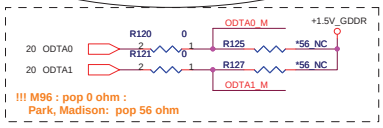
DDR3 64MX16, CH A : 512MB



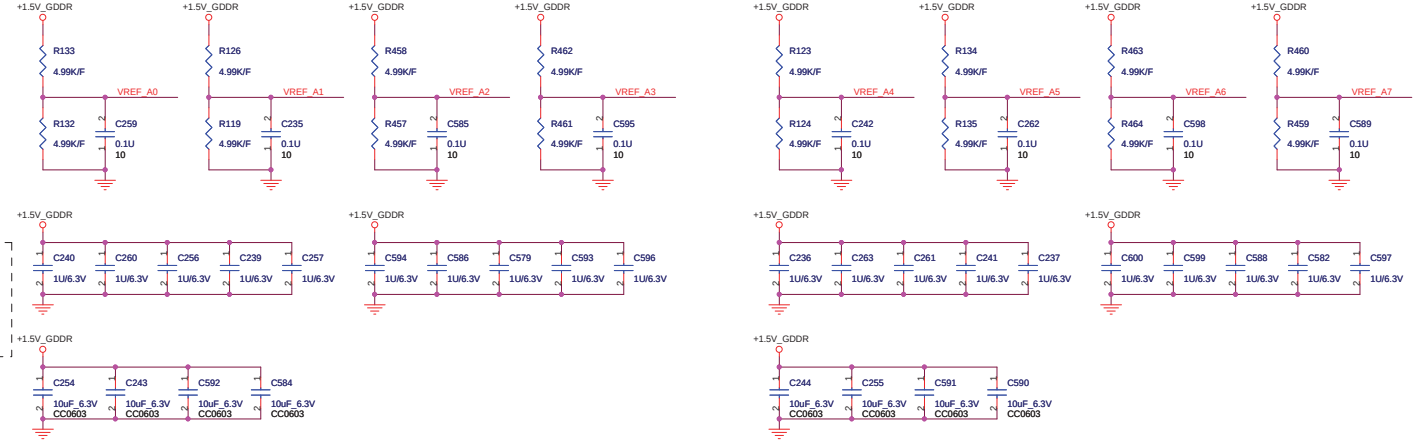
20 MDA[63..0]
20 MAA[13..0]
20 QSA#[7..0]
20 QSA[7..0]
20 DQMA#[7..0]
20 A_BA[2..0]

Placement has to be close to VRAM





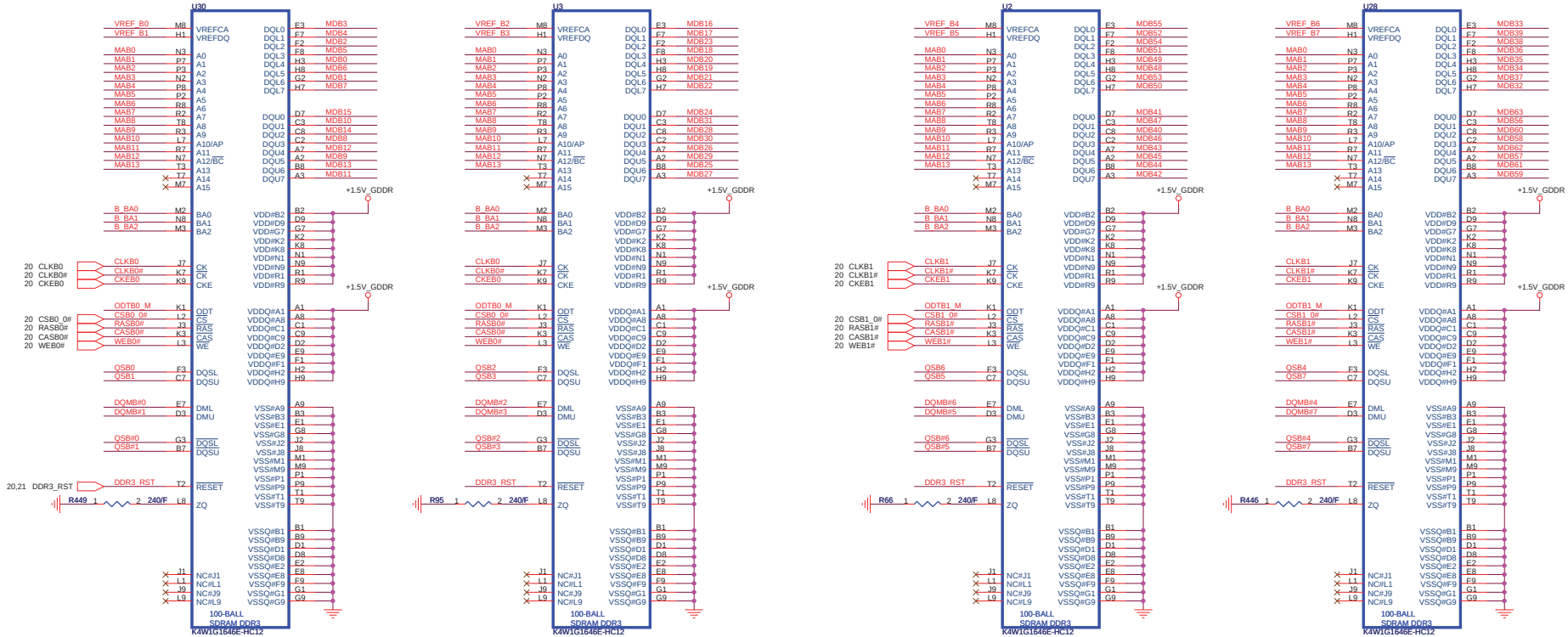
!!! M96 : pop 0 ohm :
Park, Madison: pop 56 ohm

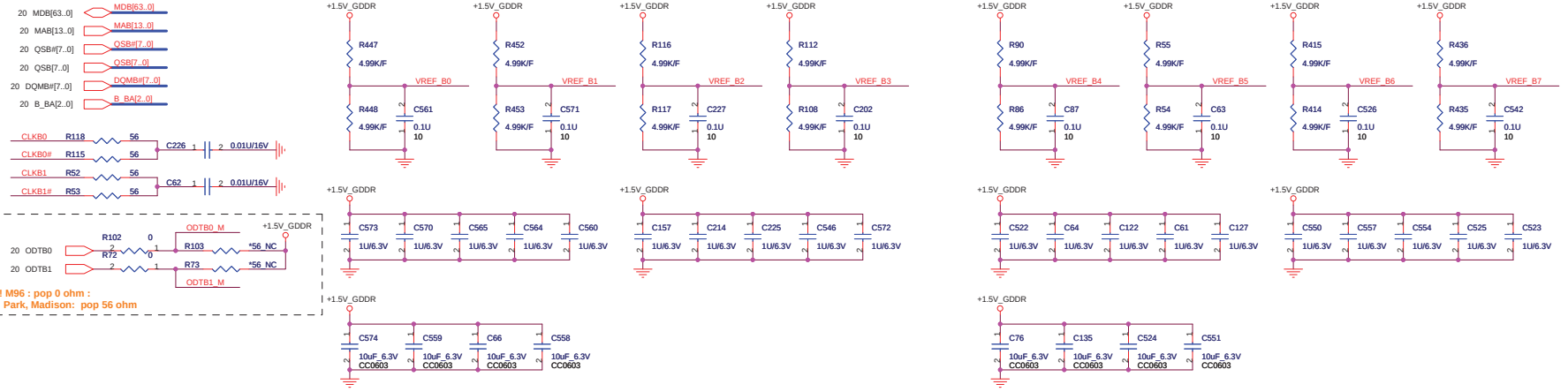


QUANTA COMPUTER

Title	M96XT_DDR3_A_512M	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 21 of 61	

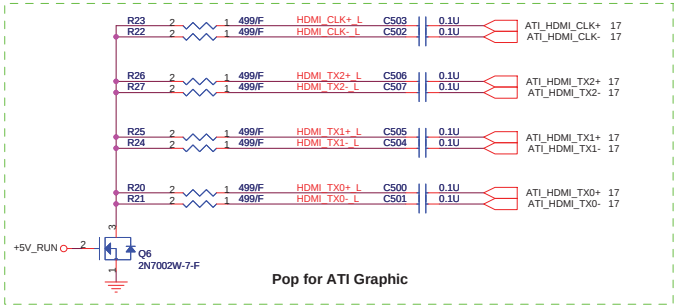
DDR3 64MX16, CH B : 512MB



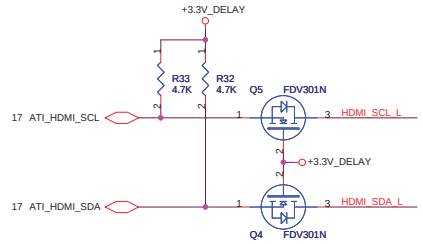


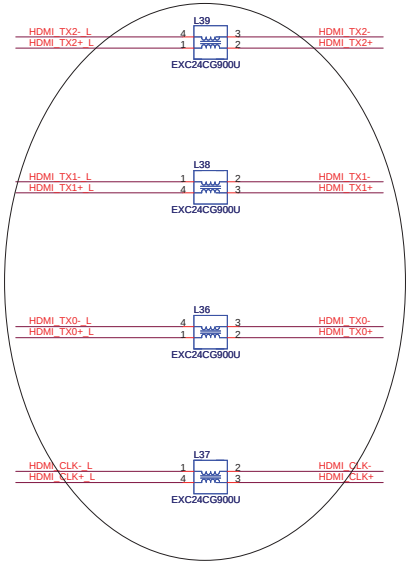
QUANTA COMPUTER

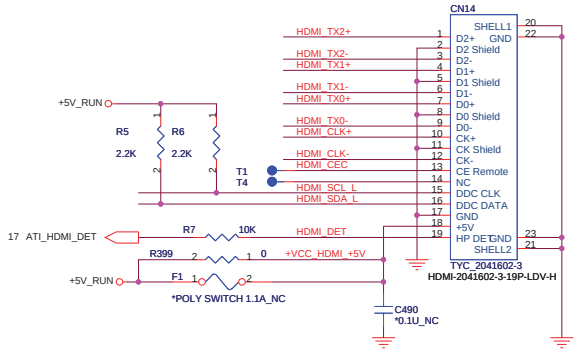
Title	M96XT_DDR3_B_512M	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 22 of 61	



Pop for ATI Graphic



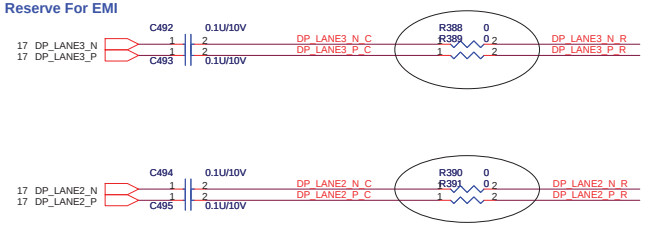




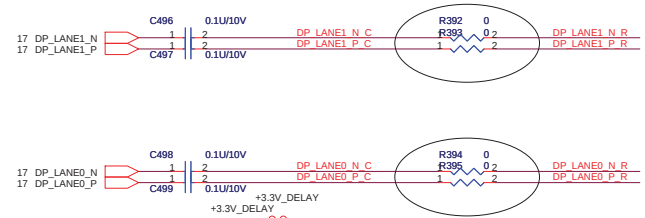
Scott_0814:Delete 0ohm reserve resistors as confirm with EMI.

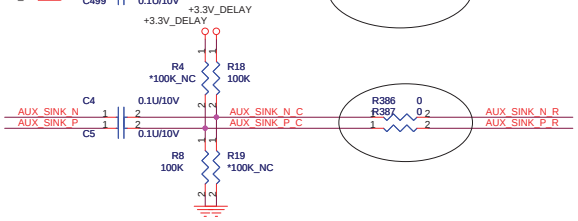
Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.

Reserve For EMI

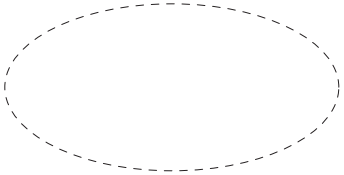


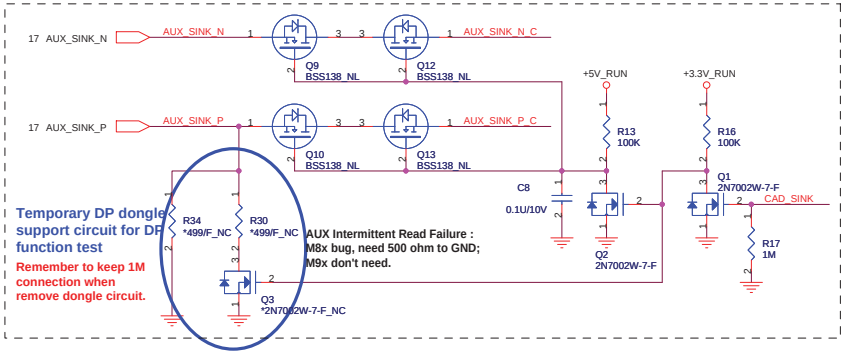
Scott_0814:Delete reserve choke as confirm with EMI.





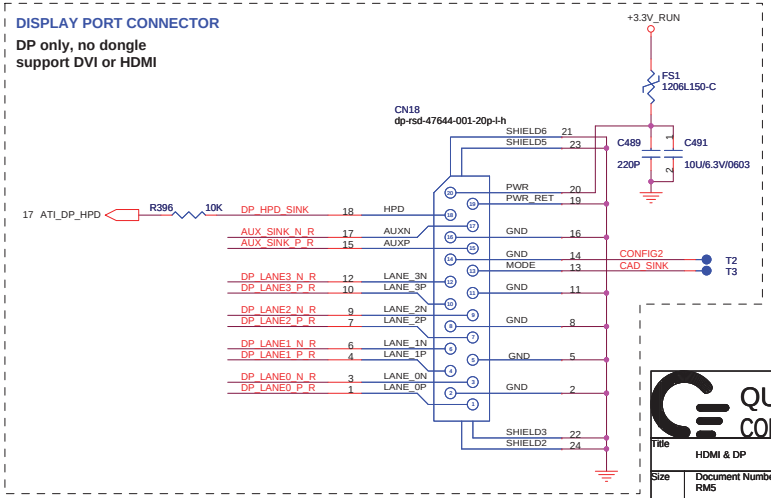
Scott_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.





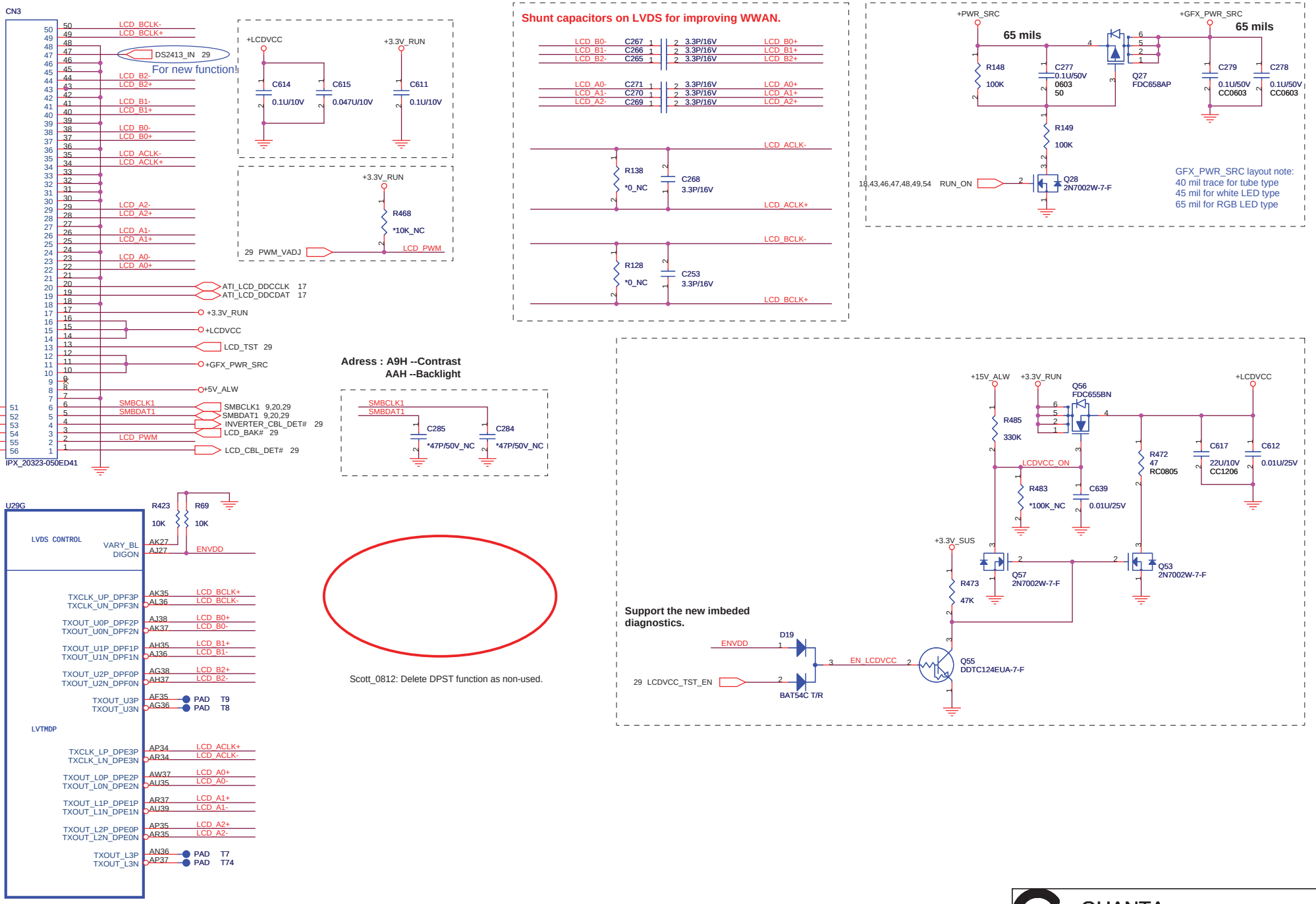
DISPLAY PORT CONNECTOR

DP only, no dongle support DVI or HDMI



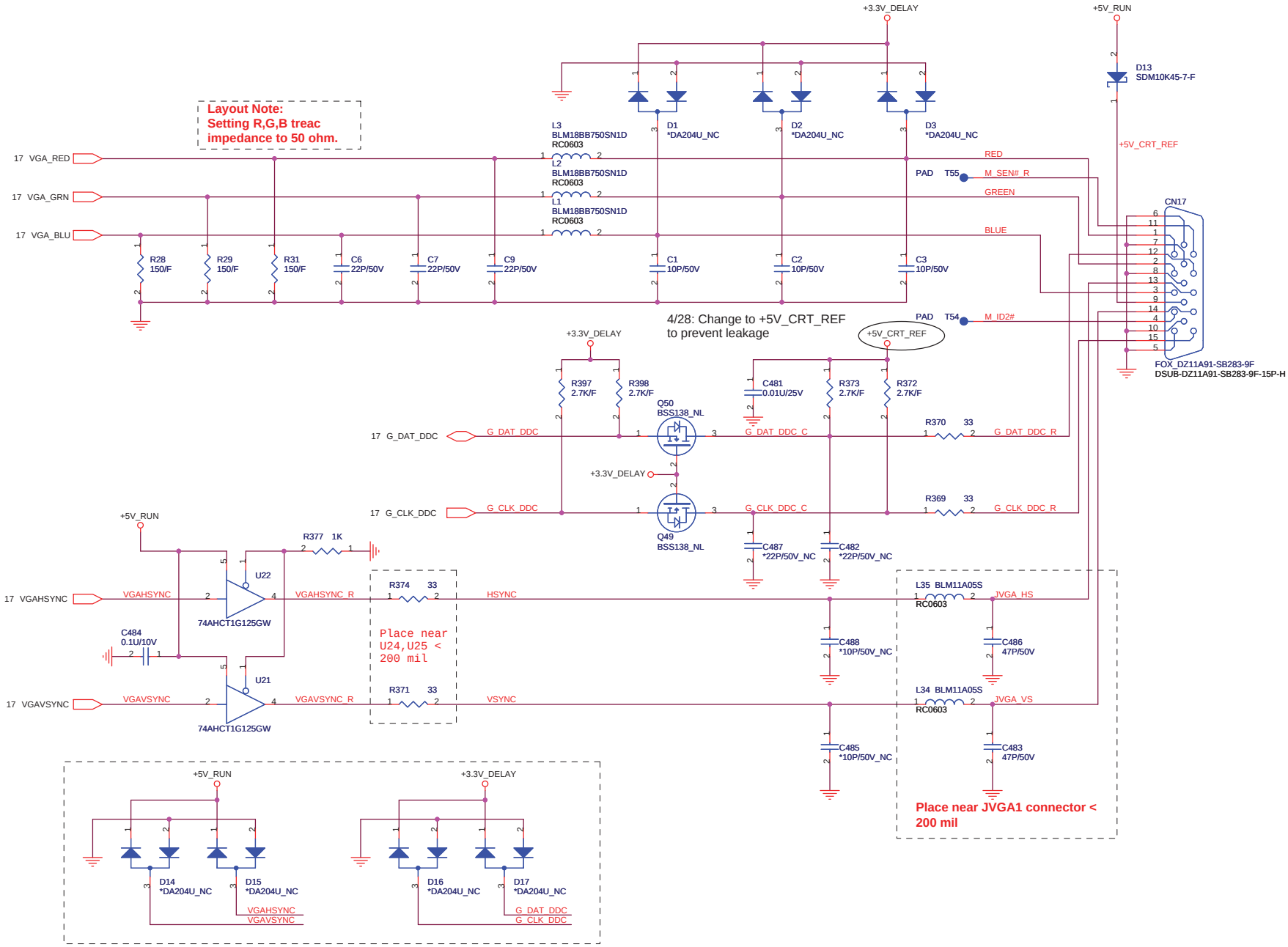
Title	HDMI & DP		
Size	Document Number RM5		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 23 of 61	

QUANTA COMPUTER



QUANTA COMPUTER

Title	M96XT_LVDS & LCD CONN	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 24 of 61	



QUANTA COMPUTER

Title	CRT CONN	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 25 of 61	

Place close U23

Close to RU230
Shield GND Required

4/30: Change C812 to 27pF
Change C813 to 22pF

5/13: Reseved 100P
cap for EMI concern!

5/18: Added 10K pull-up to avoid floating signal
when powering up cardreader IC

MFIO Pin Assignment Table

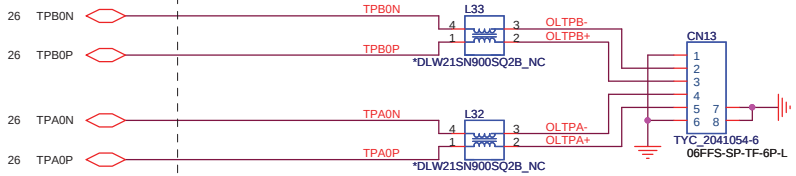
MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

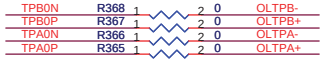
QUANTA COMPUTER

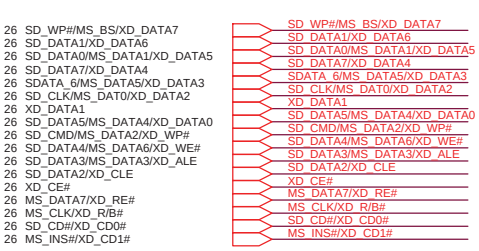
Title	CardReader (5C833)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 26 of 61	

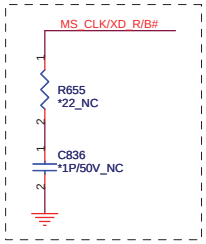
1. TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
2. TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
3. Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

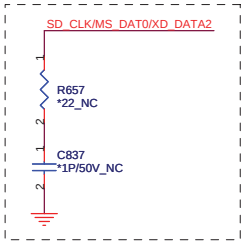
Reserved EMI Solution



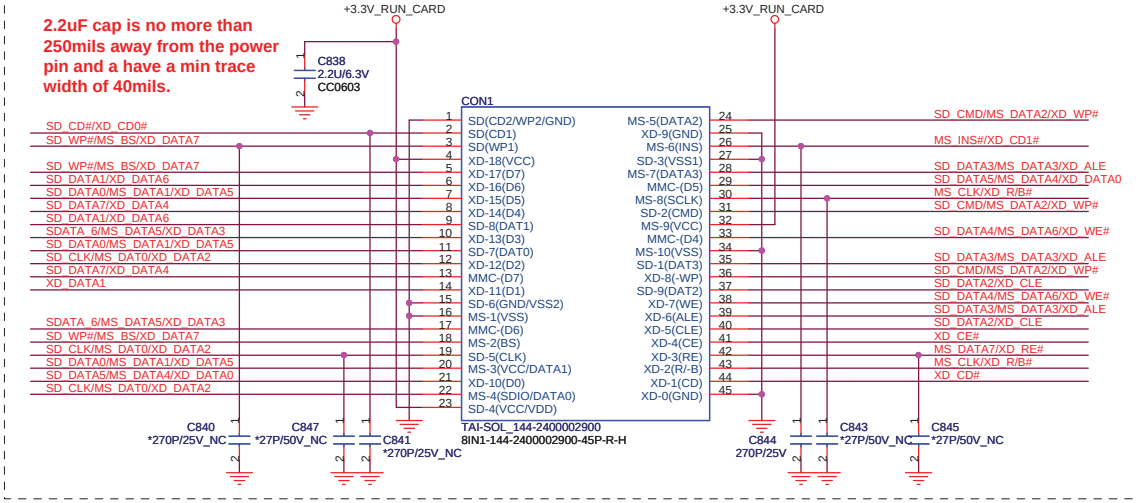




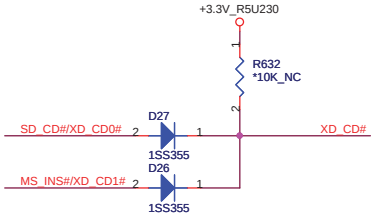




2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

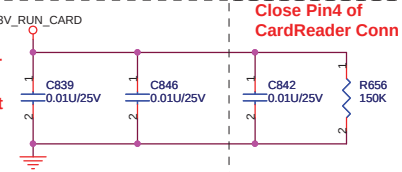


Close to the Chip



The trace width for +3.3V_RUN_CARD should be 40MIL at least.

Close Pin4 of CardReader Conn

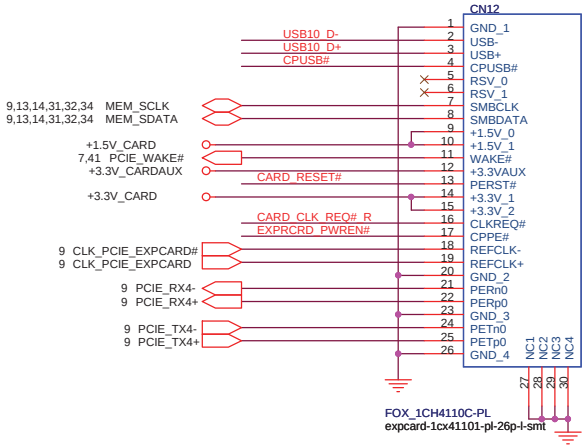


QUANTA COMPUTER

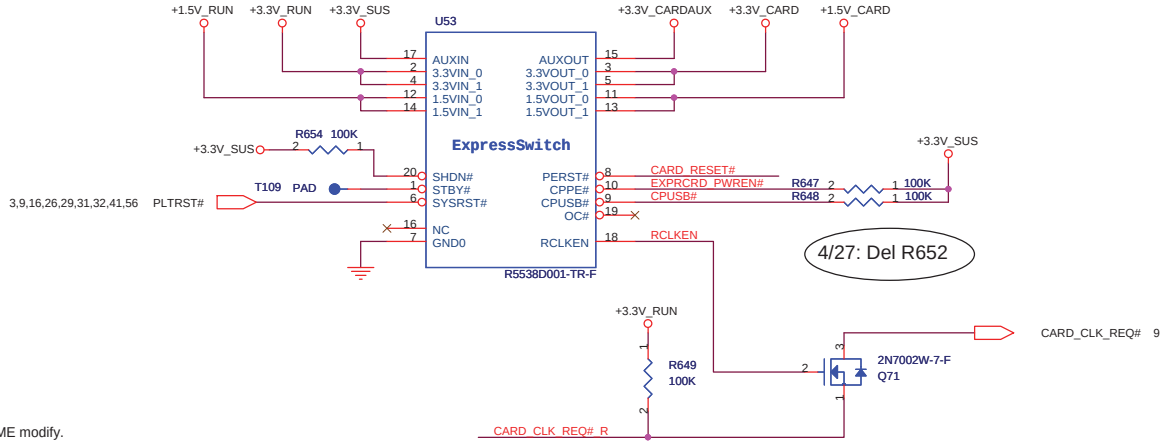
Title	8 IN 1 & 1394 CONN	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 27 of 61	

Express Card

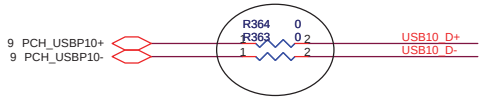
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



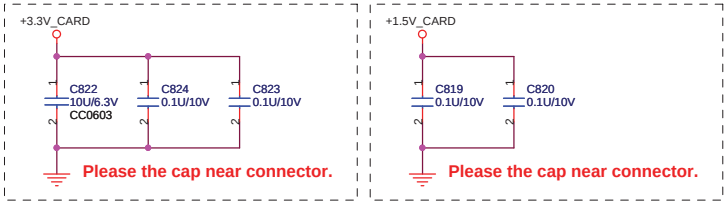
Scott_0813:Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt as ME modify.

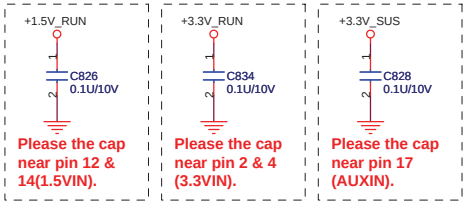


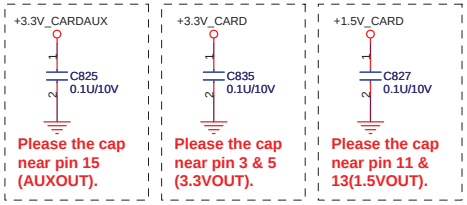
PCI-Express TX and RX direct to connector.



Scott_0814:Delete L31 as confirm with EMI.

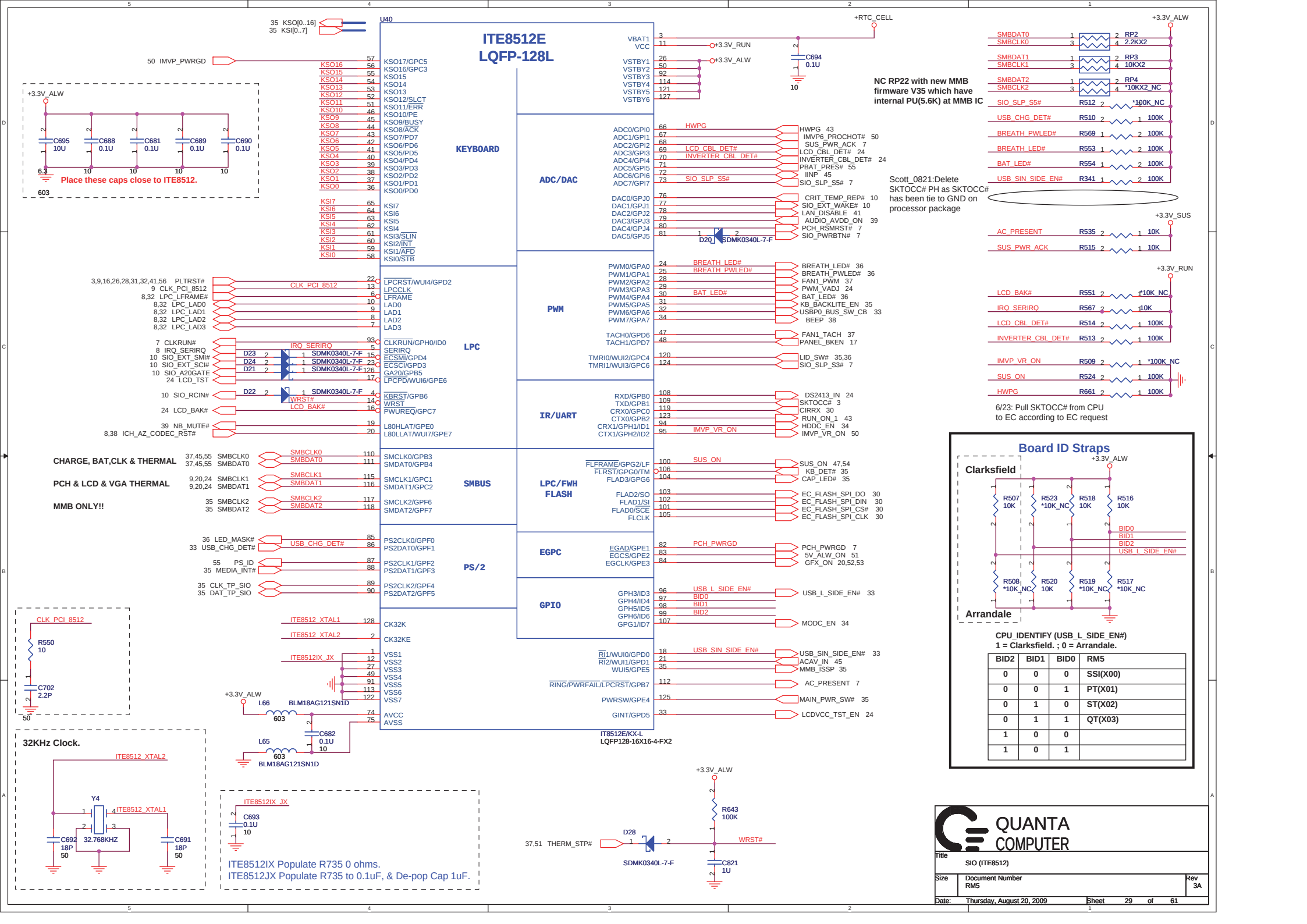






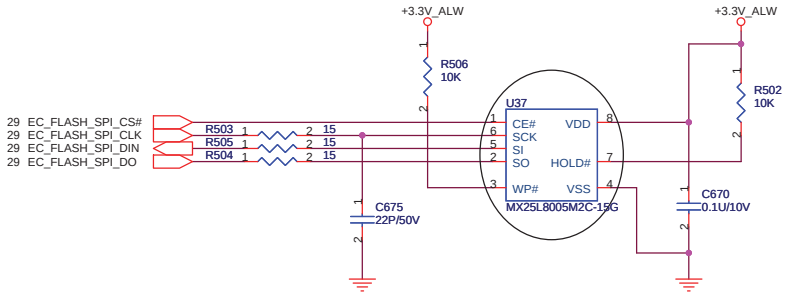
QUANTA COMPUTER

Title	EXPRESS CARD	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 28 of 61	

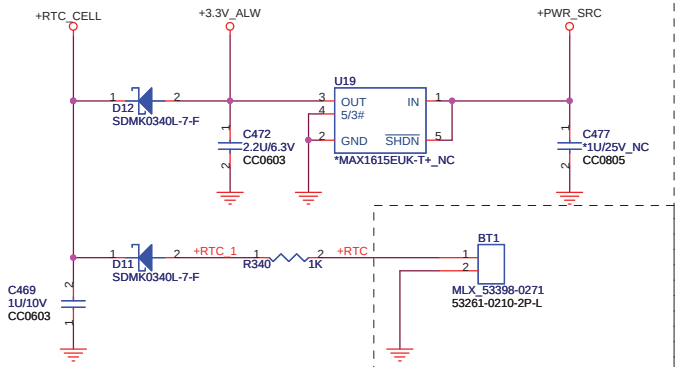

ITE8512E
LQFP-128L
U40
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH
FLASH
EGPC
PS/2
GPIO
IT8512E/KX-L
LQFP128-16X16-4-FX2
Place these caps close to ITE8512.
NC RP22 with new MMB firmware V35 which have internal PU(5.6K) at MMB IC
Scott_0821:Delete SKTOCC# PH as SKTOCC# has been tie to GND on processor package
6/23: Pull SKTOCC# from CPU to EC according to EC request
CHARGE, BAT,CLK & THERMAL
PCH & LCD & VGA THERMAL
MMB ONLY!!
32KHz Clock.
ITE8512IX Populate R735 0 ohms.
ITE8512JX Populate R735 to 0.1uF, & De-pop Cap 1uF.
Board ID Straps
Clarksfield
Arrandale
CPU_IDENTIFY (USB_L_SIDE_EN#)
1 = Clarksfield. ; 0 = Arrandale.
BID2 BID1 BID0 RM5
0 0 0 SSI(X00)
0 0 1 PT(X01)
0 1 0 ST(X02)
0 1 1 QT(X03)
1 0 0
1 0 1
QUANTA COMPUTER
Title SIO (ITE8512)
Size Document Number RM5 Rev 3A
Date: Thursday, August 20, 2009 Sheet 29 of 61

EC SPI ROM, 8Mbit (1M Byte)

5/12: Change U37 from 2MB to 1MB according to BIOS request!

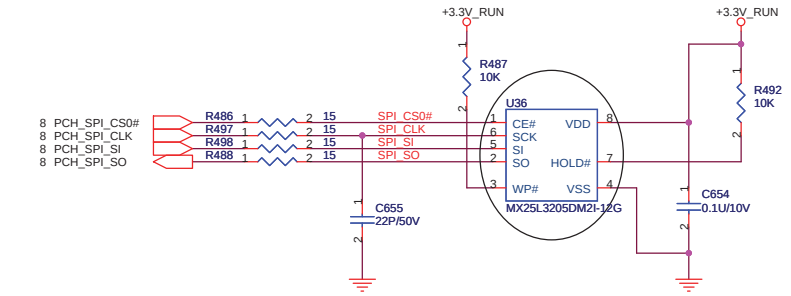


RTC BATTERY

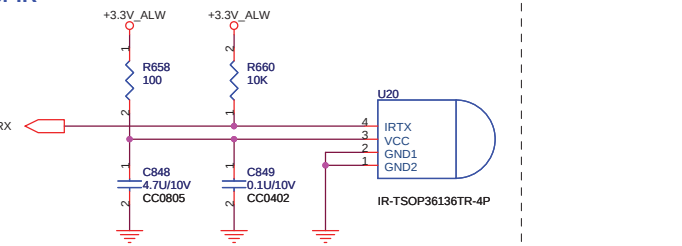


PCH SPI ROM, (4M Byte)

5/12: Change U36 from 2MB to 4MB according to BIOS request!



Consumer IR



QUANTA COMPUTER

Title	FLASH/ RTC/ CIR	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 30 of 61	

MiniCard WLAN Connector

Mini Card Nut

H21
Mini Card Align (h6.6)

5/15: Change WAKE# to NC as it is not required

MINI1CLK_REQ#
C698
220P/50V

CN24

32 COEX2_WLAN_ACTIVE	1	WAKE#	3.3V_1	2	+3.3V_RUN
32 COEX1_BT_ACTIVE_MINI	3	RESERVED_1	GND0	4	
9 MINI1CLK_REQ#	5	RESERVED_2	1.5V_1	6	+1.5V_RUN
MINI1CLK_REQ#	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	
9 CLK_PCIE_MINI1#	11	REFCLK-	UIM_CLK	12	
9 CLK_PCIE_MINI1	13	REFCLK+	UIM_RESET	14	
	15	GND2	UIM_VPP	16	
	17	UIM_C8	GND3	18	
	19	UIM_C4	W_DISABLE#	20	WLAN_RADIO_OFF#
	21	GND4	PERST#	22	
9 PCIE_RX2-	23	PERn0	3.3VAUX1	24	+3.3V_RUN
9 PCIE_RX2+	25	PERp0	GND5	26	
	27	GND6	1.5V_2	28	
	29	GND7	SMB_CLK	30	MEM_SCLK 9,13,14,28,32,34
9 PCIE_TX2-	31	PETn0	SMB_DATA	32	MEM_SDATA 9,13,14,28,32,34
9 PCIE_TX2+	33	PETp0	GND8	34	
	35	GND9	USB_D-	36	USB4_D-
10 PCIE_MCARD1_DET#	37	RESERVED_3	USB_D+	38	USB4_D+
	39	RESERVED_4	GND10	40	USB_MCARD1_DET# 9
	41	RESERVED_5	LED_WWAN#	42	PAD T106
	43	RESERVED_6	LED_WLAN#	44	LED_WLAN_OUT# 36
	45	RESERVED_7	LED_WPAN#	46	PAD T105
	47	RESERVED_8	1.5V_3	48	
	49	RESERVED_9	GND11	50	
	51	RESERVED_10	3.3V_2	52	

1759513-1
MIPCIEXP-1775838-1-52P

PCI-Express TX and RX direct to connector

C853 100P 50 NPO

PLTRST# 3,9,16,26,28,29,32,41,56

5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

Reserved PAD for EMI

L70
USB4_D-
USB4_D+
PCH_USBP4- 9
PCH_USBP4+ 9
*DLW21SN900SQ2B_NC
R708 0
R709 0

Suport for WoW

D25
SDMK0340L-7-F
WLAN_RADIO_OFF#
WLAN_RADIO_DIS# 10
R612 *0_NC

Prevent backdrive when WoW is enabled.

Place caps close to connector.

+1.5V_RUN
C434 0.047U/10V
C779 0.047U/10V

+3.3V_RUN
C460 0.1U/10V
C767 0.047U/10V
C456 0.1U/10V
C457 0.047U/10V
C449 4.7U/10V CC0805

QUANTA COMPUTER

Title	MINI-CARD (WLAN)		
Size	Document Number RM5		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 31 of 61	

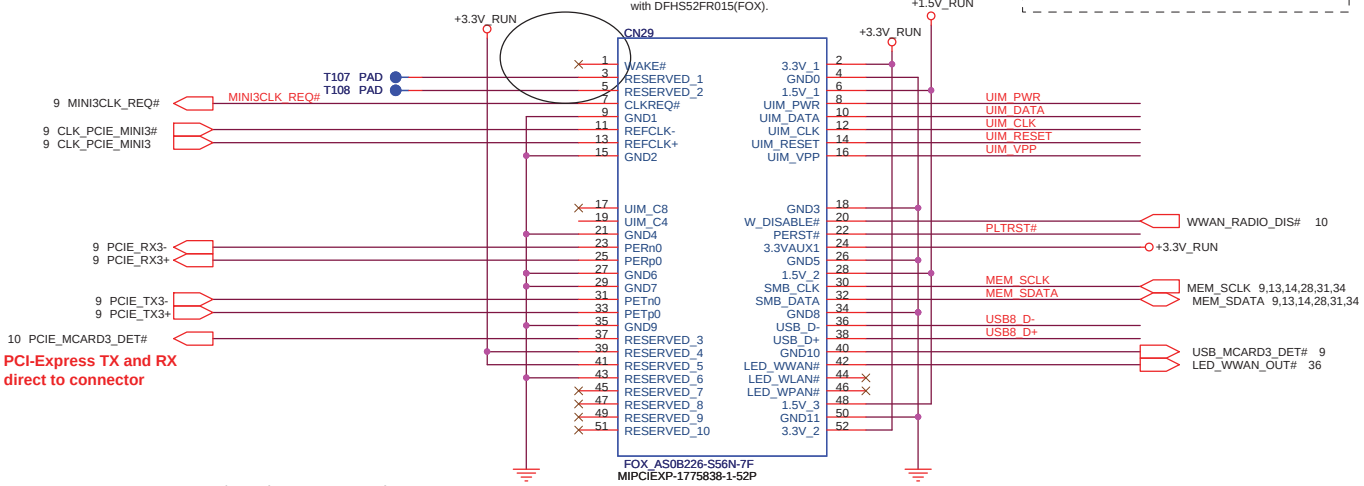
5/13: Pull up WAKE# to 3.3V_RUN so as to avoid leakage

5/15: Change WAKE# to NC as it is not required

5/08: Swap WWAN and WPAN according to antenna team's suggestion

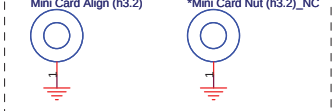
MiniCard WWAN Connector

Scott_0123:Change CN31 PN with DFHS52FR015(FOX).

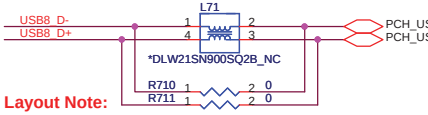


PCI-Express TX and RX direct to connector

Mini Card Nut

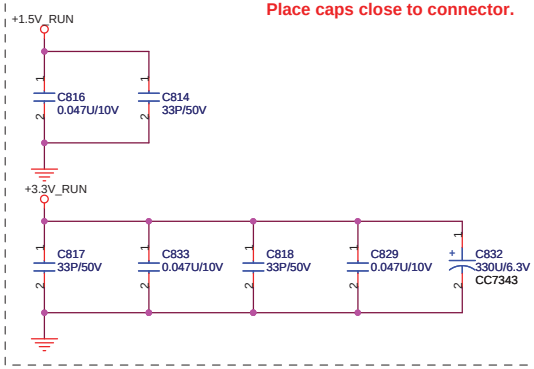


Reserve For EMI

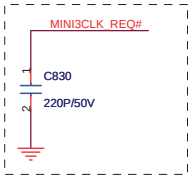


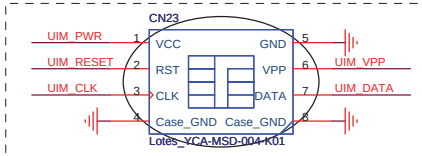
Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.



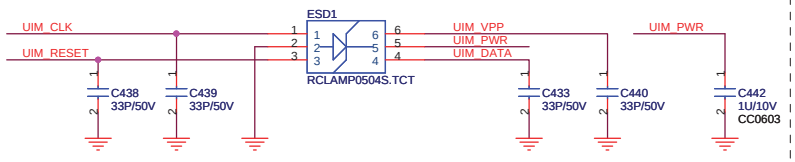
5/13: Change SIM card connector to Lotes



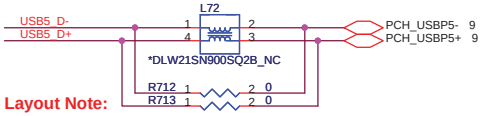


Place as close as possible to JMINI connector

layout note:10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil

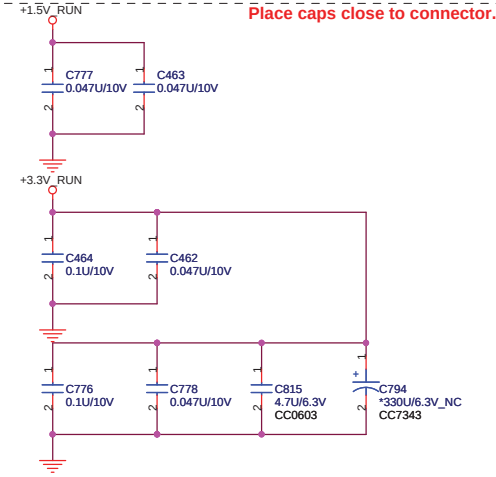


Reserve For EMI



Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

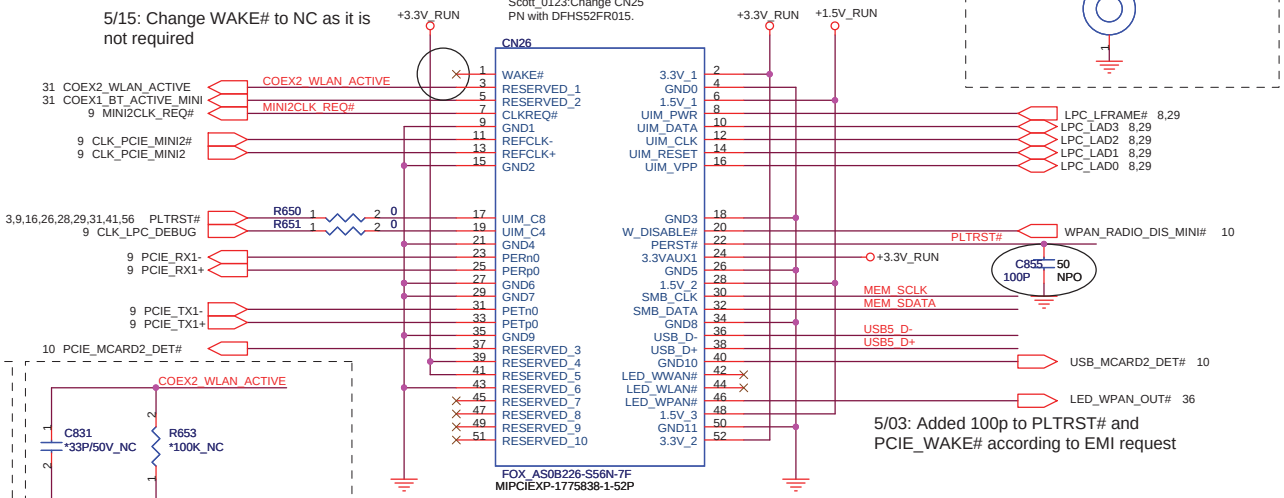
Place caps close to connector.



MiniCard Robson, BT. UWB Connector

5/15: Change WAKE# to NC as it is not required

Scott_0123:Change CN25 PN with DFHS52FR015.



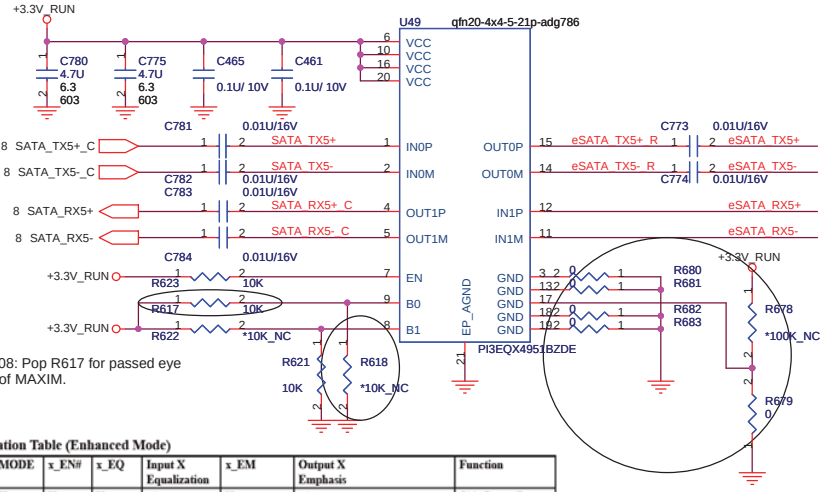
Mini Card Nut

5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

Title	MINI-CARD (WPAN,WWAN)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 32 of 61	

QUANTA COMPUTER

eSATA Re-driver IC



Scott_0708: Pop R617 for passed eye diagram of MAXIM.

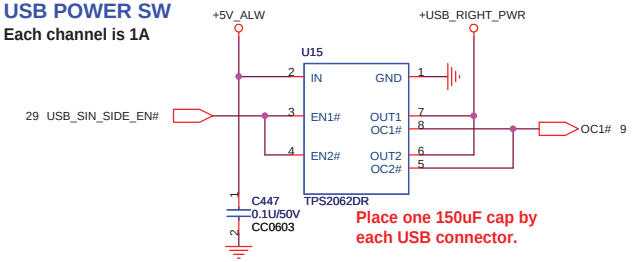
Configuration Table (Enhanced Mode)

EN	MODE	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, high input equalization

5/11: Reserved 0 ohms for Pericom enhanced mode select
5/12: Change IC to Pericom as Maxim failed EA test
6/23: NC according to Pericom reccomandation!

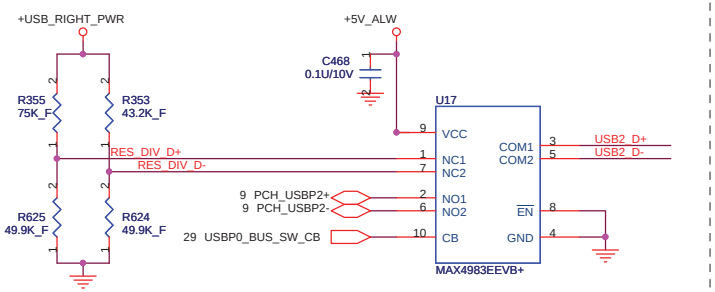
USB POWER SW

Each channel is 1A

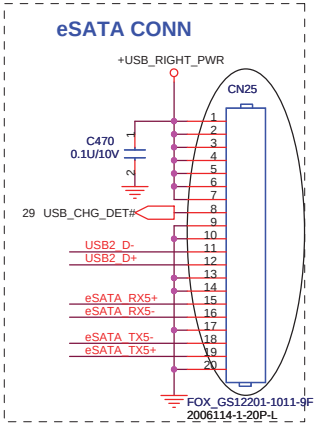


Place one 150uF cap by each USB connector.

USB Power Share



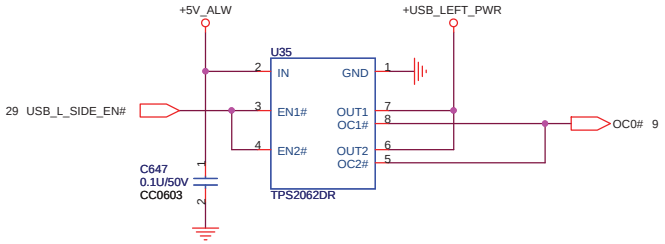
eSATA CONN



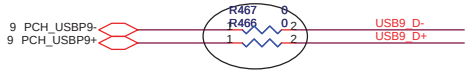
5/13: Change Connector to Foxconn to avoid material shortage for Tyco

USB POWER SW

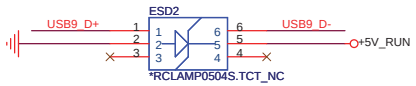
Each channel is 1A

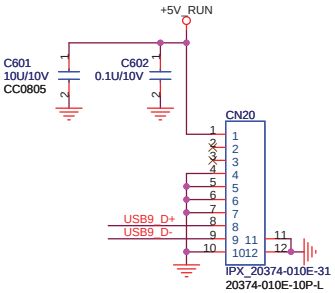


TV module

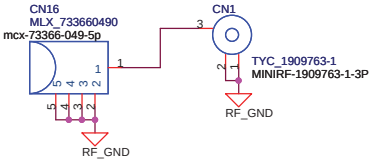


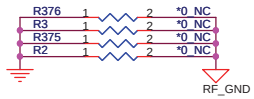
Scott_0814:Delete L58 as confirm with EMI.

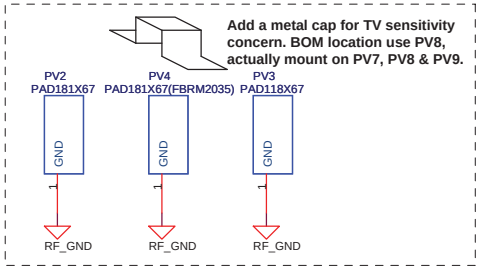




TV RF Jack & Microwave connector



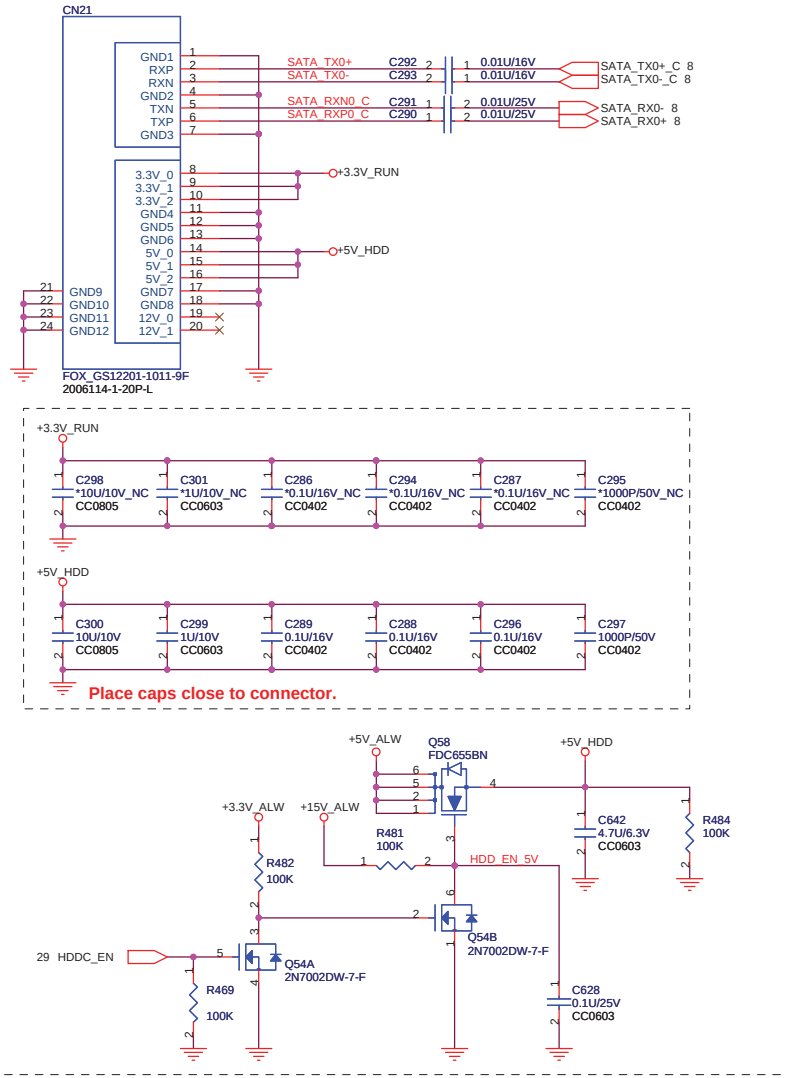




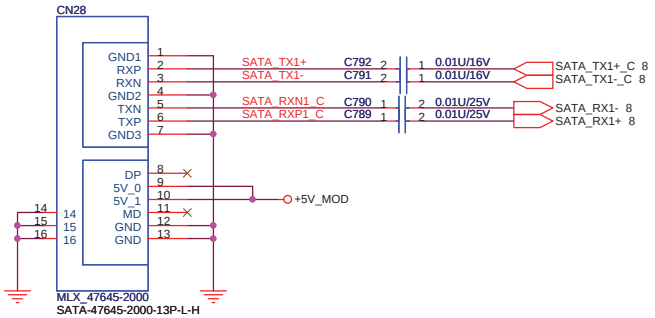
QUANTA COMPUTER

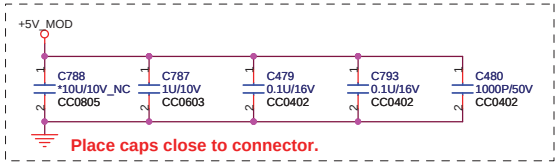
Title	USB & eSATA & TV	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 33 of 61	

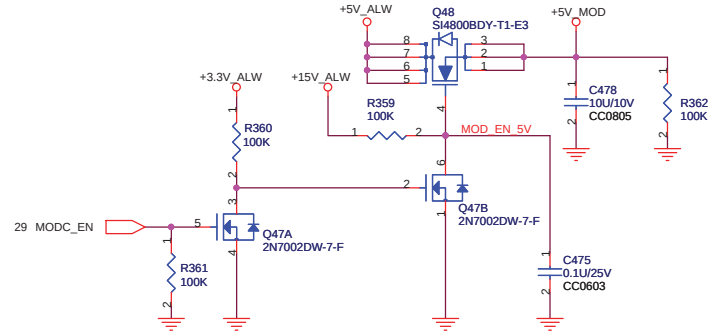
SATA Connector



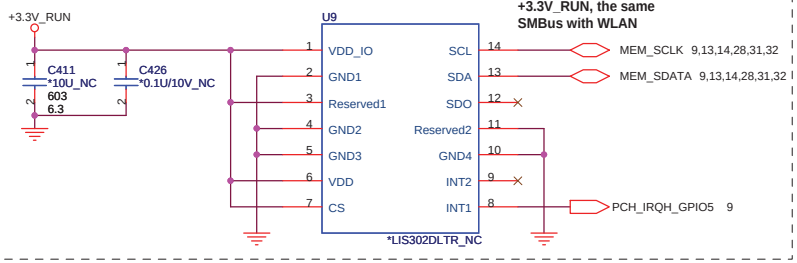
ODD Connector







3-axis Fall Sensor (HDD data protector)



QUANTA COMPUTER

Title	HDD & ODD (SATA)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 34 of 61	

To Daughter Board connector

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3);

Scott_0123:Change CN8 PN with DFHD32MR003(With mylar)

CN9

Power Button
- 36 BREATH_PWRLED_INT
- POWER_SW_IN0#

Speaker
- 39 AUD_SPK_L1
- 39 AUD_SPK_L2
- 39 AUD_SPK_R1
- 39 AUD_SPK_R2

KB LED
- 8 KB_LED_DET
- 29 KB_BACKLITE_EN
- +5V_RUN
- R588 200K/F
- R594 100K

Touch Pad
- 29 DAT_TP_SIO
- 29 CLK_TP_SIO
- +3.3V_ALW

Media Button
- +5V_ALW
- +MMB_PWR
- 29 MEDIA_INT#
- SMBDAT2_MMB
- SMBCLK2_MMB
- MEDIA_INT#

FOX_QB5RF321-1203-8F
gb5rf341-12037f-32p-l

Power Button

+3.3V_ALW, +3.3V_ALW
D29 *DA204U_NC
R666 100K
R668 10K
POWER_SW_IN0#
MAIN_PWR_SW# 29
C850 1U/10V CC0603

Hall Switch

+3.3V_ALW
"MEDIA_INT#" PU at MB side
R599 100K
MEDIA_INT#
C626 0.1U/10V
+3.3V_ALW
U7
VDD
VSS
OUT
EM-6781-T3
LID_SW#
LID_SW# 29,36

Active high for ISSP reset

Q44 SI2303BDS-T1-E3
+5V_ALW2
+MMB_PWR
C405 0.1U/10V
R287 10K
R279 100
+3.3V_ALW
R284 100K
29 MMB_ISSP
Q39 2N7002W-7-F
Q40 2N7002W-7-F

+MMB_PWR
Q42 2N7002W-7-F
R286 *20K_NC
R299 *20K_NC
29 SMBDAT2
SMBDAT2_MMB
+MMB_PWR
Q43 2N7002W-7-F
29 SMBCLK2
SMBCLK2_MMB

NC R620 & R621 with new MMB firmware V35 which have internal PU(5.6K) at MMB IC

KEYBOARD CONNECTOR

29 KSI[0..7]
29 KSO[0..16]
R493 100K
+3.3V_ALW
29 KB_DET#
CN7
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0 KSO5 KSO7 KSO6 KSO4 KSO1 KSO3 KSO8 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10 CAP_LED_L
GND1
GND2
HRS_FH28-60(30)SB-1SH(86)
FH28-30SB-1SH-30P-R

+3.3V_ALW, +3.3V_ALW, +5V_RUN
R265 100K
29 CAP_LED#
Q41 2N7002W-7-F
Q38 DDTA114YUA-7-F
47k
10K
R253 150
CAP_LED_L

CP2 100PX4
CP1 100PX4
CP4 100PX4
CP3 100PX4
CP6 100PX4
CP5 100PX4
50 NPO 1206
C656 100P/50V
KSI7

100P CAPS close to KB connector

5/03: Populate according to EMI request!
5/12: Change from CA110084N04 to CA110084N39 due to material shortage!

Array Microphone & Camera

Scott_0814:Delete L29 as confirm with EMI.

+3.3V_RUN, +3.3V_RUN, +3.6V_RUN
R628 100K
L30 BLM11A05S RC0603
L28 *BLM11A05S_NC RC0603

The GND (pin 8) for DMIC is defined as AGND. Connect with GND at MB, but separate AGND & GND at coaxial cable & CCD module.

9 PCH_USBP11+
9 PCH_USBP11-
R358
R357
USB11_D+
USB11_D-
CAM_VCC
CN10
IPX_20374-010E-31
20374-010E-10P-L

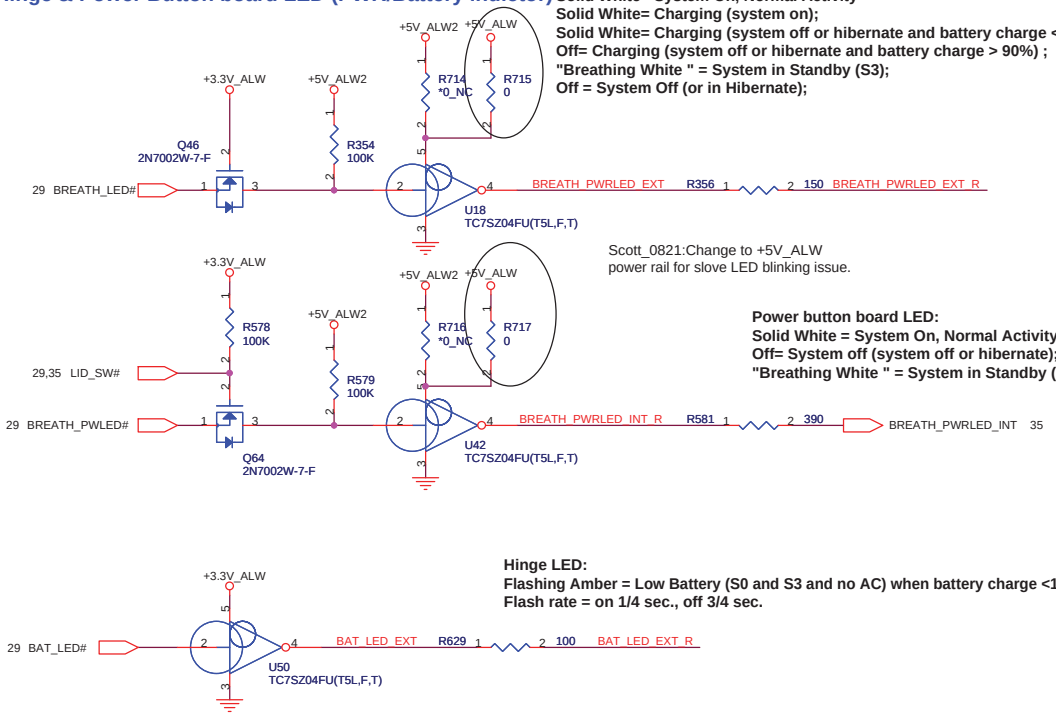
38 DMIC_DATA
38 DMIC_CLK
10 CAMERA_CBL_DET#
R627 0/0603 RC0603
R626 22/0603 RC0603
DMIC_DATA_R
DMIC_CLK_R

C785 *33P/50V_NC
C786 *33P/50V_NC
C471 10U/10V CC0805

+5V_RUN
U16
IN
EN
GND
OUT
NC/FB
*TPS76301DBVR_NC
+3.6V_RUN
C459 *1U/10V_NC CC0603
R351 *100K/F_NC
C467 *27P/50V_NC
R352 *49.9K/F_NC
C466 *4.7U/6.3V_NC CC0603

QUANTA COMPUTER			
Title	KB/ CCD/ UI		
Size	Document Number RM5		Rev 3A
Date: Thursday, August 20, 2009		Sheet 35 of 61	

Hinge & Power Button board LED (PWR/Battery indictor)



Hinge LED
Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%) ;
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

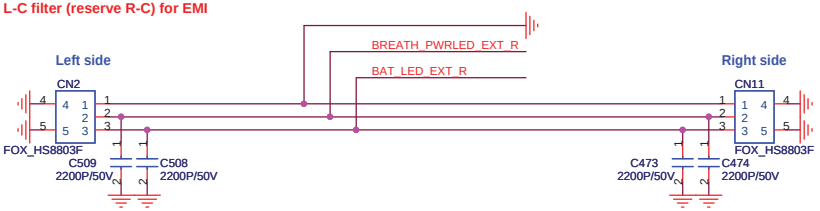
Scott_0821:Change to +5V_ALW
power rail for slove LED blinking issue.

Power button board LED:
Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3)

Hinge LED:
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

Hinge LED (PWR/Battery indictor)

L-C filter (reserve R-C) for EMI

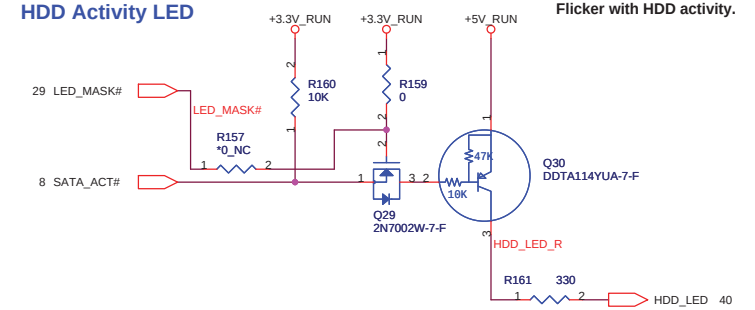


Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

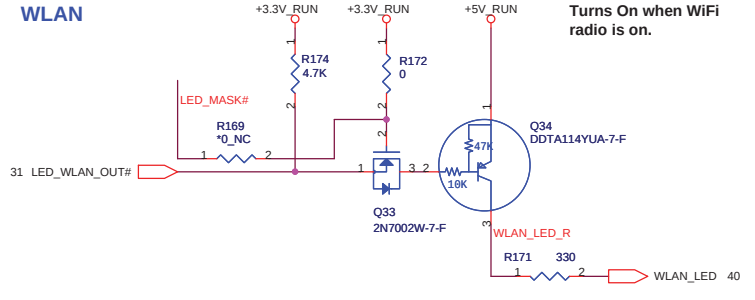
HDD Activity LED

Flicker with HDD activity.



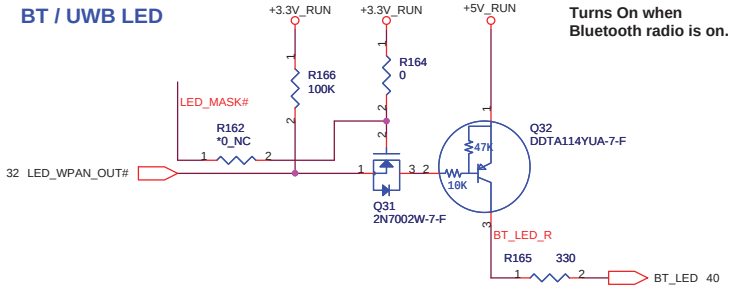
WLAN

Turns On when WiFi radio is on.



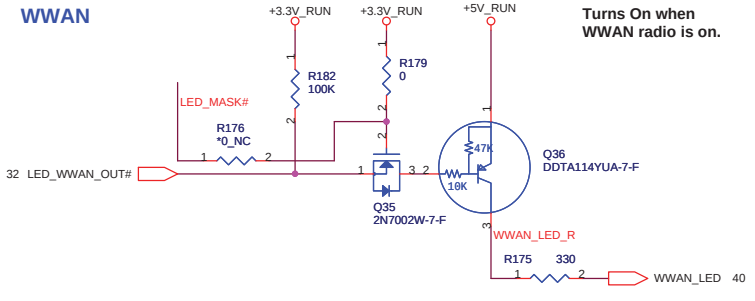
BT / UWB LED

Turns On when Bluetooth radio is on.



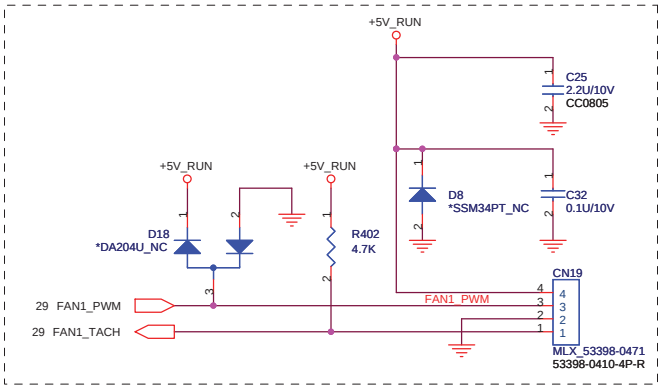
WWAN

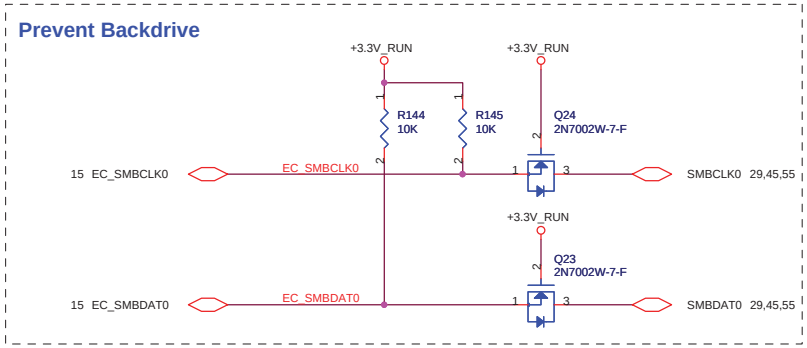
Turns On when WWAN radio is on.

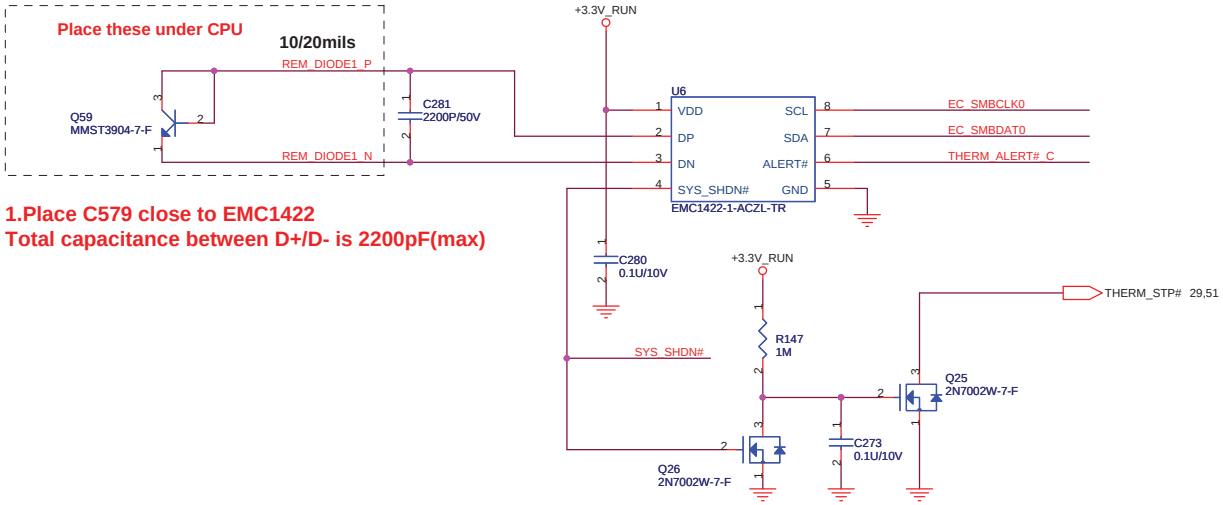


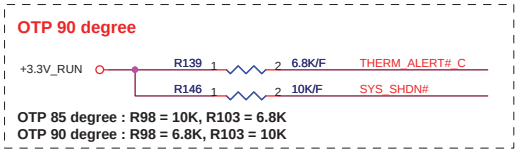
QUANTA COMPUTER

Title	LED	
Size	Document Number RM5	Rev 3A
Date: Friday, August 21, 2009	Sheet 36 of 61	



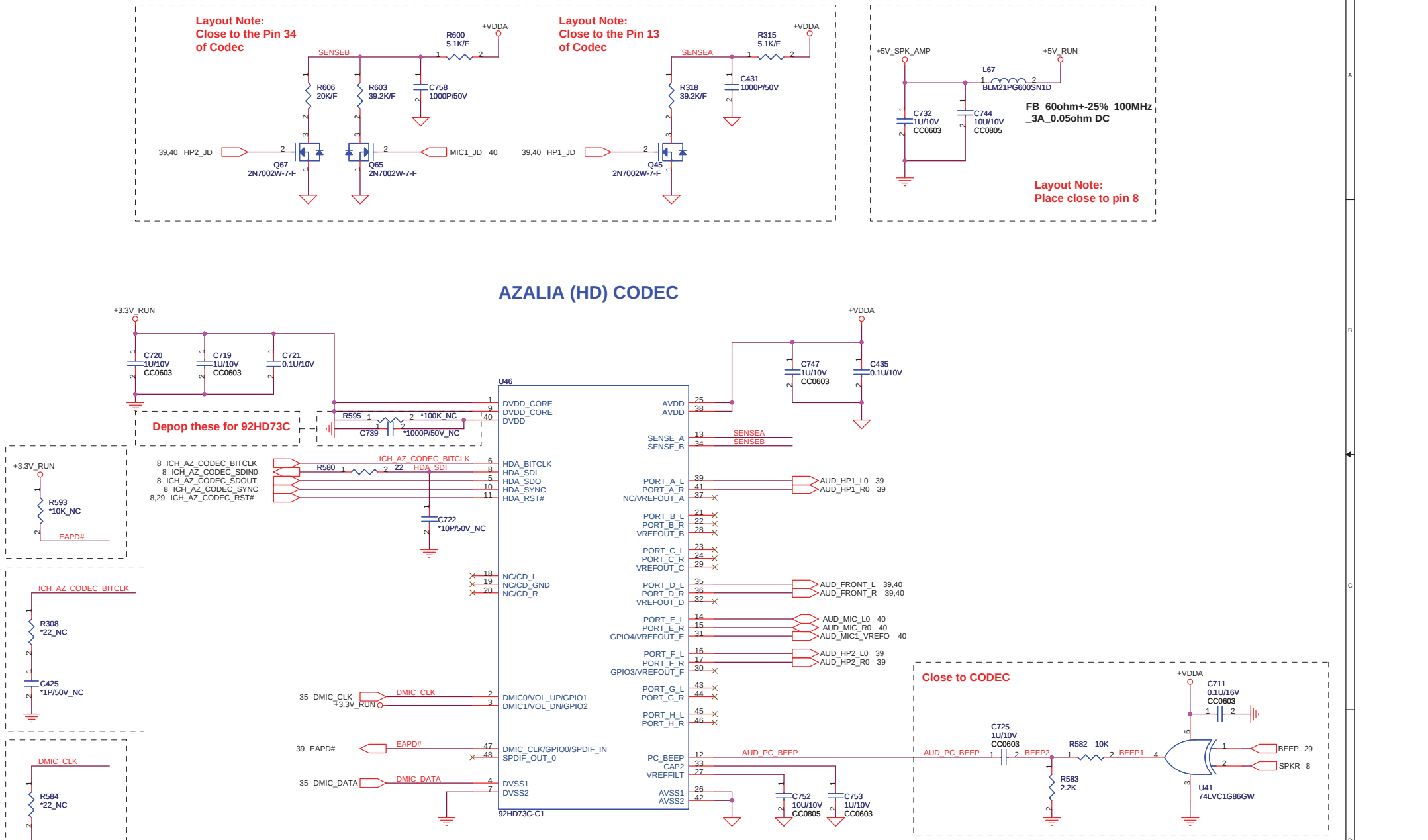




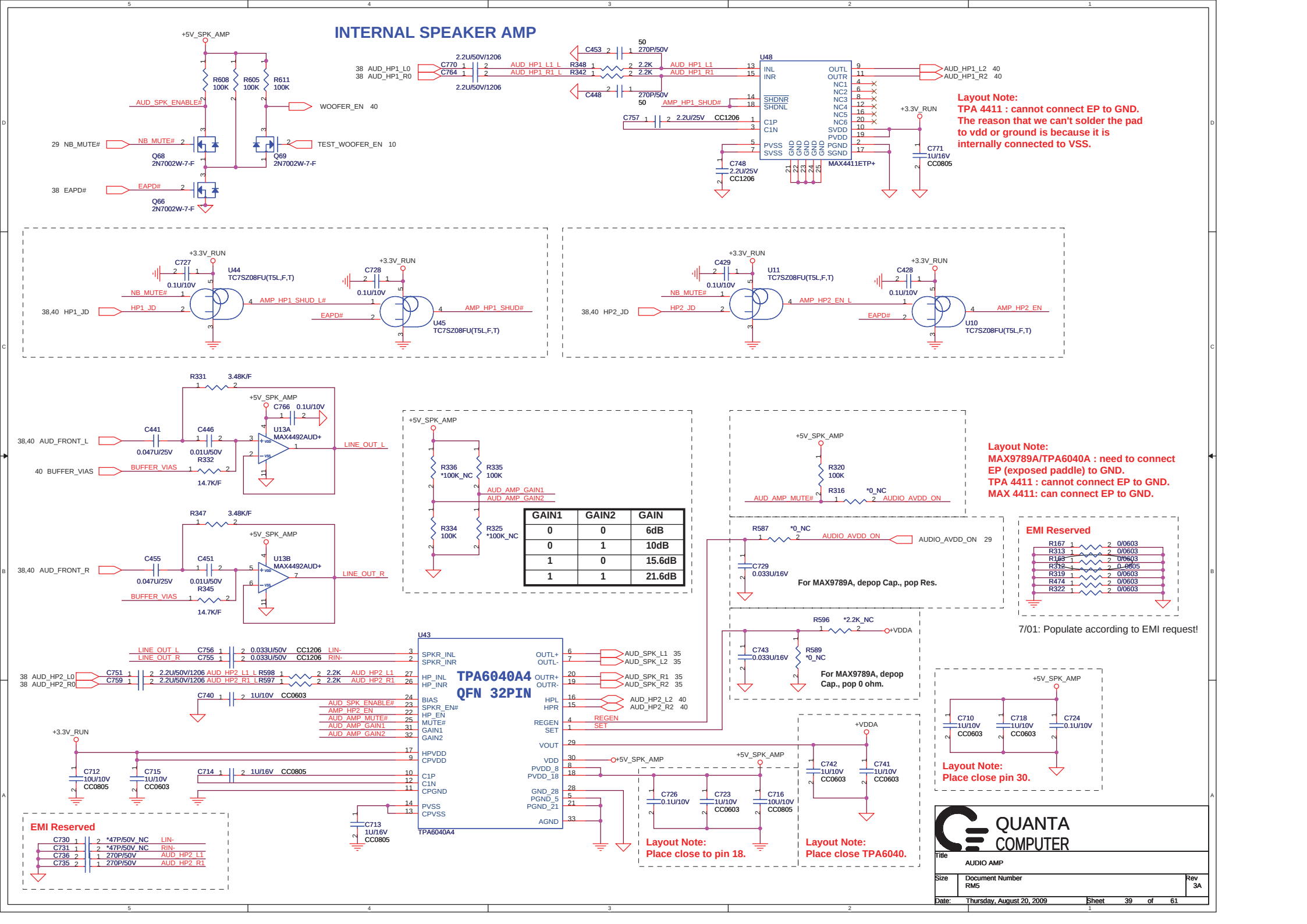


QUANTA COMPUTER

Title	FAN /THERMAL	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 37 of 61	


Layout Note:
Close to the Pin 34
of Codec
SENSEB
+VDDA
R600
5.1K/F
R606
20K/F
R603
39.2K/F
C758
1000P/50V
39,40 HP2_JD
Q67
2N7002W-7-F
Q65
2N7002W-7-F
MIC1_JD 40
Layout Note:
Close to the Pin 13
of Codec
SENSEA
+VDDA
R315
5.1K/F
R318
39.2K/F
C431
1000P/50V
39,40 HP1_JD
Q45
2N7002W-7-F
+5V_SPK_AMP
+5V_RUN
L67
BLM21PG600SN1D
FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
C732
1U/10V
CC0603
C744
10U/10V
CC0805
Layout Note:
Place close to pin 8
AZALIA (HD) CODEC
+3.3V_RUN
C720
1U/10V
CC0603
C719
1U/10V
CC0603
C721
0.1U/10V
Depop these for 92HD73C
R595
*100K_NC
C739
*1000P/50V_NC
U46
DVDD_CORE
DVDD_CORE
DVDD
AVDD
AVDD
C747
1U/10V
CC0603
C435
0.1U/10V
SENSE_A
SENSE_B
SENSEA
SENSEB
8 ICH_AZ_CODEC_BITCLK
8 ICH_AZ_CODEC_SDIN0
8 ICH_AZ_CODEC_SDOUT
8 ICH_AZ_CODEC_SYNC
8,29 ICH_AZ_CODEC_RST#
R580
22
HDA_SDI
ICH_AZ_CODEC_BITCLK
HDA_BITCLK
HDA_SDI
HDA_SDO
HDA_SYNC
HDA_RST#
C722
*10P/50V_NC
PORT_A_L
PORT_A_R
NC/VREFOUT_A
AUD_HP1_L0 39
AUD_HP1_R0 39
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
NC/CD_L
NC/CD_GND
NC/CD_R
PORT_D_L
PORT_D_R
VREFOUT_D
AUD_FRONT_L 39,40
AUD_FRONT_R 39,40
PORT_E_L
PORT_E_R
GPIO4/VREFOUT_E
AUD_MIC_L0 40
AUD_MIC_R0 40
AUD_MIC1_VREFO 40
PORT_F_L
PORT_F_R
GPIO3/VREFOUT_F
AUD_HP2_L0 39
AUD_HP2_R0 39
35 DMIC_CLK
+3.3V_RUN
DMIC_CLK
DMIC0/VOL_UP/GPIO1
DMIC1/VOL_DN/GPIO2
PORT_G_L
PORT_G_R
PORT_H_L
PORT_H_R
39 EAPD#
EAPD#
DMIC_CLK/GPIO0/SPDIF_IN
SPDIF_OUT_0
PC_BEEP
CAP2
VREFFILT
AUD_PC_BEEP
35 DMIC_DATA
DMIC_DATA
DVSS1
DVSS2
AVSS1
AVSS2
C752
10U/10V
CC0805
C753
1U/10V
CC0603
92HD73C-C1
+3.3V_RUN
R593
*10K_NC
EAPD#
ICH_AZ_CODEC_BITCLK
R308
*22_NC
C425
*1P/50V_NC
DMIC_CLK
R584
*22_NC
C717
*1P/50V_NC
Close to CODEC
+VDDA
C711
0.1U/16V
CC0603
C725
1U/10V
CC0603
AUD_PC_BEEP
BEEP1
R582 10K
R583
2.2K
BEEP 29
SPKR 8
U41
74LVC1G86GW
QUANTA
COMPUTER
Title
AZELIA CODEC (92HD73C)
Size
Document Number
RM5
Rev
3A
Date:
Thursday, August 20, 2009
Sheet 38 of 61

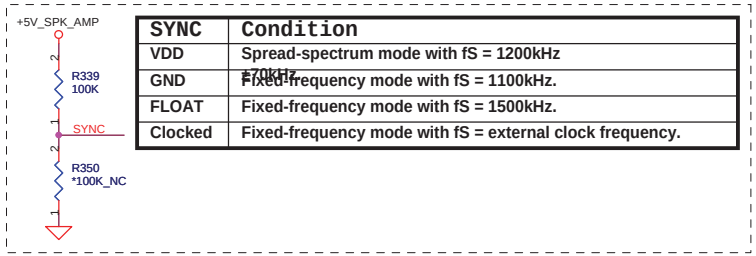
INTERNAL SPEAKER AMP



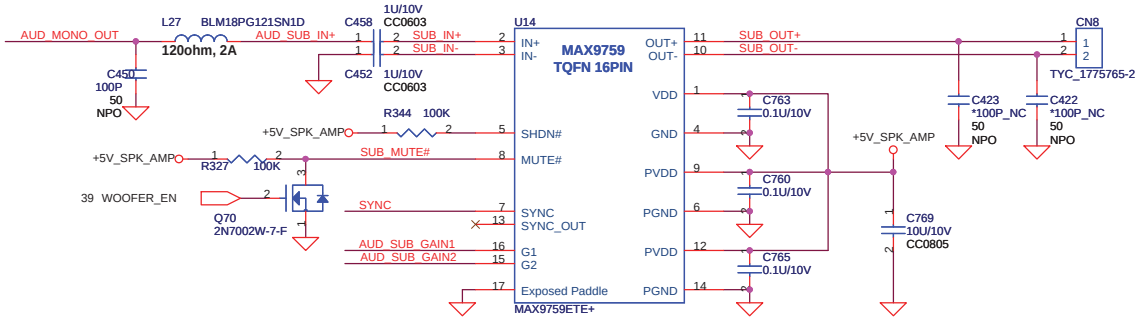
QUANTA COMPUTER

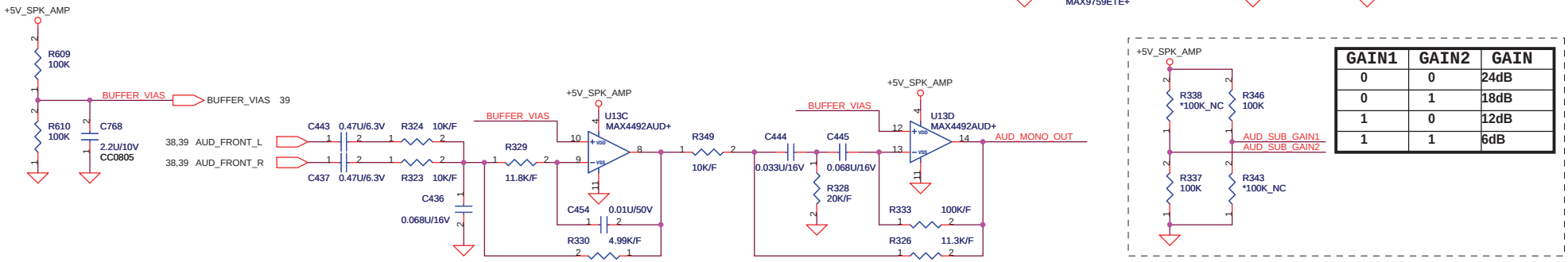
Title	AUDIO AMP	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 39 of 61	

INTERNAL SUBWOOFER AMP



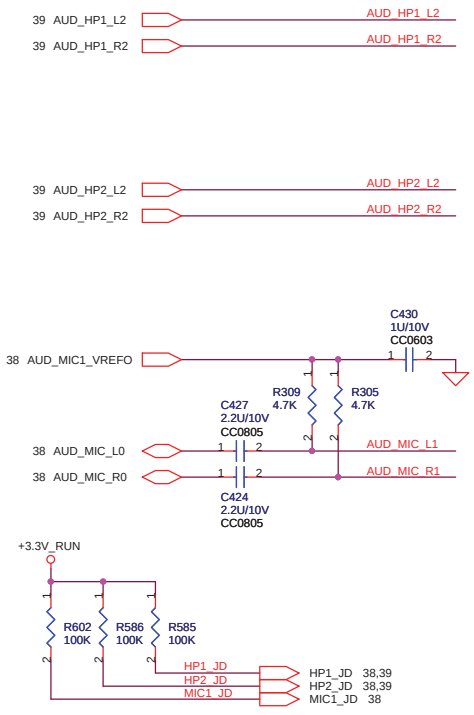
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



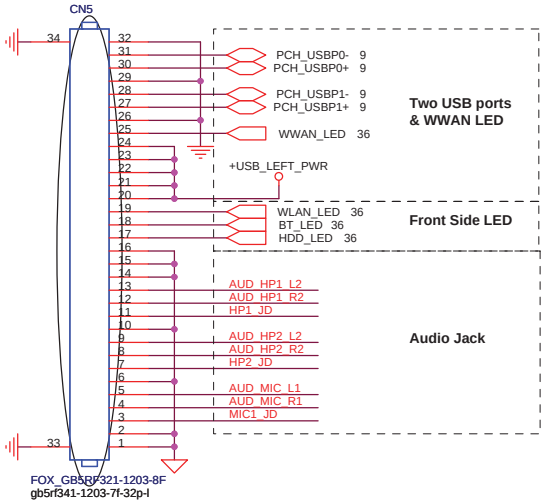


GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

Ambient Parts of Headphone & MIC Jack

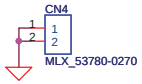


To IB(IO Board) connector



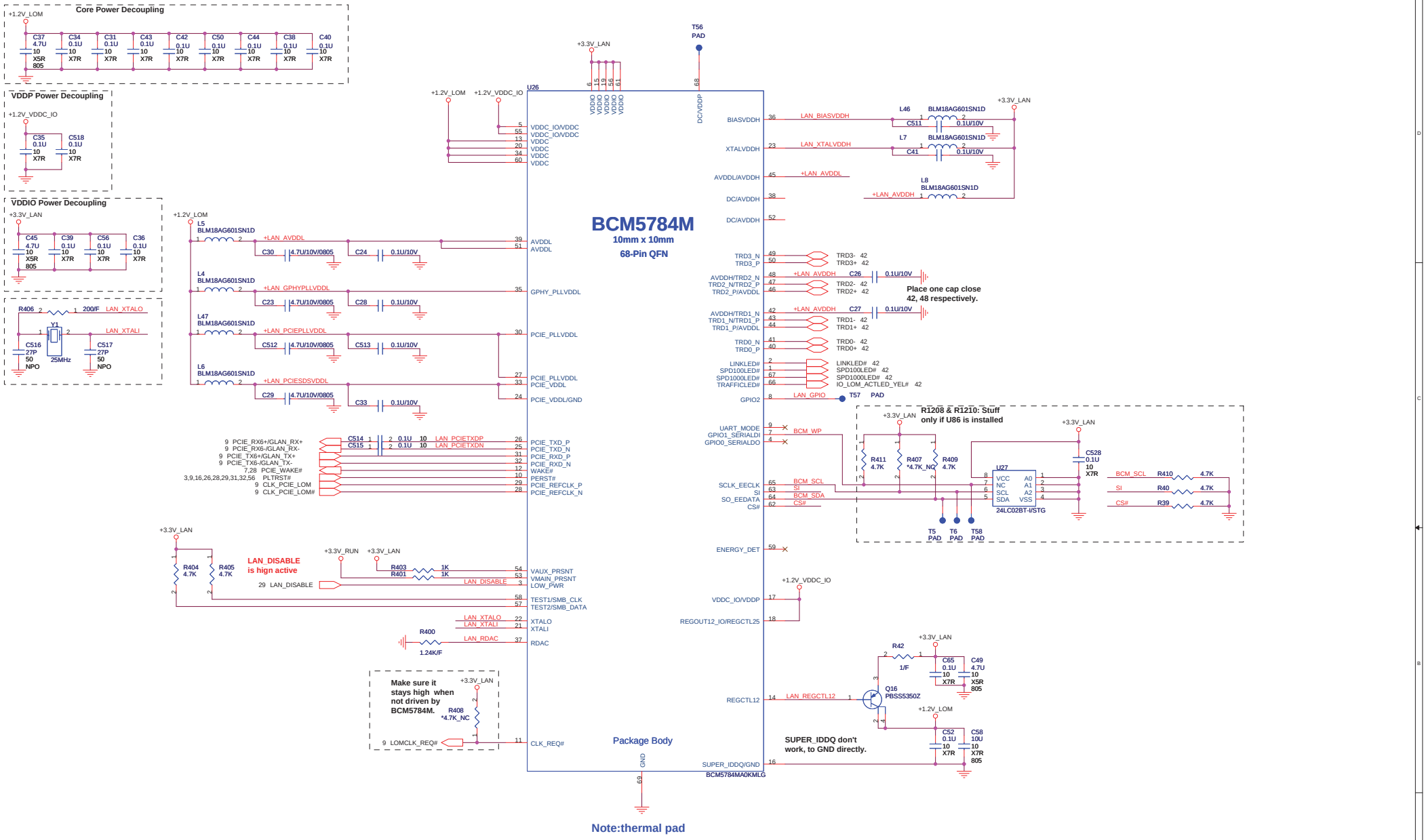
Scott_0123:Change CN5 PN with DFHD32MR003 (FOX).

Adding additional AGND



Title	IB CONN & SUBWOOFER	
Size	Document Number RM5	Rev 3A
Date:	Thursday, August 20, 2009	Sheet 40 of 61

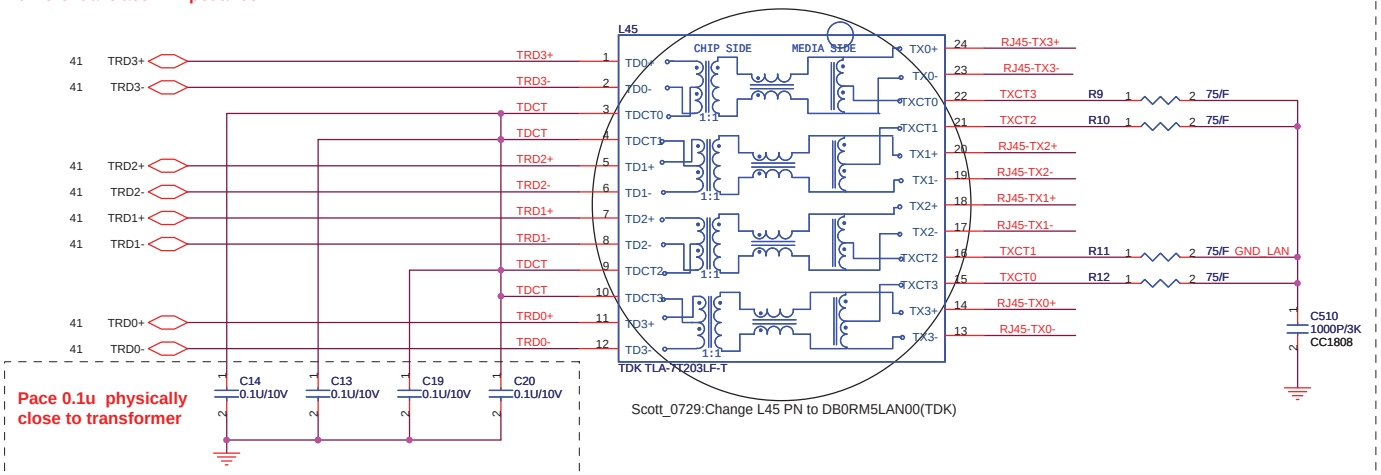
QUANTA COMPUTER



Title	LAN (BCM5784M)
Size	Document Number RM5
Rev	3A
Date:	Thursday, August 20, 2009
Sheet	41 of 61

TRANSFORMER

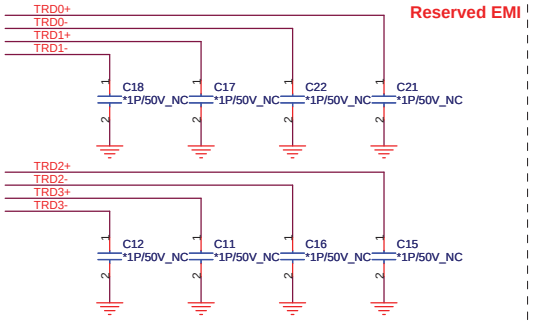
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace immpedance.



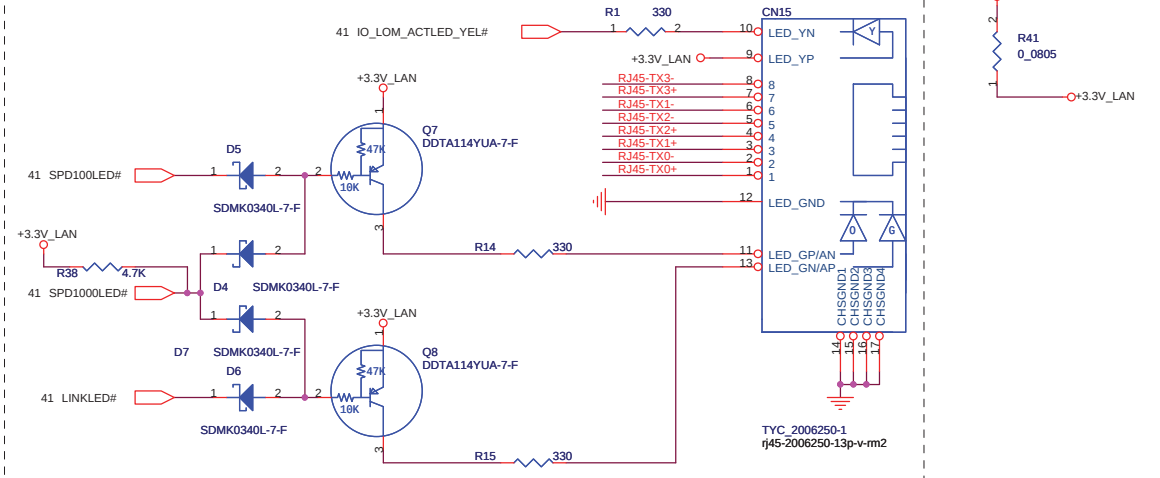
Pace 0.1u physically close to transformer

Scott_0729:Change L45 PN to DB0RM5LAN00(TDK)

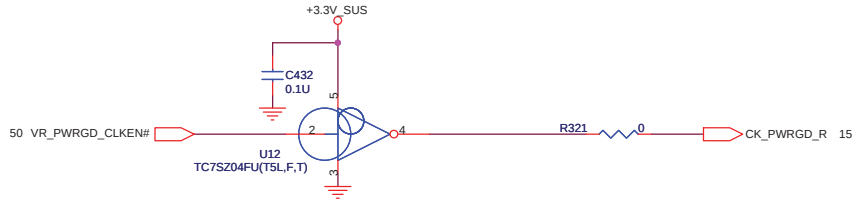
Reserved EMI

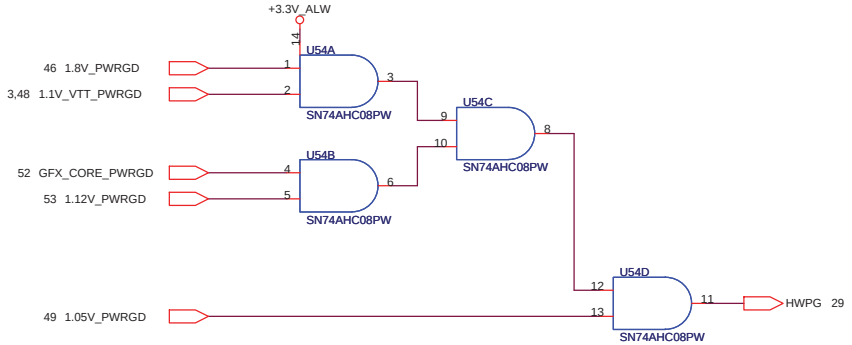


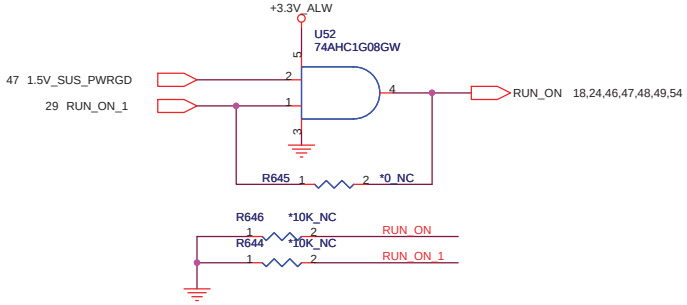
RJ-45 Connector



QUANTA COMPUTER		
Title: LAN SWITCH		
Size	Document Number: RM5	Rev: 3A
Date: Thursday, August 20, 2009	Sheet 42 of 61	



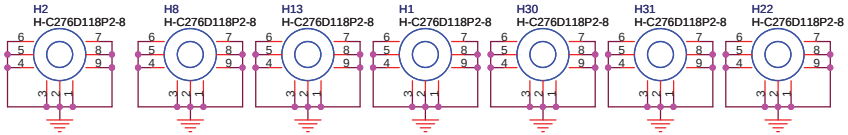




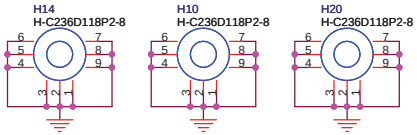
QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 43 of 61	

H-C276D118P2-8 * 7

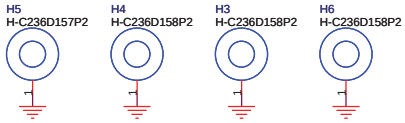


H-C236D118P2-8 * 3

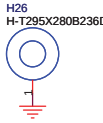


h-c236d197p2 * 1

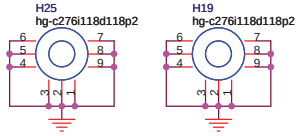
H-C236D158P2 * 4



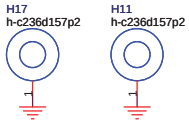
H-T295X280B236D118P2 * 1



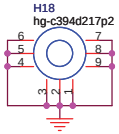
hg-c276i118d118p2 * 2



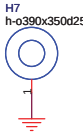
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1

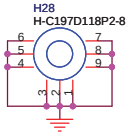


Scott_0731: change H7 & H18 footprint as ME change

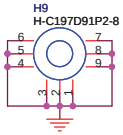
Scott_0812:Delete H7 Pin2~Pin9 for layout requite.

h-c236d236n * 2

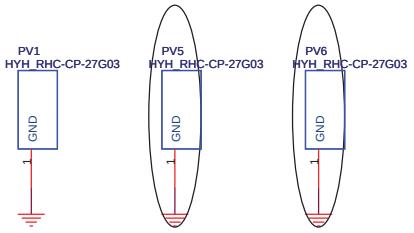
H-C197D118P2-8 * 1



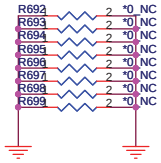
H-C197D91P2-8 * 1



h-o205x157d138x91p2 * 1



Scott_0701:: Added PV6 according to EMI's suggestion

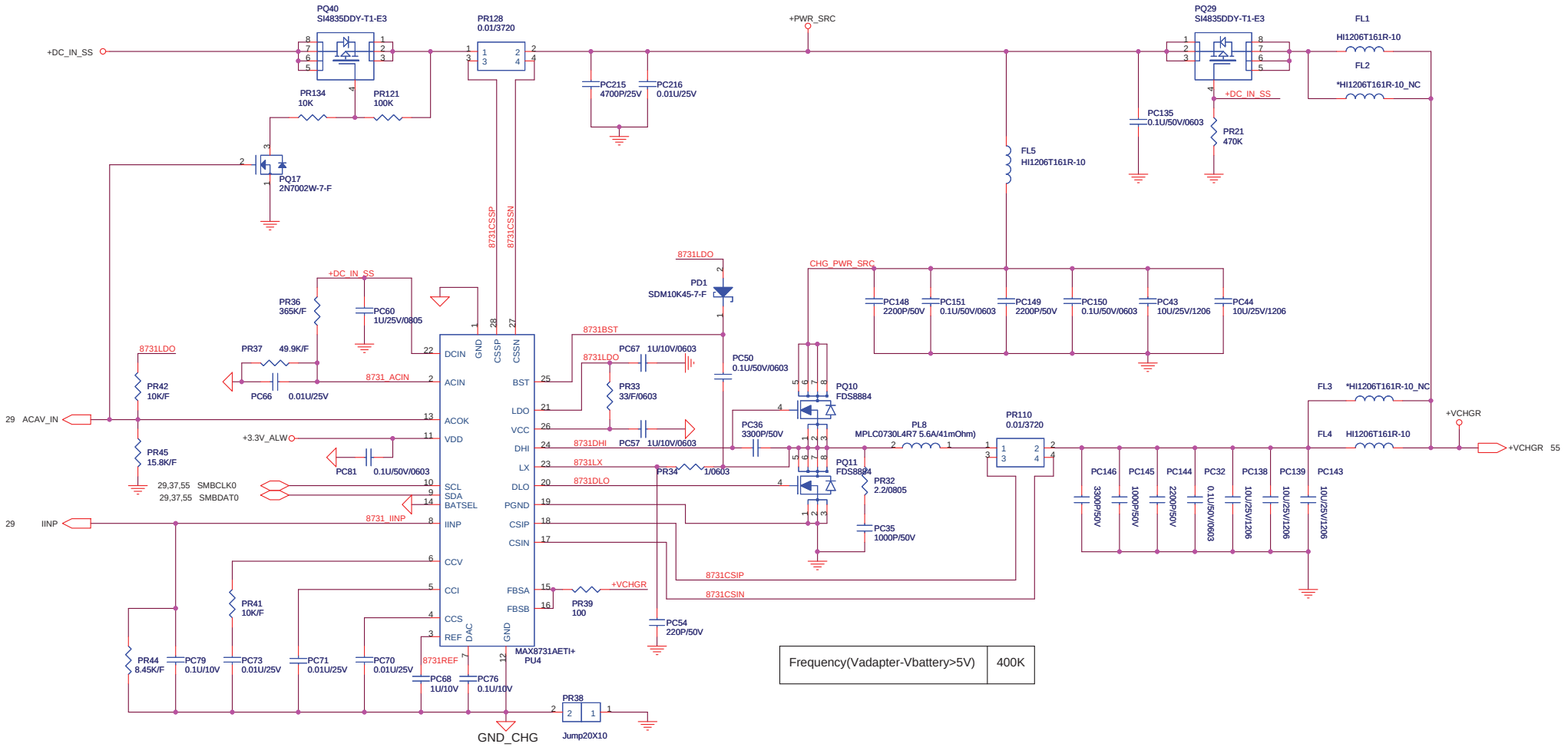


Scott_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

Scott_0707: Reserver R692~R699.

QUANTA COMPUTER

Title	PAD & SCREW & SPRING	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 44 of 61	

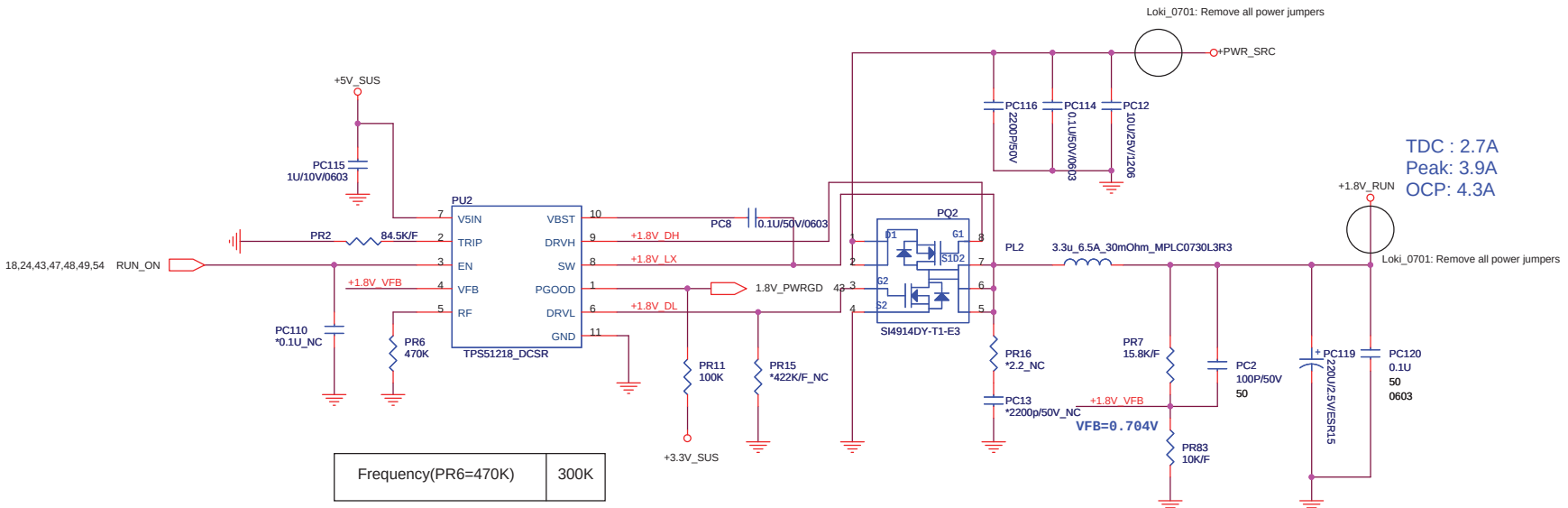


Frequency(Vadapter-Vbattery>5V)	400K

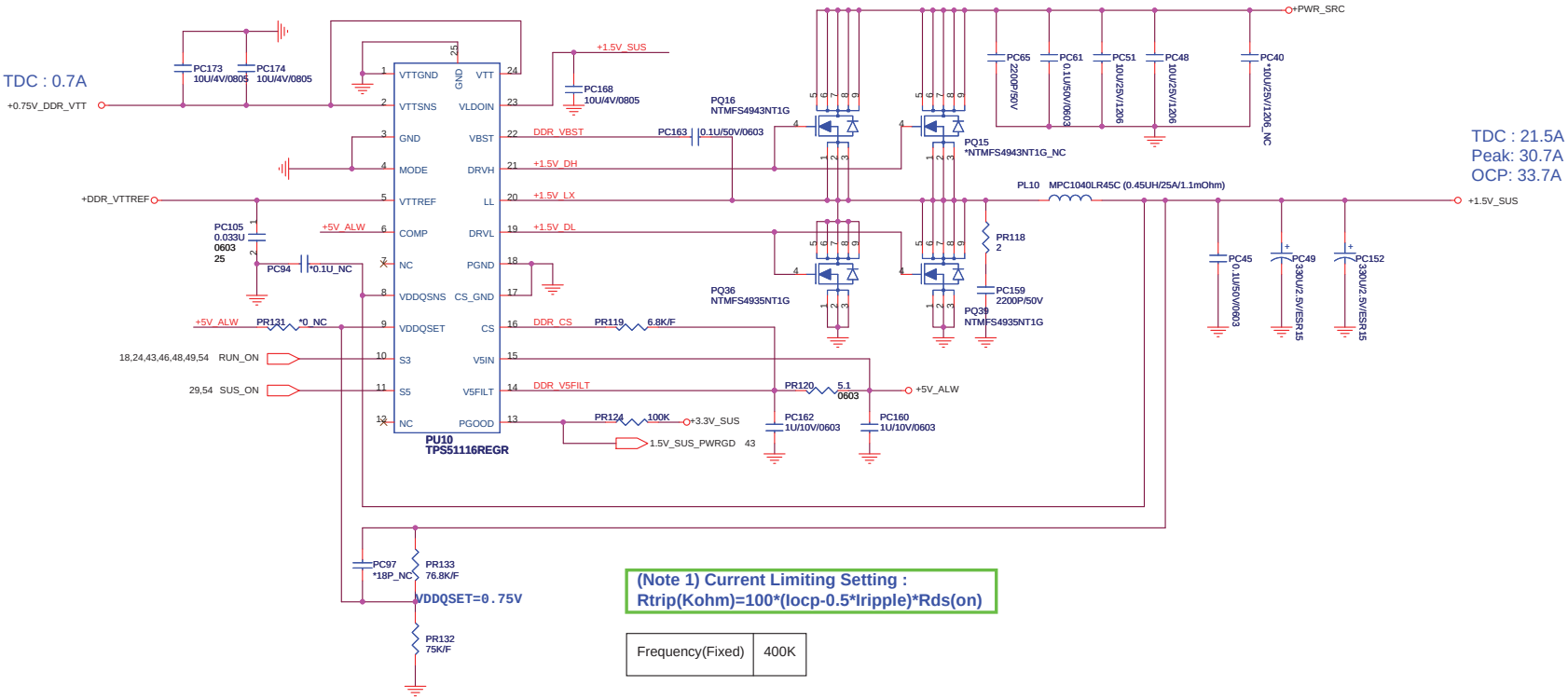
QUANTA COMPUTER

Title	CHARGER (MAX8731A)	
Size	Document Number RM3	Rev 3A
Date:	Sheet 45 of 61	

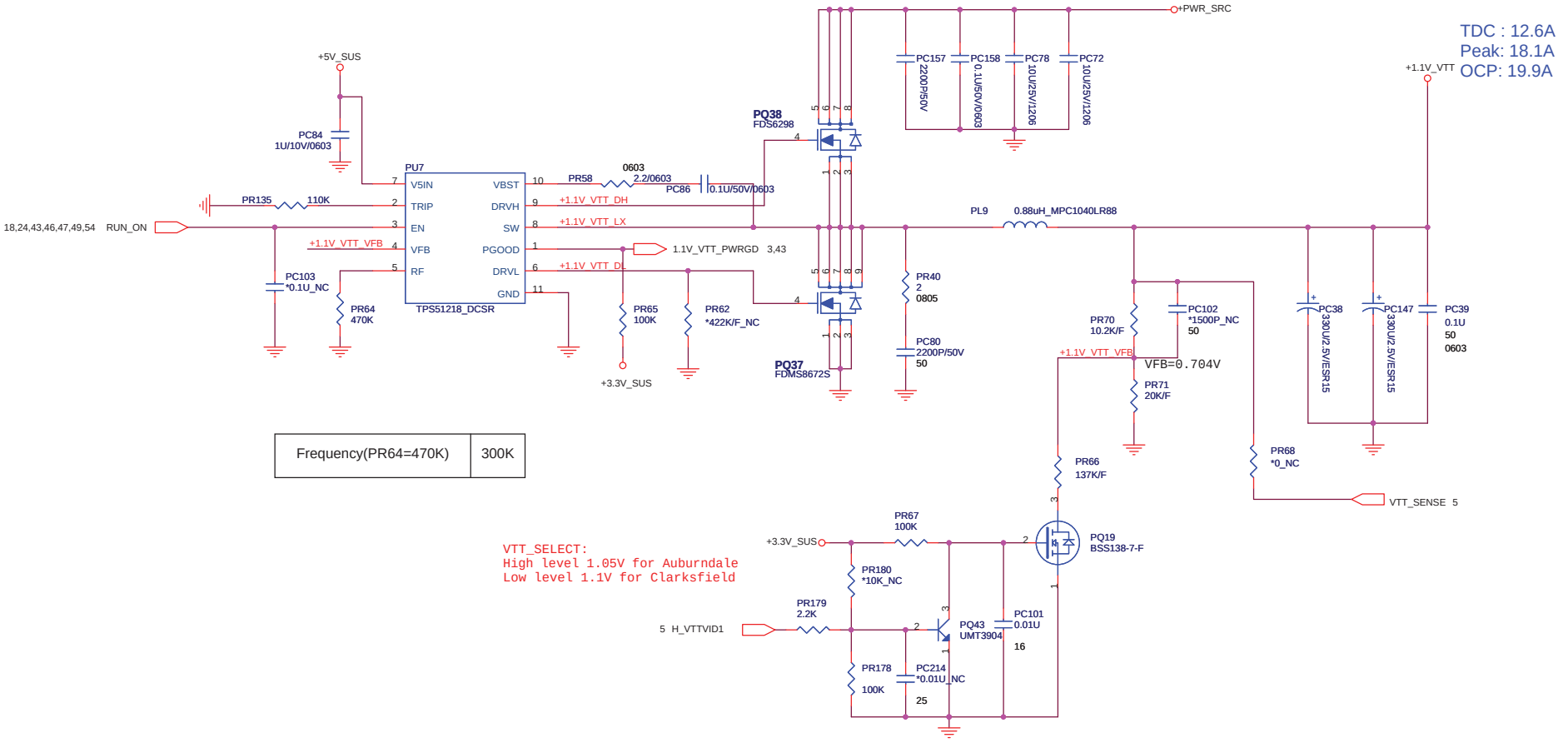
2005/4/21



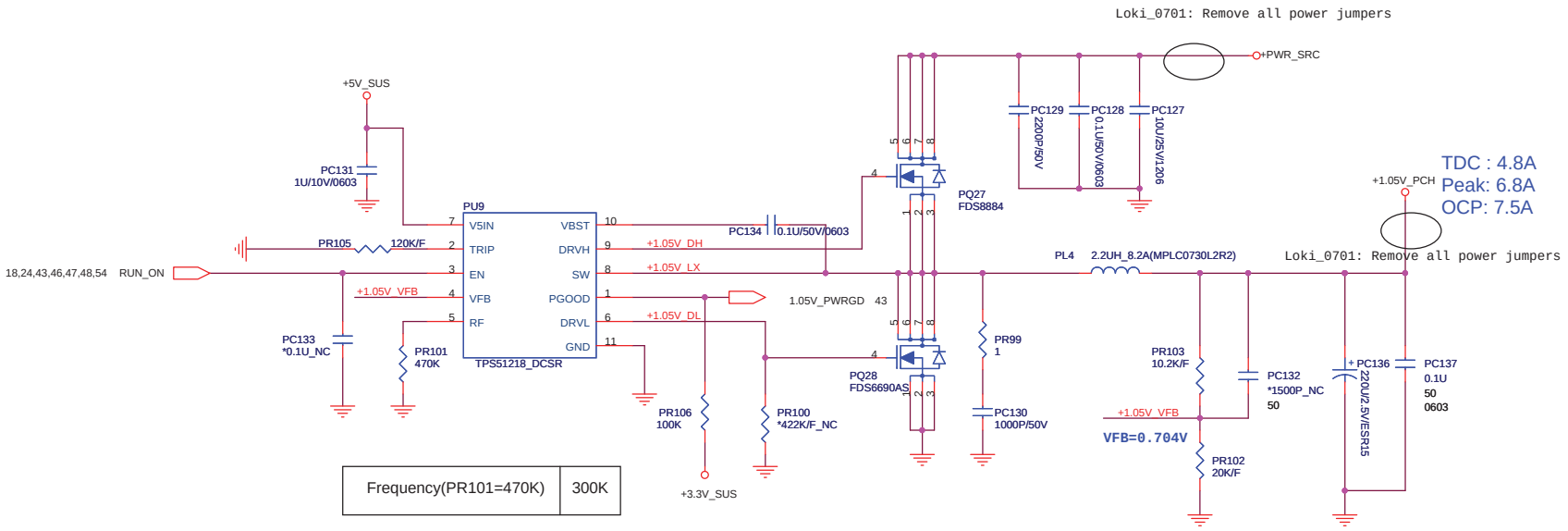
Title	+1.8V_RUN(TPS51218)
Size	Document Number RM5 — Rev 3A
Date:	Thursday, August 20, 2009 — Sheet 46 of 61



Title	+1.5V_SUS/+0.75V_VTT(TPS51218)
Size	Document Number RM5
Rev	3A
Date:	Thursday, August 20, 2009
Sheet	47 of 61



Title	+1.1V_VTT(TPS51218)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 48 of 61	

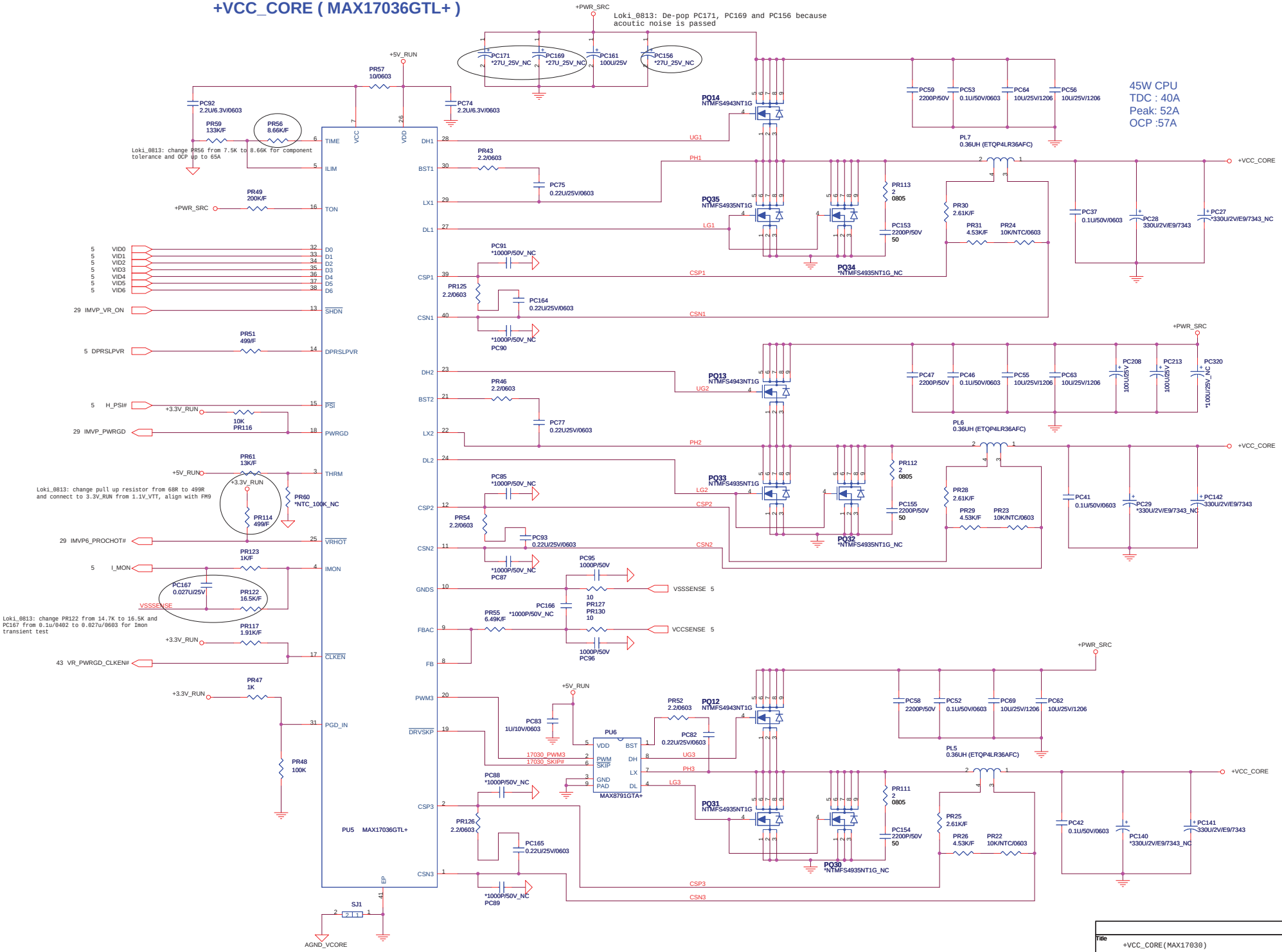


Title	+1.05V_PCH(TPS51218)
Size	Document Number: RM5 — Rev: 3A
Date:	Thursday, August 20, 2009 — Sheet 49 of 61

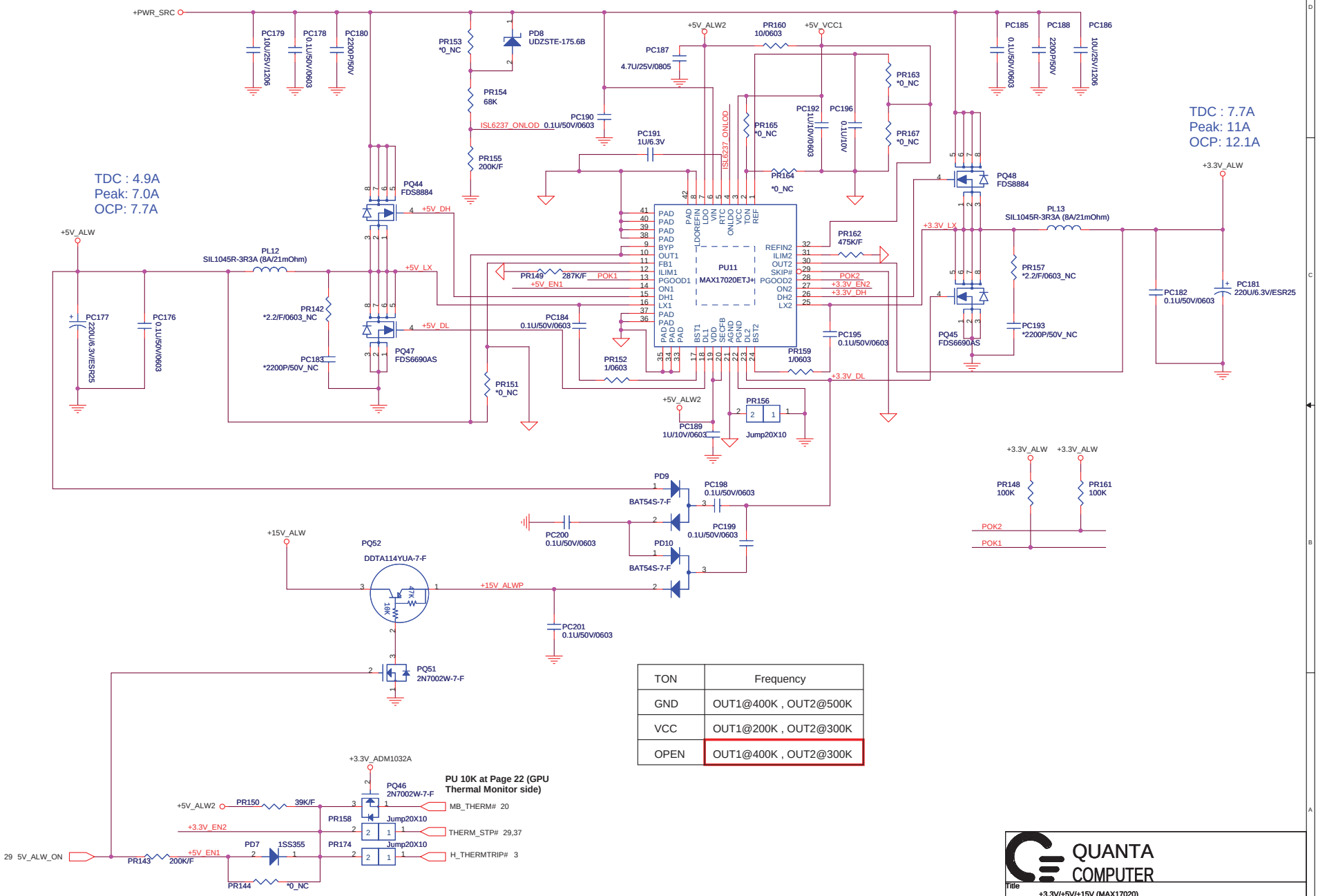
+VCC_CORE (MAX17036GTL+)

Loki_0813: De-pop PC171, PC169 and PC156 because acoutic noise is passed

45W CPU
TDC : 40A
Peak: 52A
OCP :57A



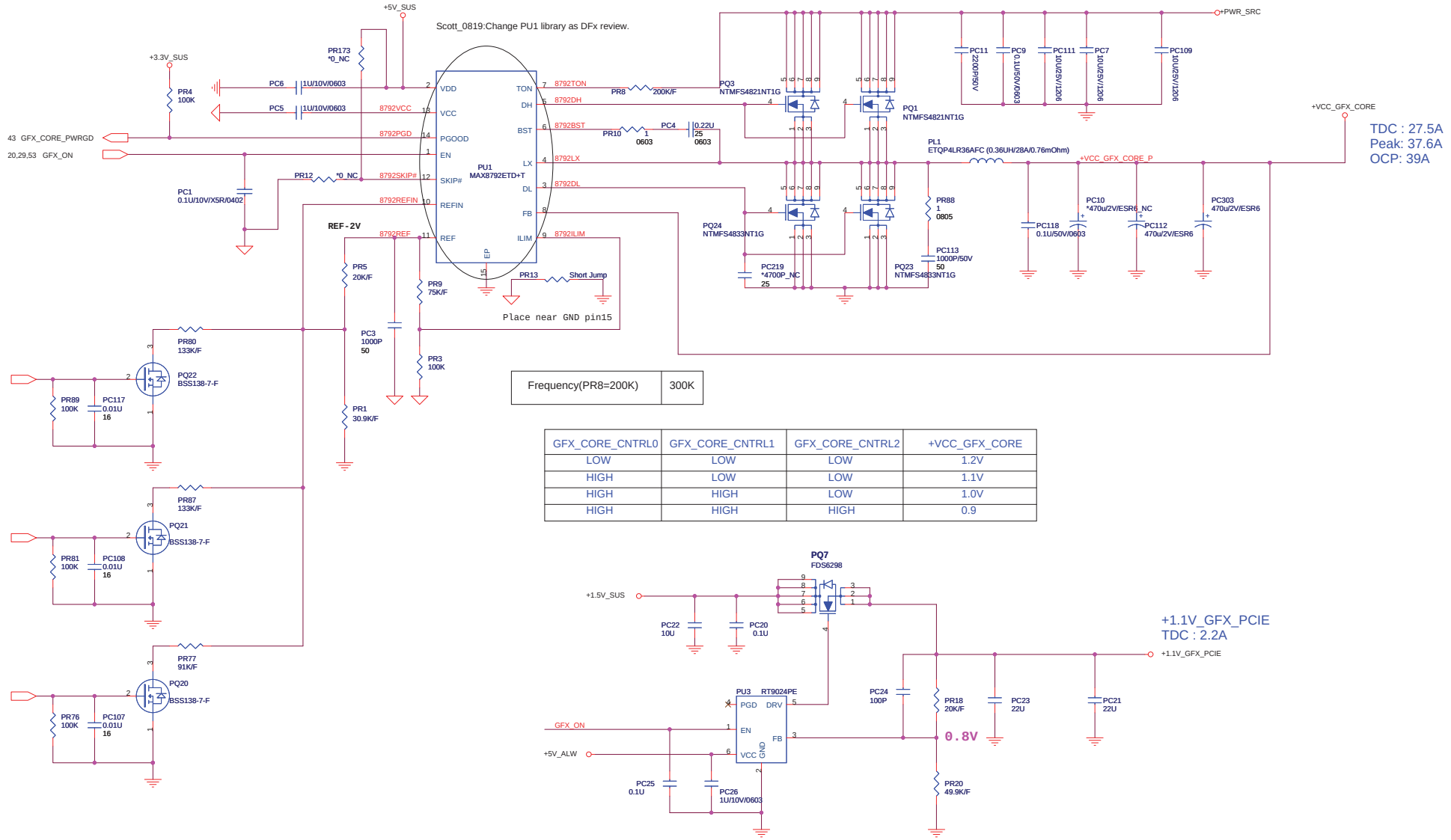
Title	+VCC_CORE(MAX17030)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 50 of 61	



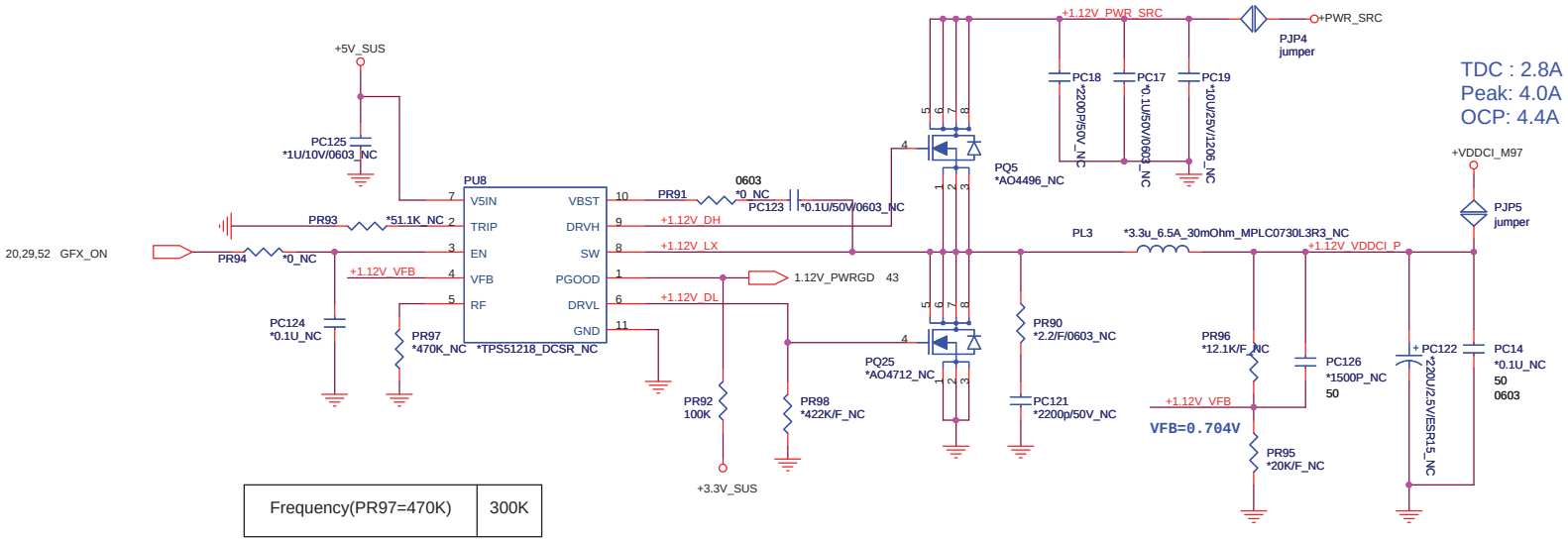
TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K

QUANTA COMPUTER

Title	+3.3V/+5V/+15V (MAX17020)		
Size	Document Number RM5		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 51 of 61	

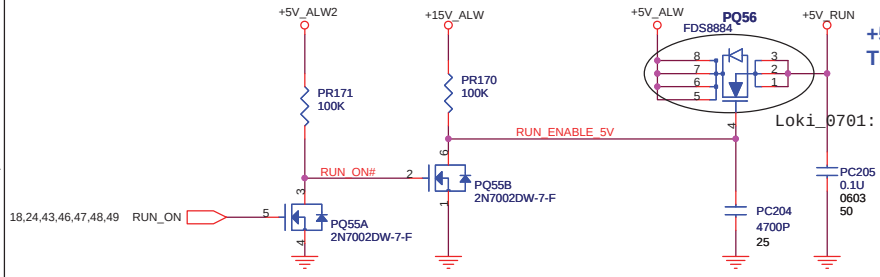


Title	+VGA_M97(MAX8792)		
Size	Document Number RM5		Rev 3A
Date: Thursday, August 20, 2009	Sheet 52 of 61		



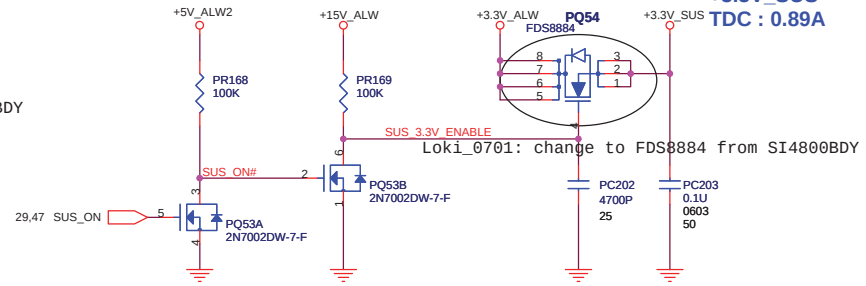
Frequency(PR97=470K)	300K

Title	+VDDCI_M97(TPS51218)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 53 of 61	



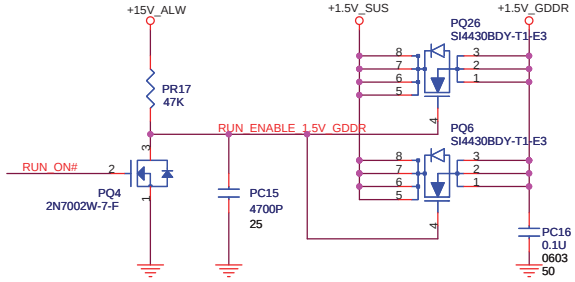
+5V_RUN
TDC :0.791A

Loki_0701: change to FDS8884 from SI4800BDY

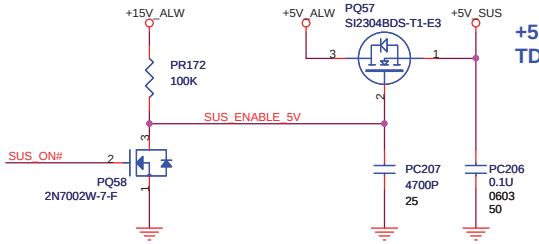


+3.3V_SUS
TDC : 0.89A

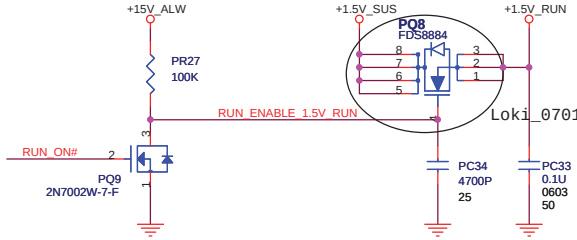
Loki_0701: change to FDS8884 from SI4800BDY



+1.5V_GDDR
TDC : 8.68A

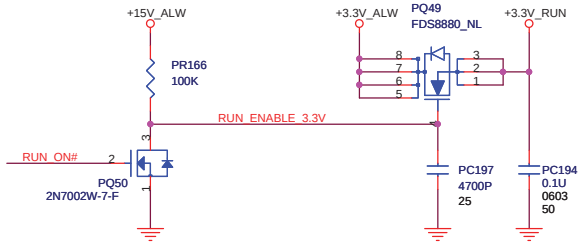


+5V_SUS
TDC : 42mA



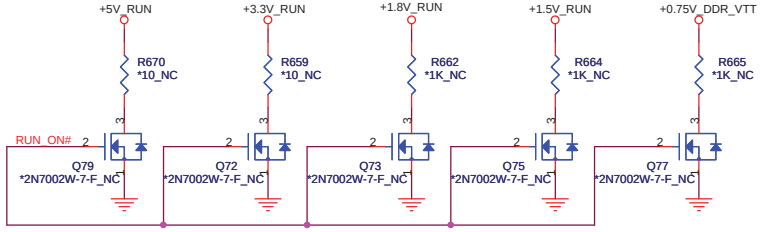
+1.5V_RUN
TDC : 1.05A

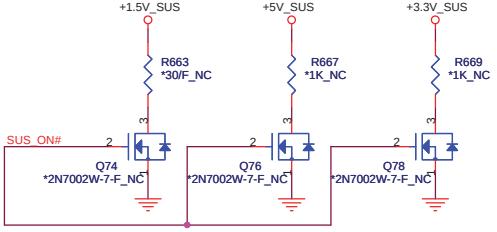
Loki_0701: change to FDS8884 from SI4800BDY



+3.3V_RUN
TDC : 6A

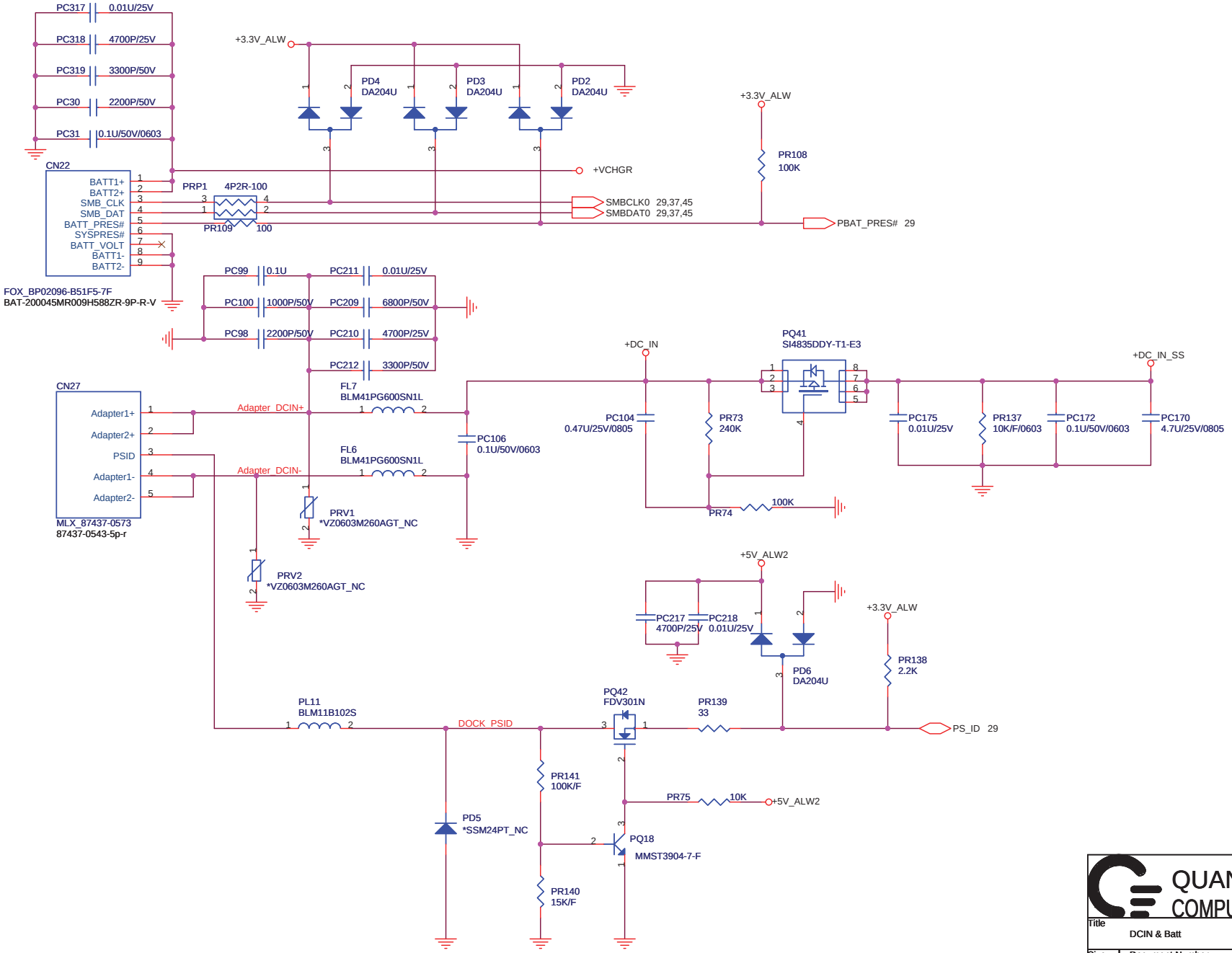
Reserve discharge path





QUANTA COMPUTER

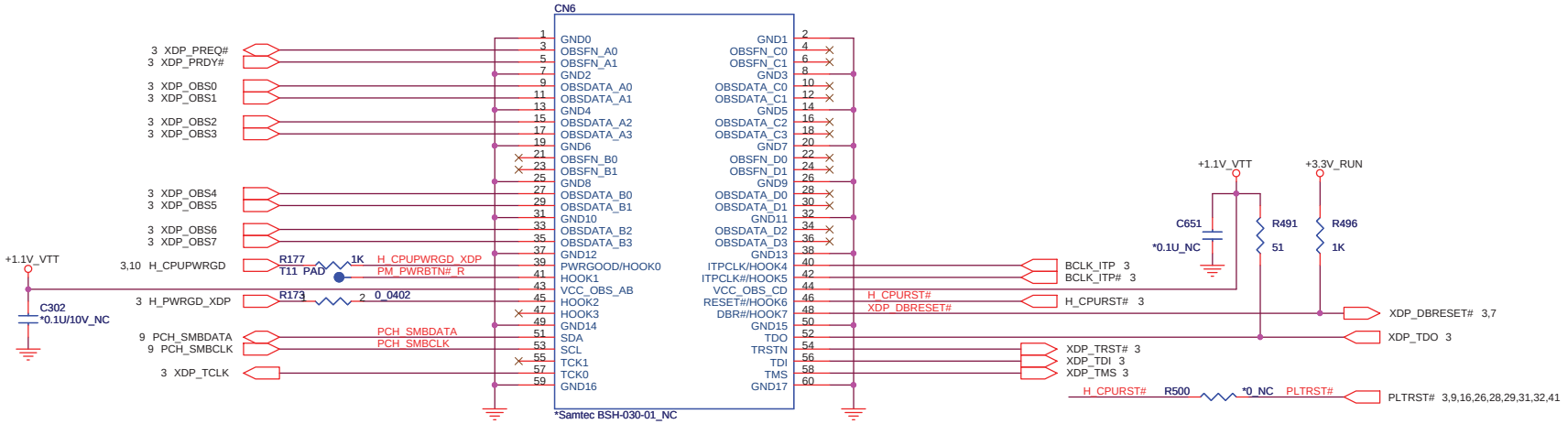
Title	RUN POWER SW	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 54 of 61	



QUANTA COMPUTER

Title	DCIN & Batt	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 55 of 61	

CPU XDP



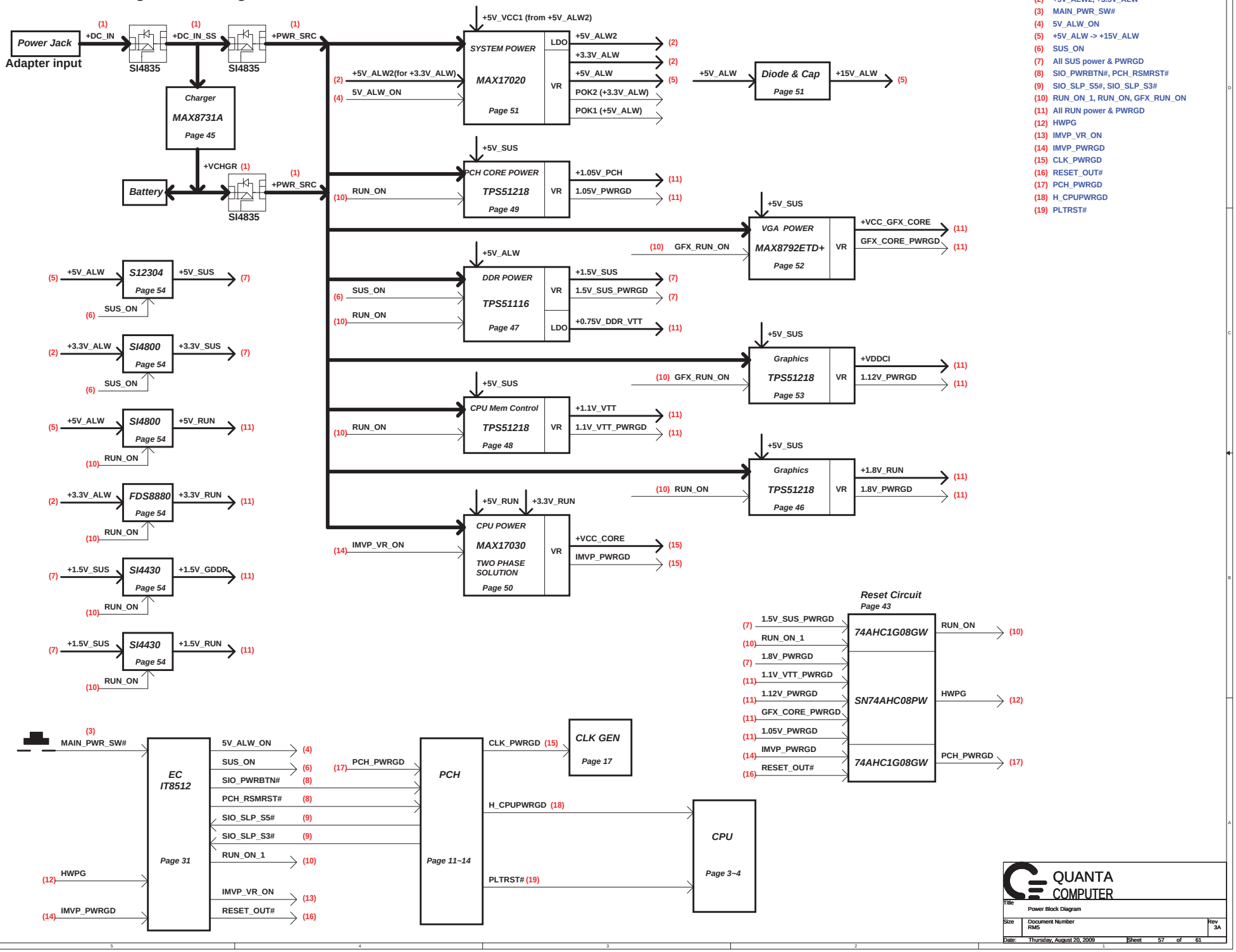
PCH XDP

DEL PCH XDP as FM9 confirmed with Intel that its not necessary!

QUANTA COMPUTER

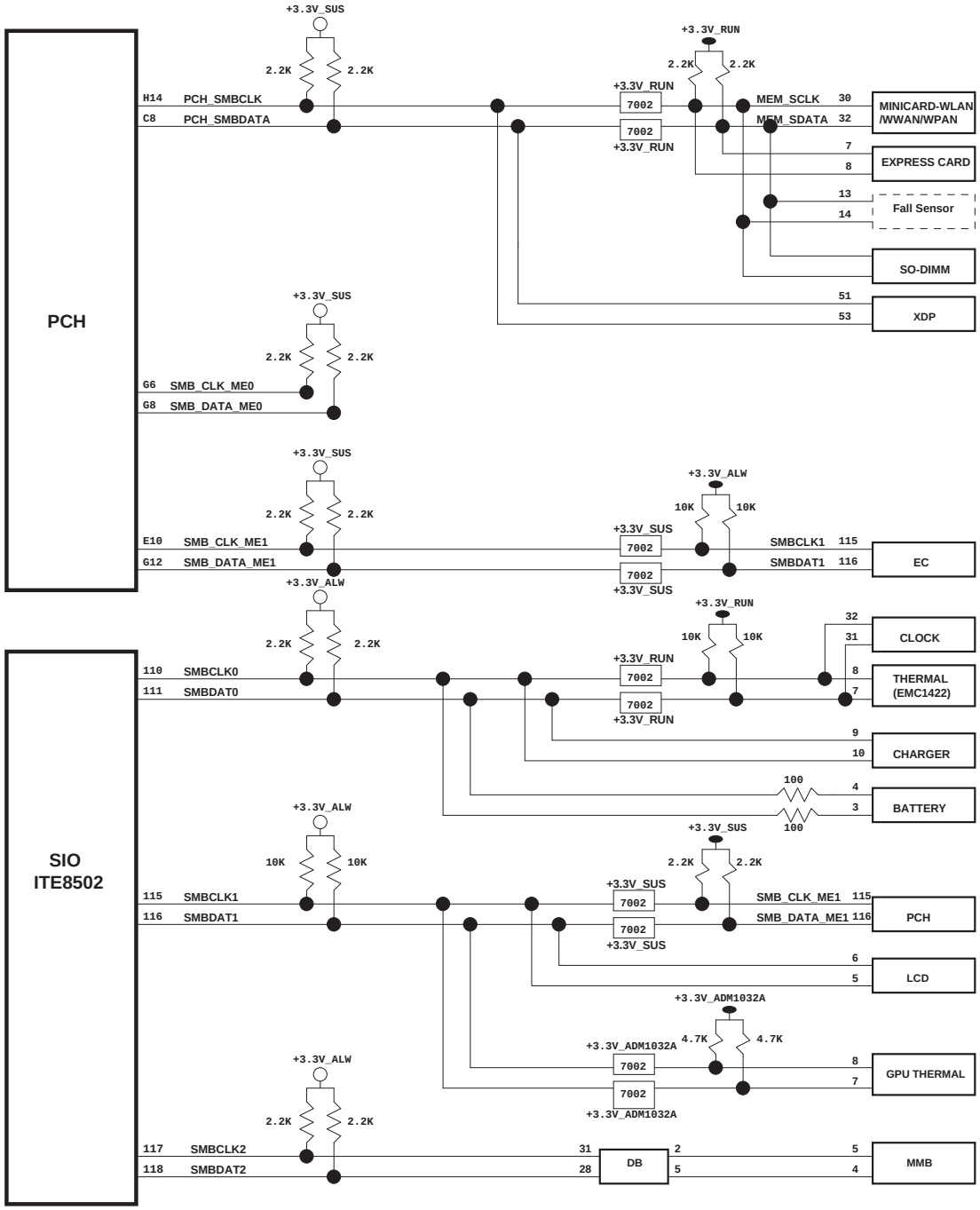
Title	XDP Connector	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 56 of 61	

RM5 Power Design Block Diagram 2009/02/25



Title	Power Block Diagram
Size	Document Number RM5 — Rev 3A
Date:	Thursday, August 20, 2009 — Sheet 57 of 61

QUANTA COMPUTER



QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number RMS	Rev 3A
Date: Thursday, August 20, 2009	Sheet 58 of 61	

POWER STATES

State \ Signal	SLP_S3#	SLP_S4#	SLP_S5#	S4_STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane / State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	
S3	ON	ON	ON	OFF	
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	
no AC/Battery	ON	OFF	OFF	OFF	

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH
IBEX PEAK-M

USB PORT#	DESTINATION
0	Side pair Top / left
1	Side pair Bottom / left
2	USB W/ E-SATA port
3	Reserved
4	Mini Card (WLAN)
5	Mini Card (WWAN)
6	Reserved
7	Reserved
8	Mini Card (WPAN)
9	TV
10	Express Card
11	Camera

PCH
IBEX PEAK-M

PCI EXPRESS	DESTINATION
Lane 1	Mini Card-1 WWAN
Lane 2	Mini Card-2 WLAN
Lane 3	Mini Card-3 WPAN
Lane 4	Express Card
Lane 5	Cardreader
Lane 6	LOM

QUANTA COMPUTER

Title	Power statu	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 59 of 61	