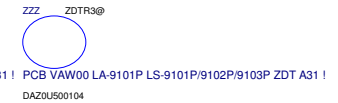
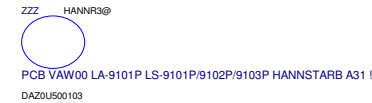
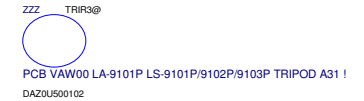
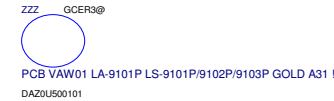


MODEL NAME : VAW01
 PROJECT CODE : ANRVAW0100
 PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B
 DA40001FO00 LS-9101P POWER BUTTON/B
 DA40001FP00 LS-9102P USB/B
 DA40001FQ00 LS-9103P TP BUTTON/B



Dell / Compal Confidential

Schematic Document

Intel Chief River Ivy Bridge (BGA) + Panther Point OAK 15" UMA/DIS AMD Mars Pro

2012-08-22

Rev: 0.4

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB9012@ : ENE KB9012 Implemented

UMA@ : Only for UMA

EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented

GCLKUMA@ : Green CLK for UMA

GCLKDIS@ : Green CLK for DIS

XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N

R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G

i3VOSR1@ : CPU i3-2365 1.4G

i5R1@ : CPU i5-3317 1.7G

i7R1@ : CPU i7-3517 1.9G

CEL1@ : CPU Celeron 887 1.5G

PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete

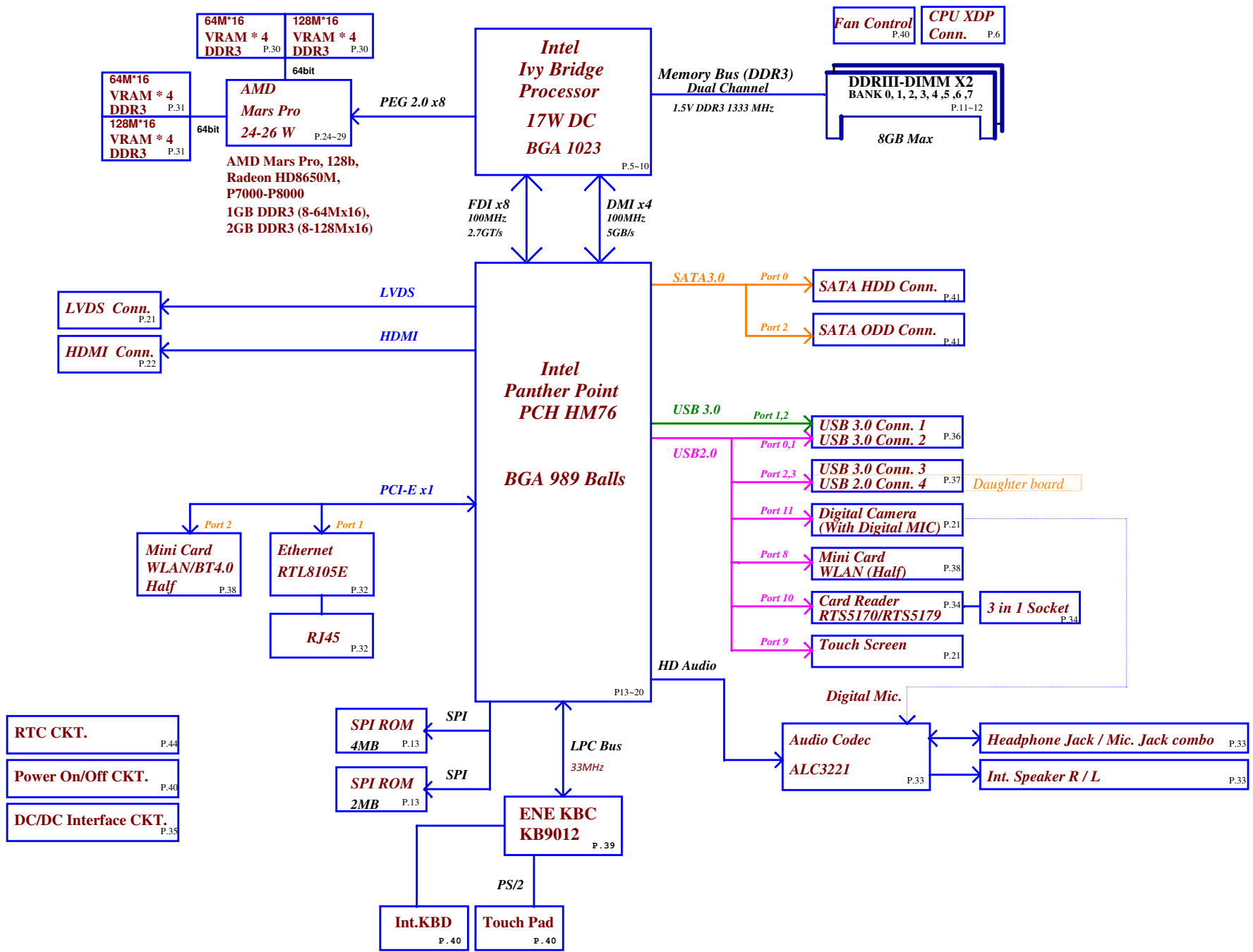
TH@/THR1@ : Thames-XT

MS@/MSR1@ : Mars Pro

X76@ :

SPI-ROM & VRAM Group

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				Rev 0.4

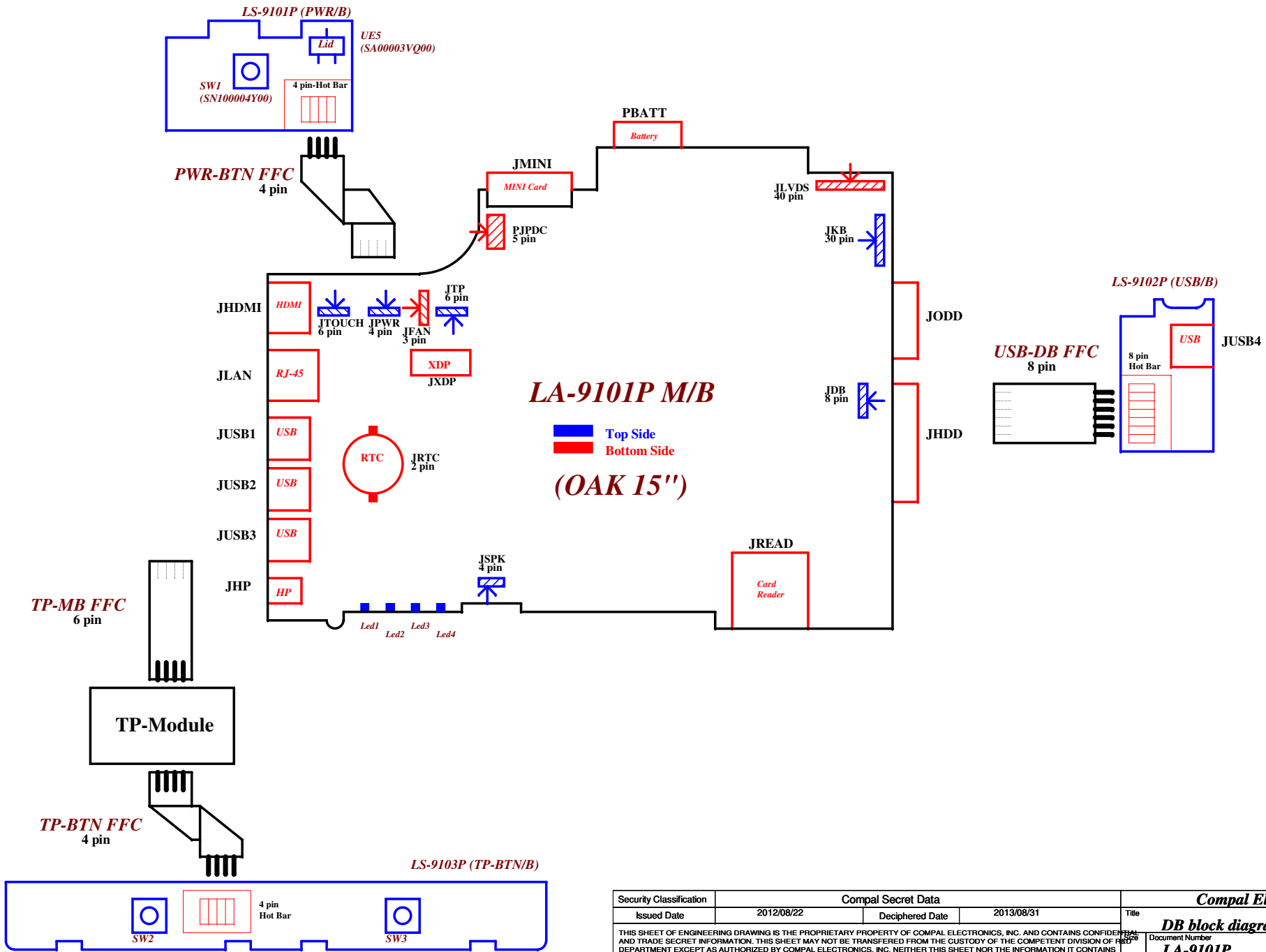


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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title
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Size	Document Number	Rev	0.4	
	LA-9101P			
Date:	Wednesday, August 29, 2012	Sheet	2	of 57

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Project Code : VAW01

File Name : LA-9101P



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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	DB block diagram
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				LA-9101P	0.4
				Date: Wednesday, August 29, 2012	Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

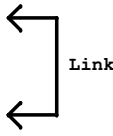
ID	PCB Revision	UMA	THM	MARS
0	0.1			
1		0.1	0.1	
2	0.2			
3		0.2	0.2	
4	0.3			
5	0.4	0.3	0.3	
6	1.0		0.4	
7		1.0	1.0	

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDPA	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
13	NC	

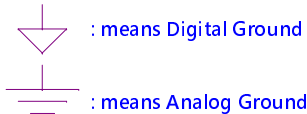
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None			

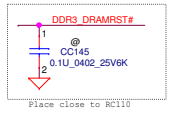
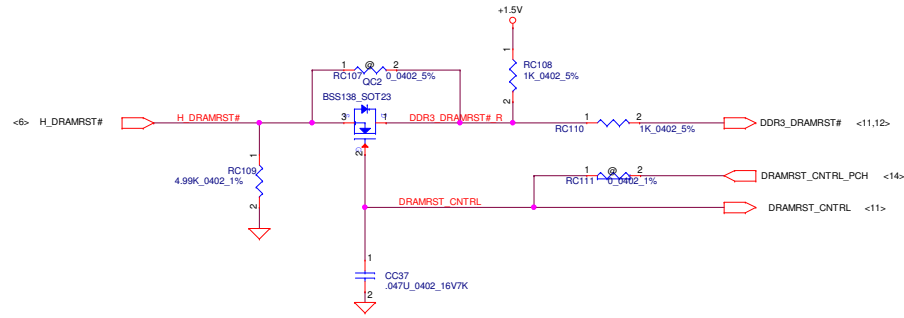
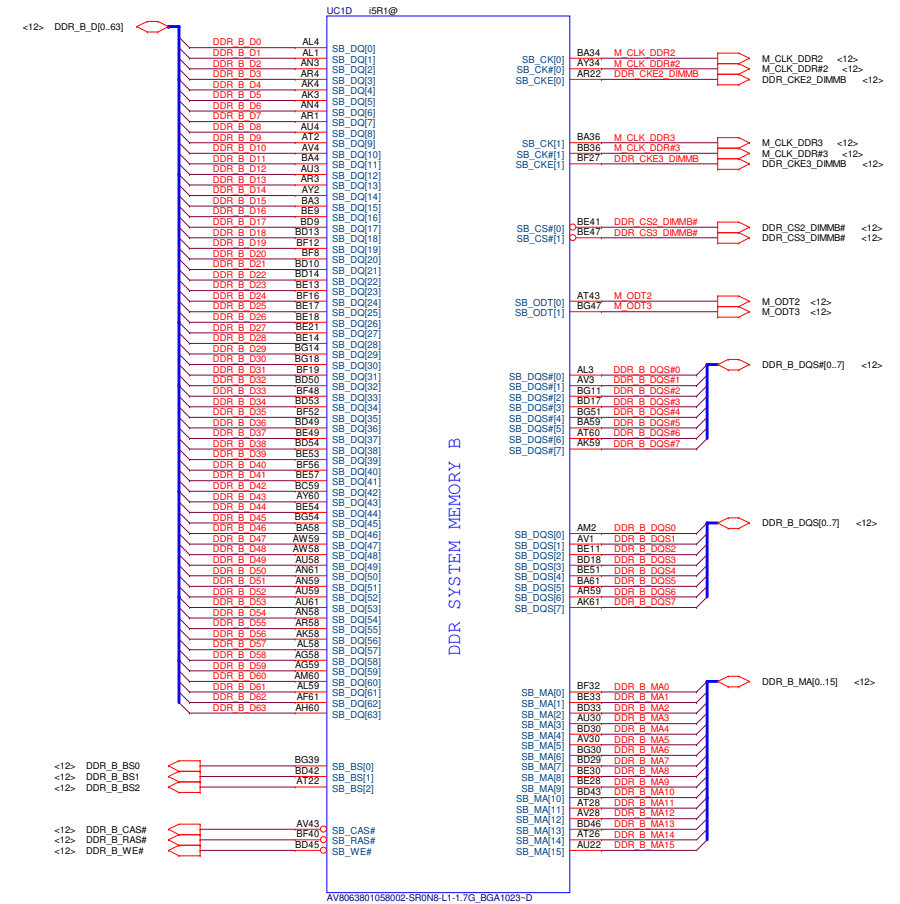
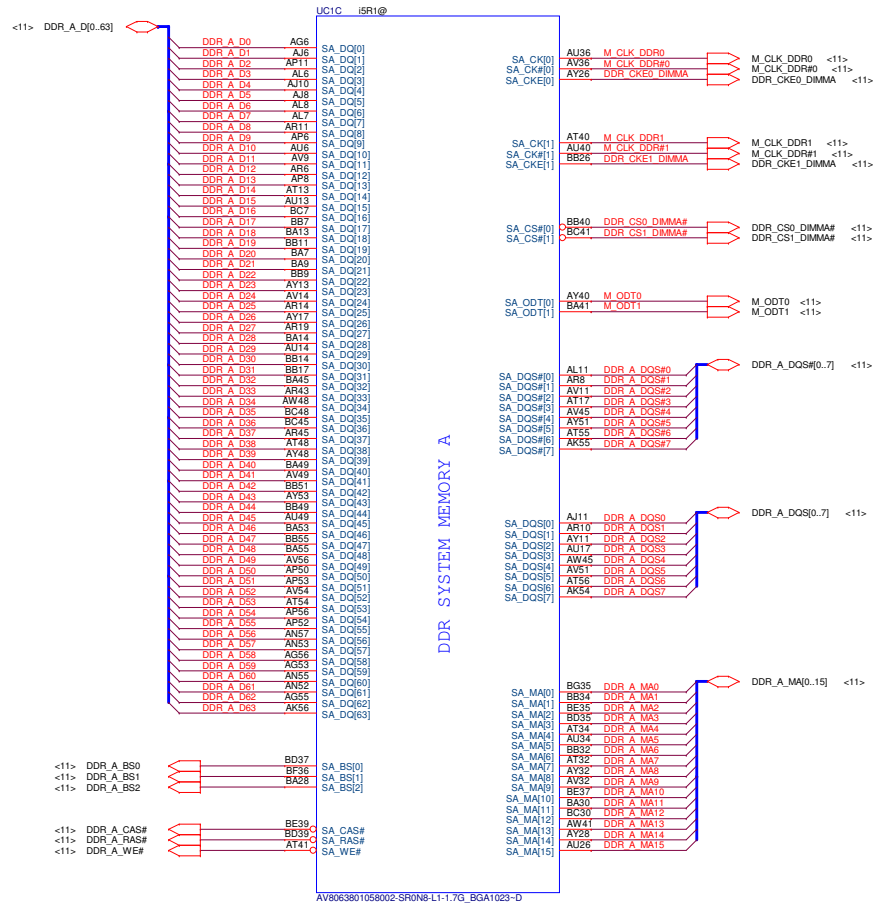
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

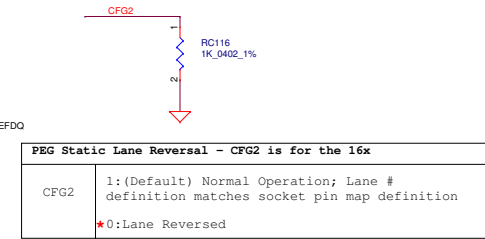
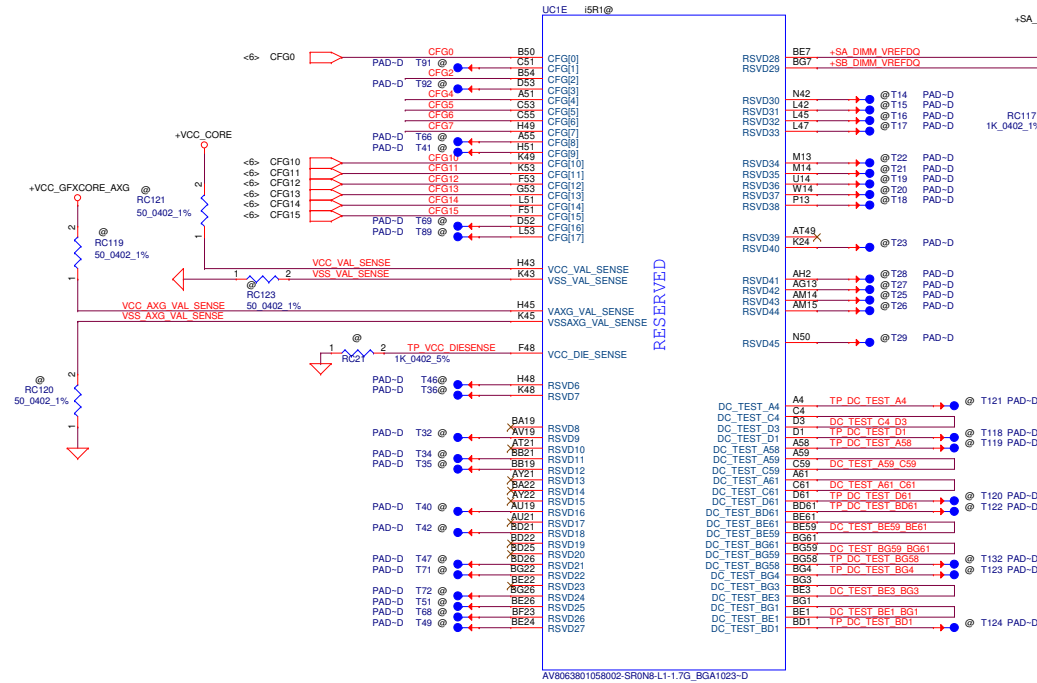
Symbol Note :





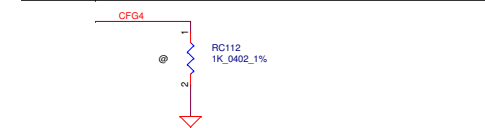
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Issued Date	2012/08/22		Deciphered Date		2013/08/31		Compal Electronics, Inc.		
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Document Number LA-9101P								Date: Wednesday, August 28, 2012	
Sheet 7 of 57									

CFG Straps for Processor



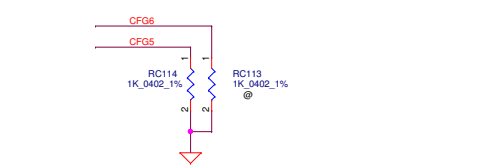
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



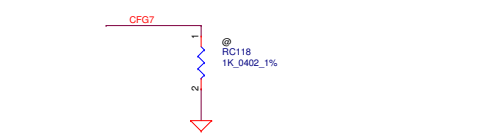
Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps

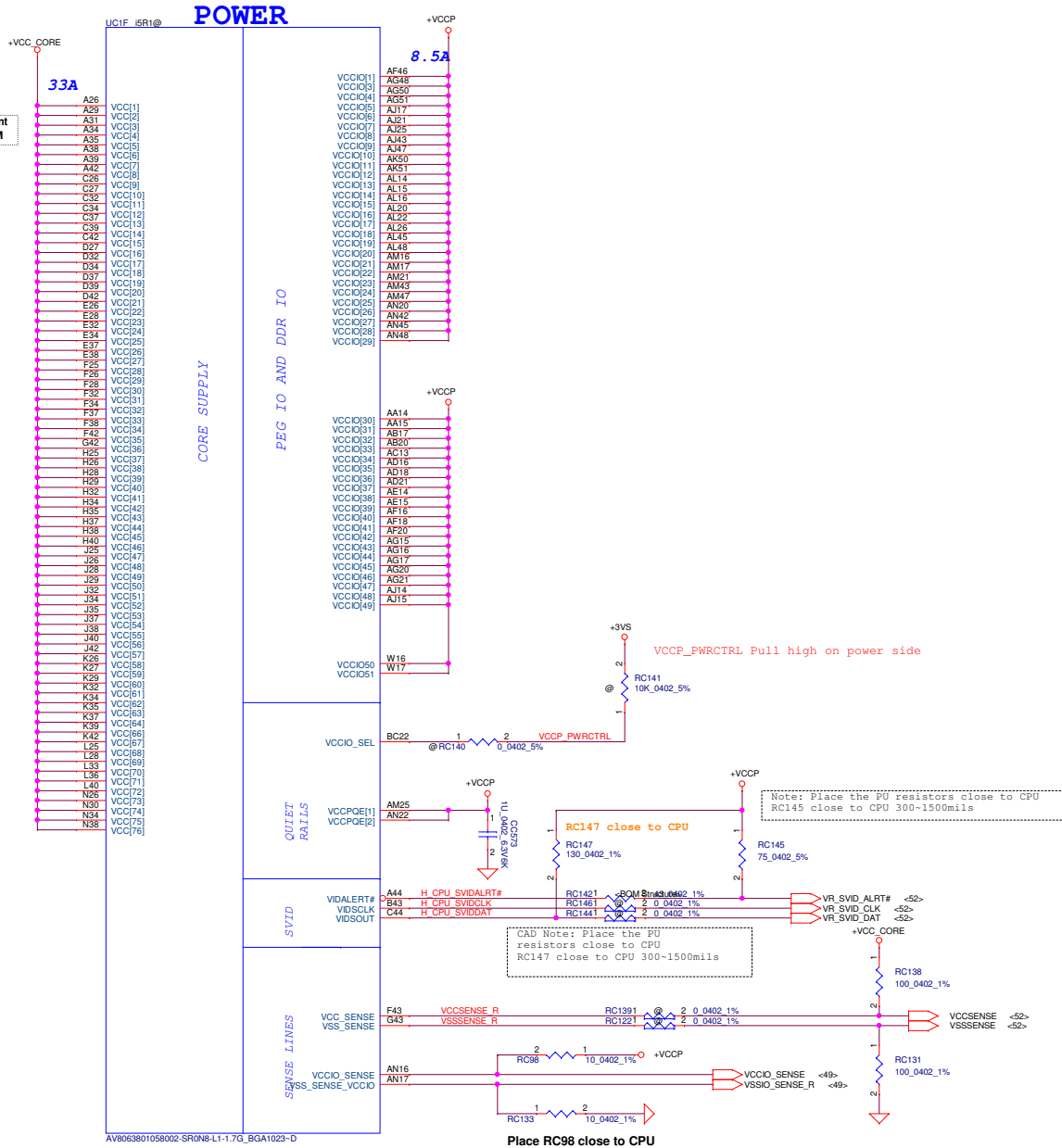
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

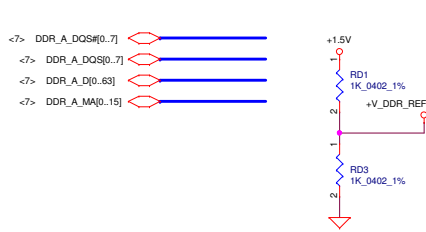
ULV 17W , Max Current
in Turbo Mode or HFM



Iccmax current changed for PDDG Rev0.7

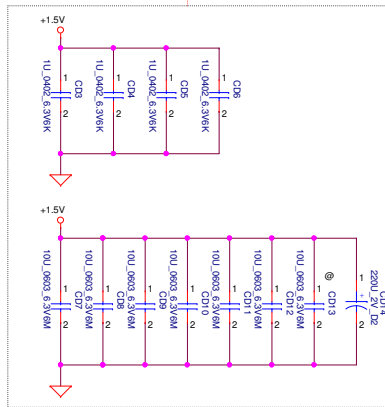
CPU Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

* Description
 5A to Mem controller (+1.5V_CPU_VDDQ)
 5-6A to 2 DIMMs/channel
 2-5A to +1.5V_RUN & +0.75V_DDR_VTT

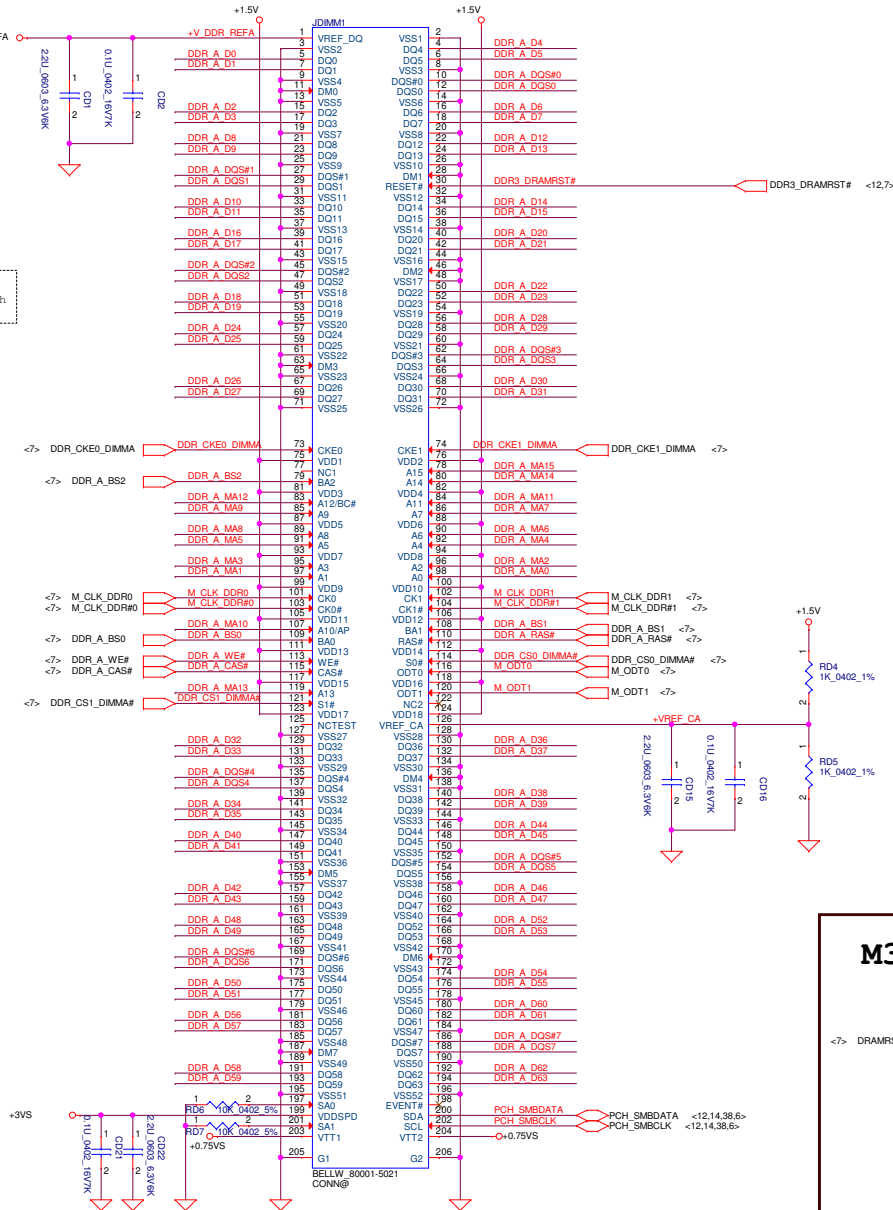
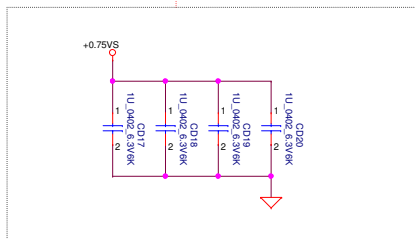


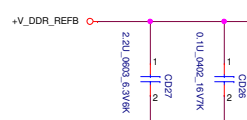
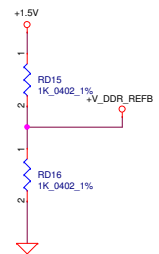
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width



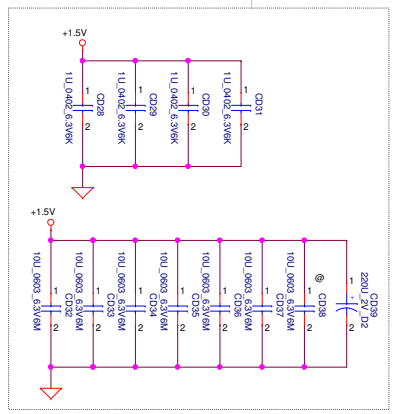
Layout Note:
Place near JDIMM1. 203, 204



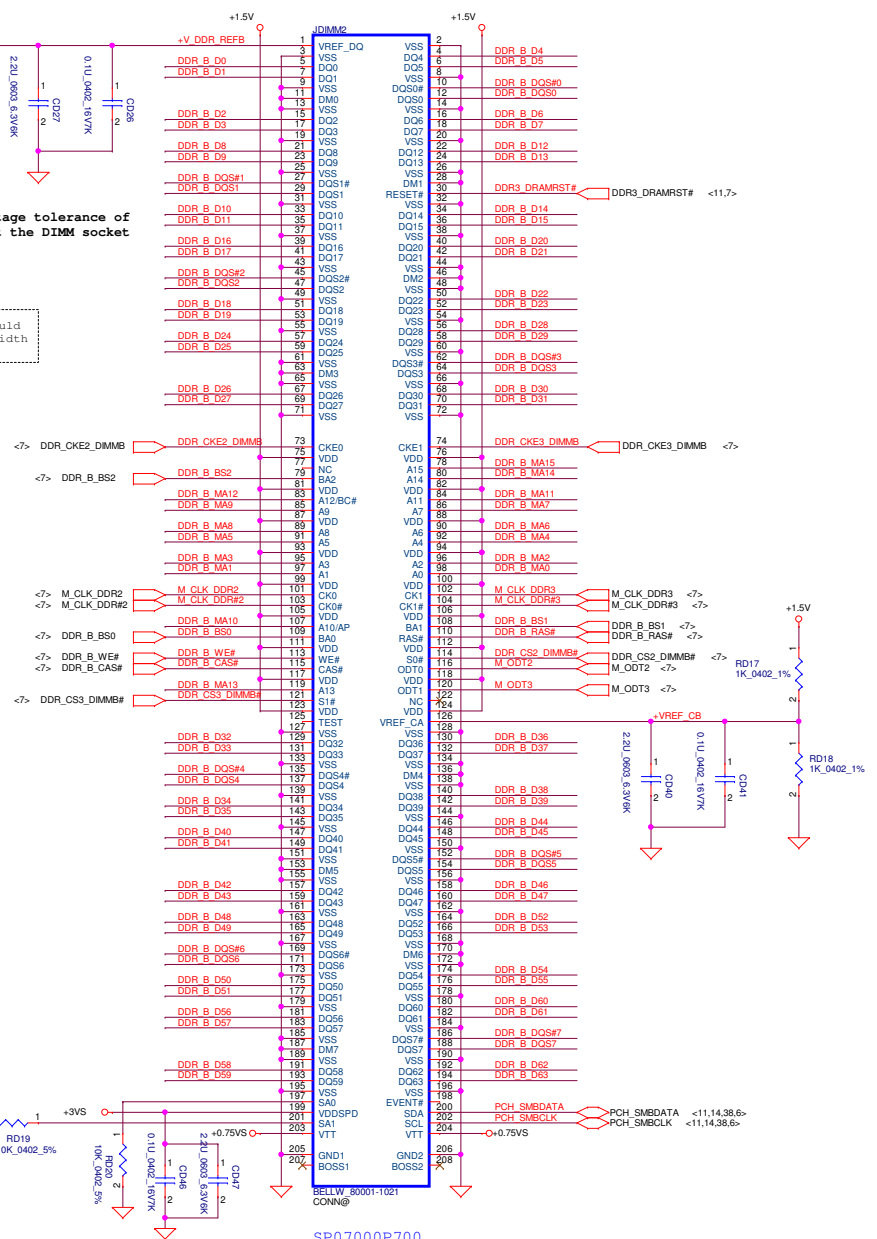
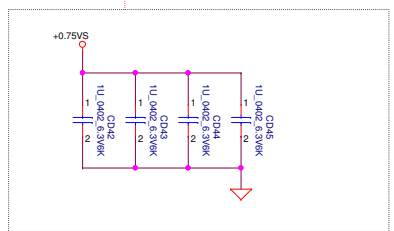


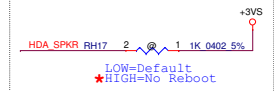
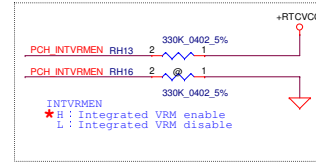
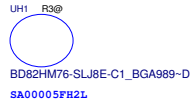
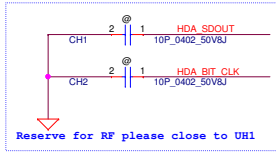
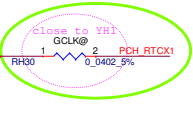
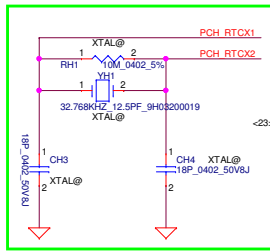
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMMB

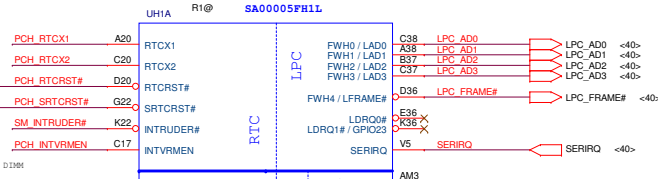
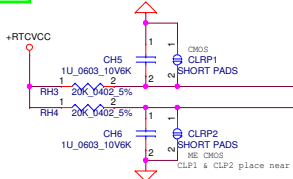


Layout Note:
Place near JDIMMB.203,204

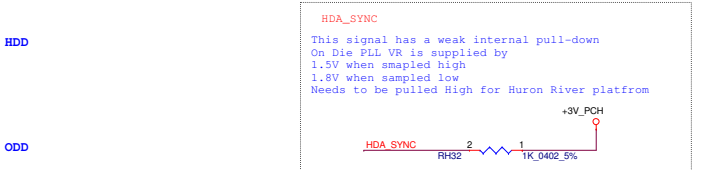
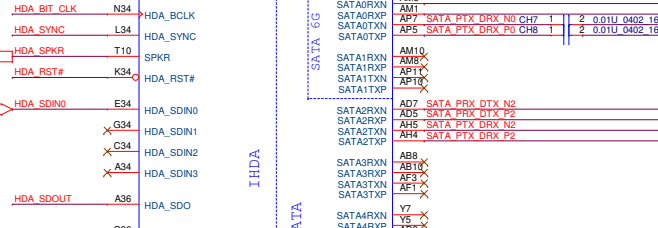
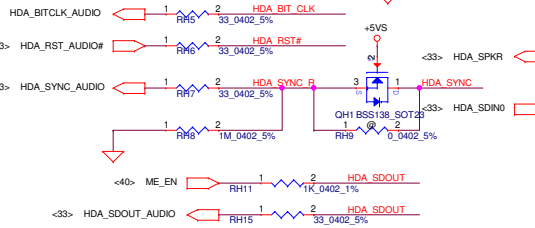
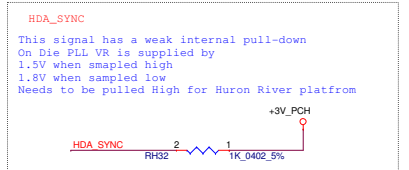
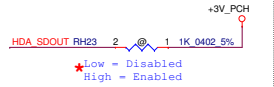




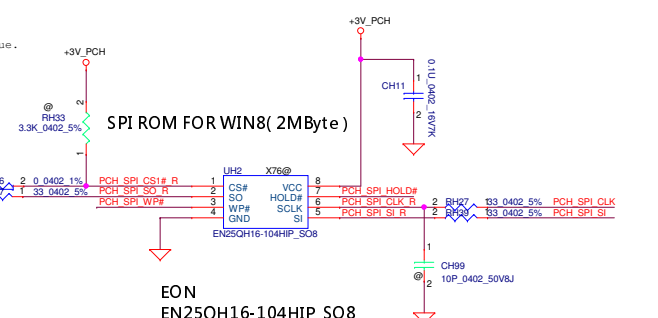
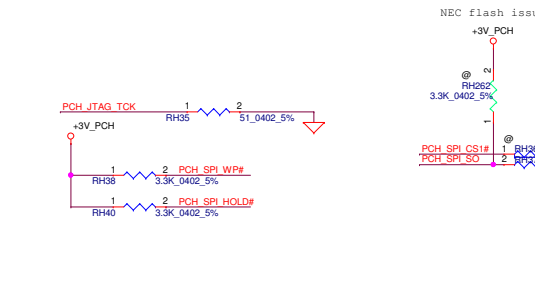
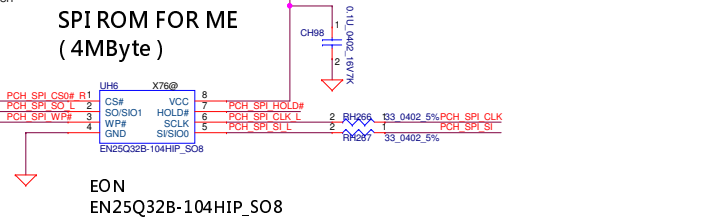
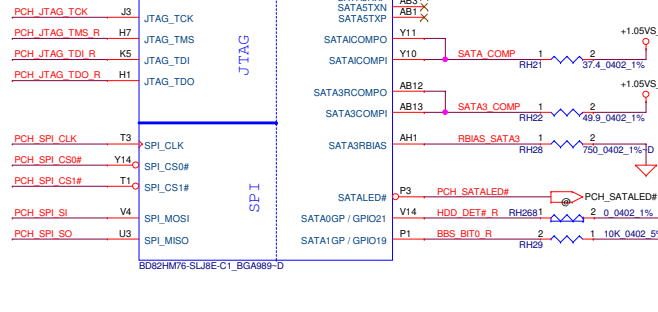
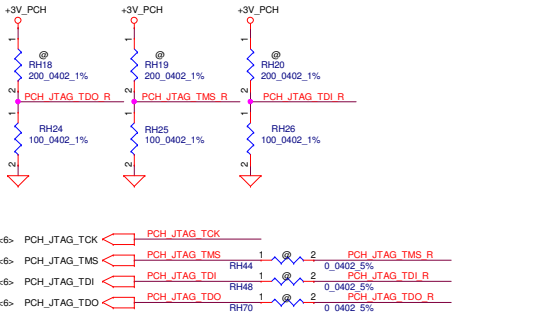
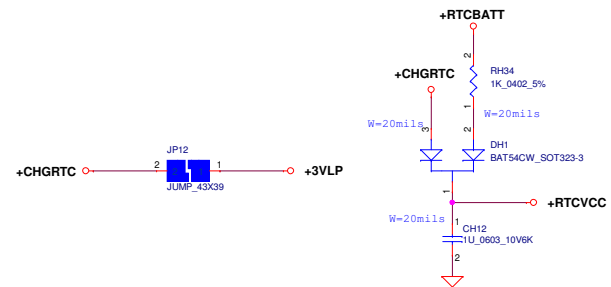
keep away hot spot



HDA_SDO
ME debug mode, this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

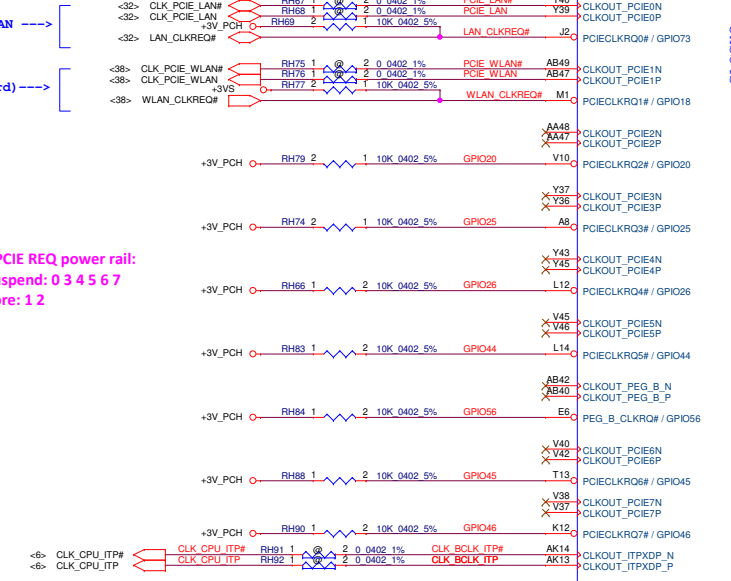
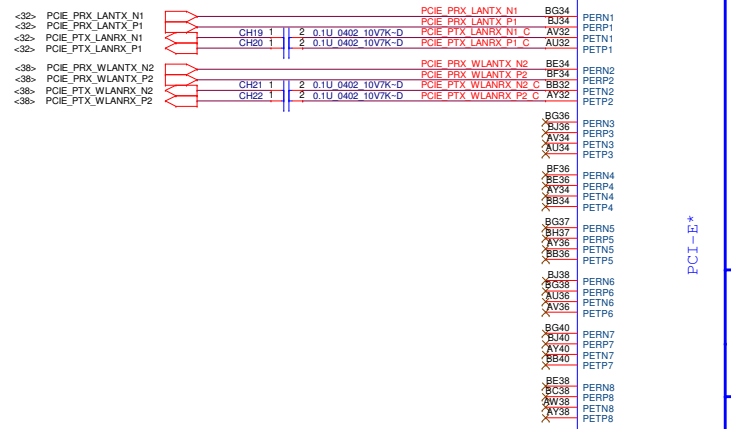


RTC Battery

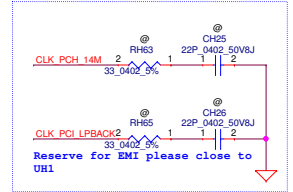
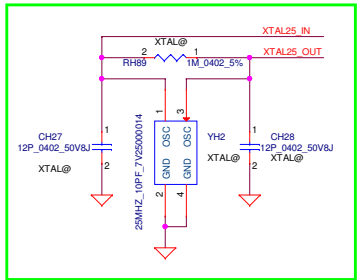


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Document Number	LA-9101P		Rev	04	
Date:	Wednesday, August 28, 2012	Sheet	13	of 57	

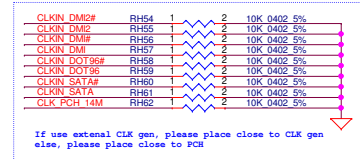
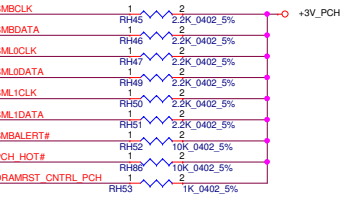
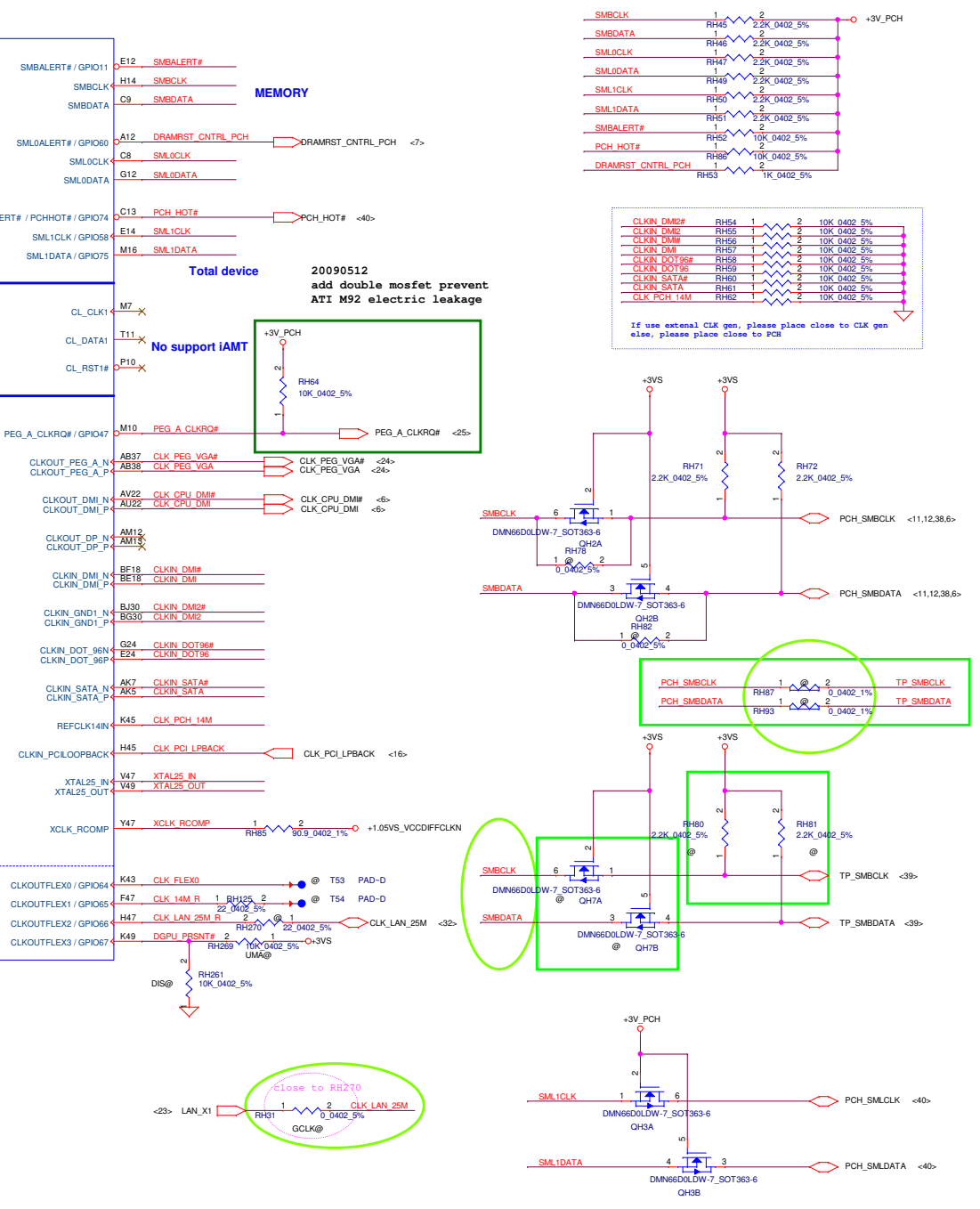
10/100 LAN --->
 WLAN (Mini Card) --->



*PCIE REQ power rail:
 suspend: 0 3 4 5 6 7
 core: 1 2

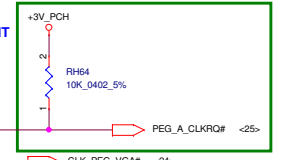


FLEX CLOCKS

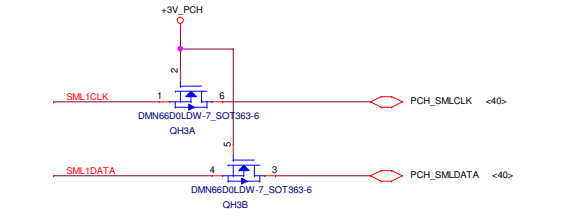
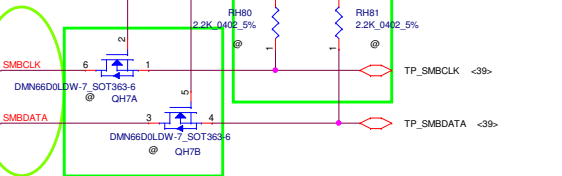
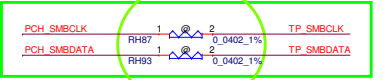
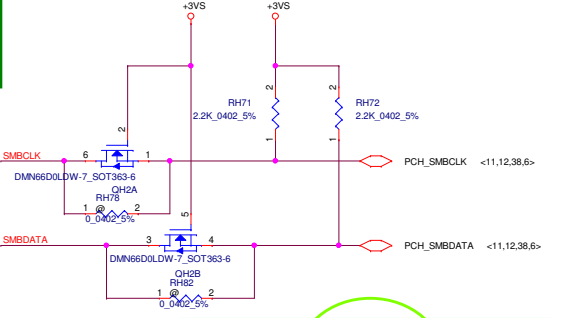


If use external clk gen, please place close to CLK gen else, please place close to PCH

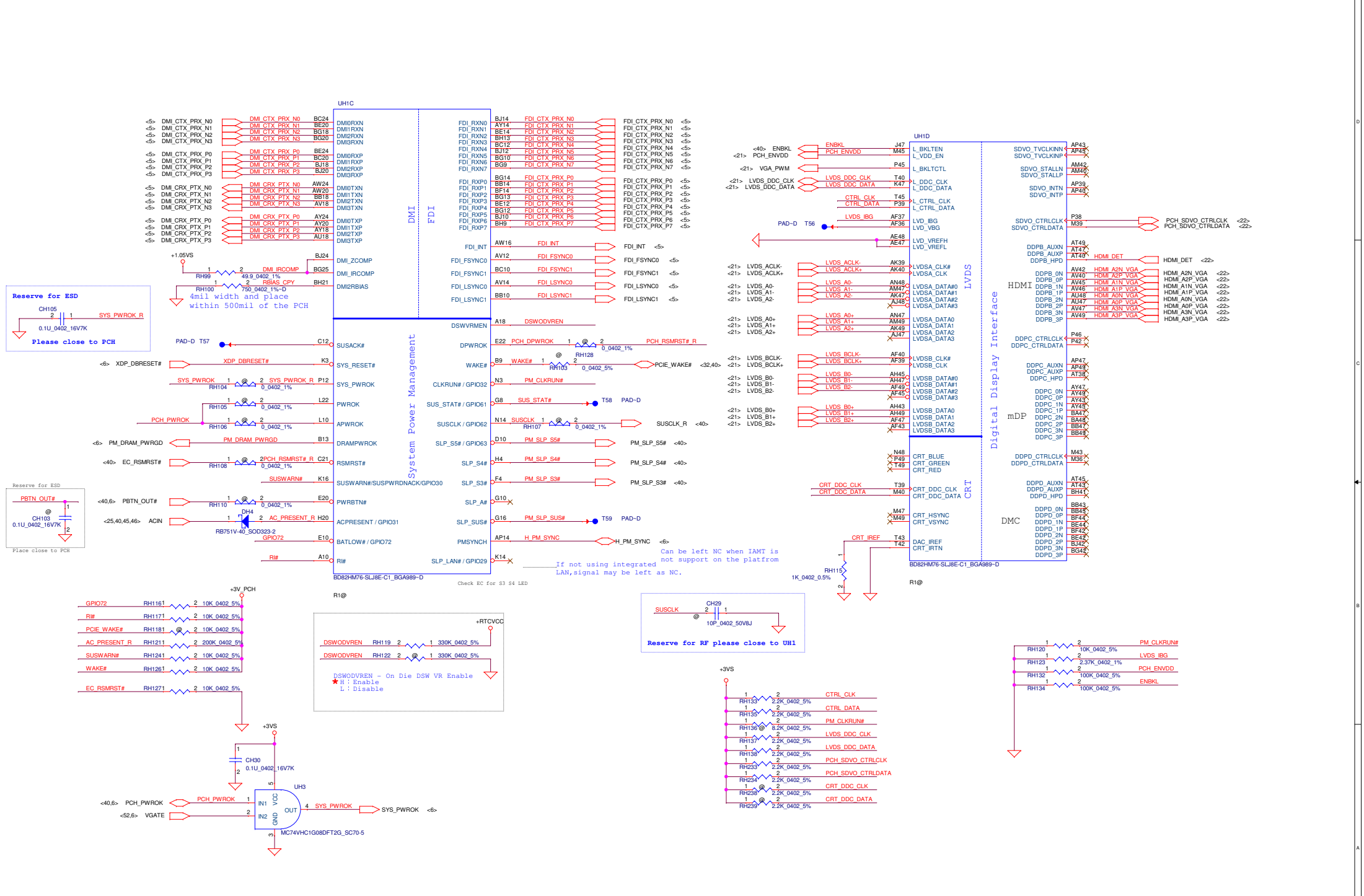
Total device 20090512
 add double mosfet prevent ATI M92 electric leakage



No support iAMT



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Document Number	LA-9101P		Rev	04	
Date	Wednesday, August 28, 2012	Sheet	14	of 57	



Reserve for ESD
 CH105
 0.1u_0402_16V7K
 Please close to PCH

Reserve for ESD
 CH103
 0.1u_0402_16V7K
 Place close to PCH

DSWODVREN RH119 2 330K 0402 5%
 DSWODVREN RH122 2 330K 0402 5%
 DSWODVREN - On Die DSW VR Enable
 * H: Enable
 L: Disable

SUSCLK CH29 10P_0402_50V8J
 Reserve for RF please close to UH1

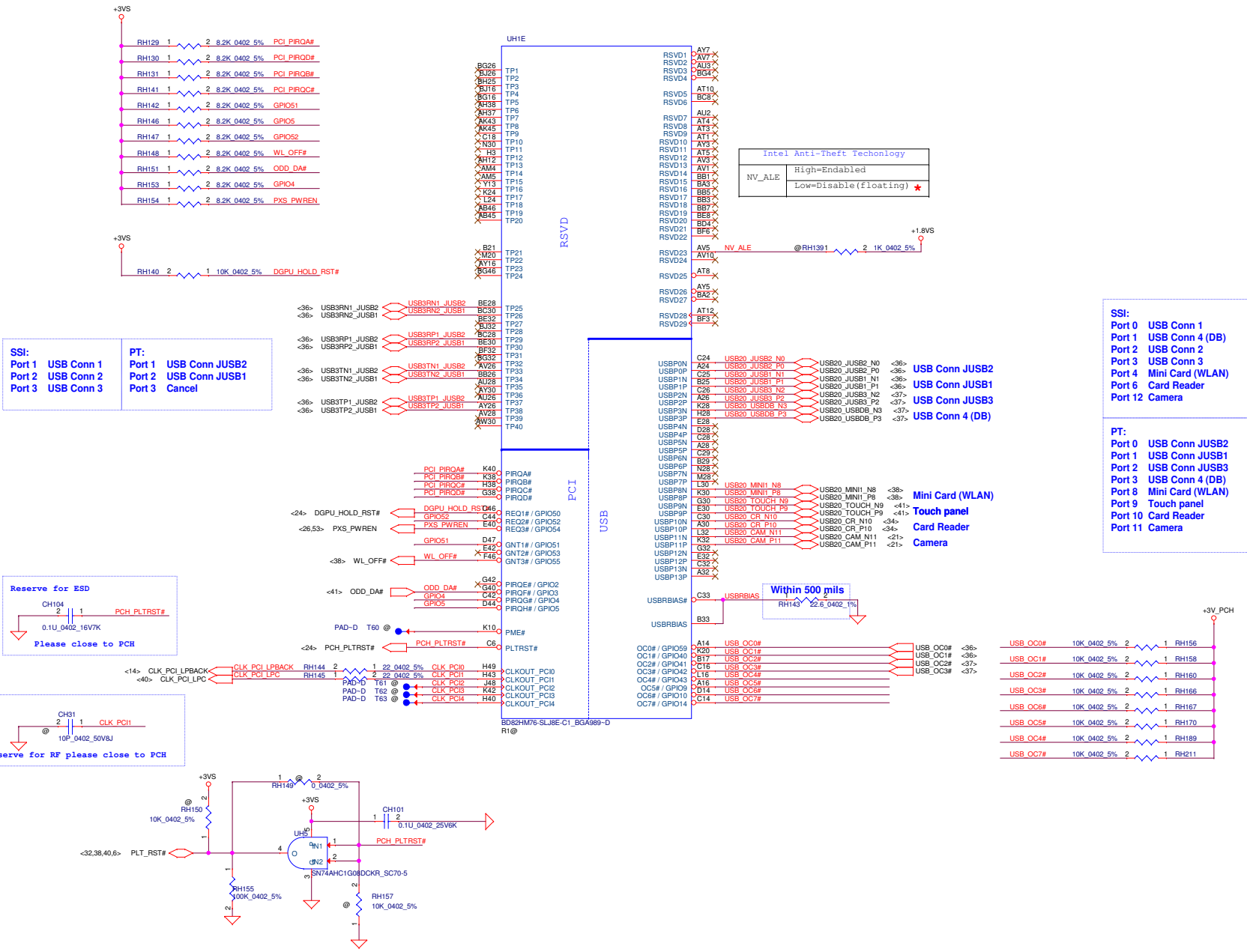
+3VS
 RH133 2.2K_0402 5% CTRL_CLK
 RH135 2.2K_0402 5% CTRL_DATA
 RH136 2.2K_0402 5% PM_CLKRUN#
 RH137 2.2K_0402 5% LVDS_DDC_CLK
 RH138 2.2K_0402 5% LVDS_DDC_DATA
 RH253 2.2K_0402 5% PCH_SDVO_CTRLCLK
 RH254 2.2K_0402 5% PCH_SDVO_CTRLDATA
 RH258 2.2K_0402 5% CRT_DDC_CLK
 RH259 2.2K_0402 5% CRT_DDC_DATA

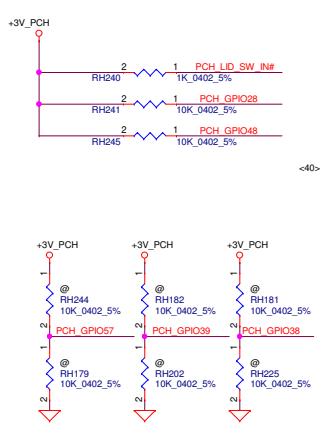
RH120 10K_0402 5% PM_CLKRUN#
 RH123 2.37K_0402 1% LVDS_IBG
 RH132 100K_0402 5% PCH_ENVDD
 RH134 100K_0402 5% ENBK_L

+3V PCH
 RH1161 2 10K 0402 5% GPIO72
 RH1171 2 10K 0402 5% R#
 RH1181 2 10K 0402 5% PCIE_WAKE#
 RH1211 2 200K 0402 5% AC_PRESENT_R
 RH1241 2 10K 0402 5% SUSWARN#
 RH1261 2 10K 0402 5% WAKE#
 RH1271 2 10K 0402 5% EC_RSMRST#

+3VS
 CH30 0.1u_0402_16V7K
 UH3
 IN1
 IN2
 OUT
 4
 SYS_PWROK
 SYS_PWROK <->
 MC74VHC1G08DFT2G_SC70-5

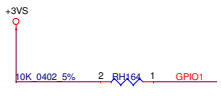
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (3/8) DMI/FDI/PM/GFX/XP	
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Document Number	LA-9101P		Rev	04	
Date	Wednesday, August 28, 2012	Sheet	15	of 57	





System ID

	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

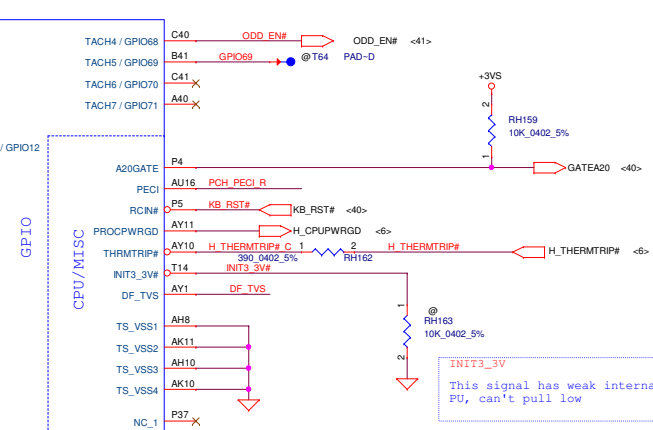
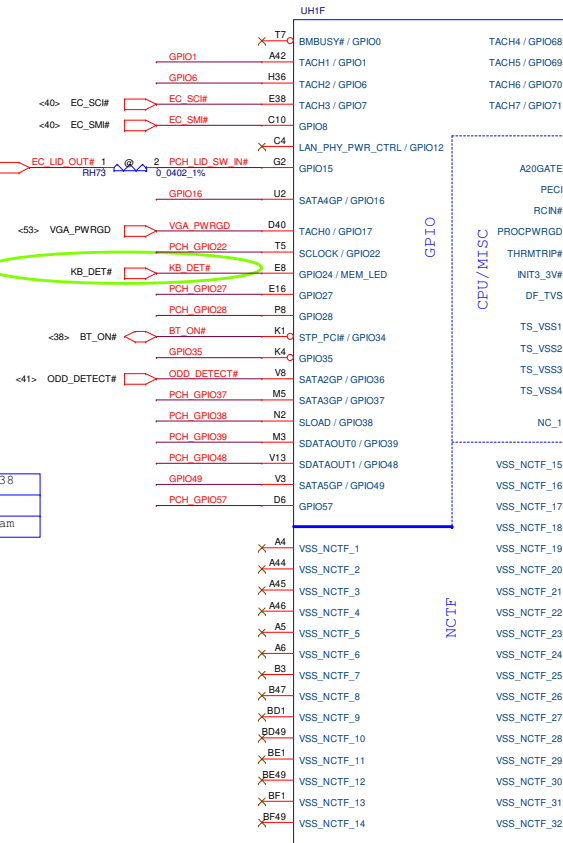
- H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE

- LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

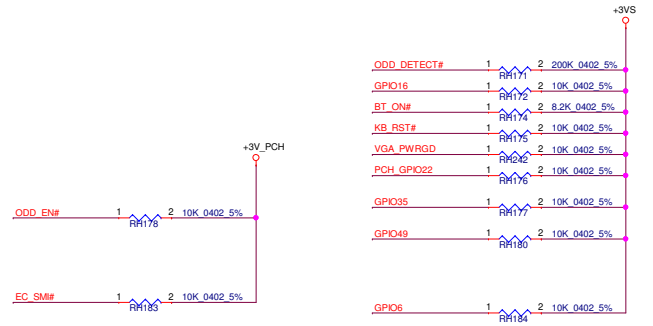


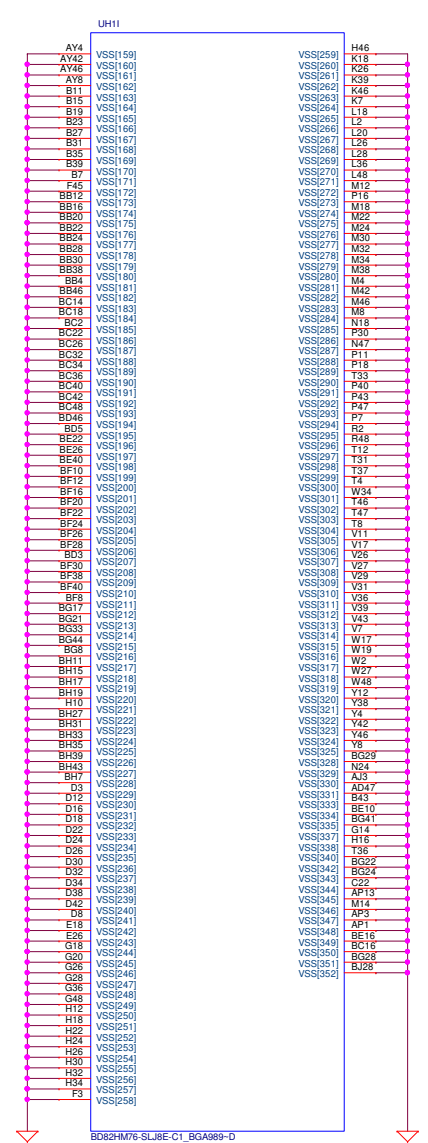
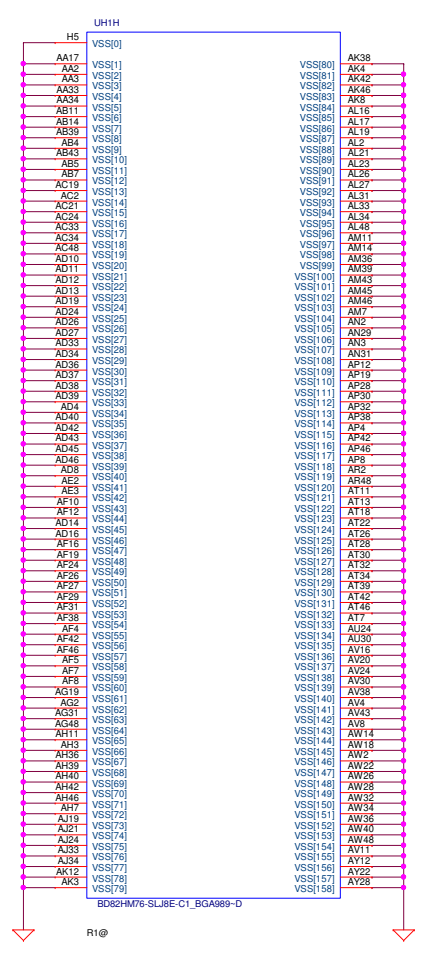
Due to remove VCCDFERM jumper (PJ66), need to change the power rail to +1.8V_RUN for D12" only

PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU and NVRAM CONNECTOR)

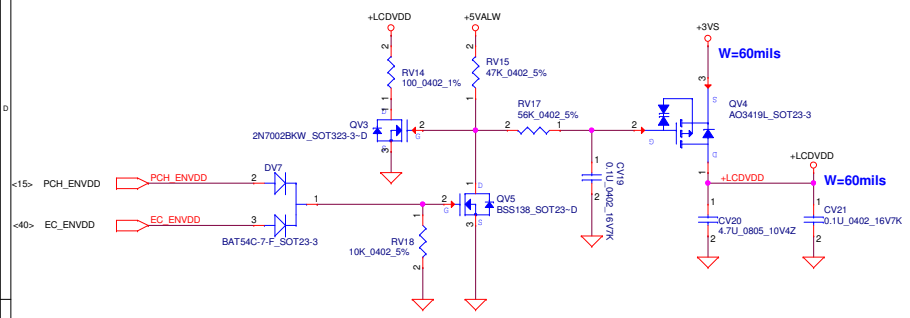
RH149 need to close to CPU

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

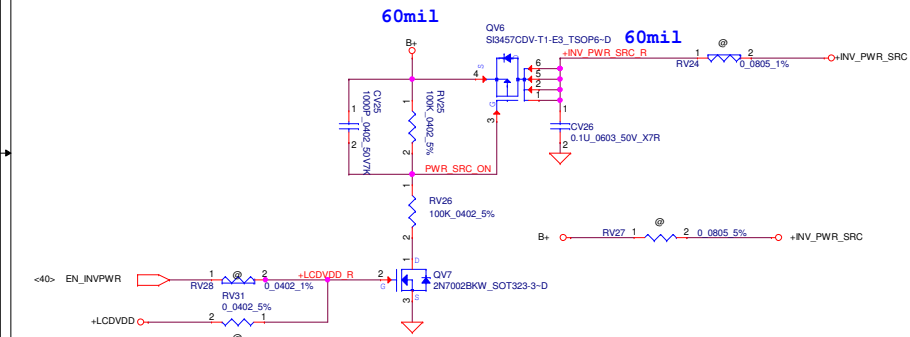




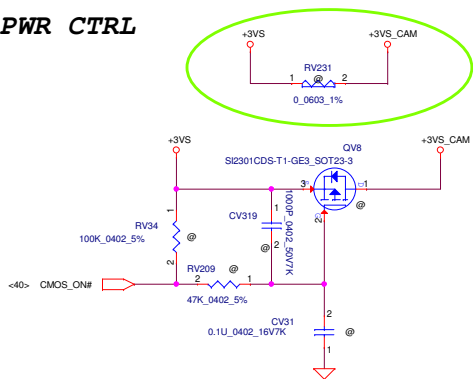
LCD PWR CTRL



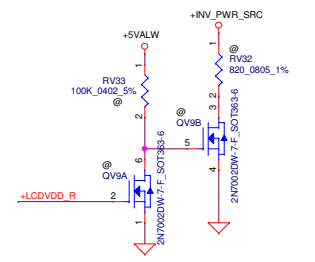
LCD backlight PWR CTRL



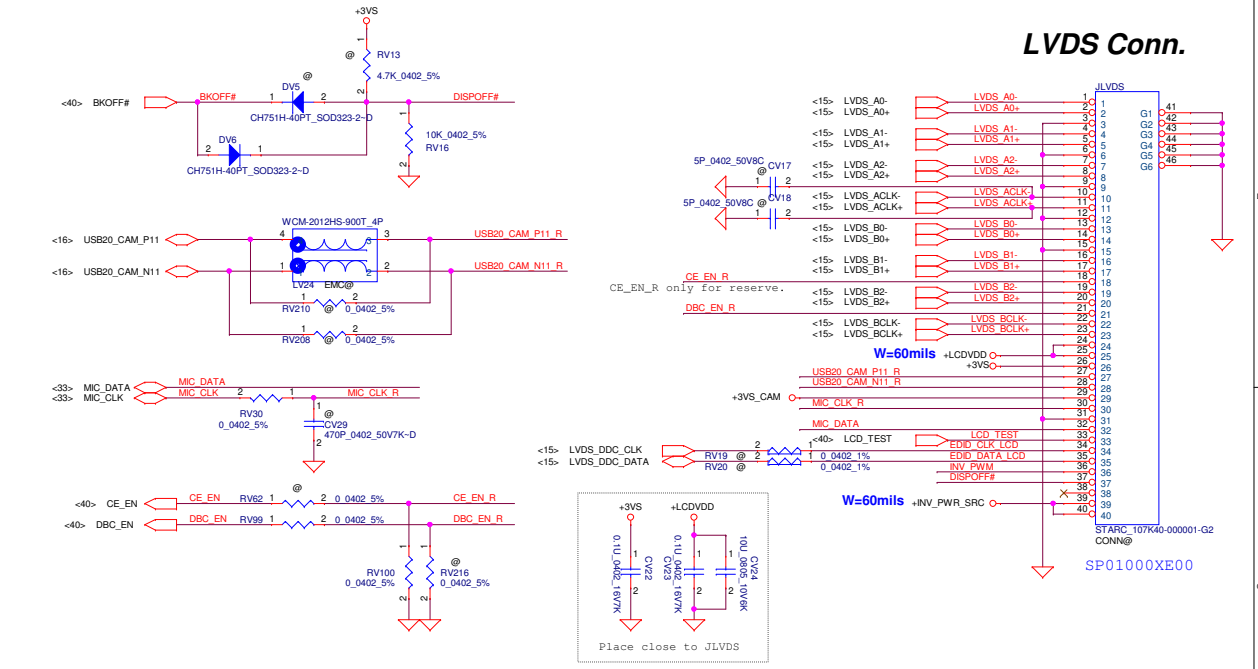
Webcam PWR CTRL



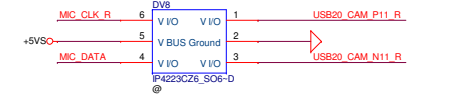
* Reserved for LCD sequence tuning



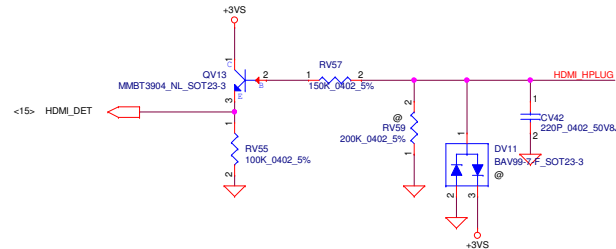
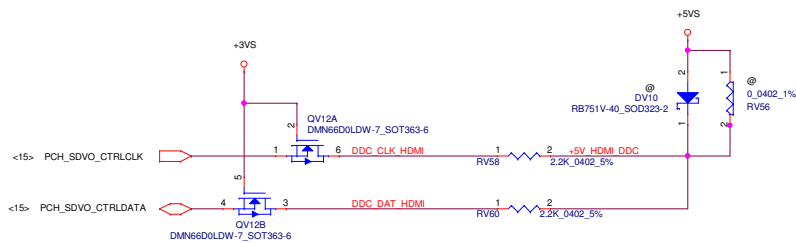
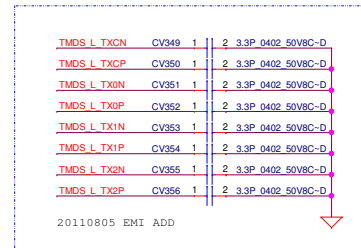
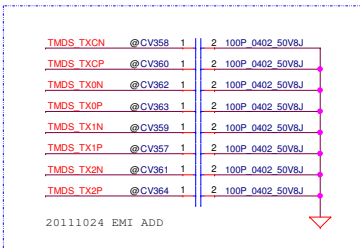
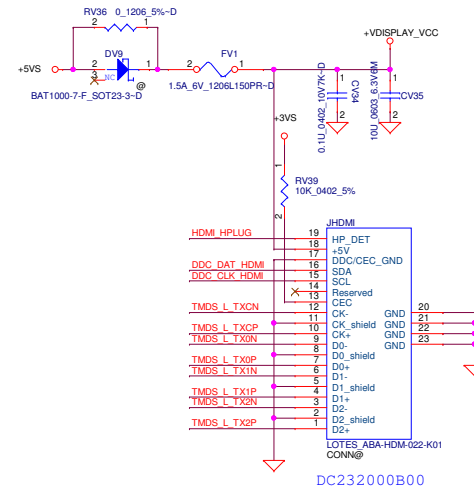
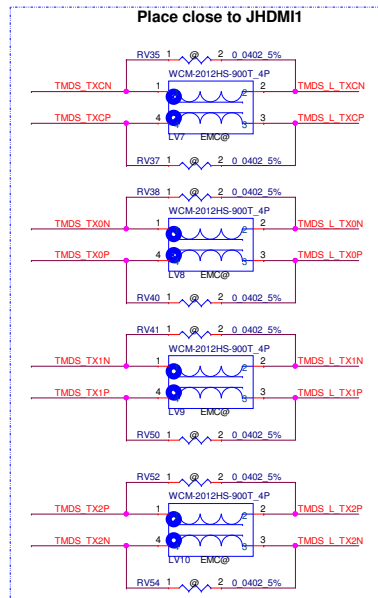
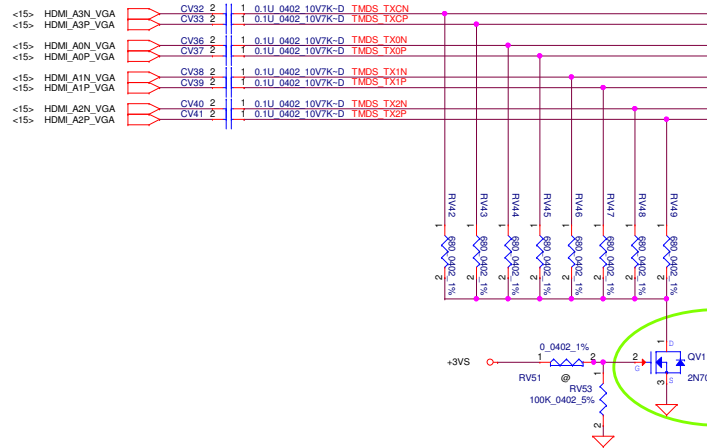
LVDS Conn.



*** Reserved for EMI/ESD/RF need to close to JLVDS**

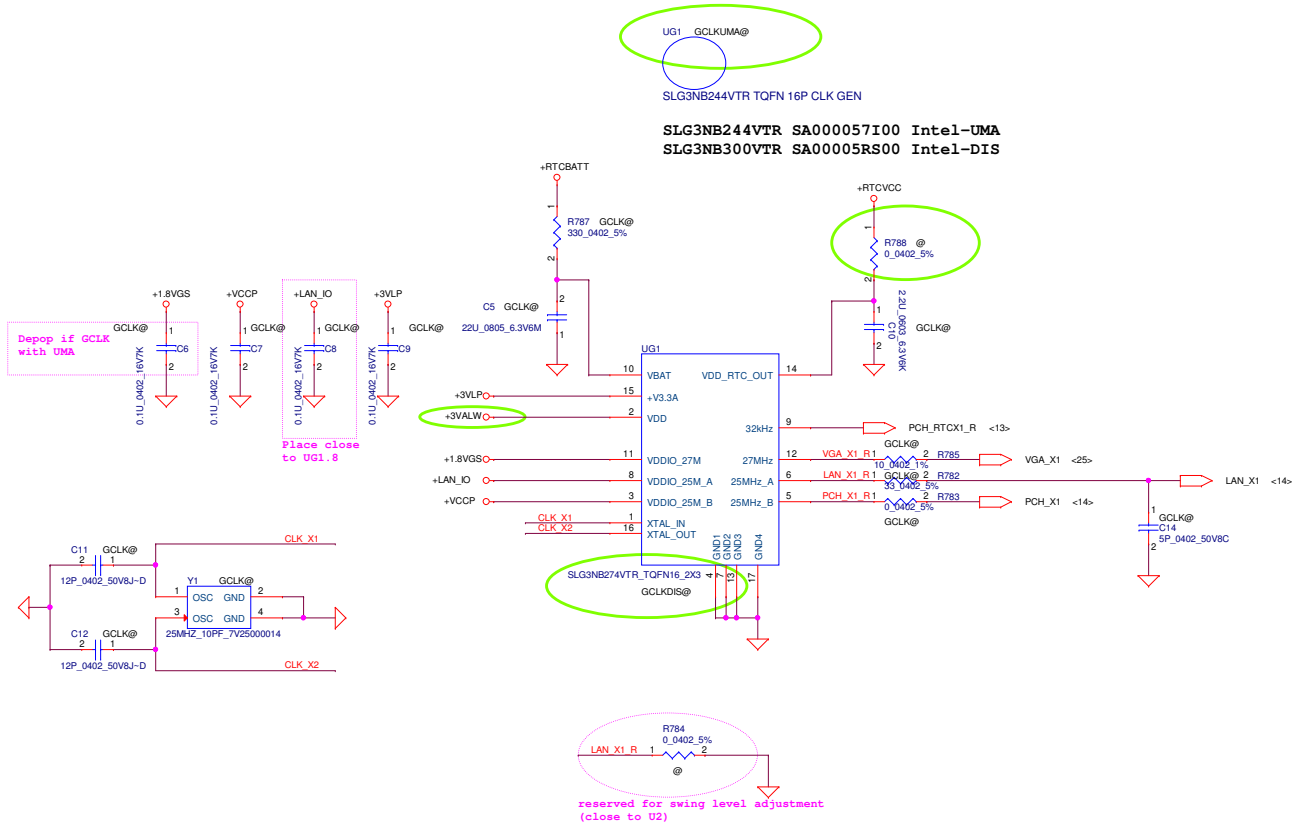


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Date: Wednesday, August 28, 2012				Sheet 21 of 57



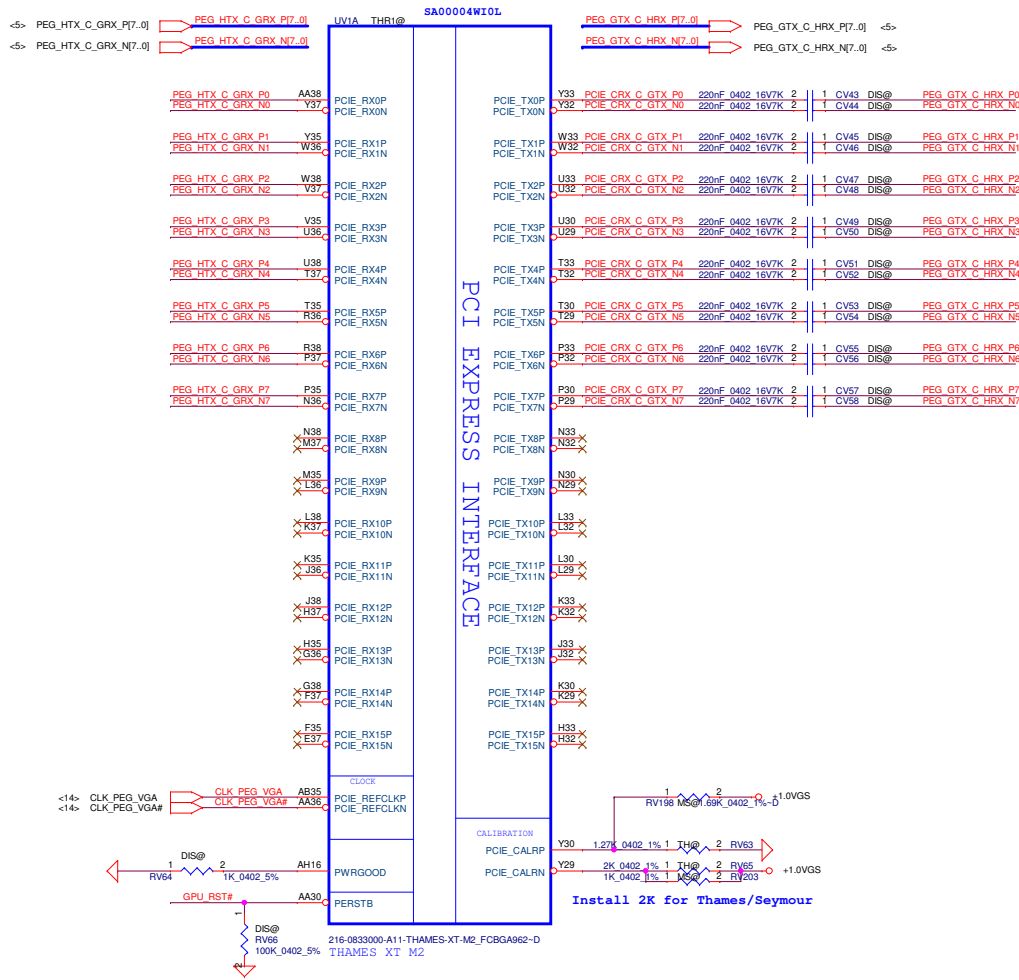
46@	ROYALTY HDMI W/LOGO
Part Number	Description
8000000023M	HDMI W/LogoR000000023M

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Date: Wednesday, August 28, 2012				Sheet	22 of 57

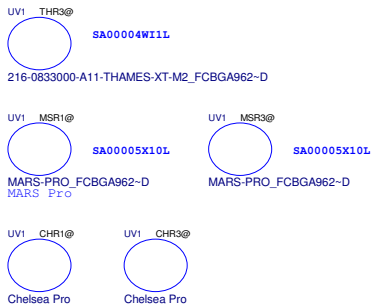
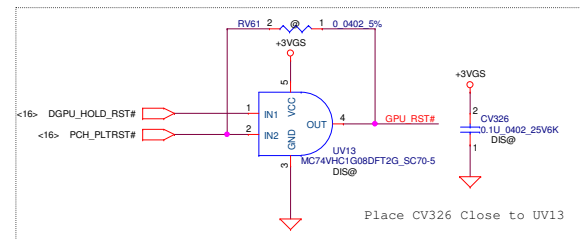
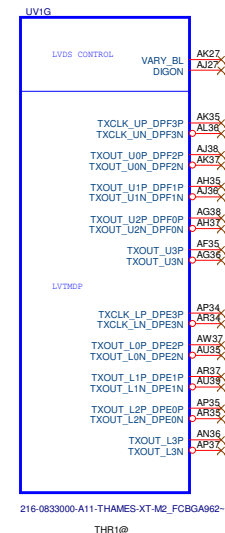


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Date: Wednesday, August 23, 2012				Sheet 23 of 57

GFX PCIE LANE REVERSAL



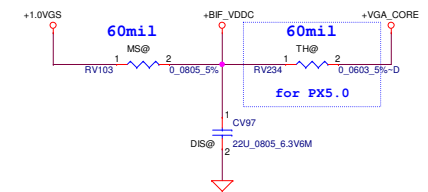
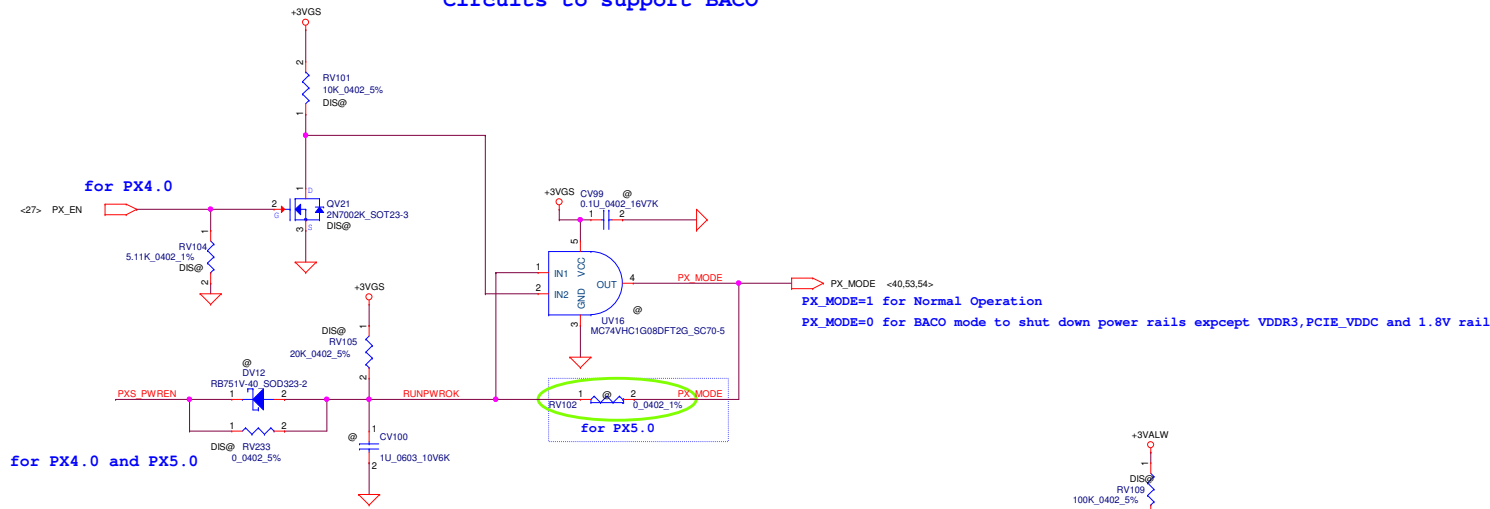
LVDS Interface



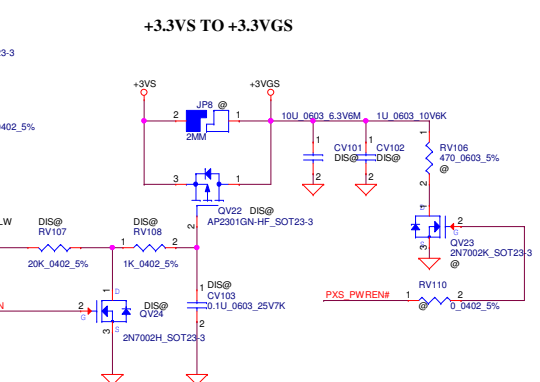
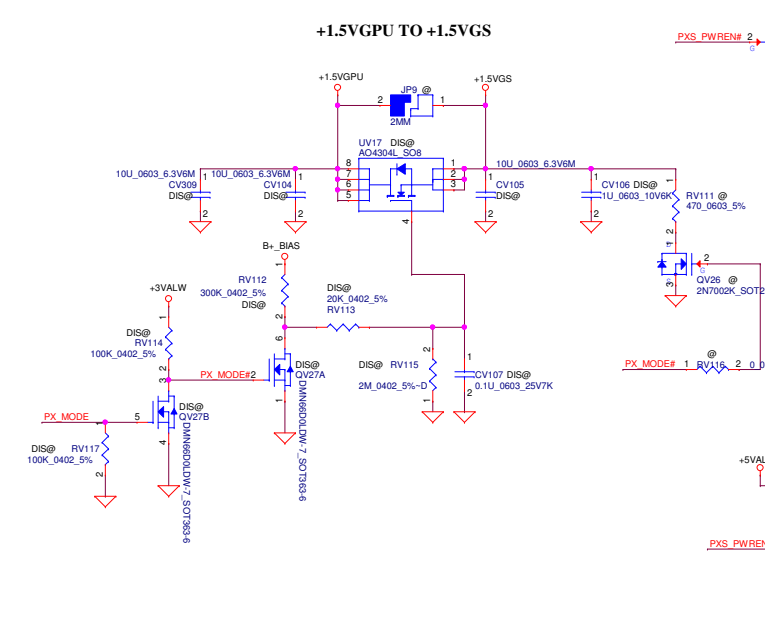
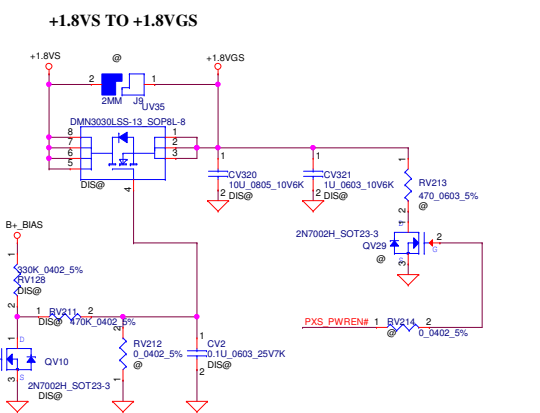
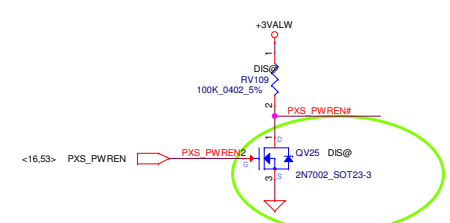
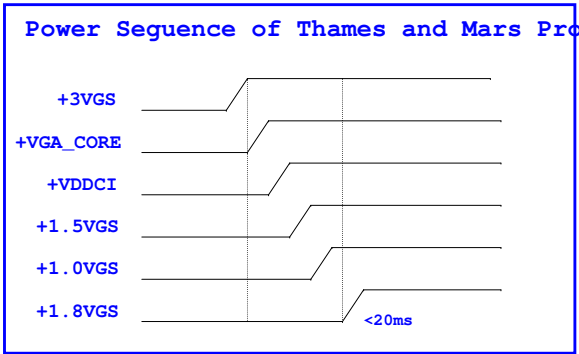
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		216-0833000-A11-THAMES-XT-M2_FCBGA962-D	
2012/08/22		2013/08/31		ATI ThamesXT M2 PCIe/LVDS	
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				Date: Wednesday, August 28, 2012 Sheet 24 of 57	

55mA@1.0V, in BACO mode

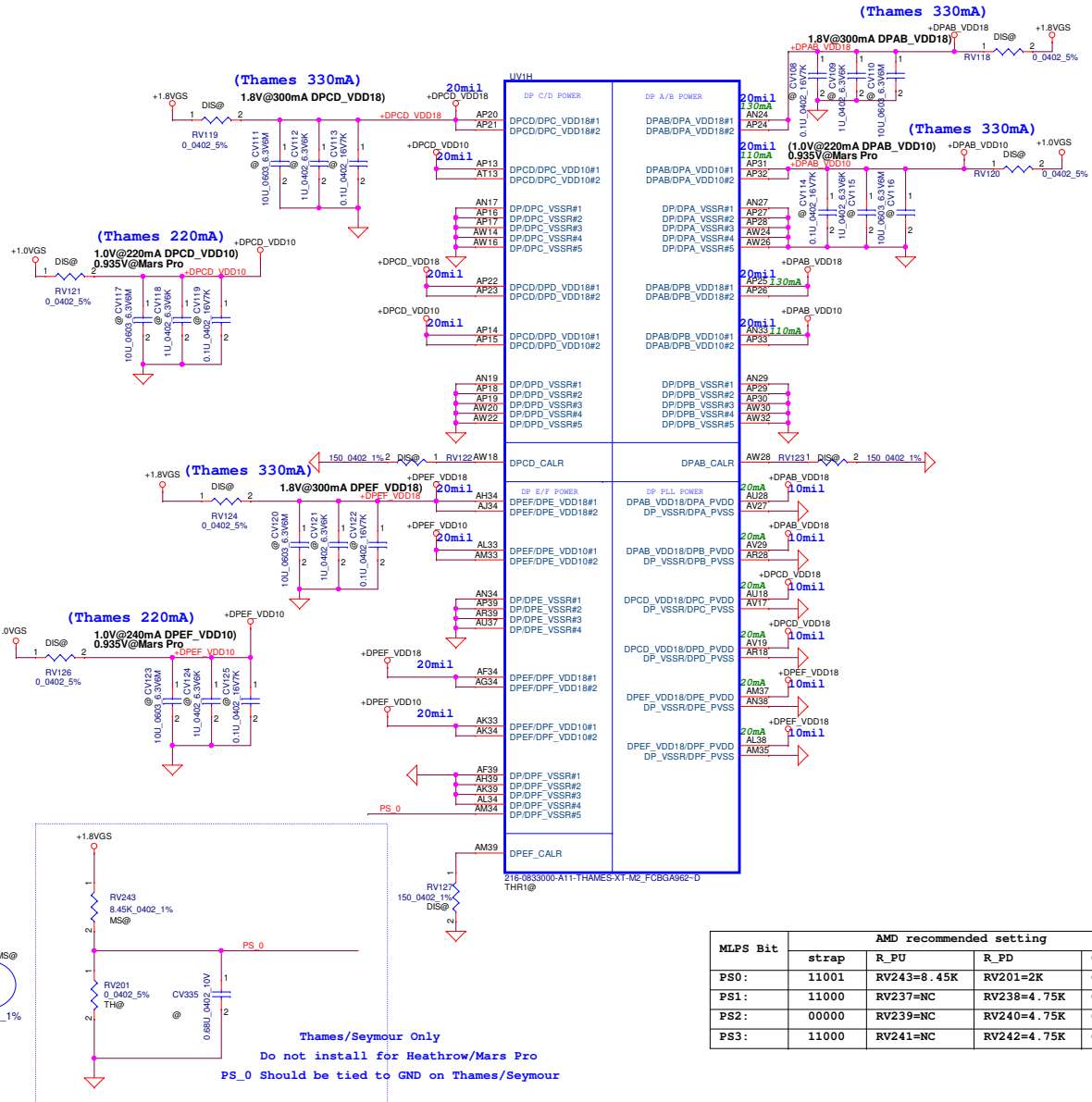
Circuits to support BACO



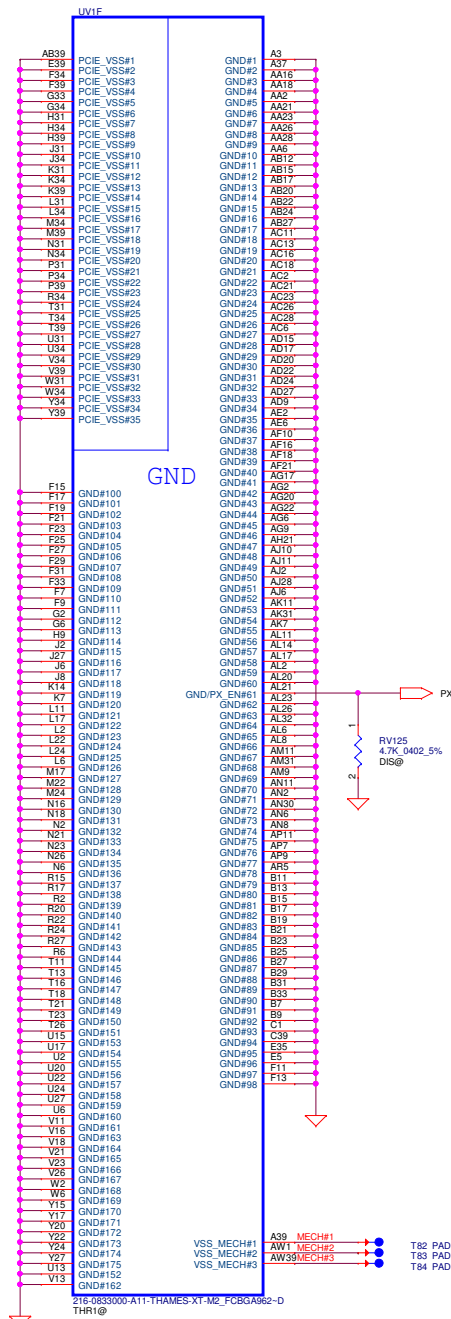
Note:
 PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

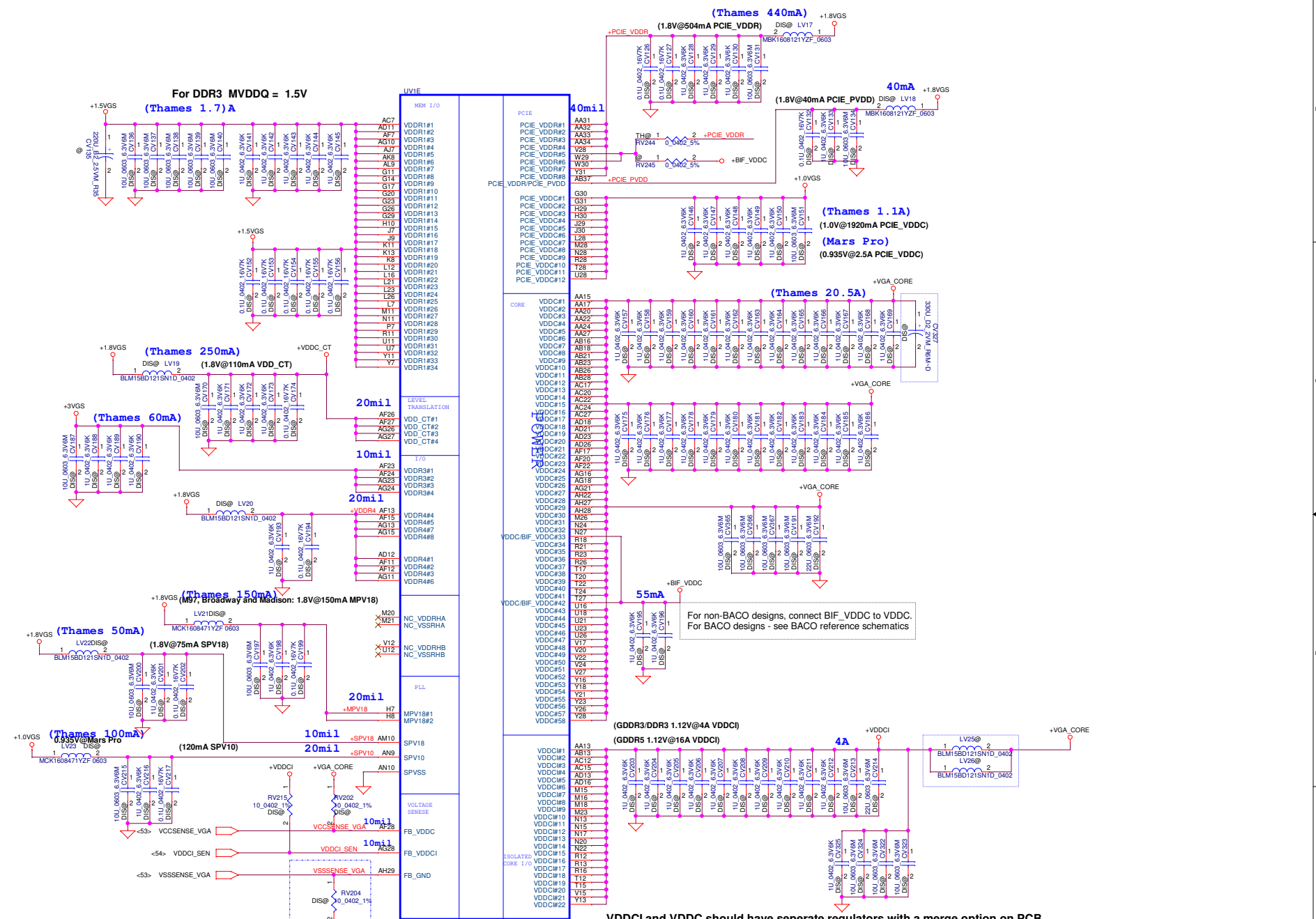


Security Classification	Compal Secret Data		Title	
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				LA-9101P
Date: Wednesday, August 28, 2012				Sheet 26 of 57



MLPS Bit	AMD recommended setting			
	strap	R_RU	R_FD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

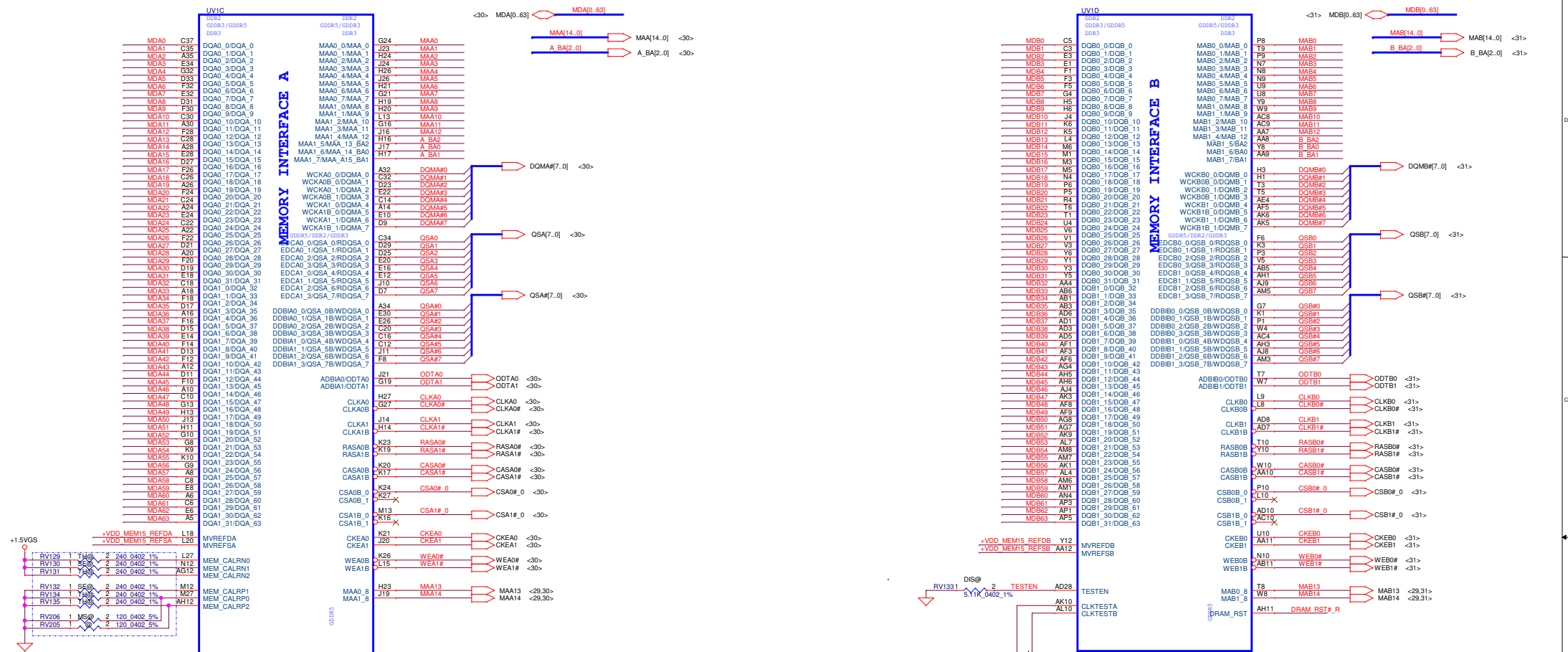




216-0833000-A11-1-THAMES-X1-M2_F0CBA962-D
THR1@

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

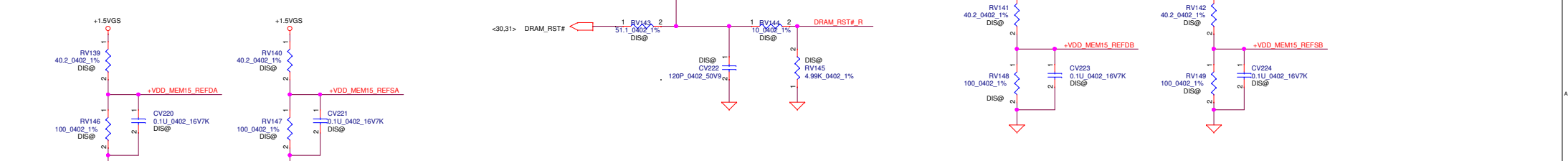
Security Classification	Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI ThamesXT M2_Power
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Document Number	LA-9101P			Rev 0.4
Date:	Wednesday, August 28, 2012	Sheet	28	of 57



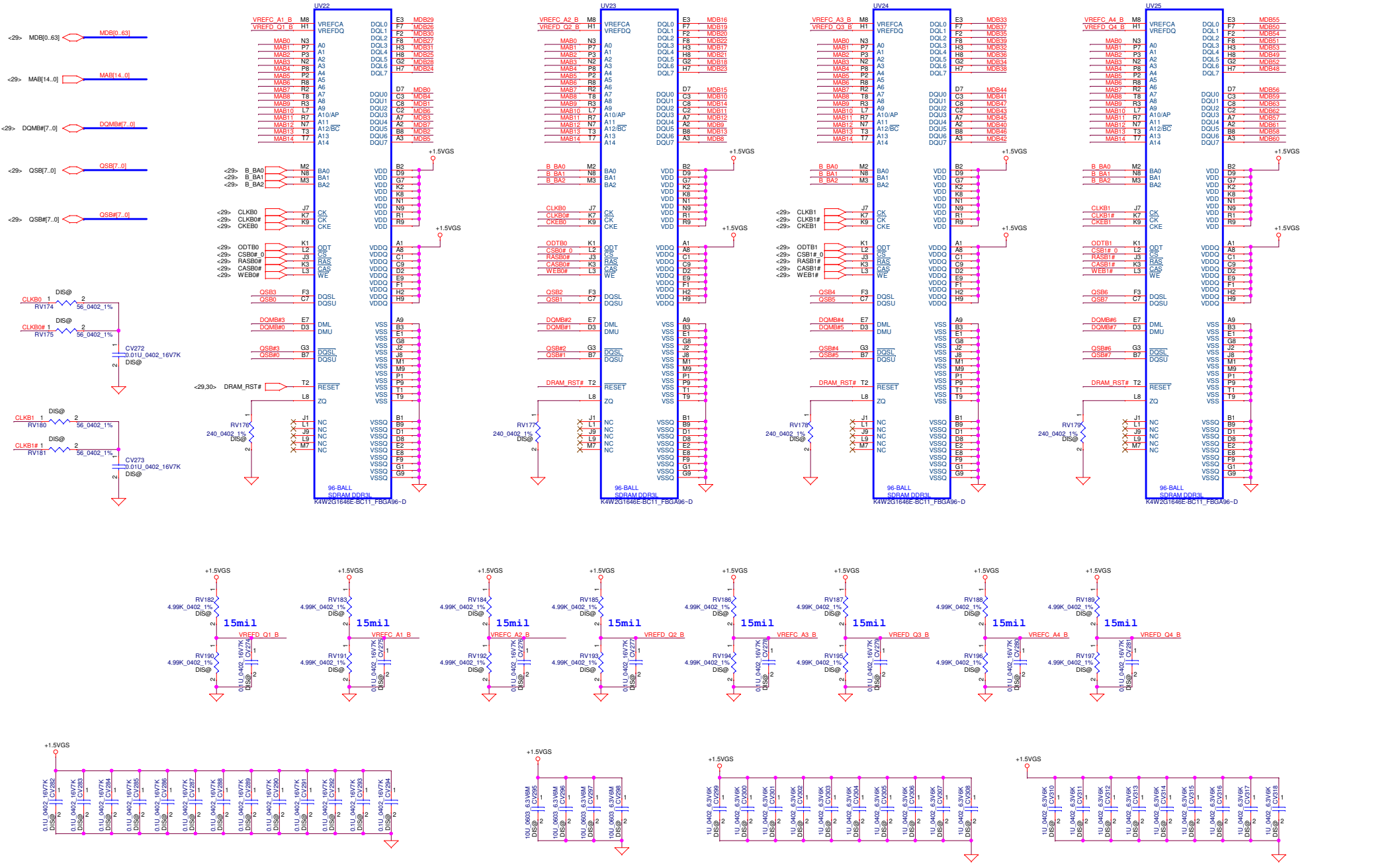
Co-lay Thames/Seymour/Mars Pro

	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

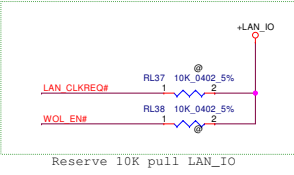
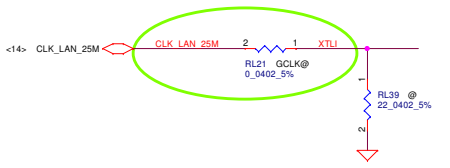
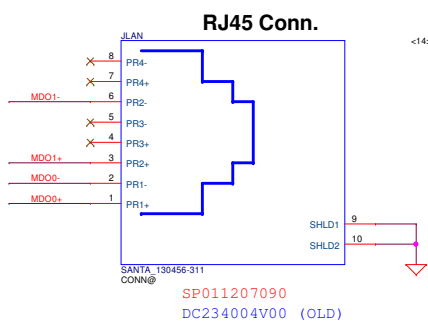
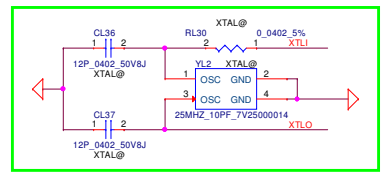
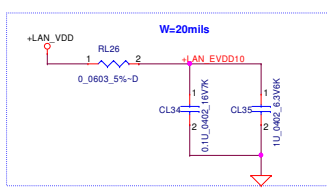
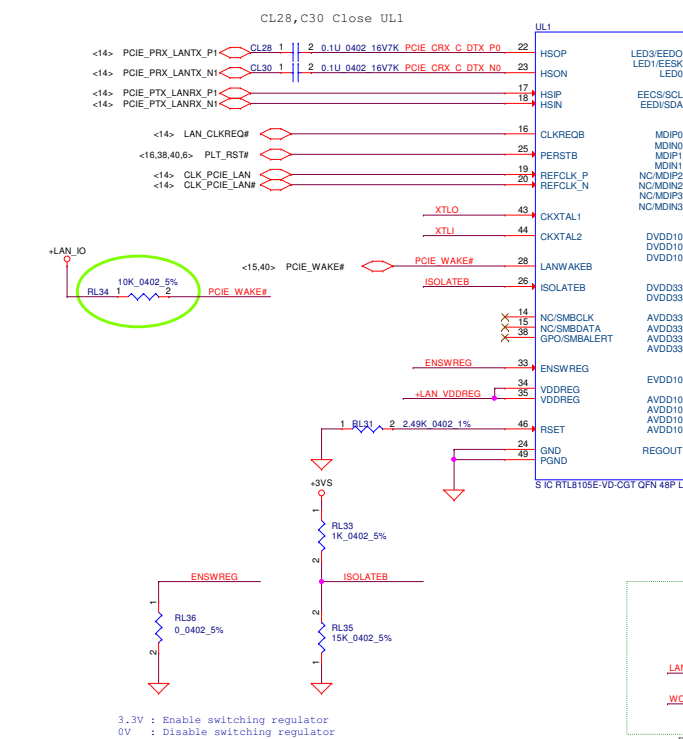
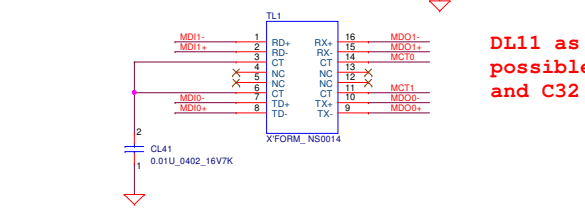
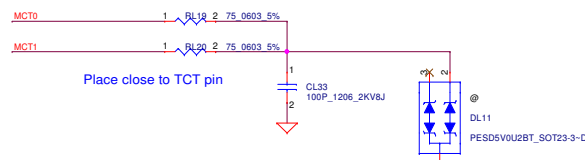
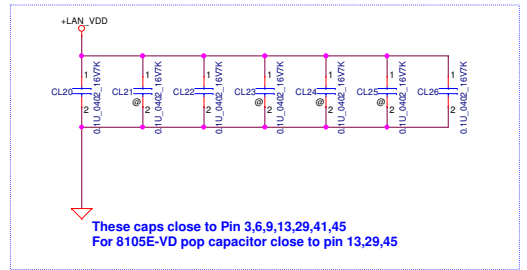
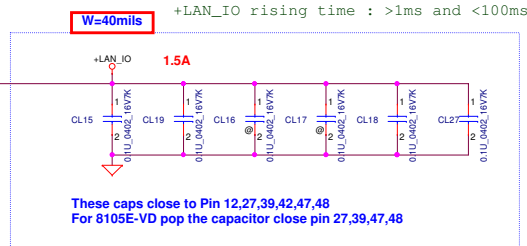
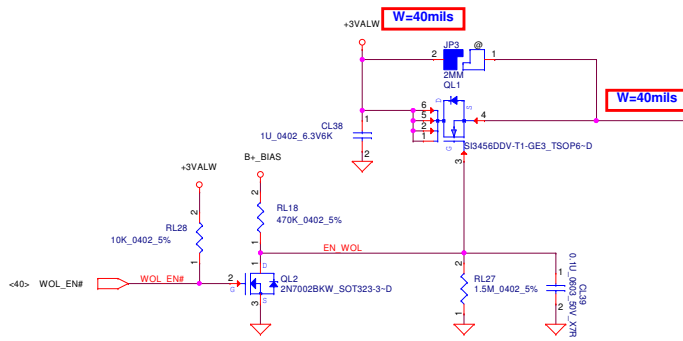
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



CHANNEL B : 256MB/512MB DDR3

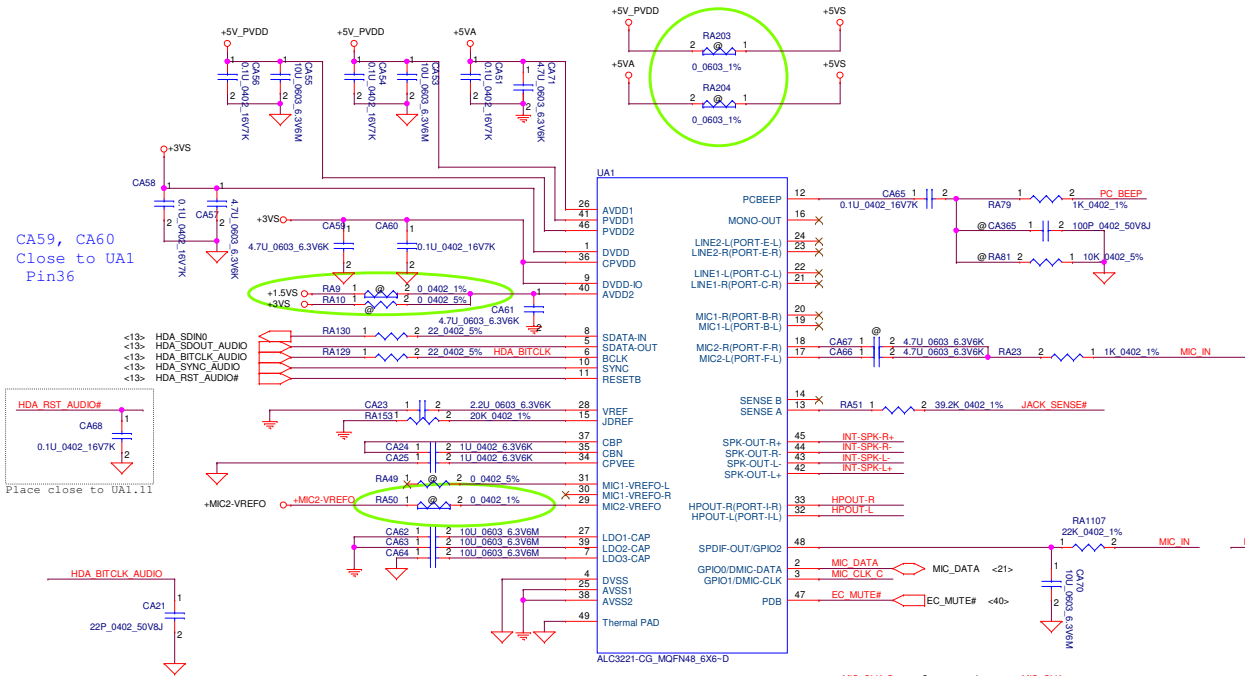


Security Classification		Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI ThamesXT M2 VRAM B	
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Size	Document Number	LA-9101P		Rev	0.4
Date:	Wednesday, August 23, 2012	Sheet	31	of 57	

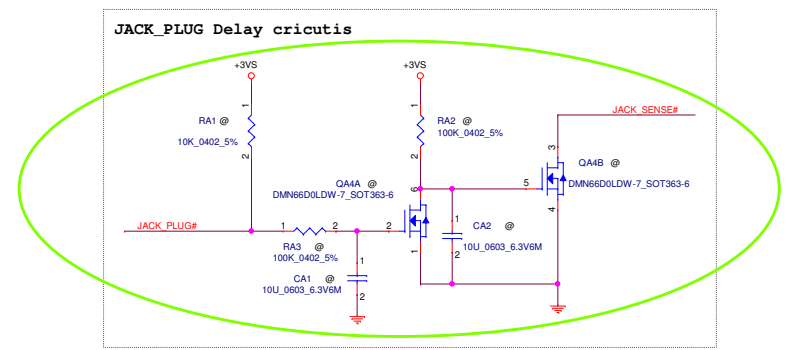
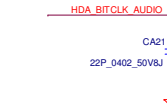
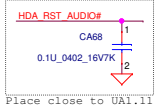


10/100 : 100@ (LDO mode used)

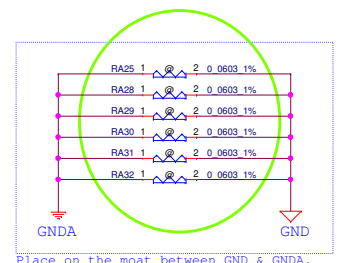
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Issued Date	2012/08/22	Deciphered Date	2013/08/31
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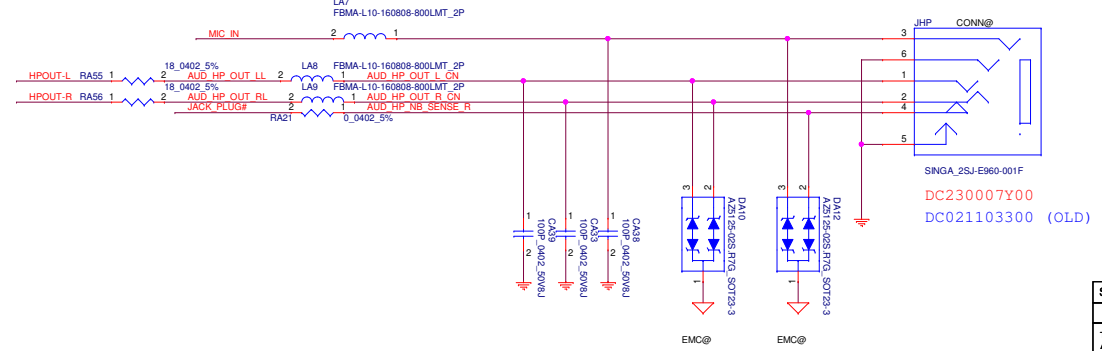
CA59, CA60
Close to U1
Pin36



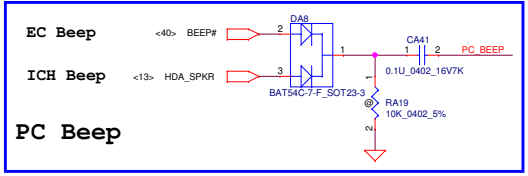
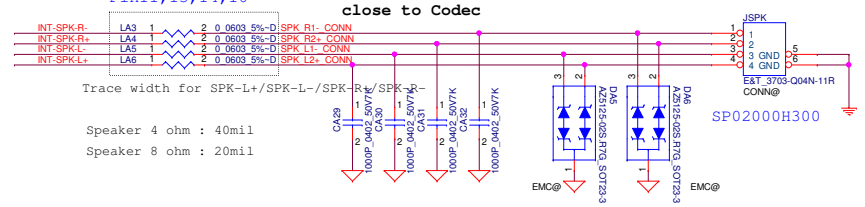
Reserve for cancel Delay circuit



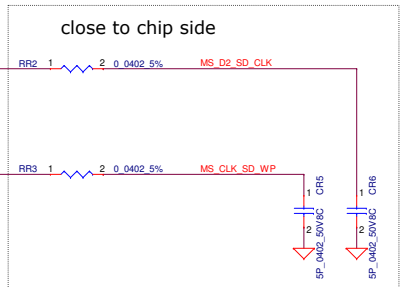
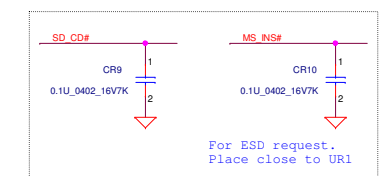
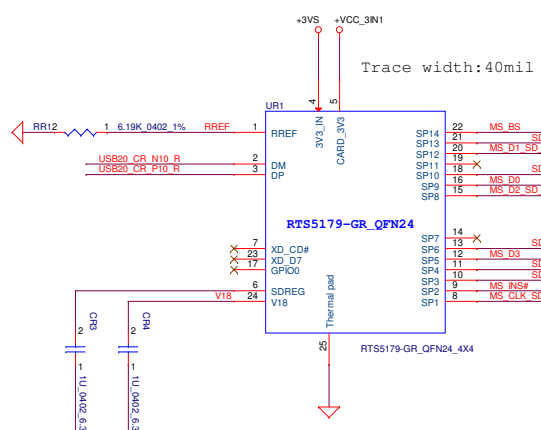
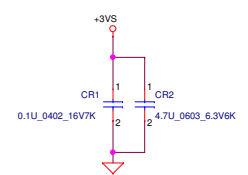
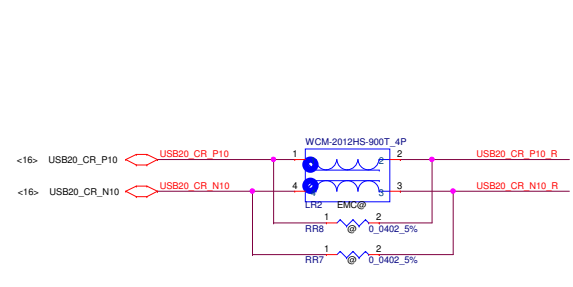
iPhone type Combo Jack



Close to U1
Pin11,13,14,16

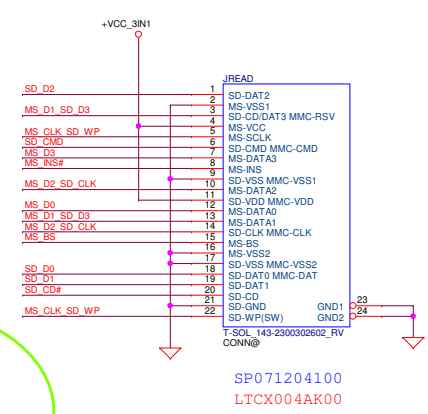
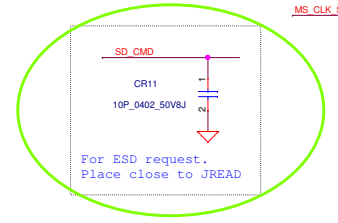
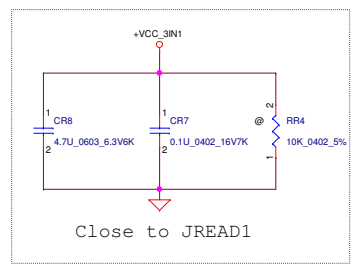


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Issued Date		Deciphered Date		Compal Electronics, Inc.	
2012/08/22		2013/08/31		Audio Codec ALC3221	
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Document Number				Rev	
LA-9101P				04	
Date		Sheet		of	
Wednesday, August 28, 2012		33		57	



拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

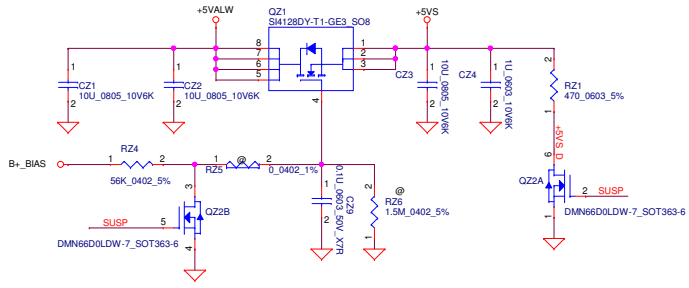
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



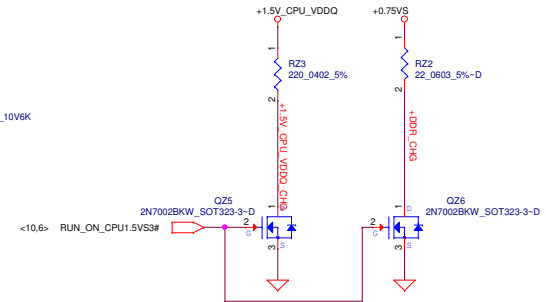
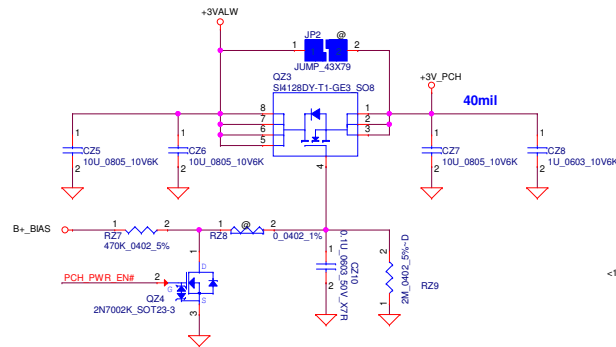
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LTCX004AK00

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Card Reader RTSS179		
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					LA-9101P	0.4
				Date:	Wednesday, August 28, 2012	Sheet 34 of 57

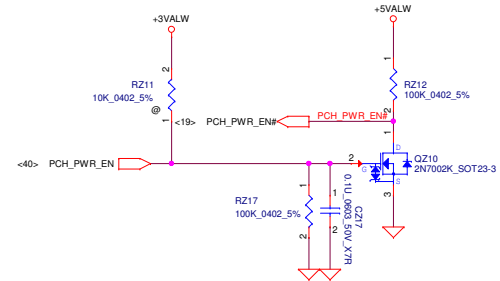
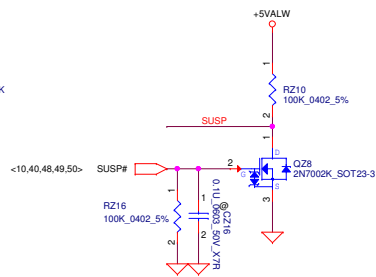
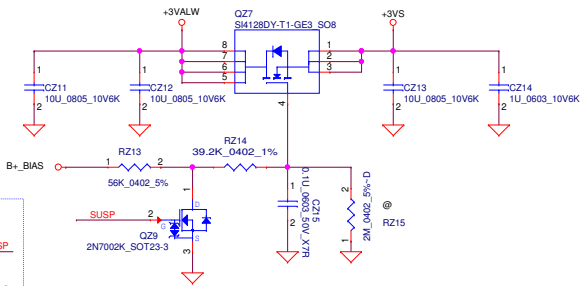
+5VALW to +5VS



+3VALW to +3V_PCH

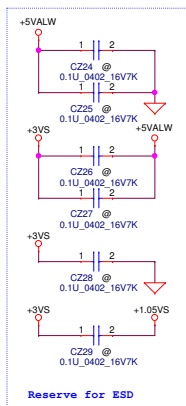
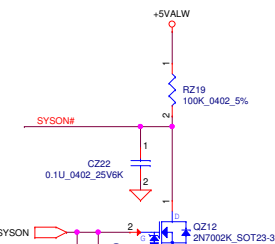
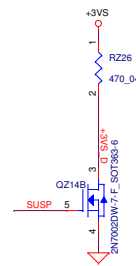
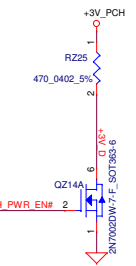
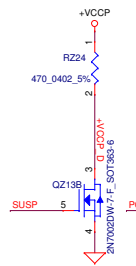
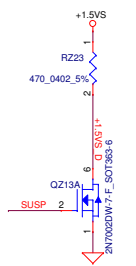
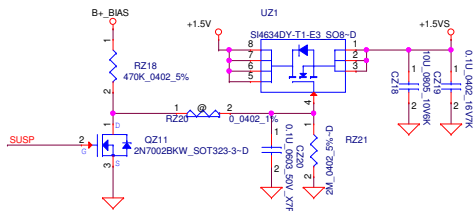


+3VALW to +3VS



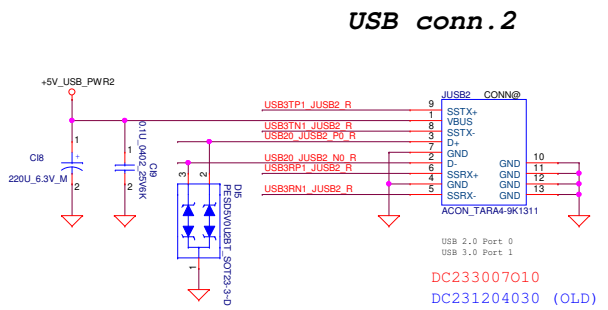
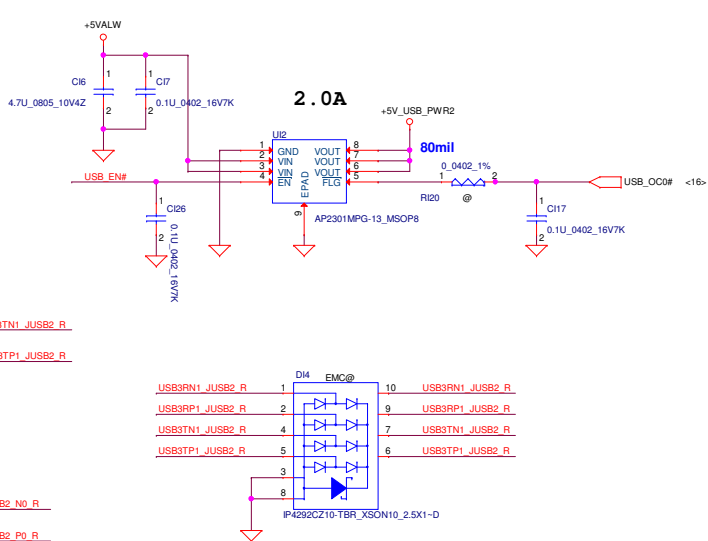
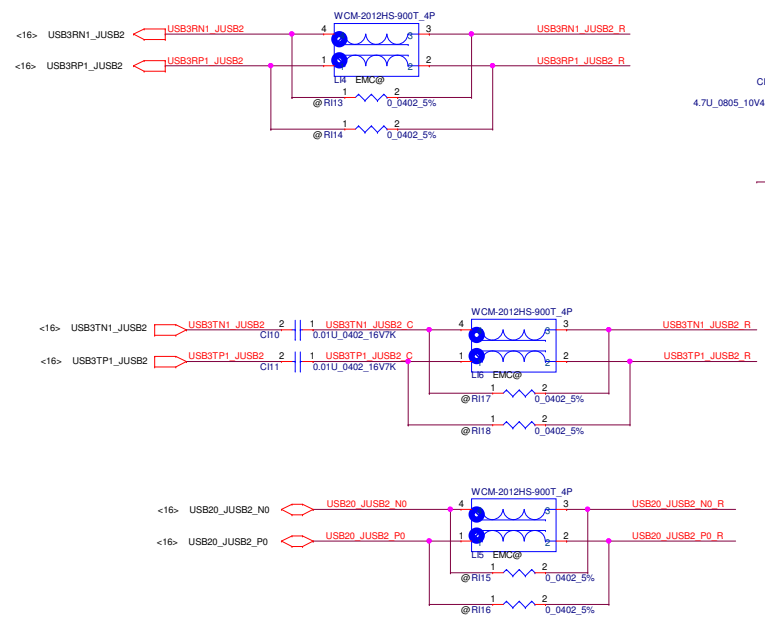
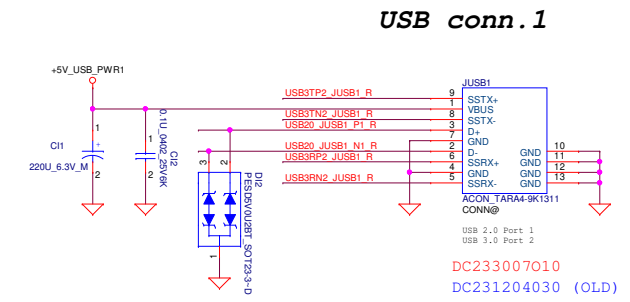
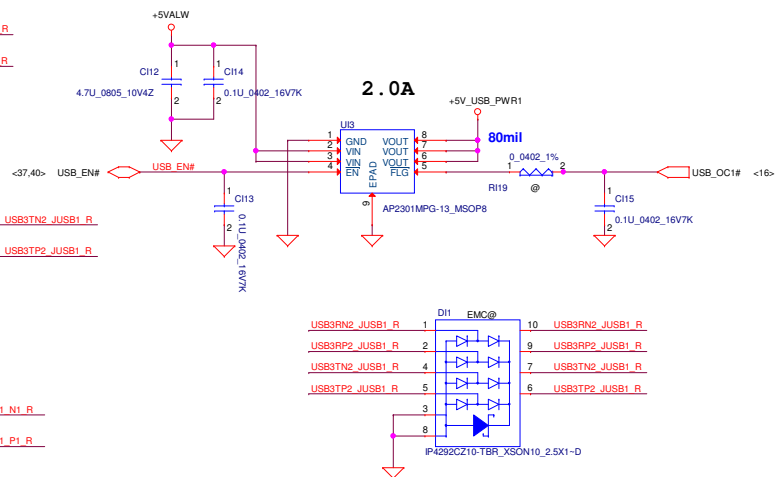
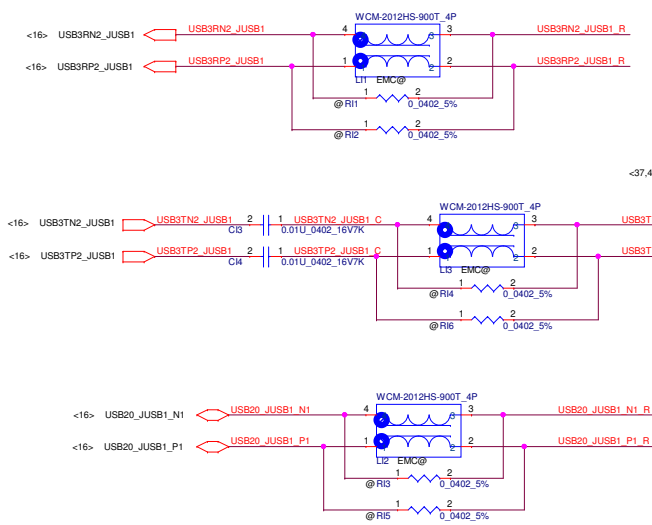
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CZ23 @ 0.1U_0402_16V7K
Please close to QZ9

+1.5V To +1.5VS

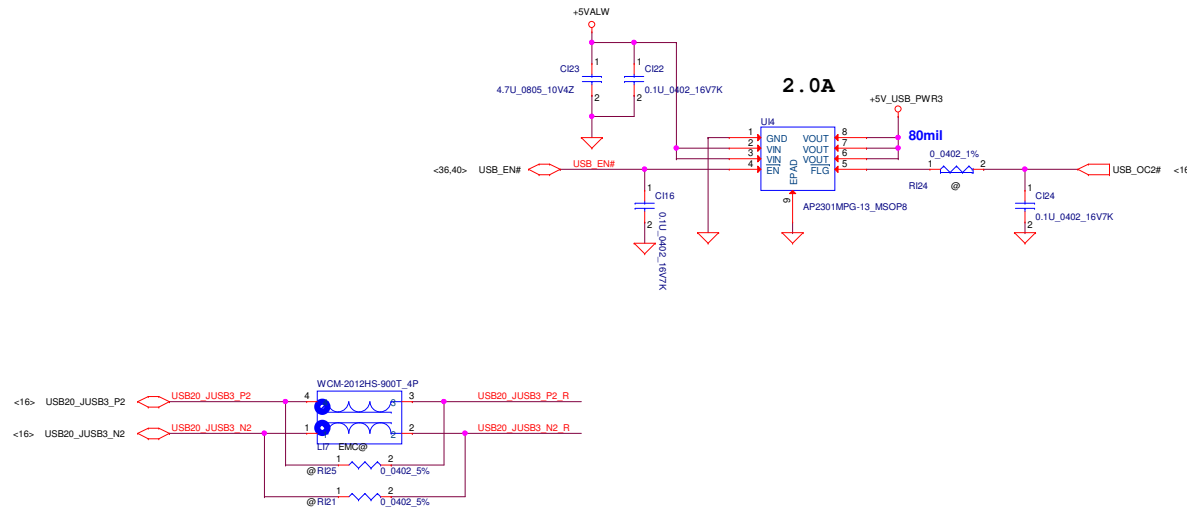


Reserve for ESD

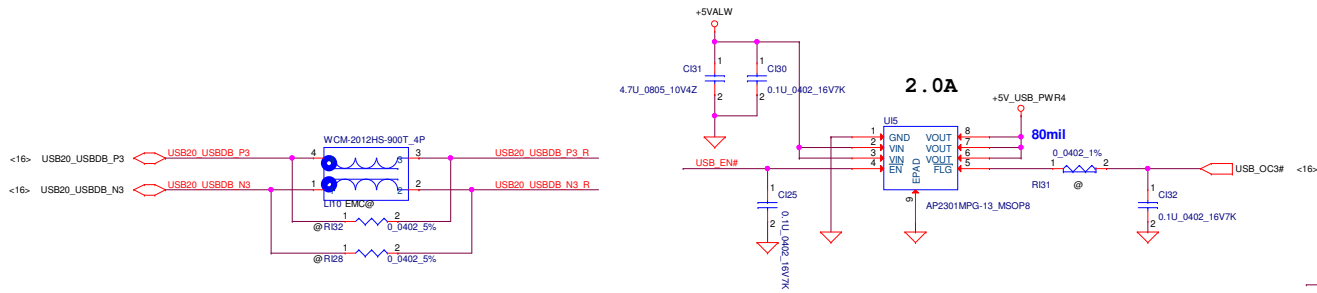
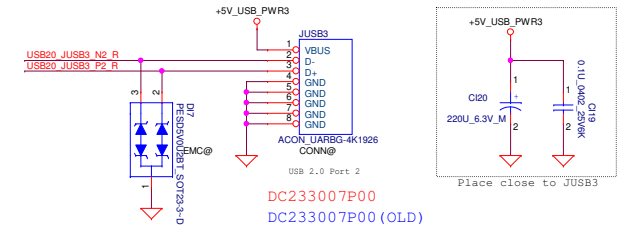
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	DC/DC Interface
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Date: Wednesday, August 28, 2012				Sheet 35 of 57



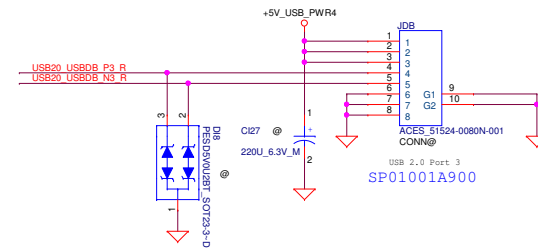
Security Classification	Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	USB3.0
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Doc No	LA-9101P	Rev	04	Date
Wednesday, August 28, 2012		Sheet	36	of 57



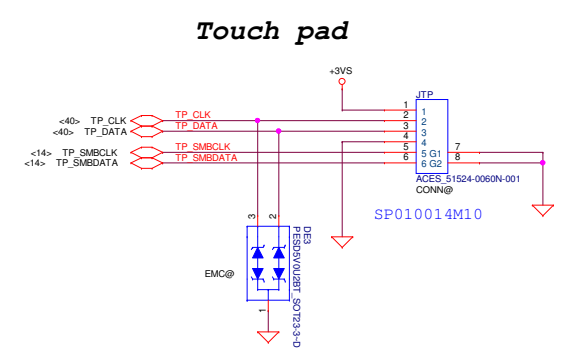
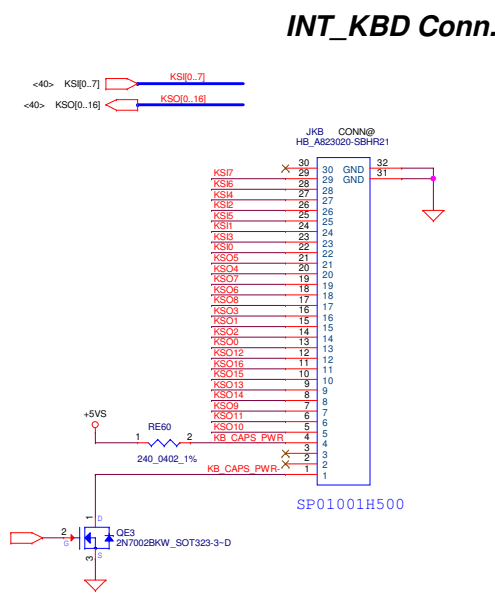
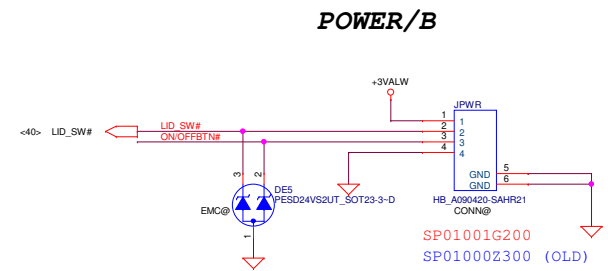
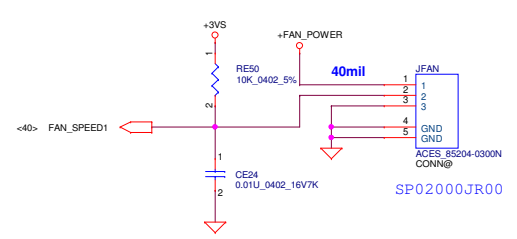
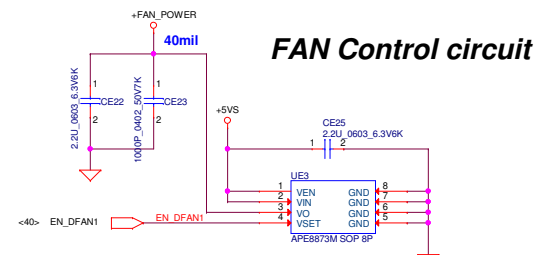
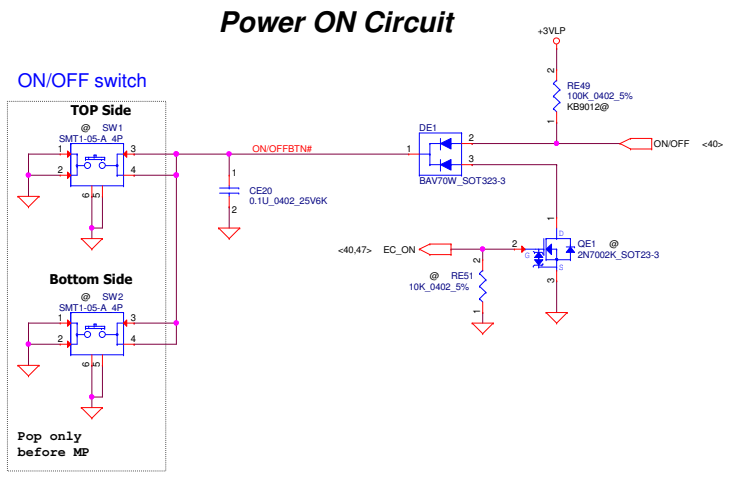
USB conn. 3



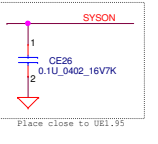
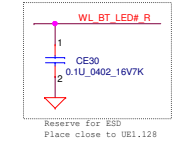
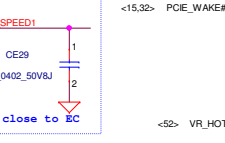
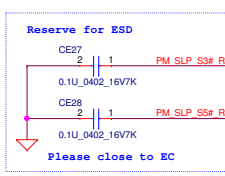
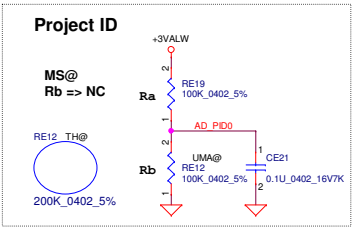
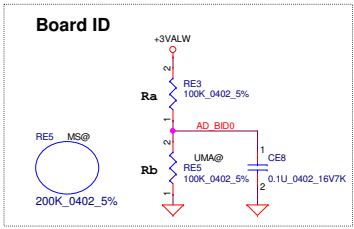
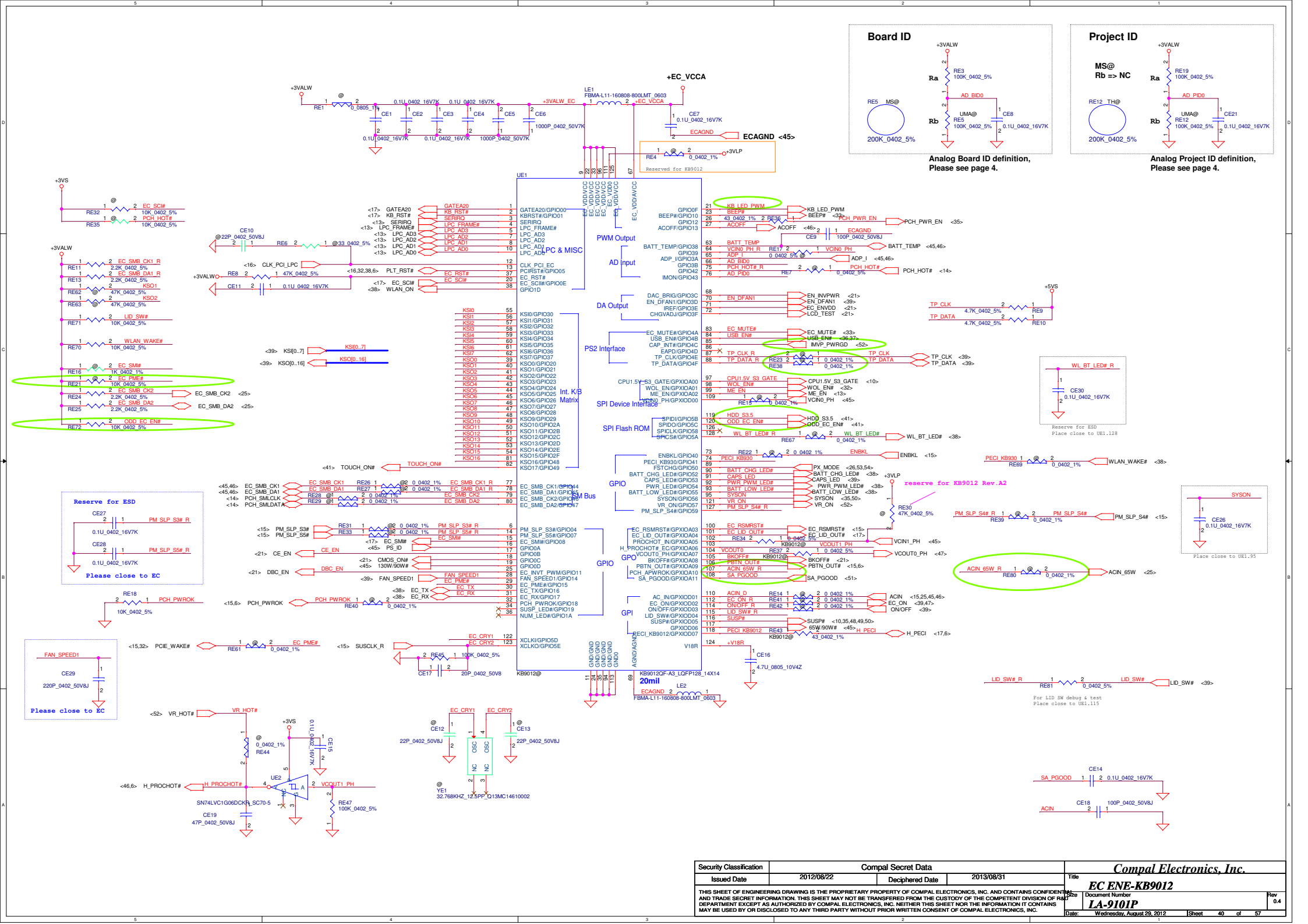
USB conn. 4



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				Rev 0.4 Sheet 37 of 57



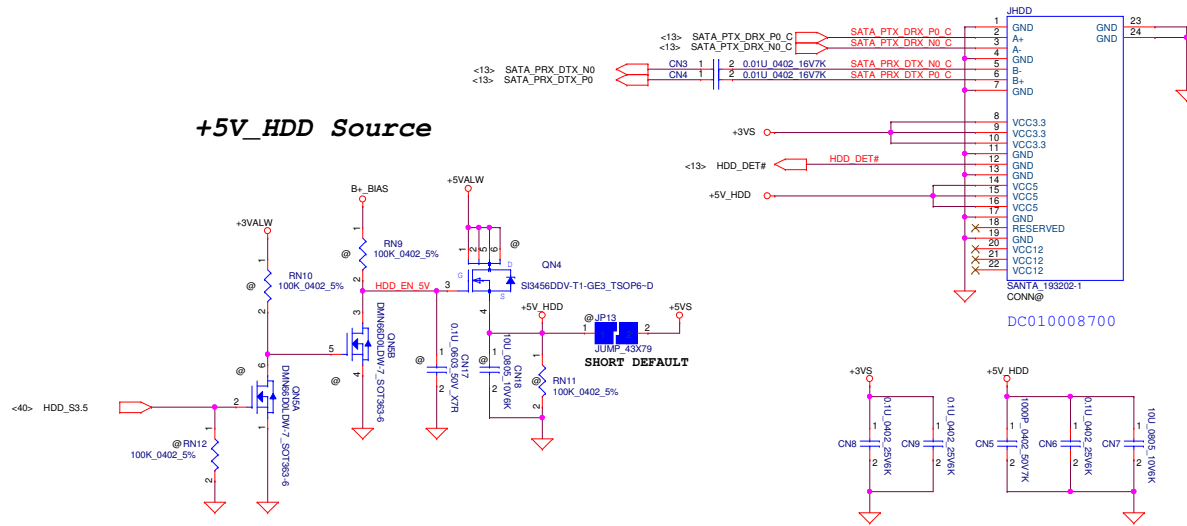
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	FAN/TP/KB/PWR SW	
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				LA-9101P	0.4
				Date: Wednesday, August 28, 2012	Sheet 39 of 57



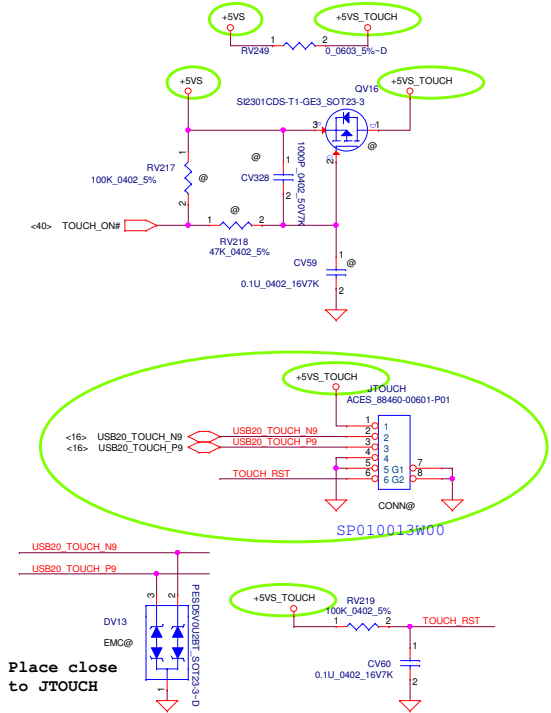
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Date: Wednesday, August 28, 2012				Sheet	40 of 57

SATA HDD Conn.

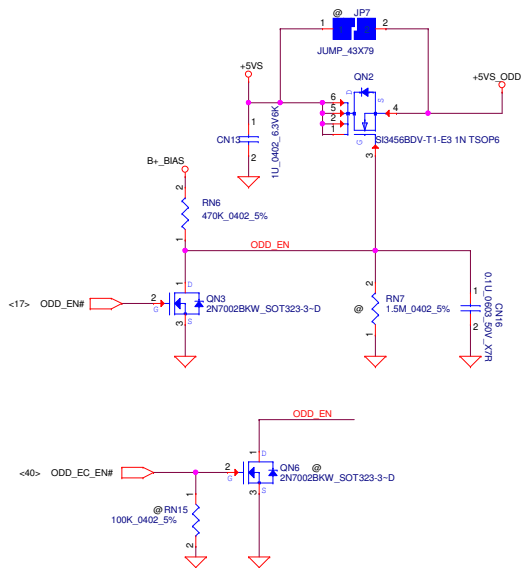
+5V_HDD Source



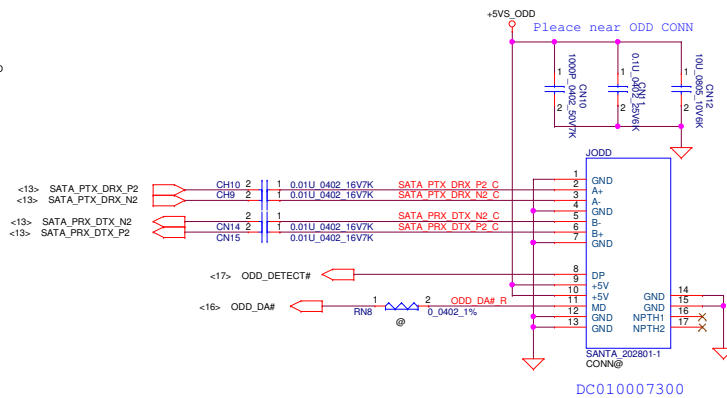
* Touch Screen Panel



ODD Power Control

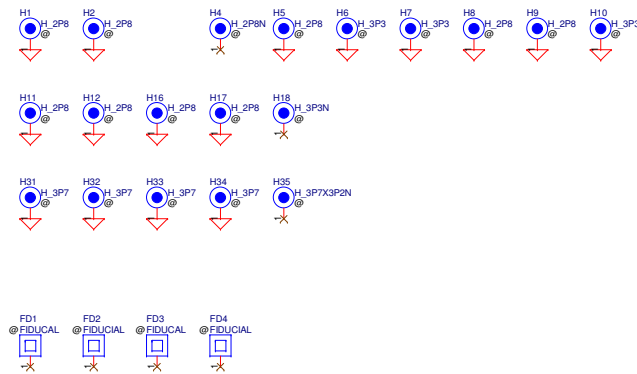


SATA ODD Conn.



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Screw Hole

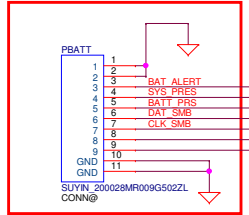
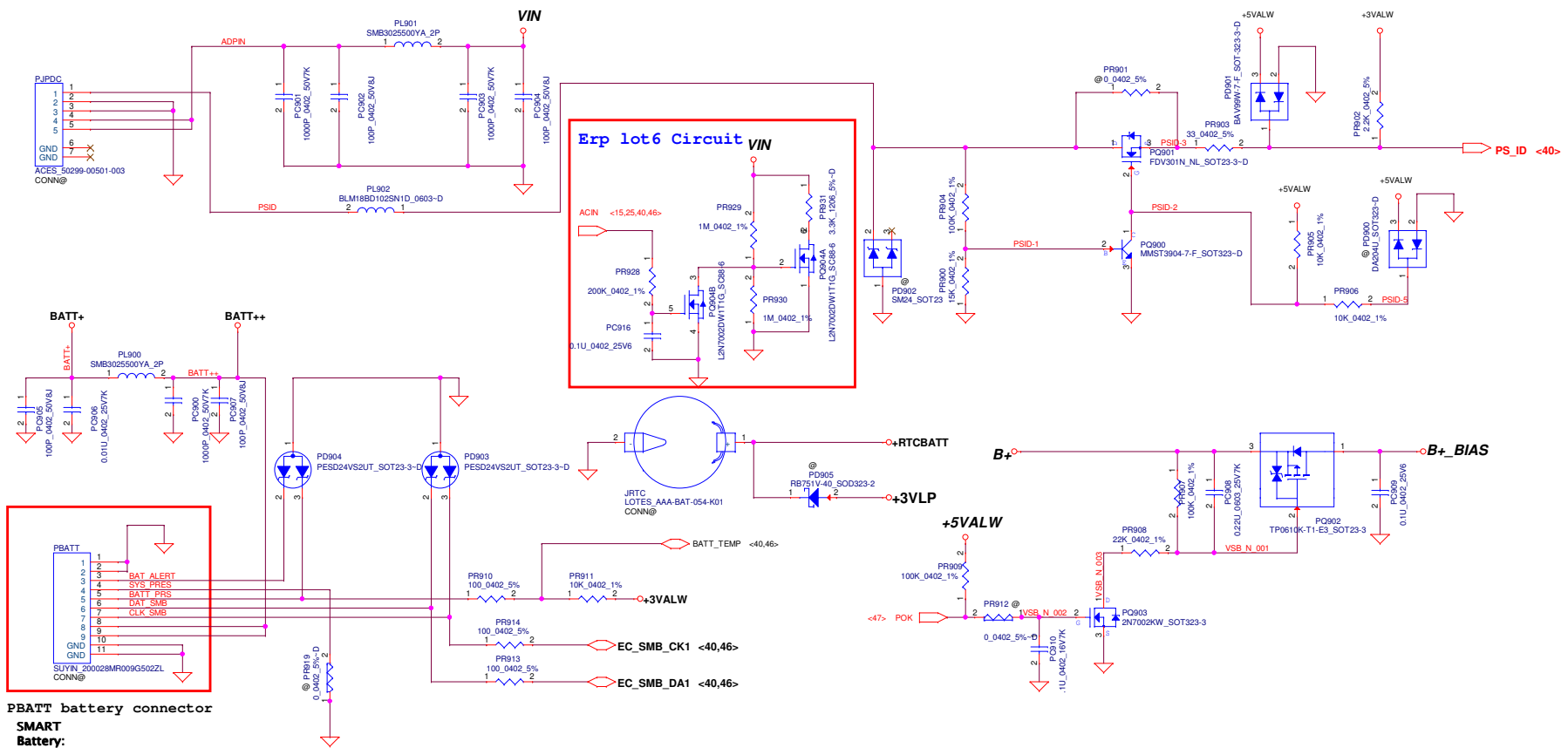


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				Sheet 42 of 57 Rev 0.4

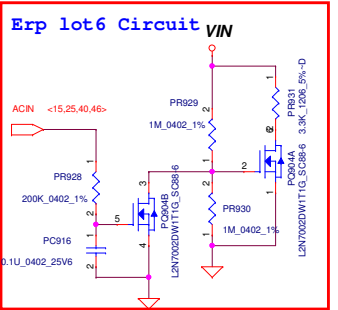
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2	40	Keyboard	2012/05/03	SED	Keyboard pin define change.	Follow new SPEC.SWAP JKB pin define.	0.2
3	16, 21, 34, 36, 37, 38	USB	2012/05/04	Function team	Change USB port assignment for function team request	USB port change detail please reference Page.16 description.	0.2
4	26	VGA	2012/05/05	HW	Delete reserve BACO circuit	Delete UV15, QV16, QV17, QV18, QV19, QV20, RV99, RV100, RV249, CV96, CV98	0.2
5	42	DC/DC	2012/05/07	HW	Design change	UN-POP R211, POP R217	0.2
6	33	Audio codec	2012/05/09	ESD	ESD team ask solution	Add RA29, RA30, RA31, RA32 and place on the moat between GND & GNDA	0.2
7	6, 17	PCH	2012/05/09	ESD	ESD team ask reserve solution	Add CC151, CH102 for reserve	0.2
8	32	LAN	2012/05/10	HW	Remove China Go-rural for DELL request	Remove DL7, DL8, DL9	0.2
9	16, 38	USB	2012/05/10	HW	Remove JUSB3 USB3.0	Delete LI8, LI9, DI6 and change JUSB3 to USB2.0 type	0.2
10	32	Crystal	2012/05/15	HW	Crystal vendor suggestion	Change CL36, CL37 from 33p/0402 to 12p/0402	0.2
11	21, 39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
12	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
13	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Separate NET JACK_PLUG to -> JACK_SENSE# & -> JACK_PLUG#	0.2
14	16, 21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
15	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
16	21, 39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
17	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1, QA1, QA2, QA3, RA24, RA26, RA60, RA62, RA68, RA109, CA72, CA73	0.2
18	15, 16, 39, 41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104, CZ23, CH105, CE27, CE28	0.2
19	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31, RH41, RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
20	10, 26, 41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, R218 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402	0.2
21	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change R215 to DE-POP	0.2
22	06, 15, 16, 39, 41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
23	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21, RL30 from "g" to "GCLK#"	0.2
24	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change R24, R213 from 470K/0402 56K/0402	0.2
25	35, 41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
26	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move RH42, RH43 from Page.13 to Page.41.	0.2
27	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.3
28	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.3
29	21, 35, 39, 40, 41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41 and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.3
30	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.3
31	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75, RV76, RV81 from "DIS#" to "TH#"	0.3
32	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.3
33	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.3
34	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.3
35	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.3
36	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.3
37	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.3
38	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.3
39	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44, RH48, RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_IDO_R for break signal trace	0.3
40	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.3
41	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.3

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				LA-910IP	0.4
				Date	Wednesday, August 28, 2012
				Sheet	43 of 57

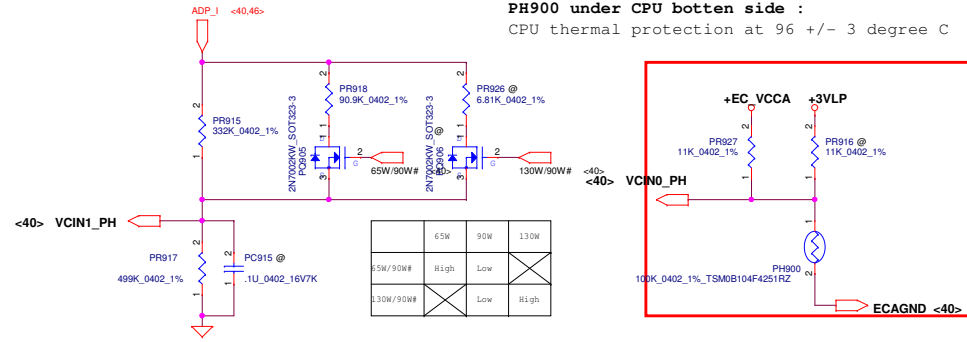
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.3
41	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.3
42	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.4
43	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.4
44	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.4
45	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.4
46	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	0.4
47	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.4
48	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	0.4
49	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	0.4
50	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	0.4
51	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	0.4
52	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006000 to SC50000DC00	0.4
53	38	WLAN	2012/08/20	HW	Remove AQAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	0.4
54	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	0.4

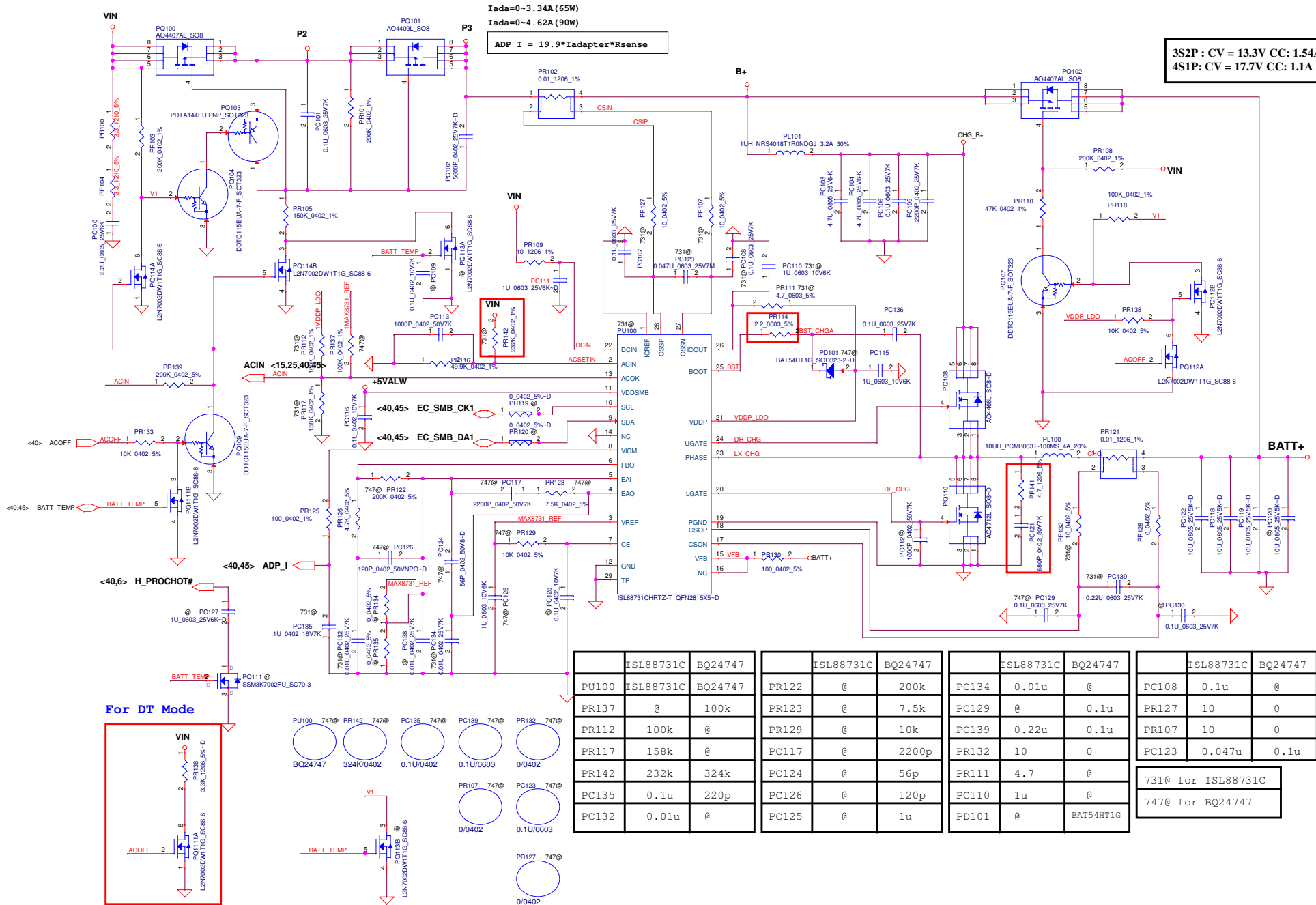


PBATT battery connector
SMART Battery:
 01.BATT+
 02.BATT+
 03.CLK_SMB
 04.DAT_SMB
 05.BATT_PRS
 06.SYS_PRES
 07.BAT_ALERT
 08.GND1
 09.GND2

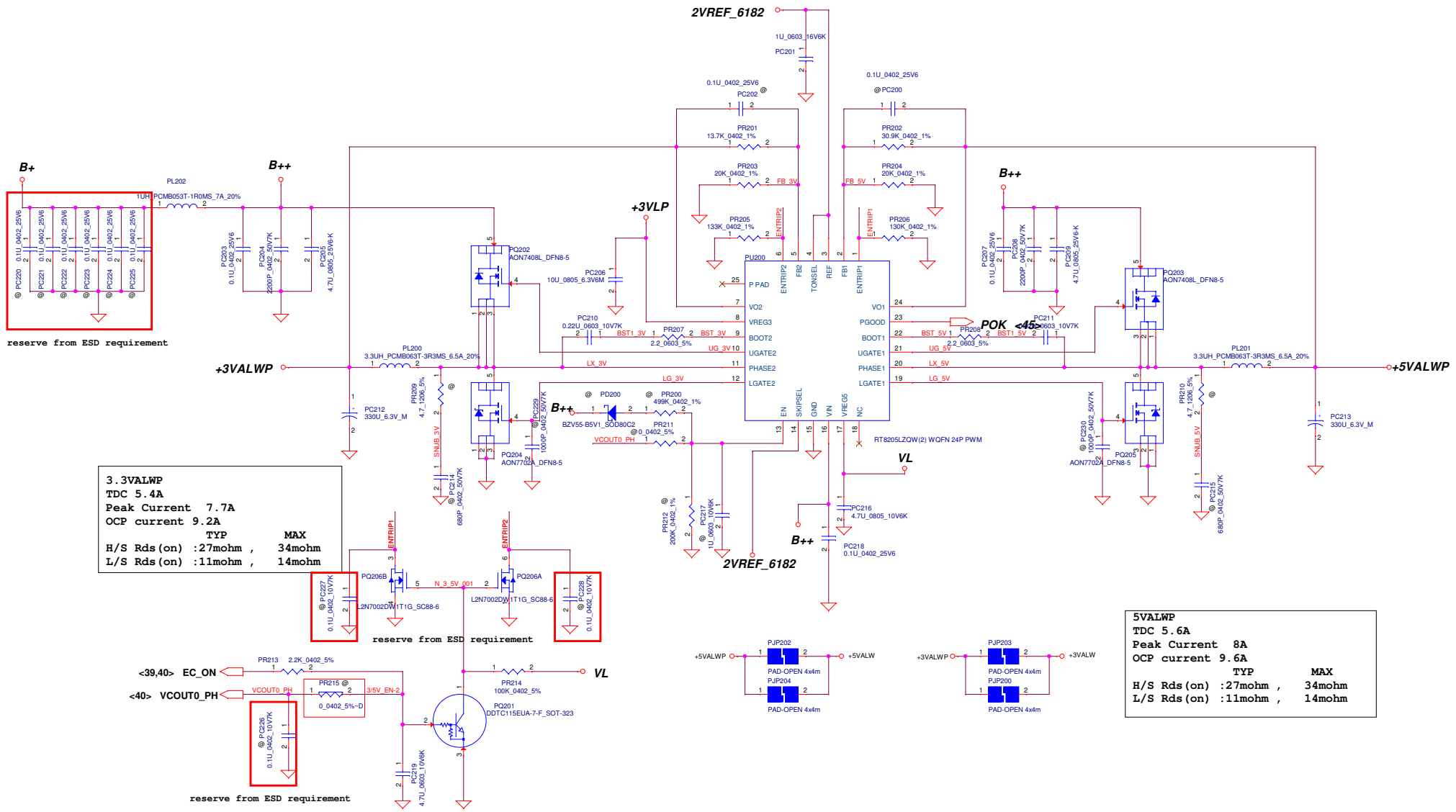


PH900 under CPU bottom side :
 CPU thermal protection at 96 +/- 3 degree C





	ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747
PU100	ISL88731C	BQ24747	PR122	@	200k	PC134	0.01u	@	PC108	0.1u	@
PR137	@	100k	PR123	@	7.5k	PC129	@	0.1u	PR127	10	0
PR112	100k	@	PR129	@	10k	PC139	0.22u	0.1u	PR107	10	0
PR117	158k	@	PC117	@	2200p	PR132	10	0	PC123	0.047u	0.1u
PR142	232k	324k	PC124	@	56p	PR111	4.7	@	731@ for ISL88731C 747@ for BQ24747		
PC135	0.1u	220p	PC126	@	120p	PC110	1u	@			
PC132	0.01u	@	PC125	@	1u	PD101	@	BAI54HT1G			



B+

reserve from ESD requirement

+3VALWP

3.3VALWP
 TDC 5.4A
 Peak Current 7.7A
 OCP current 9.2A

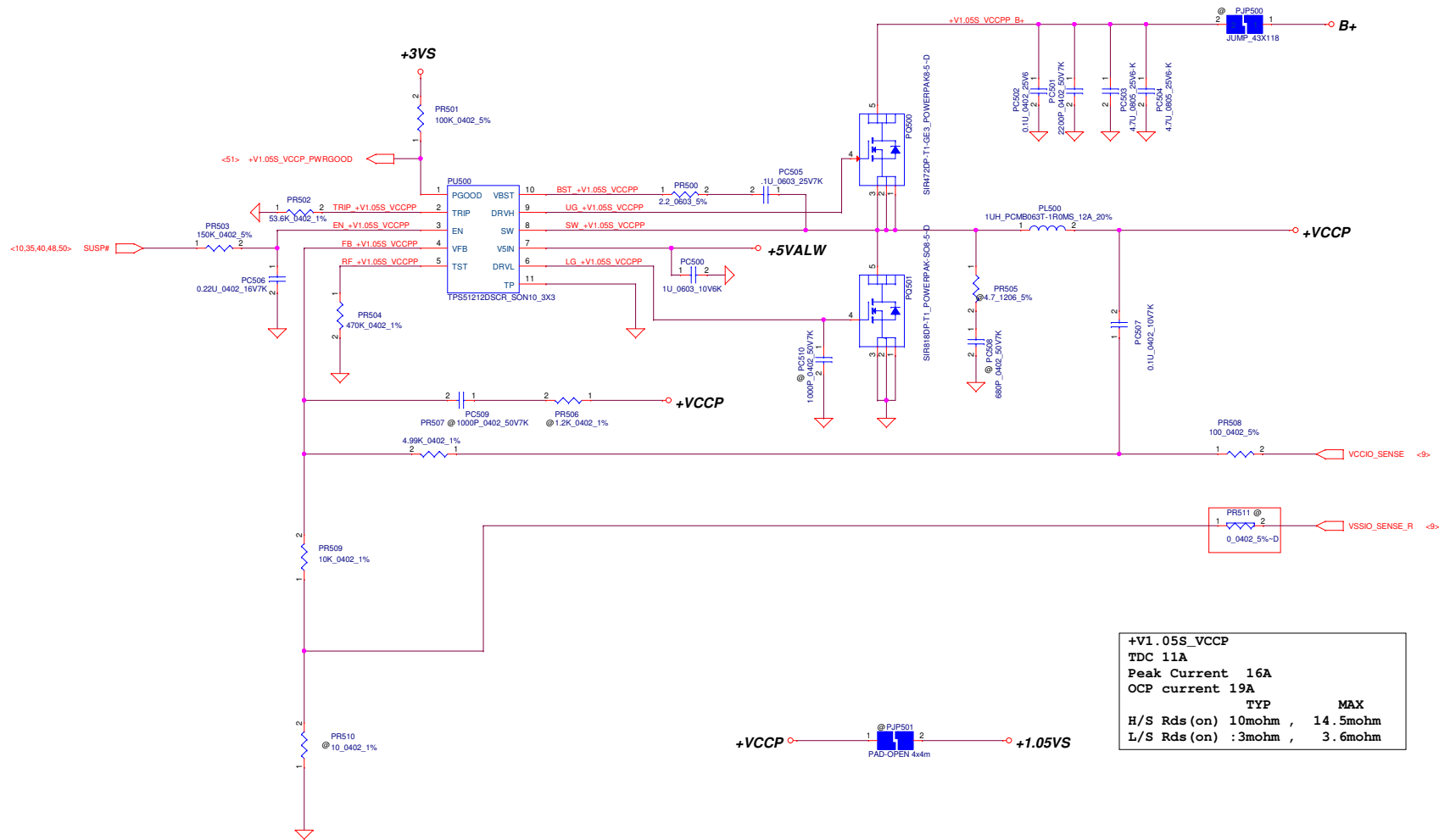
	TYP	MAX
H/S Rds (on)	: 27mohm	34mohm
L/S Rds (on)	: 11mohm	14mohm

reserve from ESD requirement

5VALWP
 TDC 5.6A
 Peak Current 8A
 OCP current 9.6A

	TYP	MAX
H/S Rds (on)	: 27mohm	34mohm
L/S Rds (on)	: 11mohm	14mohm

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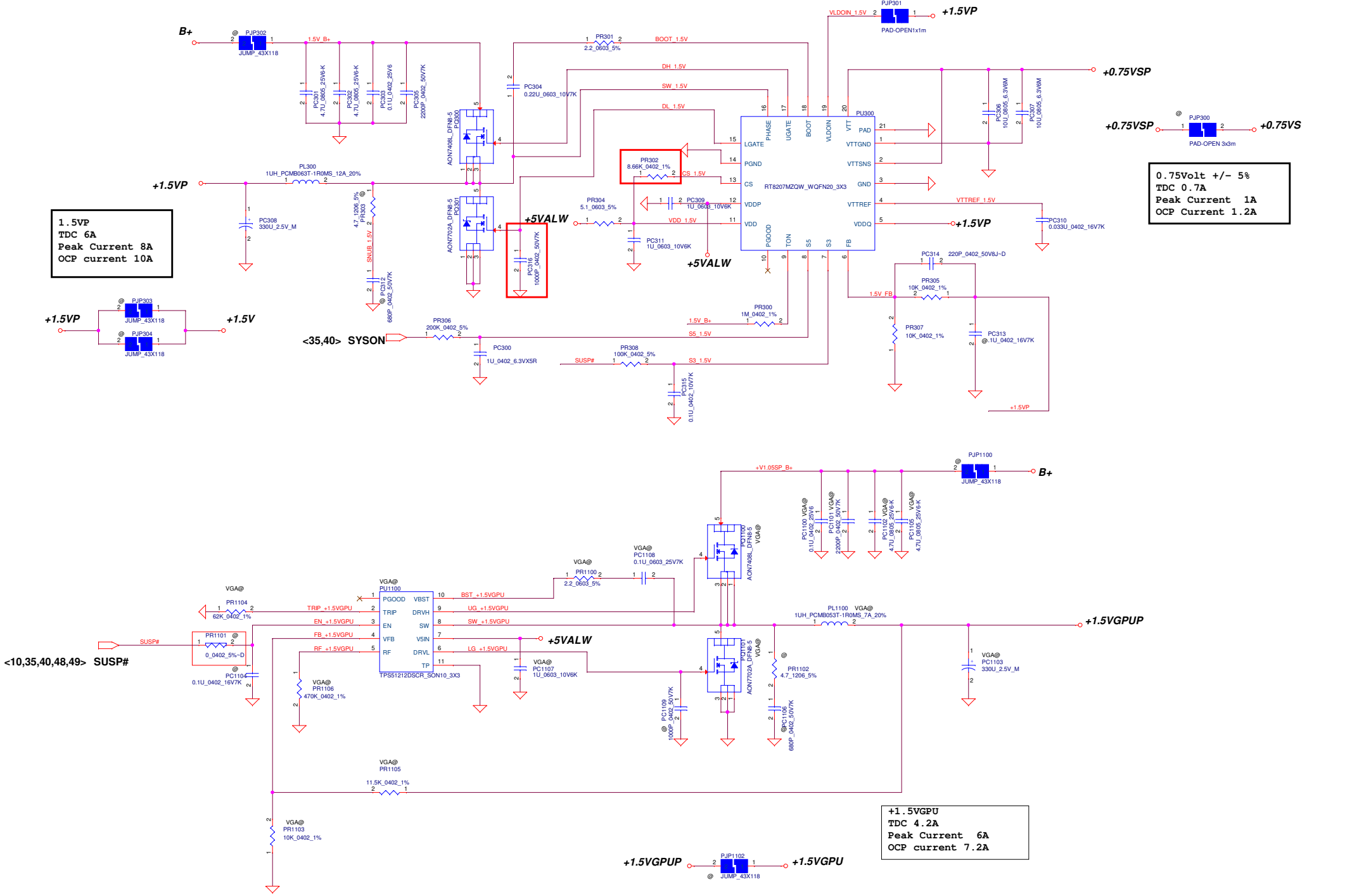
+V1.05S_VCCP
TDC 11A
Peak Current 16A
OCF current 19A
TYP MAX
H/S Rds (on) 10mohm , 14.5mohm
L/S Rds (on) : 3mohm , 3.6mohm

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2012/08/22		2013/07/31		Document Number	
				LA-9101P	
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				Sheet 49 of 57	

1.5VP
 TDC 6A
 Peak Current 8A
 OCP current 10A

0.75Volt +/- 5%
 TDC 0.7A
 Peak Current 1A
 OCP Current 1.2A

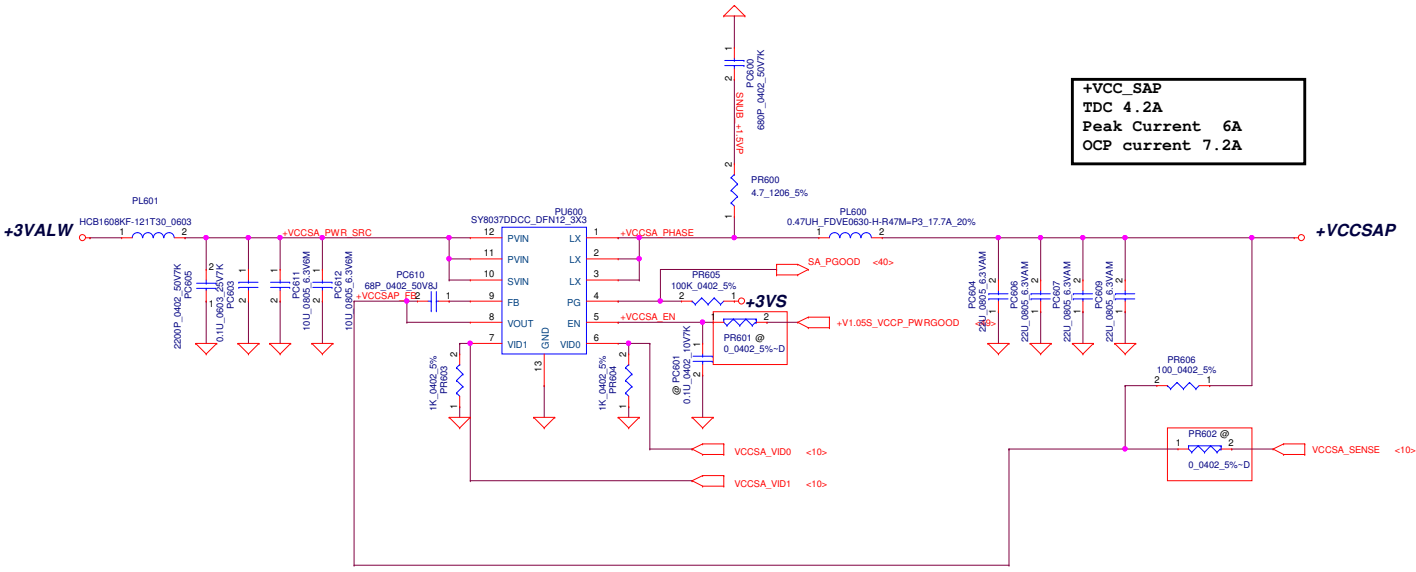
+1.5VGPU
 TDC 4.2A
 Peak Current 6A
 OCP current 7.2A



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Sheet 50 of 57				

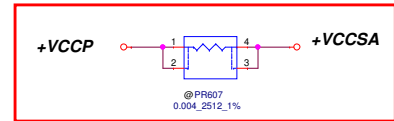
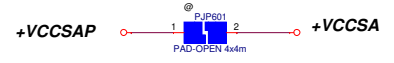
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

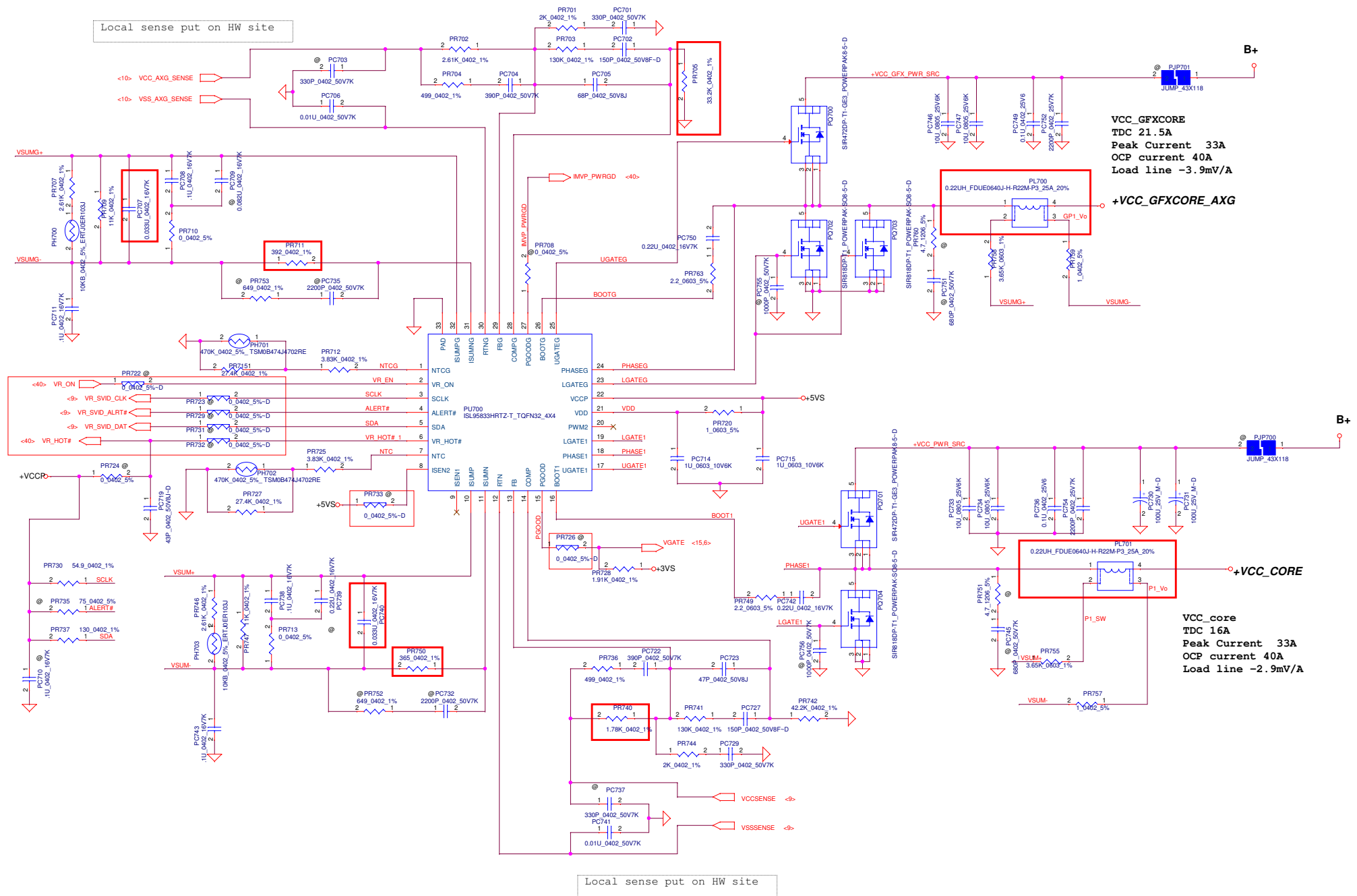


+VCC_SAP
 TDC 4.2A
 Peak Current 6A
 OCP current 7.2A

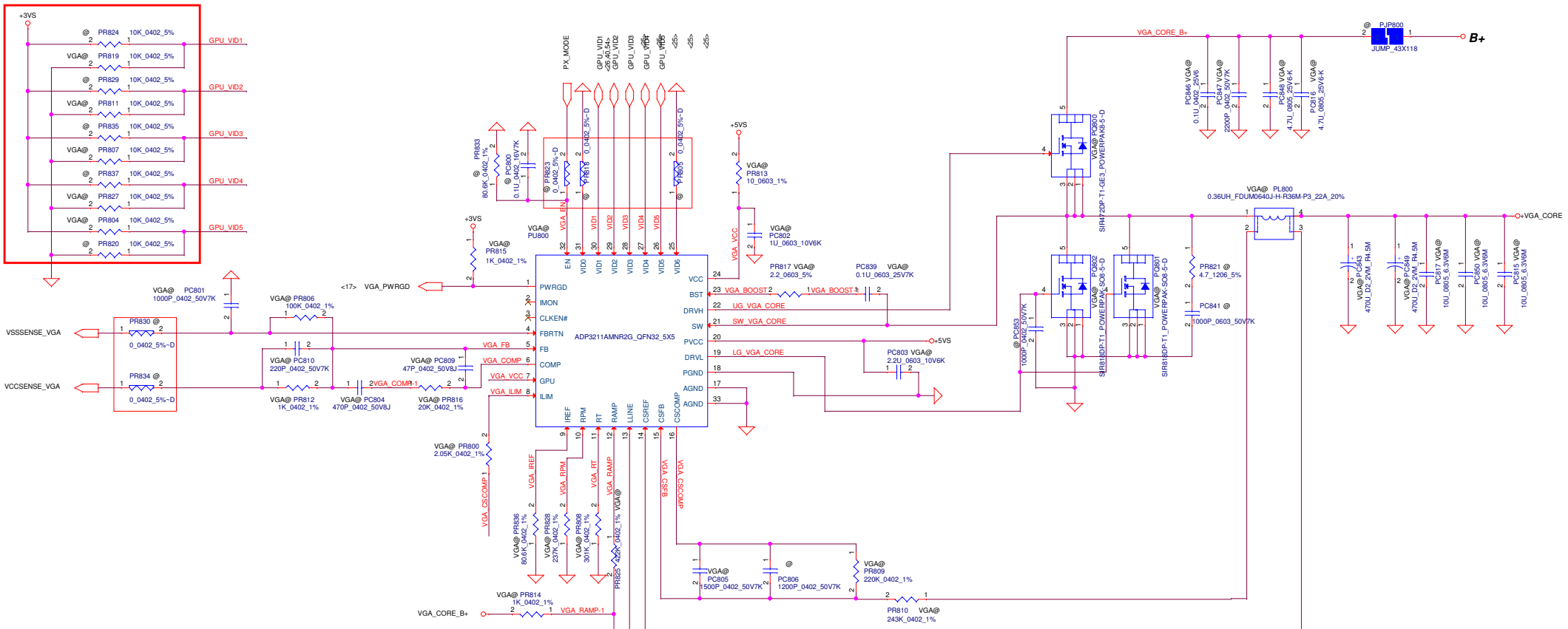
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only



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Date: Wednesday, August 28, 2012				Sheet 52 of 57



Mars Pro

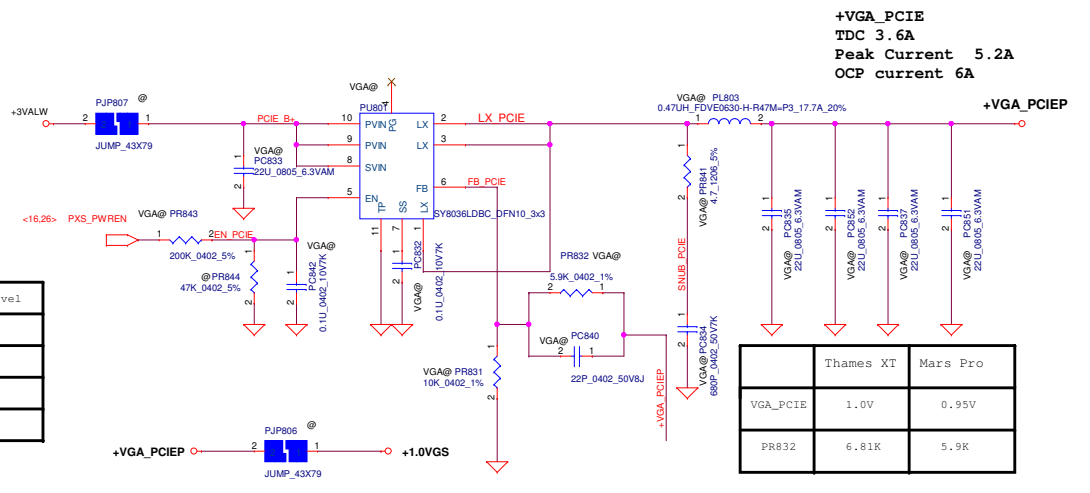
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA_CORE
 TDC 22A
 Peak Current 30A
 OCP current 36A
 FSW=350kHz
 DCR 1.1mohm +/-5%
 Loadline = 1.5mohm

Thames XT

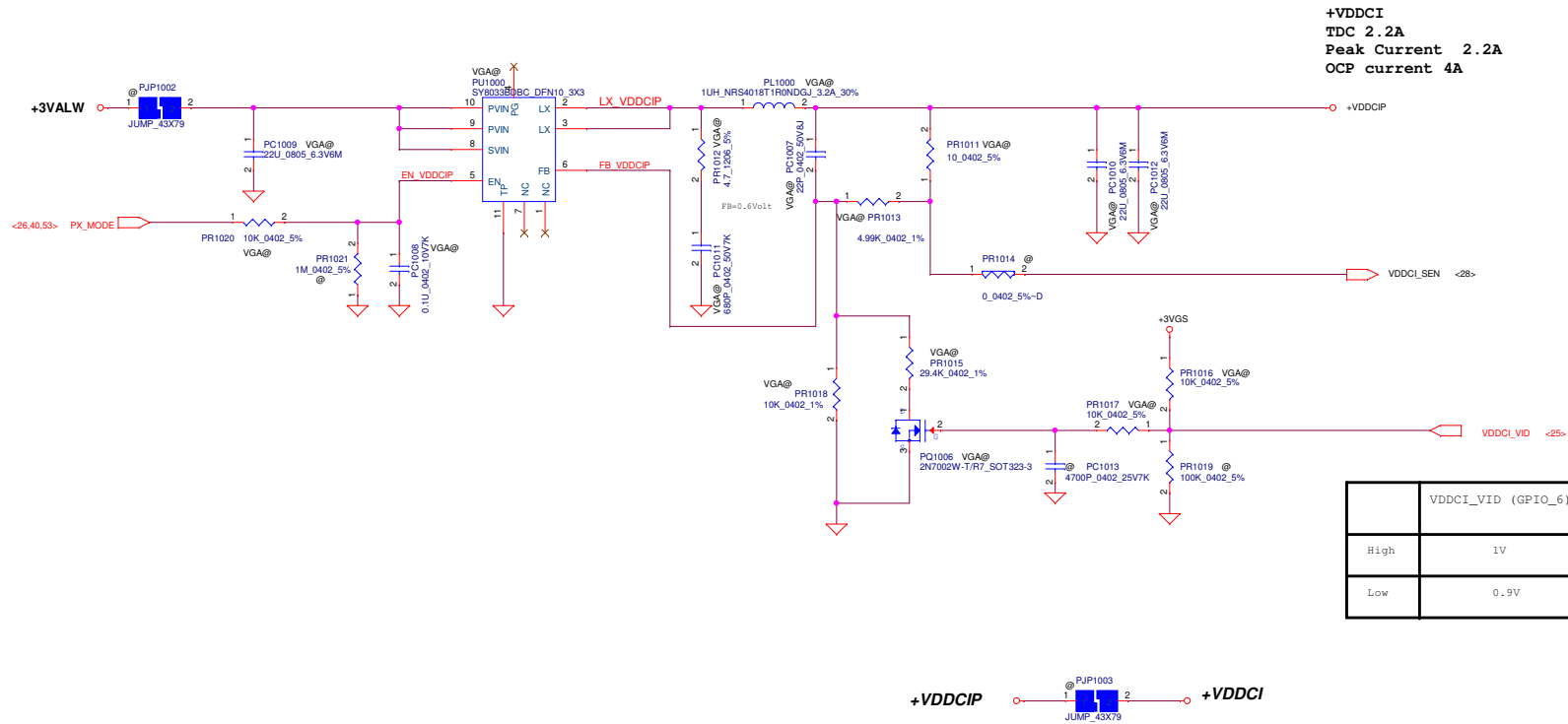
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V

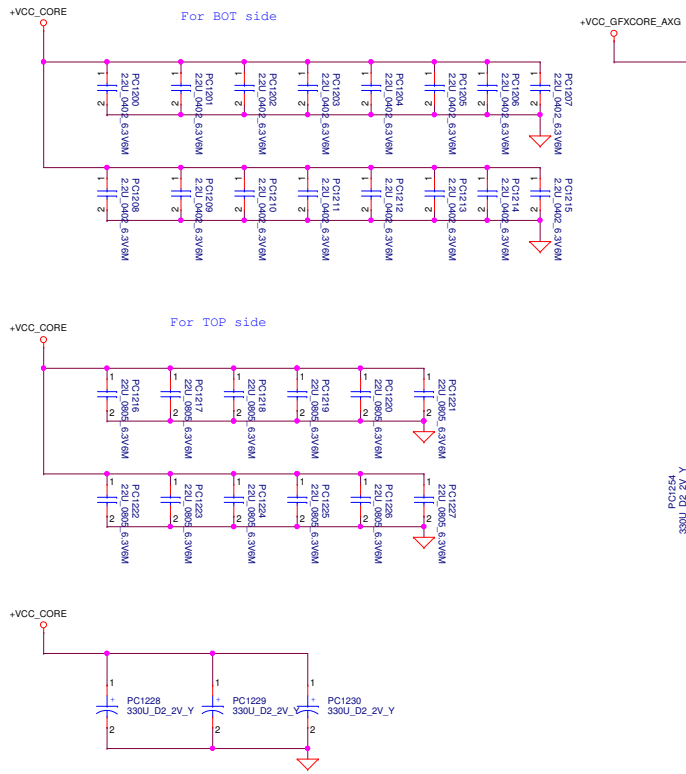
+VGA_CORE
 TDC 20A
 Peak Current 30A
 OCP current 36A
 FSW=350kHz
 DCR 1.1mohm +/-5%



+VGA_PCIE
 TDC 3.6A
 Peak Current 5.2A
 OCP current 6A

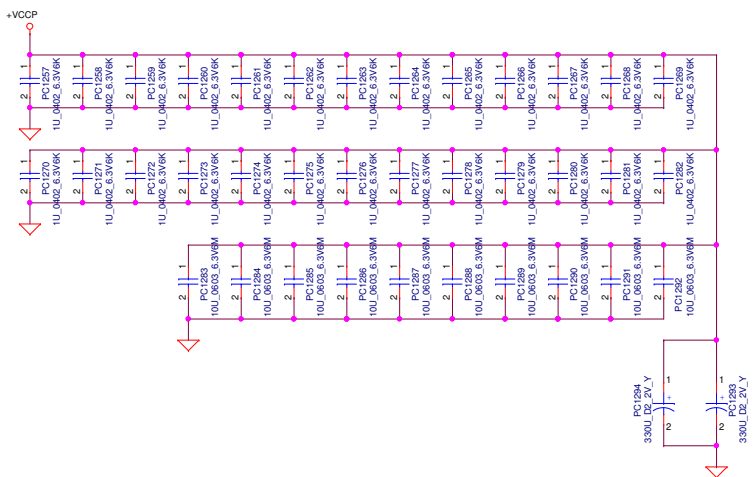
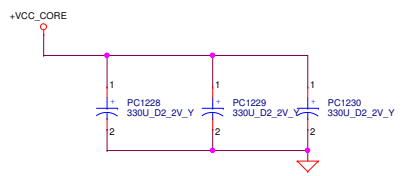
	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



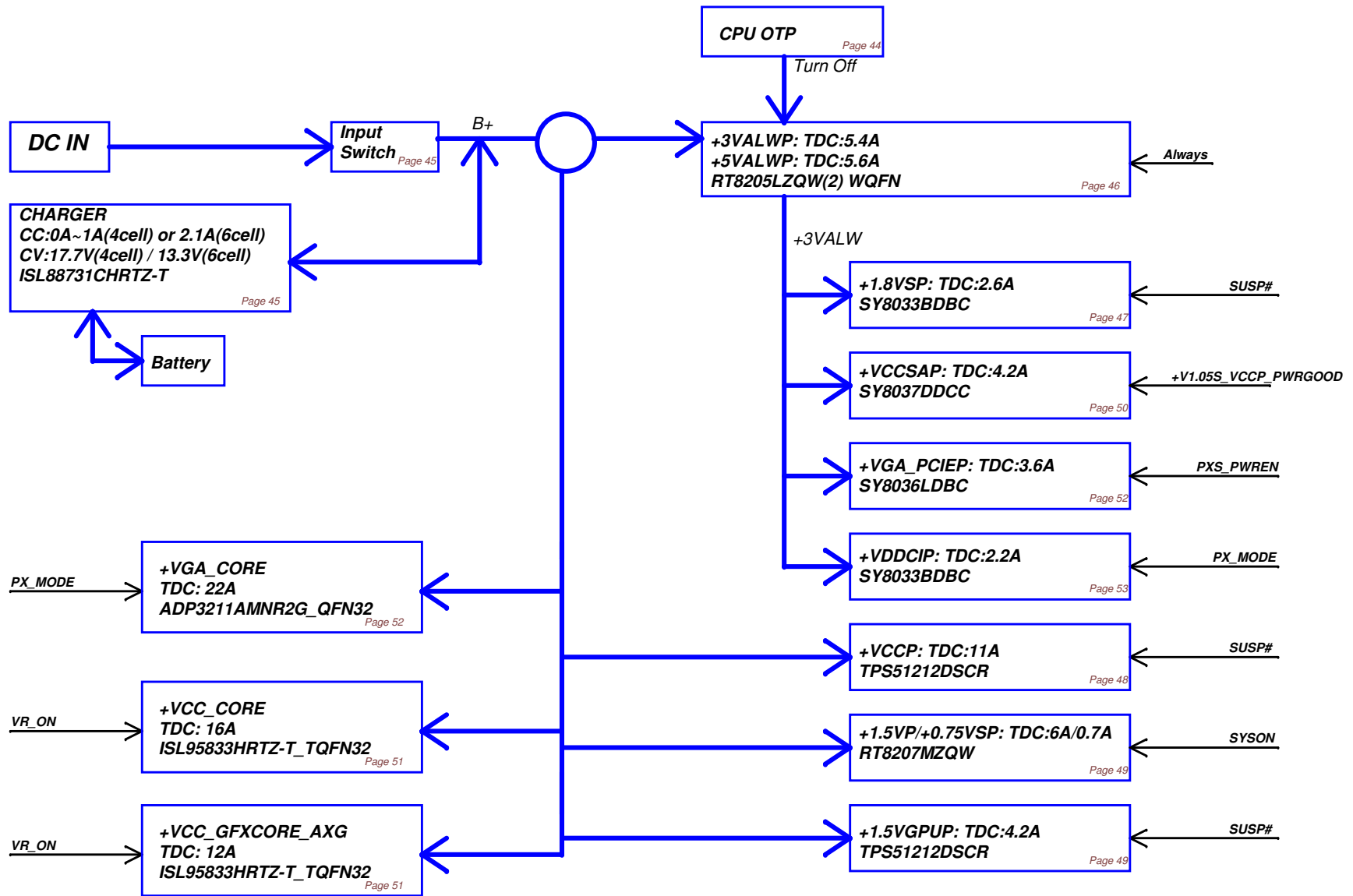


Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



Power block



Version Change List (P. I. R. List)

<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

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