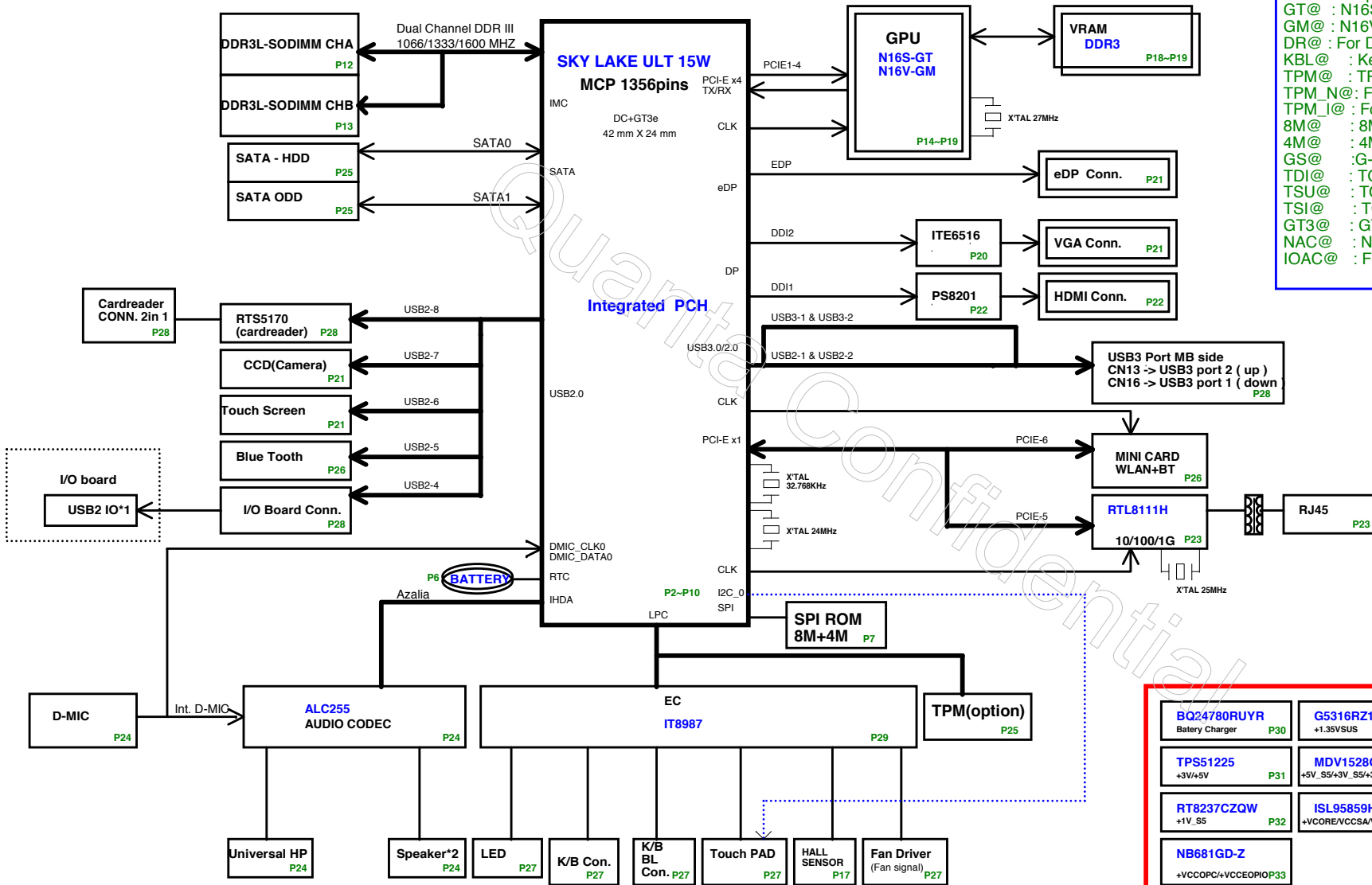


# Zoro SL (ZRW) SKL ULT SYSTEM BLOCK DIAGRAM

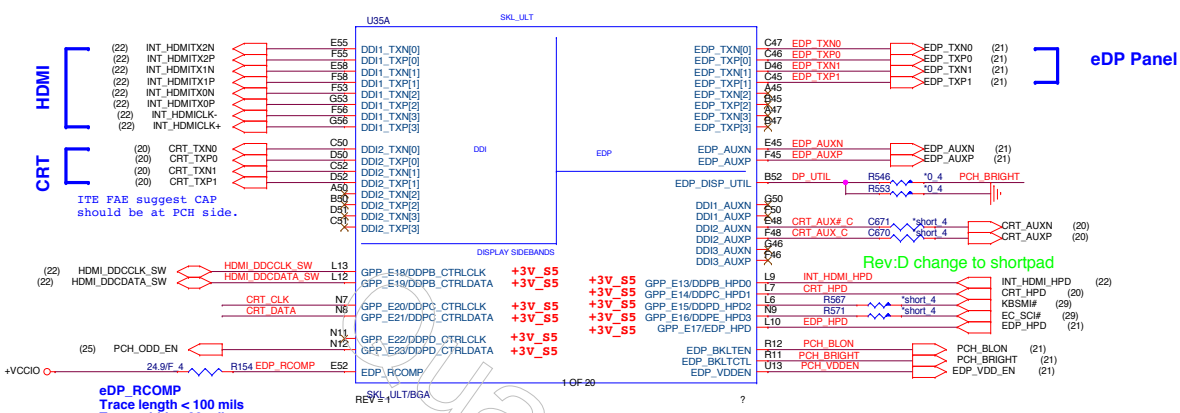


**BOM**

- IV@ : iGPU
- EV@ : Optimus
- GT@ : N16S-GT / GC6
- GM@ : N16V-GM / WO GC6
- DR@ : For Dual Rank ( VRAM 8 pcs)
- KBL@ : Keyboard backlight
- TPM@ : TPM
- TPM\_N@: For TPM 2.0
- TPM\_I@: For TPM 1.2
- 8M@ : 8M FLASH ROM
- 4M@ : 4M FLASH ROM
- GS@ : G-SENSOR
- TDI@ : TOUCH PAD I2C
- TSU@ : TOUCH SCREEN USB
- TSI@ : TOUCH SCREEN I2C
- GT3@ : GT3 CPU
- NAC@ : Non IOAC
- IOAC@ : For IOAC

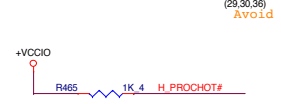
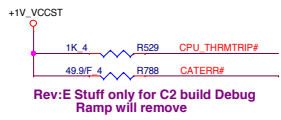
<b>BQ24780RUYR</b> Battery Charger P30	<b>G5316RZ1D</b> +1.35VSUS P35	<b>Thermal Protection</b> Discharger P40
<b>TPS51225</b> +3V/+5V P31	<b>MDV1528Q</b> +5V_S5/+3V_S5/+3V/+5V P31	<b>UP1658RQKF</b> +VGPU CORE P41
<b>RT8237CZQW</b> +1V_S5 P32	<b>ISL95859HRTZ-T</b> +VCORE/VCCSA/VCCGT P38	<b>RT8068AZQW</b> +1.05V_GFX/+3V_GFX +1.5V_GFX P42
<b>NB681GD-Z</b> +VCCOP/+VCCOP/OP33		

Skylake ULT (DISPLAY,eDP)



ITE FAE suggest CAP should be at PCH side.

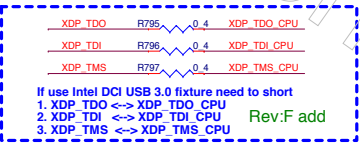
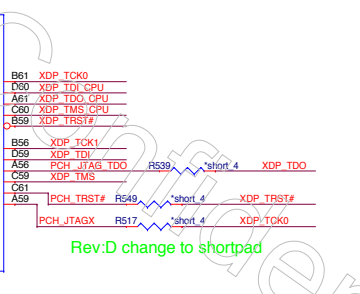
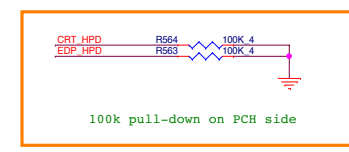
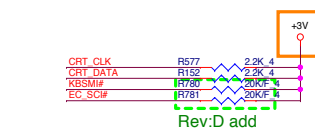
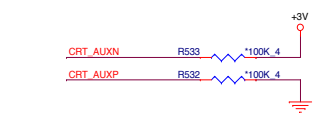
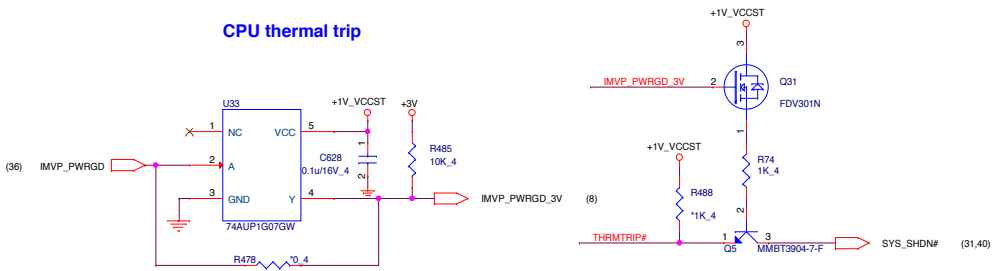
eDP\_RCMP Trace length < 100 mils Trace width = 20 mils Trace spacing = 25 mils



BPM#[0:7] Trace Length 1-6 inches Length match < 300 mils

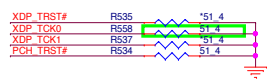
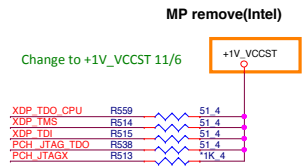
SM\_RCMP[0:2] Trace length < 500 mils Trace width = 12-15 mils Trace spacing = 20 mils

CPU thermal trip



PCH JTAG JTAG\_TCK,JTAG\_TMS Trace Length < 9000mils

TCK,TMS Trace Length < 9000mils



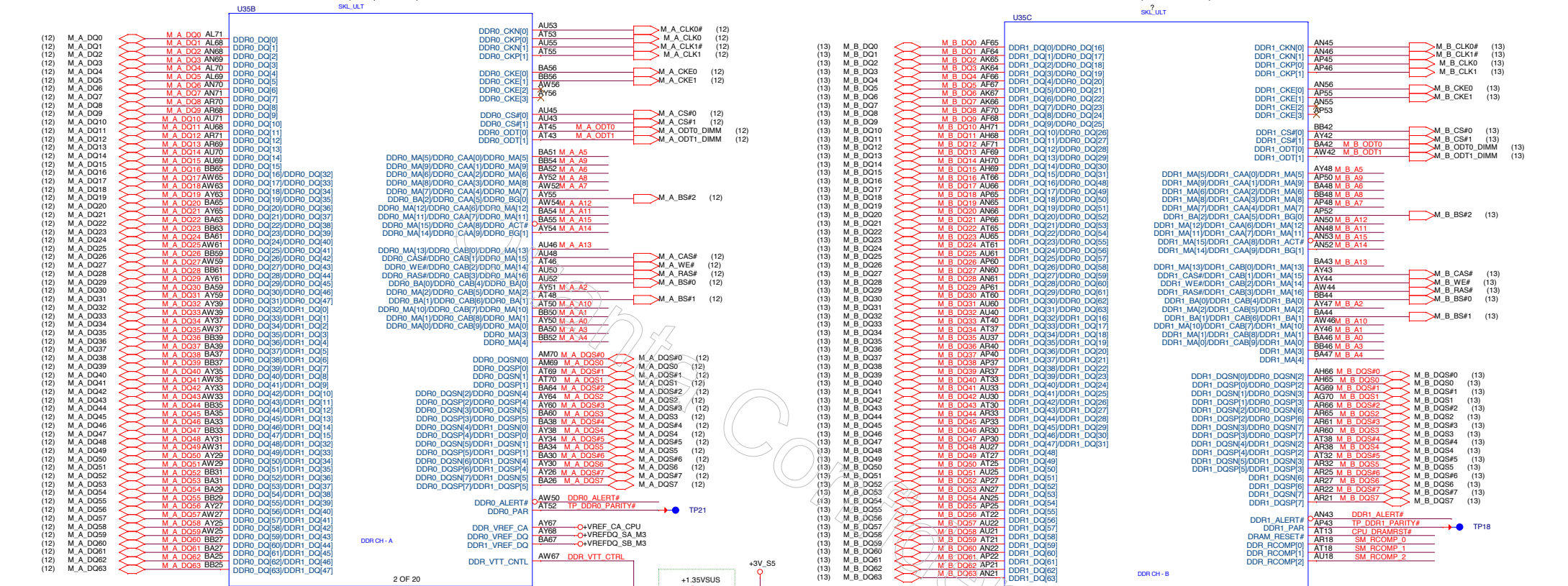
2/16 XDP\_TCK1,XDP\_TMS don't need pull up or pull down

5/29 XDP\_TCK0 R558 Stuff

Change Data and DQS to interleave.

SKL ULT (DDR3L)

SKL ULT (DDR3L)



Stuff Q54 for both UMA and GPU in DDR\_VTT\_CNTL

REV:E connect to GND

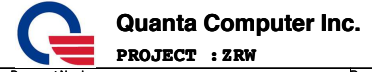
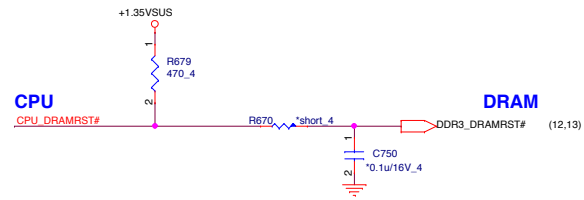
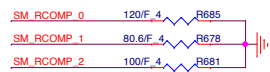
DDR0\_ALERT#  
DDR1\_ALERT#

DRAM COMP

DRAMRST

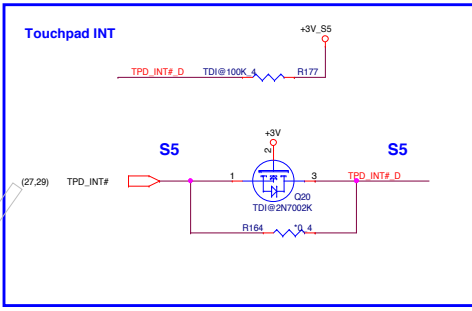
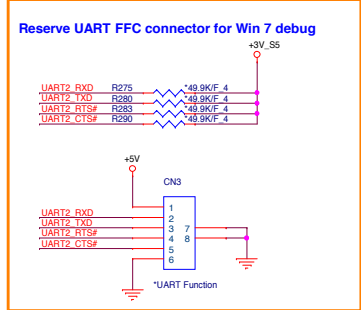
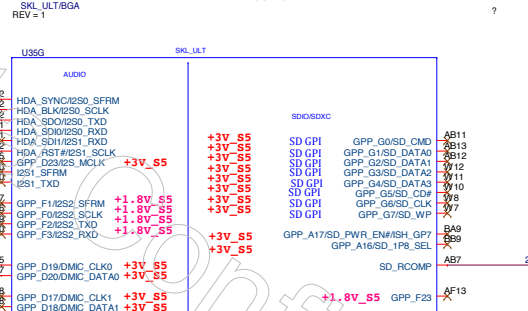
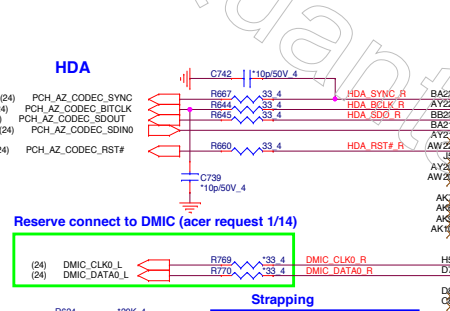
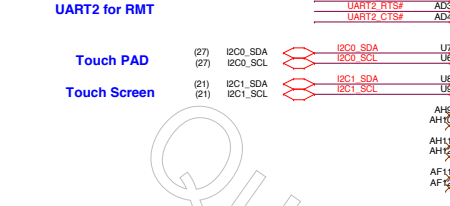
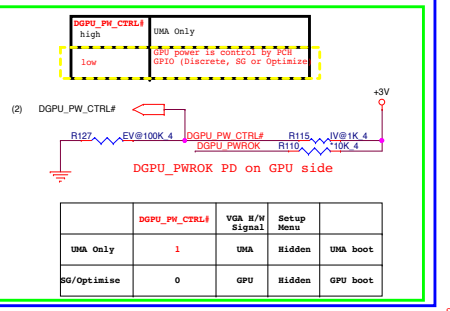
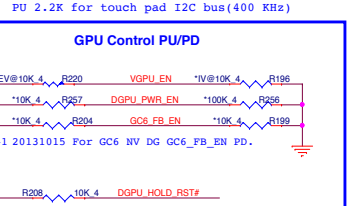
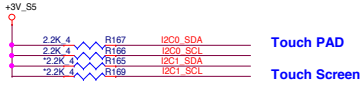
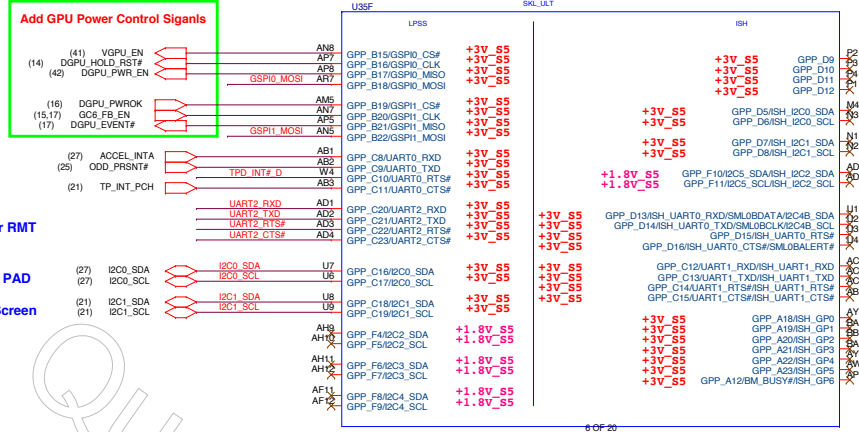
CPU

DRAM



H\_PECI (50ohm)  
Route on microstrip only  
Spacing >18 mils  
Trace Length: 0.4-6.125 inches

H\_PWRGOOD (50ohm)  
Trace Length: 1-11.25 inches

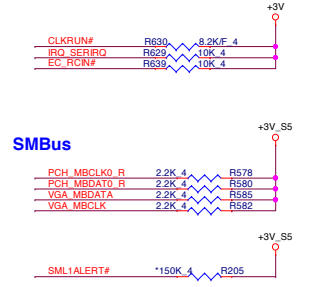
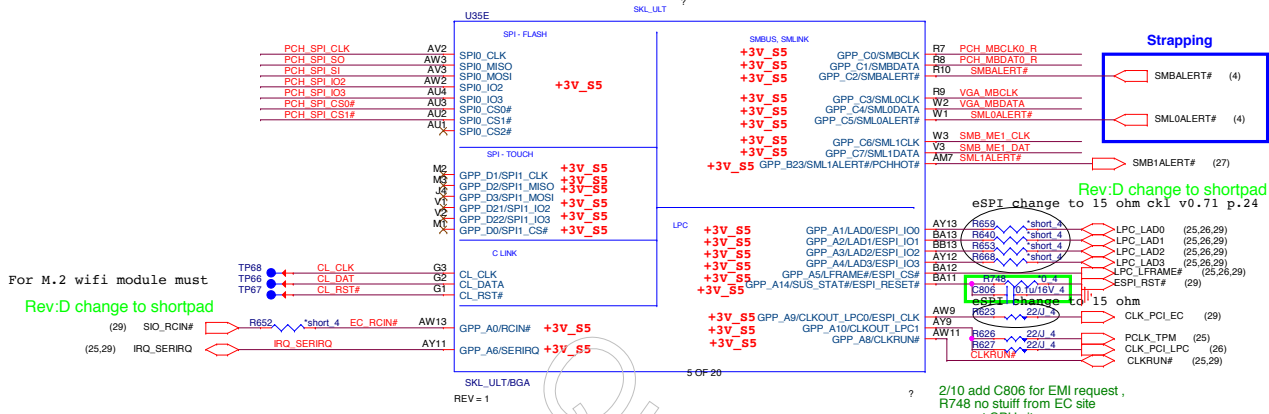


Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (IPD 20K) 1 = Enable Top Swap Mode	+3V ○ R625 ~1K 4 SPKR
GPP_B18 (GSPi0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) 1 = Enable No Reboot Mode	+3V ○ R619 ~1K 4 GSPi0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS (IPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_S5 ○ R160 ~10K 4 SMBALERT# (7)
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (IPD 20K) 1 = LPC	+3V ○ R207 ~1K 4 GSPi1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (IPD 20K) 1 = eSPI selected for EC	+3V_S5 ○ R586 ~1K 4 SML0ALERT# (7)
SPI0_MOSI	Reserved	RSMRST#	(IPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(IPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# / PCHHOT#)	Reserved	RSMRST#	(IPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(IPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(IPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (IPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal +3V_S5 ○ HDA_SDO_R R733 ~1K 4 ME_WR# (29)
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (IPD 20K) 1 = Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (IPD 20K) 1 = Port C is detected	



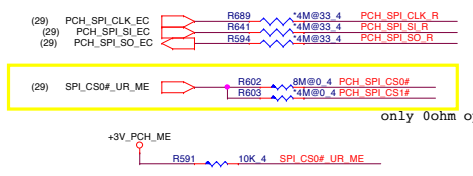
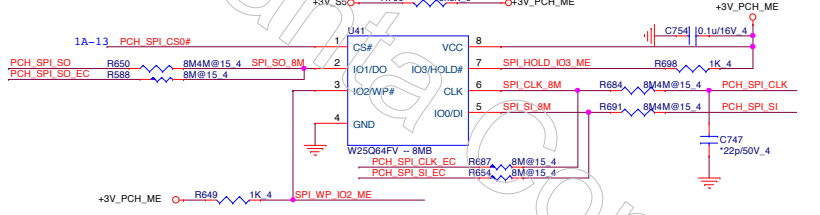




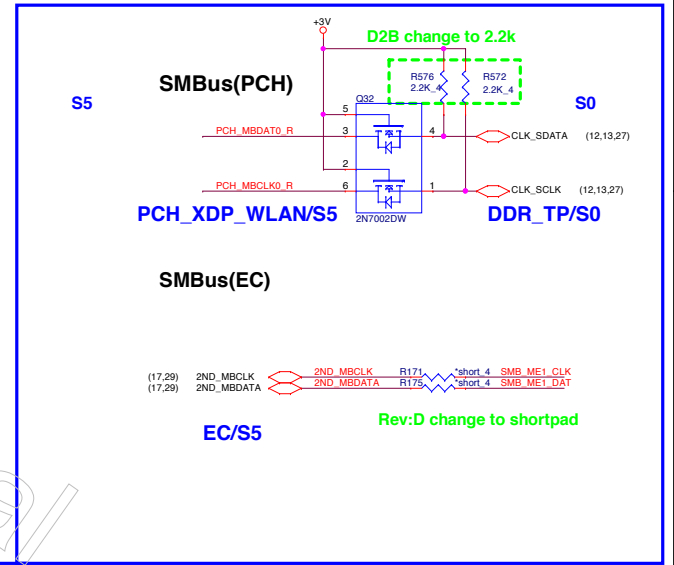
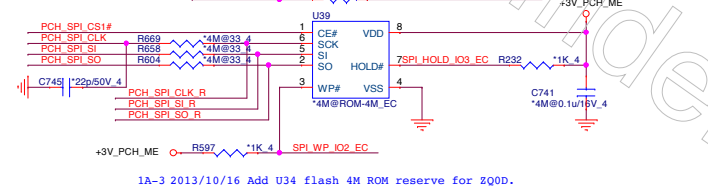
For M.2 wifi module must  
Rev:D change to shortpad

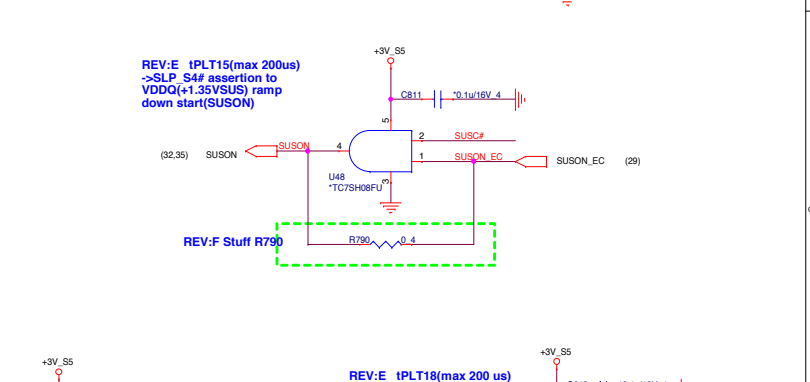
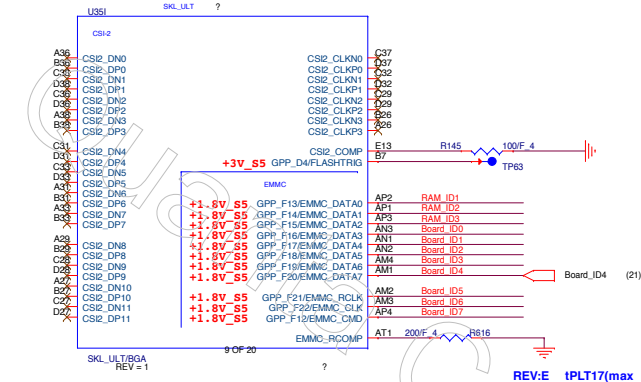
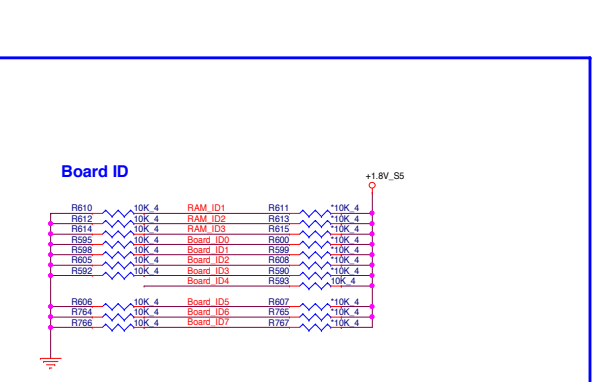
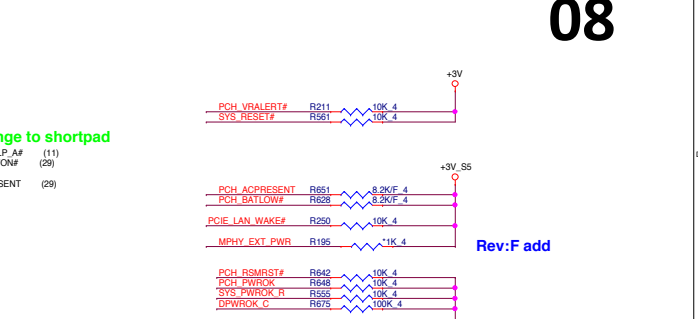
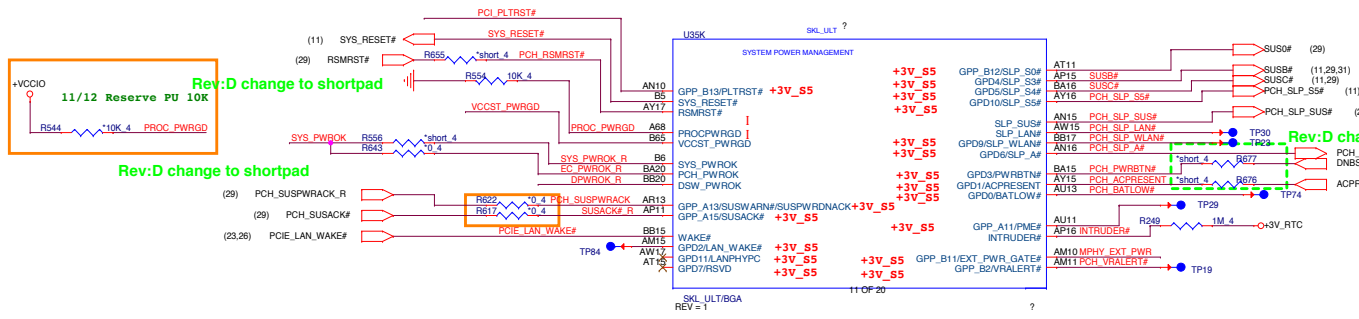
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZNOQ00	GD25B64CSIGR

**PCH SPI ROM(8M+4M)**  
15ohm CS01502JB12  
33ohm CS03302JB29

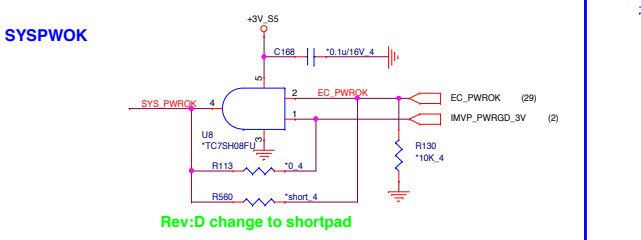
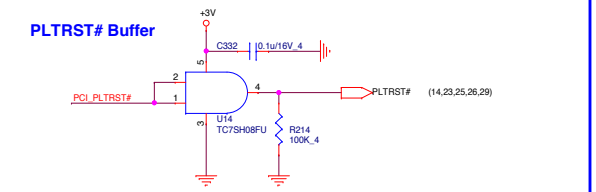
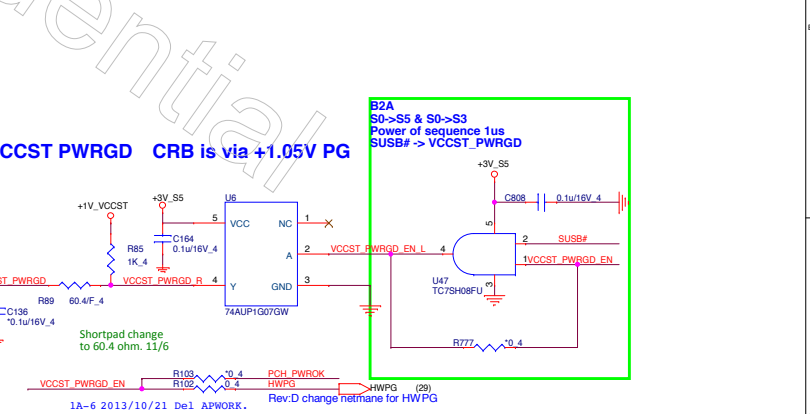
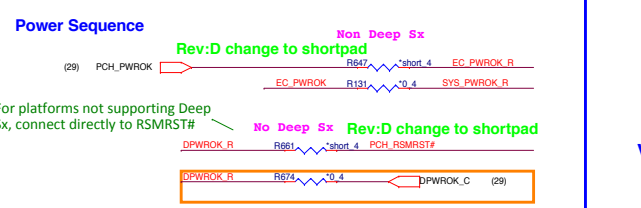


**3.3K is original and for no support fast read function**

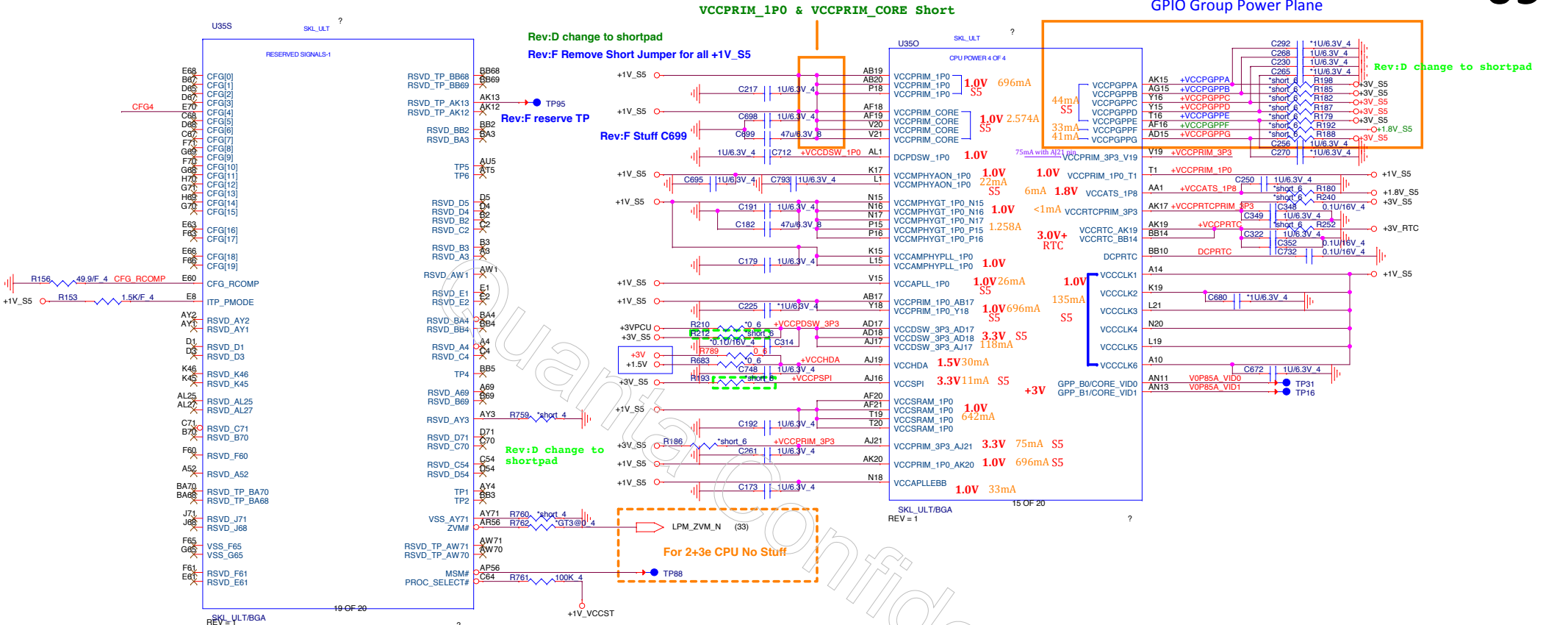




	Low	High		Low	High
BOARD_ID0	VRAM 2GB	VRAM 4GB	BOARD_ID5	Realtek Audio codec	CPU DSP
BOARD_ID1	Non IOAC	IOAC	BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID2	No G-sensor	G-sensor	BOARD_ID7	Reserved (Default)	Reserve
BOARD_ID3	No TPM	TPM			
BOARD_ID4	No touch panel	touch panel			

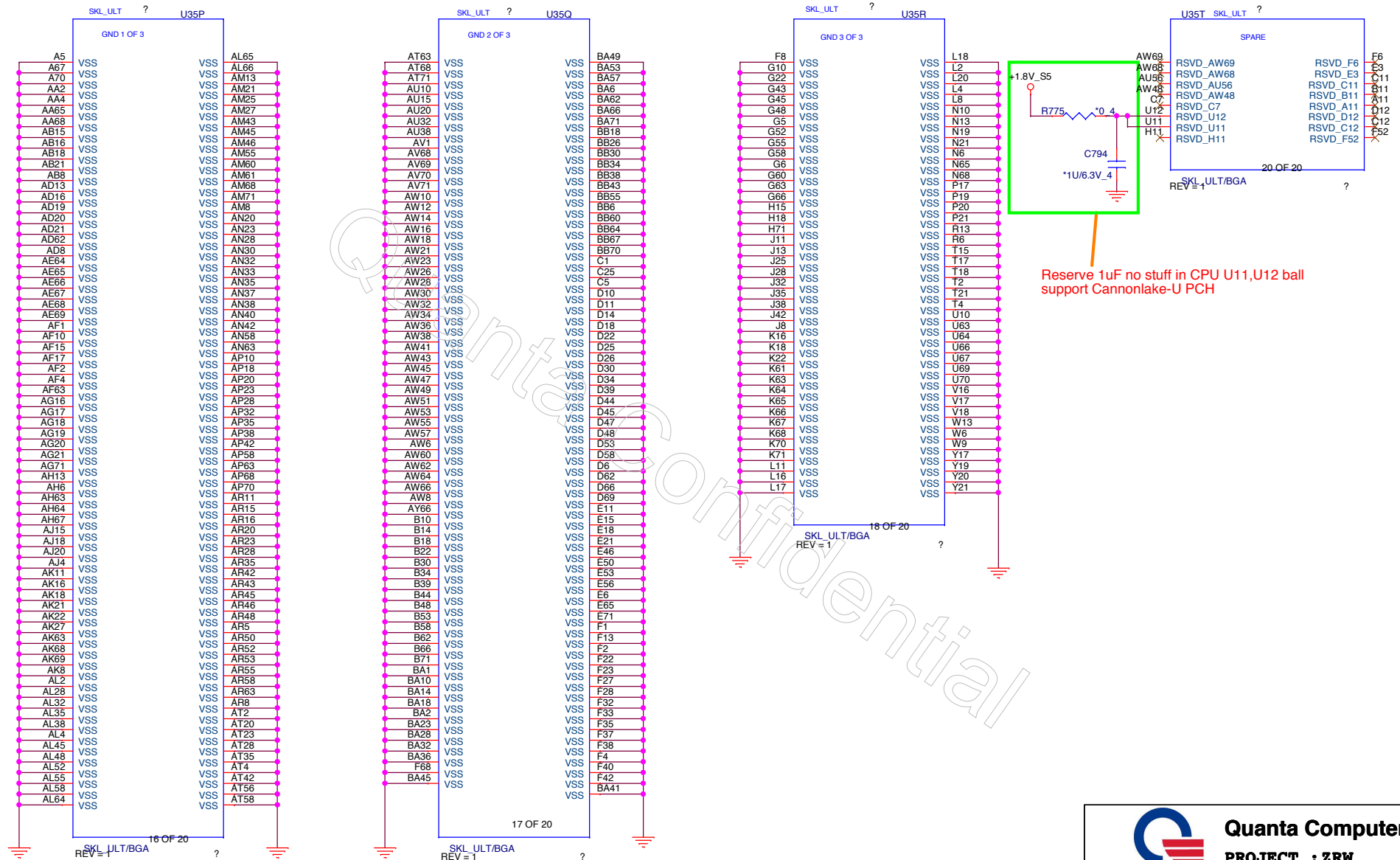






Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (IPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation (IPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (IPU 3K) 0 = *Enabled	CFG4 R548 1K 4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediately follow RESET# de-assertion (IPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		

# Skylake ULT (GND)



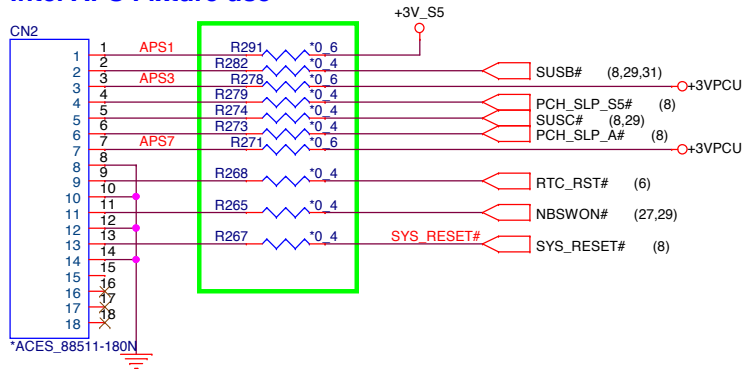
**Quanta Computer Inc.**  
**PROJECT : ZRW**

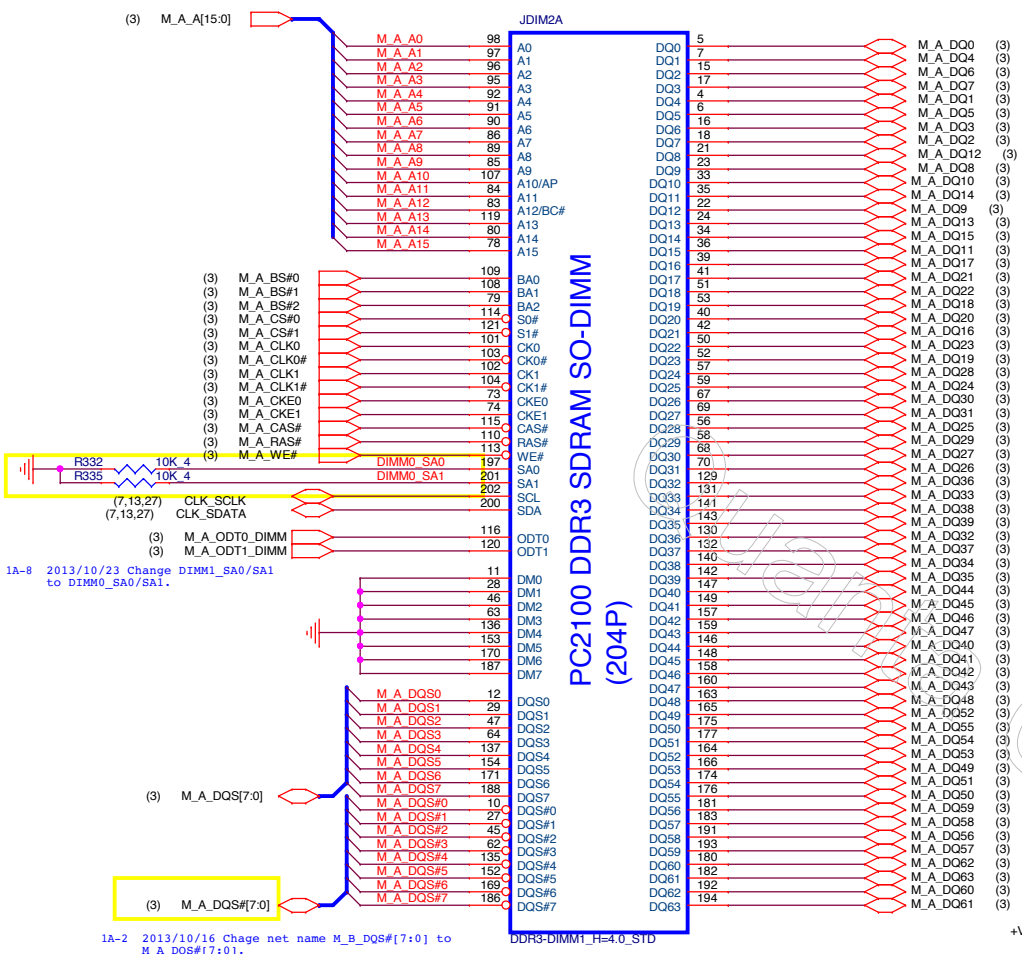
Size	Document Number	Rev
	<b>Skylake 10/17/18 (GND)</b>	3A
Date:	Monday, July 20, 2015	Sheet 10 of 48

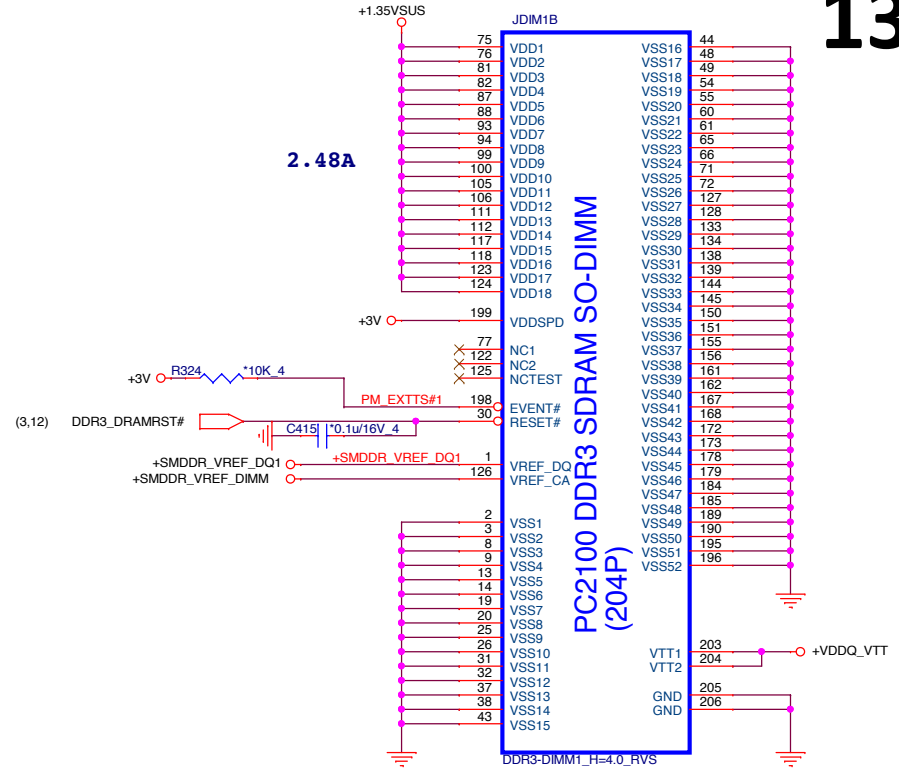
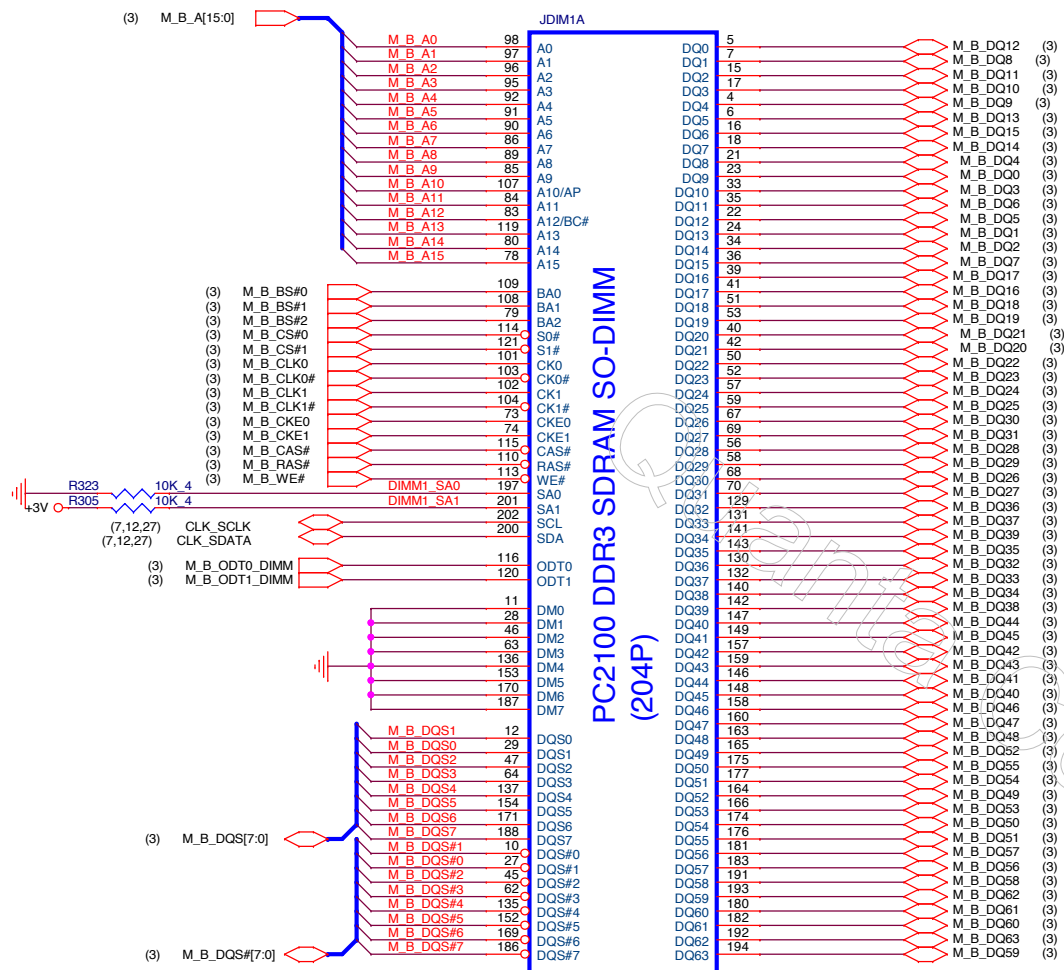
Quanta Confidential



Intel APS Fixture use

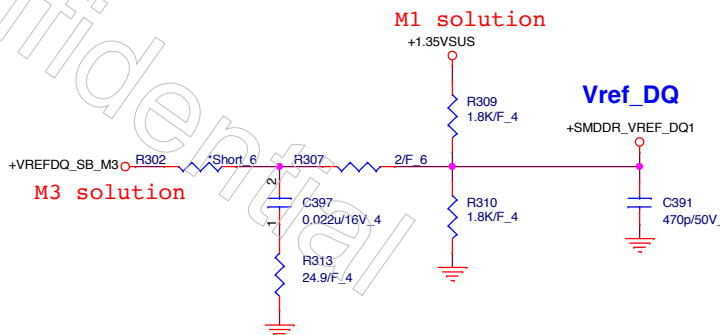




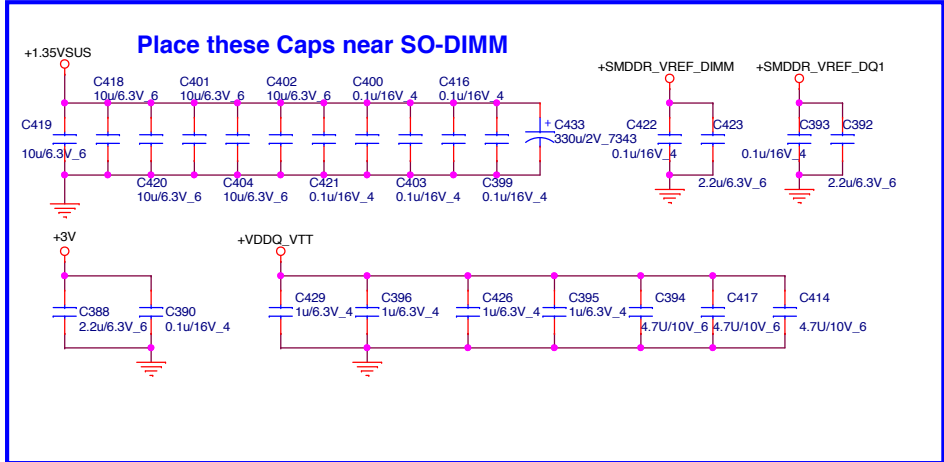


1A-22013/10/16 Swap M\_B\_DQS2/M\_B\_DQS3 and swap M\_B\_DQS#2/M\_B\_DQS#3.

DDR3-DIMM1\_H=4.0\_RVS



	SA1	SA0
CHA	0	0
CHB	1	0

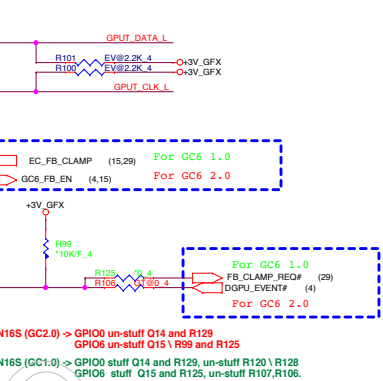
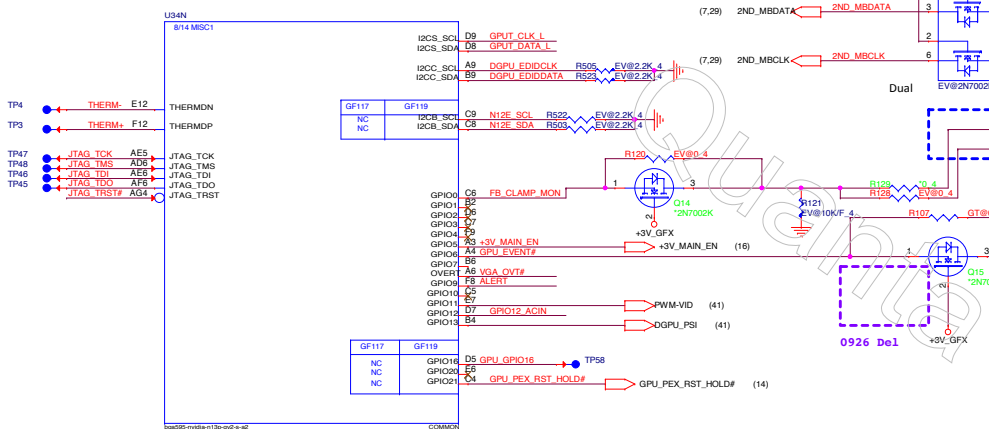
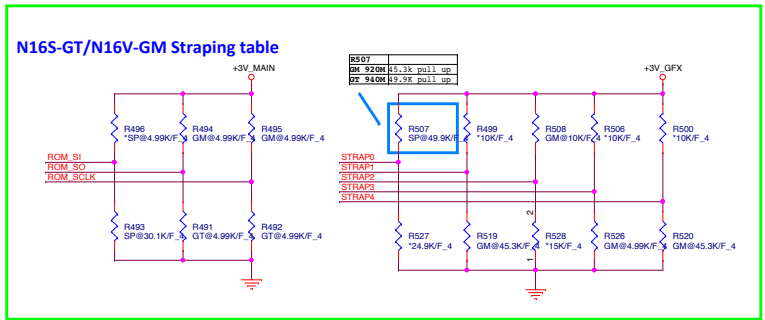
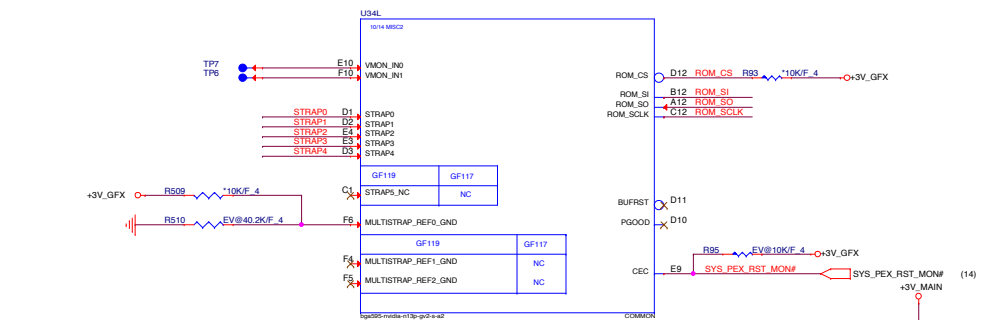








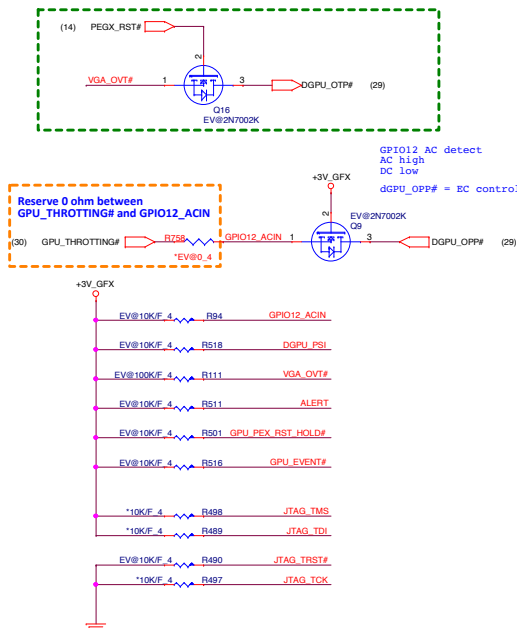




**N16S-GT DID=0x1347 [940M]**  
 ROM\_SCLK = Stuff 4.99K pull down  
 ROM\_SO = Stuff 4.99K pull down  
 STRAP0 = Stuff 49.9K pull up  
 STRAP1 = NC  
 STRAP2 = NC  
 STRAP3 = NC  
 STRAP4 = NC  
 ROM\_SI = VRAM Configuration follow below table

**N16V-GM DID=0x1299 [920M]**  
 ROM\_SCLK = Stuff 4.99K pull up  
 ROM\_SO = Stuff 4.99K pull up  
 STRAP0 = Stuff 45.3K pull up. (EDID Panel)  
 STRAP1 = Stuff 45.3K pull down. (Gen3 support)  
 STRAP2 = Stuff 10K pull up. (DID 0x1299)  
 STRAP3 = Stuff 4.99K pull down. (No display out)  
 STRAP4 = Stuff 45.3K pull down. (Gen3/max speed)  
 ROM\_SI = VRAM Configuration follow below table

Note: GC6 2.0 is supported by N16x GPU in the GB2B, GB4B-12B, and GB3B-25B packages.



**GPIO ASSIGNMENTS**

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

**N16S-GT/N16V-GM Strapping table**

**ROM\_SI N16S-GT [940M]**

- 2G Hynix 128Mx16 -> 34.8K PD
- 2G Micron 128Mx16 -> 45.3K PD
- 2G Samsung 128Mx16 -> 4.99K PU
- 4G Hynix 256Mx16 -> 30.1K PU Single Rank
- 4G Hynix 256Mx16 -> 24.9K PU Dual Rank
- 4G Micron 256Mx16 -> 10K PD
- 4G Samsung 256Mx16 -> 15K PD

**ROM\_SI N16V-GM [920M Single RAM]**

- 2G Hynix 128Mx16 -> 20K PD
- 2G Micron 128Mx16 -> 30.1K PD
- 2G Samsung 128Mx16 -> 34.8K PD
- 4G Micron 256Mx16 -> 10K PD
- 4G Hynix 256Mx16 -> 10K PU
- 4G Samsung 256Mx16 -> 24.9K PD

**Resistor P/N**

- 4.99K -> CS24992FB26
- 10K -> CS31002FB26
- 15K -> CS31502FB24
- 20K -> CS32002FB29
- 24.9K -> CS32492FB16
- 30.1K -> CS33012FB18
- 34.8K -> CS33482FB22
- 45.3K -> CS34532FB18 GM
- 49.9K -> CS34992FB10 GT

**Logical Strap Bit Mapping**

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

**N16S-GM/GT-LP VRAM Configuration Table ROM\_SI**

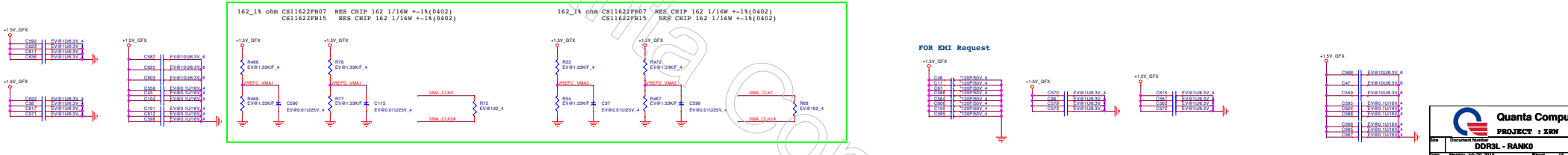
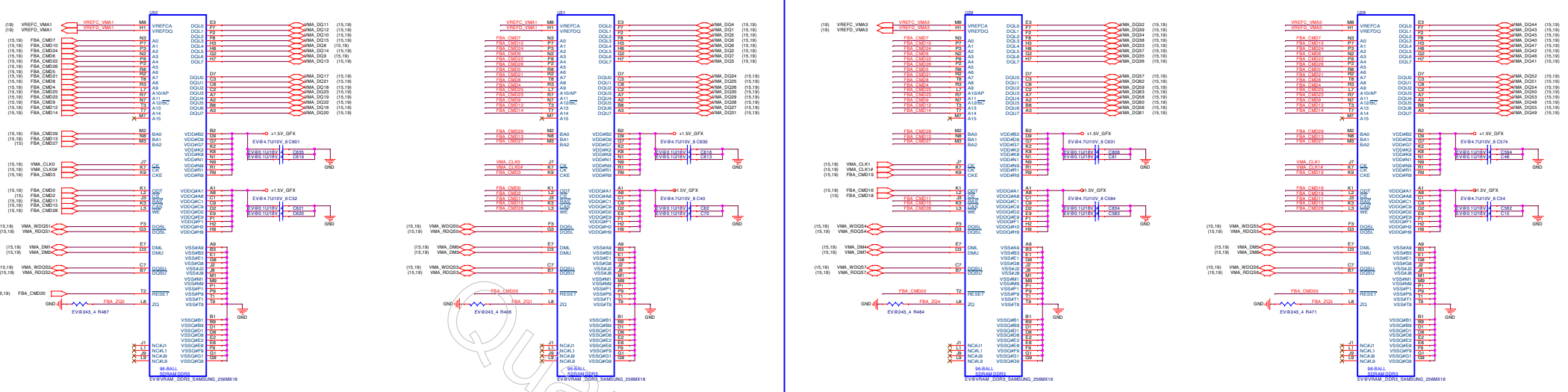
RAMCFG [3:0]	DESCRIPTION	1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0101 0x5	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	HYNIX C-die	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank 2GB
1100 0xC	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	HYNIX C-die	H5TC4G63CFR-N0C	PU 24.9K ohm	AKD5PZDTW03	Dual Rank 4GB
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank Dual Rank
0100 0x2	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	SAMSUNG D-die	K4W4G1646D-BC1A	PD 15K ohm	AKD5PGWT504	Single Rank Dual Rank
0010 0x4	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	SAMSUNG E-die	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT504	Single Rank 2GB
1101 0xD	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	SAMSUNG E-die	K4W4G1646E-BC1A	PU 30.1K ohm	AKD5PGDT504	Dual Rank 4GB

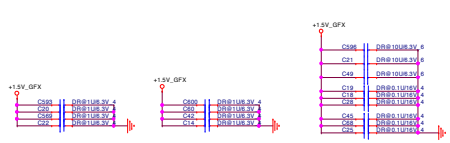
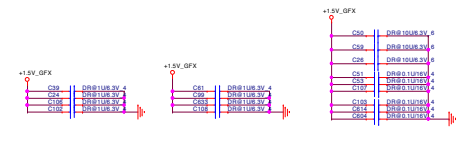
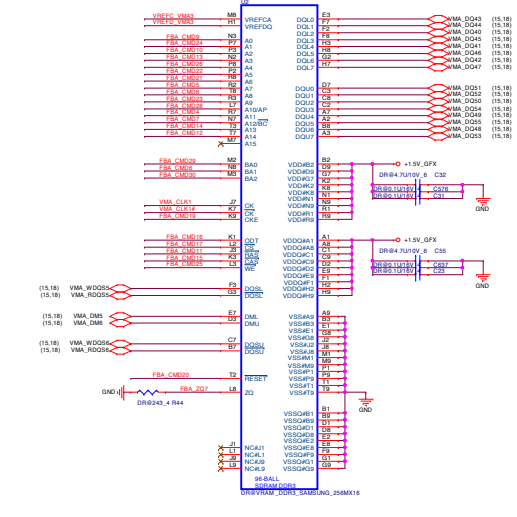
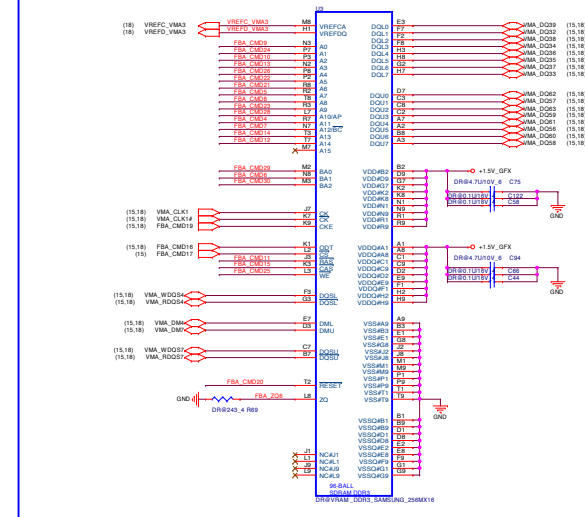
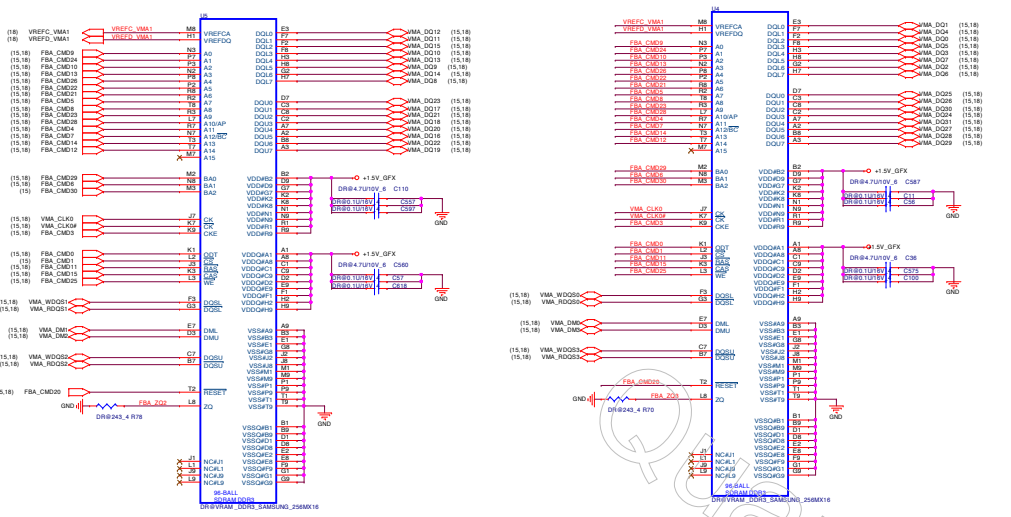
**N16V-GM/GL VRAM Configuration Table ROM\_SI**

RAMCFG [3:0]	DESCRIPTION	1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank or Single Rank stuffing for Dual Rank
1001 0x9	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	HYNIX C-die	H5TC4G63CFR-N0C	PU 10K ohm	AKD5PZDTW03	
0100 0x4	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	SAMSUNG D-die	K4W4G1646D-BC1A	PD 24.9K ohm	AKD5PGWT504	
1010 0xA	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz	256Mx16	SAMSUNG E-die	K4W4G1646E-BC1A	PU 15K ohm	AKD5PGDT504	

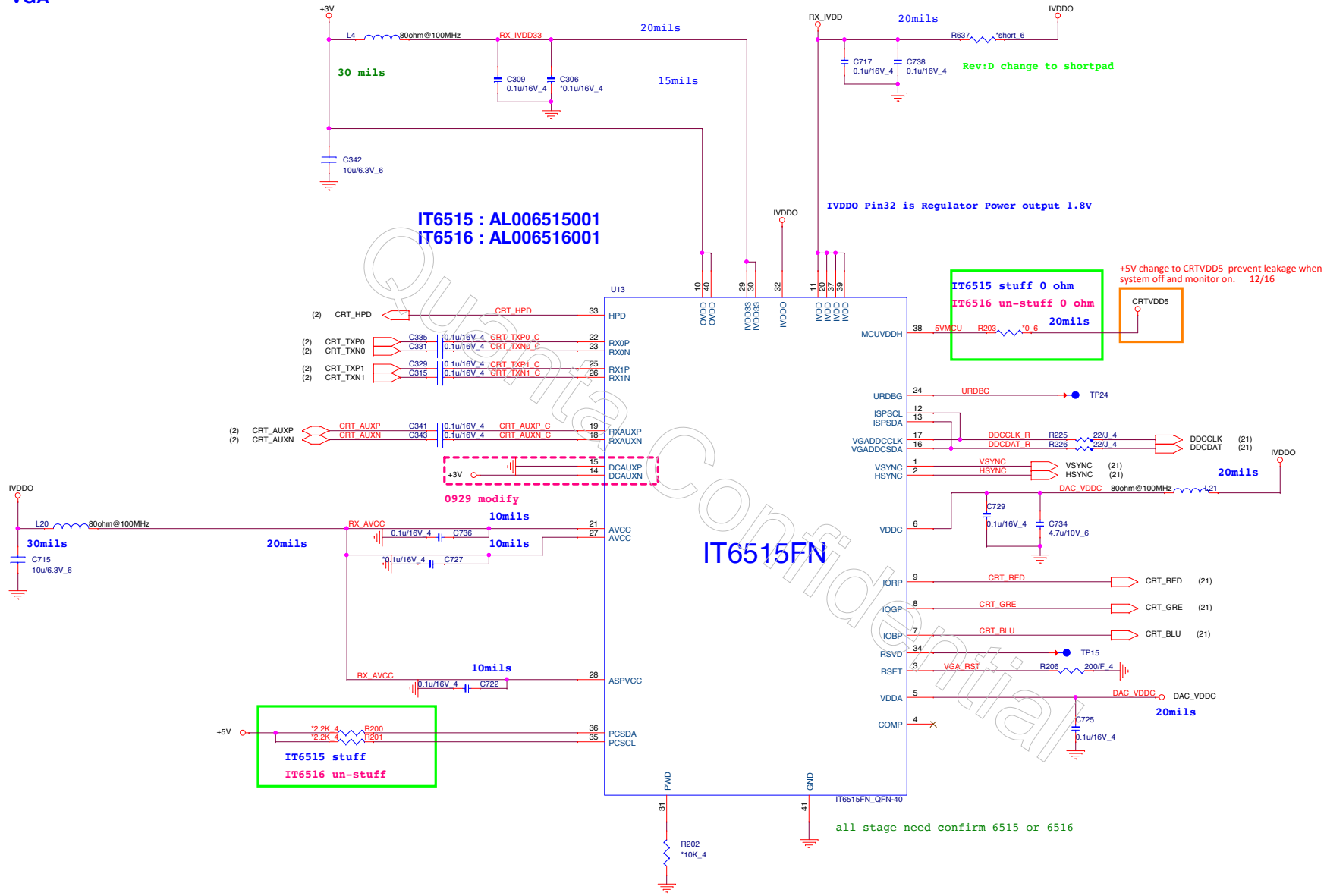
**N16V-GM strap0-3 table**

STRAP0 = Stuff 45.3K pull up. (EDID Panel)  
 STRAP1 = Stuff 45.3K pull down. (Gen3 support)  
 STRAP2 = Stuff 10K pull up. (DID 0x1299)  
 STRAP3 = Stuff 4.99K pull down. (No display out)  
 STRAP4 = Stuff 45.3K pull down. (Gen3/max speed)






DP TO VGA



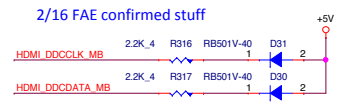
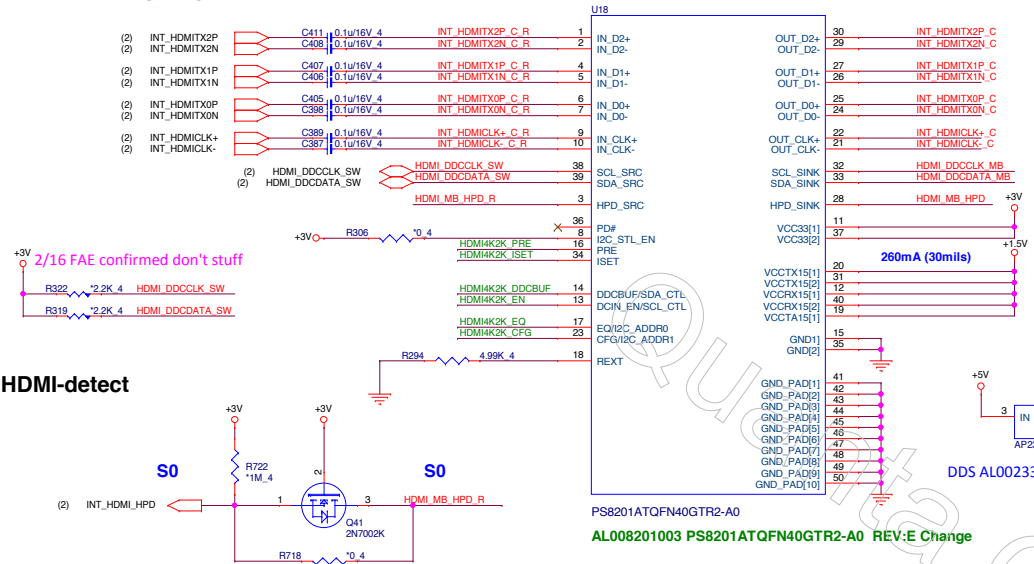
(2,4,6,7,8,9,12,13,14,15,16,21,22,23,24,25,27,28,31,32,35,36,40,41,42) +3V  
 (4,21,22,24,25,27,31,40) +5V

 <b>Quanta Computer Inc.</b> PROJECT : ZRM		
Size	Document Number	Rev
	<b>DP to VGA iT6165</b>	<b>3A</b>
Date:	Monday, July 20, 2015	Sheet 20 of 48

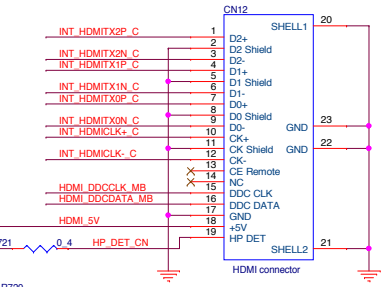


<HDM>

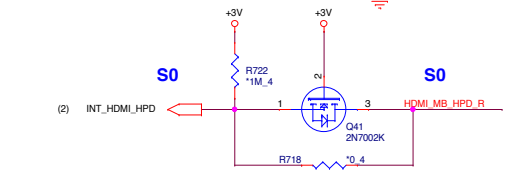
From PCH



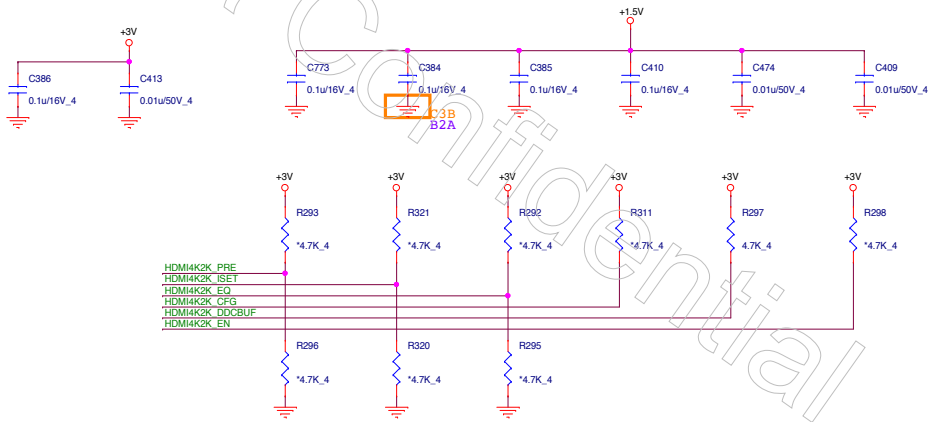
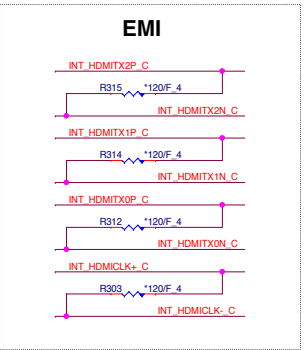
HDMI connector



HDMI-detect



EMI



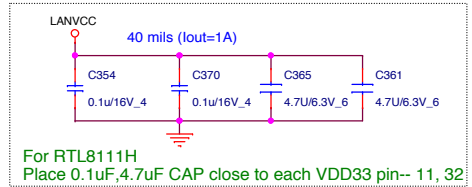
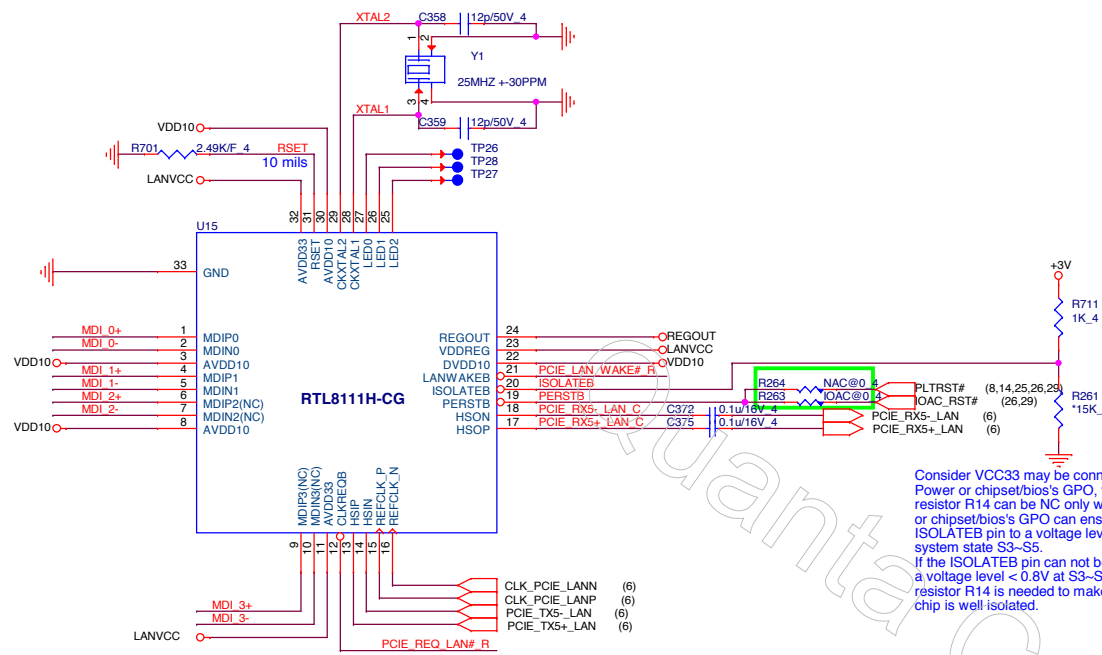
	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC (Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default, AC coupling input
1 (High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A



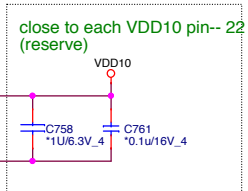
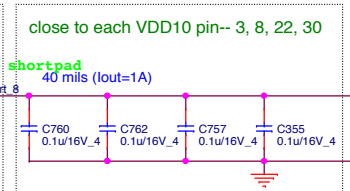
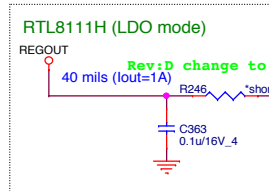
Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

(2,4,6,7,8,9,12,13,14,15,16,20,21,23,24,25,26,27,28,29,31,32,33,35,36,40,41,42)  
(4,20,21,24,25,27,31,40)

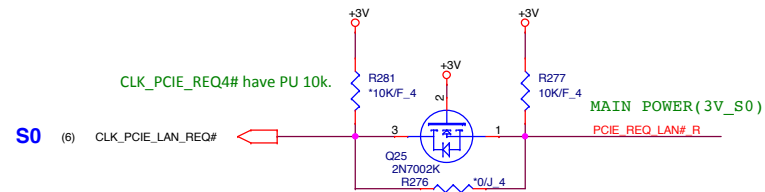


For RTL8111H  
Place 0.1uF,4.7uF CAP close to each VDD33 pin-- 11, 32



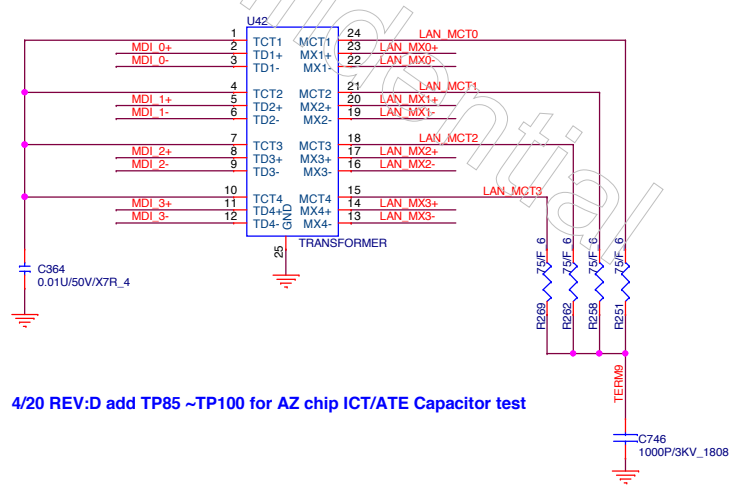
Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3-S5.  
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3-S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

Leakage circuit (MPC)



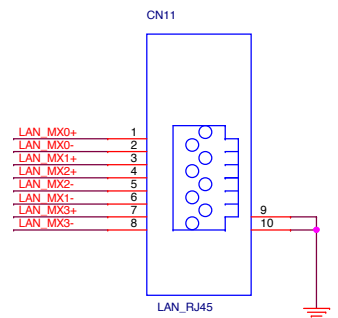
Transformer

Layout: All termination signal should have 30 mil trace

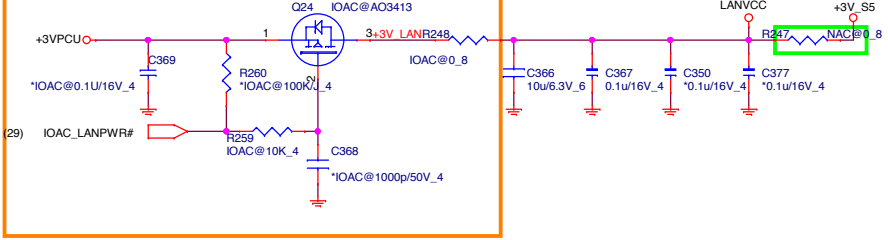


4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

RJ45 Connector



Reserve IOAC No Stuff

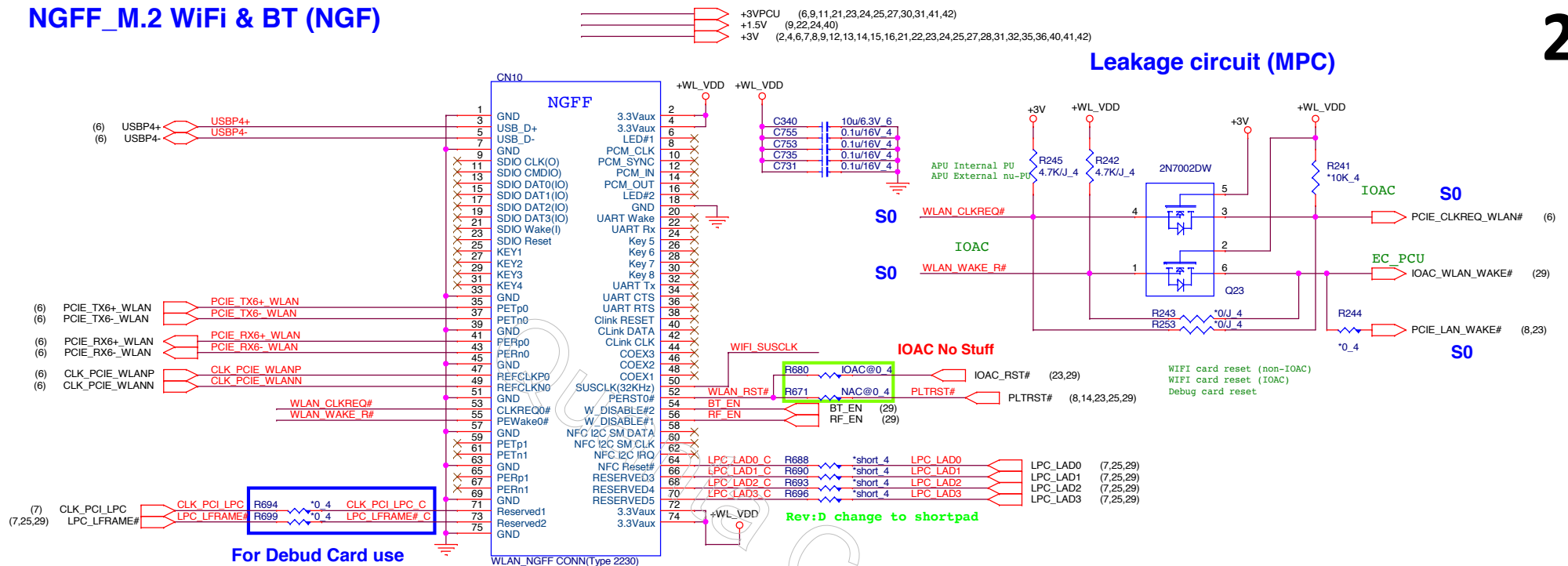








Leakage circuit (MPC)

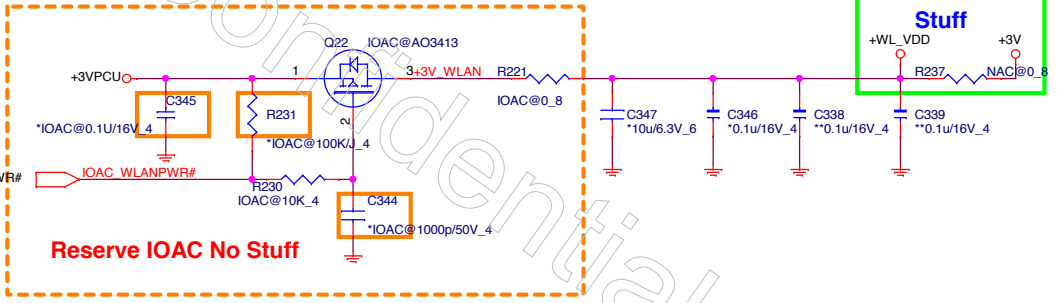


For Debug Card use

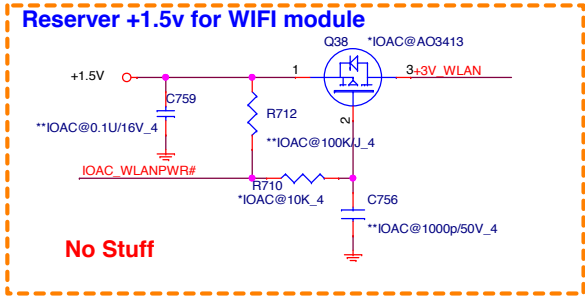
Low	Mini card +3V power enable
High	Mini card +3V power disable

(29) IOAC\_WLANPWR#

Reserve only for Intel module no need to stuff by default 11/24

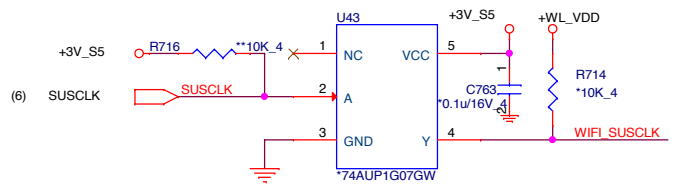


Reserve IOAC No Stuff

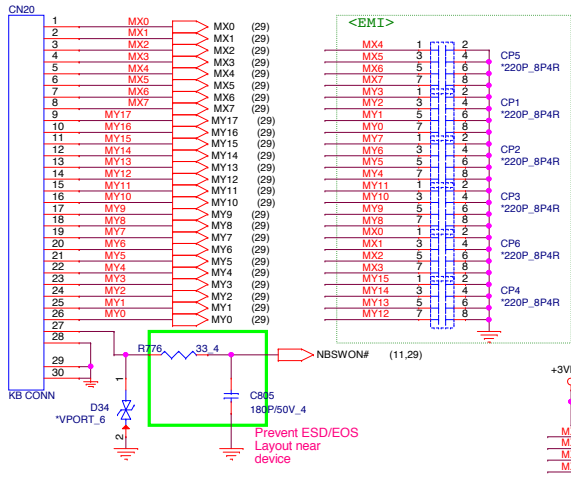


Reserver +1.5v for WIFI module

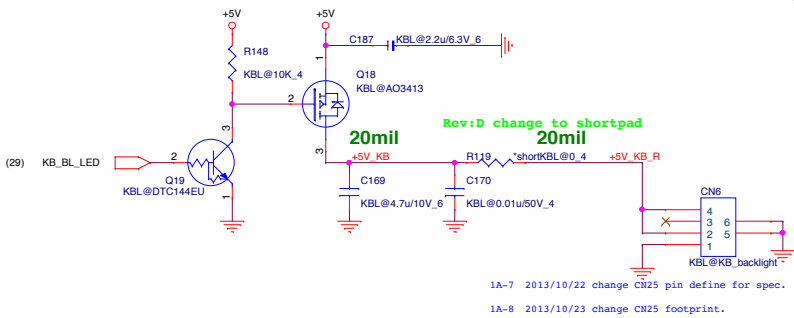
No Stuff



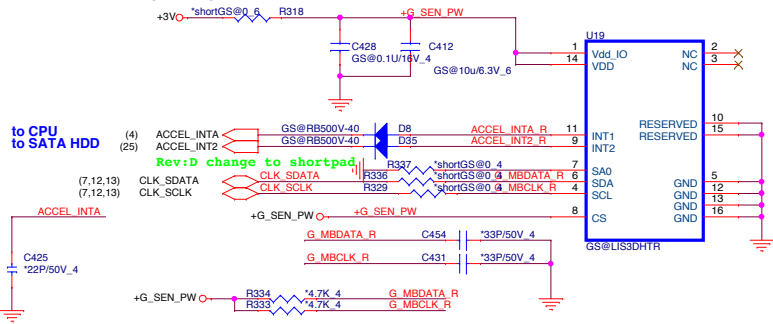
### KEYBOARD (KBC)



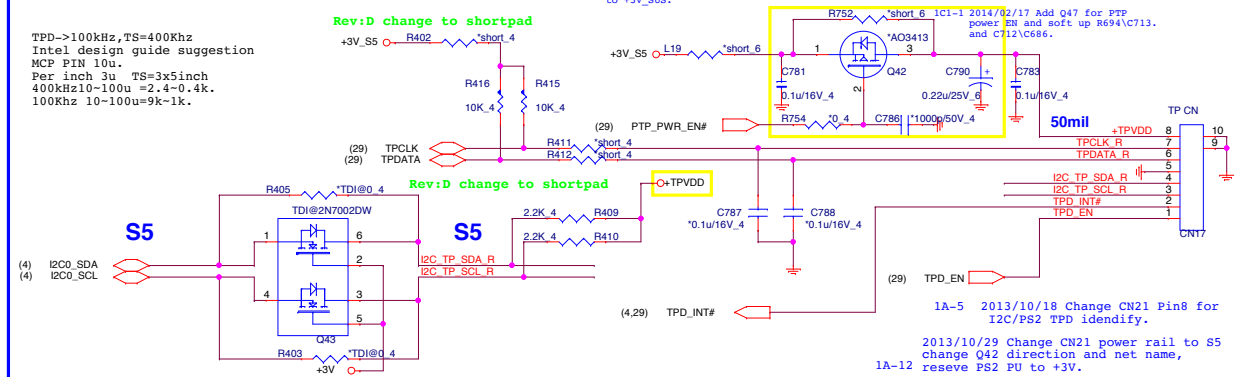
### KB\_BL LED (KBC)



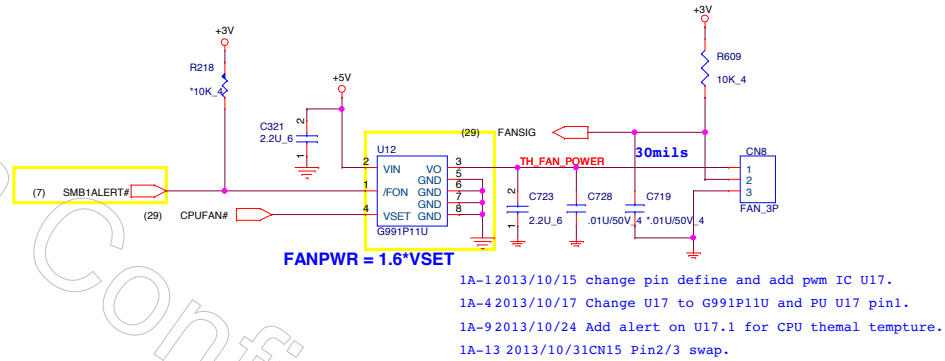
### G-sensor(ACS)



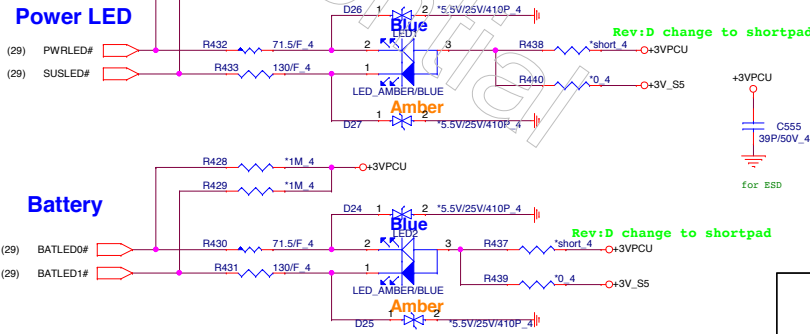
### TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



### CPU FAN (THM)



### POWER LED(UIF)



**Quanta Computer Inc.**  
PROJECT : ZRW

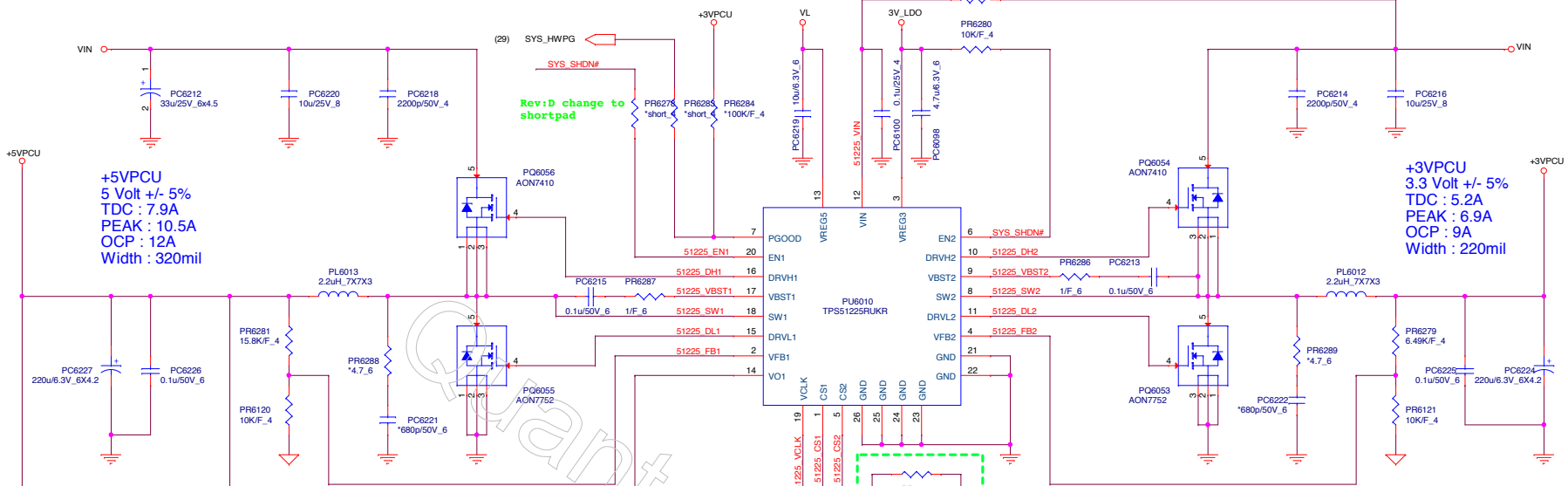
Size	Document Number	Rev
	KB/TP/FAN	3A
Date:	Monday, July 20, 2015	Sheet 27 of 48







(2,40) SYS\_SHDN# ← SYS\_SHDN#

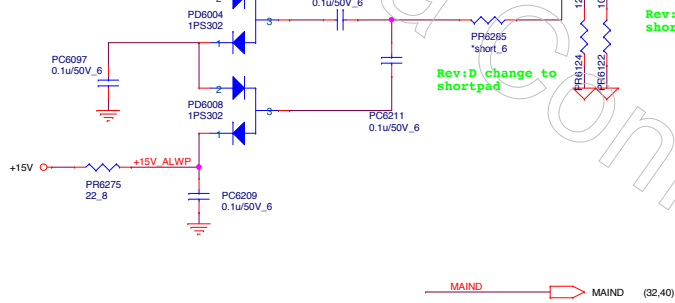


**+5VPCU**  
5 Volt +/- 5%  
TDC : 7.9A  
PEAK : 10.5A  
OCP : 12A  
Width : 320mil

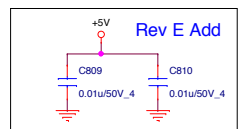
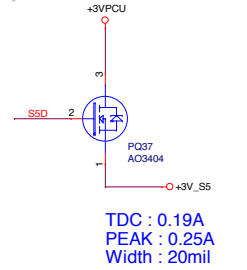
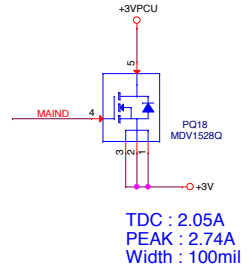
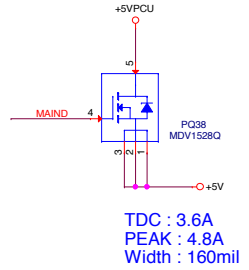
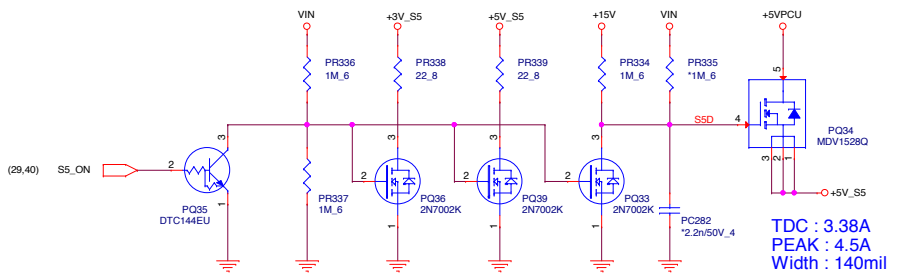
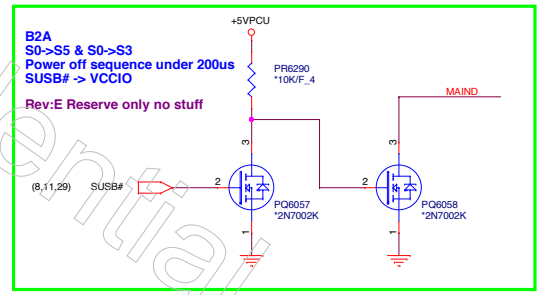
**+3VPCU**  
3.3 Volt +/- 5%  
TDC : 5.2A  
PEAK : 6.9A  
OCP : 9A  
Width : 220mil

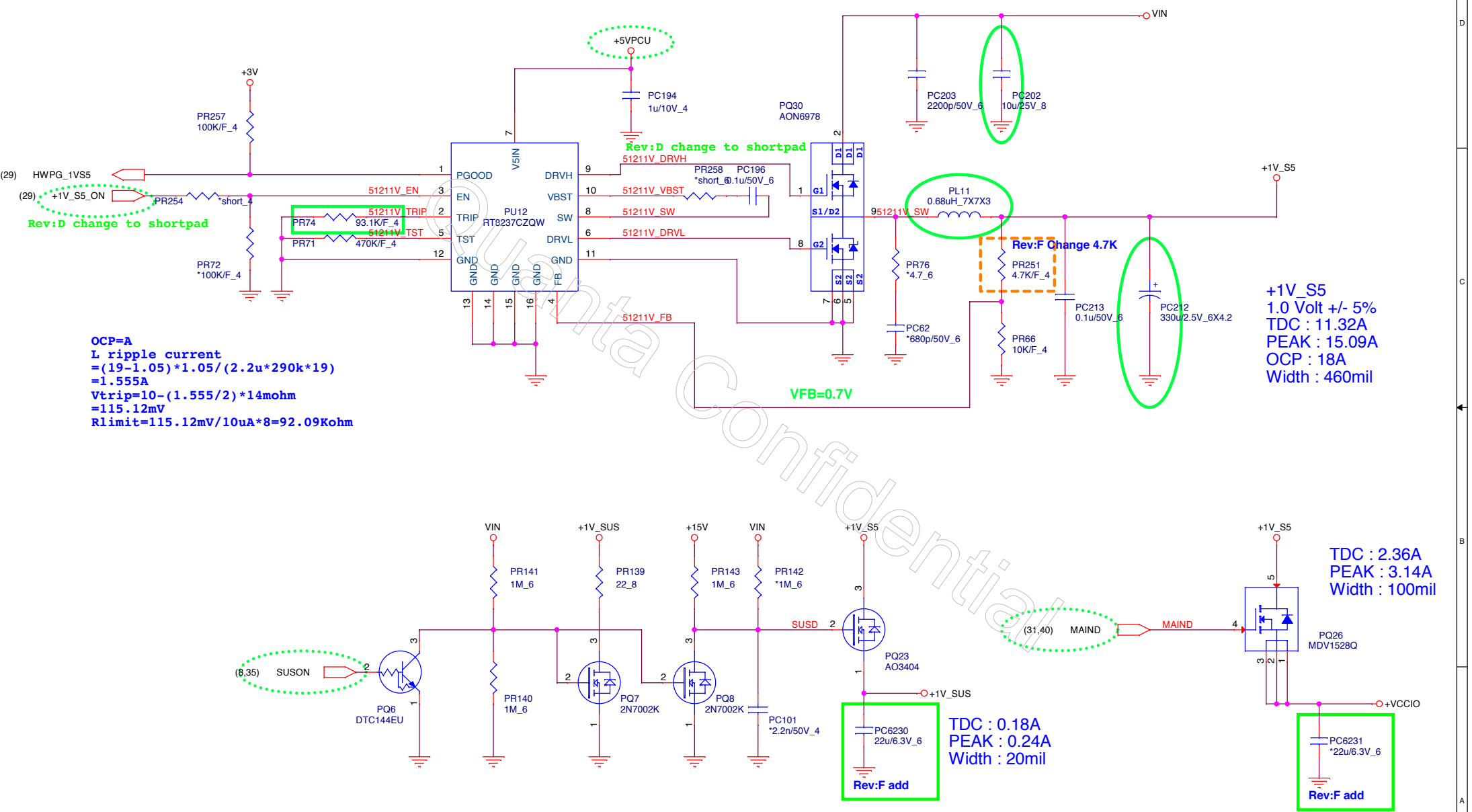
**OCP:12A**  
L(ripple current)  
=(9-3.3)\*5/(2.2u\*0.3M\*9)  
=3.367A  
I<sub>ocp</sub>=12-(3.367/2)=10.316A  
V<sub>th</sub>=(10.316A\*14.5mOhm)+1mV=150.589mV  
R(IIim)=(150.589mV\*8)/10uA  
~120.47K

**OCP:9A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.35M\*9)  
~2.676A  
I<sub>ocp</sub>=9-(2.676/2)=7.661A  
V<sub>th</sub>=(7.661A\*14.5mOhm)+1mV=112.098mV  
R(IIim)=(112.098mV\*8)/10uA  
=89.68K



MAINID (32,40)





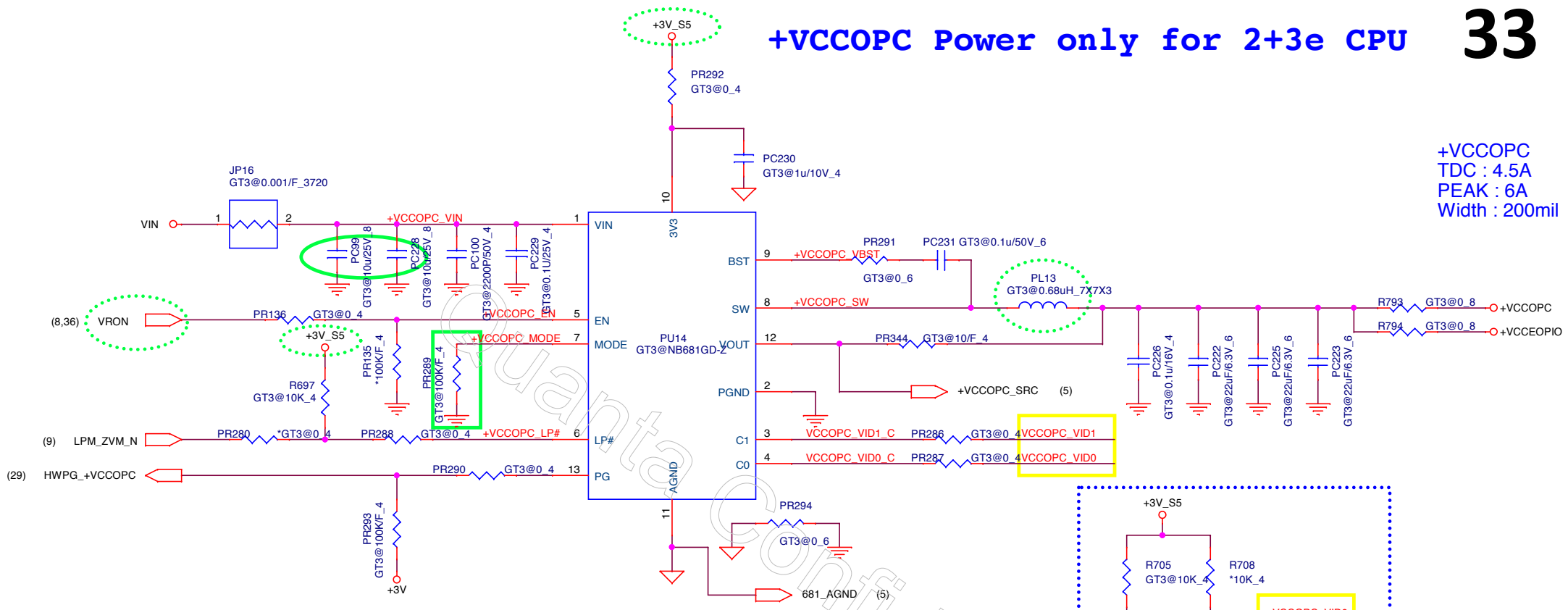
**Quanta Computer Inc.**  
**PROJECT : ZRW**

Size	Document Number	Rev
	<b>+1V_S5 (RT8237CZQW)</b>	3A
Date:	Monday, July 20, 2015	Sheet 32 of 48



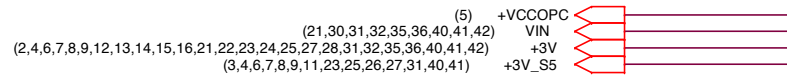
## +VCCOPC Power only for 2+3e CPU

+VCCOPC  
TDC : 4.5A  
PEAK : 6A  
Width : 200mil



Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EPIO
150K	Other

	LP#	C1	C0	Vo
<b>VCCEDRAM</b>	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V



**Quanta Computer Inc.**  
**PROJECT : ZRW**

Size	Document Number <b>+VCCOPC (NB681GD-Z)</b>	Rev 3A
Date:	Monday, July 20, 2015	Sheet 33 of 48

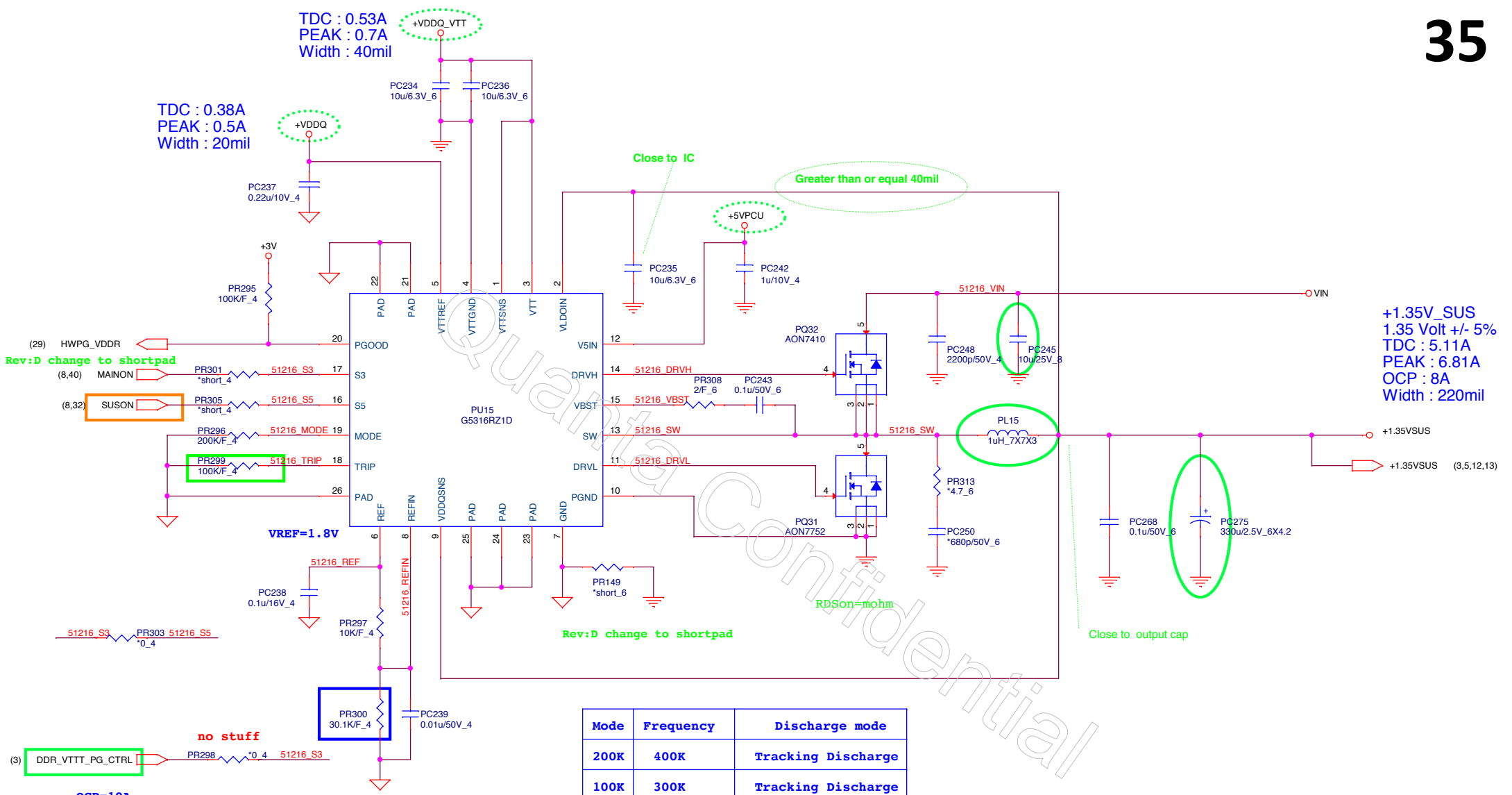
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**PROJECT : ZRW**

Size	Document Number	Rev
	<b>+VCCEOPIO (NB681GD-Z)</b>	<b>2A</b>

Date: Thursday, June 25, 2015 Sheet 34 of 48



TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

+VDDQ\_VTT  
TDC : 0.53A  
PEAK : 0.7A  
Width : 40mil

+1.35V\_SUS  
1.35 Volt +/- 5%  
TDC : 5.11A  
PEAK : 6.81A  
OCP : 8A  
Width : 220mil

Rev:D change to shortpad

Rev:D change to shortpad

Close to output cap

no stuff  
DDR\_VTT\_PG\_CTRL

OCP=10A  
L ripple current  
= (19-1.35) \* 1.35 / (2.2u \* 400k \* 19)  
= 1.425A  
Vtrip=10 - (1.425/2) \* 2.2mohm  
= 20.432mV  
Rlimit=20.432mV / 10uA \* 8 = 16.35kohm

DDR=1.35V  
PR84=10K/F\_4  
PR86=30.1K/F\_4

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

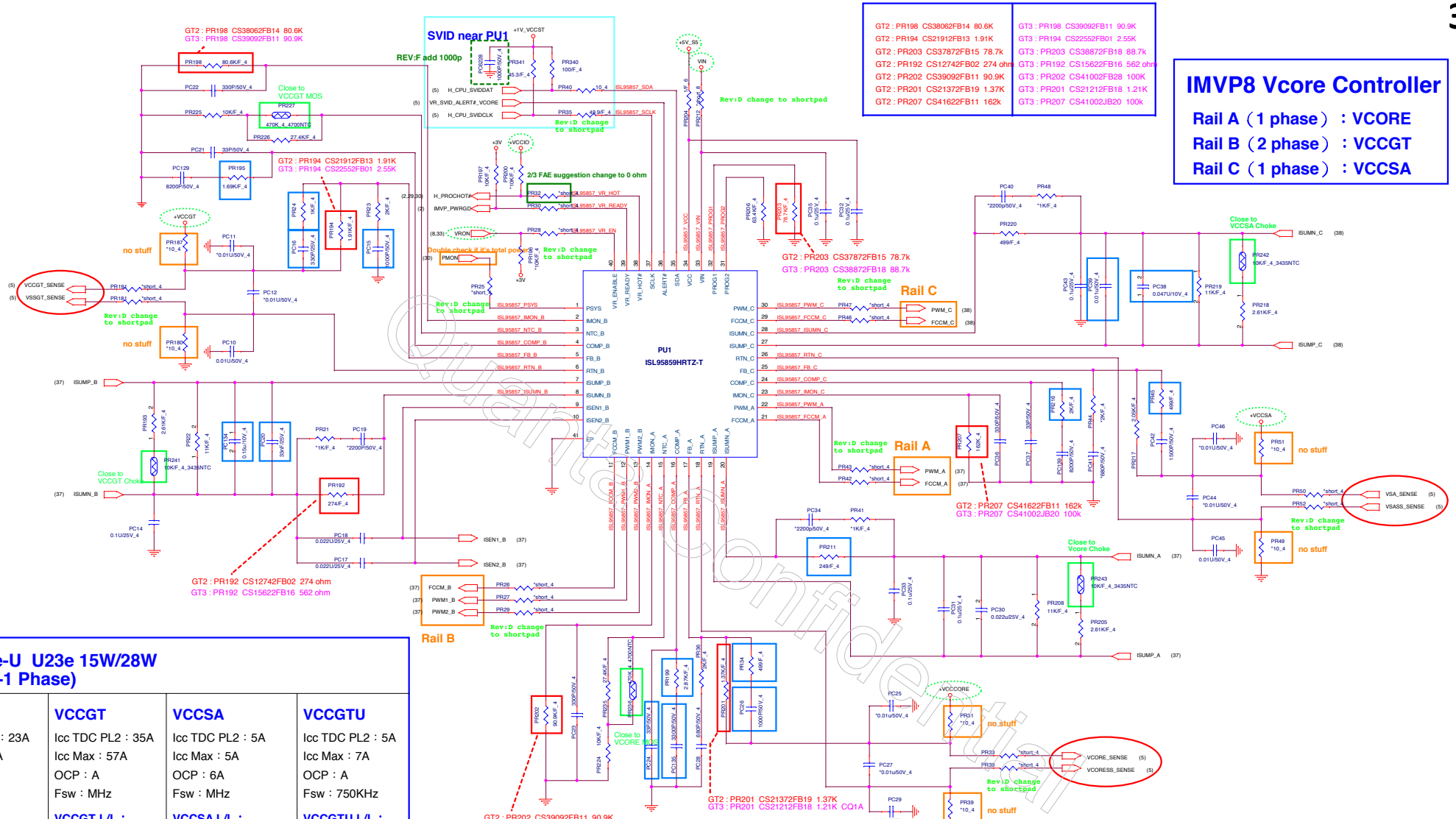
**Quanta Computer Inc.**  
PROJECT : ZRW

Size Document Number Rev 3A  
DDR 1.35V (G5316RZ1D)

Date: Monday, July 20, 2015 Sheet 35 of 48

# IMVP8 Vcore Controller

Rail A (1 phase) : VCORE  
 Rail B (2 phase) : VCCGT  
 Rail C (1 phase) : VCCSA



Skylake-U U23e 15W/28W (1+2+1+1 Phase)			
<b>VCORE</b>	<b>VCCGT</b>	<b>VCCSA</b>	<b>VCCGTU</b>
Icc TDC PL2 : 23A	Icc TDC PL2 : 35A	Icc TDC PL2 : 5A	Icc TDC PL2 : 5A
Icc Max : 29A	Icc Max : 57A	Icc Max : 5A	Icc Max : 7A
OCP : 35A	OCP : A	OCP : 6A	OCP : A
Fsw : MHz	Fsw : MHz	Fsw : MHz	Fsw : 750KHz
<b>VCORE L/L :</b>	<b>VCCGT L/L :</b>	<b>VCCSA L/L :</b>	<b>VCCGTU L/L :</b>
R_DC_LL : 2.1mV/A	R_DC_LL : 2mV/A	R_DC_LL : 10.3mV/A	R_DC_LL : 6mV/A
R_AC_LL : 2.1mV/A	R_AC_LL : 2mV/A	R_AC_LL : 10.3mV/A	R_AC_LL : 6mV/A

GT2 : PR198 CS38062FB14 80.6K	GT3 : PR198 CS39092FB11 90.9K
GT2 : PR194 CS21912FB13 1.91K	GT3 : PR194 CS22552FB01 2.55K
GT2 : PR203 CS37872FB15 78.7K	GT3 : PR203 CS38872FB18 88.7K
GT2 : PR192 CS12742FB02 274 ohm	GT3 : PR192 CS15622FB16 562 ohm
GT2 : PR202 CS39092FB11 90.9K	GT3 : PR202 CS41002FB28 100K
GT2 : PR201 CS21372FB19 1.37K	GT3 : PR201 CS21212FB18 1.21K
GT2 : PR207 CS41622FB11 162K	GT3 : PR207 CS41002JB20 100K

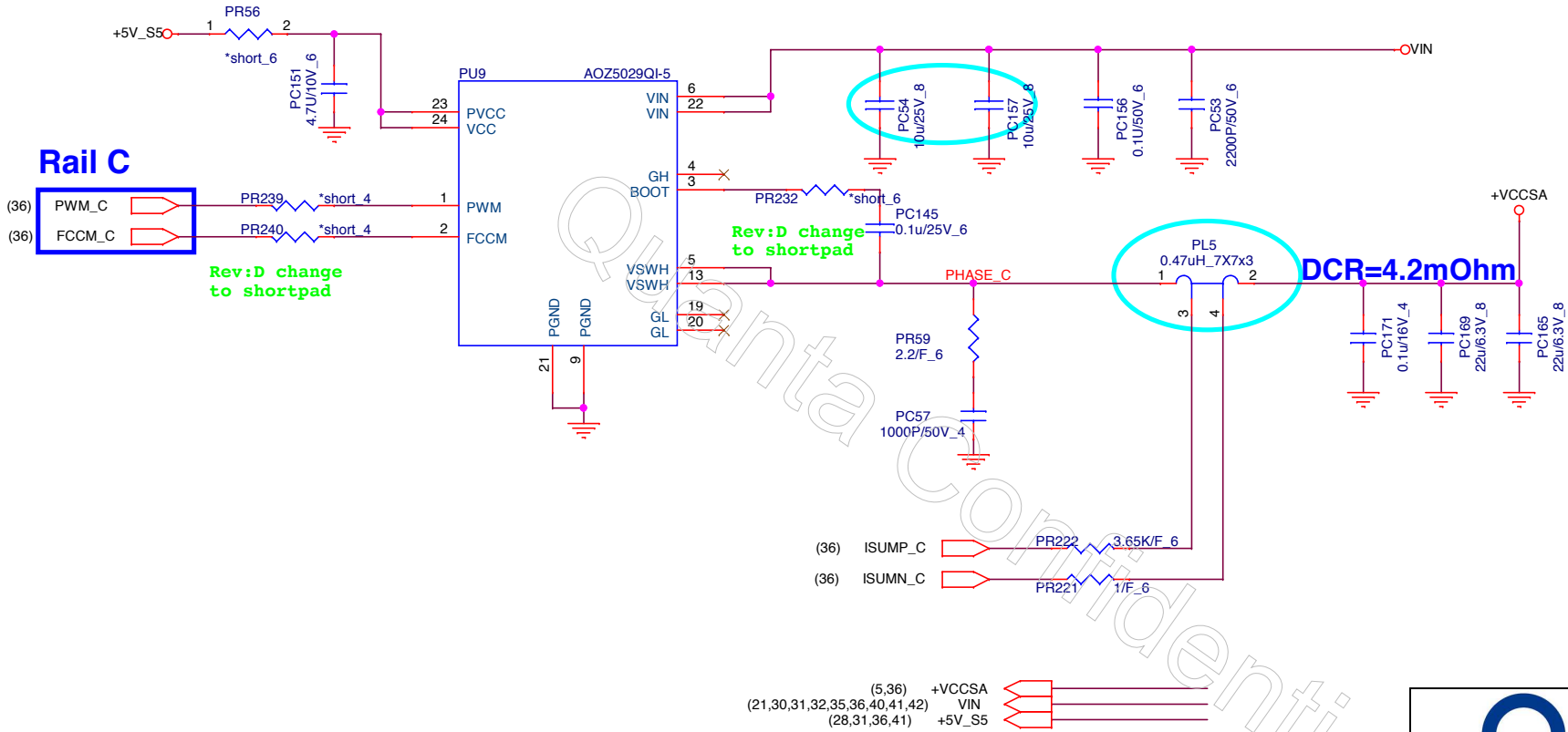


Rev:D change to shortpad

### Rail C

Rev:D change to shortpad

DCR=4.2mOhm



**VCCSA**


Icc TDC PL2 : 5A  
 Icc Max : 5A  
 OCP : 6A  
 Fsw : 800KHz

**VCCSA L/L :**  
 R\_DC\_LL : 10.3mV/A  
 R\_AC\_LL : 10.3mV/A

**Quanta Computer Inc.**  
**PROJECT : ZRW**

Size	Document Number	Rev
	<b>VCCSA (ISL95857HRTZ-T)</b>	3A
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		<b>Quanta Computer Inc.</b>
		<b>PROJECT : ZRW</b>
Size	Document Number	Rev
	<b>+VCCGTX (ISL95853HRZ-T)</b>	<b>2A</b>
Date:	Thursday, June 25, 2015	Sheet 39 of 48

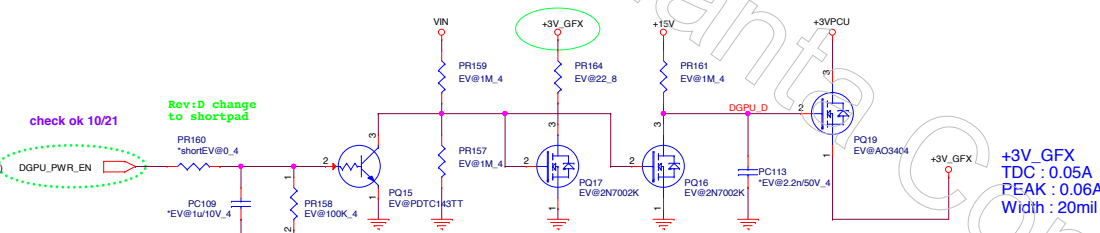
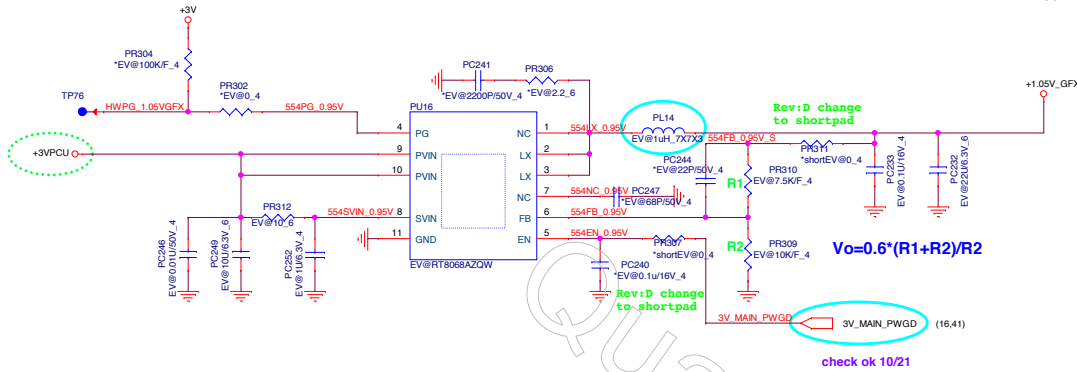






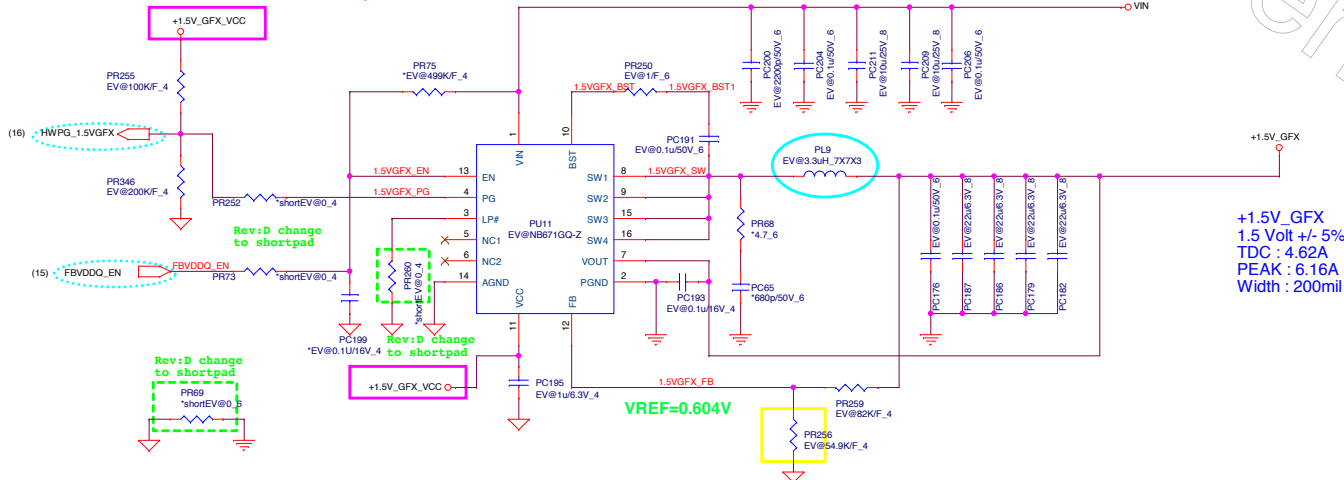
(14,15,16) +1.05V\_GFX  
(14,16,17,29) +3V\_GFX

+1.05V\_GFX  
TDC : 1.57A  
PEAK : 2.09A  
Width : 80mil



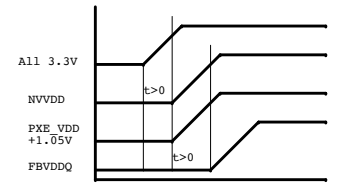
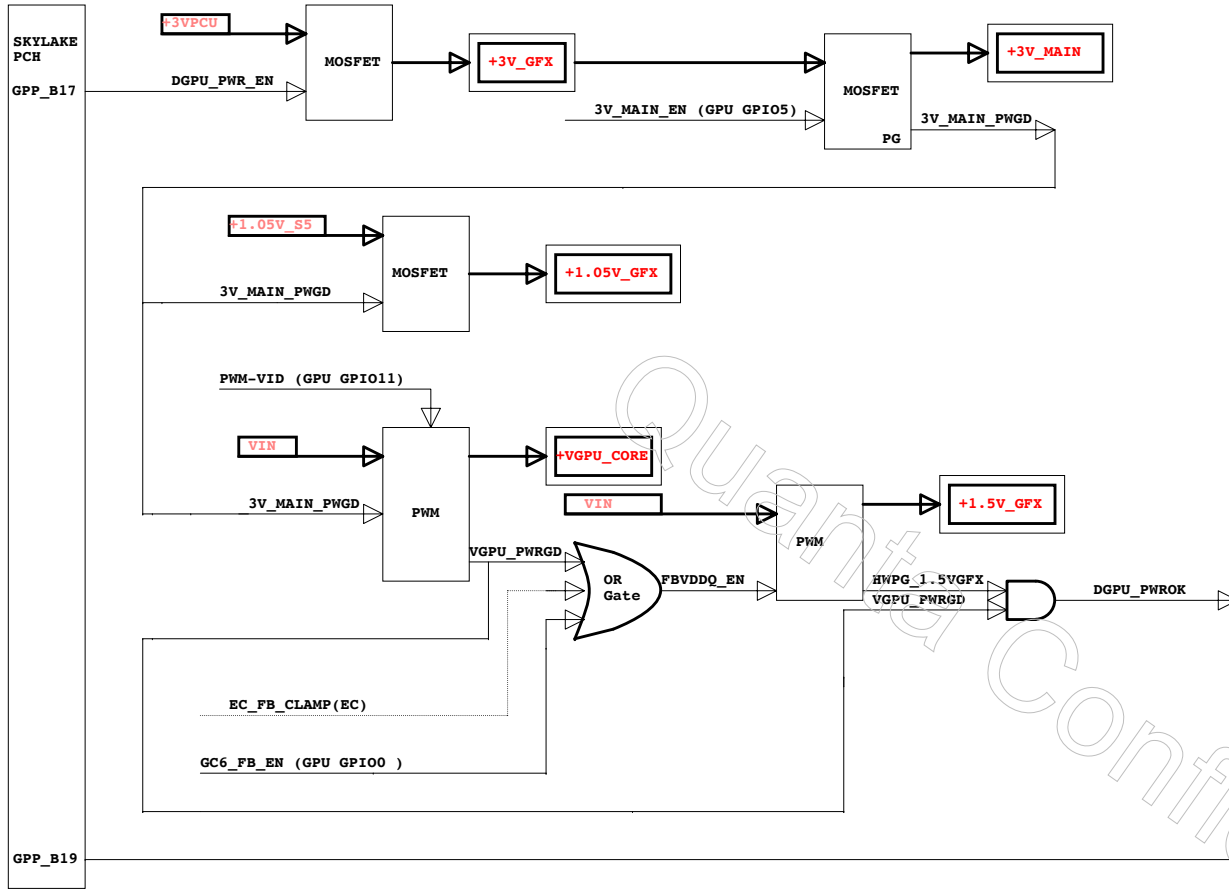
+3V\_GFX  
TDC : 0.05A  
PEAK : 0.06A  
Width : 20mil

Note: HWP\_G\_1.5V\_GFX need PU 100k to MPS NB671 pin11



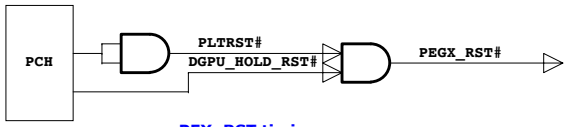
+1.5V\_GFX  
1.5 Volt +/- 5%  
TDC : 4.62A  
PEAK : 6.16A  
Width : 200mil

VGA power up sequence

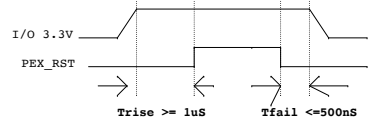


N15x Power on sequence  
 Notes: -All 3.3V includes all rails powered at 3.3V  
 -PEX\_VDD 1.05V includes all rails that are shared

VGA Reset

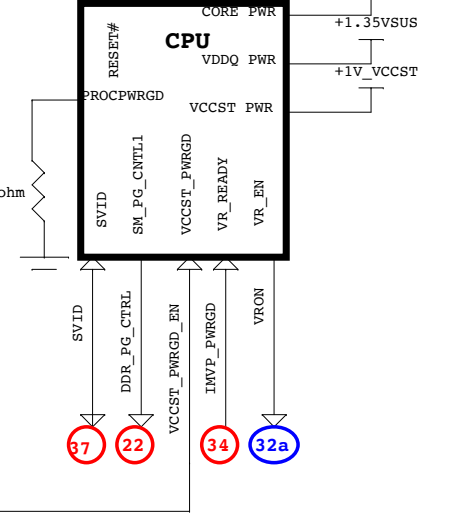
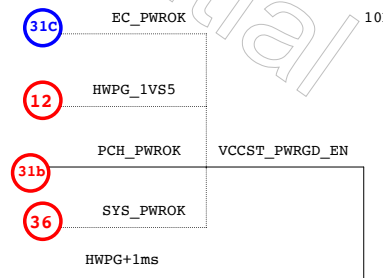
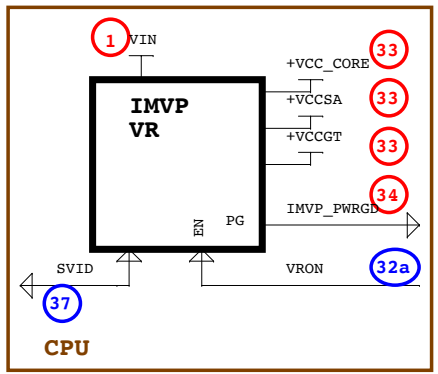
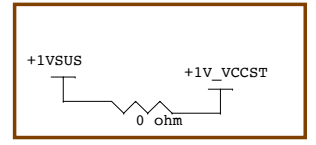
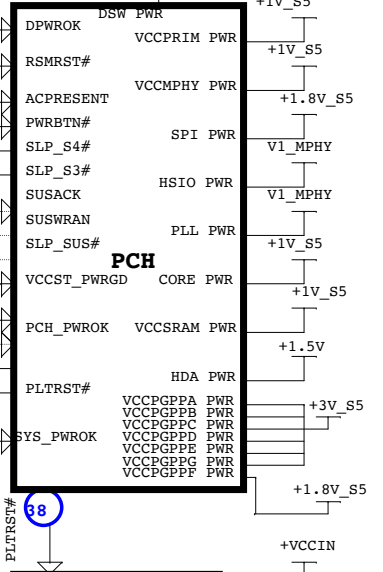
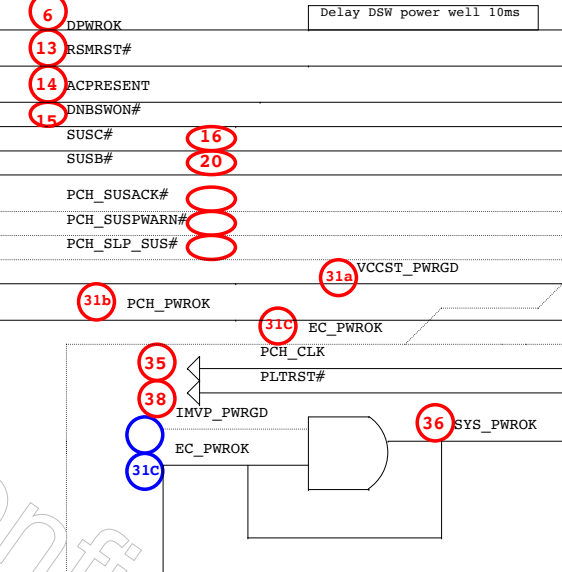
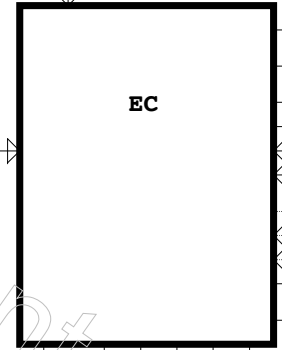
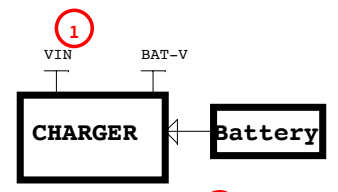
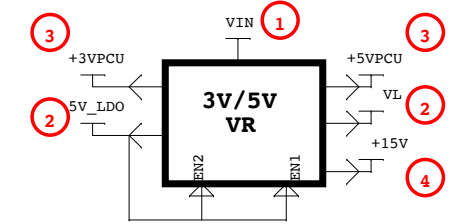
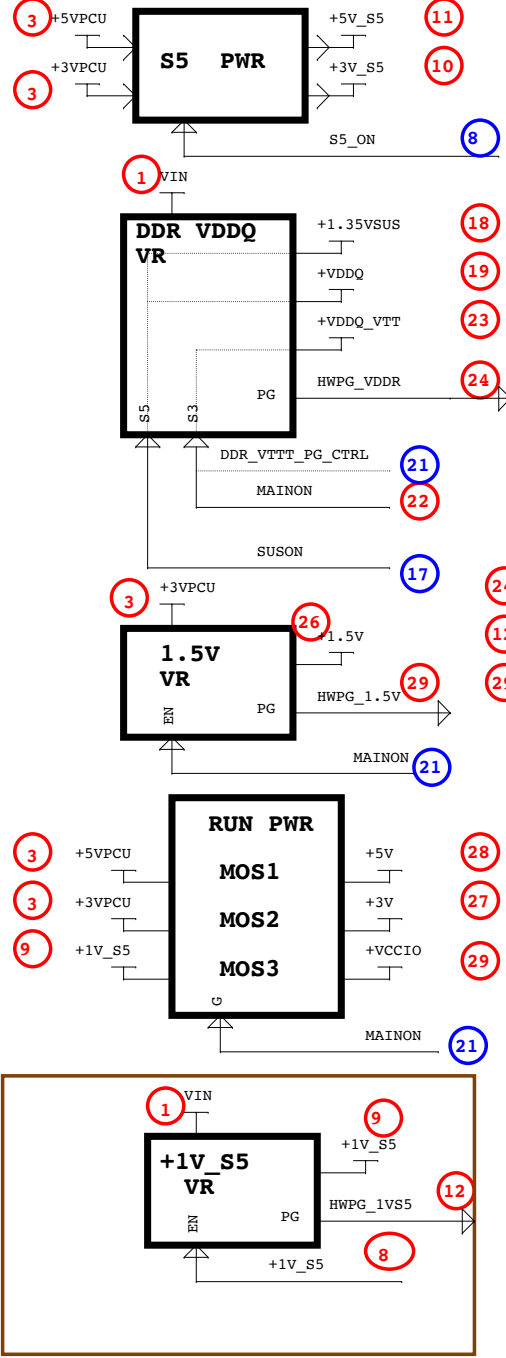


PEX\_RST timing

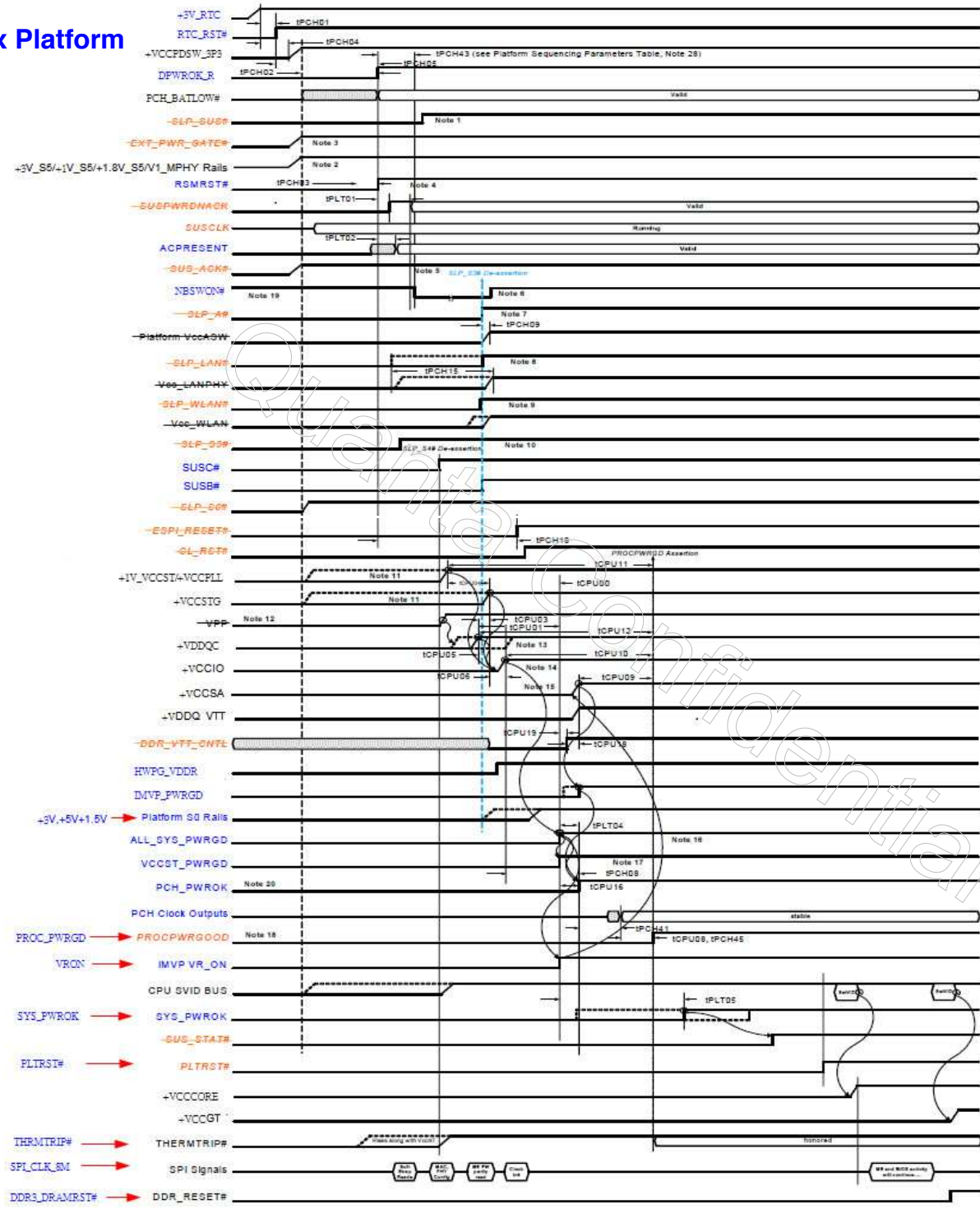


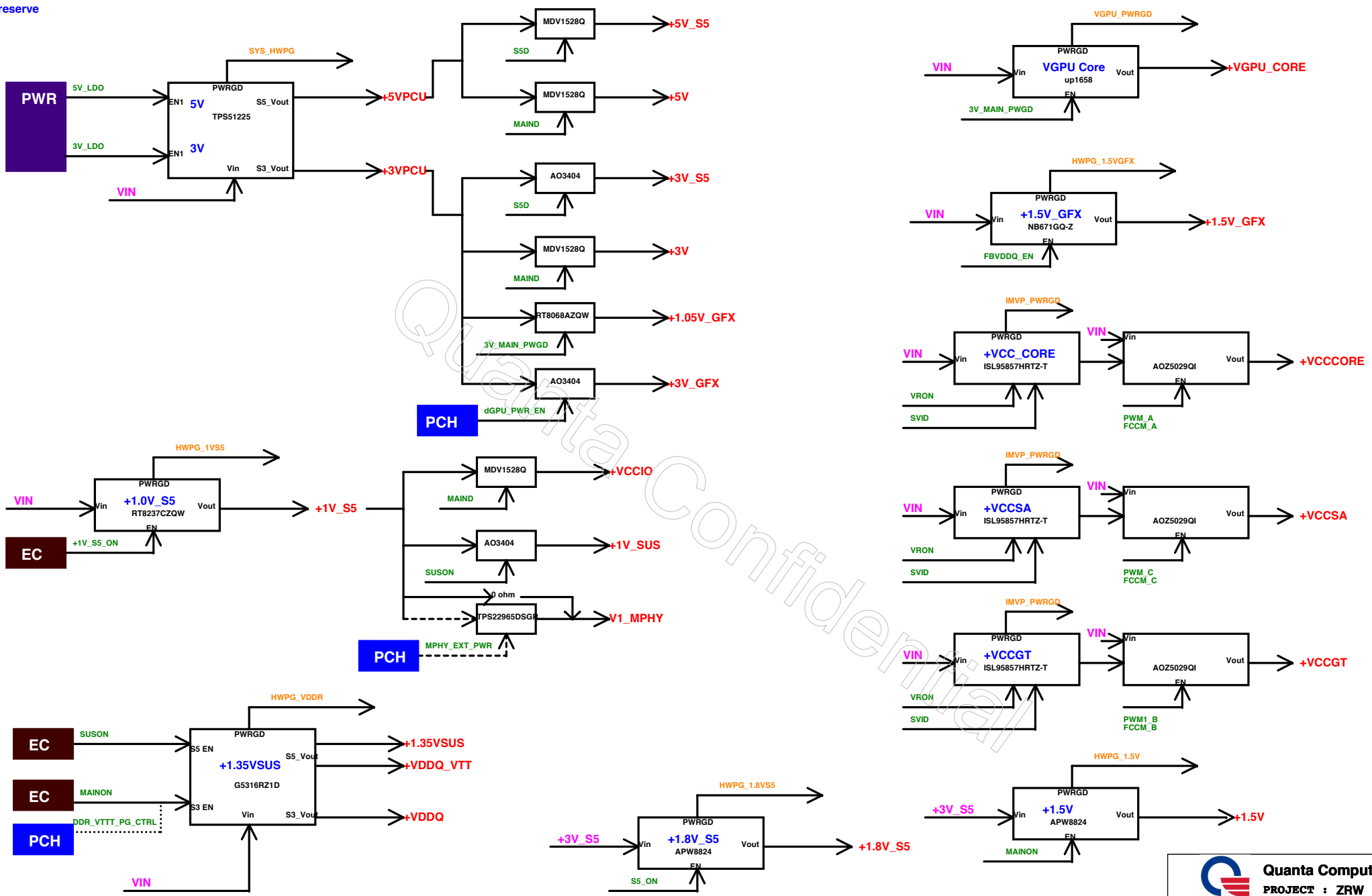
# Battery Mode

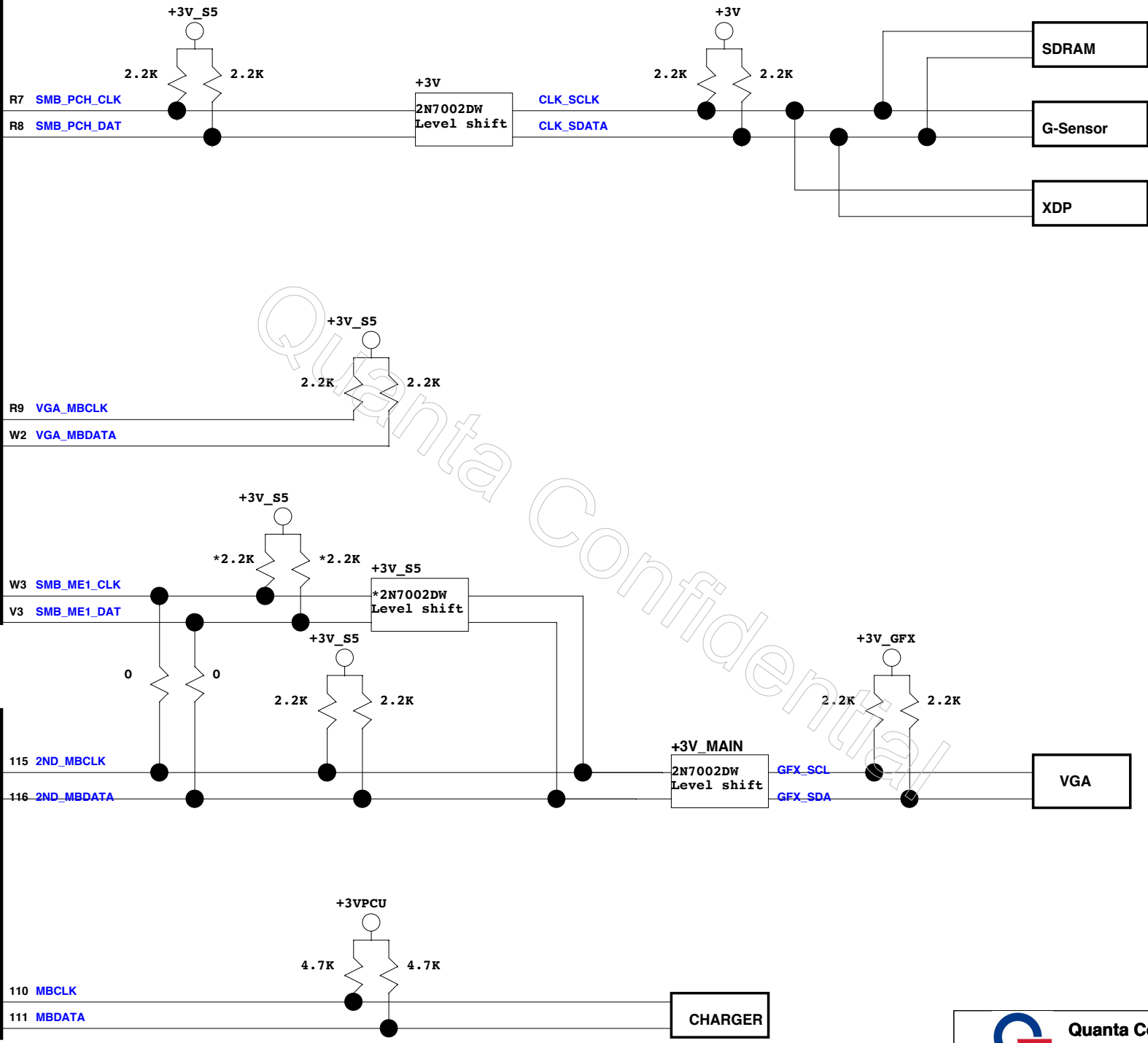
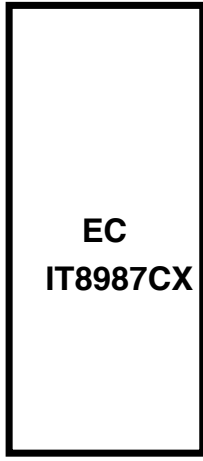
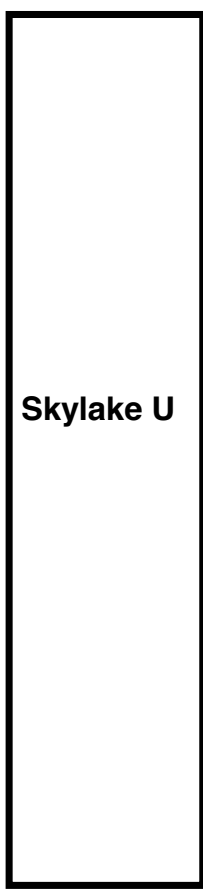
## Non Deep Sx



# Skylake U Non-Deep Sx Platform Power on sequence







Model	Date	CHANGE LIST
ZRW REV:A	1/20	1. FIRST RELEASED
ZRW REV:B	2/4	1. PU3#3 enable pin from VGPU_EN change to 3V_MAIN_PWGD control , add PR343 0ohm. (page 41) 2. U35#U11 #U12 connect to +1.8V_S5 for support Cannonlake-U PCH. (page 10) 3. U46#3 from net USB_OC1# change connect to USB_OC2# PCH. (page 28) 4. Add R776 33 Ohm and C805 180 pf in NBSWON#. (page 27) 5. Change LAN_WAKE# pin from CPU LAN_WAKE# to WAKE#(ball BB15) to support CPPM(PCIE LTR&OBFF&L1 off) (page 08) 6. add PR344 between PU14#12 & JP13. for GT3 CPU (page 33) 7. add PR345 between PU13#12 & JP12 for GT3 CPU (page 34)
	2/12	1. net ACCEL_INTA from U35#AD1 change to U35#AB1 [ UART0_RX ] net TP_INT_PCH from U35#AD2 change to U35#AB3 [ UART0_CTS# ] (page 04) 2. CN3 all pin from UART1 change connect to UART2 (page 04) 3. R587 from 0 ohm change to 1k pull down for USB2_ID (page 06) 4. add C806 for EMI request R748 0 ohm no stuff from EC site move at CPU site (page 07) 5. R293 stuff 4.7k , R294 from 4.99k change to 5.49k (page22) 6. XDP_TCK0,XDP_TCK1,XDP_TMS,XDP_TDI don't need pull up or pull down NO Stuff R515 , R558, R514, R537. (page 02)
	2/12	1. p.40 PR153 from 22 ohm change to 220 ohm for S3/S4/S5 bo bo sound issue.
	3/4	1. p.15 & p.16 L1 & L2 footprint from 0603 change to 0402 2. p.6 Delete UART1 4 pcs TP 3. p.25 EMI request add C807 33p for CLKRUN# 4. p.31 +3vpcu & +5vpcu from MPS NB679 change to TPS51225 5. p.24 R420 & R422 vendor suggest from 56 ohm change to 62 ohm [ CS06202JB15 ]
ZRW REV:C1	4/30	1. p.2 Stuff 10k ohm_4 of R780 & R781. [ KBSMI# & EC_SCI# ] Pull up to +3V. 2. P.29 U45 EC pin 70 connect to p.30 PU5#8 IDCHG net 3. P.29 U45 EC pin 95 connect to net IOAC_LANPWR# 4. P.06 Add PQ6059 & PQ6060 for EC_RTCSRST control reset RTC_SRTC_RST# & RTC_RST#
	5/7	1. p.09 removed MPHYS_EXT_PWR control power function. [ Removed U11, R195, R197,C208,C253 ] 2. p.07 R576 & R572 from value 4.7k change to 2.2k
ZRW REV:C2	5/8	1. p.36 & p37 change new PU6,PU7,PU8,PU9 footprint AOZ5029Q1-5 & partnumber AL005029001 2. p.28 Delete L8,L9,L10,L14,L15,17 EMI Choke footprint
	5/25	1. p.09 R762 [LPM_ZVM_N] & R763 [ MSM# ] No Stuff for GT3 2. p.09 add R789 0 ohm for VCCHDA p.24 R365 stuff 0 ohm connect to +3V , R363 0 ohm no stuff connect to +1.5v 3. p.34 delete +VCCOEPIO circuit 4. p.05 delete R141 , R133 , R547 for SVID data,Alert#,clk 5. p.39 delete VCCGT circuit 6. p.37 delete PR77 & PR88 for VCCGT connect to VCCGT
	5/28	1. p.03 Delete R656 & R189. DDR0_ALERT# & DDR1_ALERT# connect to GND 2. p.09 Delete R763 0 ohm for net MSM#.
ZRW REV:C3	6/18	1. p.05 Add C814 1000p/50v_4 connect +1V_VCCST and near R138 SVID. 2. p.36 Add PC6228 1000p/50v_4 connect +1V_VCCST and near RR341 SVID. 3. p.02 Add R795 , R796 , R797 0ohm for DCI USB 3.0 test fixture 4. p.11 delete XDP function connector U27 , U30 , CN1 5. p.09 Remove short Jumper for all +1V_S5. 1. R163 , R159 ,R581, R146 ,R149 , R157 , R173 , R151 , R170 , R136 2. R545 , R144 , R150 , R147 , R551 , R557, R584 [ VCCCLK1-6 ] 3. R168 [ +1_S5 -> V1_MPHY ] 6. p.36 remove PR37 Shortpad for SVID_ALERT# 7. p.07 Delete Q33 , R579 ,R583 for SMBus(EC)
	6/23	1. p.02 Delete TP82 and Net [ SKTOCC# ] 2. p.05 reserve 5 pcs 1000 pF capacitor in +1V_VCCST [ C815,C816,C817,C818,C819 ] , no stuff by default 3. p.09 Reserve test point TP95 for CPU AK13 ball 4. p.32 add PC6230 22u/6.3v_6 in connect to PQ23.1 [+1V_SUS]

Confidential

 <b>Quanta Computer Inc.</b> PROJECT : ZRW Change list	DOC NO.	PROJECT MODEL : ZWA	APPROVED BY:	DATE:
		PART NUMBER:	DRAWING BY:	REVISION: