

Intel BayTrail-D Platform

Date : 2013/12/27
Version 1.0

Compal Confidential

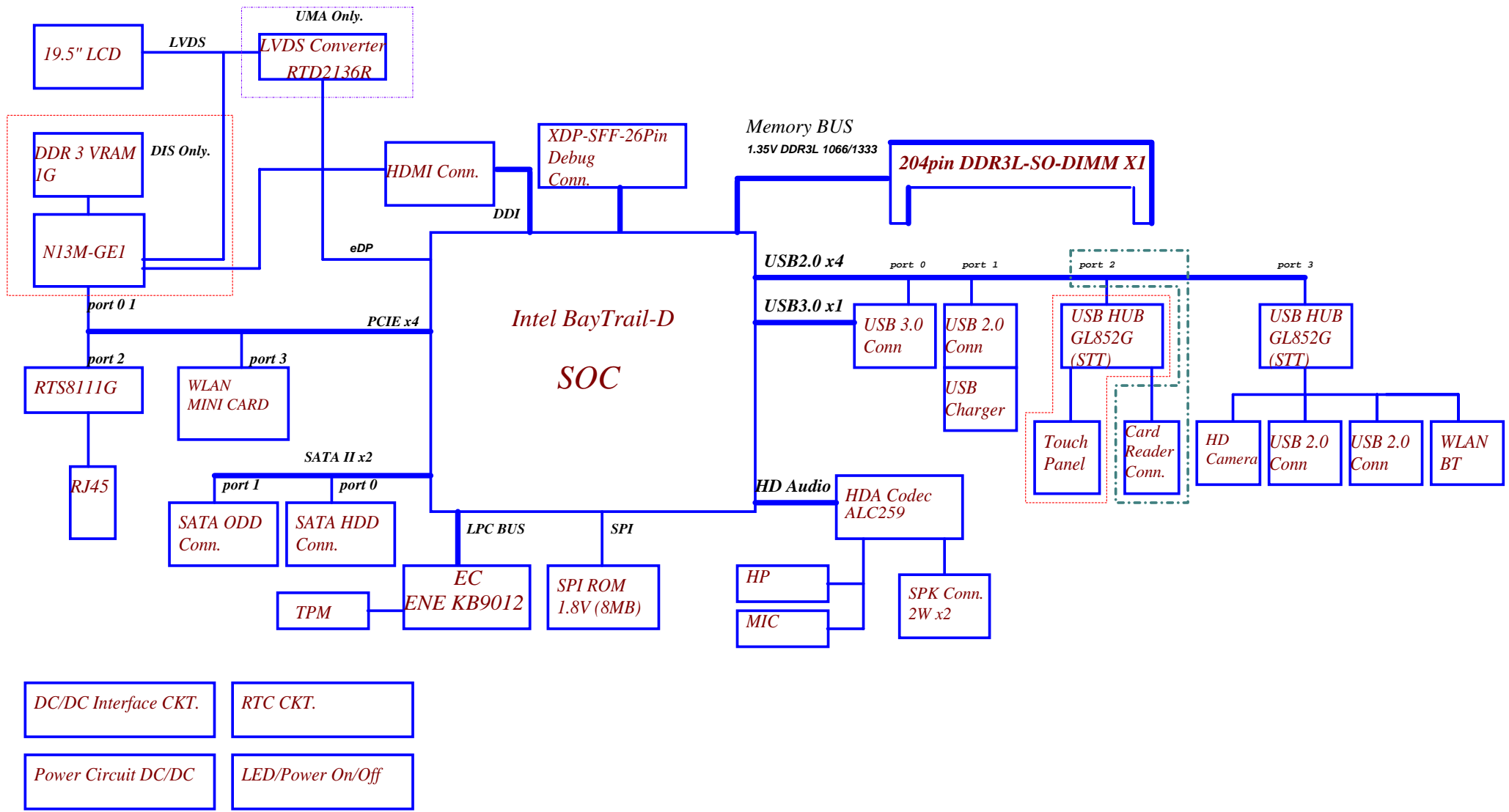
ZAA00(C260) LA-B001P Schematics Document

Intel BayTrail-D Platform

AIO M/B

REV: 1.0

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID / SKU ID Table for AD channel

Board ID	R281	VAD_BID min	VAD_BID typ	VAD_BID max
Vcc	3.3V +/- 5%			
R280	100K +/- 5%			
0.1	0	0 V	0 V	0 V
0.2	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
0.3	18K +/- 5%	0.436 V	0.503 V	0.538 V
1.0	33K +/- 5%	0.712 V	0.819 V	0.875 V
	56K +/- 5%	1.036 V	1.185 V	1.264 V
	100K +/- 5%	1.453 V	1.650 V	1.759 V
	200K +/- 5%	1.935 V	2.200 V	2.341 V
	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0.1	R281=0 Ohm; R280 open
0.2	R281=8.2K Ohm; R280 100K Ohm
0.3	R281=18K Ohm; R280 100K Ohm
1.0	R281=33K Ohm; R280 100K Ohm

BOM Option Table(Config)

Option	Value	Unit	Min	Max	Rev
R281	0 Ohm	Ohm			
R280	100K	Ohm			
R281	8.2K	Ohm			
R281	18K	Ohm			
R281	33K	Ohm			

UMA/DIS ID Table

	0(DIS)	1(UMA)
AD_PID1	R287=10K Ohm; R288 open	R287 open; R288=10K Ohm
UD	R330 = 10K Ohm; R289 open	R330 open; R299=10K Ohm

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

SOC SM Bus address

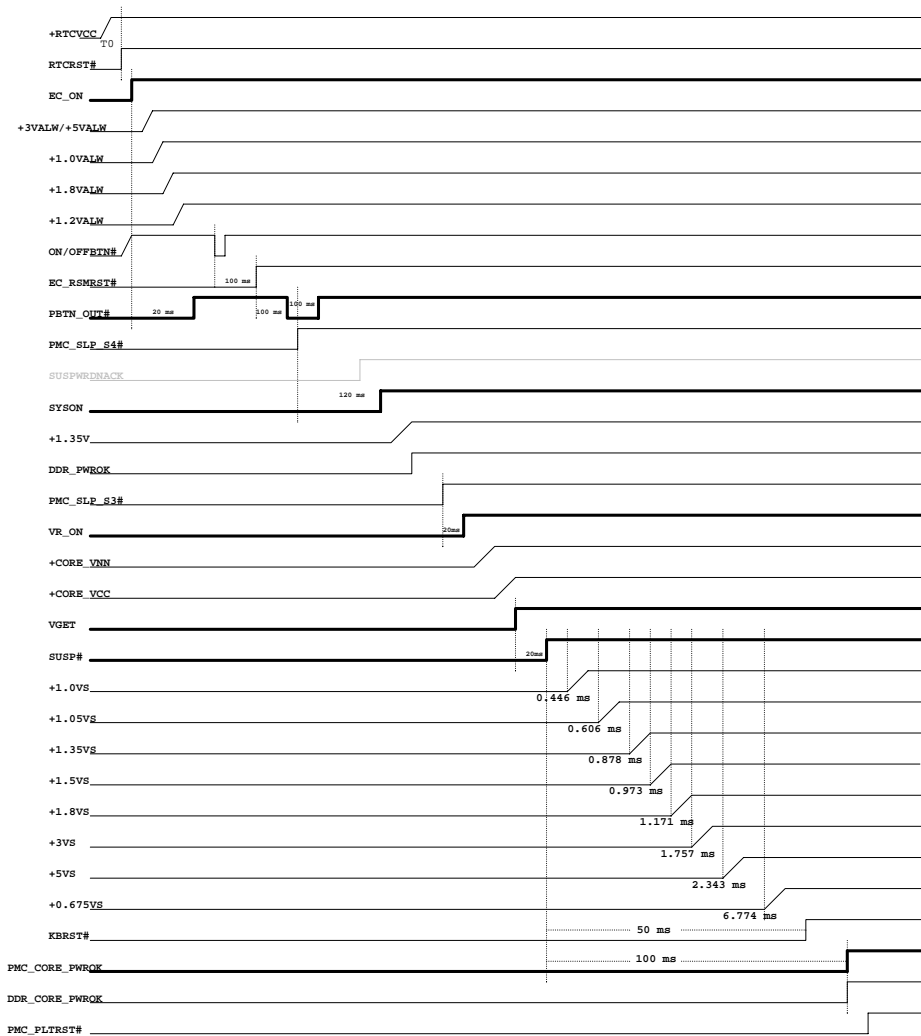
Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

43 level BOM table

43 Level	Description	BOM Structure
4319RF38L01~20	ZAA00	None Touch SKU
4319RF38L30~50	ZAA20	Touch SKU

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				Notes List
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Power ON



T0: +RTCVCC stable to RTCRST# high > 9ms
 T1: VR ramp up time from 10% to 90% voltage level < 2ms
 T2 :Rail to subsequent rail turn on delay < 2ms
 T3 :+VALWAS stable to EC_RSMRST# high > 10ms
 T4 :+VS rails stable to PMC_CORE_PWRCK > TBD

NOTE:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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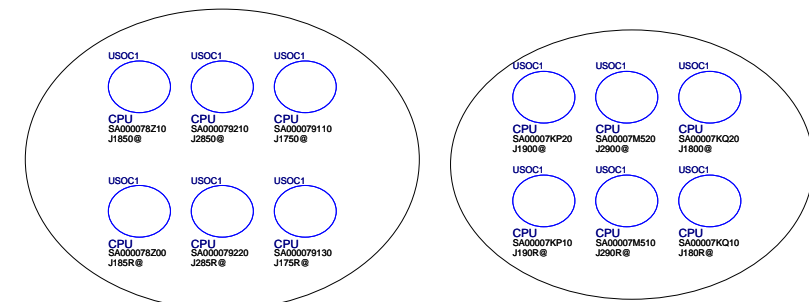
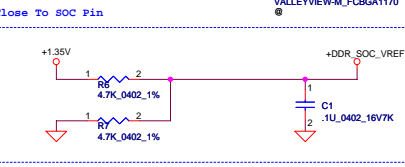
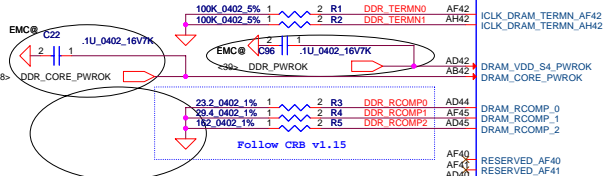
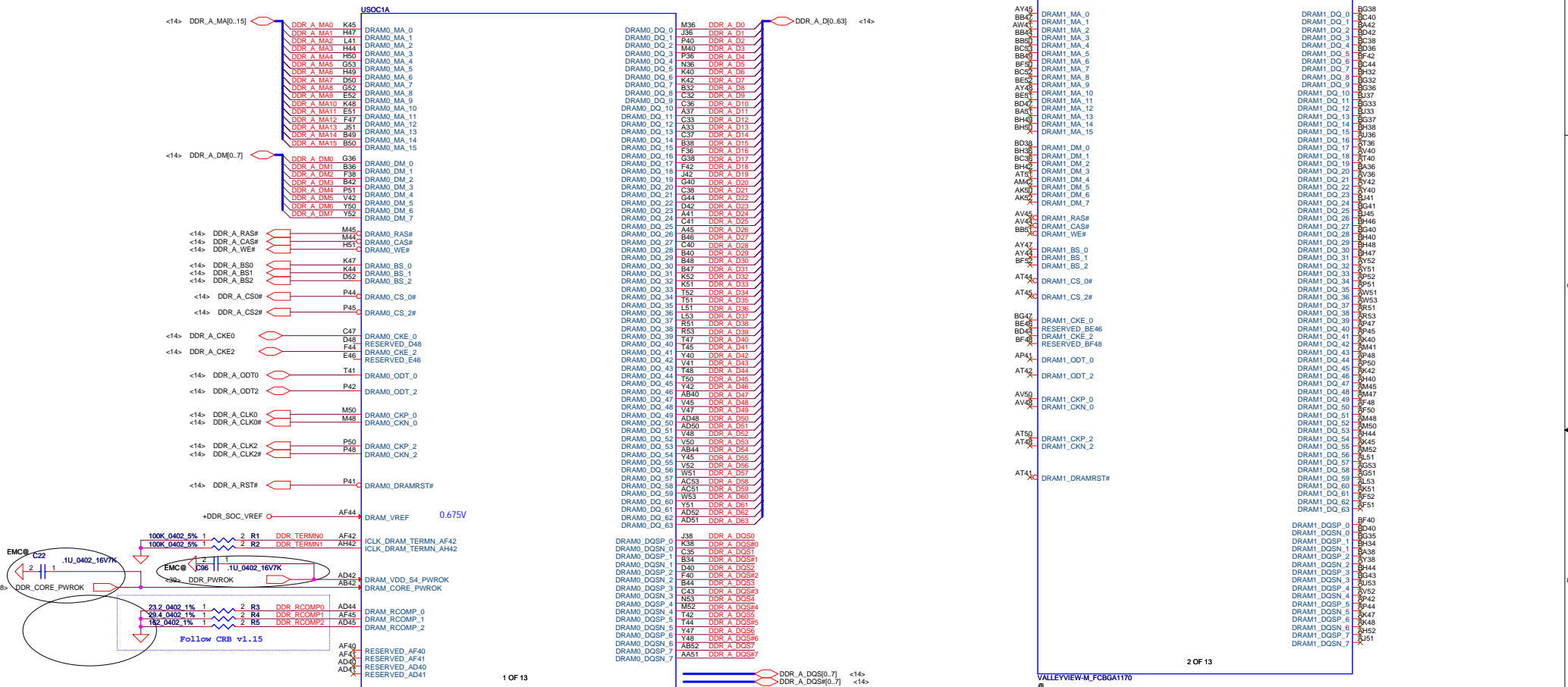
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ZZZ1

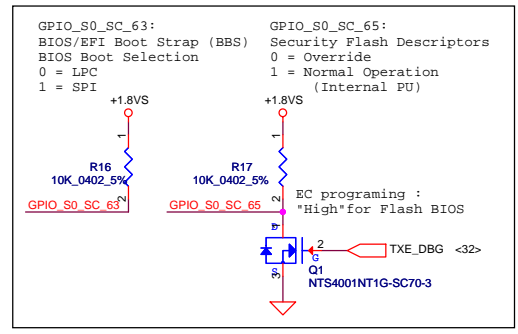
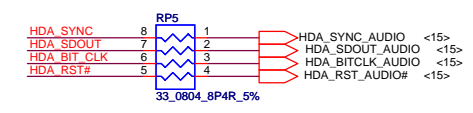
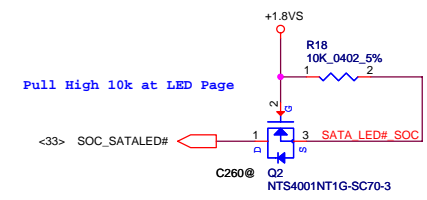
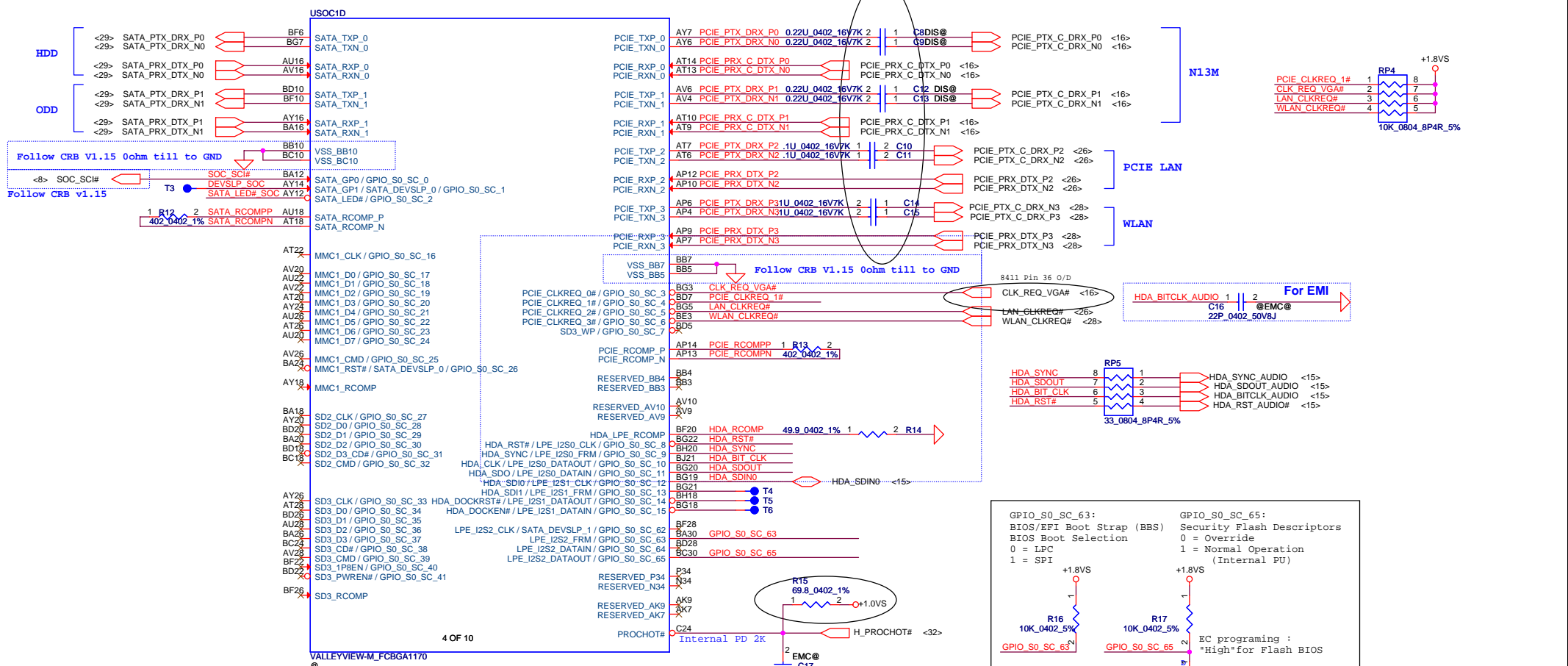
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Channel A Only

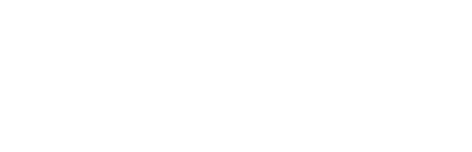
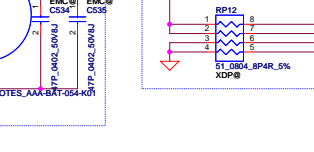
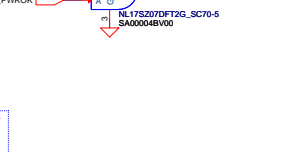
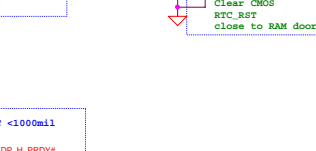
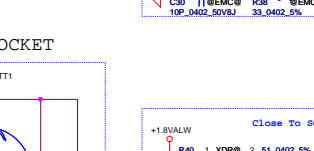
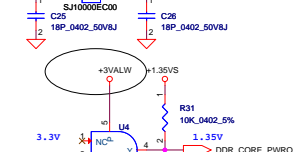
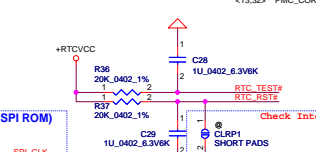
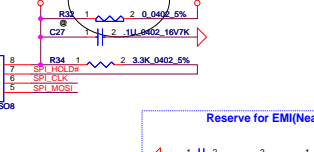
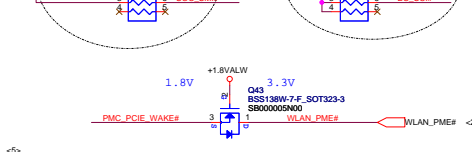
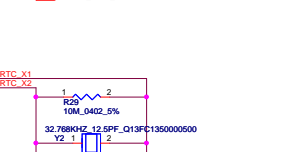
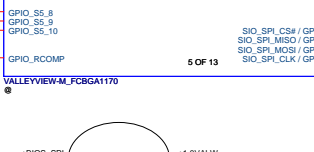
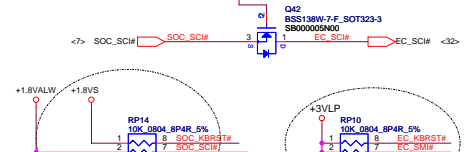
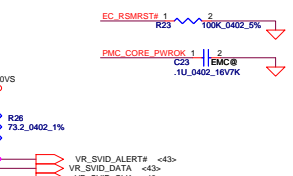
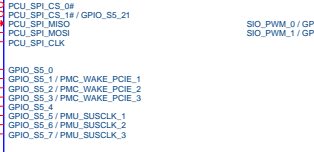
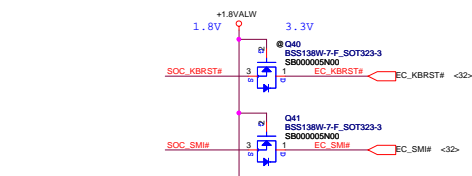
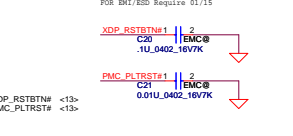
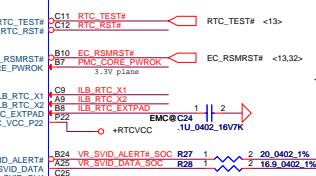
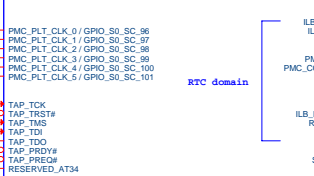
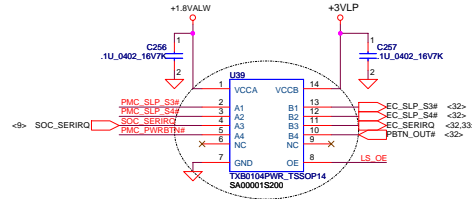
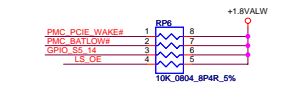
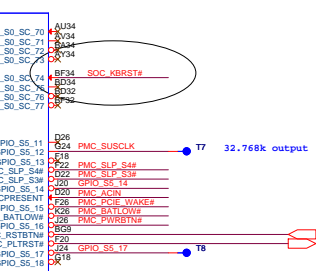
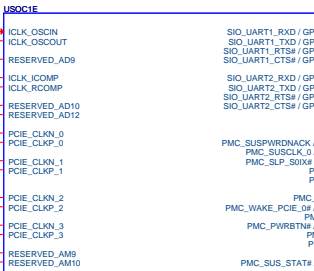
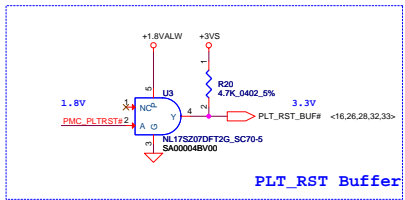
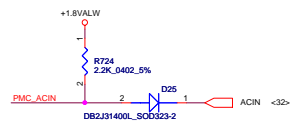
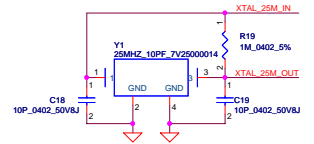
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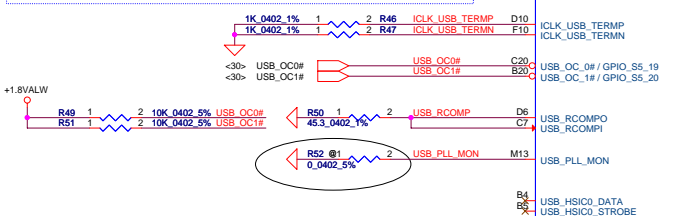
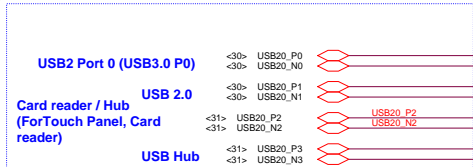
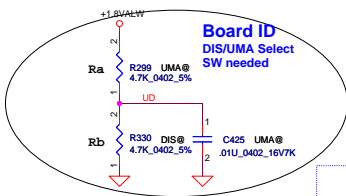
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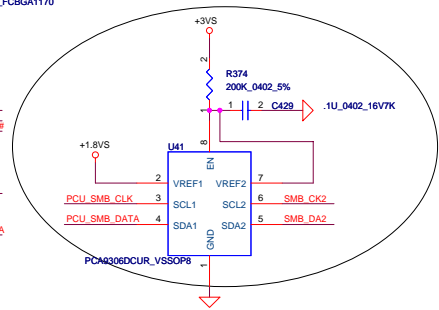
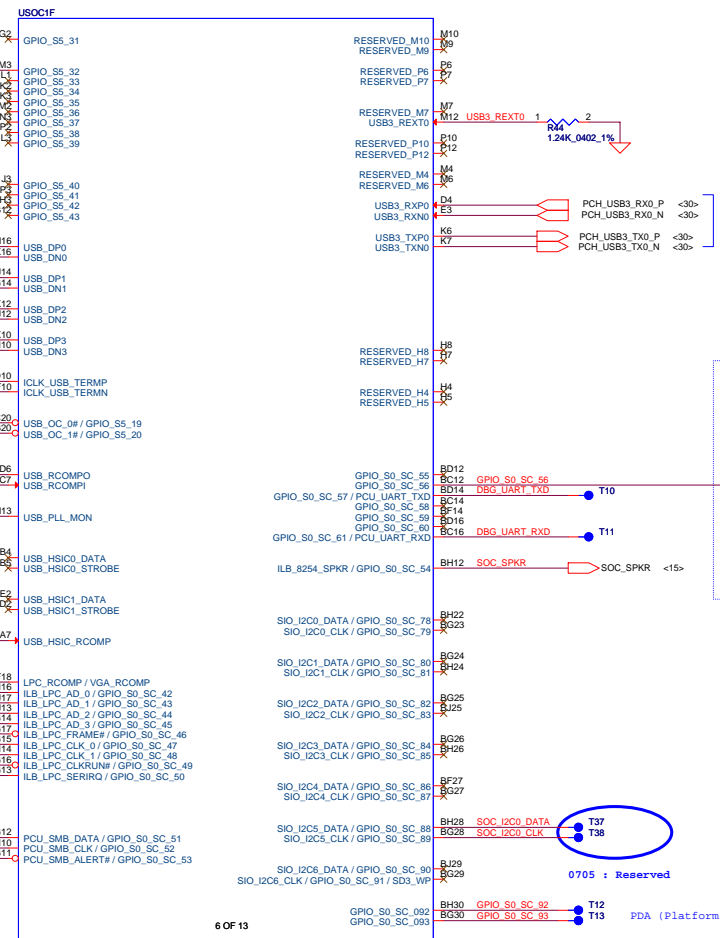
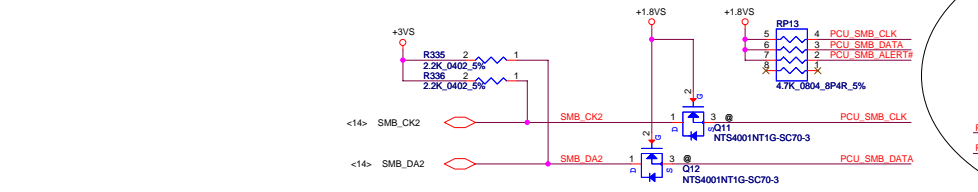
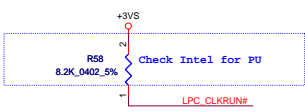
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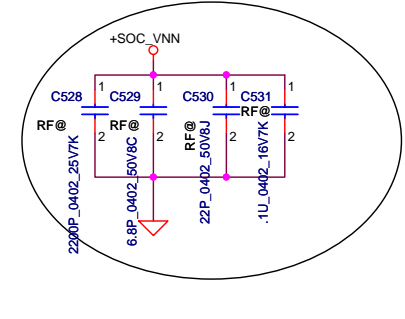
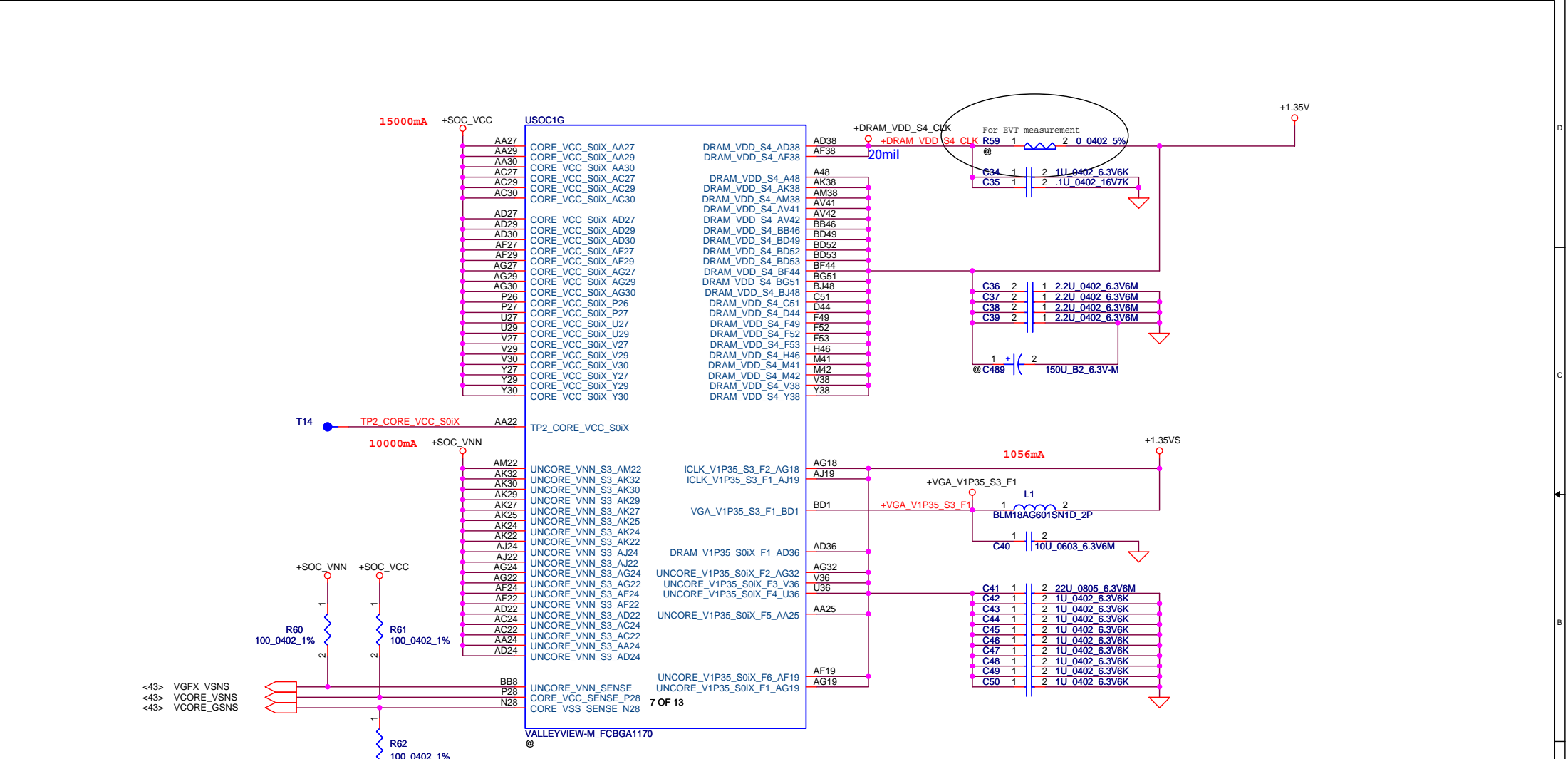
NOTE: Ref checklist rev1.0 p.25
 USB_HSIC_RCOMP must NOT float if they are not being used.

ILB_LPC_CLK_0 : Output of 25MHz,
 Need Check with EC

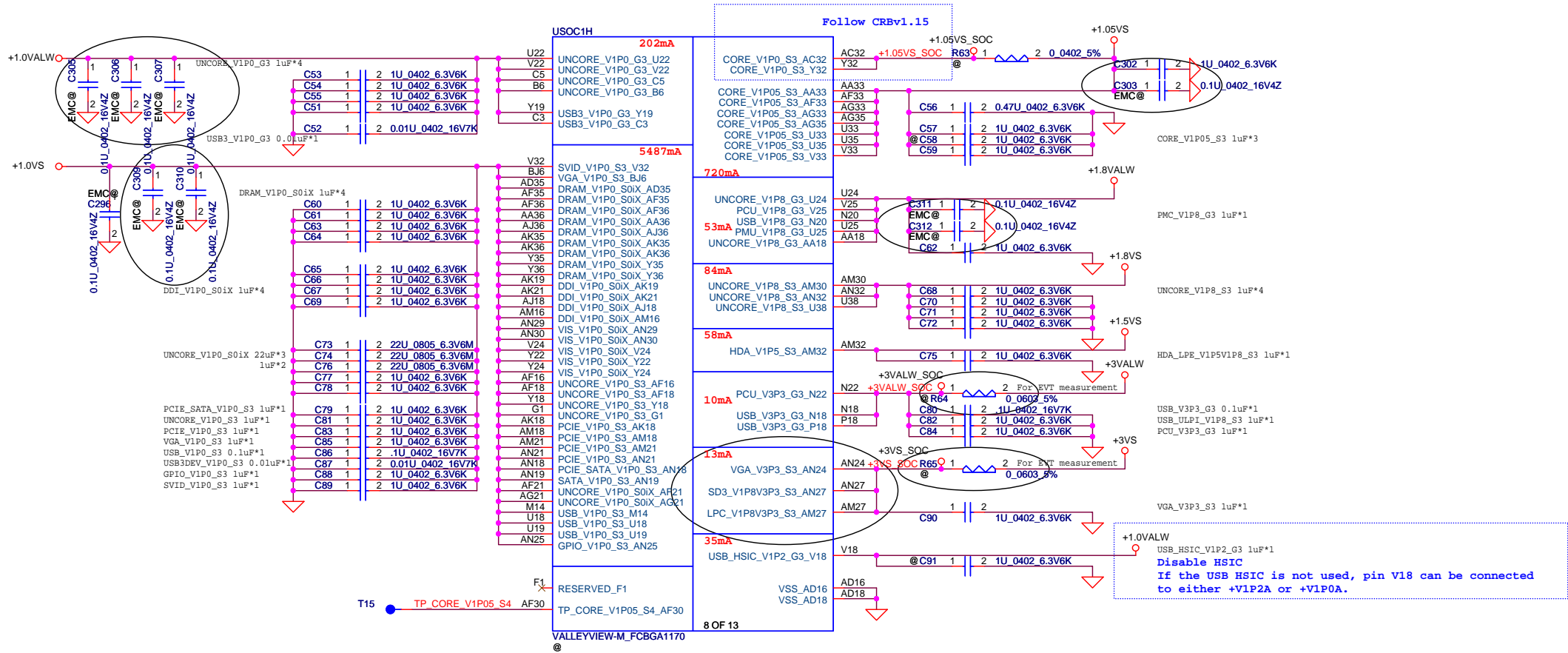
ILB_LPC_CLK_1 is for CLK_0 feedback.(Input)
 Set to Output for Normal Usage



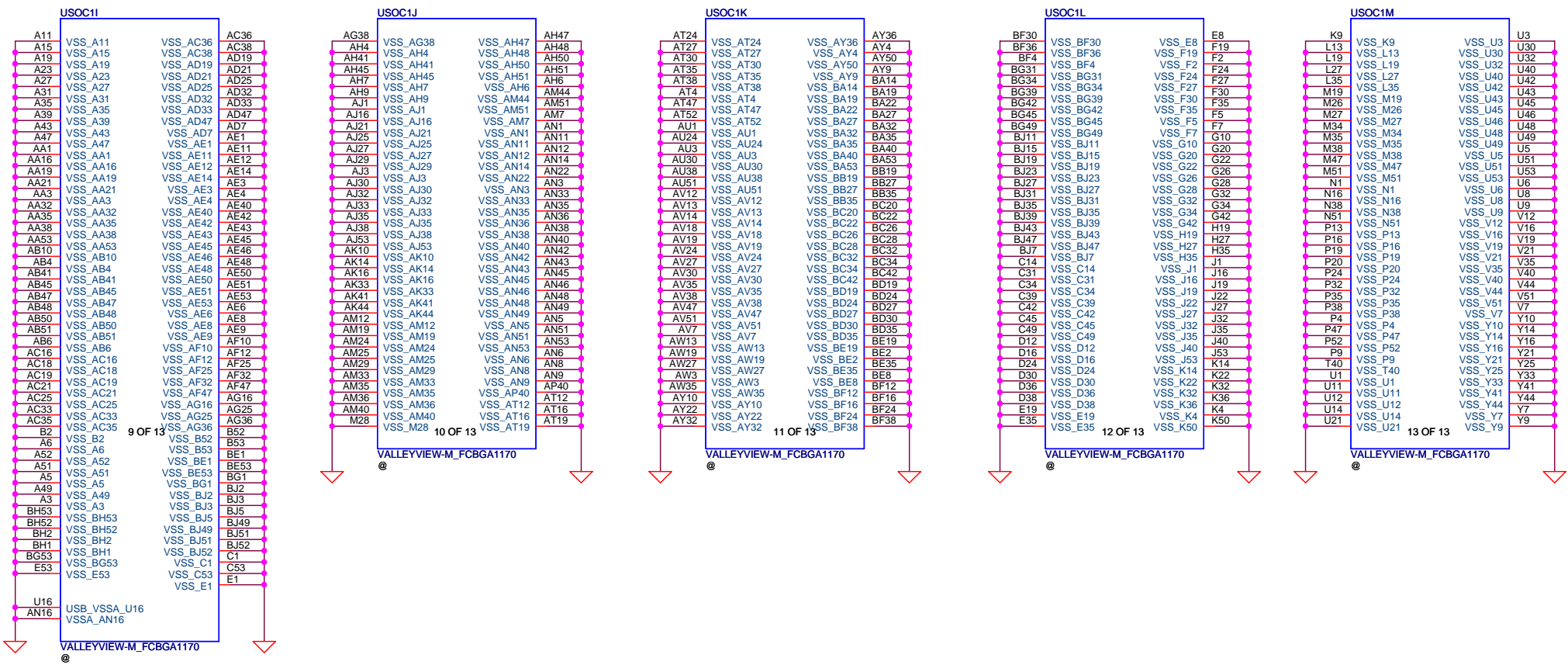
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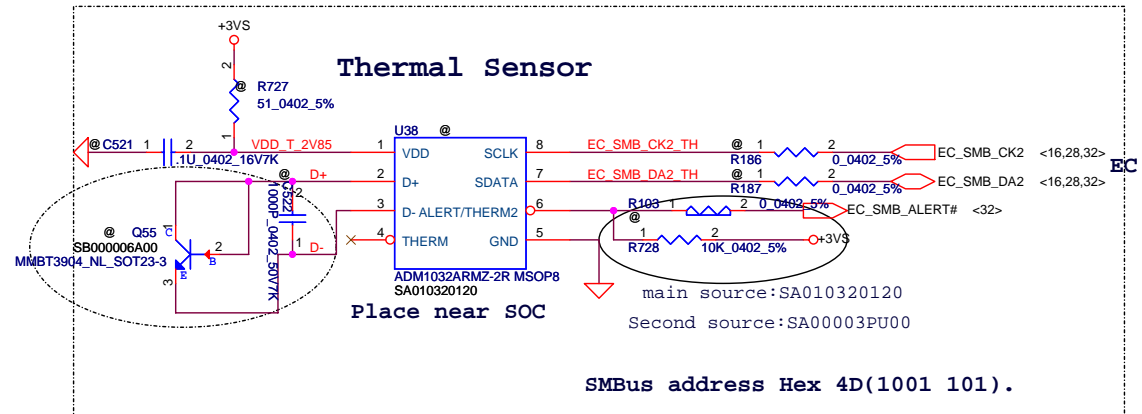
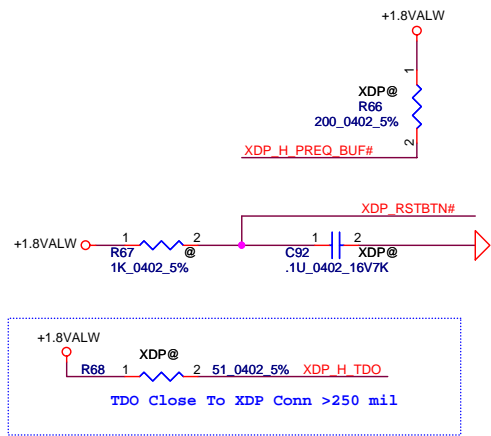


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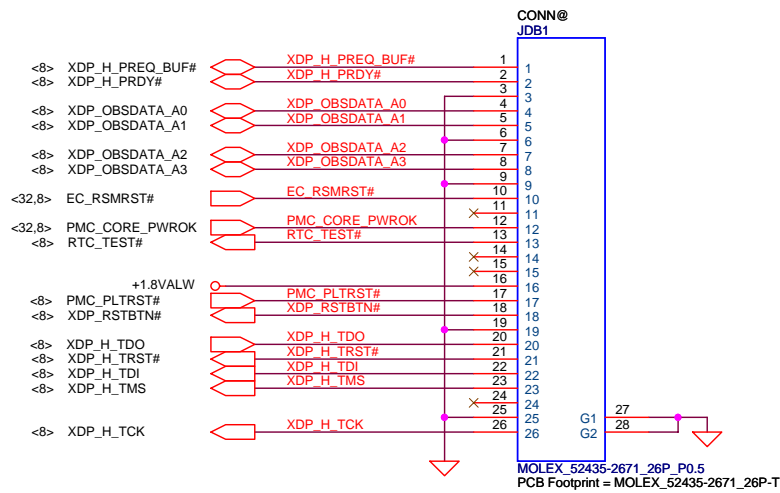


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Compal Electronics, Inc.
BayTrail-D GND

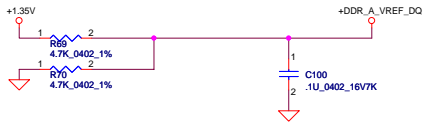


XDP-SFF-26Pin

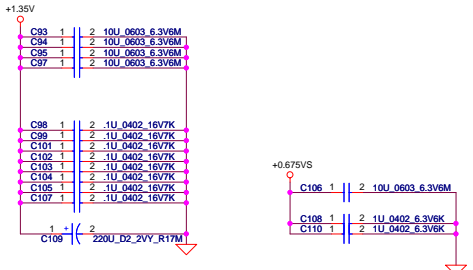
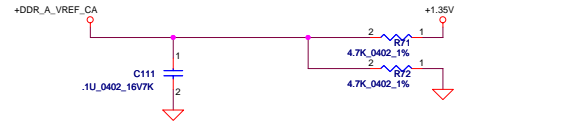
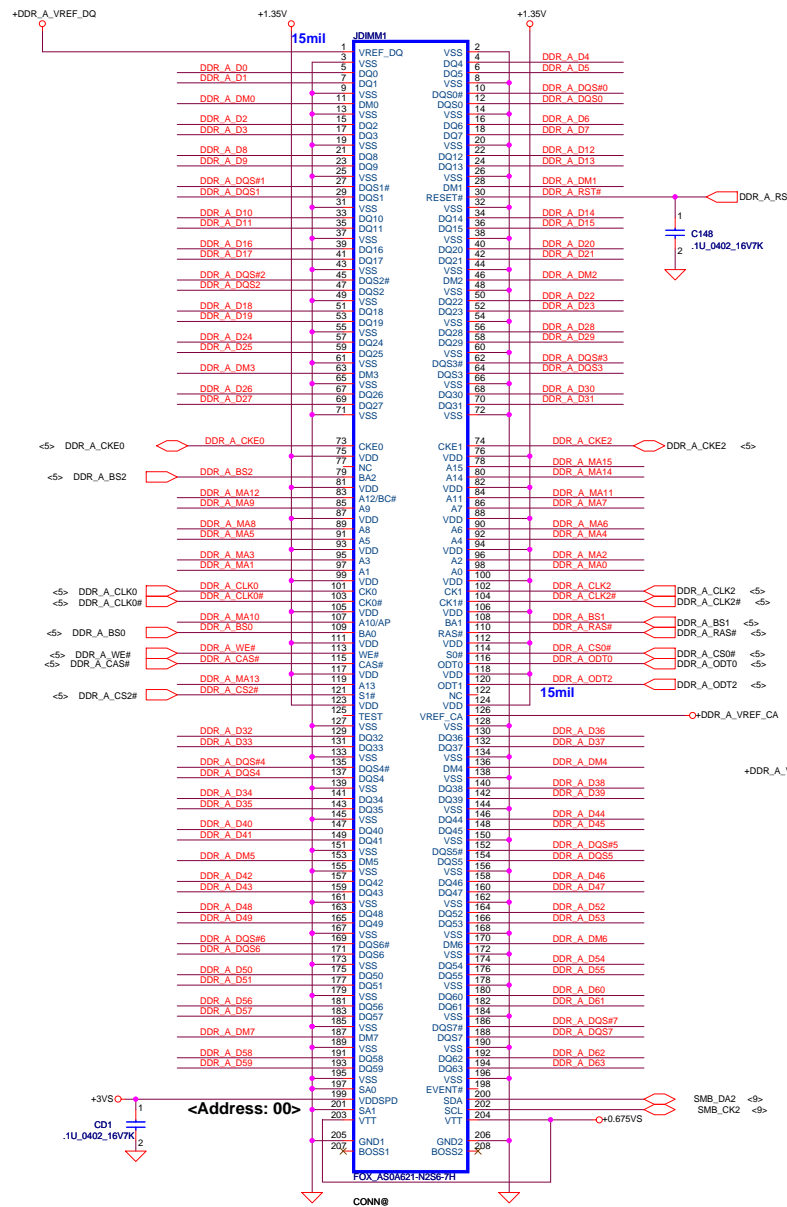


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				Date: Tuesday, March 25, 2014	Sheet 13 of 48

Signal voltage level = 0.675 V
 PLACE TWO 4.7K RESISTORS CLOSE TO
 DIMM5 ON DIMM_VREF_CA / DIMM_VREF_DQ
 Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SDDIMM.

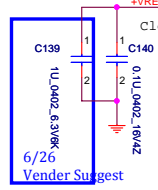
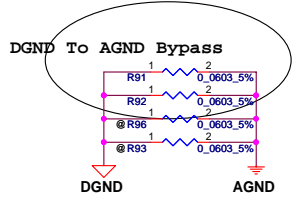
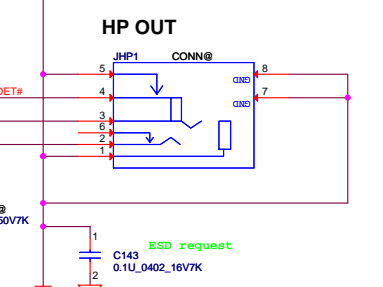
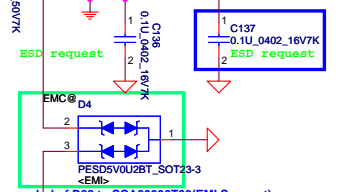
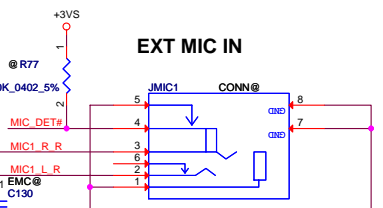
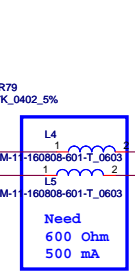
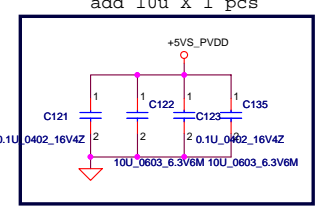
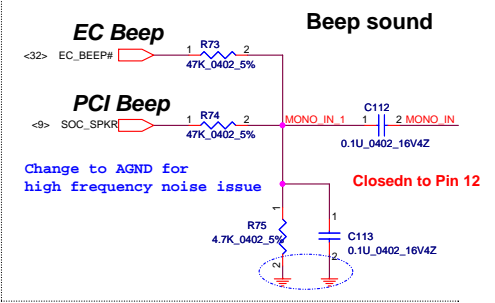
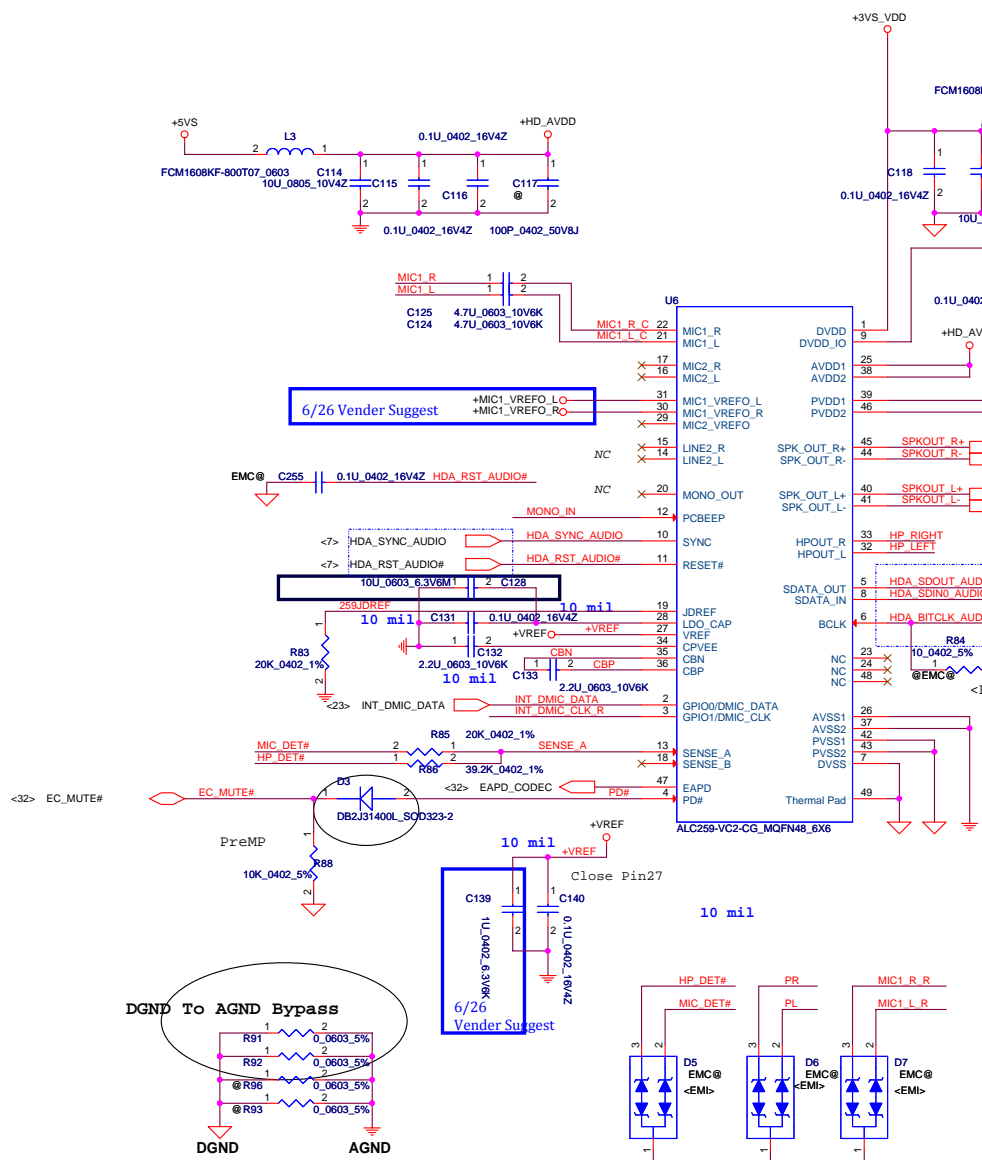


- DDR_A DQ[0..63] <-> DDR_A_DQ[0..63] <->
- DDR_A MA[0..15] <-> DDR_A_MA[0..15] <->
- DDR_A DM[7..0] <-> DDR_A_DM[0..7] <->
- DDR_A DQS[7..0] <-> DDR_A_DQS[0..7] <->
- DDR_A DQS# [7..0] <-> DDR_A_DQS#[0..7] <->



DIMM_A H:4mm Reverse--> STD 0809

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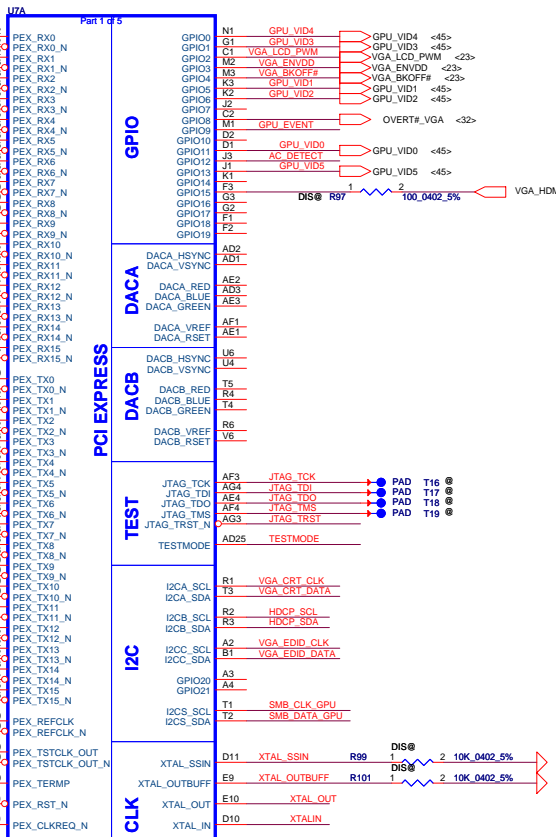


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	HP-OUT (PIN 32,33)
	20K	MIC1 (PIN 21, 22)

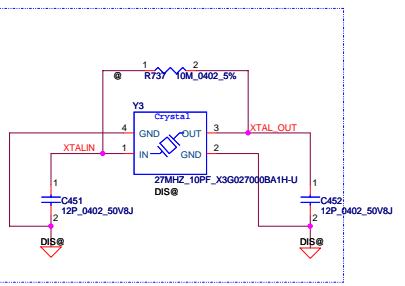
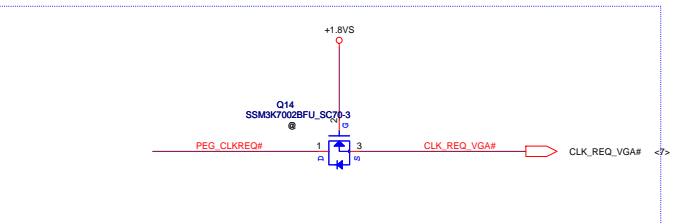
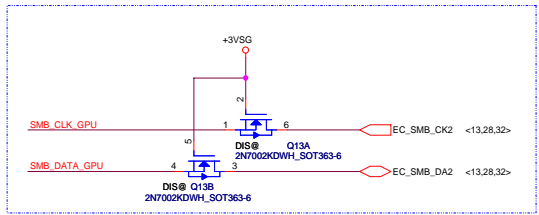
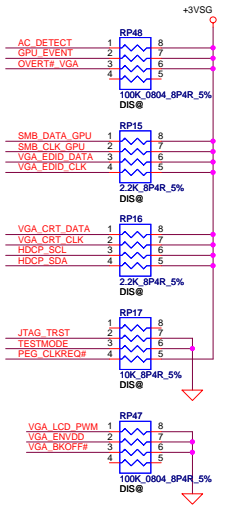
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 <-7> PCIE_PTX_C_DRX_N0 PCIE_PTX_C_DRX_N0 AF12
 <-7> PCIE_PTX_C_DRX_P1 PCIE_PTX_C_DRX_P1 AG13
 <-7> PCIE_PTX_C_DRX_N1 PCIE_PTX_C_DRX_N1 AF13

<-7> PCIE_PRX_C_DTX_P0 DIS@ 2 1 C144 0.22U 0.402 16W7K PRX_DTX_P0 AD10
 <-7> PCIE_PRX_C_DTX_N0 DIS@ 2 1 C145 0.22U 0.402 16W7K PRX_DTX_N0 AD11
 <-7> PCIE_PRX_C_DTX_P1 DIS@ 2 1 C146 0.22U 0.402 16W7K PRX_DTX_P1 AD12
 <-7> PCIE_PRX_C_DTX_N1 DIS@ 2 1 C147 0.22U 0.402 16W7K PRX_DTX_N1 AC12

<8> CLK_PCIE_VGA CLK_PCIE_VGA AB10
 <8> CLK_PCIE_VGA# CLK_PCIE_VGA# AC10
 PEX_TSTCLK_OUT+ PEX_TSTCLK_OUT+ AF10
 PEX_TSTCLK_OUT- PEX_TSTCLK_OUT- AE10
 R98 DIS@ 200_0402_1%
 PEX_TREMP# PEX_TREMP# AG10
 <26.28.32.33.8> PLT_RST_BUF# PLT_RST_BUF# AD9
 PEX_RST_N PEX_RST_N AD9
 PEX_CLKREQ_N PEX_CLKREQ_N AE9



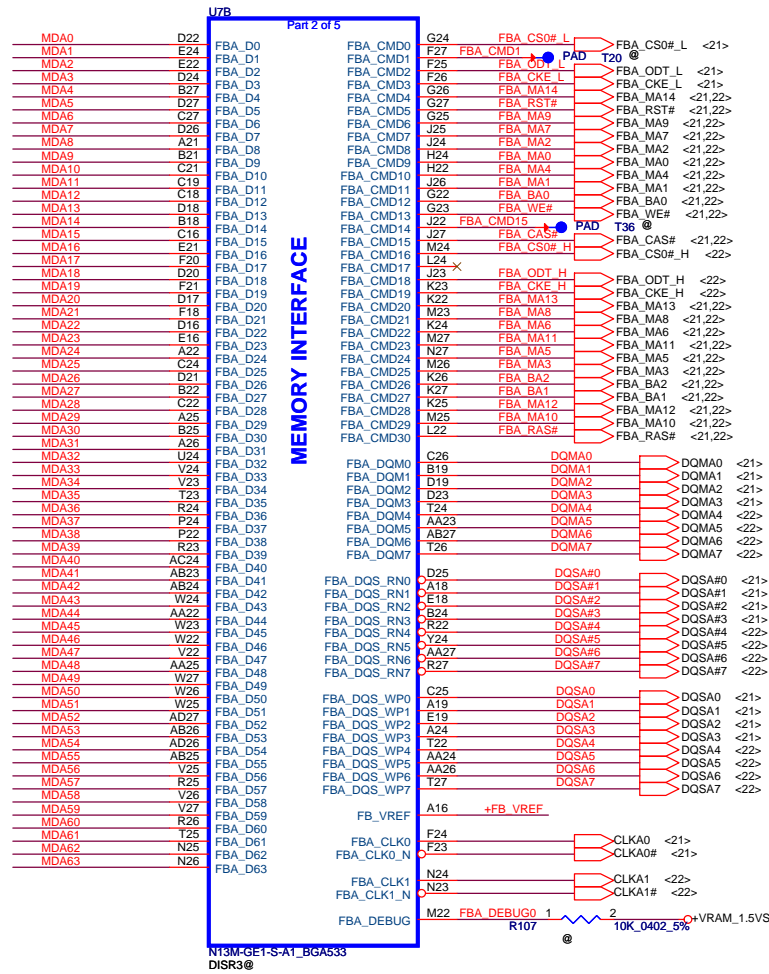
D1B3@ N13M-GE1-S-A1_BGA533



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VRAM Interface

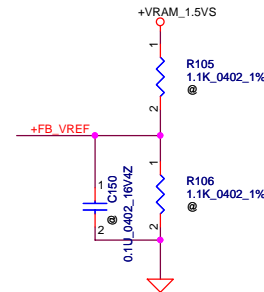
<21> MDA[31..0] ← MDA[31..0]
 <22> MDA[63..32] ← MDA[63..32]



N13M-GE1-S-A1_BGA533
 DISR3@

Mode D Address	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

*A15 is not required for any x16 device, even up to 4Gb density. *A15 is only needed if we support x8 configurations, and only at 4Gb.

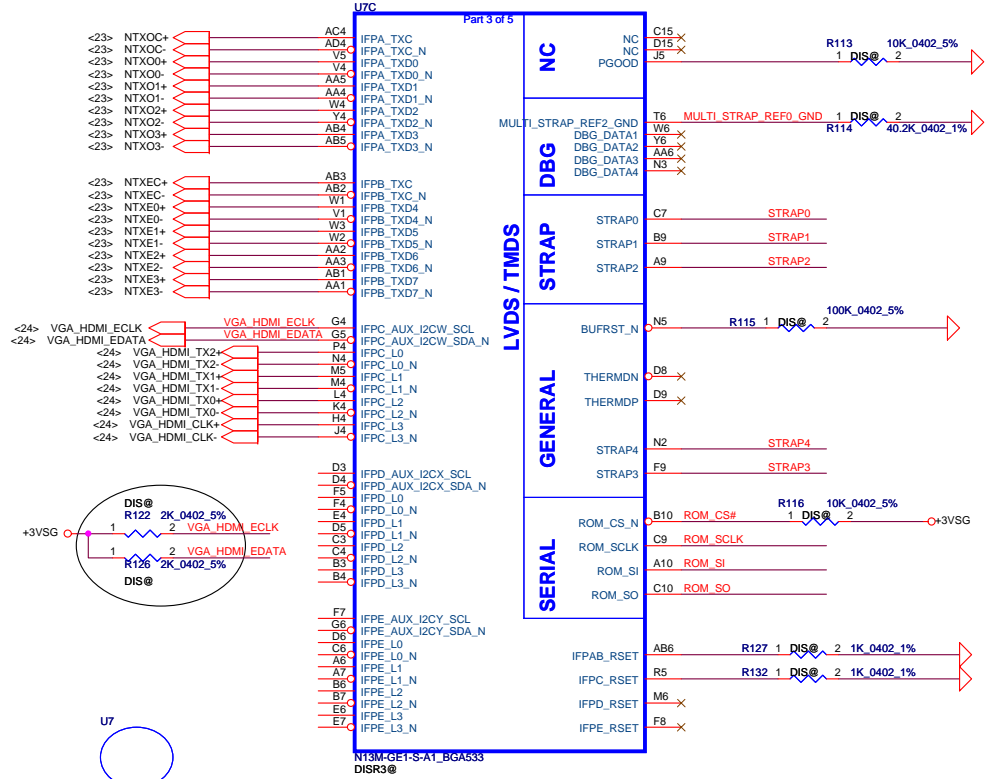


Place close to the first T point

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

FBA_ODT_H R108 1 DIS@ 2 10K_0402_5%
 FBA_ODT_L R109 1 DIS@ 2 10K_0402_5%
 FBA_CKE_H R110 1 DIS@ 2 10K_0402_5%
 FBA_CKE_L R111 1 DIS@ 2 10K_0402_5%
 FBA_RST# R112 1 DIS@ 2 10K_0402_5%

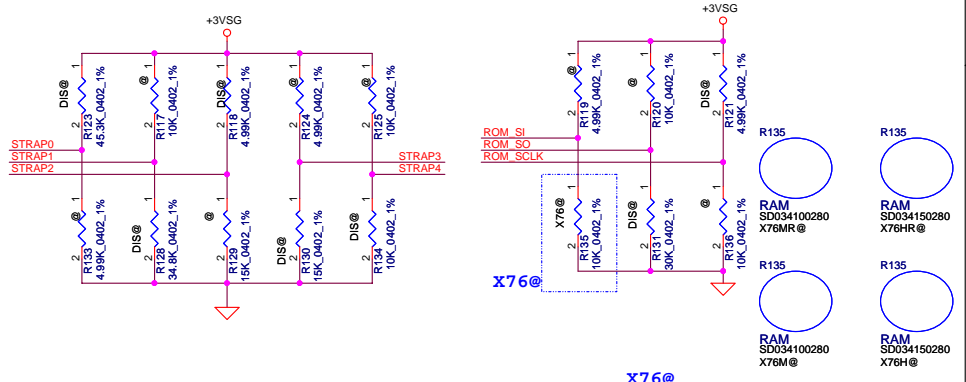
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	N13M VRAM Interface
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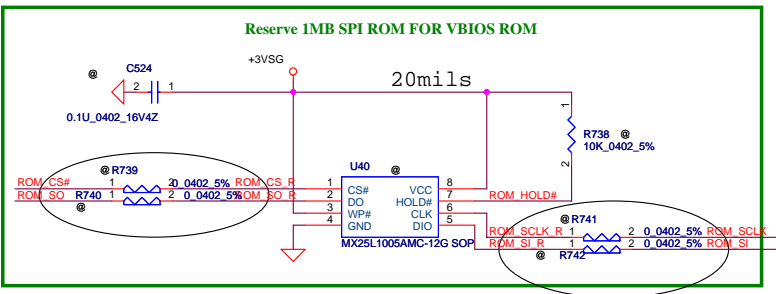
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	bit5 to bit0
N13M-GE1-S	0x1058	011000

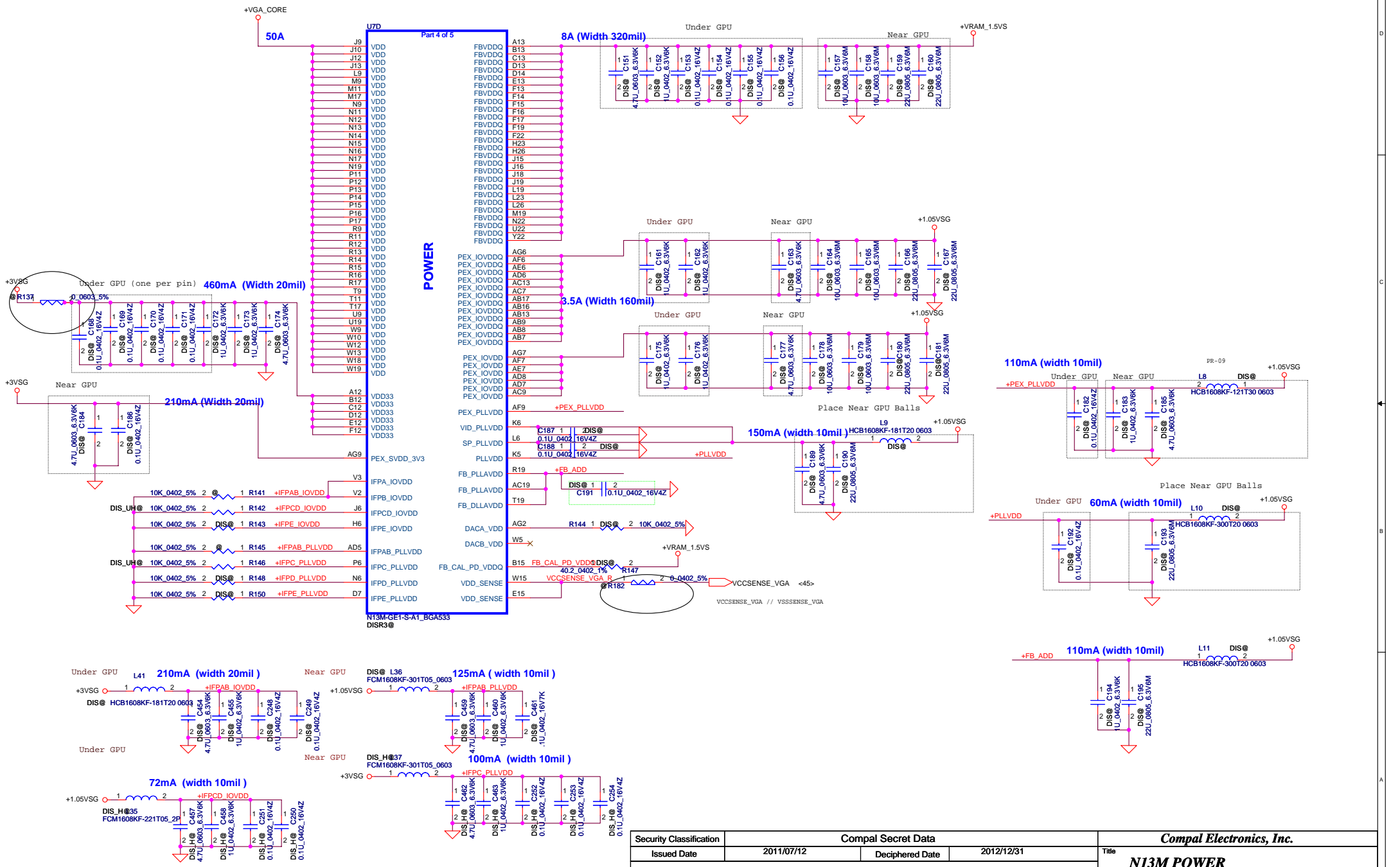
Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



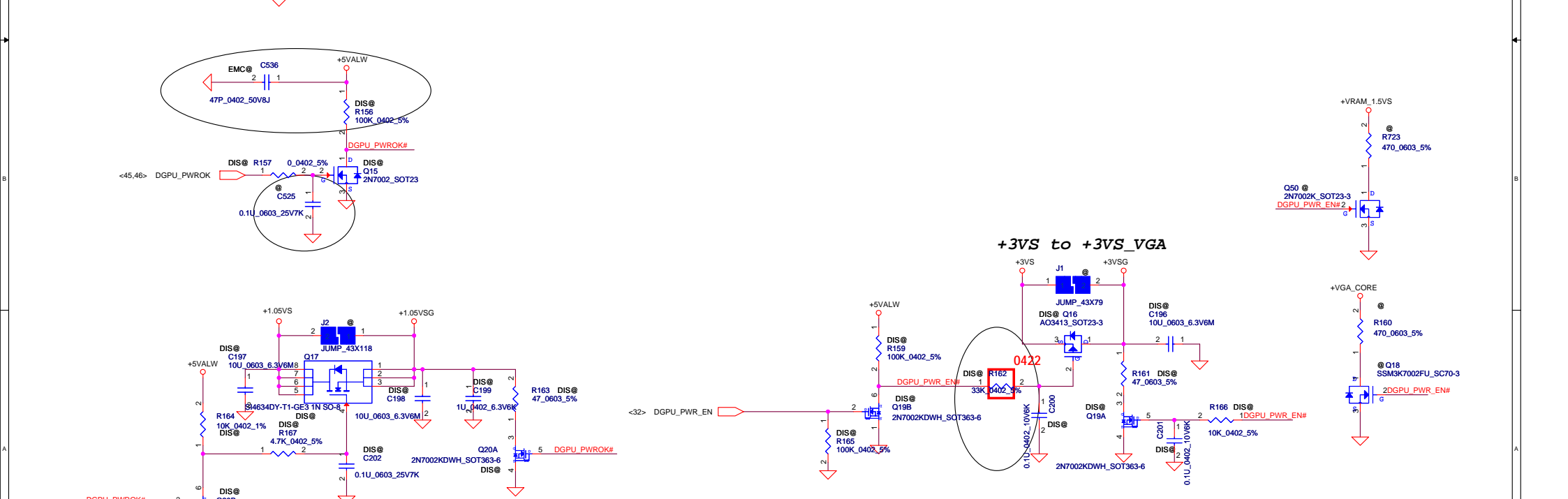
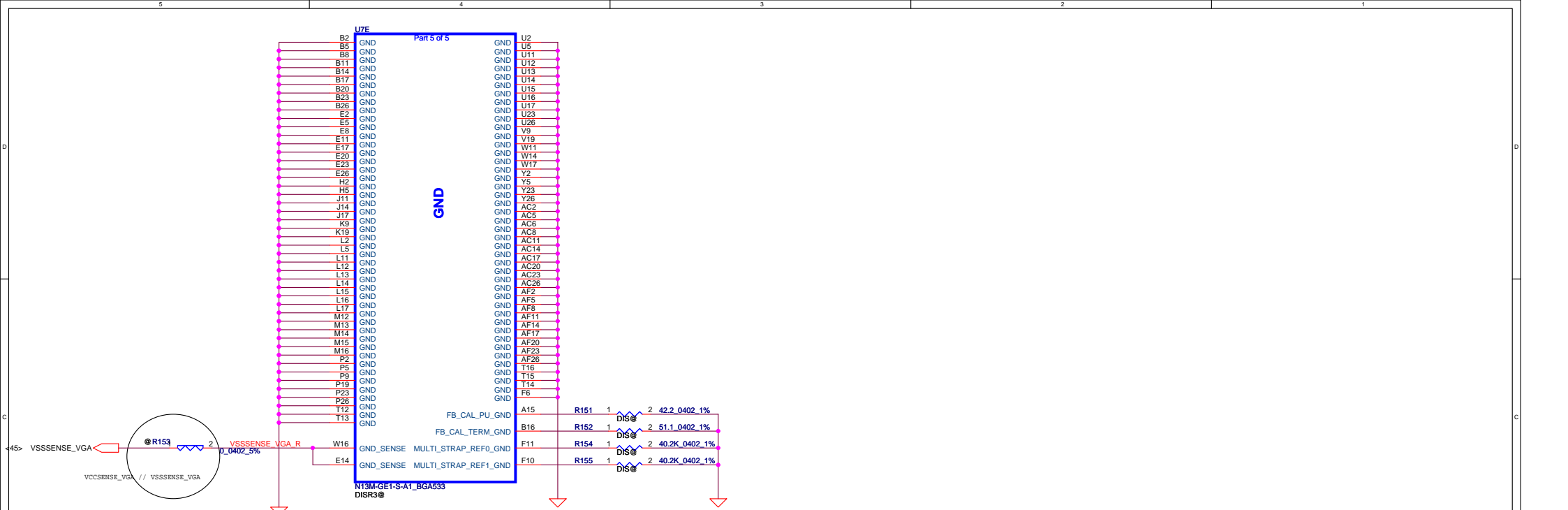
GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M* 16* 4	Micron MT41J128M16JT-107G.K	1111	0110	1000	0010	0001	0000	0101	1000
	900 MHz	128M* 16* 4	Hynix H5T2C663FFR-11C	R123 PU 45K	R128 PD 35K	R118 PU 5K	R130 PD 15K	R134 PD 10K	R135 PD 10K	R120 PD 30K	R121 PU 5K



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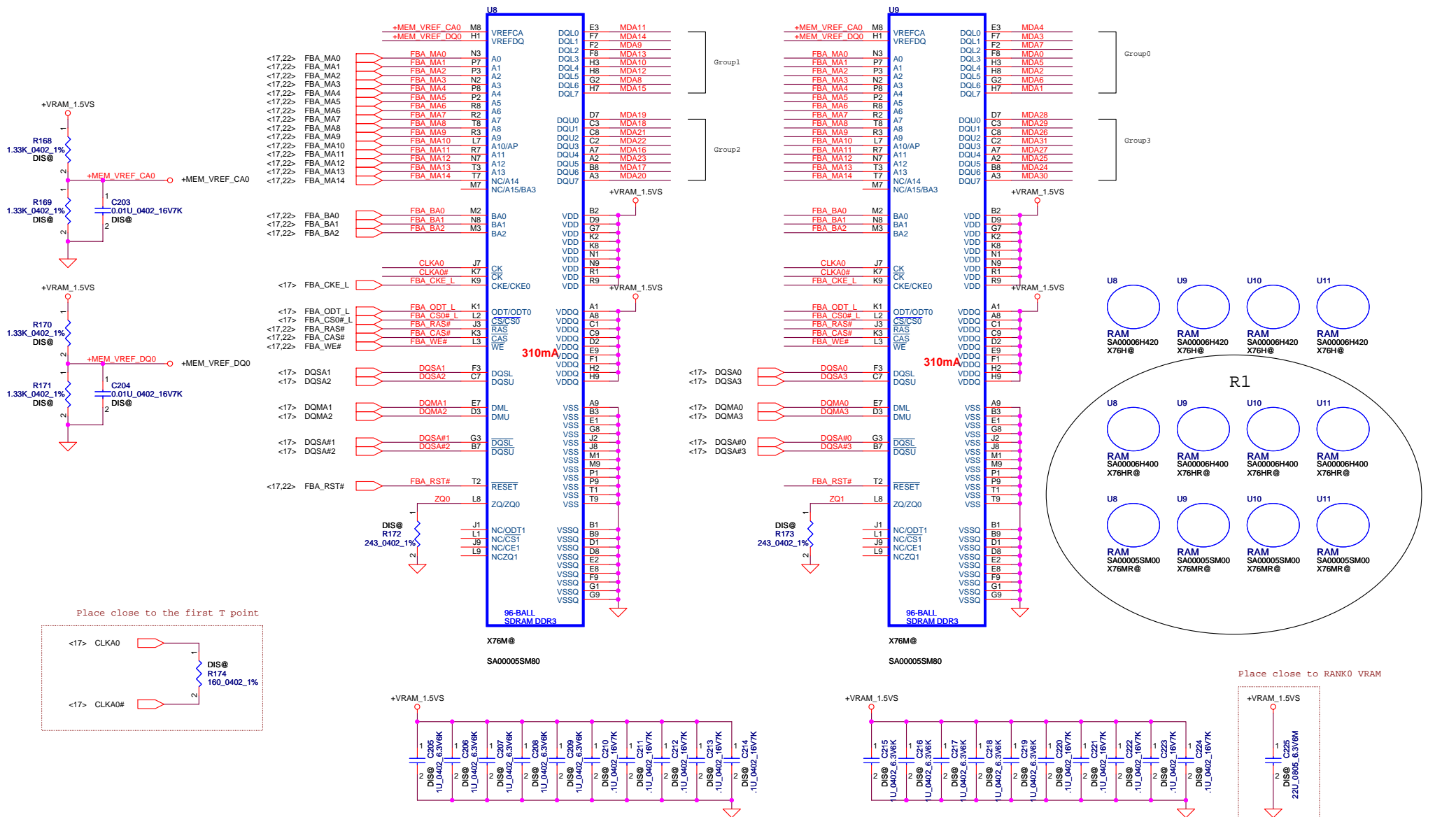
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	N13M POWER	
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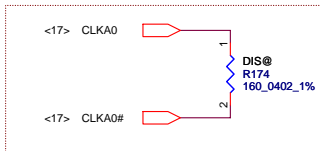
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	N13M POWER & GND	
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RANK 0 [31...0] VRAM DDR3 Chips

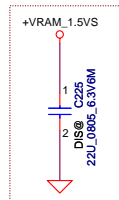
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Place close to the first T point



Place close to RANK0 VRAM

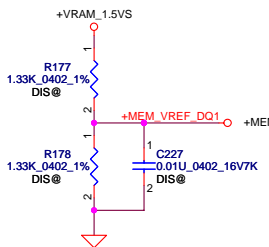
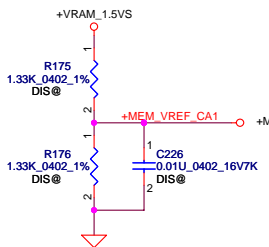
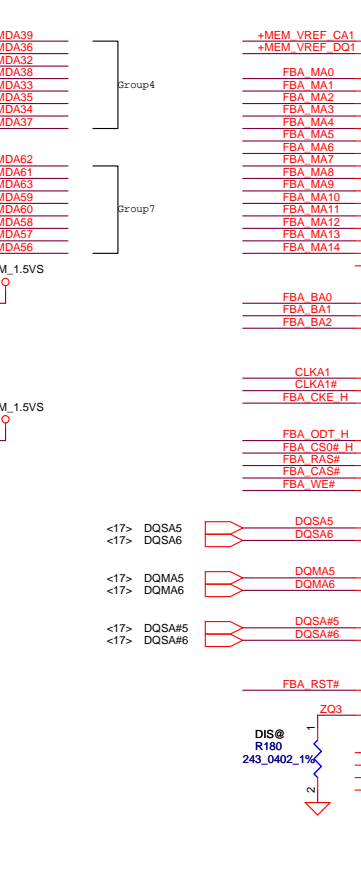
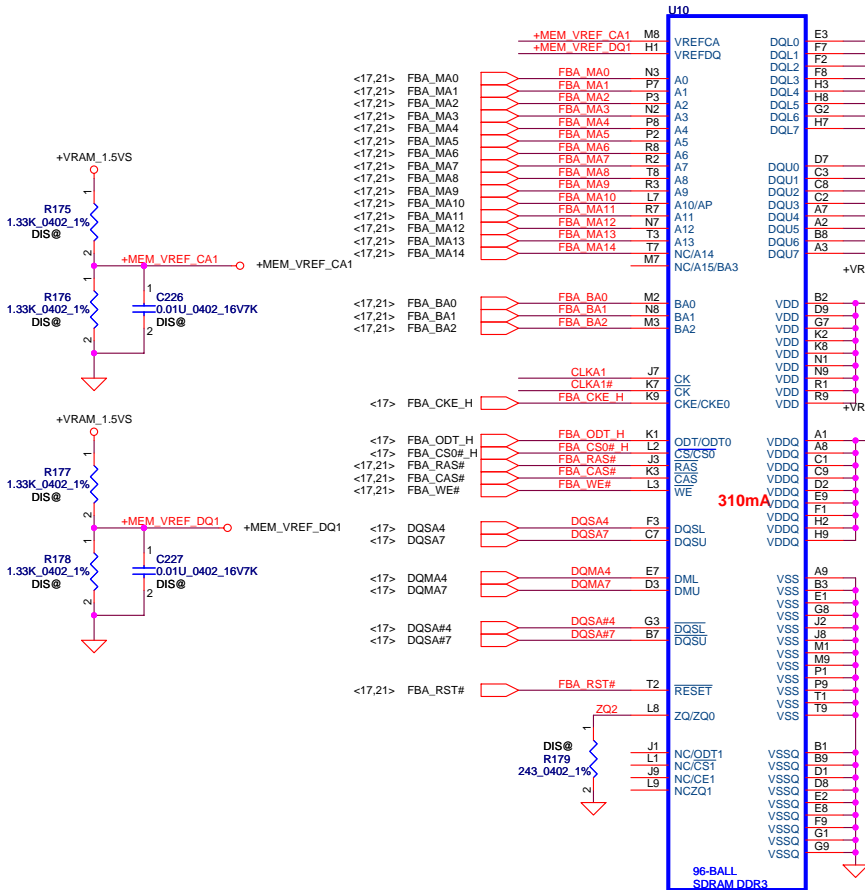


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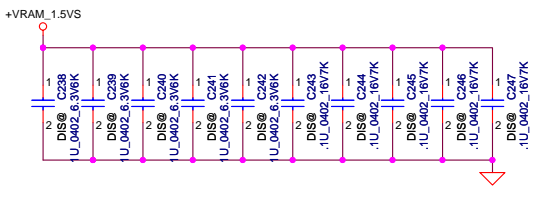
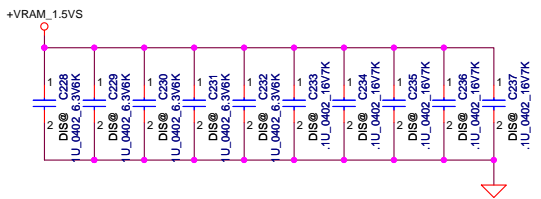
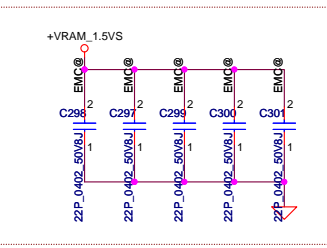
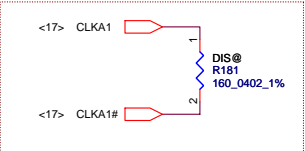
RANK 0 [63...32]

VRAM DDR3 Chips

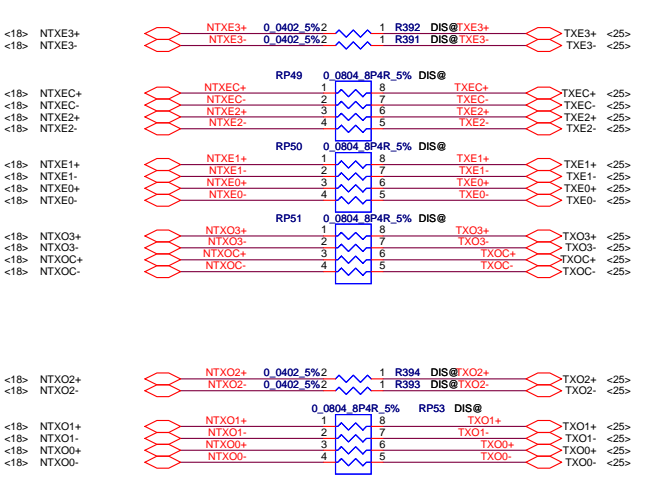
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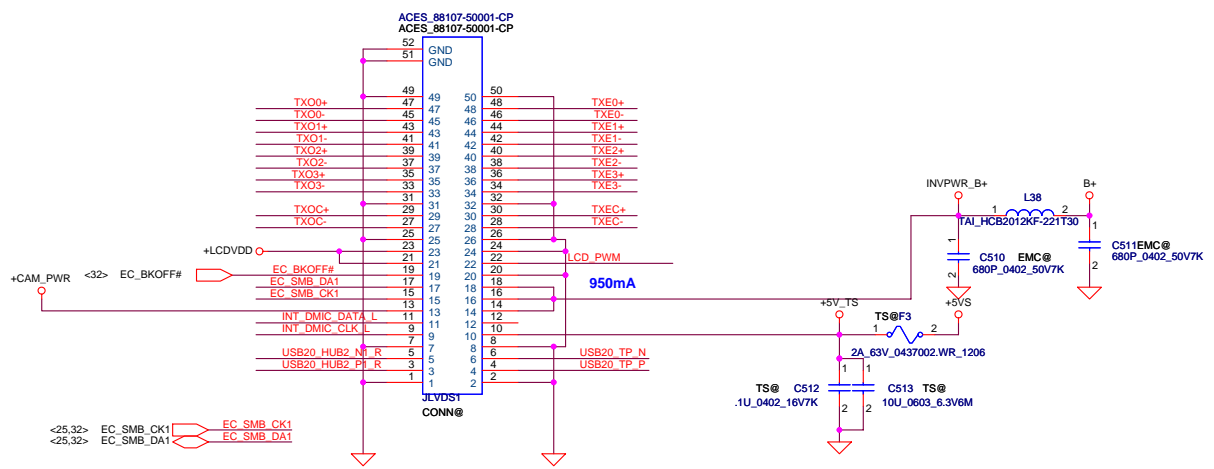
Place close to the first T point



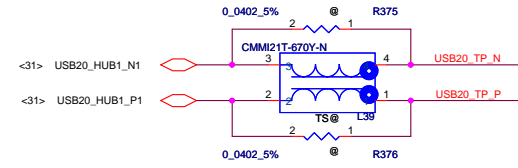
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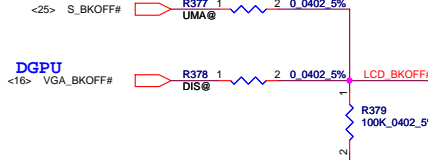
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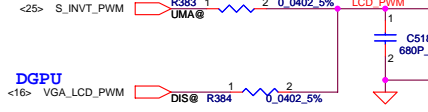
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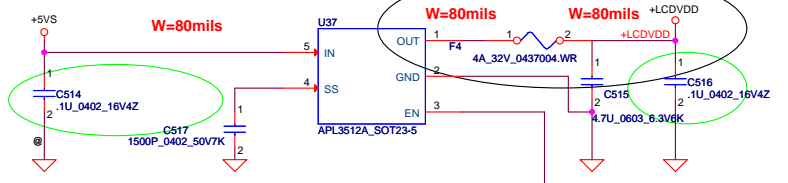
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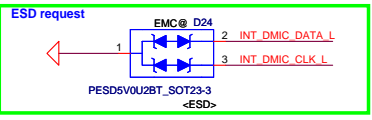
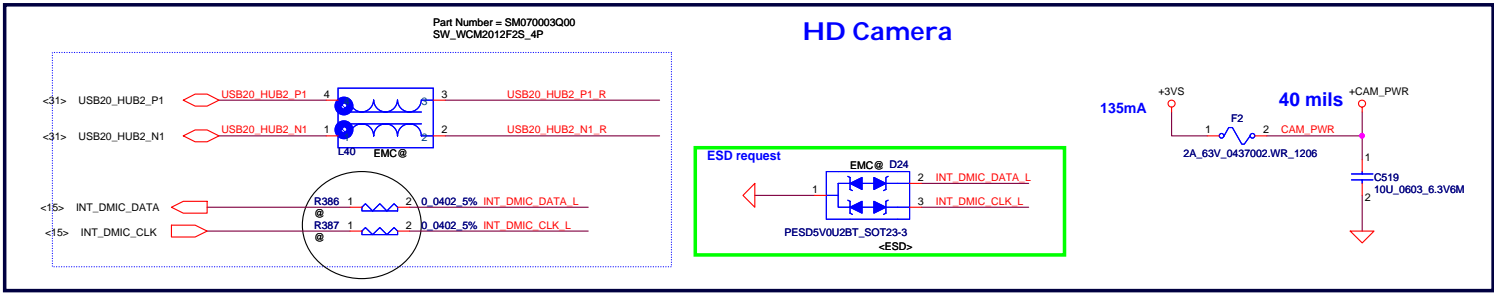
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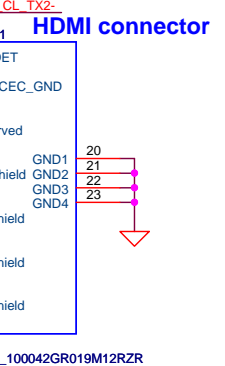
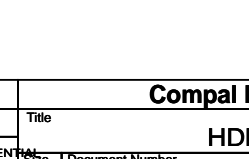
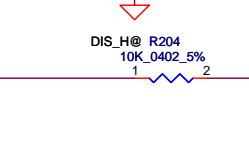
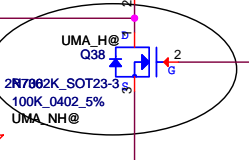
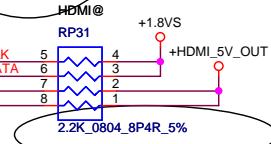
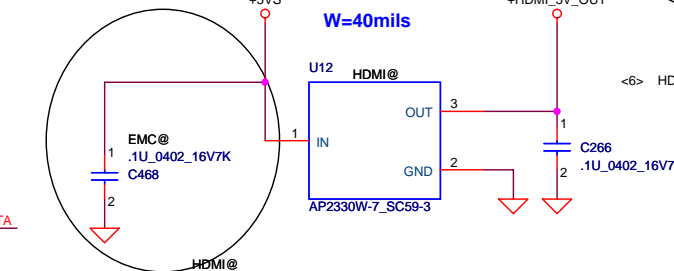
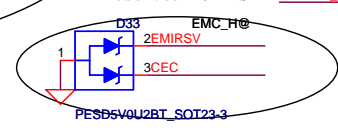
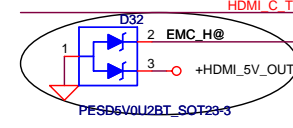
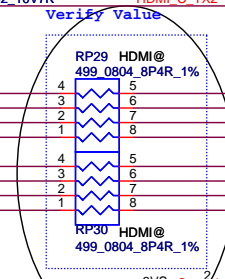
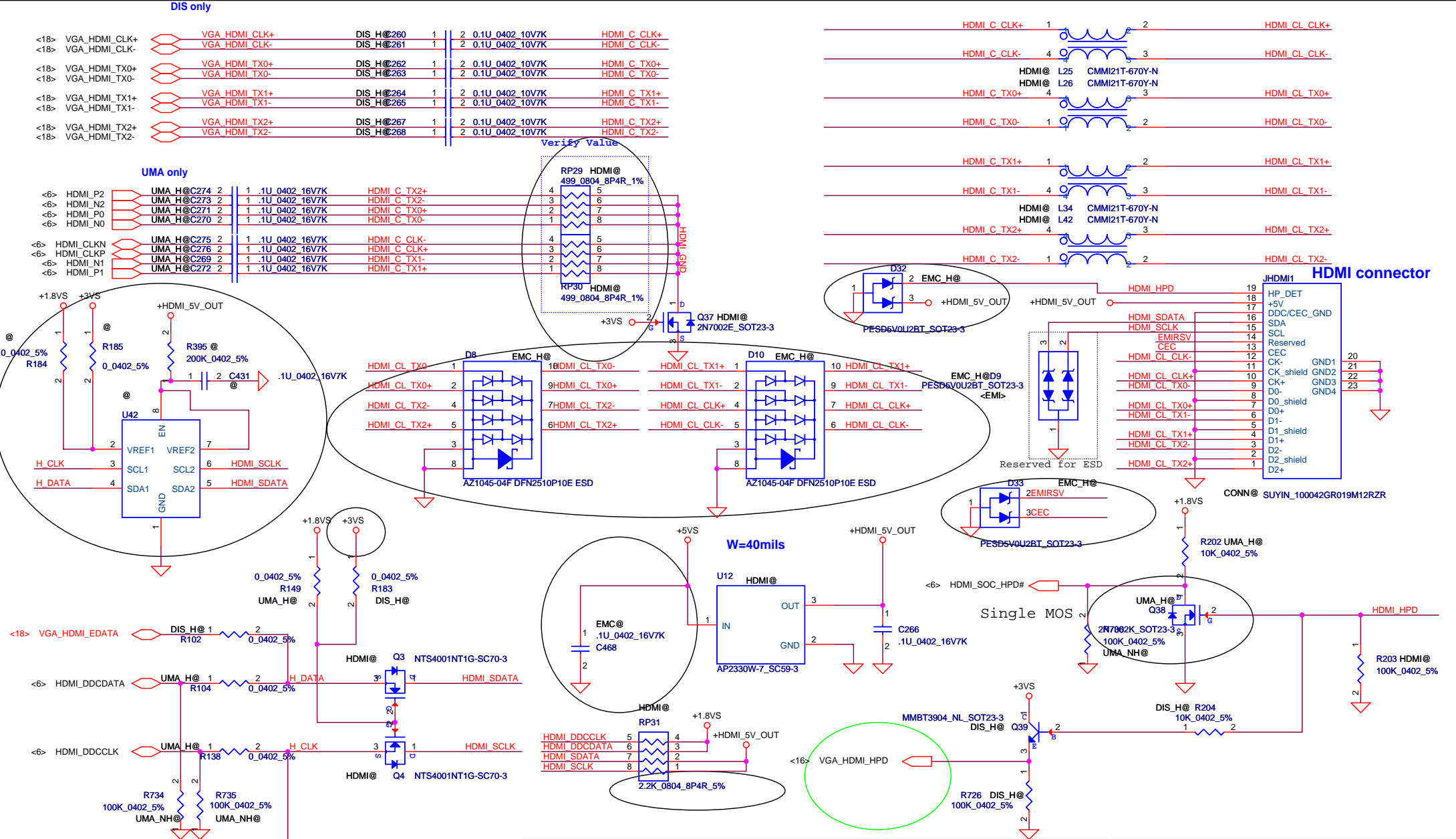
LVDS-POWER



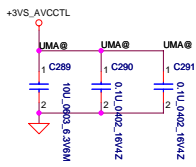
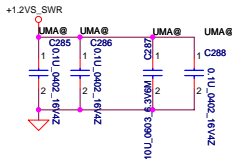
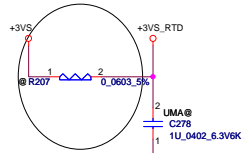
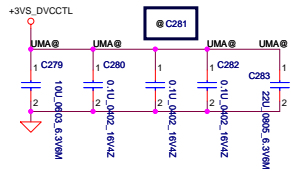
HD Camera



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				HDMI CONN.
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Power Consumption:

Pin 22 (PVCC) < 50 mA
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

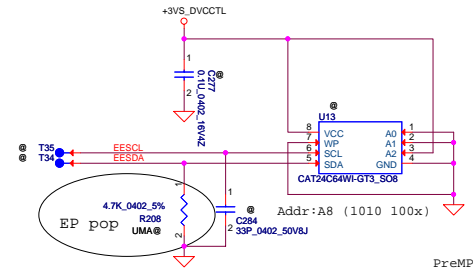
Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

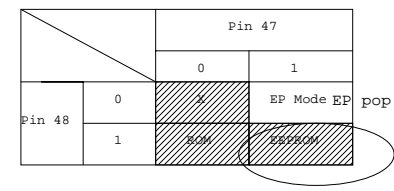
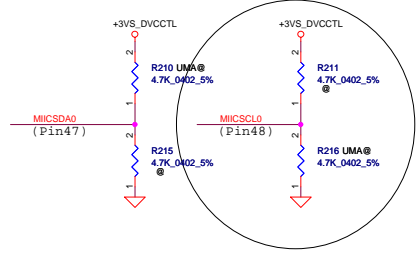
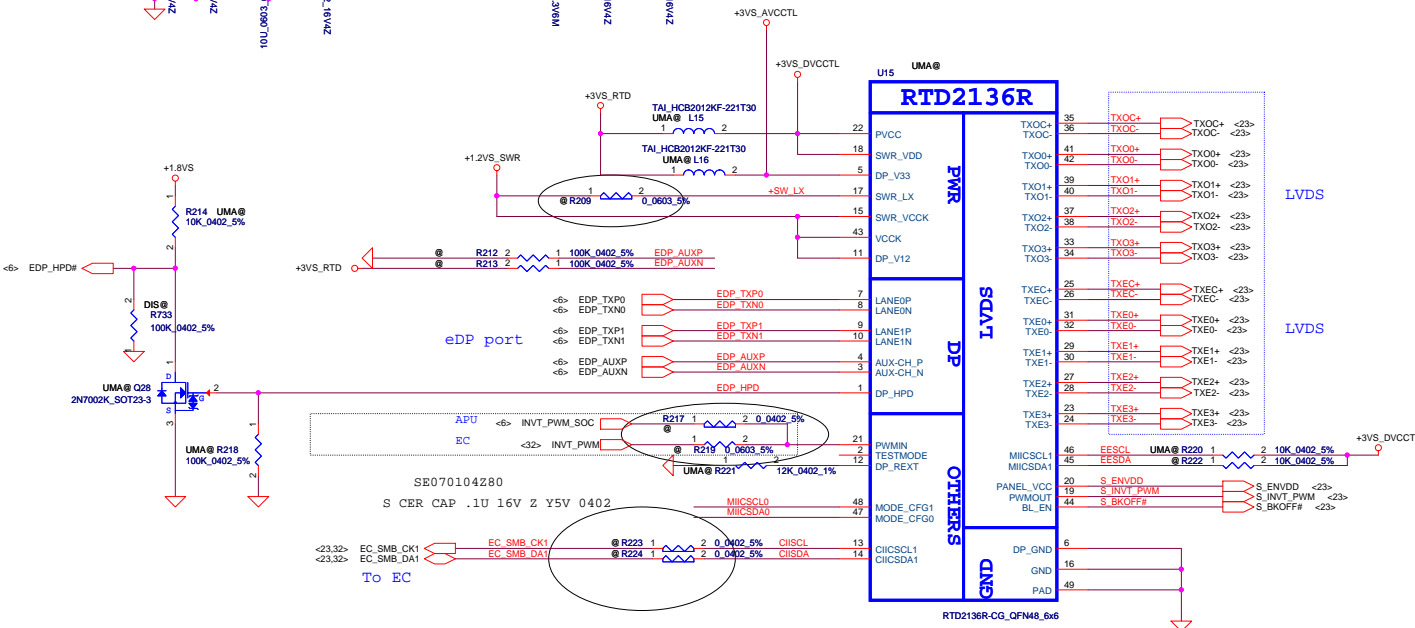
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)

Pin 43 (VCCK) < 50mA

Pin 11 (DPV12) < 100mA

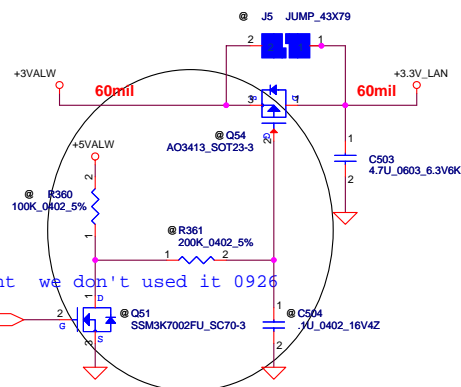


PreMP



RTD2136R
 S IC RTD2136R-CG QFN 48P DP/LVDS CTRL

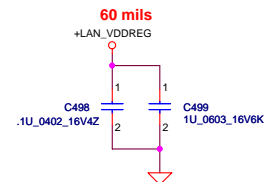
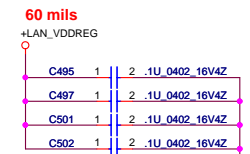
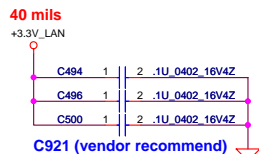
WOL circuit (Connect +3V_LAN to +3VALW)



Remove component we don't used it 0926

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

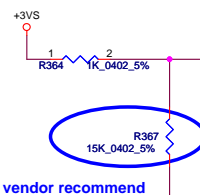
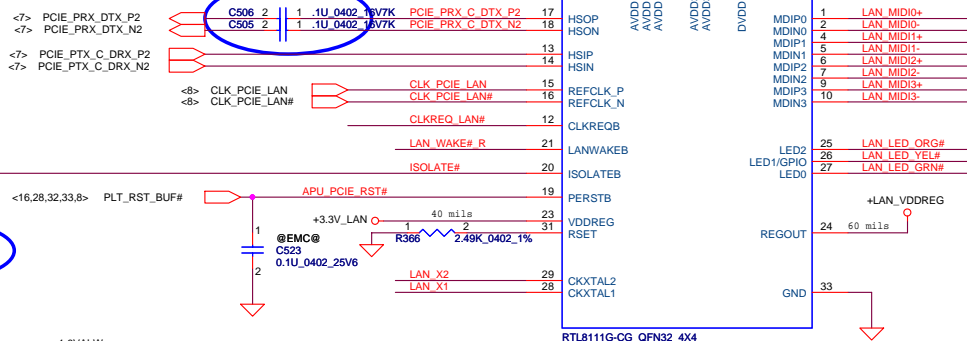


C494, C496, C500 close to U36
Pin 11,32 ,23, respectively

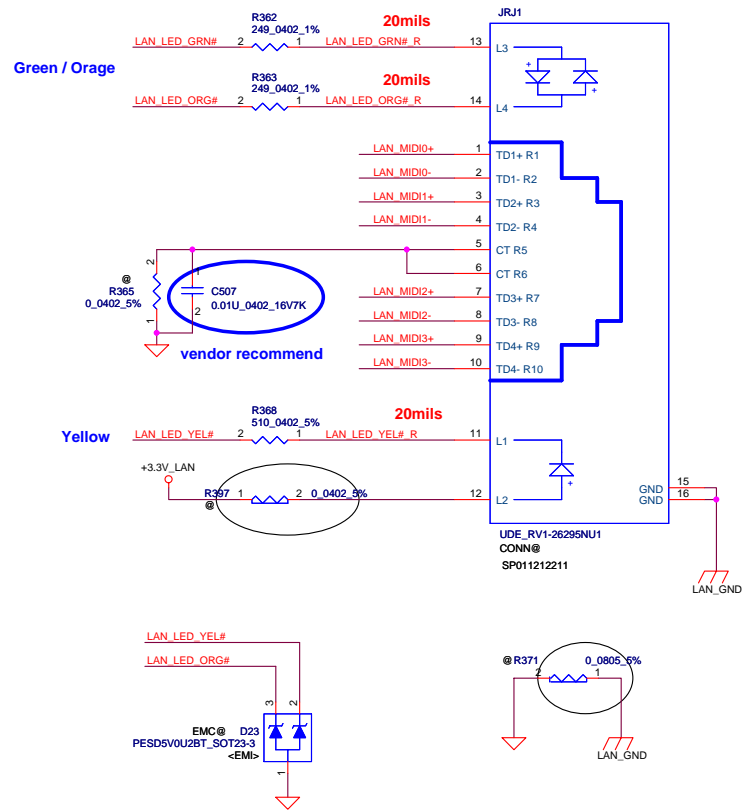
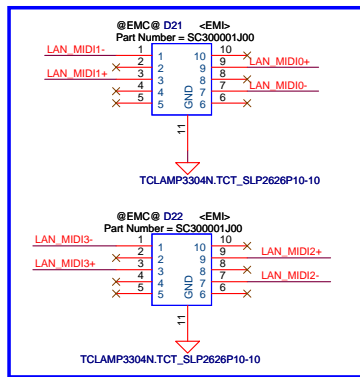
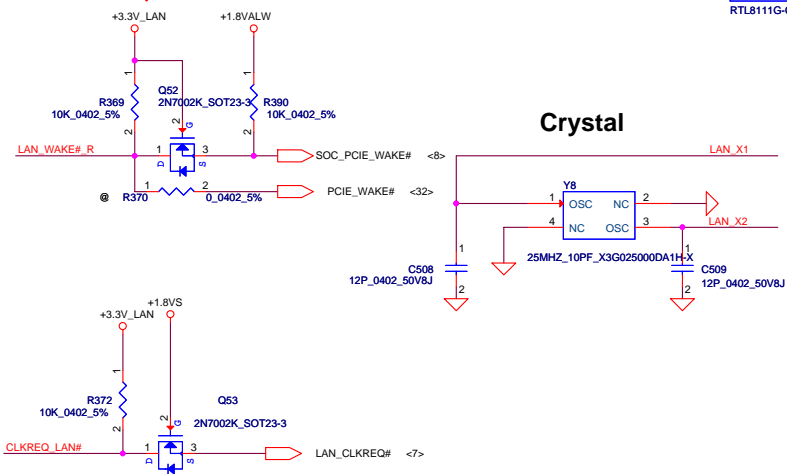
C495, C497, C501, C502, close to U36
Pin 3,8,24,30, respectively

C498, C499 close to U36
Pin22

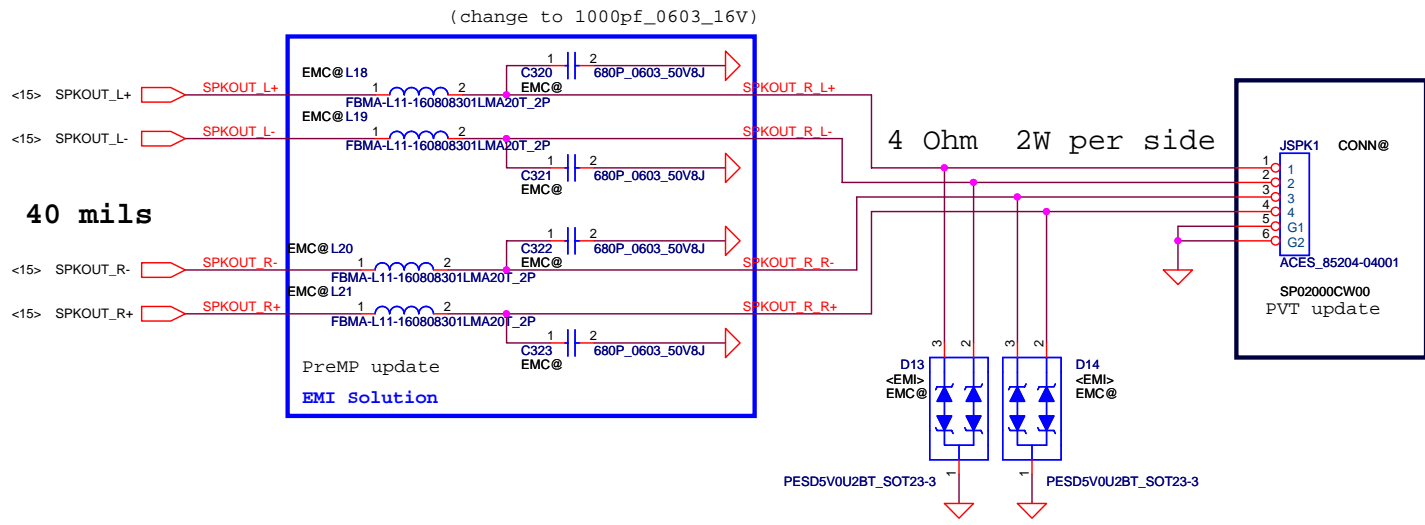
C505, C506, close to U36
Pin 17,18, respectively



Crystal

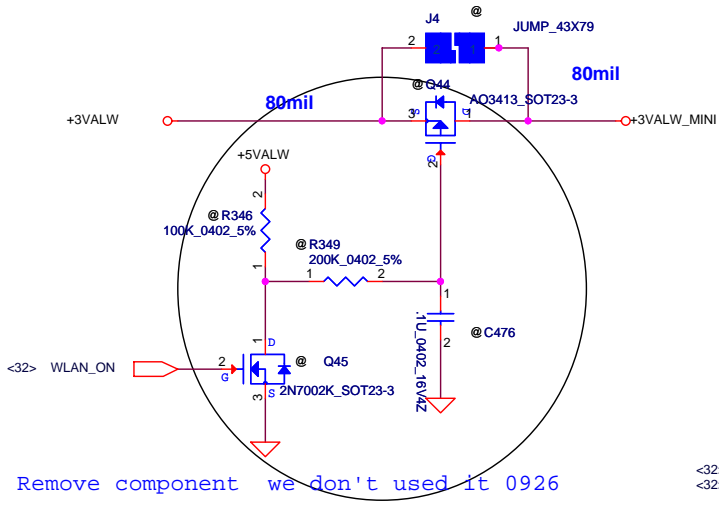


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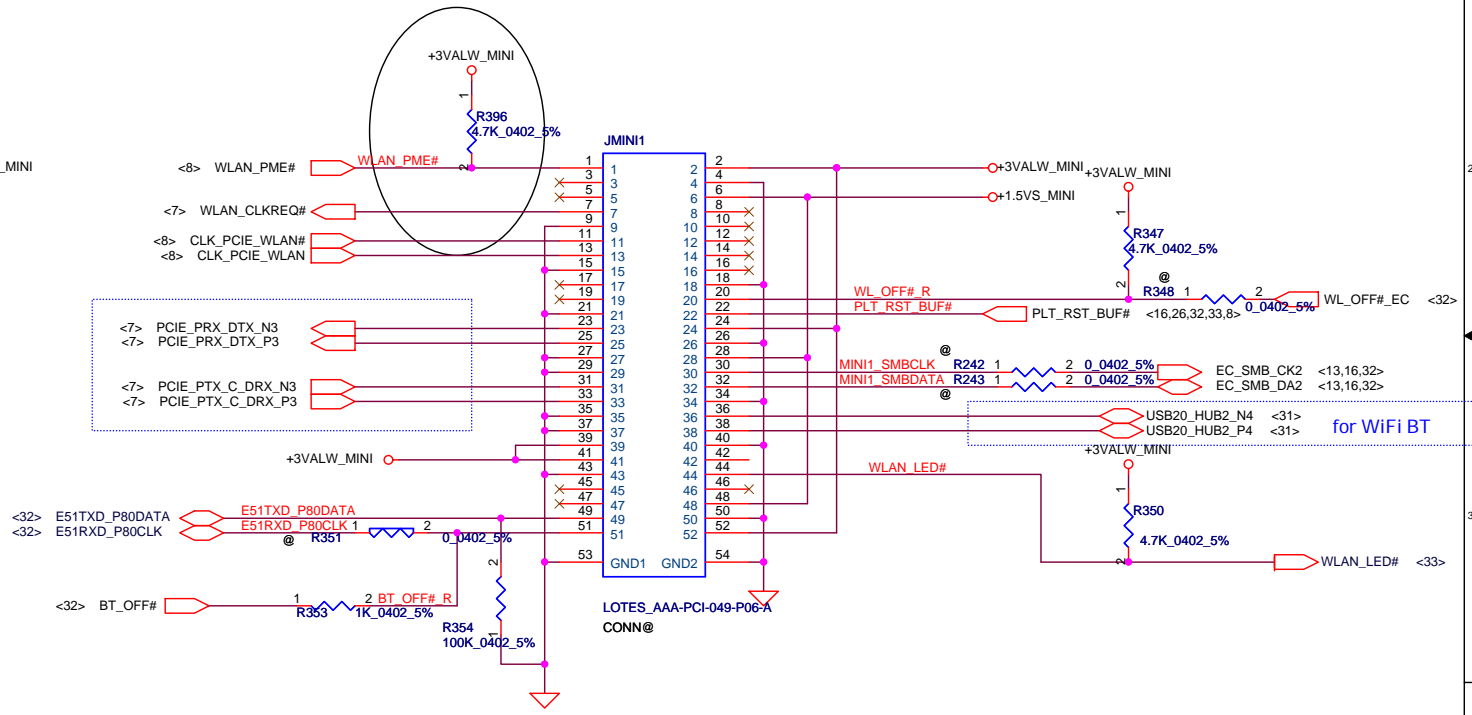
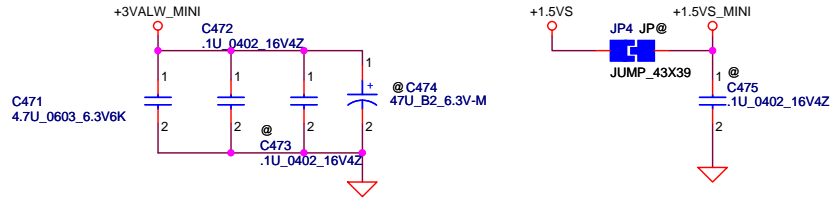


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For Wireless LAN

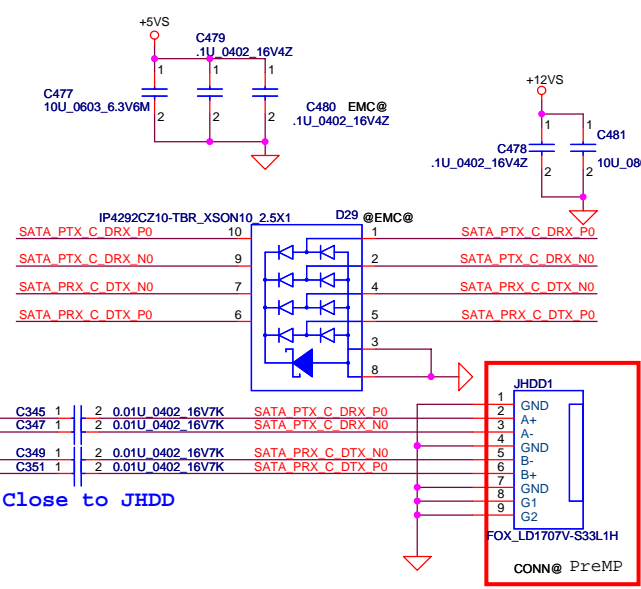
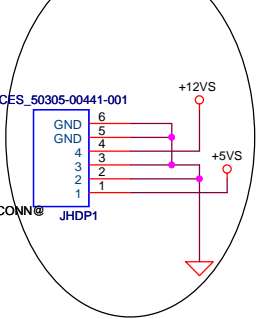


Remove component we don't used it 0926

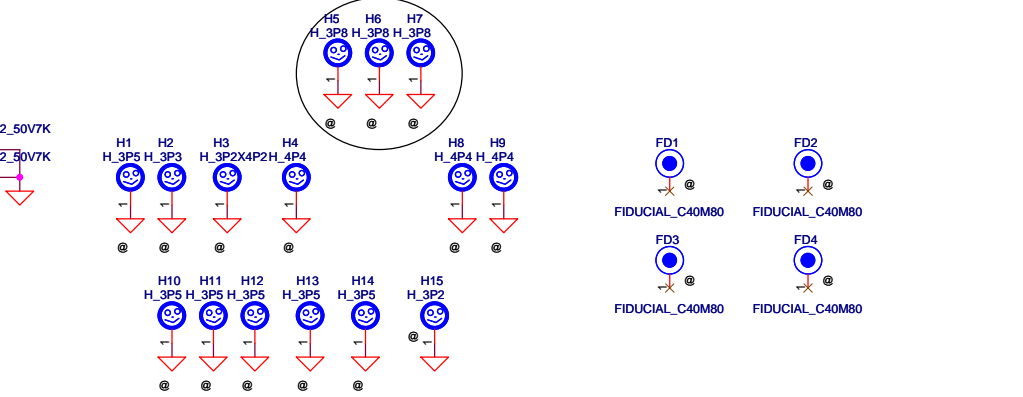
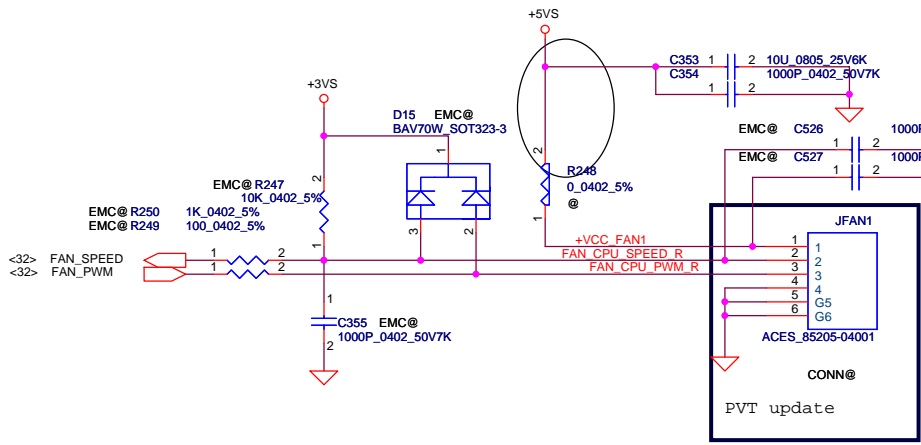
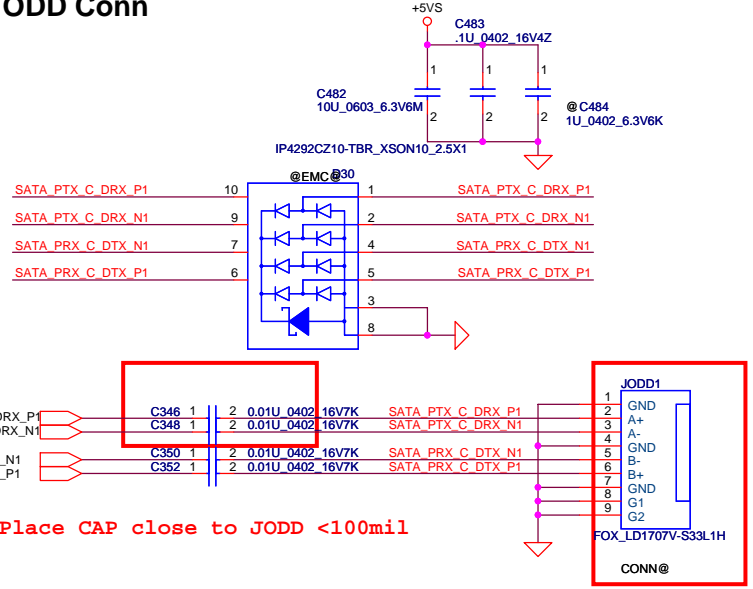
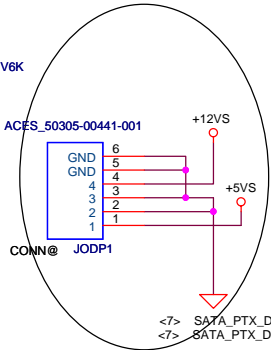


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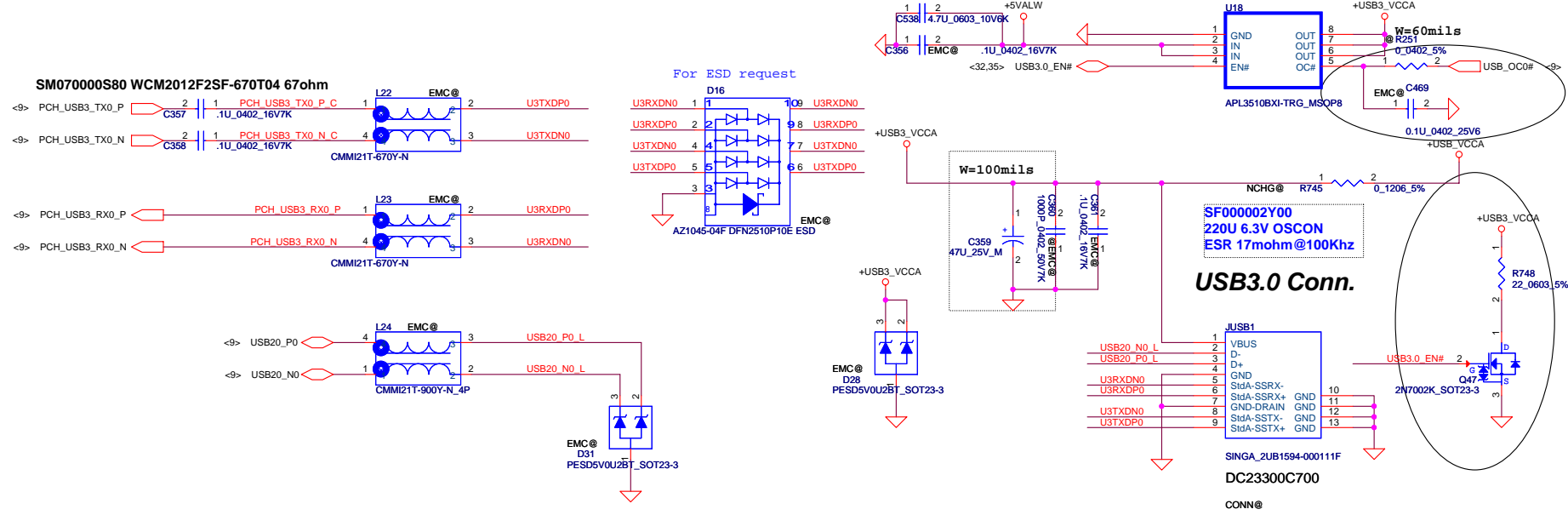
SATA HDD Conn.



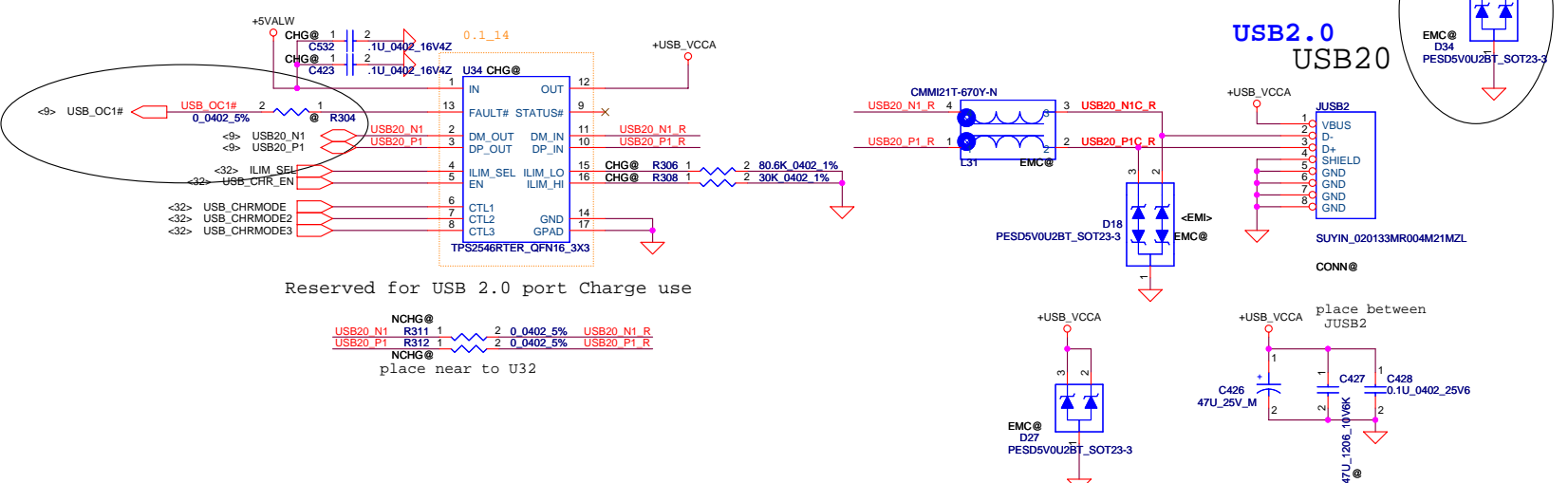
SATA ODD Conn

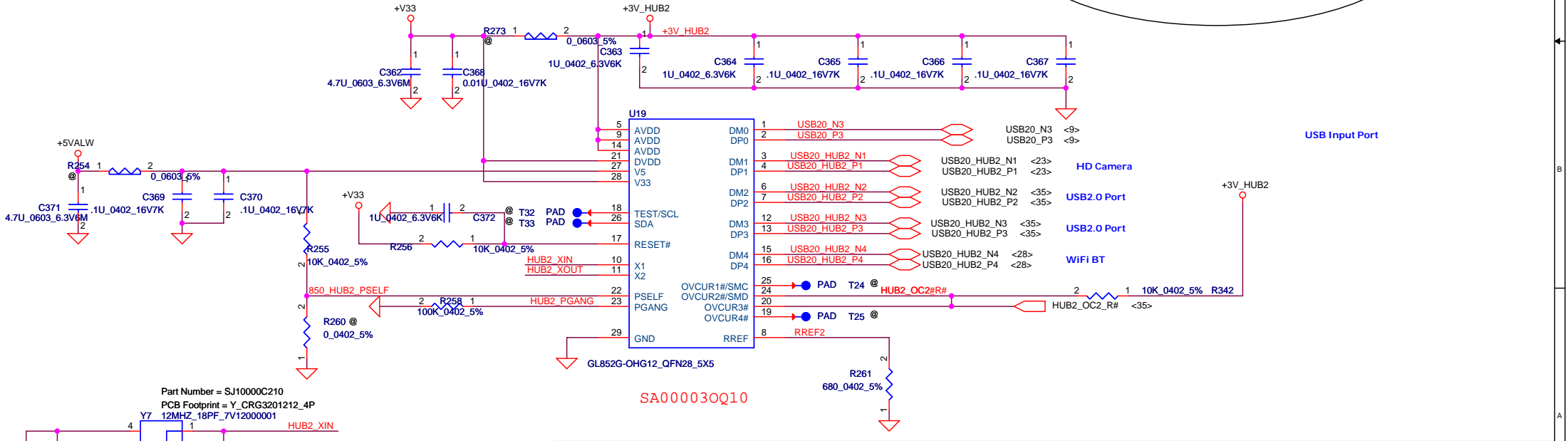
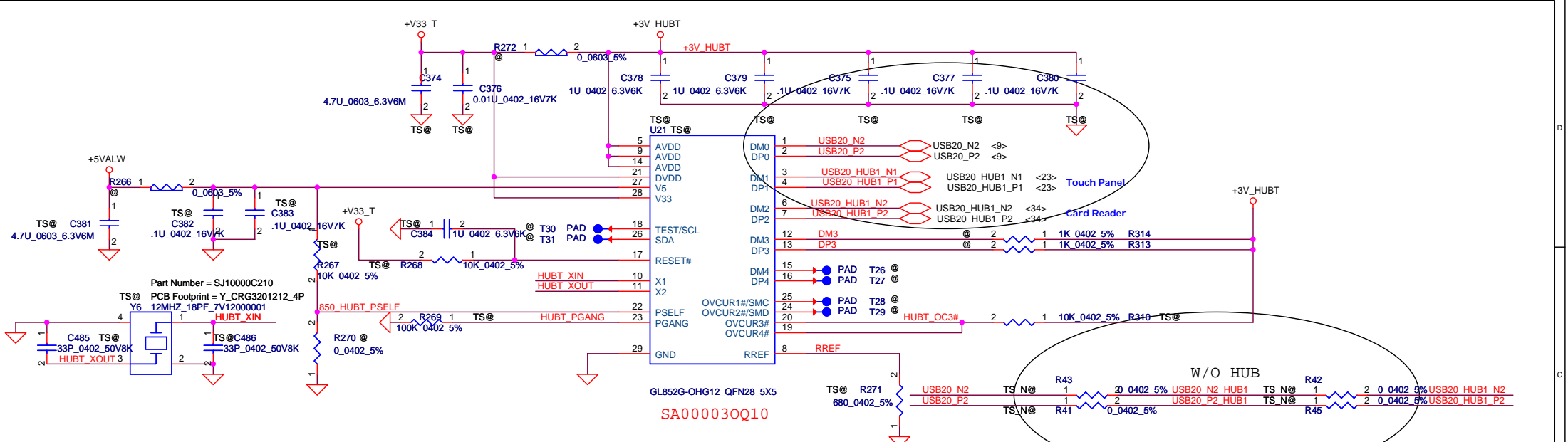


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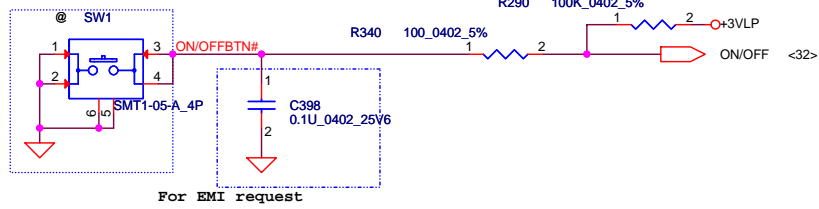
System Global Power State	TPS2546/TPS2544 Mode	Charging	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP		1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs		1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake		0	0	1	1	ILIM_HI





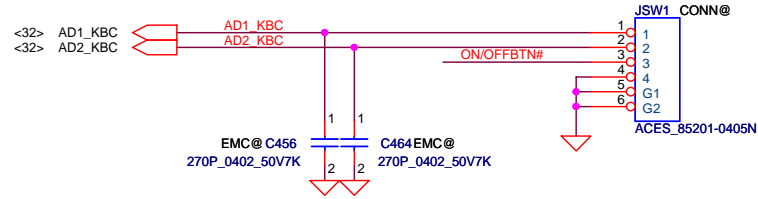
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TOP side
For debug

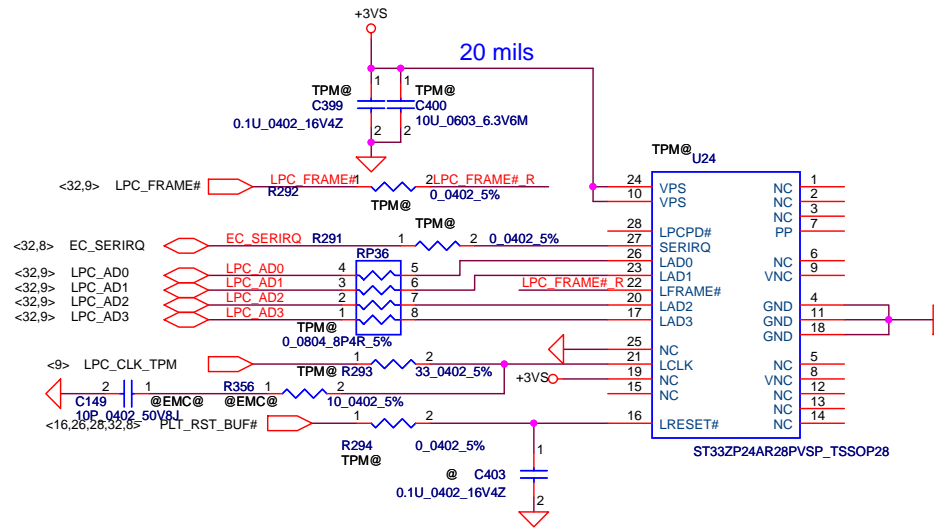


Power Brd Connector

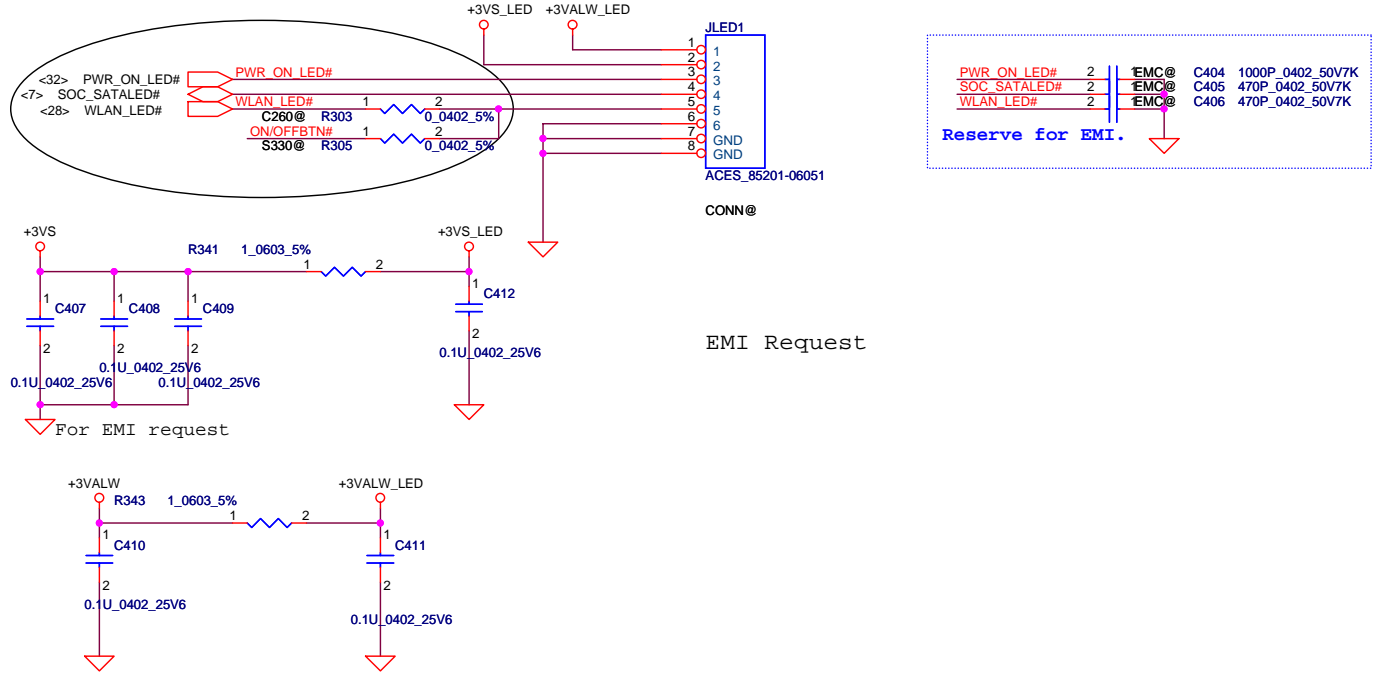
PU 4.7K on EC side



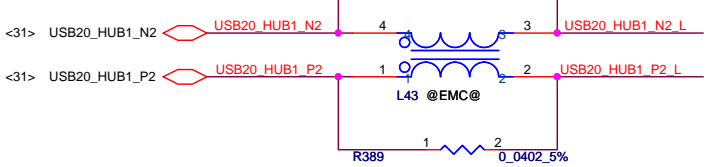
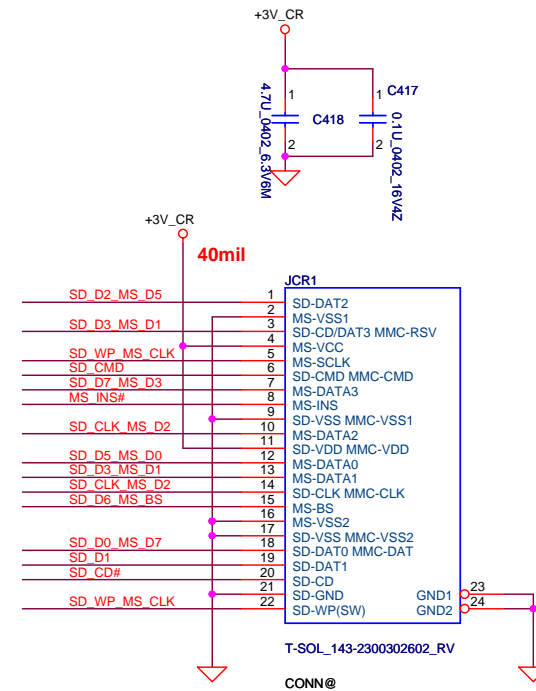
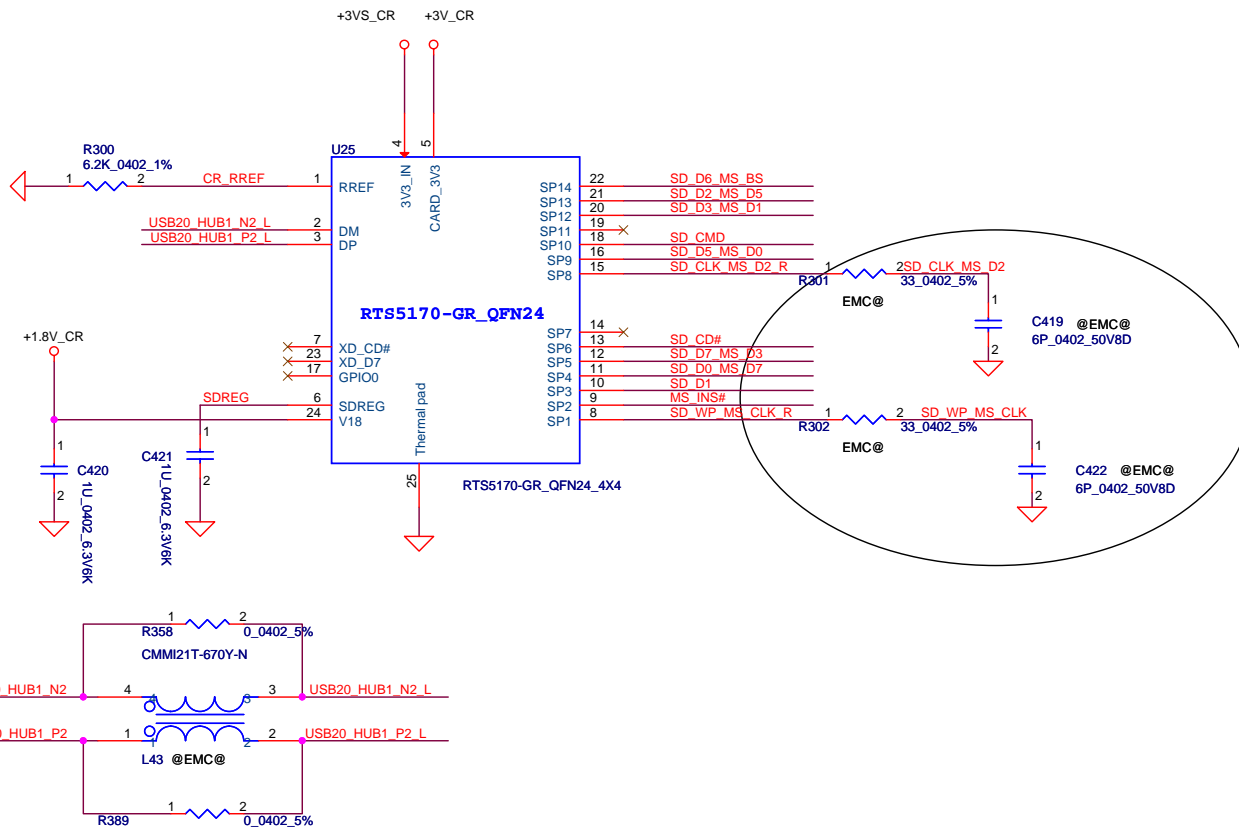
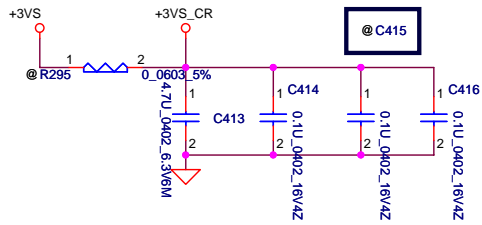
TPM (Reserve)



LED Brd Connector

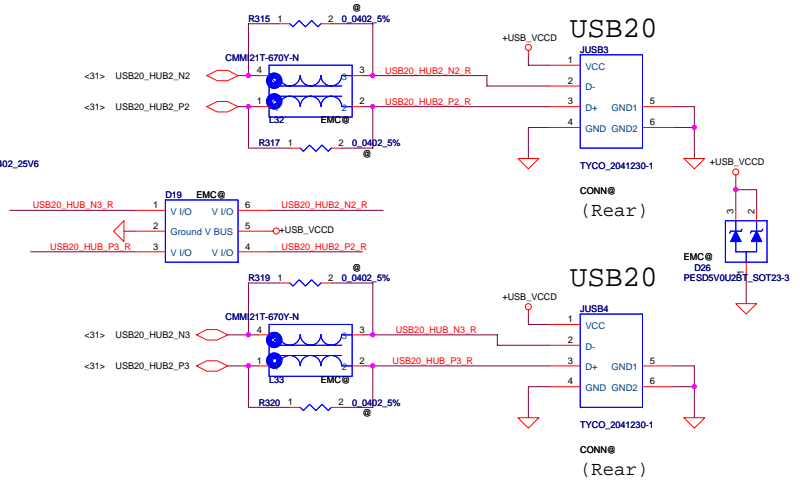
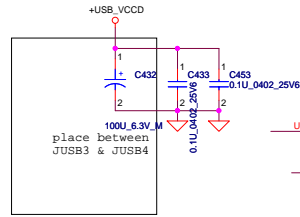
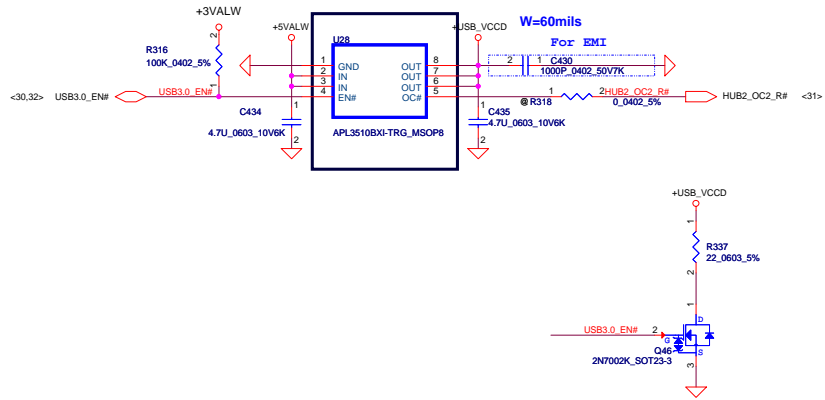


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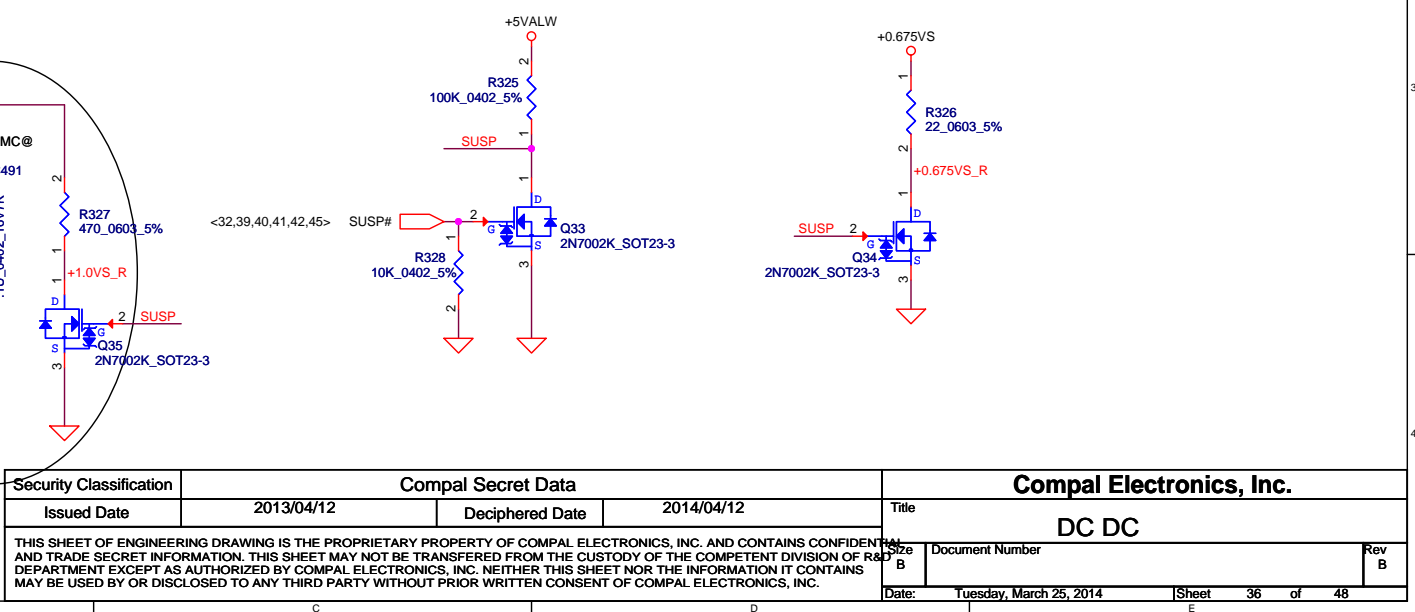
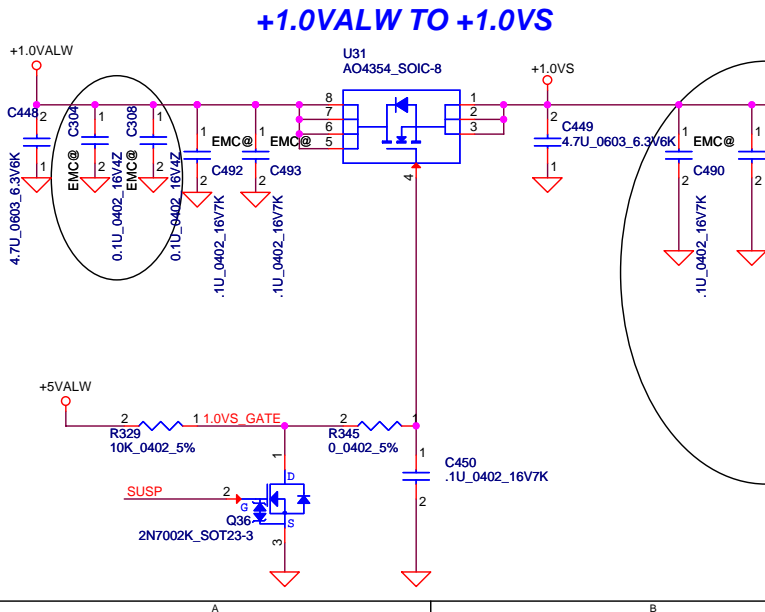
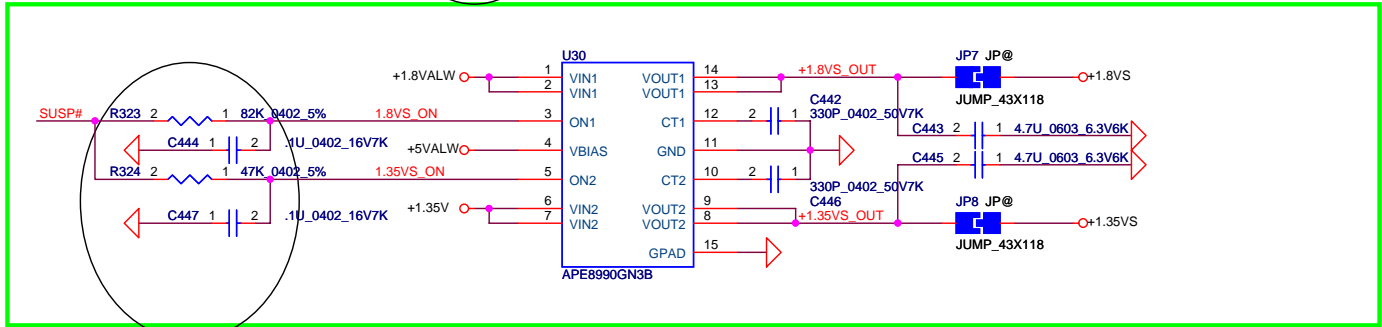
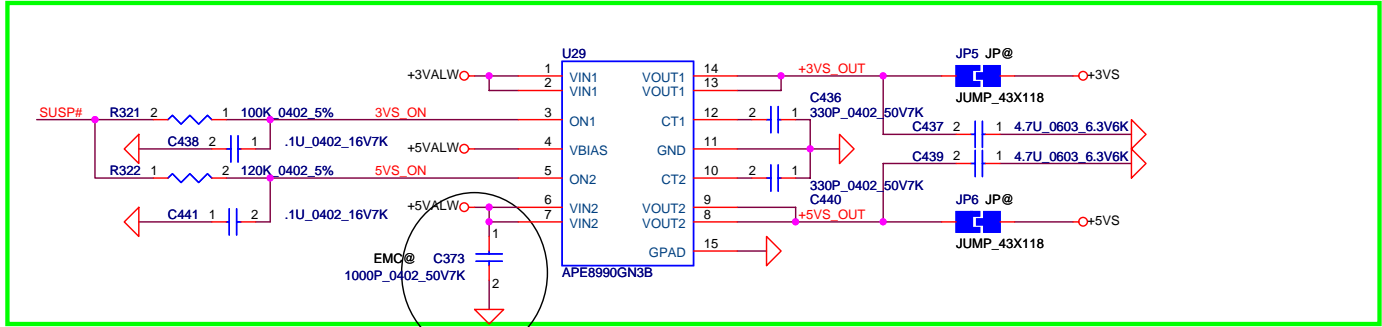
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USB2.0 Power

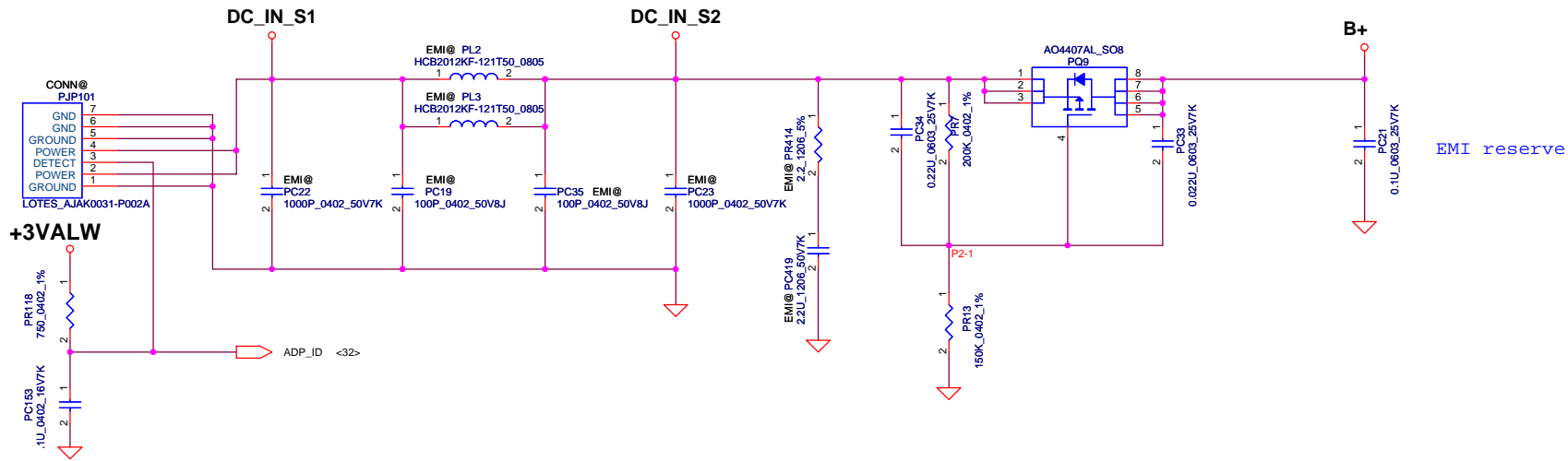


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Normal Platform (Not support M-STATE and Deep Sleep)



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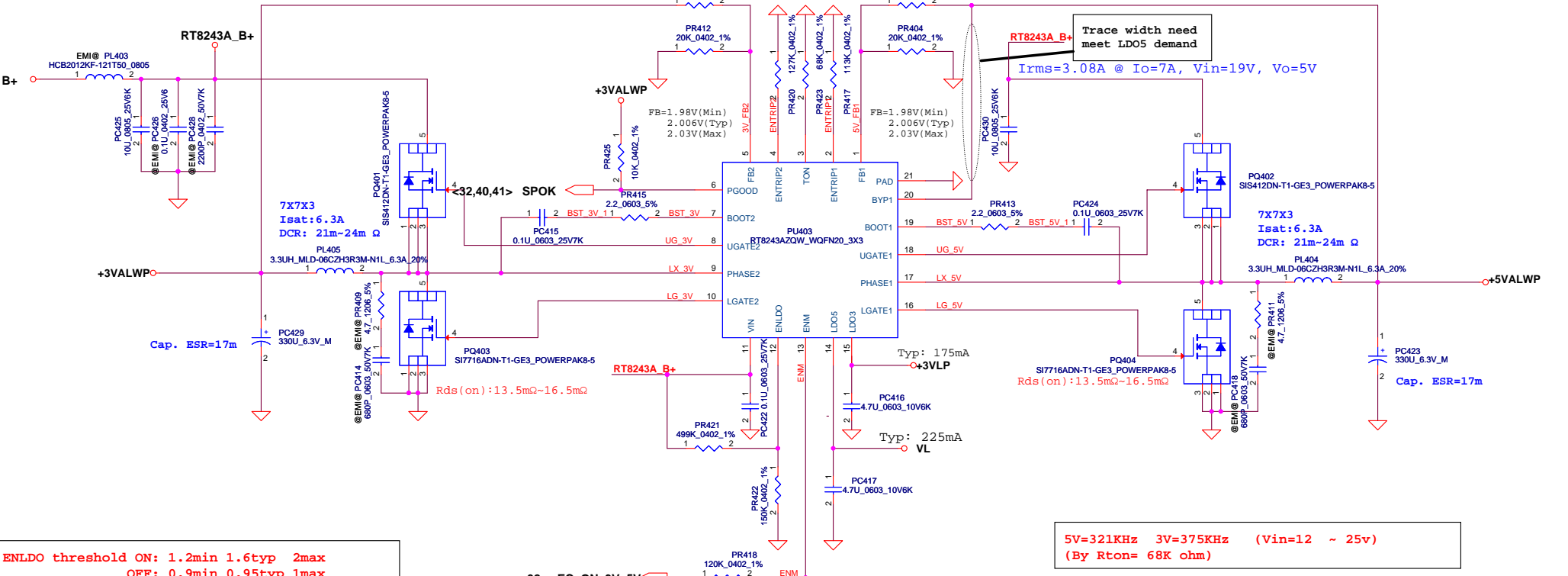
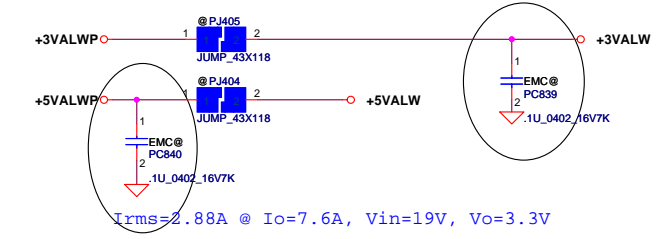
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Module model information

RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

ENTRIPx adjustment range: 0.5V~3V, floating or over 4.5V will shutdown channel.



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+V_3.3VP
Ipeak=6A; Imax=3.1A; Iocp(set)>=10A
Fsw=300K

Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=2.22A
LIR=Delta IL/Ipeak=0.37

L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=3.3uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=379.53uF

CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.1uF

5V=321KHz 3V=375KHz (Vin=12 ~ 25v)
(By Rton= 68K ohm)

+V_5VP
Ipeak=6A ; Imax=4.9A, Iocp(set)>=10A
Fsw=321K,
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=3.54A
LIR=Delta IL/Ipeak=0.59

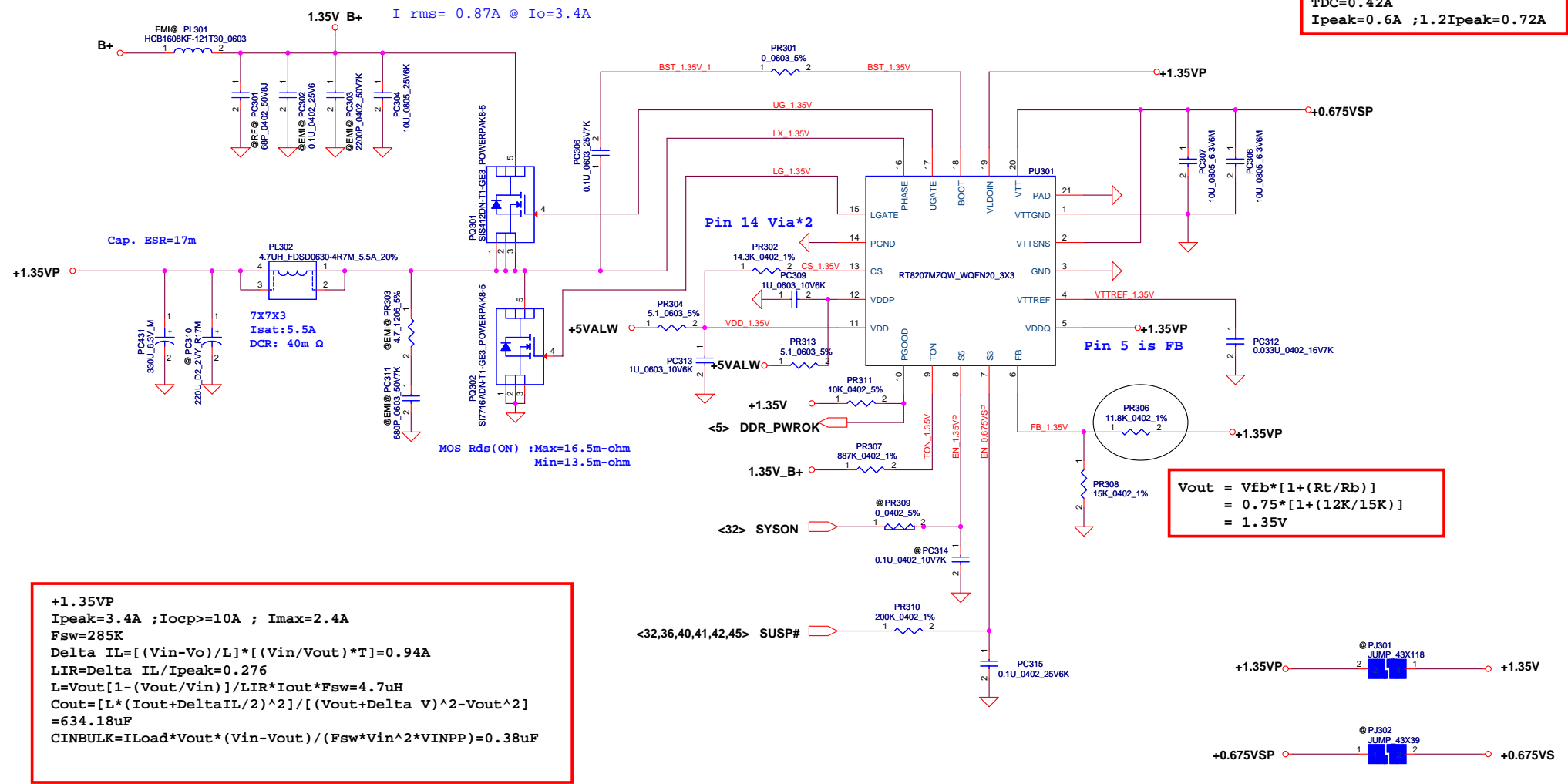
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=3.3uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=197.26uF

CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.75uF

For EC use +3VALW, mark "@" for +3VL

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+0.675VSP
 TDC=0.42A
 Ipeak=0.6A ; 1.2Ipeak=0.72A



+1.35VP
 Ipeak=3.4A ; Iocp>=10A ; Imax=2.4A
 Fsw=285K
 $\Delta IL = [(Vin - Vout) / L] * [(Vin / Vout) * T] = 0.94A$
 $LIR = \Delta IL / Ipeak = 0.276$
 $L = Vout [1 - (Vout / Vin)] / LIR * Iout * Fsw = 4.7uH$
 $Cout = [I * (Iout + \Delta IL / 2) ^ 2] / [(Vout + \Delta V) ^ 2 - Vout ^ 2] = 634.18uF$
 $CINBULK = ILoad * Vout * (Vin - Vout) / (Fsw * Vin ^ 2 * VINPP) = 0.38uF$

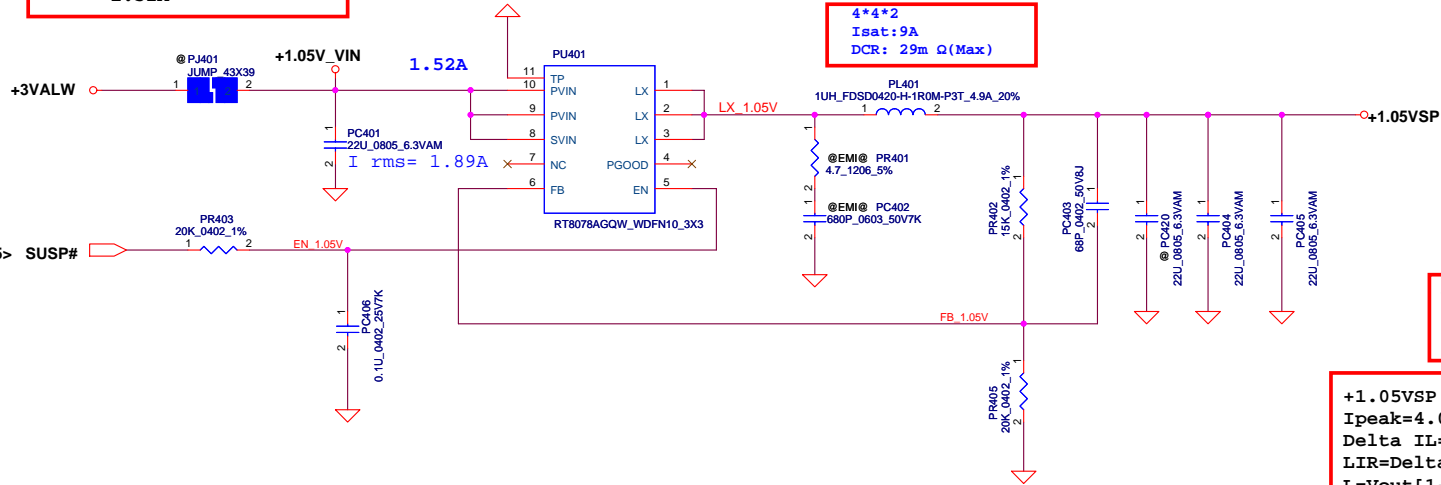
$V_{out} = V_{fb} * [1 + (R_t / R_b)]$
 $= 0.75 * [1 + (12K / 15K)]$
 $= 1.35V$

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Issued Date	2013/08/12	Deciphered Date	2014/08/12	+1.35VP / +0.675VSP	
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+1.05VSP
 $V_{in} = 3.3V$
 $I_{in} = 4.05 * 1.05 / 0.85 / 3.3$
 $= 1.52A$

+1.05VSP

4*4*2
 $I_{sat}: 9A$
 $DCR: 29m \Omega (Max)$



$$V_{out} = V_{fb} * [1 + (R_t/R_b)]$$

$$= 0.6 * [1 + (15K/20K)]$$

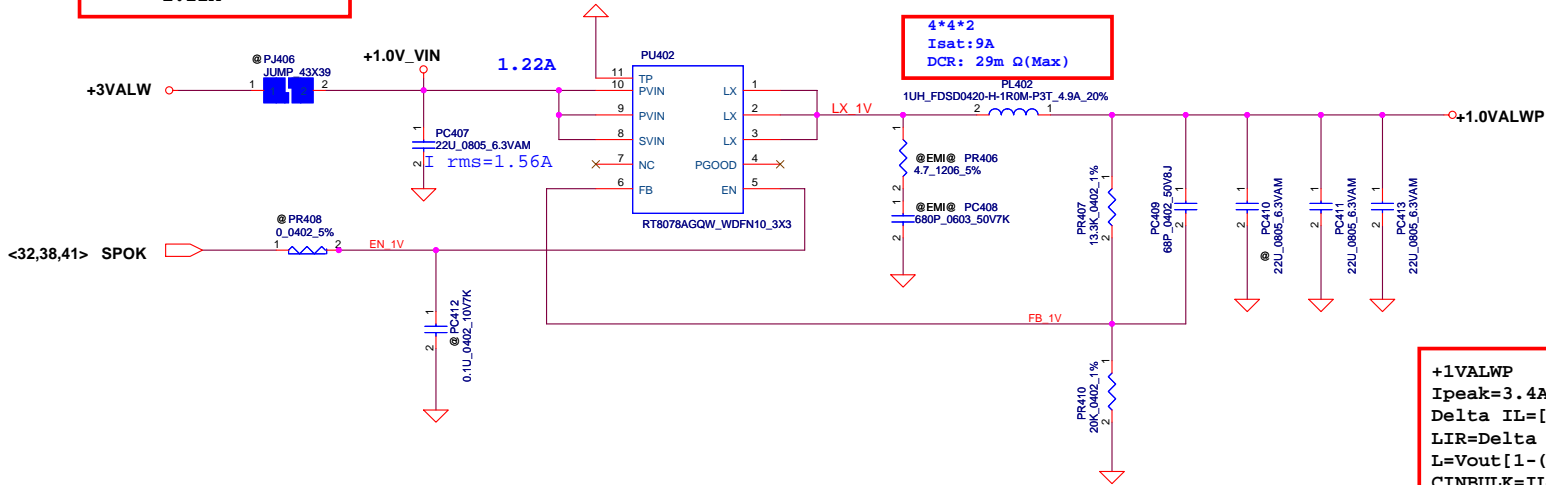
$$= 1.05V$$

+1.05VSP
 $I_{peak} = 4.05A$; $CL(min) \geq 4.4A$; $F_{sw} = 1MHz$
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{in} / V_{out}) * T] = 0.716A$
 $LIR = \Delta IL / I_{peak} = 0.177$
 $L = V_{out} [1 - (V_{out} / V_{in})] / LIR * I_{out} * F_{sw} = 1.0uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 2.66uF$

+1.0VALWP
 $V_{in} = 3.3V$
 $I_{in} = 3.4 * 1 / 0.85 / 3.3$
 $= 1.22A$

+1.0VALWP

4*4*2
 $I_{sat}: 9A$
 $DCR: 29m \Omega (Max)$



$$V_{out} = V_{fb} * [1 + (R_t/R_b)]$$

$$= 0.6 * [1 + (9.76K/14.7K)]$$

$$= 1V$$

+1VALWP
 $I_{peak} = 3.4A$; $CL(min) \geq 4.4A$; $F_{sw} = 1MHz$
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{in} / V_{out}) * T] = 0.697A$
 $LIR = \Delta IL / I_{peak} = 0.205$
 $L = V_{out} [1 - (V_{out} / V_{in})] / LIR * I_{out} * F_{sw} = 1.0uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 2.18uF$

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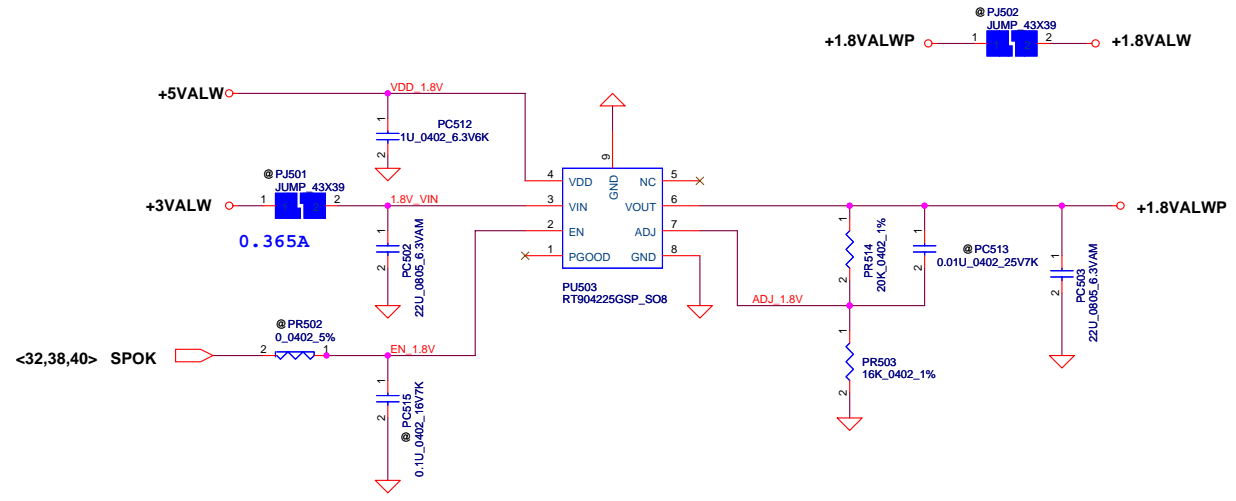
$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.8 * [1 + (20K / 16K)]$$

$$= 1.8V$$

+1.8VALWP
 Ipeak=0.365A ;
 Iocp>=3.1A

RT9042:
 Quiescent Current (GND Current)
 IQ(typ)=0.6mA, IQ(max)=1.2mA
 PD =(Vin-Vout)*Iout + Vin*IQ =0.551W
 θ JA= 75°C/W*0.551=41.35°C



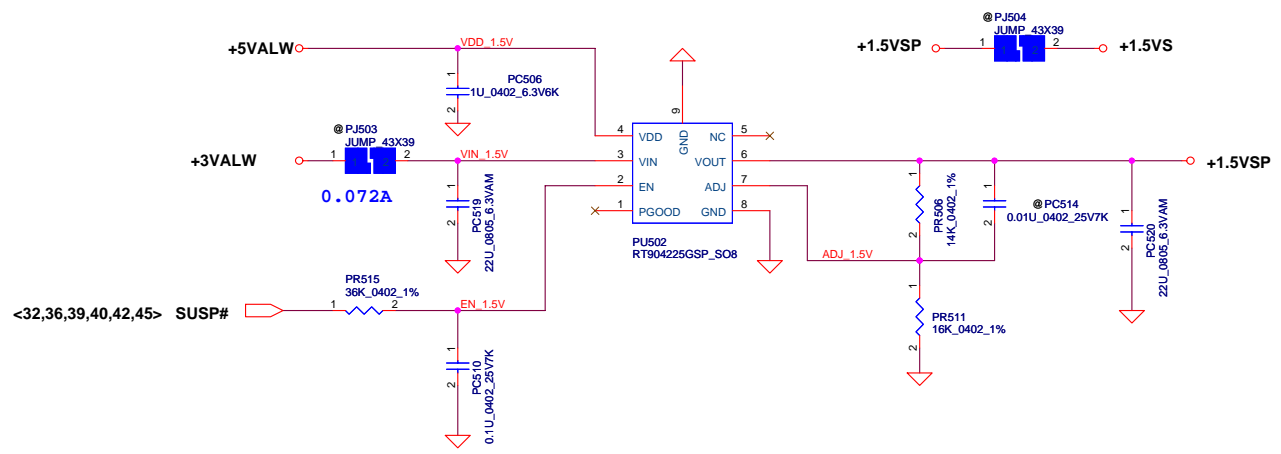
$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.8 * [1 + (14K / 16K)]$$

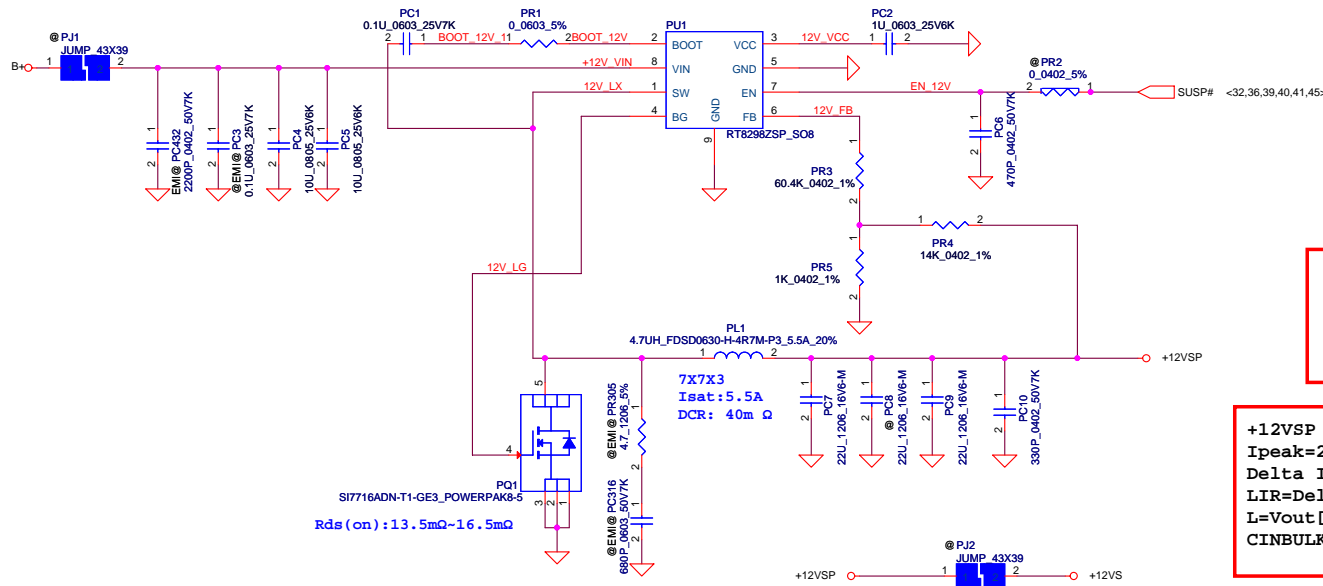
$$= 1.5V$$

+1.5VSP
 Ipeak=0.072A
 Iocp>=3.1A

RT9042:
 Quiescent Current (GND Current)
 IQ(typ)=0.6mA, IQ(max)=1.2mA
 PD =(Vin-Vout)*Iout + Vin*IQ =0.133W
 θ JA= 75°C/W*0.551=10.01°C



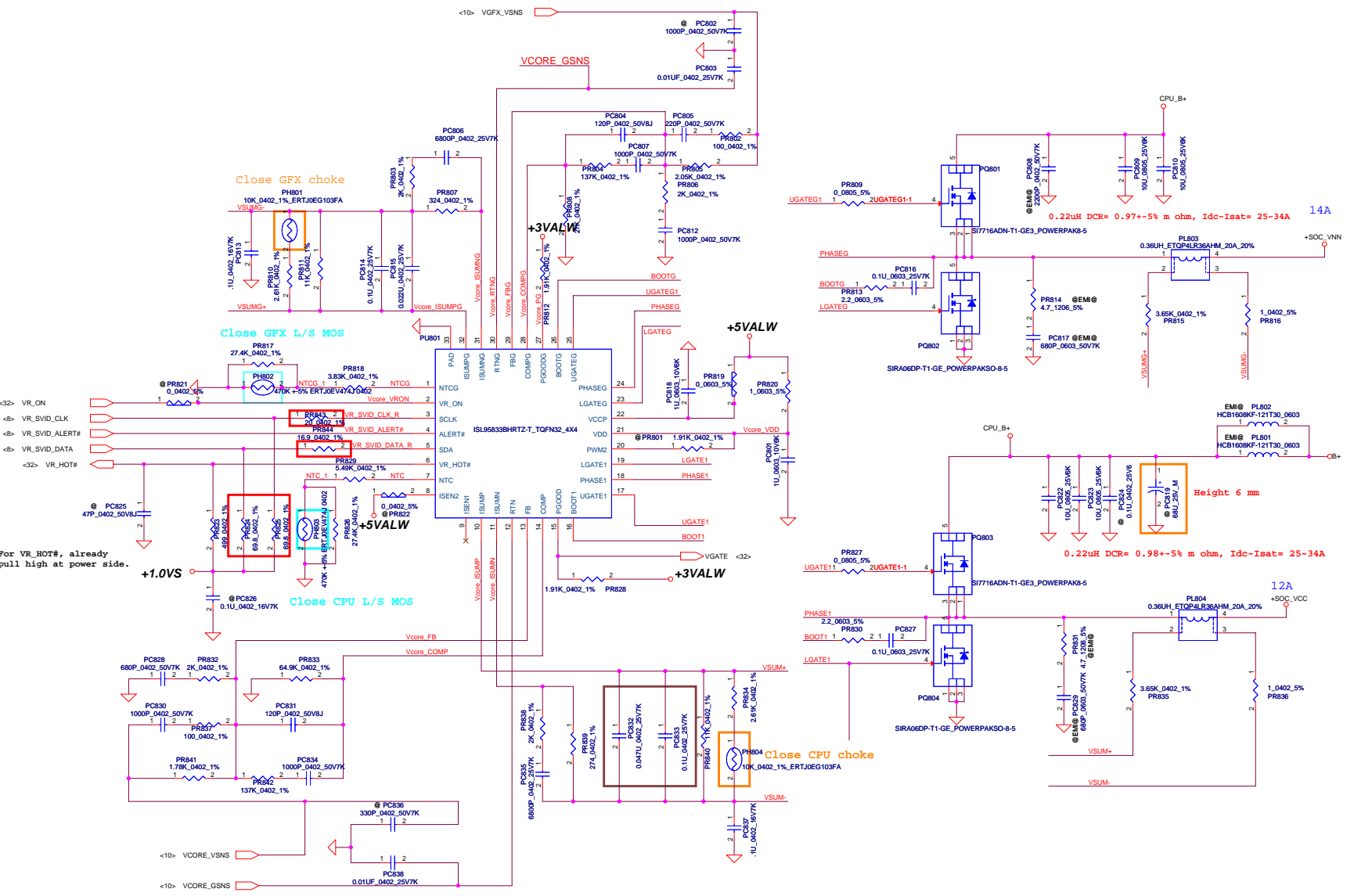
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$V_{FB} = 0.8V$
 $V_o = 0.8(1 + R_t/R_b) = 0.8(1 + 14k/1k) = 12V$
 $CL(\min) = 8A; CL(\min) = 10A; CL(\min) = 12A$

+12VSP
 $I_{peak} = 2.5A; F_{sw} = 600KHz$
 $\Delta IL = [(V_{in} - V_o)/L] * [(V_{in}/V_{out}) * T] = 1.702A$
 $LIR = \Delta IL / I_{peak} = 0.851$
 $L = V_{out} [1 - (V_{out}/V_{in})] / LIR * I_{out} * F_{sw} = 4.7uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 2.59uF$

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<32> VR_ON
 <8> VR_SVID_CLK
 <8> VR_SVID_ALERT#
 <8> VR_SVID_DATA
 <32> VR_HOT#

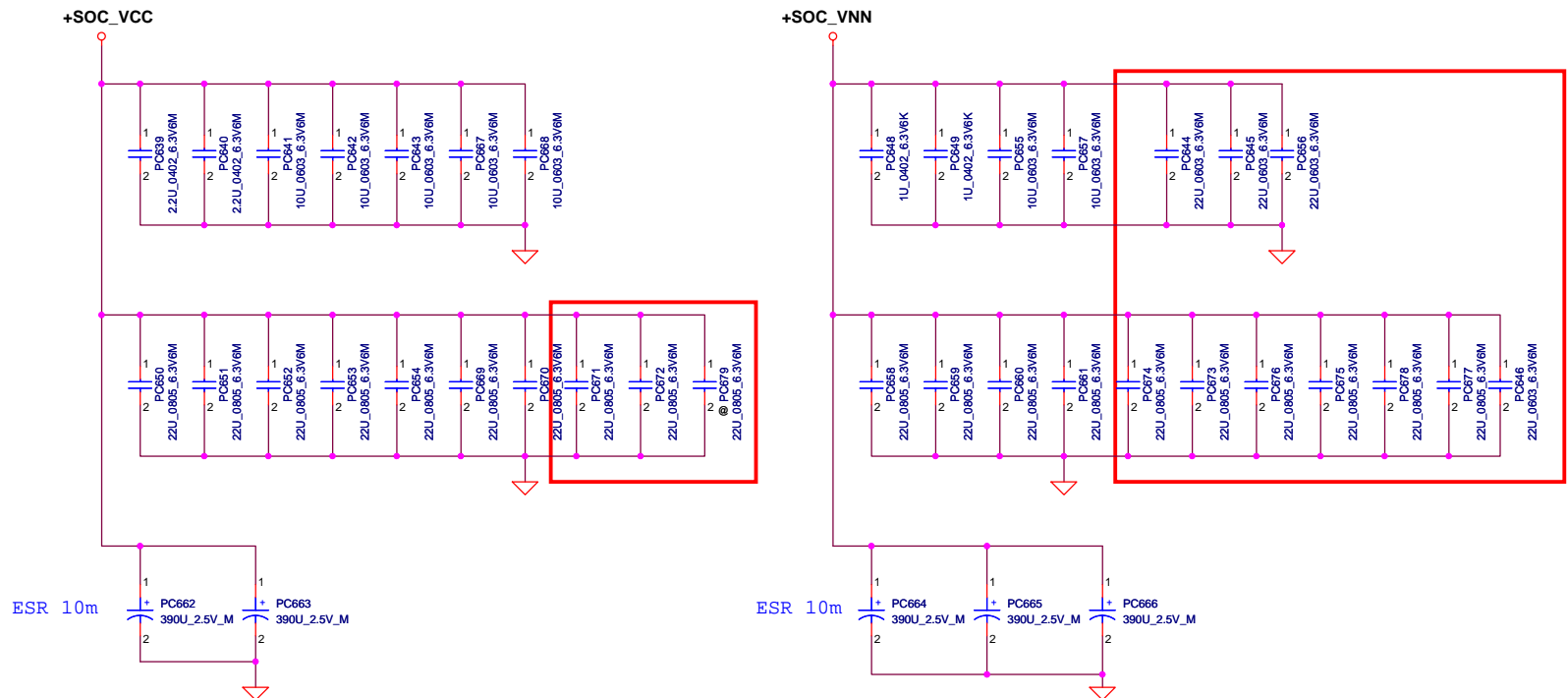
For VR_HOT#, already pull high at power side.

OCP:
 +SO_C_VCC: 18A
 +SOC_VNN: 21A
 OTP:
 VR_HOT at 110 deg.
 VR_ALERT at 107 deg

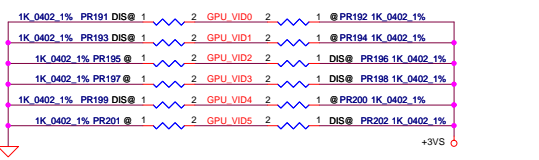
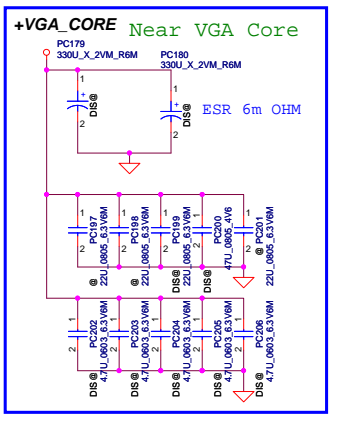
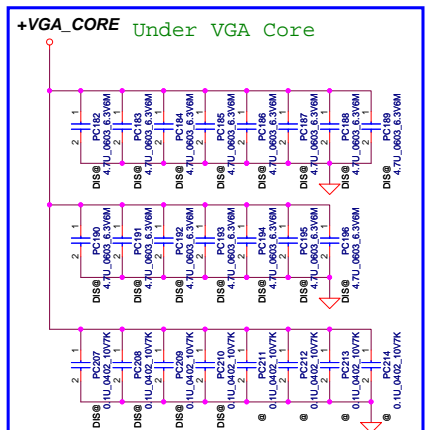
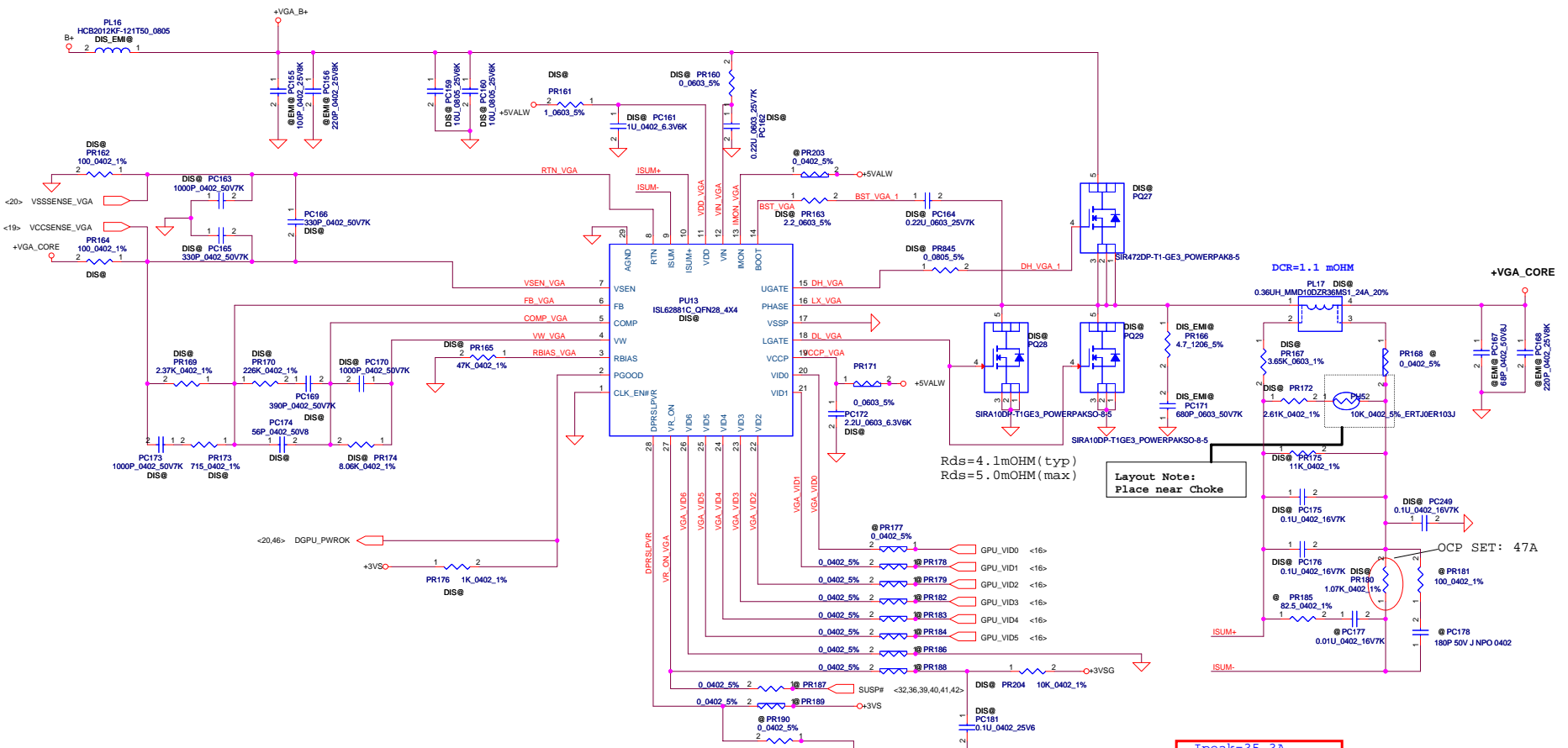
+SOC_VCC:
 Ipeak=12A; Fsw=450KHz; Vboot=1.1V
 Iocp>=18A
 Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=10.5A
 LIR=Delta IL/Ipeak=0.875
 L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=0.22uH
 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
 =1339.17uF
 CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

+SOC_VNN:
 Ipeak=14A; Fsw=450KHz; Vboot=1.1V
 Iocp>=21A
 Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=10.5A
 LIR=Delta IL/Ipeak=0.75
 L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=0.22uH
 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
 =1667.7uF
 CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF

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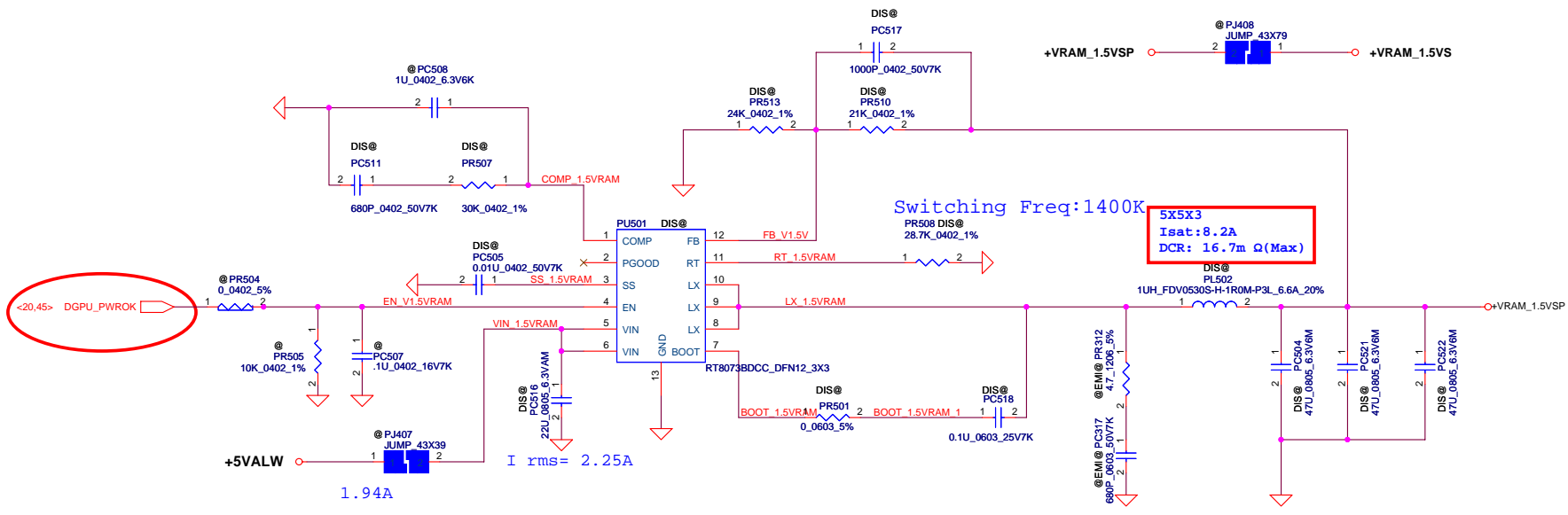
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	
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Layout Note:
Place near Choke

Ipeak=35.3A
Imax=24.7A
IOCP=42.38A
F=300KHZ
Total capacitor
1460u
ESR=1.8m ohm

+VGA_CORE:
Ipeak=35.3A; Imax=24.7A; Fsw=300KHz; Vboot=1.1V
Iocp(set)>=47A
Delta IL=[(Vin-Vo)/L]*[(Vin/Vout)*T]=9.625A
LIR=Delta IL/Ipeak=0.273
L=Vout/[1-(Vout/Vin)]/LIR*Iout*Fsw=0.36uH
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11849uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=3.06uF



$I_{peak}=5.5A, I_{max}=3.84A, F_{sw}=1400KHz$
 $CL(min)=7A, CL(typ)=9A$
 $\Delta IL=[(V_{in}-V_o)/L]*[(V_{in}/V_{out})*T]=0.75A$
 $LIR=\Delta IL/I_{peak}=0.136$
 $L=V_{out}[1-(V_{out}/V_{in})]/LIR*I_{out}*F_{sw}=1.0uH$
 $CINBULK=I_{Load}*V_{out}*(V_{in}-V_{out})/(F_{sw}*V_{in}^2*VINPP)=1.65uF$

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POWER PIR (Product Improve Record)

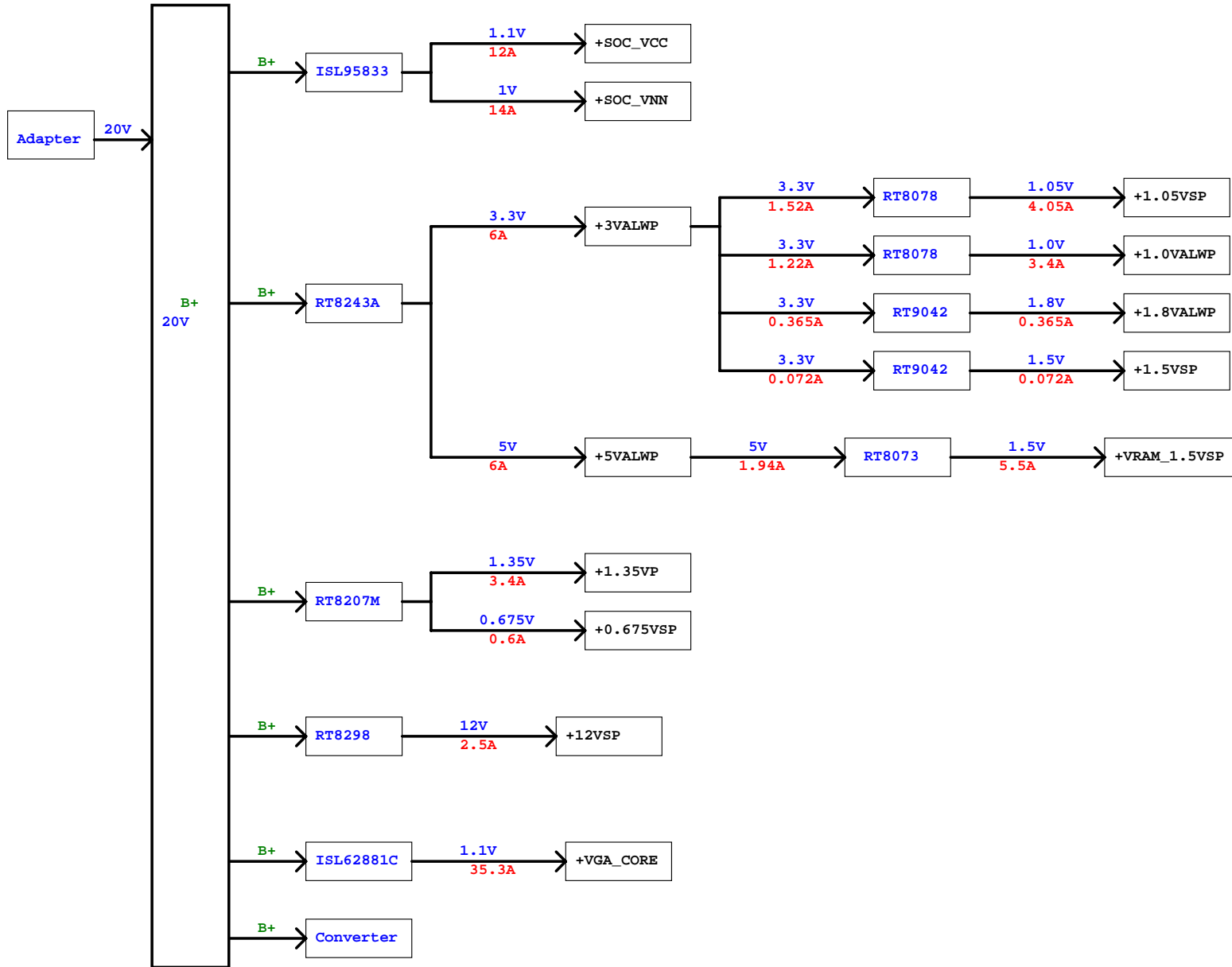
ZAA00 LA-XXXX SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1
 GERBER-OUT DATE: 2013/08/xx

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2013/08/12	43	PR814, PR833 change to 0402	module layout

NO	DATE	PAGE	MODIFICATION LIST(DVT)	PURPOSE
2	2013/09/14	39	change PR311 to 10K and pull high to +1.35V	design change
3	2013/09/17	43	change PC829 and PC817 to 0603 size	meet C38 MB design guide
4	2013/09/23	39	change PR306=12K, PR308=15K	meet voltage level
5	2013/09/23	44	add PC671,PC672,PC673,PC674,PC675,PC676, reserve PC677,PC678, PC679,PC646	meet Intel spec
6	2013/09/23	38	change PR418=12K, PR424=10K, PC417=un-pop	meet C38 MB design guide, light load Switching freq. >22KHz
7	2013/09/24	43	change PR807=324, PC815=0.022uF, PR839=274, PR837=100,PC830=1000pF, PL803=0.36uF, PL804=0.36uF, PC819= un-pop	meet Intel spec
8	2013/09/26	40,41	change PR403=20K, PR515=36K, PC406=0.1uF, PC510=0.1uF	meet Power sequence
9	2013/10/04	43	change PR802=100, PC805=220pF, PC812=1000pF	meet Intel spec
10	2013/10/04	37	change PC34=0.22uF, PC33=0.022uF	meet inrush spec
11	2013/10/08	46	change PC504=47uF, PC521=47uF, PC522=47uF, PR507=30k	meet Vram spec
12	2013/10/09	39	PC310=SGA00008S00	meet design spec

NO	DATE	PAGE	MODIFICATION LIST(PVT)	PURPOSE
13	2013/10/14	46	add PC517=1000pF	meet Vram spec
14	2013/10/29	43	1. Change the PC831 from 68pF to 120pF. 2. Change the PC834 from 150pF to 1000pF. 3. Change the PR838 from 649 Ohm to 2kOhm. 4. Change the PC804 from 68pF to 120pF. 5. Change the PC807 from 150pF to 1000pF. 6. Change the PR803 from 649 Ohm to 2kOhm.	solve can't boot issue
15	2013/11/12	38	1.PR418=120K 2.P424=100K	reduce current sink
16	2013/11/13	44	PC644,PC645,PC646,PC656= 22uF(0603 size) PU801= ISL95833B(SA000071G00)	meet Intel spec
17	2013/11/18	38,39	PR425=10K PR306=11.8K	HW request
18	2013/11/21	38	PC839, PC840=0.1uF	EMC request

NO	DATE	PAGE	MODIFICATION LIST(Pre MP)	PURPOSE
1	2013/12/20	ALL	Change to short pad PR171,PR819 PR2,PR168,PR177,PR178,PR179, PR182,PR183,PR184,PR186,PR188, PR189,PR203,PR309,PR502,PR504, PR822,PR821,PR408	cost down



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				Date:	Tuesday, March 25, 2014	Sheet 48 of 48