

Z96Jm

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Default	EC
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSERVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/			GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRLED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0/GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4/GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSC#/#GPD3	EXT_SC#	ECSC#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

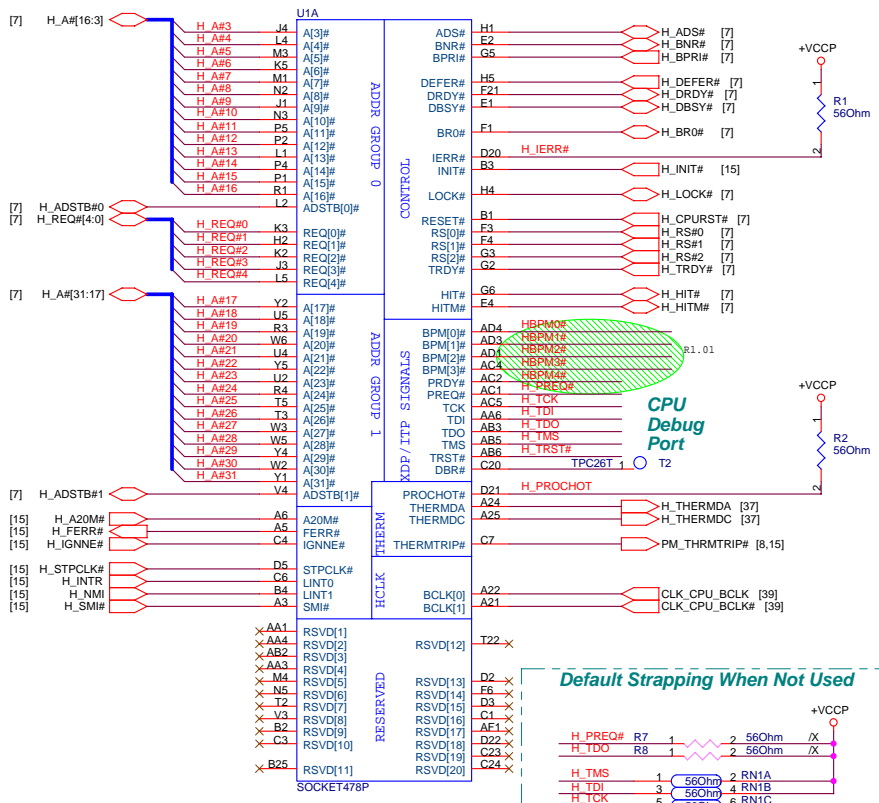
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0100110X (98)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

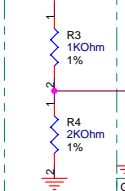
ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCL_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCL_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCL_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCL_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCL_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCL_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCL_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

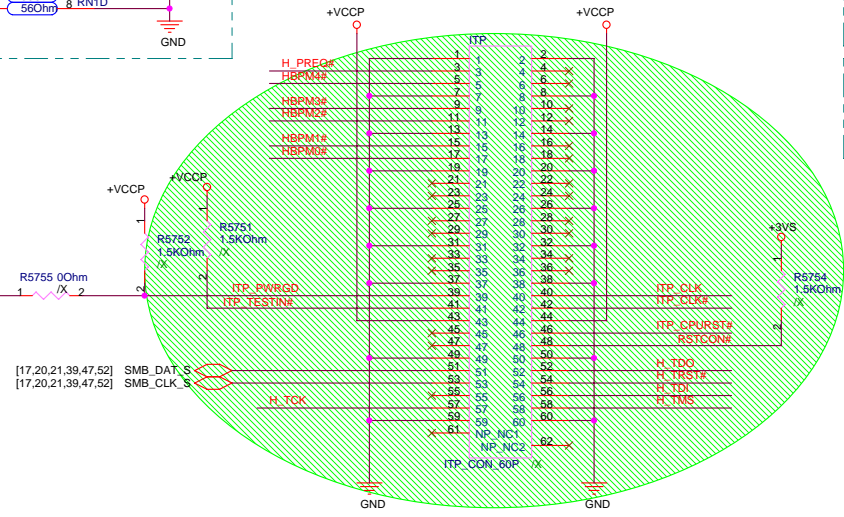
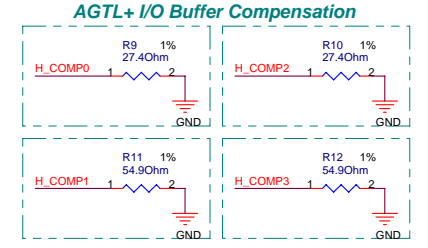
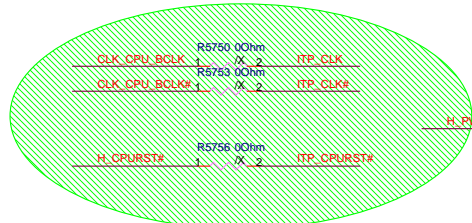
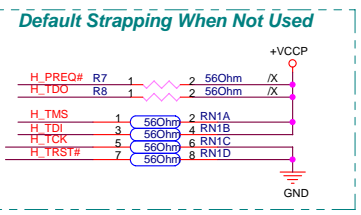
ASUS Title : <Title>
 ASUSTek Computer, INC. Engineer: Alan Chu
 Size Project Name
 Custom Z96Jm Rev 1.0
 Date: Monday, August 21, 2006 Sheet 2 of 91



AGTL+ I/O Voltage Reference



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

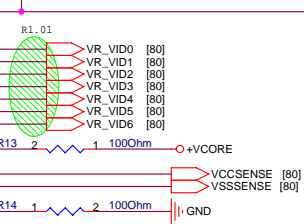
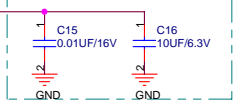
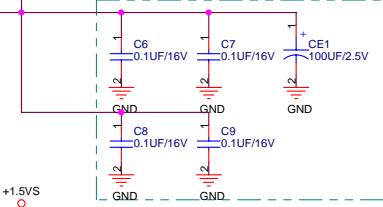
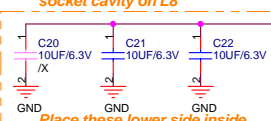
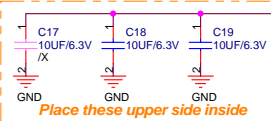
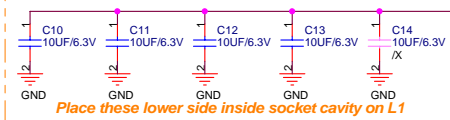
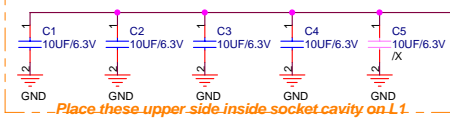
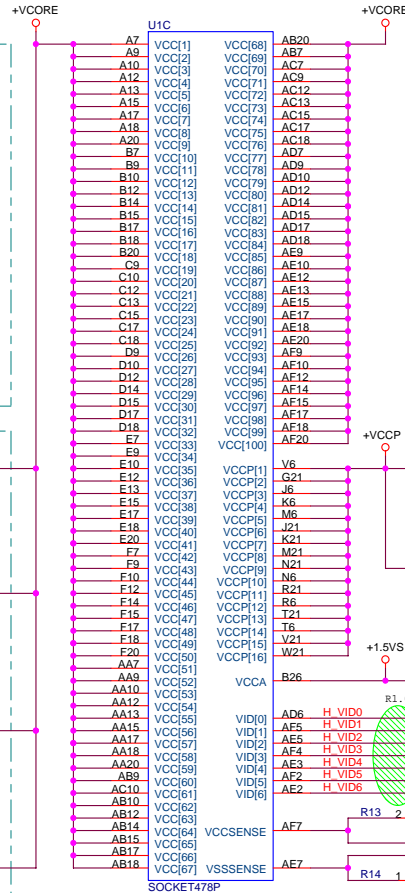


**CPU +VCORE
Bulk-Decoupling
Capacitors**

**CPU +VCORE
Mid-Frequency
Capacitors**

**CPU +VCCP
Decoupling
Capacitors**

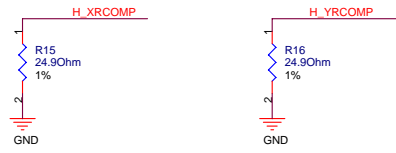
**CPU +VCCA
Decoupling
Capacitors**



- +VCORE Mid-Frequency Capacitor
Intel: 22UF *32
R1F: 10UF *16
- +VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4

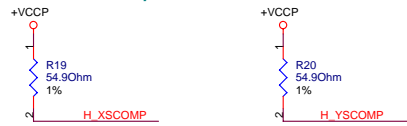
RCOMP

For Calibrating the FSB I/O Buffer



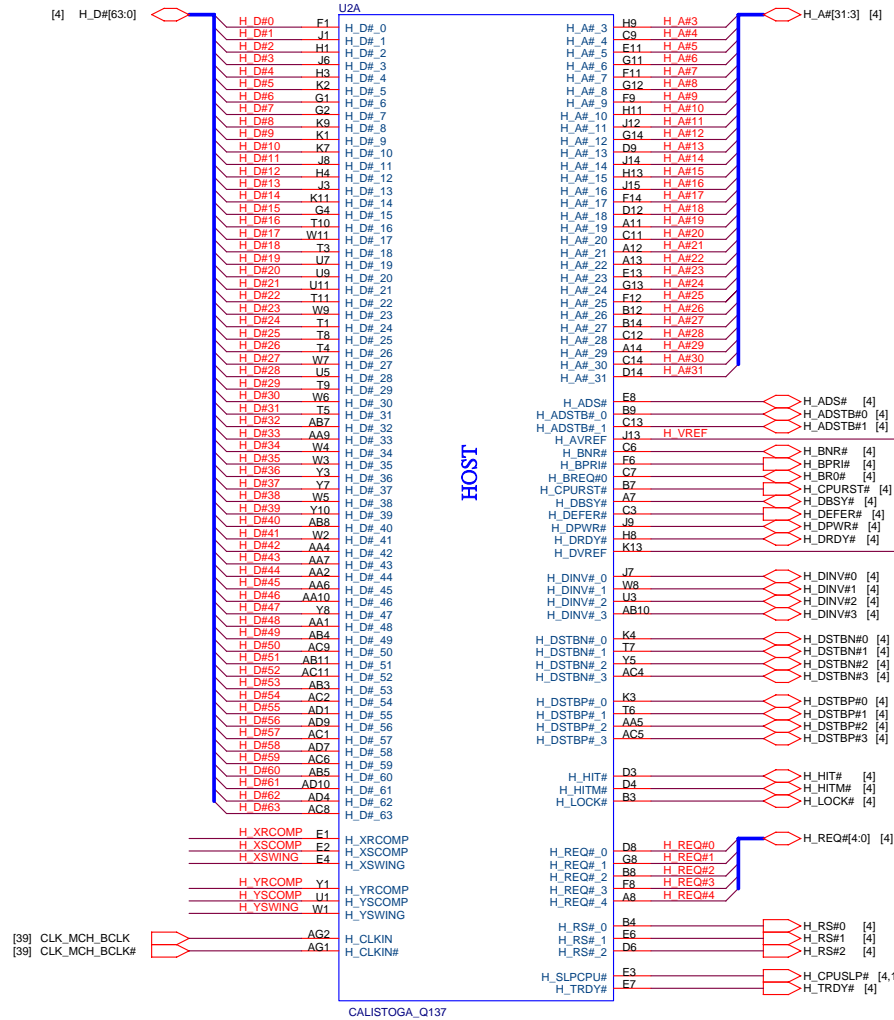
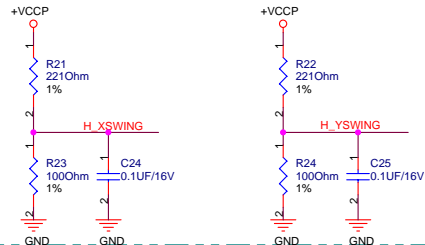
SCOMP

For Slew Rate Compensation on the FSB

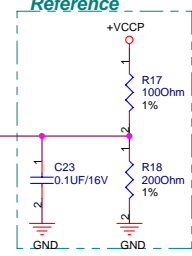


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



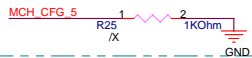
AGTL+ I/O Voltage Reference



GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

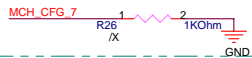


CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

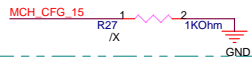
CFG7 : CPU Strap

0 = DT/Transportable CPU
1 = Mobile CPU (D)



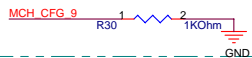
CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)



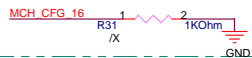
CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



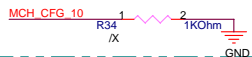
CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



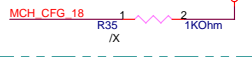
CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)



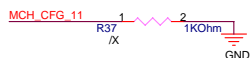
CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V



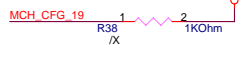
CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)



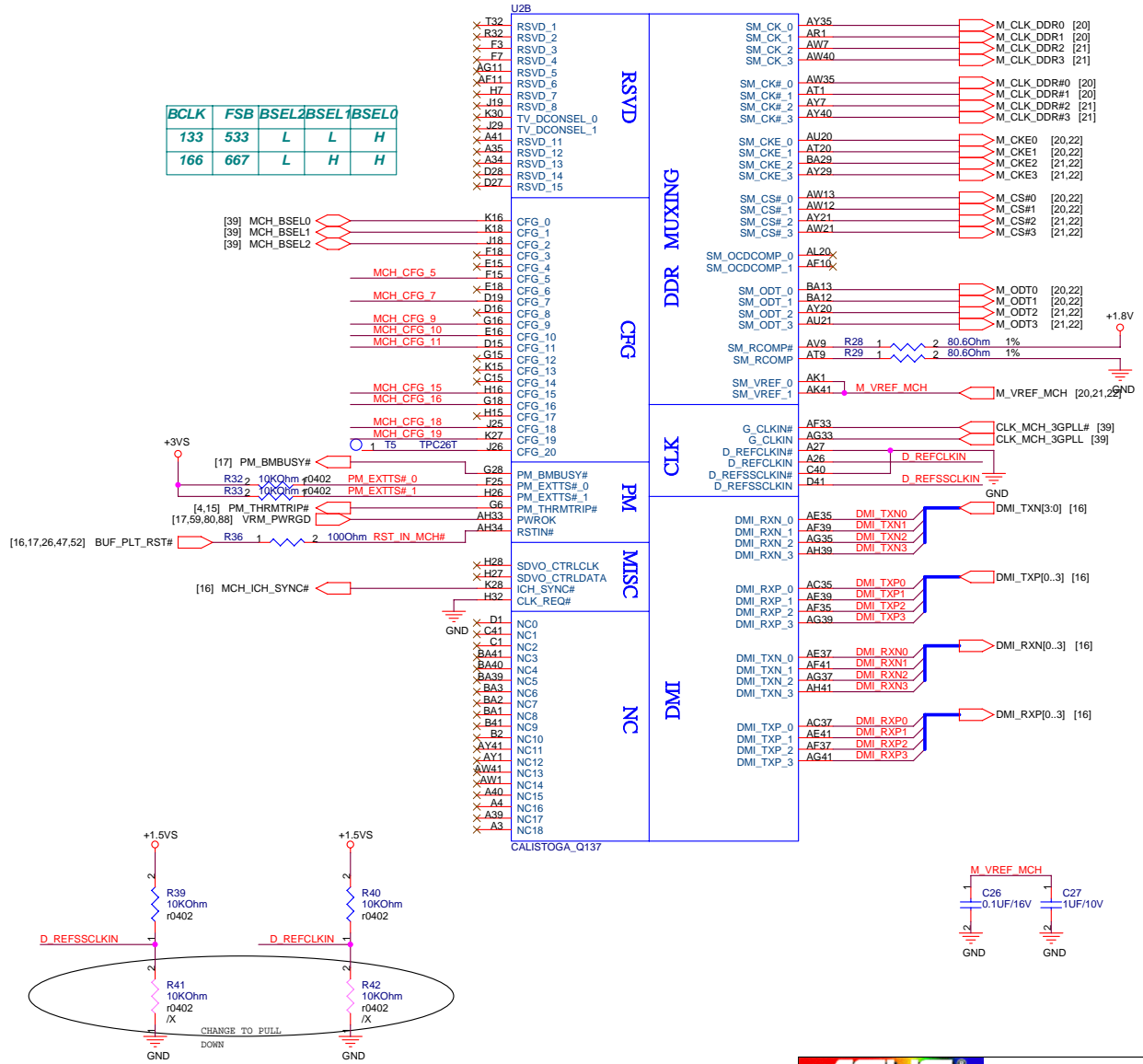
CFG19 : DMI Lane Reversal

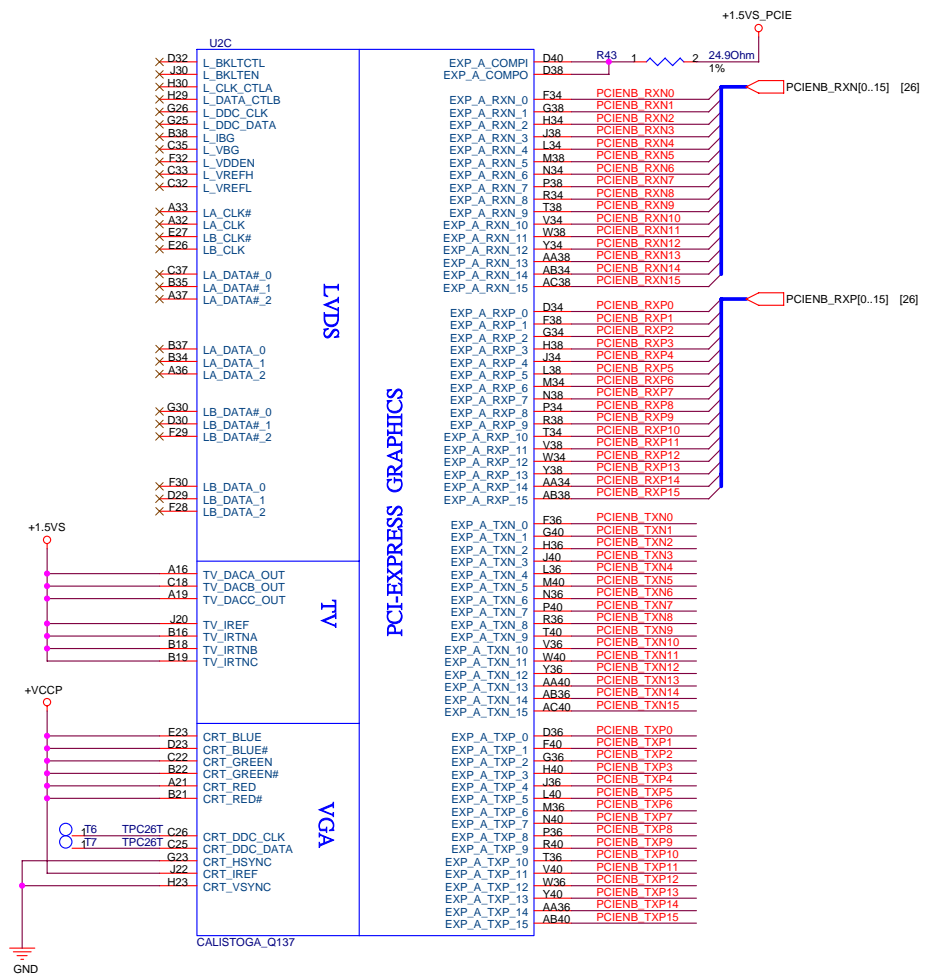
0 = Normal Operation (D)
1 = Lanes Reversed



Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

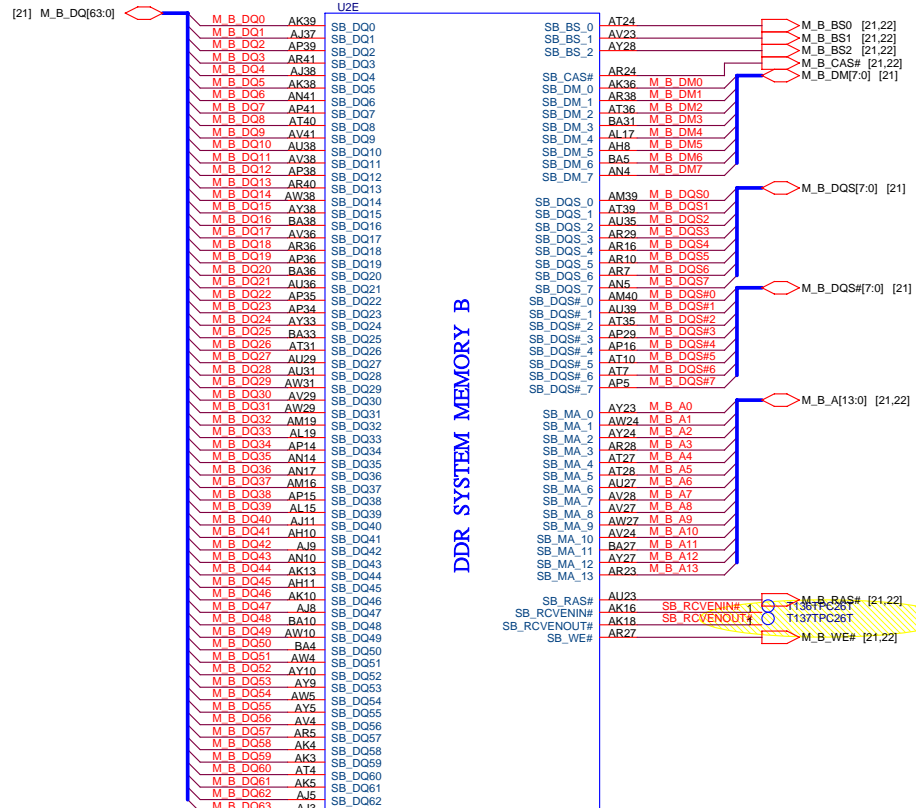
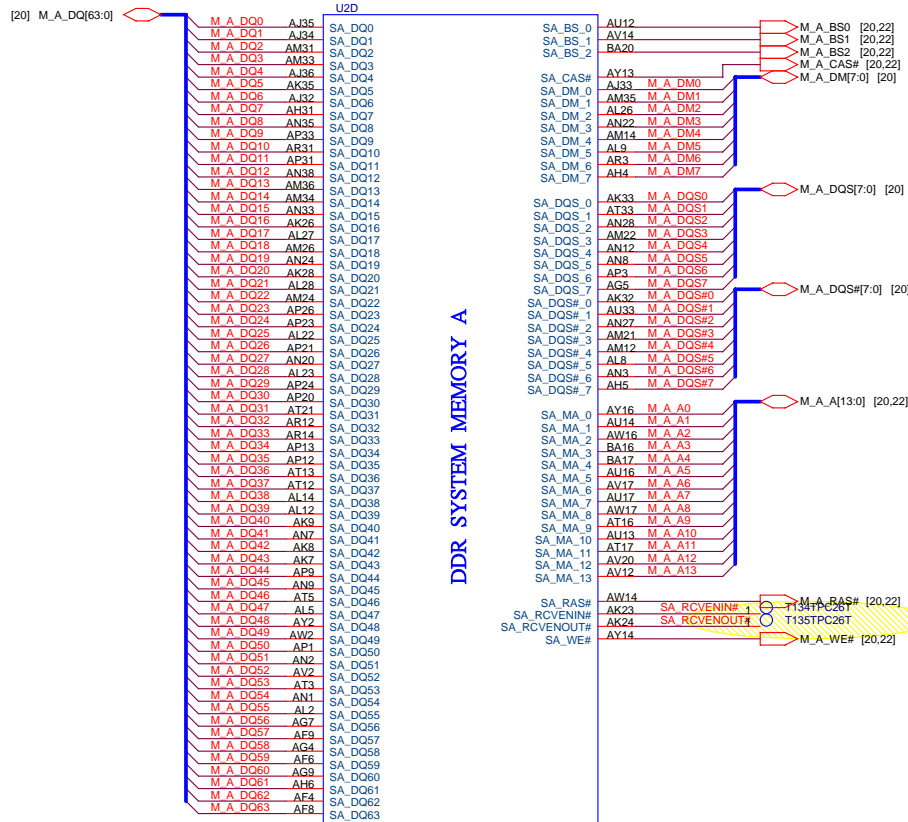


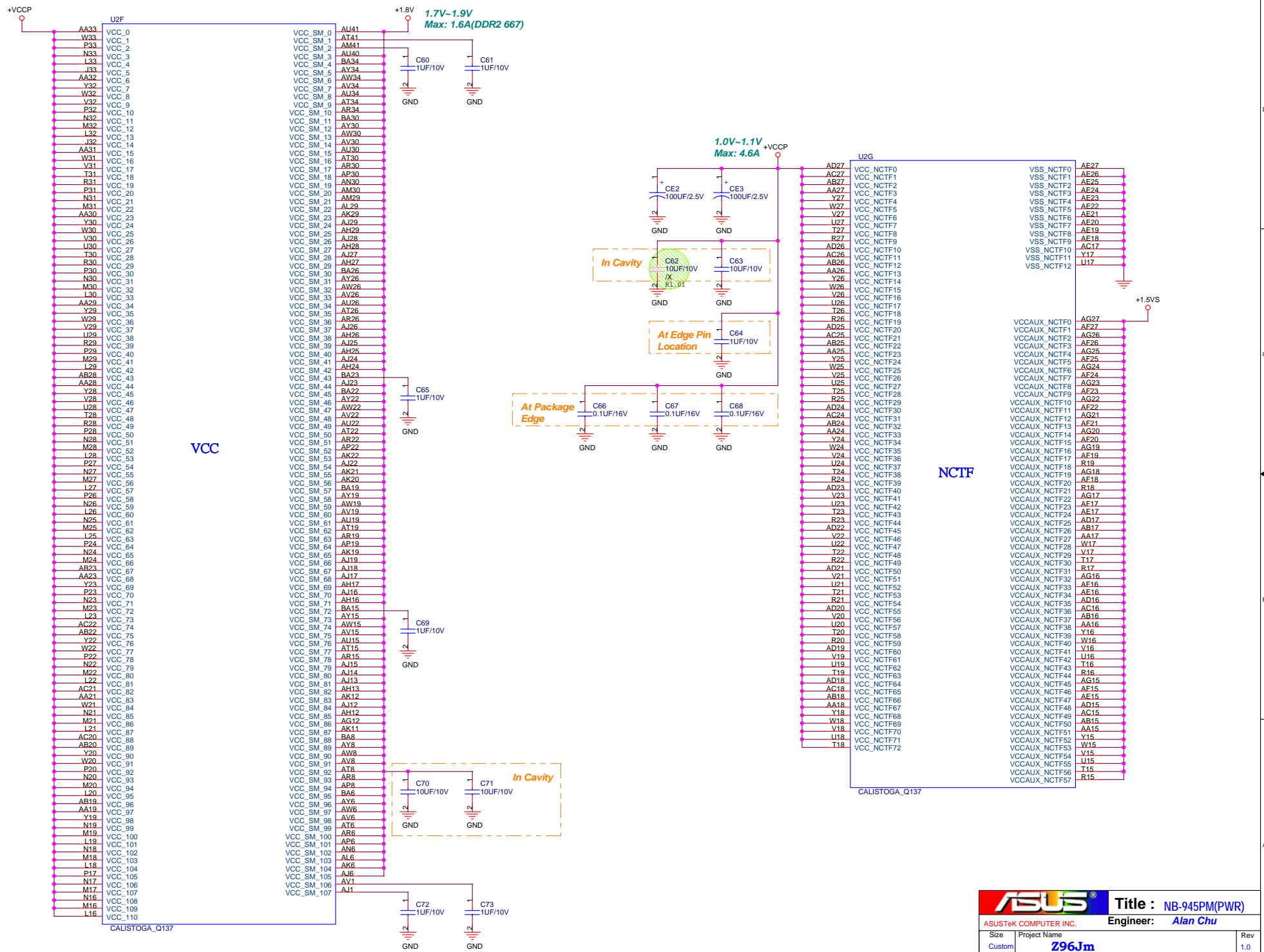


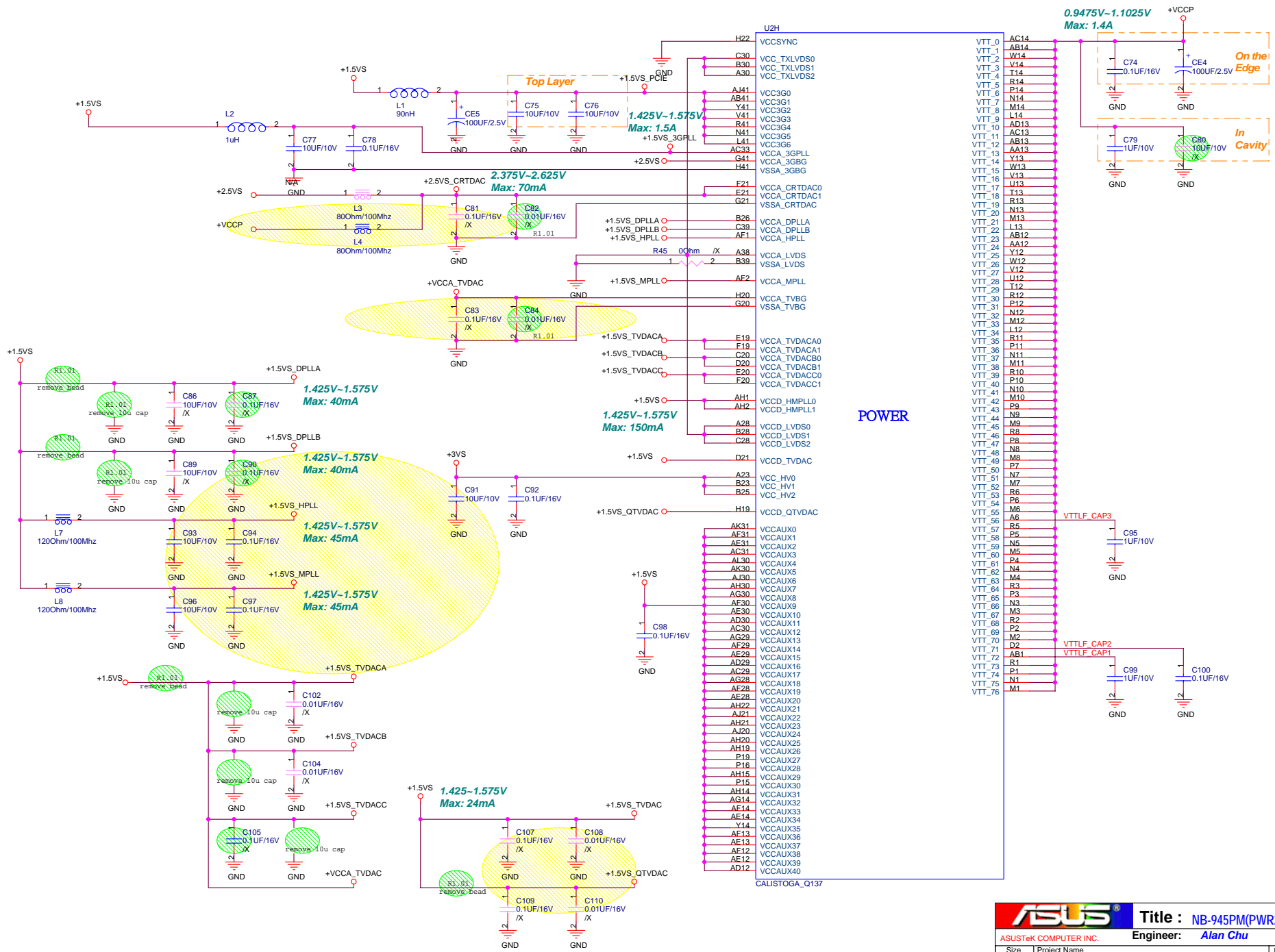
PCI-EXPRESS GRAPHICS

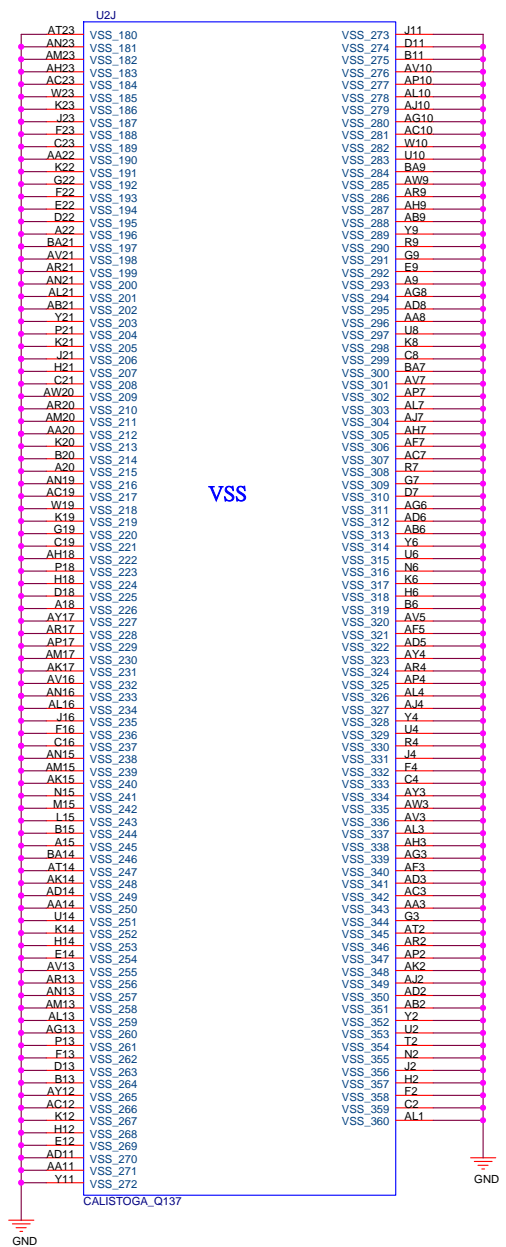
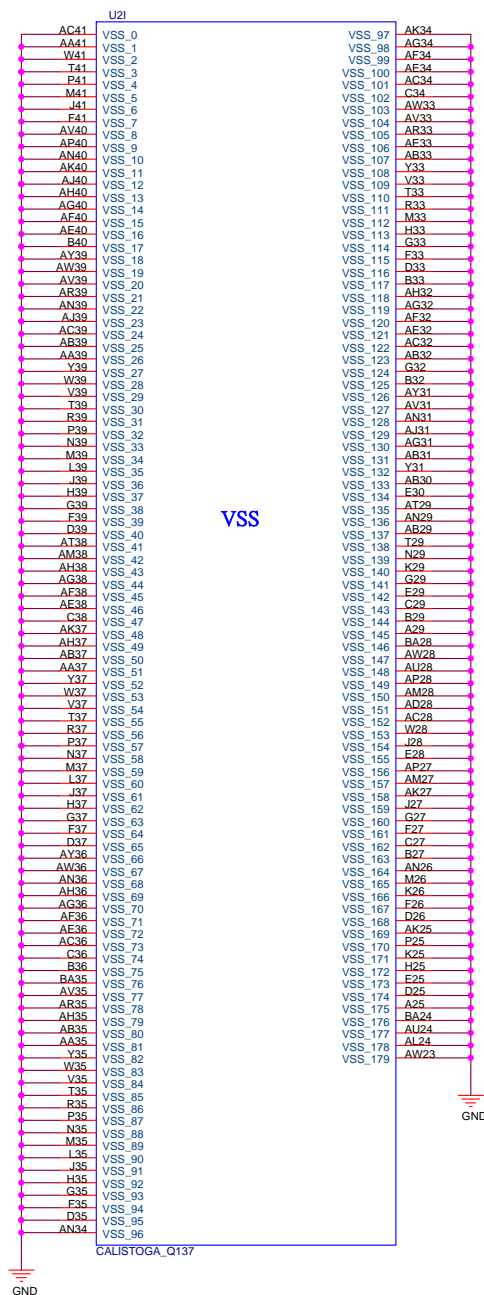
EXP_A_COMP1	D40	R43	1	2	24.90 Ohm	
EXP_A_COMPO	D38				1%	
EXP_A_RXN_0	F34	PCIENB_RXN0				
EXP_A_RXN_1	G38	PCIENB_RXN1				
EXP_A_RXN_2	H34	PCIENB_RXN2				
EXP_A_RXN_3	J38	PCIENB_RXN3				
EXP_A_RXN_4	L34	PCIENB_RXN4				
EXP_A_RXN_5	M38	PCIENB_RXN5				
EXP_A_RXN_6	N34	PCIENB_RXN6				
EXP_A_RXN_7	P38	PCIENB_RXN7				
EXP_A_RXN_8	R34	PCIENB_RXN8				
EXP_A_RXN_9	T38	PCIENB_RXN9				
EXP_A_RXN_10	V34	PCIENB_RXN10				
EXP_A_RXN_11	W38	PCIENB_RXN11				
EXP_A_RXN_12	Y34	PCIENB_RXN12				
EXP_A_RXN_13	AA38	PCIENB_RXN13				
EXP_A_RXN_14	AB34	PCIENB_RXN14				
EXP_A_RXN_15	AC38	PCIENB_RXN15				
EXP_A_RXP_0	D34	PCIENB_RXP0				
EXP_A_RXP_1	F38	PCIENB_RXP1				
EXP_A_RXP_2	G34	PCIENB_RXP2				
EXP_A_RXP_3	H38	PCIENB_RXP3				
EXP_A_RXP_4	J34	PCIENB_RXP4				
EXP_A_RXP_5	L38	PCIENB_RXP5				
EXP_A_RXP_6	M34	PCIENB_RXP6				
EXP_A_RXP_7	N38	PCIENB_RXP7				
EXP_A_RXP_8	P34	PCIENB_RXP8				
EXP_A_RXP_9	R38	PCIENB_RXP9				
EXP_A_RXP_10	T34	PCIENB_RXP10				
EXP_A_RXP_11	V38	PCIENB_RXP11				
EXP_A_RXP_12	W34	PCIENB_RXP12				
EXP_A_RXP_13	Y38	PCIENB_RXP13				
EXP_A_RXP_14	AA34	PCIENB_RXP14				
EXP_A_RXP_15	AB38	PCIENB_RXP15				
EXP_A_TXN_0	F36	PCIENB_TXN0				
EXP_A_TXN_1	G40	PCIENB_TXN1				
EXP_A_TXN_2	H36	PCIENB_TXN2				
EXP_A_TXN_3	J40	PCIENB_TXN3				
EXP_A_TXN_4	L36	PCIENB_TXN4				
EXP_A_TXN_5	M40	PCIENB_TXN5				
EXP_A_TXN_6	N36	PCIENB_TXN6				
EXP_A_TXN_7	P40	PCIENB_TXN7				
EXP_A_TXN_8	R36	PCIENB_TXN8				
EXP_A_TXN_9	T40	PCIENB_TXN9				
EXP_A_TXN_10	V36	PCIENB_TXN10				
EXP_A_TXN_11	W40	PCIENB_TXN11				
EXP_A_TXN_12	Y36	PCIENB_TXN12				
EXP_A_TXN_13	AA40	PCIENB_TXN13				
EXP_A_TXN_14	AB36	PCIENB_TXN14				
EXP_A_TXN_15	AC40	PCIENB_TXN15				
EXP_A_TXP_0	D36	PCIENB_TXP0				
EXP_A_TXP_1	F40	PCIENB_TXP1				
EXP_A_TXP_2	G36	PCIENB_TXP2				
EXP_A_TXP_3	H40	PCIENB_TXP3				
EXP_A_TXP_4	J36	PCIENB_TXP4				
EXP_A_TXP_5	L40	PCIENB_TXP5				
EXP_A_TXP_6	M36	PCIENB_TXP6				
EXP_A_TXP_7	N40	PCIENB_TXP7				
EXP_A_TXP_8	P36	PCIENB_TXP8				
EXP_A_TXP_9	R40	PCIENB_TXP9				
EXP_A_TXP_10	T36	PCIENB_TXP10				
EXP_A_TXP_11	W40	PCIENB_TXP11				
EXP_A_TXP_12	Y36	PCIENB_TXP12				
EXP_A_TXP_13	AA36	PCIENB_TXP13				
EXP_A_TXP_14	AB40	PCIENB_TXP14				
EXP_A_TXP_15	AB40	PCIENB_TXP15				

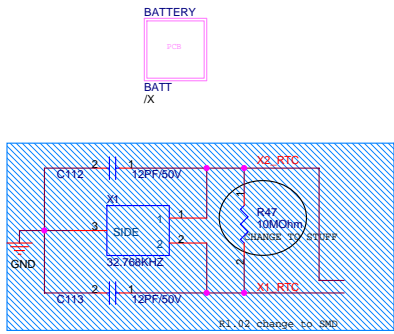
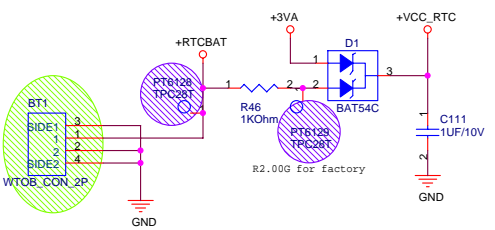
PCIENB_TXP15	1	2		PCIENB_RXN15	
PCIENB_TXP14	C28	0.1UF/16V	2	PCIENB_RXP14	
PCIENB_TXP13	1	2	C29	0.1UF/16V	PCIENB_RXP13
PCIENB_TXP12	C30	0.1UF/16V	2	PCIENB_RXP12	
PCIENB_TXP11	1	2	C31	0.1UF/16V	PCIENB_RXP11
PCIENB_TXP10	C32	0.1UF/16V	2	PCIENB_RXP10	
PCIENB_TXP9	1	2	C33	0.1UF/16V	PCIENB_RXP9
PCIENB_TXP8	C34	0.1UF/16V	2	PCIENB_RXP8	
PCIENB_TXP7	1	2	C35	0.1UF/16V	PCIENB_RXP7
PCIENB_TXP6	C36	0.1UF/16V	2	PCIENB_RXP6	
PCIENB_TXP5	1	2	C37	0.1UF/16V	PCIENB_RXP5
PCIENB_TXP4	C38	0.1UF/16V	2	PCIENB_RXP4	
PCIENB_TXP3	1	2	C39	0.1UF/16V	PCIENB_RXP3
PCIENB_TXP2	C40	0.1UF/16V	2	PCIENB_RXP2	
PCIENB_TXP1	1	2	C41	0.1UF/16V	PCIENB_RXP1
PCIENB_TXP0	C42	0.1UF/16V	2	PCIENB_RXP0	
PCIENB_TXN15	1	2	C43	0.1UF/16V	PCIENB_RXN15
PCIENB_TXN14	C44	0.1UF/16V	2	PCIENB_RXN14	
PCIENB_TXN13	1	2	C45	0.1UF/16V	PCIENB_RXN13
PCIENB_TXN12	C46	0.1UF/16V	2	PCIENB_RXN12	
PCIENB_TXN11	1	2	C47	0.1UF/16V	PCIENB_RXN11
PCIENB_TXN10	C48	0.1UF/16V	2	PCIENB_RXN10	
PCIENB_TXN9	1	2	C49	0.1UF/16V	PCIENB_RXN9
PCIENB_TXN8	C50	0.1UF/16V	2	PCIENB_RXN8	
PCIENB_TXN7	1	2	C51	0.1UF/16V	PCIENB_RXN7
PCIENB_TXN6	C52	0.1UF/16V	2	PCIENB_RXN6	
PCIENB_TXN5	1	2	C53	0.1UF/16V	PCIENB_RXN5
PCIENB_TXN4	C54	0.1UF/16V	2	PCIENB_RXN4	
PCIENB_TXN3	1	2	C55	0.1UF/16V	PCIENB_RXN3
PCIENB_TXN2	C56	0.1UF/16V	2	PCIENB_RXN2	
PCIENB_TXN1	1	2	C57	0.1UF/16V	PCIENB_RXN1
PCIENB_TXN0	C58	0.1UF/16V	2	PCIENB_RXN0	
			C59	0.1UF/16V	





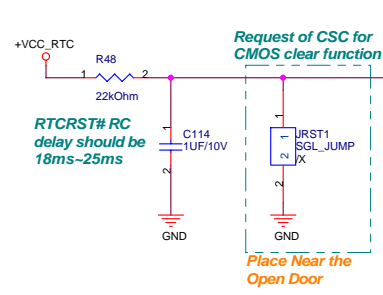






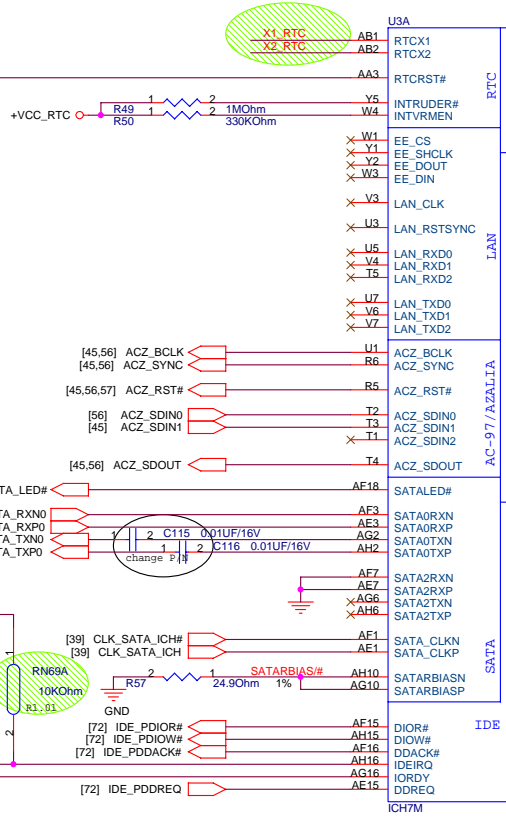
R1.01 change connector

R1.02 change to 000

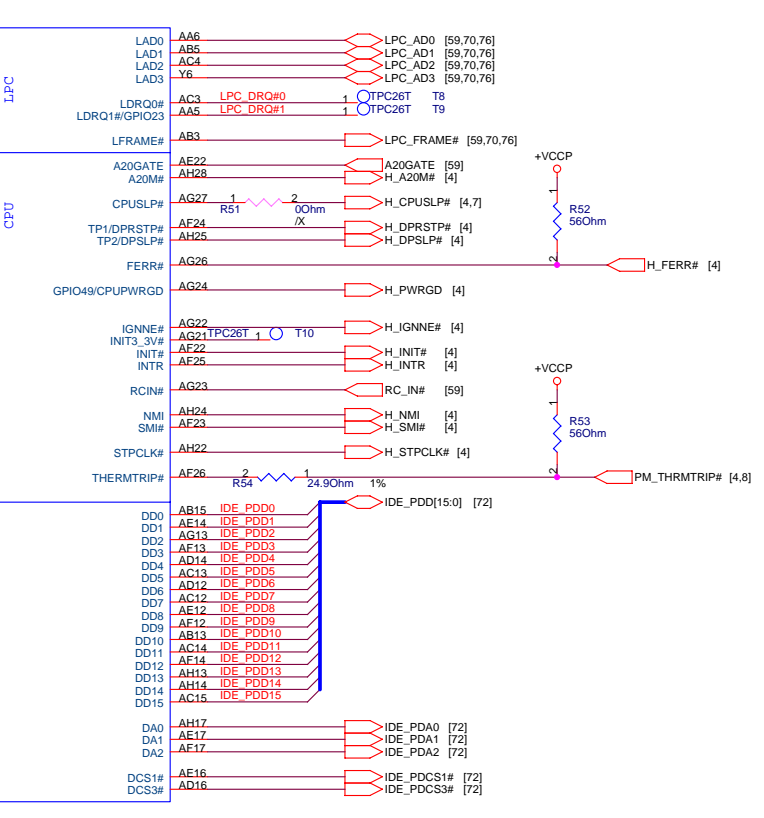


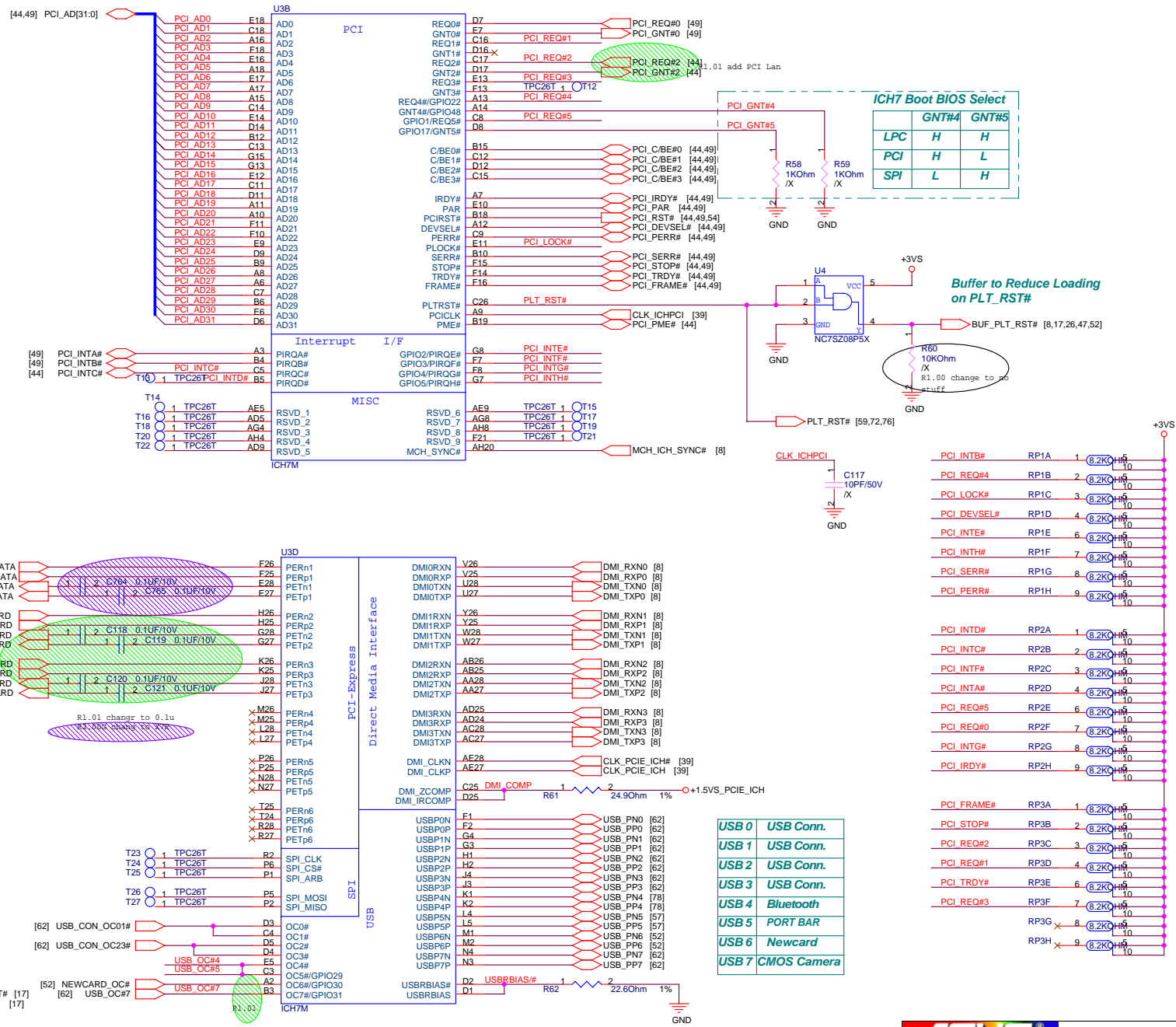
RTC RST# RC delay should be 18ms~25ms

Place Near the Open Door

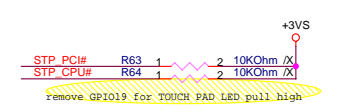
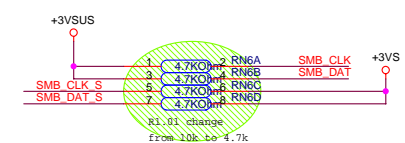
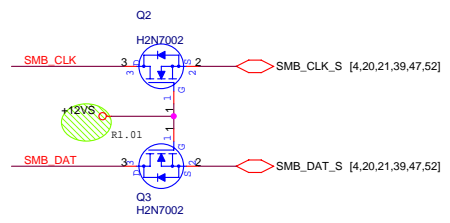
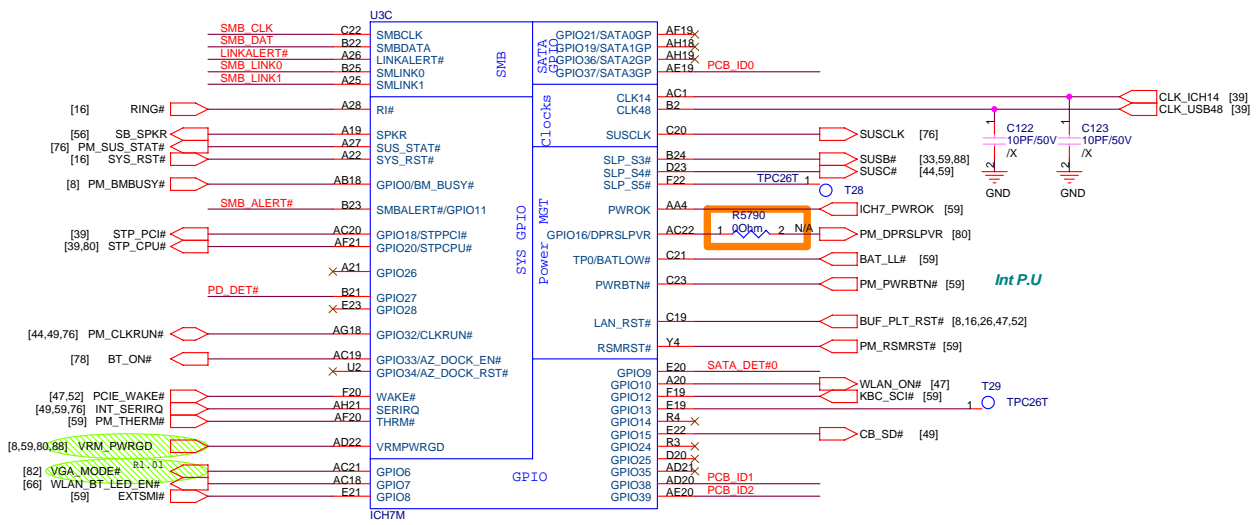


ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM

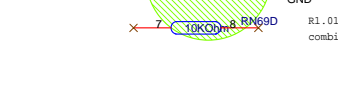
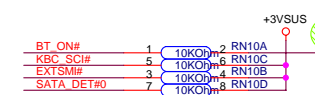
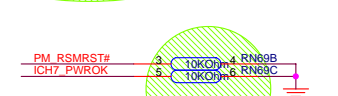
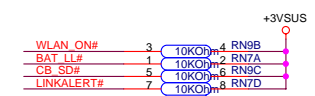
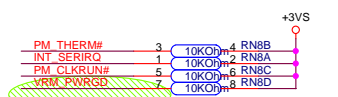
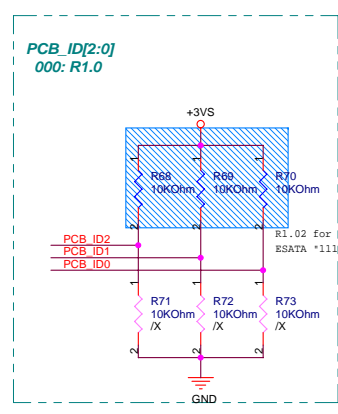


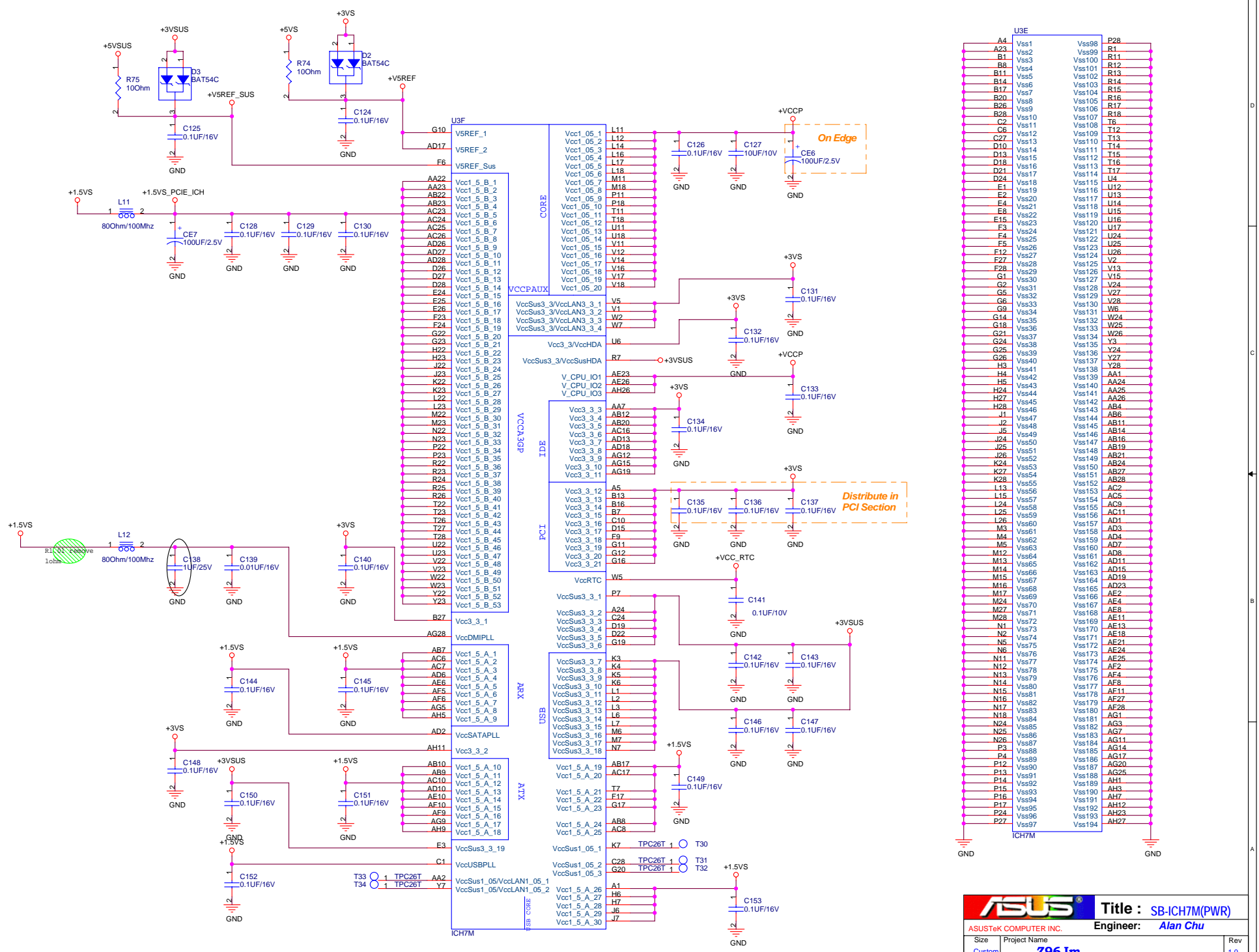


R1.01 add VGA mode select
 GPU_VID = 1; Battery Mode ; +1.15V0 = 1.055V
 GPU_VID = 0; Performance Mode ; +1.15V0 = 1.158V



Remove GPIO19 for TOUCH PAD LED pull high

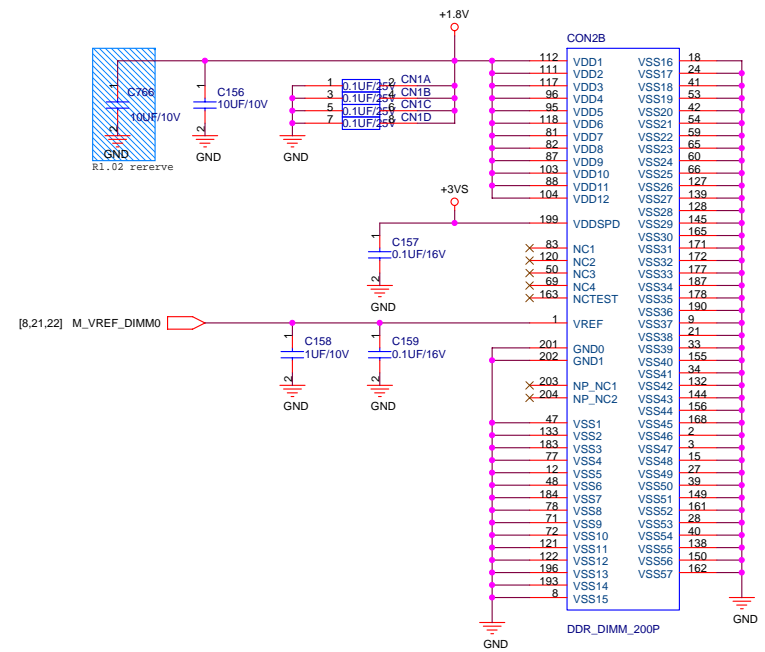




U3E		P28	
A4	Vss1	Vss98	R1
A23	Vss2	Vss100	R11
B1	Vss3	Vss101	R12
B8	Vss4	Vss102	R13
B11	Vss5	Vss103	R14
B14	Vss6	Vss104	R15
B17	Vss7	Vss105	R16
B20	Vss8	Vss106	R17
B26	Vss9	Vss107	R18
B28	Vss10	Vss108	T6
C2	Vss11	Vss109	T12
C6	Vss12	Vss110	T13
C27	Vss13	Vss111	T14
D10	Vss14	Vss112	T15
D13	Vss15	Vss113	T16
D18	Vss16	Vss114	T17
D21	Vss17	Vss115	U4
D24	Vss18	Vss116	U12
E1	Vss19	Vss117	U13
E2	Vss20	Vss118	U14
E4	Vss21	Vss119	U15
E8	Vss22	Vss120	U16
F15	Vss23	Vss121	U24
F3	Vss24	Vss122	U25
F4	Vss25	Vss123	U26
F5	Vss26	Vss124	U27
F12	Vss27	Vss125	V13
F22	Vss28	Vss126	V15
F28	Vss29	Vss127	V16
G1	Vss30	Vss128	V24
G2	Vss31	Vss129	V27
G5	Vss32	Vss130	V28
G6	Vss33	Vss131	W6
G9	Vss34	Vss132	W24
G14	Vss35	Vss133	W25
G18	Vss36	Vss134	W26
G21	Vss37	Vss135	Y3
G24	Vss38	Vss136	Y24
G25	Vss39	Vss137	Y27
G26	Vss40	Vss138	Y28
H3	Vss41	Vss139	AA1
H4	Vss42	Vss140	AA24
H5	Vss43	Vss141	AA25
H24	Vss44	Vss142	AA26
H27	Vss45	Vss143	AB4
H28	Vss46	Vss144	AB6
J1	Vss47	Vss145	AB11
J2	Vss48	Vss146	AB14
J5	Vss49	Vss147	AB16
J24	Vss50	Vss148	AB19
J25	Vss51	Vss149	AB24
J26	Vss52	Vss150	AB27
K24	Vss53	Vss151	AB28
K27	Vss54	Vss152	AC2
K28	Vss55	Vss153	AC5
L13	Vss56	Vss154	AC9
L14	Vss57	Vss155	AD3
L24	Vss58	Vss156	AD11
L25	Vss59	Vss157	AD7
L26	Vss60	Vss158	AD7
M2	Vss61	Vss159	AD7
M4	Vss62	Vss160	AD7
M5	Vss63	Vss161	AD8
M12	Vss64	Vss162	AD17
M13	Vss65	Vss163	AD15
M14	Vss66	Vss164	AD23
M15	Vss67	Vss165	AE2
M16	Vss68	Vss166	AE4
M17	Vss69	Vss167	AE5
M24	Vss70	Vss168	AE11
M28	Vss71	Vss169	AE13
N1	Vss72	Vss170	AE18
N2	Vss73	Vss171	AE24
N5	Vss74	Vss172	AE25
N6	Vss75	Vss173	AE25
N11	Vss76	Vss174	AF2
N12	Vss77	Vss175	AF2
N13	Vss78	Vss176	AF4
N14	Vss79	Vss177	AF4
N15	Vss80	Vss178	AF7
N16	Vss81	Vss179	AF28
N17	Vss82	Vss180	AG7
N18	Vss83	Vss181	AG7
N24	Vss84	Vss182	AG3
N25	Vss85	Vss183	AG11
N26	Vss86	Vss184	AG14
P3	Vss87	Vss185	AG17
P4	Vss88	Vss186	AG20
P12	Vss89	Vss187	AG25
P13	Vss90	Vss188	AH1
P14	Vss91	Vss189	AH3
P15	Vss92	Vss190	AH7
P16	Vss93	Vss191	AH12
P17	Vss94	Vss192	AH23
P24	Vss95	Vss193	AH27
P27	Vss96	Vss194	AH27
P27	Vss97	Vss194	AH27

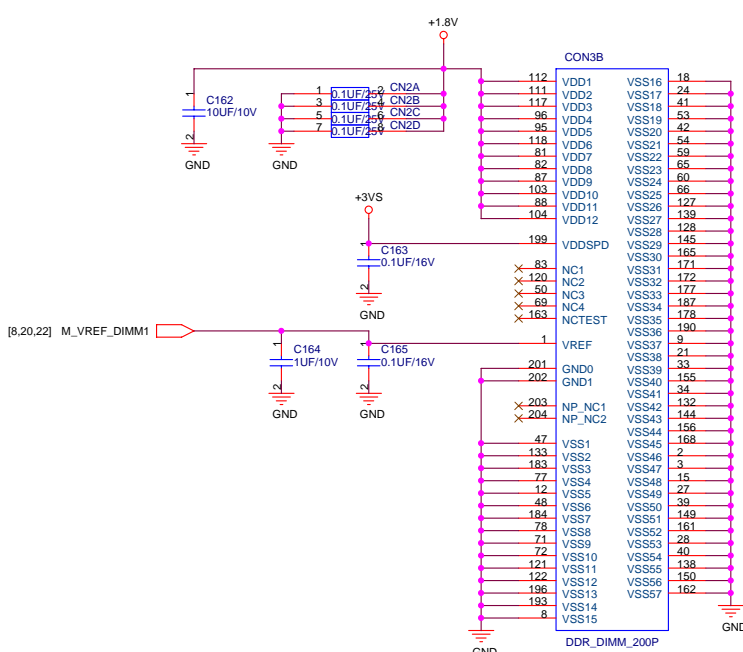
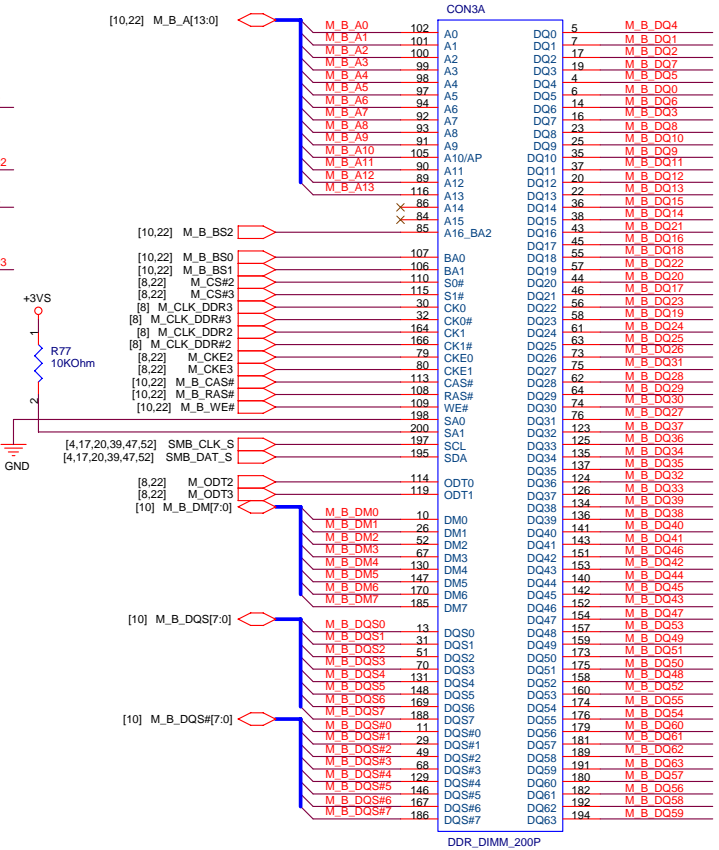
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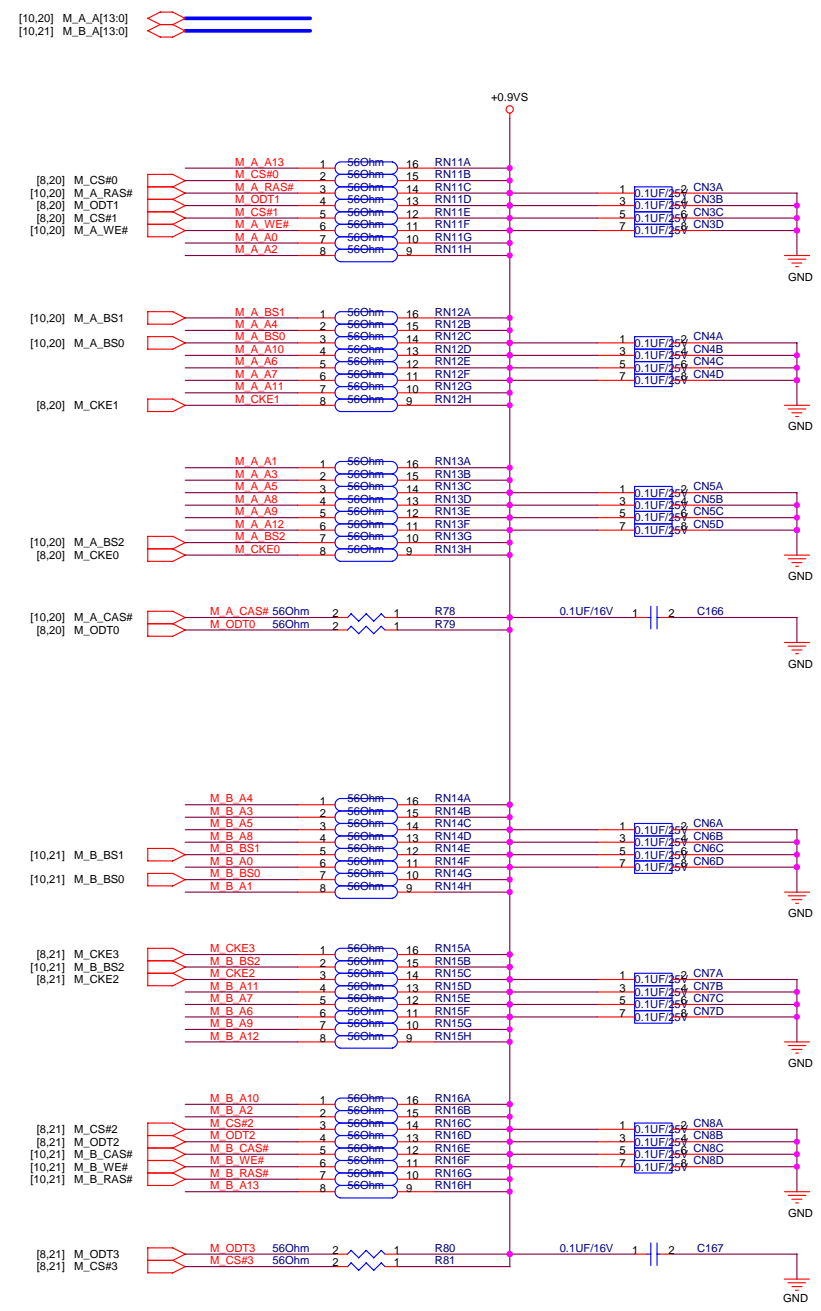
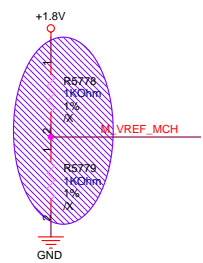
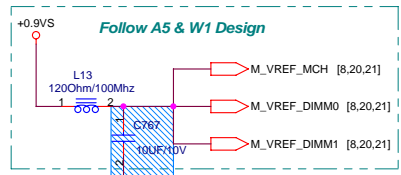
REV Type

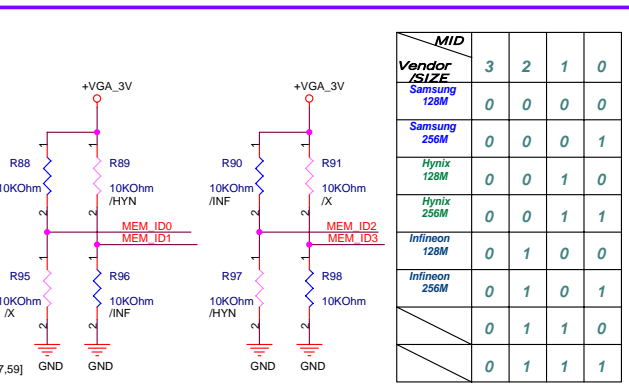
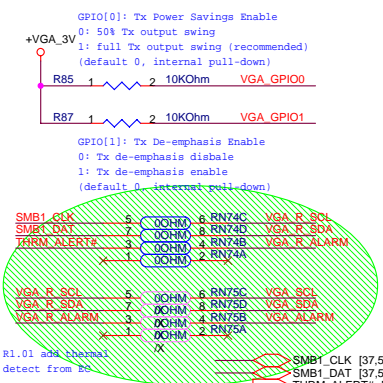


M_B_DQ[63:0] [10]

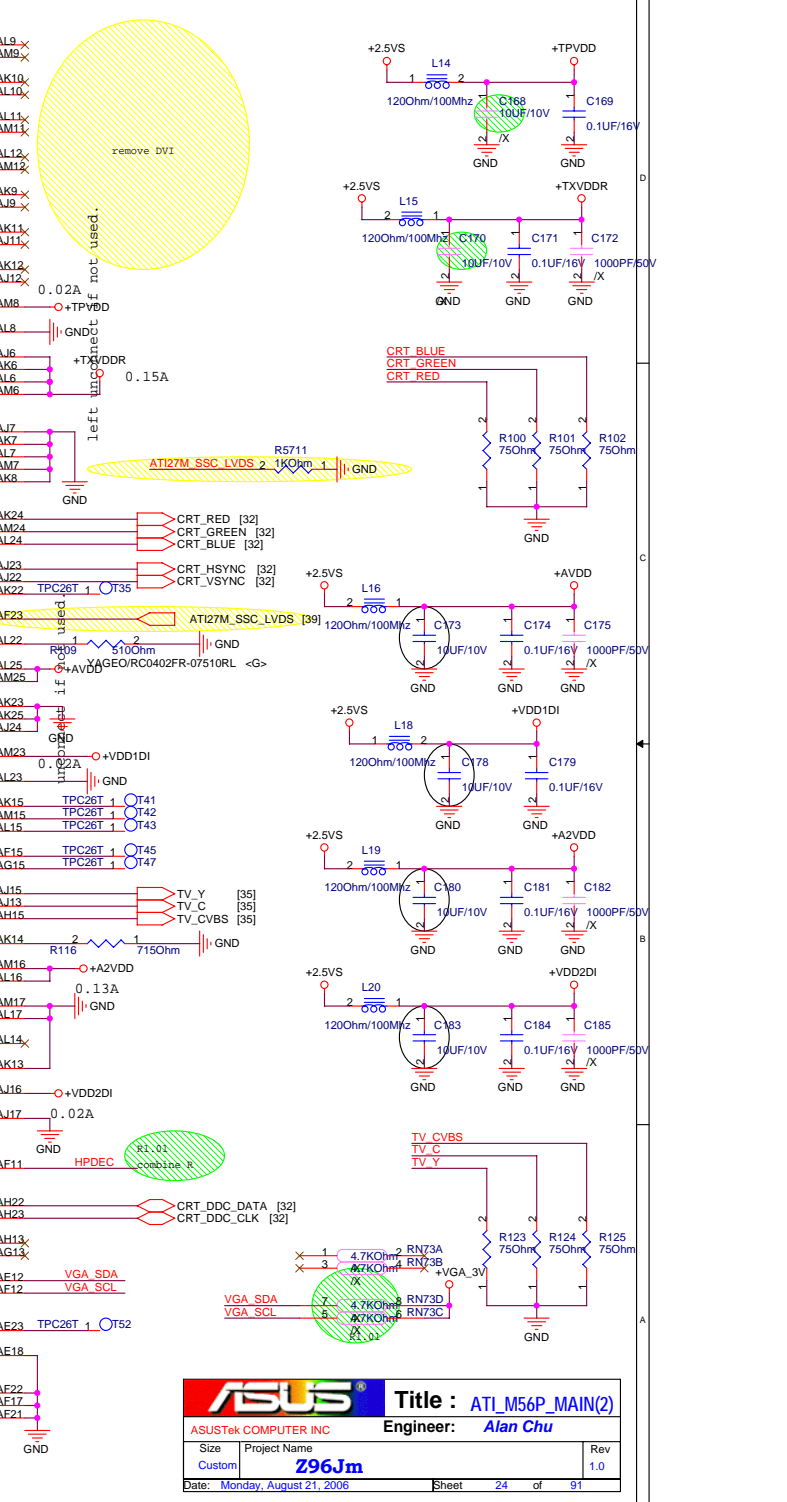
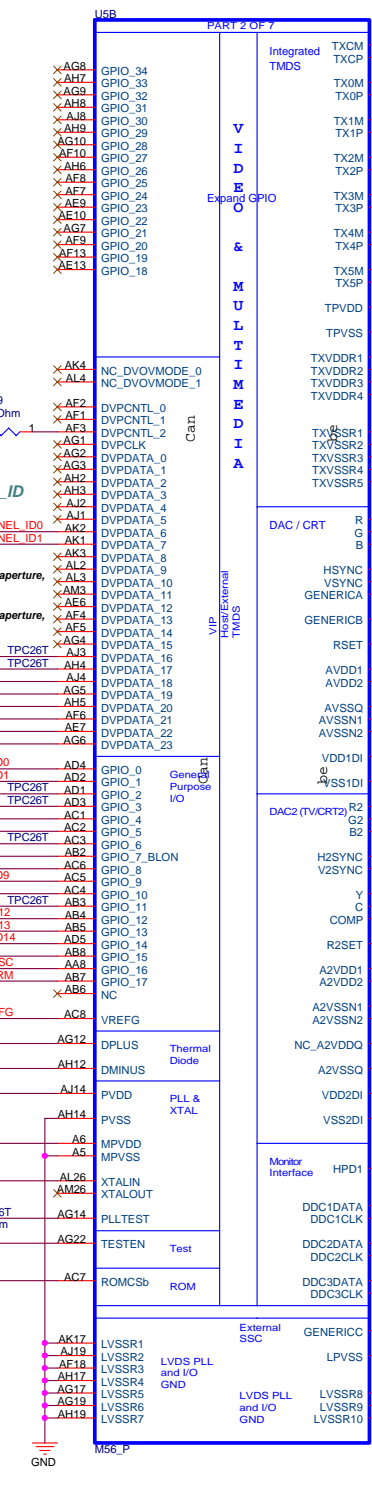
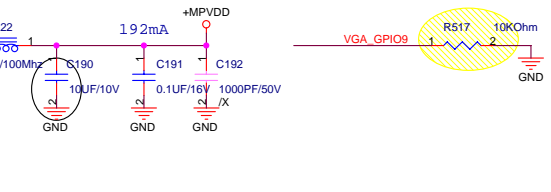
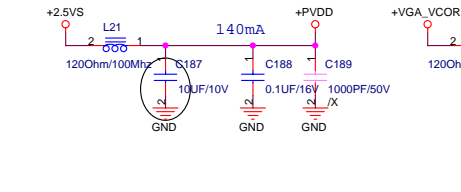
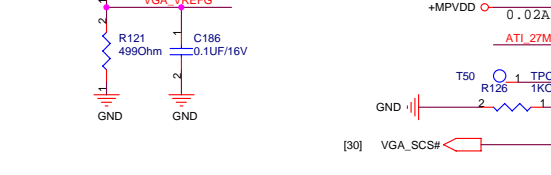
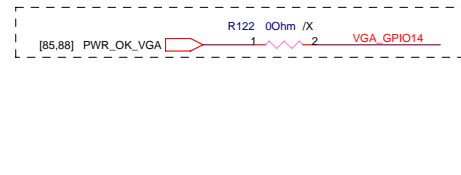
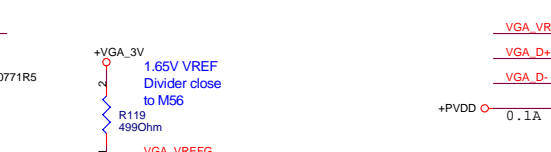
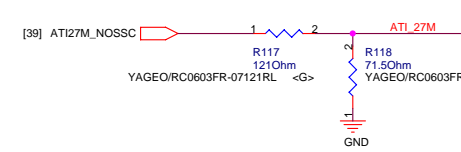
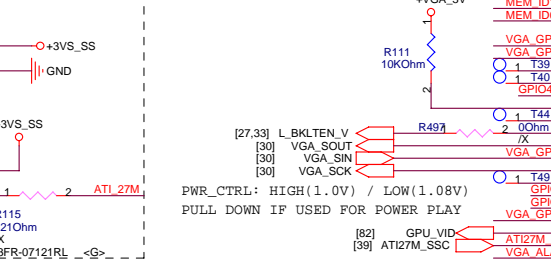
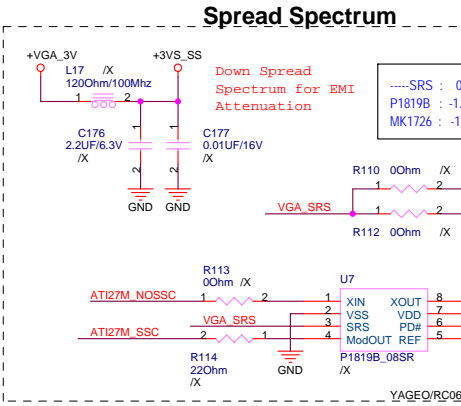
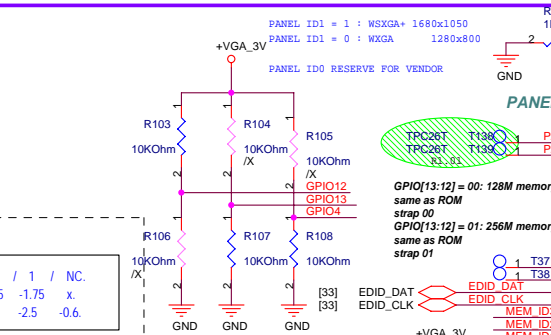
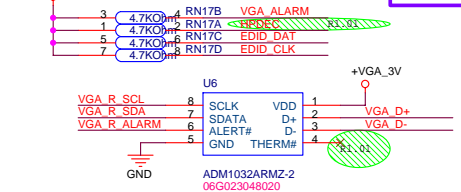
STD Type

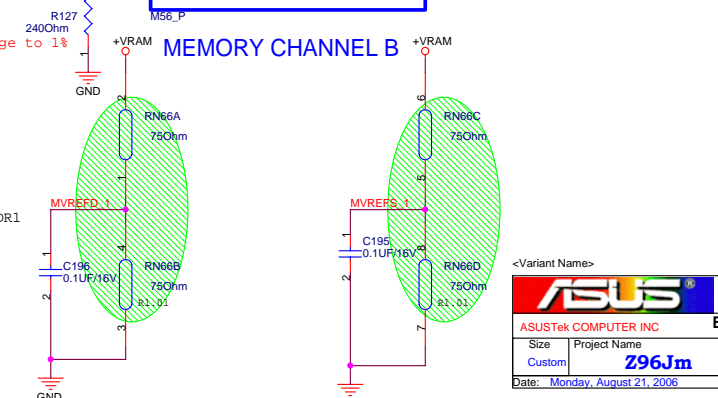
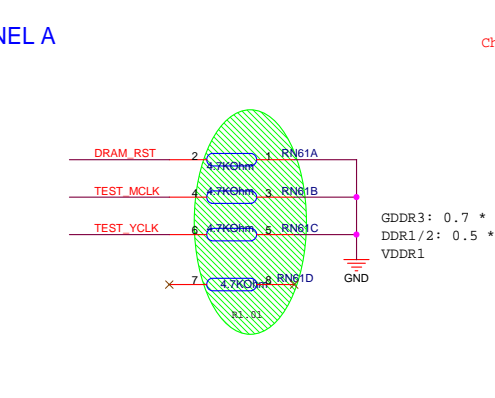
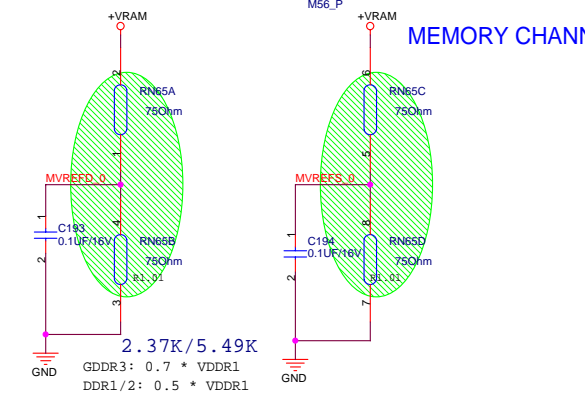
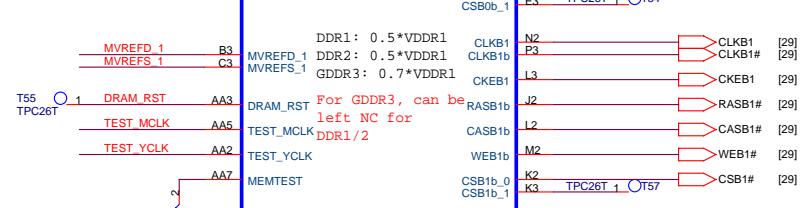
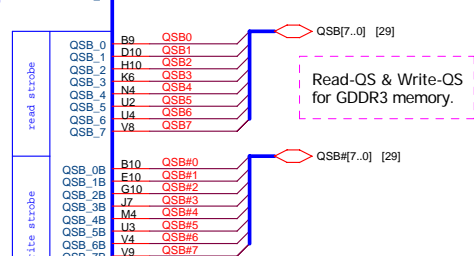
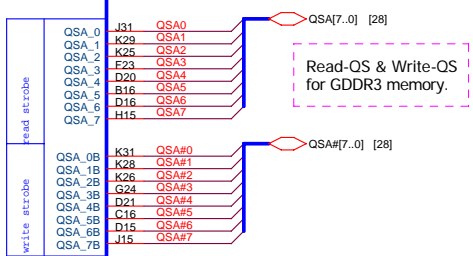
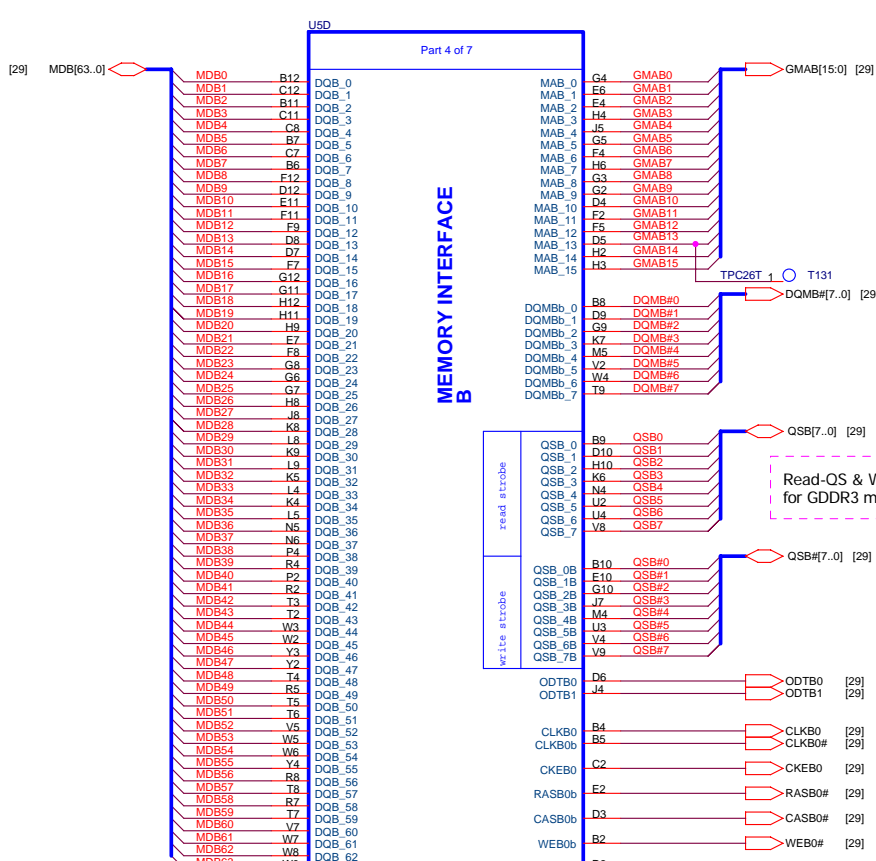
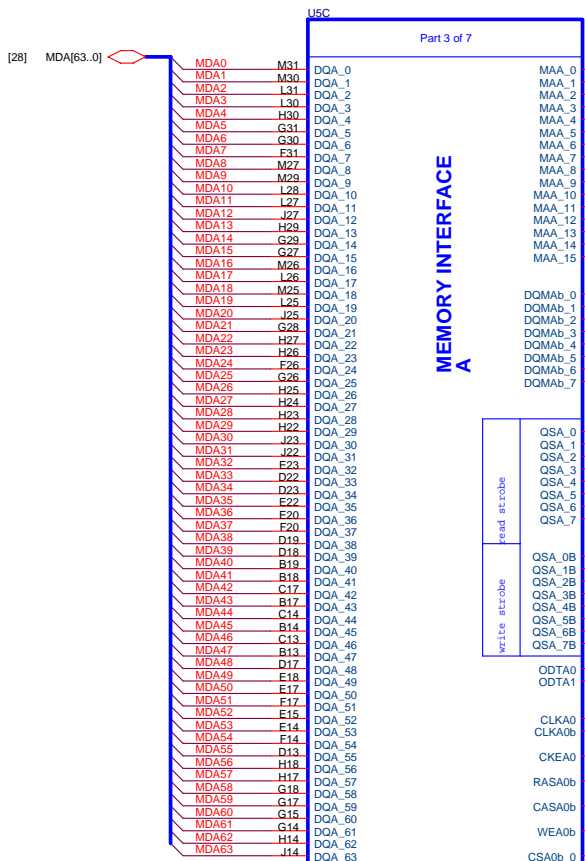






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Vendor	SIZE				
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Samsung	256M	0	0	0	1
Hynix	128M	0	0	1	0
Hynix	256M	0	0	1	1
Infineon	128M	0	1	0	0
Infineon	256M	0	1	0	1
		0	1	1	0
		0	1	1	1





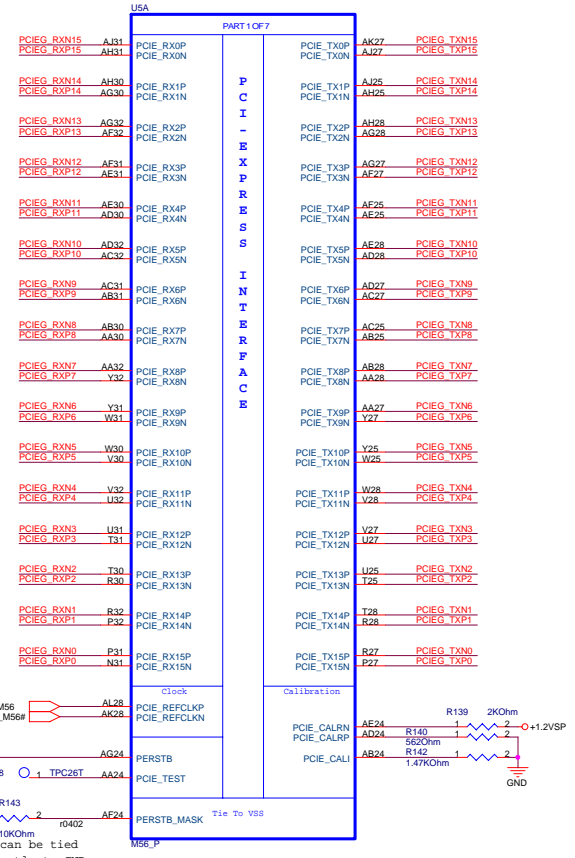
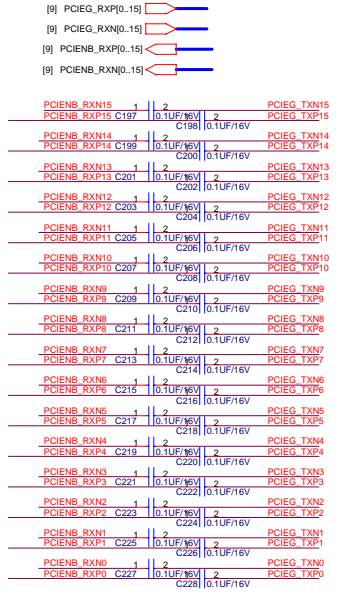
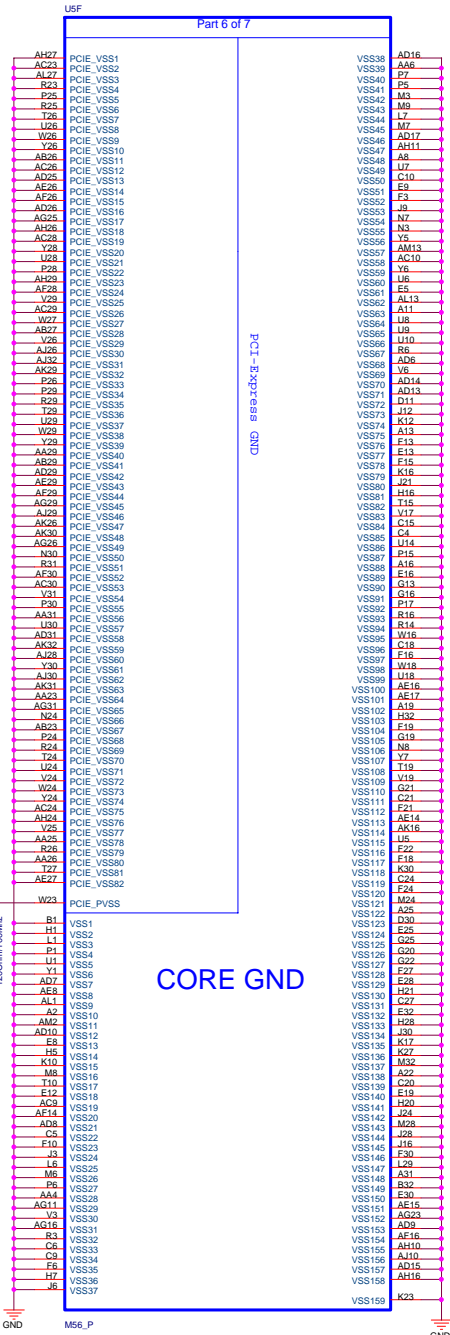
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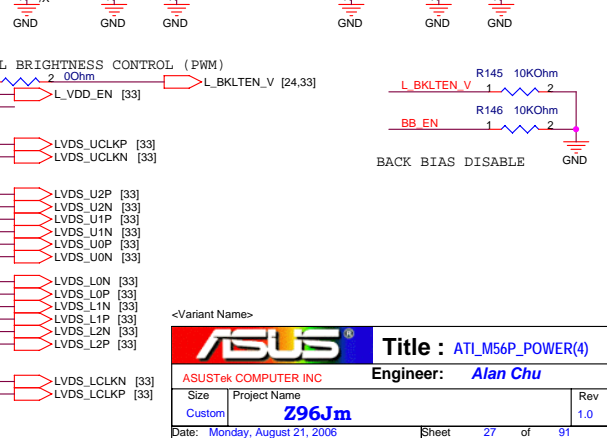
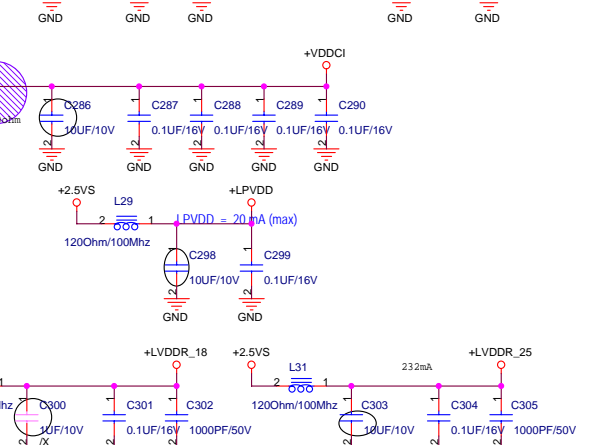
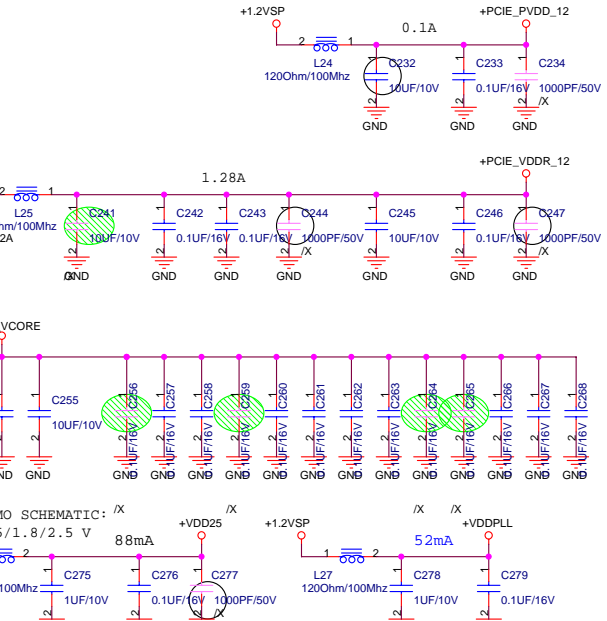
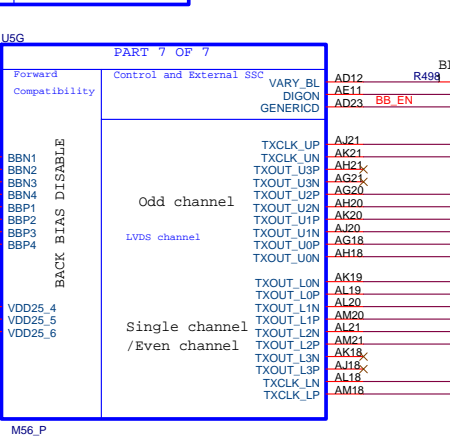
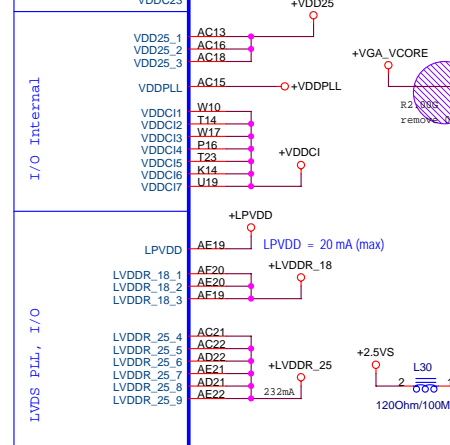
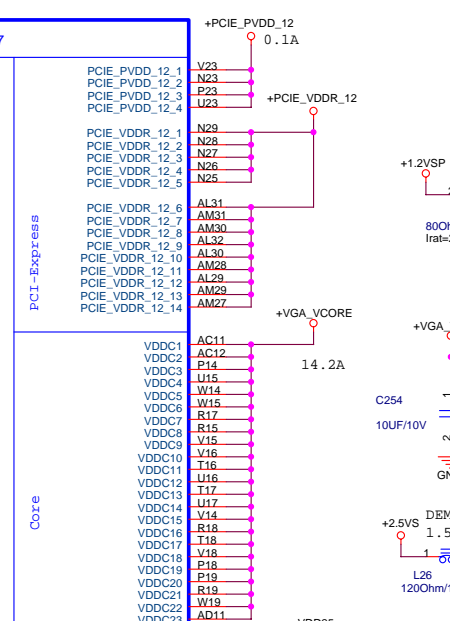
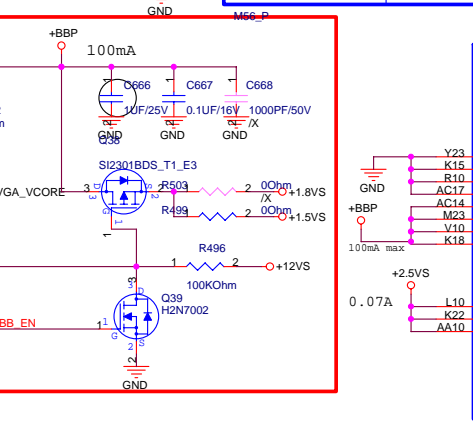
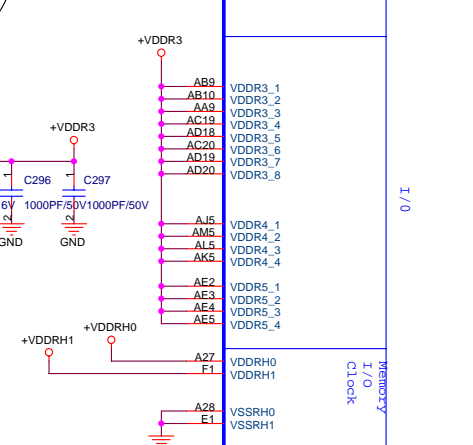
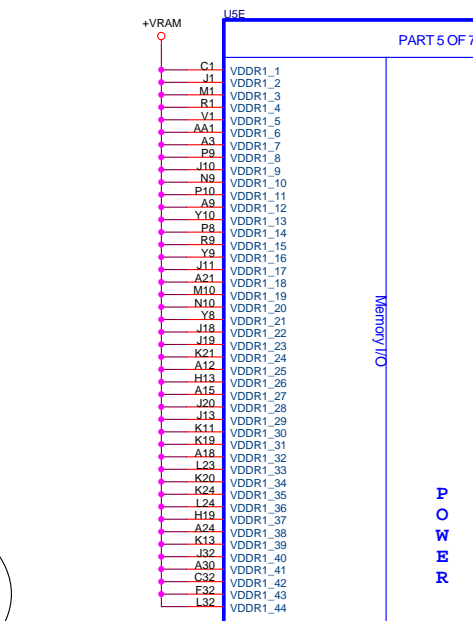
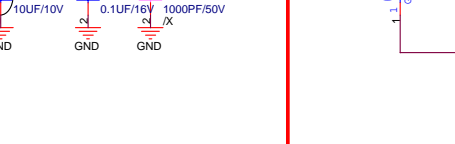
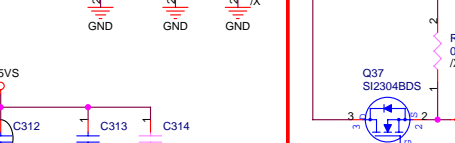
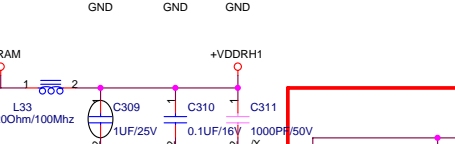
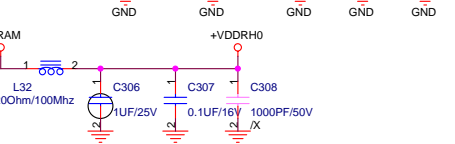
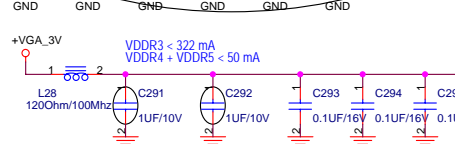
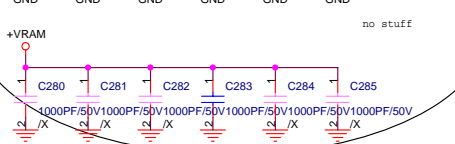
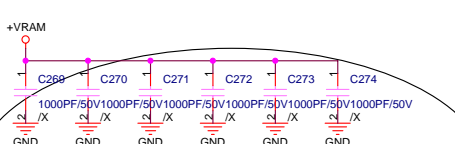
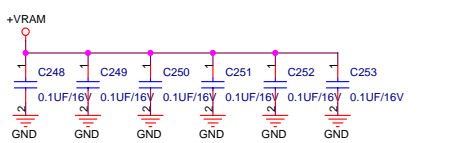
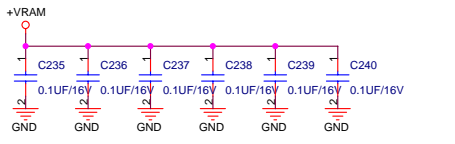
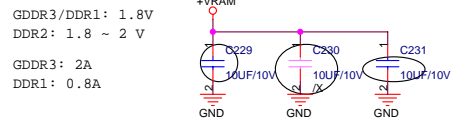
ASUS Title : AT1_M56P_Memory(3)

ASUSTek COMPUTER INC Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 25 of 91





<Variant Name>

Title : ATL_M56P_POWER(4)

ASUSTek COMPUTER INC Engineer: Alan Chu

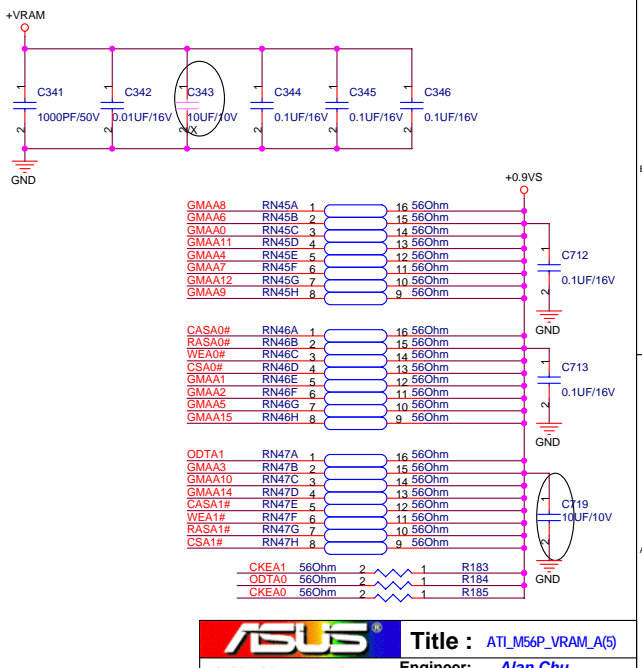
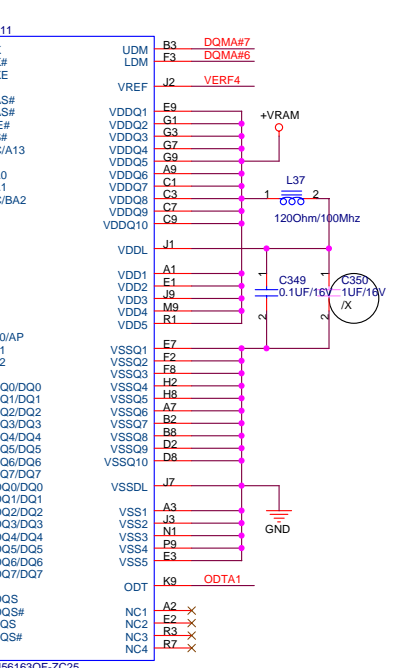
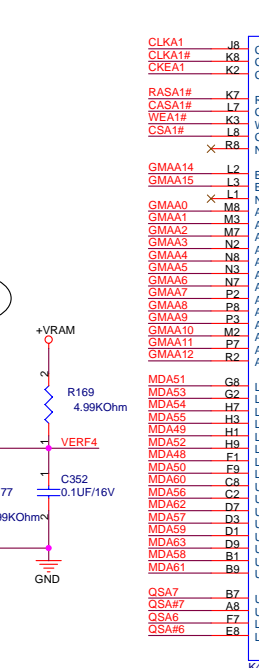
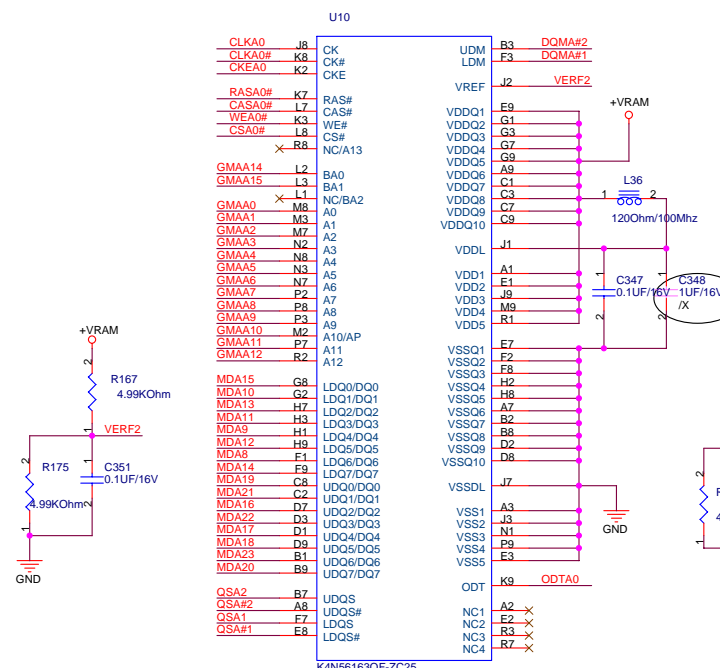
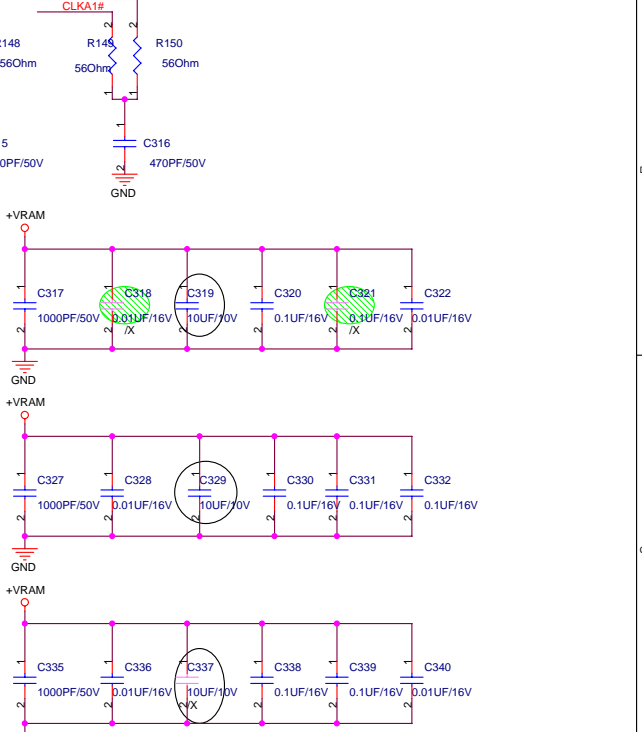
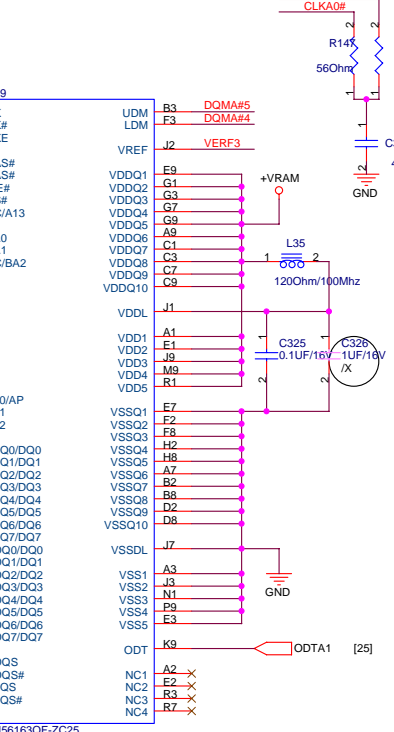
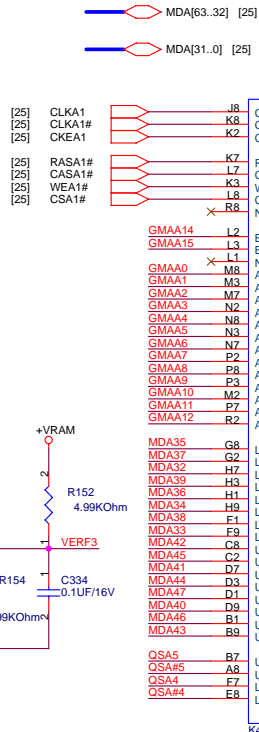
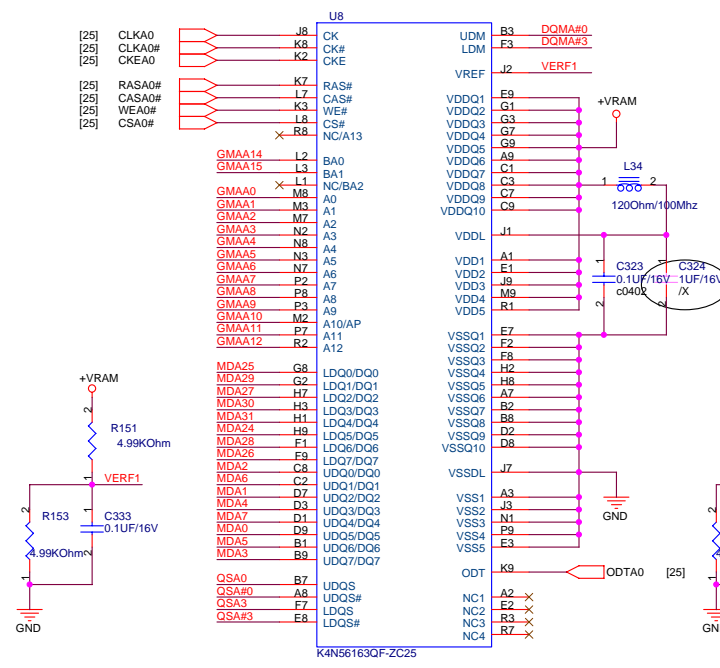
Size Project Name

Custom 296Jm

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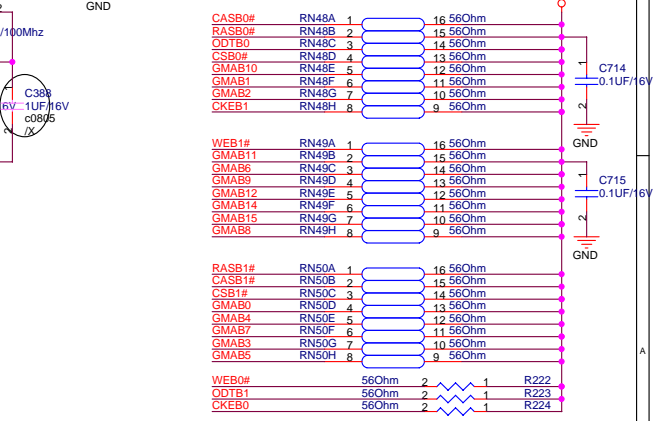
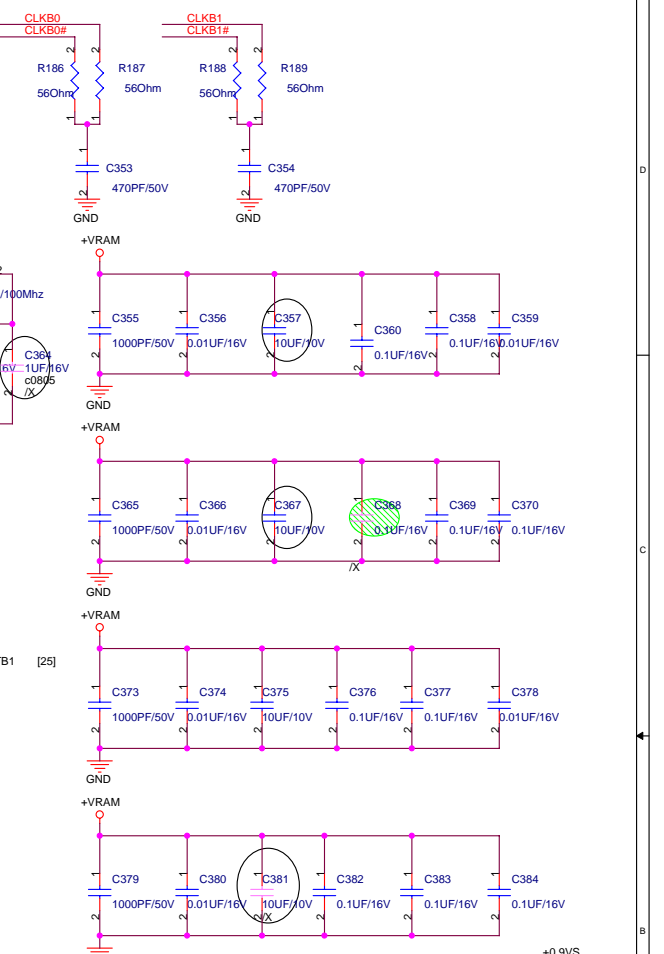
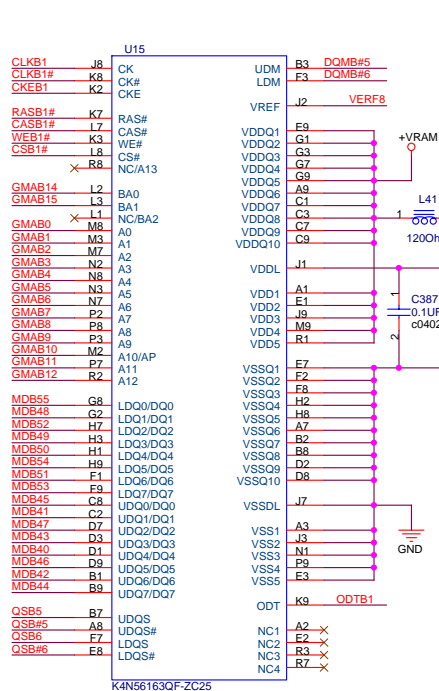
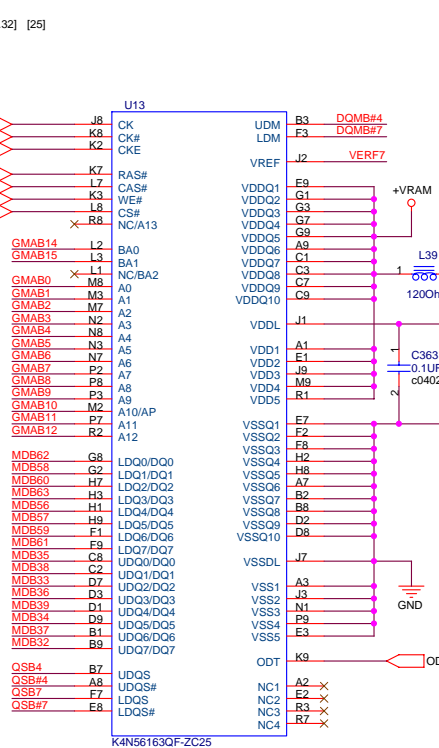
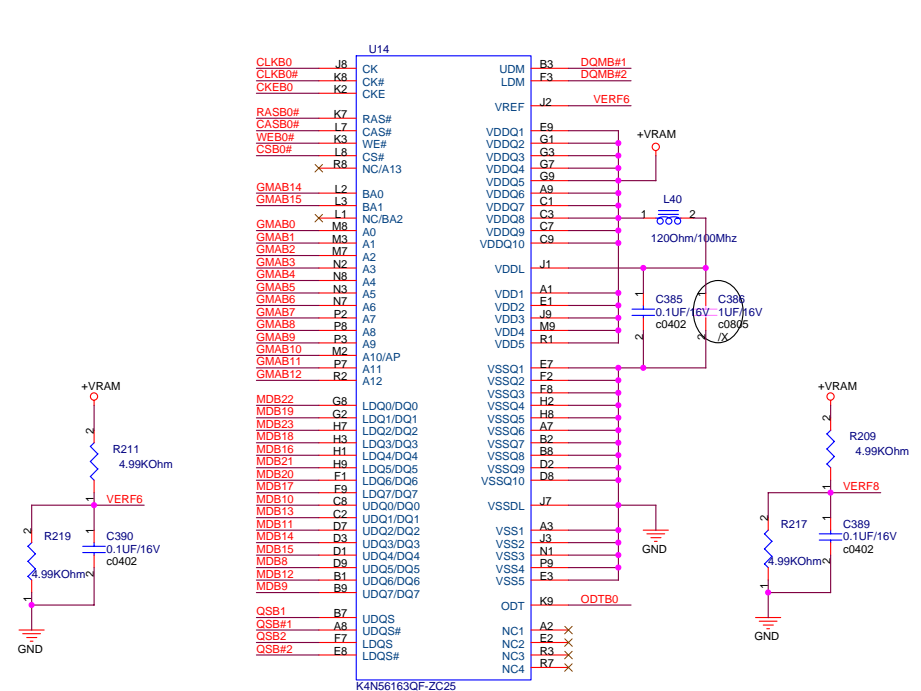
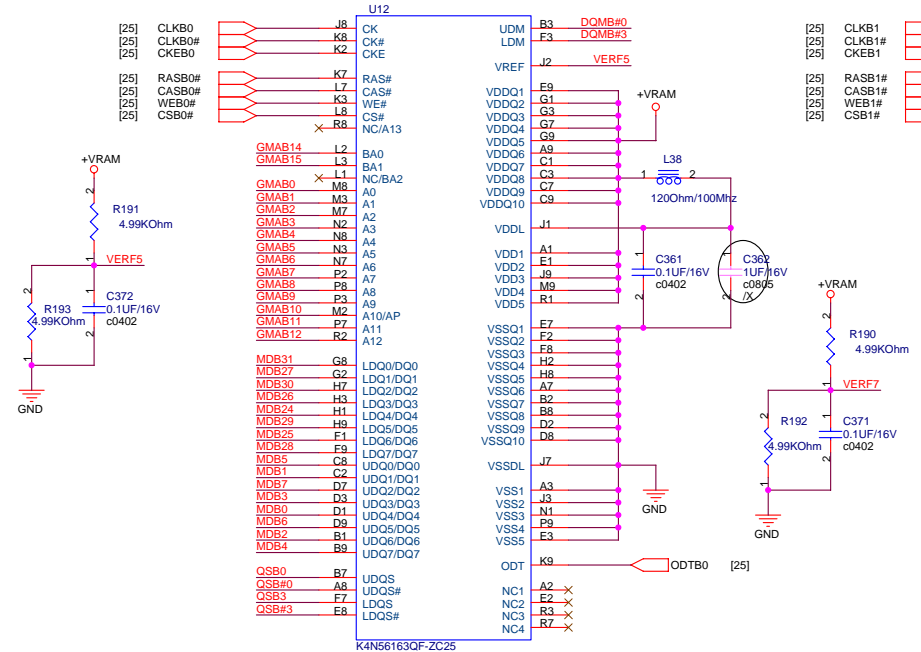
Rev 1.0

[25] GMAA[15..0] [25] QSA#[7..0]
 [25] GMAA[7..0] [25] DQMA#[7..0]



ASUS Title : ATL_M56P_VRAM_A(5)
 ASUSTek COMPUTER INC Engineer: Alan Chu
 Size Project Name
 Custom Z96Jm
 Date: Monday, August 21, 2006 Sheet 28 of 91
 Rev 1.0

- [25] GMAB[15..0]
- [25] QSB[7..0]
- [25] QSB# [7..0]
- [25] DQMB# [7..0]

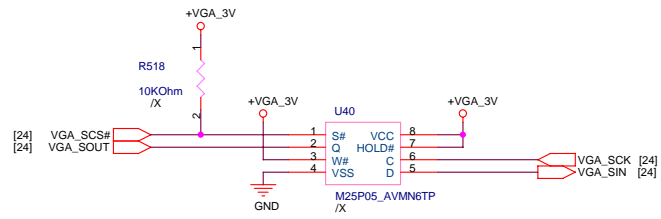


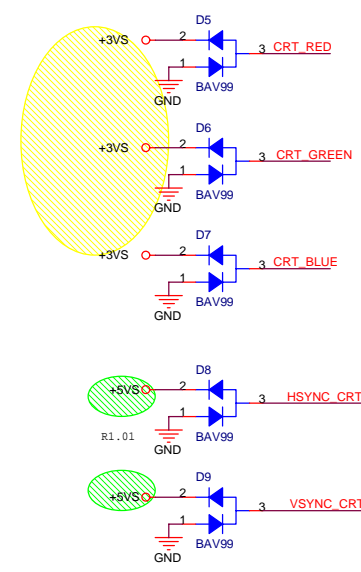
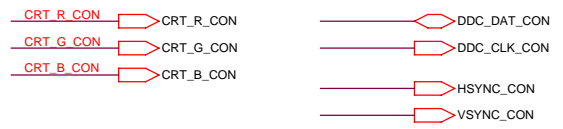
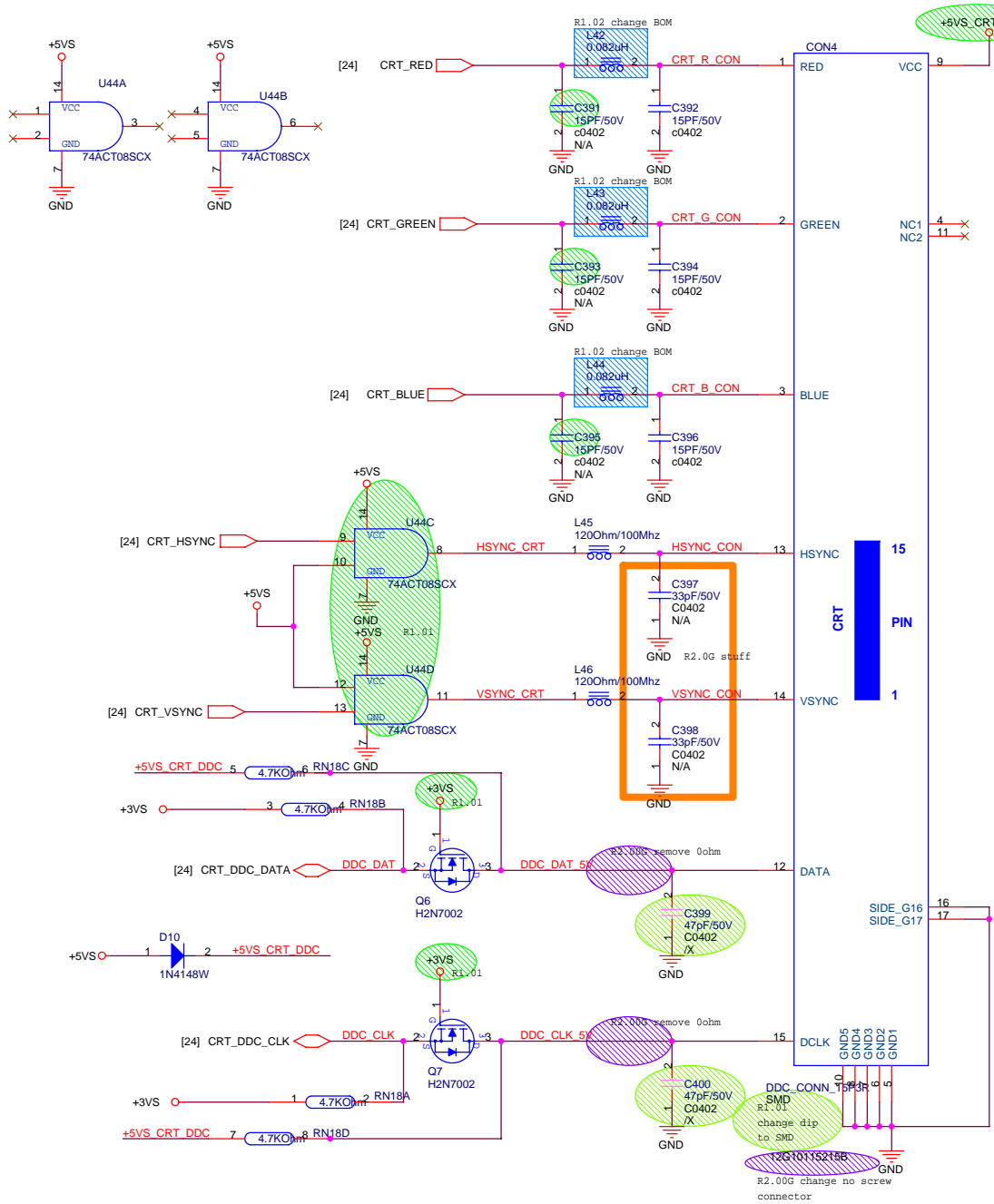
ASUS Title : ATI_M56P_VRAM(B)

ASUSTek COMPUTER INC Engineer: Alan Chu

Size Project Name
Custom Z96Jm

Date: Monday, August 21, 2006 Sheet 29 of 91



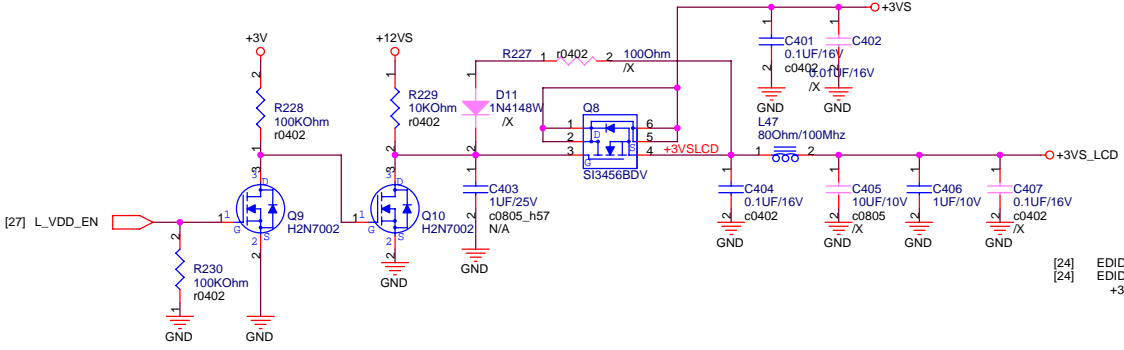


PLACE ESD Diodes near VGA port

ASUS		Title : CRT	
ASUSTek COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
Custom	Z96Jm	1.0	
Date: Monday, August 21, 2006	Sheet 32 of 91		

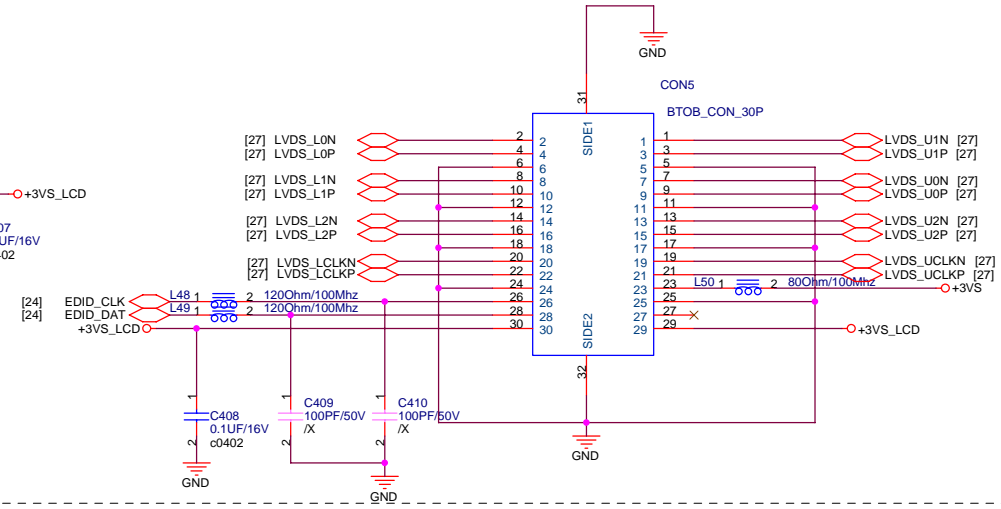
LCD Backlight Control

LCD Power



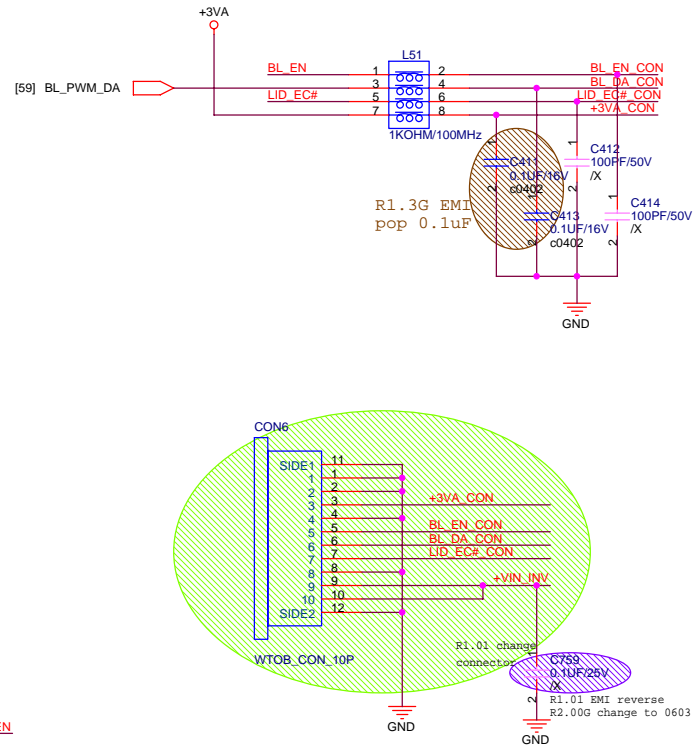
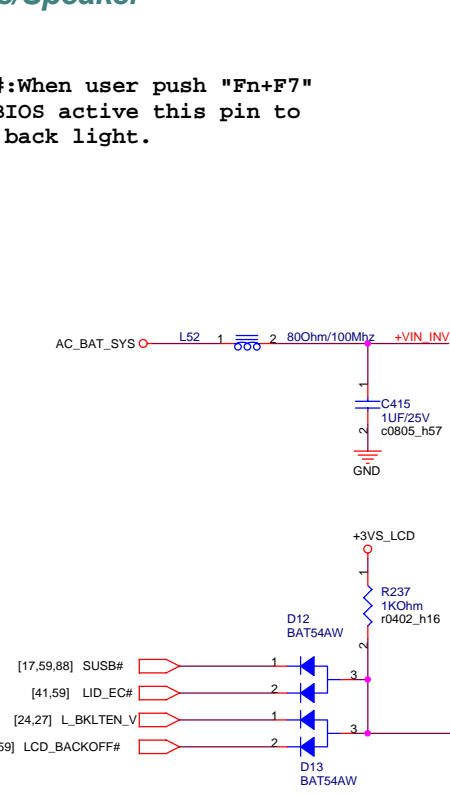
Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair (Not Ribbon)
 Maximum Length <= 16"

LCD LVDS Interface



INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.

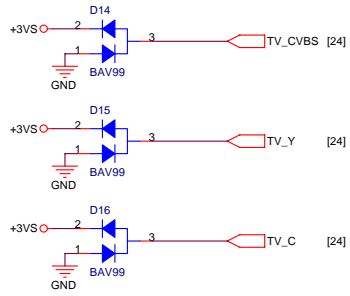


R1.01 remove #B reserve panel ID

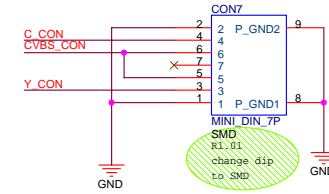
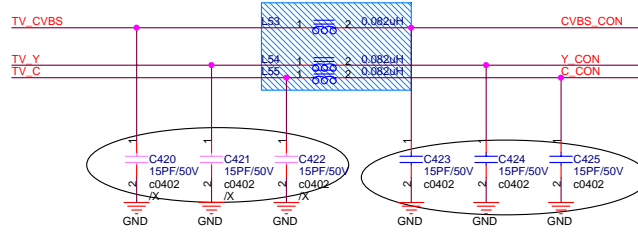
R1.01 change connector
 R1.01 EMI reverse
 R2.00G change to 0603

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
Custom	Z96Jm	1.0	
Date: Monday, August 21, 2006	Sheet	33	of 91

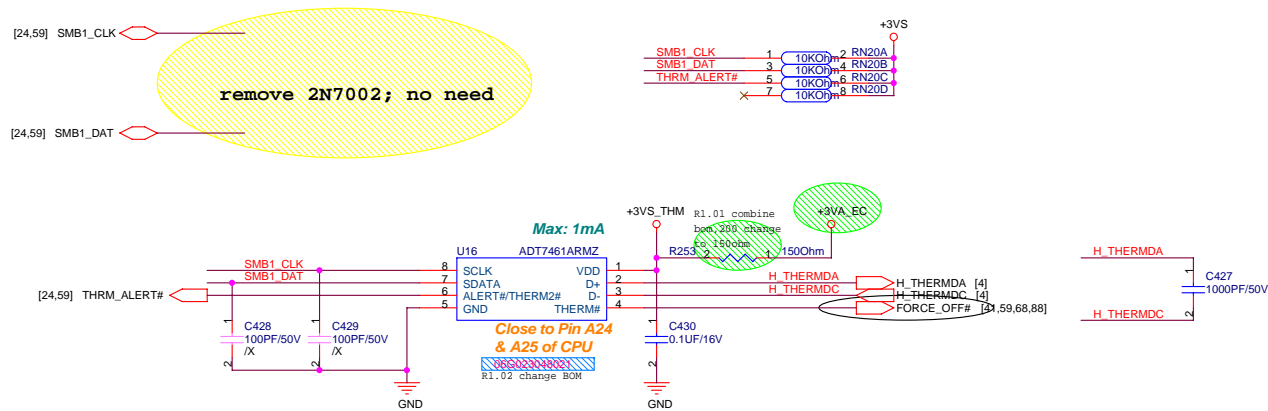
TV OUT



PLACE ESD
Diodes near
TV port



Thermal Sensor

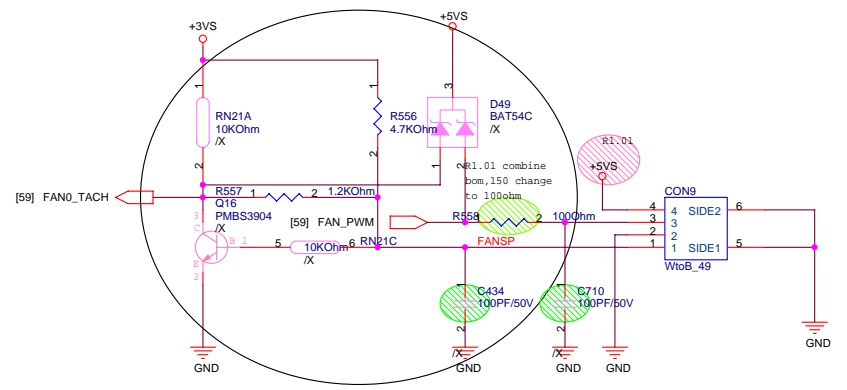
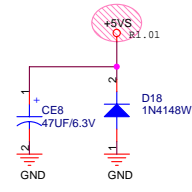
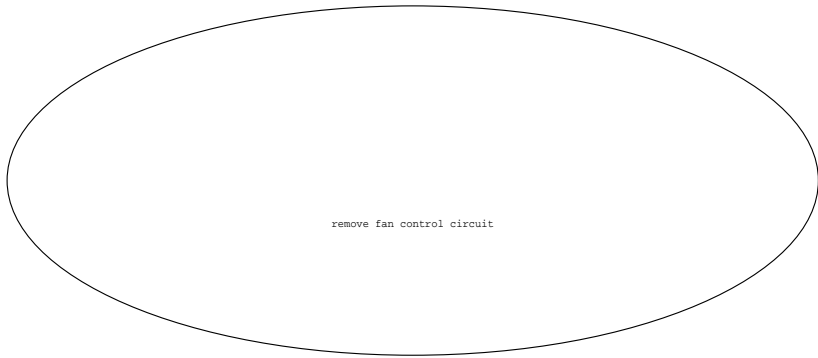


Route H_THERMDA and H_THERMDC on the same layer

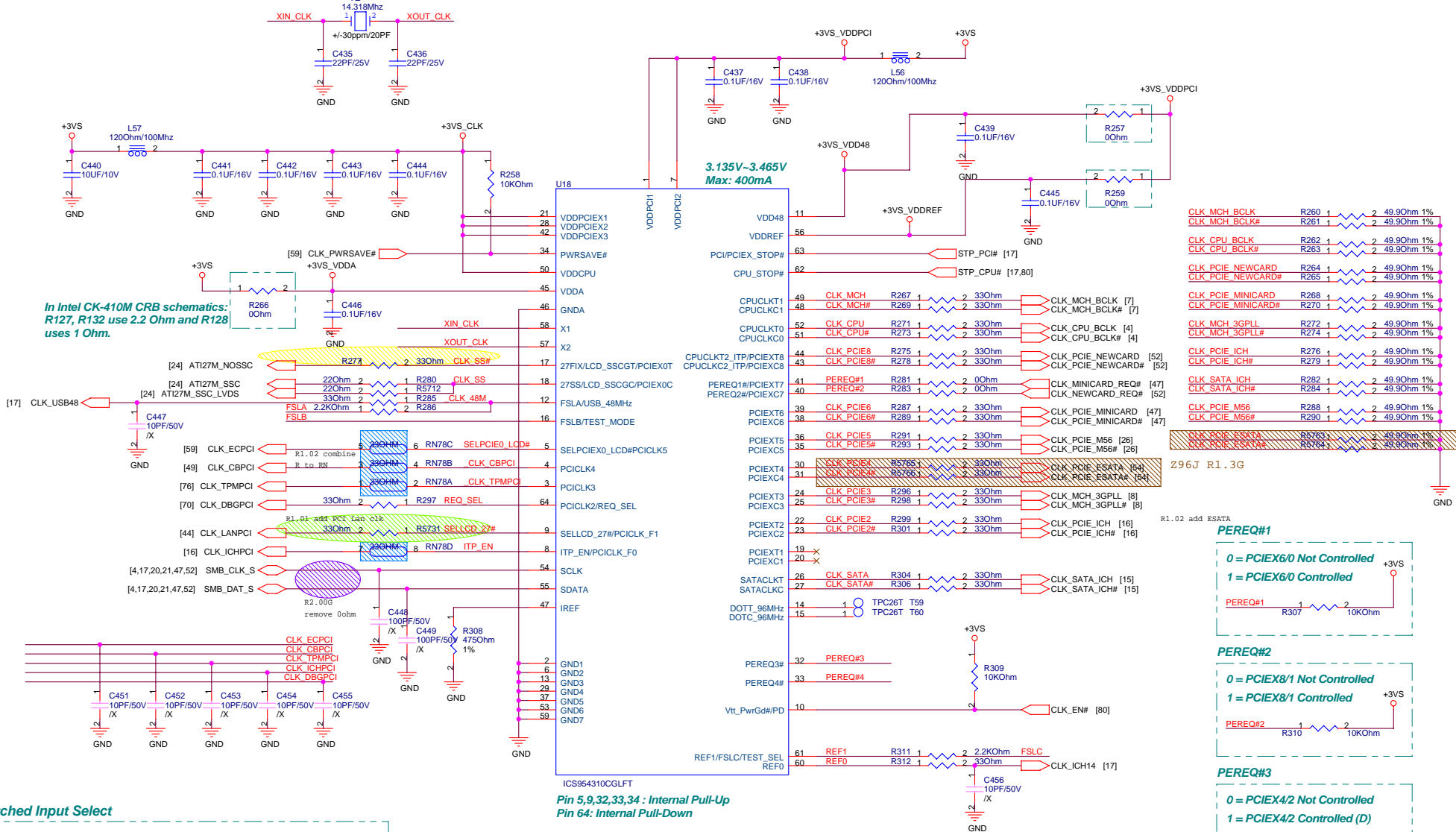
-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



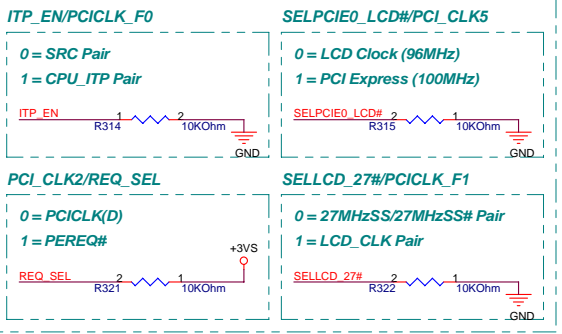
CPU FAN will be forced on:
1) Thermal Sensor Over-temperature
2) WATCHDOG asserted by EC



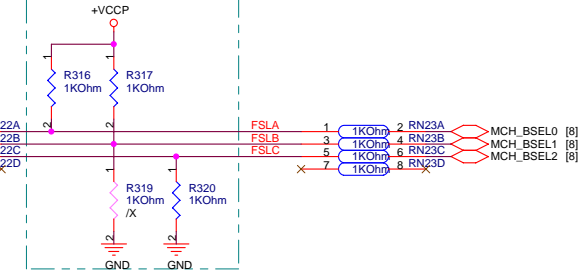
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128
uses 1 Ohm.

ICS954310CGLFT
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down

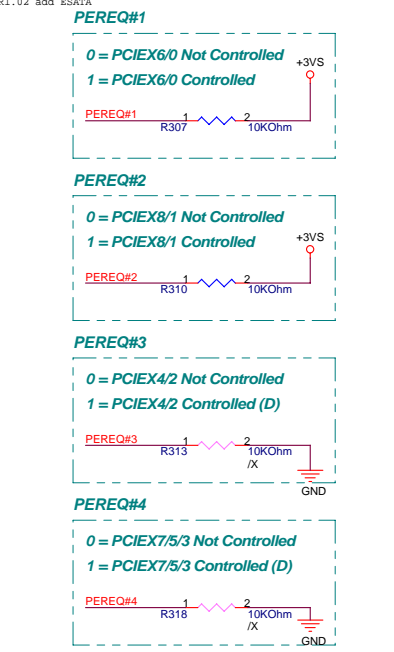
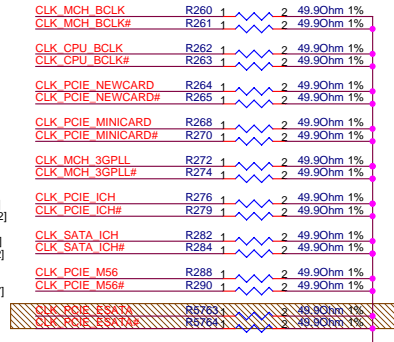
Latched Input Select

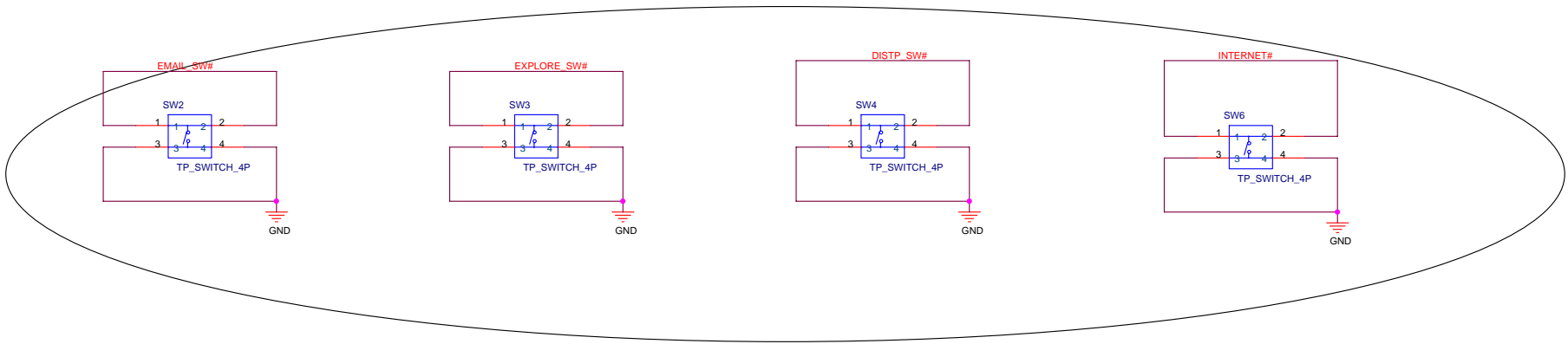
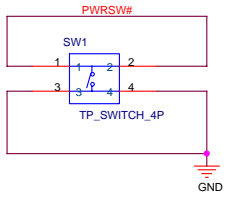


Reserved for Debug & Experiment

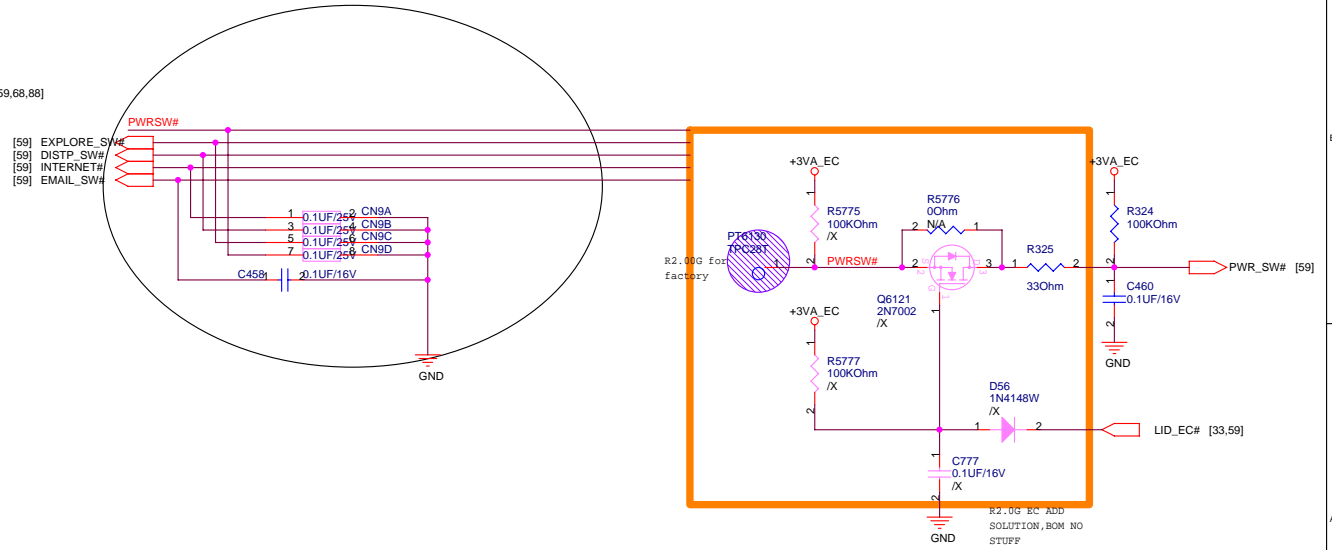
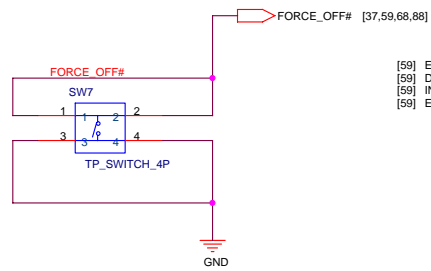


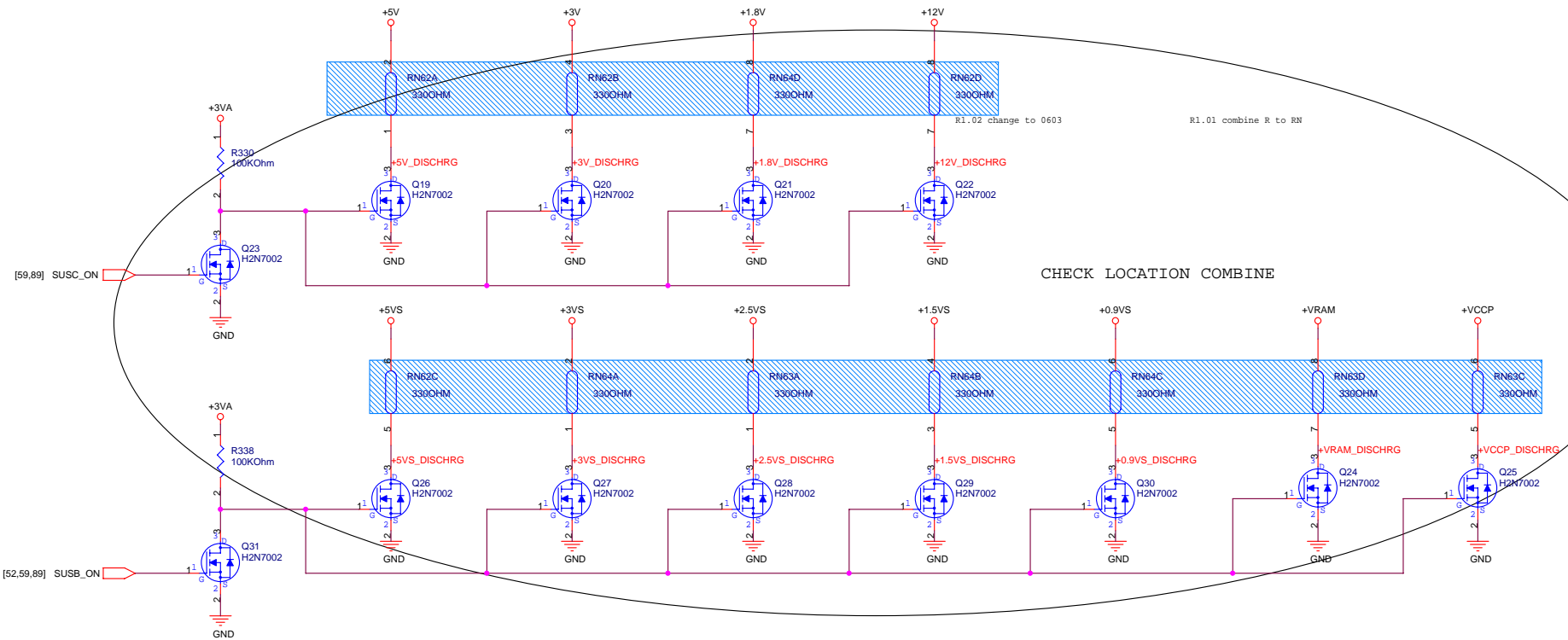
BCLK	FSB	BSEL1	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H





SHUT_DOWN#



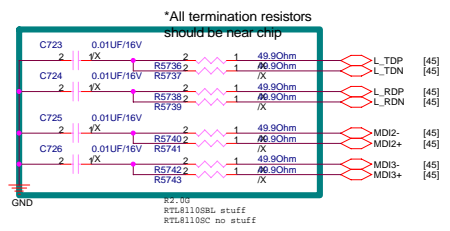
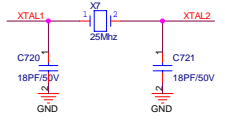
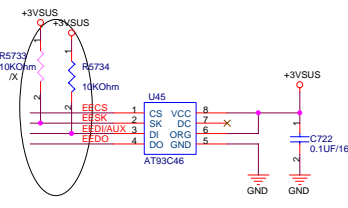


[59,89] SUSC_ON

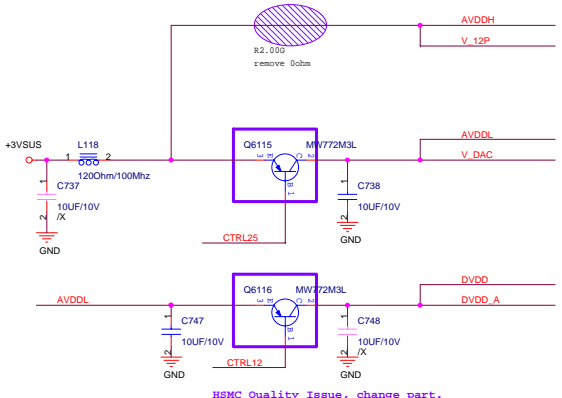
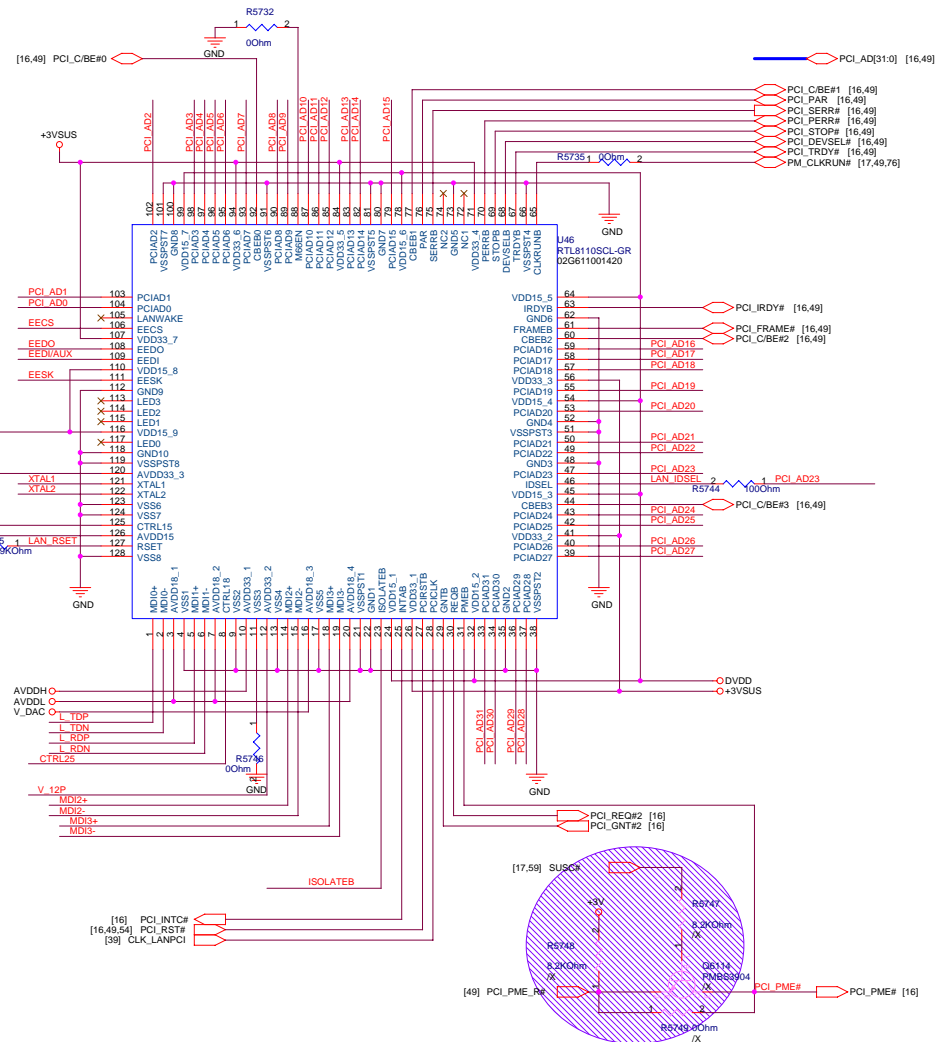
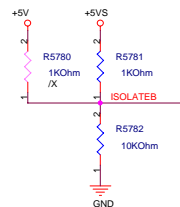
[52,59,89] SUBS_ON

CHECK LOCATION COMBINE

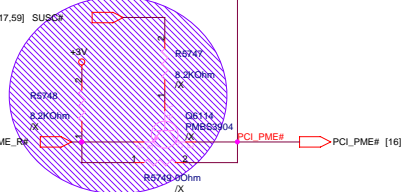
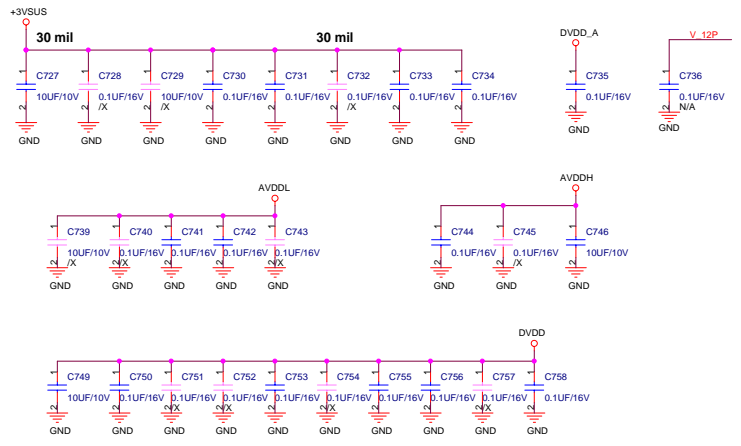
3 330OHM 4 RN63B



10/100=> 5.6K,1% resistor
 GLAN=> 2.49K,1% resistor

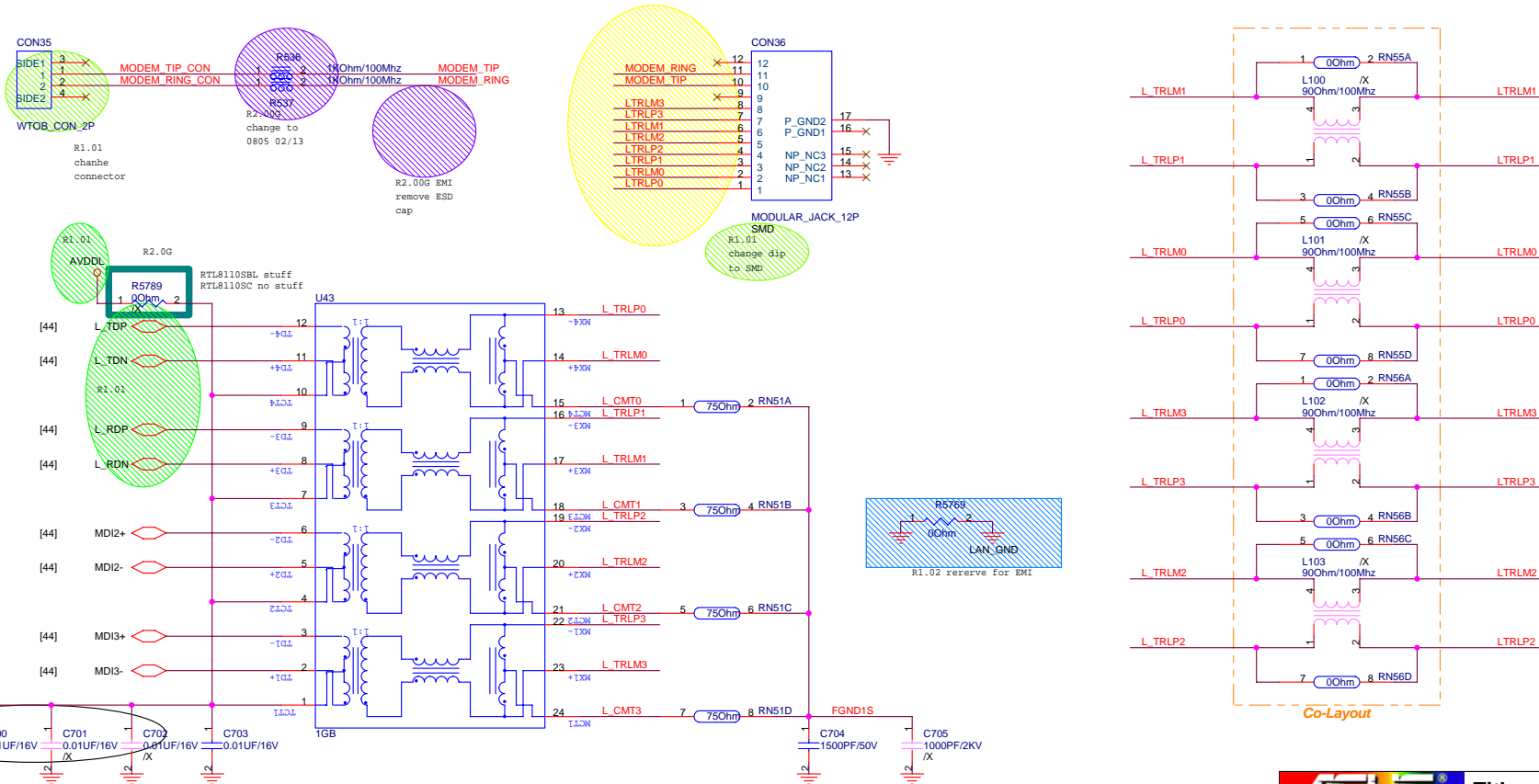
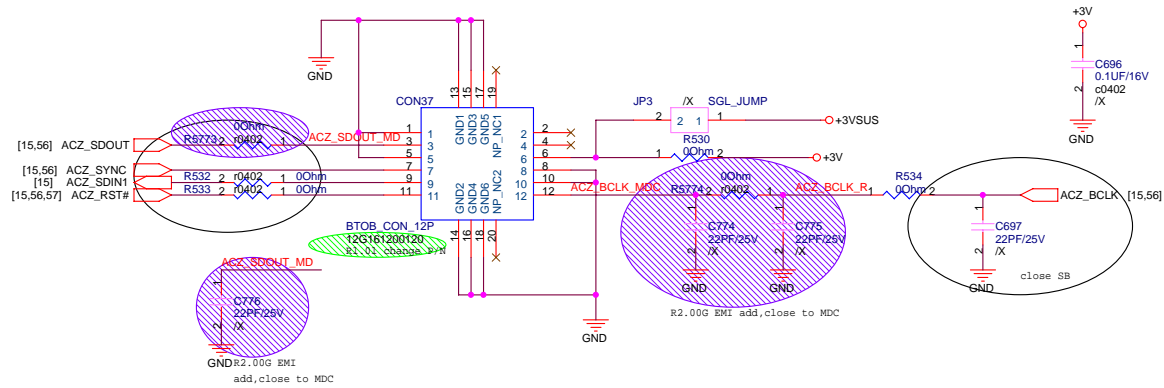


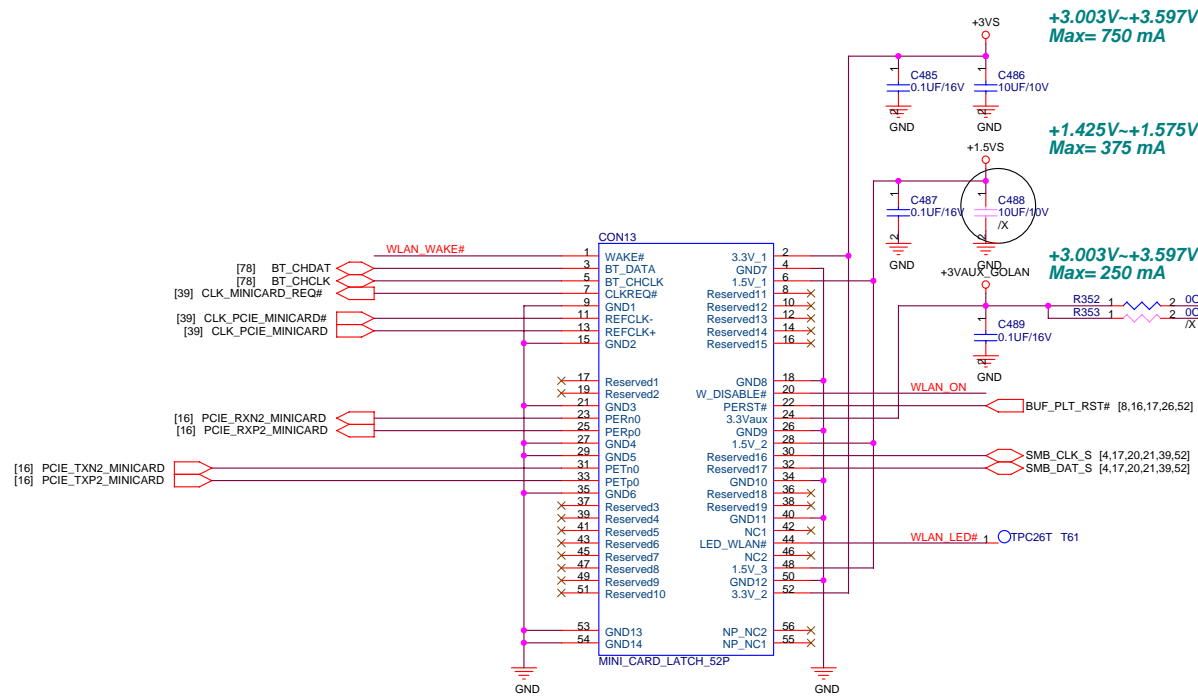
HSMC Quality Issue, change part.



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

MDC CONN.





+3.003V~+3.597V
Max= 750 mA

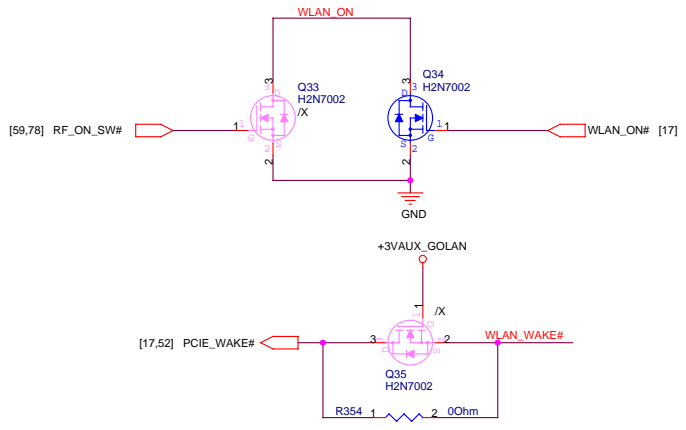
+1.425V~+1.575V
Max= 375 mA

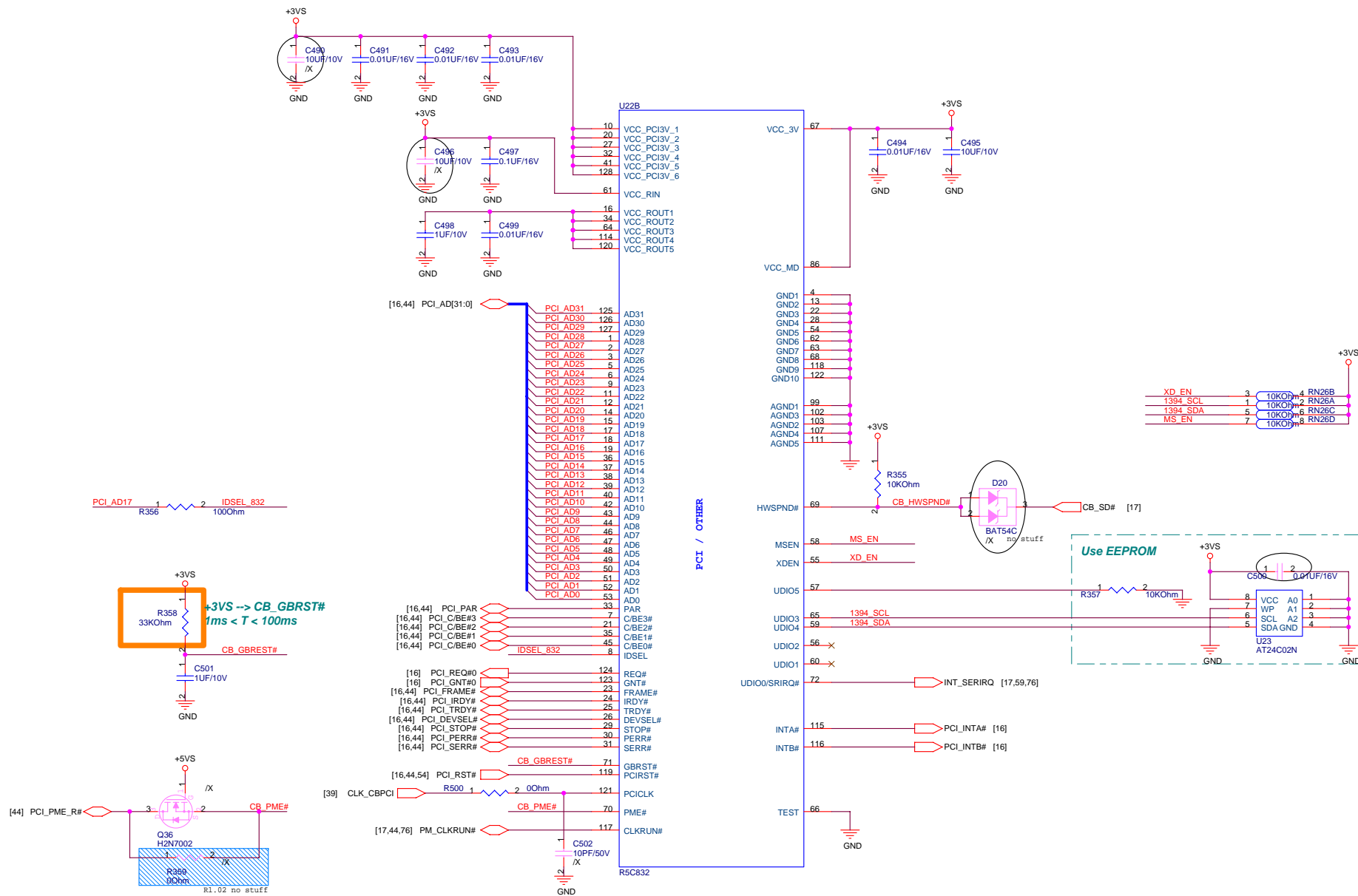
+3.003V~+3.597V
Max= 250 mA

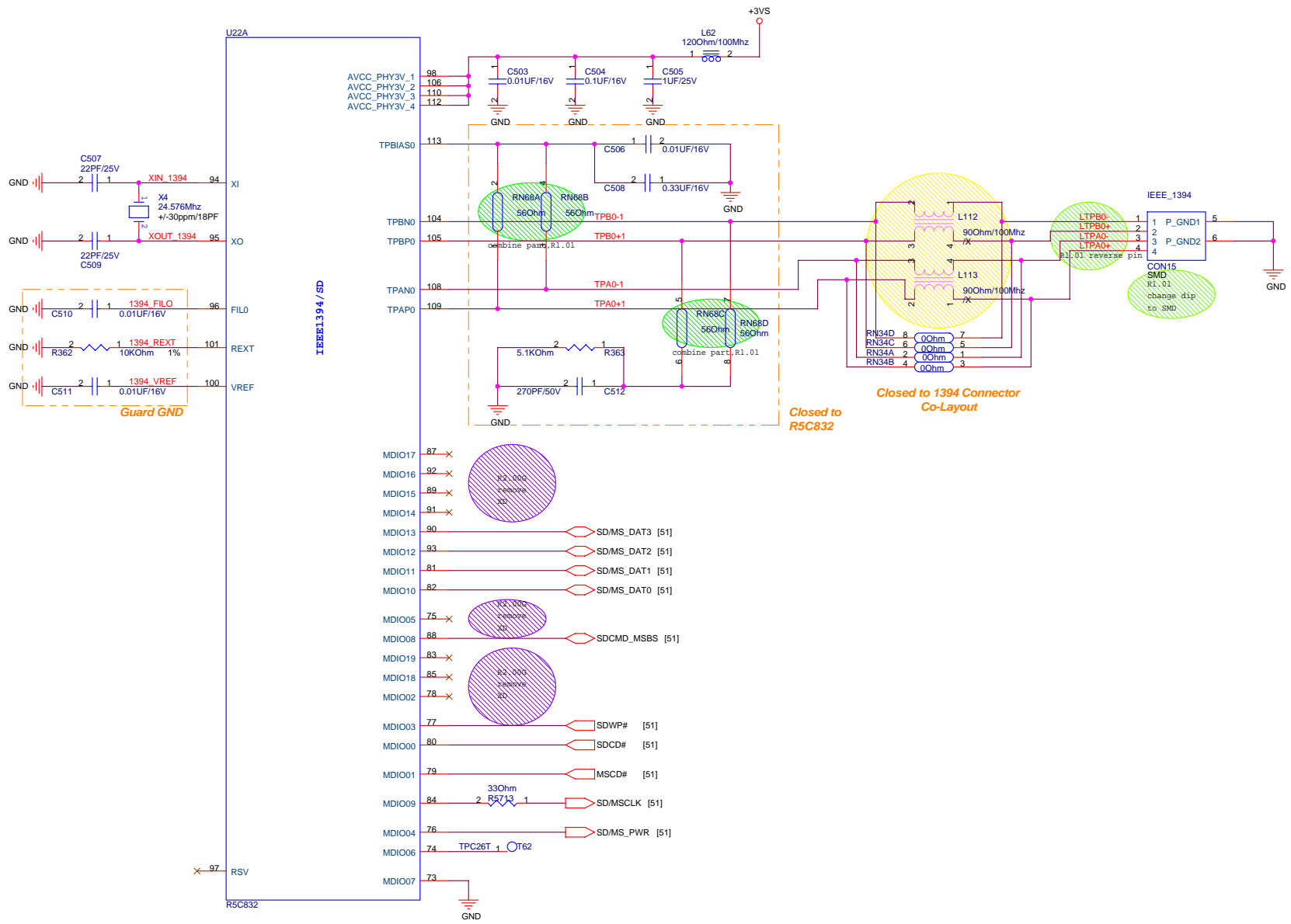
Reserved R to +3VSUS for Wake on WLAN function!

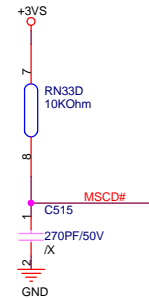
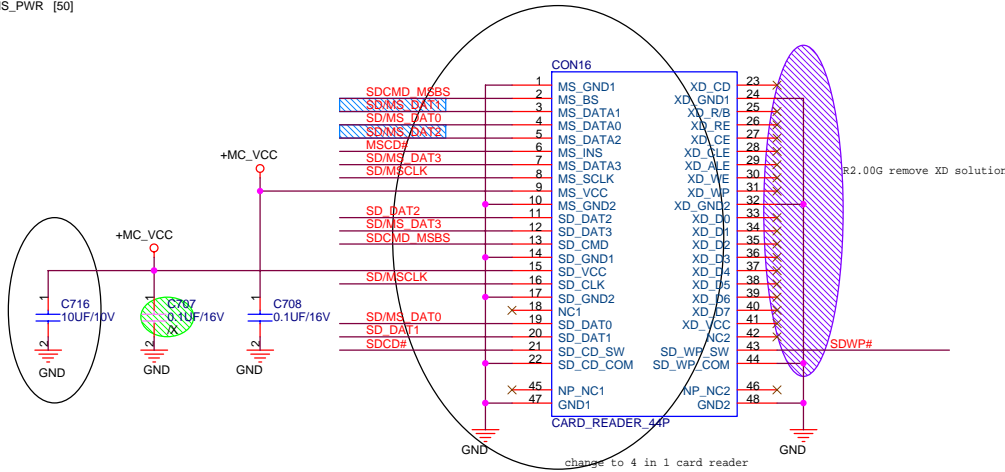
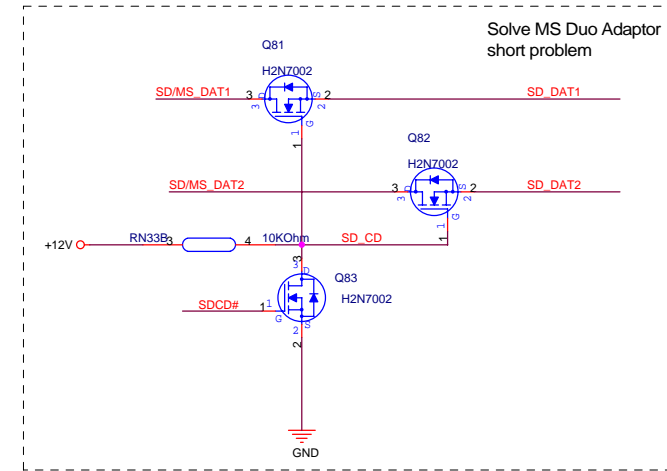
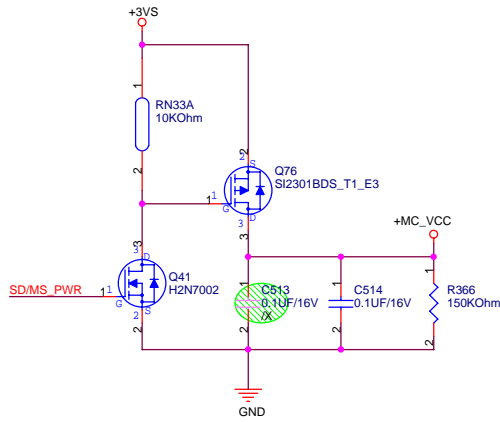
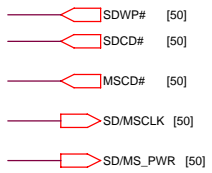
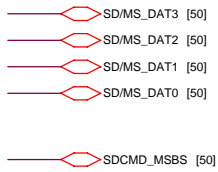
H54 & H56

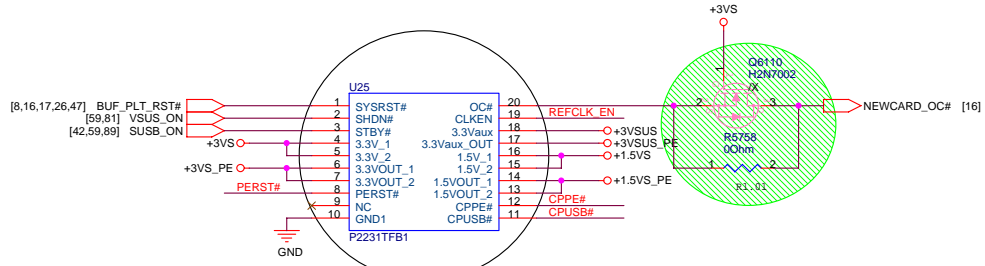
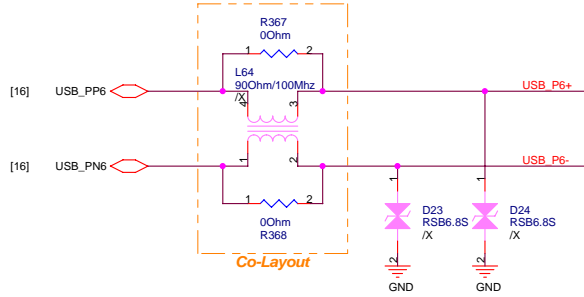
R1, Q1 remove connector, change to screw



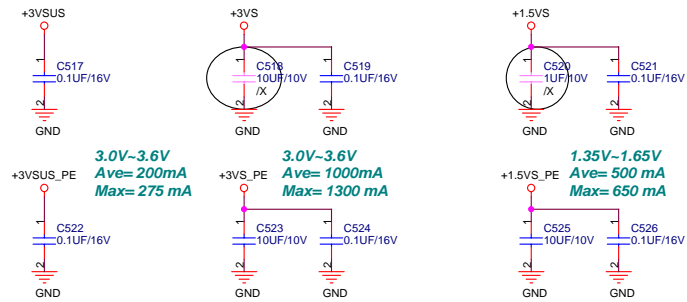
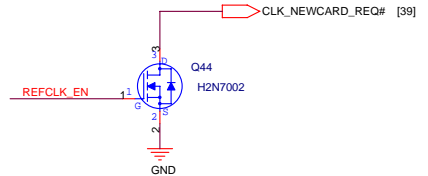








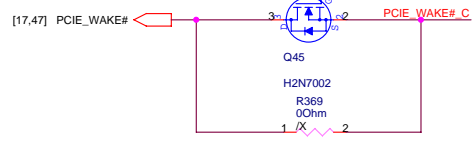
change part to Lead free



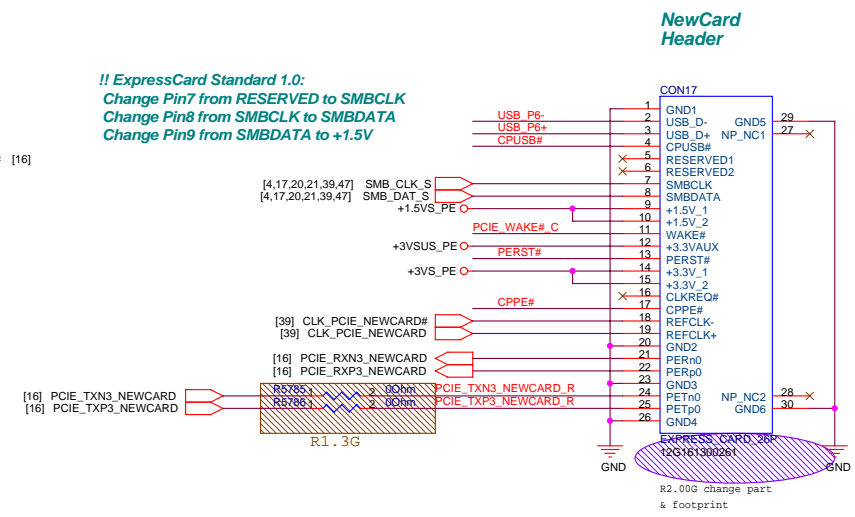
3.0V~3.6V
Ave= 200mA
Max= 275 mA

3.0V~3.6V
Ave= 1000mA
Max= 1300 mA

1.35V~1.65V
Ave= 500 mA
Max= 650 mA

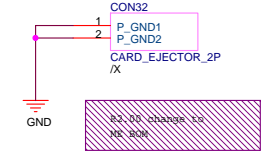


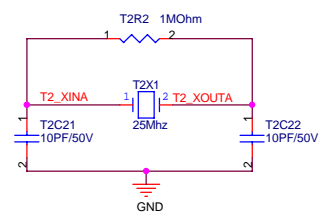
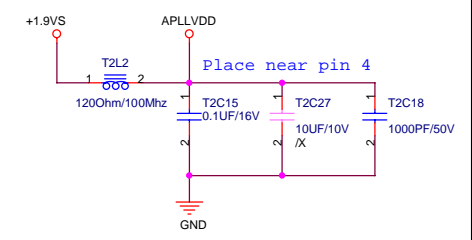
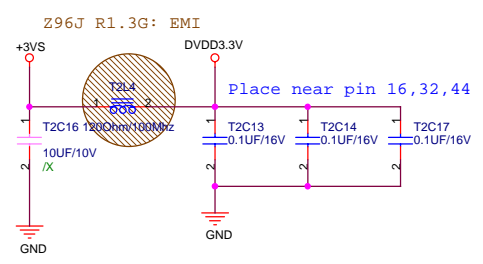
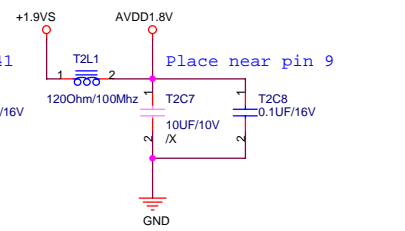
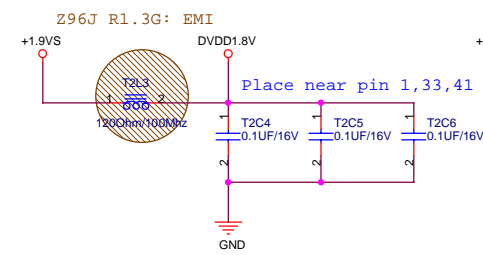
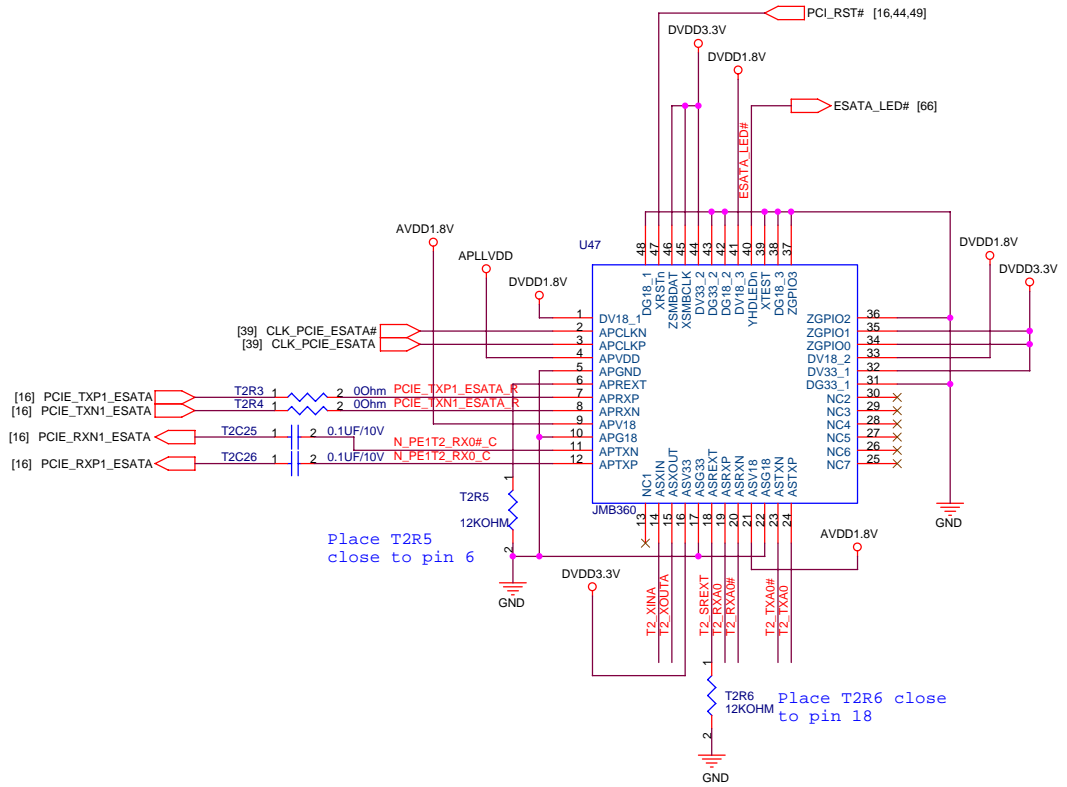
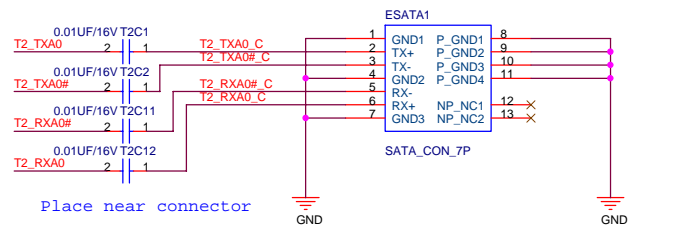
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

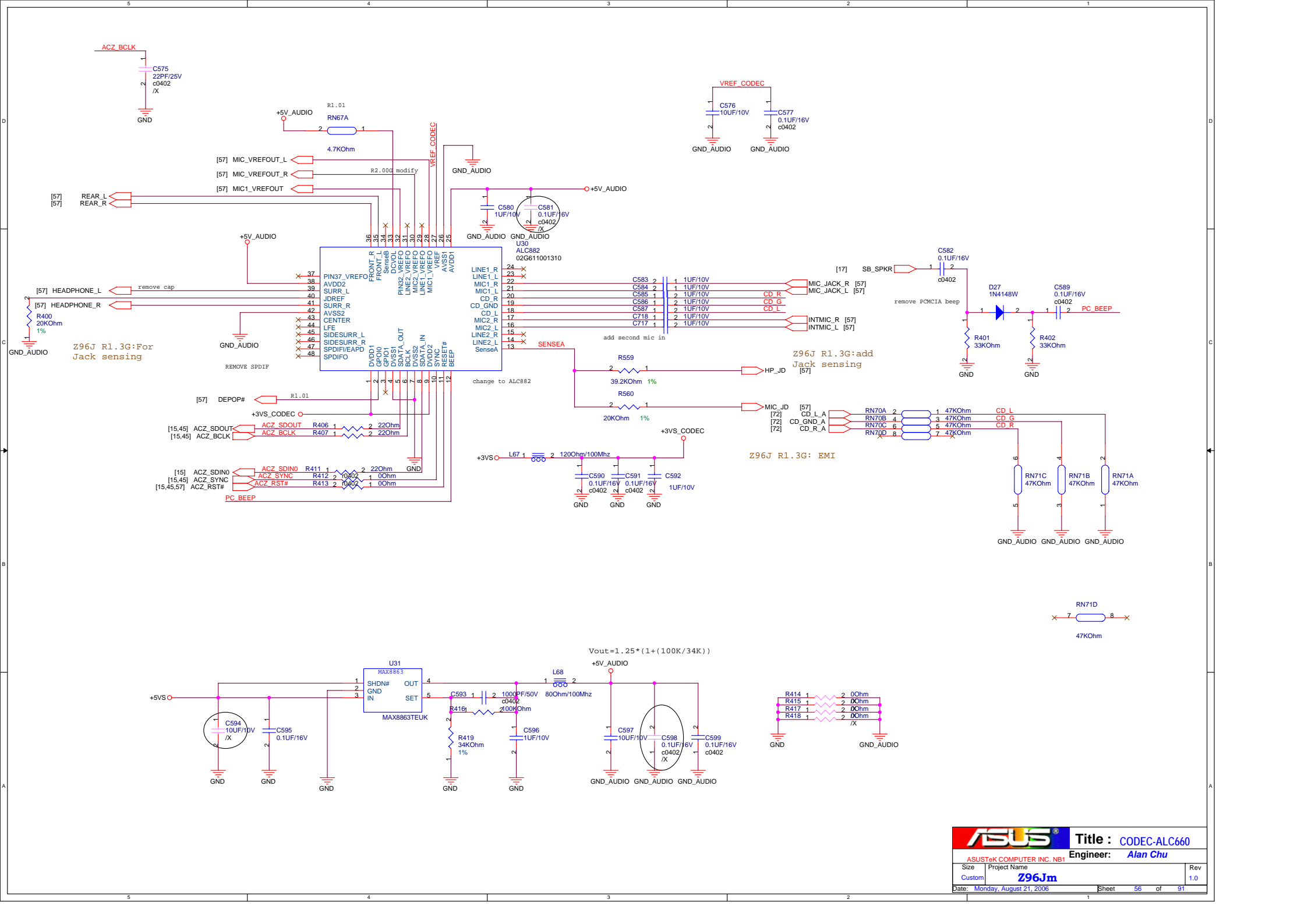


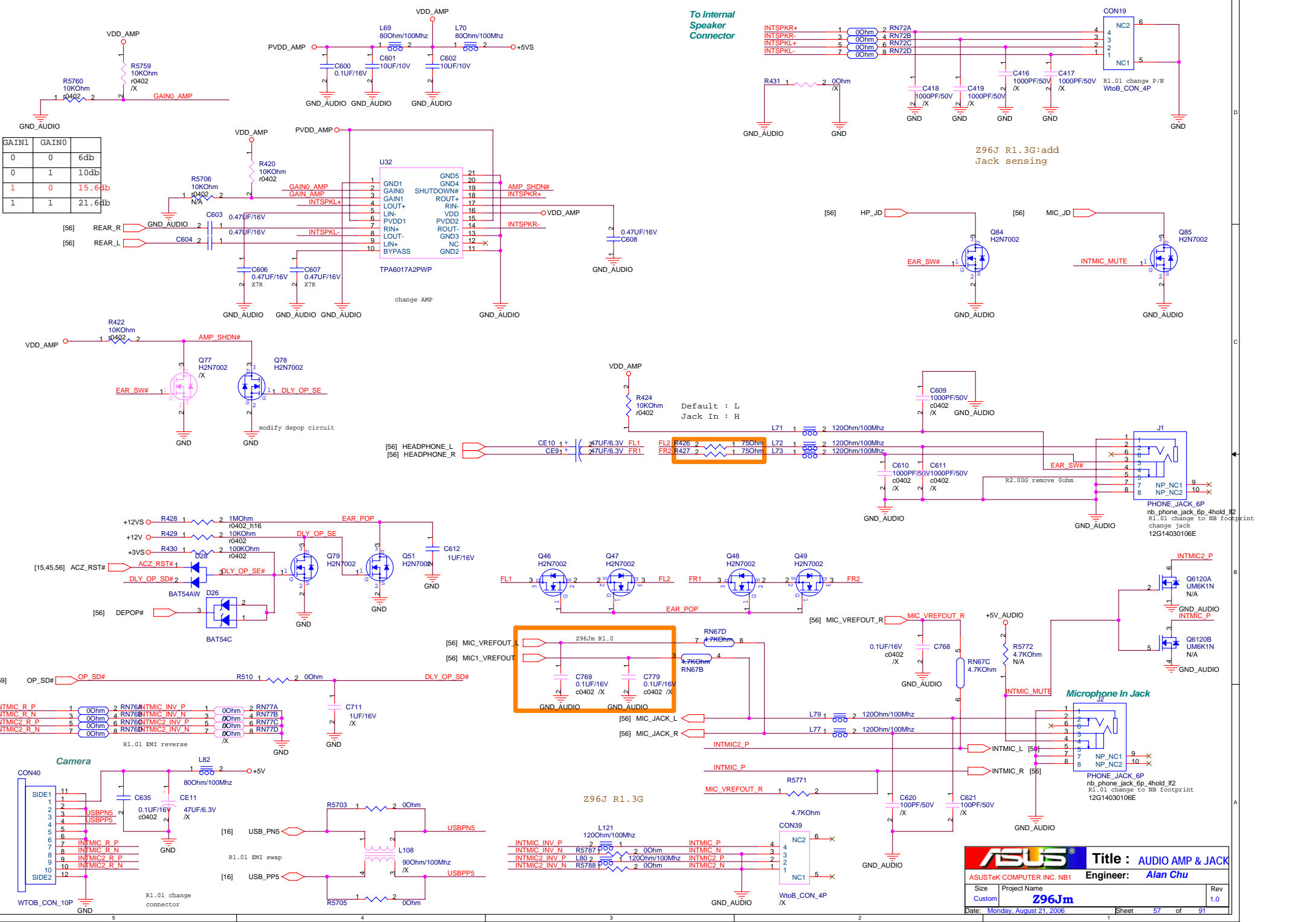
NewCard Header

NewCard Ejector

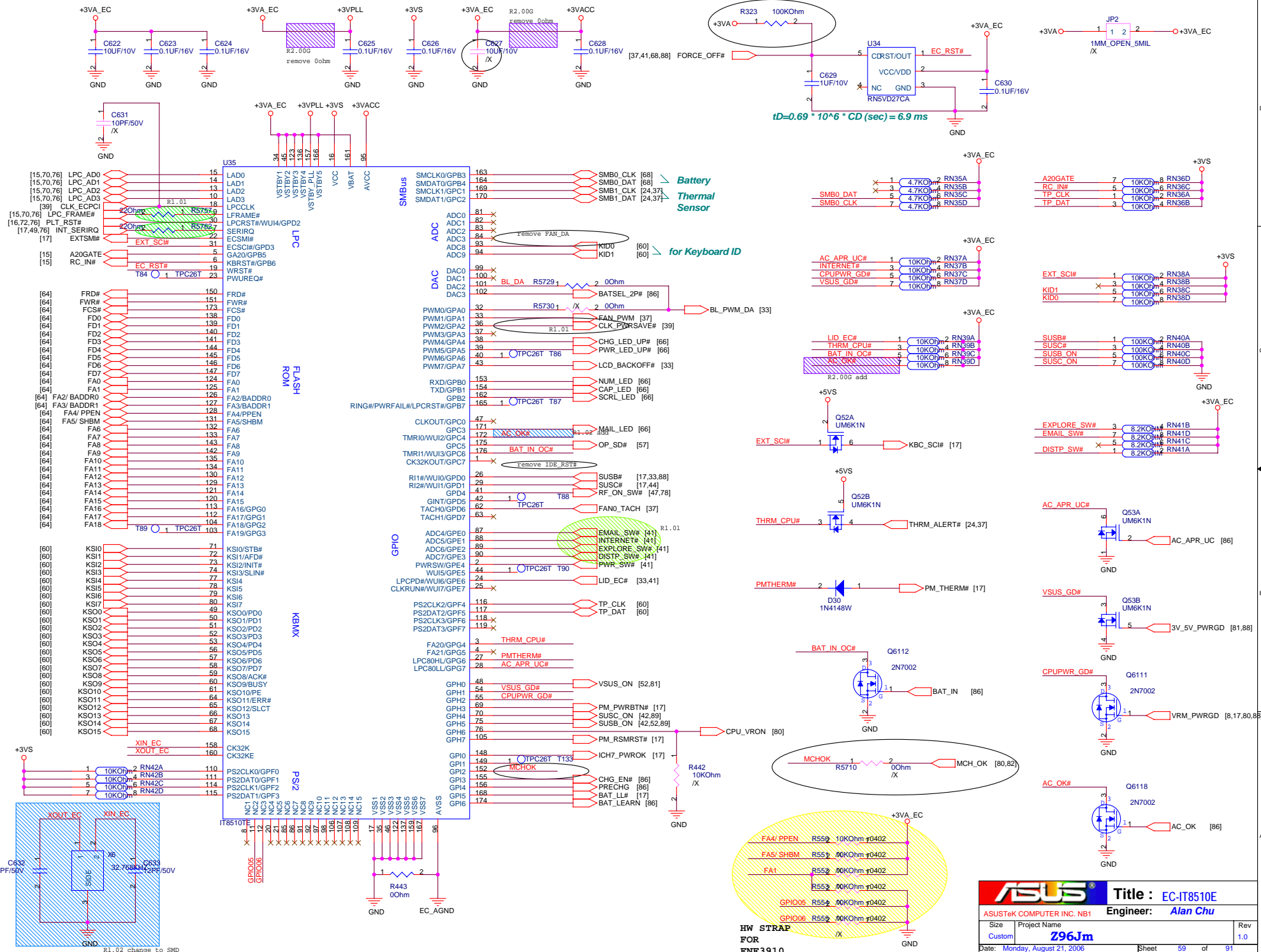








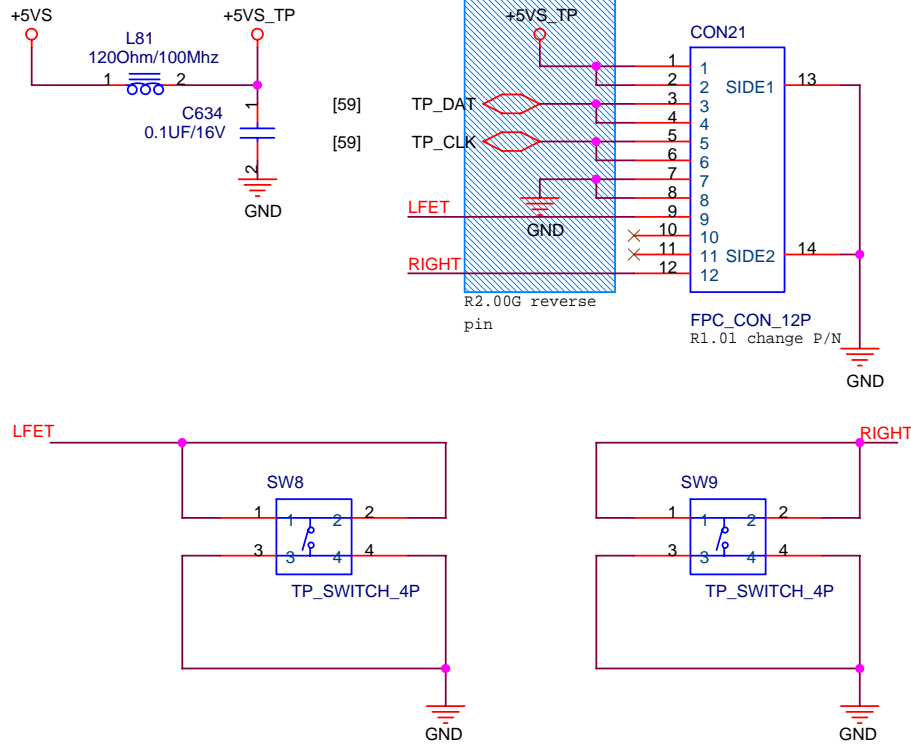
ASUS Title : **AUDIO AMP & JACK**
 ASUSTek COMPUTER INC. N81 Engineer: **Alan Chu**
 Size Project Name
 Custom **Z96Jm** Rev 1.0
 Date: Monday, August 21, 2006 Sheet 57 of 91



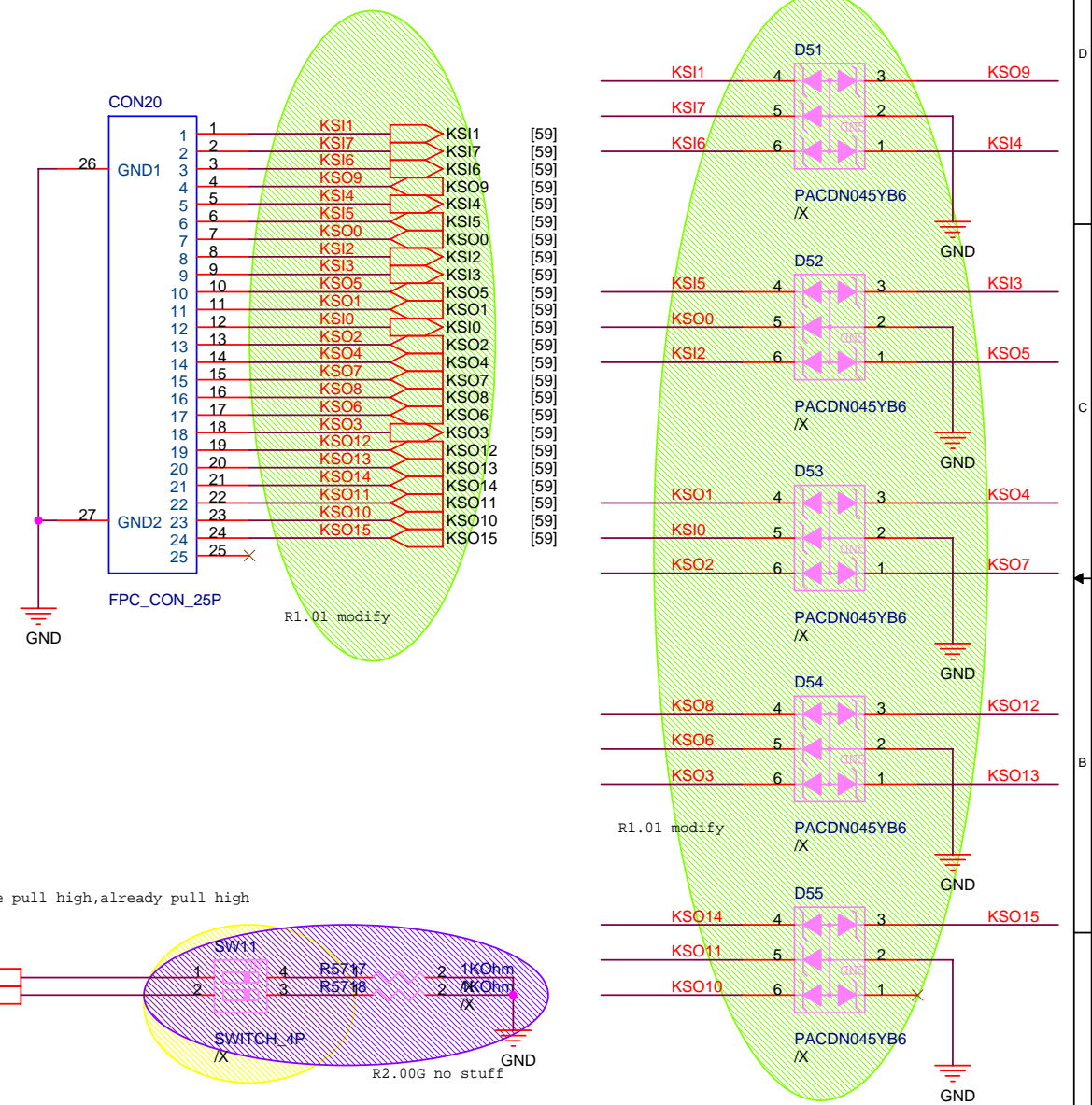
HW STRAP FOR BNR3910

R1.02 change to SMD

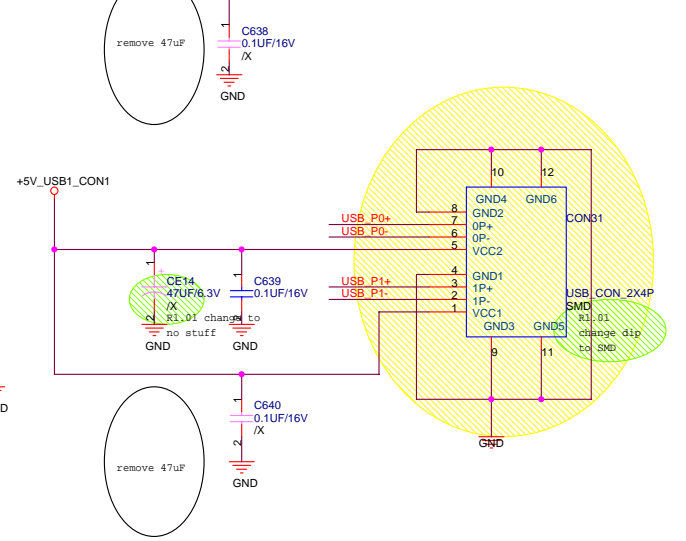
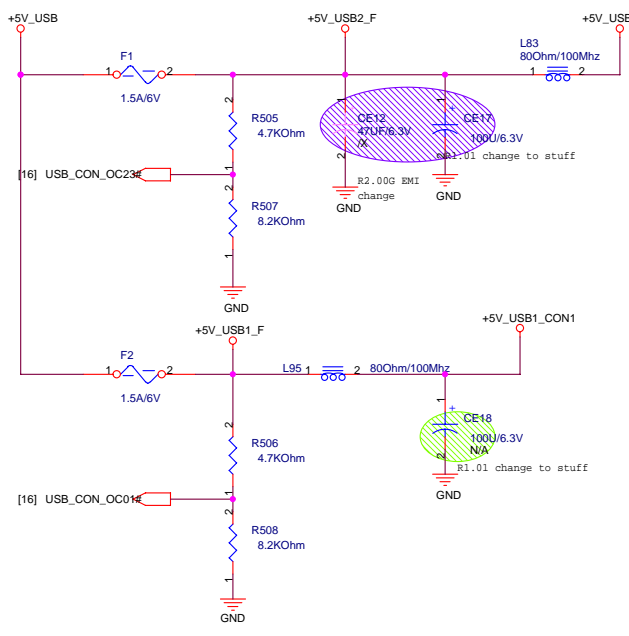
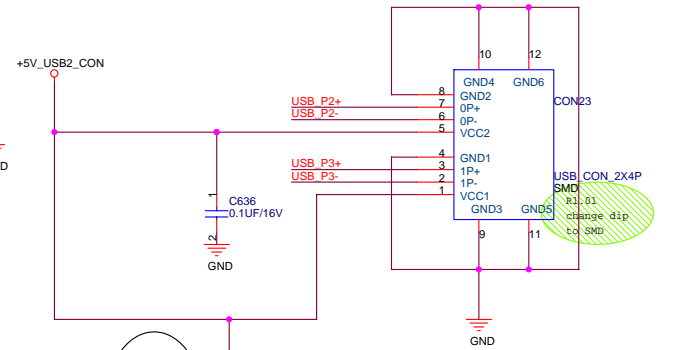
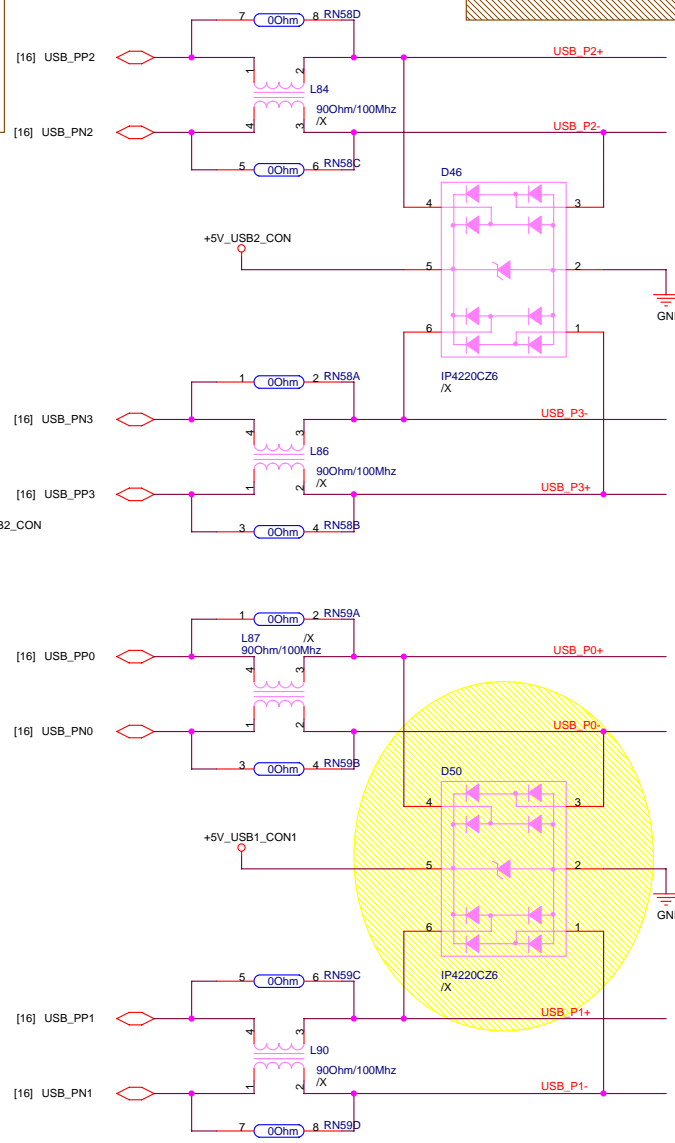
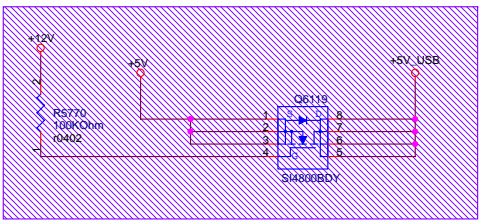
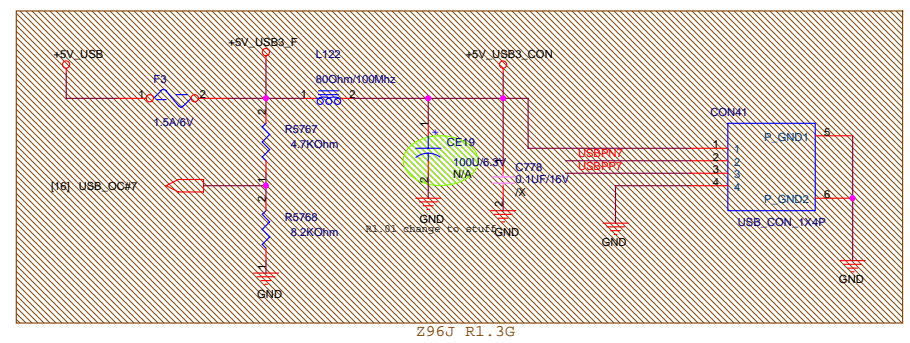
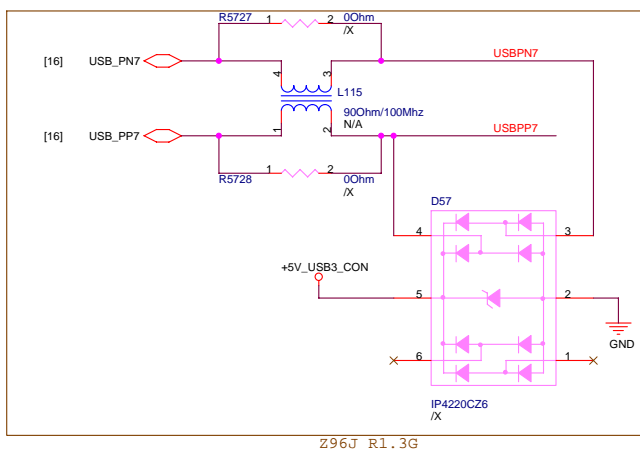
For Touch-Pad



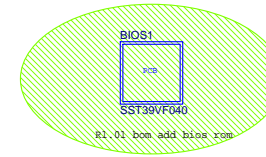
For Keyboard



ASUS		Title : Touch Pad & KB	
ASUSTeK COMPUTER INC. MB6		Engineer: ALAN CHU	
Size A4	Project Name Z96Jm	Rev 1.0	
Date: Monday, August 21, 2006		Sheet 60 of 91	



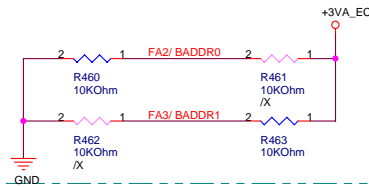
ISA ROM



EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

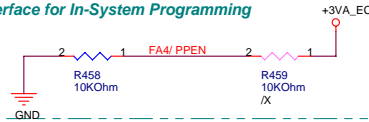
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

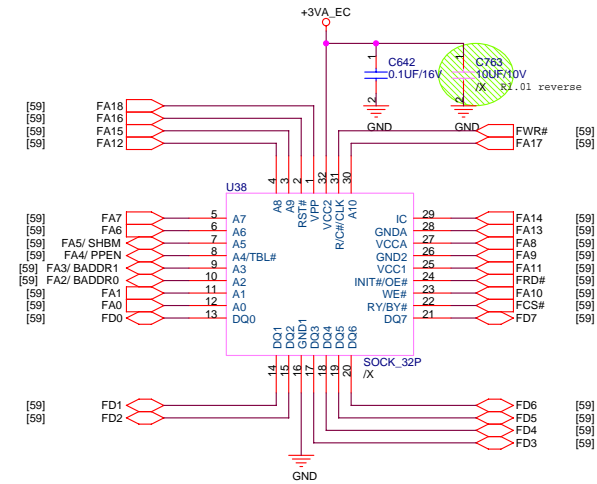
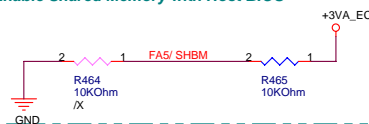
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



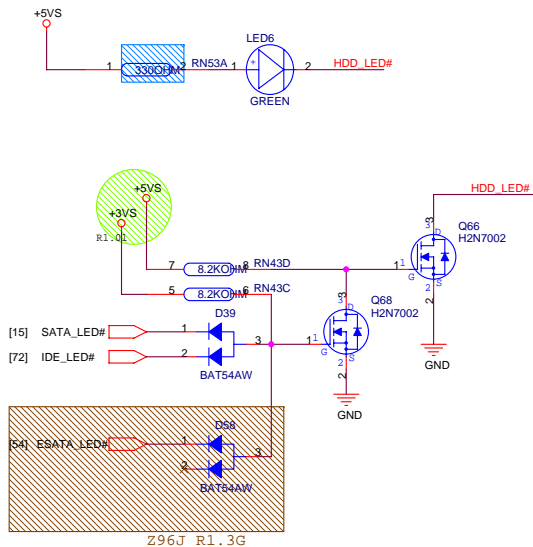
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

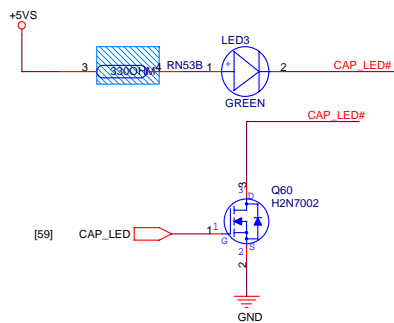


For LED

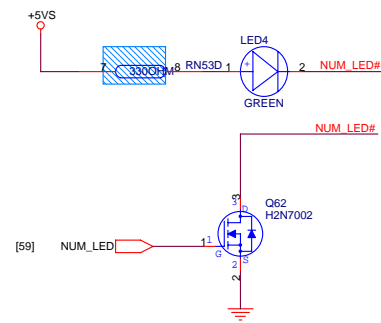
For SATA/IDE LED



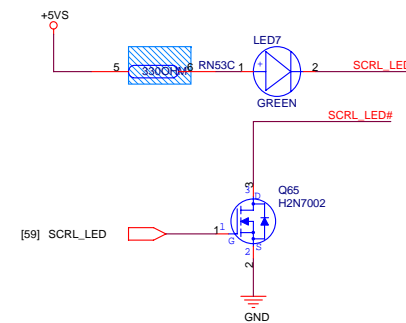
for Cap. Lock



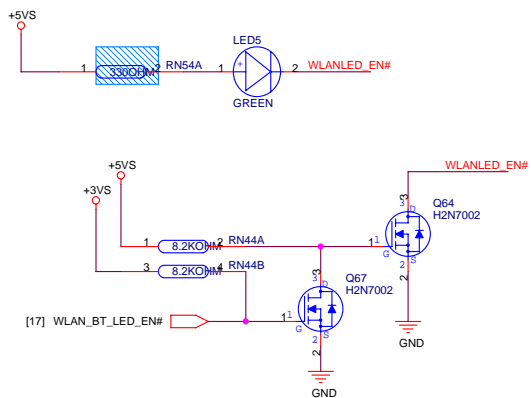
for Num Lock



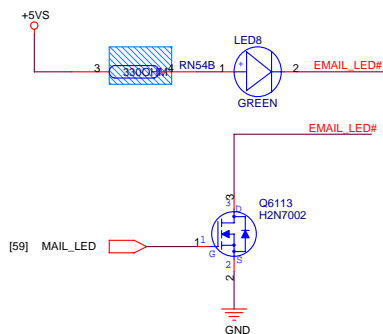
for Scroll Lock



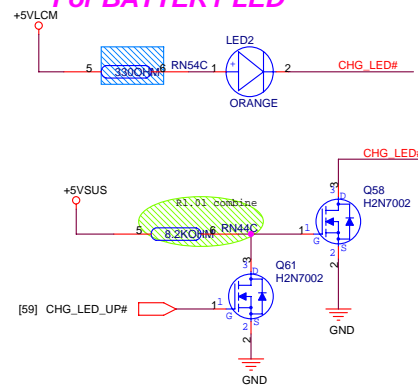
For WireLess LED



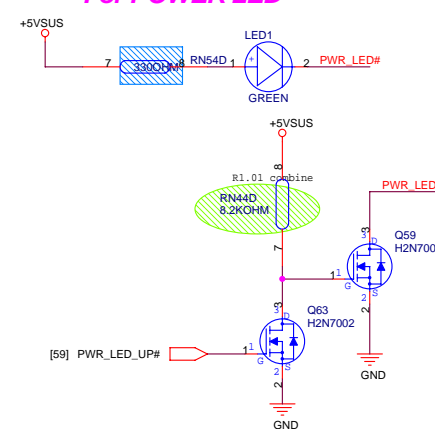
for email



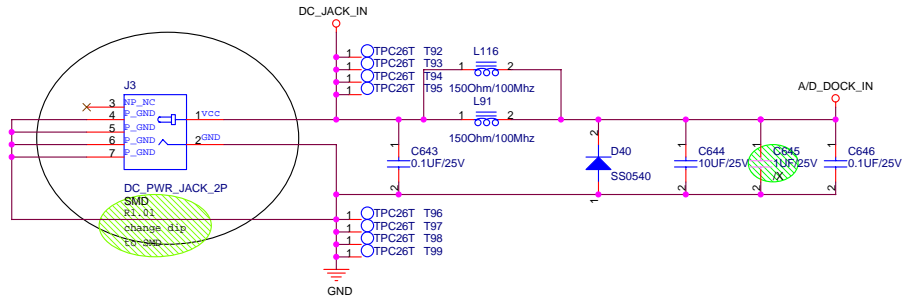
For BATTERY LED



For POWER LED

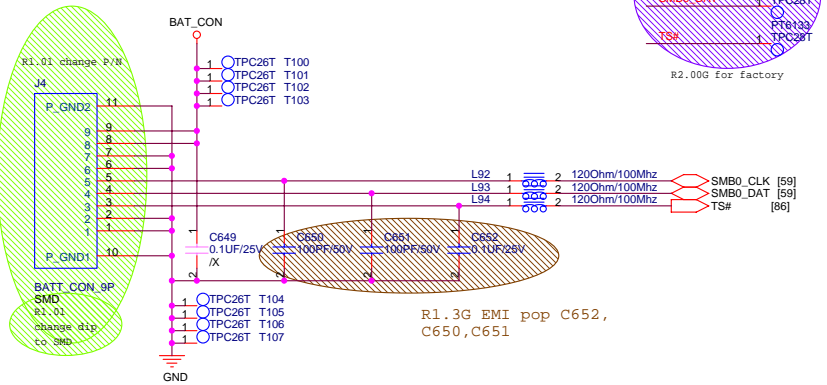


DC IN

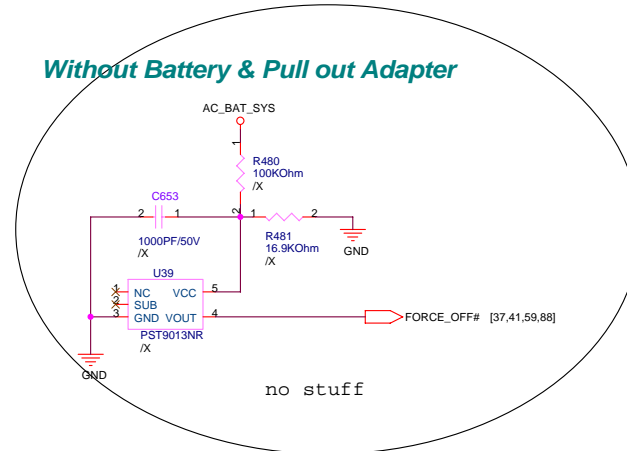


remove AC DC detect; no need

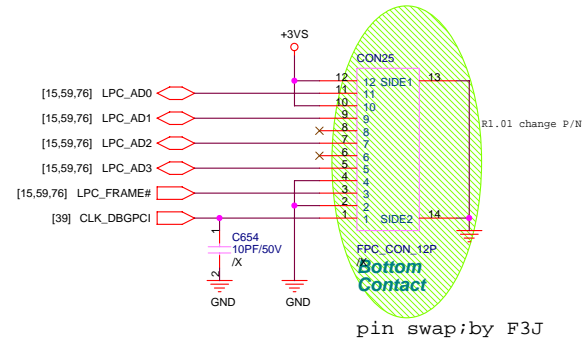
BAT IN



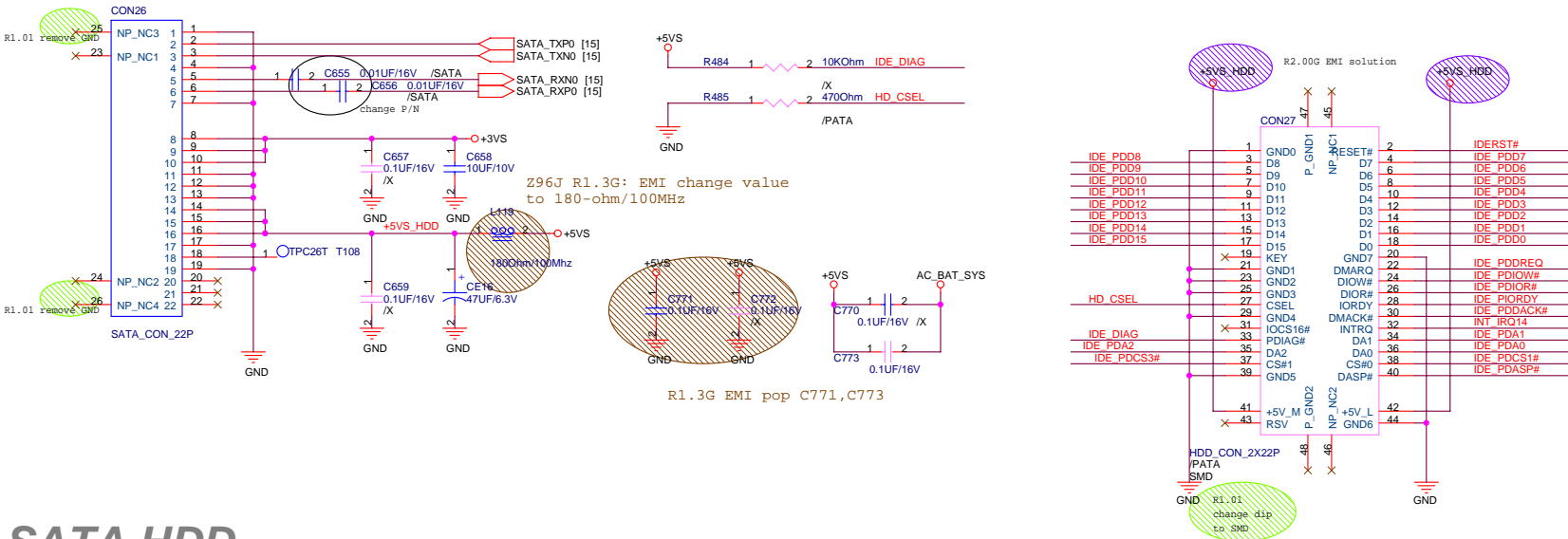
Without Battery & Pull out Adapter



For Debug

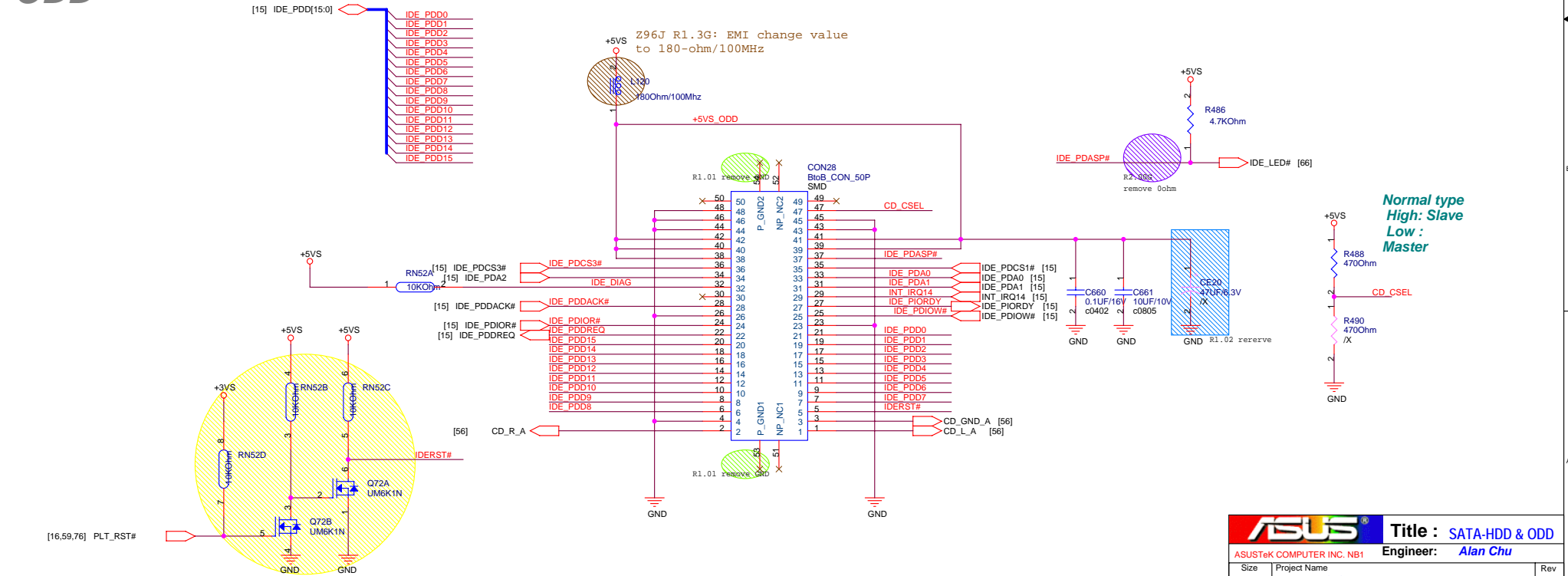


HD_CSEL : Pull-Down, HDD as Master

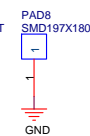
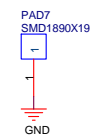
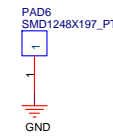
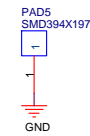
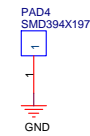
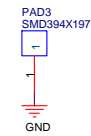
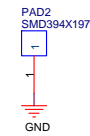
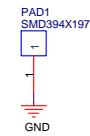
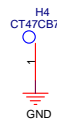
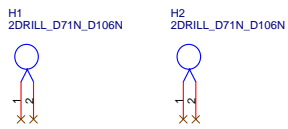


SATA HDD

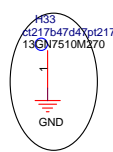
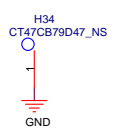
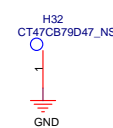
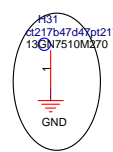
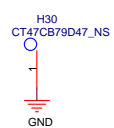
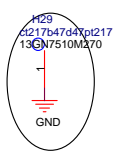
ODD



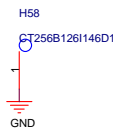
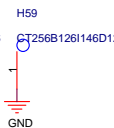
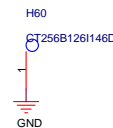
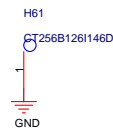
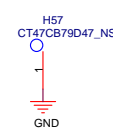
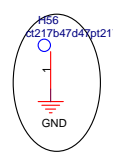
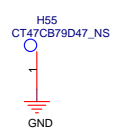
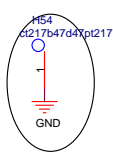
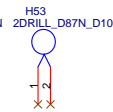
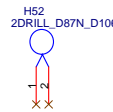
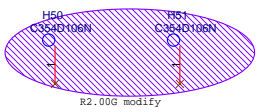
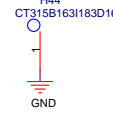
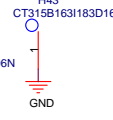
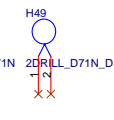
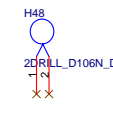
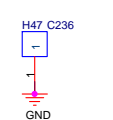
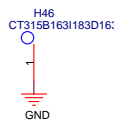
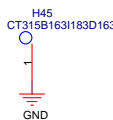
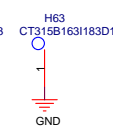
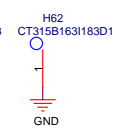
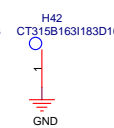
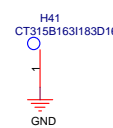
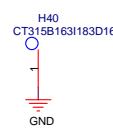
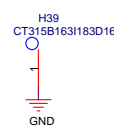
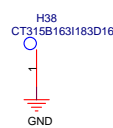
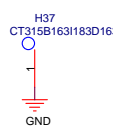
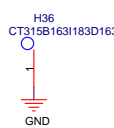
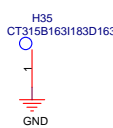
Normal type
High : Slave
Low : Master



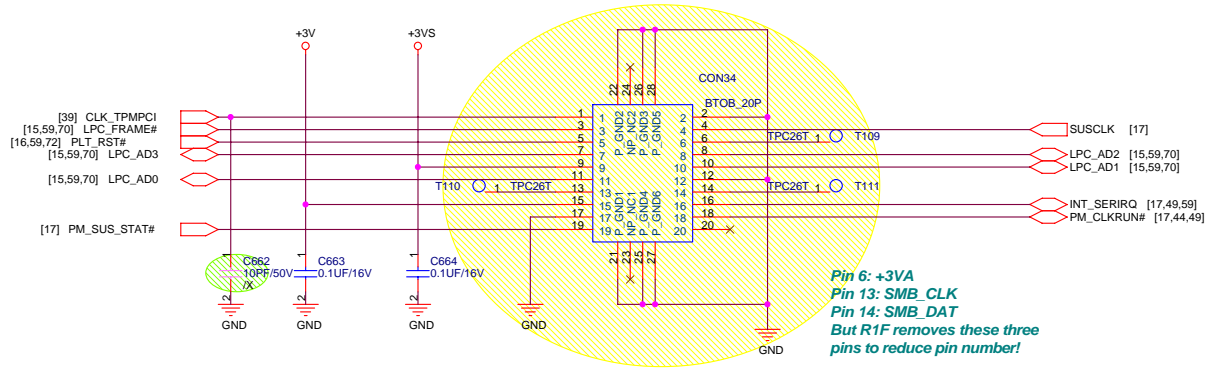
FOR SCREW HOLE



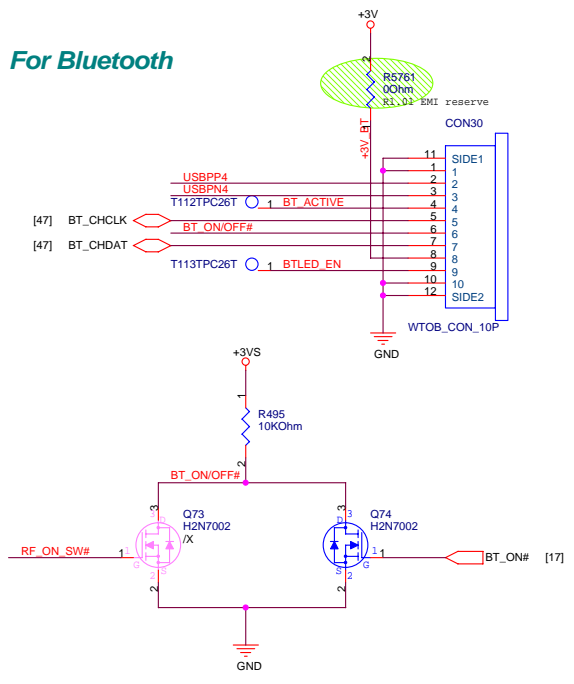
FOR SCREW HOLE



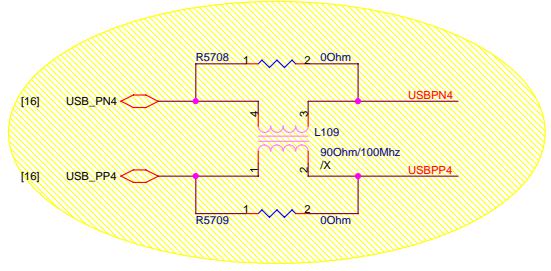
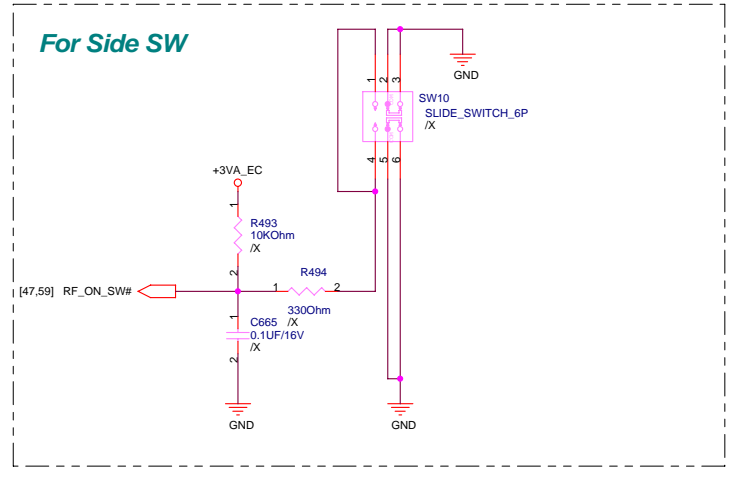
For TPM Module

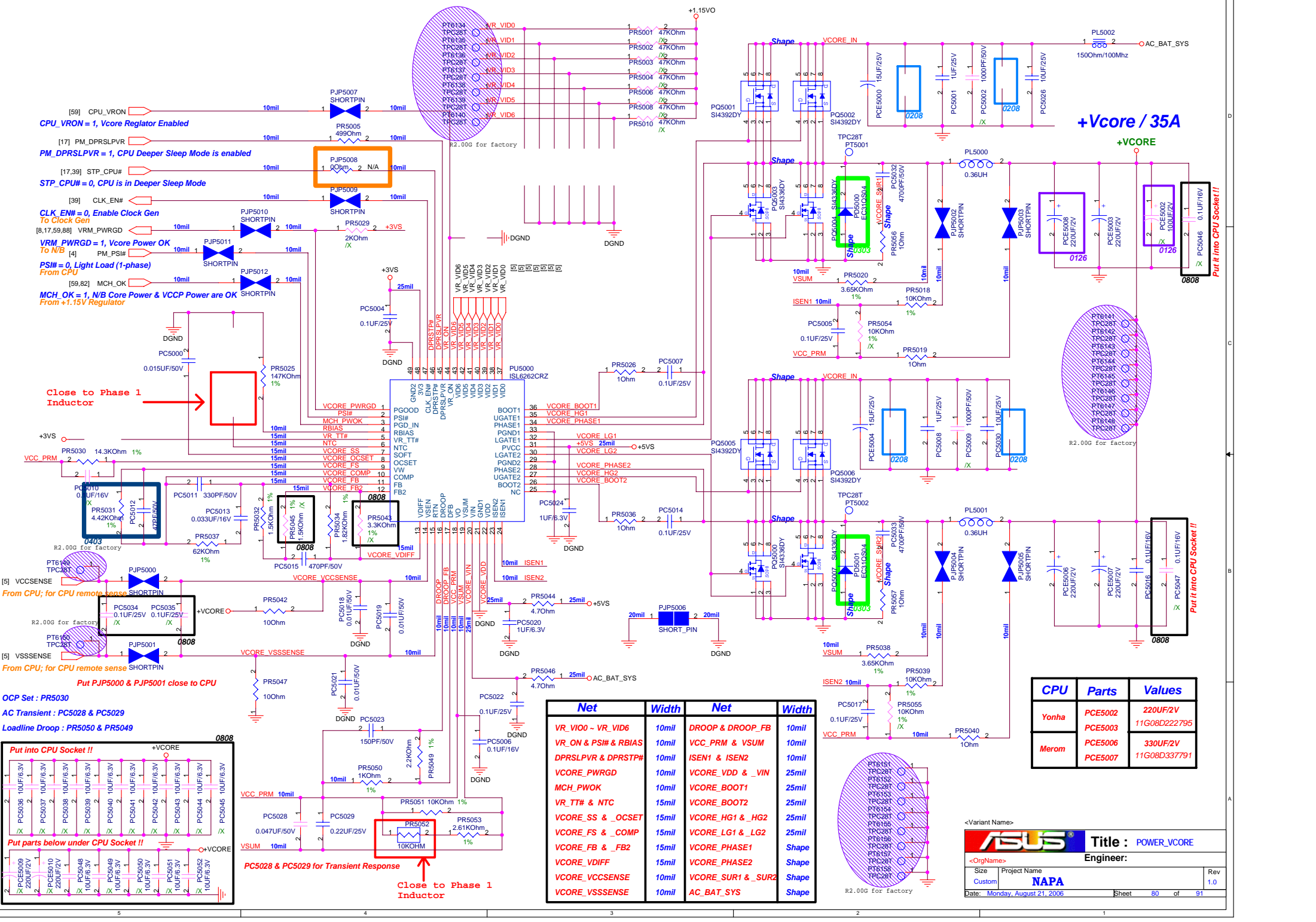


For Bluetooth



For Side SW



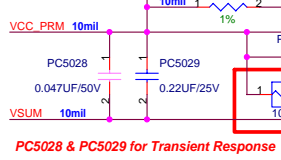
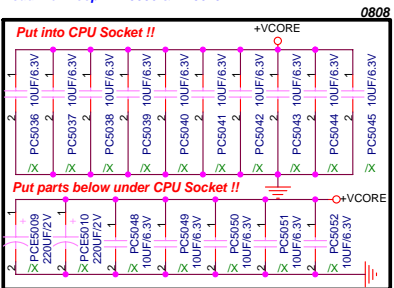


[59] CPU_VRON = 1, Vcore Regulator Enabled
 CPU_VRON = 1, Vcore Regulator Enabled
 [17] PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
 PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
 [17,39] STP_CPU# = 0, CPU is in Deeper Sleep Mode
 STP_CPU# = 0, CPU is in Deeper Sleep Mode
 [39] CLK_EN# = 0, Enable Clock Gen
 To Clock Gen
 [8,17,59,88] VRM_PWRGD = 1, Vcore Power OK
 To N/B
 [4] PM_PSI# = 0, Light Load (1-phase)
 From CPU
 [59,82] MCH_OK = 1, N/B Core Power & VCCP Power are OK
 From +1.15V Regulator

Close to Phase 1 Inductor

From CPU; for CPU remote sense
 From CPU; for CPU remote sense
 Put PJP5000 & PJP5001 close to CPU

OCP Set : PR5030
 AC Transient : PC5028 & PC5029
 Loadline Droop : PR5050 & PR5049



Net	Width	Net	Width
VR_VIO0 - VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
Vcore_PWRGD	10mil	Vcore_VDD & _VIN	25mil
MCH_PWOK	10mil	Vcore_BOOT1	25mil
VR_TT# & NTC	15mil	Vcore_BOOT2	25mil
Vcore_SS & _OCSET	15mil	Vcore_HG1 & _HG2	25mil
Vcore_FS & _COMP	15mil	Vcore_LG1 & LG2	25mil
Vcore_FB & _FB2	15mil	Vcore_PHASE1	Shape
Vcore_VDIFF	15mil	Vcore_PHASE2	Shape
Vcore_VCSSENSE	10mil	Vcore_SUR1 & _SUR2	Shape
Vcore_VSSSENSE	10mil	AC_BAT_SYS	Shape

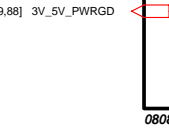
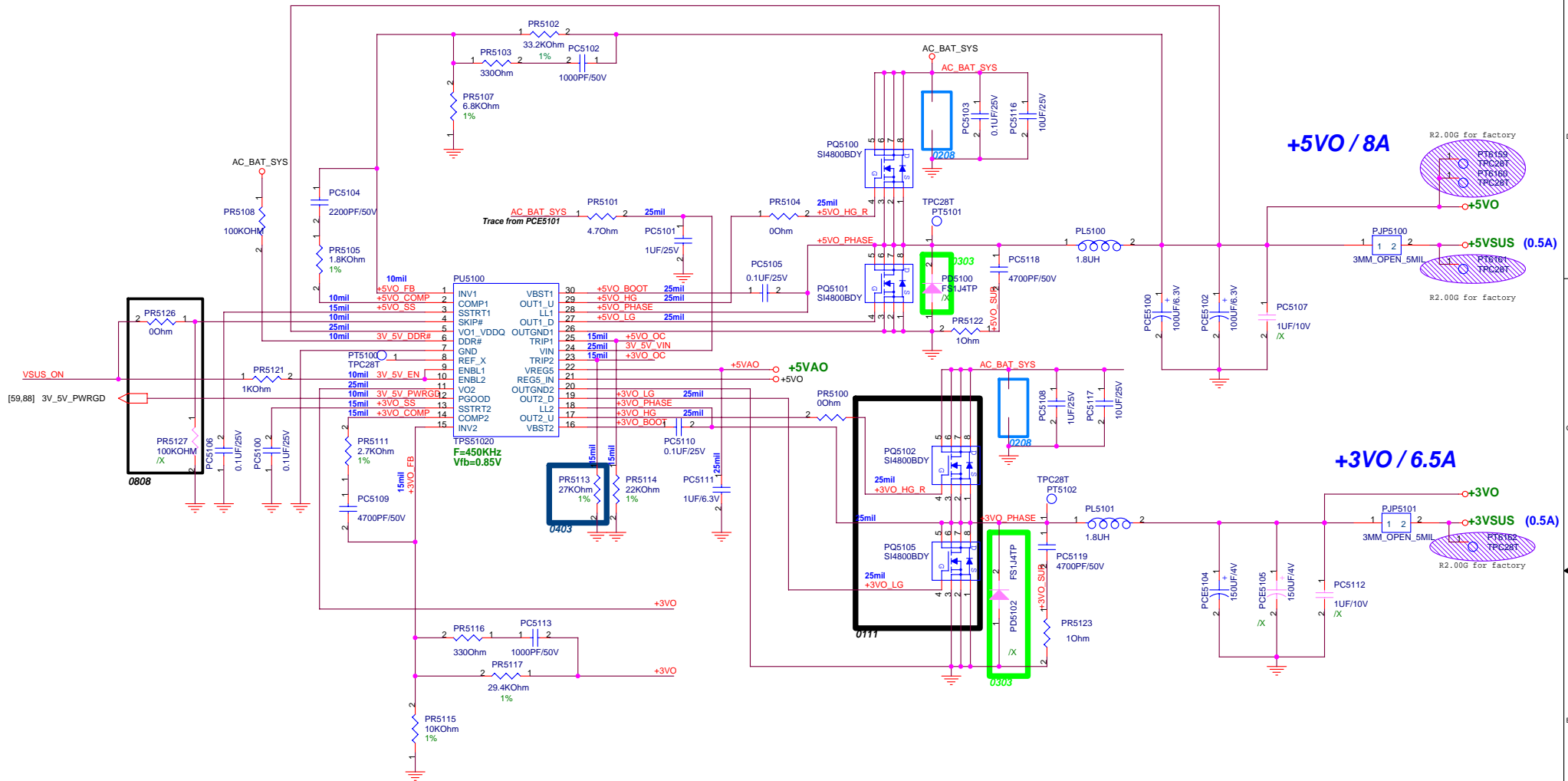
CPU	Parts	Values
Yonha	PCE5002	220UF/2V
Yonha	PCE5003	11G08D222795
Merom	PCE5006	330UF/2V
Merom	PCE5007	11G08D337791

<Variant Name>

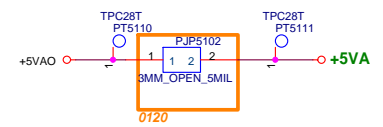
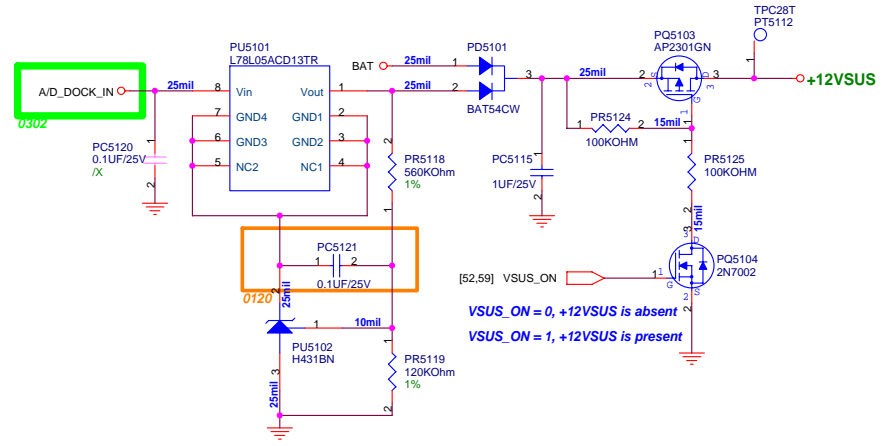
ASUS Title : POWER_VCORE

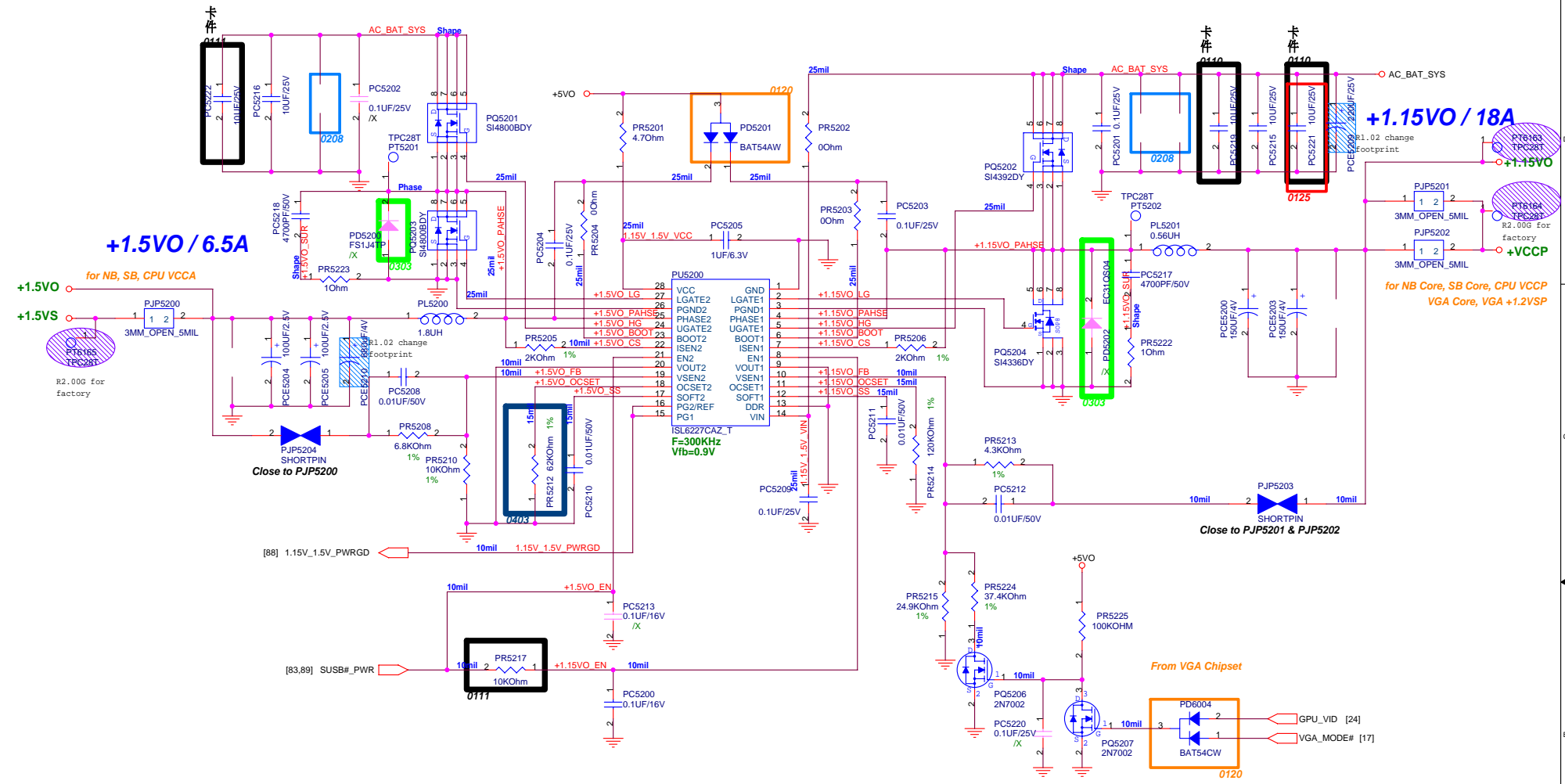
<OrgName> Engineer:

Size Project Name
 Custom NAPA
 Date: Monday, August 21, 2006 Sheet 80 of 91



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_PHASE	Shape
+5VO_HG_R	25mil	+3VO_SUR	Shape
+5VO_LG	25mil	+3VO_OC	15mil
+5VO_PHASE	Shape	+12VSUS_ADJ	10mil
+5VO_SUR	Shape	+5VDRV	25mil





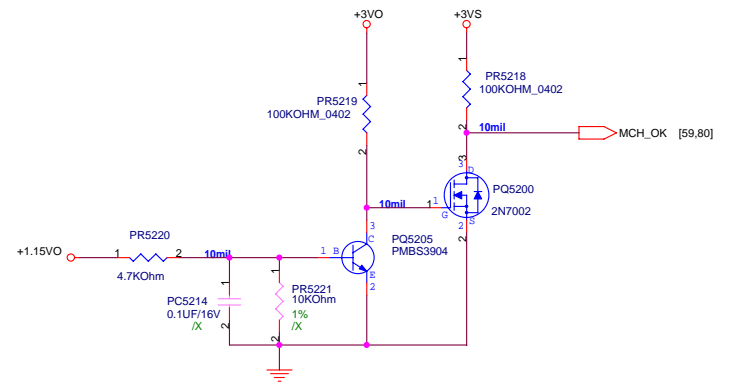
+1.5VO / 6.5A
for NB, SB, CPU VCCA

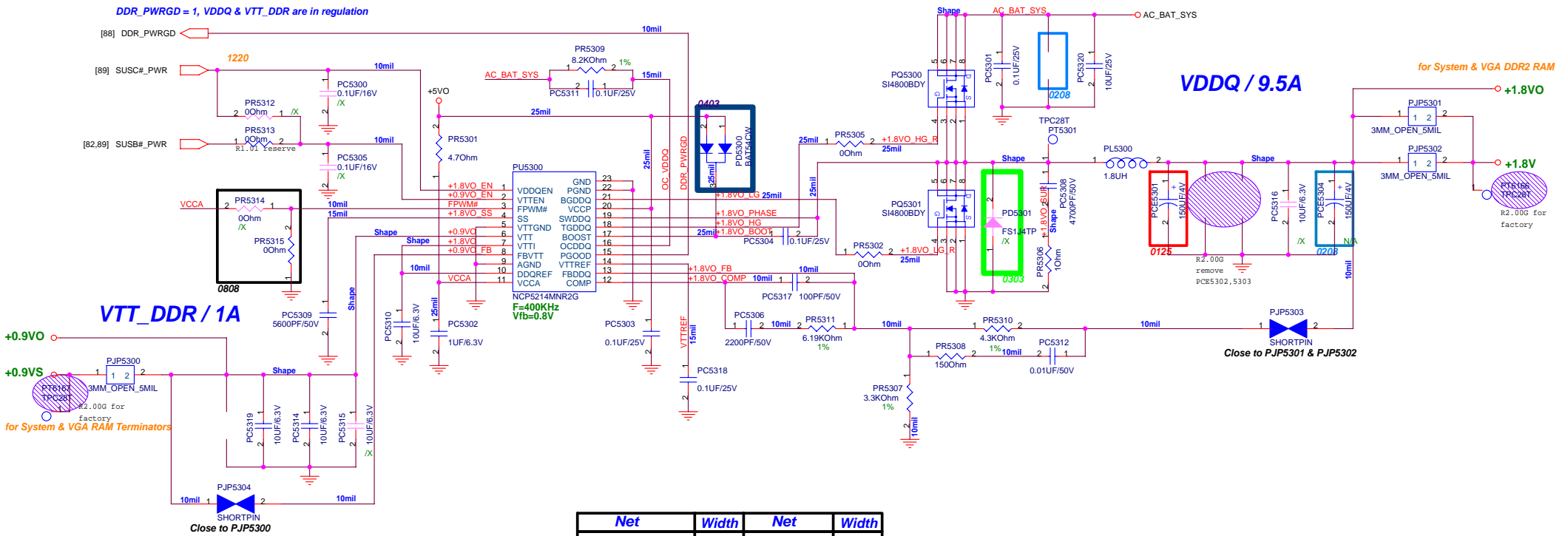
+1.15VO / 18A

for NB Core, SB Core, CPU VCCP
VGA Core, VGA +1.2VSP

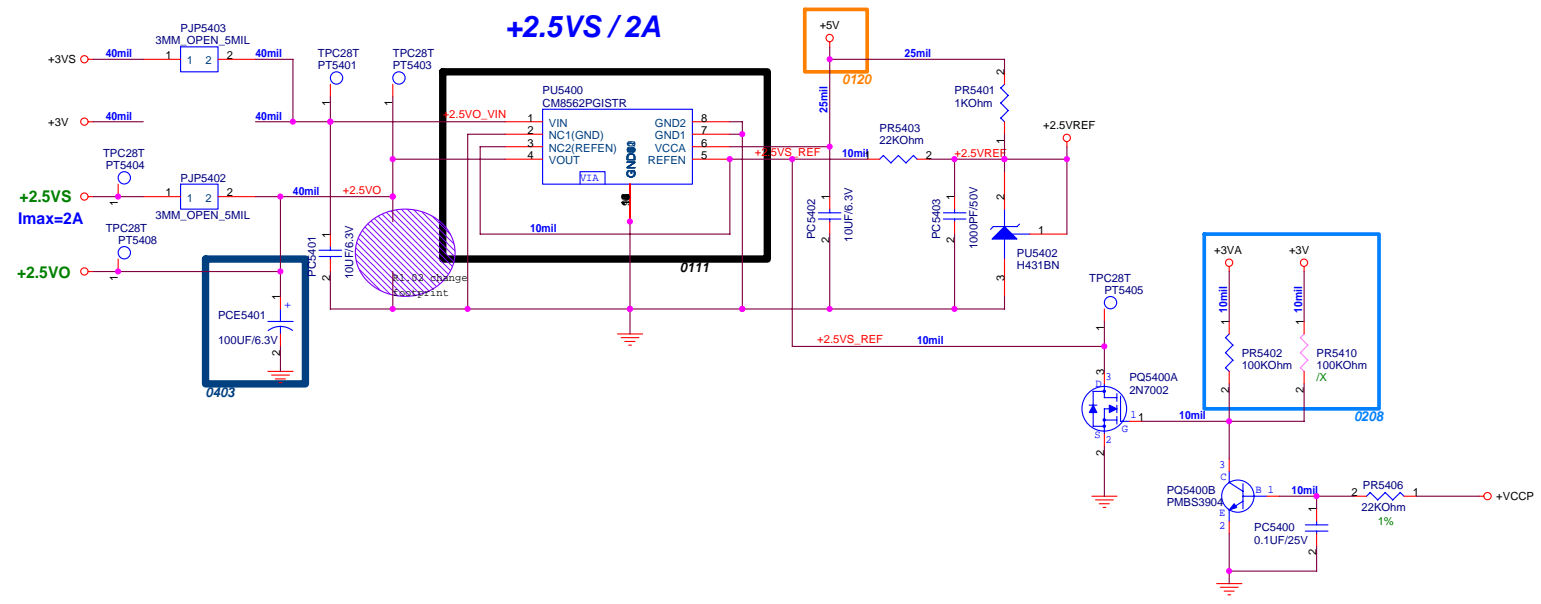
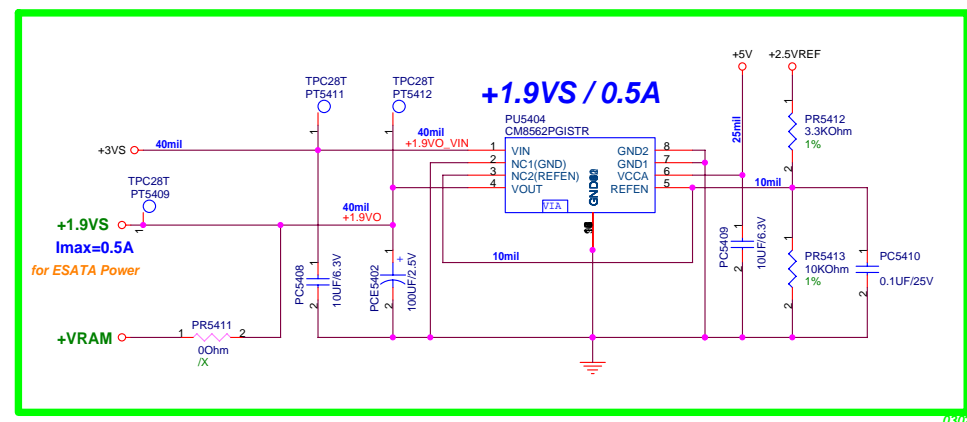
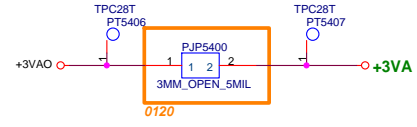
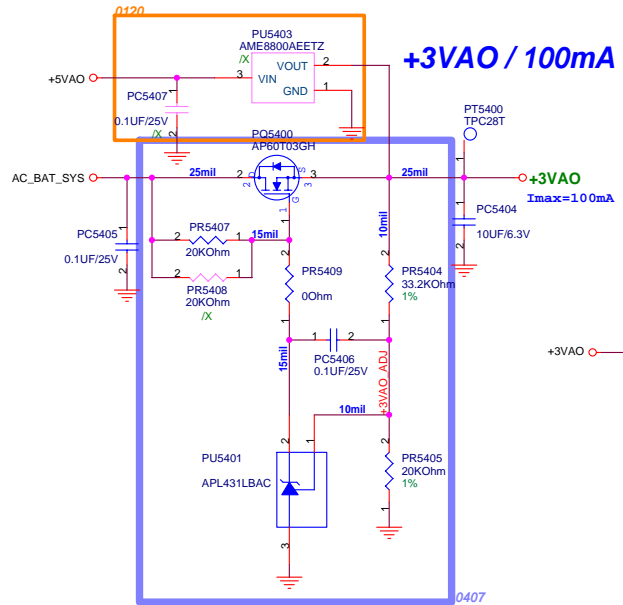
From VGA Chipset
GPU_VID = 1; Battery Mode ; +1.15VO = 1.055V
GPU_VID = 0; Performance Mode ; +1.15VO = 1.158V

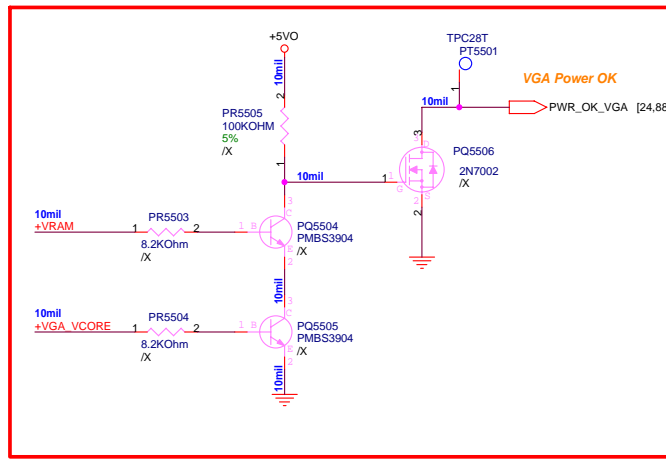
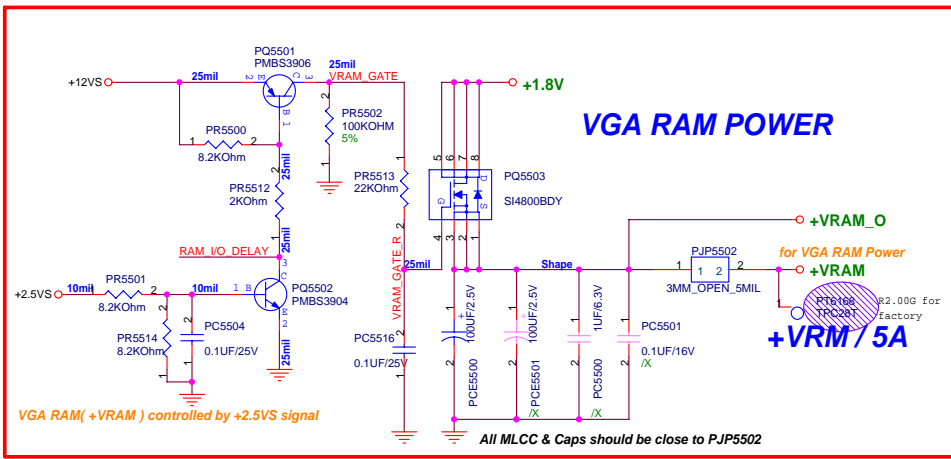
Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape



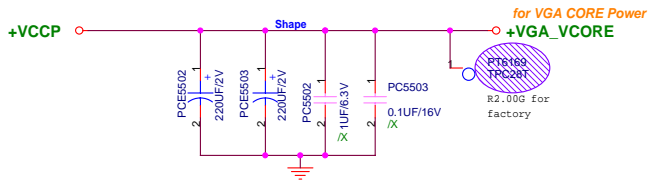


Net	Width	Net	Width
+1.8V_EN	10mil	+1.8V_BOOT	25mil
+1.8V_O	Shape	+1.8V_COMP	10mil
+0.9V_EN	10mil	+1.8V_HG_R	25mil
+0.9V_O	Shape	+1.8V_LG_R	25mil
+0.9V_FB	10mil	+1.8V_HG	25mil
+1.8V -> DDQREF	10mil	+1.8V_LG	25mil
VTTREF	15mil	+1.8V_PHASE	Shape
FPWM#	10mil	+1.8V_SUR	Shape
VCCA	10mil	+1.8V_FB	10mil
DDR_PWRGD	10mil	+1.8V_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

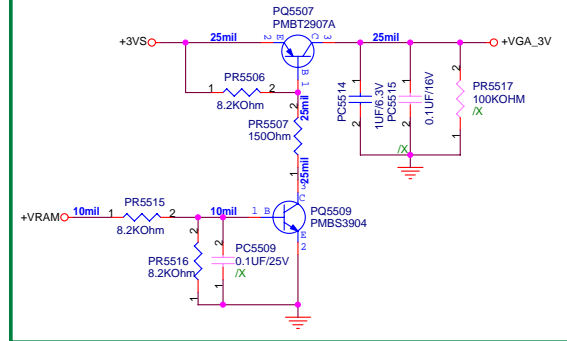




VGA CORE POWER



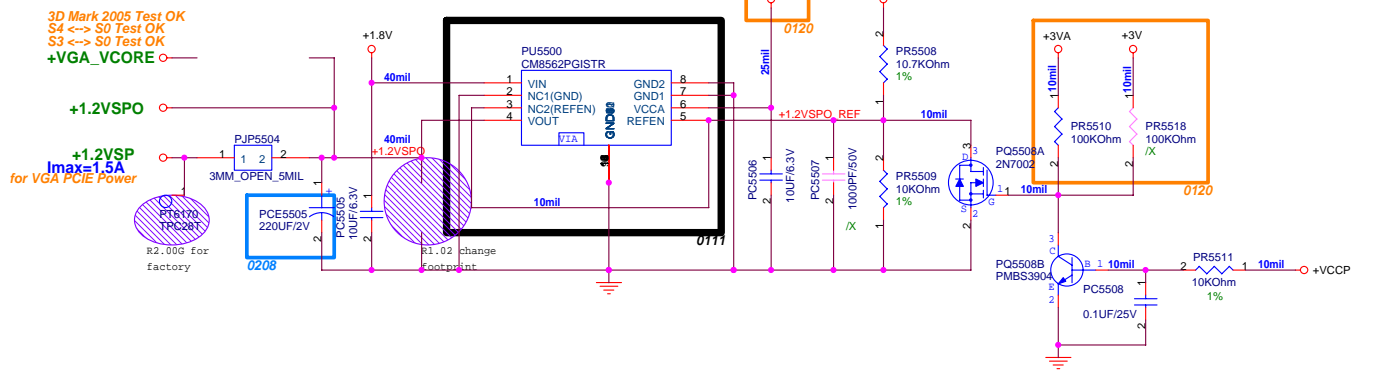
VGA I/O POWER



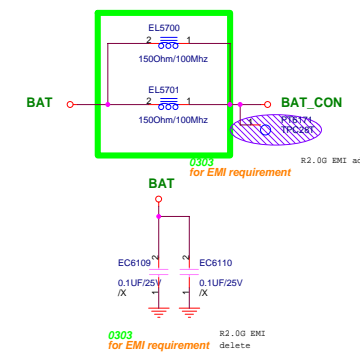
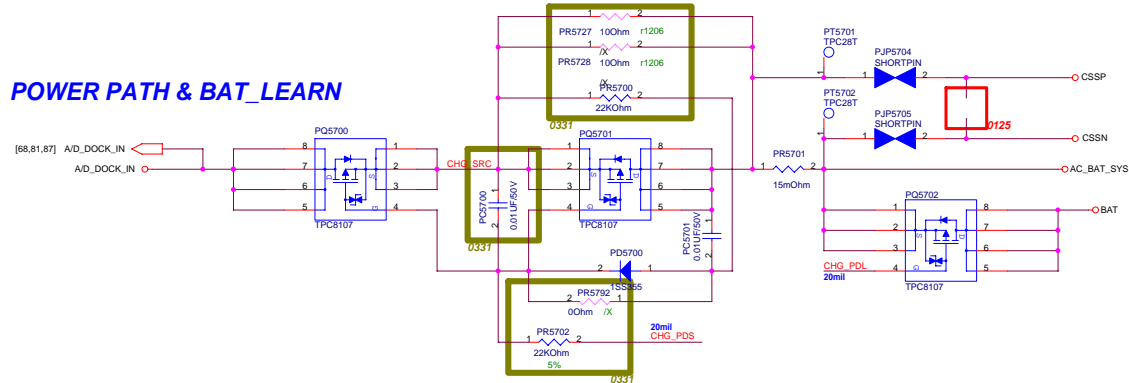
VGA PCI-E POWER

3D Mark 2005 Test OK
S4 ↔ S0 Test OK
S3 ↔ S0 Test OK
+VGA_VCORE

+1.2VSPO / 1.5A



POWER PATH & BAT_LEARN



Charger shut down condition :

1. $V_{ictl} < 0.06V$
2. $PKPRES\# > 55\%$ of $MAX8725_LDO$
3. AC Adaptor Removed

The timing of PDL & PDS switch :

BAT - A/D_DOCK_IN > 100mV-> Battery mode

The current capacity of MAX8725_LDO is 10mA.

VBAT_DLGV is a voltage for driving MOSFET.

$MAX8725_ACIN < 10.27V$, AC Adaptor absent
 $MAX8725_ACIN > 10.27V$, AC Adaptor absent

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<V _{mode} <2V)	Battery Learn

$MAX8725_REF : 4.2235V$
 $MAX8725_LDO : 5.4V$

Battery Charging Voltage :
 $+V_BAT = 3 \times [4.2235 + (V_{ictl} - 1.8) / 9.52]$

Battery Charging Current :
 $I_{charge} = (0.075 / PR5706) \times (V_{ictl} / 3.6)$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (0.075 / PR5701) \times (V_{cls} / 4.2235)$

Pre-Charging Mode :

Precharging current = 150 - 160mA
 $V_{ictl} = 0.100V - 0.120V$

Battery Cell Selection :

$BATSEL_2P\# = 1, 3$ Cells; $V_{ictl} = 2.084V$, $CHG_EN\# = 0$, Charger Enabled
 $\Rightarrow I_{charge} = 2.894A$

$BATSEL_2P\# = 0, 6$ or 9 Cells; $V_{ictl} = 3.219V$, $AC_OK = 1$, Adaptor is present
 $\Rightarrow I_{charge} = 4.472A$

Adaptor Max. Current :

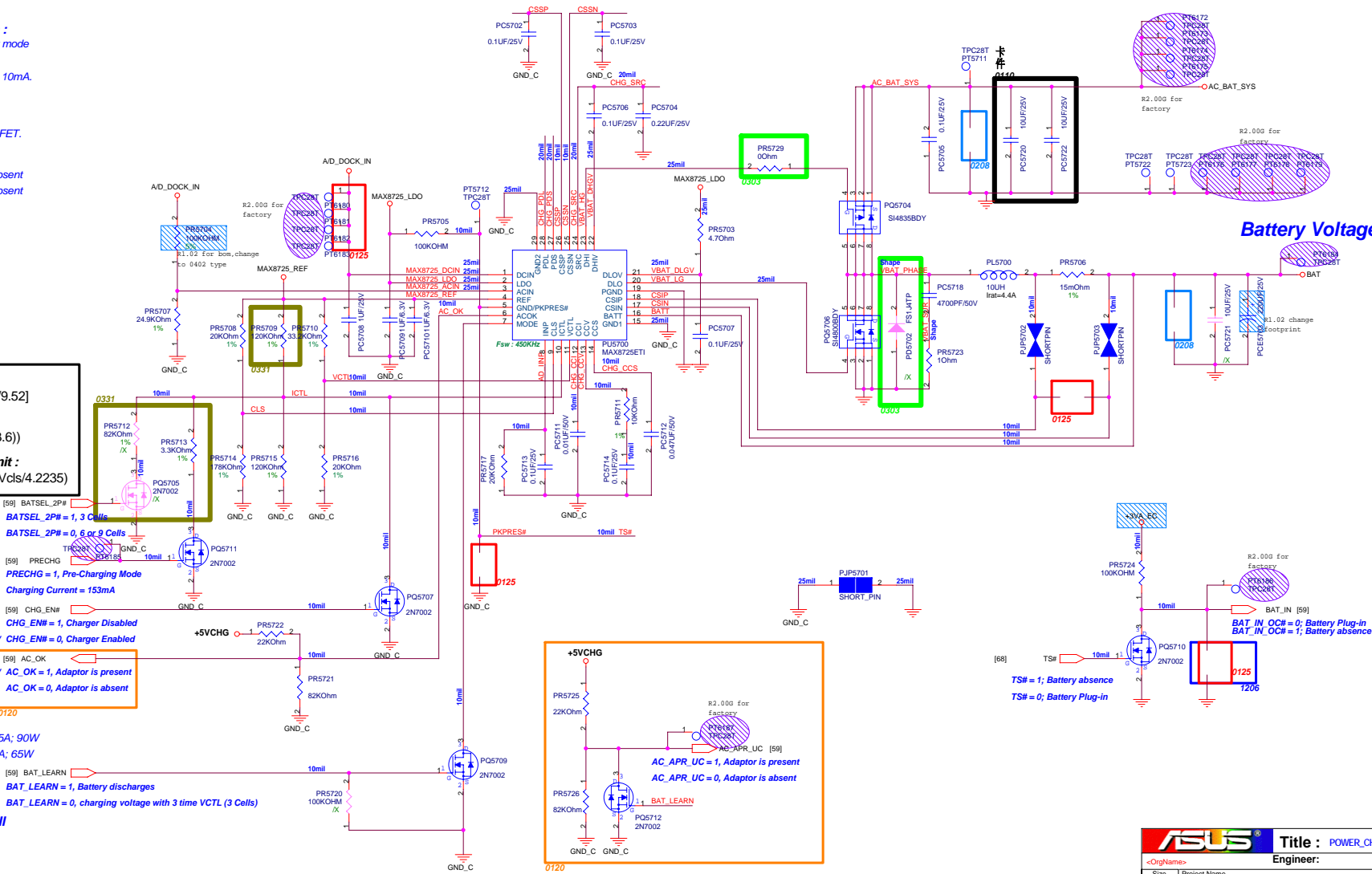
$PR5714 = 178K$; $V_{cls} = 3.79V$, $I_{limit} = 4.5A$; 90W
 $PR5714 = 47K$; $V_{cls} = 2.96V$, $I_{limit} = 3.5A$; 65W

BATSEL_SP# = 1, 3-Cell

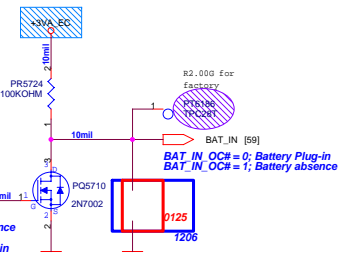
$V_{ictl} = 1.22V$ / $I_{charge} = 1.69A$

BATSEL_SP# = 0, 6-Cell or 9-Cell

$V_{ictl} = 2.11V$ / $I_{charge} = 2.93A$

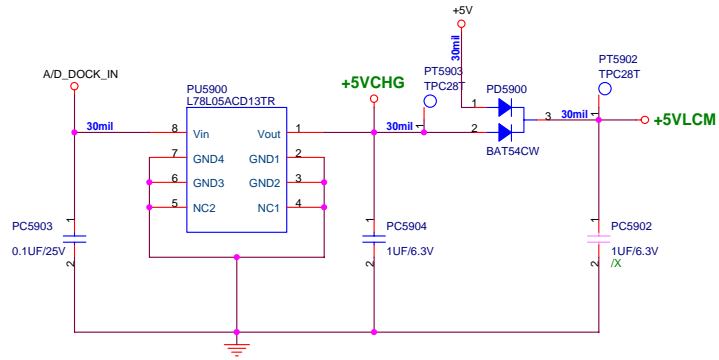


Battery Voltage

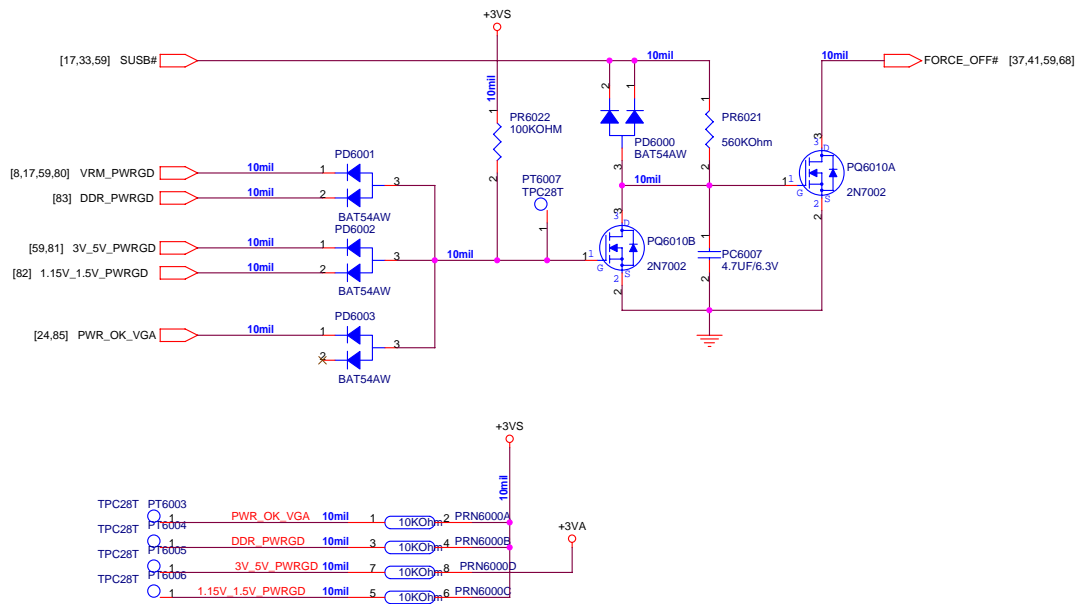


REMOVE BATTERY IN DETECT

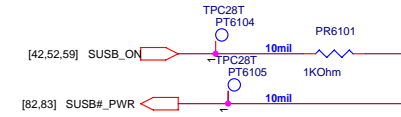
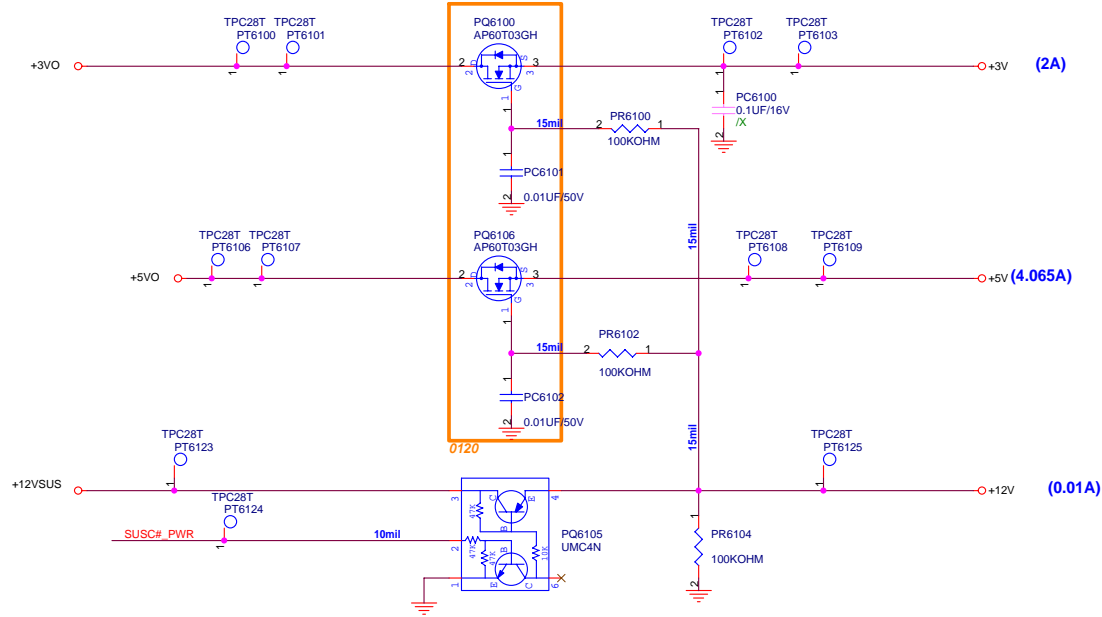
+5VLCM / +5VCHG



Power Good Detector



SUSC#_PWR POWER



SUSB#_PWR POWER

