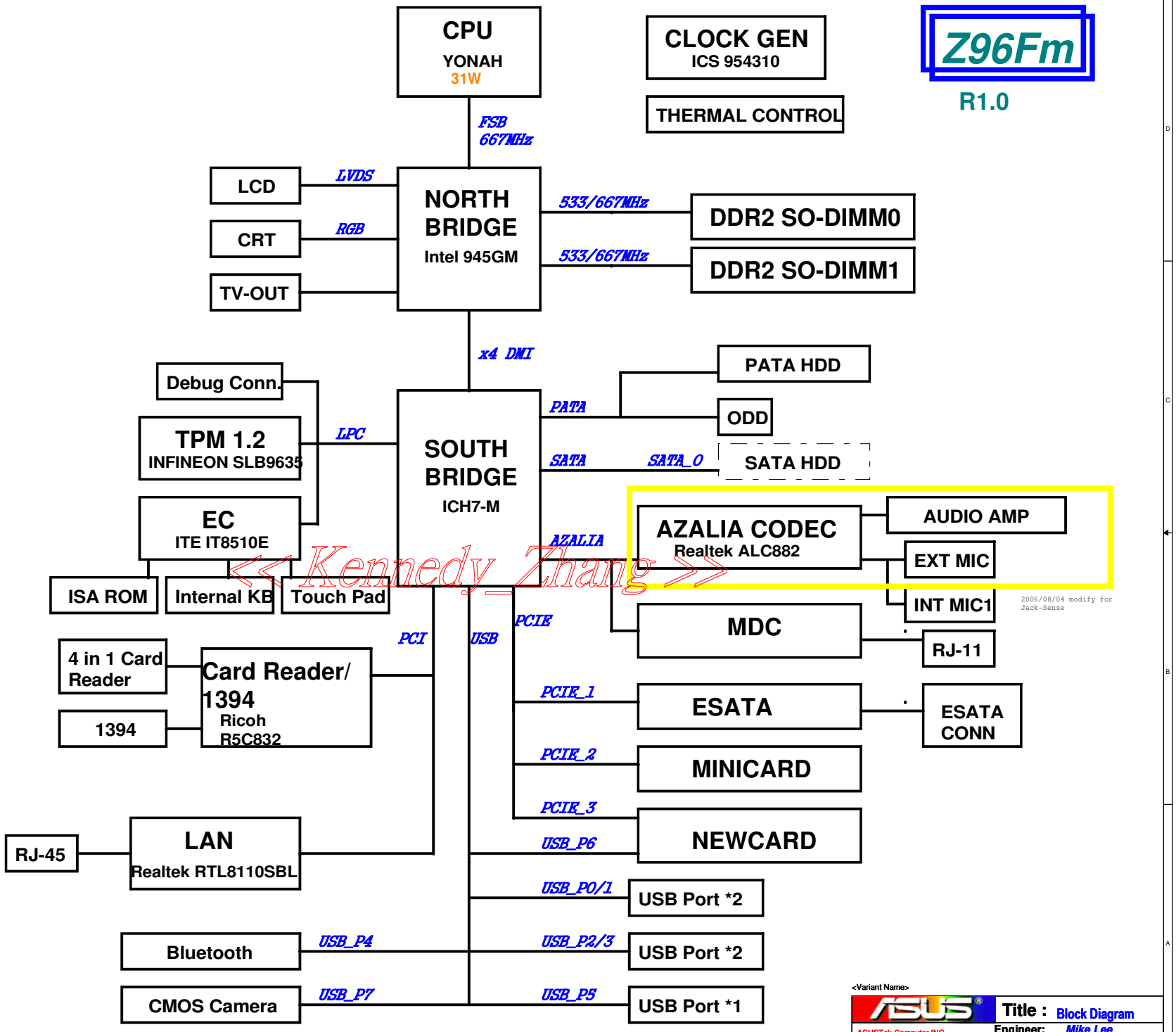



<Variant Name>

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 1 of 96

## EC GPIO SETTING

| Pin | Pin Name | Signal Name | Type | Z96J Default | EC Default |
|---|---|---|---|---|---|
| 32 | PWM0/GPA0 | / | | | GPI |
| 33 | PWM1/GPA1 | FAN_PWM | O | H | GPI |
| 36 | PWM2/GPA2 | CLK_PWRSAVE# | O | H | GPI |
| 37 | PWM3/GPA3 | / | I | | GPI |
| 38 | PWM4/GPA4 | CHG_LED_UP# | O | H | GPI |
| 39 | PWM5/GPA5 | PWR_LED_UP# | O | H | GPI |
| 40 | PWM6/GPA6 | / | O | | GPI |
| 43 | PWM7/GPA7 | LCD_BACKOFF# | O | H | GPI |
| 153 | RXD/GPB0 | NUM_LED | O | L | GPI |
| 154 | TXD/GPB1 | CAP_LED | O | L | GPI |
| 162 | GPB2 | SCRL_LED | O | L | GPI |
| 163 | SMCLK0/GPB3 | SMB0_CLK | SMCLK0 | | GPI |
| 164 | SMDAT0GPB4 | SMB0_DAT | SMDAT0 | | GPI |
| 5 | GA20/GPB5 | A20GATE | GA20 | | GPO |
| 6 | KBRST#/GPB6 | RC_IN# | KBRST# | | KBRST# |
| 165 | GPB7 | / | I | | GPI |
| 47 | CLKOUT/GPC0 | / | O | | GPI |
| 169 | SMCLK1/GPC1 | SMB1_CLK | SMCLK1 | | GPI |
| 170 | SMDAT1/GPC2 | SMB1_DAT | SMDAT1 | | GPI |
| 171 | GPC3 | MAIL_LED | O | L | GPI |
| 172 | TMRI0/WUI2/GPC4 | [redacted] | I | | GPI |
| 175 | GPC5 | OP_SD# | O | H | GPI |
| 176 | TMRI1/WUI3/GPC6 | BAT_IN_OC# | I | H | GPI |
| 1 | CK32KOUT/GPC7 | / | | | GPI |
| 26 | RI1#/WUI0/GPD0 | SUSB# | I | | GPI |
| 29 | RI2#/WUI1/GPD1 | SUSC# | I | | GPI |
| 30 | LPCRST#/WUI4//GPD2 | PLT_RST# | LPCRST | | LPCRST |
| 31 | ECSCI#/GPD3 | EXT_SCI# | ECSCI# | H | GPI |
| 41 | GPD4 | RF_ON_SW# | O | H | GPI |
| 42 | GINT/GPD5 | / | | | GPI |
| 62 | TACH0/GPD6 | FAN0_TACH | TACH0 | | GPI |
| 63 | TACH1/GPD7 | / | | | GPI |
| 87 | ADC4/GPE0 | DISTP_SW# | I | | GPI |
| 88 | ADC5/GPE1 | / | | | GPI |
| 89 | ADC6/GPE2 | EMAIL_SW# | I | | GPI |
| 90 | ADC7/GPE3 | EXPLORE_SW# | I | | GPI |
| 2 | PWRSW/GPE4 | PWR_SW# | PWRSW | | GPI |
| 44 | WUI5/GPE5 | / | | | GPI |
| 24 | LPCPD#/WUI6/GPE6 | LID_EC# | I | | GPI |
| 25 | CLKRUN#/WUI7/GPE7 | / | | | GPI |
| 110 | PS2CLK0/GPF0 | / | | | GPI |
| 111 | PS2DAT0/GPF1 | / | | | GPI |
| 114 | PS2CLK1/GPF2 | / | | | GPI |
| 115 | PS2DAT1/GPF3 | / | | | GPI |
| 116 | PS2CLK2/GPF4 | TP_CLK | PS2CLK2 | | GPI |
| 117 | PS2DAT2/GPF5 | TP_DAT | PS2DAT2 | | GPI |
| 118 | PS2CLK3/GPF6 | / | | | GPI |
| 119 | PS2DAT3/GPF7 | INTERNET# | I | | GPI |
| 113 | FA16/GPG0 | FA16 | FA16 | | GPI |
| 112 | FA17/GPG1 | FA17 | FA17 | | GPI |
| 104 | FA18/GPG2 | FA18 | FA18 | | GPI |
| 103 | FA19/GPG3 | / | | | GPI |
| 3 | FA20/GPG4 | THRM_CPU# | I | H | GPI |
| 4 | FA21/GPG5 | / | | | GPI |
| 27 | LPC80HL/GPG6 | PMTHERM# | O | H | GPI |
| 28 | LPC80LL/GPG7 | [redacted] | I | H | GPI |

06/01/23

| Pin | Pin Name | Signal Name | Type | Default | |
|---|---|---|---|---|---|
| 48 | GPH0 | VSUS_ON | O | L | GPI |
| 54 | GPH1 | VSUS_GD# | I | H | GPI |
| 55 | GPH2 | CPUPWR_GD# | I | H | GPI |
| 69 | GPH3 | PM_PWRBTN# | O | H | GPI |
| 70 | GPH4 | SUSC_ON | O | L | GPI |
| 75 | GPH5 | SUSB_ON | O | L | GPI |
| 76 | GPH6 | CPU_VRON | O | L | GPI |
| 105 | GPH7 | PM_RSMRST# | O | L | GPI |
| 148 | GPI0 | ICH7_PWROK | O | L | GPI |
| 149 | GPI1 | / | O | | GPI |
| 152 | GPI2 | MCHOK | I | L | GPI |
| 155 | GPI3 | CHG_EN# | O | H | GPI |
| 156 | GPI4 | PRECHG | O | L | GPI |
| 168 | GPI5 | BAT_LL# | O | H | GPI |
| 174 | GPI6 | BAT_LEARN | O | L | GPI |
| 93 | ADC8 | KID0 | I | | |
| 94 | ADC9 | KID1 | I | | |
| 101 | DAC2 | BL_PWM_DA | O | | |
| 102 | DAC3 | BATSEL_2P# | O | | |

## ICH7-M GPIO SETTING

| Pin | Pin Name | Signal Name | Type | Power_Well | Default |
|---|---|---|---|---|---|
| AB18 | GPIO00/BM_BUSY# | PM_BMBUSY# | I | Core(To:3.3V) | GPI |
| C8 | GPIO01/REQ5# | PCI_REQ#5 | I/O | Core(To:5V) | GPI |
| G8 | GPIO02/PIRQE# | PCI_INTE# | I(OD) | Core(To:5V) | GPI |
| F7 | GPIO03/PIRQF# | PCI_INTF# | I(OD) | Core(To:5V) | GPI |
| F8 | GPIO04/PIRQG# | PCI_INTG# | I(OD) | Core(To:5V) | GPI |
| G7 | GPIO05/PIRQH# | PCI_INTH# | I(OD) | Core(To:5V) | GPI |
| AC21 | GPIO06 | NC | I/O | Core(To:3.3V) | GPI |
| AC18 | GPIO07 | WLAN_BT_LED_EN# | I | Core(To:3.3V) | GPI |
| E21 | GPIO08 | EXTSMI# | I | SUS(To:3.3V) | GPI |
| E20 | GPIO09 | SATA_DET#0 | I/O | SUS(To:3.3V) | GPI |
| A20 | GPIO10 | WLAN_ON# | O | SUS(To:3.3V) | GPI |
| B23 | SMBALERT#/GPIO11 | SMB_ALERT# | I/O | SUS(To:3.3V) | Native |
| F19 | GPIO12 | KBC_SCI# | I | SUS(To:3.3V) | GPI |
| E19 | GPIO13 | TP | I/O | SUS(To:3.3V) | GPI |
| R4 | GPIO14 | NC | I/O | SUS(To:3.3V) | GPI |
| E22 | GPIO15 | CB_SD# | I/O | SUS(To:3.3V) | GPI |
| AC22 | GPIO16/DPRSLPVR | PM_DPRSLPVR | O | Core(To:3.3V) | Native |
| D8 | GPIO17/GNT5# | PCI_GNT#5 | I/O | Core(To:3.3V) | GPO |
| AC20 | GPIO18/STP_PCI# | STP_PCI# | O | Core(To:3.3V) | GPO |
| AH18 | GPIO19/SATA1GP | NC | O | Core(To:3.3V) | GPI |
| AF21 | GPIO20/STP_CPU# | STP_CPU# | O | Core(To:3.3V) | GPO |
| AE19 | GPIO21/SATA0GP | NC | I/O | Core(To:3.3V) | GPI |
| A13 | GPIO22/REQ4# | PCI_REQ#4 | I/O | Core(To:3.3V) | Native |
| AA5 | LDRQ1#/GPIO23 | TP | I/O | Core(To:3.3V) | Native |
| R3 | GPIO24 | NC | I/O | SUS(To:3.3V) | GPO |
| D20 | GPIO25 | NC | I/O | SUS(To:3.3V) | GPO |
| A21 | GPIO26/EL_RSVD | NC | I/O | SUS(To:3.3V) | GPO |
| B21 | GPIO27/EL_STATE0 | PD_DET# | I/O | SUS(To:3.3V) | GPO |
| E23 | GPIO28/EL_STATE1 | NC | I/O | SUS(To:3.3V) | GPO |
| C3 | GPIO29/OC#5 | USB_OC#5 | I/O | SUS(To:3.3V) | Native |
| A2 | GPIO30/OC#6 | NEWCARD_OC# | I | SUS(To:3.3V) | Native |
| B3 | GPIO31/OC#7 | USB_OC#7 | I/O | SUS(To:3.3V) | Native |
| AG18 | GPIO32/CLKRUN# | PM_CLKRUN# | O | Core(To:3.3V) | GPO |
| AC19 | GPIO33/AZ_DOCK_EN# | BT_ON# | O | Core(To:3.3V) | GPO |
| U2 | GPIO34/AZ_DOCK_RST# | NC | I/O | Core(To:3.3V) | GPO |
| AD21 | GPIO35 | NC | I/O | Core(To:3.3V) | GPO |
| AH19 | GPIO36/SATA2GP | NC | I/O | Core(To:3.3V) | GPI |
| AE19 | GPIO37/SATA3GP | PCB_ID0 | I | Core(To:3.3V) | GPI |
| AD20 | GPIO38 | PCB_ID1 | I | Core(To:3.3V) | GPI |
| AE20 | GPIO39 | PCB_ID2 | I | Core(To:3.3V) | GPI |
| A14 | GNT4#/GPIO48 | PCI_GNT#4 | I/O | Core(To:3.3V) | Native |
| AG24 | GPIO49/CPUPWRGD | H_PWRGD | O | V_CPU_IO | Native |



| SM-Bus Device | SM-Bus Address |
|---|---|
| Clock Generator | 1101001x ( D2 ) |
| SO-DIMM 0 | 1010000x ( A0 ) |
| SO-DIMM 1 | 1010001x ( A2 ) |
| Thermal Sensor | 01001100 ( 4C ) |
| | |
| | |

| PCI Device | IDSEL# | REQ/GNT# | Interrupts |
|---|---|---|---|
| | | | |
| CARD READER | AD17 | 0 | B |
| 1394 | AD17 | 0 | A |
| LAN | AD23 | 2 | C |

<Variant Name>

Title : <Title>

ASUSTek Computer INC. Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 2 of 96

<< Kennedy_Zhang >>

<Variant Name>

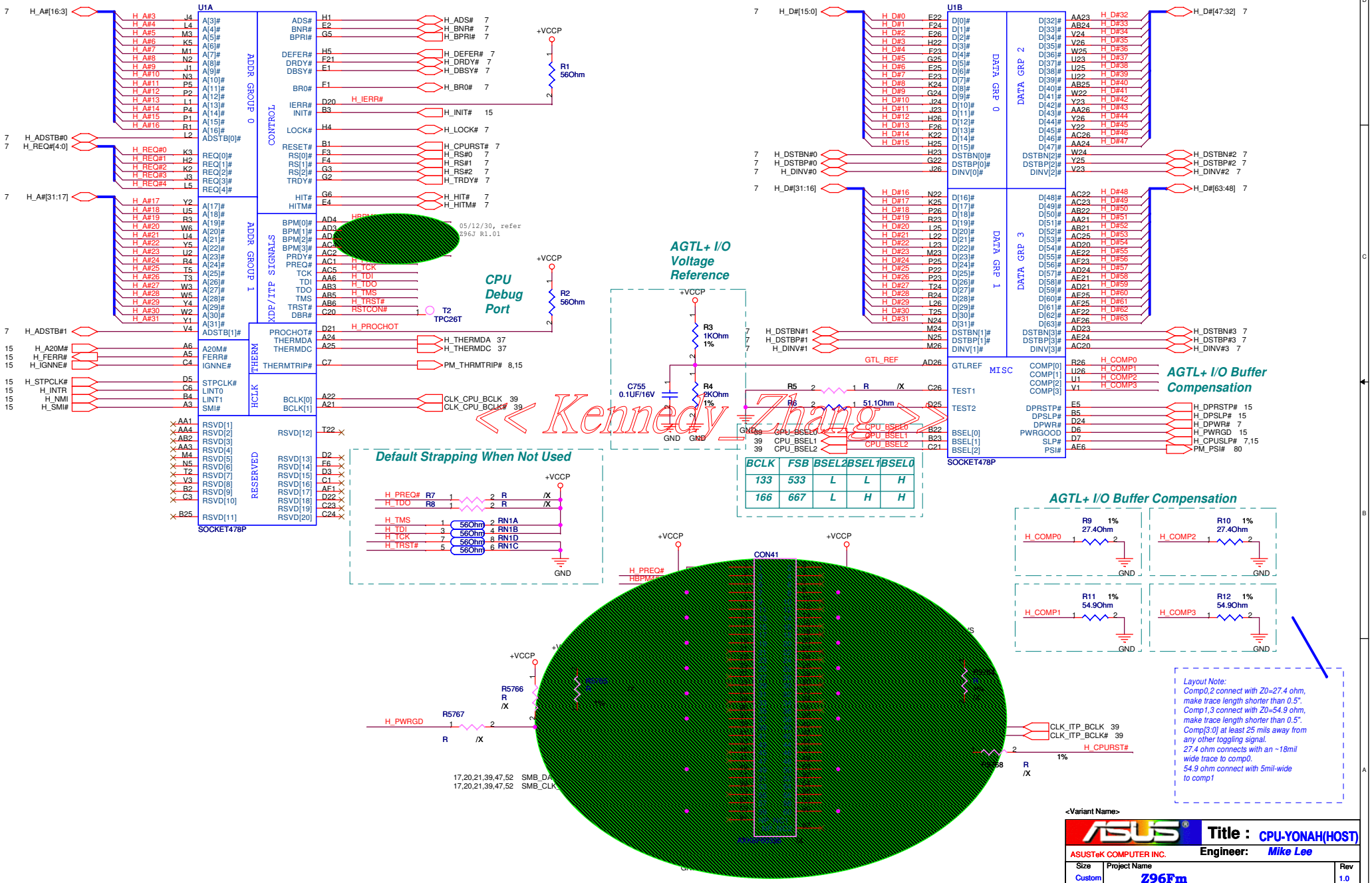
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 3 of 96




<Variant Name>

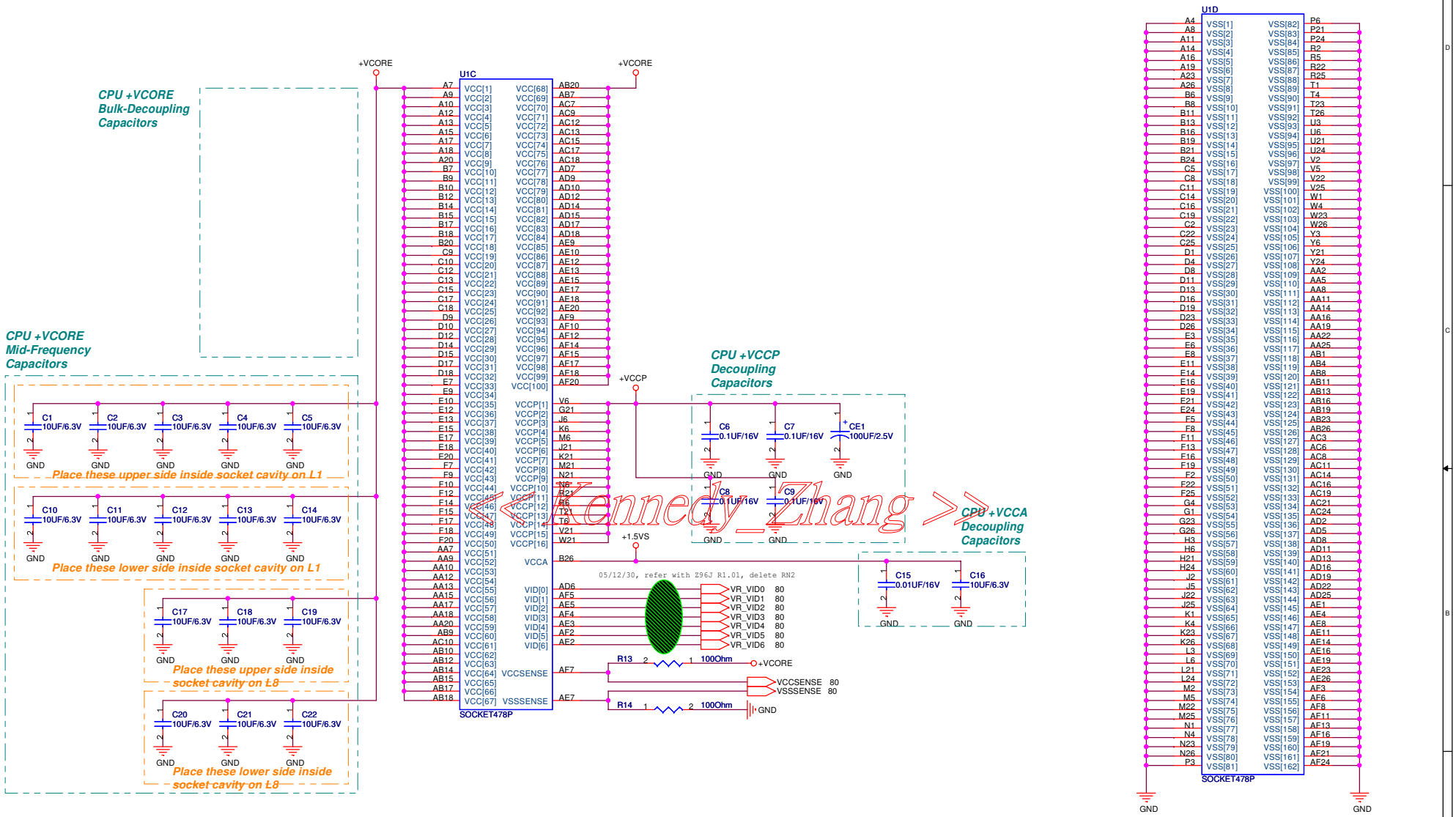
ASUSTeK COMPUTER INC.

Title : CPU-YONAH(HOST)

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 4 of 96






*+VCORE Mid-Frequency Capacitor*
*Intel: 22UF *32*
*R1F: 10UF *16*
*+VCCP Decoupling Capacitor*
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CPU_YONAH(PWR) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 5 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

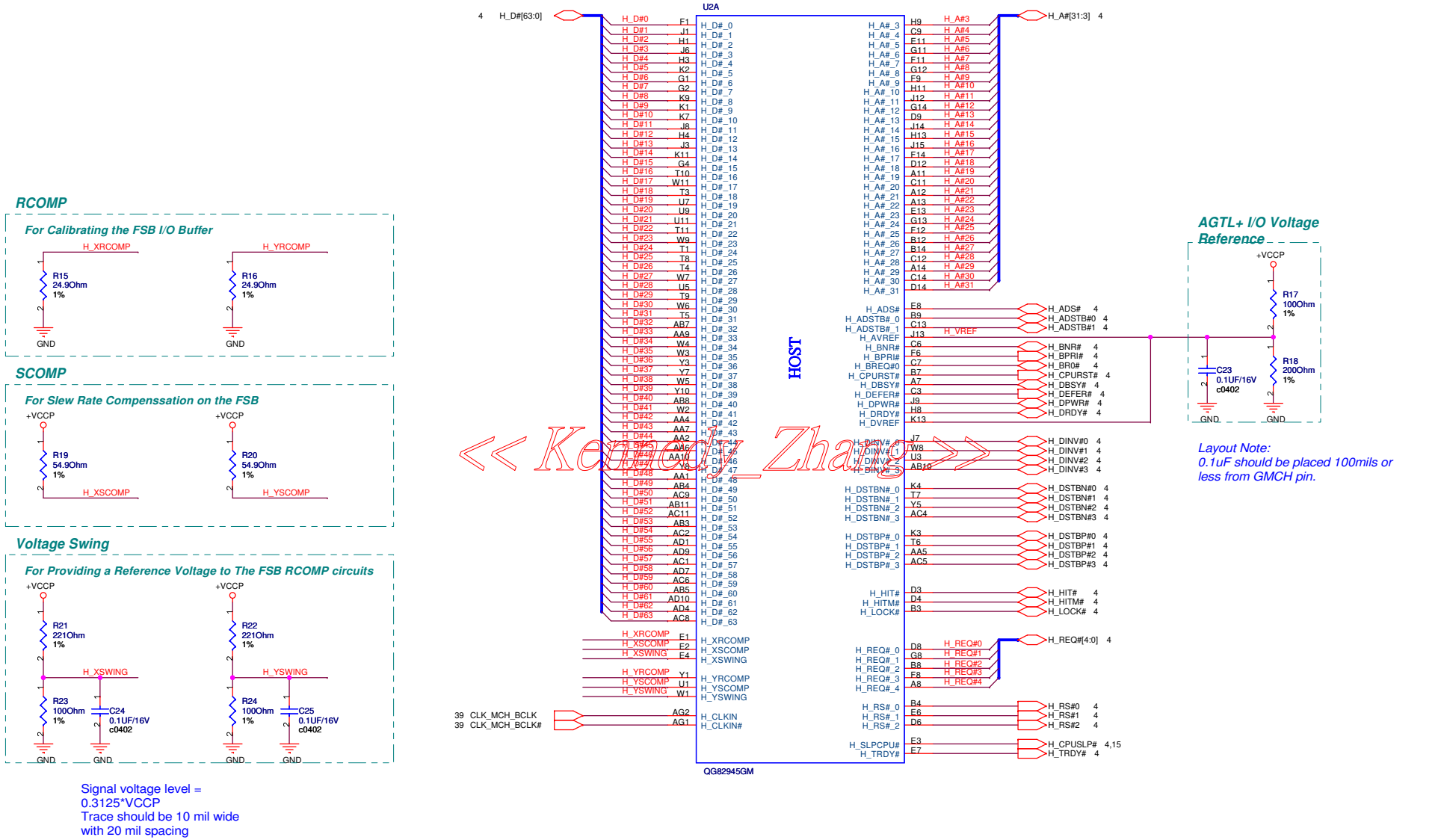
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 6 of 96

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|---|---|---|
| Title : NB-945GM(HOST) | | |
| ASUSTeK COMPUTER INC. | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 7 of 96 | |

## GMCH Strapping

**CFG5 : DMI Strap**

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — R25 /X — GND

**CFG[13:12] : GMCH Test Mode**

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

**CFG7 : CPU Strap**

0 = DT/Transpotable CPU
1 = Mobile CPU (D)

MCH_CFG_7 — R26 /X — GND

**CFG15 : ICH RESET Disable**

0 = ICH Reset Disable
1 = Normal Operation (D)

MCH_CFG_15 — R27 /X — GND

**CFG9 : PCIE Graphic Lane**

0 = Reverse Lane
1 = Normal Operation (D)

MCH_CFG_9 — R30 /X — GND

**CFG16 : FSB Dynamic ODT**

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 /X — GND

**CFG10 : HOST PLL VCO Select**

0 = Reserved
1 = Mobility (D)

MCH_CFG_10 — R34 /X — GND

**CFG18 : VCC Select**

0 = 1.05V (D)
1 = 1.5V

MCH_CFG_18 — R35 /X — +2.5VS

**CFG11 : PSB 4x CLK Enable**

0 = 4x Enable
1 = 8x Enable (D)

MCH_CFG_11 — R37 /X — GND

**CFG19 : DMI Lane Reversal**

0 = Normal Operation (D)
1 = Lanes Reversed

MCH_CFG_19 — R38 /X — +2.5VS

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 133 | 533 | L | L | H |
| 166 | 667 | L | H | H |

U2B

RSVD: RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 TV_DCONSEL_0 TV_DCONSEL_1 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15

CFG: CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM: PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 PM_THRMTRIP# PWROK RSTIN#

MISC: SDVO_CTRLCLK SDVO_CTRLDATA ICH_SYNC# CLK_REQ#

NC: NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

QG82945GM

39 MCH_BSEL0
39 MCH_BSEL1
39 MCH_BSEL2

MCH_CFG_5 MCH_CFG_7 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_15 MCH_CFG_16 MCH_CFG_18 MCH_CFG_19

+3VS — TPC26T T3 — 17 PM_BMBUSY#

R32 10KOhm r0402 PM_EXTTS#_0
R33 10KOhm r0402 PM_EXTTS#_1

4,15 PM_THRMTRIP#
17,59,80,90 VRM_PWRGD

16,17,47,52 BUF_PLT_RST# — R36 100Ohm — RST_IN_MCH#

16 MCH_ICH_SYNC#

R5794 0Ohm — GND

DDR MUXING

SM_CK_0 SM_CK_1 SM_CK_2 SM_CK_3 → M_CLK_DDR0 20, M_CLK_DDR1 20, M_CLK_DDR2 21, M_CLK_DDR3 21

SM_CK#_0 SM_CK#_1 SM_CK#_2 SM_CK#_3 → M_CLK_DDR#0 20, M_CLK_DDR#1 20, M_CLK_DDR#2 21, M_CLK_DDR#3 21

SM_CKE_0 SM_CKE_1 SM_CKE_2 SM_CKE_3 → M_CKE0 20,22, M_CKE1 20,22, M_CKE2 21,22, M_CKE3 21,22

SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 → M_CS#0 20,22, M_CS#1 20,22, M_CS#2 21,22, M_CS#3 21,22

SM_OCDCOMP_0 SM_OCDCOMP_1 — M_OCDCOMP0 R5792 — M_OCDCOMP1 R5793 — GND

SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 → M_ODT0 20,22, M_ODT1 20,22, M_ODT2 21,22, M_ODT3 21,22

SM_RCOMP# SM_RCOMP — R28 80.6Ohm 1% — R29 80.6Ohm 1% — +1.8V — GND

SM_VREF_0 SM_VREF_1 — M_VREF_MCH — M_VREF_MCH 20,21,22

Layout Note: Route as short as possible

CLK

G_CLKIN# G_CLKIN D_REFCLKIN# D_REFCLKIN D_REFSSCLKIN# D_REFSSCLKIN

CLK_UMA_96M# CLK_UMA_96M CLK_LCD_SSCG# CLK_LCD_SSCG

→ CLK_MCH_3GPLL# 39, CLK_MCH_3GPLL 39, CLK_UMA_96M# 39, CLK_UMA_96M 39, CLK_LCD_SSCG# 39, CLK_LCD_SSCG 39

DMI

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 → DMI_TXN[3:0] 16

DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 → DMI_TXP[0..3] 16

DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 → DMI_RXN[0..3] 16

DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 → DMI_RXP[0..3] 16

M_VREF_MCH — C26 0.1UF/16V c0402 — GND; C27 1UF/10V — GND

R5798: 17,80 PM_DPRSLPVR — PM_EXTTS#_1



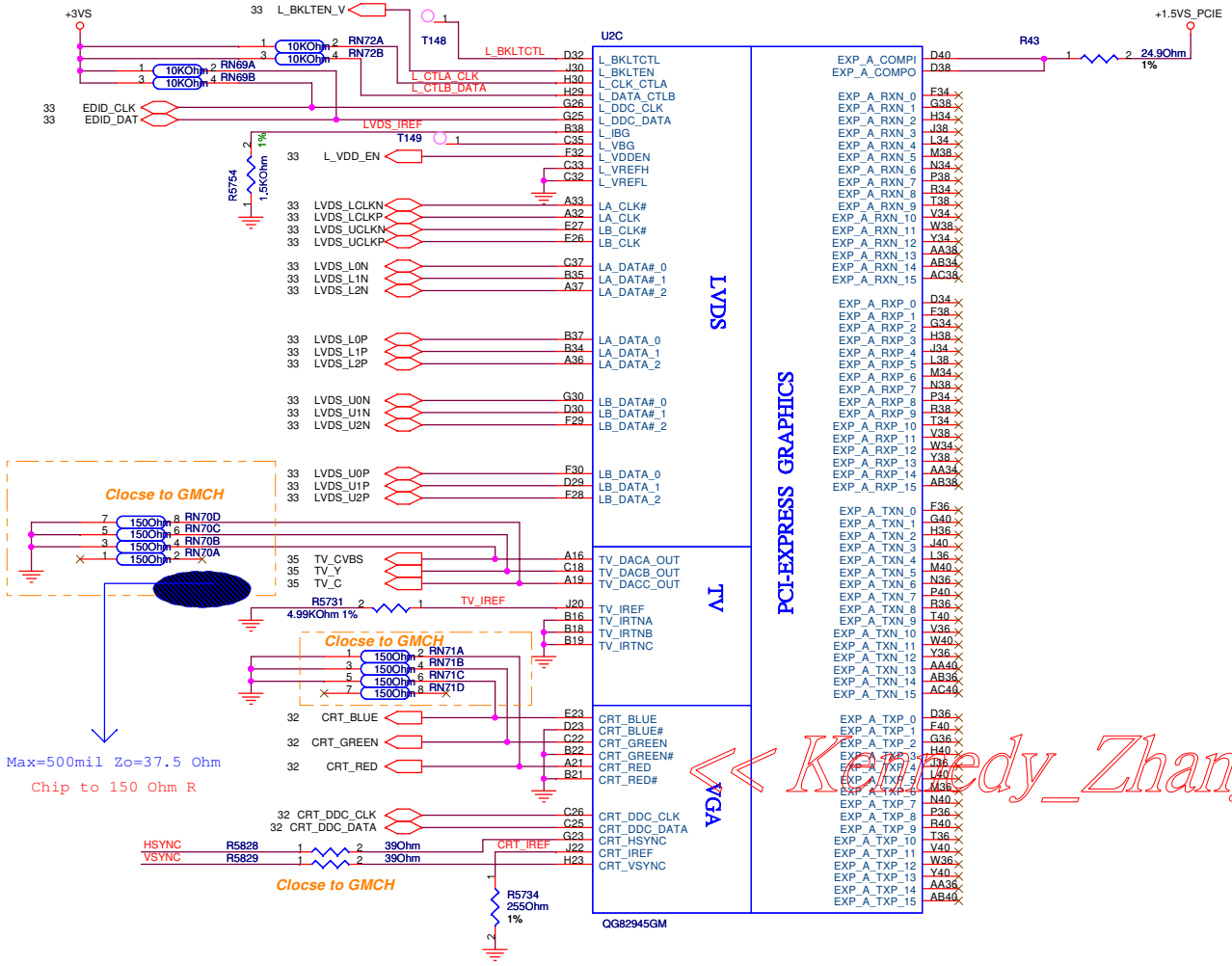
<Variant Name>

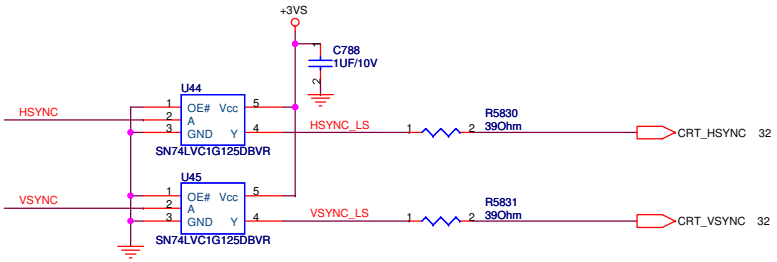
Title : NB-945GM(DMI & CFG)

ASUSTeK COMPUTER INC. Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 8 of 96

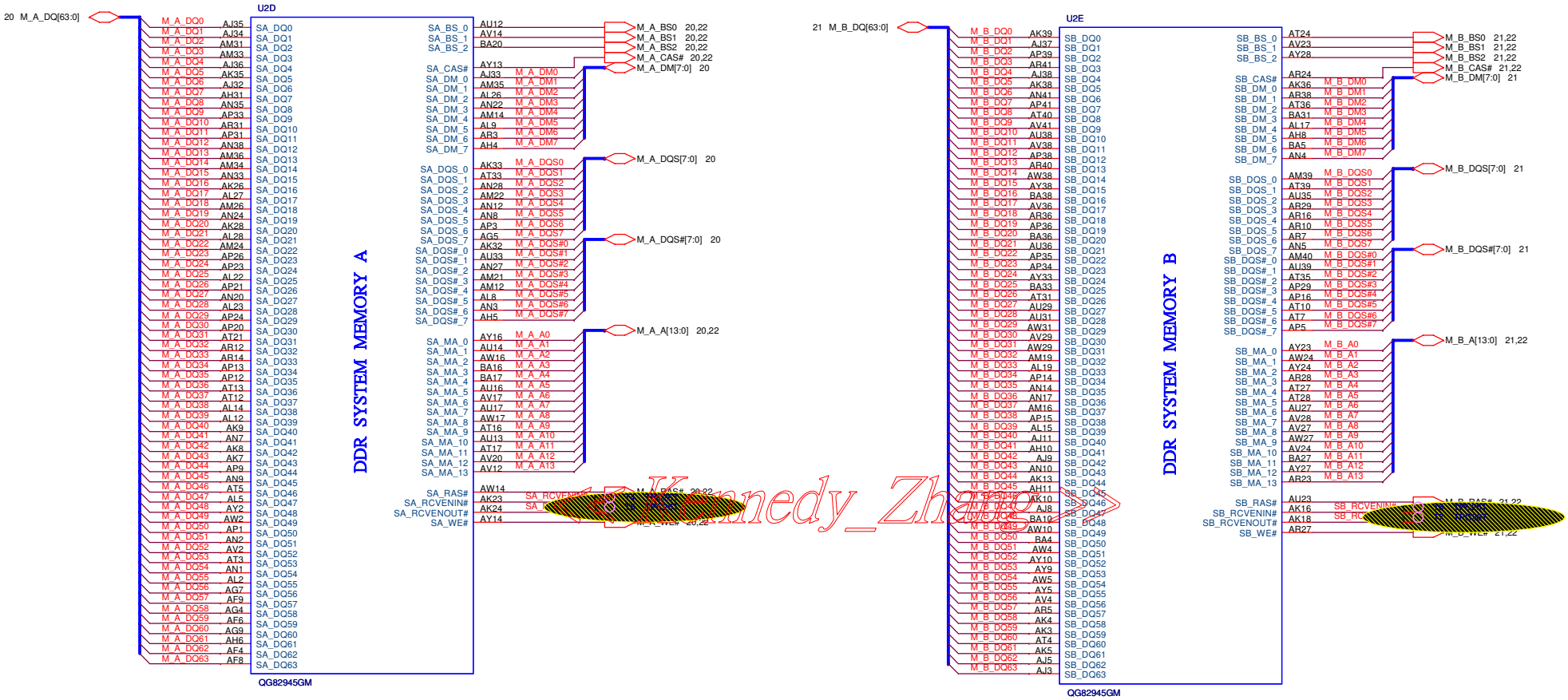





<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : NB-945GM(GRAPHIC) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 9 of 96 | |



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| | | |
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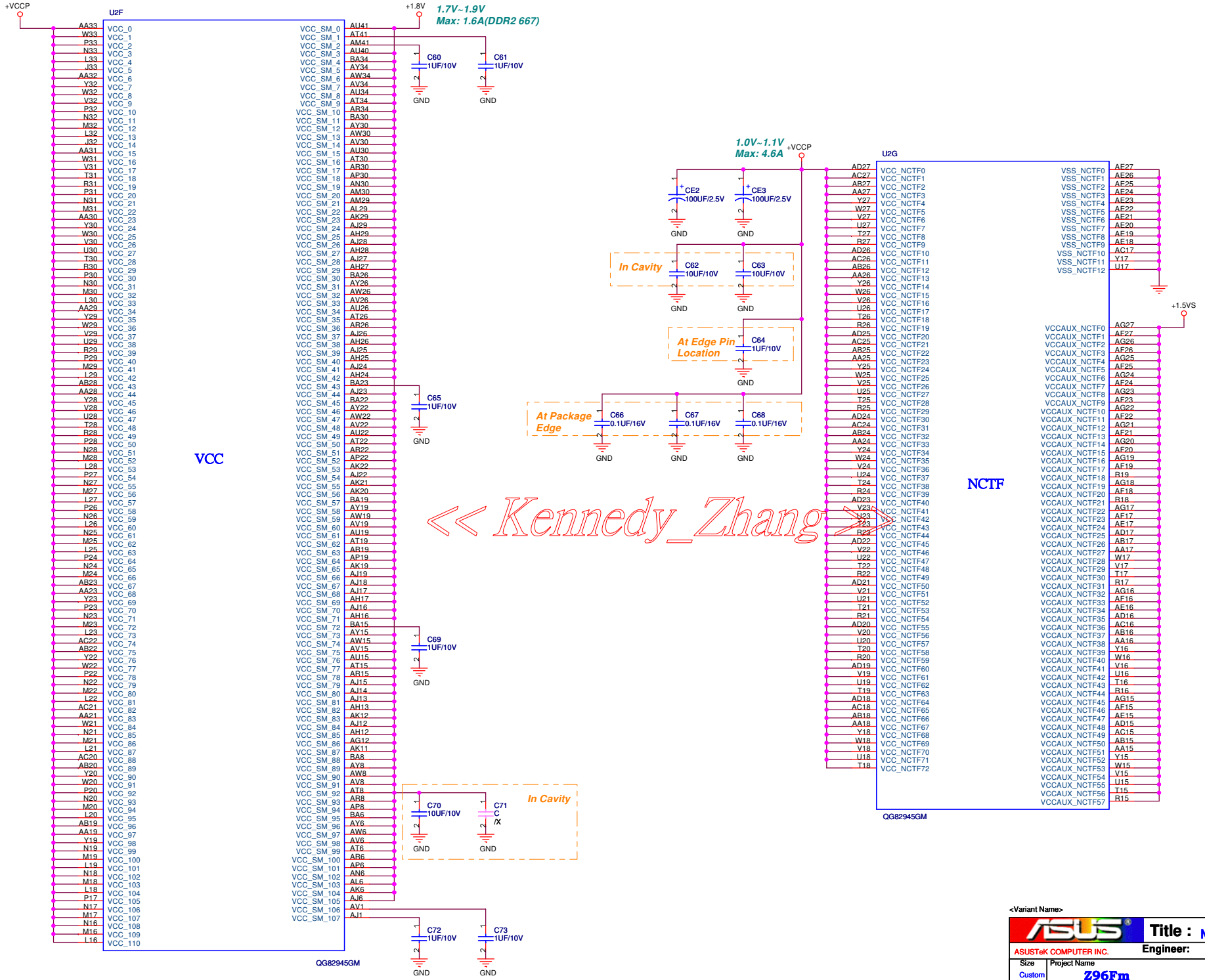
| ASUSTeK COMPUTER INC. | Title : NB-945GM(DDR2) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 10 of 96 | |




<Variant Name>

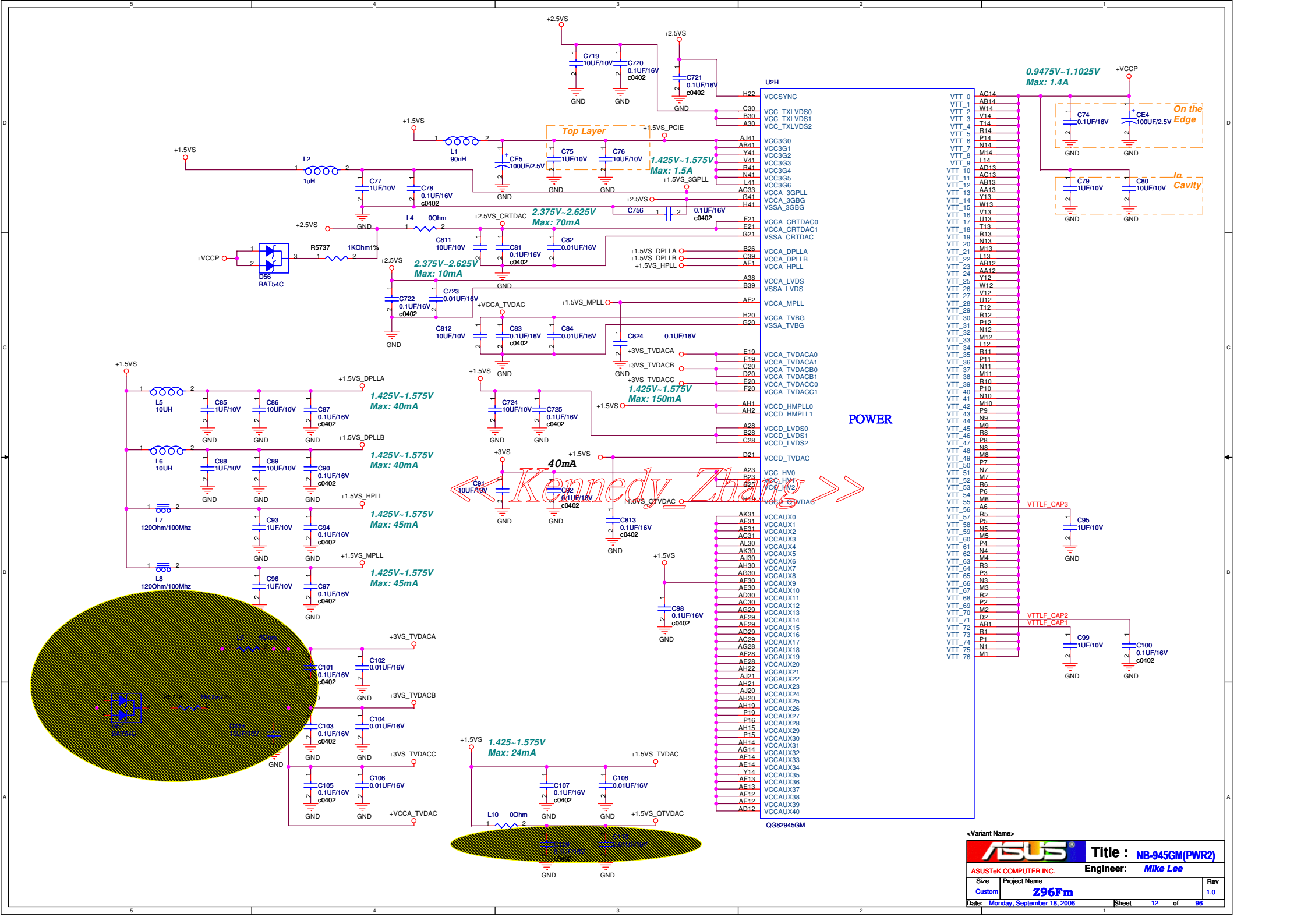
ASUSTeK COMPUTER INC.

Title : NB-945GM(PWR)

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 11 of 96


U2H
POWER
QG82945GM
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
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VTT_11
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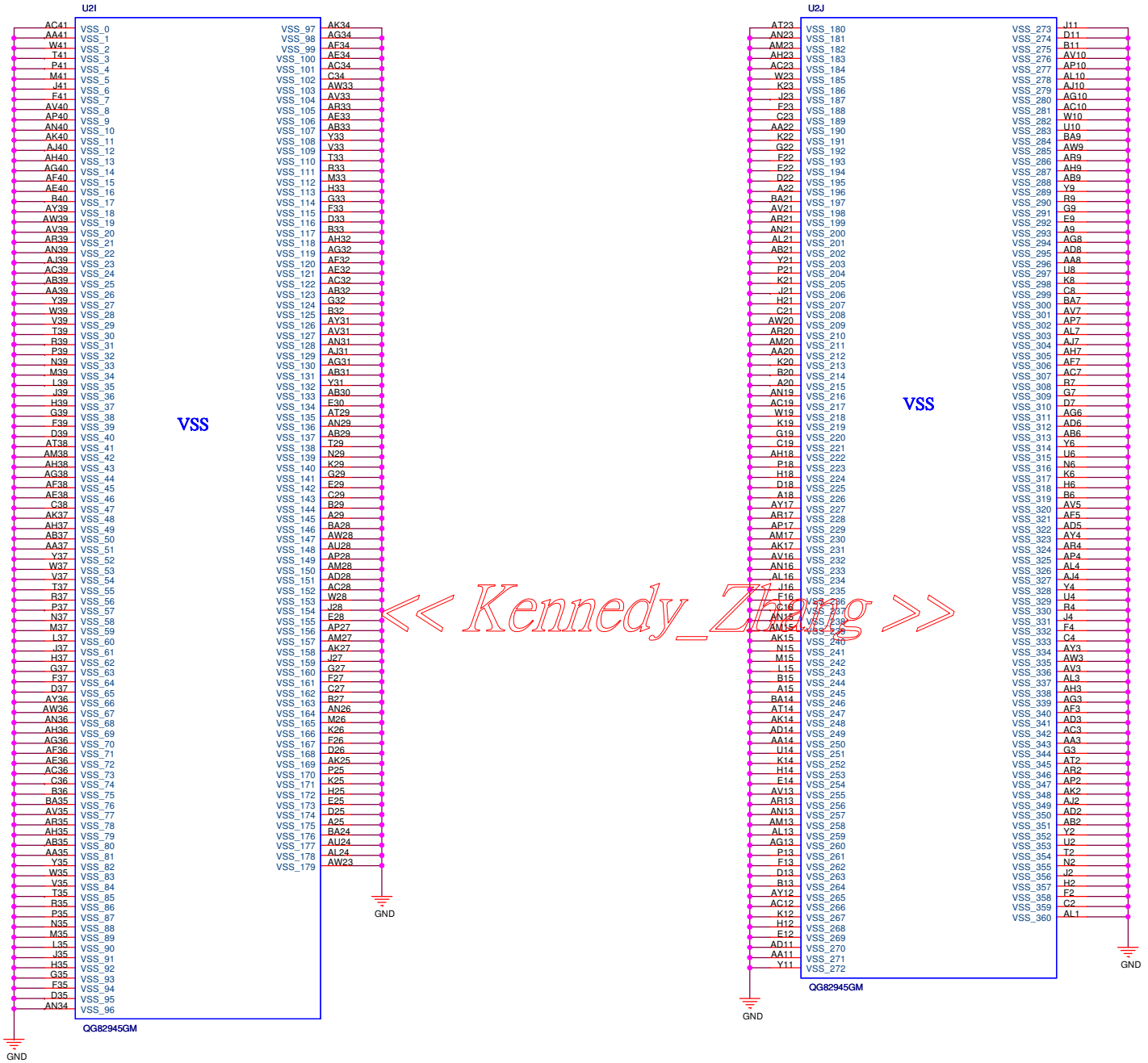
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
+2.5VS
+1.5VS
+1.5VS_PCIE
+1.5VS_3GPLL
+2.5VS_CRTDAC
+VCCA_TVDAC
+1.5VS_MPLL
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_QTVDAC
+VCCP
+3VS
GND
Top Layer
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
2.375V~2.625V
Max: 10mA
1.425V~1.575V
Max: 150mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
40mA
1.425~1.575V
Max: 24mA
0.9475V~1.1025V
Max: 1.4A
On the Edge
In Cavity
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
L1 90nH
L2 1uH
L4 0Ohm
L5 10UH
L6 10UH
L7 120Ohm/100Mhz
L8 120Ohm/100Mhz
L10 0Ohm
R5737 1KOhm1%
D56 BAT54C
C719 10UF/10V
C720 0.1UF/16V c0402
C721 0.1UF/16V c0402
CE5 100UF/2.5V
C75 1UF/10V
C76 10UF/10V
C77 1UF/10V
C78 0.1UF/16V c0402
C756 0.1UF/16V c0402
C811 10UF/10V
C81 0.1UF/16V c0402
C82 0.01UF/16V
C722 0.1UF/16V c0402
C723 0.01UF/16V
C812 10UF/10V
C83 0.1UF/16V c0402
C84 0.01UF/16V
C824 0.1UF/16V
C724 10UF/10V
C725 0.1UF/16V c0402
C91 10UF/10V
C92 0.1UF/16V c0402
C813 0.1UF/16V c0402
C98 0.1UF/16V c0402
C85 1UF/10V
C86 10UF/10V
C87 0.1UF/16V c0402
C88 1UF/10V
C89 10UF/10V
C90 0.1UF/16V c0402
C93 1UF/10V
C94 0.1UF/16V c0402
C96 1UF/10V
C97 0.1UF/16V c0402
C101 0.1UF/16V c0402
C102 0.01UF/16V
C103 0.1UF/16V c0402
C104 0.01UF/16V
C105 0.1UF/16V c0402
C106 0.01UF/16V
C107 0.1UF/16V c0402
C108 0.01UF/16V
C74 0.1UF/16V
CE4 100UF/2.5V
C79 1UF/10V
C80 10UF/10V
C95 1UF/10V
C99 1UF/10V
C100 0.1UF/16V c0402
<Kennedy Zhang>>
<Variant Name>
Title : NB-945GM(PWR2)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
Sheet 12 of 96


U2I
AC41 AA41 W41 T41 P41 M41 J41 F41 AV40 AP40 AN40 AK40 AJ40 AH40 AG40 AF40 AE40 B40 AY39 AW39 AV39 AR39 AN39 AJ39 AC39 AB39 AA39 Y39 W39 V39 T39 R39 P39 N39 M39 L39 J39 H39 G39 F39 D39 AT38 AM38 AH38 AG38 AF38 AE38 C38 AK37 AH37 AB37 AA37 Y37 W37 V37 T37 R37 P37 N37 M37 L37 J37 H37 G37 F37 D37 AY36 AW36 AN36 AH36 AG36 AF36 AE36 AC36 C36 B36 BA35 AV35 AR35 AH35 AB35 AA35 Y35 W35 V35 T35 R35 P35 N35 M35 L35 J35 H35 G35 F35 D35 AN34
VSS_0 VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96
VSS
VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148 VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179
AK34 AG34 AF34 AE34 AC34 C34 AW33 AV33 AR33 AE33 AB33 Y33 V33 T33 R33 M33 H33 G33 F33 D33 B33 AH32 AG32 AF32 AE32 AC32 AB32 G32 B32 AY31 AV31 AN31 AJ31 AG31 AB31 Y31 AB30 F30 AT29 AN29 AB29 T29 N29 K29 G29 E29 C29 B29 A29 BA28 AW28 AU28 AP28 AM28 AD28 AC28 W28 J28 E28 AP27 AM27 AK27 J27 G27 F27 C27 B27 AN26 M26 K26 F26 D26 AK25 P25 K25 H25 E25 D25 A25 BA24 AU24 AL24 AW23
GND
QG82945GM
U2J
AT23 AN23 AM23 AH23 AC23 W23 K23 J23 F23 C23 AA22 K22 G22 F22 F22 D22 A22 BA21 AV21 AR21 AN21 AL21 AB21 Y21 P21 K21 J21 H21 C21 AW20 AR20 AM20 AA20 K20 B20 A20 AN19 AC19 W19 K19 G19 C19 AH18 P18 H18 D18 A18 AY17 AR17 AP17 AM17 AK17 AV16 AN16 AL16 J16 F16 C16 AN15 AM15 AK15 N15 M15 L15 B15 A15 BA14 AT14 AK14 AD14 AA14 U14 K14 H14 E14 AV13 AR13 AN13 AM13 AL13 AG13 P13 F13 D13 B13 AY12 AC12 K12 H12 E12 AD11 AA11 Y11
VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221 VSS_222 VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243 VSS_244 VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256 VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272
VSS
VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286 VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318 VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_343 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360
J11 D11 B11 AV10 AP10 AL10 AJ10 AG10 AC10 W10 U10 BA9 AW9 AR9 AH9 AB9 Y9 R9 G9 E9 A9 AG8 AD8 AA8 U8 K8 C8 BA7 AV7 AP7 AL7 AJ7 AH7 AF7 AC7 R7 G7 D7 AG6 AD6 AB6 Y6 U6 N6 K6 H6 B6 AV5 AF5 AD5 AY4 AR4 AP4 AL4 AJ4 Y4 U4 R4 J4 F4 C4 AY3 AW3 AV3 AL3 AH3 AG3 AF3 AD3 AC3 AA3 G3 AT2 AR2 AP2 AK2 AJ2 AD2 AB2 Y2 U2 T2 N2 J2 H2 F2 C2 AL1
GND
QG82945GM
GND
GND
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Title : NB-945PM(GND)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
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<< Kennedy_Zhang >>

<Variant Name>

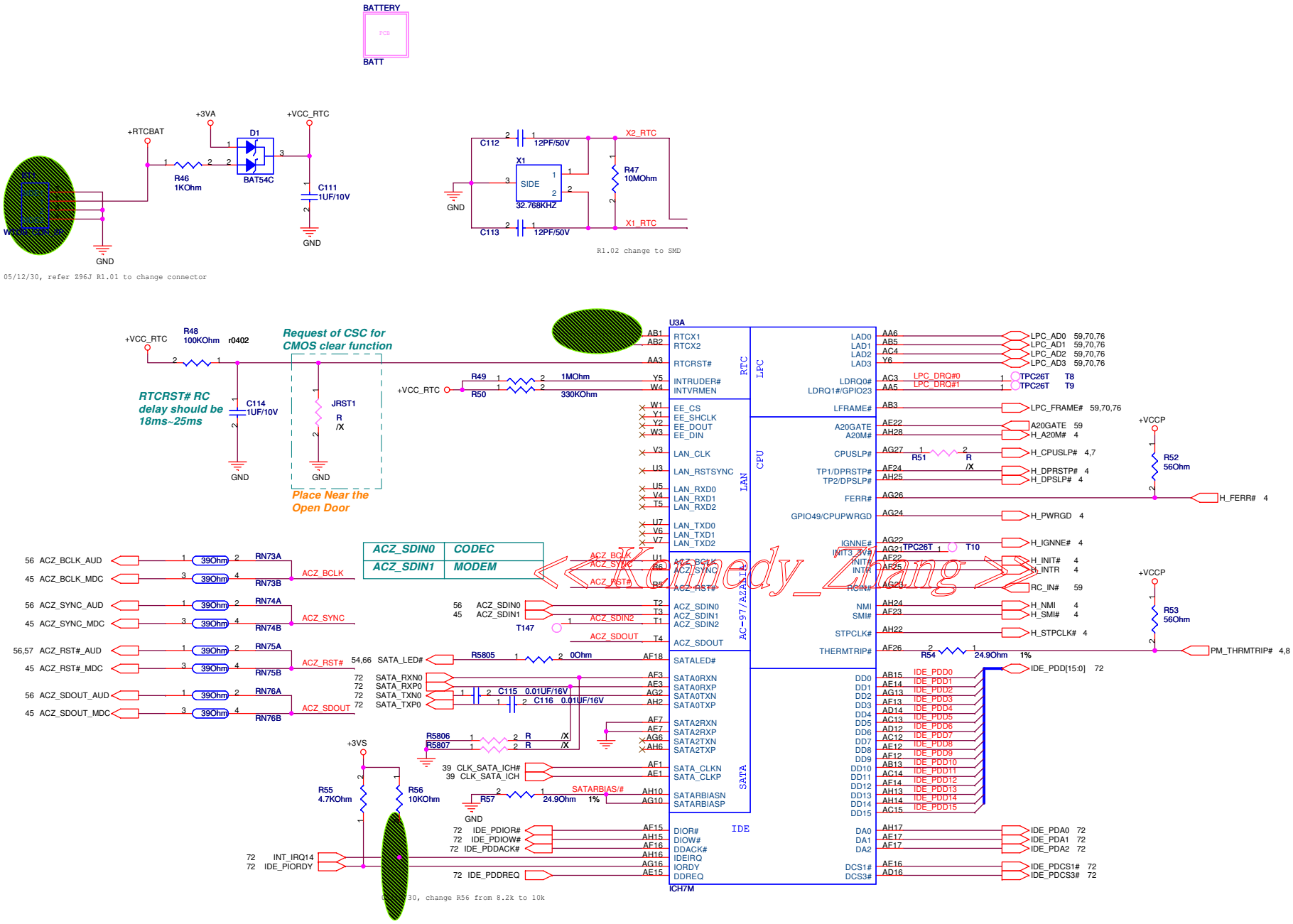
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 14 of 96

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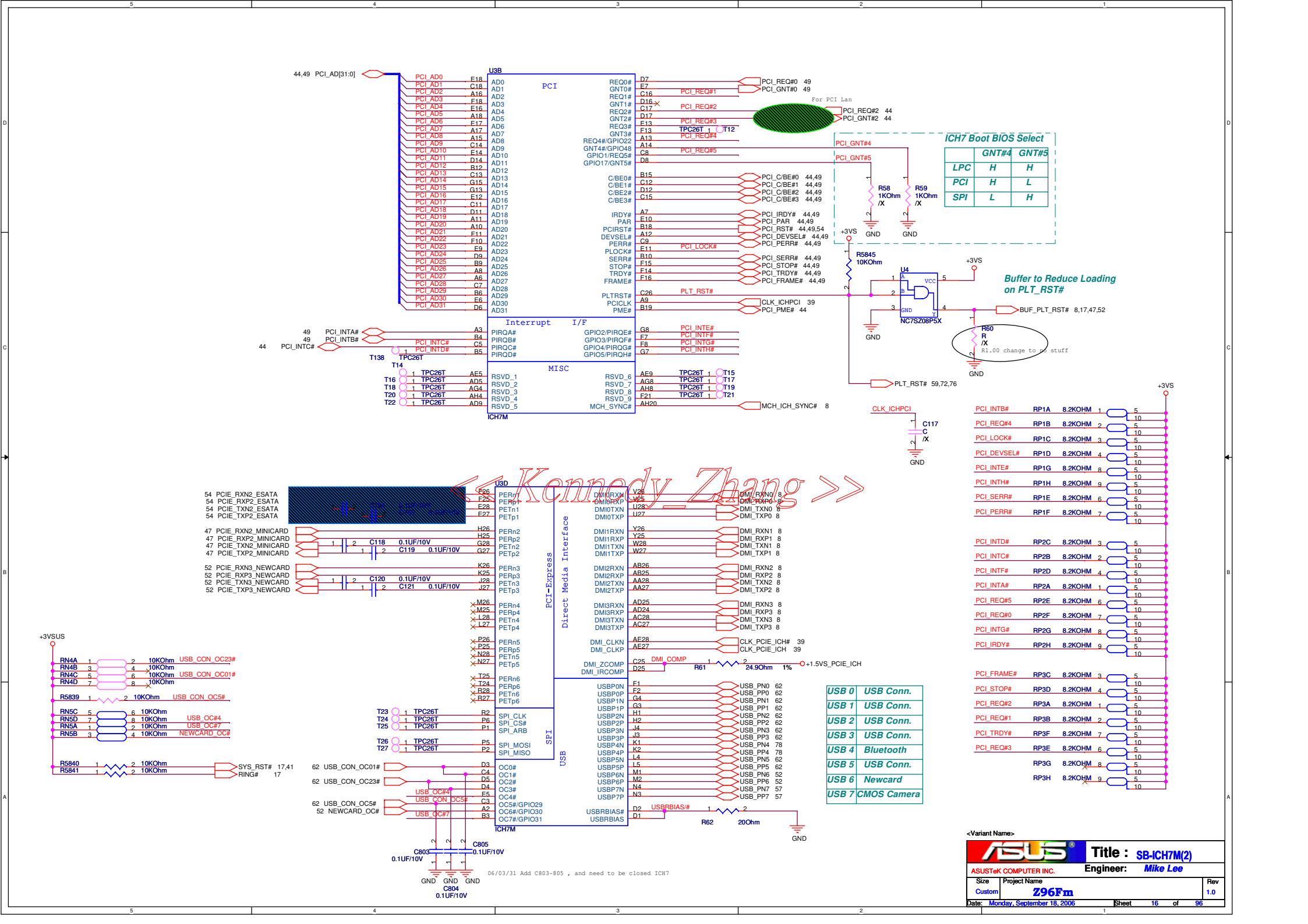
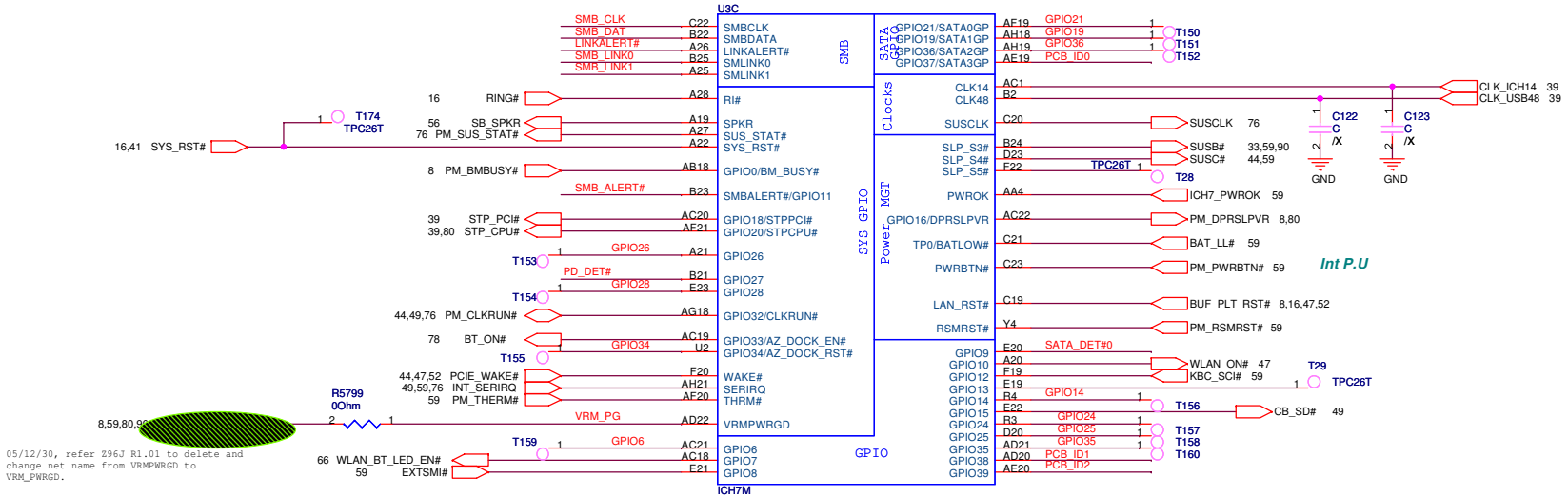
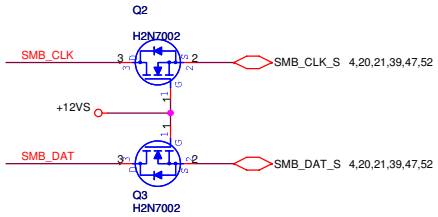
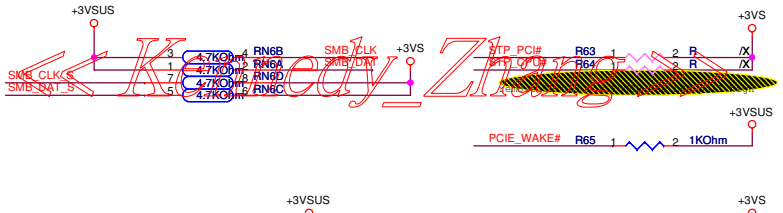
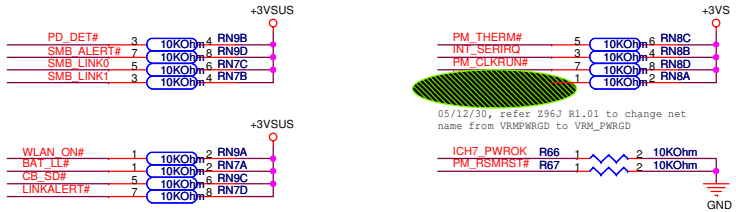
| ASUSTeK COMPUTER INC. | Title : SB-ICH7-M(1) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 15 of 96 | |

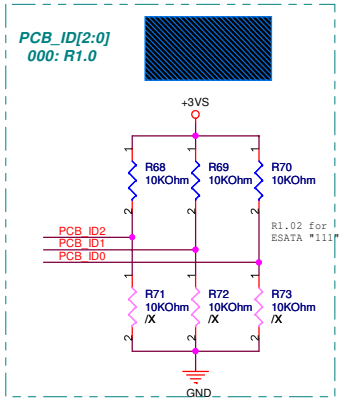

U3B
PCI
Interrupt I/F
MISC
ICH7M
U3D
PCI-Express
Direct Media Interface
USB
SPI
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
For PCI Lan
Buffer to Reduce Loading on PLT_RST#
NC7SZ08P5X
R1.00 change to no stuff
<Kennedy_Zhang>>
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 USB Conn.
USB 6 Newcard
USB 7 CMOS Camera
06/03/31 Add C803-805 , and need to be closed ICH7
<Variant Name>
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
Sheet 16 of 96




PCB_VID3 : PROJECT CODE

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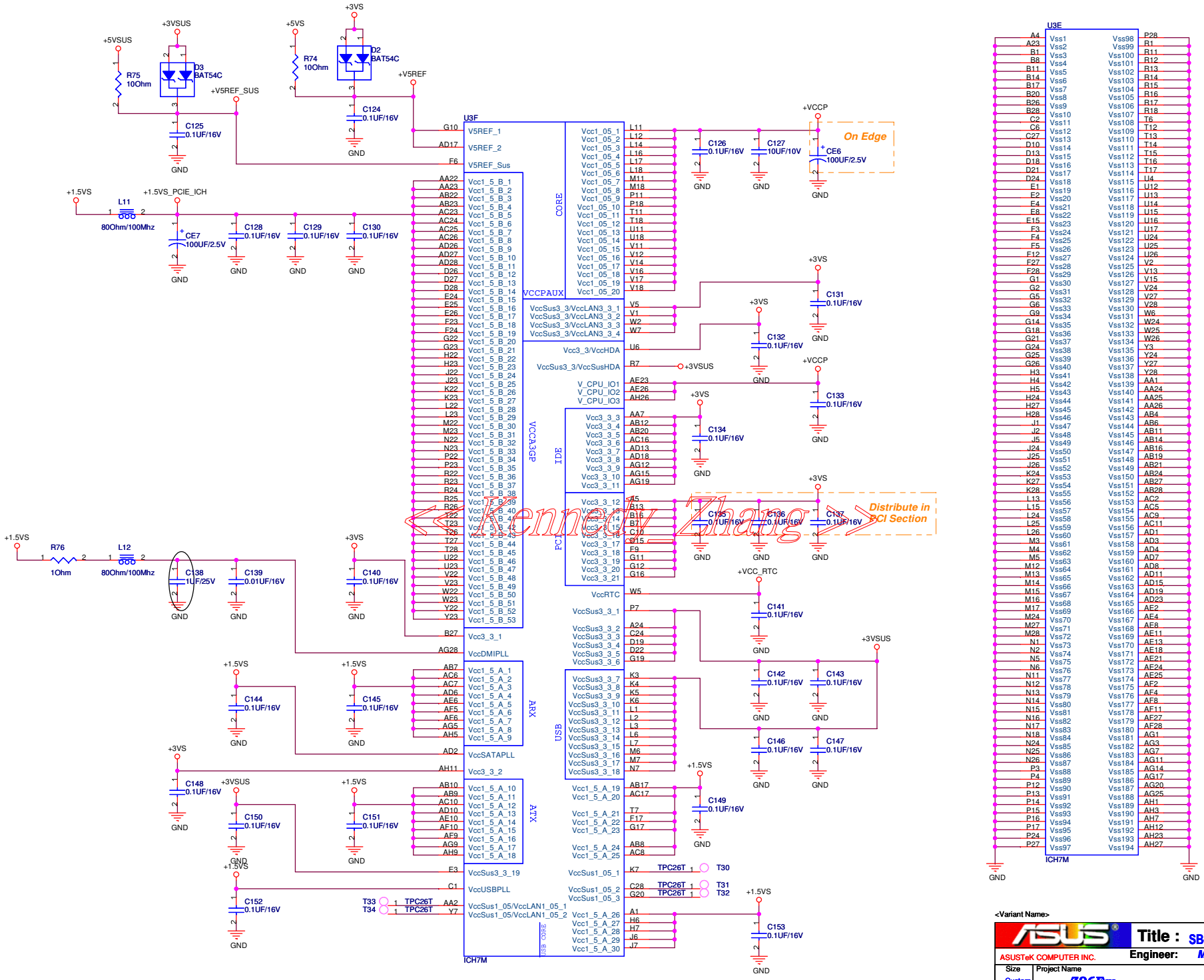
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 17 of 96 | |

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| ASUSTeK COMPUTER INC. | Title : SB-ICH7M(PWR) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 18 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

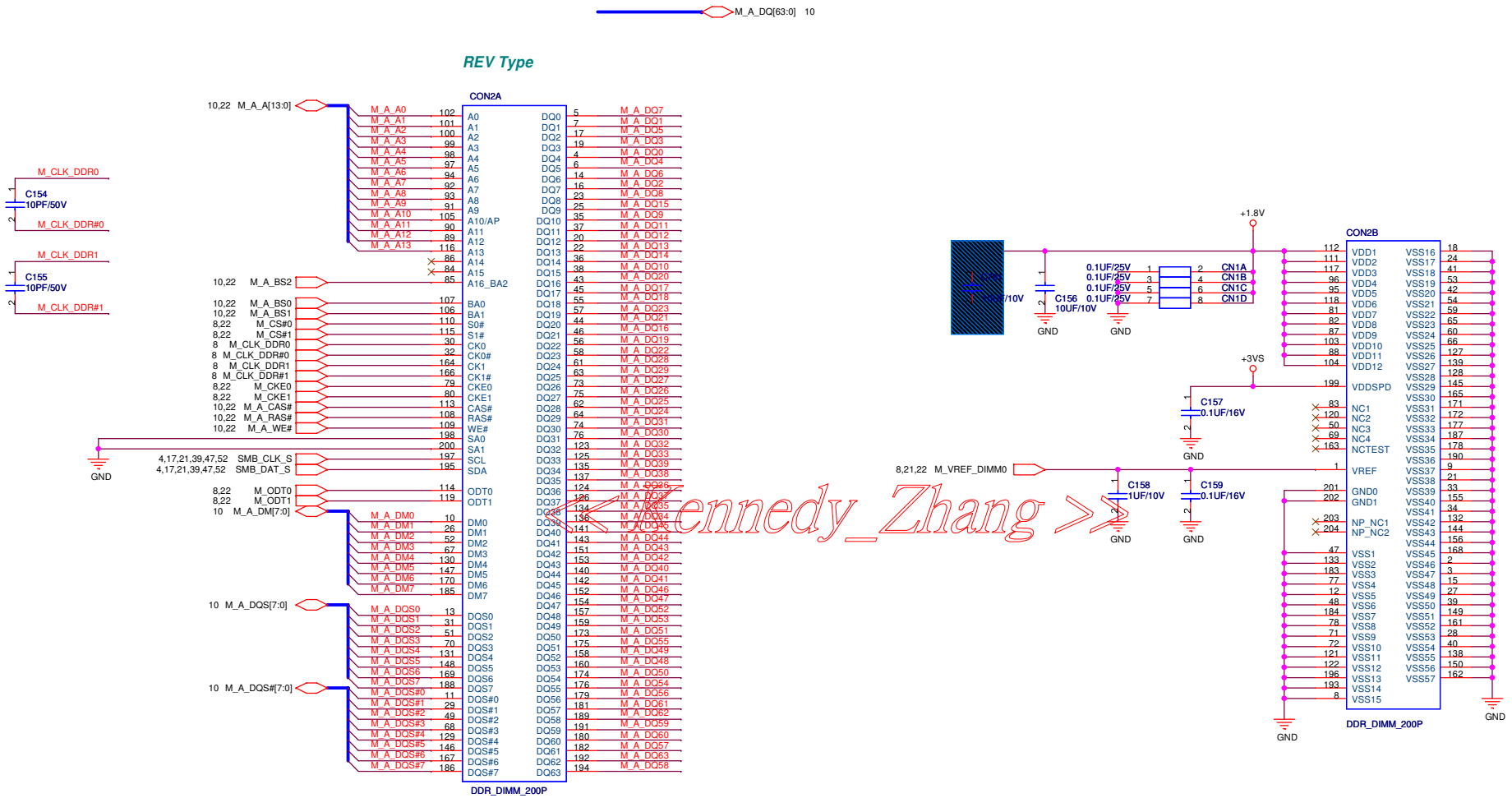
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 19 of 96

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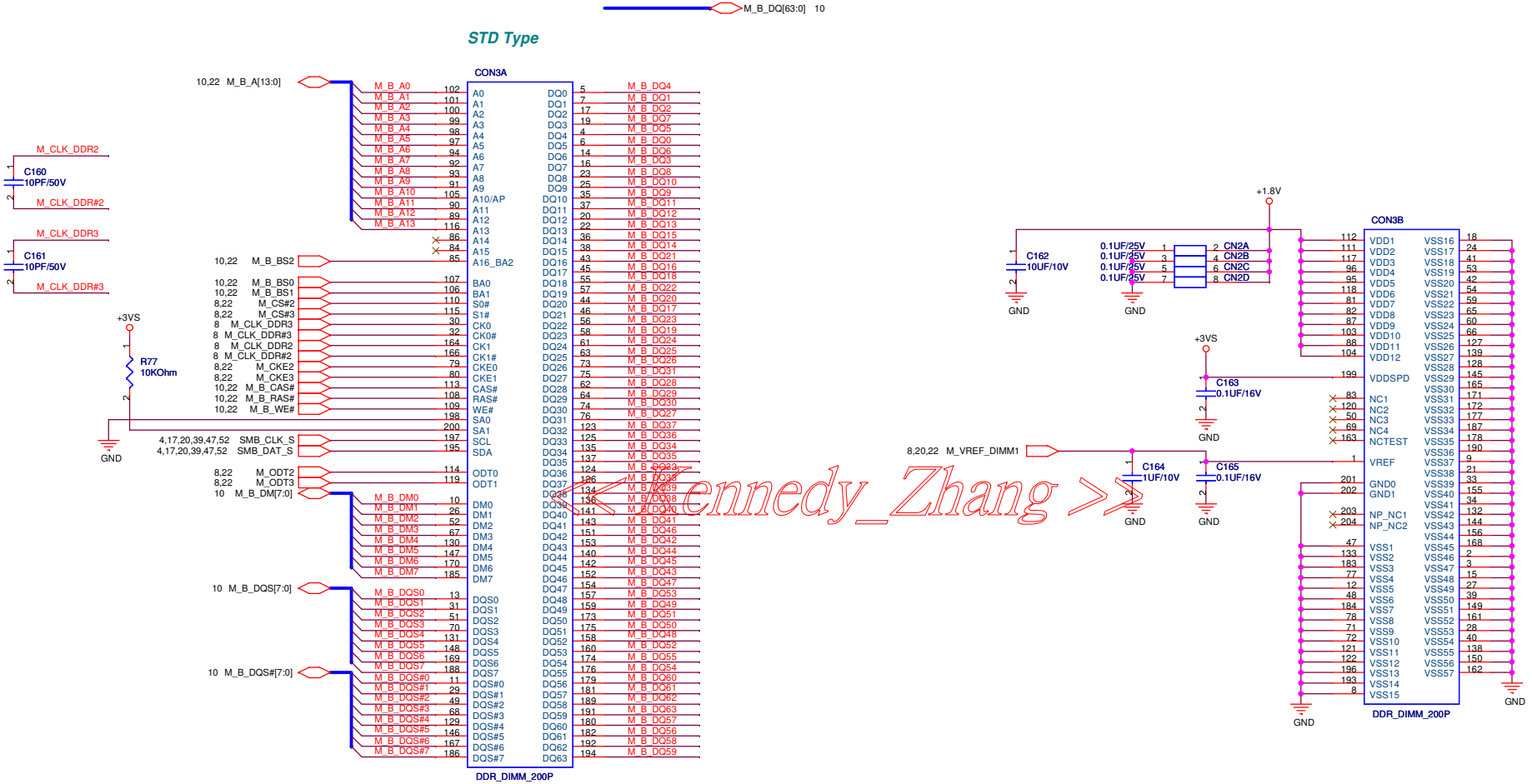
| ASUSTeK COMPUTER INC. | Title : DDR2 SO-DIMM0 | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 20 of 96 | |



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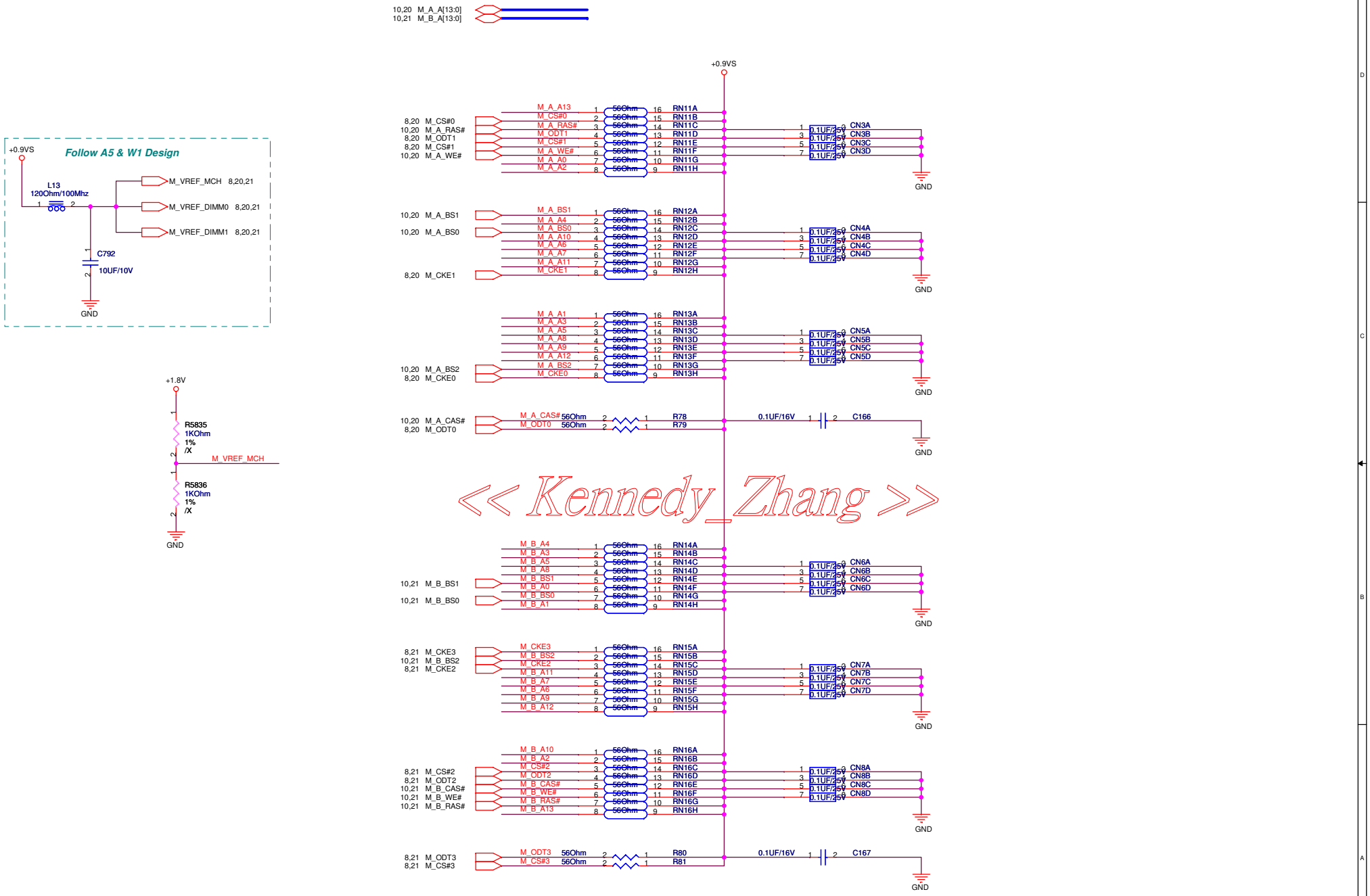
| ASUSTeK COMPUTER INC. NB1 | Title : DDR2 SO-DIMM1 | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 21 of 96 | |

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| ASUSTeK COMPUTER INC. NB1 | Title : DDR2 TERMINATION | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 22 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 23 of 96

<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 24 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 25 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

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|---|---|---|
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| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 26 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
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| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 27 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

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|---|---|---|
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| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 28 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

| | | |
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| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 29 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

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|---|---|---|
| Title <Title> | | |
| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 30 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

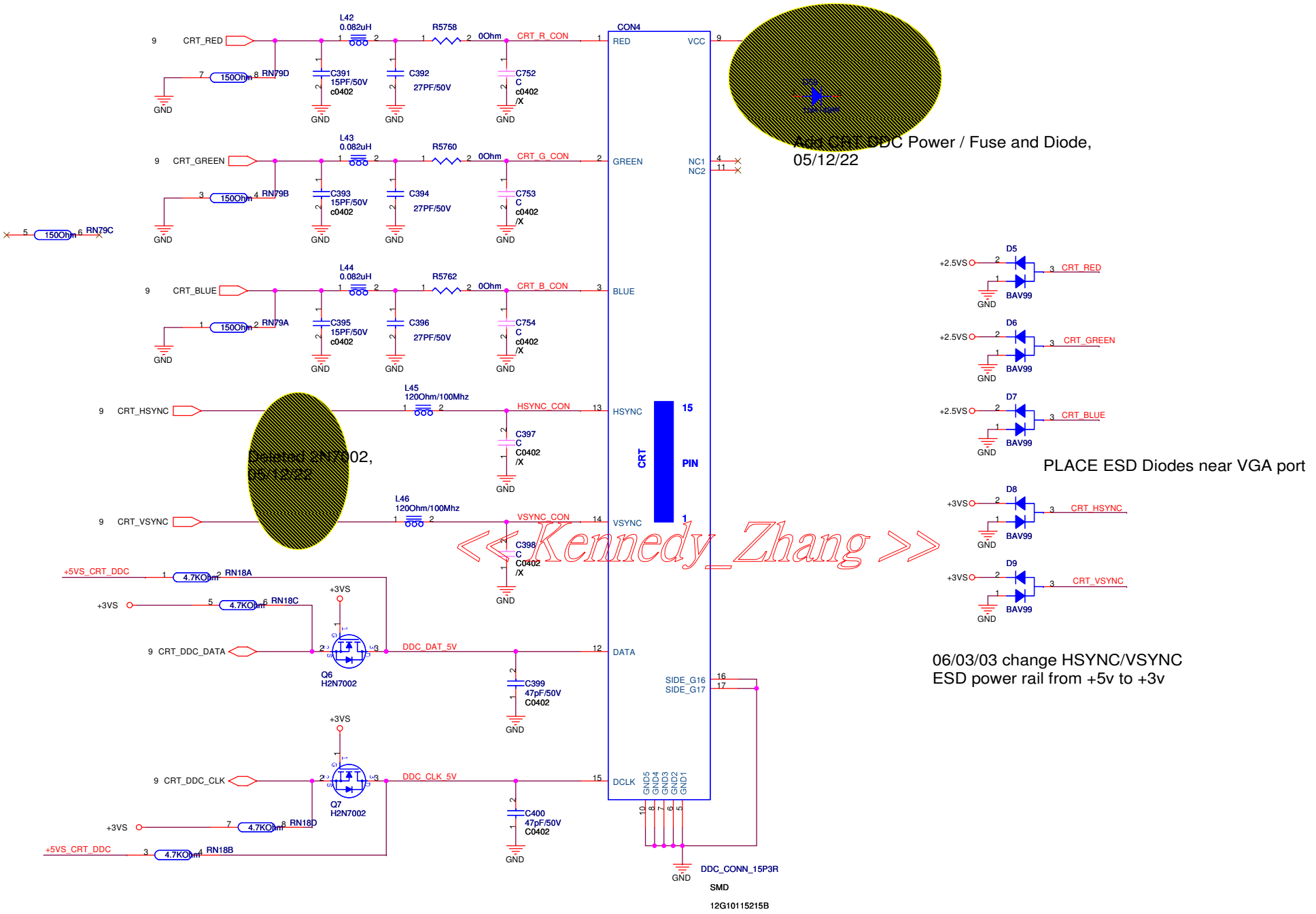
Title :

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 31 of 96




Add CRT DDC Power / Fuse and Diode, 05/12/22

Delated 2N7002, 05/12/22

<<Kennedy_Zhang >>




PLACE ESD Diodes near VGA port

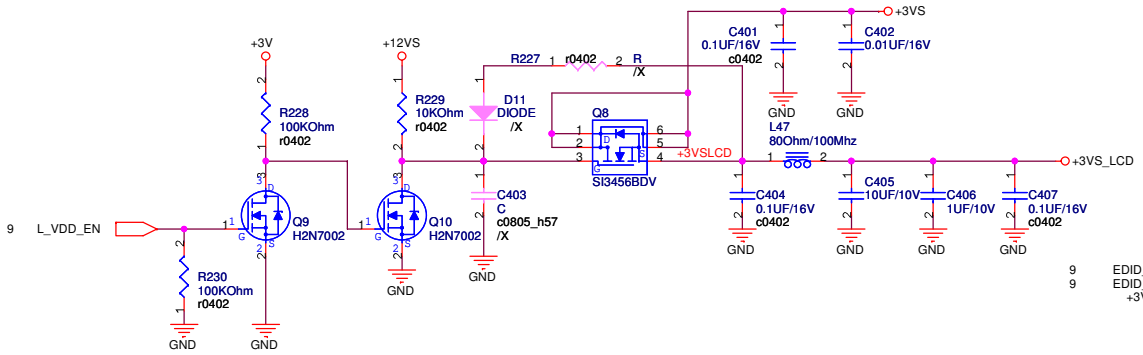
06/03/03 change HSYNC/VSYNC
ESD power rail from +5v to +3v

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CRT | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 32 of 96 | |

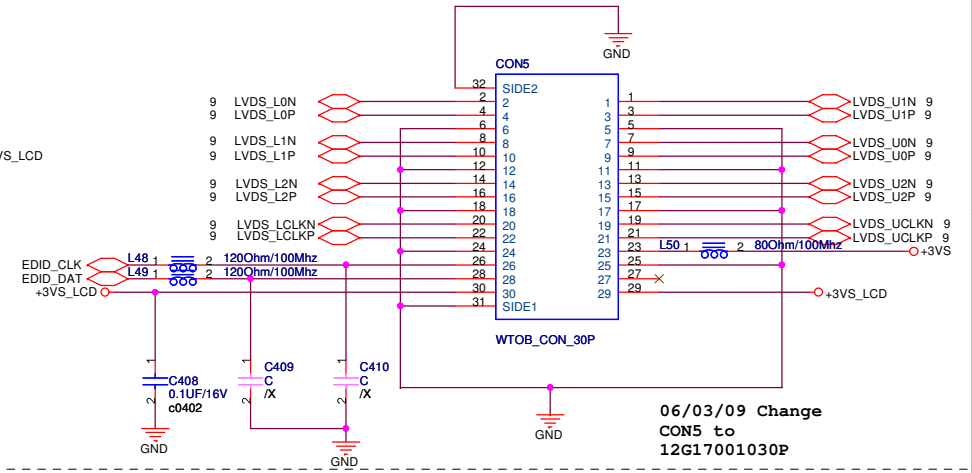
# LCD Backlight Control

## LCD Power




*Cable Requirement:*
*Impedence: 100 ohm +/- 10%*
*Length Mismatch <= 10 mils*
*Twisted Pair(Not Ribbon)*
*Maximum Length <= 16"*

# LCD LVDS Interface

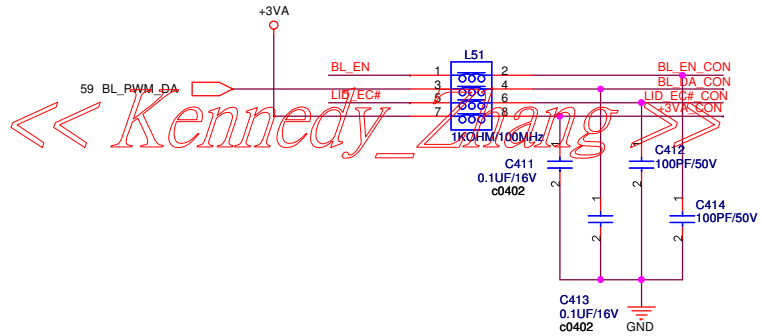



06/03/09 Change
CON5 to
12G17001030P

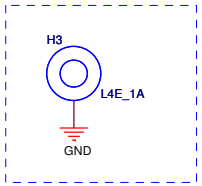
## *INVERTER Interface/Speaker CONN.*

**BIOS**

**BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.**

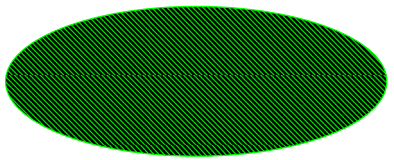


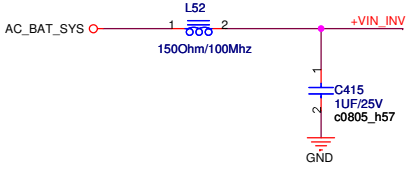


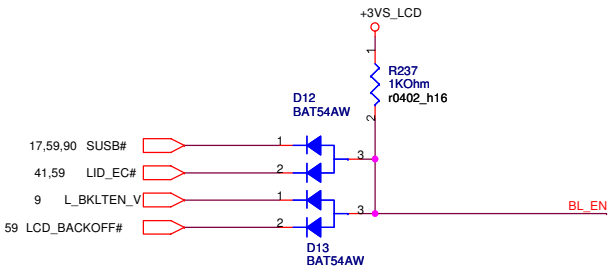



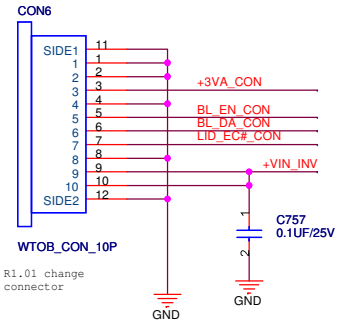

LCD NUT(3.0mm) *1

05/12/30 refer Z96J R1.01 to
remove HW pannel ID setting






R1.01 change
connector

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : LVDS & INVERTER | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 33 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

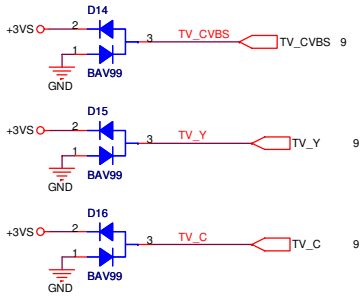
ASUSTeK COMPUTER INC

Engineer: Mike Lee

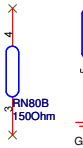
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

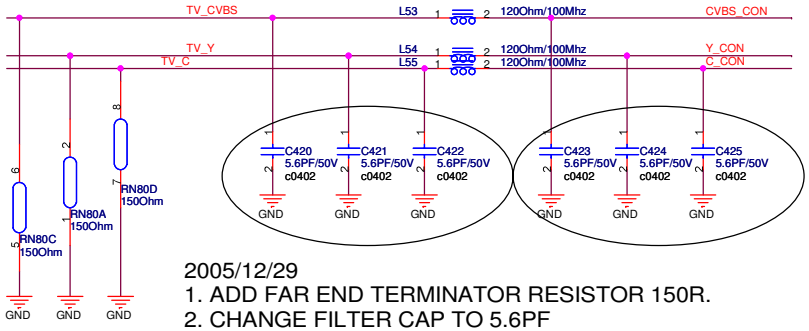
Date: Monday, September 18, 2006 Sheet 34 of 96

# TV OUT

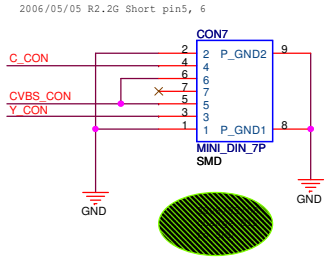


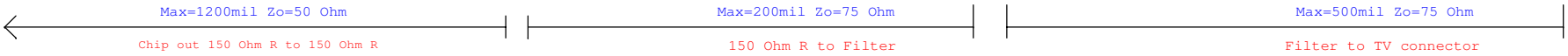

PLACE ESD
Diodes near
TV port




2005/12/29
1. ADD FAR END TERMINATOR RESISTOR 150R.
2. CHANGE FILTER CAP TO 5.6PF




<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : TV OUT & DVI CON. | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 35 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

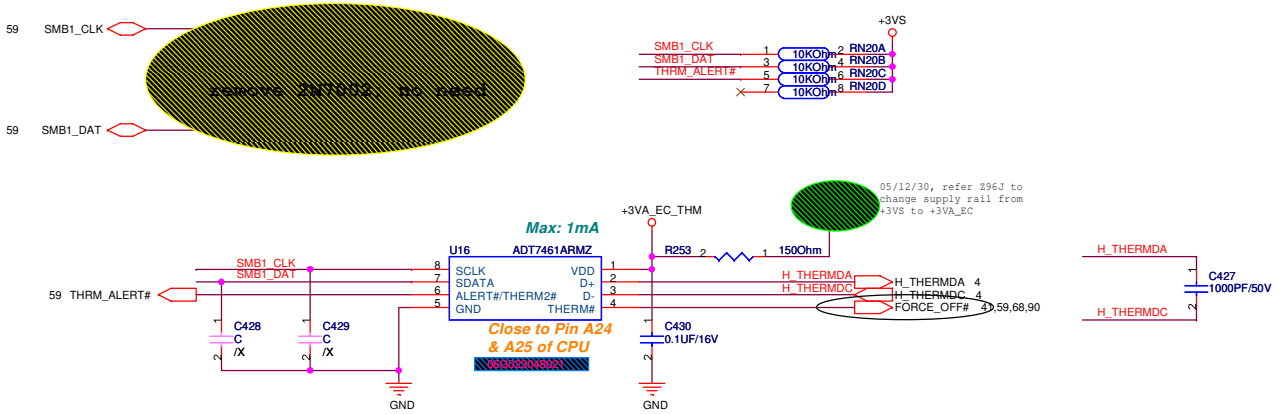
ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 36 of 96

## Thermal Sensor

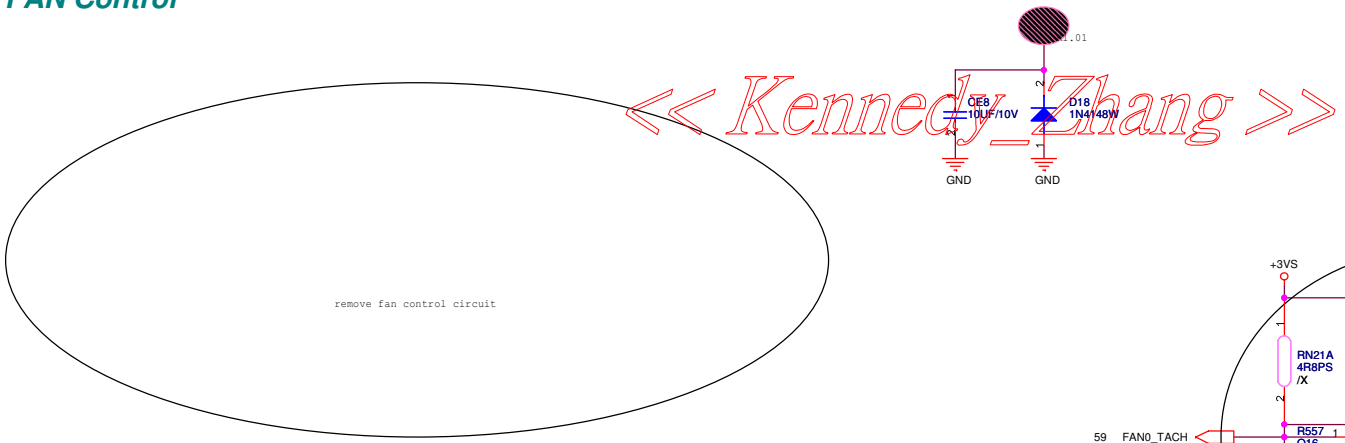


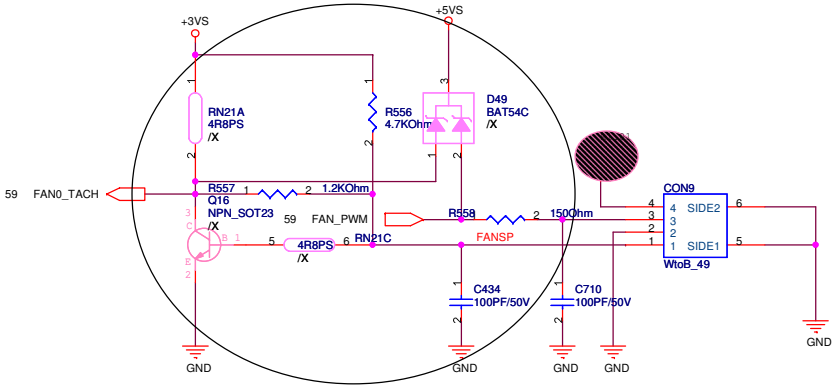

*Route H_THERMDA and H_THERMDC on the same layer*

*----------OTHER SIGNALS*
*15 mils*
*==========GND*
*10 mils*
*==========H_THERMDA(10 mils)*
*10 mils*
*==========H_THERMDC(10 mils)*
*10 mils*
*==========GND*
*15 mils*
*----------OTHER SIGNALS*

*Avoid FSB,Power*

## DC FAN Control




*CPU FAN will be forced on:*
*1) Thermal Sensor Over-temperture*
*2) WATCHDOG asserted by EC*

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : THER SENSOR & FAN | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 37 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

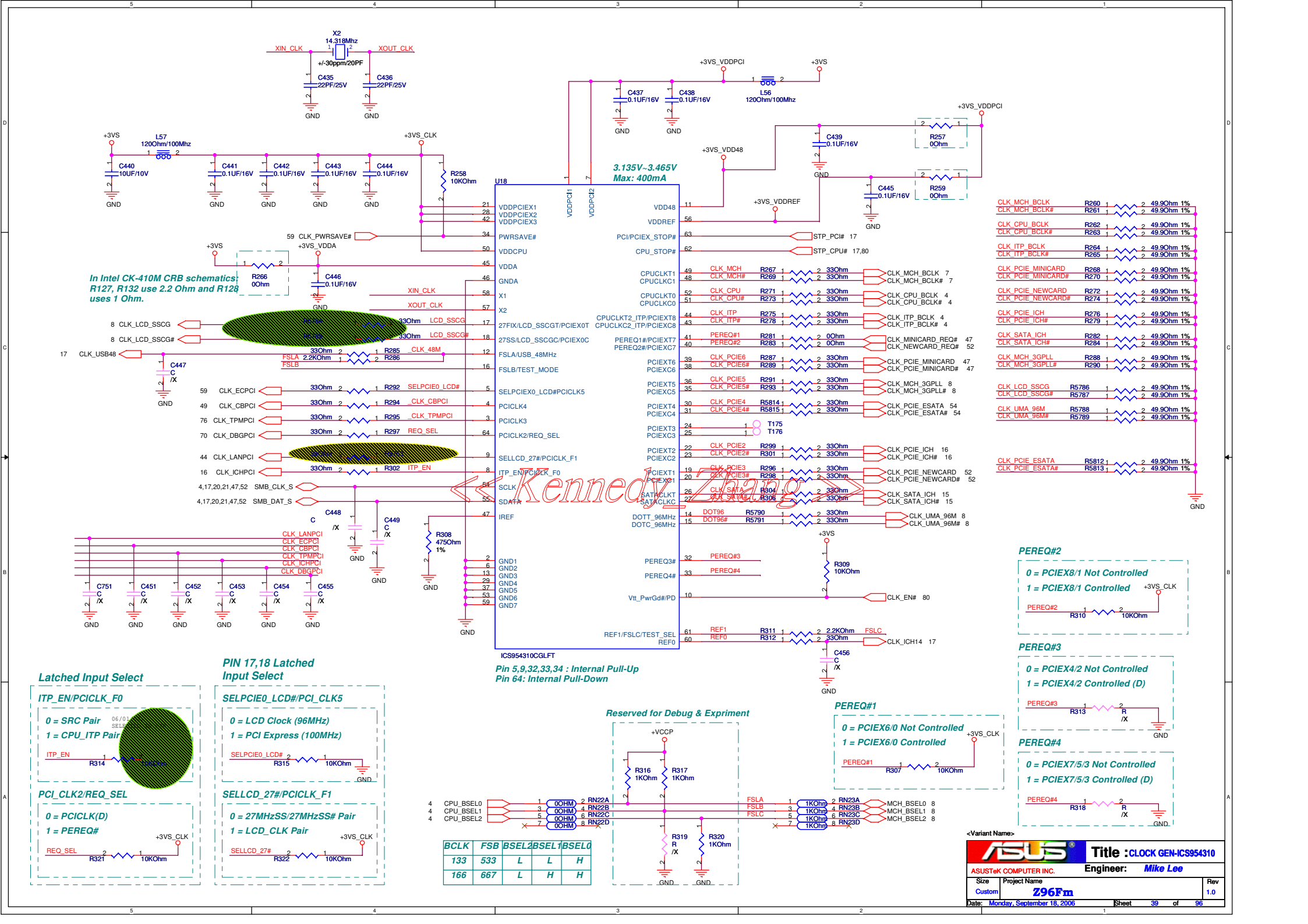
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | | 1.0 |

Date: Monday, September 18, 2006 Sheet 38 of 96


U18
ICS954310CGLFT
3.135V~3.465V
Max: 400mA
In Intel CK-410M CRB schematics: R127, R132 use 2.2 Ohm and R128 uses 1 Ohm.
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
Kennedy Zhang
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
PIN 17,18 Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
Reserved for Debug & Expriment
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
<Variant Name>
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
Sheet 39 of 96

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<Variant Name>

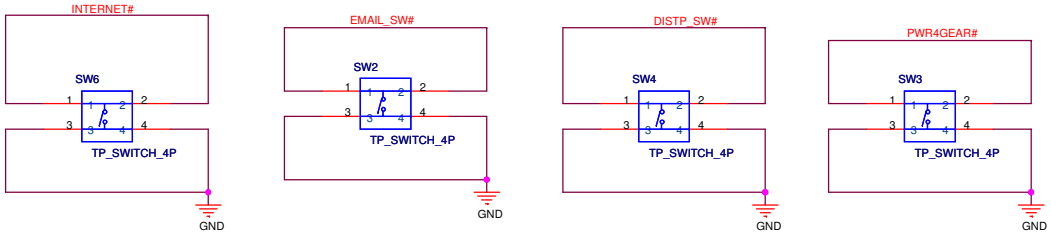
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer:

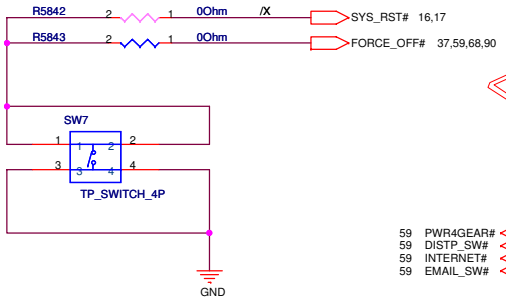
| Size | Project Name | Rev |
|---|---|---|
| Custom | | 1.0 |

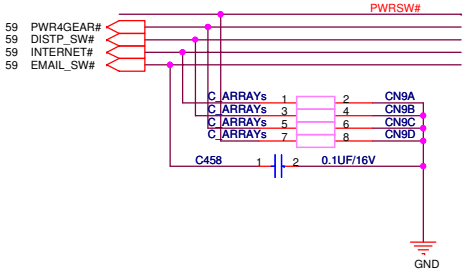
Date: Monday, September 18, 2006 Sheet 40 of 96

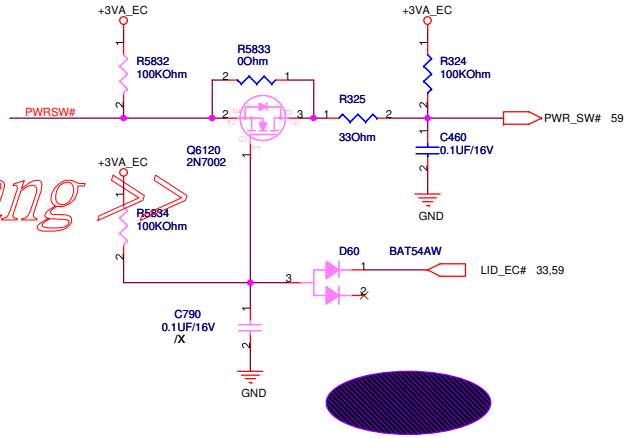



06/03/09 Change
SW1-4, SW6-7 to
12G09103004P

## SHUT_DOWN# / RESET#



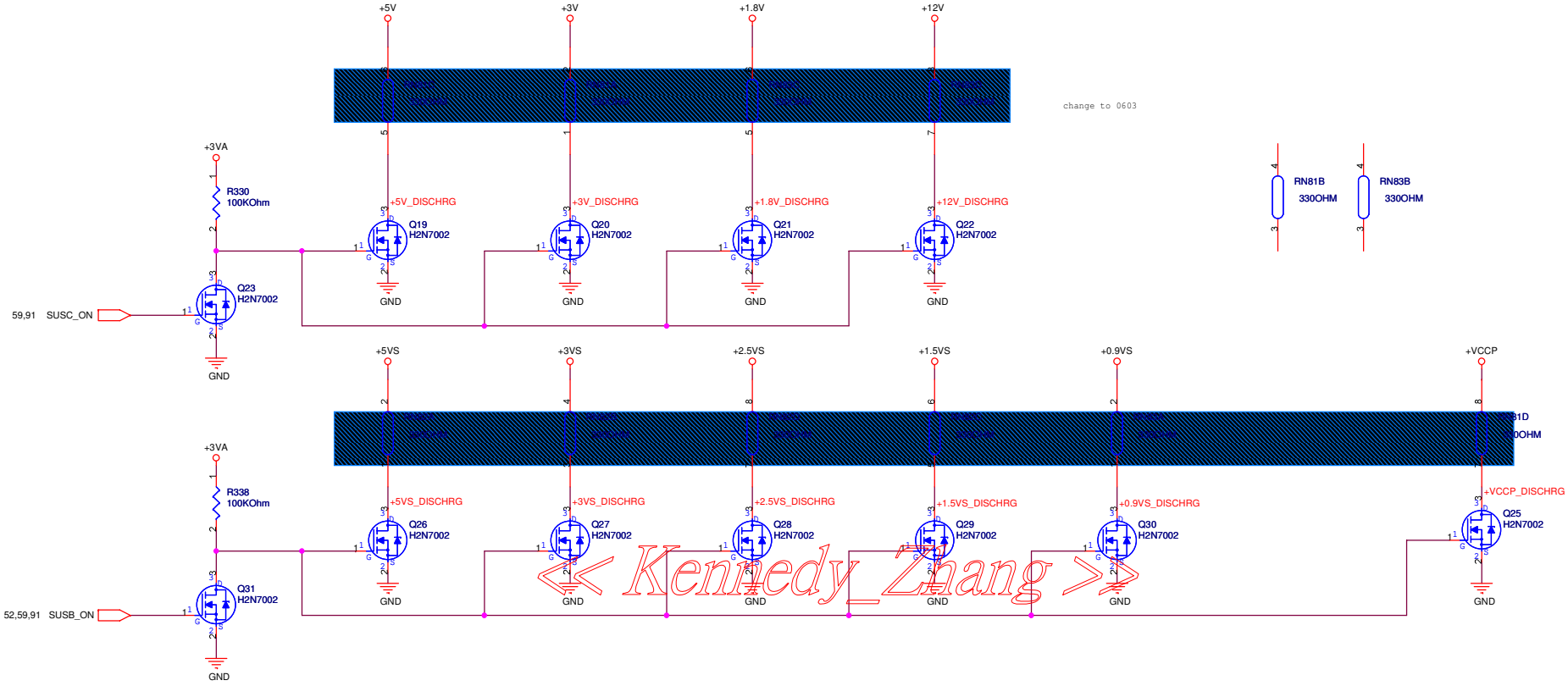






<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Power on & Res Freq | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 41 of 96 | |




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : DISCHARGE & EMI CAP | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 42 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

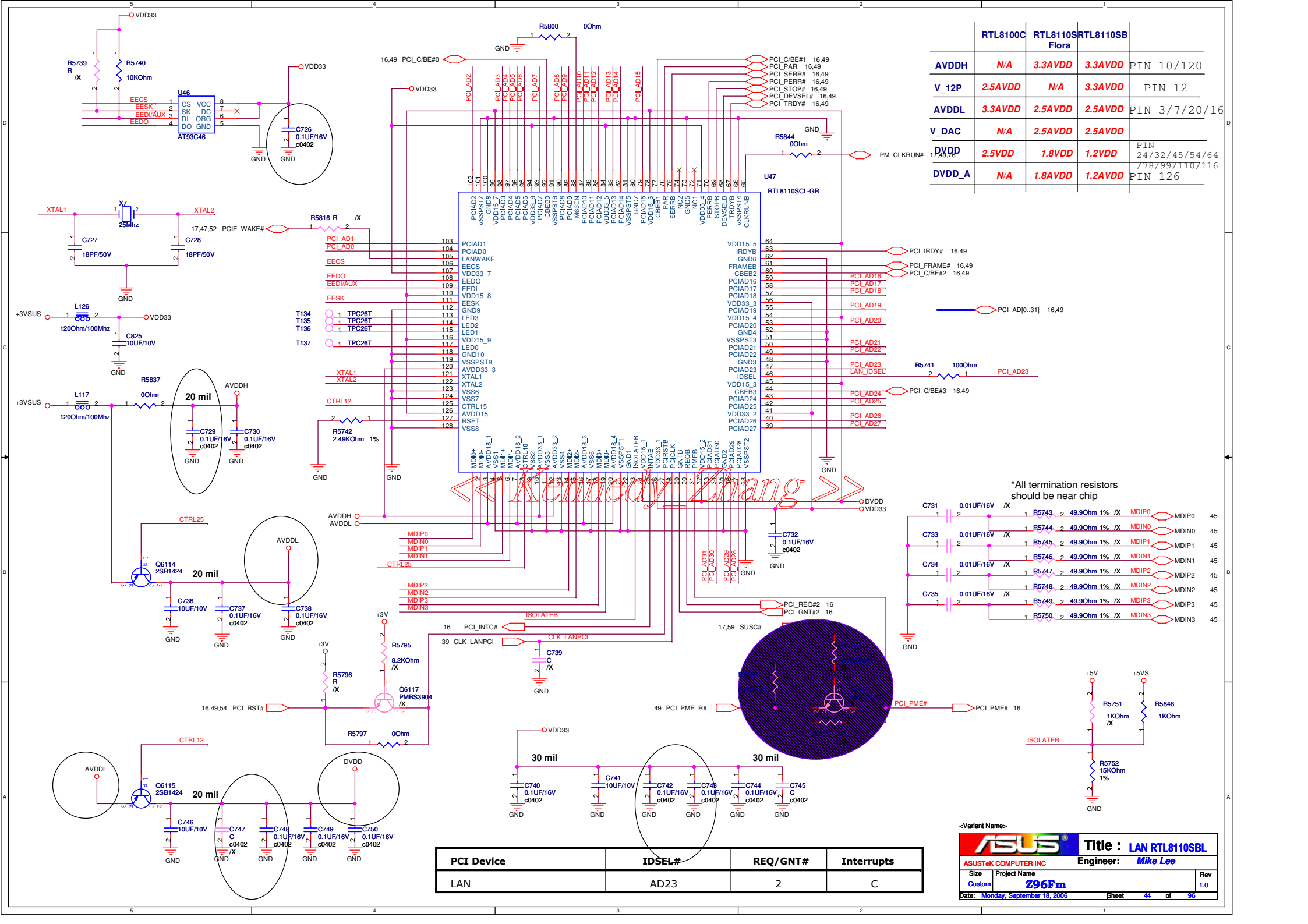
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

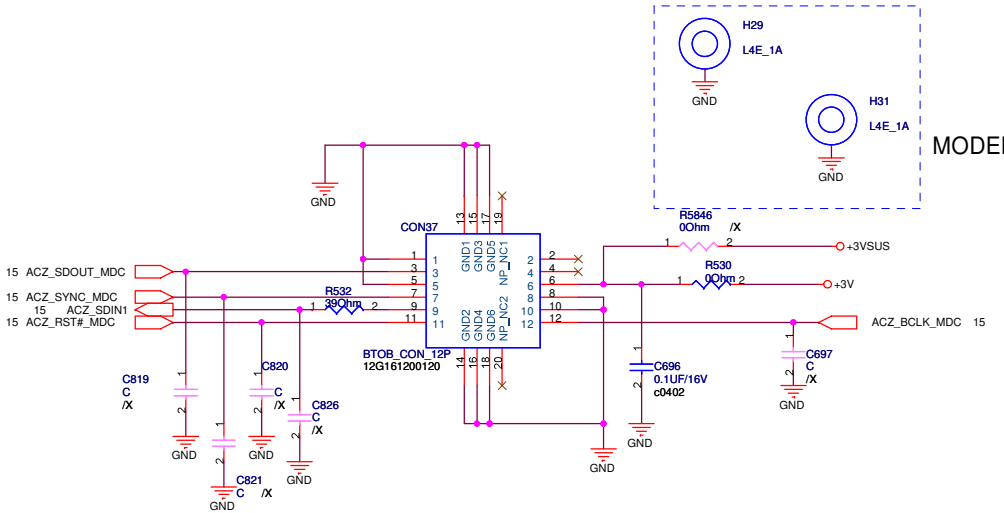
Date: Monday, September 18, 2006 Sheet 43 of 96

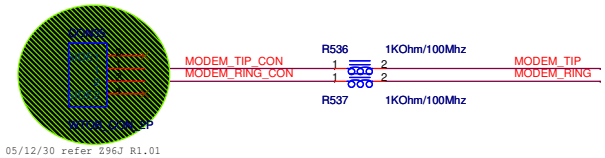


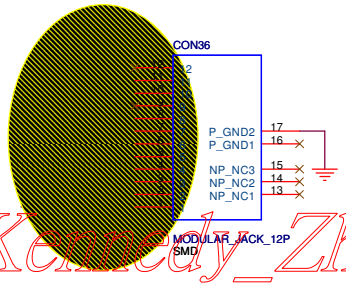

| | RTL8100C | RTL8110S Flora | RTL8110SB | |
|---|---|---|---|---|
| AVDDH | N/A | 3.3AVDD | 3.3AVDD | PIN 10/120 |
| V_12P | 2.5AVDD | N/A | 3.3AVDD | PIN 12 |
| AVDDL | 3.3AVDD | 2.5AVDD | 2.5AVDD | PIN 3/7/20/16 |
| V_DAC | N/A | 2.5AVDD | 2.5AVDD | |
| DVDD | 2.5VDD | 1.8VDD | 1.2VDD | PIN 24/32/45/54/64 77/89/99/110/116 |
| DVDD_A | N/A | 1.8AVDD | 1.2AVDD | PIN 126 |

| PCI Device | IDSEL# | REQ/GNT# | Interrupts |
|---|---|---|---|
| LAN | AD23 | 2 | C |

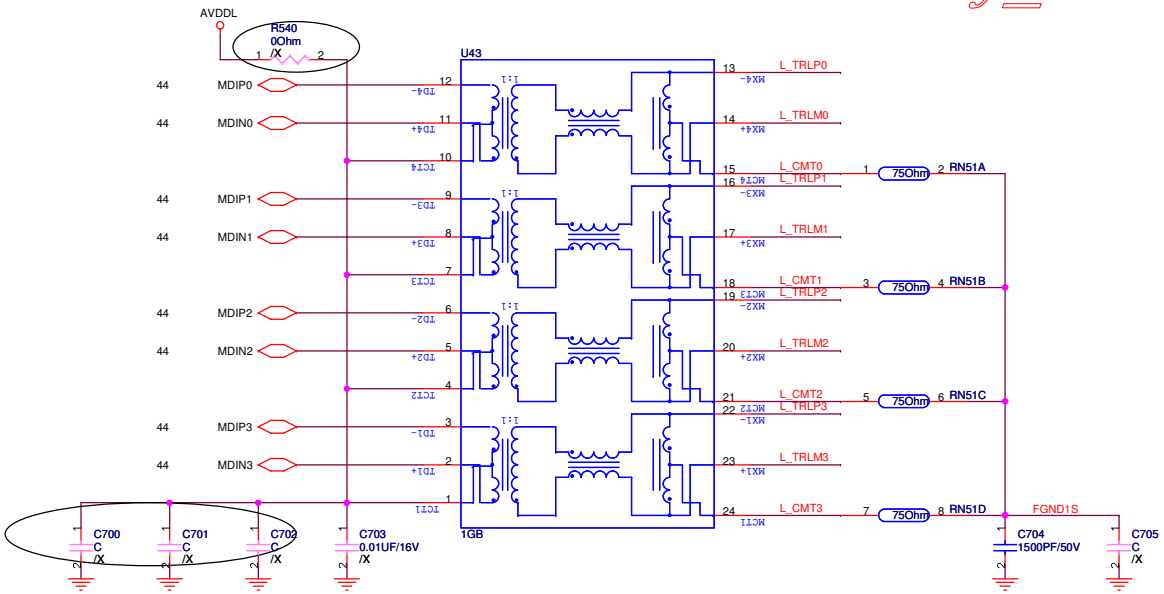
## MDC CONN.

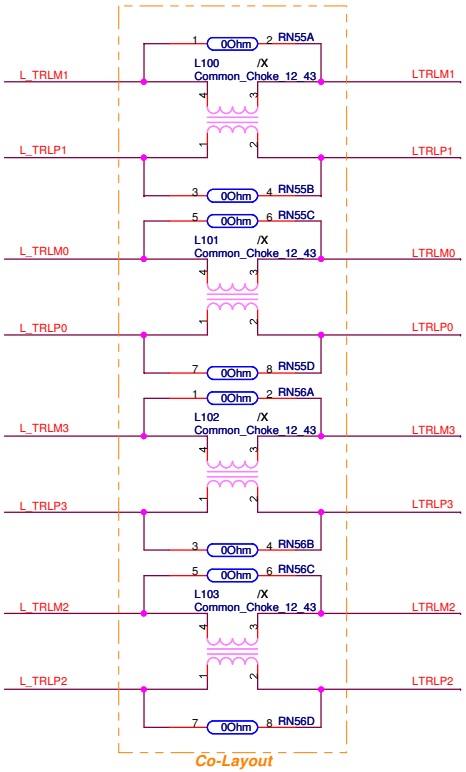





<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : RJ45&RJ11 | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 45 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

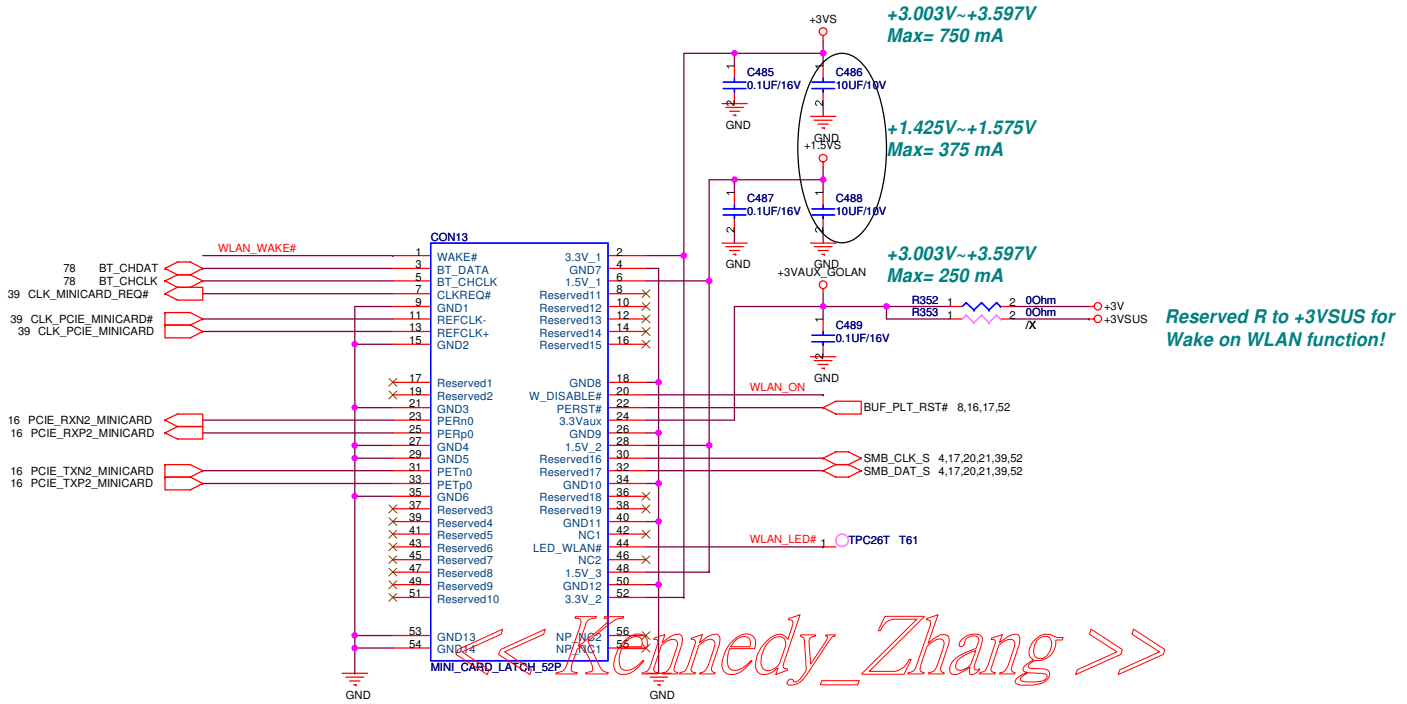
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

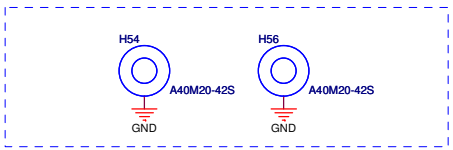
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 46 of 96

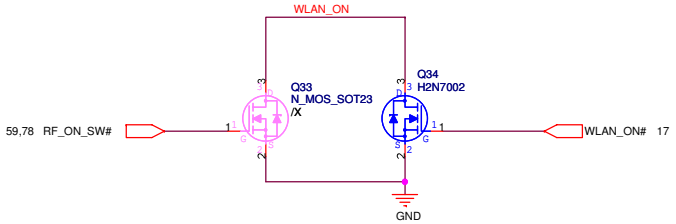


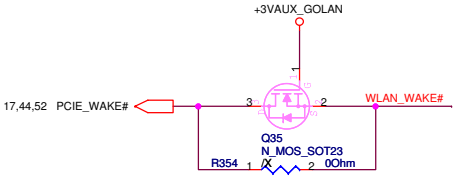



2006/03/31




MINI CARD NUT(4.2mm) *2




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. | Title : MINICARD | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 47 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

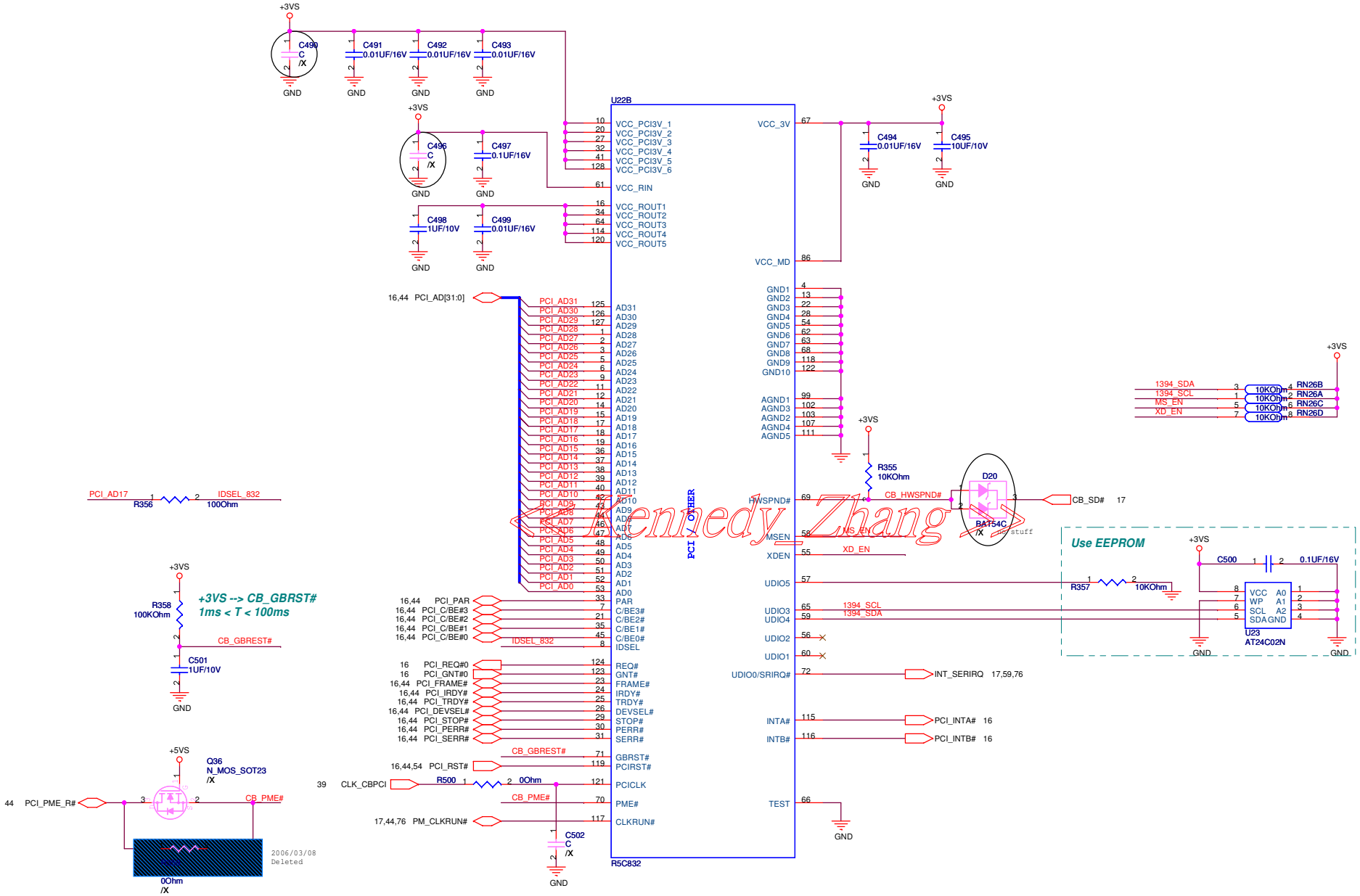
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 48 of 96




| PCI Device | IDSEL# | REQ/GNT# | Interrupts |
|---|---|---|---|
| | | | |
| CARD READER | AD17 | 0 | B |
| 1394 | AD17 | 0 | A |

<Variant Name>

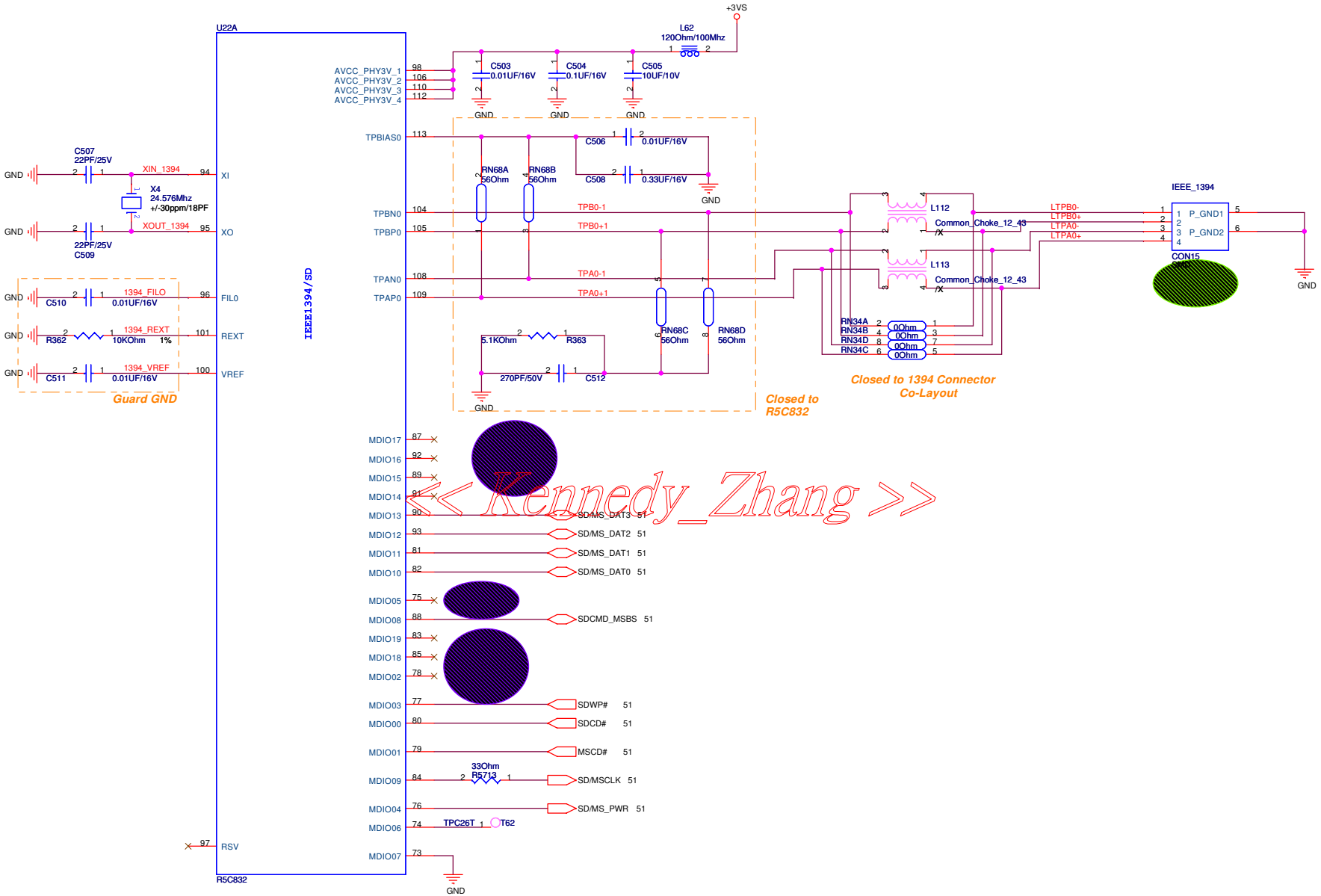
Title : CARD1394-R5C832(1)

ASUSTeK COMPUTER INC. MB6

Engineer: Mike Lee

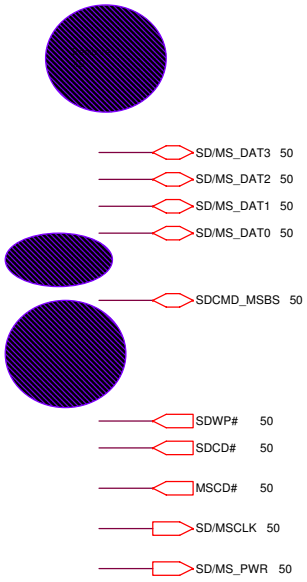
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

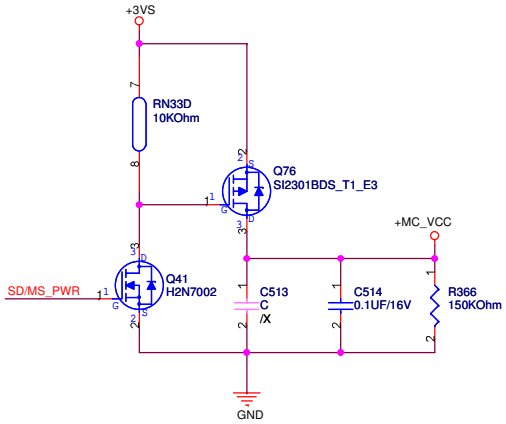
Date: Monday, September 18, 2006 Sheet 49 of 96



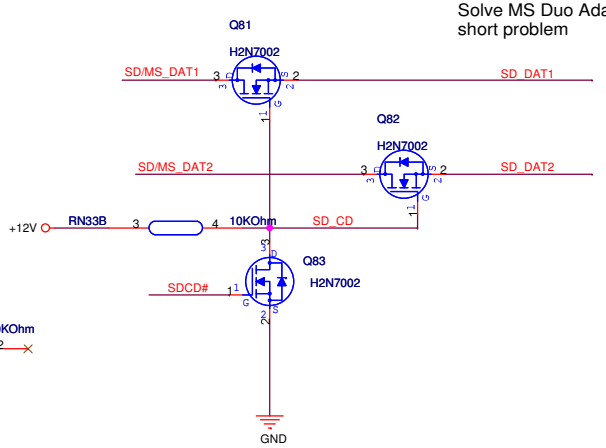

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. MB6 | Title : CARD1394-R5C832(2) | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 50 of 96 | |



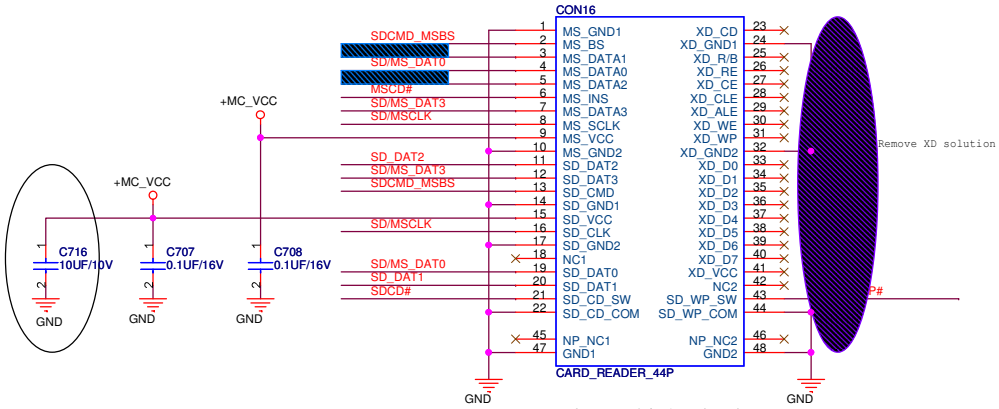




Solve MS Duo Adaptor short problem

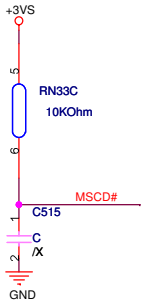




<< Kennedy_Zhang >>

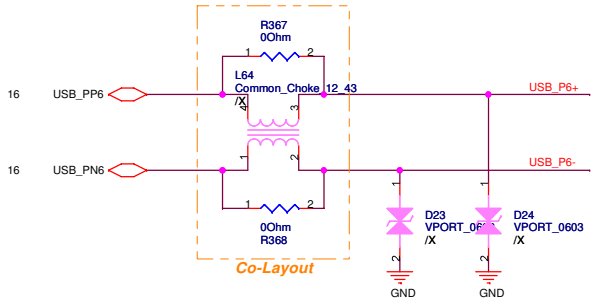


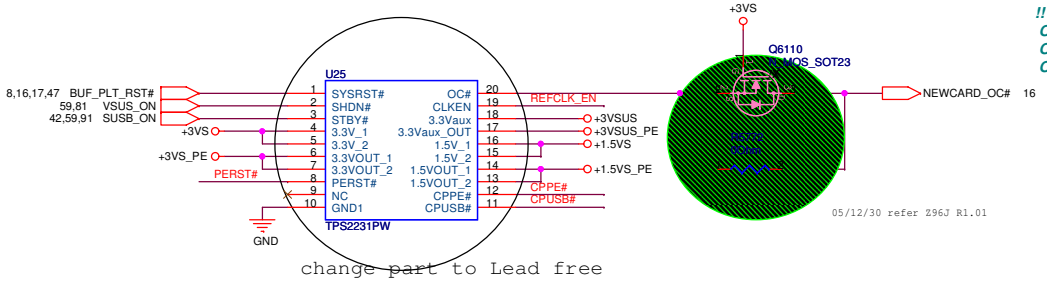

change to 4 in 1 card reader



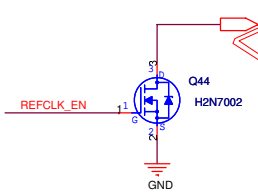

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : 4 in 1 CARD READER | |
| | Engineer: Mike Lee | |
| Size: A3 | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 51 of 96 | |



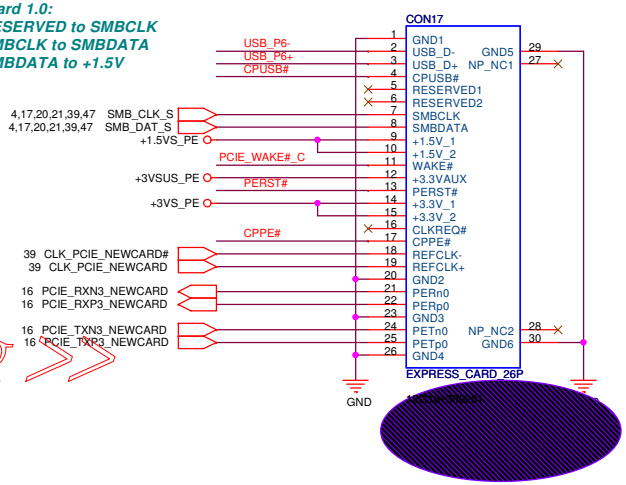

change part to Lead free

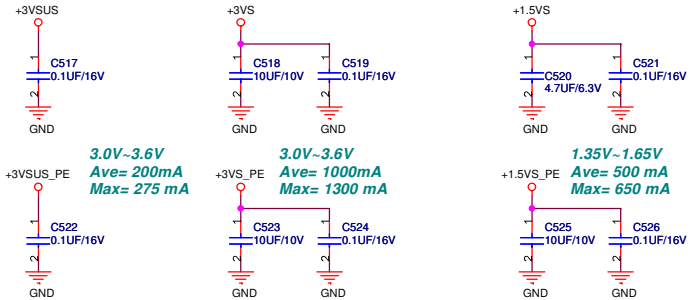


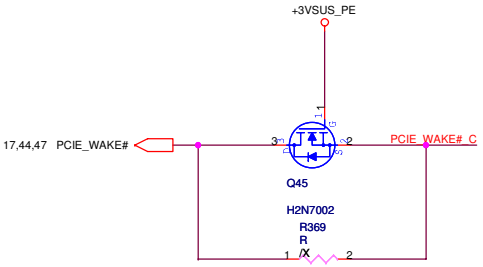



**!! ExpressCard Standard 1.0:**
**Change Pin7 from RESERVED to SMBCLK**
**Change Pin8 from SMBCLK to SMBDATA**
**Change Pin9 from SMBDATA to +1.5V**

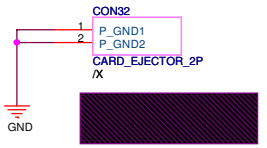
## NewCard Header




## NewCard Ejecter



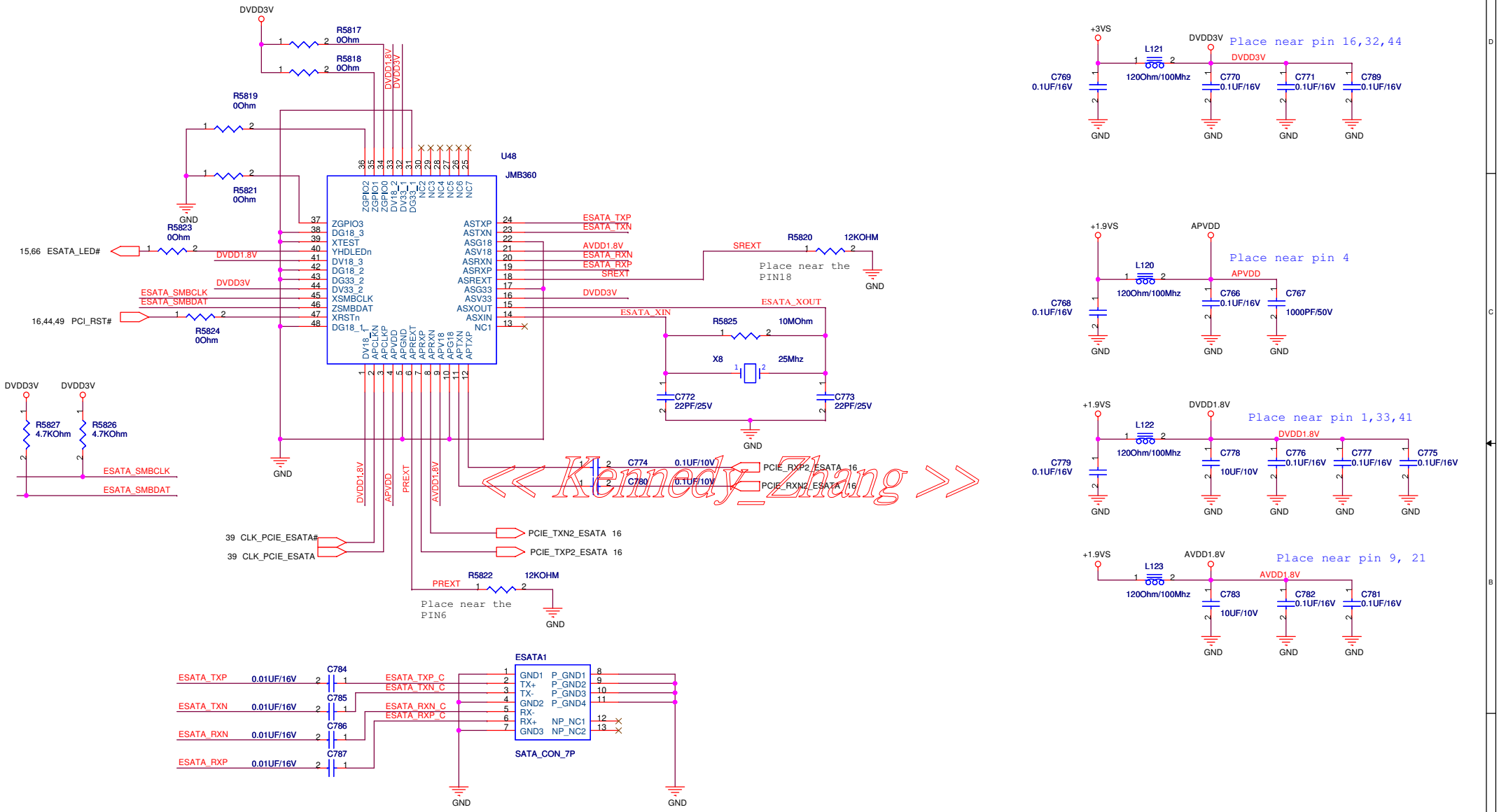

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : NEWCARD | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 52 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : <Title> | |
| | Engineer: Mike Lee | |
| Size: A | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 53 of 96 | |


















<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : ESATA | |
| | Engineer: Mike Lee | |
| Size: A3 | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 54 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

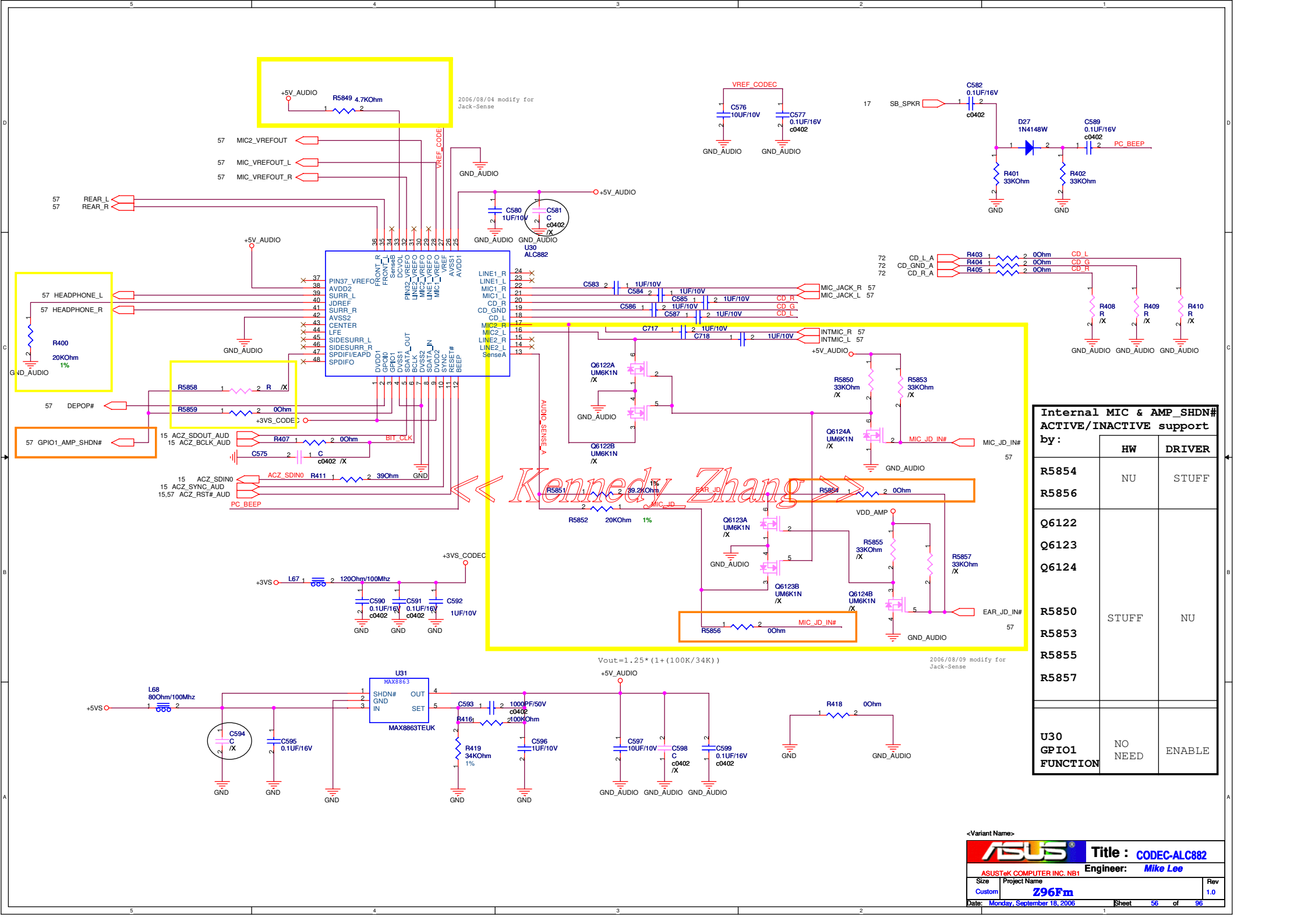
Title : BLANK

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 55 of 96






| Internal MIC & AMP_SHDN# ACTIVE/INACTIVE support by: | HW | DRIVER |
|---|---|---|
| R5854<br>R5856 | NU | STUFF |
| Q6122<br>Q6123<br>Q6124<br>R5850<br>R5853<br>R5855<br>R5857 | STUFF | NU |
| U30 GPIO1 FUNCTION | NO NEED | ENABLE |

<Variant Name>

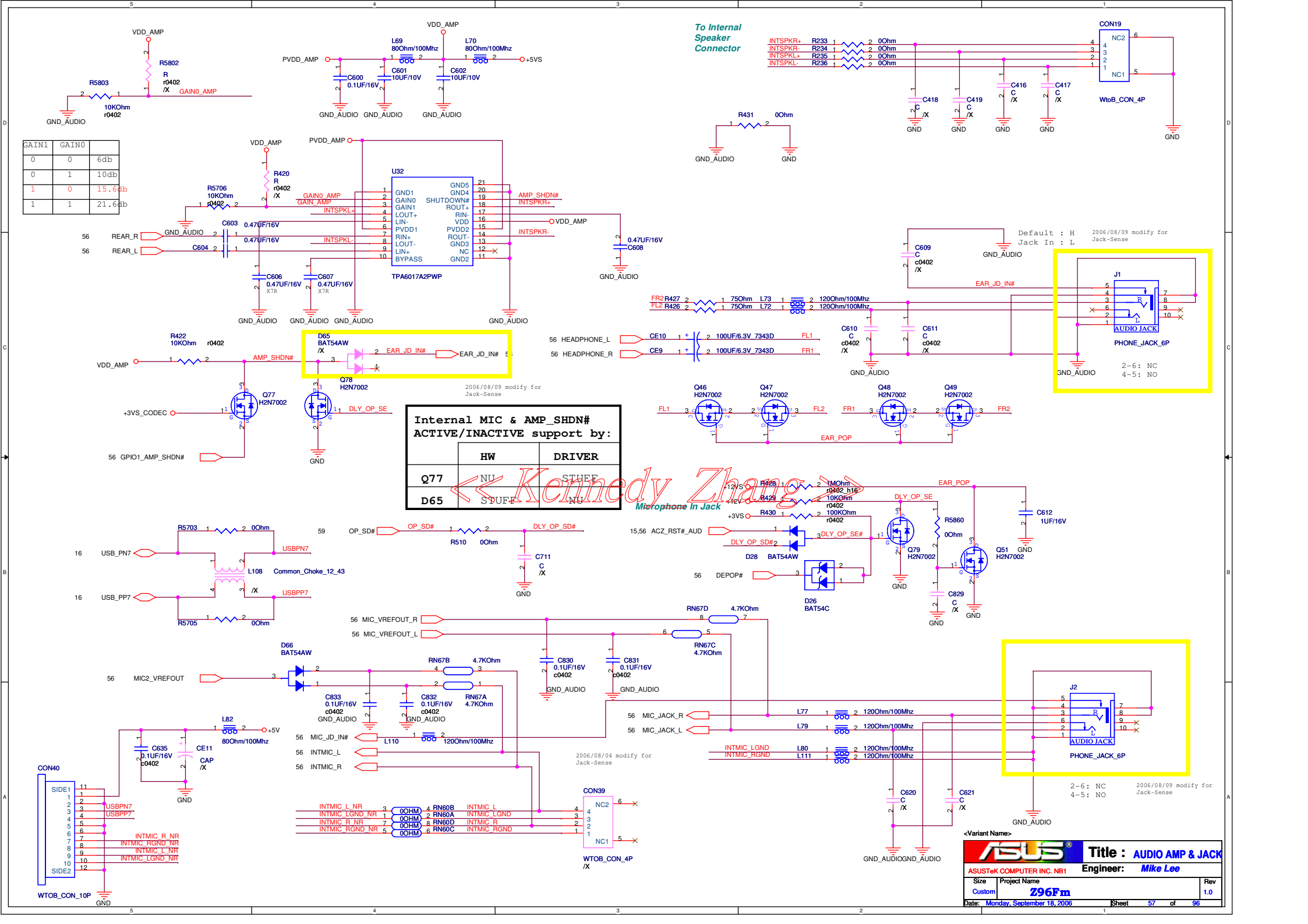
ASUSTeK COMPUTER INC. NB1

Title : CODEC-ALC882

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 56 of 96




| GAIN1 | GAIN0 | |
|---|---|---|
| 0 | 0 | 6db |
| 0 | 1 | 10db |
| 1 | 0 | 15.6db |
| 1 | 1 | 21.6db |

<< Kennedy_Zhang >>

<Variant Name>

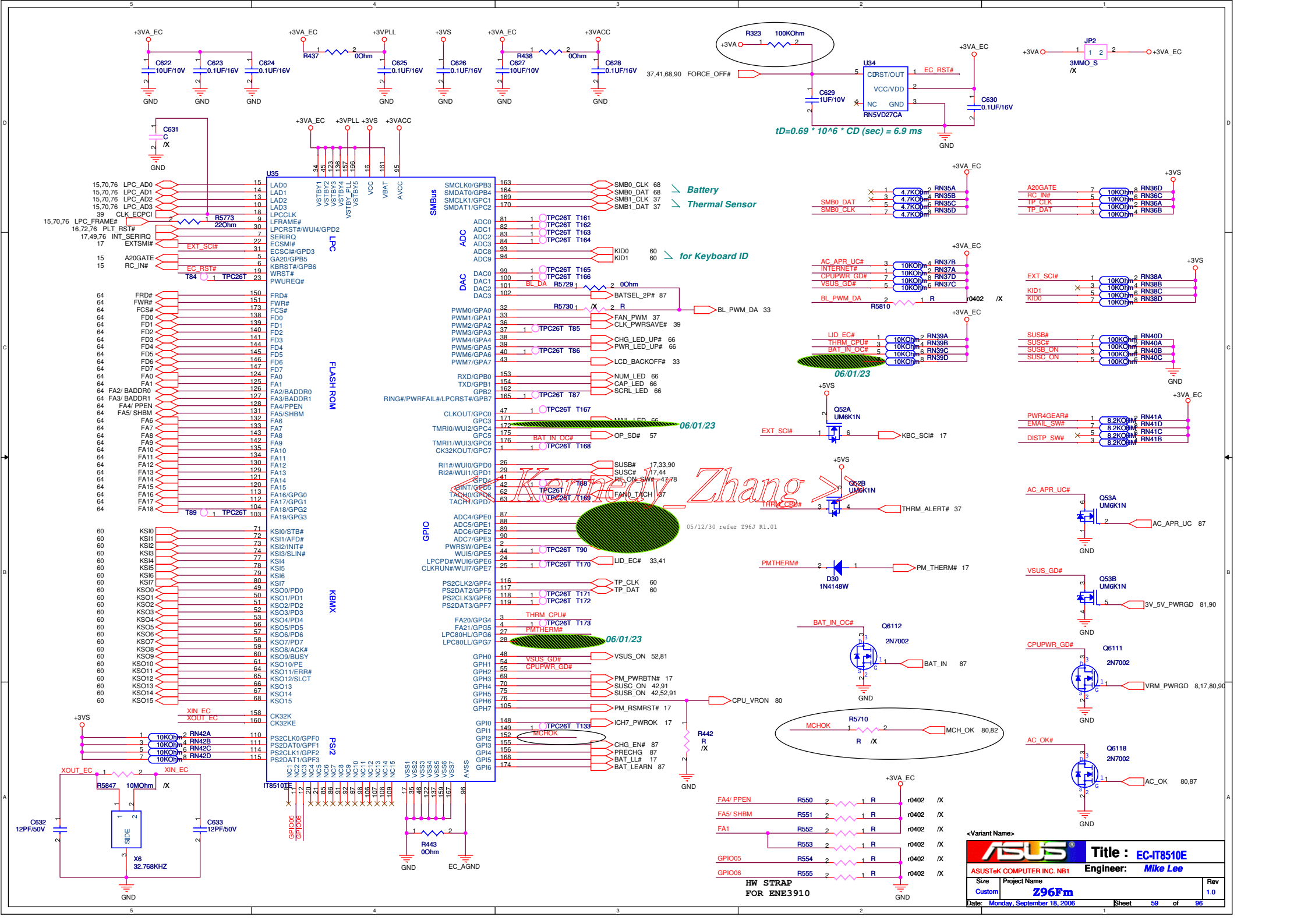
Title : Schematic page name

ASUSTeK COMPUTER INC

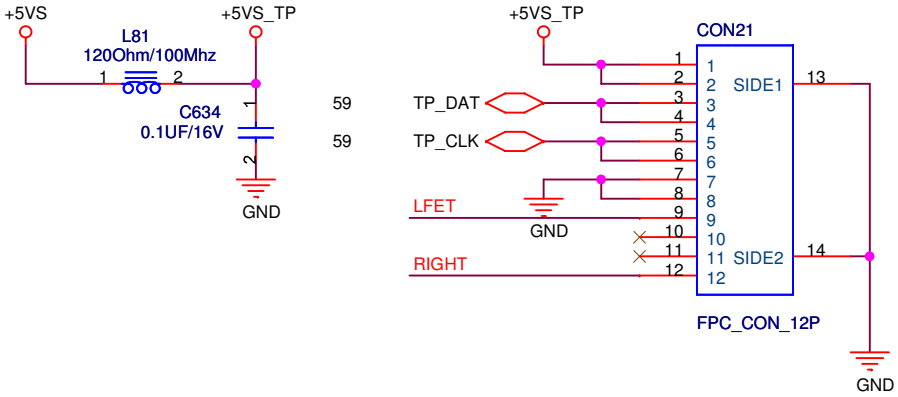
Engineer: Mike Lee

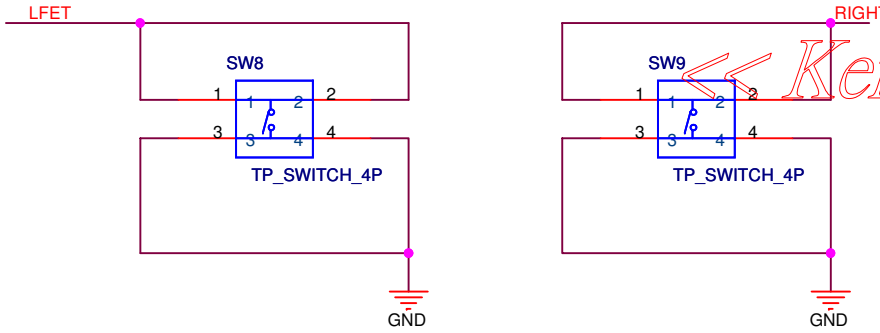
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 58 of 96

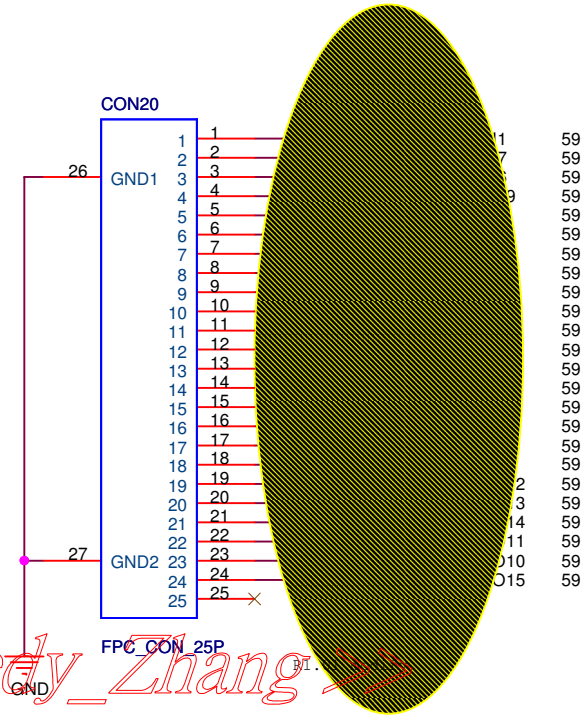

U35
IT8510E
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
for Keyboard ID
06/01/23
05/12/30 refer Z96J R1.01
Kennedy Zhang
HW STRAP
FOR ENE3910
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Mike Lee
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
Sheet 59 of 96

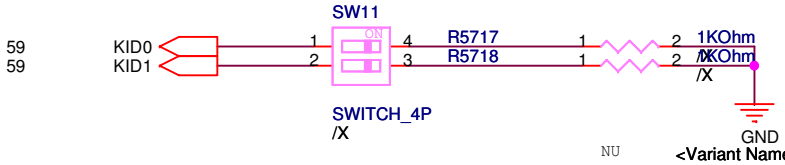
## For Touch-Pad



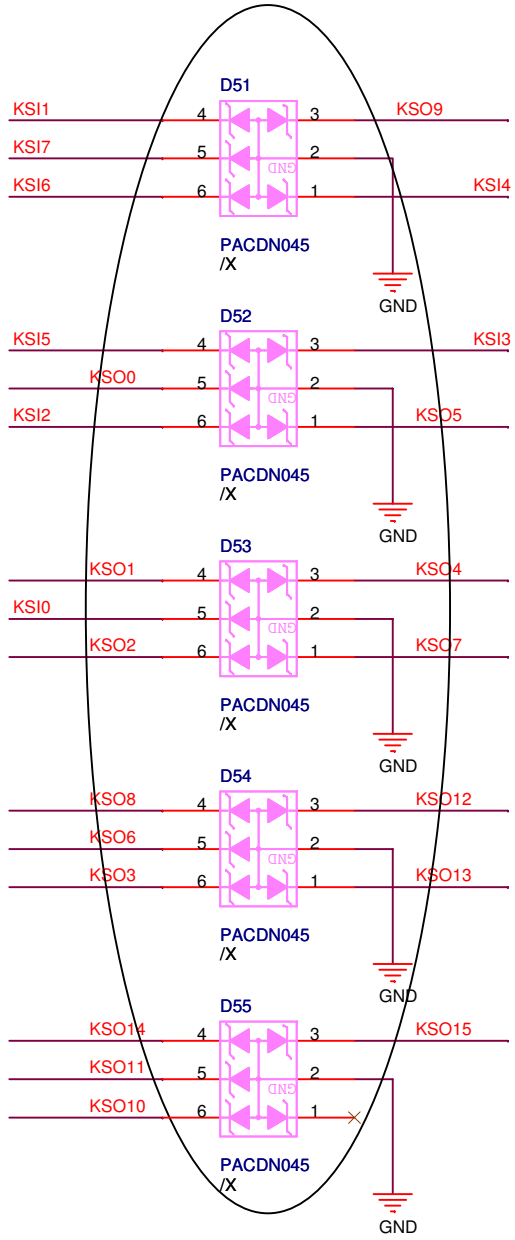

## For Keyboard






05/12/29 ESD DIODE PIN SWAPPED



<< Kennedy_Zhang >>

<Variant Name>

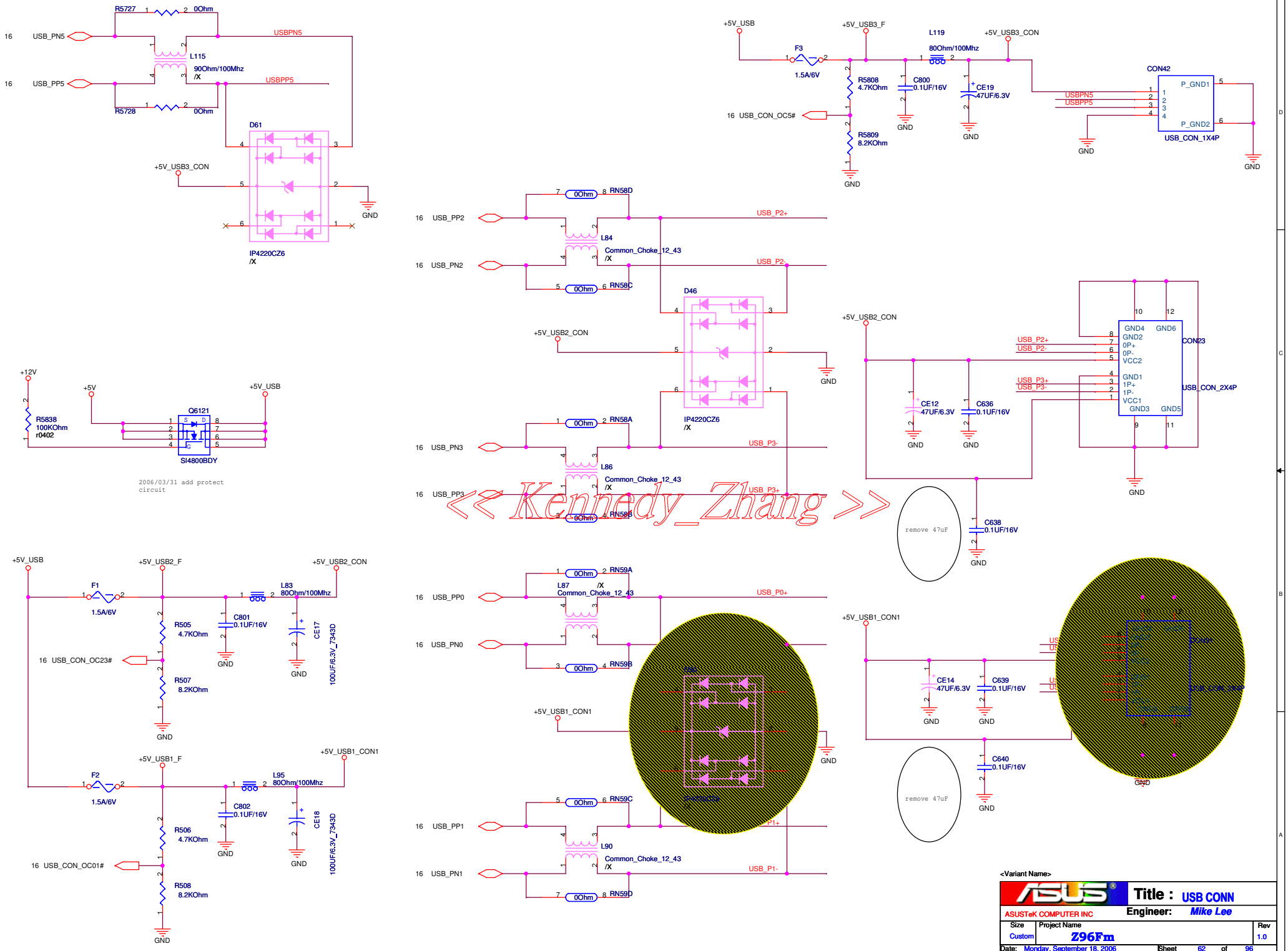
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 61 of 96




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : USB CONN | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 62 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 63 of 96

# ISA ROM

## EC Hardware Strapping

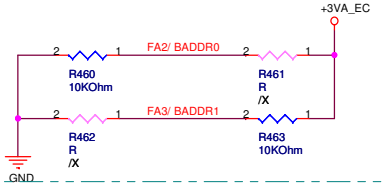
### FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

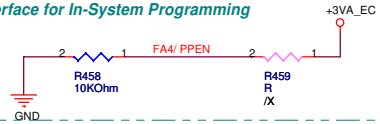



Note: Sampled at VSTBY Power Up Reset

### FA4/ PPEN

0: Normal

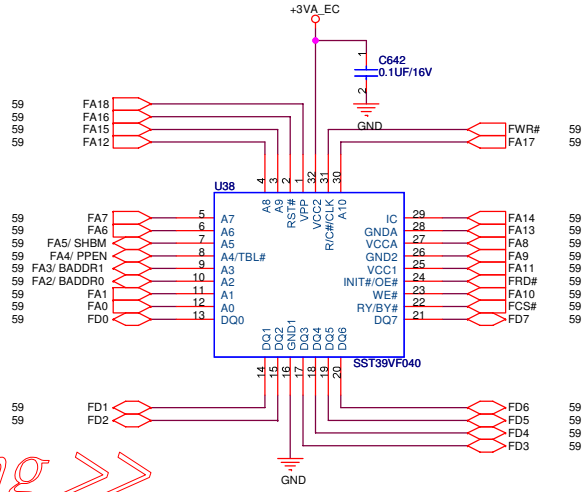
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming




### FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : ISA ROM | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 64 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

ASUSTeK COMPUTER INC

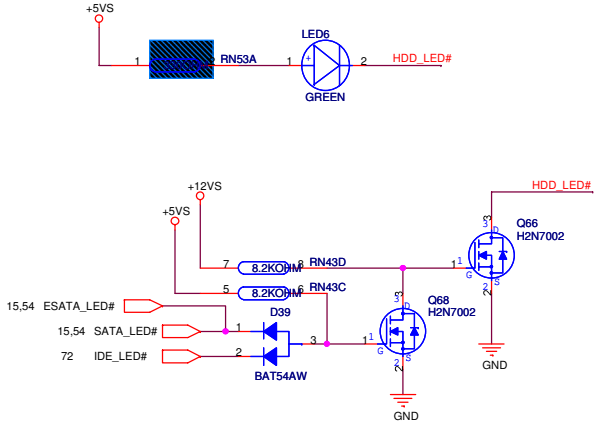
Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

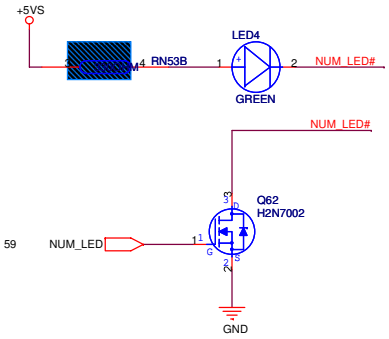
Date: Monday, September 18, 2006 Sheet 65 of 96

# For LED

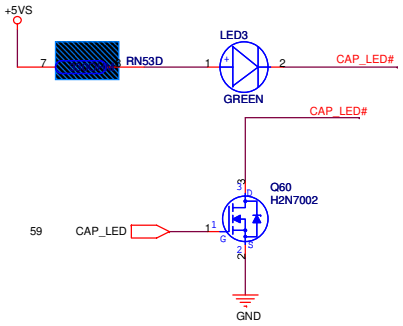
## For SATA/IDE LED



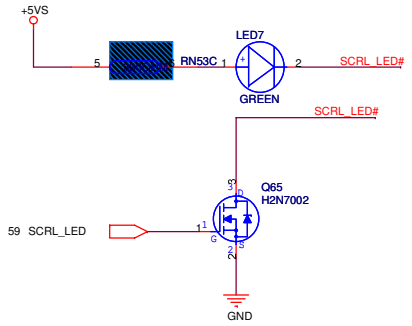

## for Num Lock



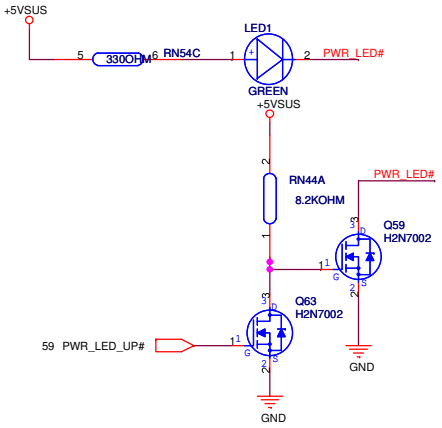

## for Cap. Lock



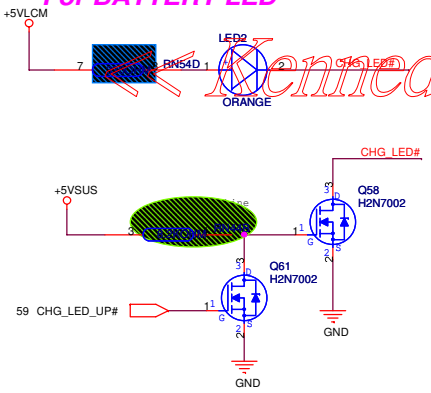

## for Scroll Lock



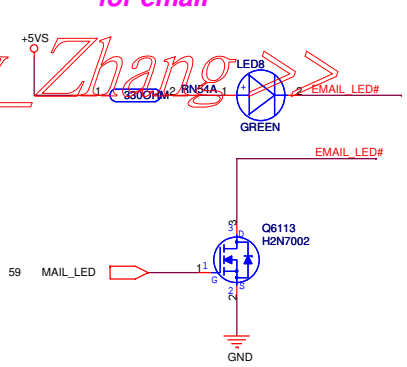

## For POWER LED



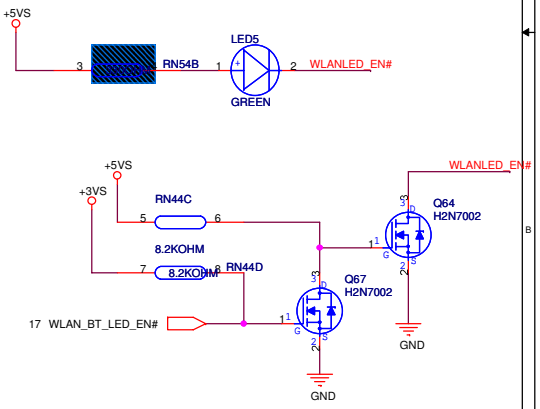

## For BATTERY LED




## for email




## For WireLess LED






<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : LED | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 66 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

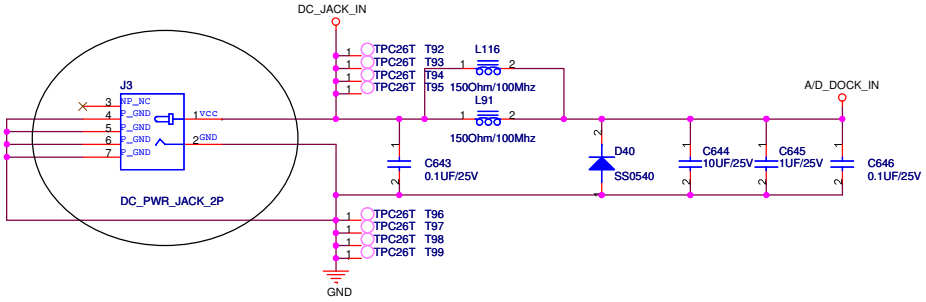
ASUSTeK COMPUTER INC

Engineer: Mike Lee

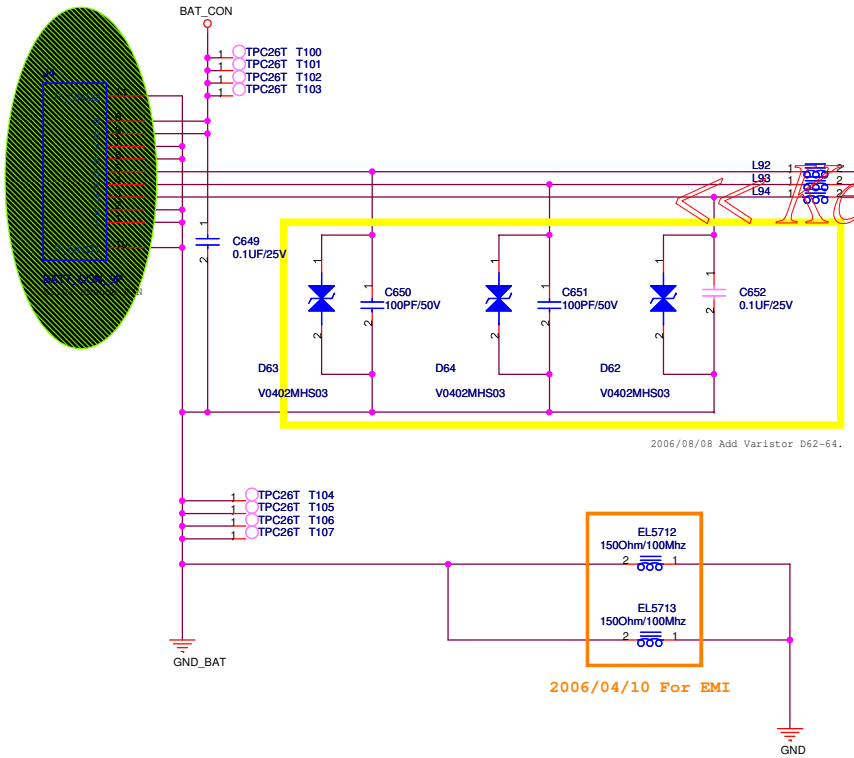
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 67 of 96

## DC IN

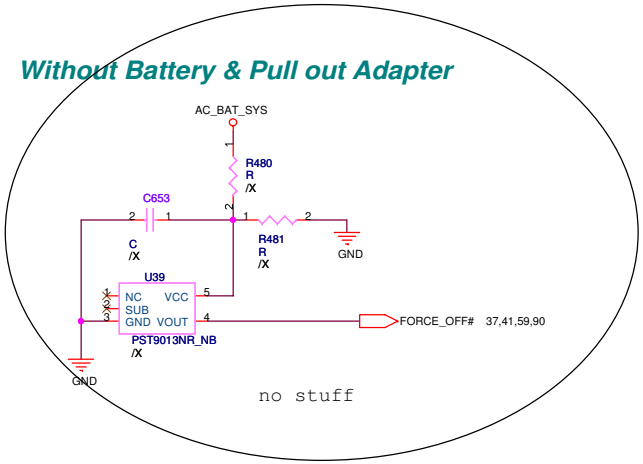



## BAT IN






### Without Battery & Pull out Adapter




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : DC & BAT IN | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 68 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : *

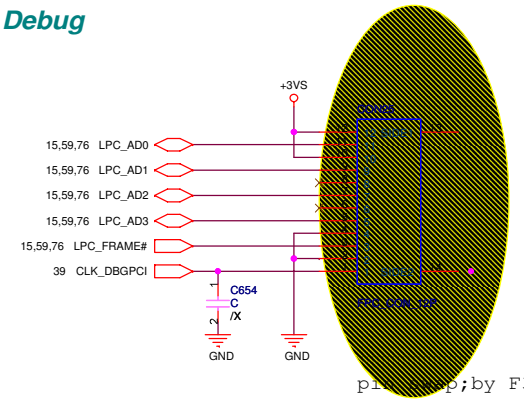
ASUSTeK COMPUTER INC

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

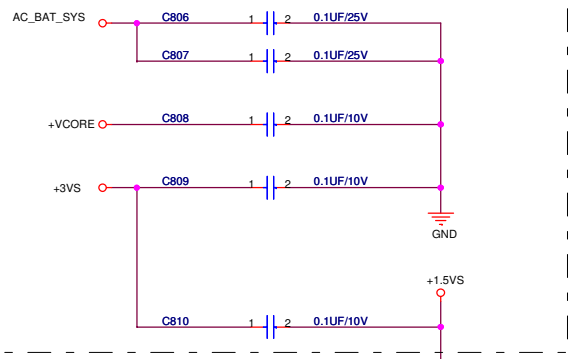
Date: Monday, September 18, 2006 Sheet 69 of 96

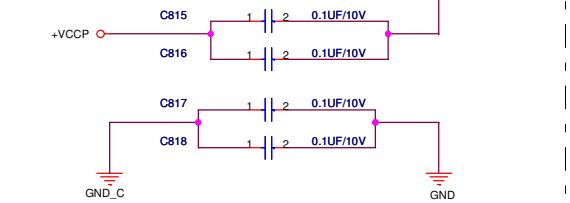
## For Debug




pi[illegible]p;by F3J

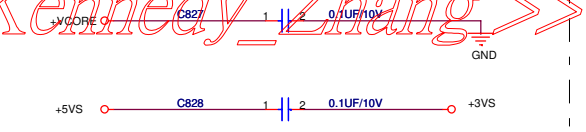
**2006/04/04 Add Stitch caps**




**2006/04/08 Add Stitch caps**






**2006/04/10 Add Stitch caps**

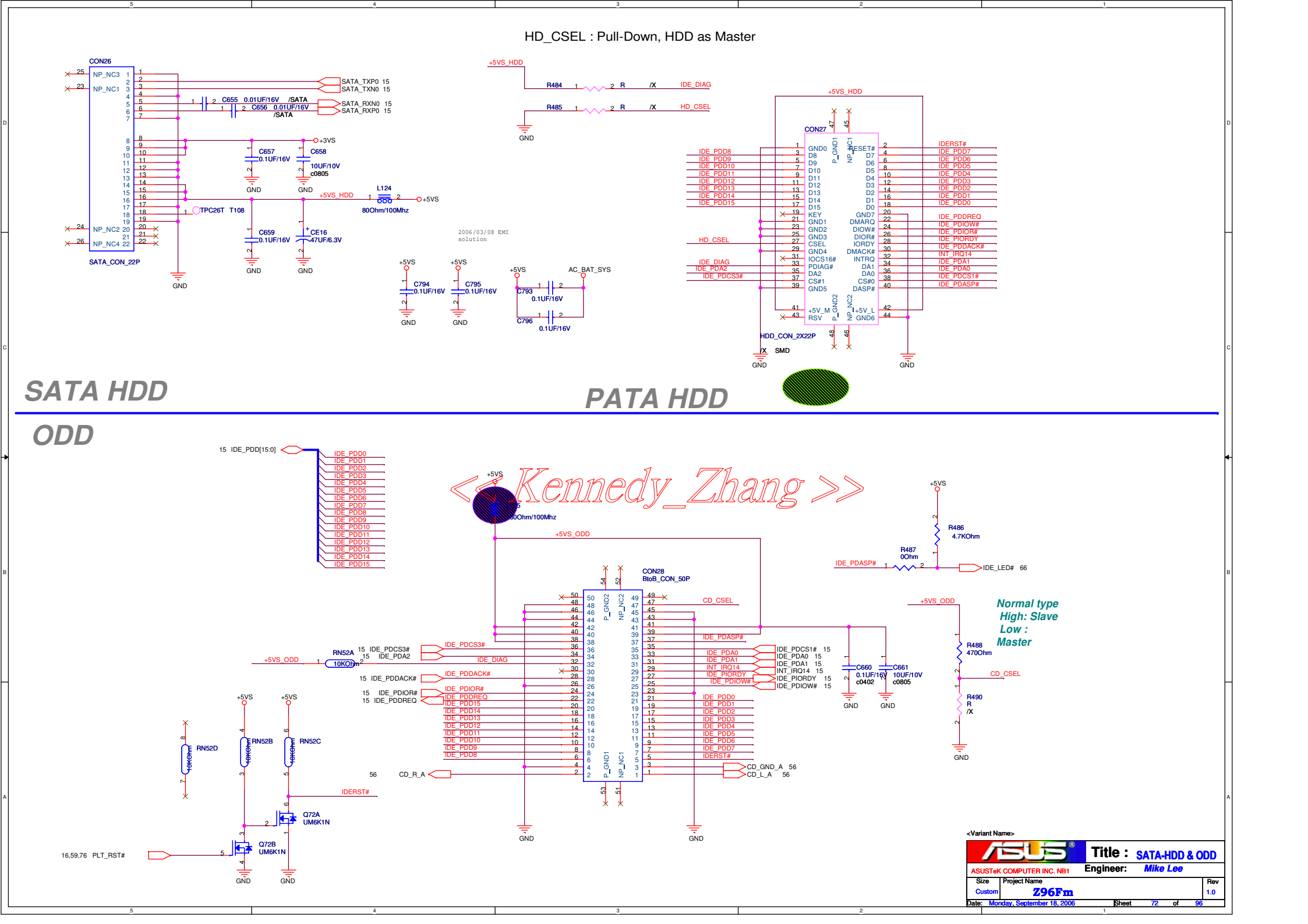
<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Debug CONN. | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 70 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Schematic page name | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 71 of 96 | |


HD_CSEL : Pull-Down, HDD as Master
CON26
SATA_CON_22P
SATA_TXP0 15
SATA_TXN0 15
SATA_RXN0 15
SATA_RXP0 15
C655 0.01UF/16V /SATA
C656 0.01UF/16V /SATA
C657 0.1UF/16V
C658 10UF/10V c0805
C659 0.1UF/16V
CE16 47UF/6.3V
L124 80Ohm/100Mhz
TPC26T T108
+3VS
+5VS_HDD
+5VS
GND
2006/03/08 EMI solution
C794 0.1UF/16V
C795 0.1UF/16V
C793 0.1UF/16V
C796 0.1UF/16V
AC_BAT_SYS
R484 R /X IDE_DIAG
R485 R /X HD_CSEL
CON27
HDD_CON_2X22P
/X SMD
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
HD_CSEL
IDE_DIAG
IDE_PDA2
IDE_PDCS3#
IDERST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0
IDE_PDDREQ
IDE_PDIOW#
IDE_PDIOR#
IDE_PIORDY
IDE_PDDACK#
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDASP#
SATA HDD
PATA HDD
ODD
15 IDE_PDD[15:0]
<< Kennedy_Zhang >>
+5VS_ODD
CON28
BtoB_CON_50P
CD_CSEL
IDE_PDASP#
IDE_PDCS3#
IDE_PDA2
IDE_DIAG
IDE_PDDACK#
IDE_PDIOR#
IDE_PDDREQ
IDE_PDCS1# 15
IDE_PDA0 15
IDE_PDA1 15
INT_IRQ14 15
IDE_PIORDY 15
IDE_PDIOW# 15
CD_GND_A 56
CD_L_A 56
CD_R_A 56
RN52A 10KOhm
RN52D 10KOhm
RN52B 10KOhm
RN52C 10KOhm
Q72A UM6K1N
Q72B UM6K1N
16,59,76 PLT_RST#
IDERST#
R486 4.7KOhm
R487 0Ohm
IDE_LED# 66
R488 470Ohm
R490 R /X
C660 0.1UF/16V c0402
C661 10UF/10V c0805
Normal type
High: Slave
Low : Master
<Variant Name>
Title : SATA-HDD & ODD
ASUSTeK COMPUTER INC. NB1
Engineer: Mike Lee
Size Custom
Project Name Z96Fm
Rev 1.0
Date: Monday, September 18, 2006
Sheet 72 of 96

<< Kennedy_Zhang >>

<Variant Name>

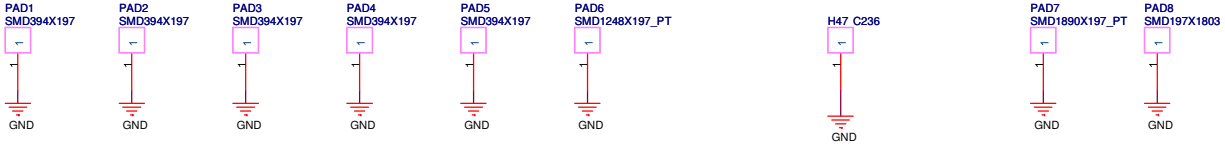
Title : Blank

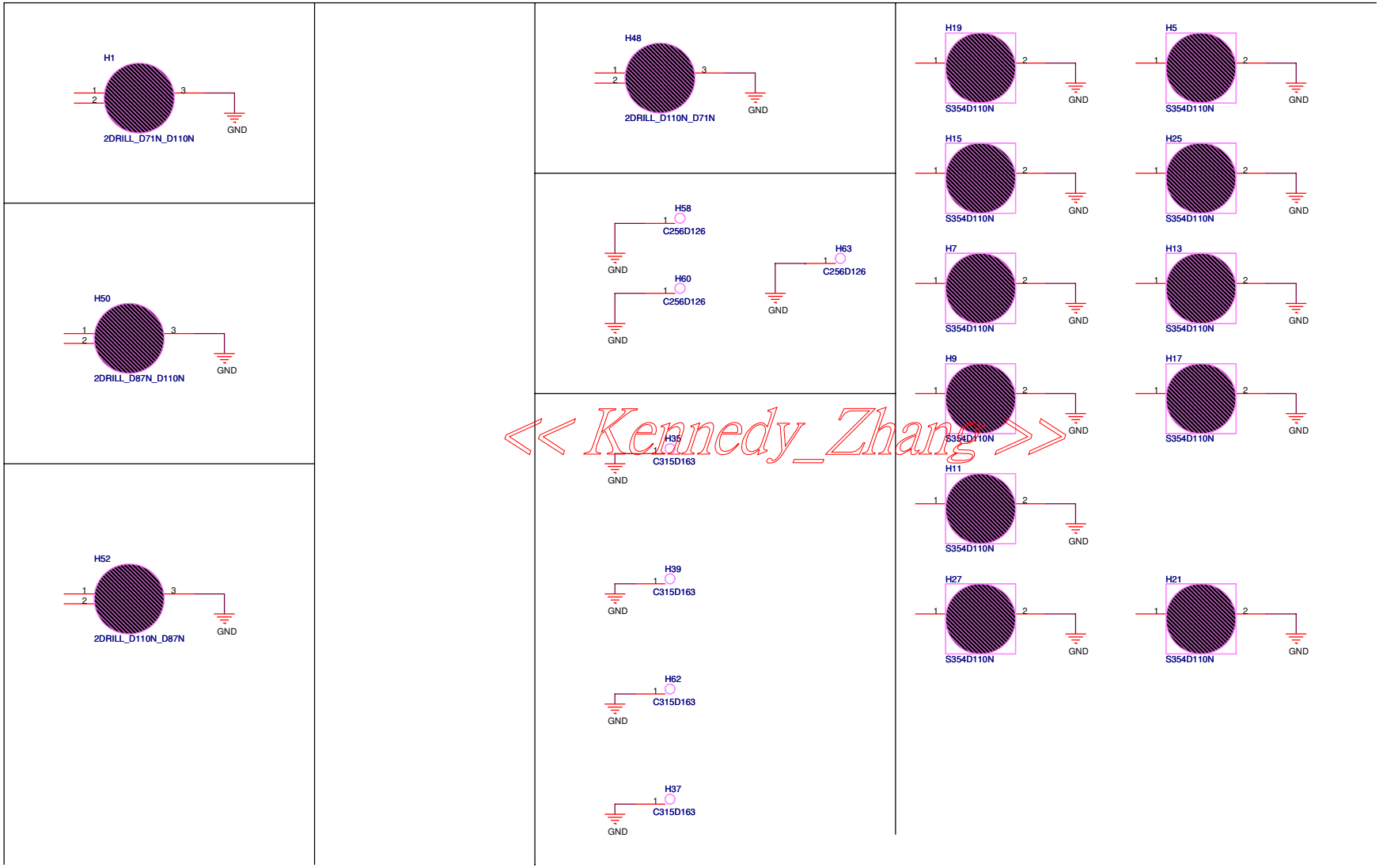
ASUSTeK COMPUTER INC. NB1

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 73 of 96






<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : SCREW HOLE | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 74 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : Schematic page name

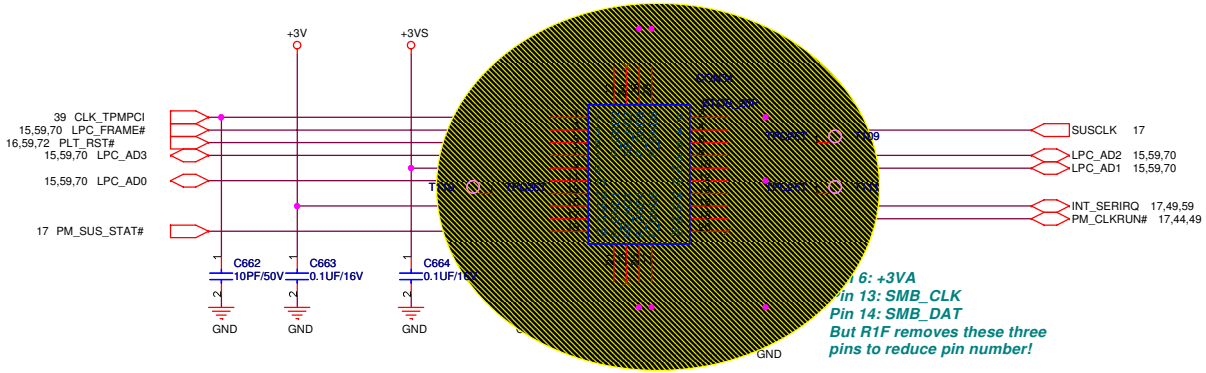
ASUSTeK COMPUTER INC

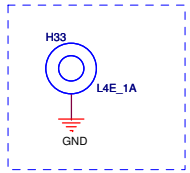
Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 75 of 96

## For TPM Module




TPM MODULE NUT(3.0mm) *1

<< Kennedy_Zhang >>

<Variant Name>

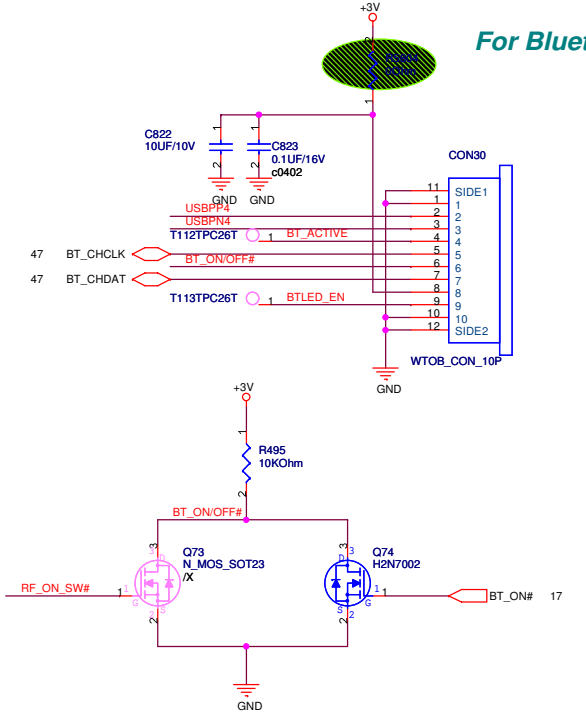
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : TPM | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 76 of 96 | |

<< Kennedy_Zhang >>

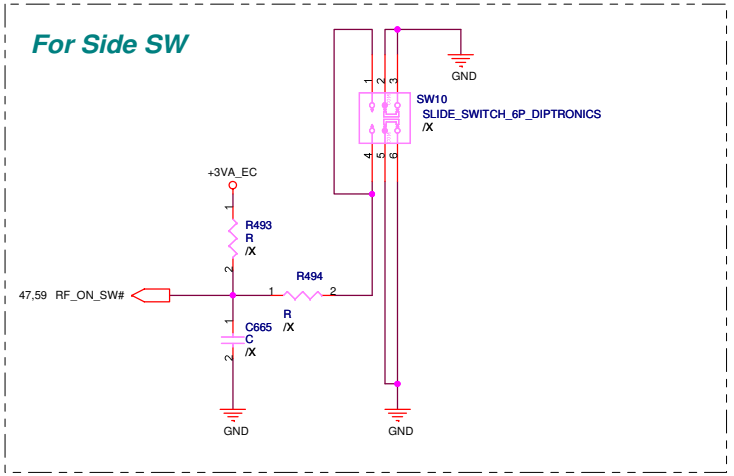
<Variant Name>

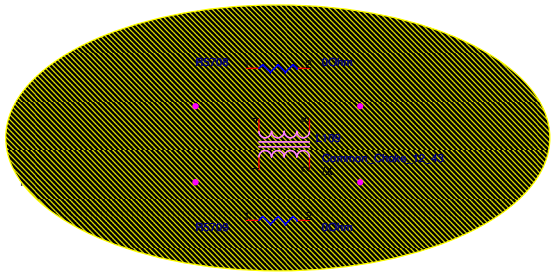
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title: Schematic page name | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 77 of 96 | |

## For Bluetooth




## For Side SW



<< Kennedy_Zhang >>

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Blue Tooth | |
| | Engineer: Mike Lee | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 78 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

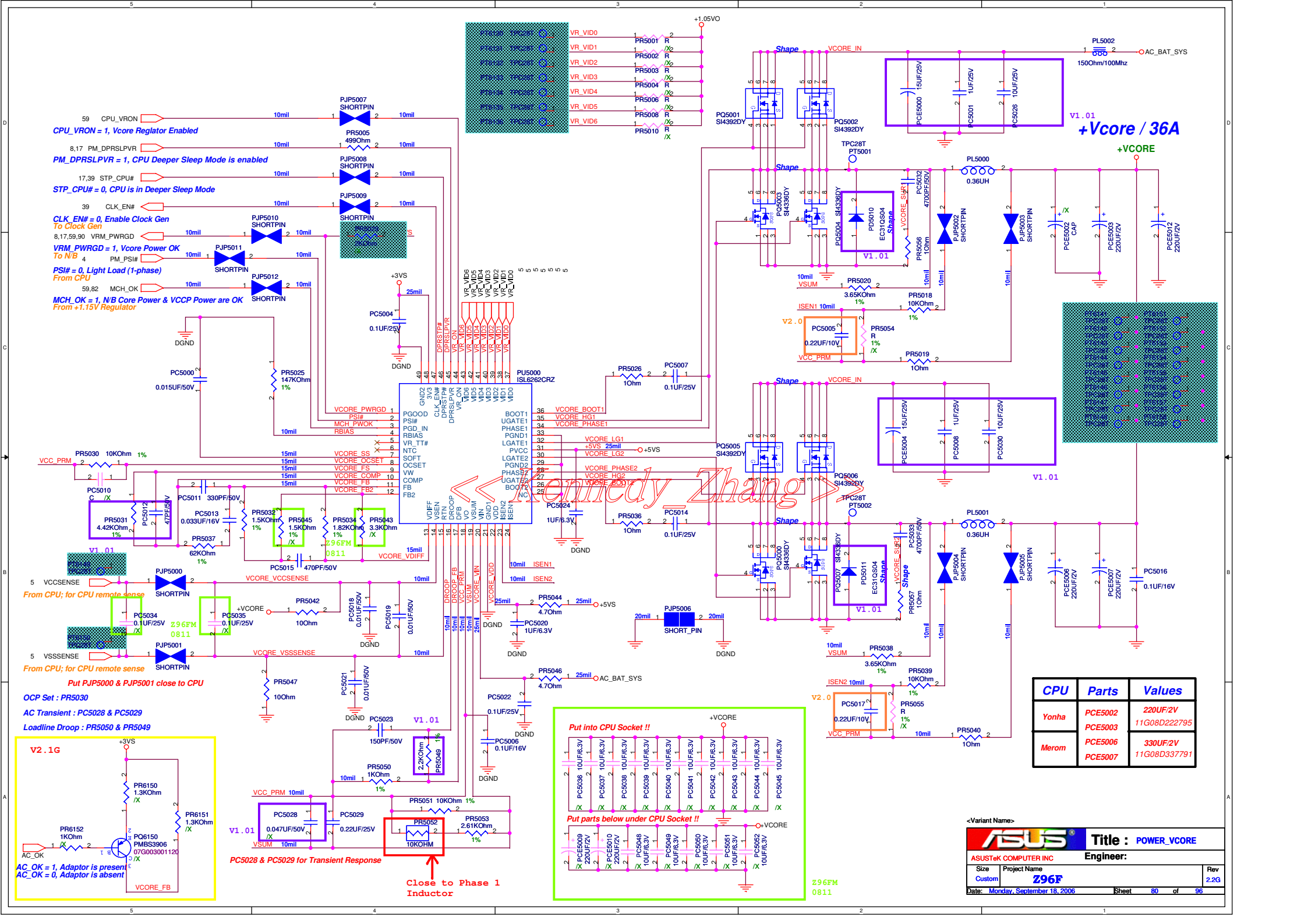
Title : Schematic page name

ASUSTeK COMPUTER INC

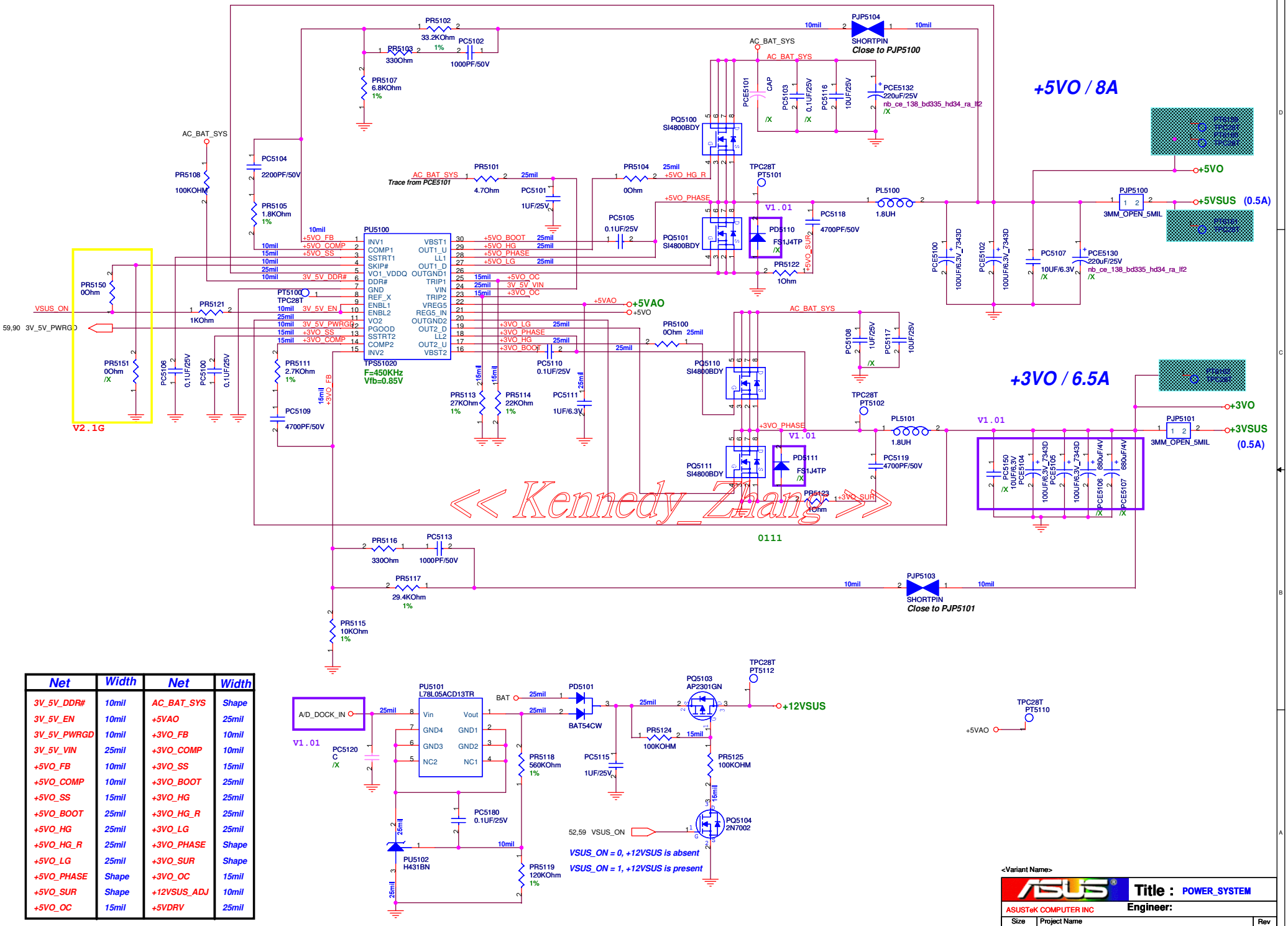
Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 79 of 96




| CPU | Parts | Values |
|---|---|---|
| Yonha | PCE5002<br>PCE5003 | 220UF/2V<br>11G08D222795 |
| Merom | PCE5006<br>PCE5007 | 330UF/2V<br>11G08D337791 |




| Net | Width | Net | Width |
|---|---|---|---|
| 3V_5V_DDR# | 10mil | AC_BAT_SYS | Shape |
| 3V_5V_EN | 10mil | +5VAO | 25mil |
| 3V_5V_PWRGD | 10mil | +3VO_FB | 10mil |
| 3V_5V_VIN | 25mil | +3VO_COMP | 10mil |
| +5VO_FB | 10mil | +3VO_SS | 15mil |
| +5VO_COMP | 10mil | +3VO_BOOT | 25mil |
| +5VO_SS | 15mil | +3VO_HG | 25mil |
| +5VO_BOOT | 25mil | +3VO_HG_R | 25mil |
| +5VO_HG | 25mil | +3VO_LG | 25mil |
| +5VO_HG_R | 25mil | +3VO_PHASE | Shape |
| +5VO_LG | 25mil | +3VO_SUR | Shape |
| +5VO_PHASE | Shape | +3VO_OC | 15mil |
| +5VO_SUR | Shape | +12VSUS_ADJ | 10mil |
| +5VO_OC | 15mil | +5VDRV | 25mil |

<Variant Name>

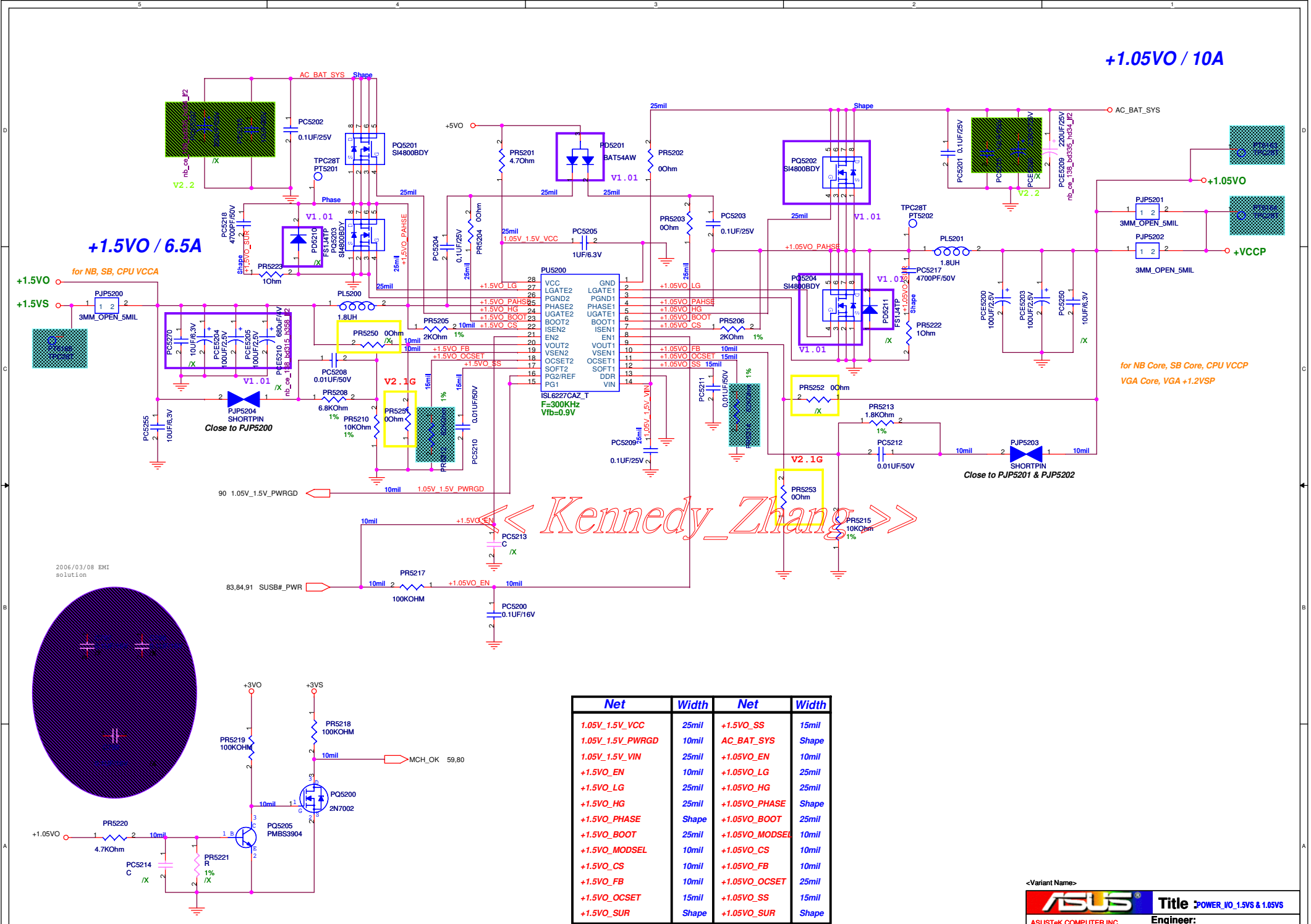
ASUSTeK COMPUTER INC

Title : POWER_SYSTEM

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 81 of 96




| Net | Width | Net | Width |
|---|---|---|---|
| 1.05V_1.5V_VCC | 25mil | +1.5VO_SS | 15mil |
| 1.05V_1.5V_PWRGD | 10mil | AC_BAT_SYS | Shape |
| 1.05V_1.5V_VIN | 25mil | +1.05VO_EN | 10mil |
| +1.5VO_EN | 10mil | +1.05VO_LG | 25mil |
| +1.5VO_LG | 25mil | +1.05VO_HG | 25mil |
| +1.5VO_HG | 25mil | +1.05VO_PHASE | Shape |
| +1.5VO_PHASE | Shape | +1.05VO_BOOT | 25mil |
| +1.5VO_BOOT | 25mil | +1.05VO_MODSEL | 10mil |
| +1.5VO_MODSEL | 10mil | +1.05VO_CS | 10mil |
| +1.5VO_CS | 10mil | +1.05VO_FB | 10mil |
| +1.5VO_FB | 10mil | +1.05VO_OCSET | 25mil |
| +1.5VO_OCSET | 15mil | +1.05VO_SS | 15mil |
| +1.5VO_SUR | Shape | +1.05VO_SUR | Shape |

<Variant Name>

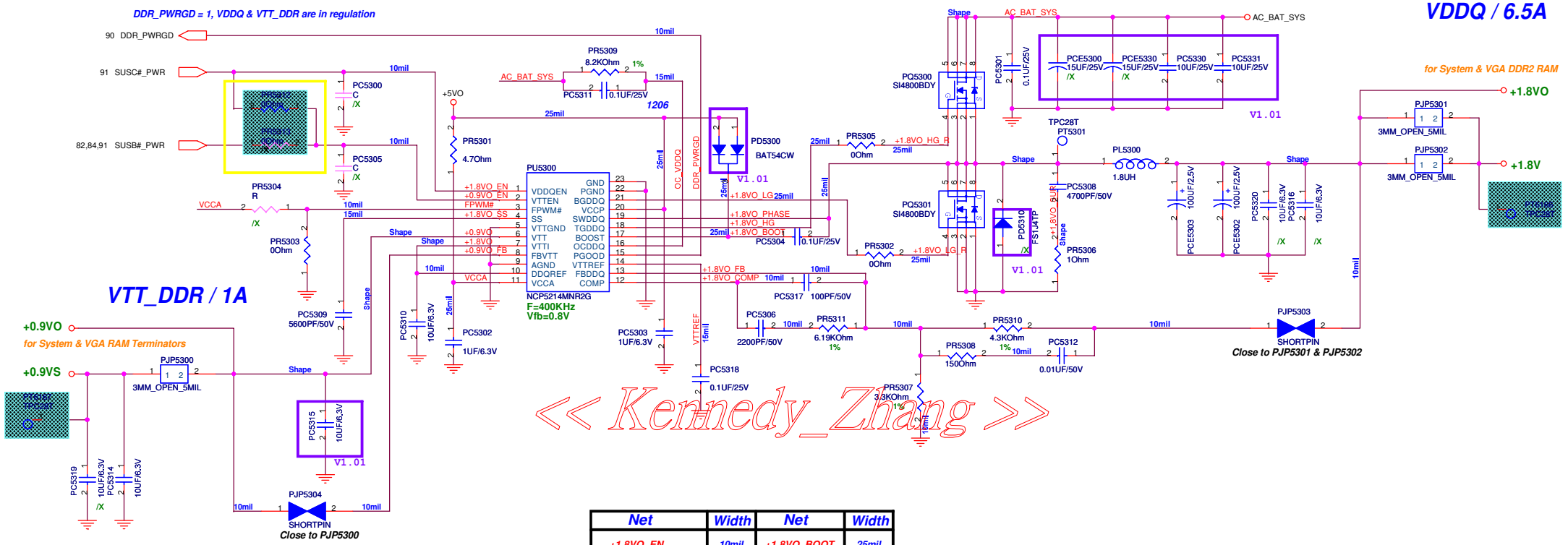
ASUSTeK COMPUTER INC

Title :POWER_I/O_1.5VS & 1.05VS

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 82 of 96




| Net | Width | Net | Width |
|---|---|---|---|
| +1.8VO_EN | 10mil | +1.8VO_BOOT | 25mil |
| +1.8VO | Shape | +1.8VO_COMP | 10mil |
| +0.9VO_EN | 10mil | +1.8VO_HG_R | 25mil |
| +0.9VO | Shape | +1.8VO_LG_R | 25mil |
| +0.9VO_FB | 10mil | +1.8VO_HG | 25mil |
| +1.8VO --> DDQREF | 10mil | +1.8VO_LG | 25mil |
| VTTREF | 15mil | +1.8VO_PHASE | Shape |
| FPWM# | 10mil | +1.8VO_SUR | Shape |
| VCCA | 10mil | +1.8VO_FB | 10mil |
| DDR_PWRGD | 10mil | +1.8VO_SS | 15mil |
| OC_VDDQ | 15mil | AC_BAT_SYS | Shape |

<Variant Name>

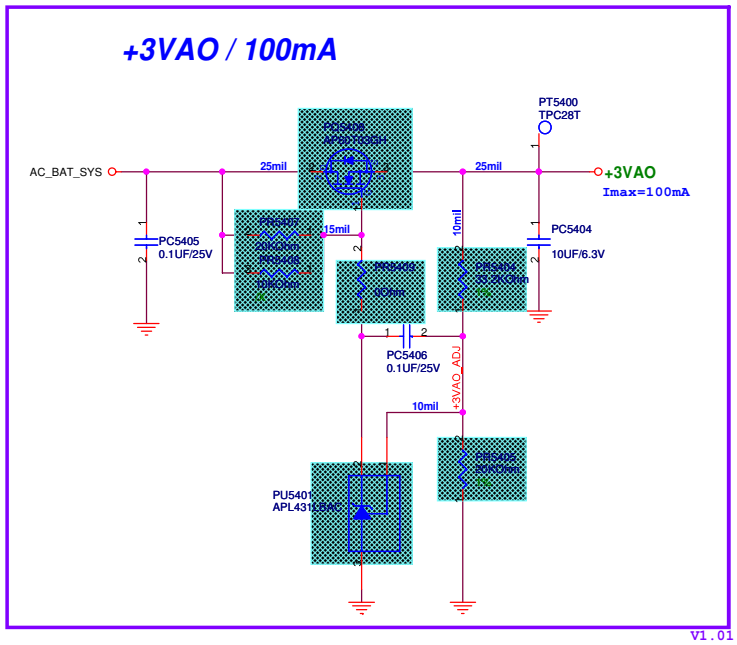
ASUSTeK COMPUTER INC

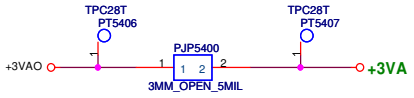
Title : POWER_I/O_DDR & VTT

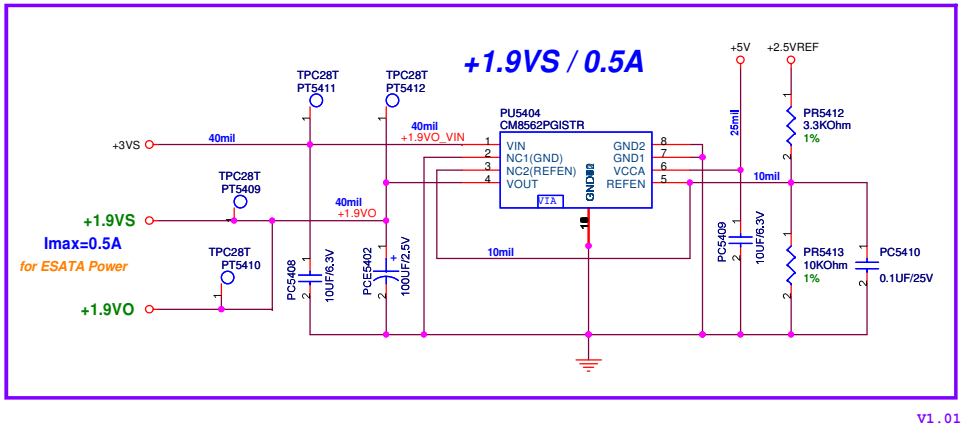
Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

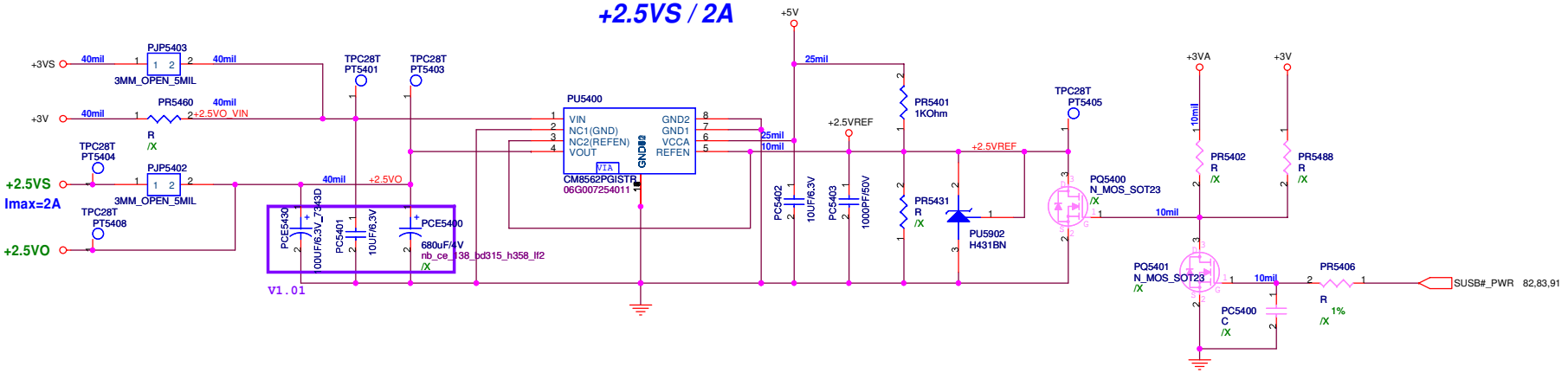
Date: Monday, September 18, 2006 Sheet 83 of 96






<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : POWER_I/O_+3VA & +2.5V | |
| | Engineer: | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 84 of 96 | |

<< Kennedy_Zhang >>

<Variant Name>

Title : POWER_VGA_CORE & RAM

ASUSTeK COMPUTER INC

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

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<Variant Name>

| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number Z96Fm | Rev 1.0 |
| Date: Monday, September 18, 2006 | Sheet 86 of 96 | |

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

### Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

**Adaptor Max. Current :**

*PR5714 = 178K; Iilimit = 4.5A; 90W*

*PR5714 = 47K; Iilimit = 3.5A; 65W*

### Setting the Charge Voltage

Vbatt = Cell * { Vref +[ (VCTL- 1.8V) / 9.52 ] }

VCTL= 1.588V => Vbatt = 4.2V

### Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

**Pre-Charging Mode :**

*Precharging current = 148 ~ 152mA*

*Victl = 0.107V ~ 0.109V*

**Battery Cell Selection :**

*BATSEL_2P# = 0, 3 Cells; Victl = 2.084V*

*=> Icharge = 1.6933A*

*BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V*

*=> Icharge = 2.9329A*

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

*MAX8725_REF : 4.2235V*

*MAX8725_LDO : 5.4V*

## POWER PATH & BAT_LEARN

## Battery Voltage



59 BATSEL_2P#

*BATSEL_2P# = 1, 6 Cells*

*BATSEL_2P# = 0, 9 Cells*

59 PRECHG

*PRECHG = 1, Pre-Charging Mode*

*Charging Current = 156mA*

59 CHG_EN#

*CHG_EN# = 1, Charger Disabled*

*CHG_EN# = 0, Charger Enabled*

59,80 AC_OK

*AC_OK = 1, Adaptor is present*

*AC_OK = 0, Adaptor is absent*

59 BAT_LEARN

*BAT_LEARN = 1, Battery discharges*

*BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)*

*AC_APR_UC = 1, Adaptor is present*

*AC_APR_UC = 0, Adaptor is absent*

*BAT_IN = 0; Battery absence*

*BAT_IN = 1; Battery Plug-in*

*TS# = 1; Battery absence*

*TS# = 0; Battery Plug-in*

<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER_CHARGER

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | 296Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 87 of 96

<< Kennedy_Zhang >>

<Variant Name>

Title : POWER_PIC

ASUSTeK COMPUTER INC

Engineer:

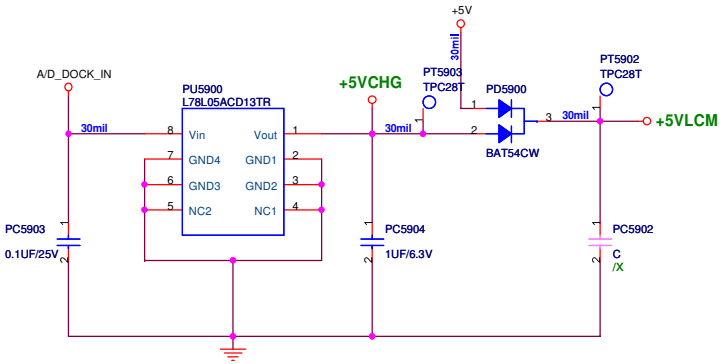
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 88 of 96

REMOVE BATTERY IN DETECT

<< Kennedy_Zhang >>

## +5VLCM / +5VCHG




<Variant Name>

Title : POWER_DETECT

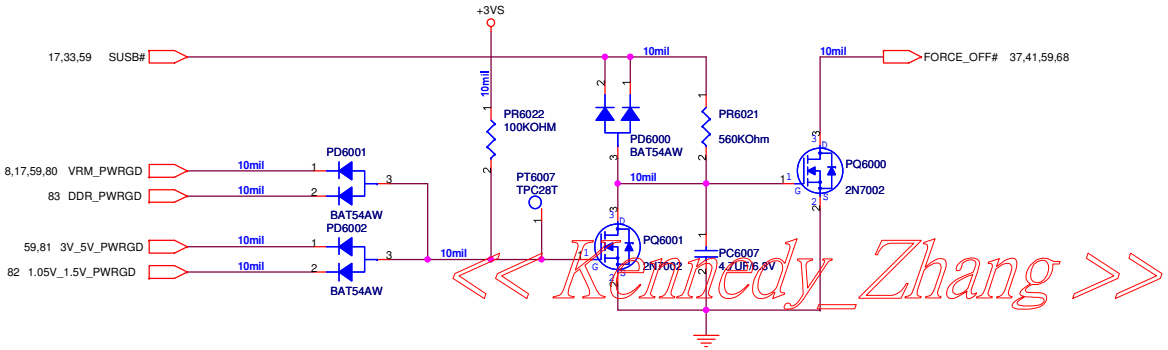
ASUSTeK COMPUTER INC

Engineer:

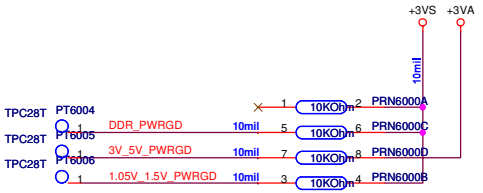
| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 89 of 96

# Power Good Detecter



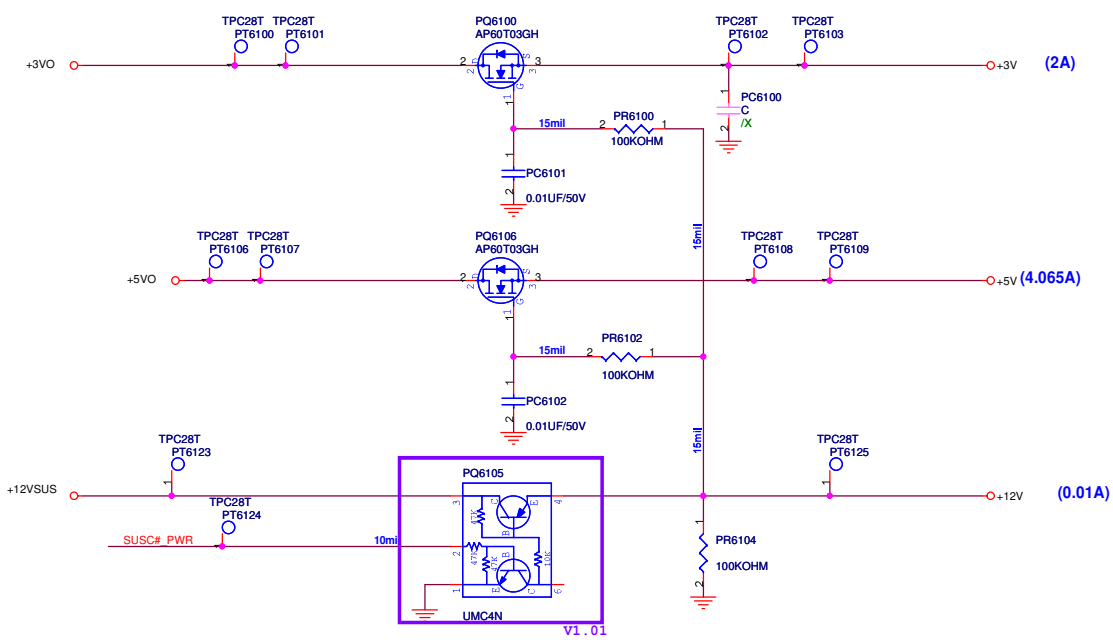


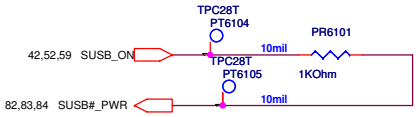




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : POWER_PROTECT | |
| | Engineer: | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 90 of 96 | |

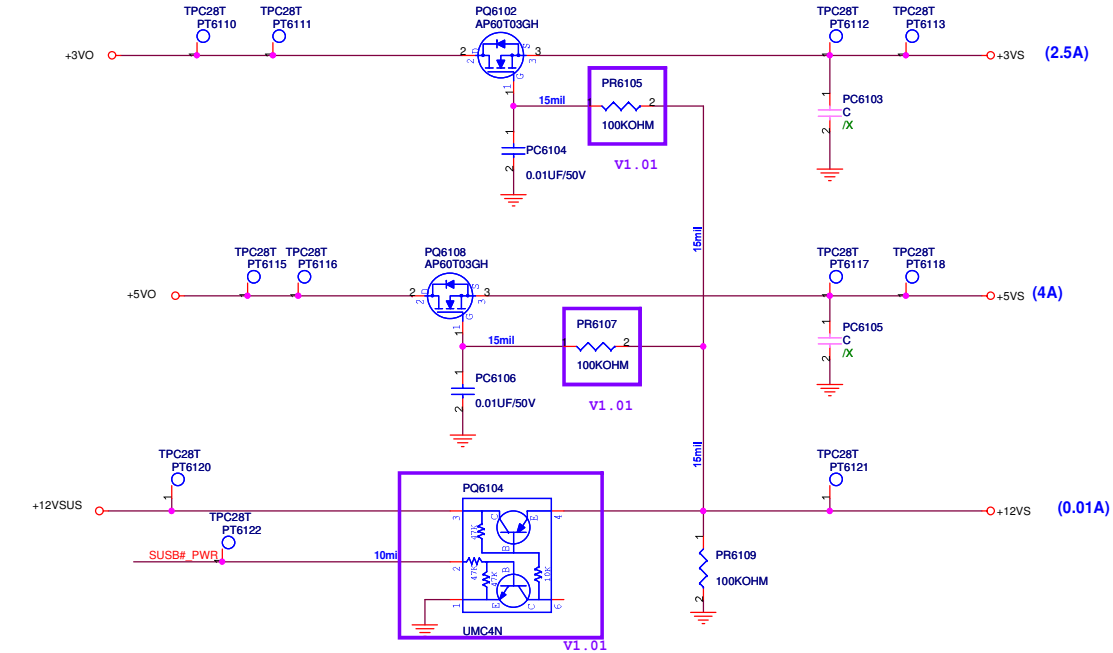
## SUSC#_PWR POWER

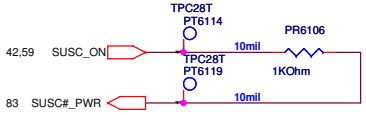



## SUSB#_PWR POWER

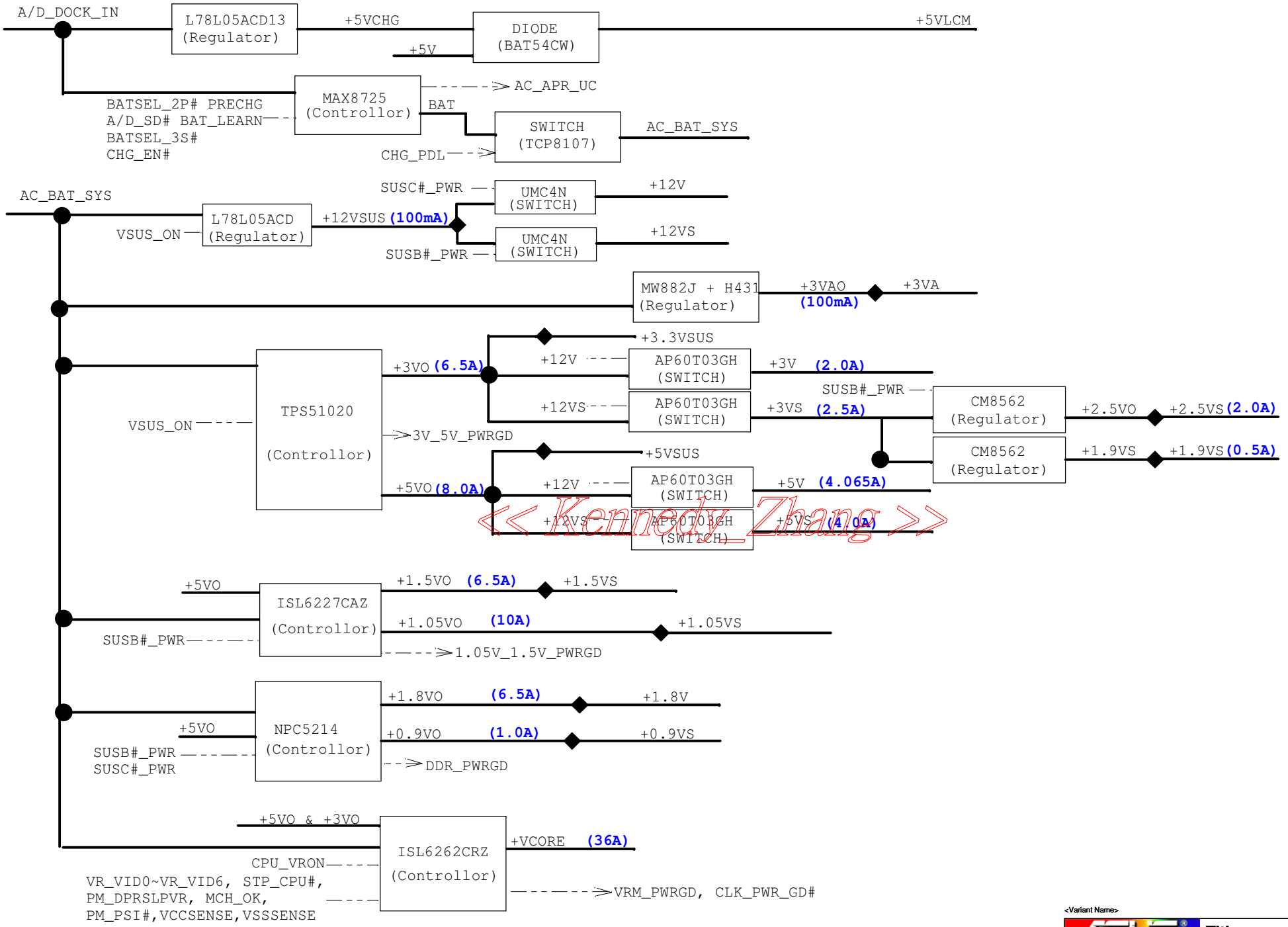





<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : POWER_LOAD SWITCH | |
| | Engineer: | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 91 of 96 | |




<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER_FLOWCHART

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 92 of 96




0106

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : POWER_SIGNAL | |
| | Engineer: | |
| Size: Custom | Project Name: Z96Fm | Rev: 1.0 |
| Date: Monday, September 18, 2006 | Sheet 93 of 96 | |

## CIRCUIT UPDATED HISTORY

| Rev | Date | Description |
|---|---|---|
| 1.00G | 2006/01/10 1430 | Initial release, revision 0.1 |
| | 2006/01/11 2100 | 1. Change NB(U2) part number from 02G010009100 to 02G10009205<br>2. Change SB(U3) part number from 02G010008800 to 02G10007741<br>3. Change RN77, RN78 signals.<br>4. Swap EC(U35) pin33/36/37 signals from CLK_PWRSAVE# / T85 / FAN_PWM to FAN_PWM / CLK_PWRSAVE# / T85.<br>5. Change power circuit page 81, 82, 83, 87 (refer Z96F_R01_0111_P.DSN)<br>6. Delete T139-T141, T143-T146<br>7. Swap Network resistor signals for layout routing. |
| | 2006/01/12 0922 | 1. Swap L84, L108, L115 signals for layout routing.<br>2. Change power circuit page 84 (refer Z96F_R01_0111_P1.DSN)<br>3. Delete T142. |
| | 2006/01/13 1509 | 1. Add C757 for EMI request.<br>2. Modify page2 EC GPIO setting notice table.<br>3. Swap Network resistor signals for layout routing.<br>4. Change PR4724 PU from MAX8725_LDO to +3VA_EC.<br>5. Remove AC_APR_UC# from U35.28 to U35.172<br>6. Delete H41-46 |
| | 2006/01/14 1301 | 1. Delete: R413-R415, R417, F3, C508, R534, R303, R305, RN73-RN76, R5732-R5736.<br>2. NU(not use): C755, R5765, R5766, R5764, R5768, C71, R47, C513, C514, C707,C708, C517, C524, C526, C568, C642, C741, C744, C745, C726, C706, C404.<br>3. page32, change RGB far end terminator from Resistor(R5759/R5761/R5763) to Network Resistor(RN79).<br>4. page35, change TV_OUT signal far end terminator from Resistor(R5755-R5757) to Network Resistor(RN80).<br>5. page42, change discharge resistor from Resistor(R5774-R5783) to Network Resistor(RN81-RN83).<br>6. Change RN77 signal.<br>7. Change 25MHz X'tal (X7) to 07G010Q12500.<br>8. Change Thermal IC U16 to SOP (06G023026011)<br>9. Change 0.1UF/25V cap from X7R +/-10% to Y5V+80-20%: C757, C643, C646, C649, C652 |
| | 2006/01/16 1530 | 1. Change power circuit page 80, 81, 82, 83 (refer Z96F_R00_0116_P.DSN)<br>2. Change X1, X6 package to same as Z84F. |
| | 2006/01/17 1046 | 1. Swap Network resistor signals for layout routing.<br>2. Change Codec ALC882(U30) part number from 02G611001300 to 02G611001310. |
| | 2006/01/17 2038 | 1. Change power circuit page 80, 83 (refer Z96F_R01_0117_P.DSN)<br>2. Add Network Resistor RN84, RN85(NU, reserved) to block VGA signal between CRT and PortBar connector( EMI request) . |
| | 2006/01/18 1103 | 1. Swap Network resistor RN81, RN83 signals for layout routing.<br>2. Stuff C755.<br>3. NU: C115, C116, R304, R306, R282, R284, R5796, CN10, C655, C656.<br>4. Add 3 0ohm resistor R5805(NU), R5806, R5807 for SATA function disable. |

| Rev | Date | Description |
|---|---|---|
| | 2006/01/18 1645 | 1. Change power circuit page 81, 82, 83, 84, 87 (refer Z96F_R01_0118_P.DSN)<br>2. Swap PCIE clock (NEWCARD & MCH_3GPLL) for layout routing.<br>3. Swap Network resistor RN58, RN77, RN78, RN84, RN85 signals for layout routing. |
| | 2006/01/19 1145 | 1. Swap Network resistor RN18, RN82, RN85 signals for layout routing.<br>2. Change U1 (CPU) ,U2 (North Bridge) ,U3 (South Bridge) to Note Book parts. |
| | 2006/01/19 2127 | 1. Change power circuit page 81 (refer Z96F_R01_0119_P.DSN) |
| | 2006/01/20 1735 | 1. DEL PORT_BAR.<br>2. Add an ESATA (page54) and an USB port.<br>3. Change CON27.47, CON27.48 / CON26.25, CON26.26 / CON28.54, CON28.53 to NC<br>4. Connect H35-H40, H62, H63 to GND |
| | 2006/01/23 1005 | 1. Change power circuit page 80- 84, 87, 91 (refer Z96F_R01_0120_P.DSN)<br>2. DEL RN84, RN85, R5719-R5726. |
| | 2006/01/23 1714 | 1. Change power circuit page 84, 87, 91 (refer Z96F_R01_0120_P1.DSN)<br>2. Change ESATA1/ CON42 connector to NB part.<br>3. Change EC(U35) pin 28 from T174 to AC_APR_UC# signal.<br>4. Change EC(U35) pin 174 signal from AC_APR_UC# to AC_OK# signal.<br>5. Add a N-MOS(Q6118) to invert AC_OK signal. |
| | 2006/01/24 1030 | 1. Change RN53, RN54, RN81-RN83 from 0402 to 0603.<br>2. Add C764-765, R5812-5815 for ESATA.<br>3. Add D59, Q6119 to switching XD card power.<br>4. Change CON21 signal.<br>5. Change U35.89/RN41.1/SW3.1/SW3.2 signal from EXPLORE_SW# to PWR4GEAR#.<br>6. Change power circuit page 81 (refer Z96F_R01_0124_P.DSN)<br>7. Swap Network resistor RN18, RN79, RN78, L115 signals for layout routing.<br>8. Change page 93 +5VA signal name to +5VAO. |
| | 2006/01/25 1425 | 1. Change RN70, RN71, RN79, RN80 to LF parts.<br>2. Change PU5700.6 signal name to AC_OK. |
| | 2006/01/25 2110 | 1. Swap Network resistor RN33, RN53, RN70, RN79, RN80 signals for layout routing.<br>2. Change T2R2 to 10M ohms. |
| | 2006/01/26 1822 | Change Revision to 1.00G |
| | 2006/02/13 1536 | Change C764, C765, C118-C121 from Y5V to X7R<br>Change T2C25, T2C26 from Y5V to X7R |
| | 2006/02/17 1639 | Modify Block Diagram |



<Variant Name>

ASUSTek COMPUTER INC

Title : History(1)

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

Date: Monday, September 18, 2006 Sheet 94 of 96

## CIRCUIT UPDATED HISTORY(2)

| Rev | Date | Description |
|---|---|---|
| 1.01G | 2006/02/27 1100 | 1. Change R5710 to NU<br>2. Add R5816(NU)<br>3. Change page54 ESATA power from +VRAM to +1.8V<br>4. Change C717, C718 connection.<br>5. Swap INTERNAL MIC R/L.<br>6. Stuff R47 (10M ohms).<br>7. Change Rev to 1.01G |
| | 2006/03/01 1120 | 1. Add R5828-5831, C788.<br>2. Swap LTPB0-/+ common choke (L112) for routing.<br>3. Swap LTPA0-/+ common choke (L113) for routing.<br>4. Swap USB_PN5/_PP5 common choke (L115) for layout routing.<br>5. Swap RN34 signals for layout routing.<br>6. Change page54 ESATA from SII3132 to JMB360.<br>7. Change page74 scrow hole type. |
| | 2006/03/02 1819 | 1. Updated power page80-84, 87, 91<br>2. Del page55 circuit. |
| | 2006/03/03 1450 | 1. Add screw hole H63<br>2. Change ESATA SMBus PU 4.7K to 3V<br>3. Change ESATA +1.8V to +1.9V<br>4. Modify page54 ESATA power rail.<br>5. Updated power circuit page80-82, 84, 87.<br>6. Change HSYNC/VSYNC level shifter (U44, U45) power rail from 5V to 3.3V. |
| | 2006/03/03 1740 | 1. Updated power circuit page80-82, 84, 87 (refer Z96F_R101G_0303_P2.DSN)<br>2. Add PWRSW# mask circuit (page41).<br>3. Change HSYNC/VSYNC ESD power rail from 5V to 3.3V. |
| 1.1G | 2006/03/06 1950 | 1. Change H54, H56 / H29, H31 / H3 / H33 from screw hole to NUTs.<br>2. Change X1 / X6 from DIP type to SMD type.<br>3. Change C112, C113 / C632, C633 value from 20pF to 12pF.<br>4. For EMI:<br>1) Add L124.<br>2) Change R536, R537 from 0R to Bead(1K ohm/100MHz).<br>3) Stuff R418, R431 with 0R.<br>4) Change L52 from 80 ohm/100MHz to 150ohm/100MHz).<br>5) Stuff C411, C412, C413, C414.<br>5. Change Rev to 1.1G (to meet NB team PN rule) |
| | 2006/03/08 1100 | 1. Del H23<br>2. Del C698, C699<br>3. Add RN73-76, C793-799 (NU, for EMI).<br>4. NU R359 |
| | 2006/03/09 2121 | 1. Swap RN44, RN54 signals for routing.<br>2. Stuff R5794, RTC BATT, R68, R69, C517, C524, C526, R550<br>3. NU R71, R72, R307<br>4. Change D58 from SS0540 to 1N4148<br>5. Change CON5 (LVDS CONN) to 12G09103004P<br>6. Change U16 to ADT7461ARMZ<br>7. Change SW1-4, SW6-7 to 12G09103004P |

| Rev | Date | Description |
|---|---|---|
| | | 8. Change X7 part.<br>9. Change C727-728 from 24p to 18p<br>10. NU R5770, R5769, Q6116, SW11, R5717, R5718<br>11. Add C500 for U23<br>12. Del XD function: Del D59, Q6119, C709. |
| | 2006/03/10 1212 | 1. Change power circuit page 81-84, 87 (refer Z96F_R11_0310_P.DSN) |
| | 2006/03/10 1538 | 1. NC CON36.16 |
| | 2006/03/13 2013 | 1. Change R48 from 22K to 100K<br>2. Del R307.<br>3. NU R5795, Q6117, R550.<br>4. Stuff R5797=0R, SW7. |
| | 2006/03/14 1430 | 1. Change U1 to 12G04600479A<br>2. Change CON2 to 12G025332003<br>3. Change CON3 to 12G025122000<br>4. Change CON36 to 12G142101100<br>5. Change CON27 to 12G161530444<br>6. Change CON13 to 12G030100522<br>7. Change J1, J2 to 12G140031067<br>8. Change power circuit page 81, 82(refer Z96F_R11_0314_P.DSN) |
| | 2006/03/16 2016 | 1. Stuff CE2 100UF/2.5V_7343<br>2. Stuff R307 10K ohm_0402<br>3. Stuff C627, C741 10UF/10V_0805<br>4. Stuff C742, C743, C744, C748 0.1UF/16V_0402 |
| 2.0G | 2006/04/03 0809 | 1. Change to Rev 2.0<br>2. Add a MOSFET Q6121 to block USB power<br>3. Add R5838, C800-C805, D61<br>4. Change NUT H56, H54 to 4.2mm<br>5. Change PR5709 P/N<br>6. Change JRST1 footprint to R0402 |
| | 2006/04/03 1527 | 1. Change JRST1<br>2. Change power circuit page 80-84, 87, 89-92(refer Z96F_R20_0403_P.DSN) |
| | 2006/04/04 0756 | 1. Change NEWCARD_CLK from U18.24-25 to U18.19-20<br>2. Add R5839, R5840, R5841<br>3. Add R5842, R5843, R5844<br>4. Stuff R5833<br>5. NU Q6120, R5832, R5834, R5834, D60 |
| | 2006/04/04 2154 | 1. Add Stitch cap C806-C810<br>2. Add C811-C814<br>3. NU R352, Stuff R353<br>4. Change CON7.6 to GND<br>5. BIOS1 to SMD and NU U38 (BIOS Socket). |
| 2.1G | 2006/04/07 1445 | 1. Change to Rev 2.1<br>2. Change power circuit page 84(refer Z96F_R20_0407_P.DSN) |



ASUSTeK COMPUTER INC

Title : History(2)

Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

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## CIRCUIT UPDATED HISTORY(3)

| Rev | Date | Description |
|---|---|---|
| 2.1G | 2006/04/08 1108 | 1. Add Stitch cap C815-C818 |
| | 2006/04/10 0945 | 1. Add C824, C819-821, R5845, R5846, R5847, R5848, L126, C825, C822, C823<br>2. Change R352 power rail to +3V.<br>3. NU R5743-R5750, R540, C703<br>4. Change C696 to close CON37.6 |
| | 2006/04/10 2103 | 1. Add Bead EL5712, EL5713.<br>2. Add stitch caps C828, C827<br>3. Add C826 |
| | 2006/04/10 2257 | 1. Change R495 PU rail to +3V |
| | 2006/04/11 0820 | 1. Change power circuit page80, 81, 82, 84 (refer Z96F_R20G_0410_P.DSN) |
| | 2006/04/11 1442 | 1. Change U38 from socket to BIOS. |
| | 2006/04/11 1942 | 1. Change power circuit page84 (refer Z96F_R20G_0411_P.DSN) |
| | | |
| 2.2G | 2006/05/05 1045 | 1. Shorted CON7 pin5, 6 |
| | 2006/05/09 1745 | 1. Change L42-L44 to 0.082uH<br>2. Change C392, C394, C396 to 27pF<br>3. Change power circuit page82, 87 (refer Z96F_R22G_P.DSN) |
| | 2006/05/10 1845 | 1. Change R62 to 20ohms 1% |
| | 2006/05/18 1645 | 1. Change L4, L9, L10 from Ferrite Bead 80ohm/2A to Resistor 0ohms/0805. |
| | 2006/05/19 2054 | 1. NU CE12, CE14.<br>2. Add CE17, CE18.<br>3. NU BATTERY. |
| | 2006/06/01 1152 | 1. Change U2 PN to 02G010009210IN QG82945GM<br>2. Change U3 PN to 02G010007741IN NH82801GBM |
| | 2006/06/13 1858 | 1. U2 PN Change back QG82945GM<br>2. U3 PN Change back NH82801GBM |
| | 2006/06/22 2038 | 1. NU C652 |
| | | |

| Rev | Date | Description |
|---|---|---|
| Z96Fm 1.0 | 2006/08/07 1530 | 1. Change project code to Z96Fm 1.0 (ER stage)<br>2. DEL R5707<br>3. ADD R5849-5852, Q6122, Q6123 |
| | 2006/08/08 1830 | 1. Add Varistor D62-D64 & PR5043, PR5045.<br>2. Change U2 PN to 02G010009210WB ( QG82945GM)<br>3. Change U3 PN to 02G010007741WB (NH82801GBM) |
| | 2006/08/10 1630 | 1. Change Audio Jack J1, J2 from 12G140301067 to 12G14030106E<br>2. ADD R5853-5857, Q6124<br>3. Stuff PR5312, NU PR5313<br>4. DEL C619<br>5. Stuff CON26, C655 - C659, C793-C796 & C115, C116, R5805 & R304, R306,R282, R284.<br>6. NU CON27 |
| | 2006/08/11 1530 | 1. Change power circuit page80 (refer Z96FM_R10_0811_P.DSN) |
| | 2006/08/14 1430 | 1. Change R5851 to 39.2K |
| | 2006/08/15 1127 | 1. Change J1, J2 pin9, 10 to NC. |
| | 2006/08/15 2002 | 1. Add R5858, R5859 |
| | 2006/08/16 1125 | 1. Add D66, R5860, C829<br>2. Change CE10, CE9 from 47uF/6.3V to 100uF/6.3V |
| | 2006/08/16 2000 | 1. NU Q6122-Q6124, R5850, R5853, R5855, R5857, D65<br>2. STUFF Q77, R5854, R5856 |
| | 2006/09/14 1900 | 1. Move L68 to be an input filter.<br>2. Change R426, R427 from 10ohm to 75ohm. |
| | 2006/09/18 1000 | 1. Swap RN67A, RN67B.<br>2. Add C830-C833.<br>3. Change PC5005, PC5017 to 0.22uF/X7R . |
| | 2006/09/18 1000 | 1. Swap RN67 |
| | | |



<Variant Name>

ASUSTeK COMPUTER INC

Title : History(3)

Engineer: Mike Lee

| Size | Project Name | Rev |
|---|---|---|
| Custom | Z96Fm | 1.0 |

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