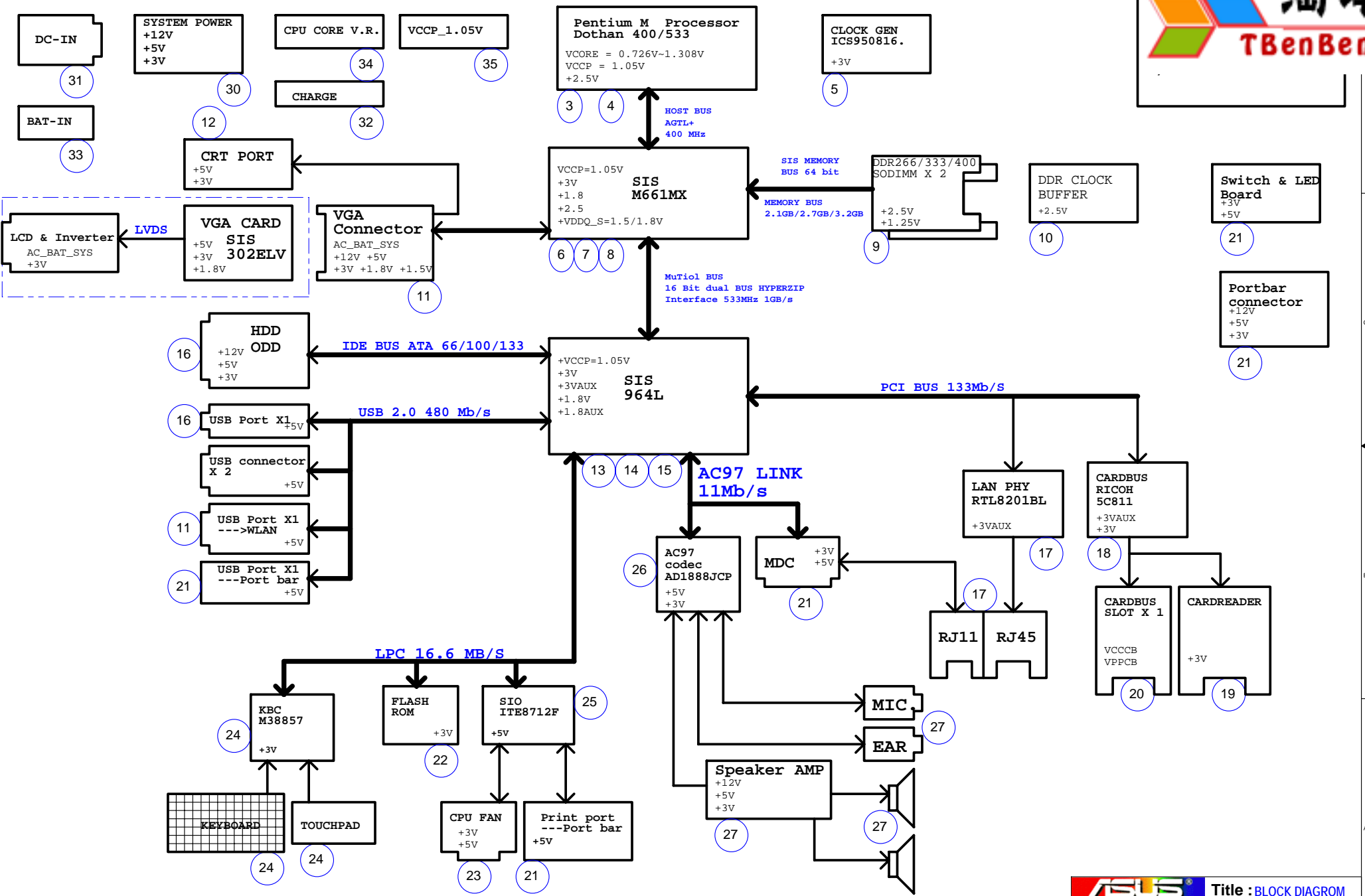


Z94 SCHEMATICS : MAIN BOARD REV 1.1

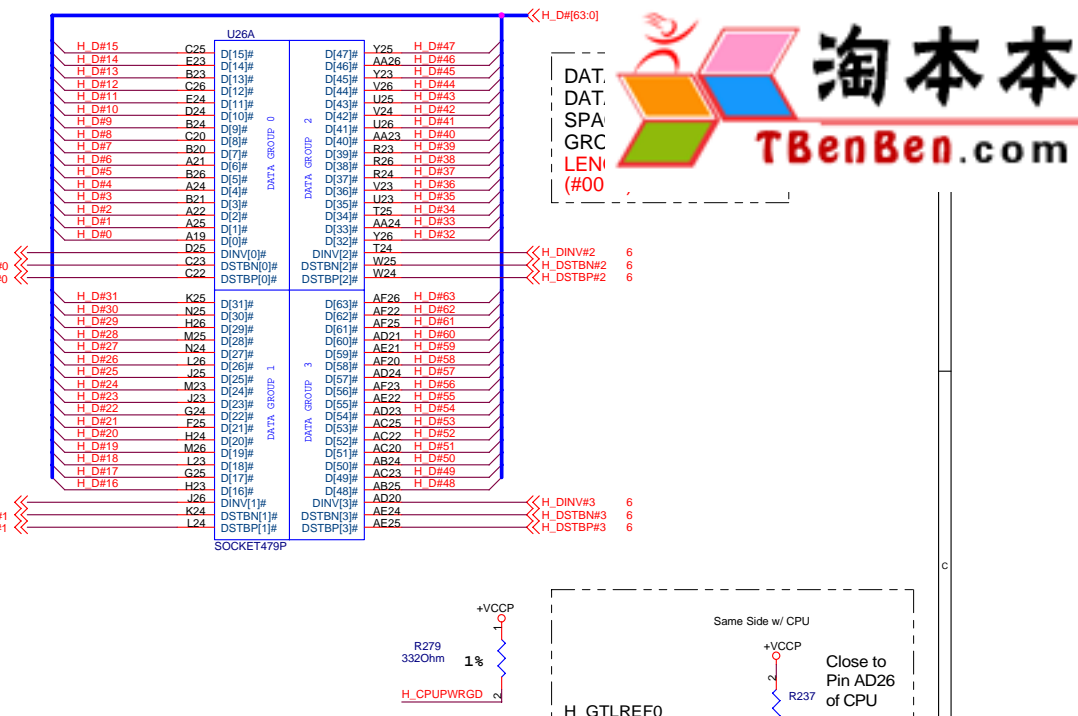
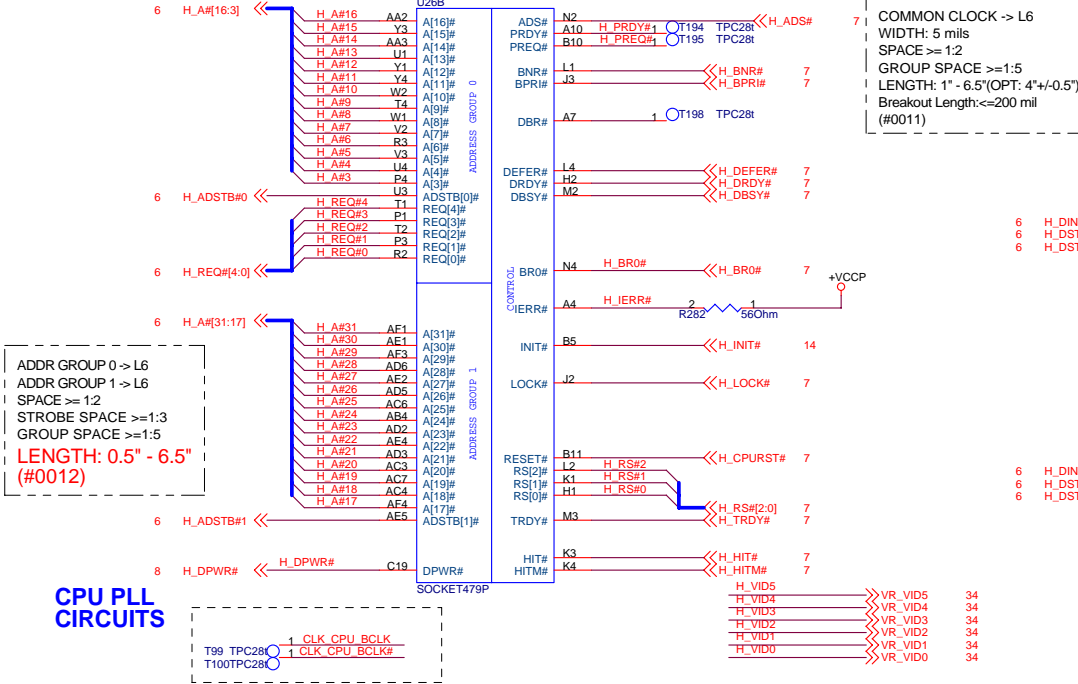


- P.01--INDEX (THIS PAGE)
- P.02--BLOCK DIAGRAM
- P.03--Pentium-M SOCKET479 - 1
- P.04--Pentium-M SOCKET479 - 2
- P.05--CLOCK GEN ICS950816
- P.06--SISM661MX (1) HOST/AGP
- P.07--SISM661MX (2) DDR/VGA/ZIP
- P.08--SISM661MX (3) PWR
- P.09--DDR Memory DIMM
- P.10--DDR Bypass & Driver
- P.11--VGA_Connector
- P.12--CRT Connector
- P.13--SIS964L - 1 PCI/ZIP/IDE
- P.14--SIS964L - 2 LPC/GPIO/AC97
- P.15--SIS964L - 3 USB/PWR
- P.16--HDD & CDROM CONN/USB
- P.17--LAN_RTL8201BL
- P.18--CardBus (1)
- P.19--CardBus (2)
- P.20--Debug Port & Hole & EMI
- P.21--Switch & MDC
- P.22--PortBar & FWH
- P.23--FAN controller
- P.24--KBC_KB38857
- P.25--Super I/O
- P.26--Audio Codec
- P.27--Audio AMP/JACK
- P.28--Power Sequence
- P.29--2.5V/1.8V/1.5V/1.25V
- P.30--SYSTEM_3V/5V
- P.31--BATLOW/SD#/DCIN
- P.32--CHARGER
- P.33--PIC16C54/BAT_IN
- P.34--Vcore
- P.35--VCCP_1.05V
- P.36--GPIO LIST
- P.37--POWER FLOW
- P.38--History



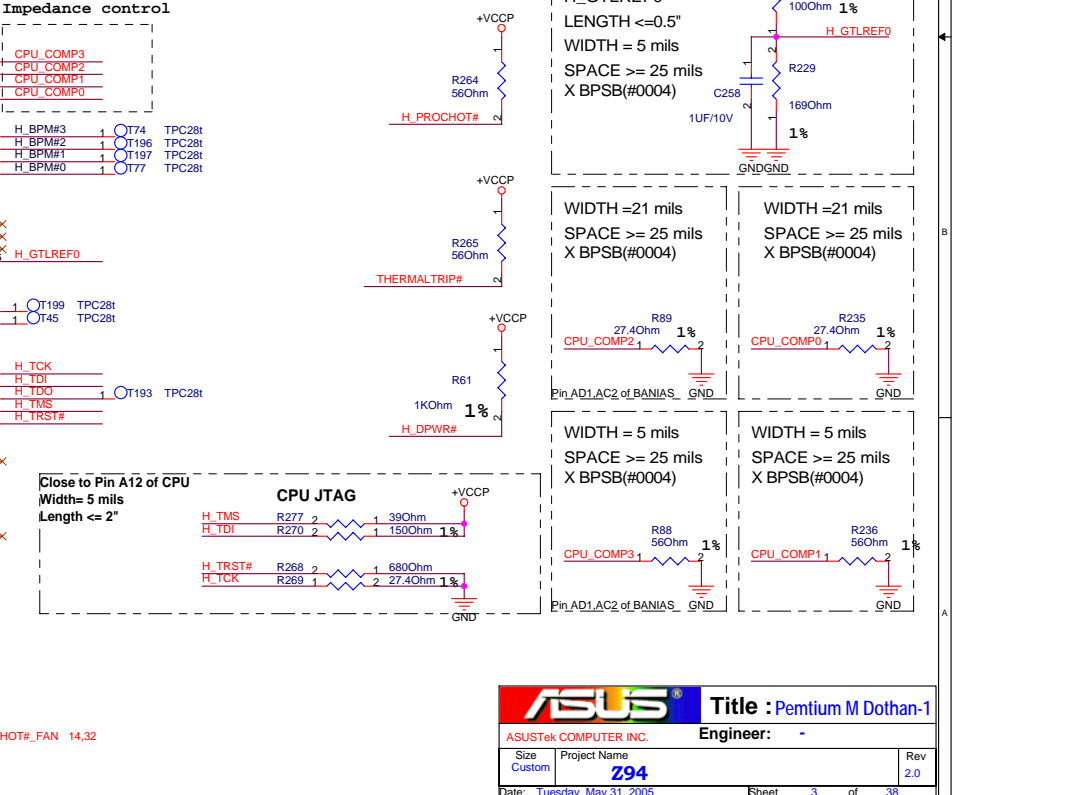
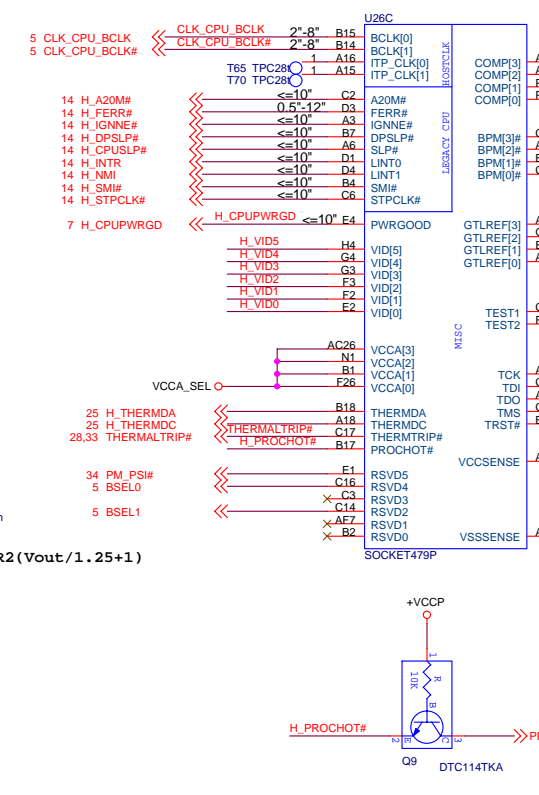
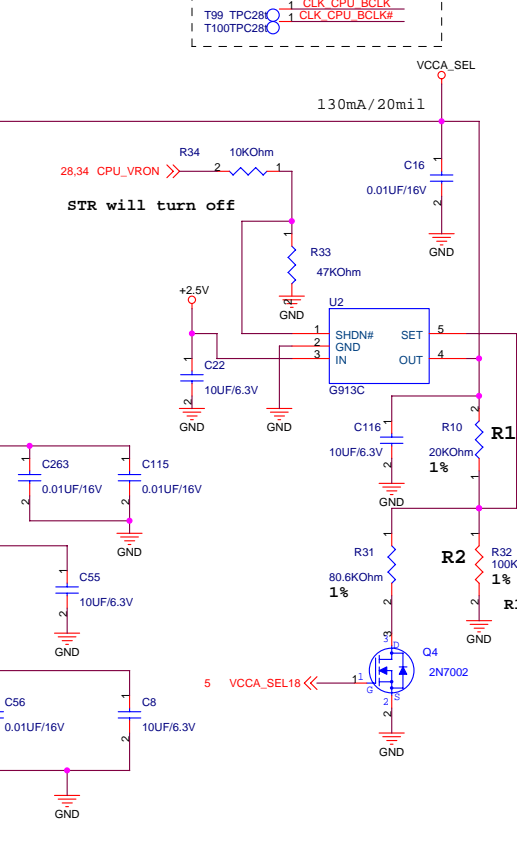


CPU Pin A1 need to be enlarged(M)

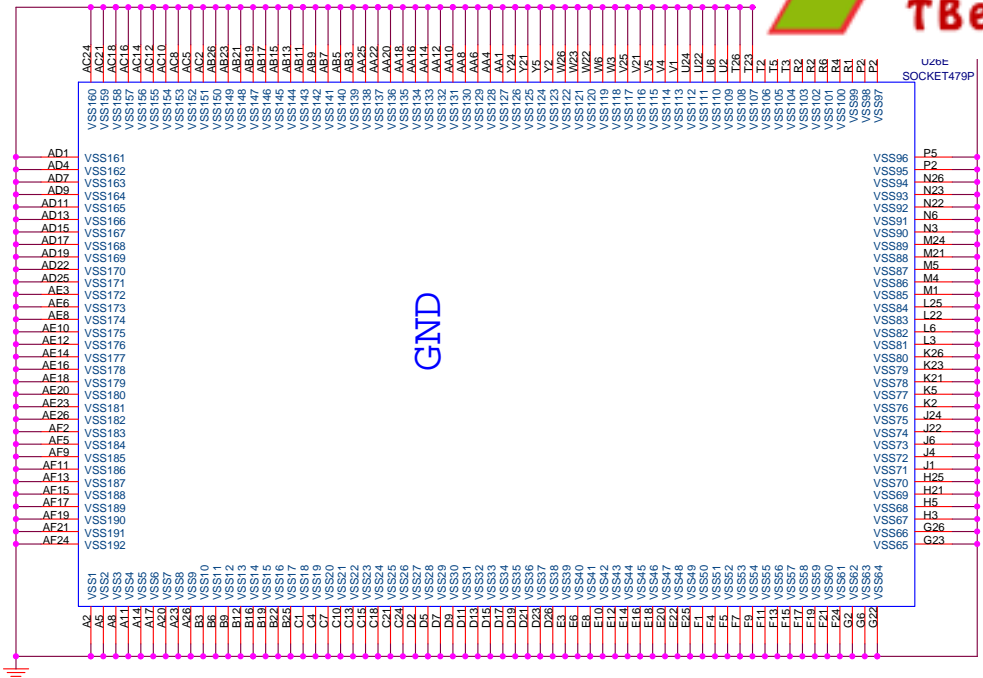
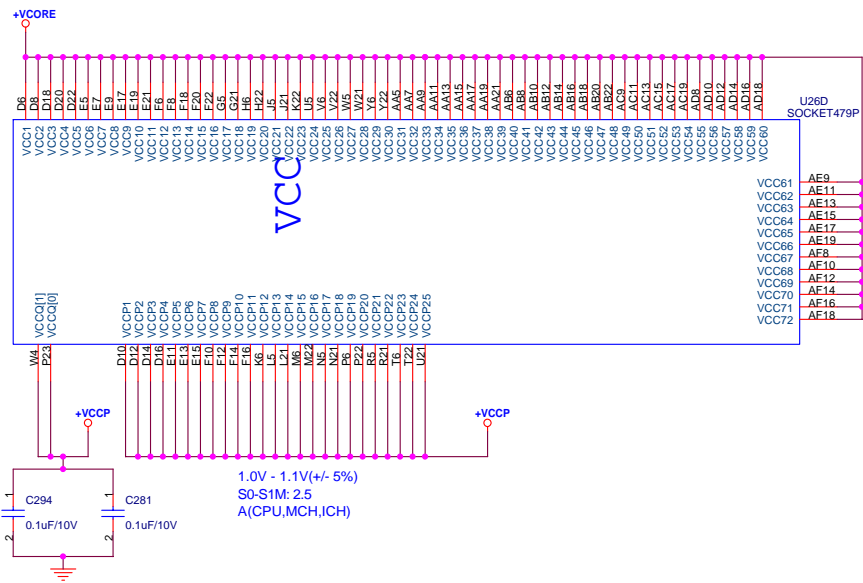


ADDR GROUP 0 > L6
 ADDR GROUP 1 > L6
 SPACE >= 1.2
 STROBE SPACE >=1.3
 GROUP SPACE >=1.5
 LENGTH: 0.5" - 6.5" (#0012)

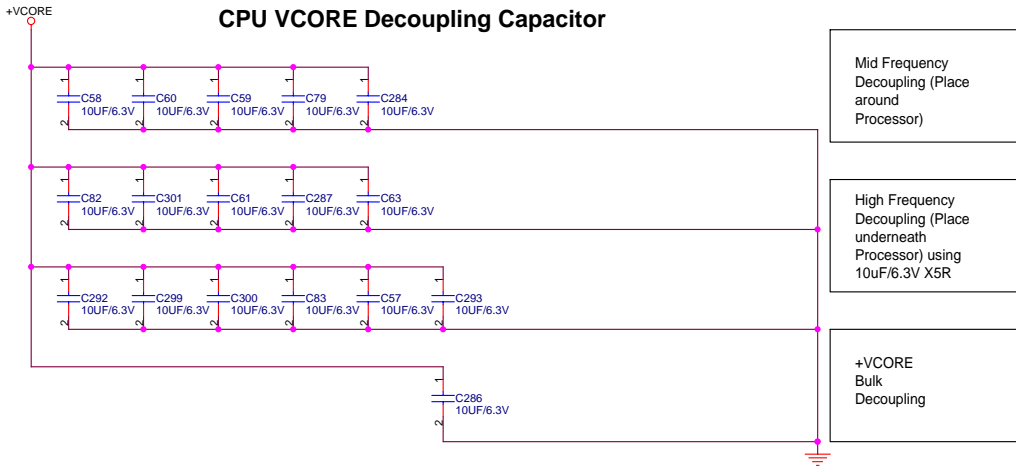
CPU PLL CIRCUITS



HFM(1.6GHz-2.13GHz): 0.726V - 1.308V(+/- 1.5%)
 1.308V C0: 23.1 A
 LFM(800MHz): C3: 8.9A
 0.988V C4: 3.7A

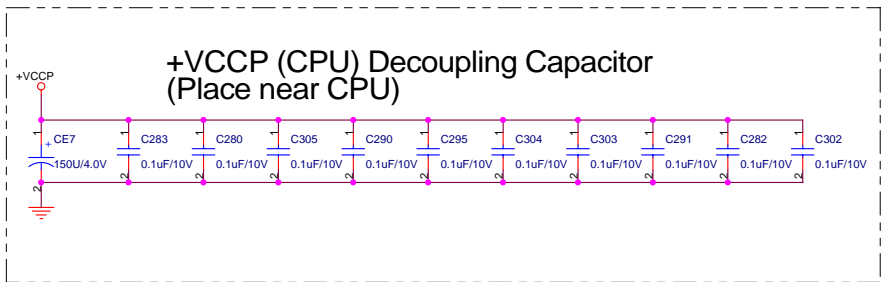


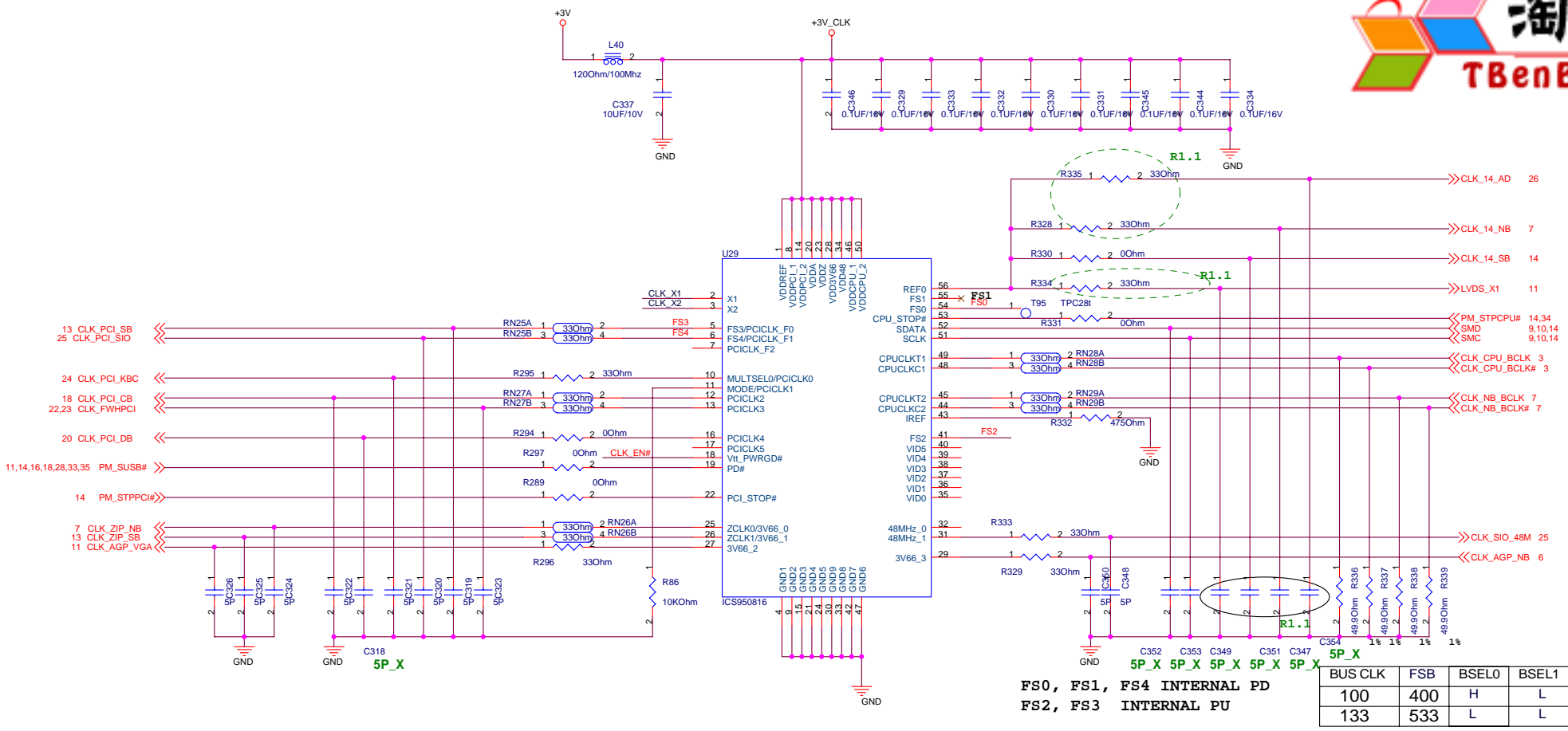
CPU VCORE Decoupling Capacitor



- Mid Frequency Decoupling (Place around Processor)
- High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R
- +VCCORE Bulk Decoupling

M3N : Four 200 uF are located in IMVP4
 A3N : Delete 10uF/6.3V from 35pcs to 17pcs

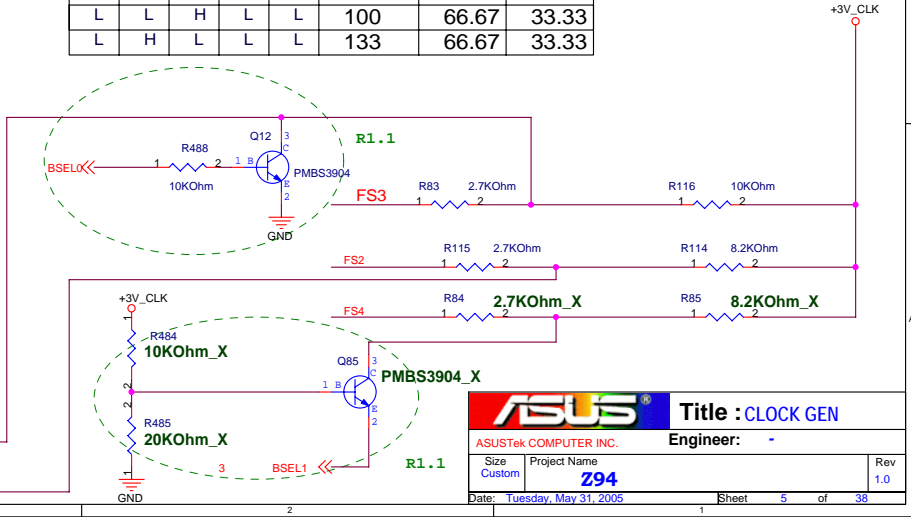
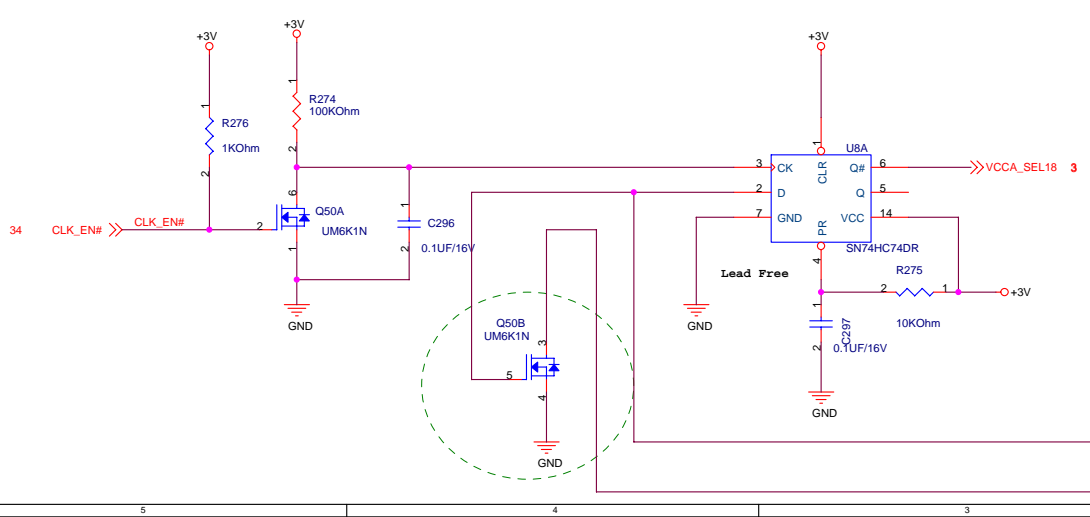




FS0, FS1, FS4 INTERNAL PD
FS2, FS3 INTERNAL PU

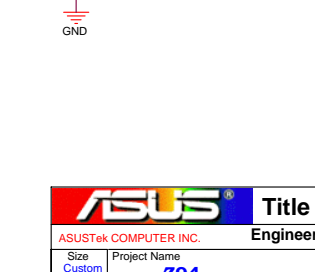
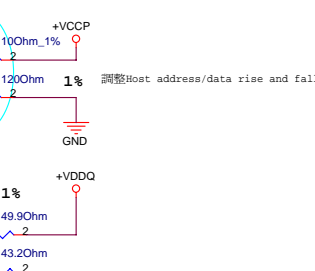
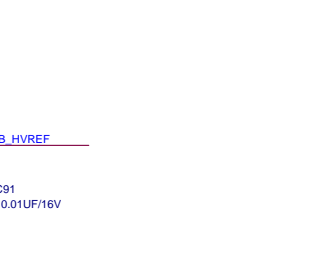
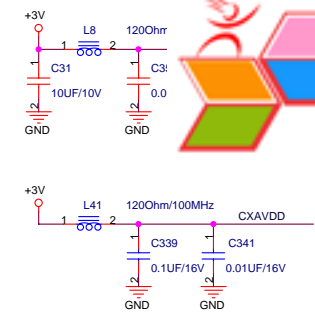
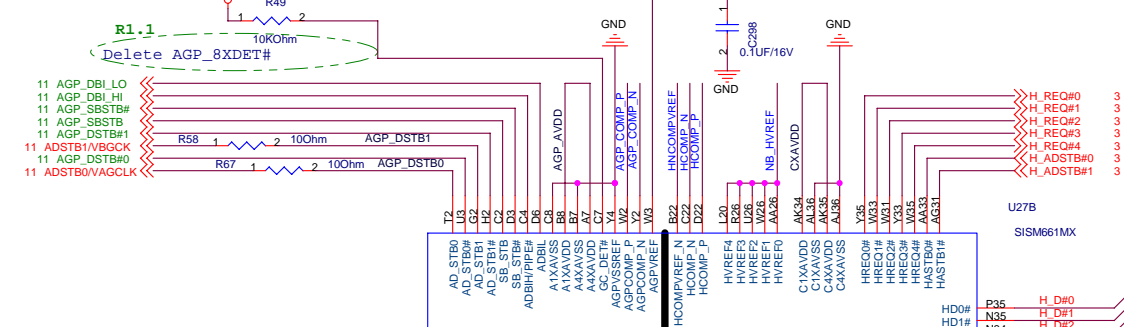
BUS CLK	FSB	BSEL0	BSEL1
100	400	H	L
133	533	L	L

FS4	FS3	FS2	FS1	FS0	CPU CLK	AGP CLK	PCI CLK
L	L	H	L	L	100	66.67	33.33
L	H	L	L	L	133	66.67	33.33



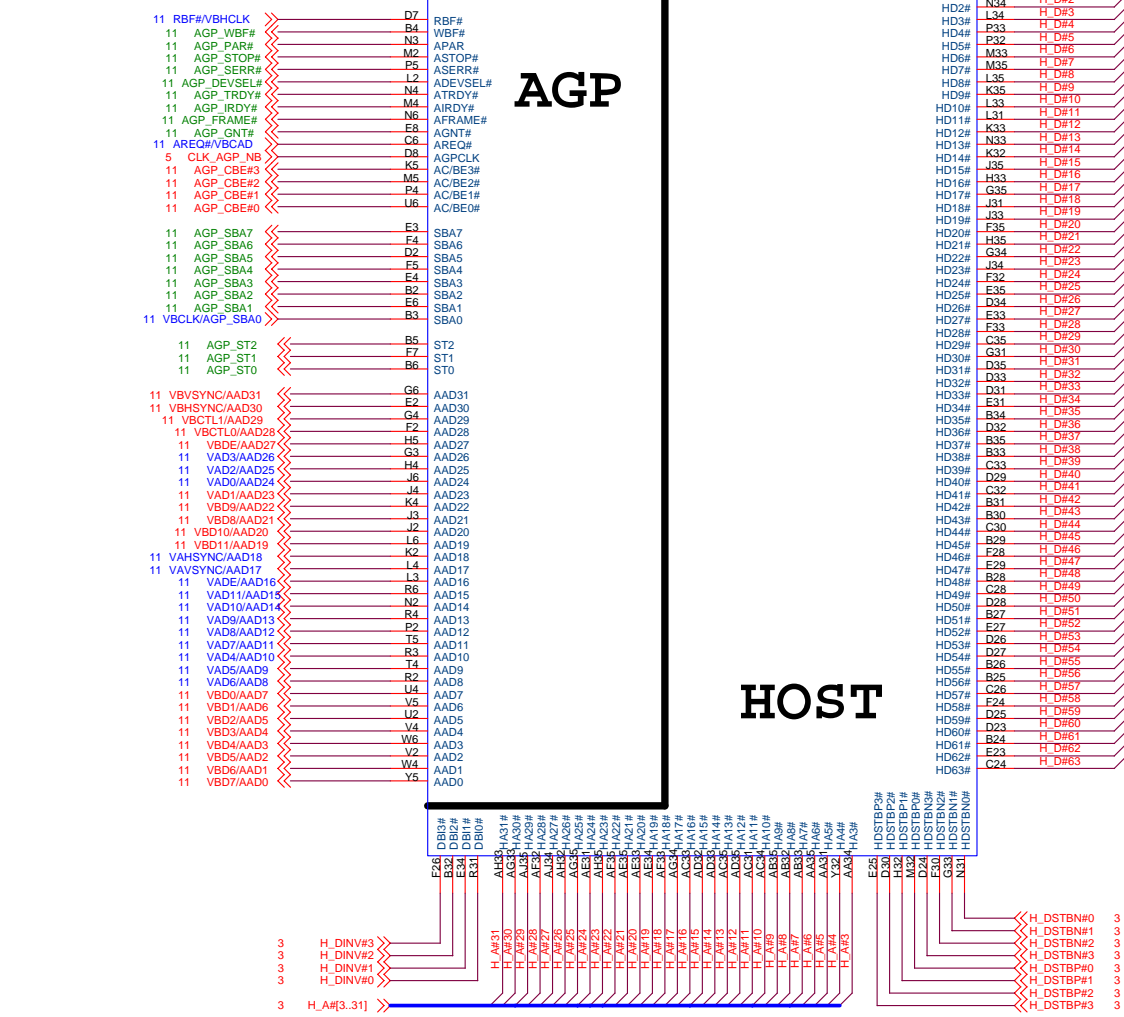


AGP_8XDET#	AGP_BUS	WGA_BUS
LO	HI	HI

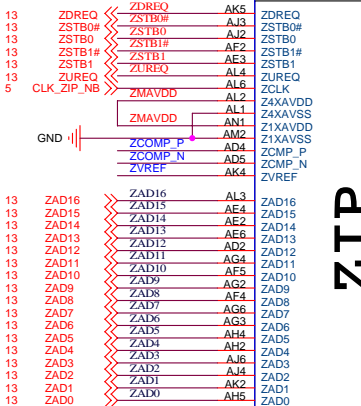
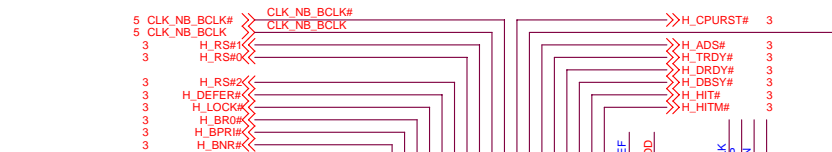


AGP

HOST

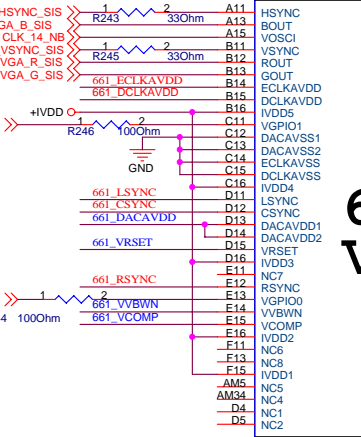


When system power ready will pass to CPU

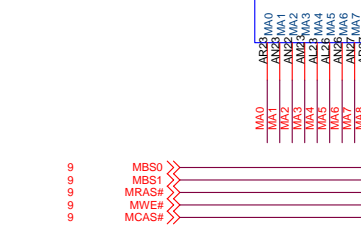


CPU IF

ZIP

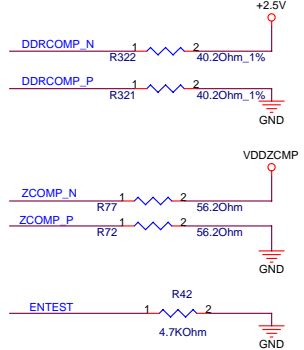
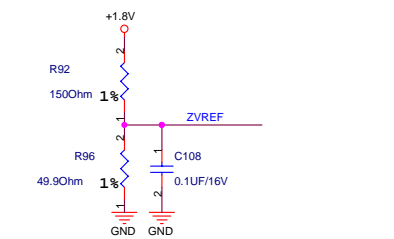
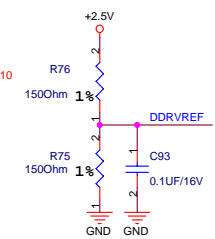
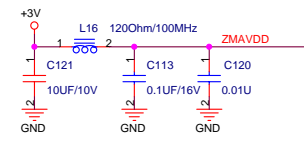
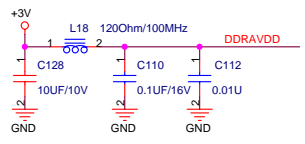
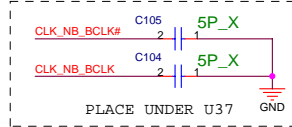
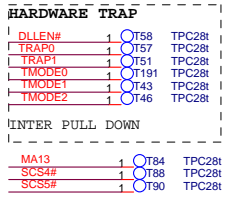
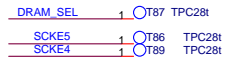
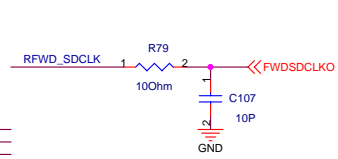
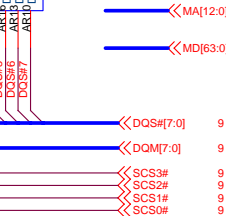


DDR

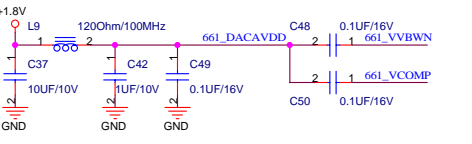
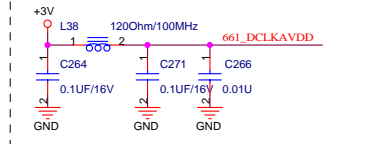


661 VGA

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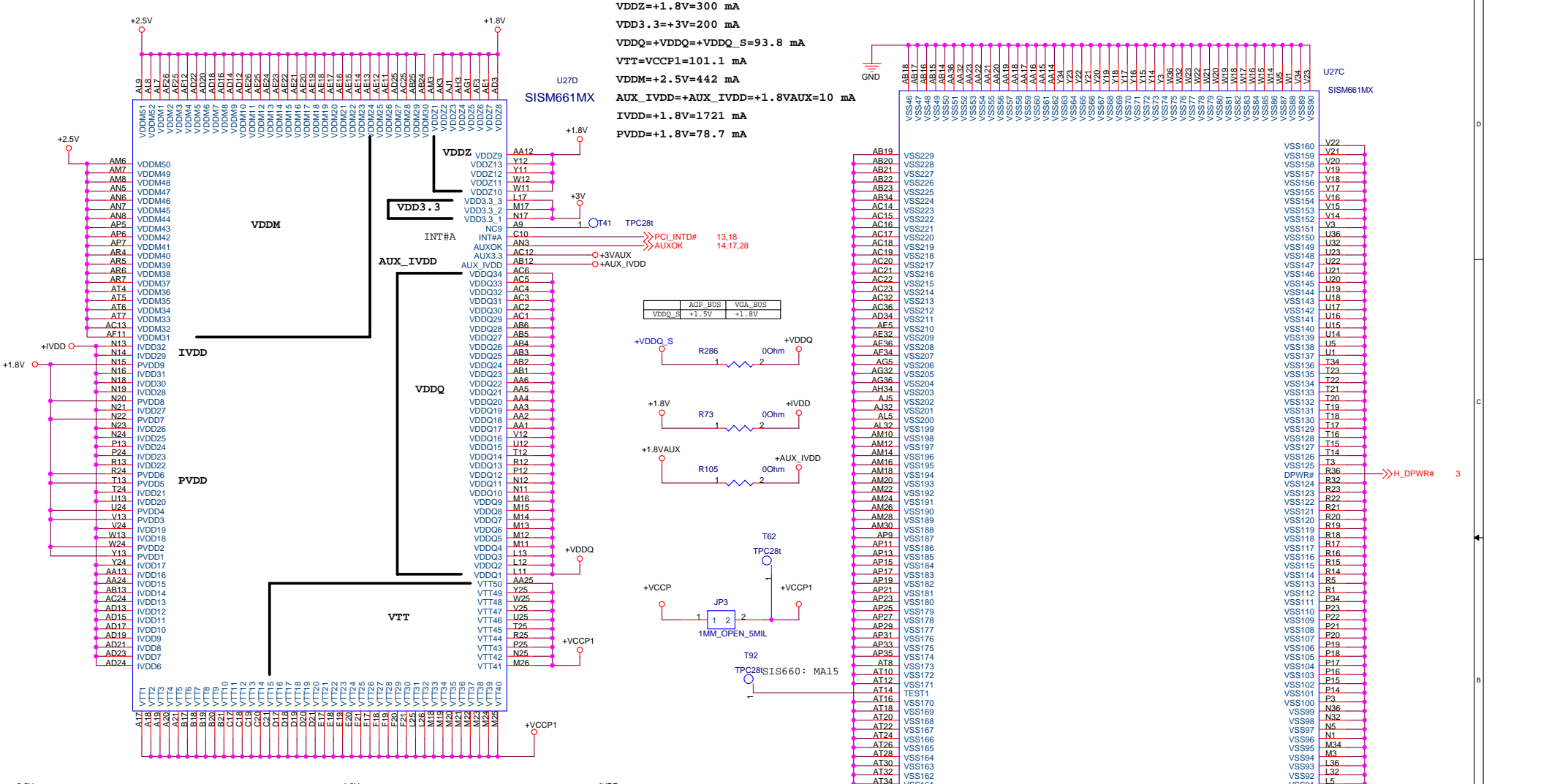


FOR SIS661 ONLY



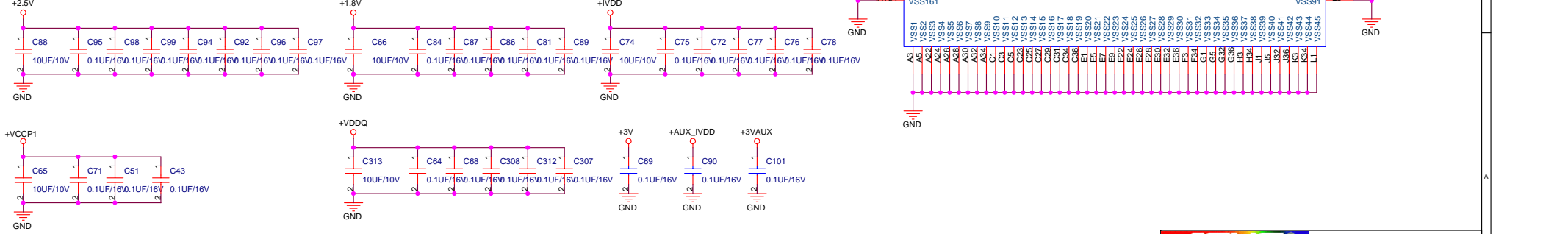
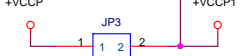
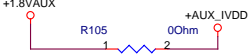
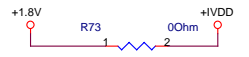
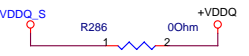
Function	Enable	Disable
RSync	VGA	1 0
LSync	TBD	0 0
CSync	TBD	0 0

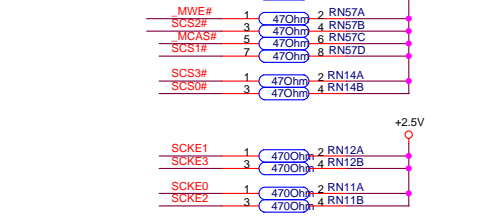
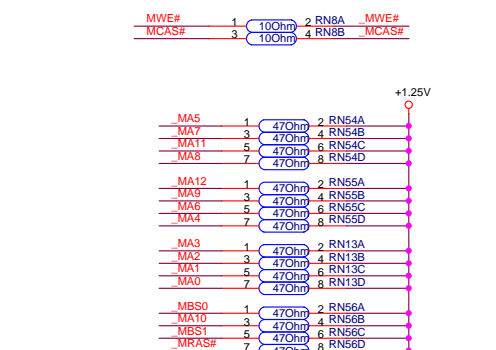
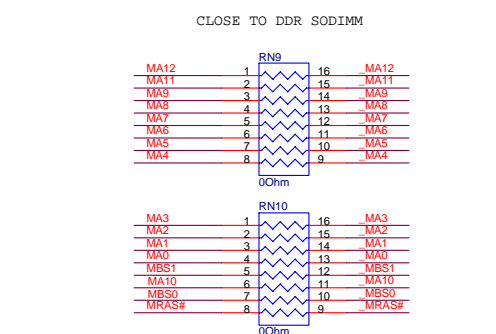
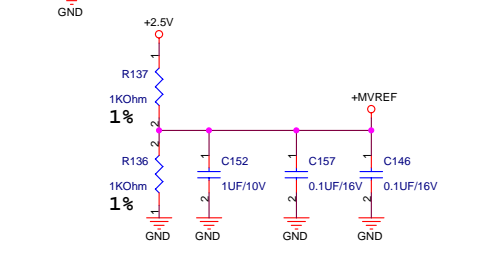
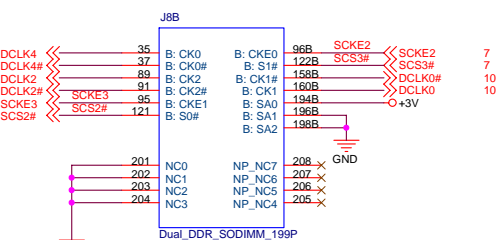
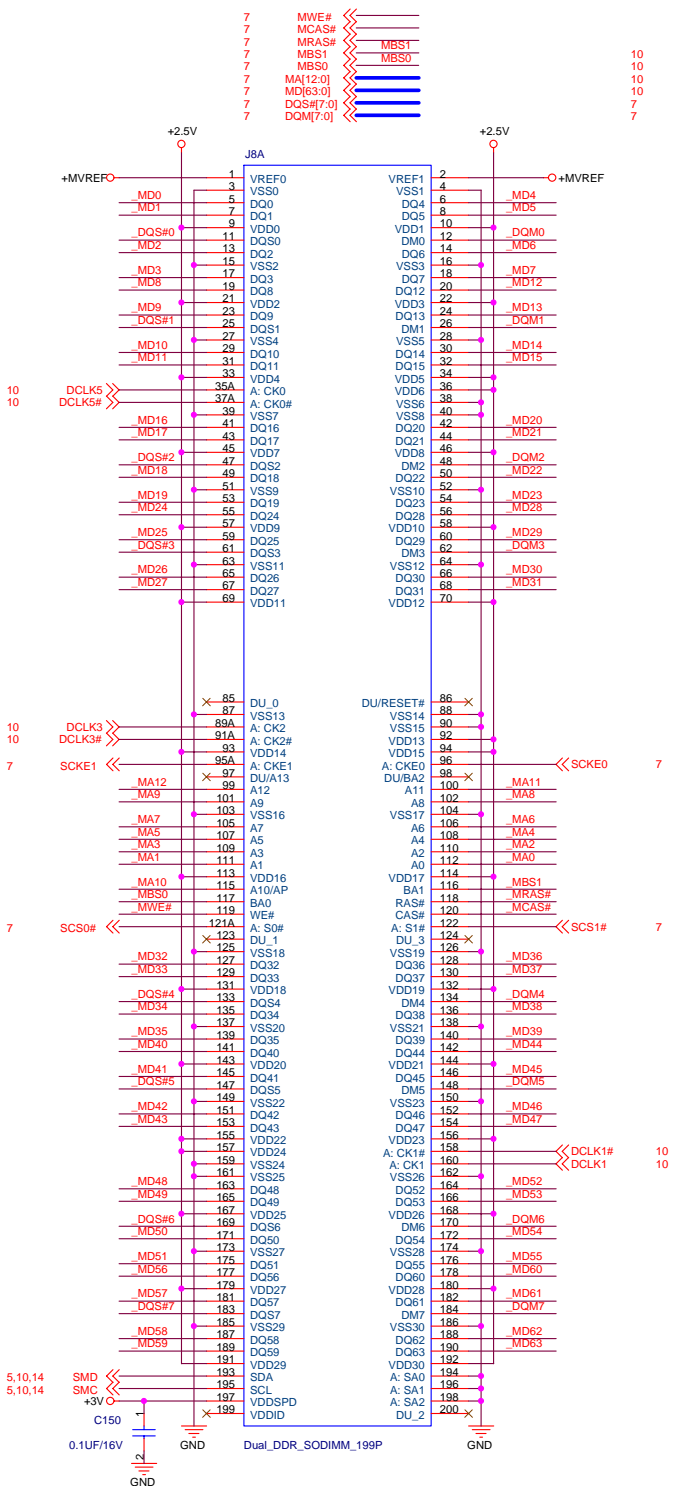
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 ASUSTek COMPUTER INC. Engineer: _____
 Size: Custom Project Name: Z94
 Date: Tuesday, May 31, 2005 Sheet 7 of 38 Rev 2.0



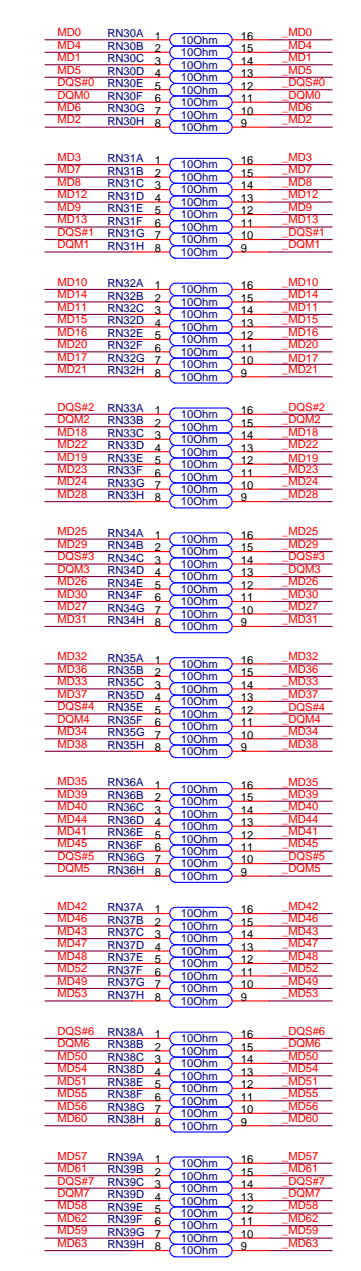
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VDD3.3=+3V=200 mA
VDDQ=+VDDQ+VDDQ_S=93.8 mA
VTT=VCCP1=101.1 mA
VDDM=+2.5V=442 mA
AUX_IVDD=+AUX_IVDD=+1.8VAUX=10 mA
IVDD=+1.8V=1721 mA
FVDD=+1.8V=78.7 mA

	AGP_BUS	VGA_BUS
VDDQ_S	+1.5V	+1.8V

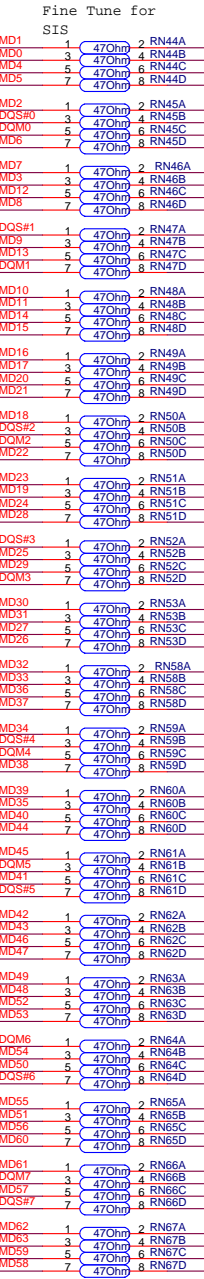




CLOSE TO DDR SODIMM



CHANGE TO 47 OHM



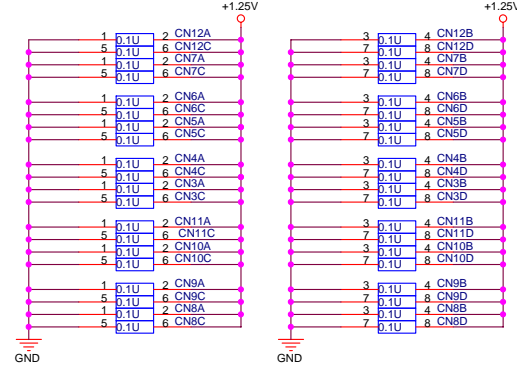
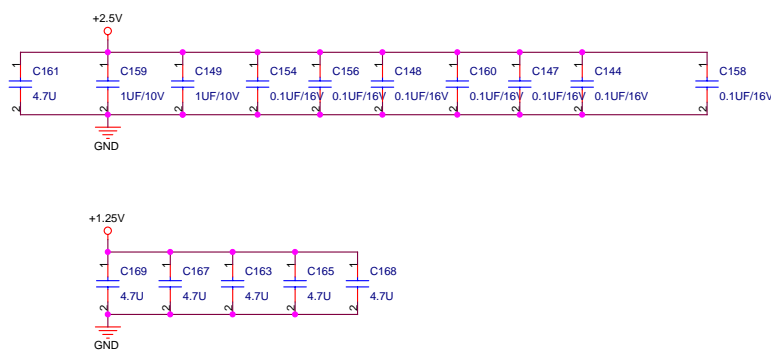
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ASUSTek COMPUTER INC. Engineer: _____

Size: Custom Project Name: **Z94**

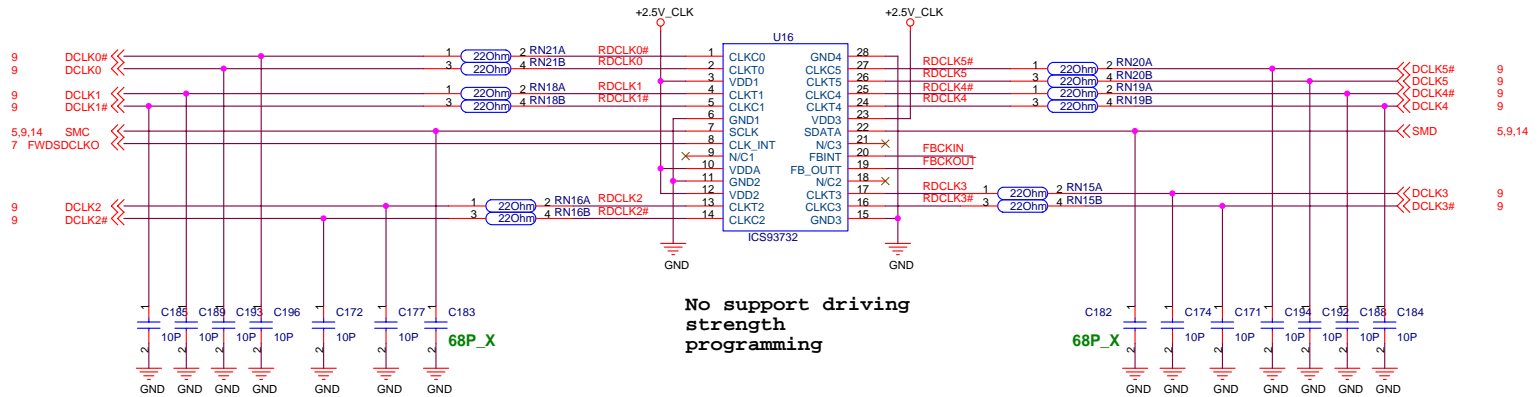
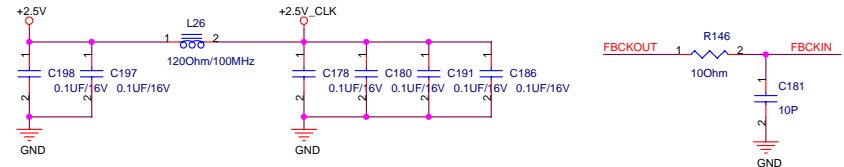
Date: Tuesday, May 31, 2005 Sheet 9 of 38

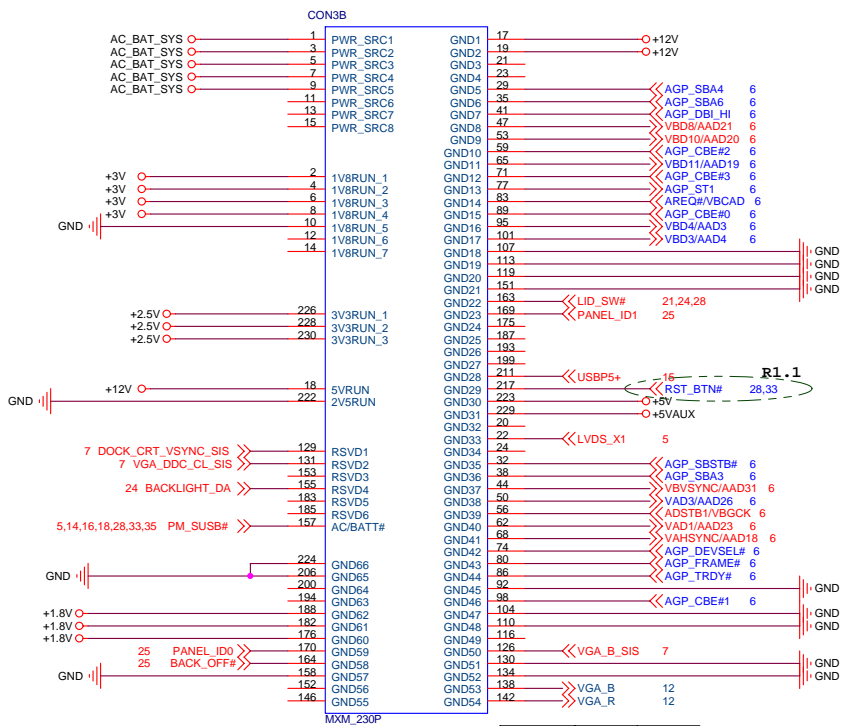
Close to DDR socket



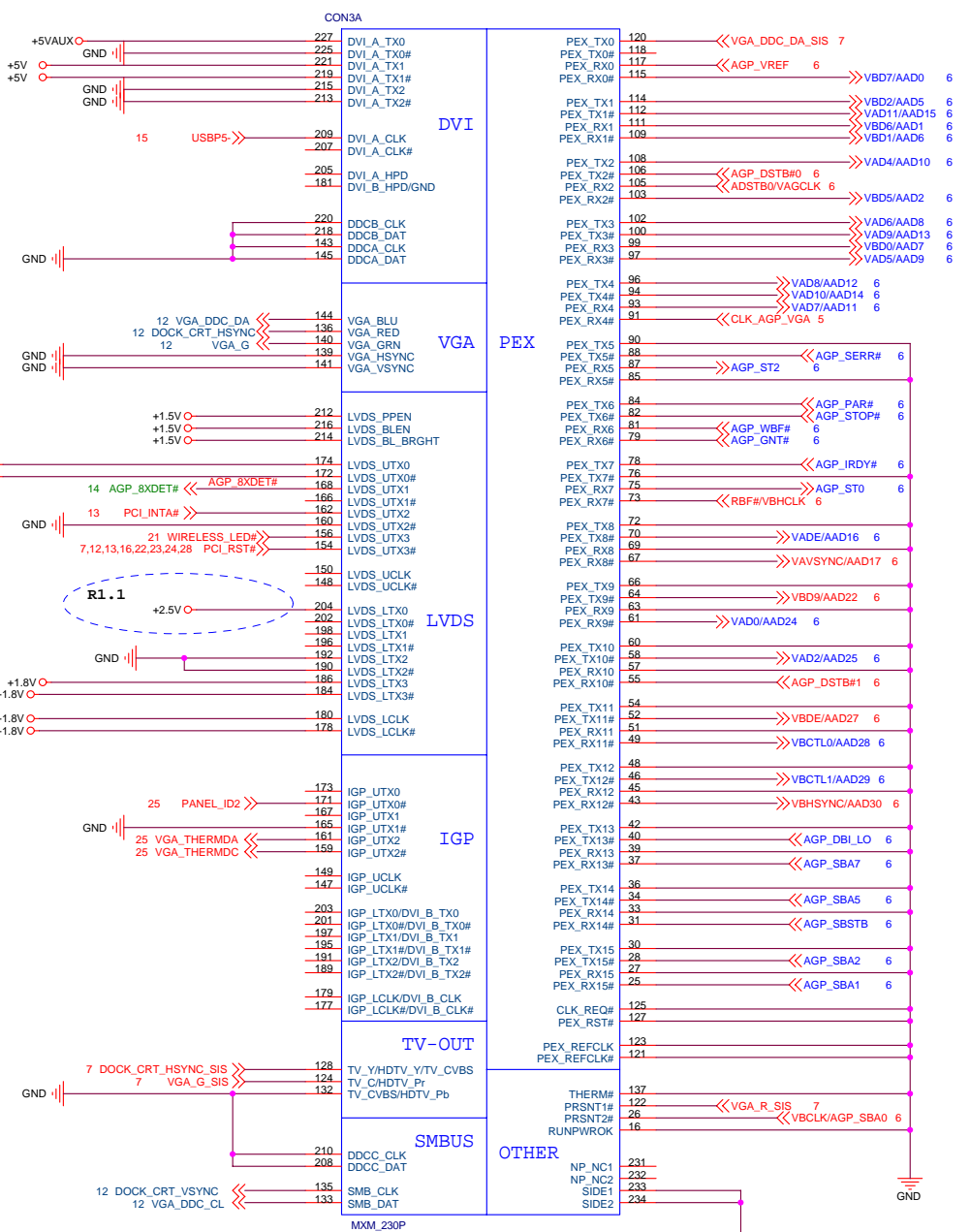
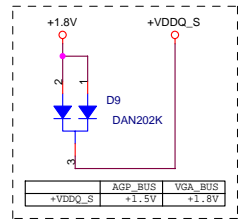
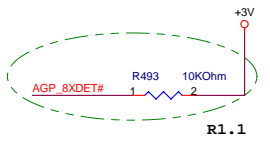
0.1U OP X 4

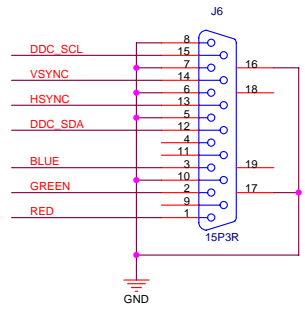
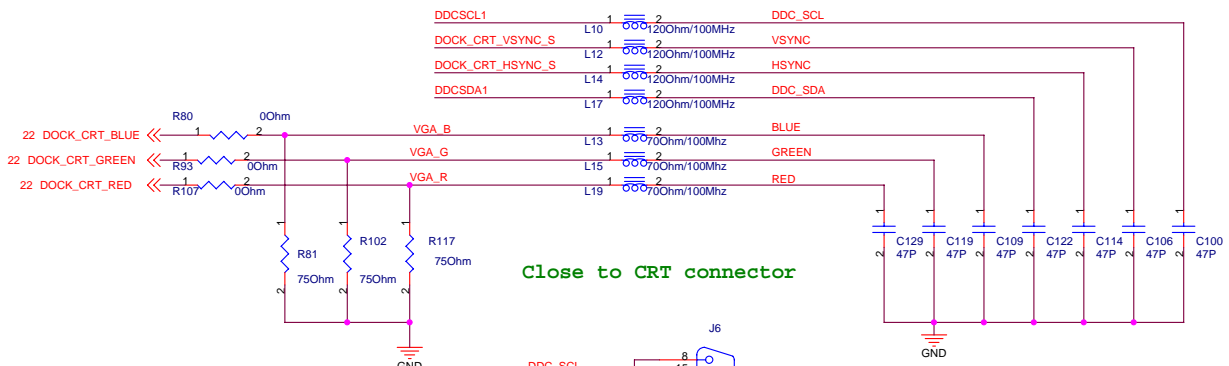
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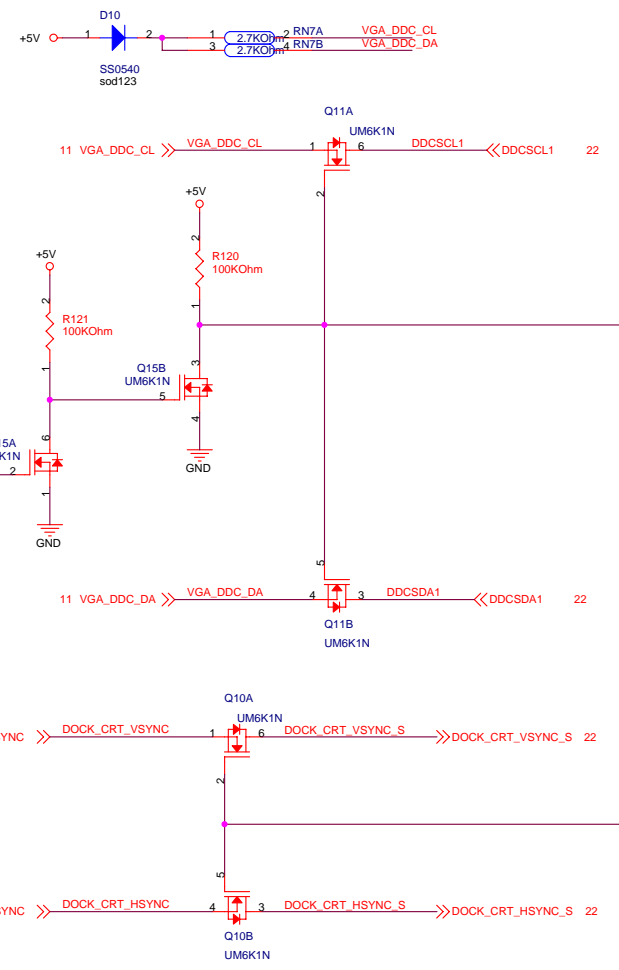
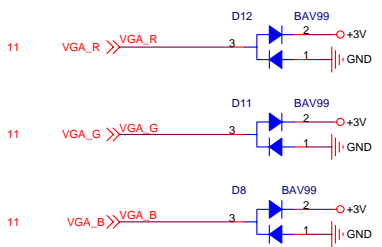


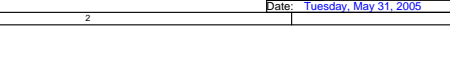
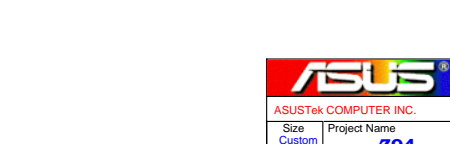
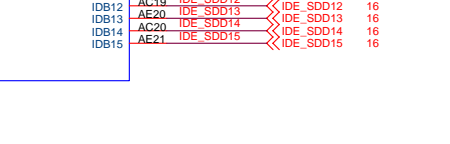
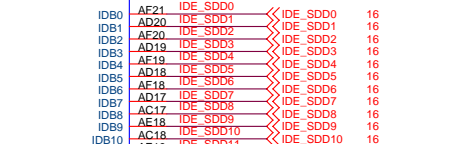
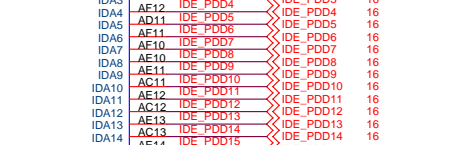
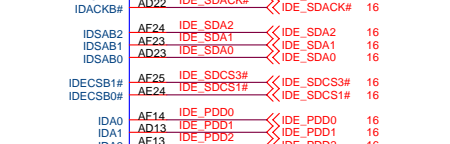
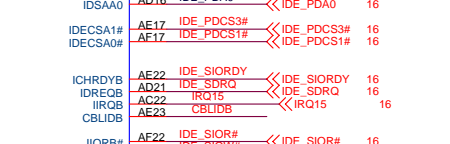
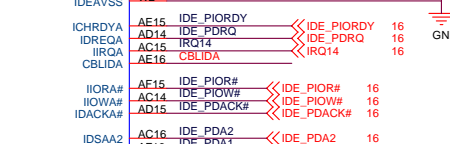
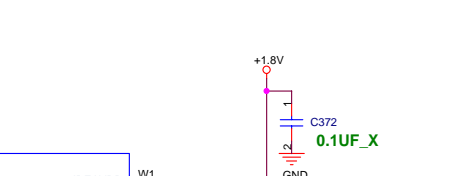
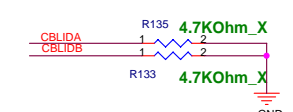
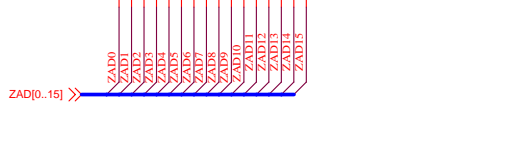
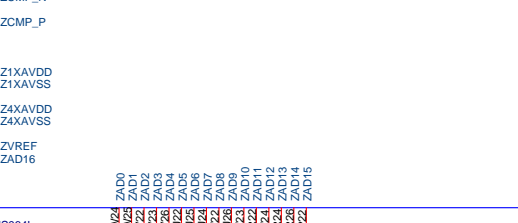
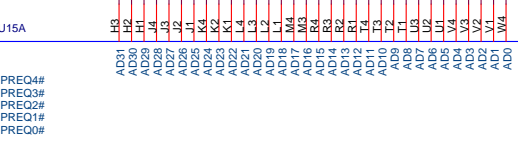
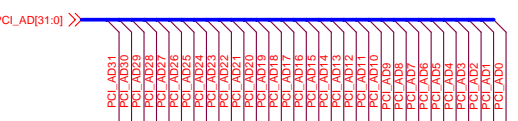
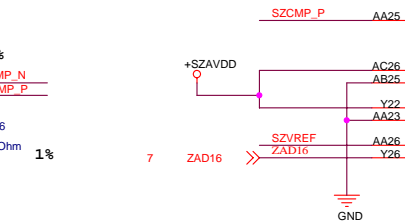
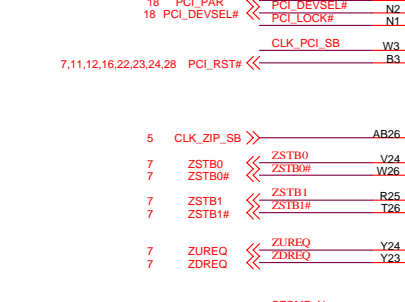
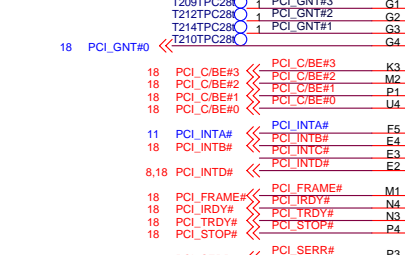
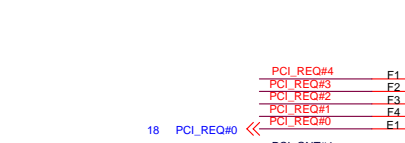
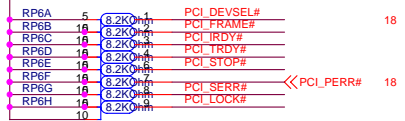
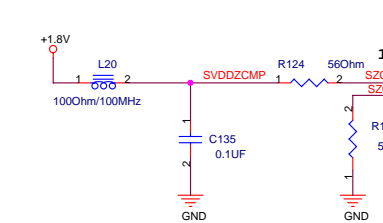
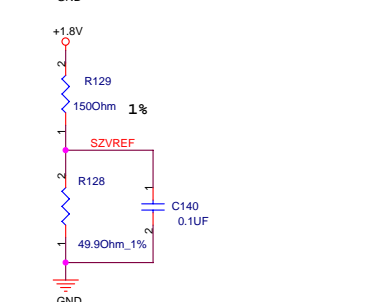
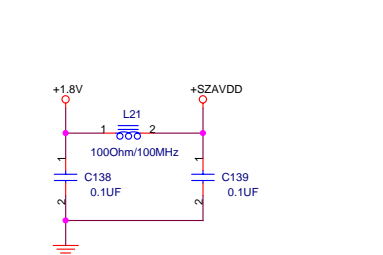
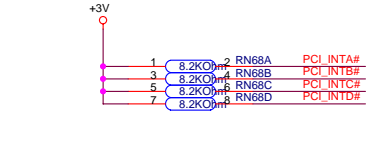
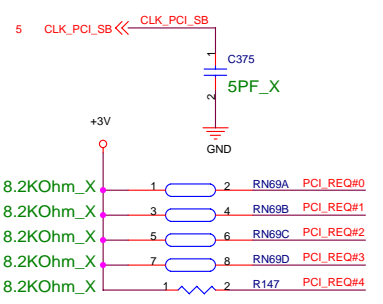
1. AC_BAT_SYS ----> 2 A
2. +12V = 0.5A
3. +5V = 1.5A
4. +3V = 1.5A
5. +2.5V = 2.0A
6. +1.8V = 2.0A
7. +5VAUX = 1.0A
7. +1.5V----> 0.5A

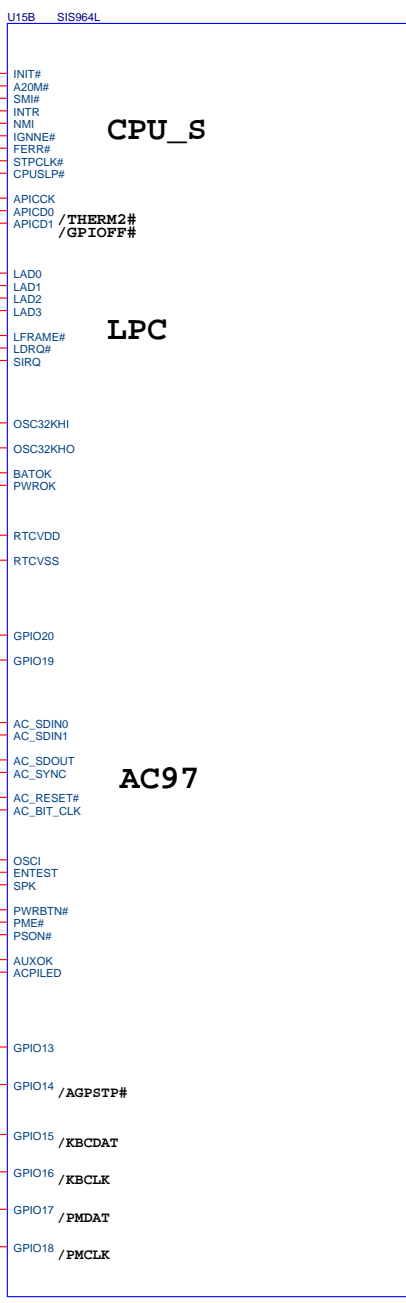
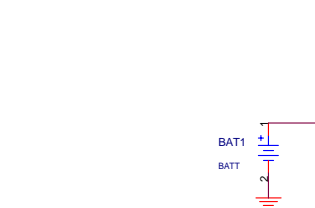
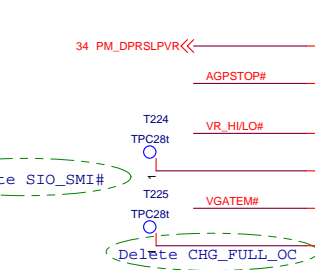
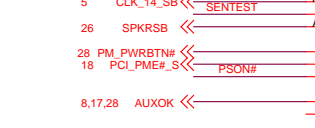
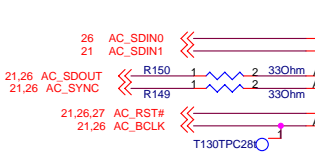
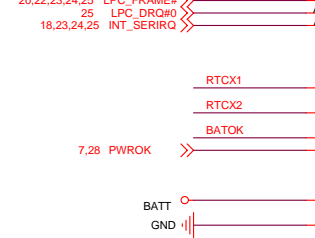
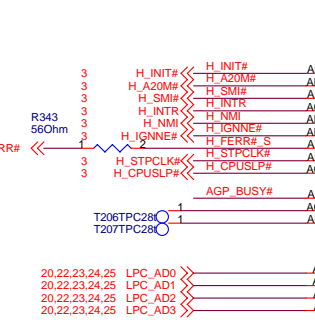
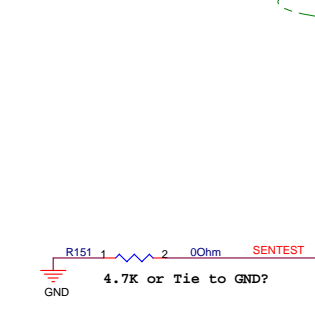
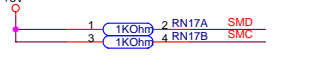
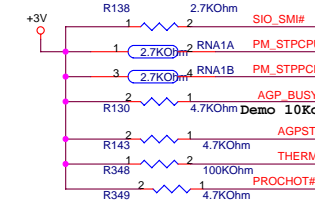
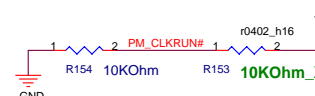
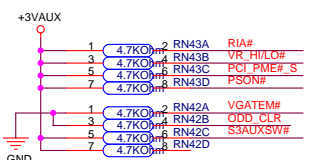
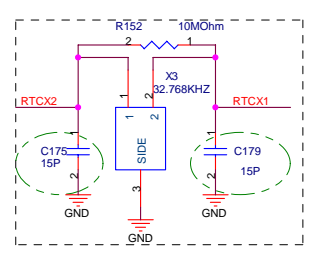
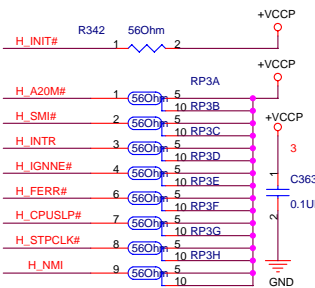




CRT connector



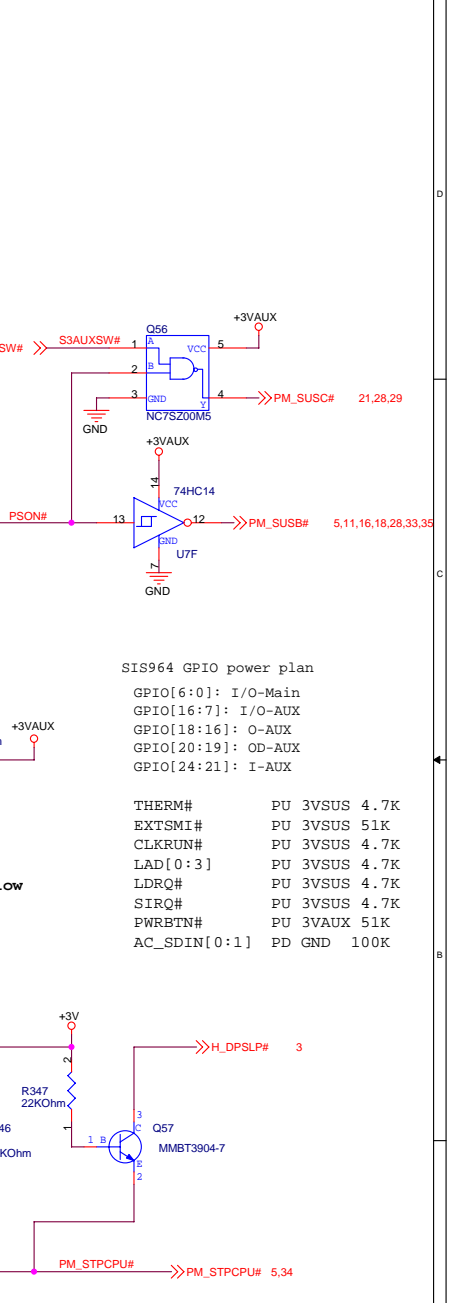
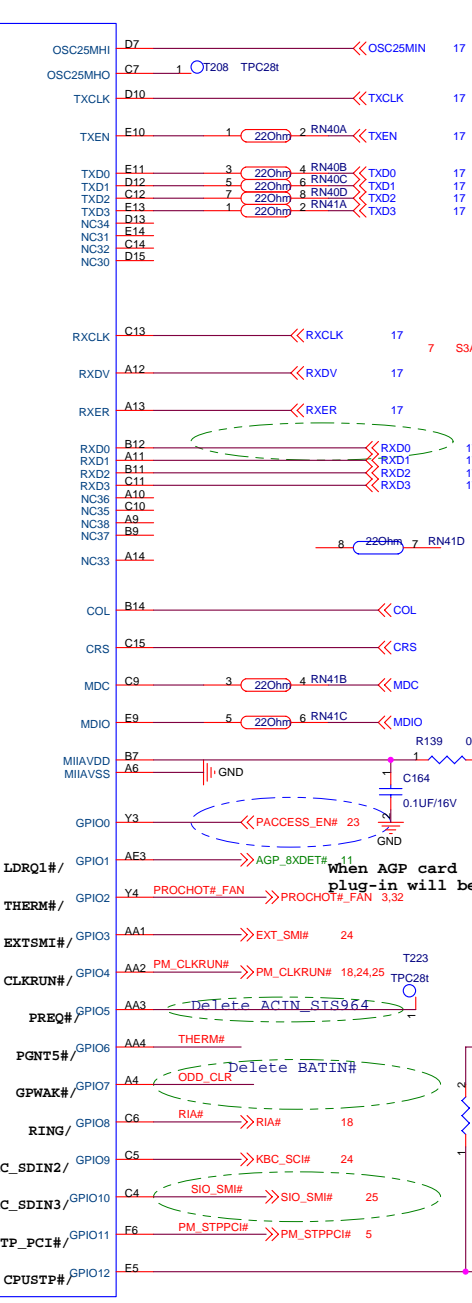




CPU_S

LPC

AC97



SIS964 GPIO power plan
 GPIO[6:0]: I/O-Main
 GPIO[16:7]: I/O-AUX
 GPIO[18:16]: O-AUX
 GPIO[20:19]: OD-AUX
 GPIO[24:21]: I-AUX

THERM# PU 3VSUS 4.7K
 EXTSMI# PU 3VSUS 51K
 CLKRUN# PU 3VSUS 4.7K
 LAD[0:3] PU 3VSUS 4.7K
 LDRQ# PU 3VSUS 4.7K
 SIRQ# PU 3VSUS 4.7K
 PWRBTN# PU 3VAUX 51K
 AC_SDIN[0:1] PD GND 100K

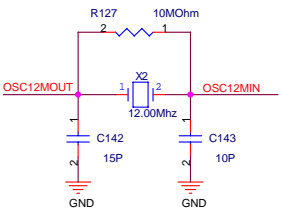
when AGP card plug-in will be low

Delete ACTN_SIS964
 Delete BATIN#
 Delete SIO_SMI#

RTC Battery

ASUS Title : SIS964L_LPC/AC97/GPIO
 ASUSTek COMPUTER INC. Engineer: -
 Size Project Name
 Custom T19
 Date: Tuesday, May 31, 2005 Sheet 14 of 38

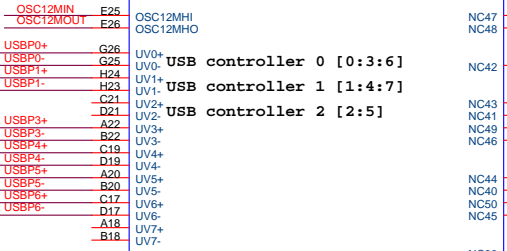
USB frequency



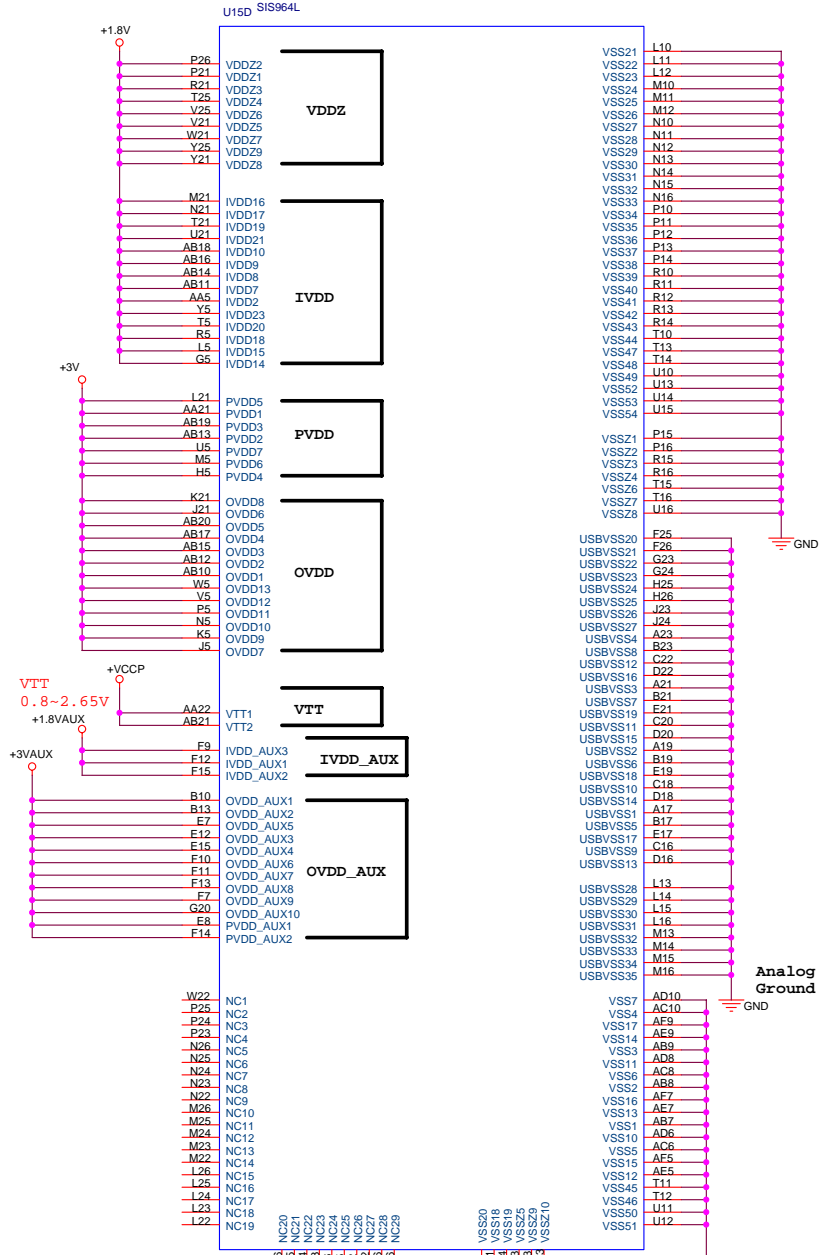
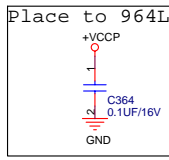
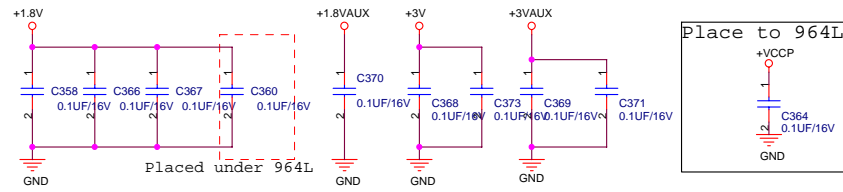
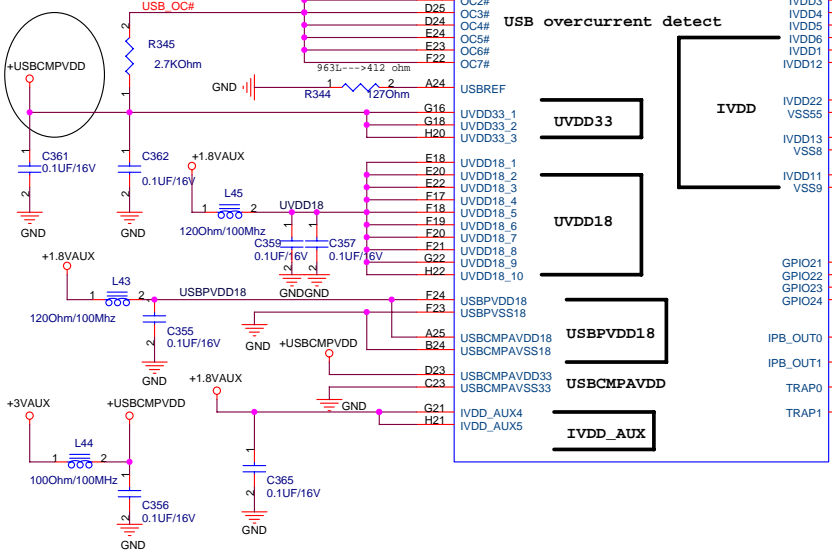
UVDD33=+3VAUX=1mA
 UVDD18=UVDD18=+1.8VAUX=274.1mA
 USBPVD18=USBPVDD18=+1.8VAUX=7.9 mA
 USBCMPVDD=+USBCMPVDD=+3VAUX=8.5 mA
 IVDD_AUX=+1.8VAUX=31.1mA

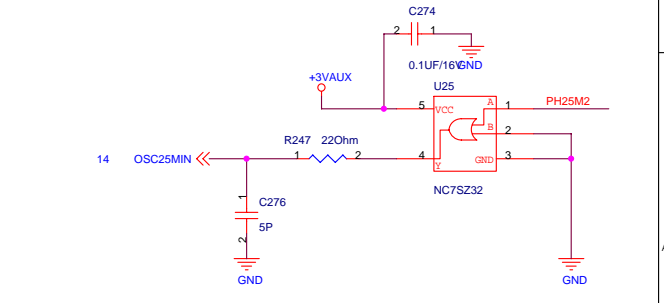
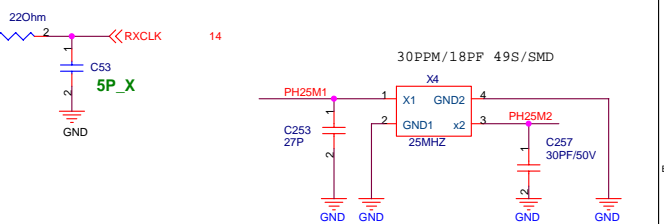
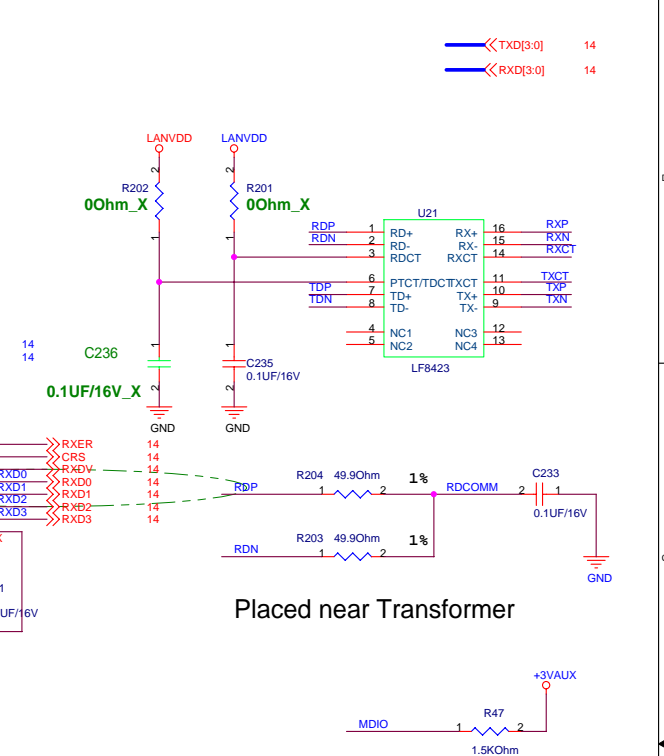
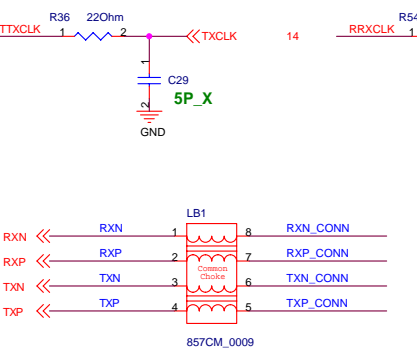
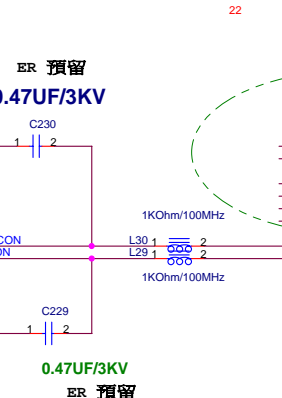
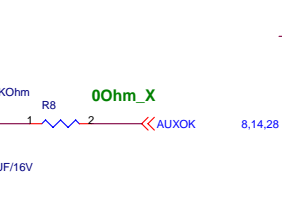
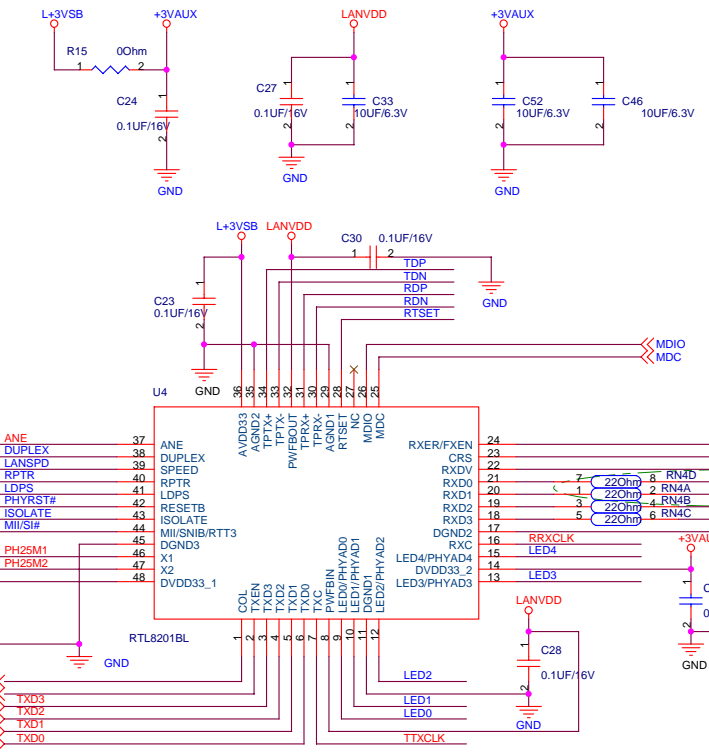
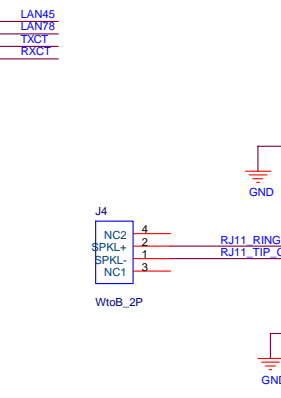
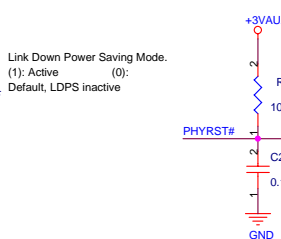
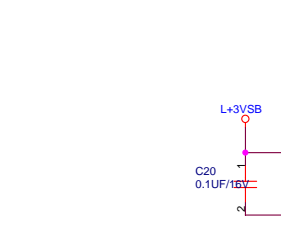
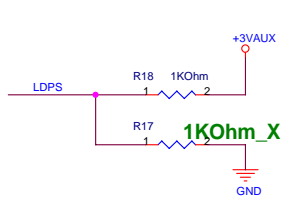
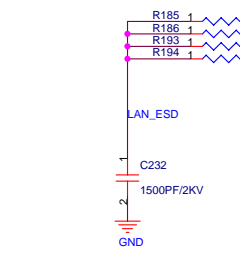
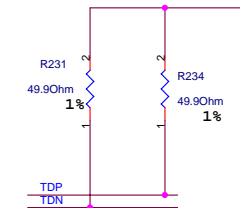
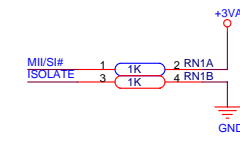
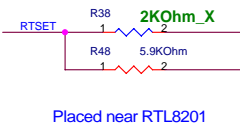
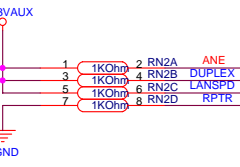
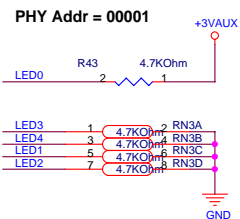
VDDZ=+1.8V=20 mA
 IVDD=+1.8V=517.4 mA
 PVDD=+3V=55 mA
 OVDD=+3V=55 mA
 VTT=+VCCP=28.7 mA
 IVDD_AUX=+1.8VAUX=31.1 mA
 OVDD_AUX=+3VAUX=52 mA

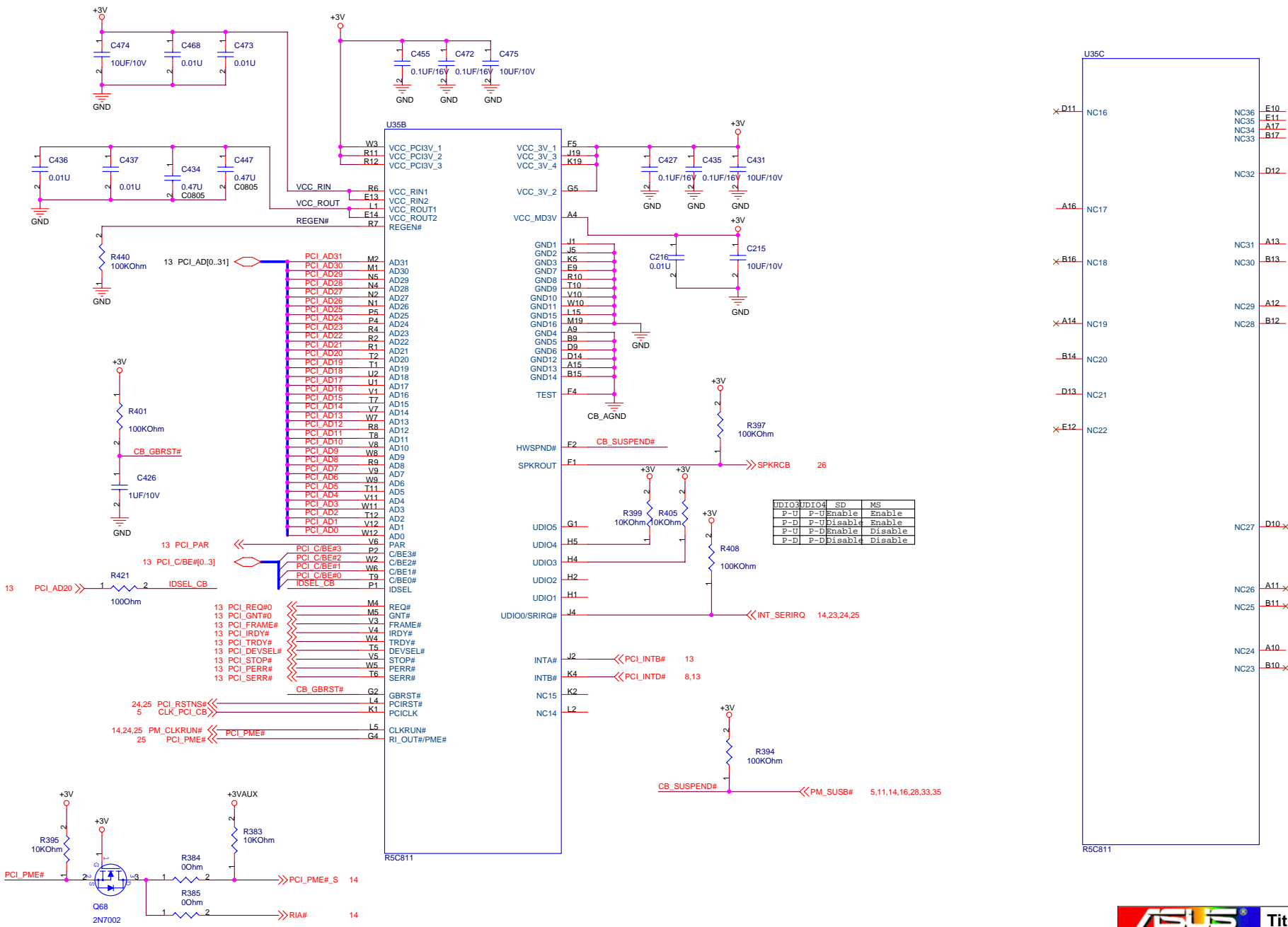
SIS964L



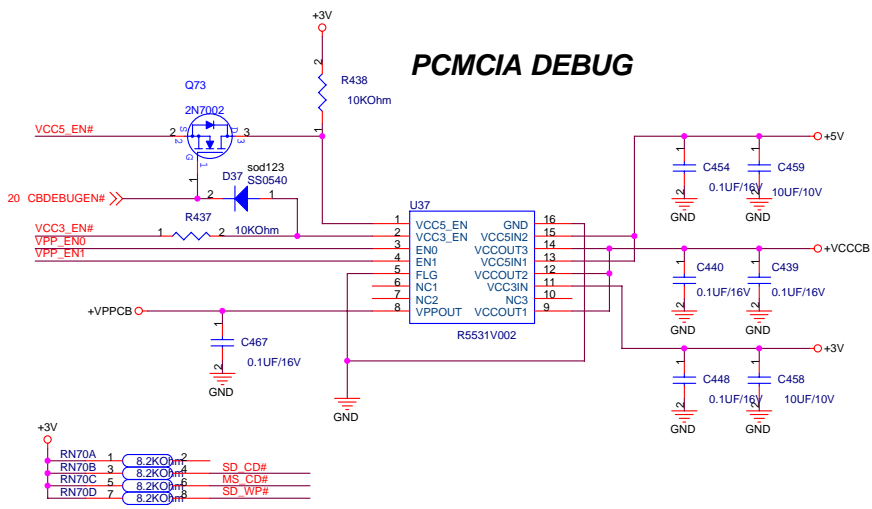
USB overcurrent detect





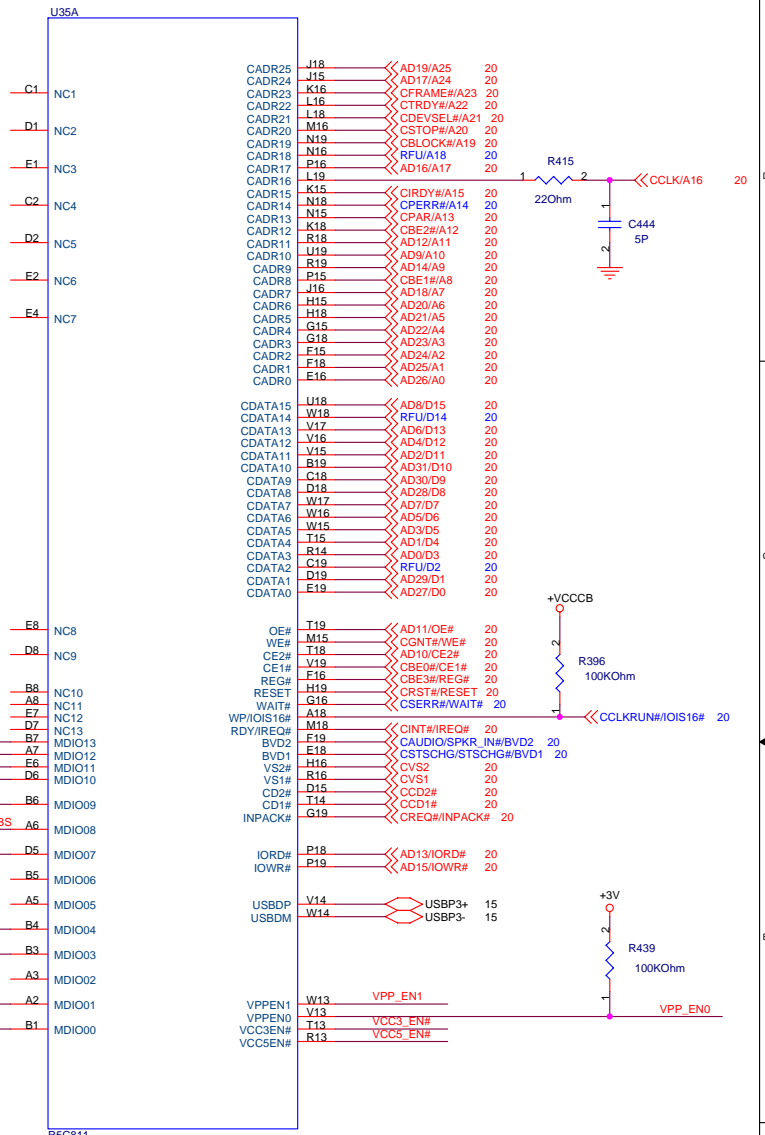


PCMCIA DEBUG



- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/ MS Power Control
- MDIO07--> SD External Clock/ MS External Clock
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

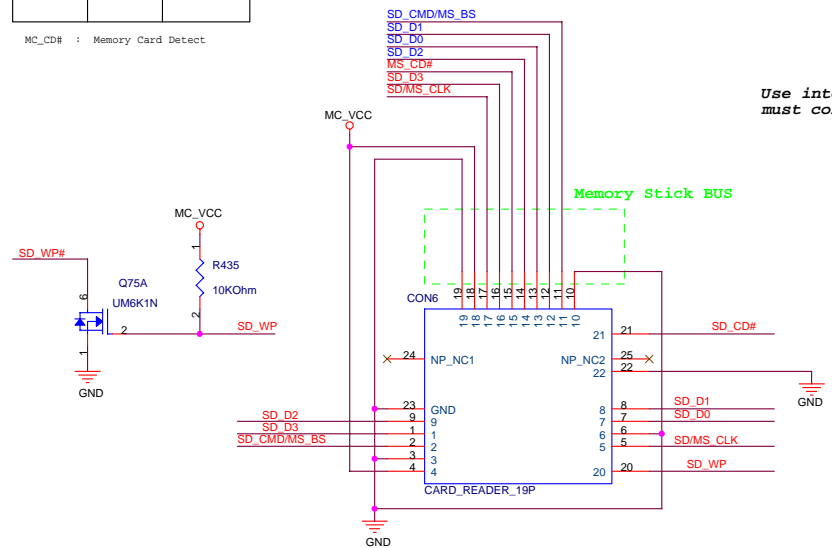
- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE



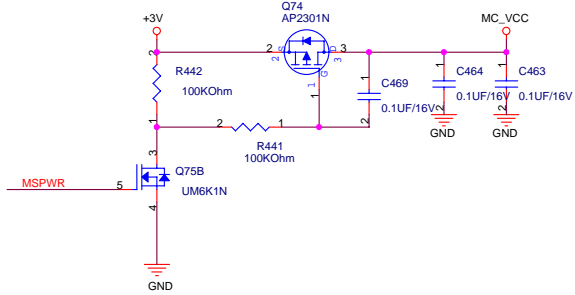
Memory Card Detect

MS_CD#	SD_CD#	Not Support
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

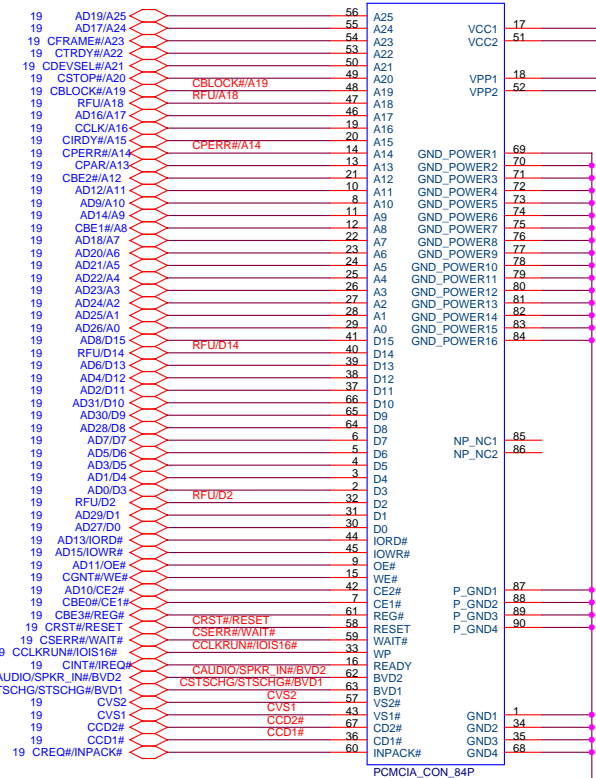
MC_CD# : Memory Card Detect



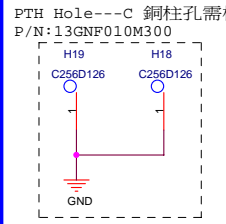
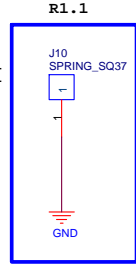
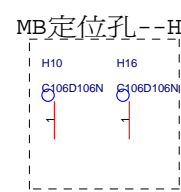
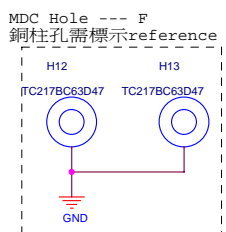
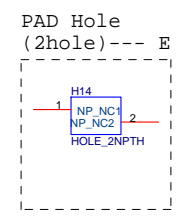
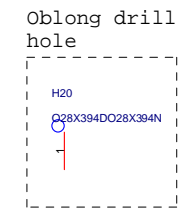
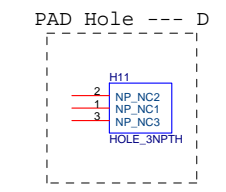
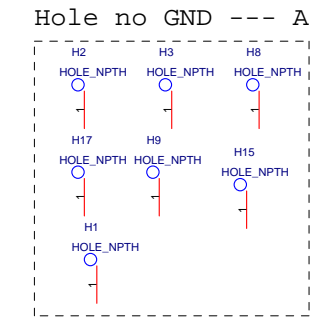
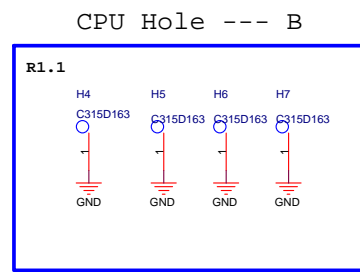
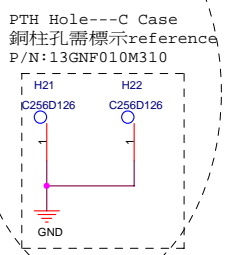
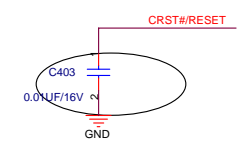
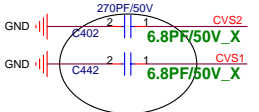
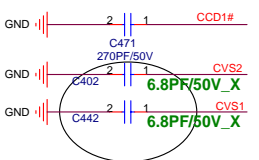
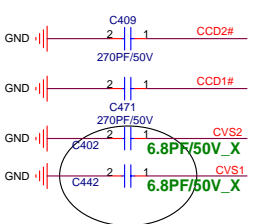
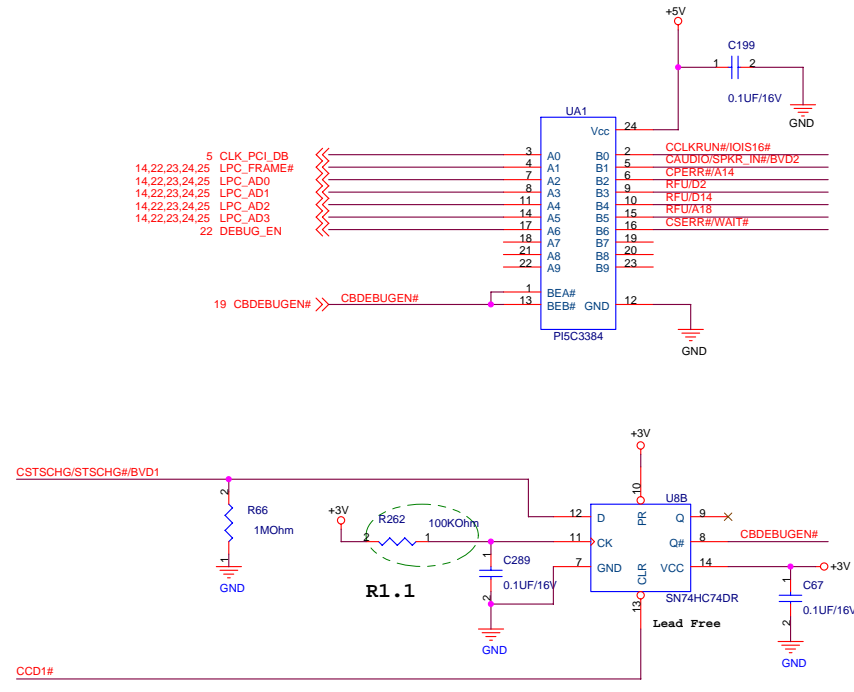
Use internal PCI clock MDIO07 must connect to GND

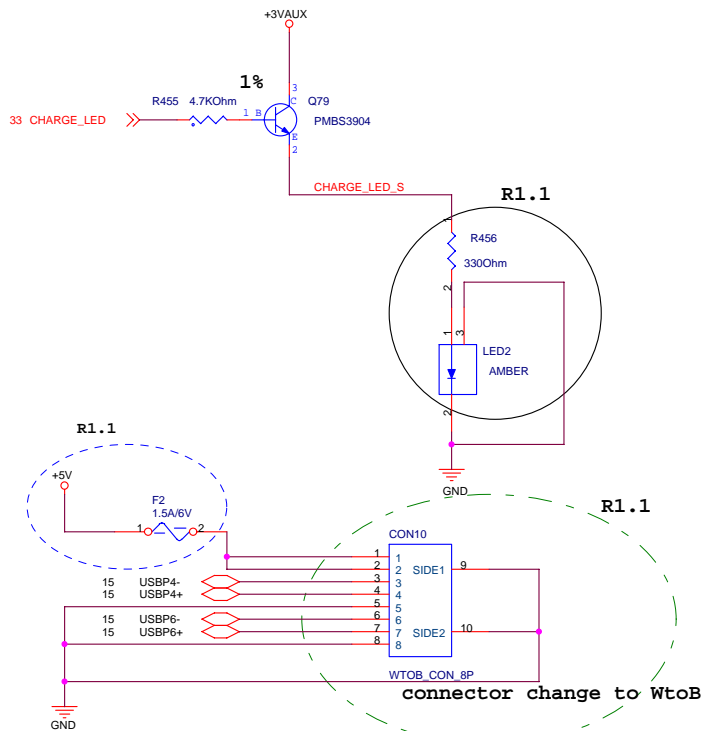
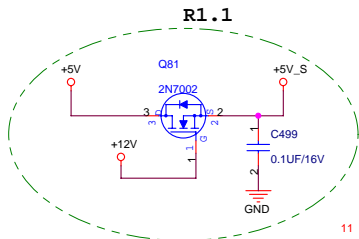
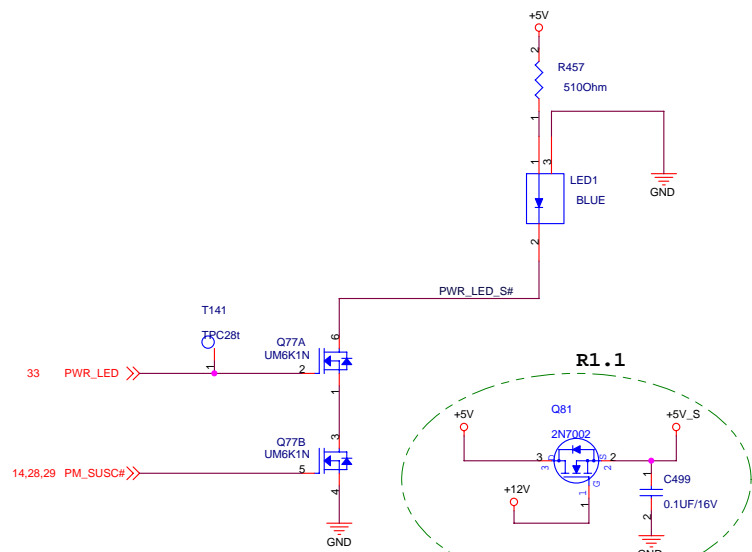


PCMCIA SOCKET

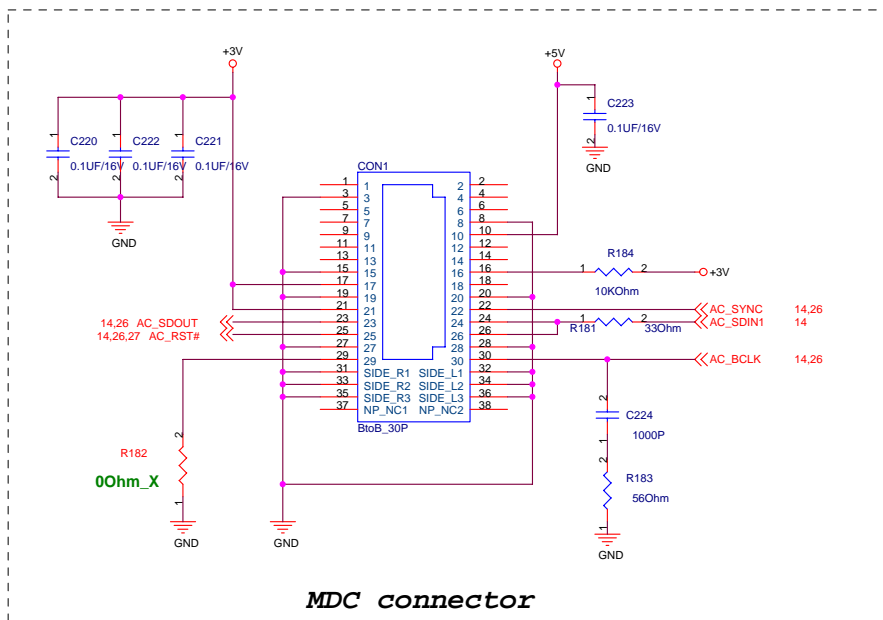
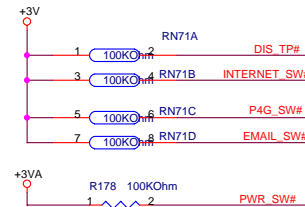
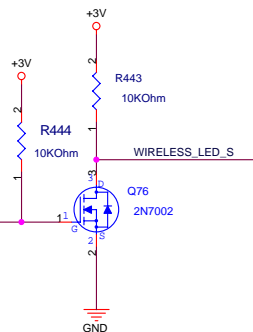
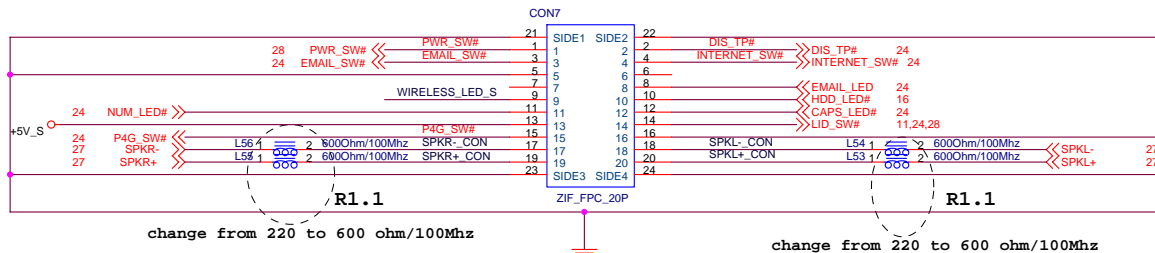


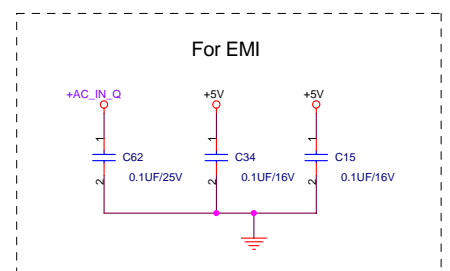
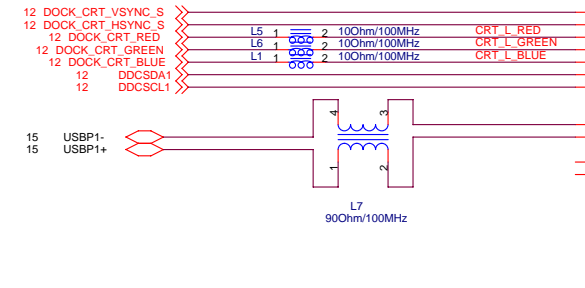
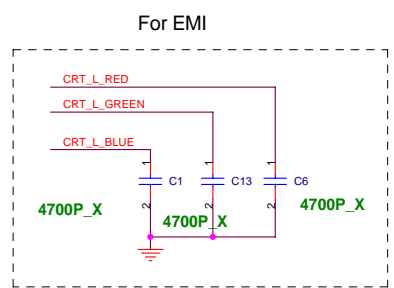
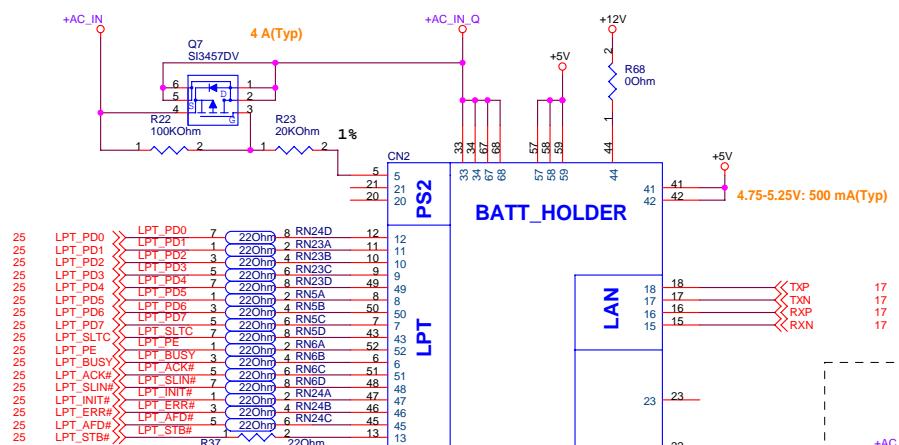
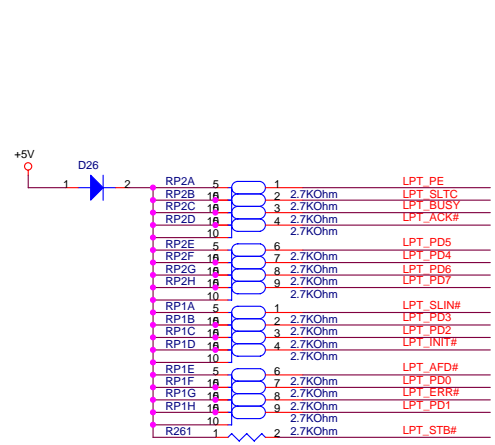
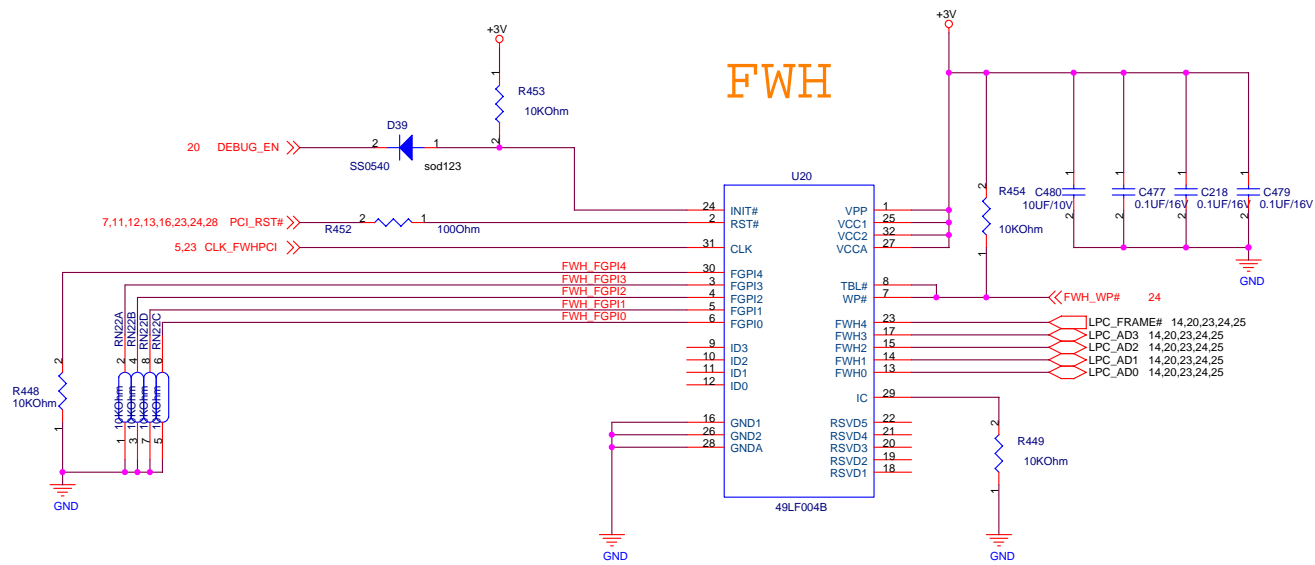
14,22,23,24,25 CLK_PCL_DB
 14,22,23,24,25 LPC_FRAME#
 14,22,23,24,25 LPC_AD0
 14,22,23,24,25 LPC_AD2
 14,22,23,24,25 LPC_AD3
 22 DEBUG_EN

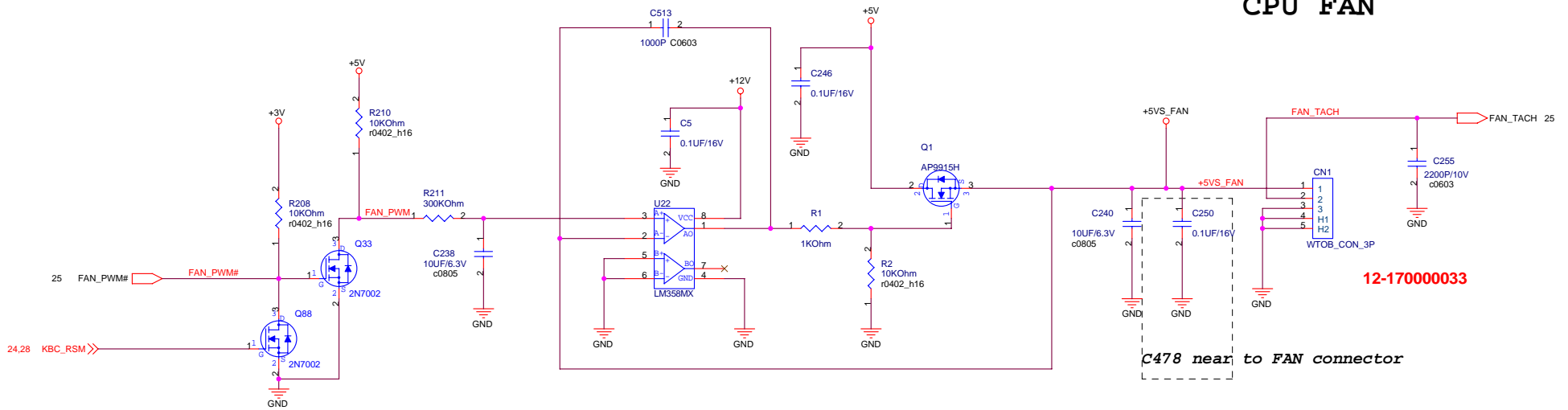




SPKL+,SPKL-,SPKR+,SPKR- trace 15mil width



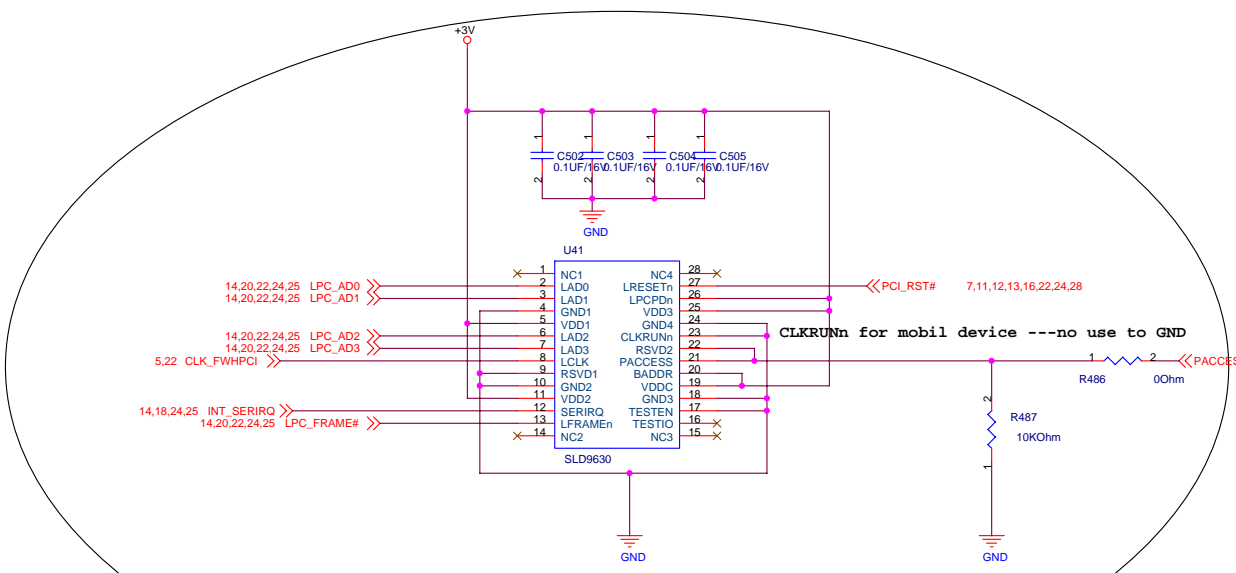




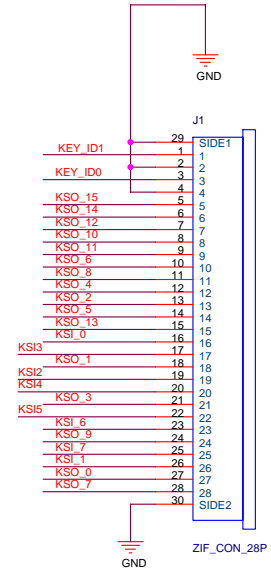
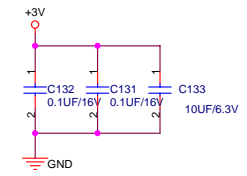
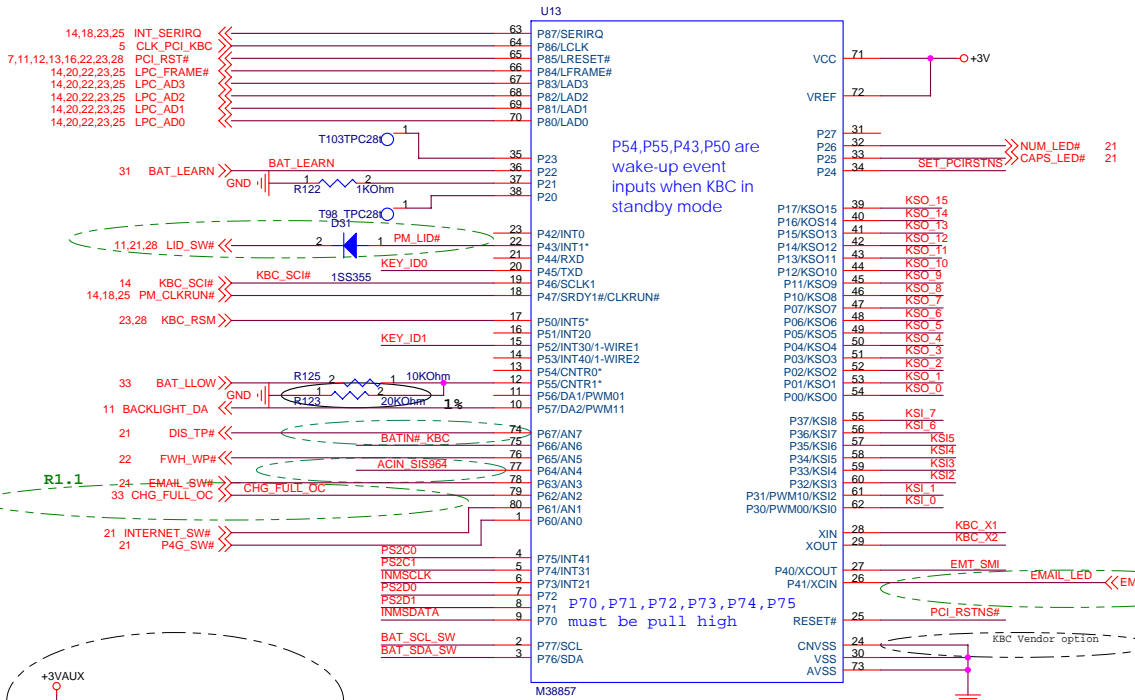
CPU FAN

12-17000033

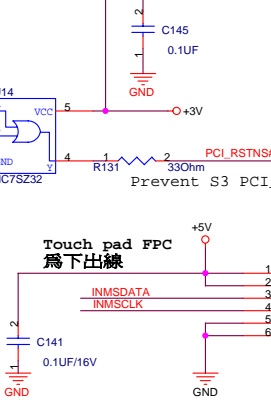
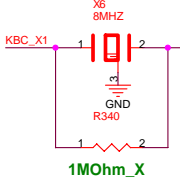
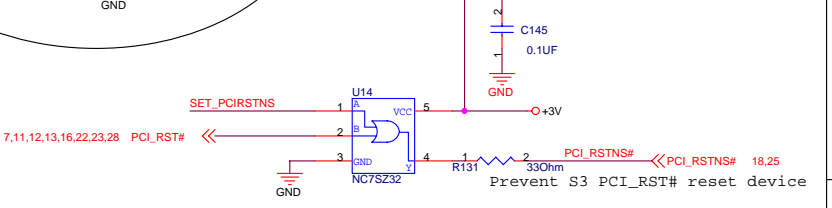
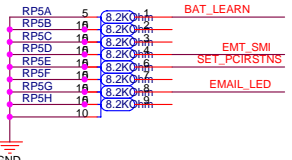
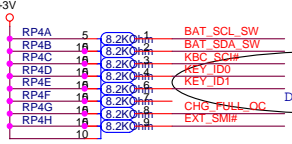
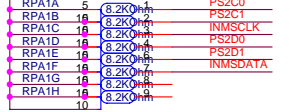
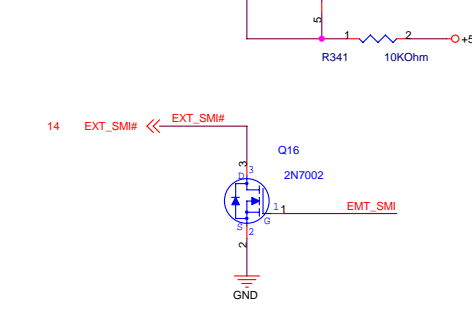
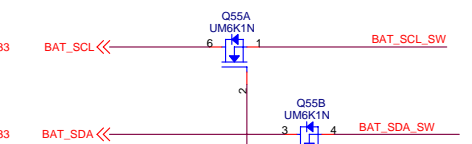
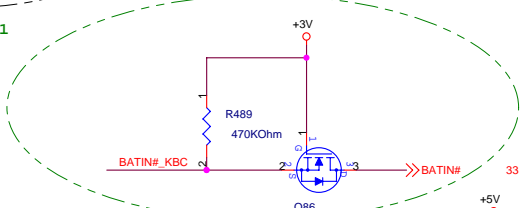
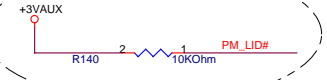
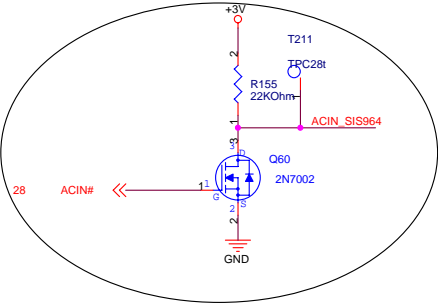
C478 near to FAN connector



	2Eh/2Fh	4Eh/4Fh
BADDR	GND	VDD



KEYBOARD CONNECTOR



Touch pad connector

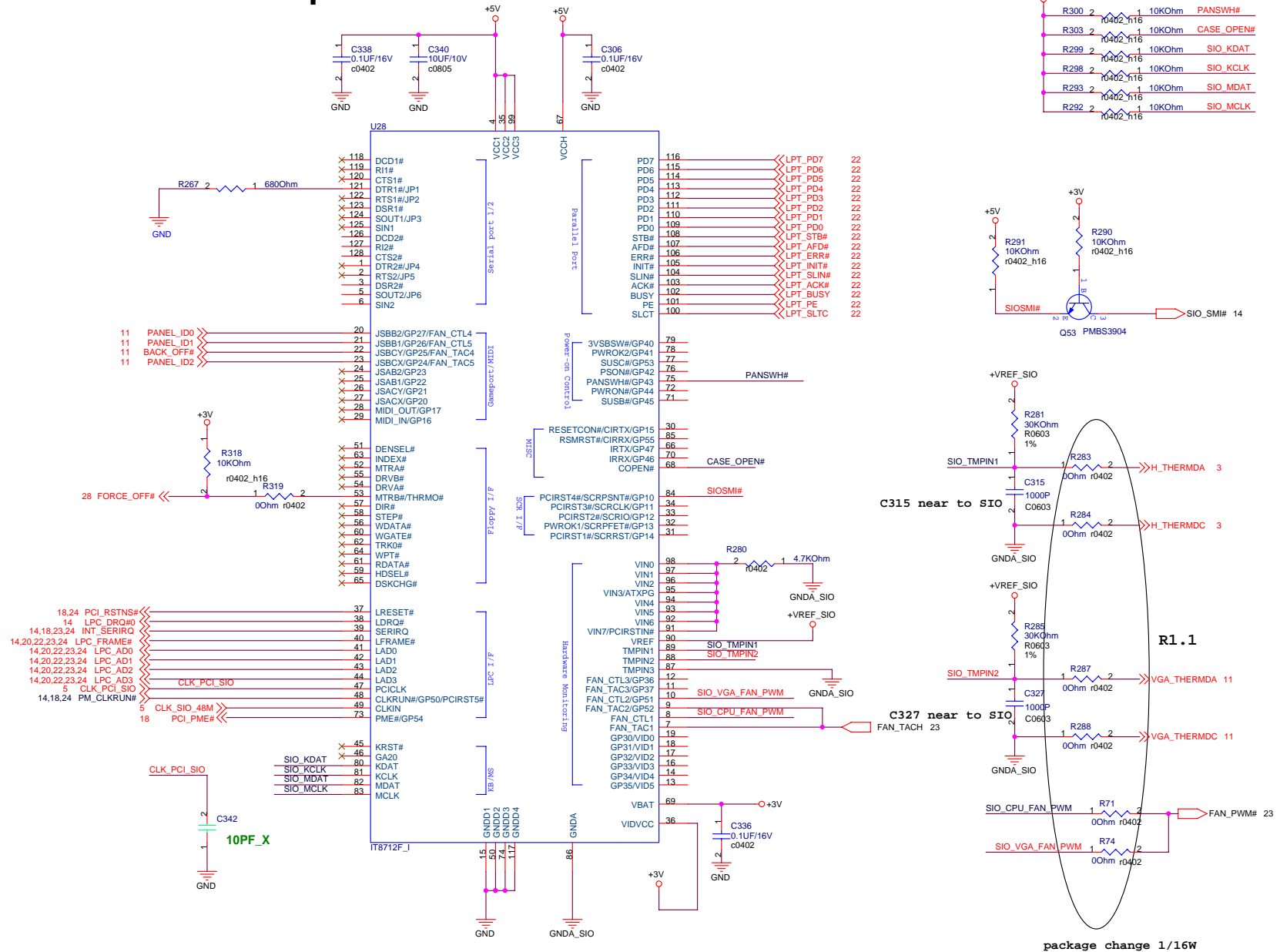
ASUS Title : KBC_M38857

ASUSTek COMPUTER INC. Engineer: -

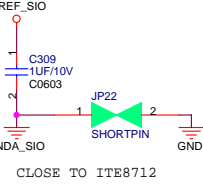
Size	Project Name	Rev
Custom	T19	1.0

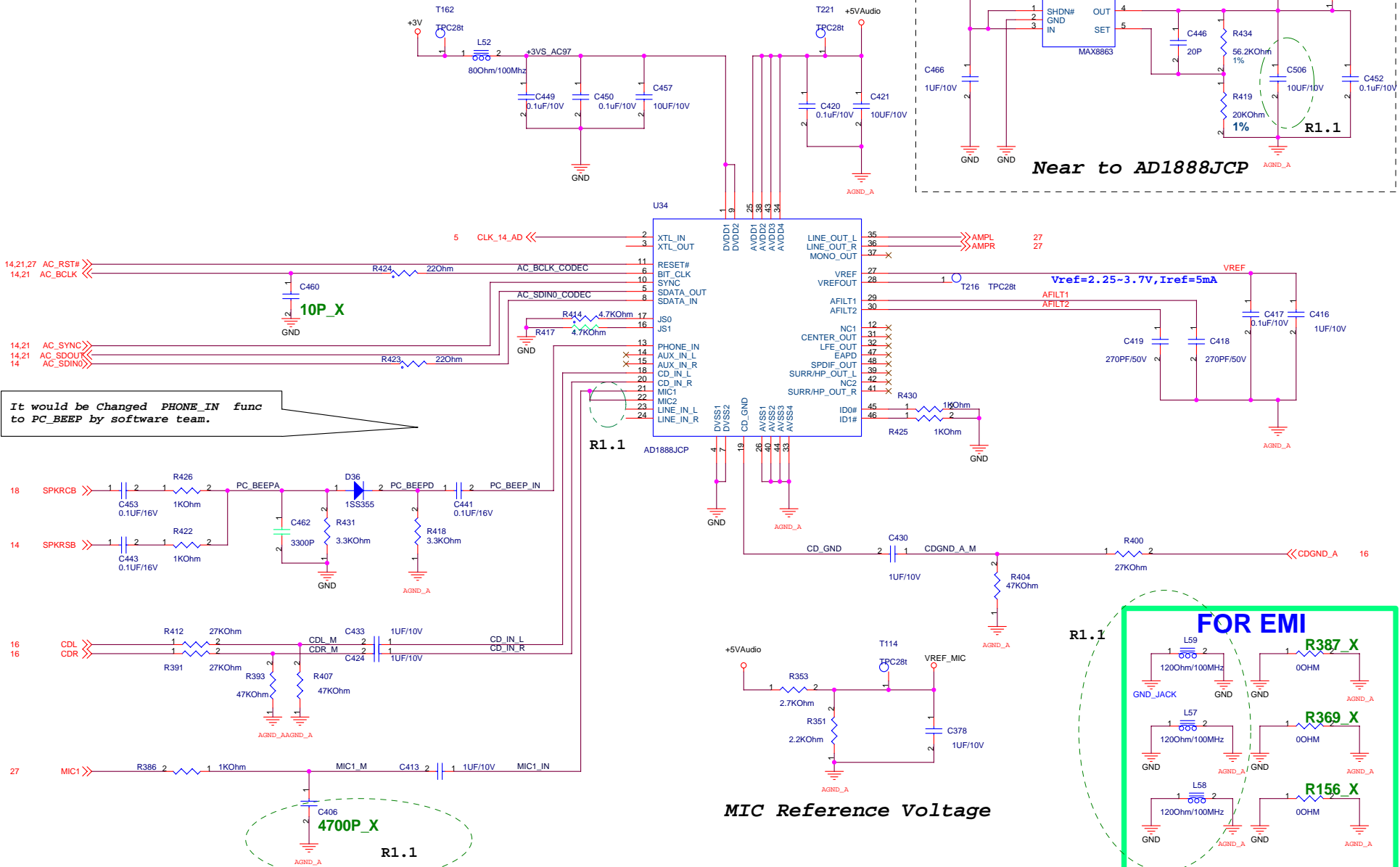
Date: Tuesday, May 31, 2005 Sheet 24 of 38

Super I/O

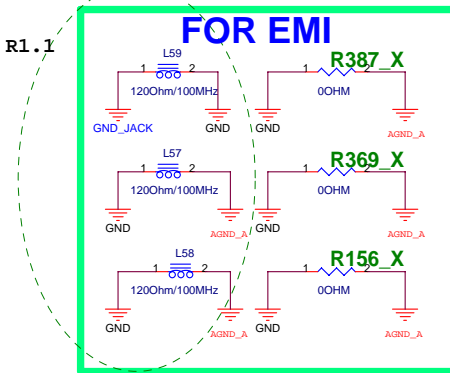


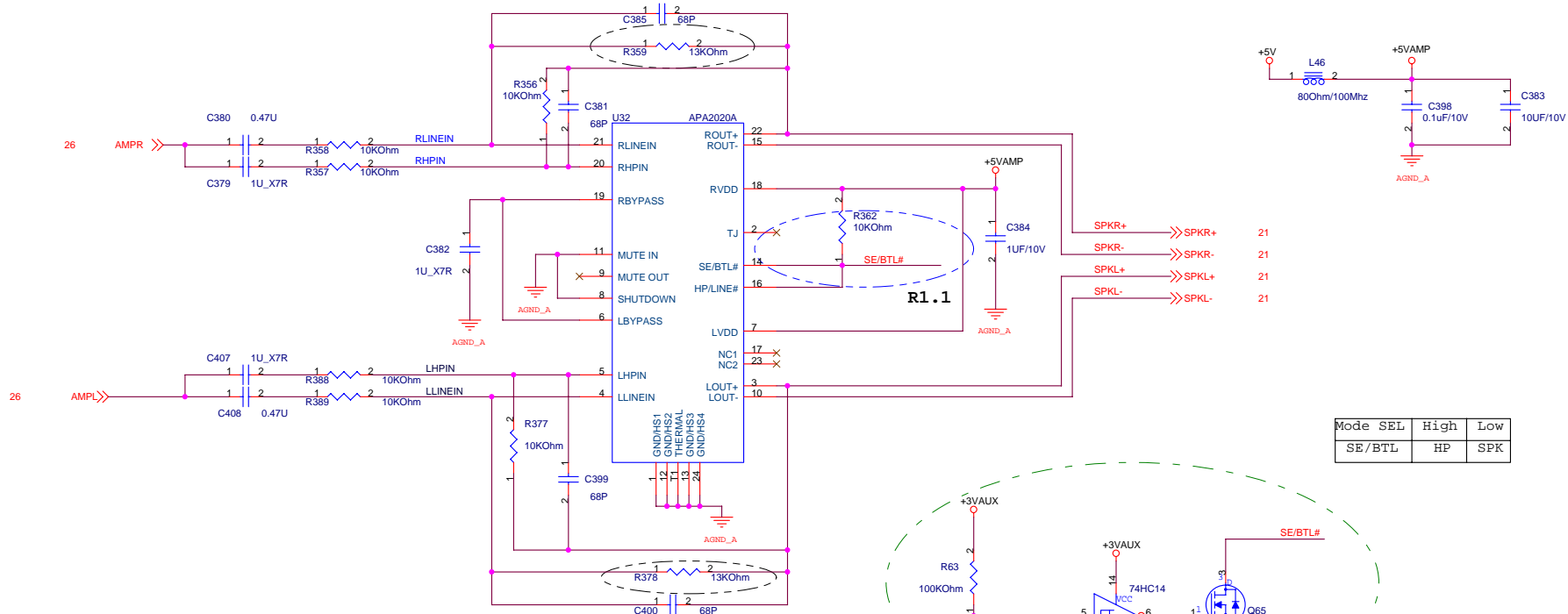
package change 1/16W





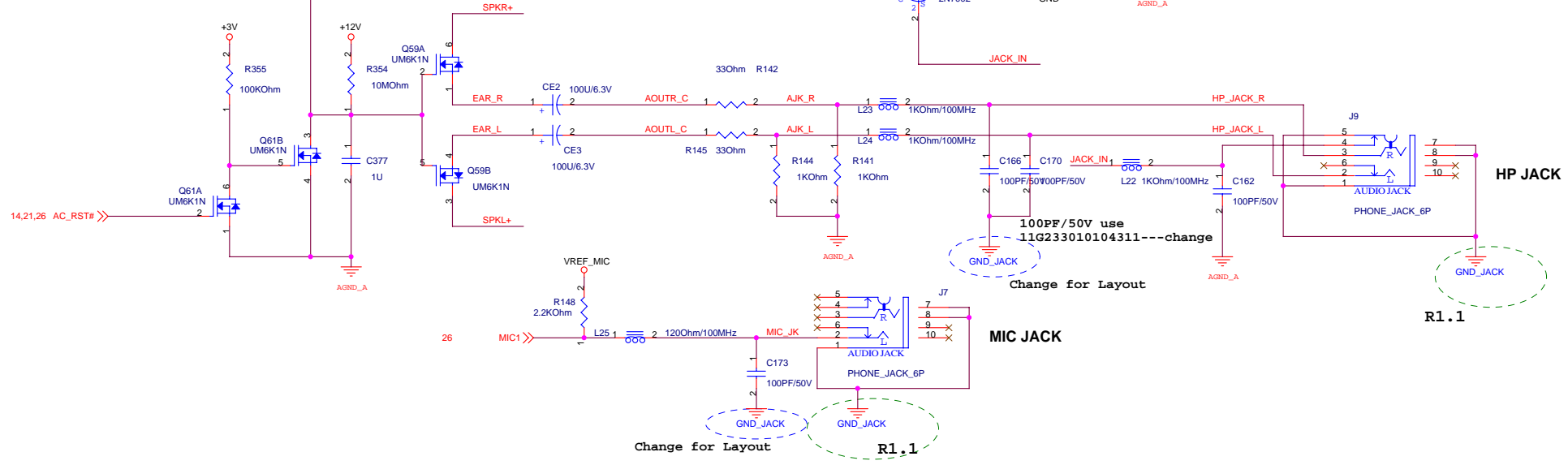
It would be changed PHONE_IN func to PC_BEEP by software team.

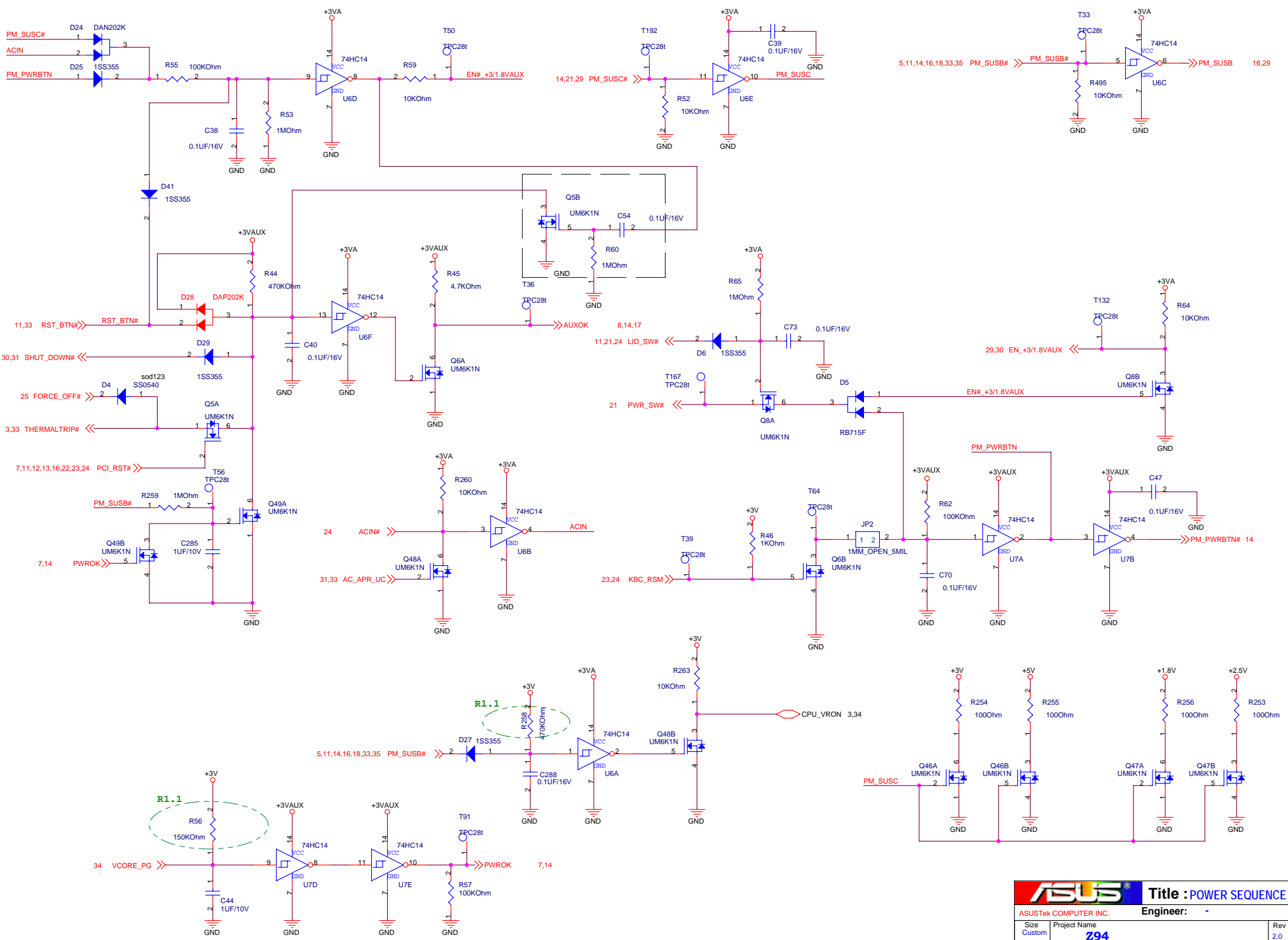


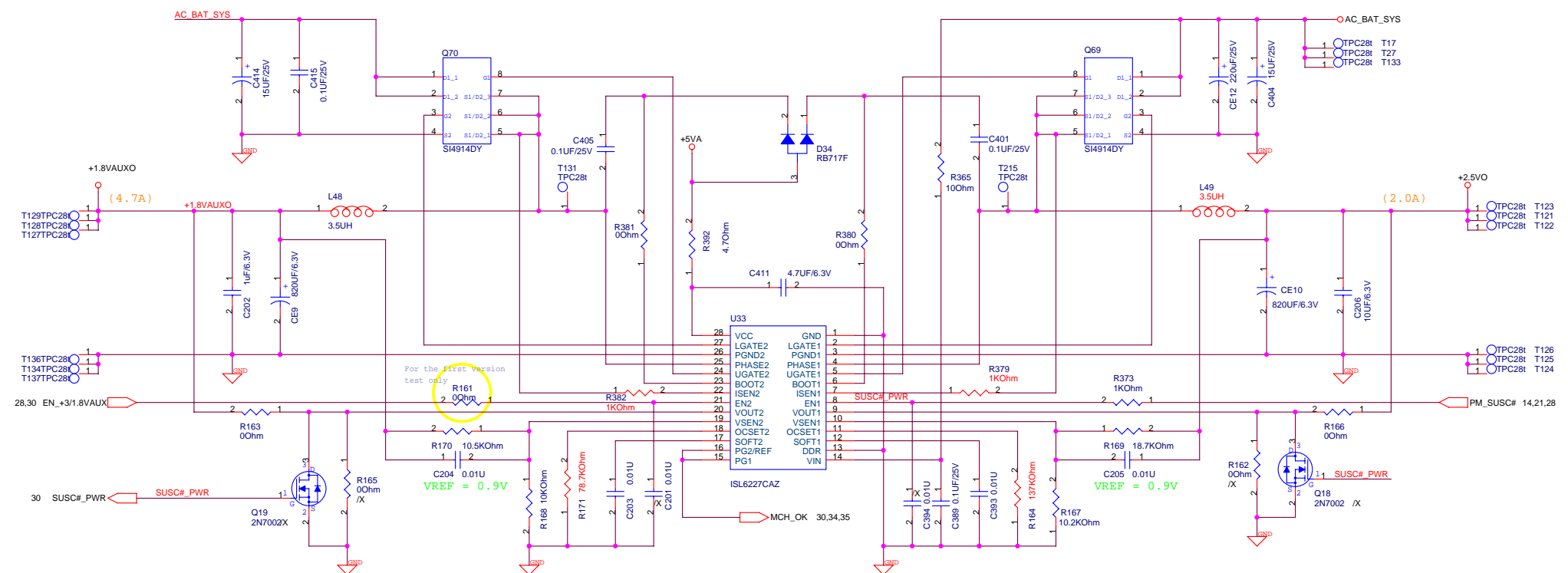


Mode	SEL	High	Low
SE/BTL		HP	SPK

TO PREVENT POP SOUND WHEN SYSTEM WAKE UP FROM S3



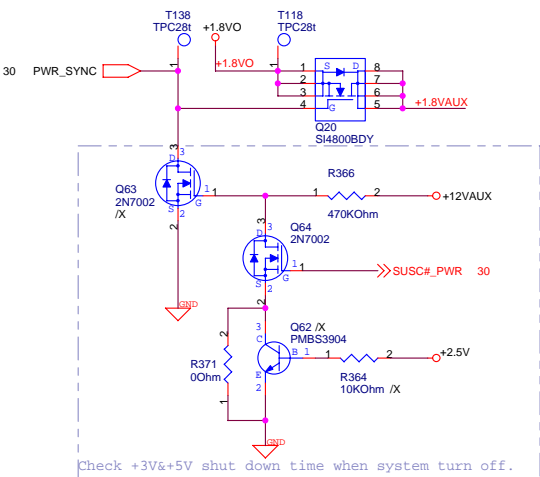
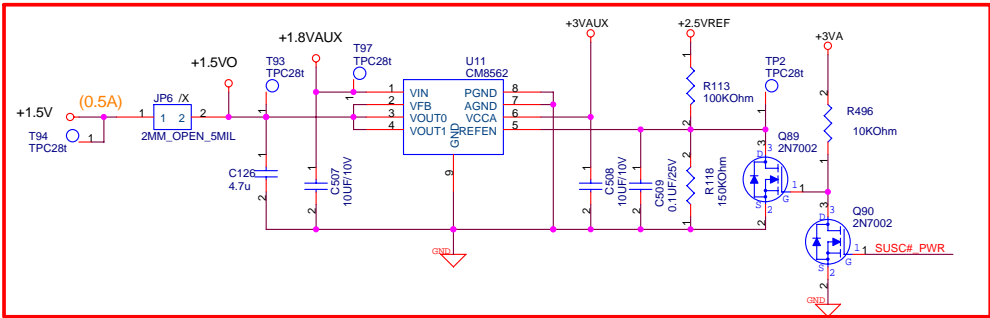




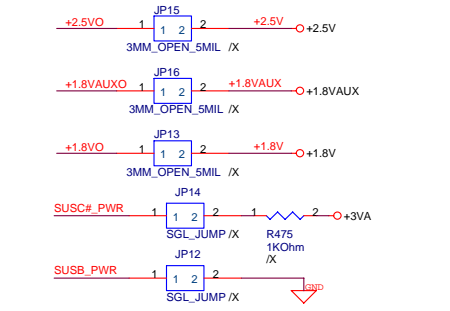
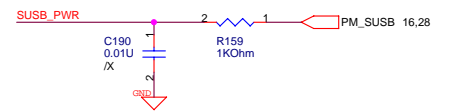
For the first version test only

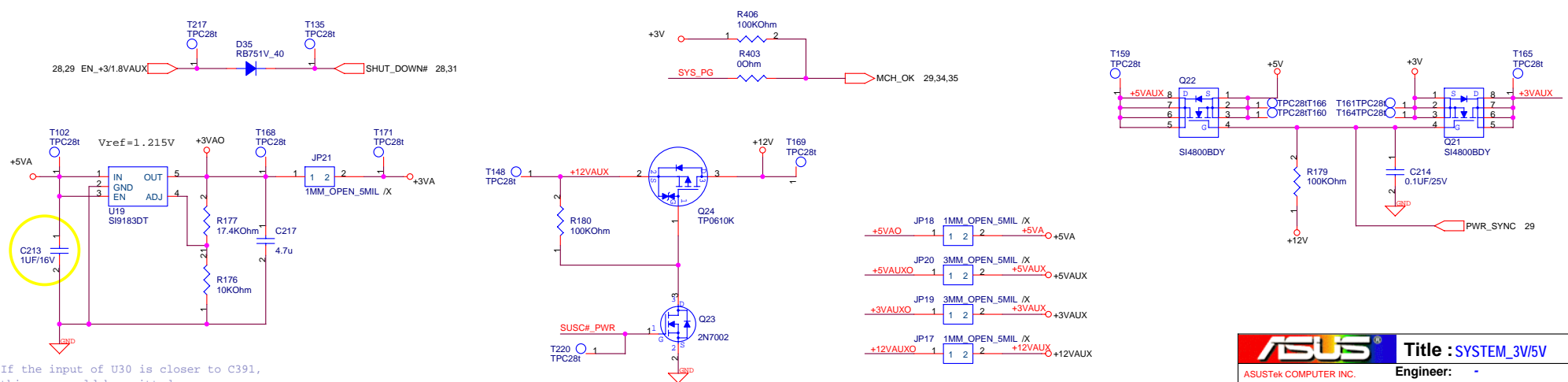
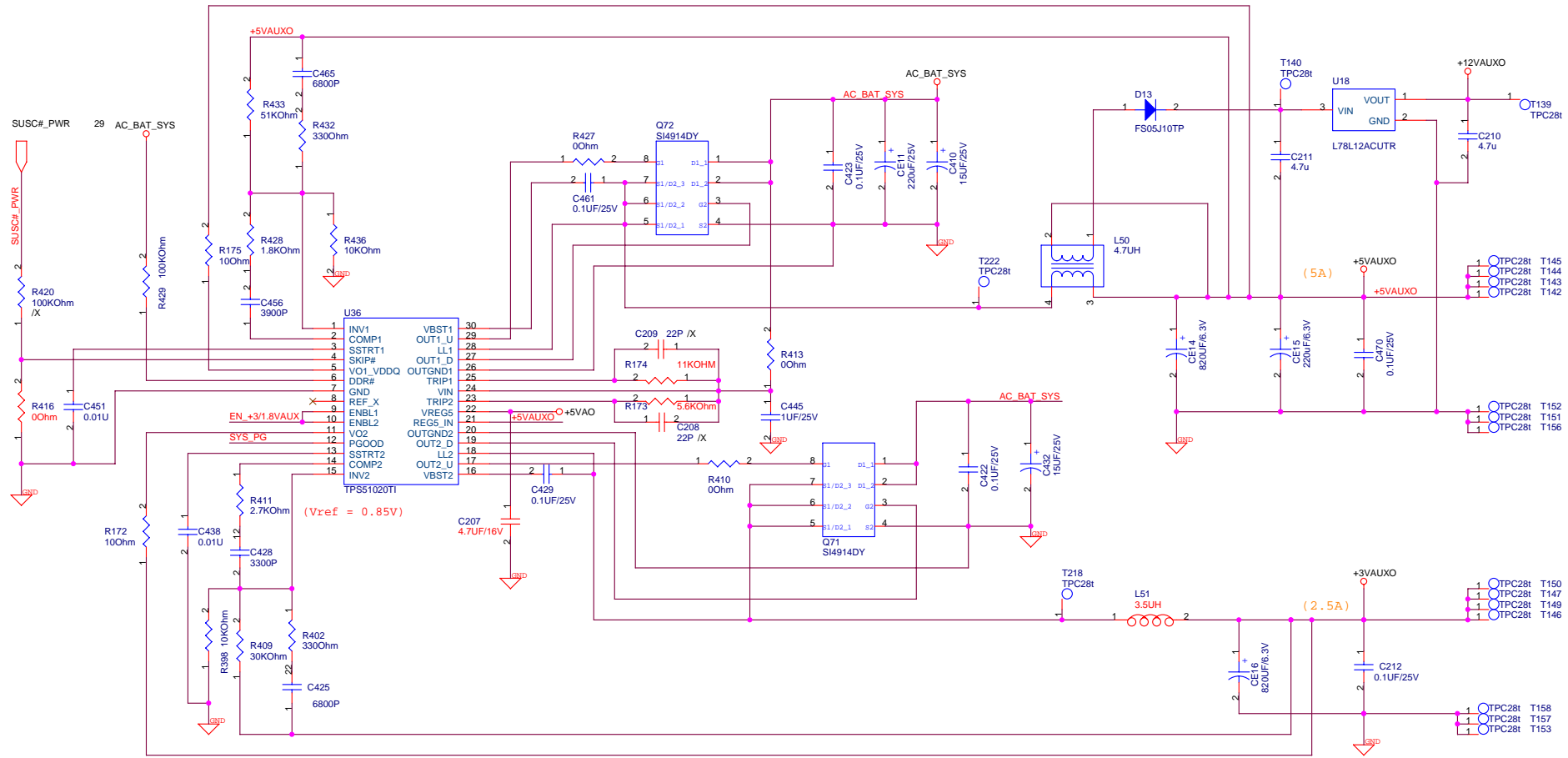
VRREF = 0.9V

VRREF = 0.9V

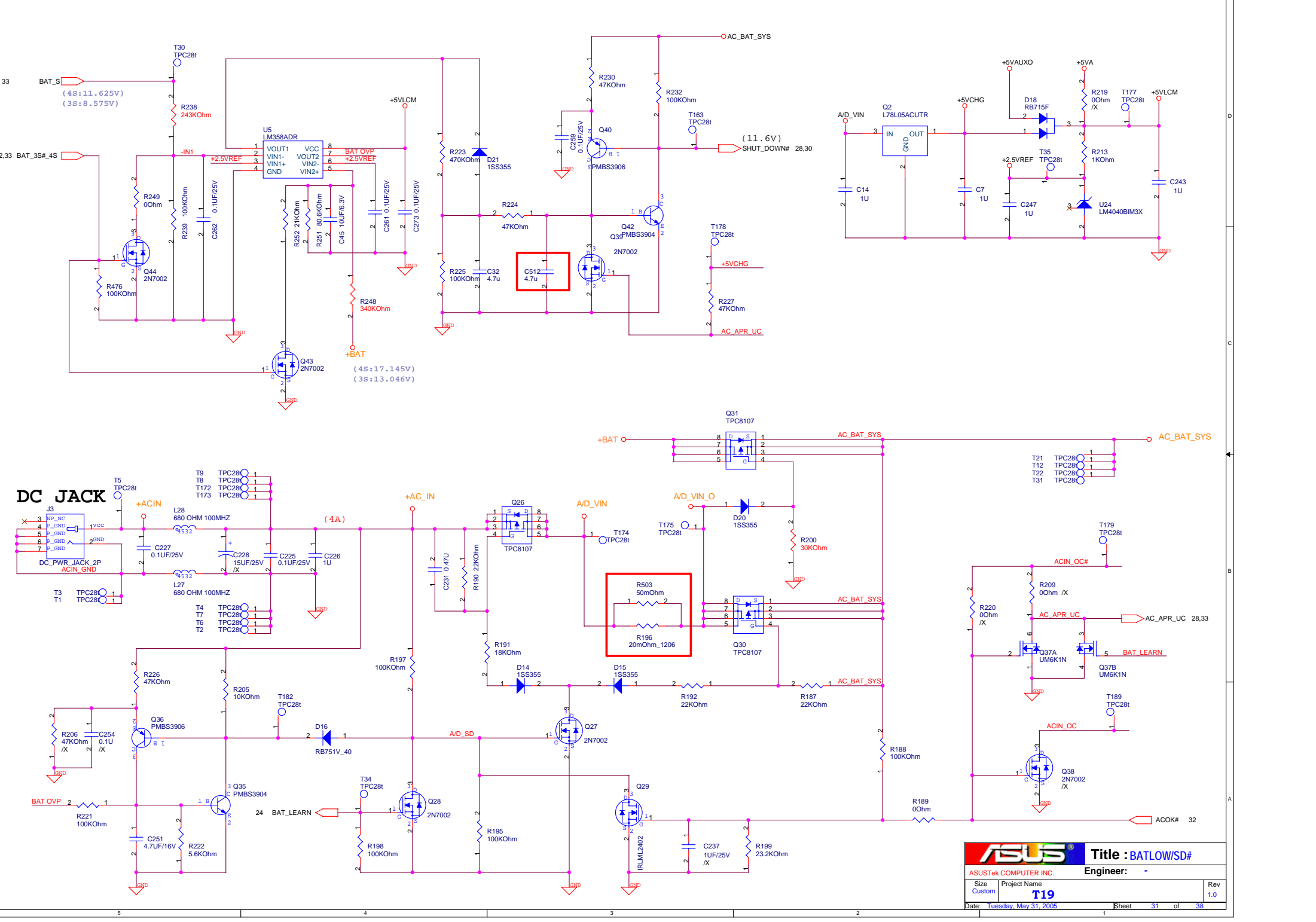


Check +3V/+5V shut down time when system turn off.



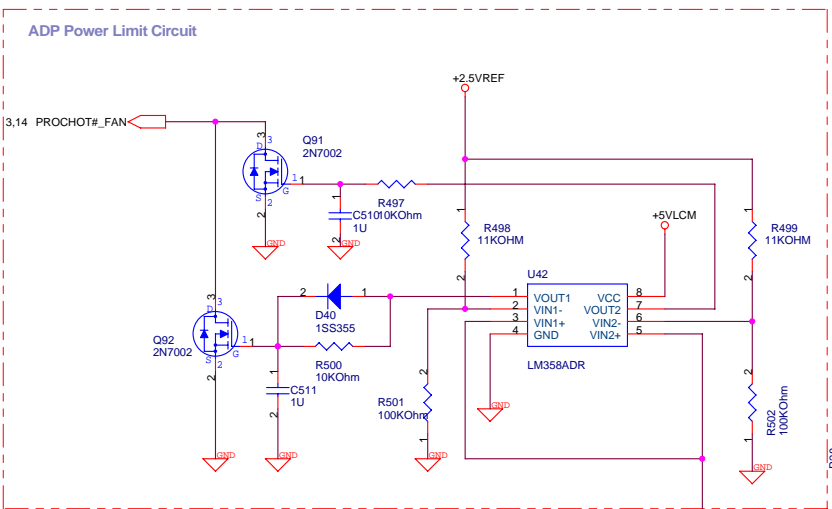


If the input of U30 is closer to C391, this cap could be omitted.

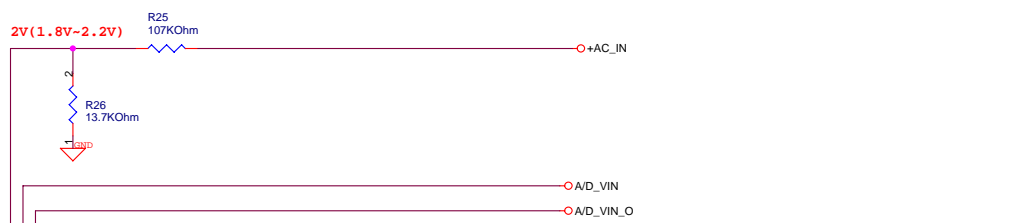


DC JACK

ASUS		Title : BATLOW/SD#	
ASUSTek COMPUTER INC.		Engineer: -	
Size Custom	Project Name T19	Date: Tuesday, May 31, 2005	Rev 1.0
		Sheet 31	of 38

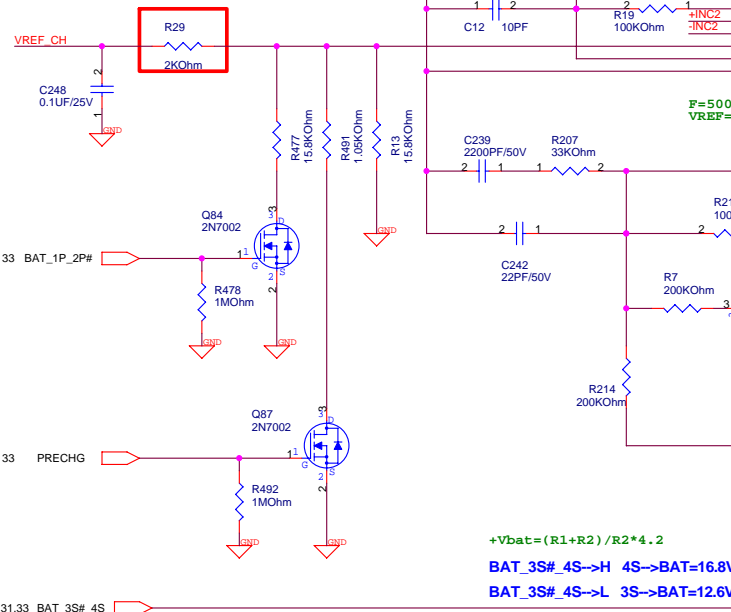


ACOK#:
 $+ACIN \geq 2V * (R25 + R26) / R26$
 $= 2 * (107 + 13.7) / 13.7 = 17.62$

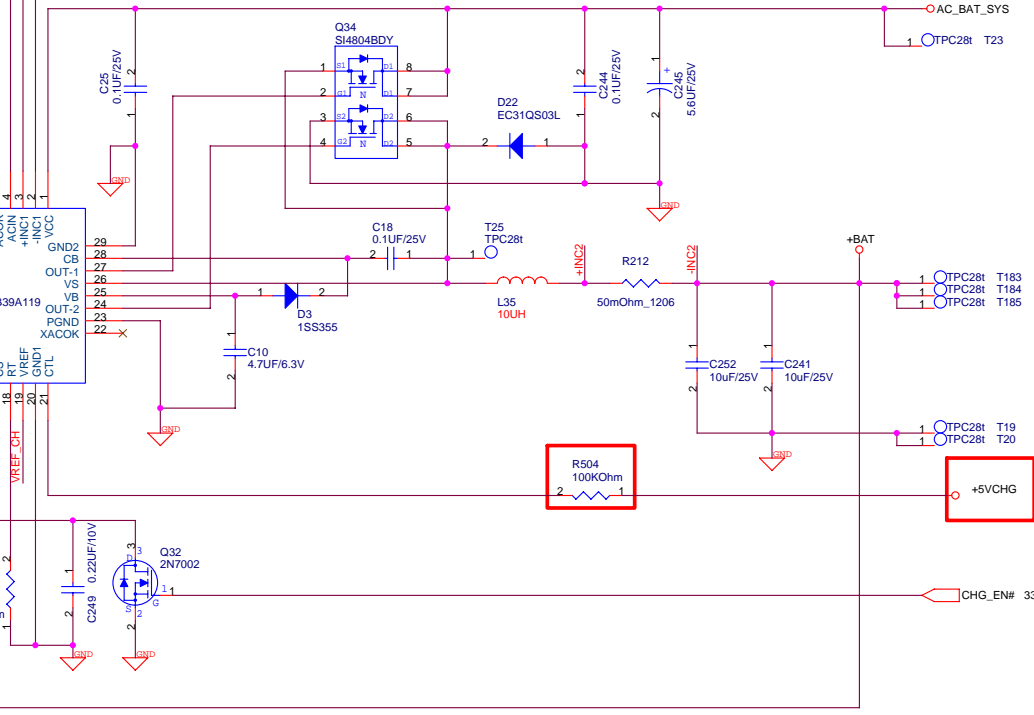


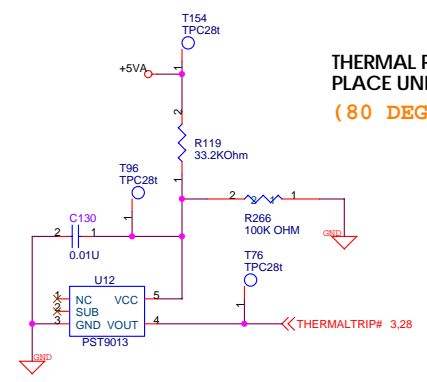
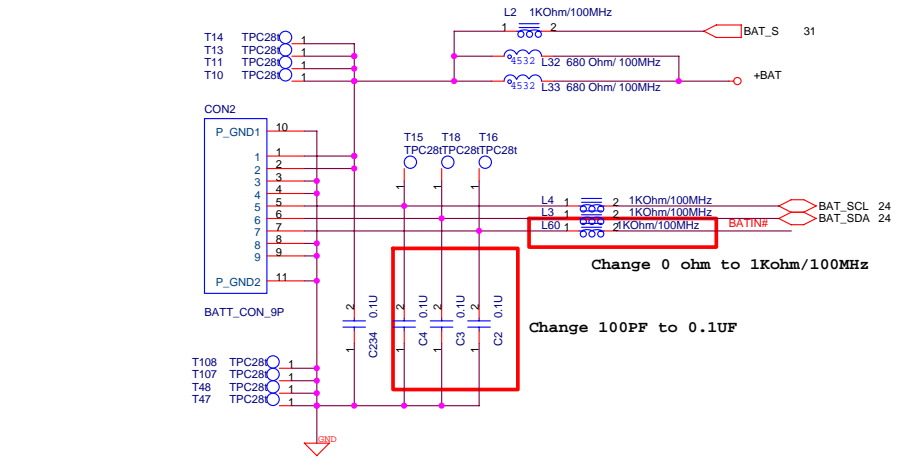
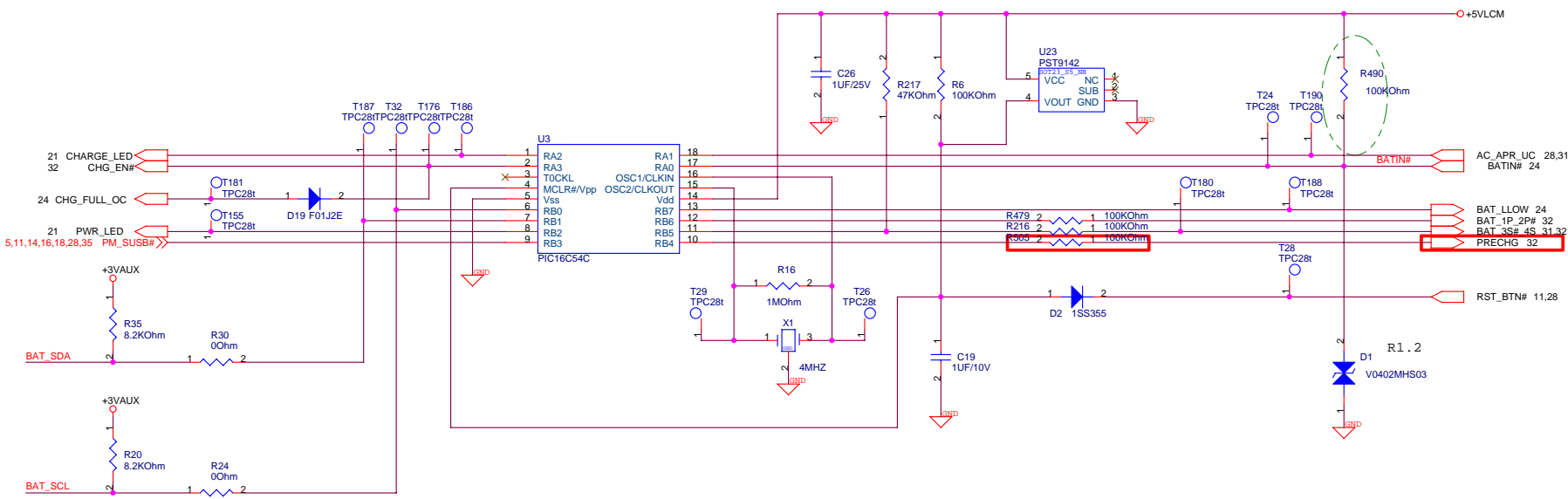
Charge Current Setting
 $V(+INE2) = 25 * I_{chg}(A) * R_{s2}$
 2P# => ICHG=2.5A
 1P => ICHG=1.25A
 Prechg. => ICHG=0.4A

Current sharing = 3.2A
 $V(+INE1) = 25 * I_{chg}(A) * R_{s1}$
 $I = (5 * R27 / (R28 + R27)) / (25 * 50m)$
 $= 3.203A$

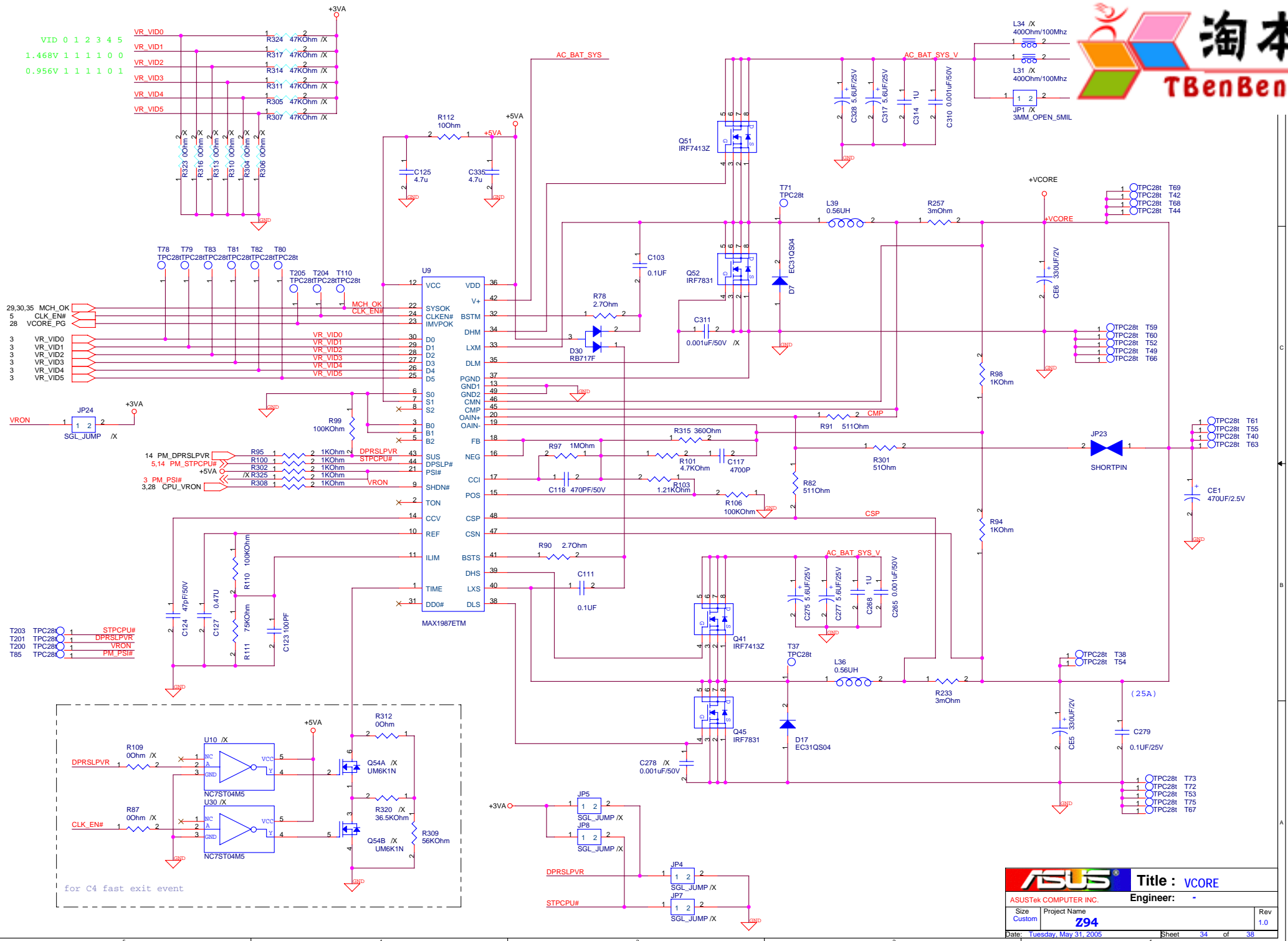


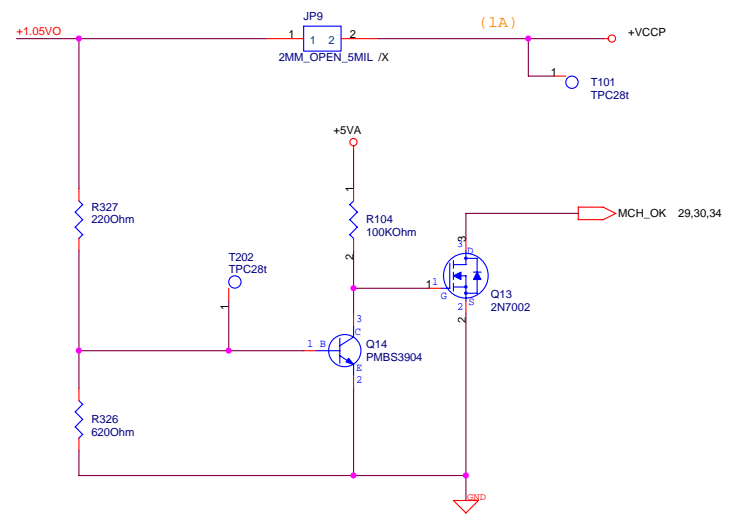
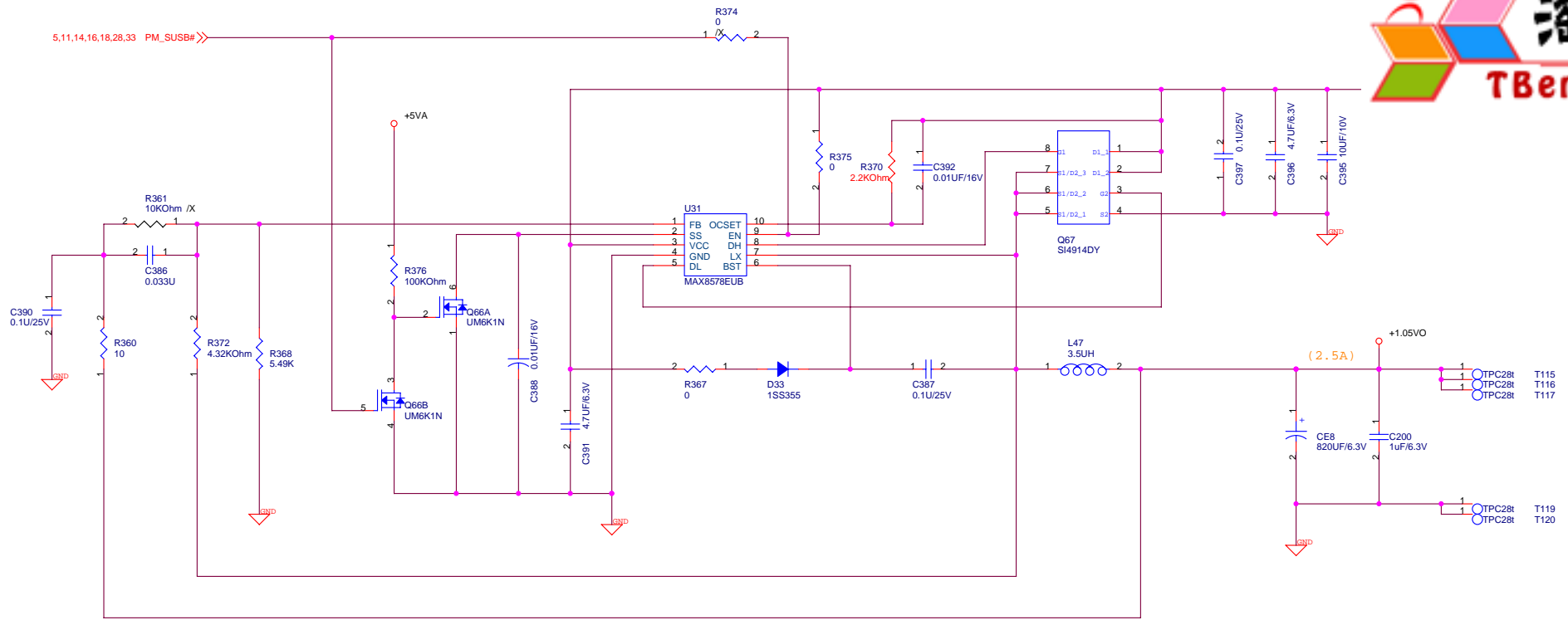
$+V_{bat} = (R1 + R2) / R2 * 4.2$
 BAT_3S#_4S->H 4S->BAT=16.8V
 BAT_3S#_4S->L 3S->BAT=12.6V





**THERMAL PROTECTION
PLACE UNDER CPU
(80 DEGREE C)**





PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (HOST TO PCI)	(AD11 Internal)			
AGP	(AD16 Internal)		D	
LAN	AD15		D	
HDD	AD13		A	IRQ15
LPC	AD13		C	
MODEM	AD13		C	
AUDIO	AD13		C	
USB	AD14		E,F,G,H	
CardBus	AD19		B,C,D	
ODD	AD13			IRQ14
1394	AD19		B,C,D	

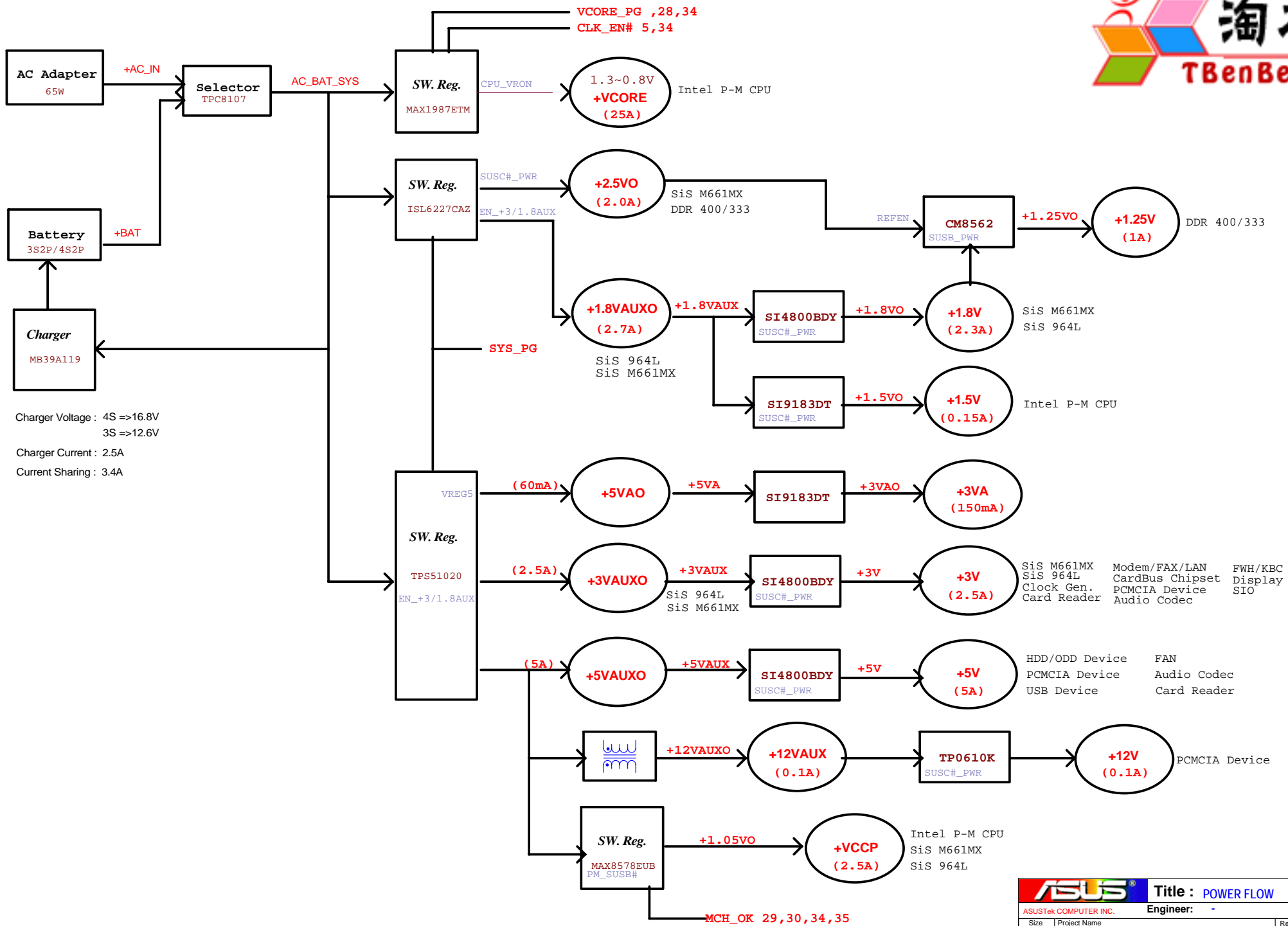


KBC GPIO USE AS				
Pin Name	Function	Signal Name	Default	S3/!
P20	NC			
P21	GPI		Low	
P22	GPO	BAT_LEARN	Low	Low
P23	NC			
P24	GPO	SET_PCIRSTNS	Low	High
P25	LEDCAP	CAPS_LED#	High	High
P26	LEDNUM	NUM_LED#	High	High
P27	SCROLL	SCROLL_LED#	High	High
P40	GPO	EMT_SMI	Low	Low
P41	GPO	EMAIL_LED	Low	Low
P42	NC			
P43	GPI	PM_LID#	High	High
P44	NC			
P45	GPI	KEY_ID0		
P46	SCI	KBC_SCI#		
P47	CLKRUN#	PM_CLKRUN#		
P50	GPO	KBC_RSM	Low	Low
P51	NC			
P52	GPI	KEY_ID1		
P53	NC			
P54	NC			
P55	GPI	BAT_LLOW		
P56	NC			
P57	GPO	BACKLIGHT_DA	anlog	anlog
P60	GPI	P4G_SW#		
P61	GPI	INTERNET_SW#		
P62	GPI	CHG_FULL_OC	Low	
P63	GPI	EMAIL_SW#		
P64	GPI	ACIN_SIS964	Low	
P65	GPO	FWH_WP#	High	High
P66	GPI	BATIN#_KBC	High	
P67	GPI	DIS_TP#		

SIS964 GPIO USE AS		
Pin Name	Function	Signal Name
GPIO0	GPI	PACCESS_EN#
GPIO1	GPI	AGP_8XDET#
GPIO2	THERM#	PROCHOT#_FAN
GPIO3	EXTSMI#	EXT_SMI#
GPIO4	CLKRUN#	PM_CLKRUN#
GPIO5	NC	
GPIO6	GPI	THERM#
GPIO7	GPI	ODD_CLR
GPIO8	RING	RIA#
GPIO9	GPI	KBC_SCI#
GPIO10	GPI	SIO_SMI#
GPIO11	STP_PCI#	PM_STPPCI#
GPIO12	CPUSTP#	PM_STPCPU#
GPIO13	DPRSLPVR	PM_DPRSLPVR
GPIO14	AGPSTOP#	AGPSTOP#
GPIO15	VR_HILO#	VR_HI/LO#
GPIO16	NC	
GPIO17	VGATEM#	VGATEM#
GPIO18	NC	
GPIO19	SMC	SMC
GPIO20	SMD	SMD
GPIO21	NC	
GPIO22	NC	
GPIO23	NC	
GPIO24	NC	

SUPER I/O ITE8712F GPIO USE AS				
Pin Name	Function	Signal Name	Default	S3/S4
GPIO10	GPO	SIOSMI#	High	
GPIO11	NC			
GPIO12	NC			
GPIO13	NC			
GPIO14	NC			
GPIO15	NC			
GPIO16	NC			
GPIO17	NC			
GPIO20	NC			
GPIO21	NC			
GPIO22	NC			
GPIO23	NC			
GPIO24	GPI	PANEL_ID1	High	
GPIO25	GPO	BACK_OFF#	High	
GPIO26	GPI	PANEL_ID1	High	
GPIO27	GPI	PANEL_ID0	High	
GPIO30	GPO	ODD_CLR	LOW	
GPIO31	GPI	ODD_SET	LOW	
GPIO32	NC			
GPIO33	NC			
GPIO34	NC			
GPIO35	NC			
GPIO36	NC			
GPIO37	NC			
GPIO40	NC			
GPIO41	NC			
GPIO42	NC			
GPIO43	PANSWH#	PANSWH#	High	
GPIO44	NC			
GPIO45	NC			
GPIO46	NC			
GPIO47	NC			
GPIO50	CLKRUN#	PM_CLKRUN#		
GPIO51	FAN_CLT2	SIO_VGA_FAN_PWM		
GPIO52	FAN_TAC2	FAN_TACH		
GPIO53	NC			
GPIO54	PME#	PCI_PME#		
GPIO55	NC			

SM BUS Address		
BUS name	Address	Device
Thermal controller	2E	ADT7460ARQ
Clock GEN	D2	ICS950816
DDR Clock	D4	ICS93732



Charger Voltage : 4S =>16.8V
 3S =>12.6V
 Charger Current : 2.5A
 Current Sharing : 3.4A

- 1.change page3 R10 from 20K 5% to 20K 1%.
- 2.page5 change R335,R328,R334 from 0 ohm to 33 ohm and delete C347,C349,C351,C354 5P capacitor.
- 3.Change page5 BSEL circuit
- 4.Page6 AGP_VREF add AGP bus reference voltage R465,R466 with 2.32 ohm 1%
- 5.Page6 AGP_8XDET# cancel connect(pull high only)
- 6.Page11 add AGP_8XDET# R493 pull high 3V.
Add net RST_BTN.
- 7.Page14 change RXD0 damp resistor near to U4 source.
- 8.Page 14 change ACIN_SIS964 to KBC GPIO64.
- 9.Page 14 change BATIN# to KBC GIP066
- 10.Page 14 change SIO_SMI# from SIS964 GPIO16 to GPIO10.
- 11.Page 14 add SIS964 GPIO7 pull high
- 12.Page 14 change CHG_FULL_OC from SIS964 GPIO18 to KBC GPIO62.
- 13.Page 14 change PM_LID# from SIS964 GPIO7 to KBC GPIO43.
- 14.Page 15 SIS964 UVDD33_1~3 power change to USBCOMPVDD.
- 15.Page 16 add ESD protection D42,D43
- 16.Page 17 RJ45 LAN pin difine inverse
- 17.Page 20 change R262 from 10K to 100K ohm to reduce delay time.
- 18.Page 21 add MOS to switch +5V ensure +5V will not sink current when USB device plug in.
- 19.Page 22 change R456 from 1.3K to 330 ohm..
- 20.Page 23 add TPM solution..
- 21.Page 24 add MUTI function EMAIL_LED and SCROLL_LED.
- 22.Page 24 add KBC pin24 to GND for KBC select.
- 23.Page 26 change from TAN_capacitor to ceramic.
- 24.Page 27 change SE/BTL select.
- 25.Page 26 add CODEC pin 22(MIC2) conect pin 21
- 26.Page 28 change R258 from 100K to 470K for power sequence.
- 27.Page 28 change R258 from 10K to 150K for power sequence.
- 28.Page 27 Jack GND net change to GND_JACK for EMI
- 29.Page 26 add L57,L58,L59 for EMI
- 30.Page 26 add L57,L58,L59 for EMI
- 31.Page 21 change CPU hole H4,H5,H6,H7 NPTH to PTH and add J10 spring for EMI
- 32.Page 21 add FUSE F2 and L53,L54,L55,L56 change to 600ohm/100MHz
- 33.Page 21 change CPU hole H4,H5,H6,H7 NPTH to PTH and add J10 spring for EMI
- 34.Page 3 Q4 N-MOSFET change to drain connect R31 pin1 source connector GND
- 35.Page 5 Change C316,C413 from 12PF to 33PF
- 36.Page 14 Change C175,C179 from 18PF to 15PF