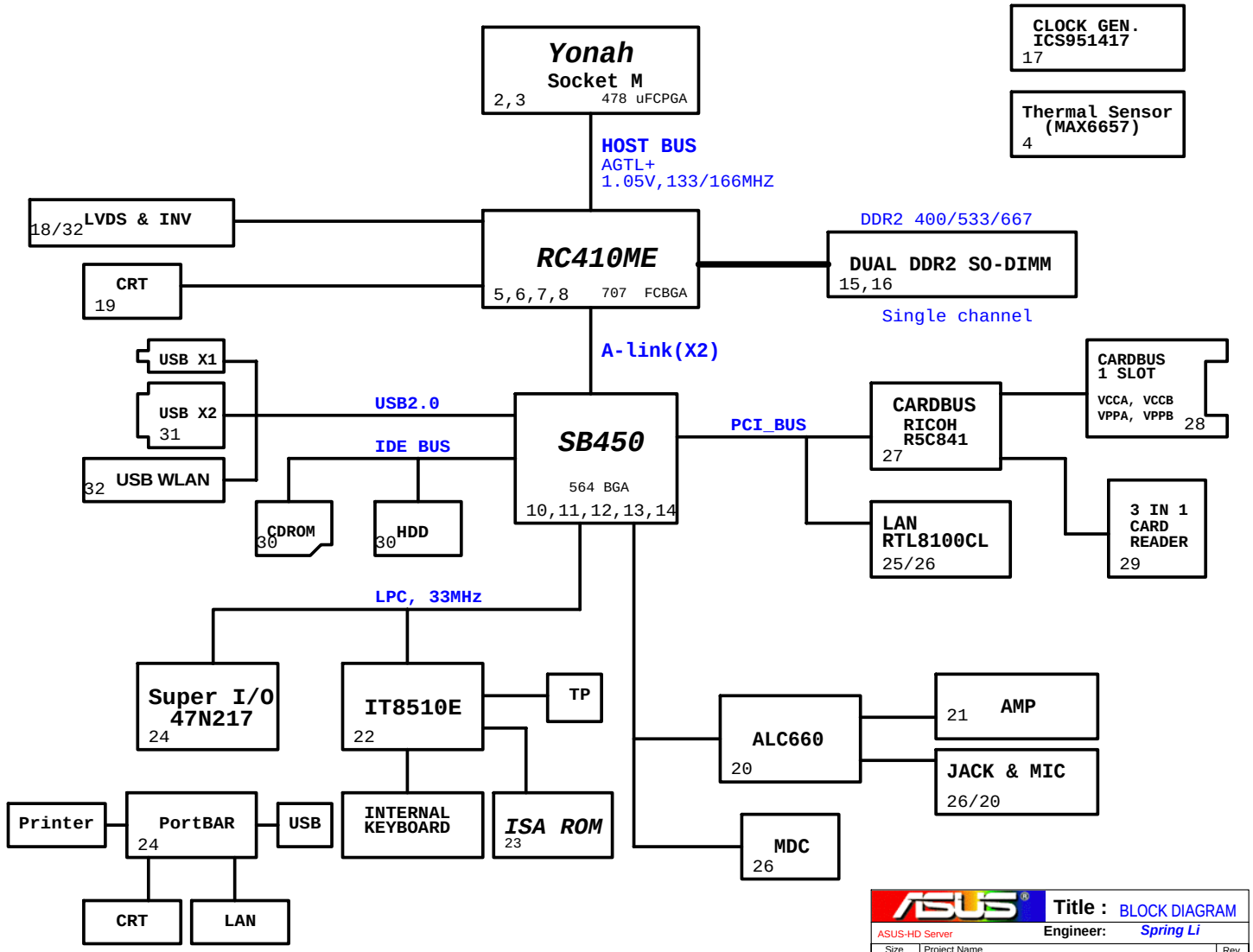
Z94Rp

Rev.1.1

Yonah/RC410ME/IXP450 BLOCK DIAGRAM



ASUS-HD Server	Title : BLOCK DIAGRAM		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 1 of 45		

U201A

(5) H_A#[16:3]

H_A#3 J4
H_A#4 L4
H_A#5 M3
H_A#6 K5
H_A#7 M1
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 P2
H_A#13 L1
H_A#14 P4
H_A#15 P1
H_A#16 R1

ADDR GROUP 0

A[3]# A[4]# A[5]# A[6]# A[7]# A[8]# A[9]# A[10]# A[11]# A[12]# A[13]# A[14]# A[15]# A[16]# ADSTB[0]#

(5) H_ADSTB#0
(5) H_REQ#[4:0]

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L5

REQ[0]# REQ[1]# REQ[2]# REQ[3]# REQ[4]#

(5) H_A#[31:17]

H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U2
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W3
H_A#28 W5
H_A#29 Y4
H_A#30 W2
H_A#31 Y1

ADDR GROUP 1

A[17]# A[18]# A[19]# A[20]# A[21]# A[22]# A[23]# A[24]# A[25]# A[26]# A[27]# A[28]# A[29]# A[30]# A[31]# ADSTB[1]#

(5) H_ADSTB#1

V4

(10) H_A20M#
(10) H_FERR#
(10) H_IGNNE#

A6 A20M#
A5 FERR#
C4 IGNNE#

(10) H_STPCLK#
(10) H_INTR
(10) H_NMI
(10) H_SMI#

D5 STPCLK#
C6 LINT0
B4 LINT1
A3 SMI#

AA1 RSVD[1]
AA4 RSVD[2]
AB2 RSVD[3]
AA3 RSVD[4]
M4 RSVD[5]
N5 RSVD[6]
T2 RSVD[7]
V3 RSVD[8]
B2 RSVD[9]
C3 RSVD[10]
B25 RSVD[11]

RESERVED

T22 RSVD[12]
A2 RSVD[A2]
D2 RSVD[13]
F6 RSVD[14]
D3 RSVD[15]
C1 RSVD[16]
AF1 RSVD[17]
D22 RSVD[18]
C23 RSVD[19]
C24 RSVD[20]

SOCKET479P

CONTROL

ADS# H1
BNR# E2
BPRI# G5

DEFER# H5
DRDY# F21
DBSY# E1

BR0# F1

IERR# D20
INIT# B3

LOCK# H4

RESET# B1
RS[0]# F3
RS[1]# F4
RS[2]# G3
TRDY# G2

HIT# G6
HITM# E4

XDP/ITP SIGNALS

BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1
TCK AC5
TDI AA6
TDO AB3
TMS AB5
TRST# AB6
DBR# C20

THERM

PROCHOT# D21
THERMDA A24
THERMDC A25

THERMTRIP# C7

HCLK

BCLK[0] A22
BCLK[1] A21

TPC28T T1
TPC28T T2
TPC28T T3
TPC28T T4
TPC28T T5
TPC28T T6

H_ADS# (5)
H_BNR# (5)
H_BPRI# (5)
H_DEFER# (5)
H_DRDY# (5)
H_DBSY# (5)
H_BR0# (5)
H_INIT# (10)
H_LOCK# (5)
H_CPURST# (5)
H_RS#0 (5)
H_RS#1 (5)
H_RS#2 (5)
H_TRDY# (5)
H_HIT# (5)
H_HITM# (5)

H_BR0# L
R201 1 1 2 200Ohm
R202 1 1 2 0Ohm
H_IERR# 1 R203 2 56Ohm

+VCCP

H_PREQ#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#

CPU Debug Port

+VCCP
R204 56Ohm

Not support prochot

H_PROCHOT_S#
CPU_THRM_DA (4)
CPU_THRM_DC (4)
route these as DIFF signal

PM_THRMTRIP#

CLK_CPU_BCLK (17)
CLK_CPU_BCLK# (17)

Default Strapping When Not Used

+VCCP

H_PREQ# R213 2 /X 1 54.9Ohm 1%
H_TDI R214 2 /X 1 54.9Ohm 1%
H_TDO R215 2 /X 1 54.9Ohm 1%
H_TMS R216 2 /X 1 54.9Ohm 1%

H_TCK R217 2 1 54.9Ohm 1%
H_TRST# R219 1 2 54.9Ohm

+VCCP
R220 1 2 1KOhm
R222 1 2 56Ohm
+3VSUS
R221 10KOhm
PM_THRMTRIP#
Q201 PMBS3904
THRMTRIP# (12)

+VCCP
H_PWRGD R227 330Ohm
H_DPSLP# R228 200Ohm
H_CPURST# R260 200Ohm

+VCCP
R235 470Ohm
H_DPRSTP#
H_DPRSTP# (62)
(10,62) PM_DPRSLPVR
R240 470Ohm
Q204 PMBS3904
GND

U201B

(5) H_D#[15:0]

H_D#0 E22
H_D#1 F24
H_D#2 E26
H_D#3 H22
H_D#4 F23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H26
H_D#13 E26
H_D#14 K22
H_D#15 H25

DATA GRP 0

D[0]# D[1]# D[2]# D[3]# D[4]# D[5]# D[6]# D[7]# D[8]# D[9]# D[10]# D[11]# D[12]# D[13]# D[14]# D[15]#

(5) H_DSTBN#0
(5) H_DSTBP#0
(5) H_DINV#0

H23 DSTBN[0]#
G22 DSTBP[0]#
J26 DINV[0]#

DATA GRP 2

D[32]# AA23
D[33]# AB24
D[34]# V24
D[35]# V26
D[36]# W25
D[37]# U23
D[38]# U25
D[39]# U22
D[40]# AB25
D[41]# W22
D[42]# Y23
D[43]# AA26
D[44]# Y26
D[45]# Y22
D[46]# AC26
D[47]# AA24

H_D#32
H_D#33
H_D#34
H_D#35
H_D#36
H_D#37
H_D#38
H_D#39
H_D#40
H_D#41
H_D#42
H_D#43
H_D#44
H_D#45
H_D#46
H_D#47

H_D#[47:32] (5)

DSTBN[2]# W24
DSTBP[2]# Y25
DINV[2]# V23

H_DSTBN#2 (5)
H_DSTBP#2 (5)
H_DINV#2 (5)

(5) H_D#[31:16]

H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L25
H_D#21 L22
H_D#22 L23
H_D#23 M23
H_D#24 P25
H_D#25 P22
H_D#26 P23
H_D#27 T24
H_D#28 R24
H_D#29 L26
H_D#30 T25
H_D#31 N24

DATA GRP 1

D[16]# D[17]# D[18]# D[19]# D[20]# D[21]# D[22]# D[23]# D[24]# D[25]# D[26]# D[27]# D[28]# D[29]# D[30]# D[31]#

(5) H_DSTBN#1
(5) H_DSTBP#1
(5) H_DINV#1

M24 DSTBN[1]#
N25 DSTBP[1]#
M26 DINV[1]#

DATA GRP 3

D[48]# AC22
D[49]# AC23
D[50]# AB22
D[51]# AA21
D[52]# AB21
D[53]# AC25
D[54]# AD20
D[55]# AF22
D[56]# AF23
D[57]# AD24
D[58]# AE21
D[59]# AF25
D[60]# AE25
D[61]# AF24
D[62]# AF22
D[63]# AE26

H_D#48
H_D#49
H_D#50
H_D#51
H_D#52
H_D#53
H_D#54
H_D#55
H_D#56
H_D#57
H_D#58
H_D#59
H_D#60
H_D#61
H_D#62
H_D#63

H_D#[63:48] (5)

DSTBN[3]# AD23
DSTBP[3]# AE24
DINV[3]# AC20

H_DSTBN#3 (5)
H_DSTBP#3 (5)
H_DINV#3 (5)

+VCCP
R205 1KOhm 1%
Place these colse to CPU SKT
R206 2KOhm 1%
Merom A1 --- Install R208
Yonah B0 --- Install R207 and R208

GTL_REF AD26

GTLREF
TEST1
TEST2
BSEL[0]
BSEL[1]
BSEL[2]

MISC

COMP[0] R26 H_COMP0
COMP[1] U26 H_COMP1
COMP[2] U1 H_COMP2
COMP[3] V1 H_COMP3

DPRSTP# E5 H_DPRSTP#
DPSLP# B5
DPWR# D24
PWRGOOD D6 H_PWRGD
SLP# D7
PSI# AE6

H_DPSLP# (10)
H_DPWR# (5)
H_PWRGD (10)
H_SLP# (10)
PM_PSI# (62)

SOCKET479P

R207 1 2 51Ohm test1 /X C26
R208 1 2 51Ohm test2 D25

CPU_BSEL0 B22
CPU_BSEL1 B23
(17) CPU_BSEL2 C21

+VCCP
R218 10KOhm /X
(17) CPU_BSEL0
CPU_BSEL0
+3VS
+VCCP
R225 4.7KOhm
R223 4.7KOhm
R226 4.7KOhm
(8) STRP_CPU_FREQ0
Q202 PMBS3904

+VCCP
R230 10KOhm /X
(17) CPU_BSEL1
CPU_BSEL1
+3VS
+VCCP
R239 4.7KOhm
R237 4.7KOhm
R243 4.7KOhm
(8) STRP_CPU_FREQ1
Q205 PMBS3904
R238 10KOhm /X

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Length <= 0.5"
Zo=27.4 ohm
Space>= 20 mils
R231 27.4Ohm 1%
H_COMP0

Length <= 0.5"
Zo=27.4 ohm
Space>= 20 mils
R232 27.4Ohm 1%
H_COMP2

Length <= 0.5"
Zo=55 ohm
Space>= 20 mils
R241 54.9Ohm 1%
H_COMP1

Length <= 0.5"
Zo=55 ohm
Space>= 20 mils
R242 54.9Ohm 1%
H_COMP3

ASUS

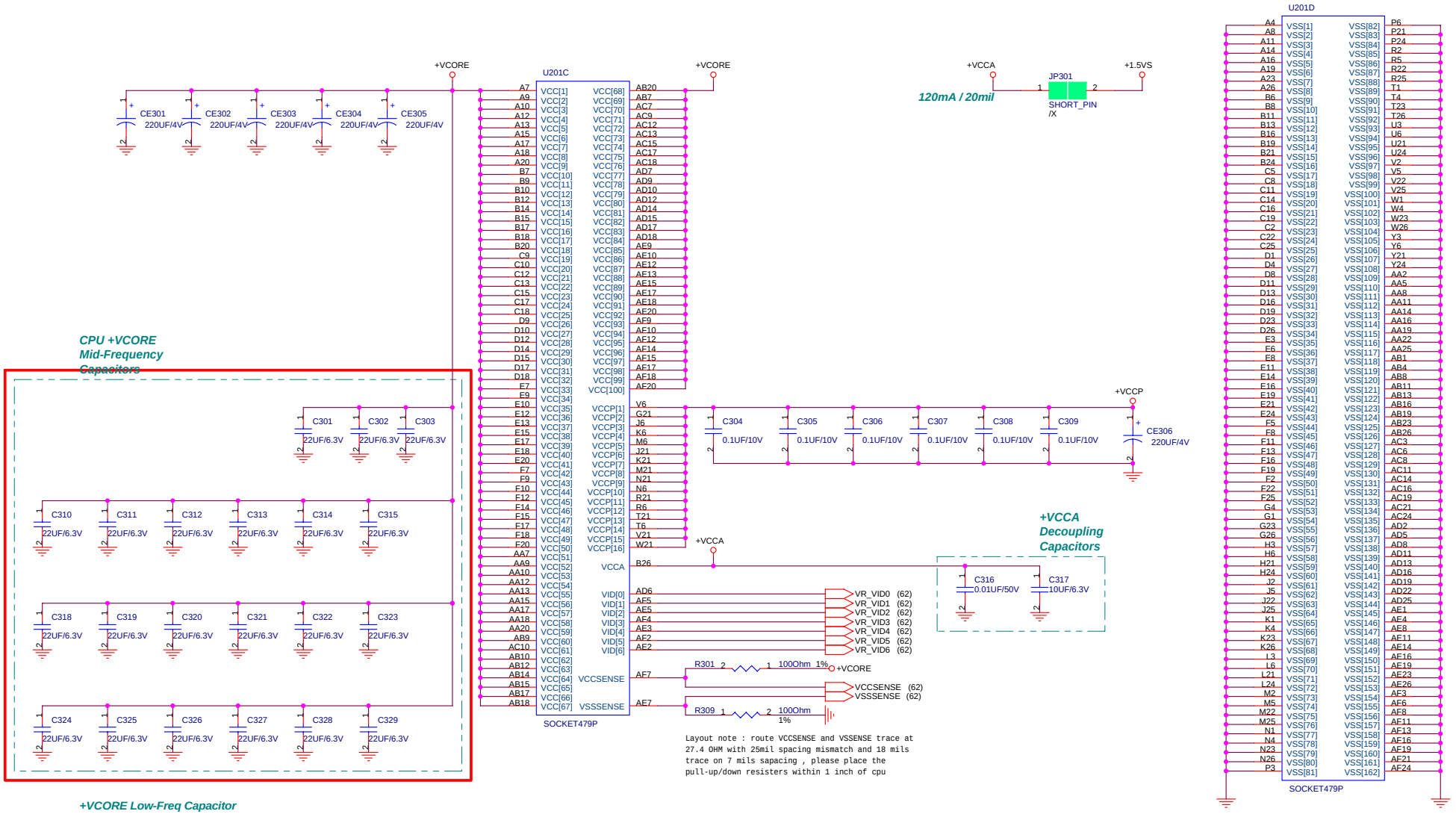
Title : Yonah CPU(1)

<OrgName>

Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

Date: Thursday, April 06, 2006 Sheet 2 of 45



+VCORE Low-Freq Capacitor
- Intel: 330UF *6
- ATI: 330UF *6
- R1F: 330UF *4
- A7J: 330UF *5

+VCORE Mid-Frequency Capacitor
- Intel: 22UF *32
- ATI: 10UF *26
- R1F: 22UF *16
- A7J: 22UF*29 use 19
- A6RF: 22UF*21 use 21

+VCCP Decoupling Capacitor
- Intel: 270UF *1, 0.1UF *6
- R1F: 220UF *1, 0.1UF *4
- A7J: 220UF *1, 0,1UF *6
- A6RF: 220UF *1, 0,1UF *6

<OrgName>	Title : Yonah CPU(2)	
	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 3 of 45	

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

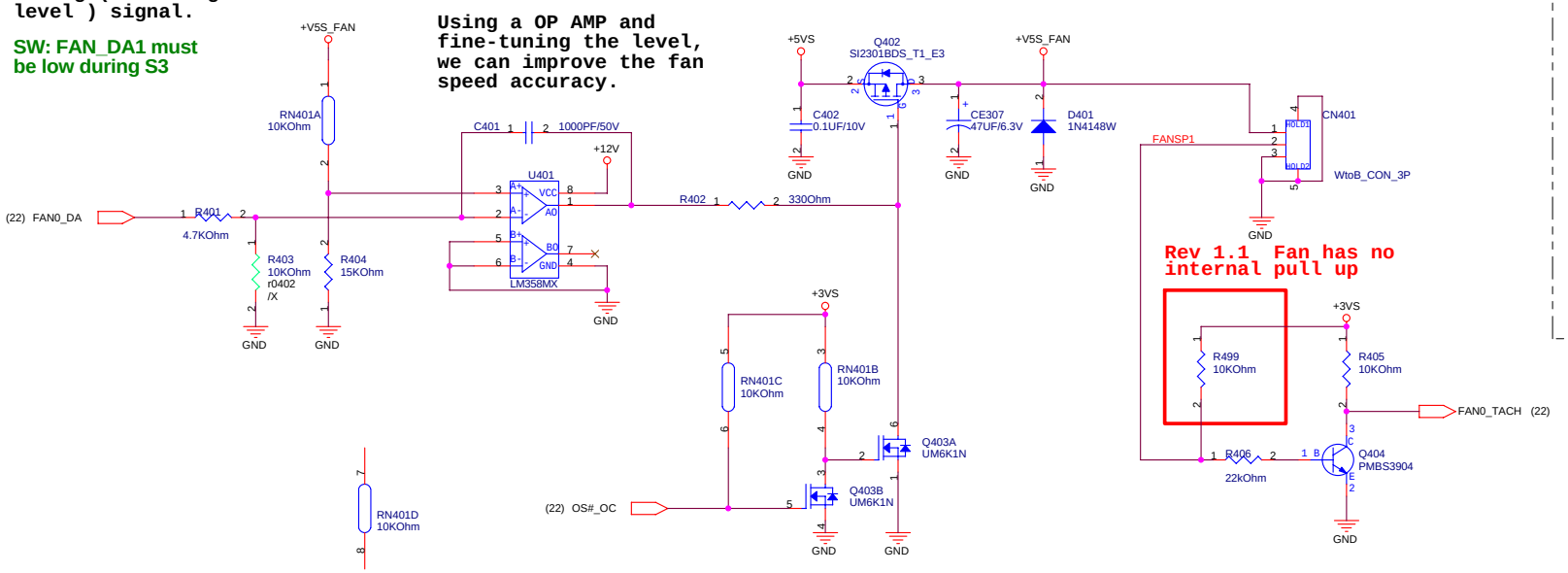
SW: FAN_DA1 must be low during S3

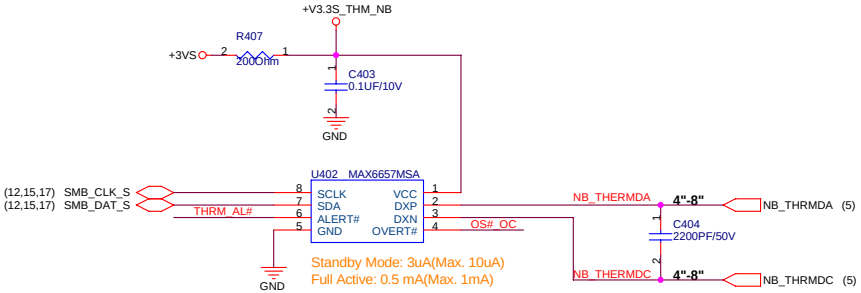
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

Route H_THERMDA and H_THERMDC on the same layer

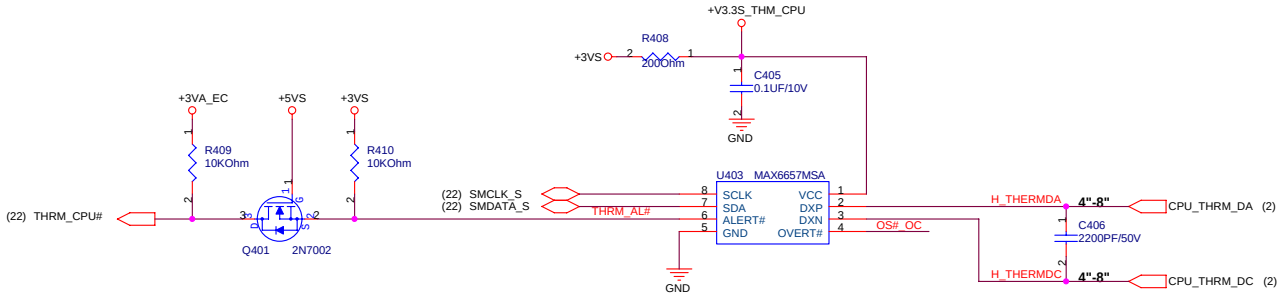
----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



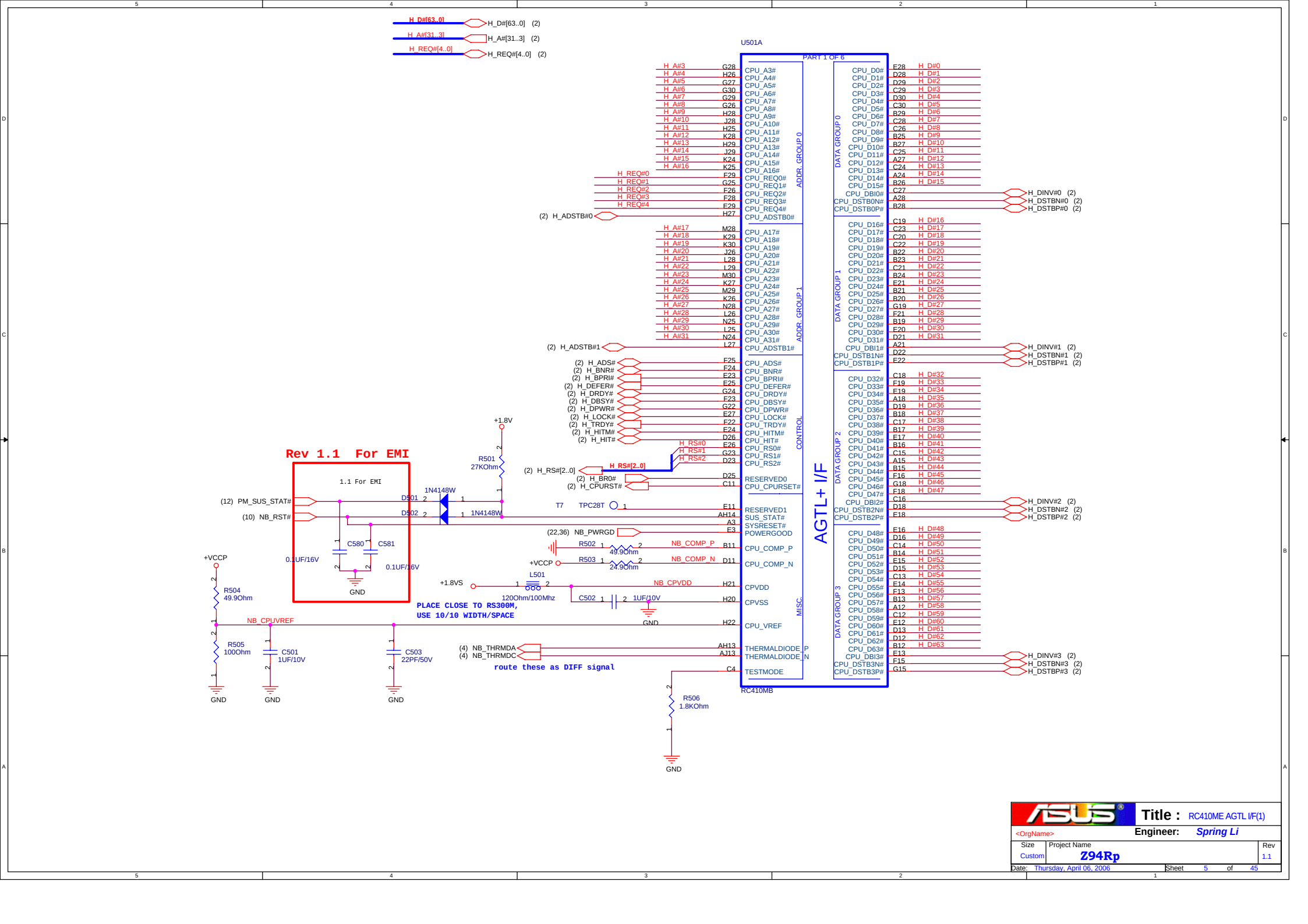


NB Detect

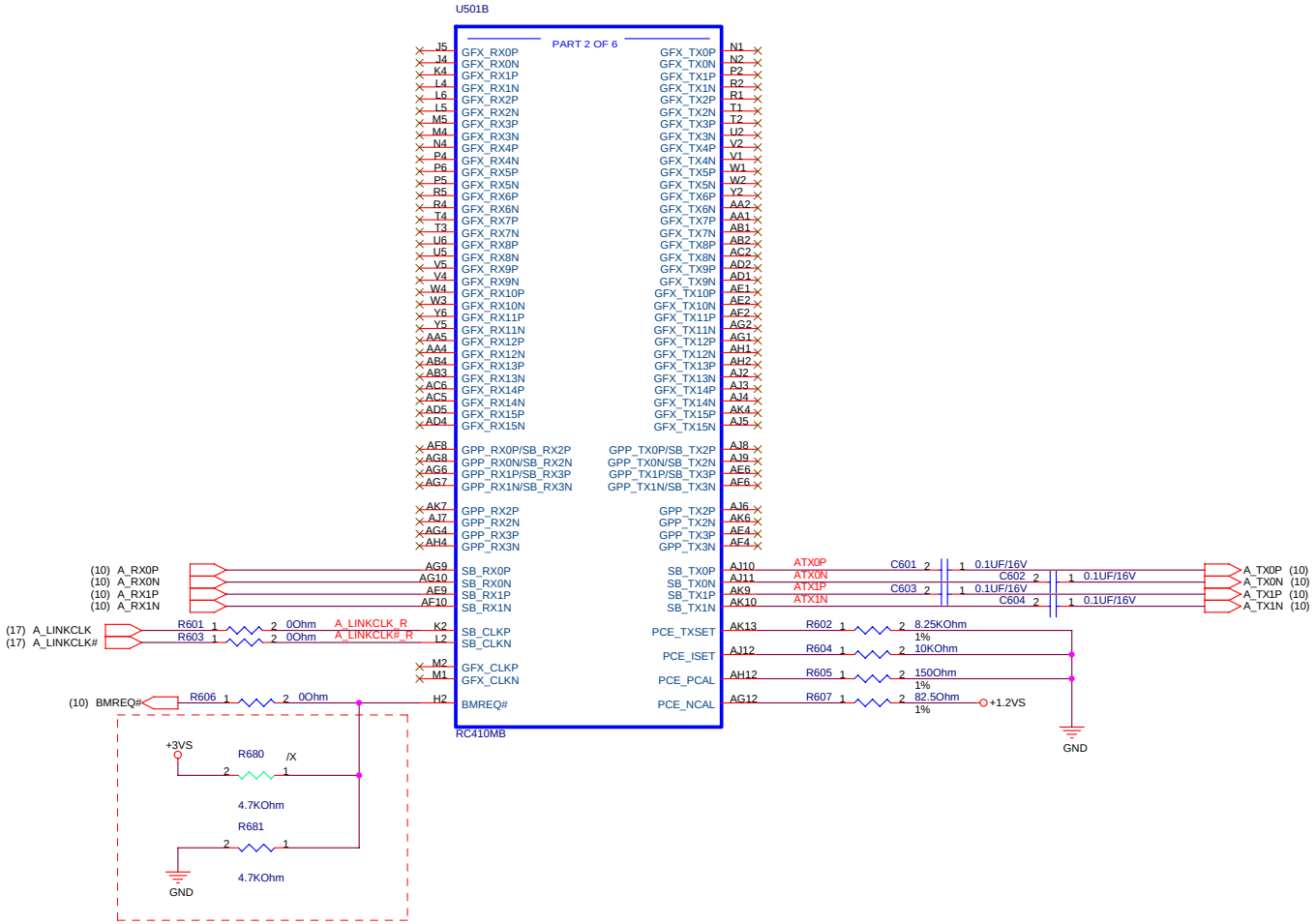


CPU Detect

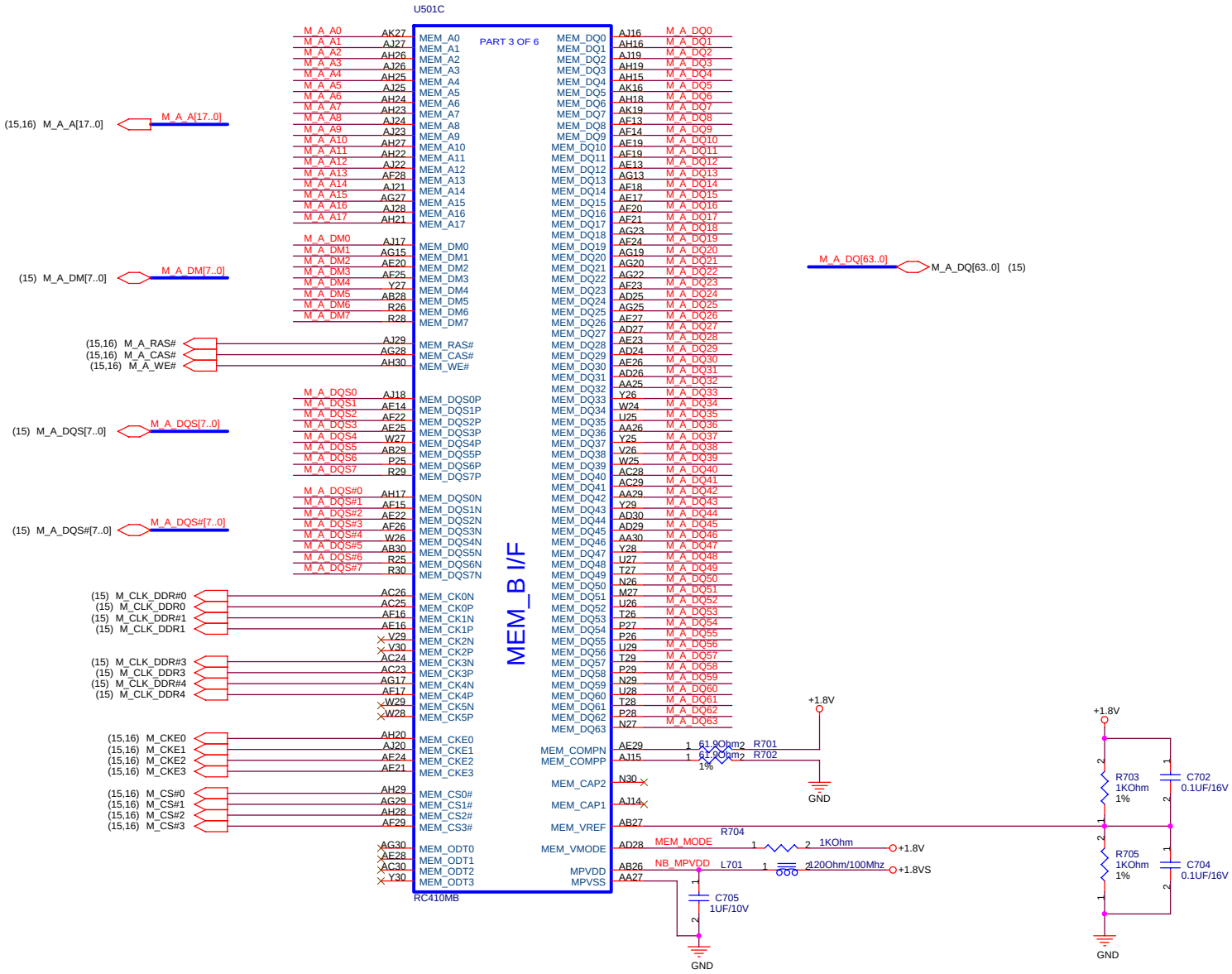
Title :	THERMAL SERSOR,FAN	
<OrgName>	Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 4 of 45	



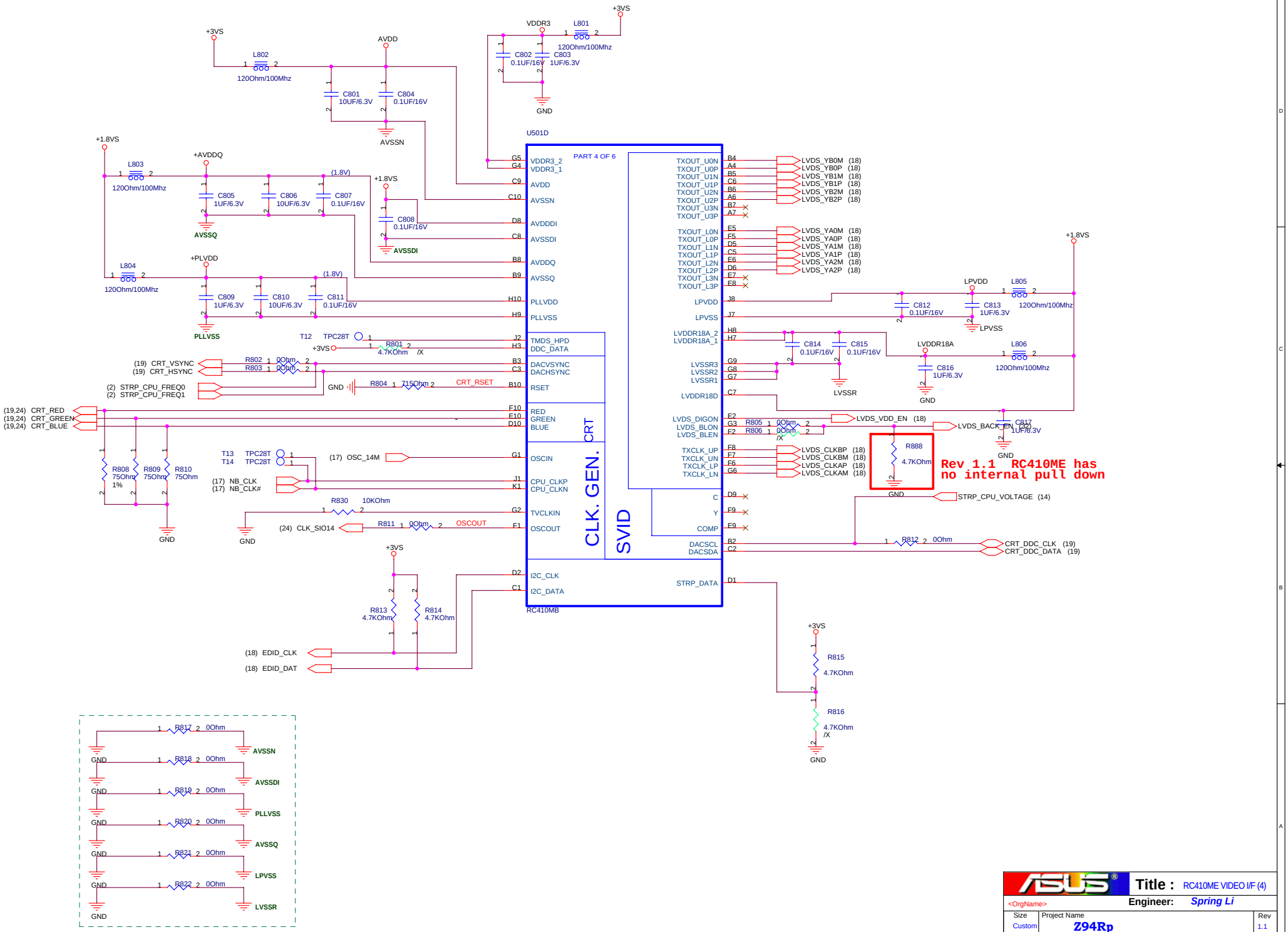
<OrgName>	Title : RC410ME AGTL I/F(1)		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 5 of 45		



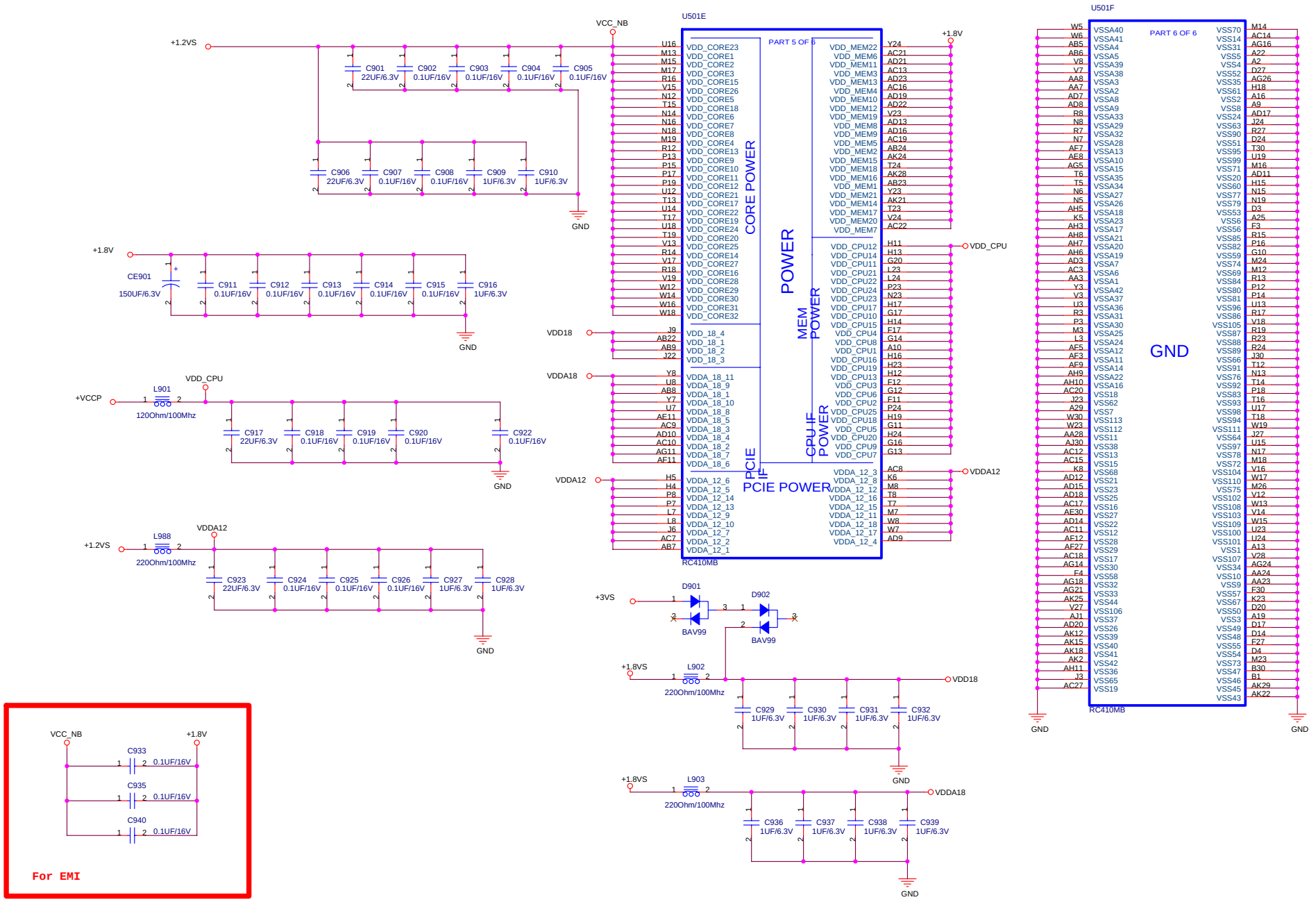
Title :	RC410ME PCIE & A-Link(2)	
<OrgName>	Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 6 of 45	



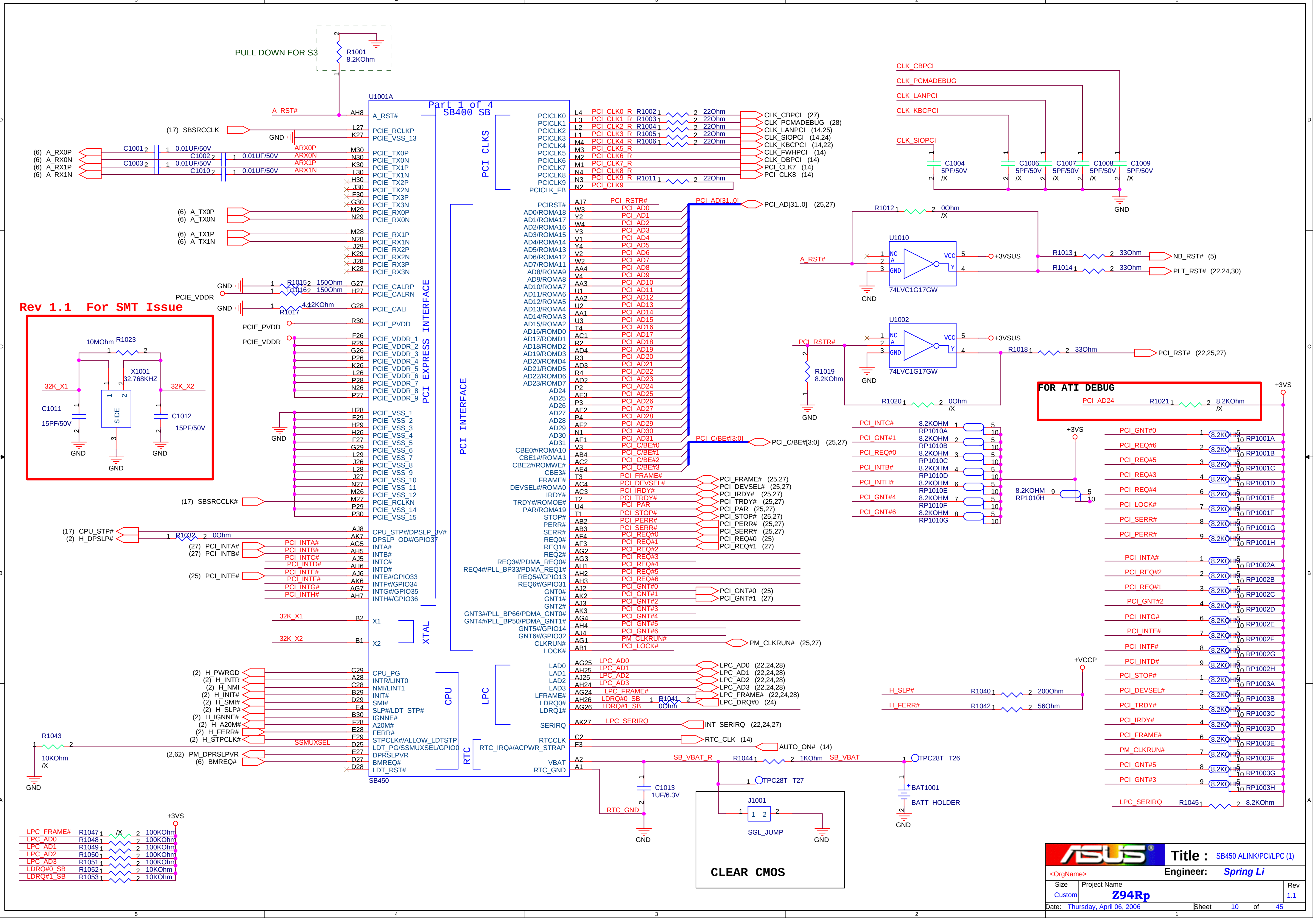
<OrgName>	Title : RC410ME DDR2 I/F (3)		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Thursday, April 06, 2006		Sheet 7 of 45	

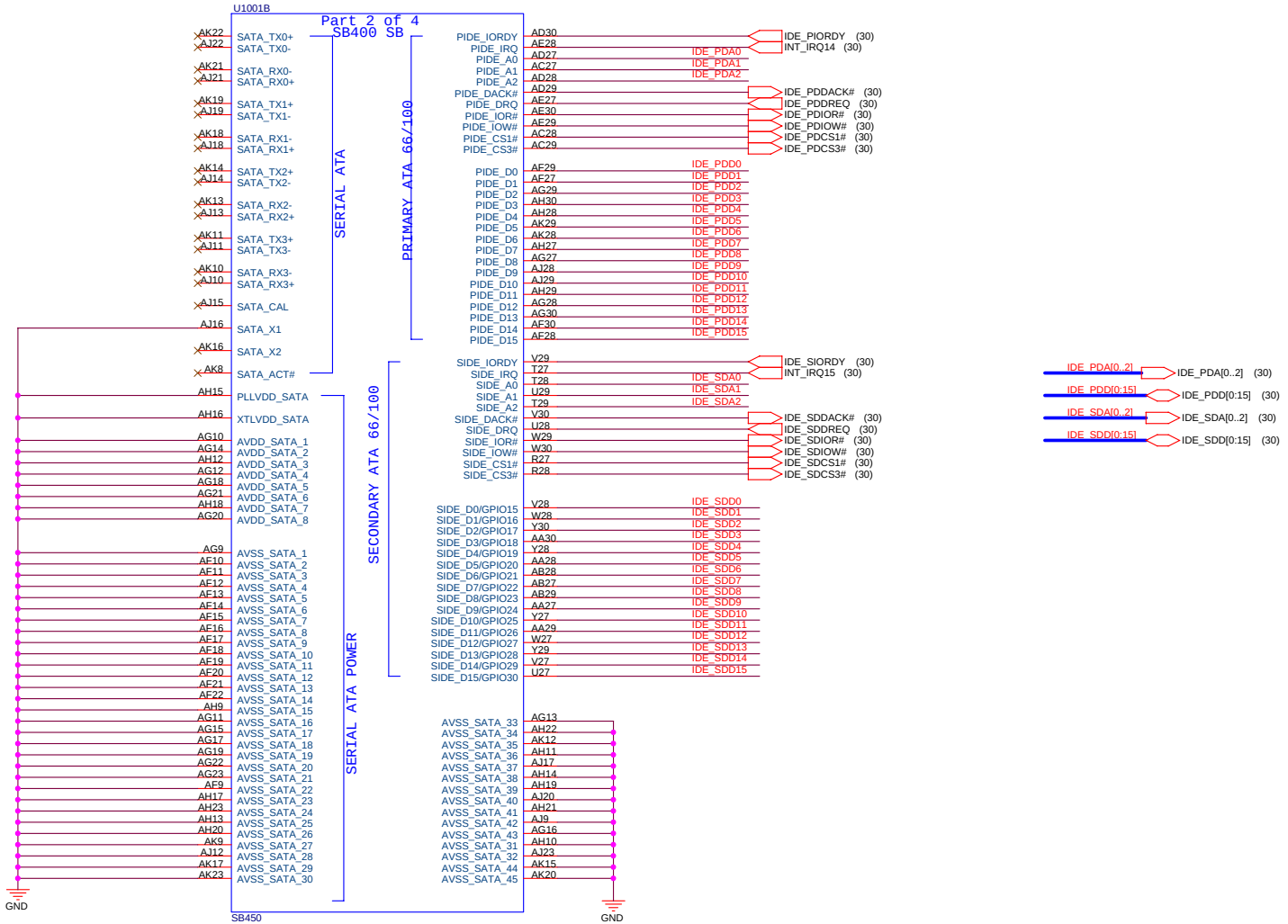


ASUS	Title :	RC410ME VIDEO I/F (4)
<OrgName>	Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 8 of 45	

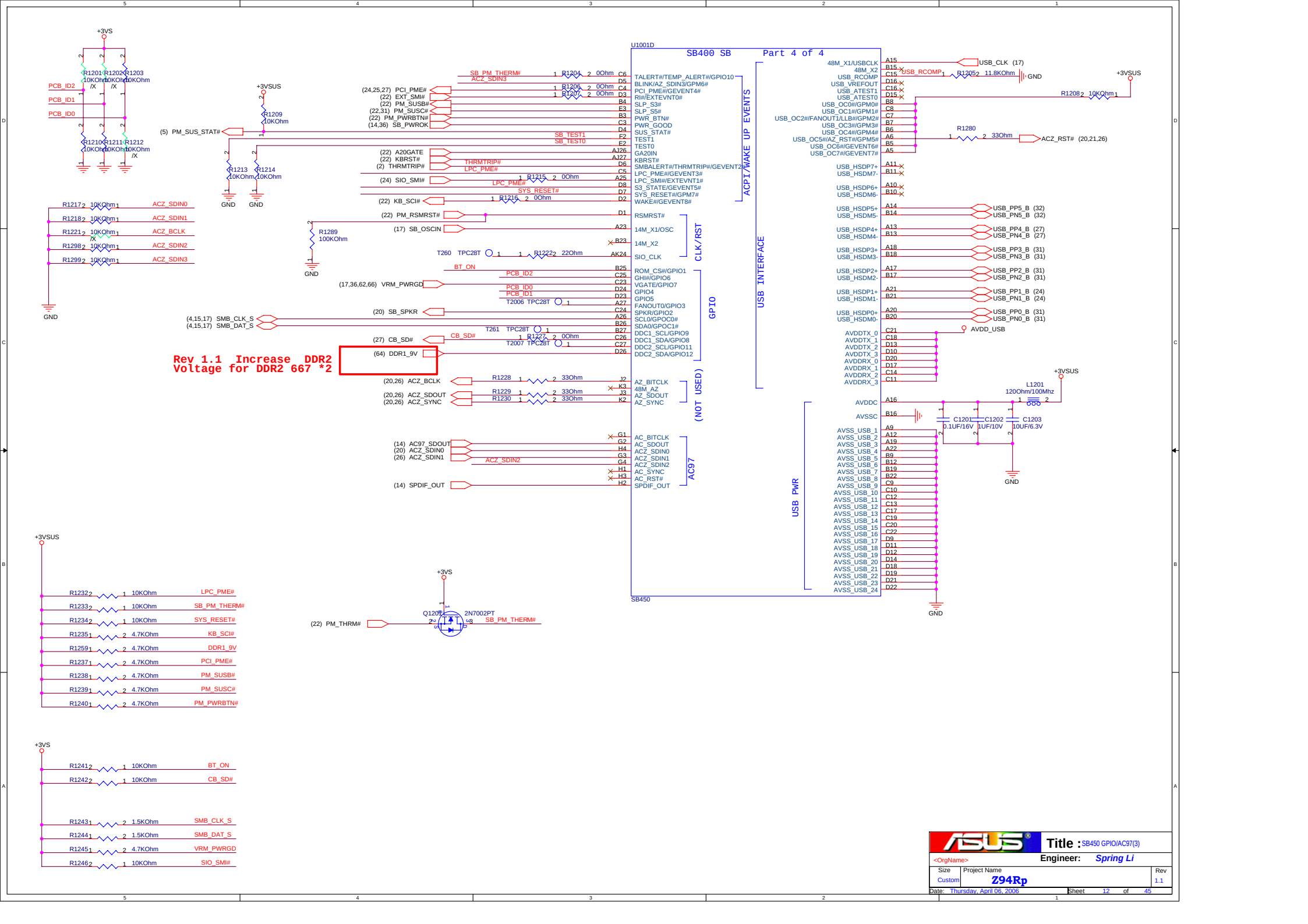


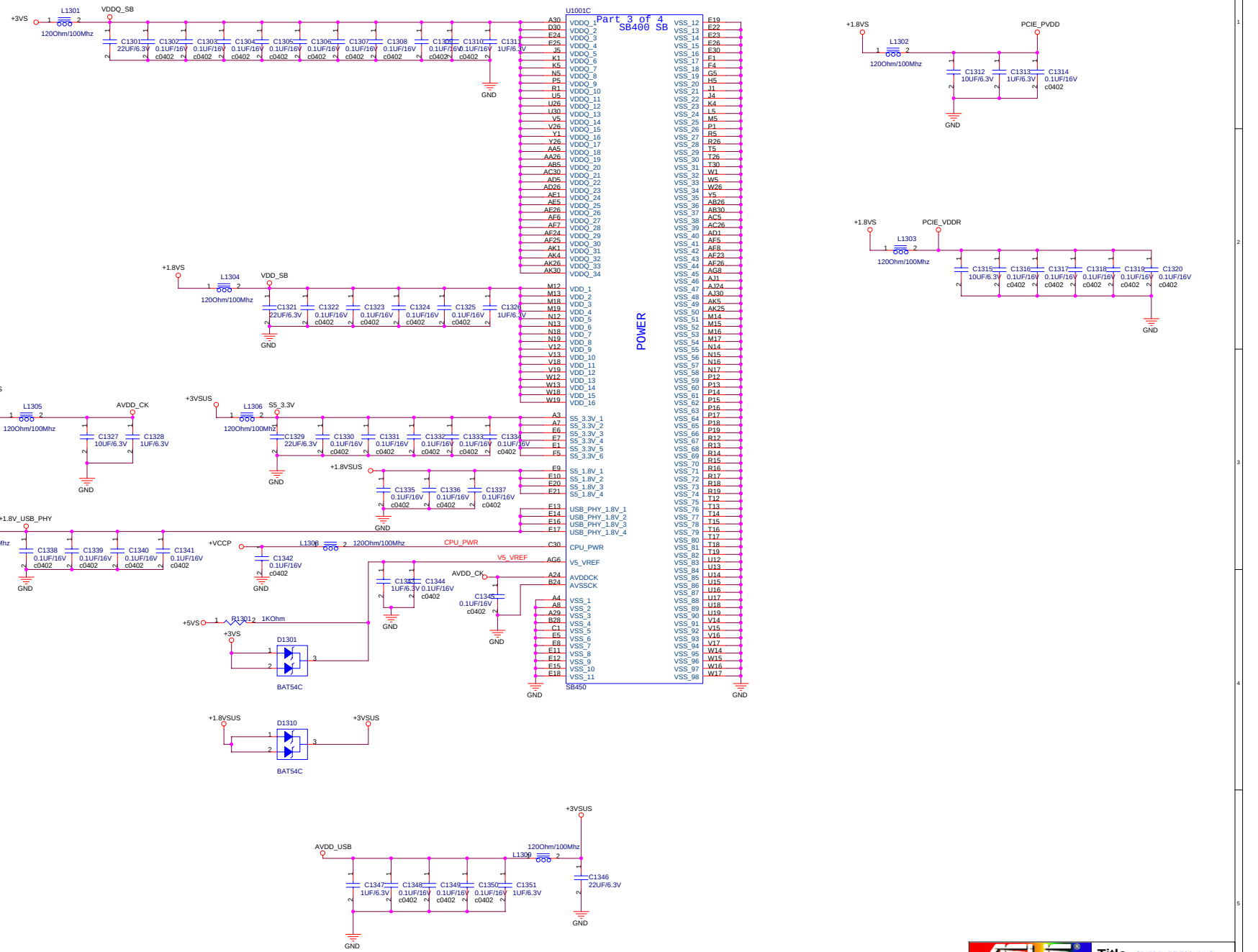
Title :	RC410ME POWER (5)		
<OrgName>	Engineer:	Spring Li	
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 9	of 45	


PULL DOWN FOR S3
R1001
8.2KOhm
U1001A
Part 1 of 4
SB400 SB
A_RST#
PCIE_RCLKP
PCIE_VSS_13
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
CPU
LPC
RTC
SB450
Rev 1.1 For SMT Issue
X1001
32.768KHZ
R1023
10MOhm
C1011
15PF/50V
C1012
15PF/50V
32K_X1
32K_X2
GND
U1010
74LVC1G17GW
U1002
74LVC1G17GW
NB_RST# (5)
PLT_RST# (22,24,30)
PCI_RST# (22,25,27)
FOR ATI DEBUG
PCI_AD[31..0] (25,27)
PCI_C/BE#[3:0] (25,27)
PM_CLKRUN# (25,27)
INT_SERIRQ (22,24,27)
RTC_CLK (14)
AUTO_ON# (14)
C1013
1UF/6.3V
J1001
SGL_JUMP
CLEAR CMOS
BAT1001
BATT_HOLDER
TPC28T T26
TPC28T T27
+3VS
+3VSUS
+VCCP
CLK_CBPCI
CLK_PCMADEBUG
CLK_LANPCI
CLK_KBCPCI
CLK_SIOPCI
C1004
C1006
C1007
C1008
C1009
5PF/50V
Title : SB450 ALINK/PCI/LPC (1)
<OrgName>
Engineer: Spring Li
Size
Custom
Project Name
Z94Rp
Rev
1.1
Date: Thursday, April 06, 2006
Sheet 10 of 45



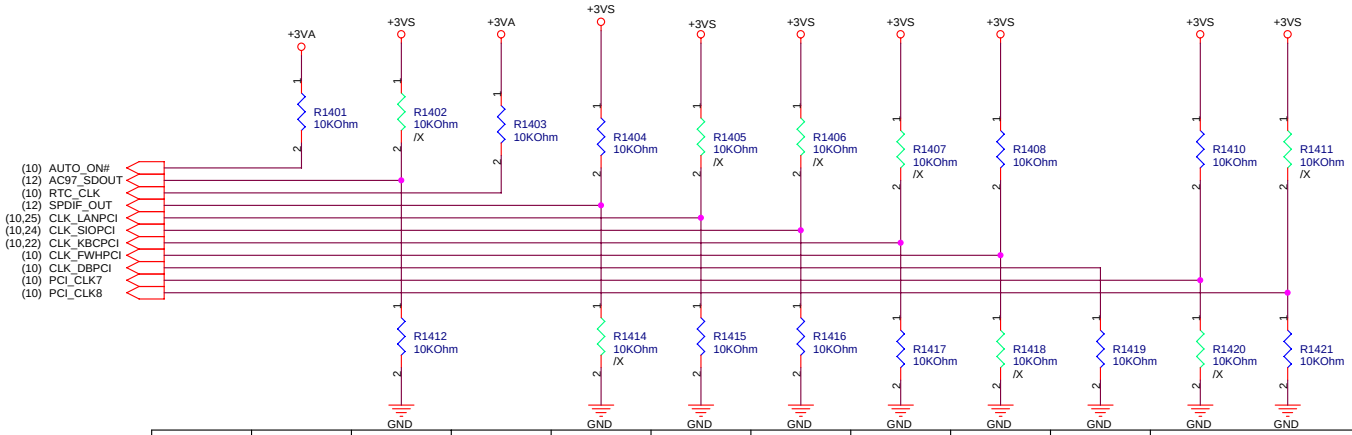
Title : SB450 IDE (2)		
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 11 of 45	


U1001D
SB400 SB Part 4 of 4
SB450
ACPI/WAKE UP EVENTS
USB INTERFACE
CLK/RST
GPIO
AC97
USB PWR
(NOT USED)
Rev 1.1 Increase DDR2
Voltage for DDR2 667 *2
Title : SB450 GPIO/AC97(3)
<OrgName>
Engineer: Spring Li
Size Custom
Project Name Z94Rp
Rev 1.1
Date: Thursday, April 06, 2006
Sheet 12 of 45



Title : SB450 PWR/DECOUPING			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 13 of 45		

REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4	

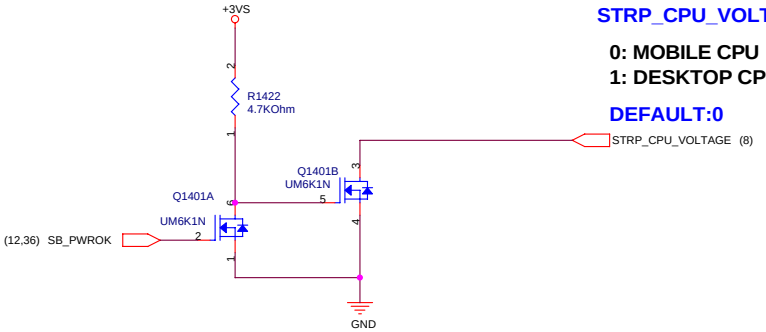
NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

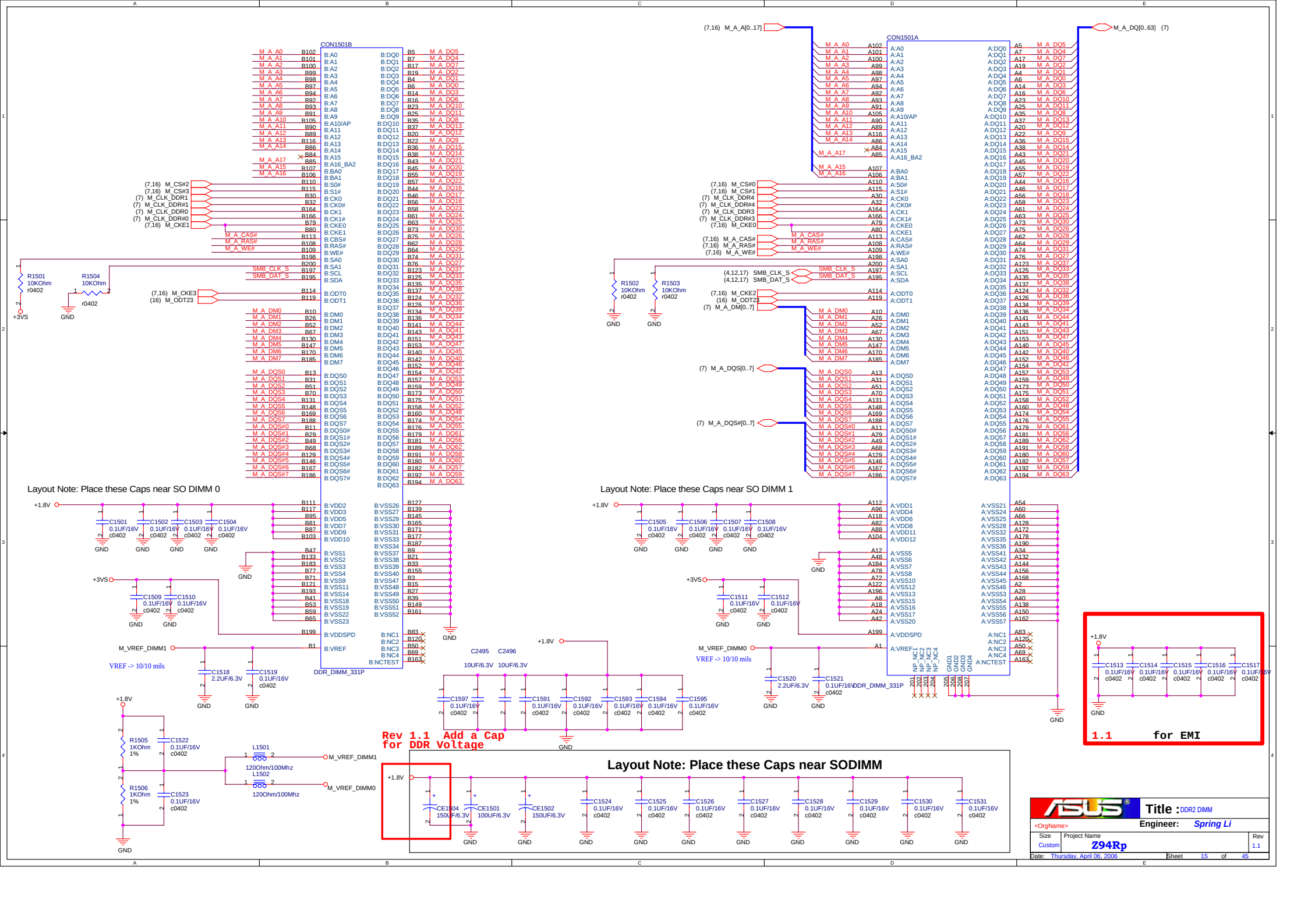


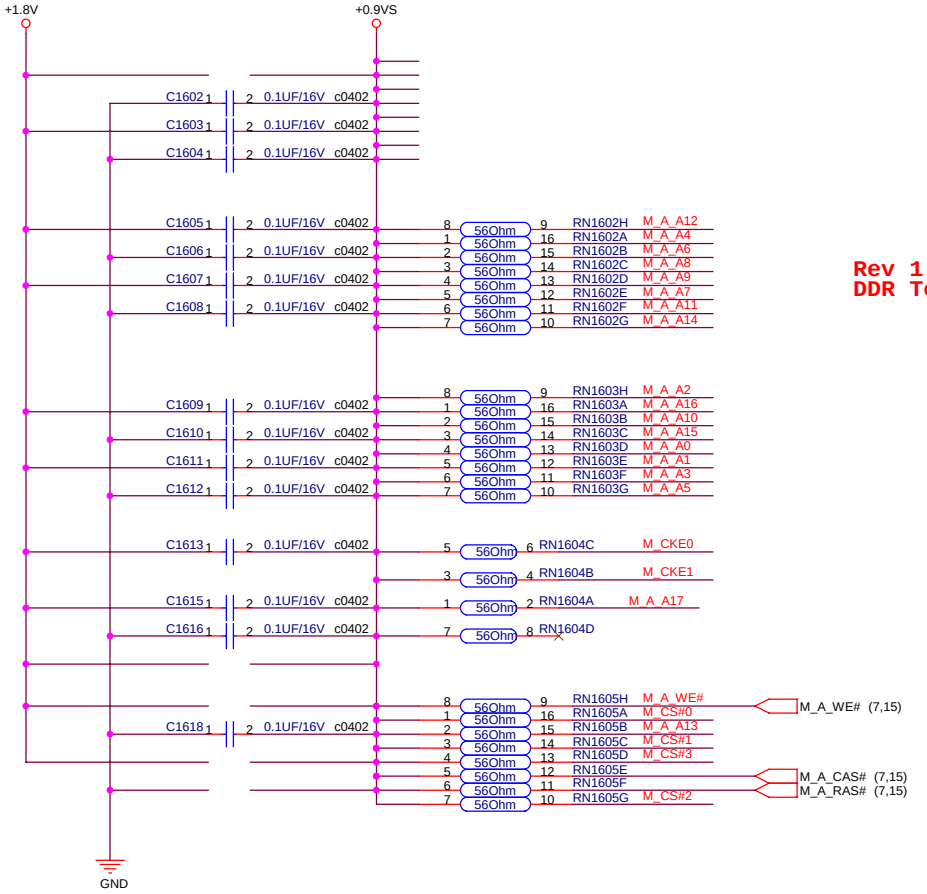
STRP_CPU_VOLTAGE: CPU VCC

0: MOBILE CPU
1: DESKTOP CPU

DEFAULT:0

<OrgName>	Title : SB450 STRAPS(5)	
	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 14 of 45	


CON1501B
CON1501A
DDR_DIMM_331P
Layout Note: Place these Caps near SO DIMM 0
Layout Note: Place these Caps near SO DIMM 1
Layout Note: Place these Caps near SODIMM
Rev 1.1 Add a Cap for DDR Voltage
1.1 for EMI
VREF -> 10/10 mils
Title : DDR2 DIMM
Engineer: Spring Li
Project Name Z94Rp
Size Custom
Rev 1.1
Date: Thursday, April 06, 2006
Sheet 15 of 45

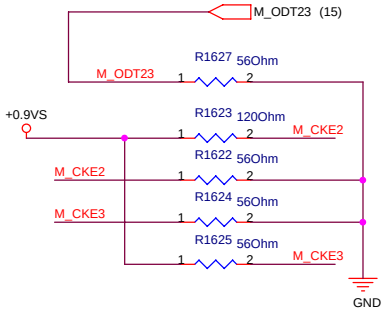


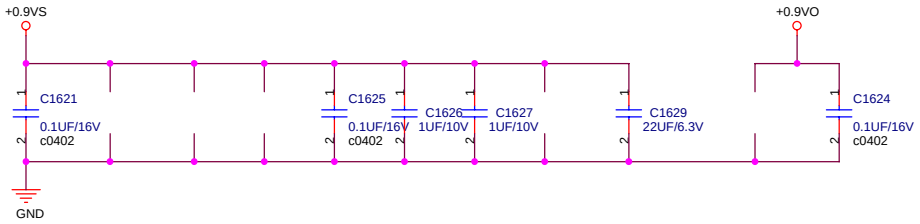
Rev 1.1 swap for DDR Termination

M_CS#[0..3] (7,15)

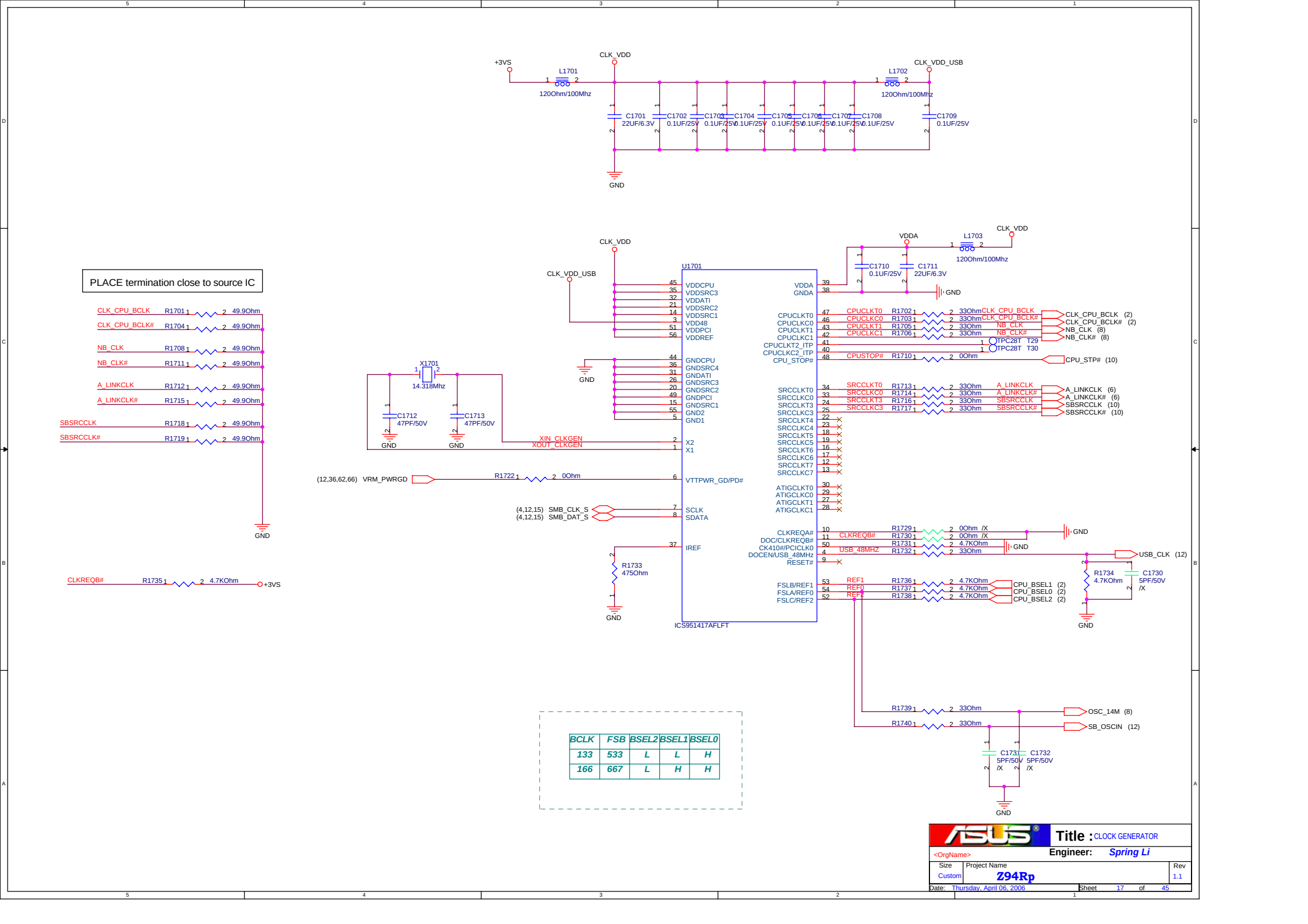
M_CKE[0..3] (7,15)

M_A_A[0..17] (7,15)

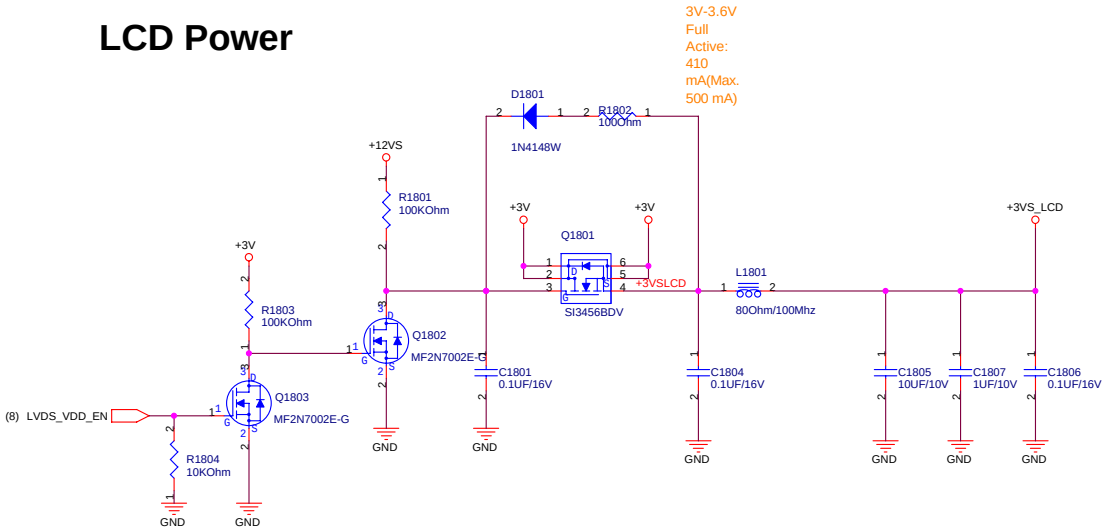


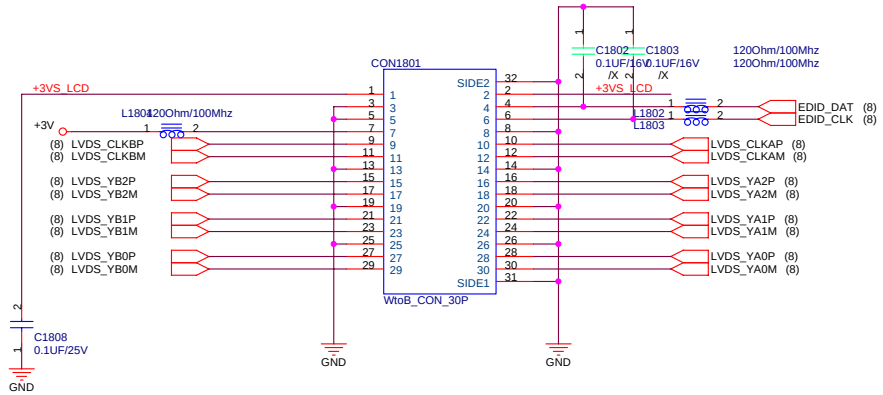


Title : DDR2 Termination		
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 16 of 45	


PLACE termination close to source IC
CLK_CPU_BCLK R1701 49.9Ohm
CLK_CPU_BCLK# R1704 49.9Ohm
NB_CLK R1708 49.9Ohm
NB_CLK# R1711 49.9Ohm
A_LINKCLK R1712 49.9Ohm
A_LINKCLK# R1715 49.9Ohm
SBSRCCLK R1718 49.9Ohm
SBSRCCLK# R1719 49.9Ohm
GND
CLKREQB# R1735 4.7KOhm +3VS
+3VS
L1701 120Ohm/100Mhz
CLK_VDD
L1702 120Ohm/100Mhz
CLK_VDD_USB
C1701 22UF/6.3V
C1702 0.1UF/25V
C1703 0.1UF/25V
C1704 0.1UF/25V
C1705 0.1UF/25V
C1706 0.1UF/25V
C1707 0.1UF/25V
C1708 0.1UF/25V
C1709 0.1UF/25V
GND
U1701
VDDCPU
VDDSRC3
VDDATI
VDDSRC2
VDDSRC1
VDD48
VDDPCI
VDDREF
GNDCPU
GNDSRC4
GNDATI
GNDSRC3
GNDSRC2
GNDPCI
GNDSRC1
GND2
GND1
X1701 14.318Mhz
C1712 47PF/50V
C1713 47PF/50V
XIN_CLKGEN
XOUT_CLKGEN
X2
X1
(12,36,62,66) VRM_PWRGD R1722 0Ohm
VTTPWR_GD/PD#
(4,12,15) SMB_CLK_S
(4,12,15) SMB_DAT_S
SCLK
SDATA
IREF
R1733 475Ohm
ICS951417AFLFT
VDDA
GNDA
L1703 120Ohm/100Mhz
C1710 0.1UF/25V
C1711 22UF/6.3V
CPUCLKT0 R1702 33Ohm CLK_CPU_BCLK
CPUCLKC0 R1703 33Ohm CLK_CPU_BCLK#
CPUCLKT1 R1705 33Ohm NB_CLK
CPUCLKC1 R1706 33Ohm NB_CLK#
CPUCLKT2_ITP
CPUCLKC2_ITP
CPU_STOP# R1710 0Ohm
TPC28T T29
TPC28T T30
CLK_CPU_BCLK (2)
CLK_CPU_BCLK# (2)
NB_CLK (8)
NB_CLK# (8)
CPU_STP# (10)
SRCCLKT0 R1713 33Ohm A_LINKCLK
SRCCLKC0 R1714 33Ohm A_LINKCLK#
SRCCLKT3 R1716 33Ohm SBSRCCLK
SRCCLKC3 R1717 33Ohm SBSRCCLK#
A_LINKCLK (6)
A_LINKCLK# (6)
SBSRCCLK (10)
SBSRCCLK# (10)
CLKREQA#
CLKREQB# R1729 0Ohm /X
CLKREQB# R1730 0Ohm /X
DOC/CLKREQB# R1731 4.7KOhm
CK410#/PCICLK0 USB_48MHZ R1732 33Ohm
DOCEN/USB_48MHz
RESET#
USB_CLK (12)
R1734 4.7KOhm
C1730 5PF/50V /X
FSLB/REF1 REF1 R1736 4.7KOhm CPU_BSEL1 (2)
FSLA/REF0 REF0 R1737 4.7KOhm CPU_BSEL0 (2)
FSLC/REF2 REF2 R1738 4.7KOhm CPU_BSEL2 (2)
R1739 33Ohm OSC_14M (8)
R1740 33Ohm SB_OSCIN (12)
C1731 5PF/50V /X
C1732 5PF/50V /X
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GENERATOR
<OrgName>
Engineer: Spring Li
Size Custom
Project Name Z94Rp
Rev 1.1
Date: Thursday, April 06, 2006
Sheet 17 of 45

LCD Power

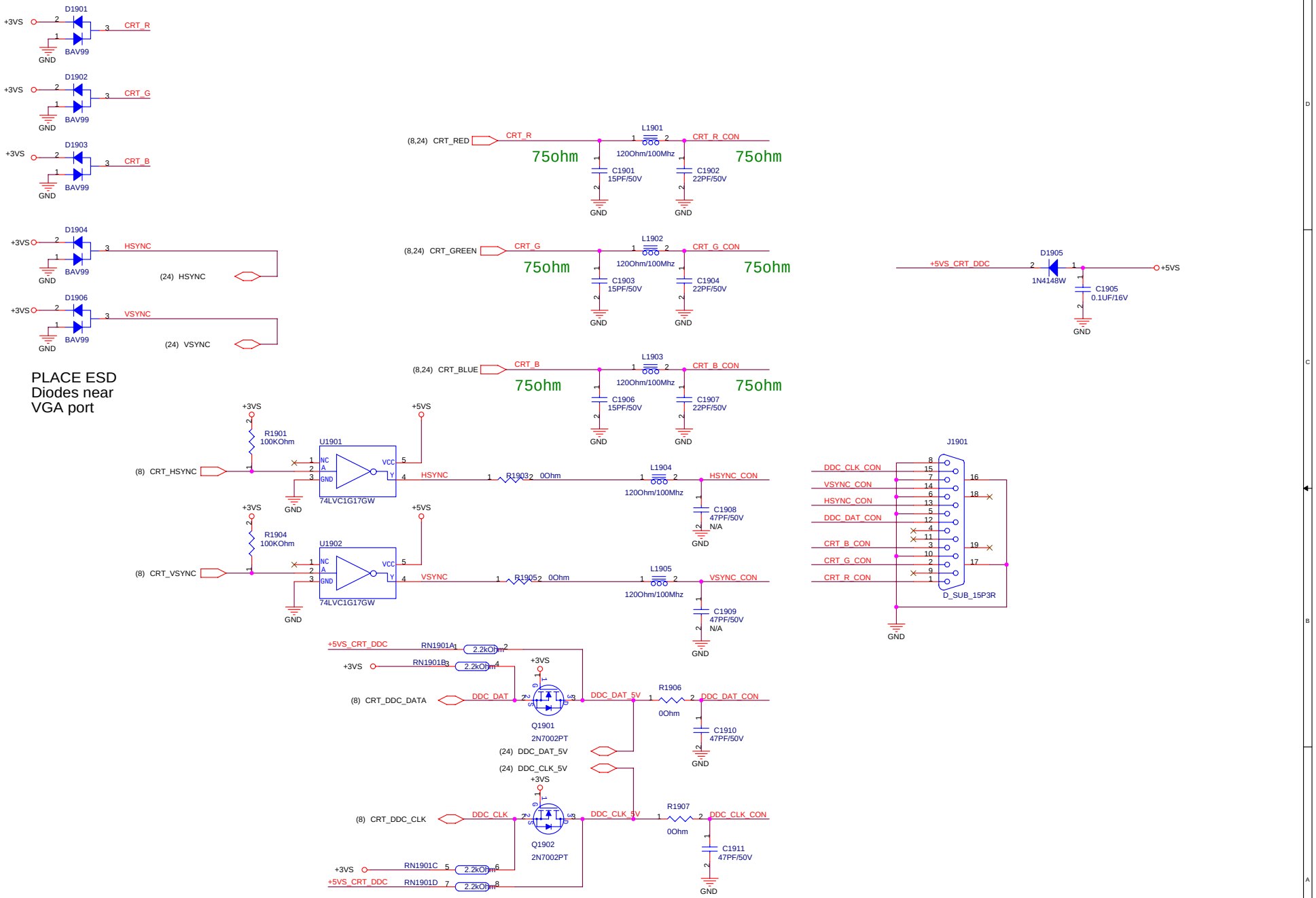




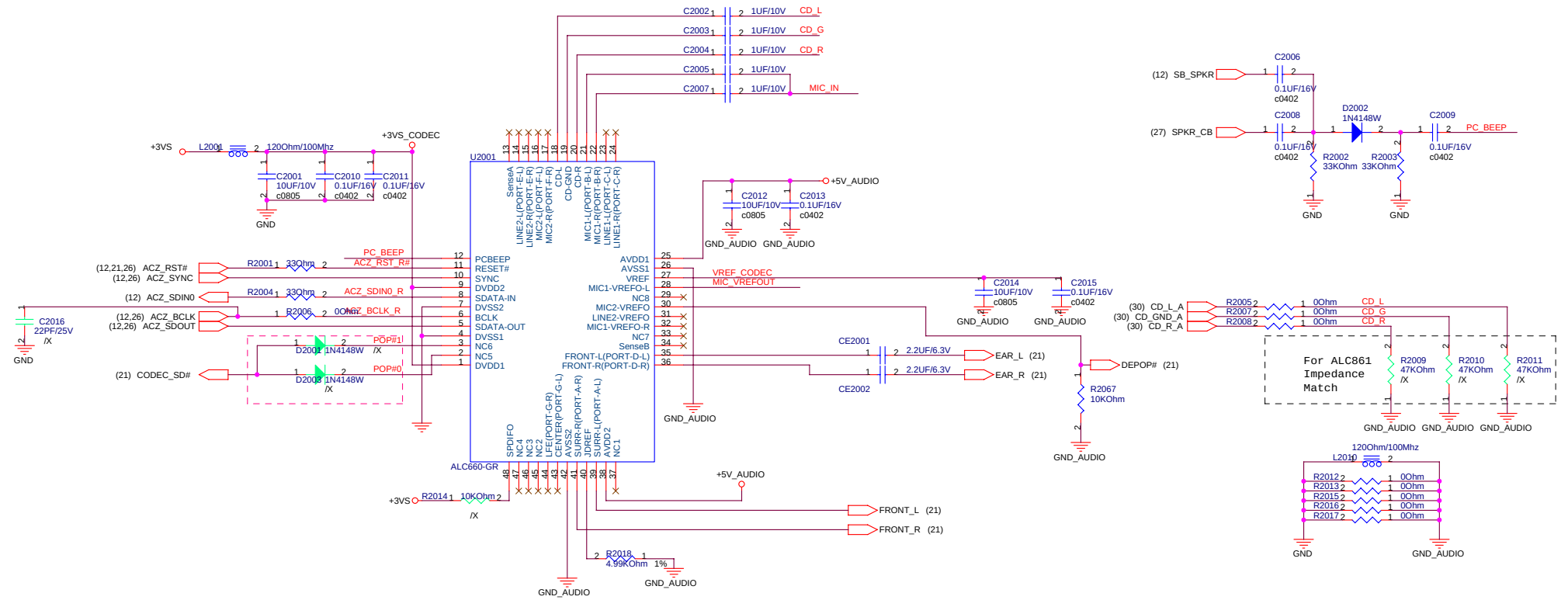
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

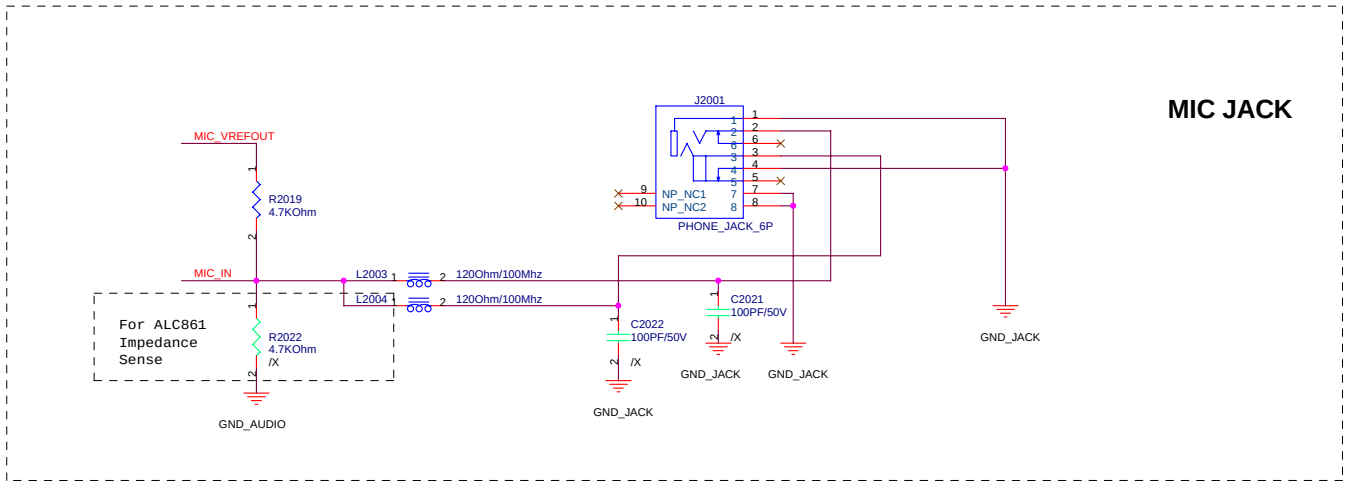
LCD LVDS Interface

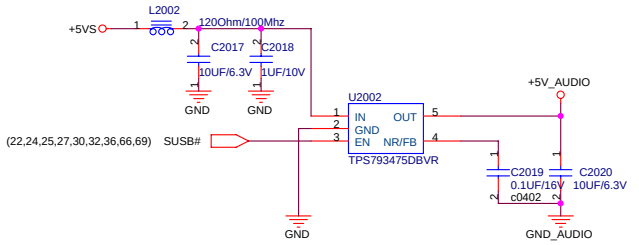
<OrgName>		Title :	LVDS & INVERTER (CAMERA)
		Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Thursday, April 06, 2006		Sheet 18 of 45	



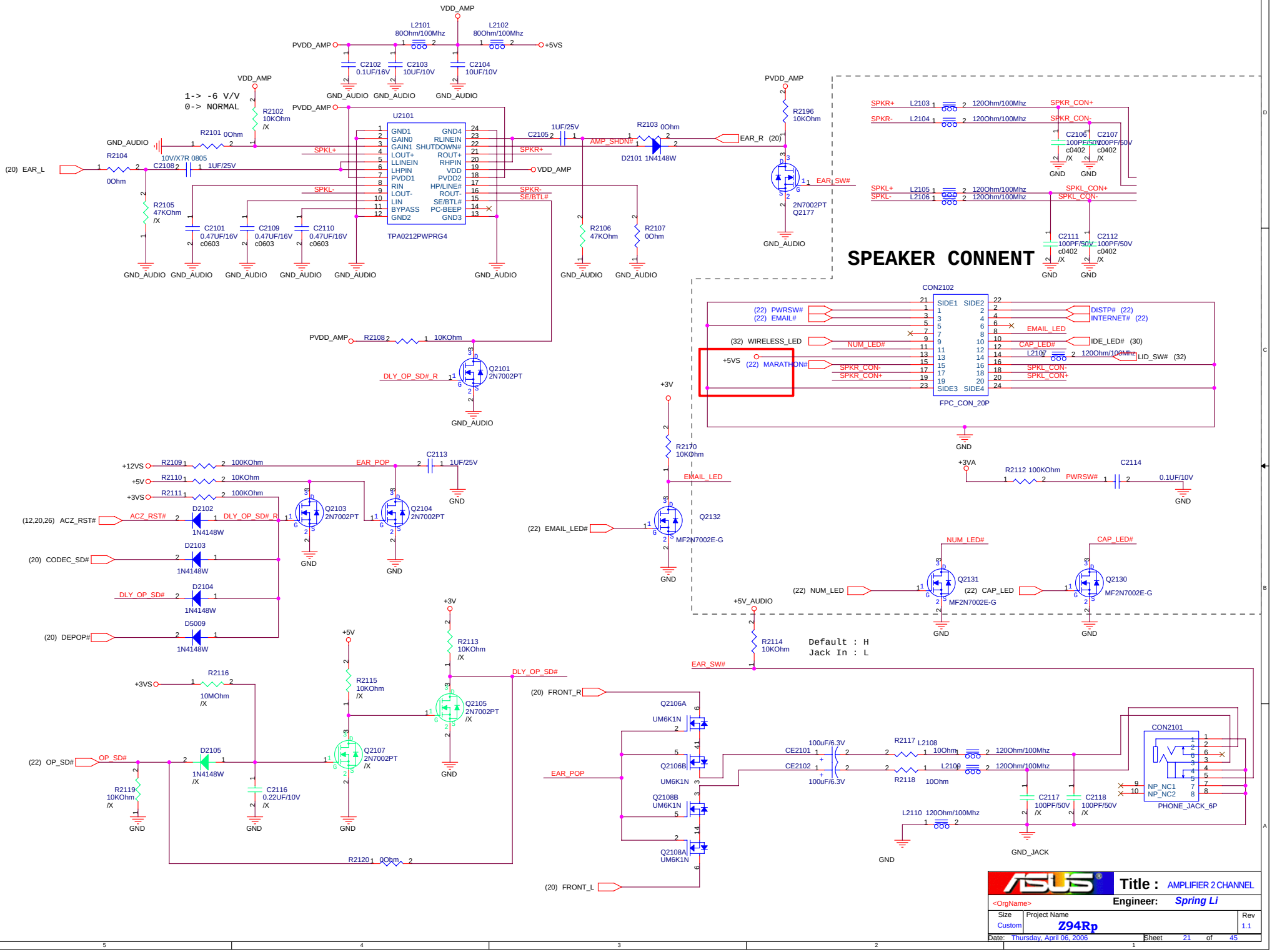
ASUS	Title : CRT CONNECTOR		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 19 of 45		

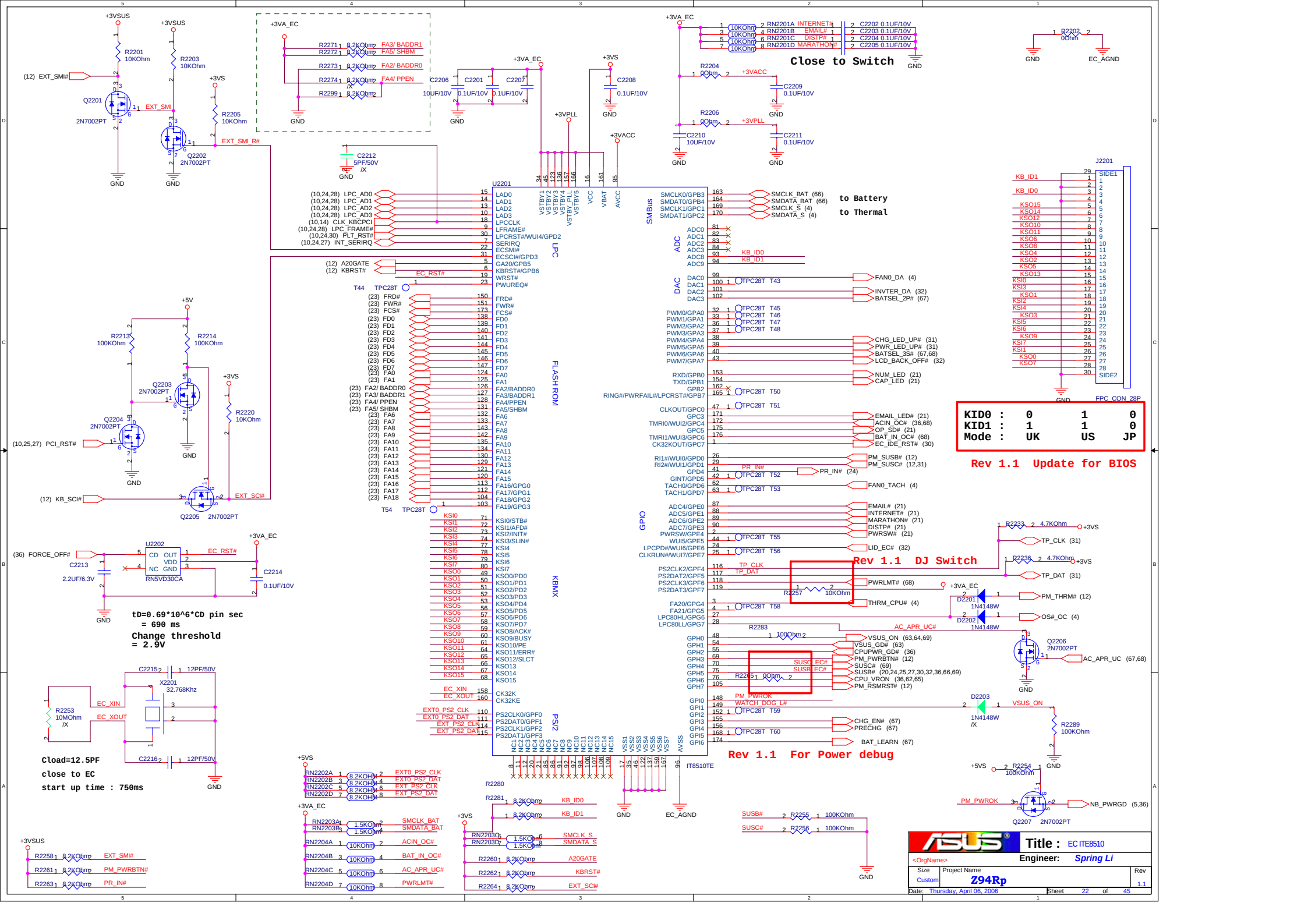






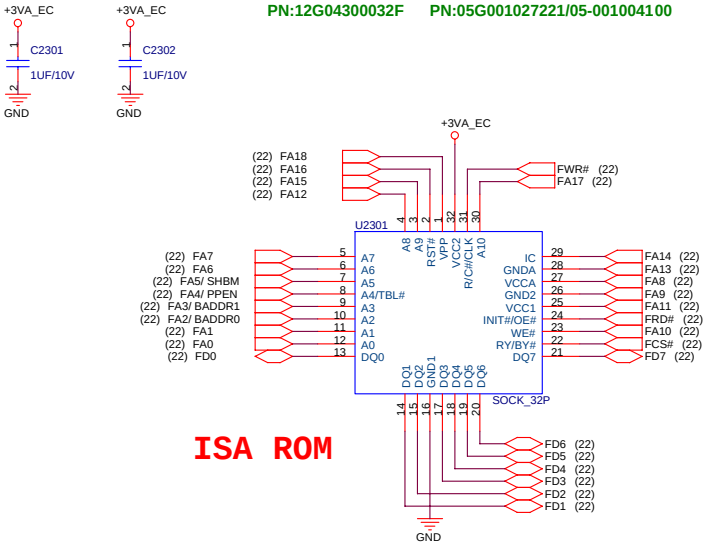
ASUS	Title : AZALIA	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 20 of 45	


SPEAKER CONNENT
U2101
TPA0212PWPRG4
1-> -6 V/V
0-> NORMAL
Default : H
Jack In : L
Title : AMPLIFIER 2 CHANNEL
Engineer: Spring Li
Z94Rp
Thursday, April 06, 2006
Sheet 21 of 45


Close to Switch
to Battery
to Thermal
Rev 1.1 Update for BIOS
KID0 : 0 1 0
KID1 : 1 1 0
Mode : UK US JP
Rev 1.1 DJ Switch
Rev 1.1 For Power debug
tD=0.69*10^6*CD pin sec
= 690 ms
Change threshold
= 2.9V
Cload=12.5PF
close to EC
start up time : 750ms
U2201
IT8510TE
J2201
FPC_CON_28P
Title : EC ITE8510
Engineer: Spring Li
Project Name
Z94Rp
Rev
1.1
Date: Thursday, April 06, 2006
Sheet 22 of 45

PLCC32 Socket
PN:12G04300032F

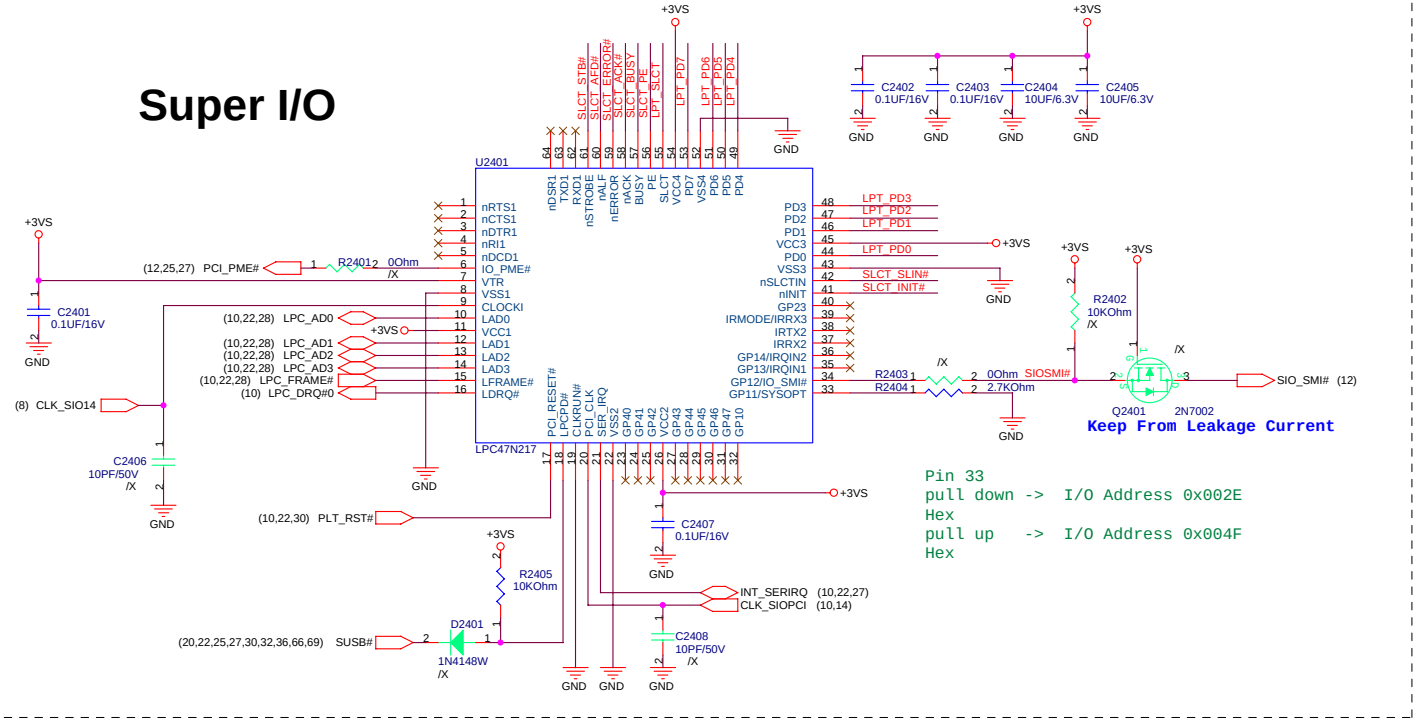
SST-PLCC32 4Mbits Flash ROM
PN:05G001027221/05-001004100

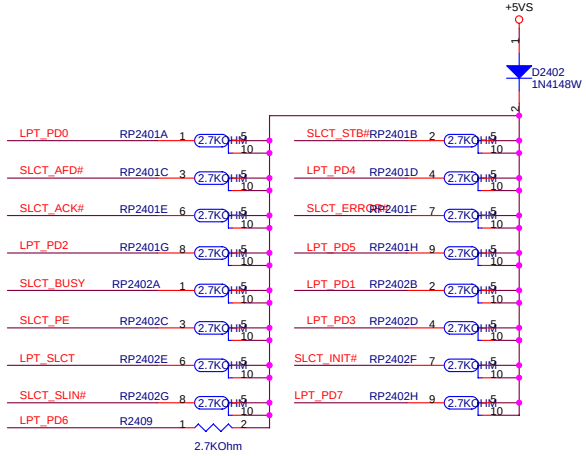


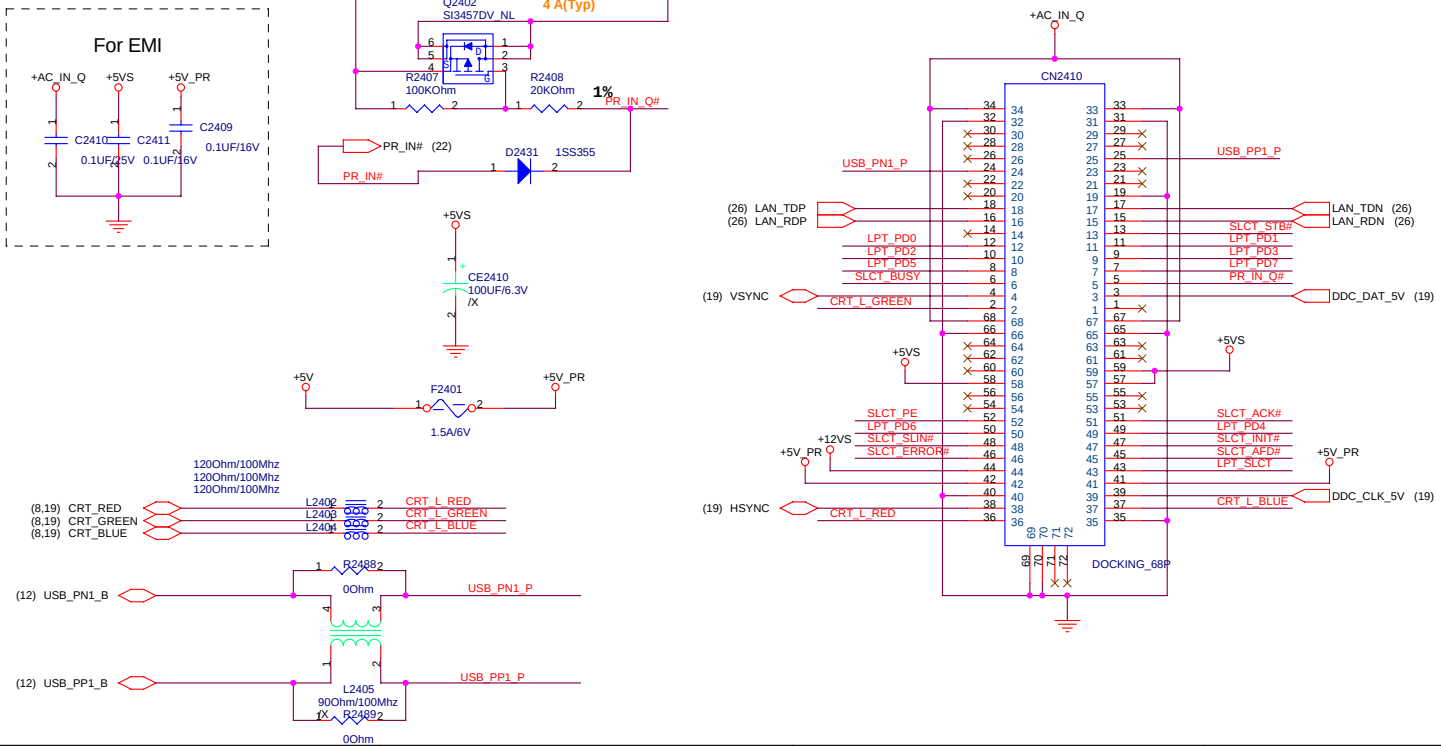
ISA ROM

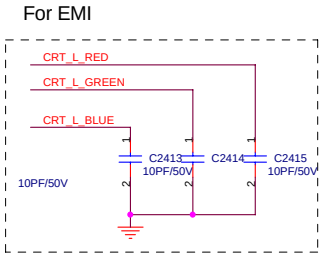
<OrgName>		Title : ISA ROM & SPI ROM	
		Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Thursday, April 06, 2006		Sheet 23 of 45	

Super I/O

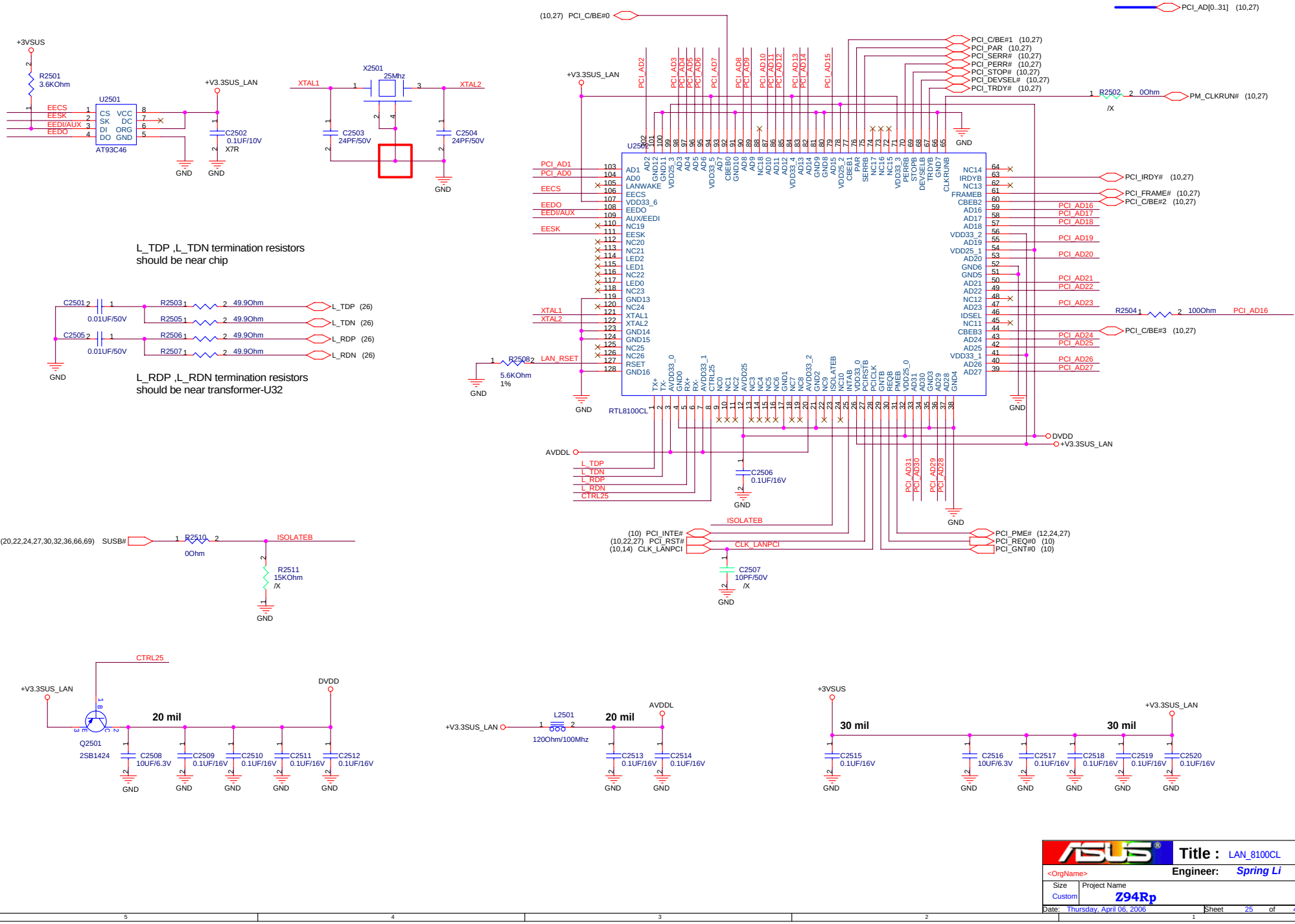






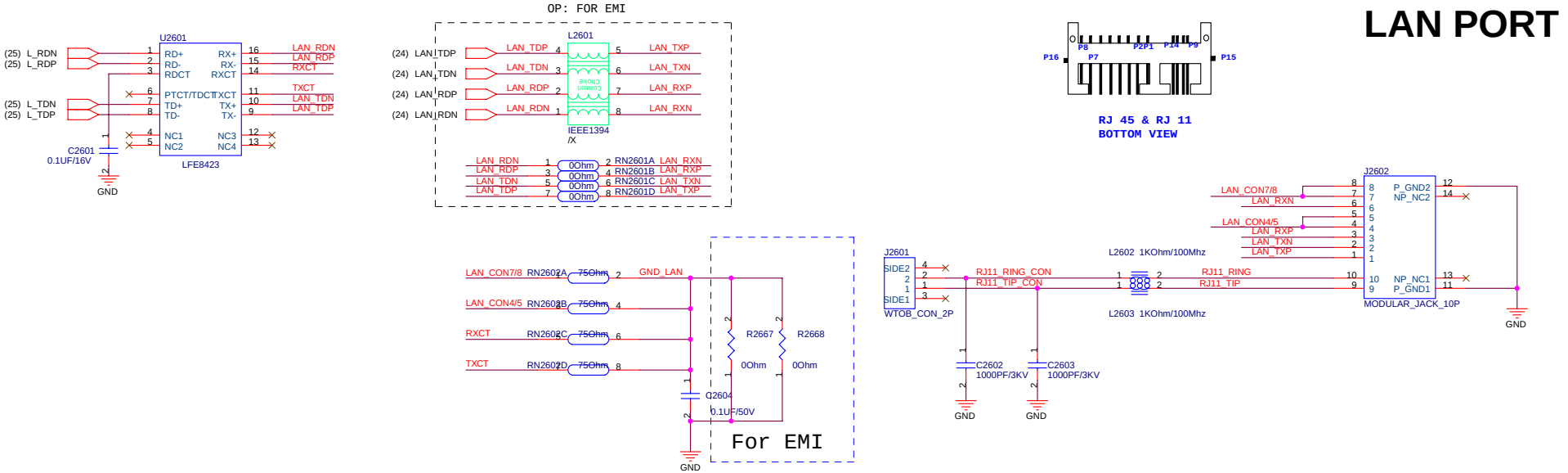


ASUS	Title : Blank	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 24 of 45	

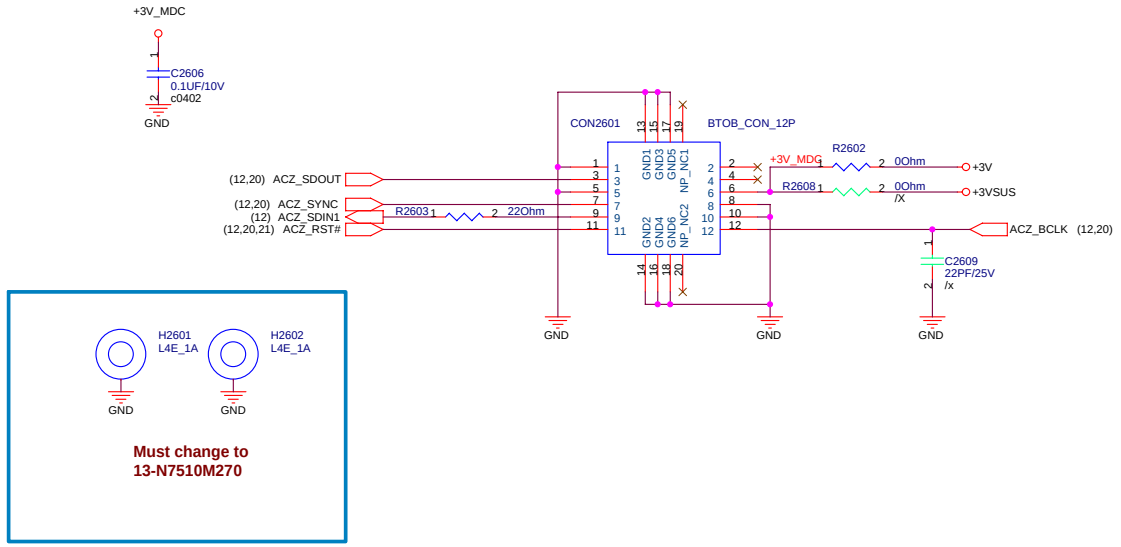


ASUS	Title : LAN_8100CL	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 25 of 45	

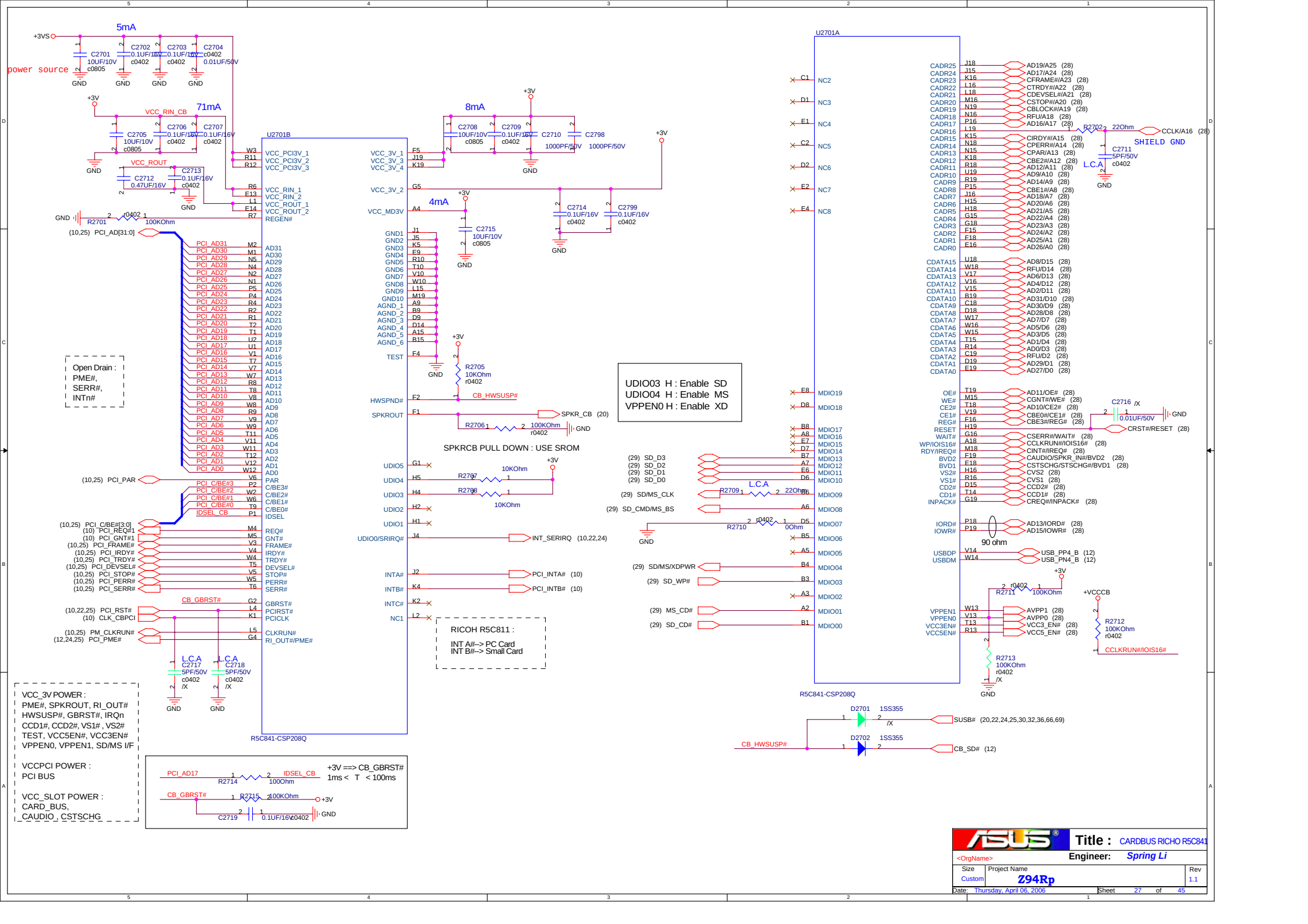
LAN PORT



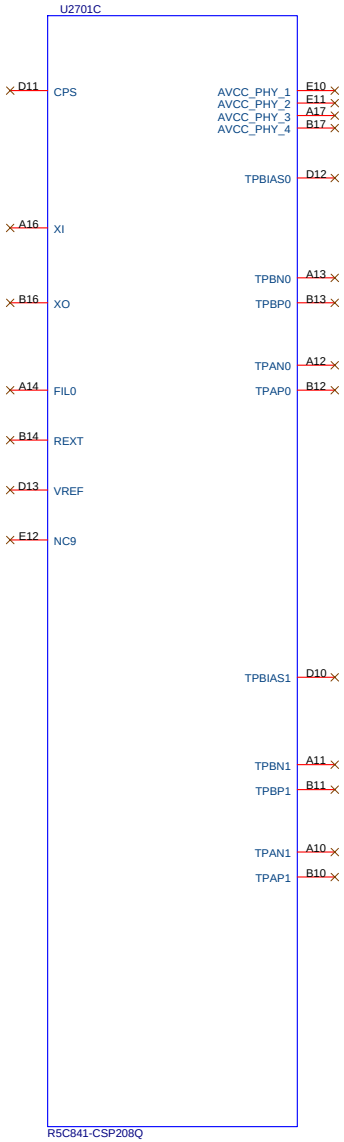
MDC

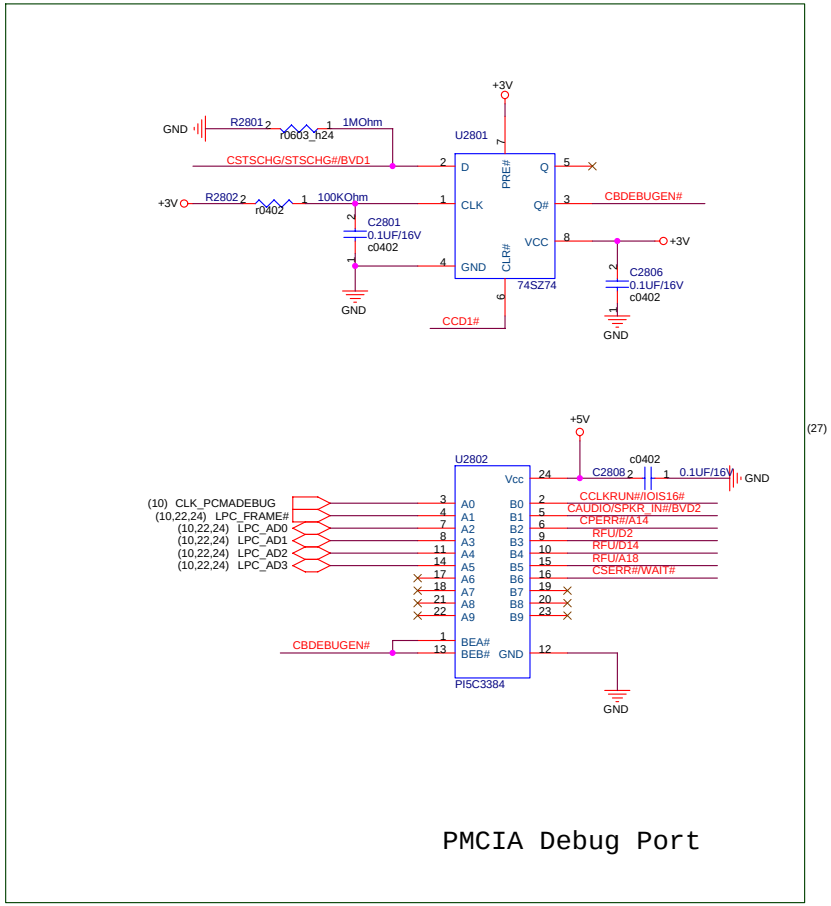


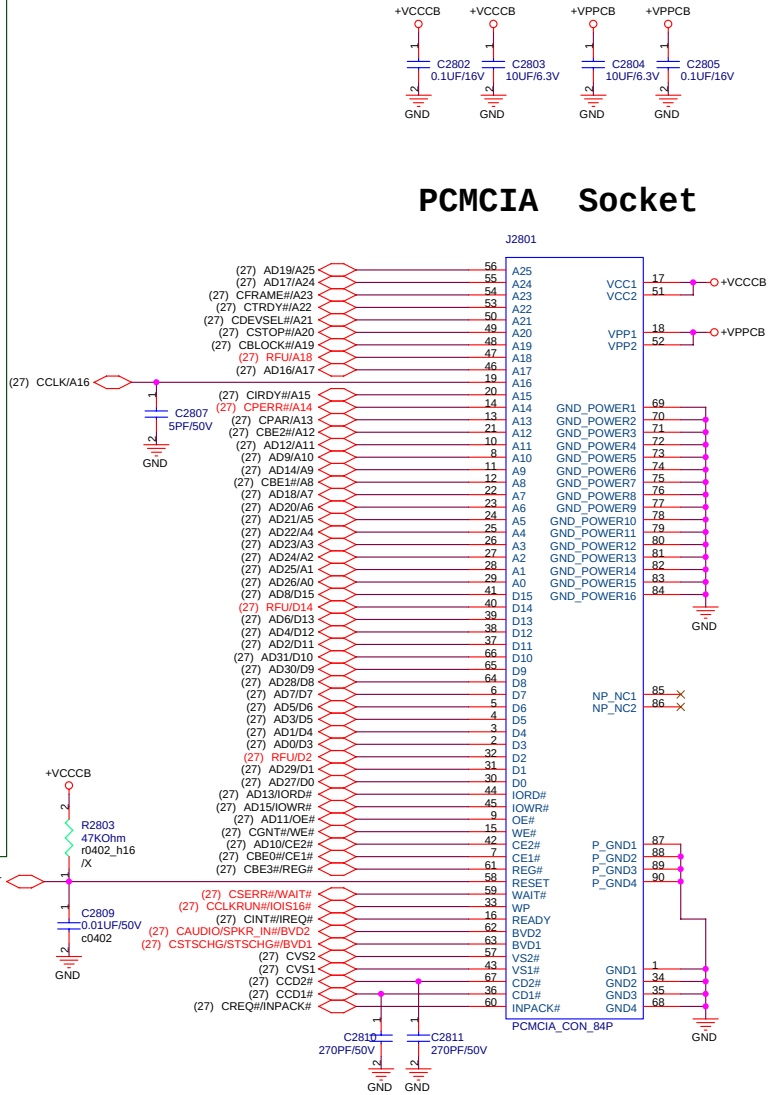
ASUS	Title :	RJ11+45 & MDC
<OrgName>	Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 26 of 45	

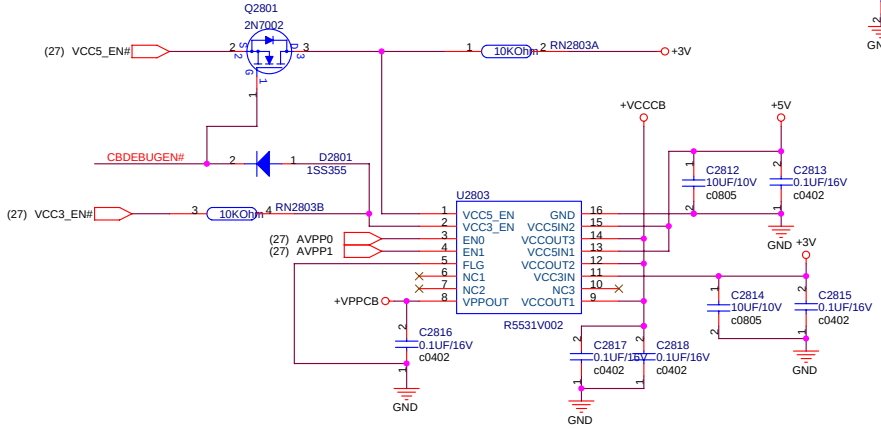


Title :	CARDBUS RICHO R5C841
<OrgName>	Engineer: Spring Li
Size: Custom	Project Name: Z94Rp
Rev: 1.1	
Date: Thursday, April 06, 2006	Sheet 27 of 45



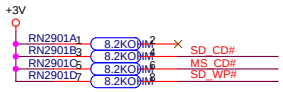






CCD1# CCD2#
L L 16bit
OTHER 32bit

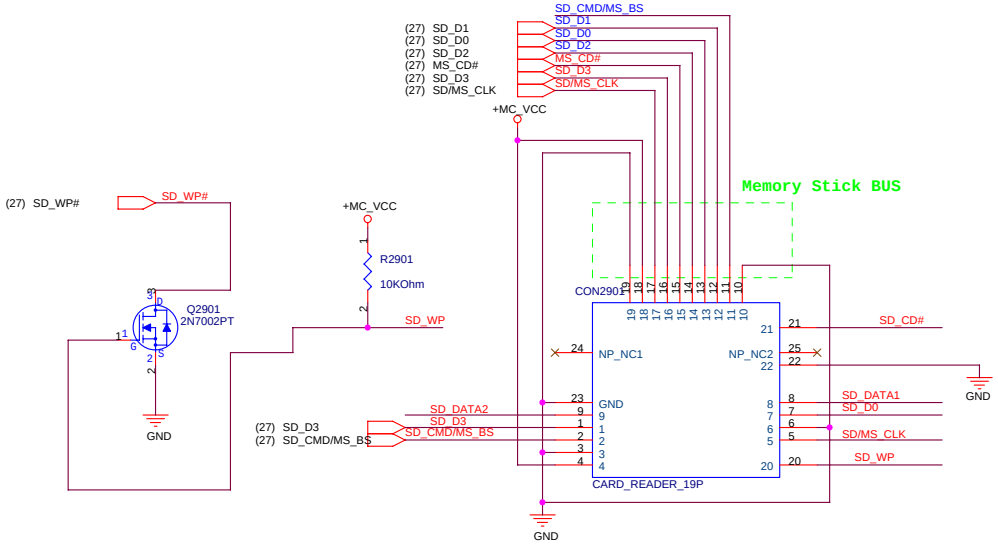
<OrgName>	Title : PCMCIA SOCKET	
	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 28 of 45	

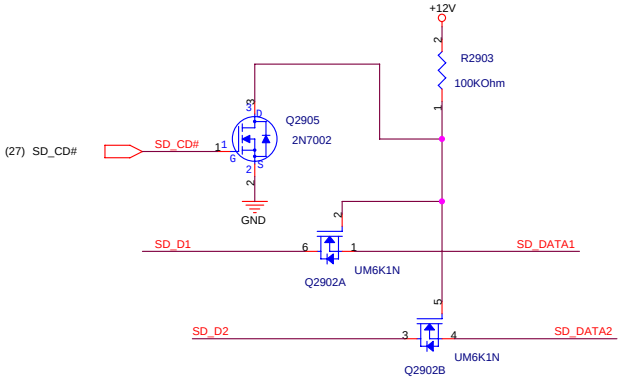


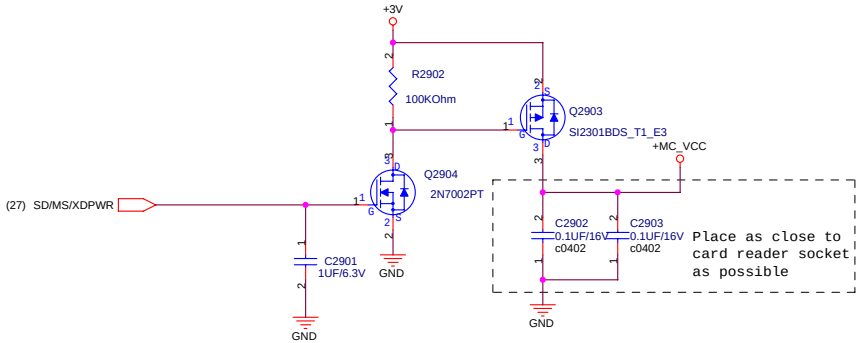
Memory Card Detect

MS_CD#	SD_CD#	
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

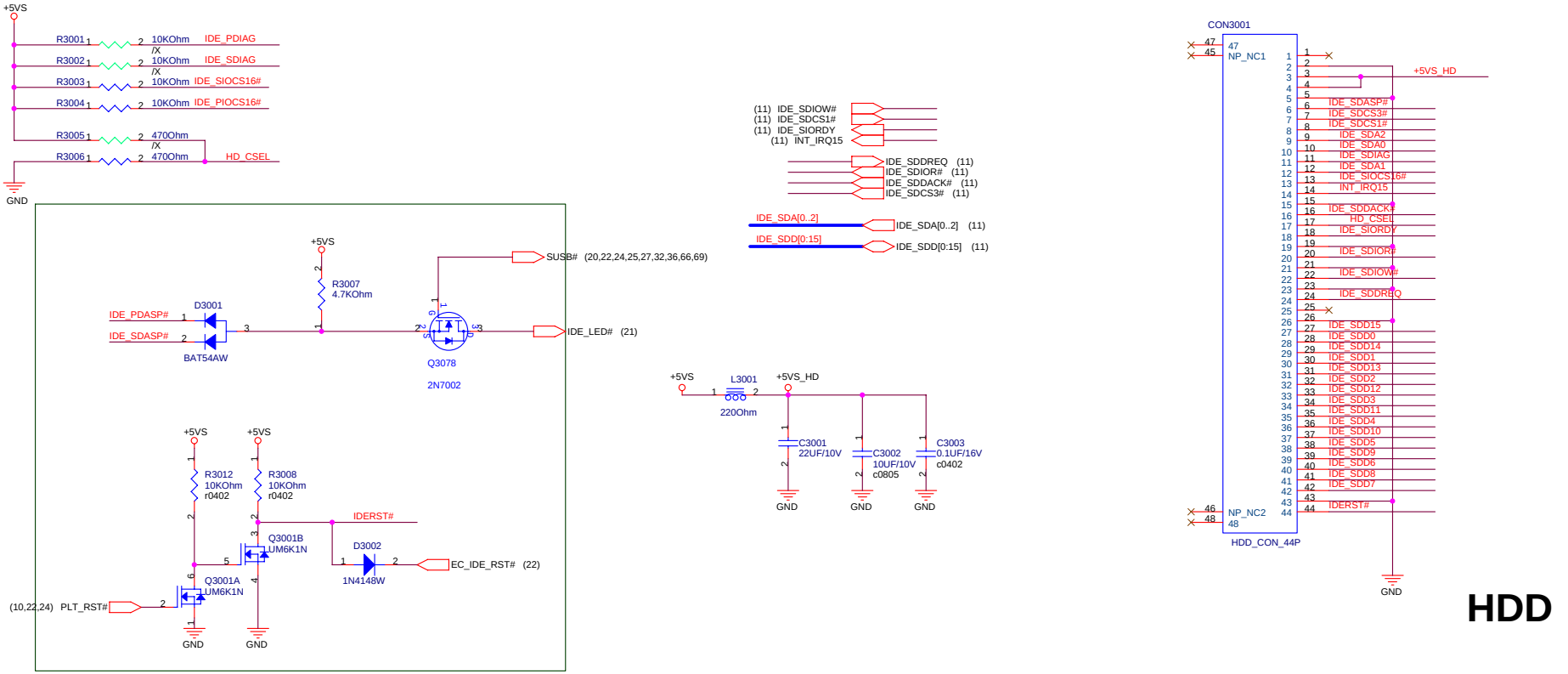
MC_CD# : Memory Card Detect



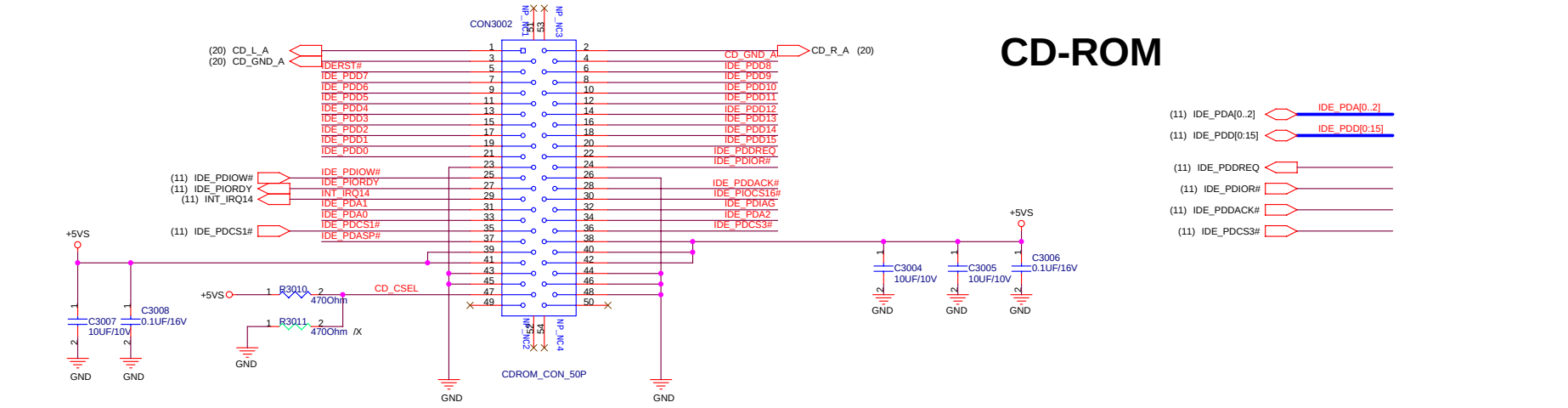




ASUS	Title : 4 IN 1 CON	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 29 of 45	



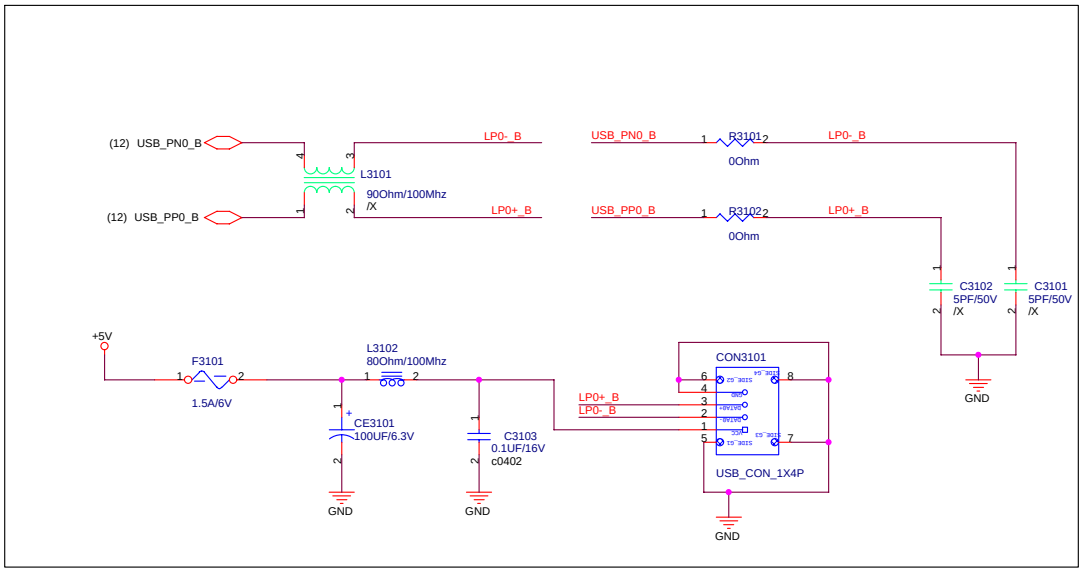
HDD

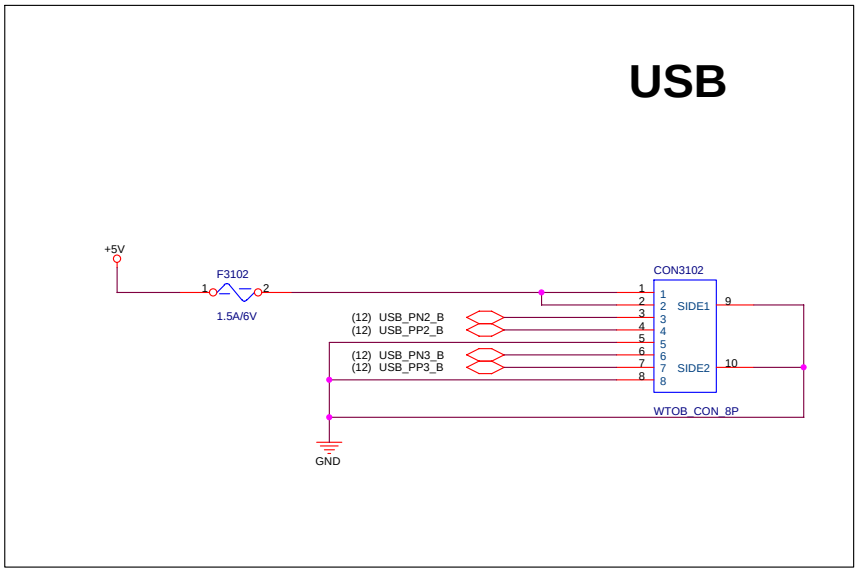


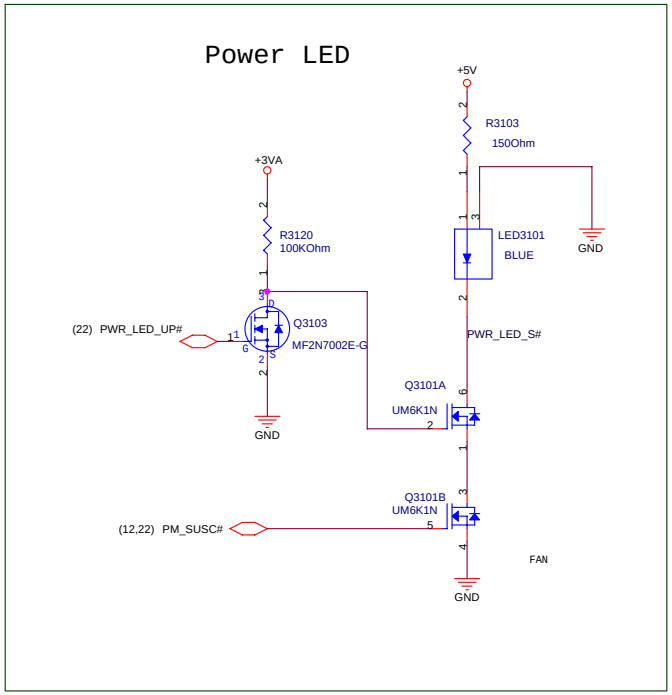
CD-ROM

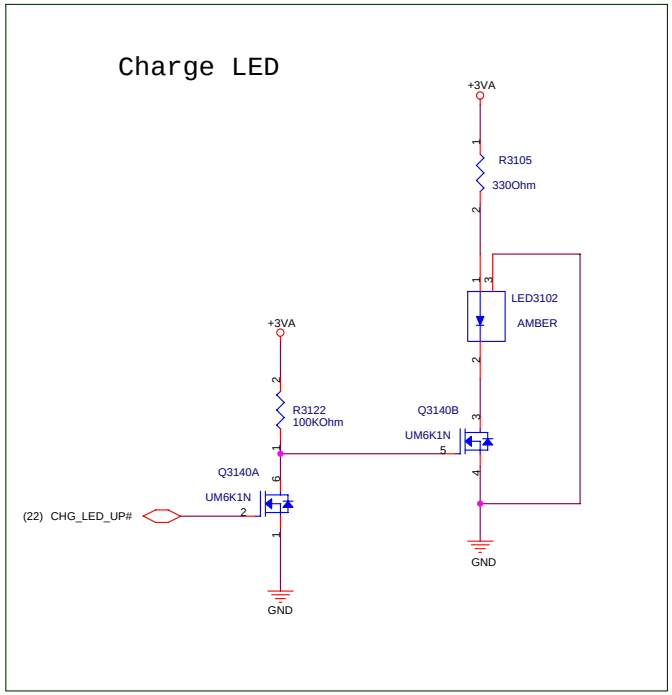
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master

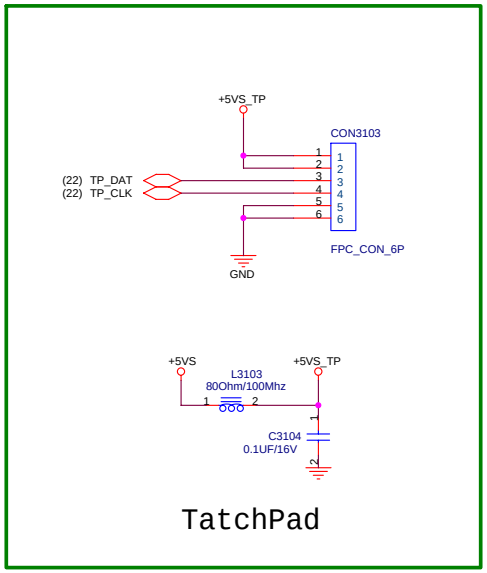
ASUS	Title : HDD & CD-ROM	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 30 of 45	



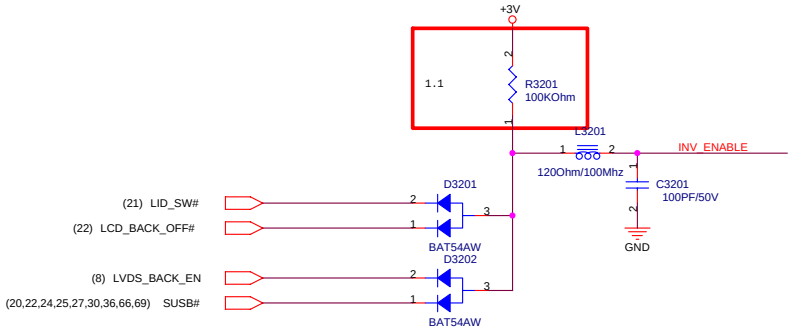




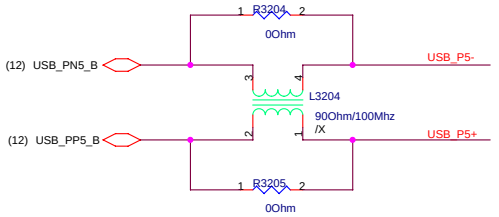


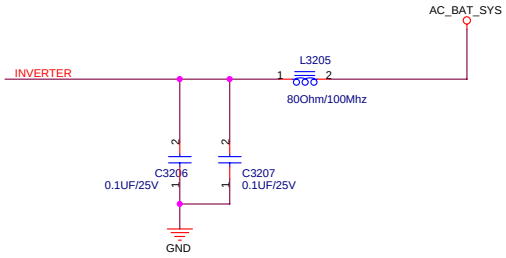


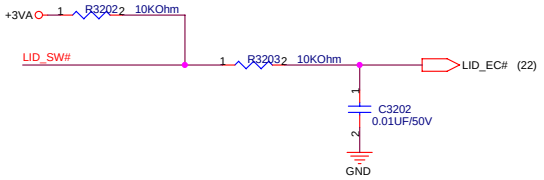
ASUS	Title : USB / LED / TP	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 31 of 45	

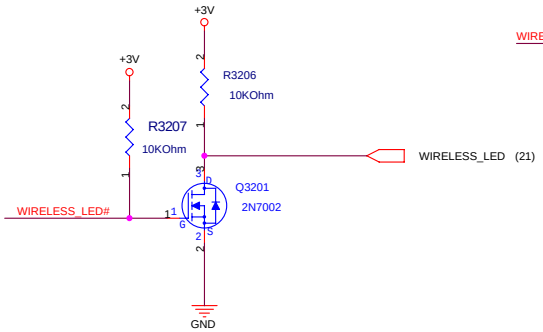


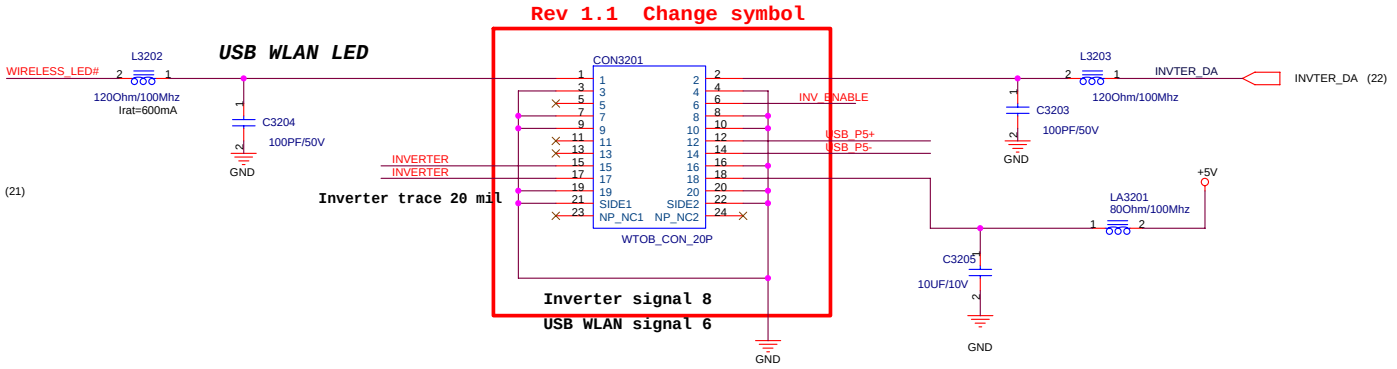
USB WIRESSLEE LAN



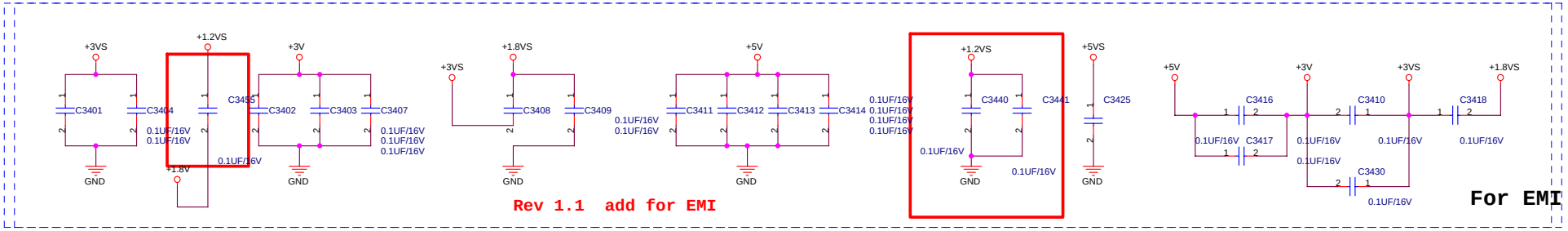




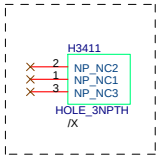




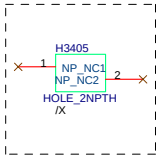
ASUS	Title : FUNCTION KEY & BT	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 32 of 45	



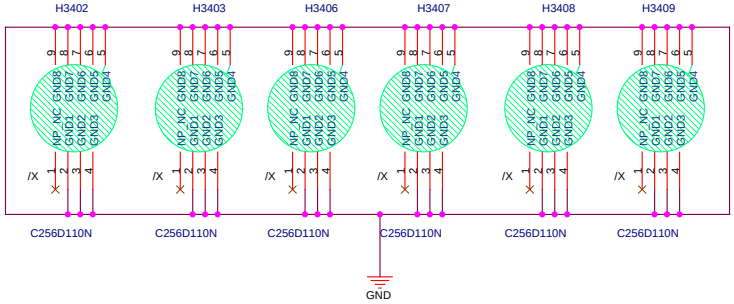
ODD



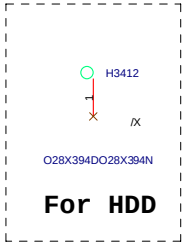
PAD Hole (2hole)--- E

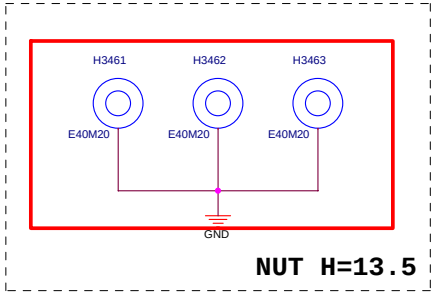


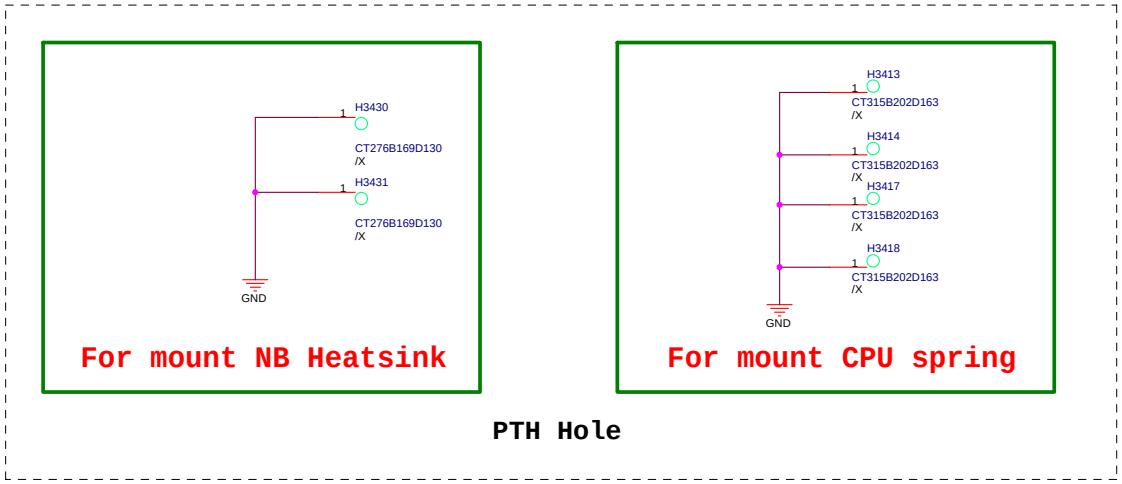
Hole no GND --- A

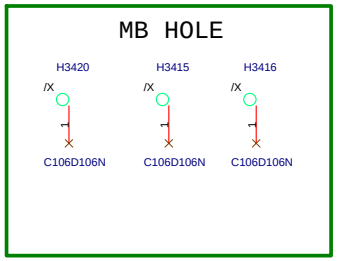


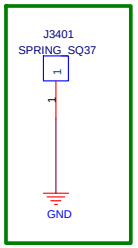
Oblong drill hole



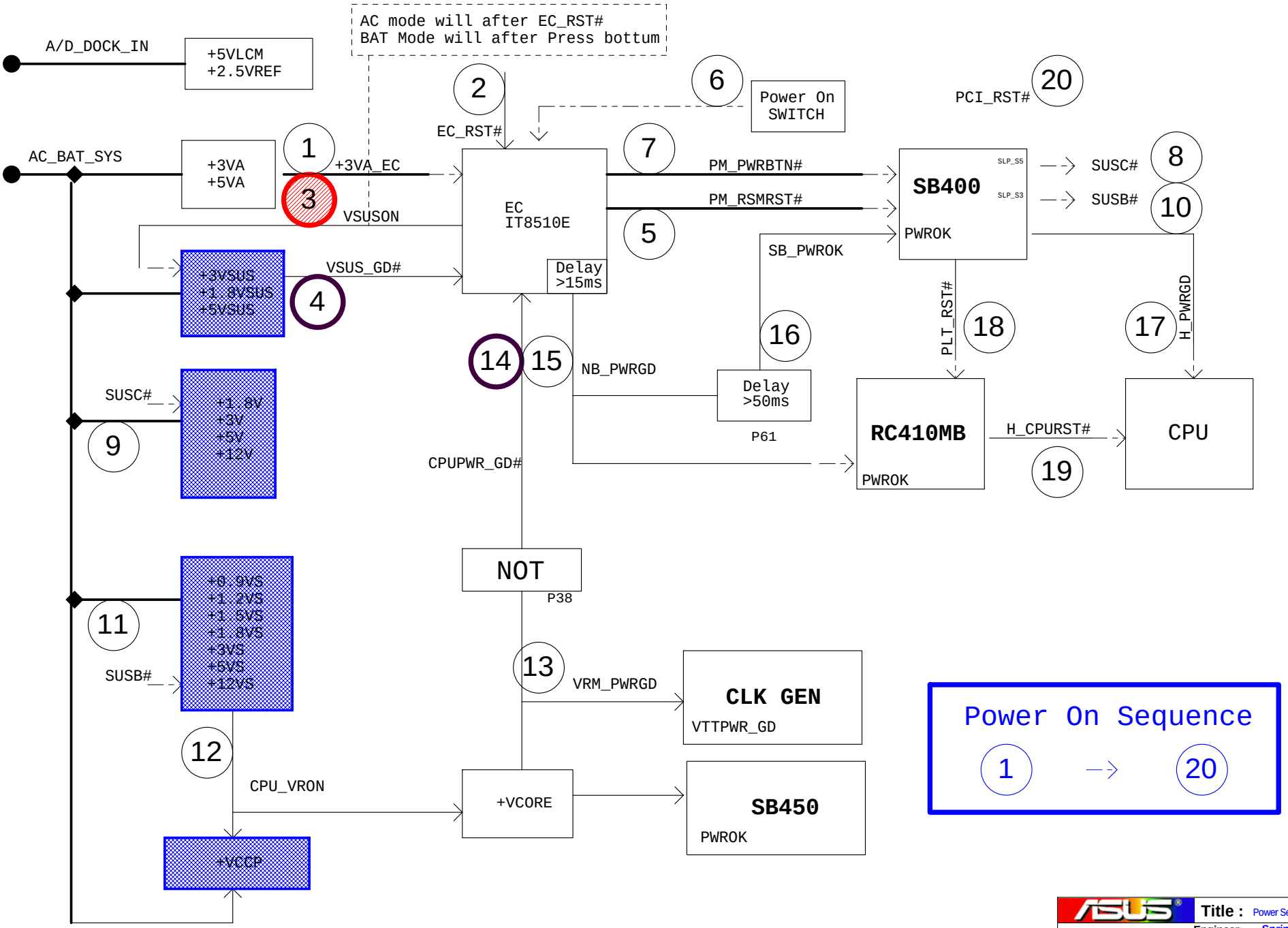








ASUS	Title : Hole	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 33 of 45	



Title :	Power Sequence		
<OrgName>	Engineer:	Spring Li	
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 34 of 45		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

ASUS

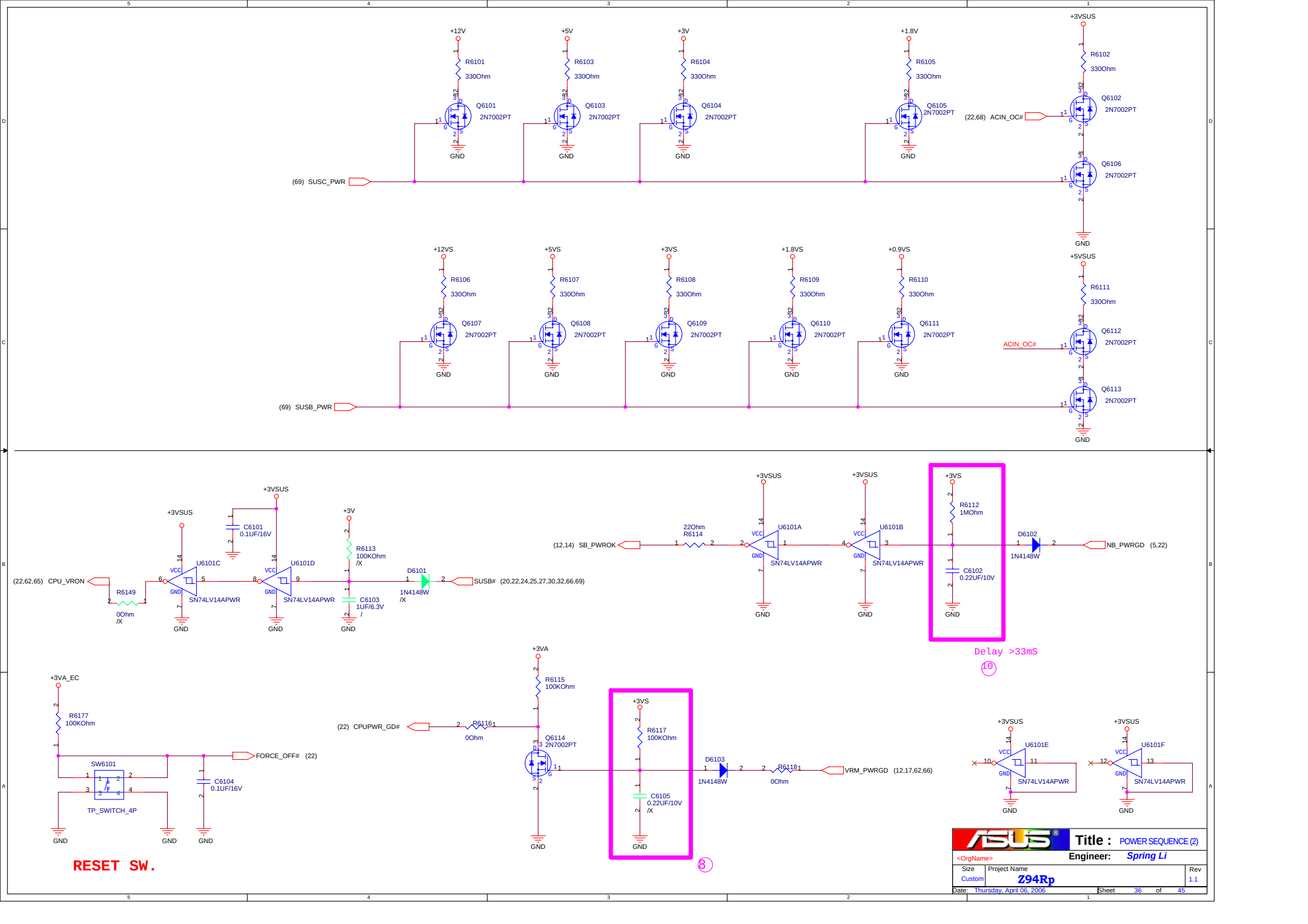
Title : SYSTEM RESOURCE

<OrgName>

Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

Date: Tuesday, April 04, 2006 Sheet 35 of 45



ASUS

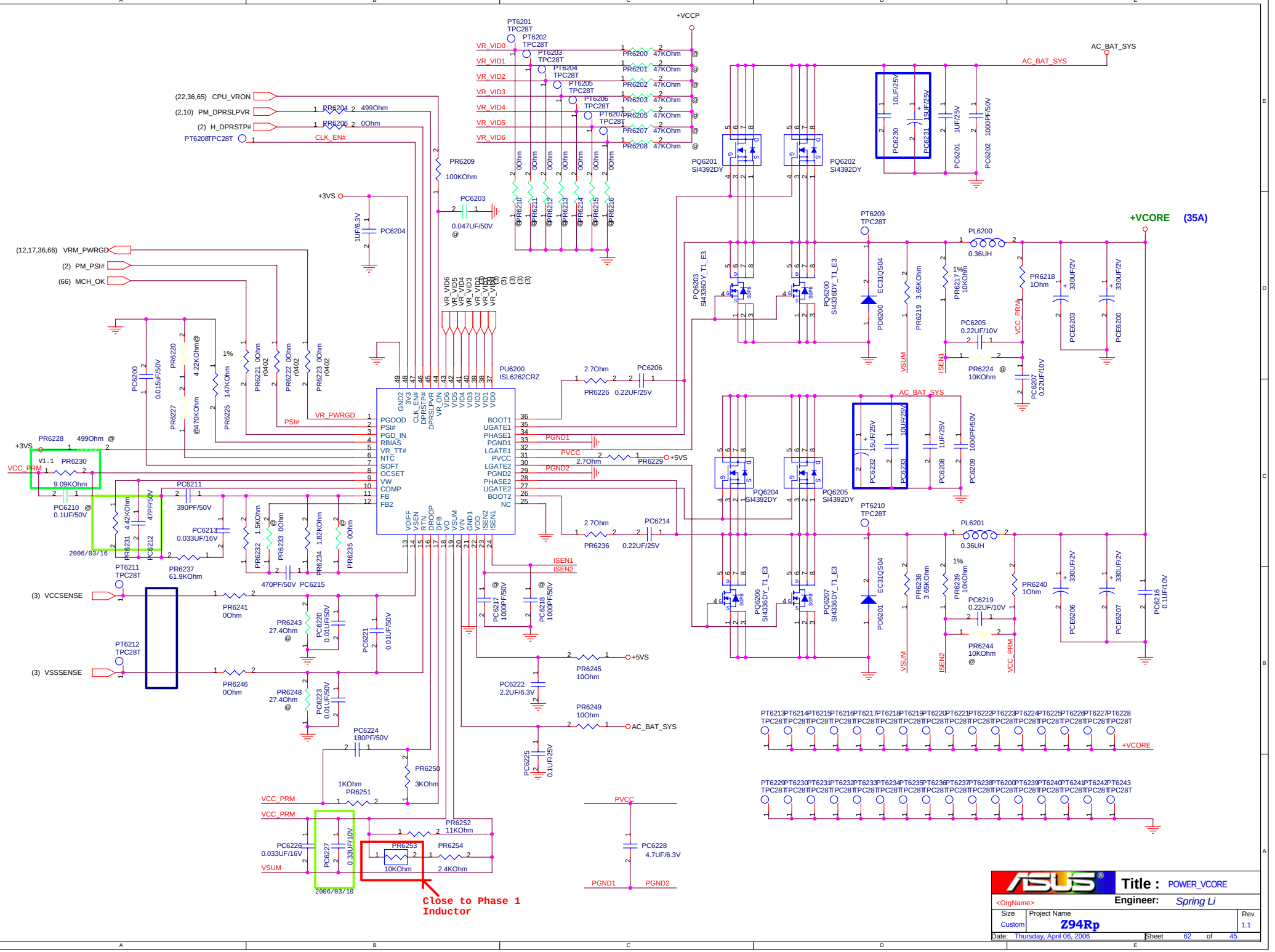
Title : POWER SEQUENCE (2)

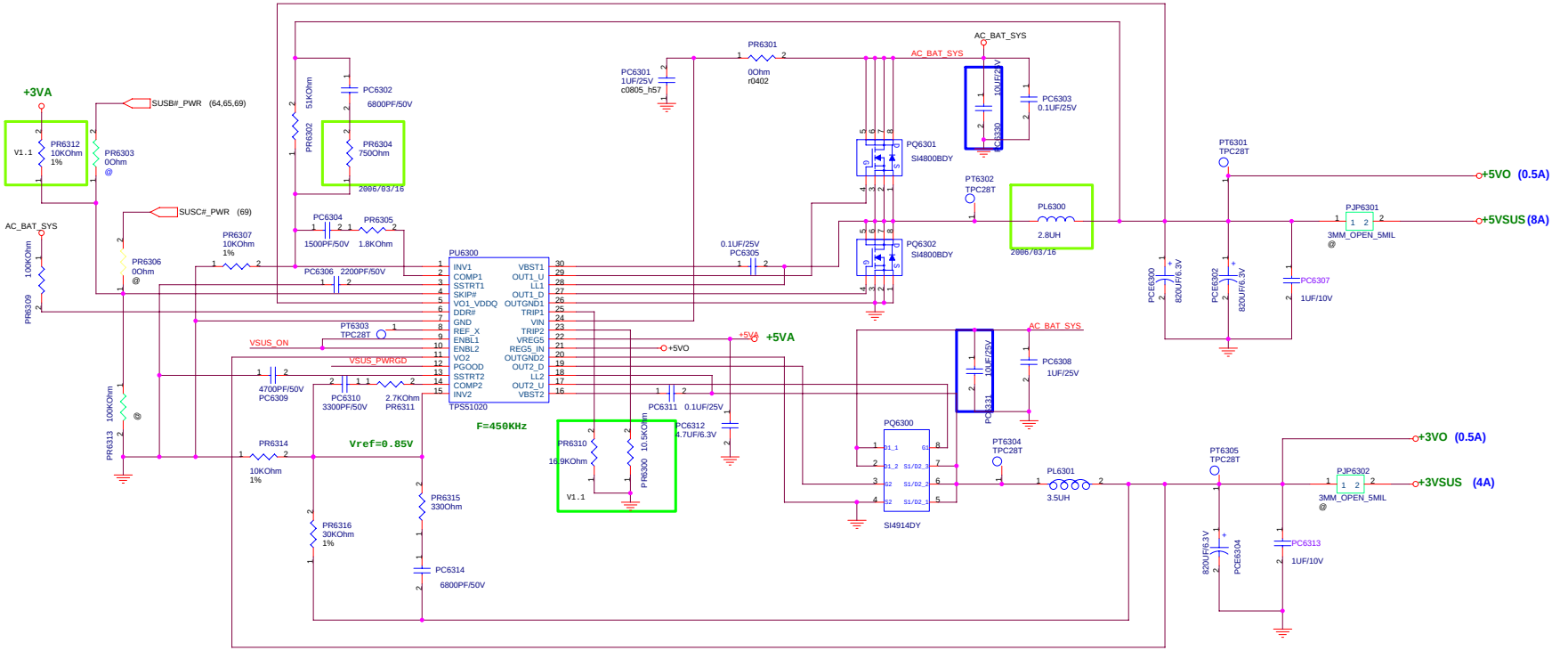
<OrgName>

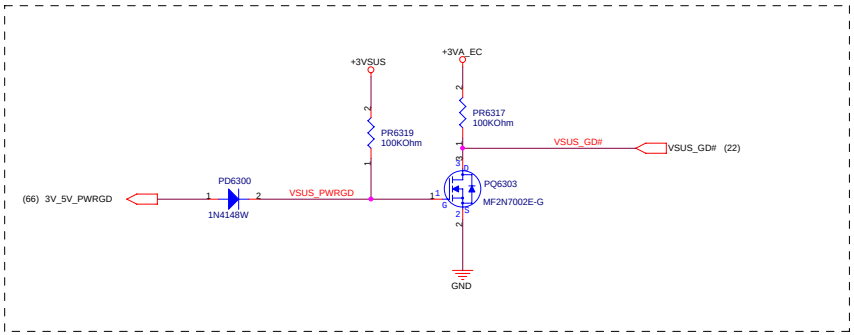
Engineer: Spring Li

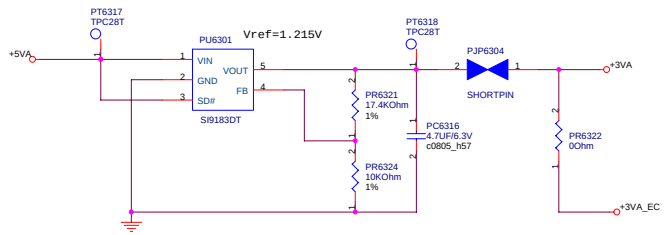
Size	Project Name	Rev
Custom	Z94Rp	1.1

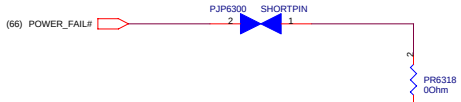
Date: Thursday, April 06, 2006 Sheet 36 of 45

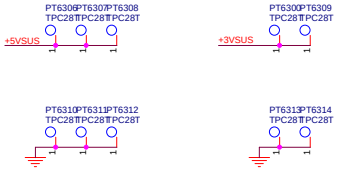

+VCCP
AC_BAT_SYS
+VCORE (35A)
PU6200 ISL6262CRZ
PQ6201 SI4392DY
PQ6202 SI4392DY
PQ6203 SI4336DY_T1_E3
PQ6200 SI4336DY_T1_E3
PQ6204 SI4392DY
PQ6205 SI4392DY
PQ6206 SI4336DY_T1_E3
PQ6207 SI4336DY_T1_E3
PD6200 EC31QS04
PD6201 EC31QS04
PL6200 0.36UH
PL6201 0.36UH
PT6209 TPC28T
PT6210 TPC28T
PT6211 TPC28T
PT6212 TPC28T
PT6213 PT6214 PT6215 PT6216 PT6217 PT6218 PT6219 PT6220 PT6221 PT6222 PT6223 PT6224 PT6225 PT6226 PT6227 PT6228 TPC28T
PT6229 PT6230 PT6231 PT6232 PT6233 PT6234 PT6235 PT6236 PT6237 PT6238 PT6200 PT6239 PT6240 PT6241 PT6242 PT6243 TPC28T
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
(22,36,65) CPU_VRON
(2,10) PM_DPRSLPVR
(2) H_DPRSTP#
PT6208TPC28T
CLK_EN#
(12,17,36,66) VRM_PWRGD
(2) PM_PSI#
(66) MCH_OK
VR_PWRGD
PSI#
PGND1
PGND2
PVCC
ISEN1
ISEN2
VSUM
VCC_PRM
(3) VCCSENSE
(3) VSSSENSE
Close to Phase 1 Inductor
2006/03/16
2006/03/10
Title : POWER_VCORE
Engineer: Spring Li
<OrgName>
Size Custom
Project Name Z94Rp
Rev 1.1
Date: Thursday, April 06, 2006
Sheet 62 of 45

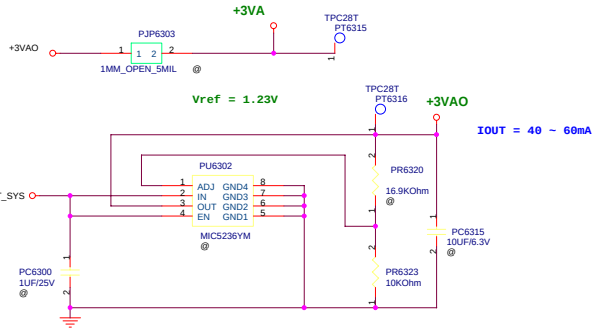




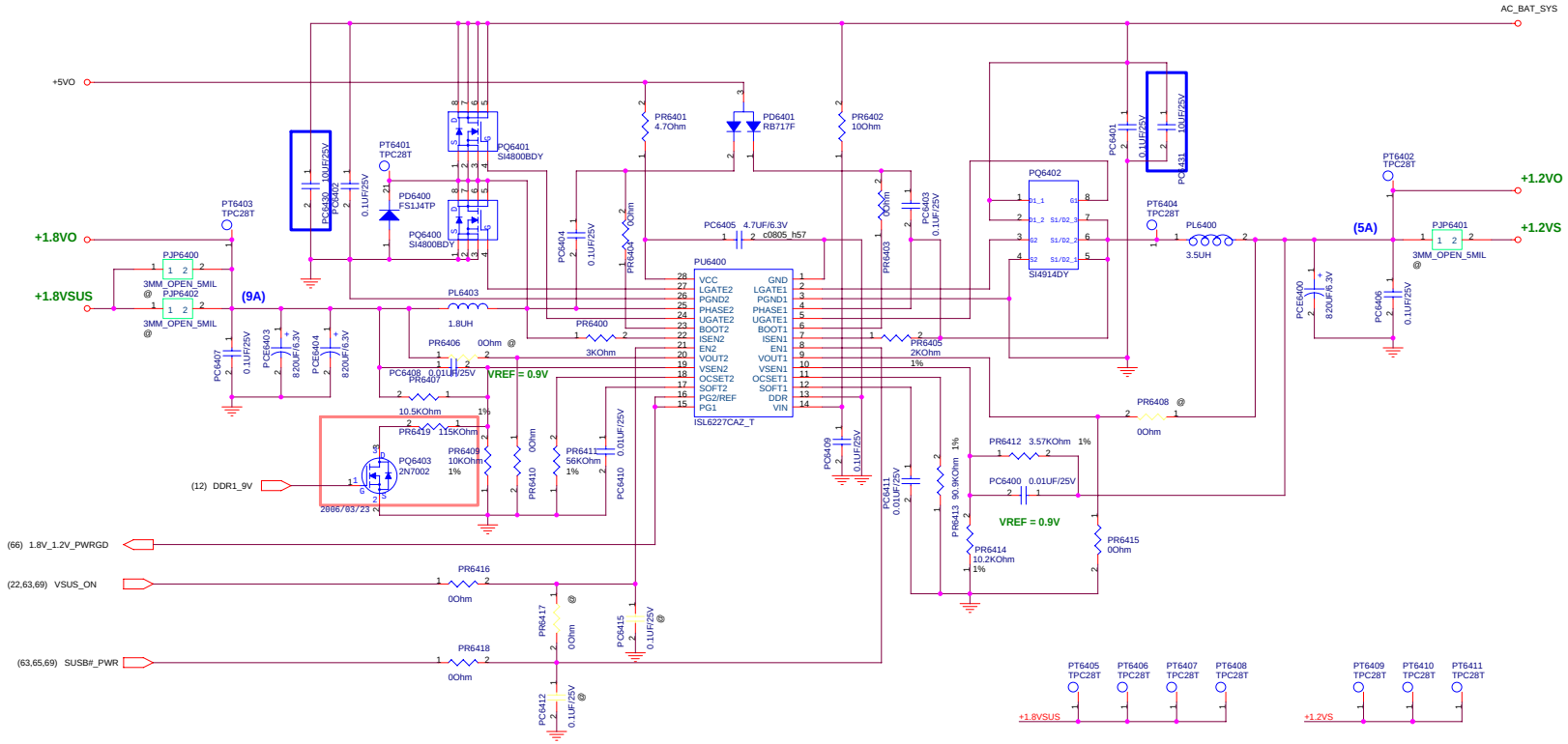


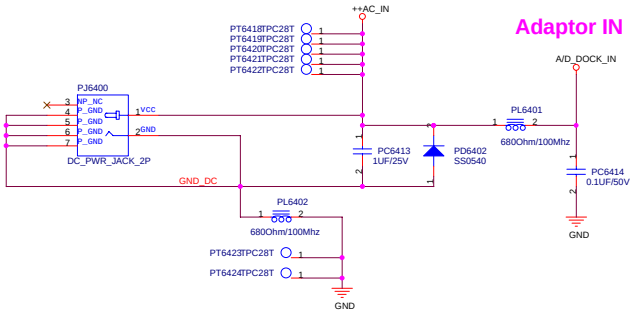




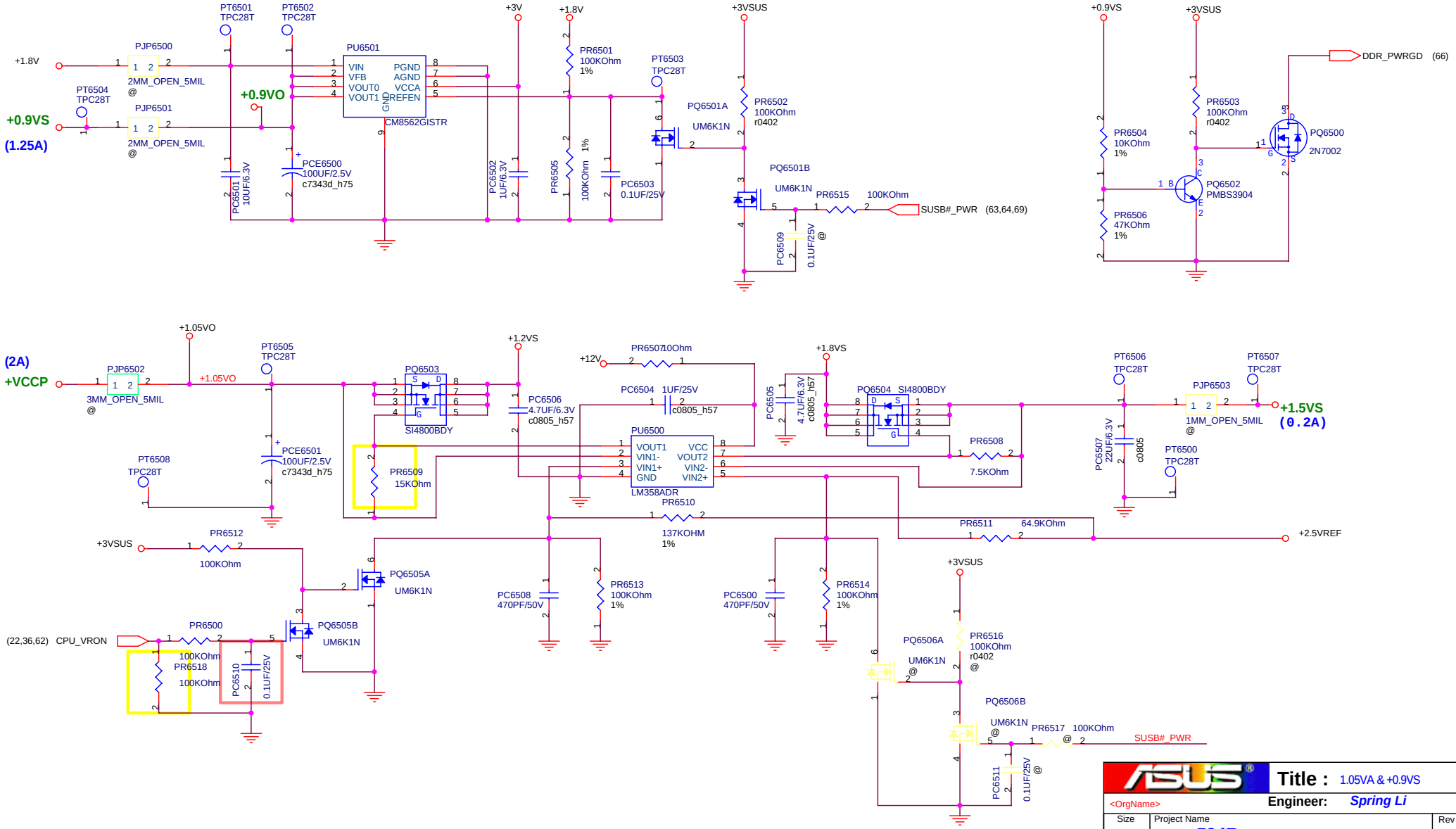


ASUS	Title :	SYSTEM_+5VA & +3VA
<OrgName>	Engineer:	Spring Li
Size: C	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 63 of 45	

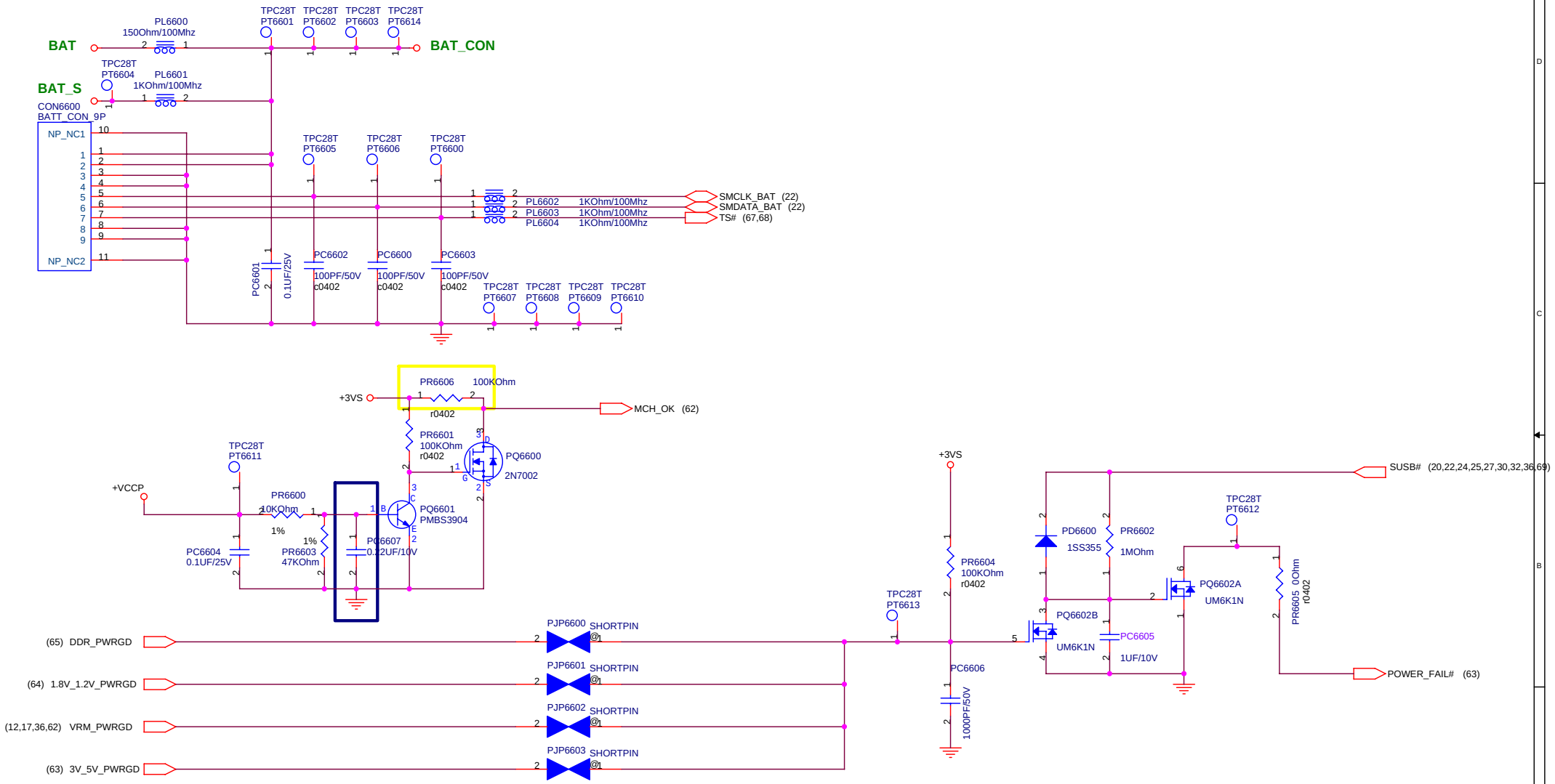




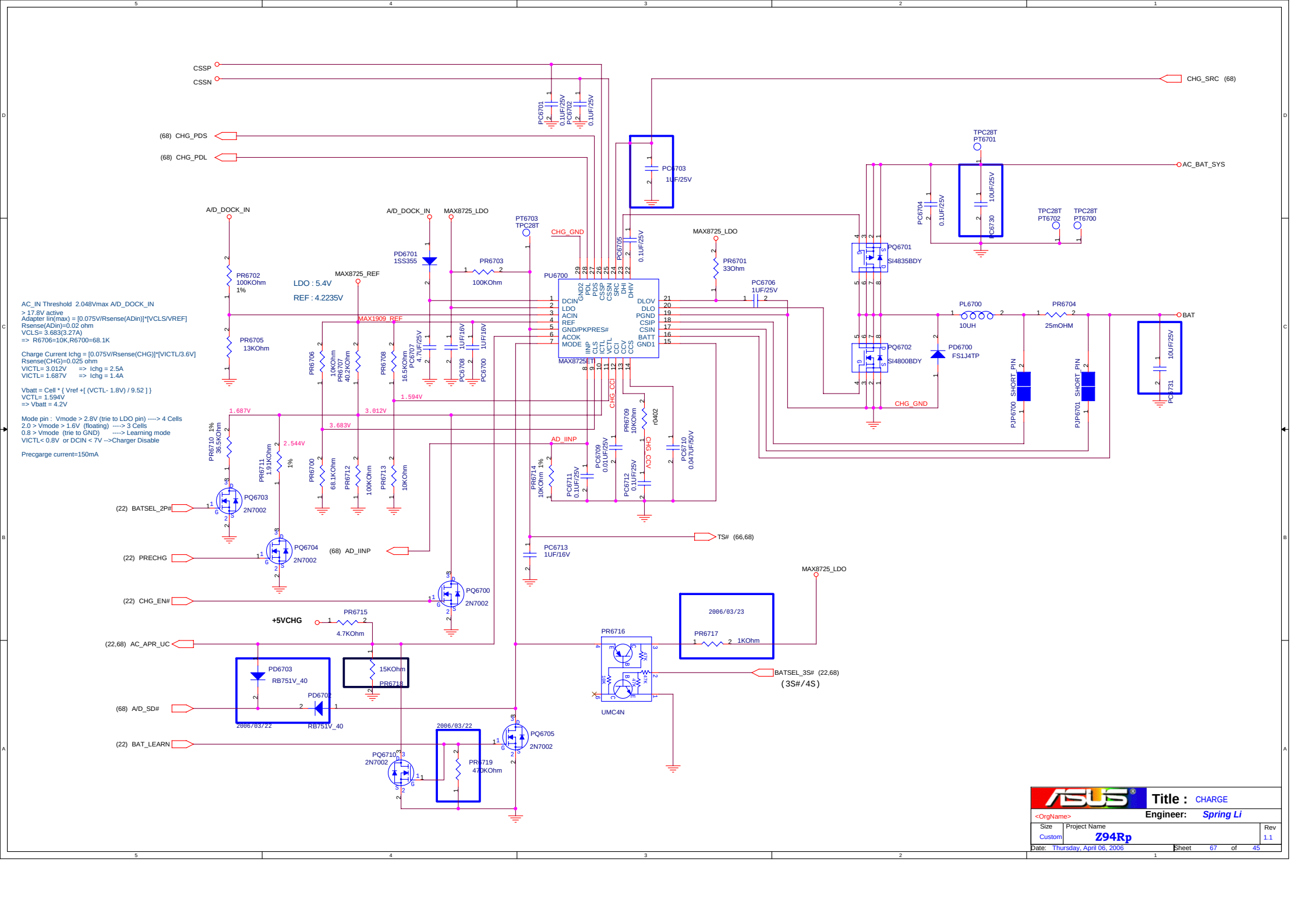
Title : 1.8V&1.2VS		
<OrgName>	Engineer: Spring Li	
Size: C	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 64 of 45	



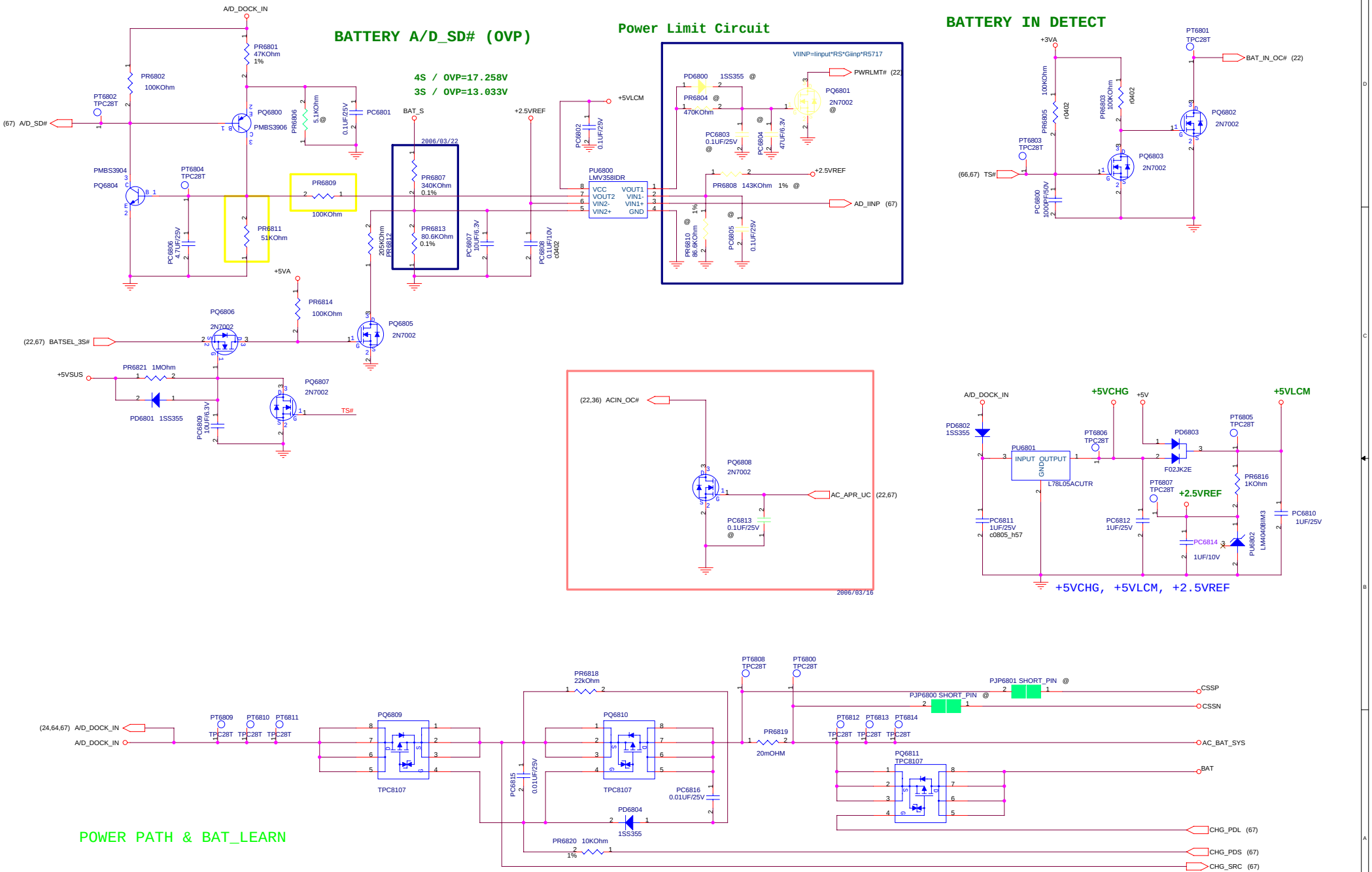
ASUS	Title : 1.05VA & +0.9VS	
<OrgName>	Engineer: Spring Li	
Size: B	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 65 of 45	



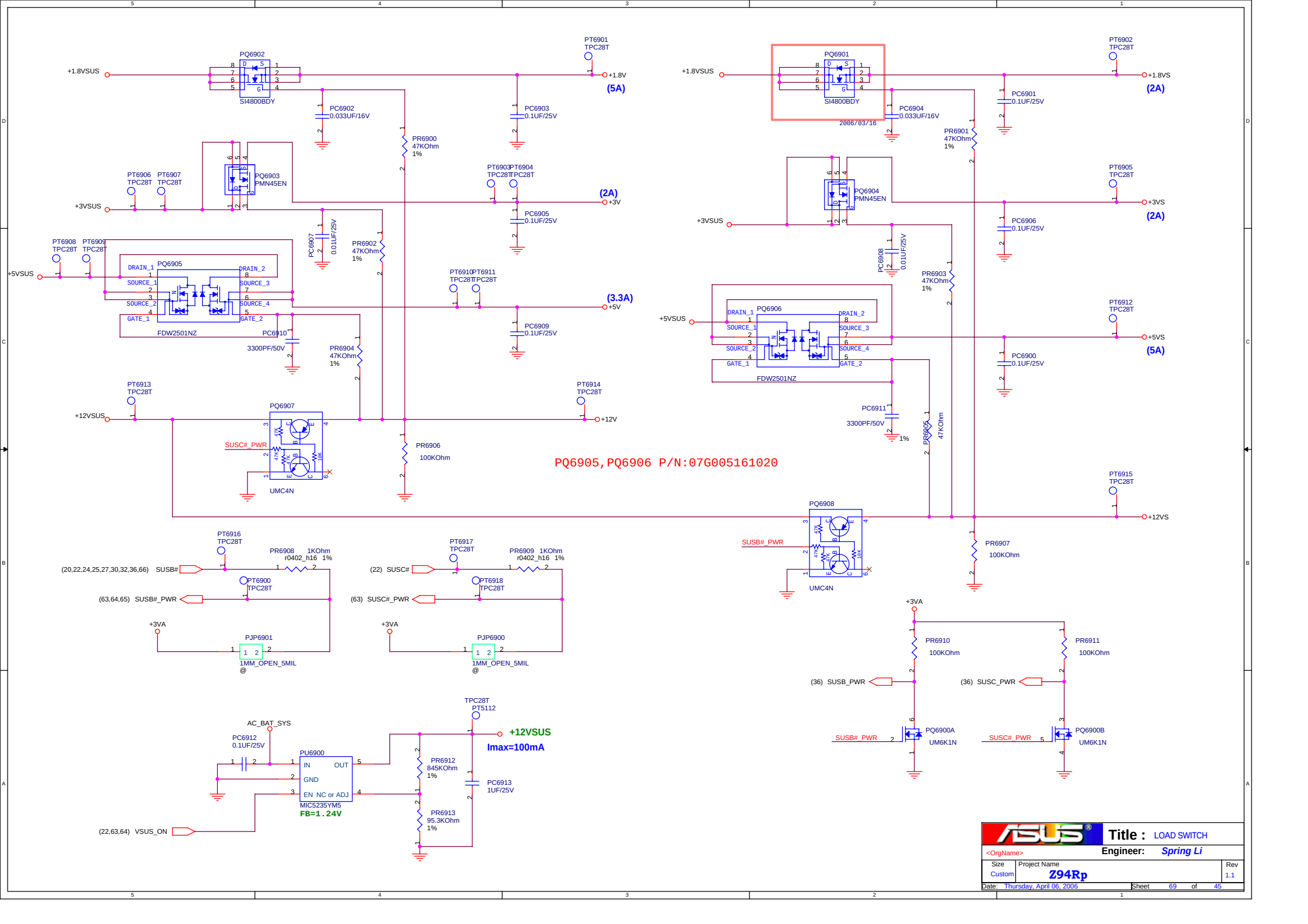
Title :	BAT CON/PWOK	
<OrgName>	Engineer:	Spring Li
Size: B	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 66 of 45	

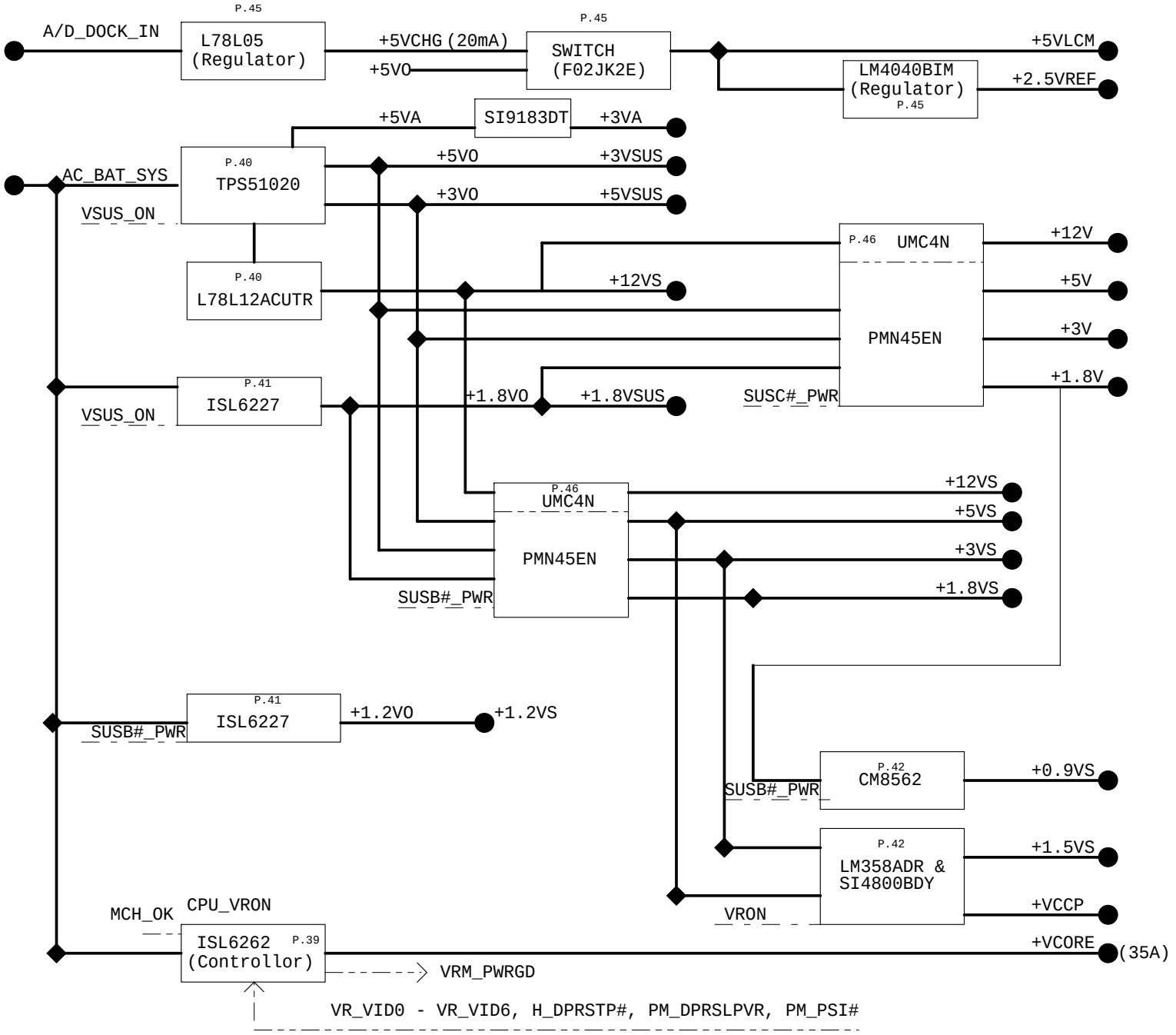


ASUS	Title : CHARGE	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 67 of 45	



ASUS	Title :	PROTECTION/SD#
<OrgName>	Engineer:	Spring Li
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Thursday, April 06, 2006	Sheet 68 of 45	


+1.8VSUS
PQ6902
SI4800BDY
PT6901 TPC28T
+1.8V
(5A)
PC6902 0.033UF/16V
PC6903 0.1UF/25V
PR6900 47KOhm 1%
PT6906 TPC28T
PT6907 TPC28T
PQ6903 PMN45EN
+3VSUS
PT6903 TPC28T
PT6904 TPC28T
(2A)
+3V
PC6905 0.1UF/25V
PC6907 0.01UF/25V
PR6902 47KOhm 1%
PT6908 TPC28T
PT6909 TPC28T
+5VSUS
PQ6905
DRAIN_1
DRAIN_2
SOURCE_1
SOURCE_3
SOURCE_2
SOURCE_4
GATE_1
GATE_2
FDW2501NZ
PC6910 3300PF/50V
PT6910 TPC28T
PT6911 TPC28T
(3.3A)
+5V
PC6909 0.1UF/25V
PR6904 47KOhm 1%
PT6913 TPC28T
+12VSUS
PQ6907
SUSC#_PWR
UMC4N
PR6906 100KOhm
PT6914 TPC28T
+12V
PQ6905,PQ6906 P/N:07G005161020
PQ6901
SI4800BDY
2006/03/16
PT6902 TPC28T
+1.8VS
(2A)
PC6901 0.1UF/25V
PC6904 0.033UF/16V
PR6901 47KOhm 1%
PQ6904 PMN45EN
PT6905 TPC28T
+3VS
(2A)
PC6906 0.1UF/25V
PC6908 0.01UF/25V
PR6903 47KOhm 1%
PQ6906
PT6912 TPC28T
+5VS
(5A)
PC6900 0.1UF/25V
PC6911 3300PF/50V
1%
PR6905 47KOhm
PT6915 TPC28T
+12VS
PQ6908
SUSB#_PWR
UMC4N
PR6907 100KOhm
PT6916 TPC28T
PR6908 1KOhm r0402_h16 1%
(20,22,24,25,27,30,32,36,66) SUSB#
PT6900 TPC28T
(63,64,65) SUSB#_PWR
+3VA
PJP6901
1MM_OPEN_5MIL
@
PT6917 TPC28T
PR6909 1KOhm r0402_h16 1%
(22) SUSC#
PT6918 TPC28T
(63) SUSC#_PWR
+3VA
PJP6900
1MM_OPEN_5MIL
@
+3VA
PR6910 100KOhm
PR6911 100KOhm
(36) SUSB_PWR
(36) SUSC_PWR
SUSB#_PWR
PQ6900A UM6K1N
SUSC#_PWR
PQ6900B UM6K1N
TPC28T
PT5112
+12VSUS
Imax=100mA
AC_BAT_SYS
PC6912 0.1UF/25V
PU6900
IN
OUT
GND
EN NC or ADJ
MIC5235YM5
FB=1.24V
PR6912 845KOhm 1%
PC6913 1UF/25V
PR6913 95.3KOhm 1%
(22,63,64) VSUS_ON
Title : LOAD SWITCH
<OrgName>
Engineer: Spring Li
Size Custom
Project Name Z94Rp
Rev 1.1
Date: Thursday, April 06, 2006
Sheet 69 of 45



<OrgName>	Title : POWER BLOCK DIAGRAM	
	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: Tuesday, April 04, 2006	Sheet 70 of 45	