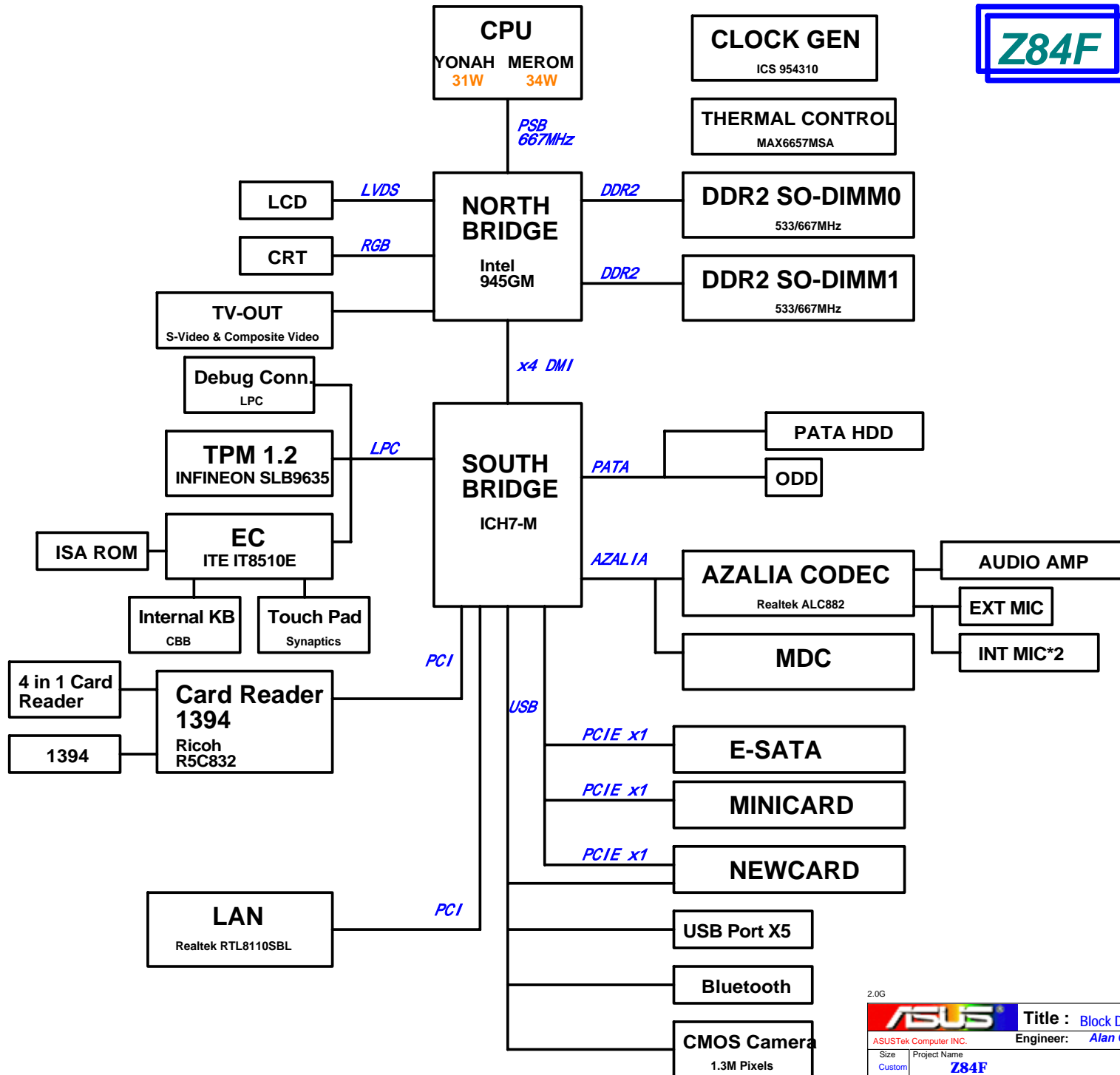


- 01_Block Diagram
- 02_System Setting
- 03_CPU-YONAH(HOST)
- 04_CPU-YONAH(PWR)
- 05_NB-945GM(HOST)
- 06_NB-945GM(DMI & CFG)
- 07_NB-945GM(GRAPHIC)
- 08_NB-945GM(DDR2)
- 09_NB-945GM(PWR)
- 10_NB-945GM(PWR2)
- 11_NB-945GM(GND)
- 12_SB-ICH7M(1)
- 13_SB-ICH7M(2)
- 14_SB-ICH7M(3)
- 15_SB-ICH7M(PWR)
- 16_DDR2 SO-DIMM0
- 17_DDR2 SO-DIMM1
- 18_DDR2 TERMINATION
- 19_CRT
- 20_LVDS & INVERTER CONNECTOR
- 21_TV OUT CONN
- 22_THER SENSOR & FAN
- 23_CLOCK GEN-ICS954310
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- 26_LAN-RTL8110SBL
- 27_MDC&RJ45&RJ11
- 28_MINI CARD
- 29_CARD1394-R5C832(1)
- 30_CARD1394-R5C832(2)
- 31_4 in 1 CARD READER
- 32_NEWCARD
- 33_CODEC-ALC882
- 34_AUDIO AMP & JCAK
- 35_EC-IT8510E
- 36_Touch Pad & KB
- 37_USB CONN
- 38_ISA ROM
- 39_LED
- 40_DC & BAT IN
- 41_Debug CONN.
- 42_SATA-HDD & ODD & E-SATA
- 43_SREW HOLE
- 44_TPM
- 45_BT
- 46_POWER_FLOWCHART
- 47_POWER_CHARGER
- 48_POWER_SYSTEM_+3VO & +5VO
- 49_POWER_VCORE
- 50_POWER_I/O_DDR & VTT
- 51_POWER_I/O_1.5VS & 1.15VS
- 52_POWER_I/O_+3VAO & +2.5VS
- 53_POWER_LOAD SWITCH
- 54_POWER_GOOD_DETECTER
- 55_POWER_SIGNAL
- 56_History
- 57_Power Sequence



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSV#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	R11#/WUI0/GPD0	SUSB#	I
29	R12#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PLT_RST#	I
31	ECSC#GPD3	EXT_SC#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCL_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCL_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCL_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCL_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCL_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCL_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCL_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

2.0G

		Title : <Title>	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size Custom	Project Name Z84F	Rev 2.00G	
Date: Friday, April 07, 2006	Sheet 2	of 57	

RCOMP

For Calibrating the FSB I/O Buffer



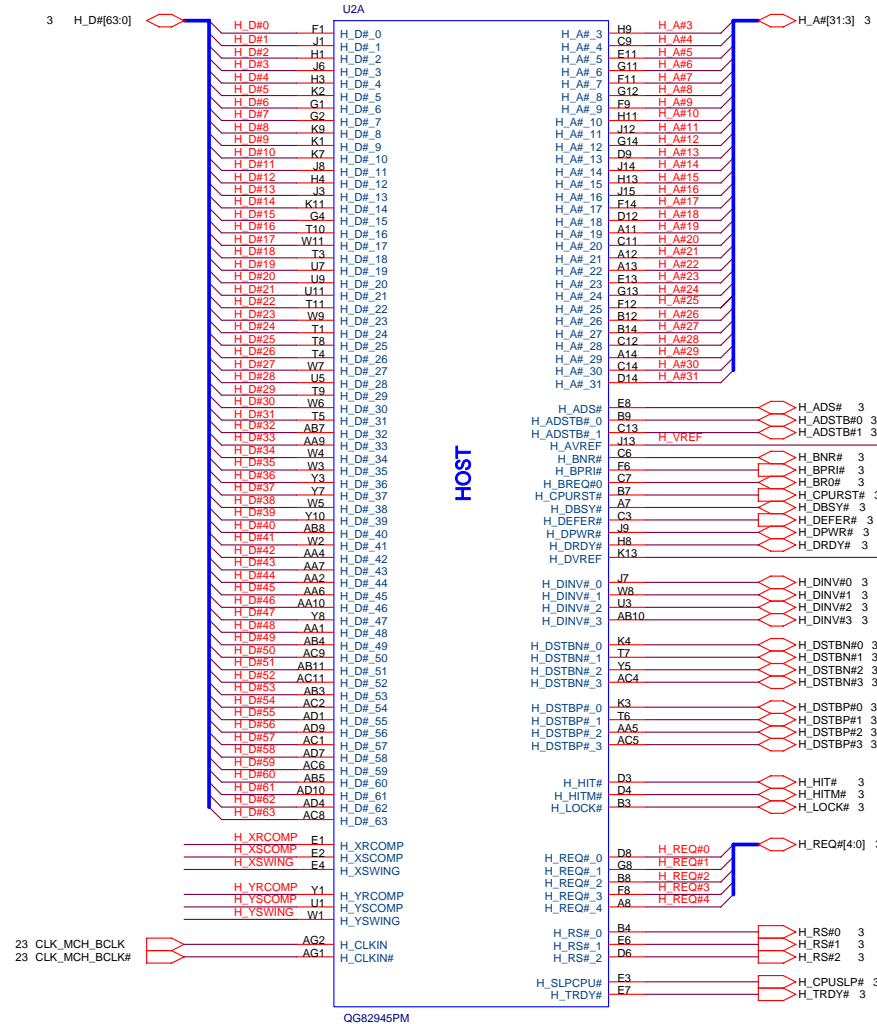
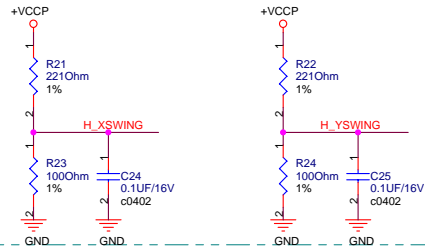
SCOMP

For Slew Rate Compensation on the FSB

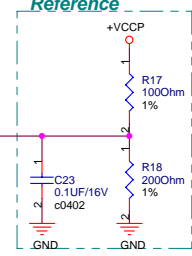


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



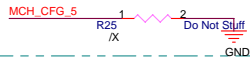
AGTL+ I/O Voltage Reference



GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

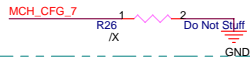


CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

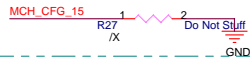
CFG7 : CPU Strap

0 = DT/Transportable CPU
1 = Mobile CPU (D)



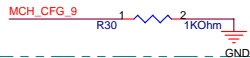
CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)



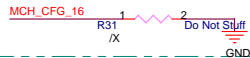
CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



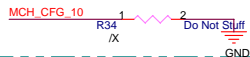
CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



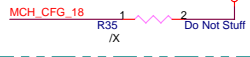
CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)



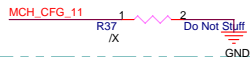
CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V



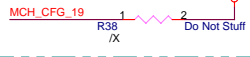
CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)



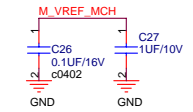
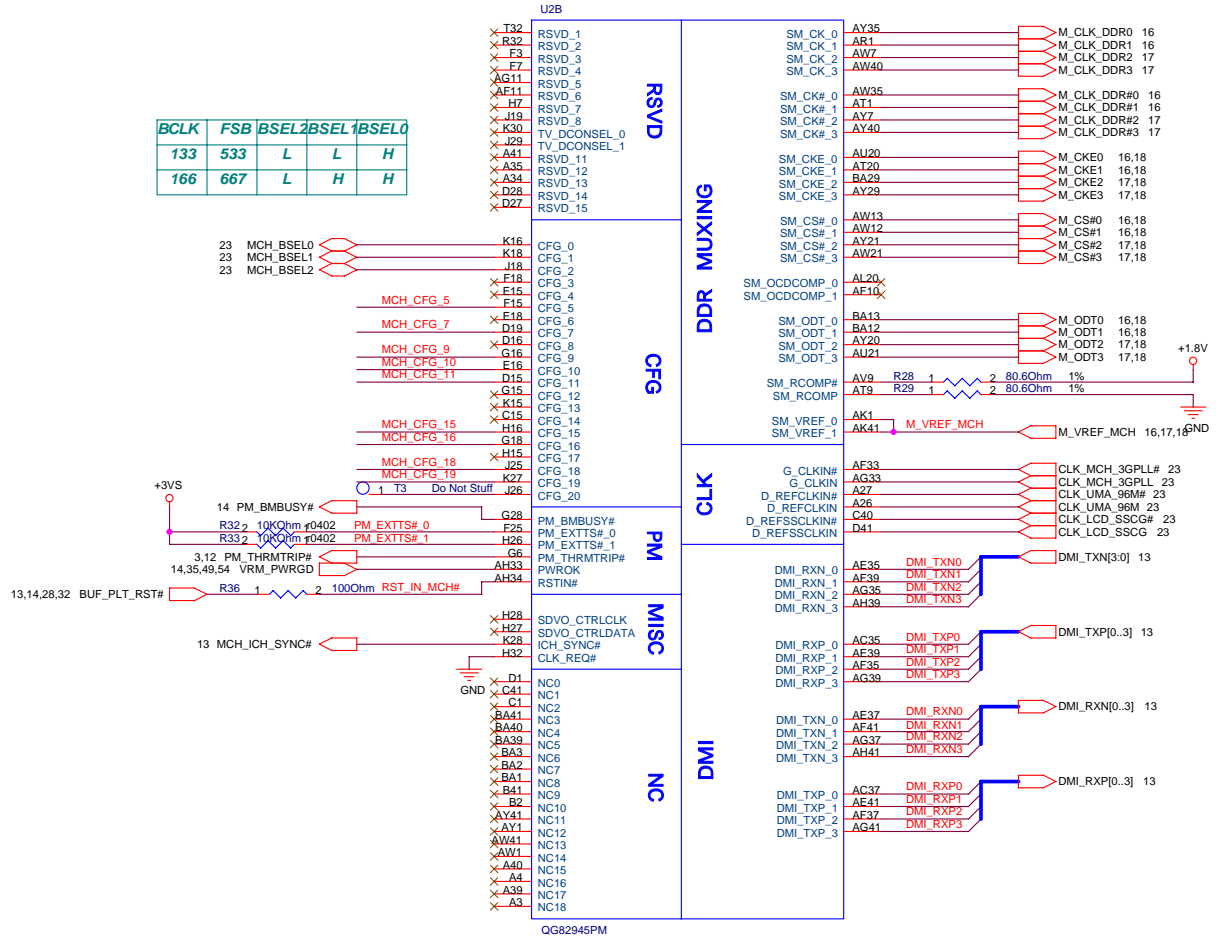
CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

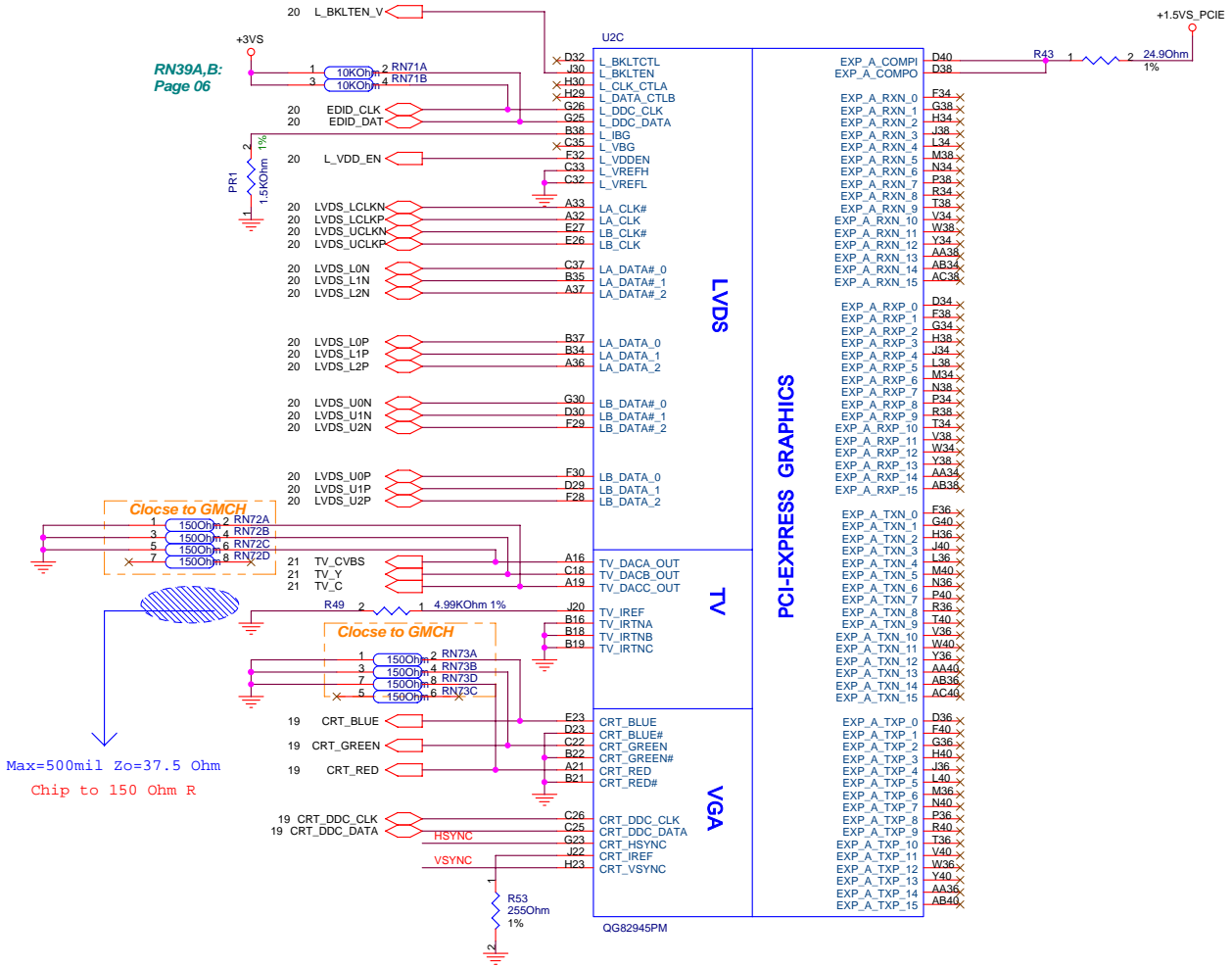


Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



2.0G

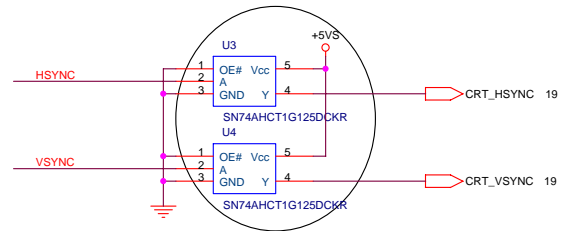


PCI-EXPRESS GRAPHICS

EXP_A_COMPI	D40	
EXP_A_COMPO	D38	
EXP_A_RXN_0	F34	X
EXP_A_RXN_1	G38	X
EXP_A_RXN_2	H34	X
EXP_A_RXN_3	J38	X
EXP_A_RXN_4	L34	X
EXP_A_RXN_5	M38	X
EXP_A_RXN_6	N34	X
EXP_A_RXN_7	P38	X
EXP_A_RXN_8	R34	X
EXP_A_RXN_9	T38	X
EXP_A_RXN_10	V34	X
EXP_A_RXN_11	W38	X
EXP_A_RXN_12	X34	X
EXP_A_RXN_13	AA38	X
EXP_A_RXN_14	AB34	X
EXP_A_RXN_15	AC38	X
EXP_A_RXP_0	D34	X
EXP_A_RXP_1	F38	X
EXP_A_RXP_2	G34	X
EXP_A_RXP_3	H38	X
EXP_A_RXP_4	J34	X
EXP_A_RXP_5	L38	X
EXP_A_RXP_6	M34	X
EXP_A_RXP_7	N38	X
EXP_A_RXP_8	P34	X
EXP_A_RXP_9	R38	X
EXP_A_RXP_10	T34	X
EXP_A_RXP_11	V38	X
EXP_A_RXP_12	W34	X
EXP_A_RXP_13	X38	X
EXP_A_RXP_14	AA34	X
EXP_A_RXP_15	AB38	X
EXP_A_TXN_0	F36	X
EXP_A_TXN_1	G40	X
EXP_A_TXN_2	H36	X
EXP_A_TXN_3	J40	X
EXP_A_TXN_4	L36	X
EXP_A_TXN_5	M40	X
EXP_A_TXN_6	N36	X
EXP_A_TXN_7	P40	X
EXP_A_TXN_8	R36	X
EXP_A_TXN_9	T40	X
EXP_A_TXN_10	V36	X
EXP_A_TXN_11	W40	X
EXP_A_TXN_12	X36	X
EXP_A_TXN_13	AA40	X
EXP_A_TXN_14	AB36	X
EXP_A_TXN_15	AC40	X
EXP_A_TXP_0	D36	X
EXP_A_TXP_1	F40	X
EXP_A_TXP_2	G36	X
EXP_A_TXP_3	H40	X
EXP_A_TXP_4	J36	X
EXP_A_TXP_5	L40	X
EXP_A_TXP_6	M36	X
EXP_A_TXP_7	N40	X
EXP_A_TXP_8	P36	X
EXP_A_TXP_9	R40	X
EXP_A_TXP_10	T36	X
EXP_A_TXP_11	V40	X
EXP_A_TXP_12	W36	X
EXP_A_TXP_13	X40	X
EXP_A_TXP_14	AA36	X
EXP_A_TXP_15	AB40	X

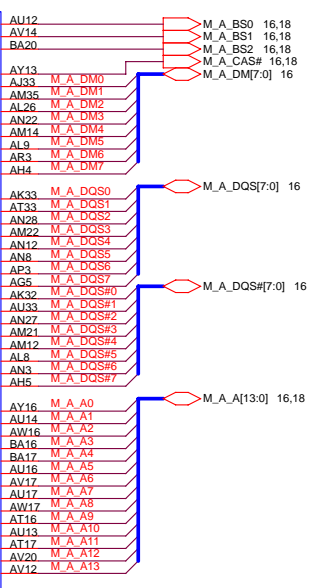
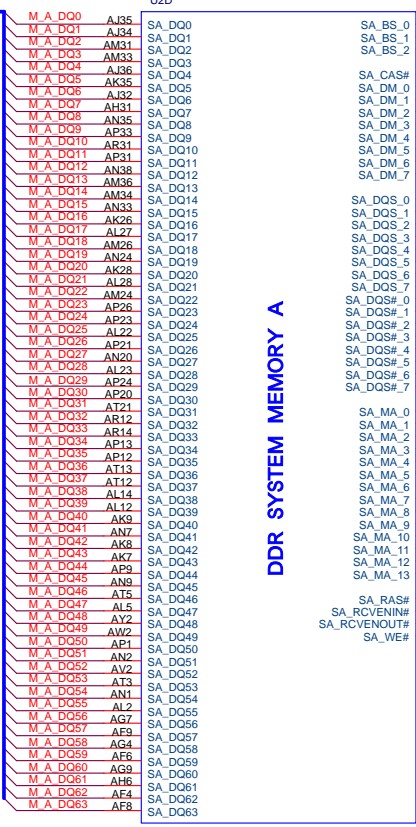
Max=500mil Zo=37.5 Ohm
Chip to 150 Ohm R

Change 5V parts



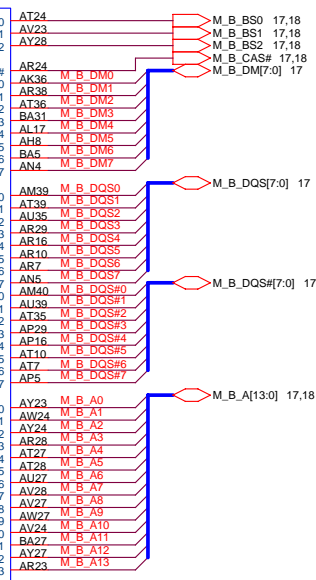
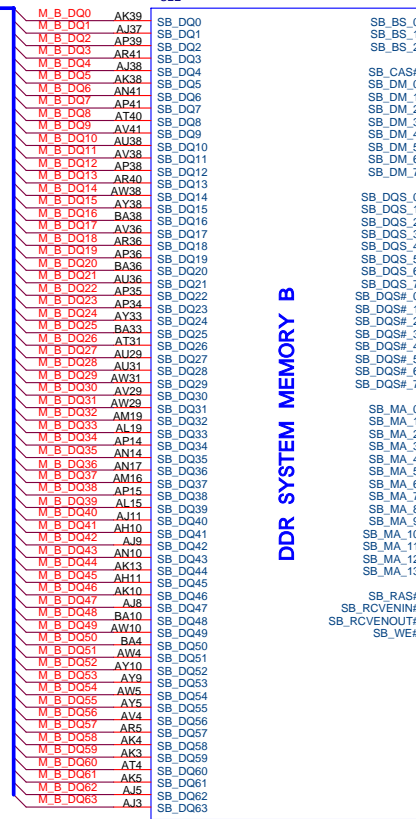
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16 M_A_DQ[63:0]



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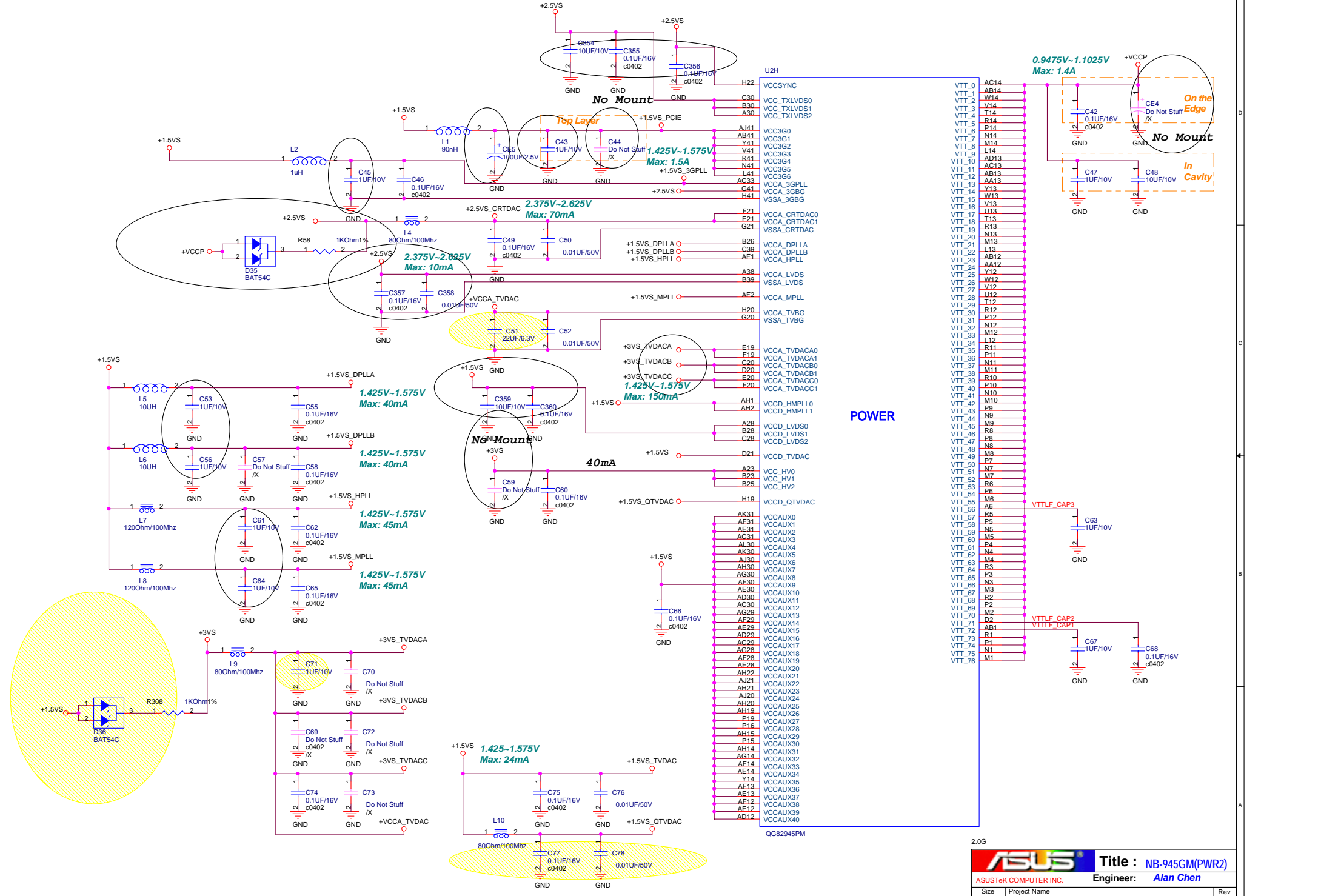
17 M_B_DQ[63:0]



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ASUS Title : NB-945GM(DDR2)
ASUSTeK COMPUTER INC. Engineer: Alan Chen
Size Project Name
Custom F84F Rev 2.00G
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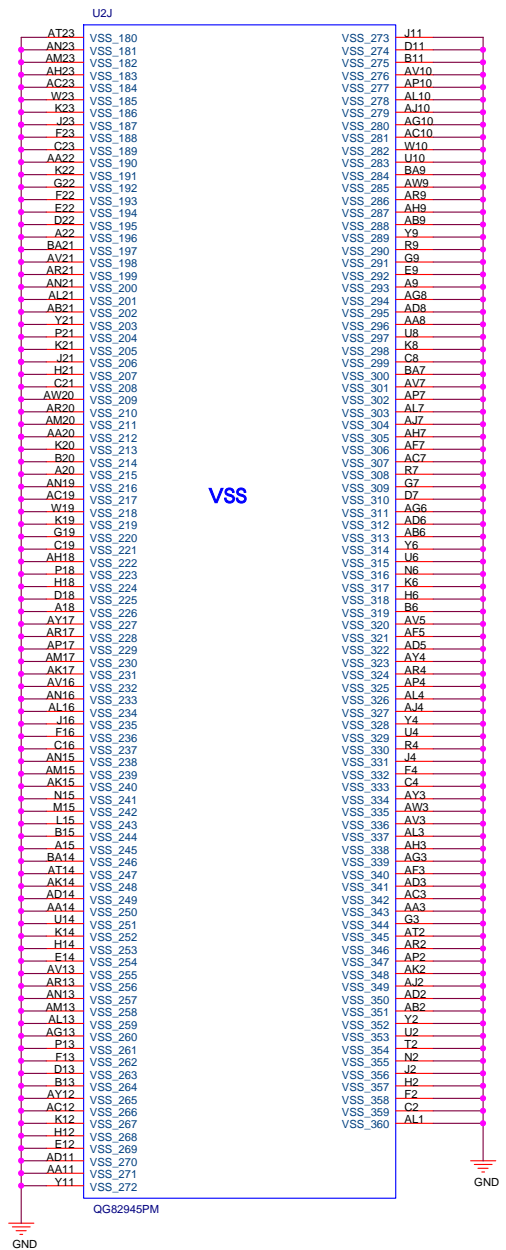
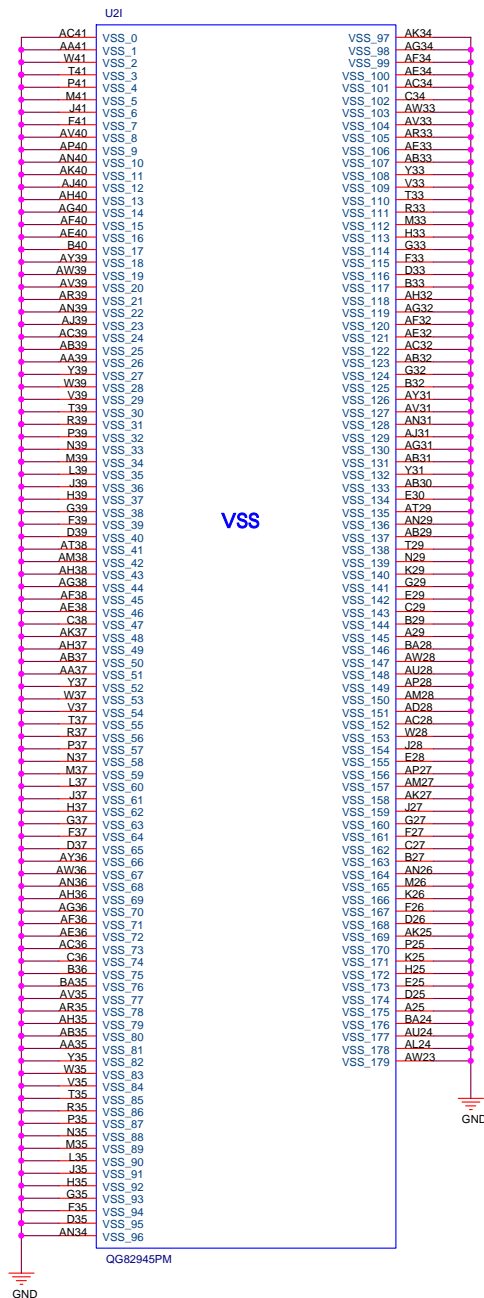
POWER

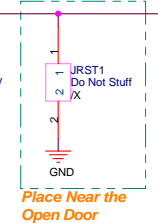
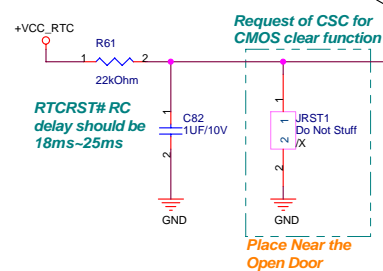
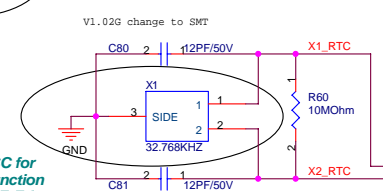
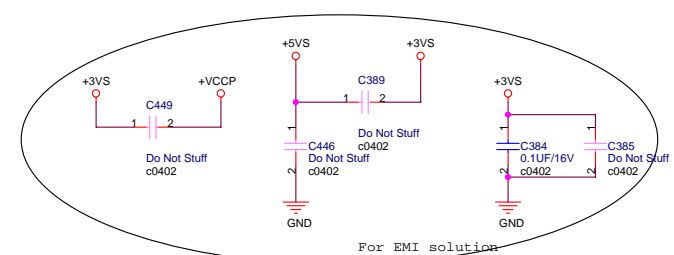
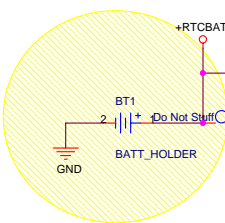
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ASUS Title : NB-945GM(PWR2)

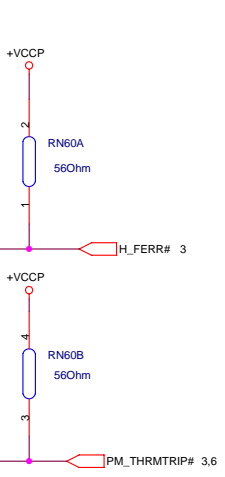
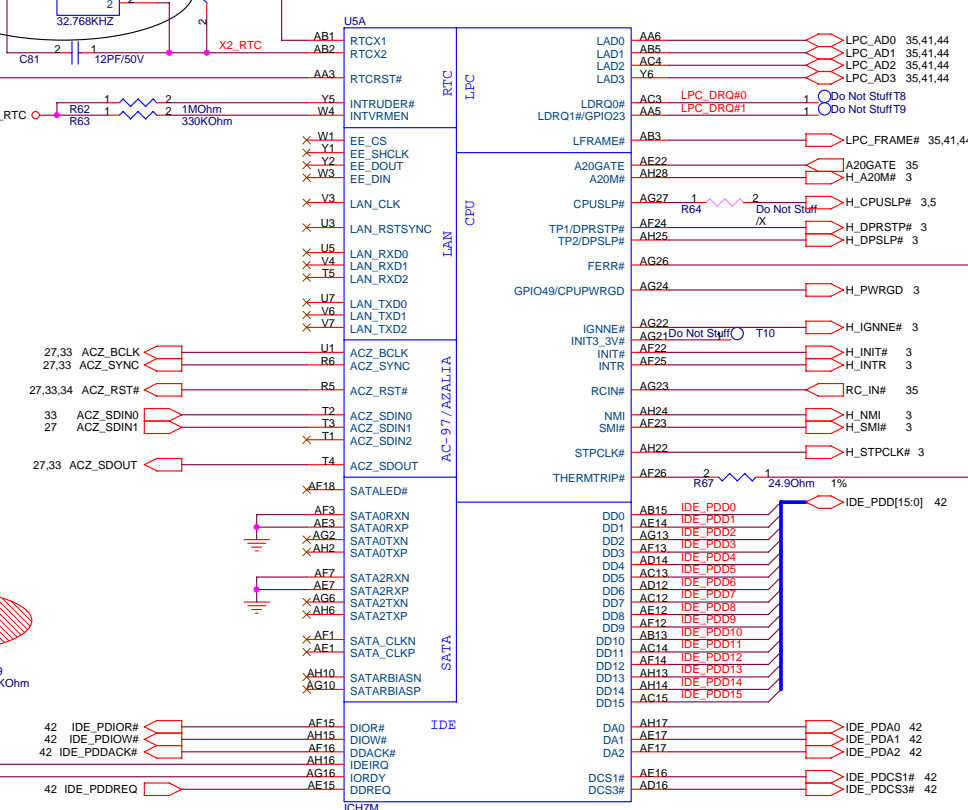
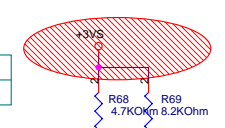
ASUSTek COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84F	2.00G
Date: Friday, April 07, 2006	Sheet 10 of 57	

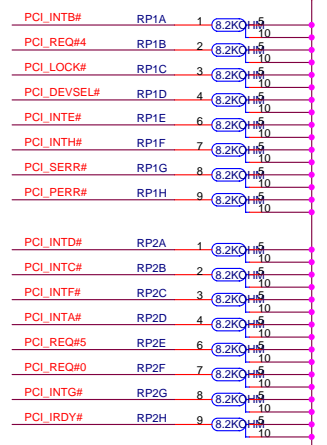
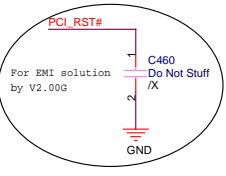
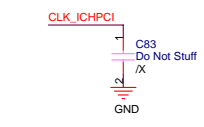
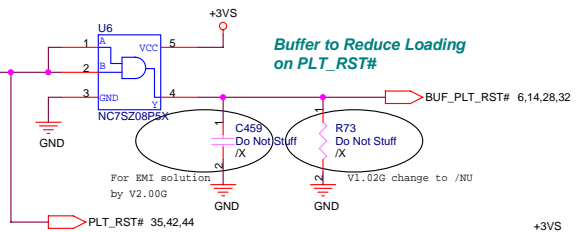
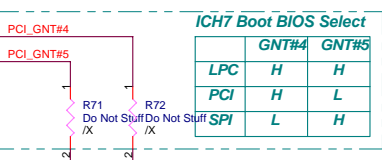
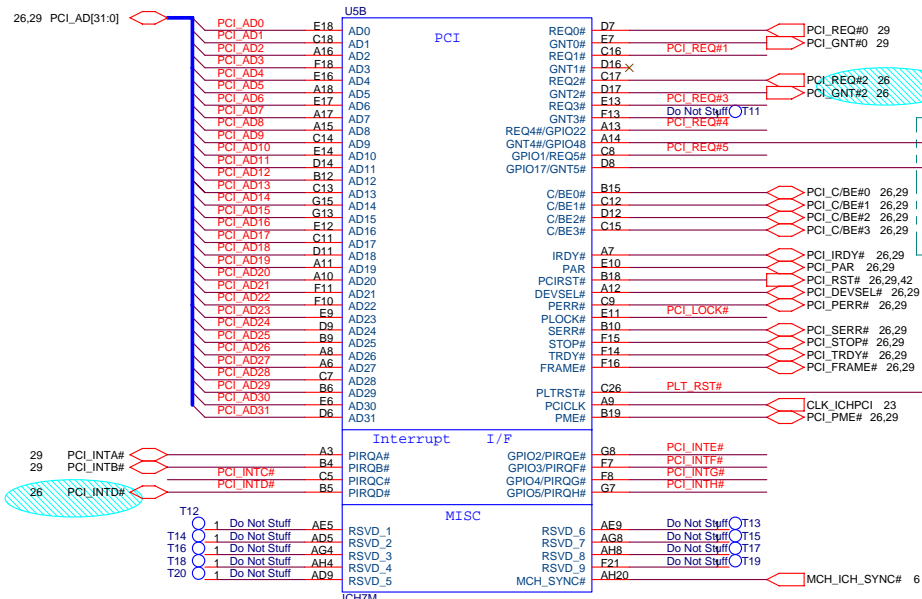




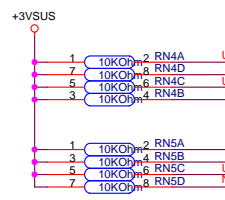
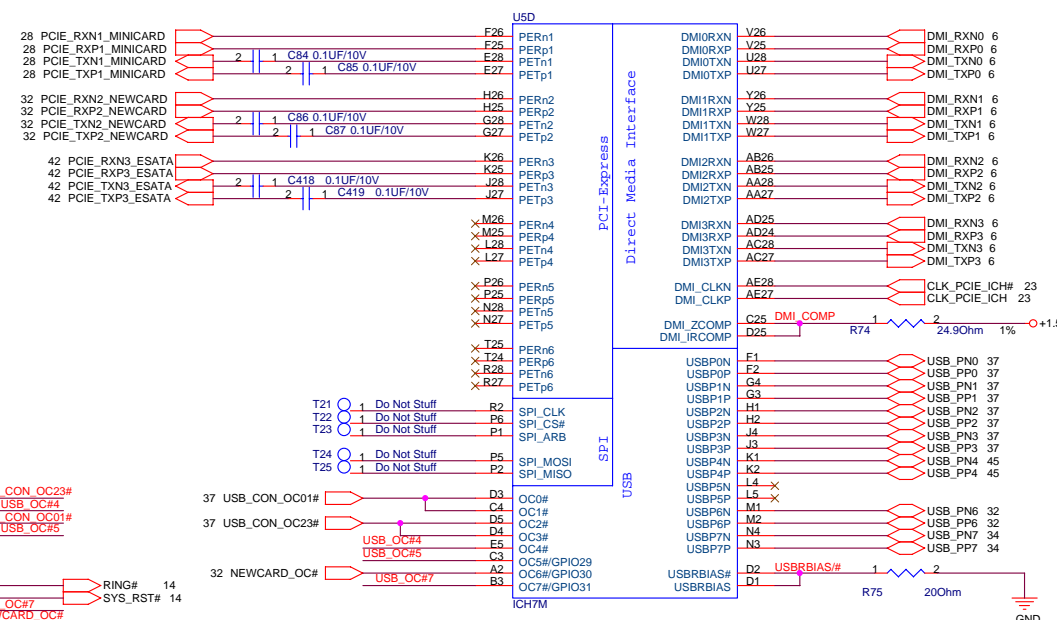
ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM



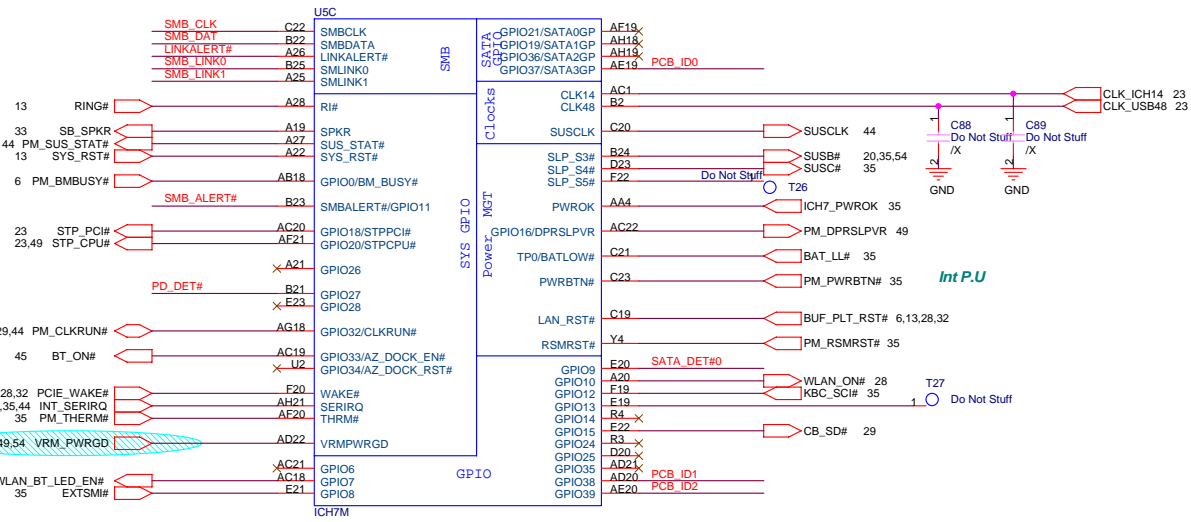
2.0G



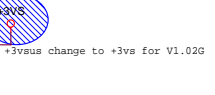
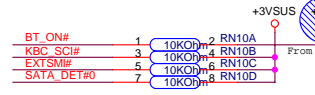
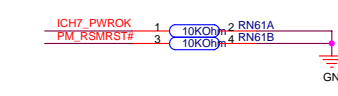
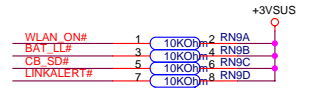
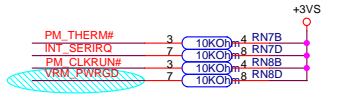
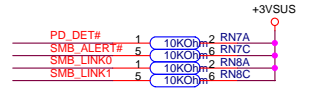
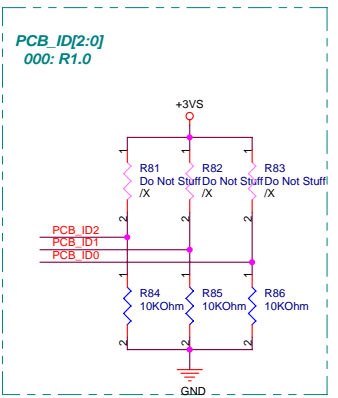
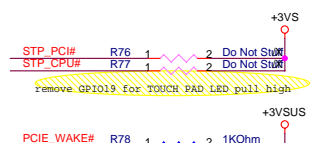
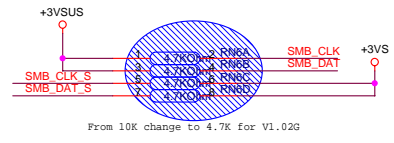
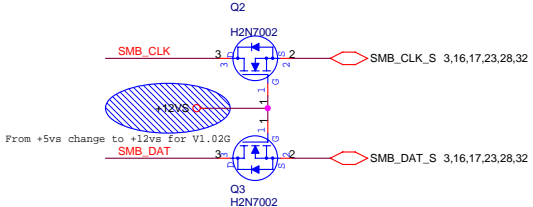
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	Bluetooth
USB 5	N/A
USB 6	New Card
USB 7	CMOS Camera



2.0G



06/03/30, refer 296J R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.

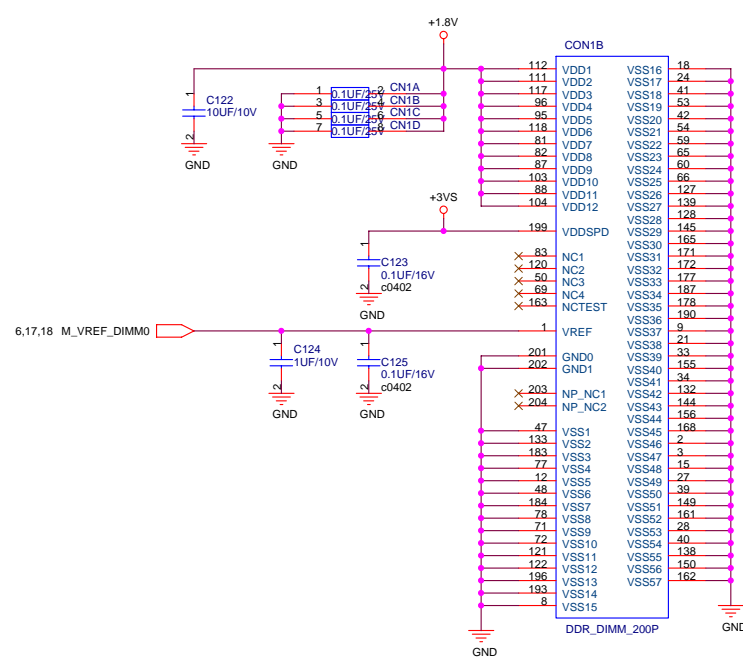


2.0G

ASUS		Title : SB-ICH7M(3)	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z84F	2.00G	
Date: Friday, April 07, 2006	Sheet	14	of 57

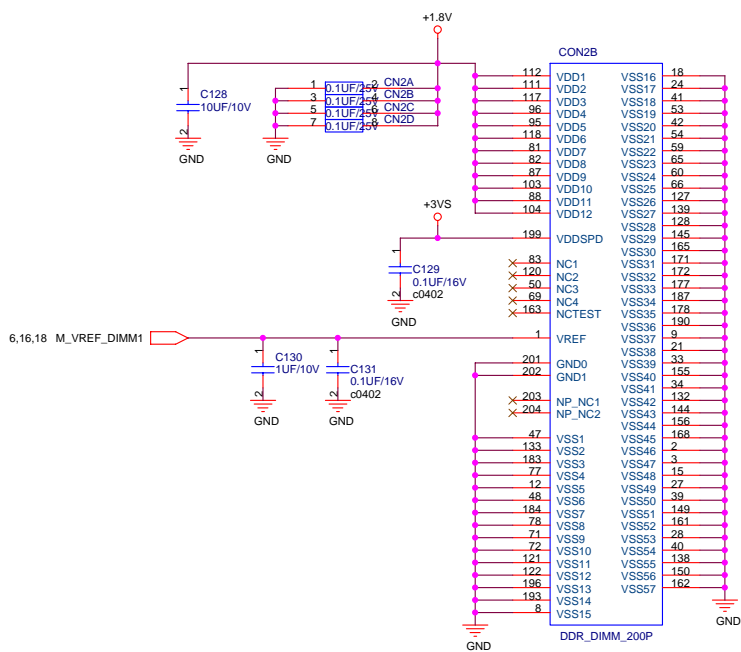
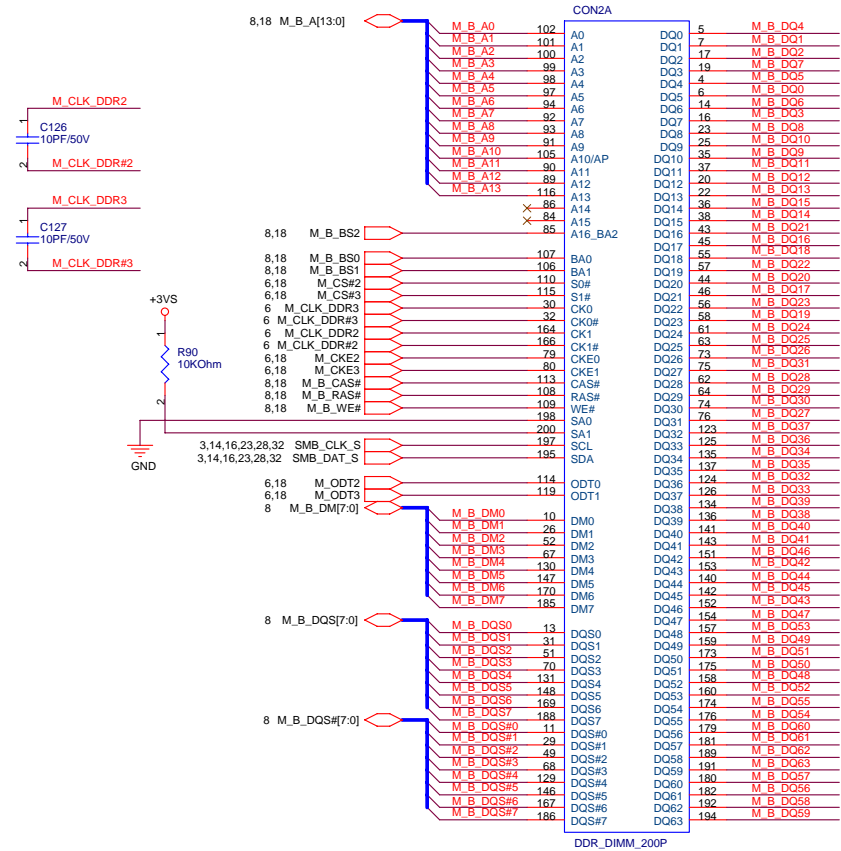
M_A_DQ[63:0] 8

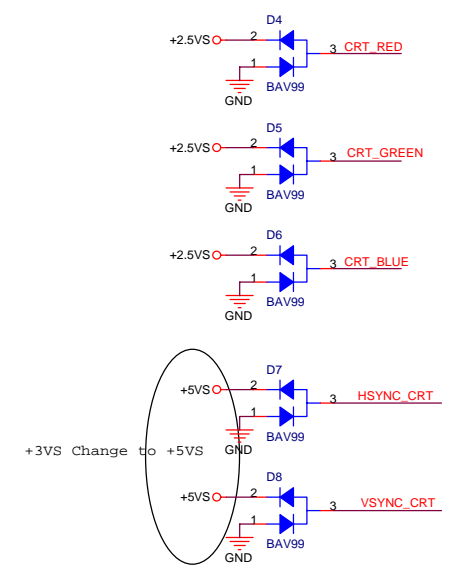
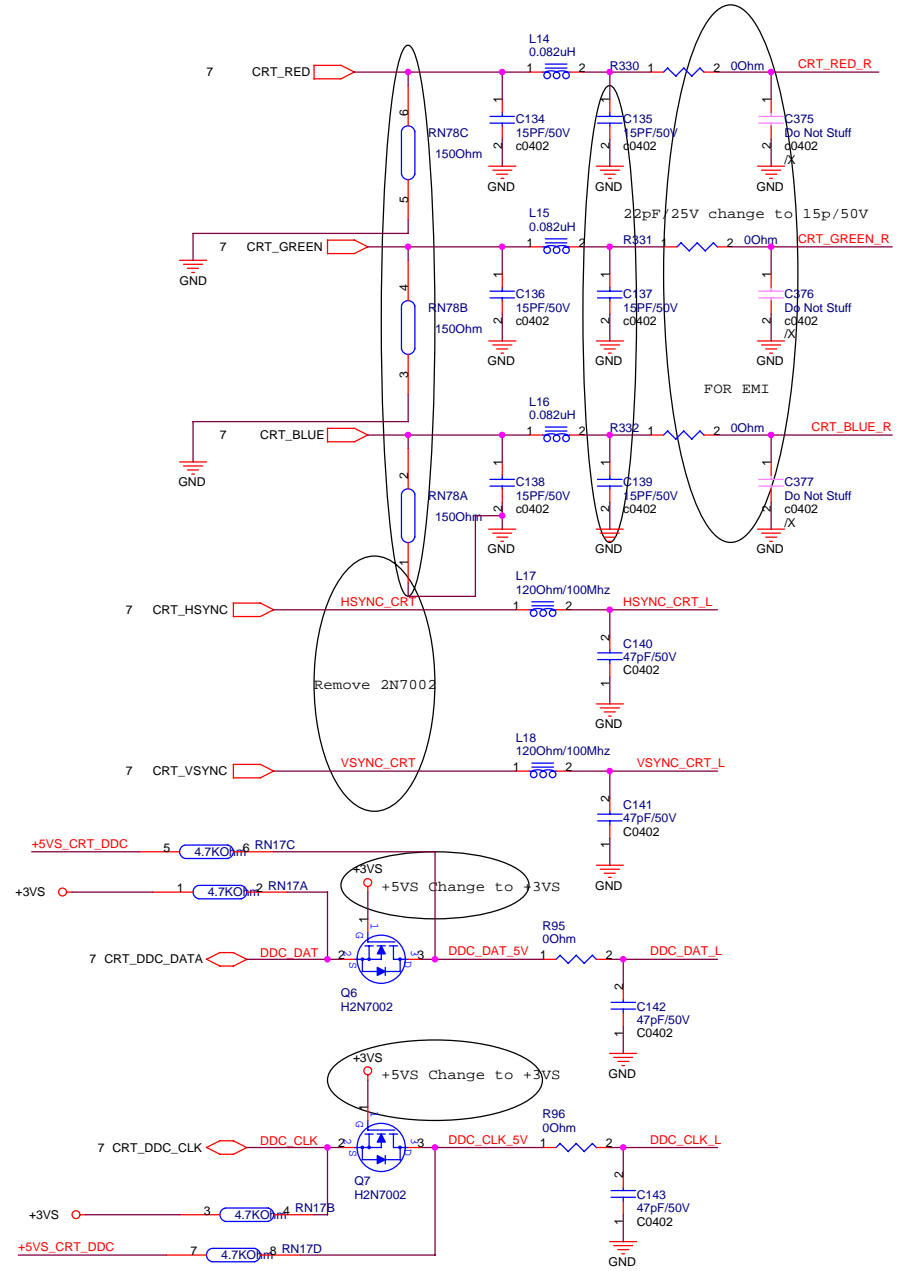
REV Type



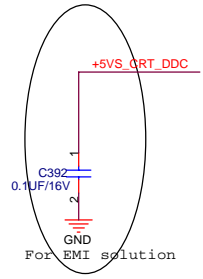
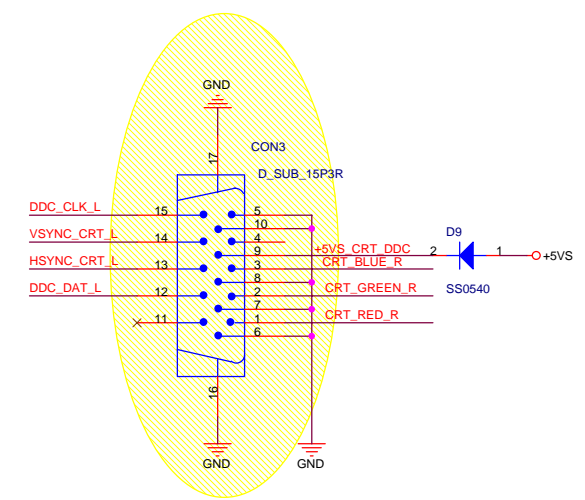
M_B_DQ[63:0] 8

STD Type





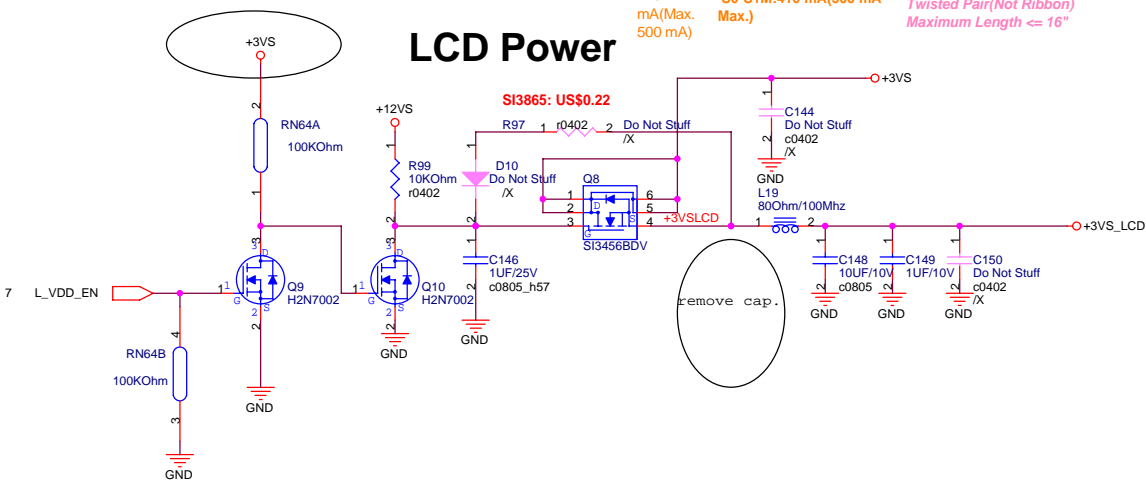
PLACE ESD Diodes near VGA port



For EMI solution

2.0G		ASUS [®] Title : CRT	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z84F	2.00G	
Date: Friday, April 07, 2006	Sheet	19	of 57

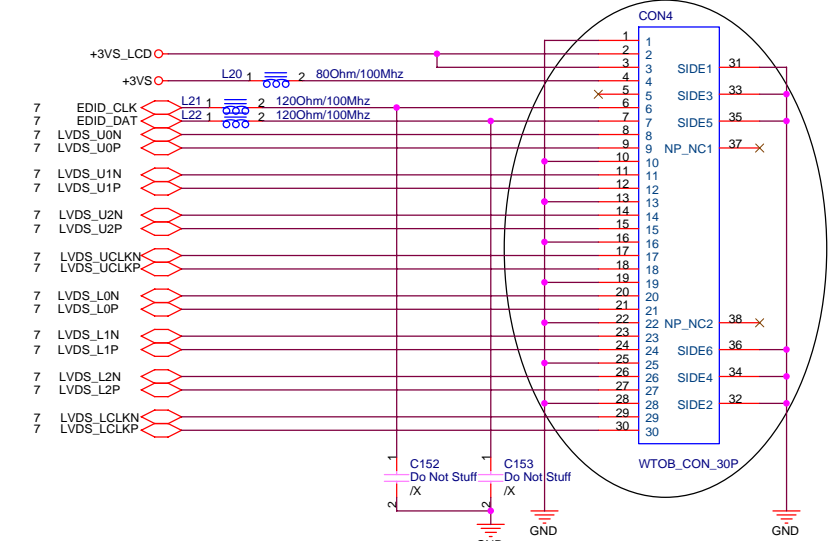
LCD Backlight Control



3V-3.6V Full
Active: 3-3.6V
410 mA(Max. 500 mA)
S0-S1M:410 mA(500 mA Max.)

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

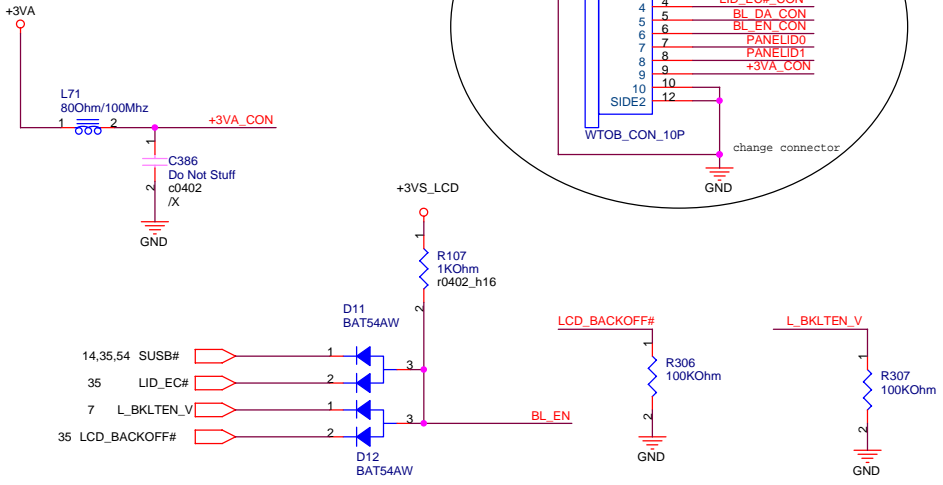
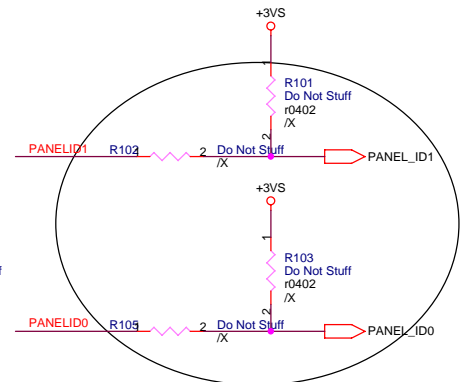
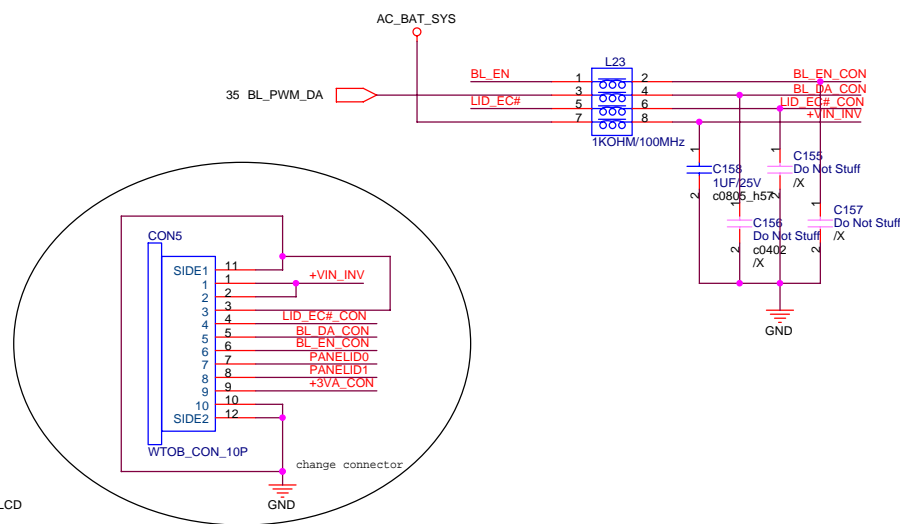
LCD LVDS Interface



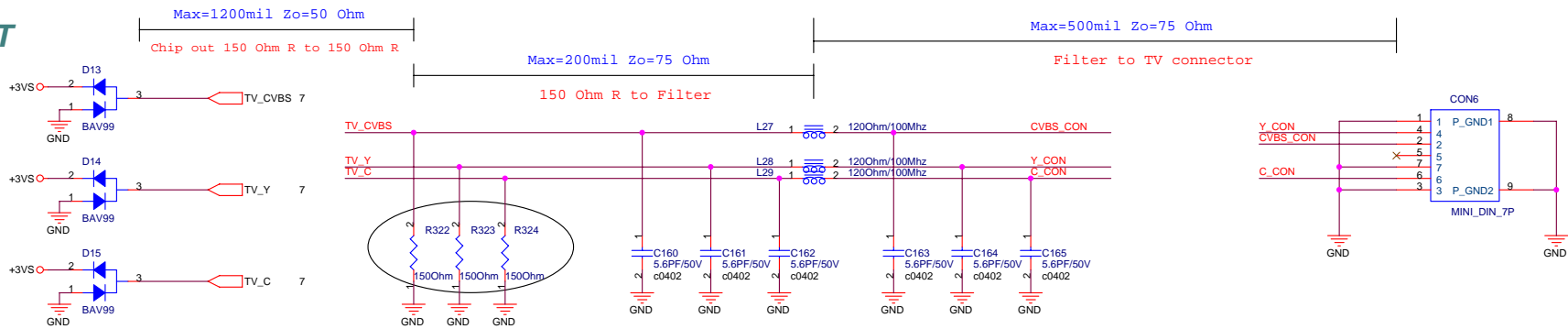
INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800
PANEL ID0 RESERVE FOR VENDOR



TV OUT

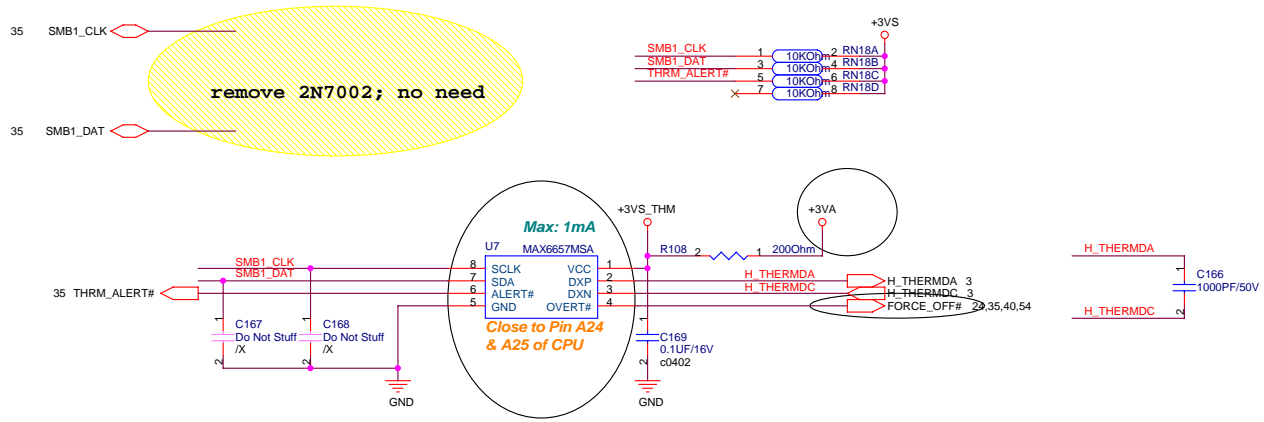


PLACE ESD
Diodes near
TV port

2.0G

		Title : TV OUT & DVI CON.	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size Custom	Project Name Z84F	Rev 2.00G	
Date: Friday, April 07, 2006		Sheet 21 of 57	

Thermal Sensor



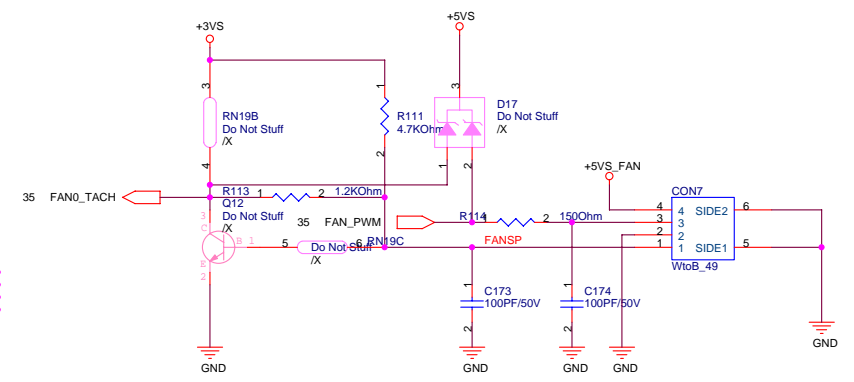
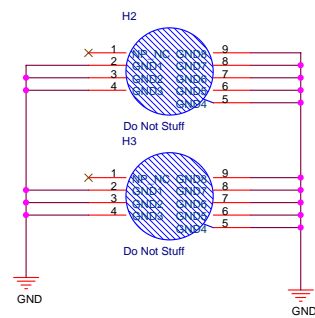
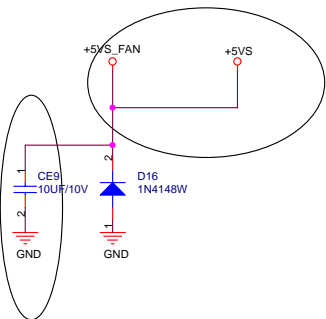
Route H_THERMDA and H_THERMDC on the same layer

- OTHER SIGNALS
- 15 mils
- =====GND
- 10 mils
- =====H_THERMDA(10 mils)
- 10 mils
- =====H_THERMDC(10 mils)
- 10 mils
- =====GND
- 15 mils
- OTHER SIGNALS

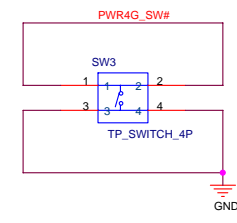
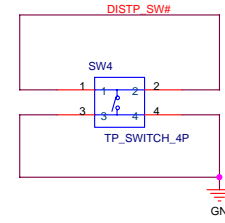
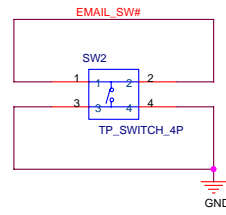
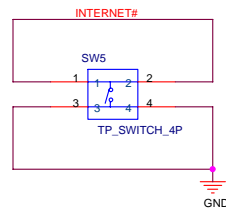
Avoid FSB,Power

DC FAN Control

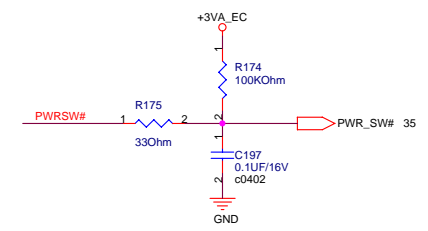
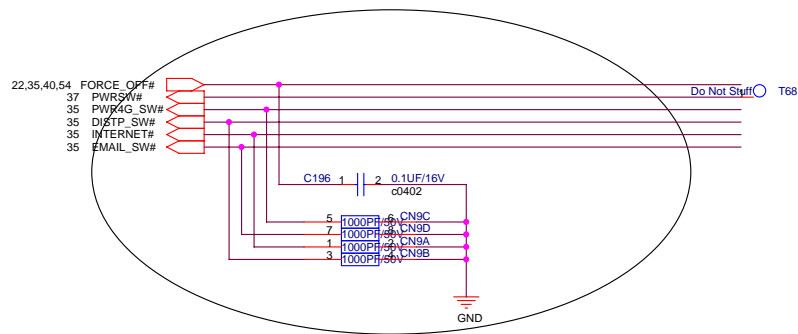
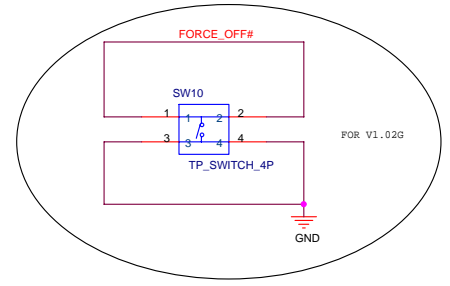
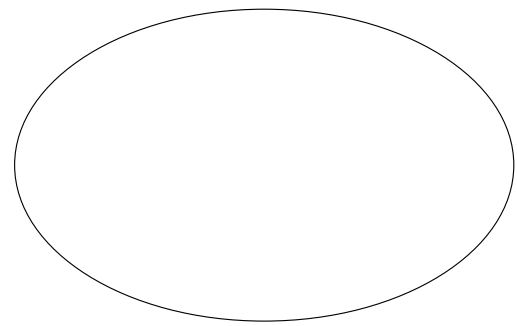
Remove Fan control circuit

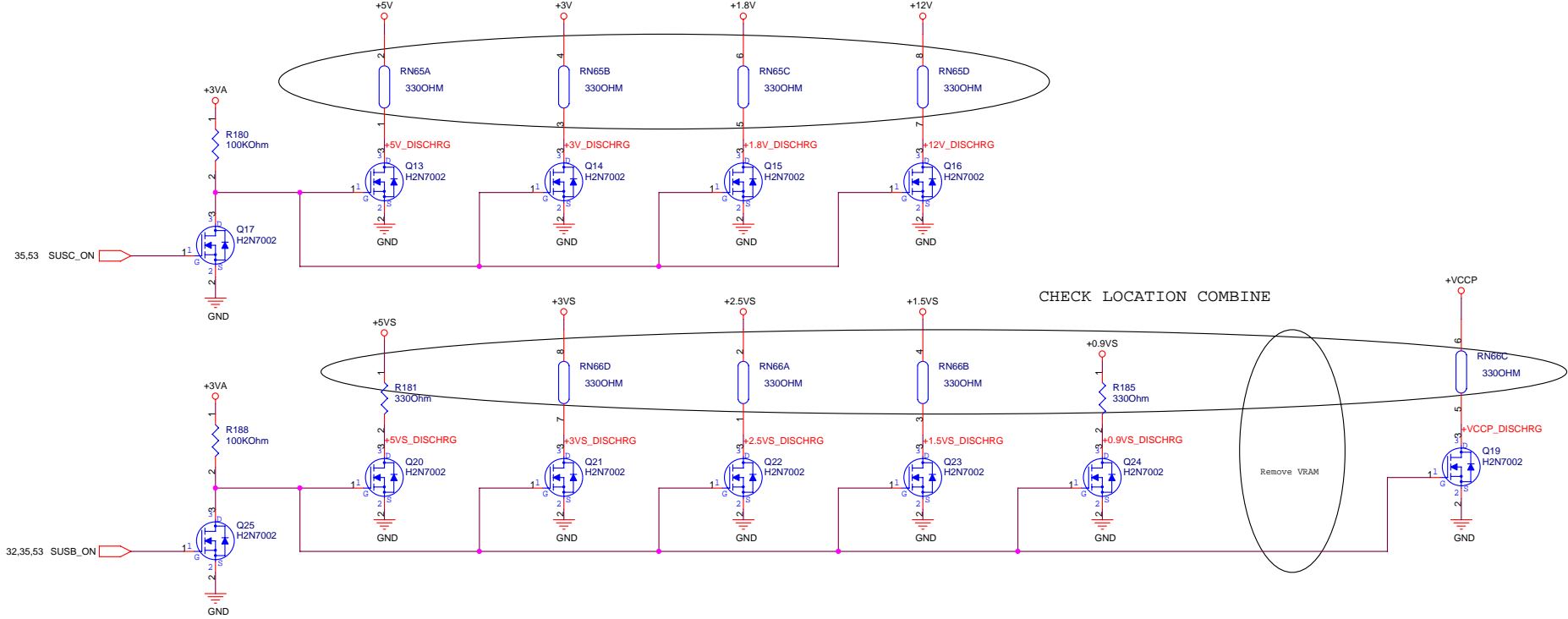


CPU FAN will be forced on:
 1) Thermal Sensor Over-temperature
 2) WATCHDOG asserted by EC



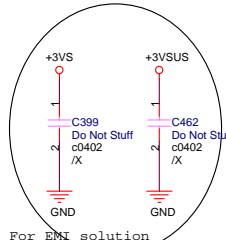
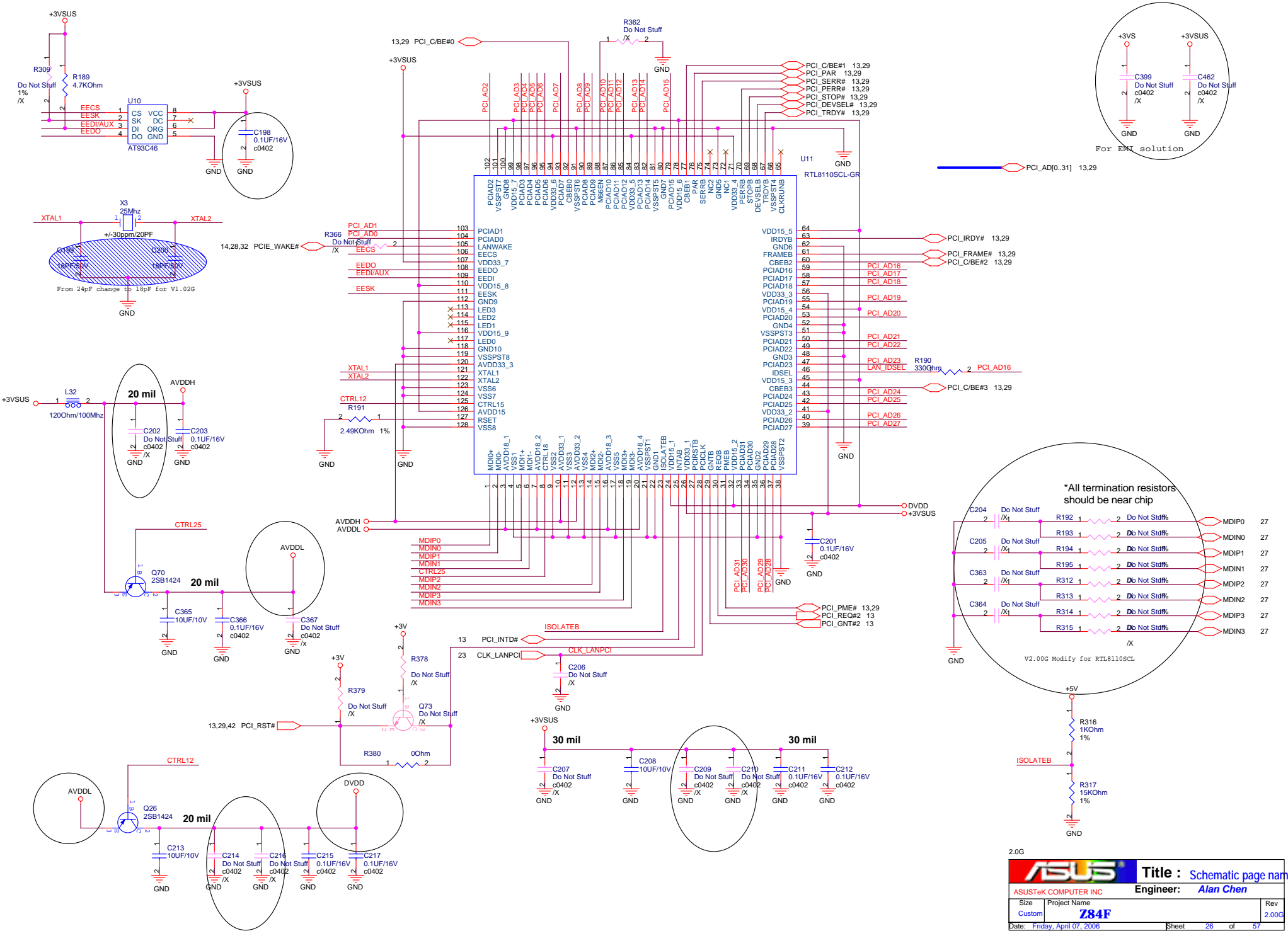
SHUT_DOWN#





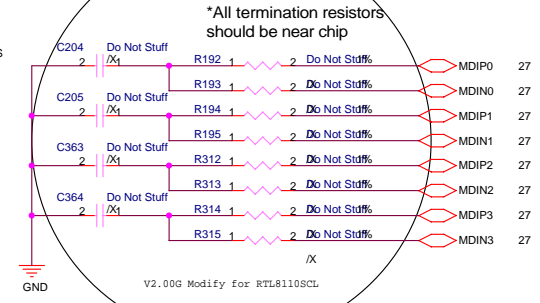
2.0G

		Title : DISCHARGE & EMI CAP
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen
Size Custom	Project Name Z84F	Rev 2.00G
Date: Friday, April 07, 2006	Sheet 25	of 57



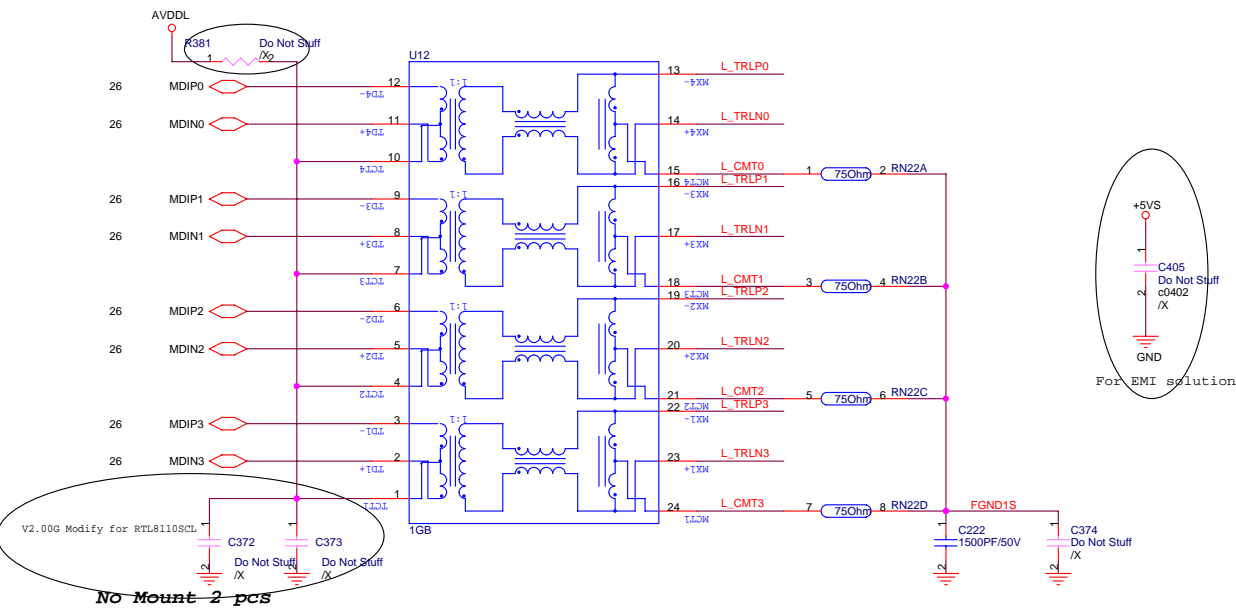
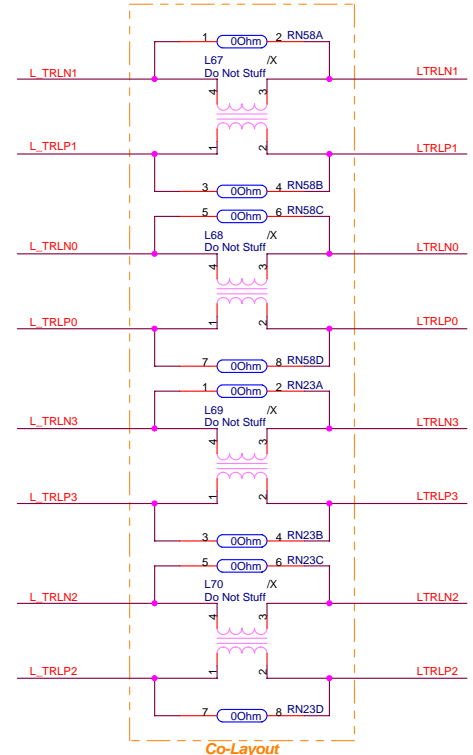
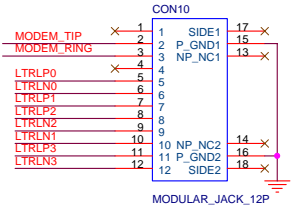
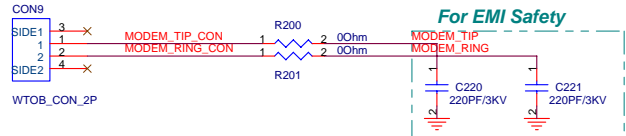
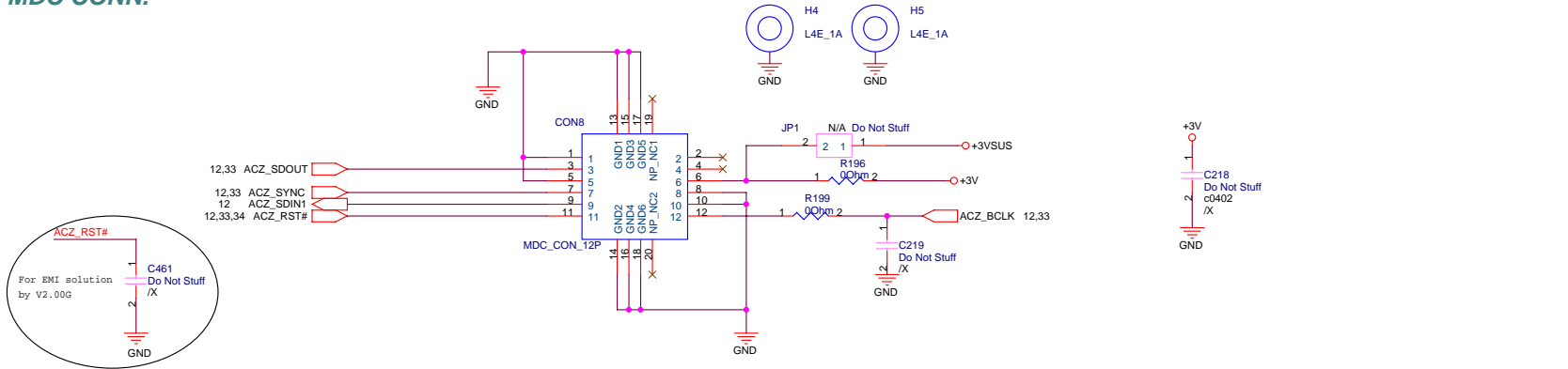
PCI_AD[0..31] 13.29

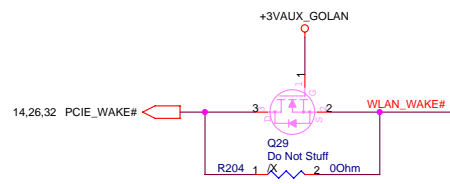
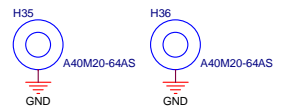
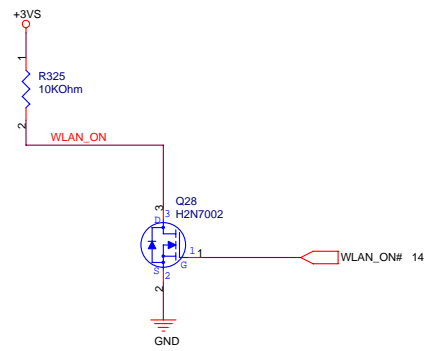
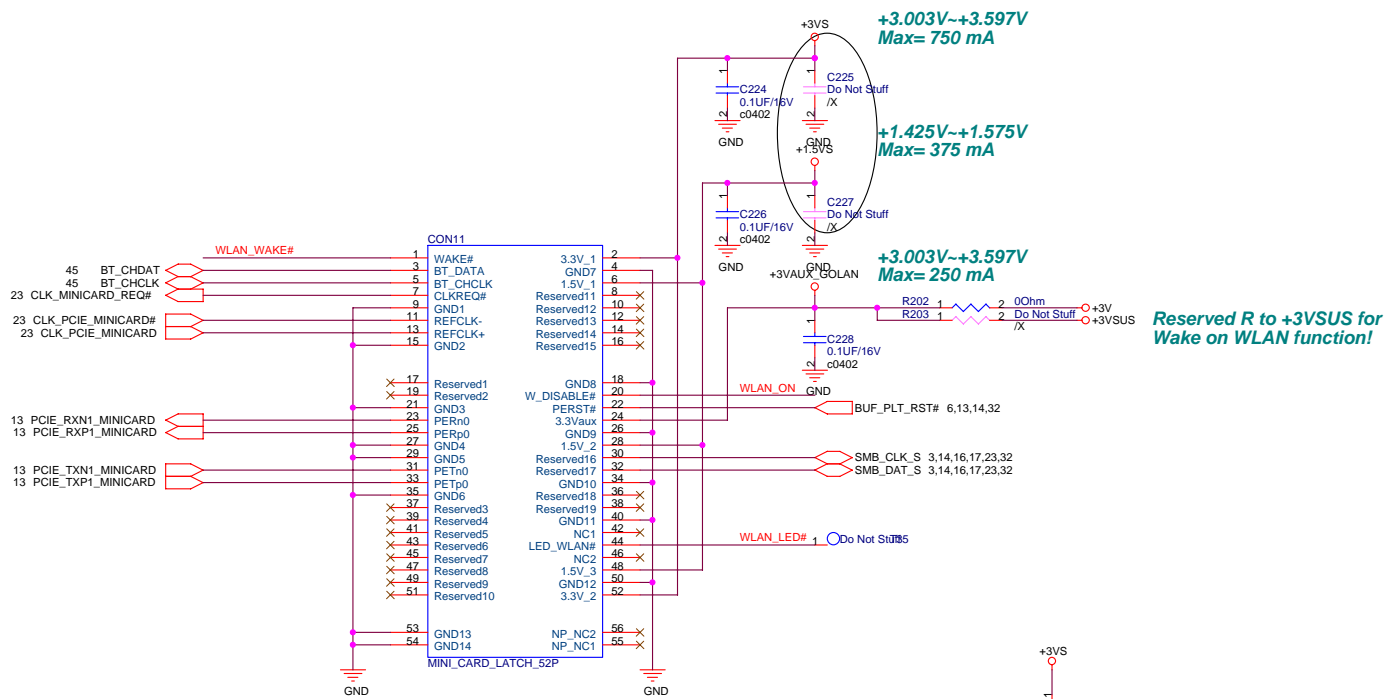
PCI_AD16 13.29

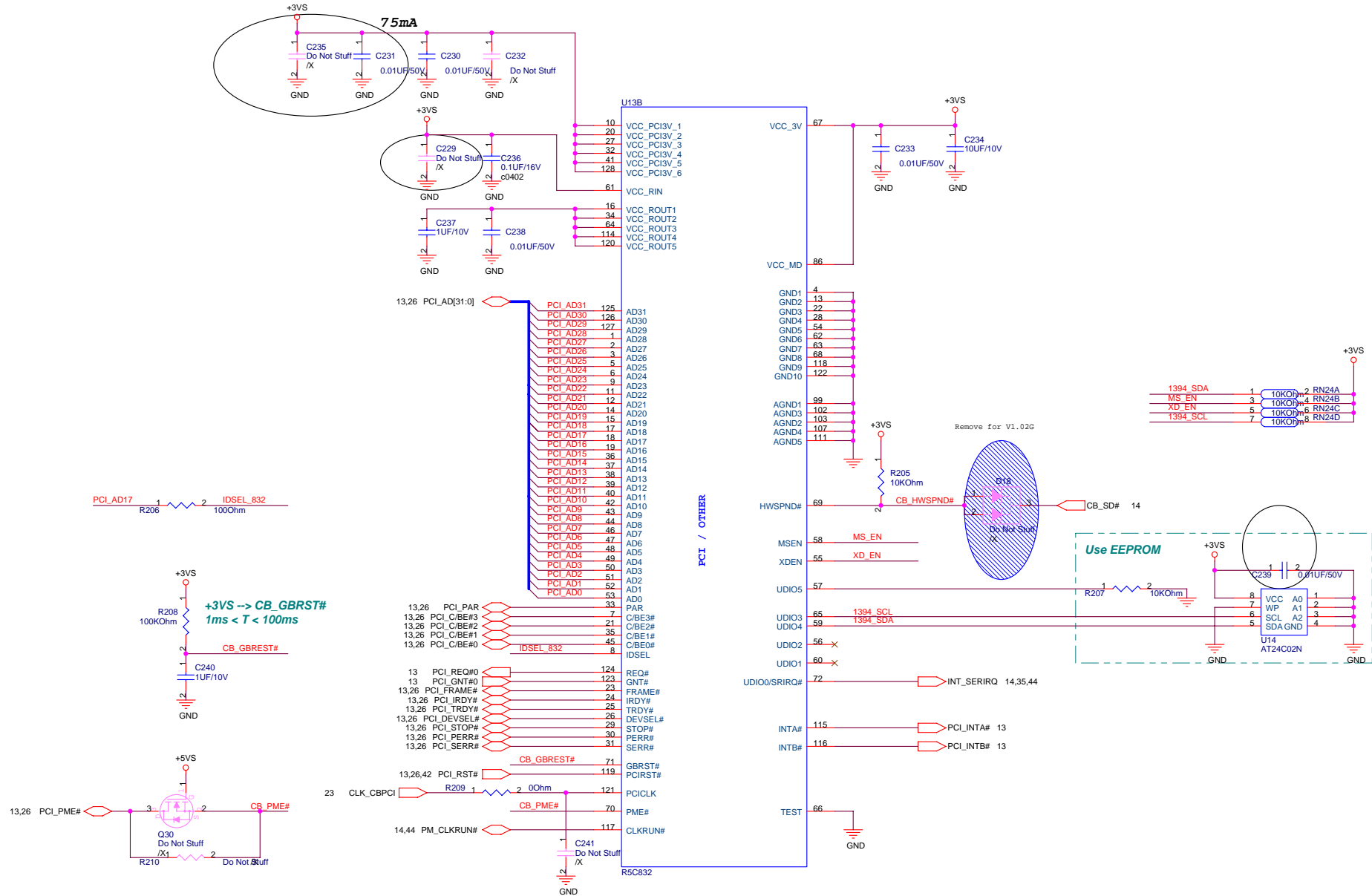


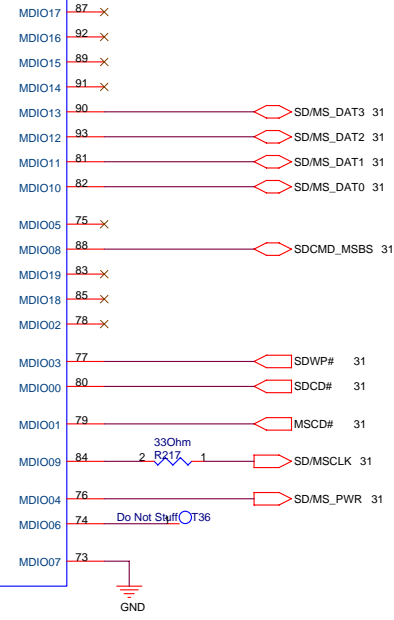
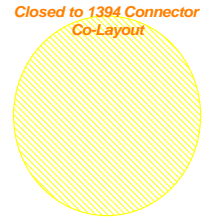
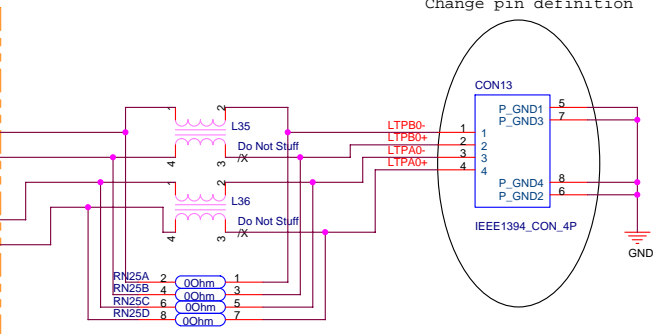
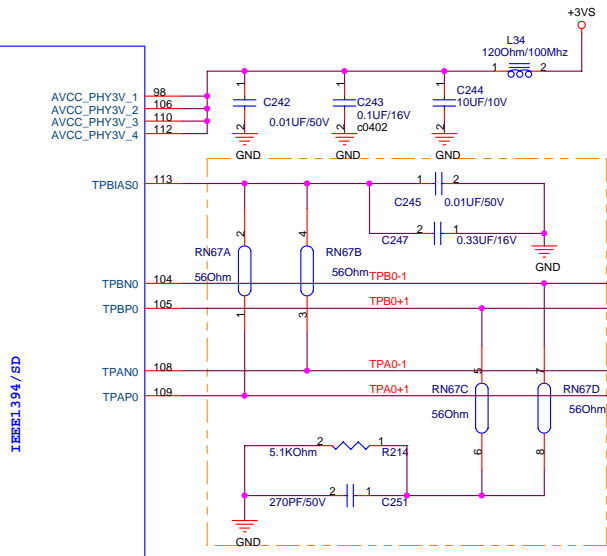
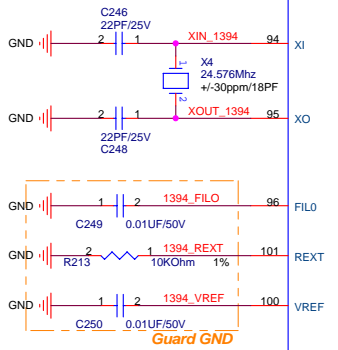
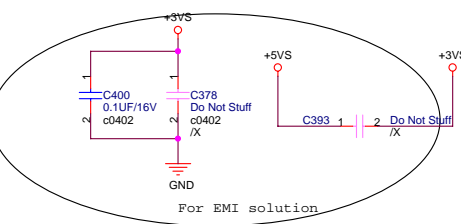
MDC CONN.

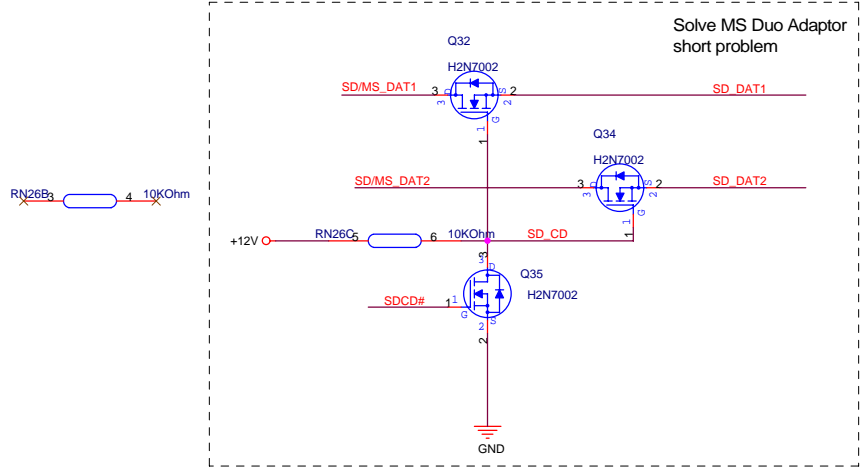
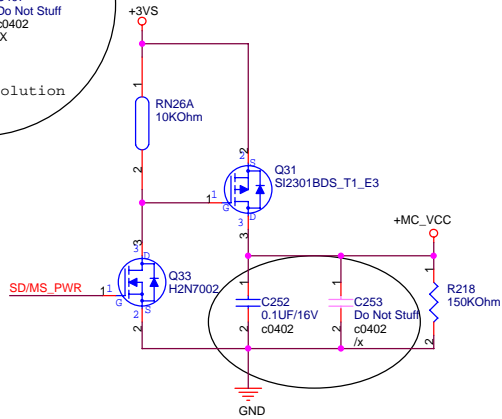
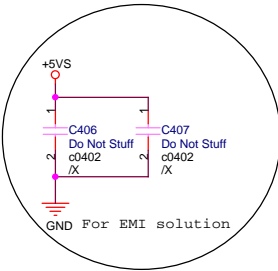
For MDC



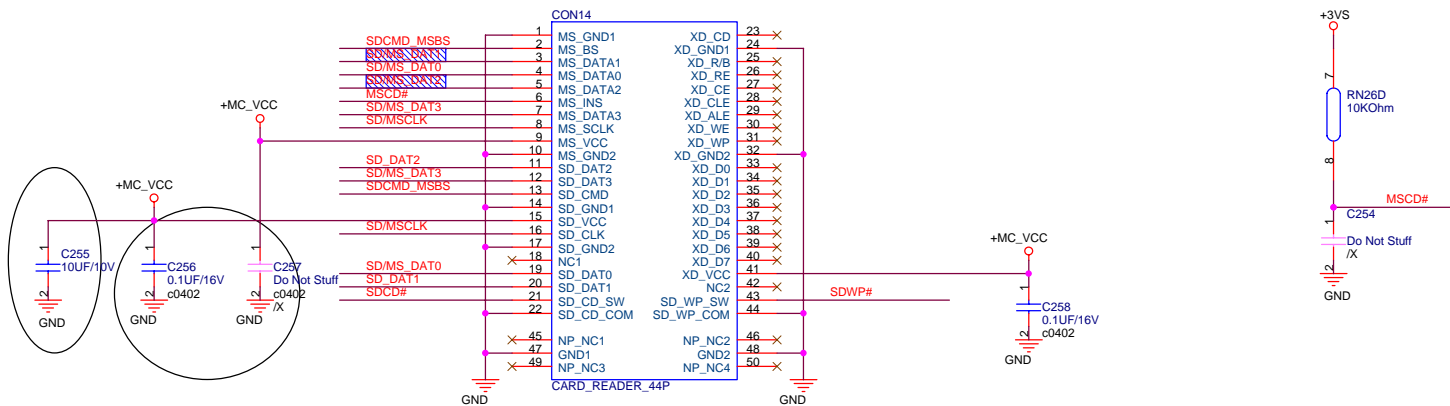


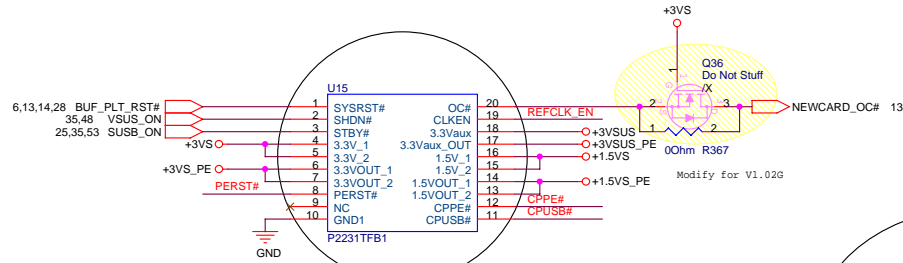
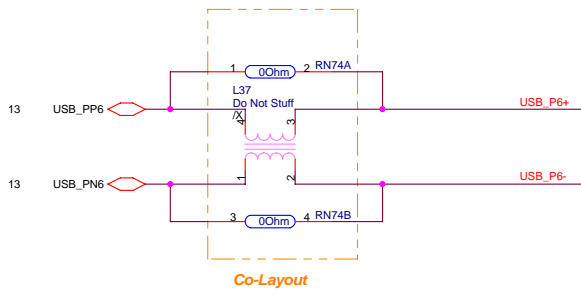






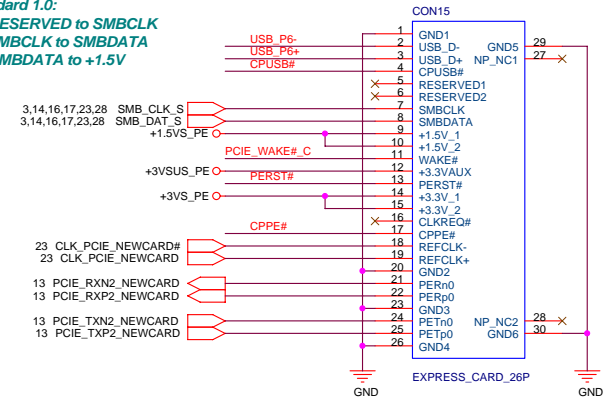
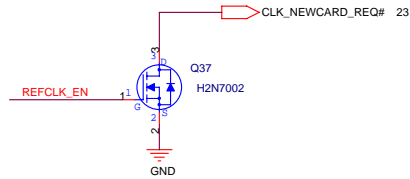
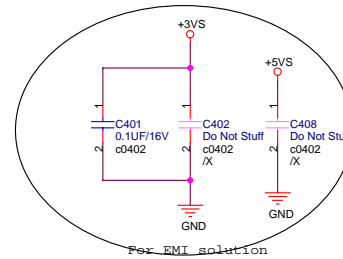
- SD/MS_DAT3 30
- SD/MS_DAT2 30
- SD/MS_DAT1 30
- SD/MS_DAT0 30
- SDCMD_MSBS 30
- SDWP# 30
- SDCD# 30
- MSCD# 30
- SD/MSCLK 30
- SD/MS_PWR 30



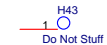
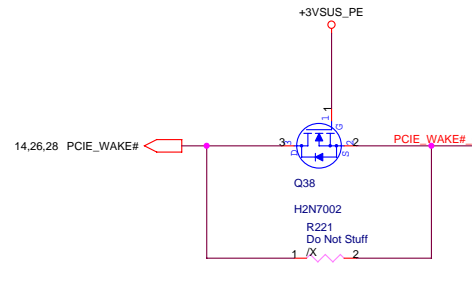
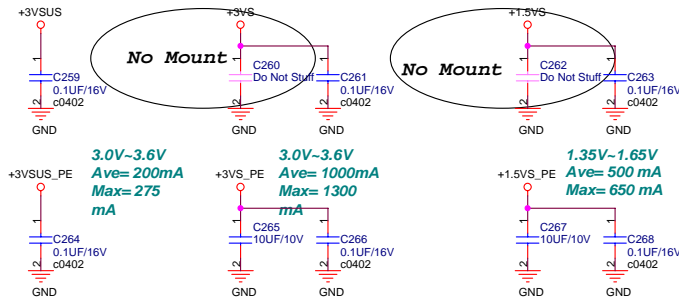
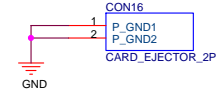


change part to Lead free

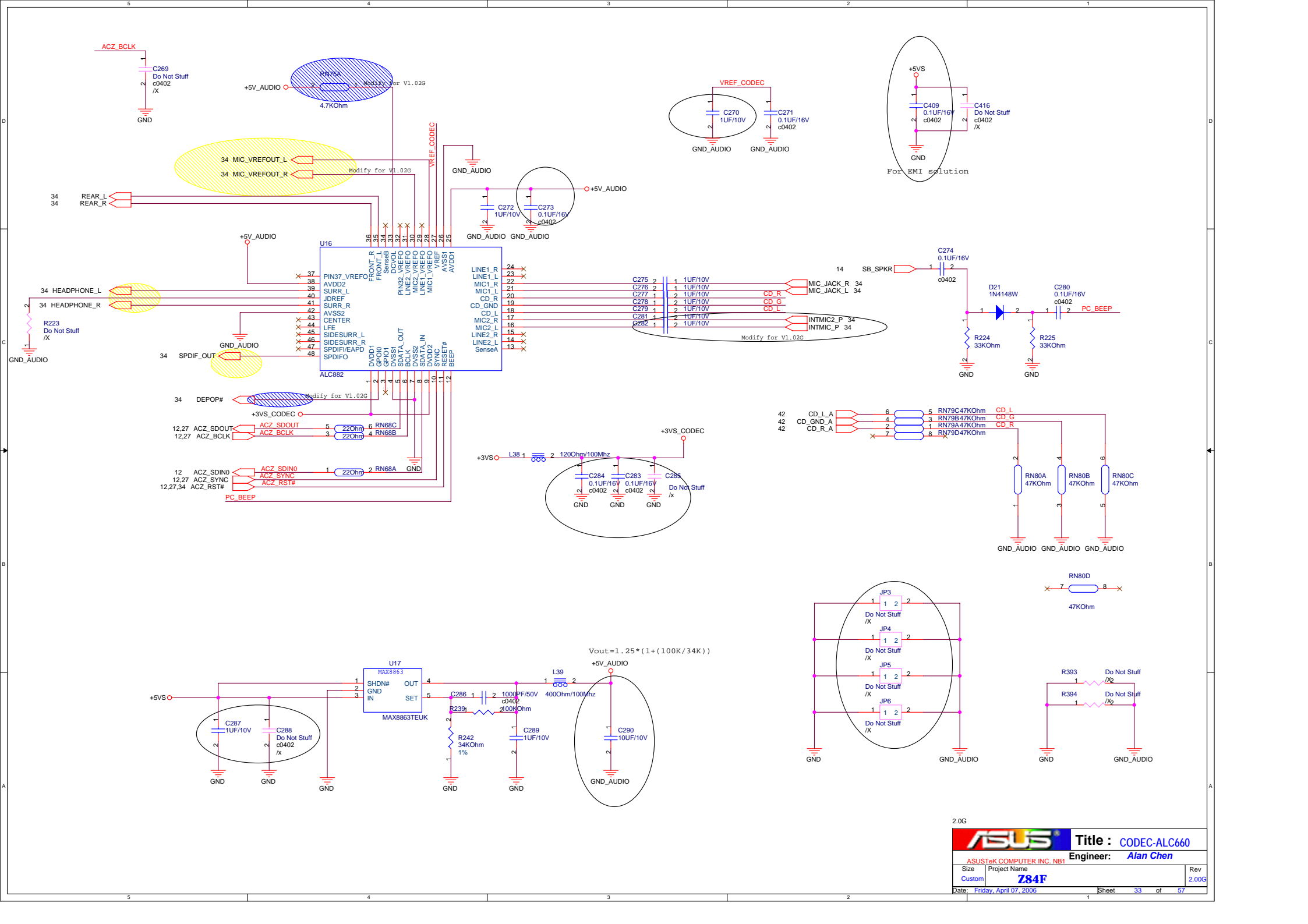
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

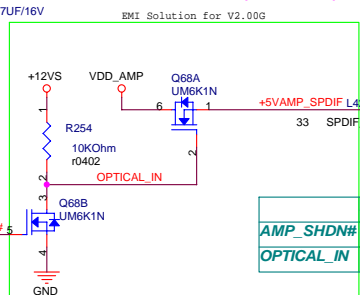
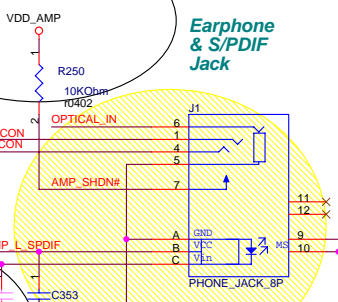
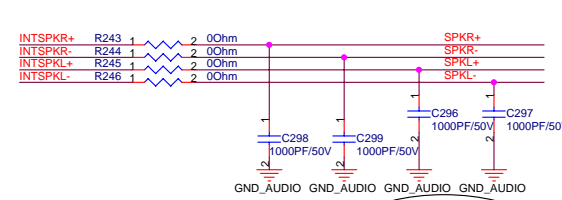
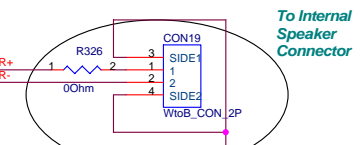
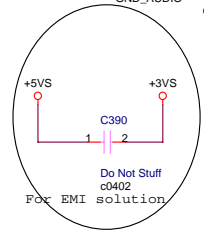
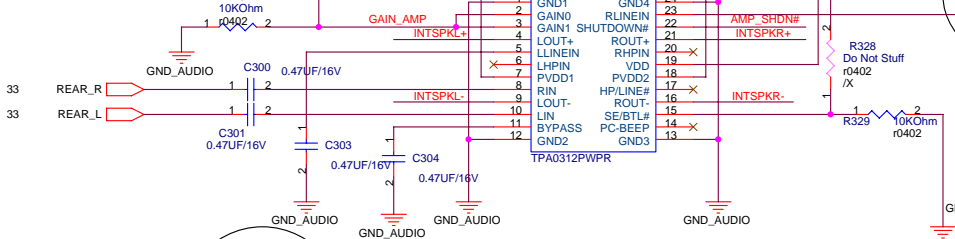
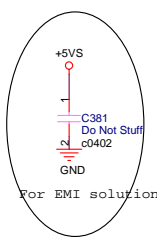


NewCard Ejector



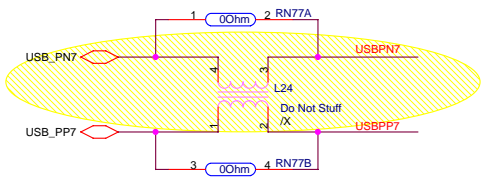
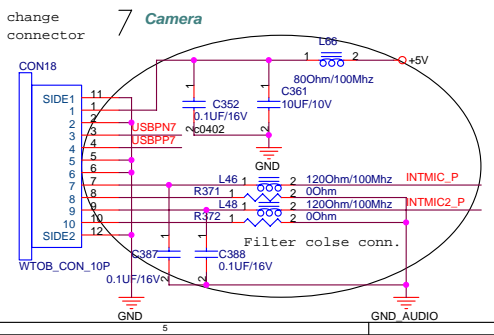
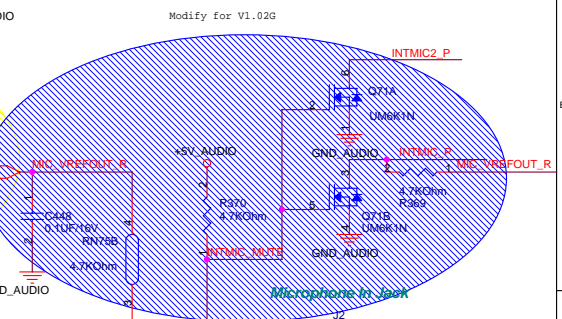
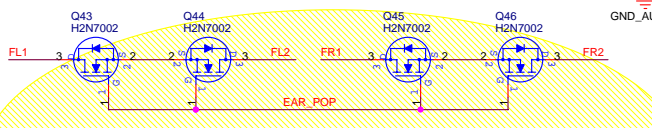
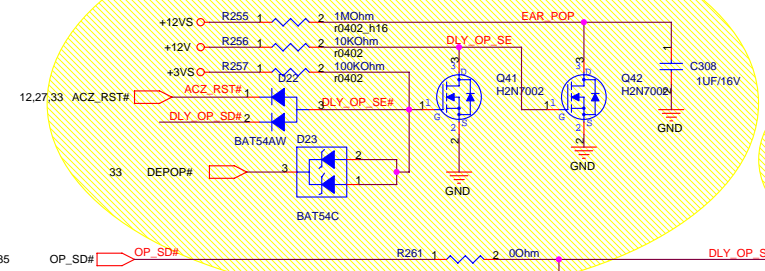
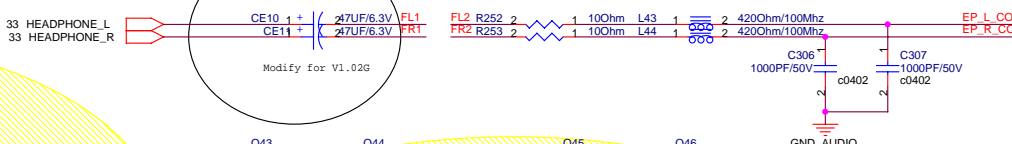
2.0G

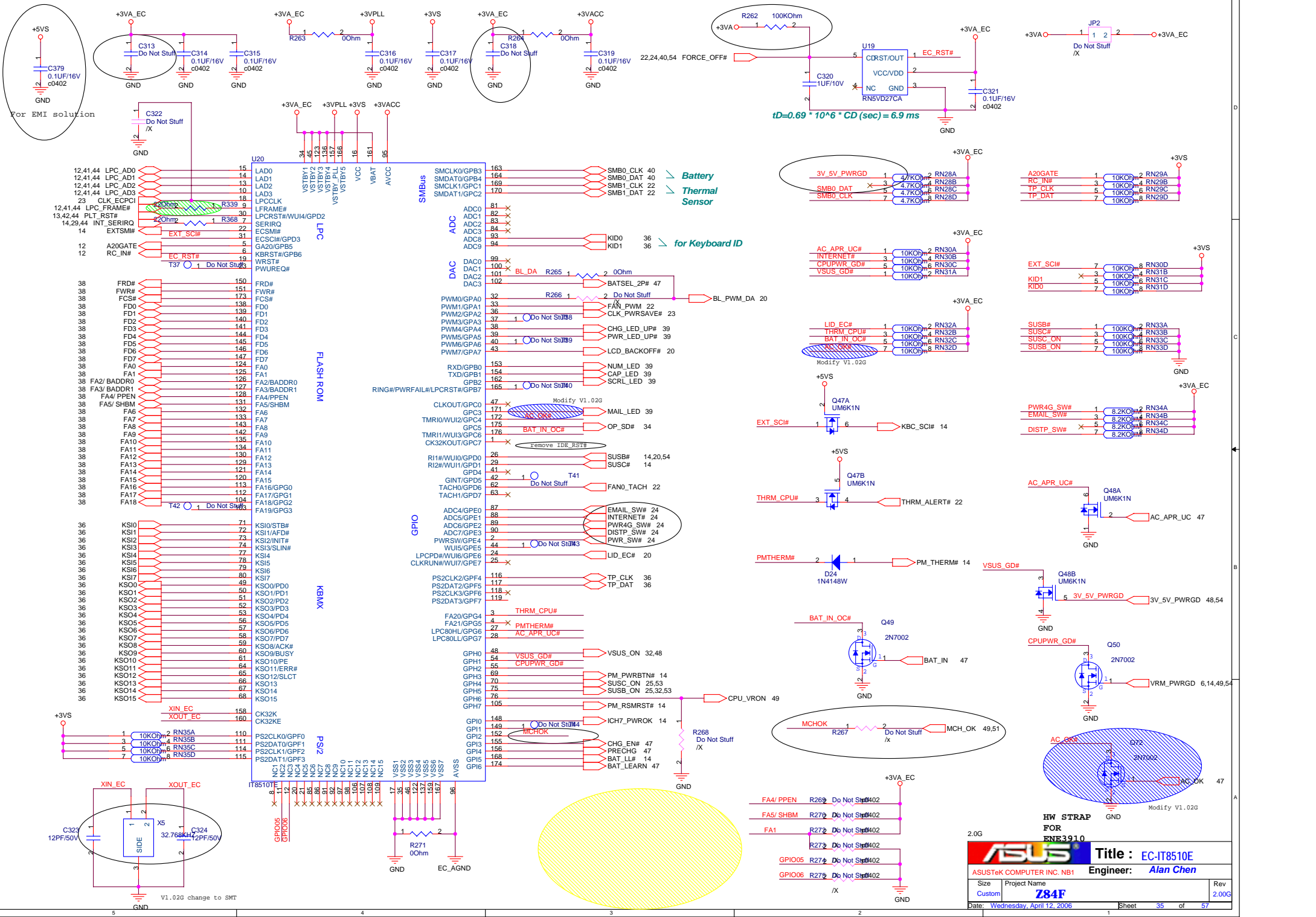




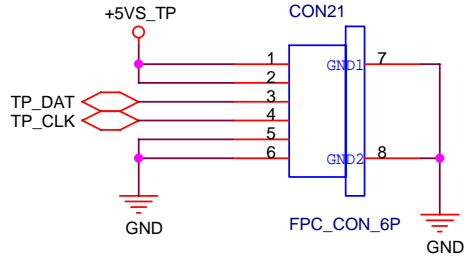
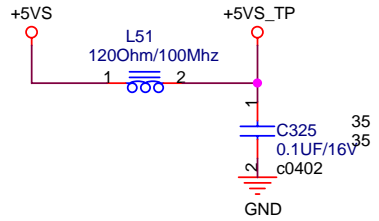
	Earphone	SPDIF	NC
AMP_SHDN#	Low	Low	High
OPTICAL_IN	Low	High	Low

For EMI solution



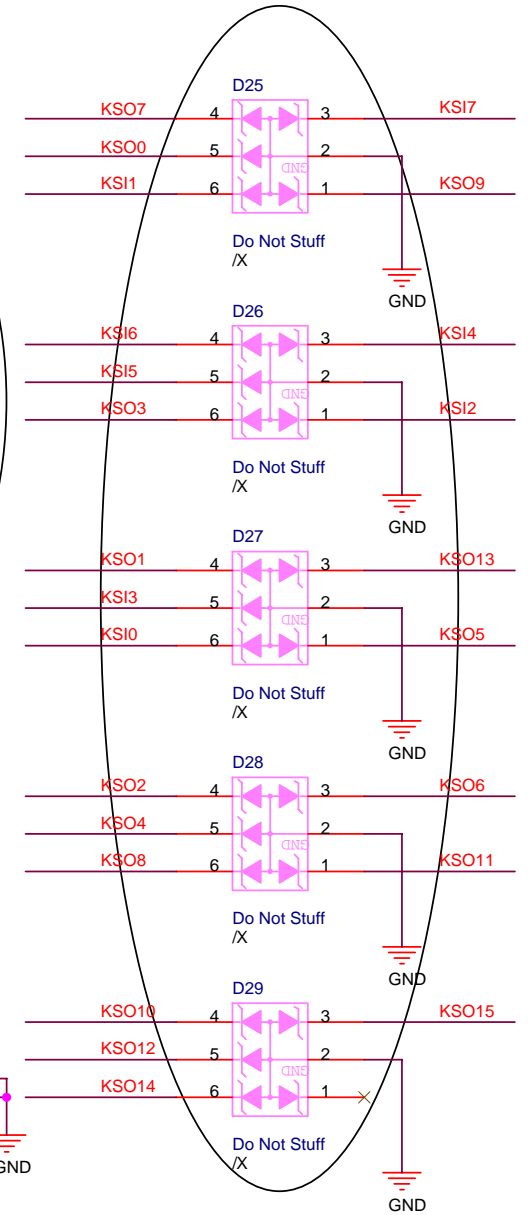
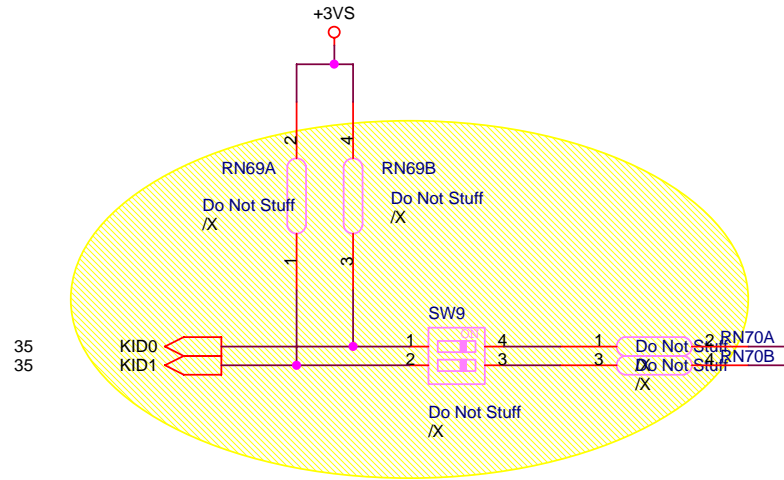
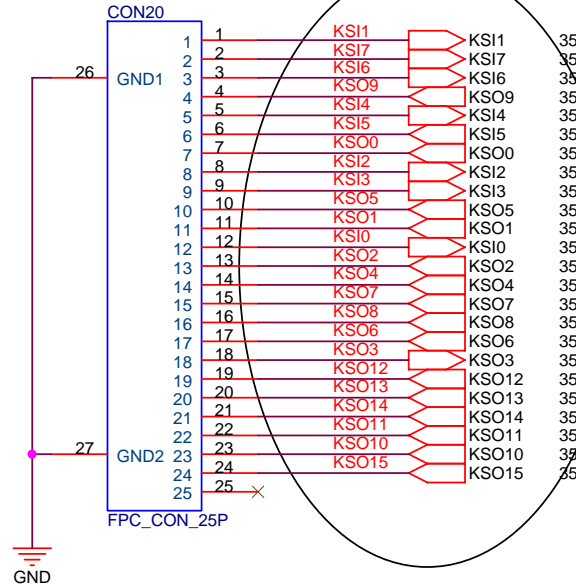


For Touch-Pad



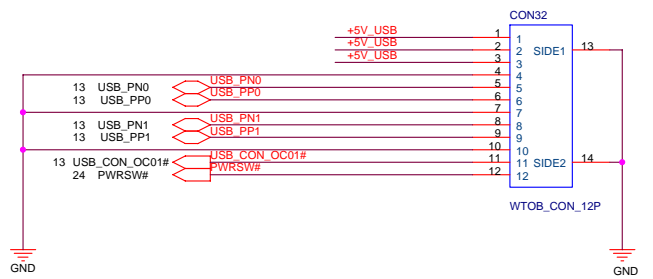
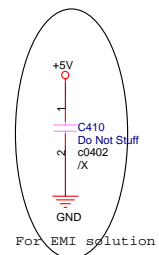
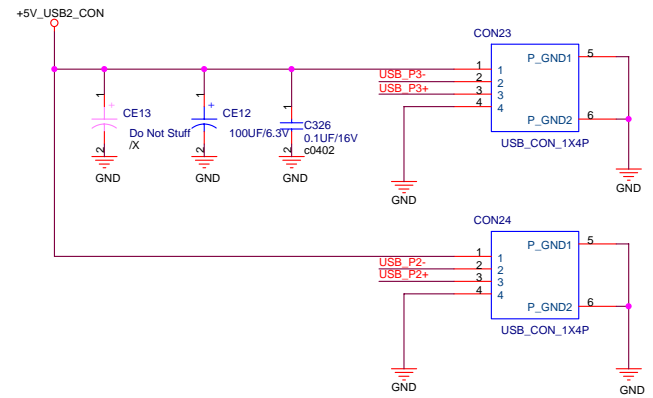
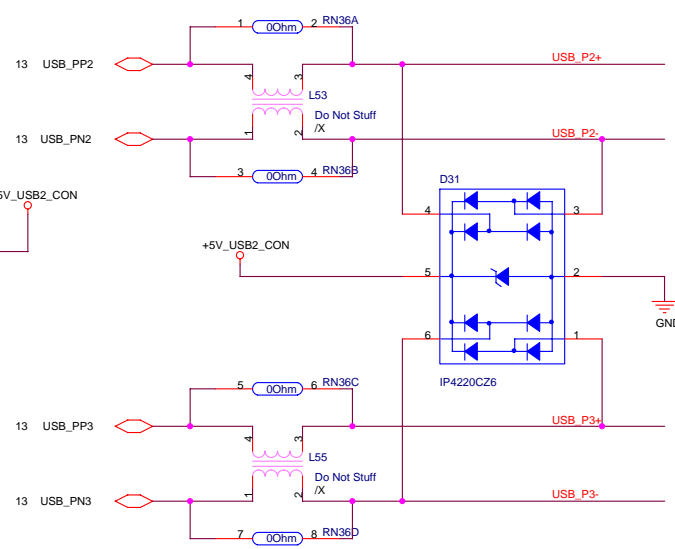
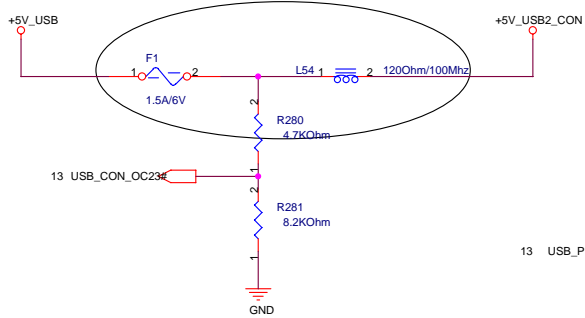
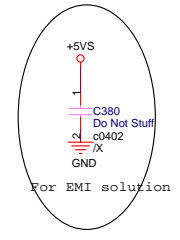
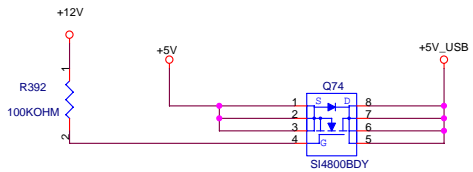
For Keyboard

For CBB -US- MATRIX



2.0G

		Title : Touch Pad & KB	
ASUSTeK COMPUTER INC. MB6		Engineer: ALAN CHEN	
Size A4	Project Name Z84F	Rev 2.00G	
Date: Friday, April 07, 2006		Sheet 36 of 57	

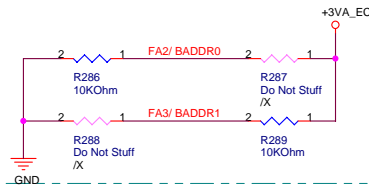


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

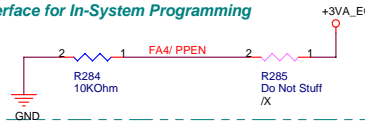
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

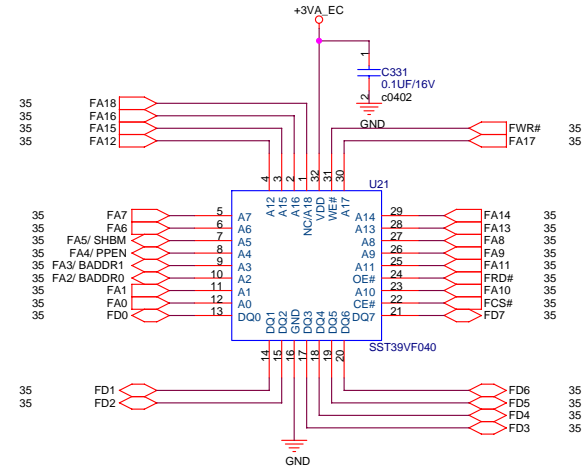
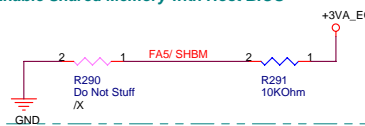
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

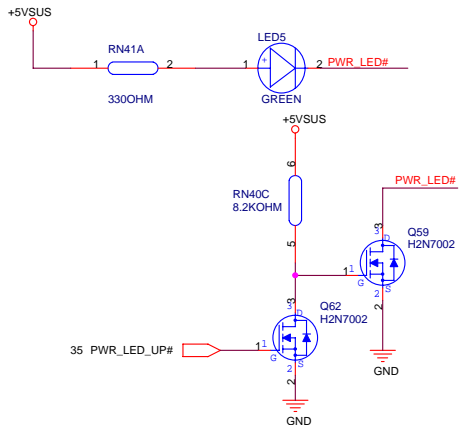
- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS



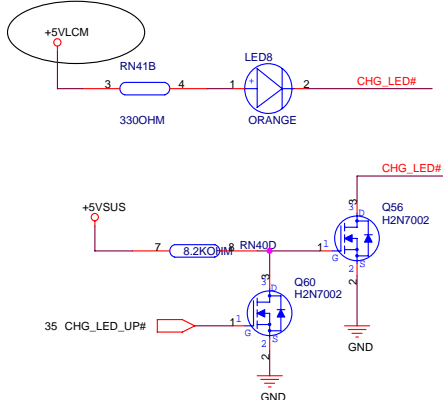
2.0G

For LED

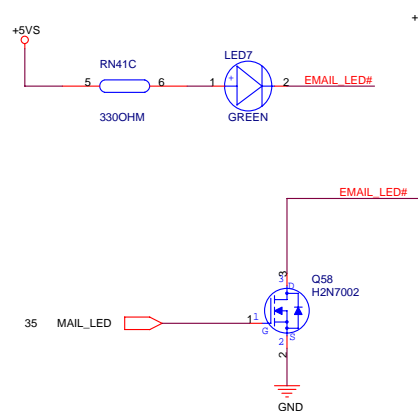
For POWER LED



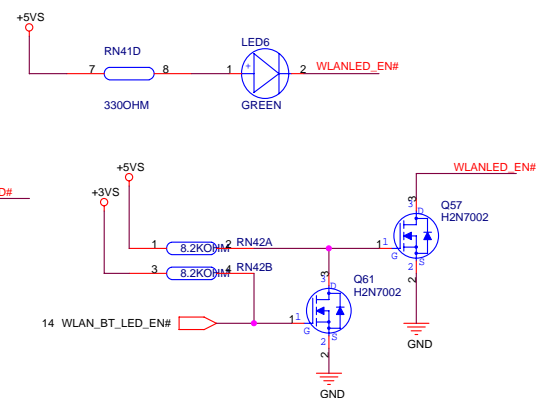
For BATTERY LED



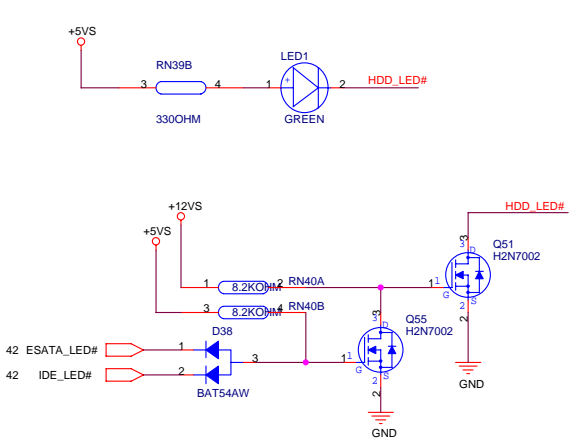
for EMIAL LED



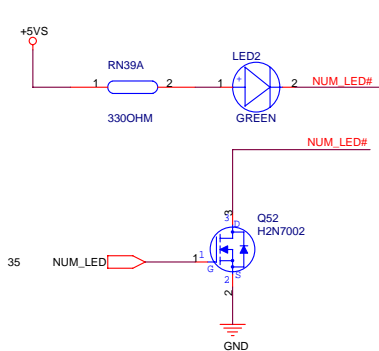
For WireLess LED



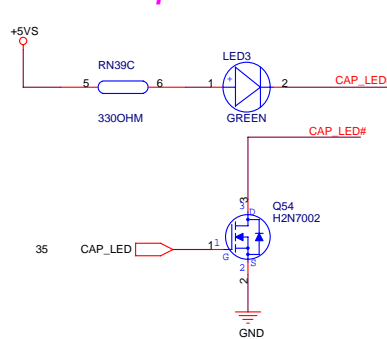
For ESATA/IDE LED



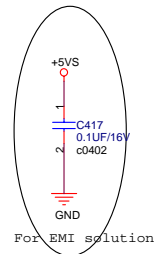
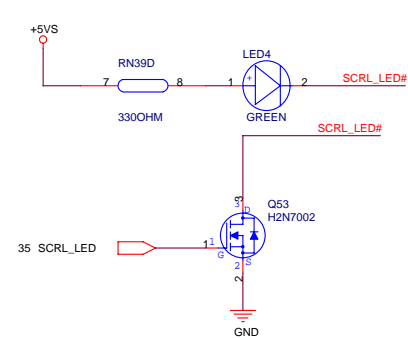
for Num Lock



for Cap. Lock



for Scroll Lock

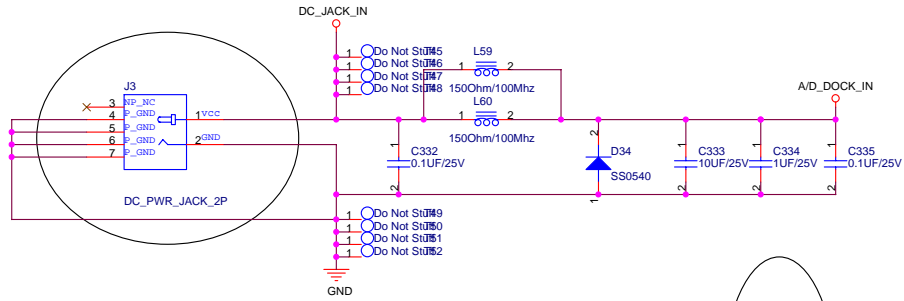


For EMI solution

2.0G

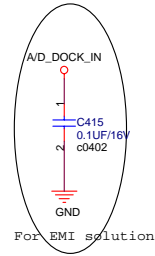
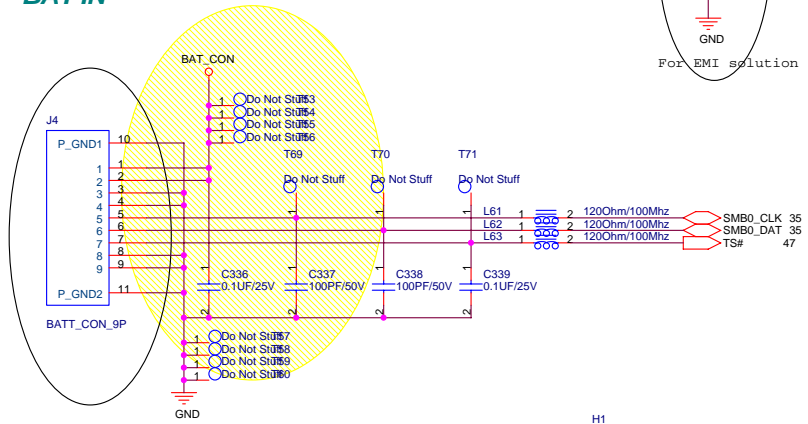
ASUS		Title : LED	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size Custom	Project Name Z84F	Rev 2.00G	
Date: Friday, April 07, 2006		Sheet 39 of 57	

DC IN

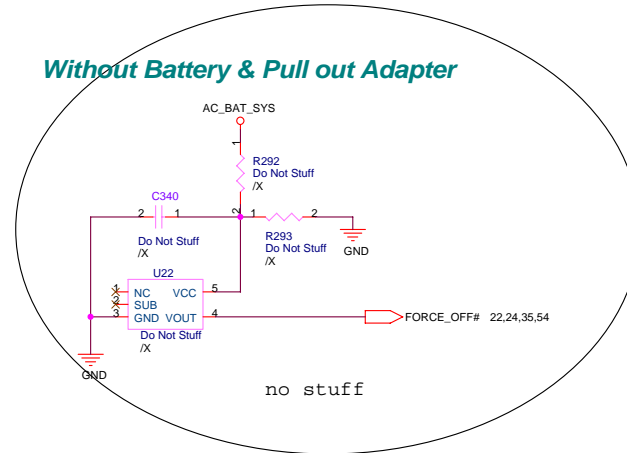


remove AC DC detect; no need

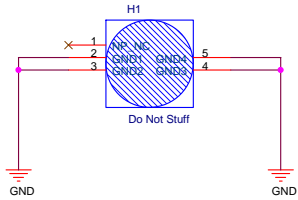
BAT IN



Without Battery & Pull out Adapter



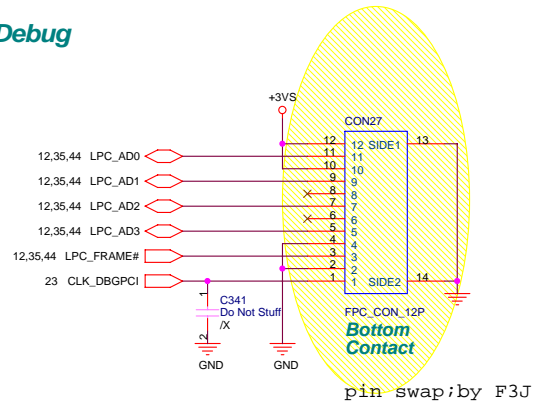
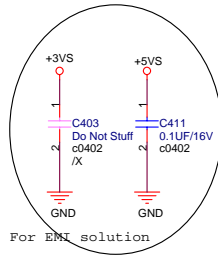
no stuff



2.0G

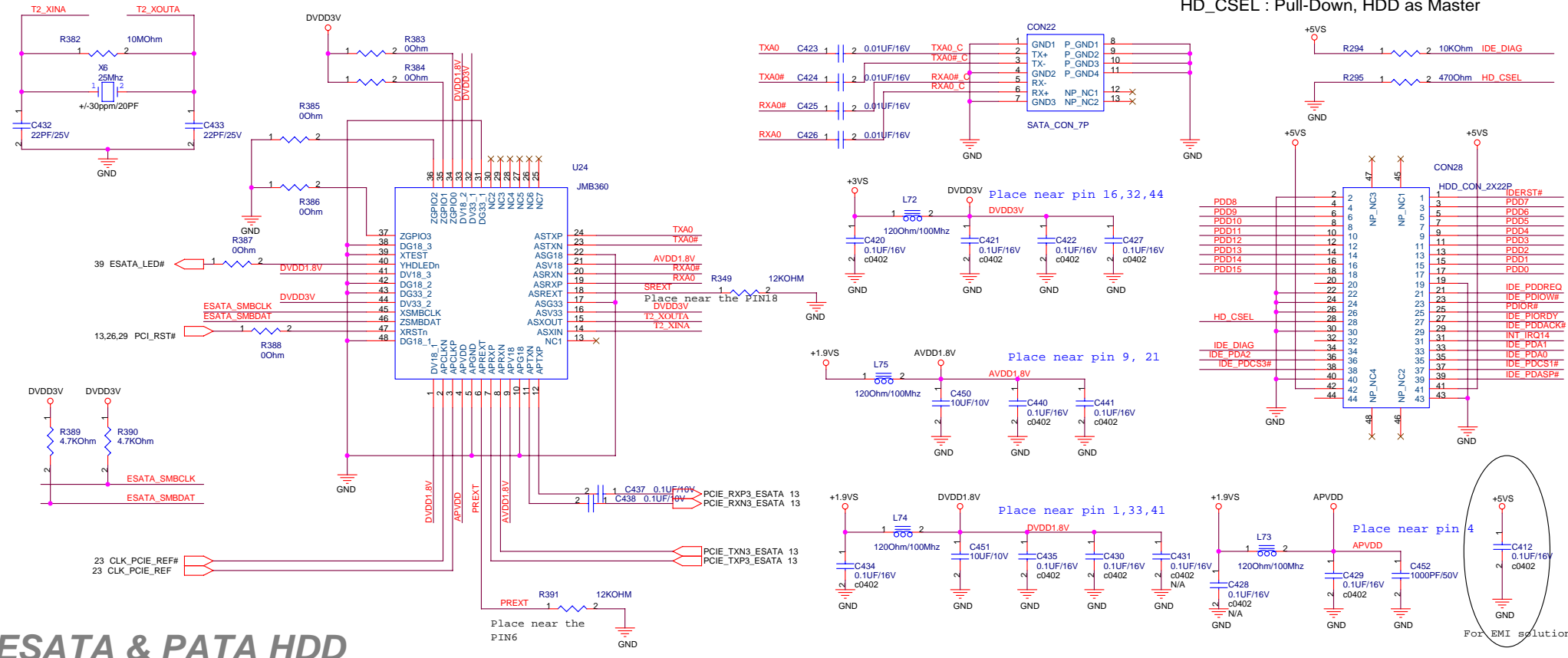
ASUS		Title : DC & BAT IN	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z84F	2.00G	
Date: Friday, April 07, 2006		Sheet 40 of 57	

For Debug

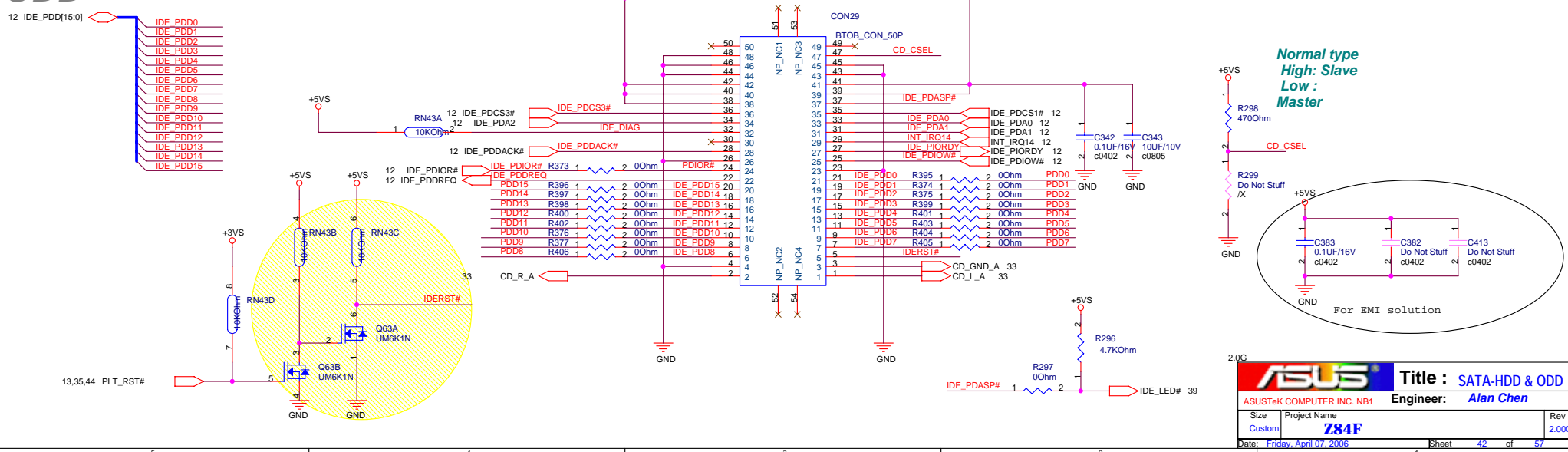


2.0G

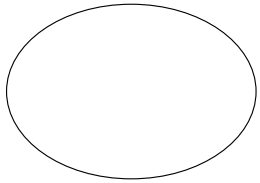
HD_CSEL : Pull-Down, HDD as Master



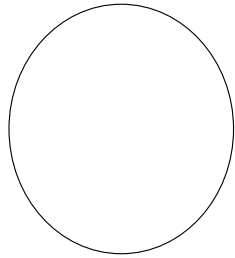
ESATA & PATA HDD



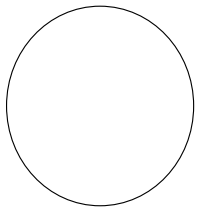
FOR LEFT UNDER



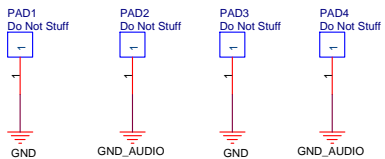
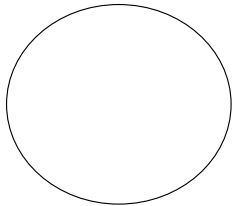
FOR FAN



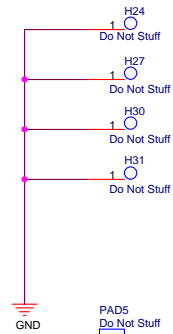
FOR RIGHT UP



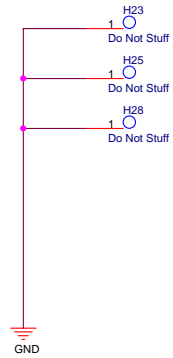
FOR FAN



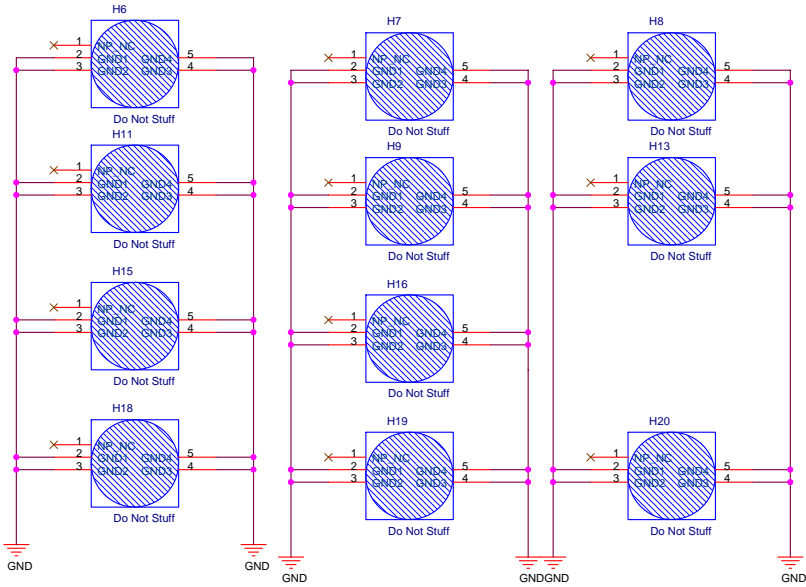
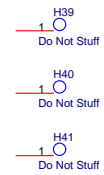
FOR CPU



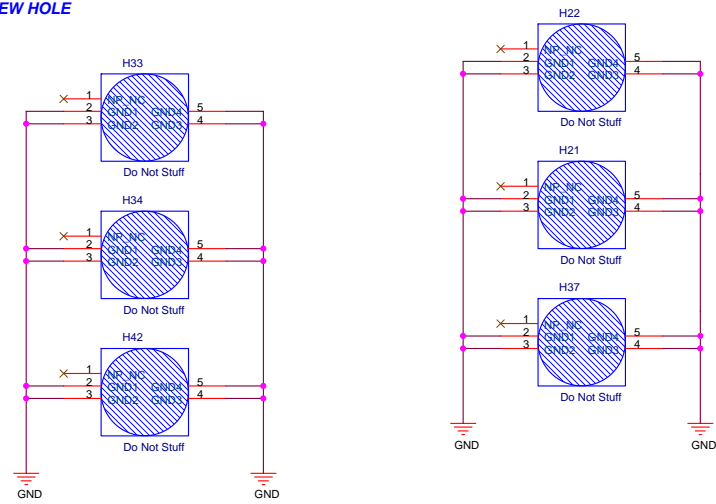
FOR VGA



Non pth hole

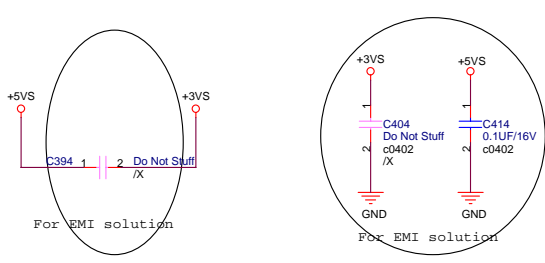
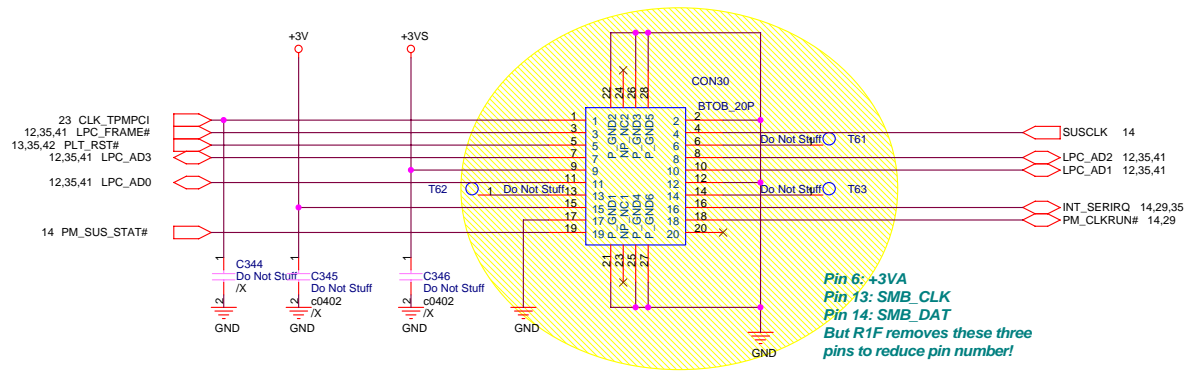


FOR SCREW HOLE

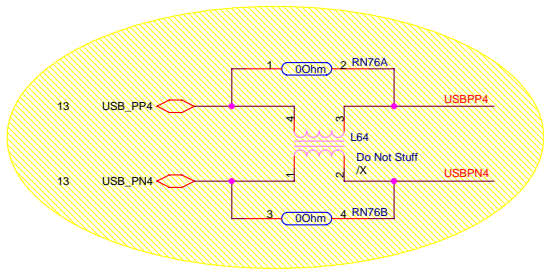
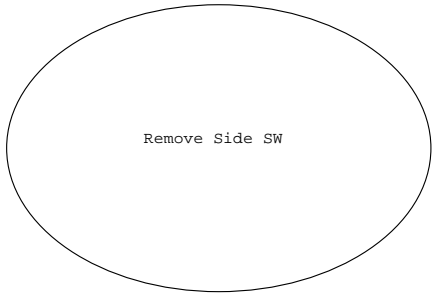
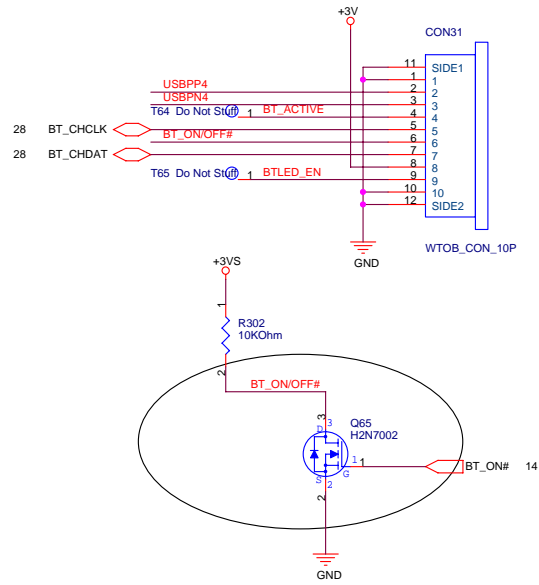


2.0G

For TPM Module

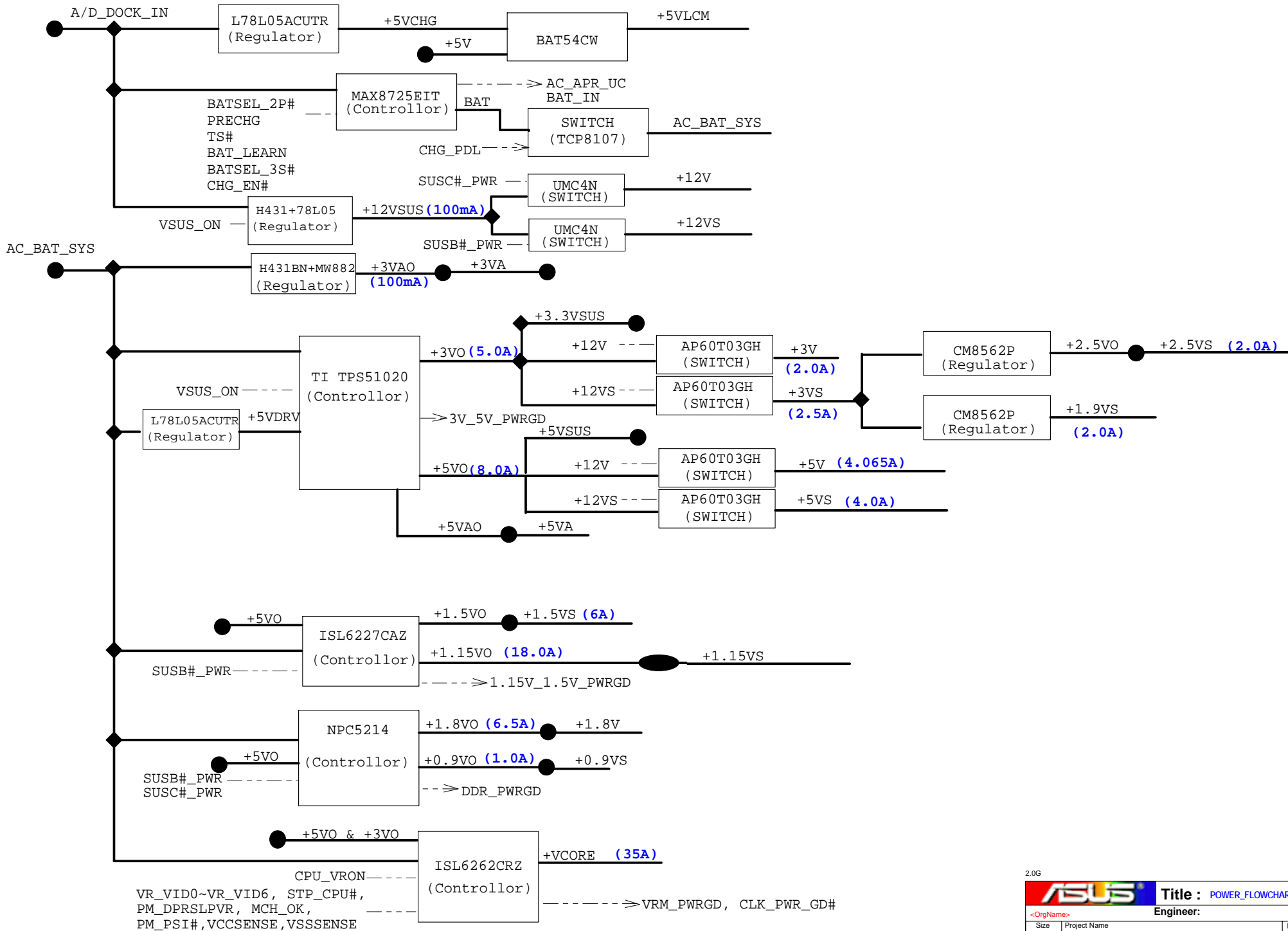


For Bluetooth



2.0G

ASUS		Title : Blue Tooth	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size Custom	Project Name Z84F	Rev 2.00G	
Date: Friday, April 07, 2006		Sheet 45 of 57	



Setting the Adaptor Input Current Limit
 Adaptor lin(max) = $[0.075V/Rsense(ADin)] * [VCLS/VREF]$
 VCLS = 2.865V
Adaptor Max. Current :
 PR5718=20K PR5714 = 178K, Ilimit = 4.5A; 90W
 PR5718=27K PR5714 = 47K, Ilimit = 3.175A; 60W

Setting the Charge Voltage
 $V_{batt} = Cell * \{ Vref + [(VCTL - 1.8V) / 9.52] \}$
 VCTL = 1.588V => Vbatt = 4.2V

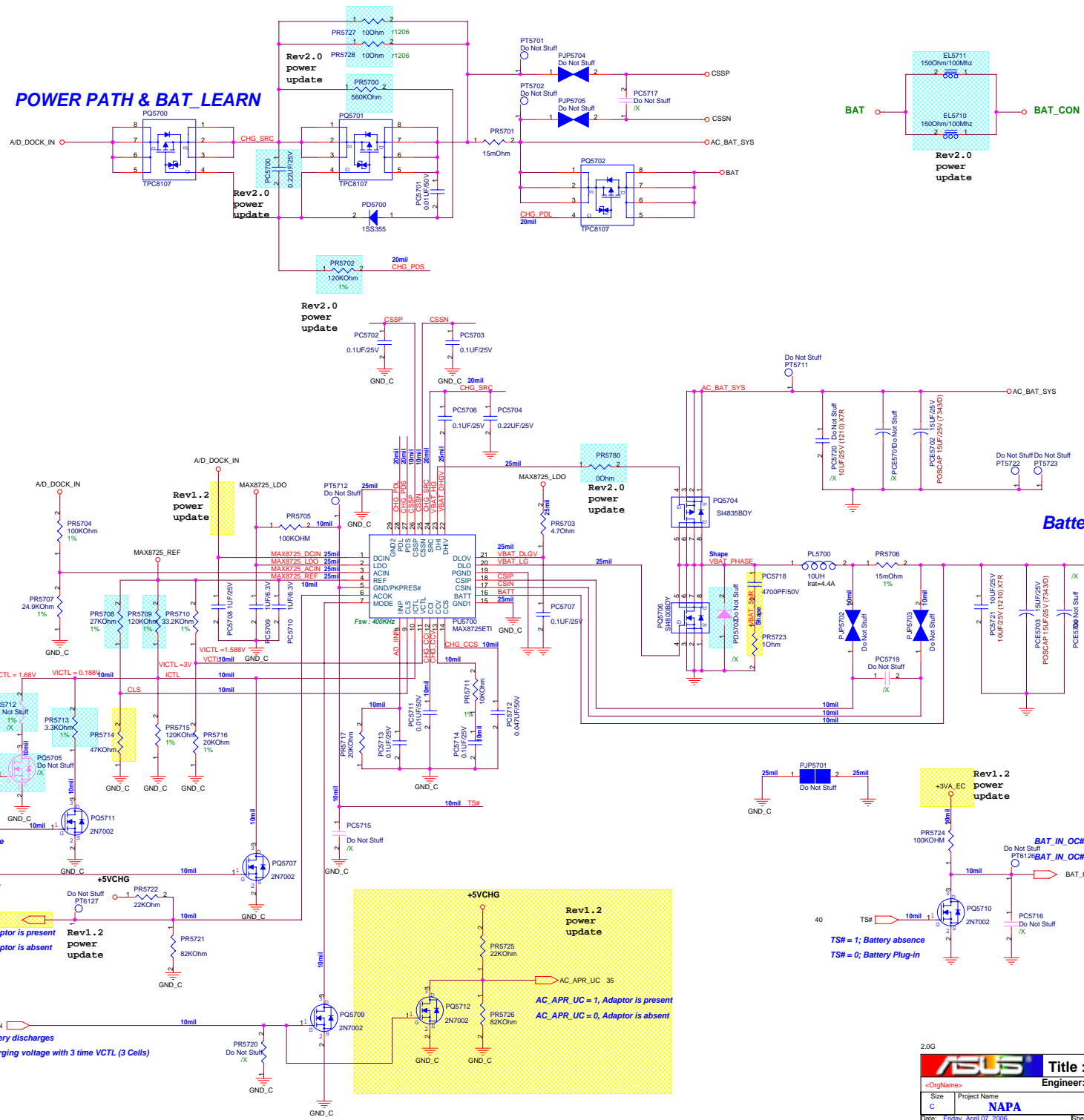
Setting the Charge Current
 Charge Current Ichg = $[0.075V/Rsense(CHG)] * [VICTL/3.6V]$
 Rsense(CHG) = 15m Ohm
Pre-Charging Mode :
 Precharging current = 148 ~ 152mA
 Vctl = 0.107V ~ 0.109V

Battery Cell Selection :
 BATSEL_2P# = 1, 3 Cells; Vctl = 2.084V
 => Icharge = 1.6933A
 BATSEL_2P# = 0, 6 or 9 Cells; Vctl = 2.111V
 => Icharge = 2.9329A

Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells
 0.8 > Vmode (try to GND) ----> Learning mode
 VICTL < 0.8V or DCIN < 7V --> Charger Disable

MAX8725_REF : 4.2235V
 MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN



Battery Voltage

35 BATSEL_2P#
 BATSEL_2P# = 1, 3 Cells
 BATSEL_2P# = 0, 6 or 9 Cells

35 PRECHG
 PRECHG = 1, Pre-Charging Mode
 Charging Current = 156mA

35 CHG_EN#
 CHG_EN# = 1, Charger Disabled
 CHG_EN# = 0, Charger Enabled

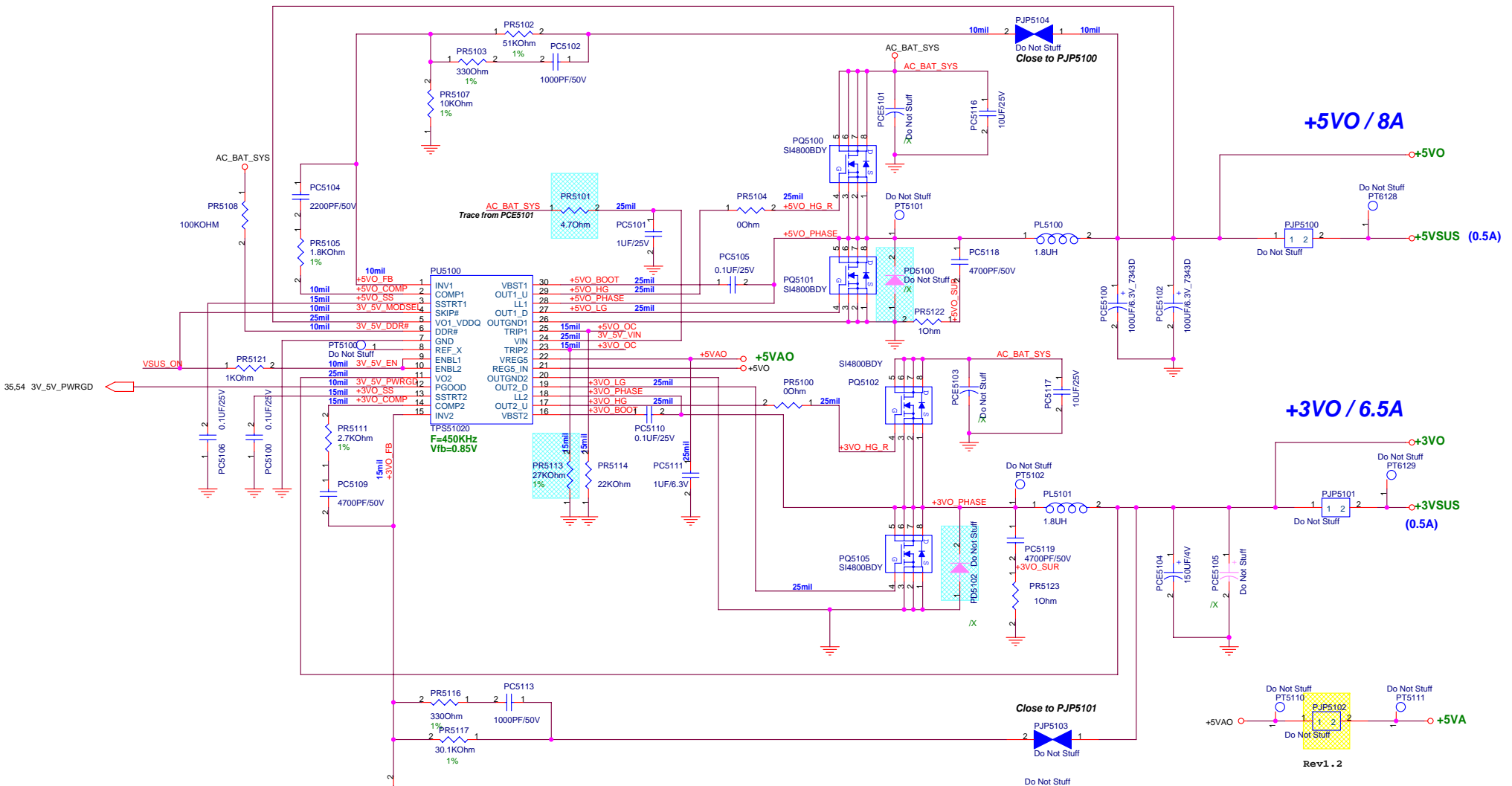
35 AC_OK
 AC_OK = 1, Adaptor is present
 AC_OK = 0, Adaptor is absent

35 BAT_LEARN
 BAT_LEARN = 1, Battery discharges
 BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

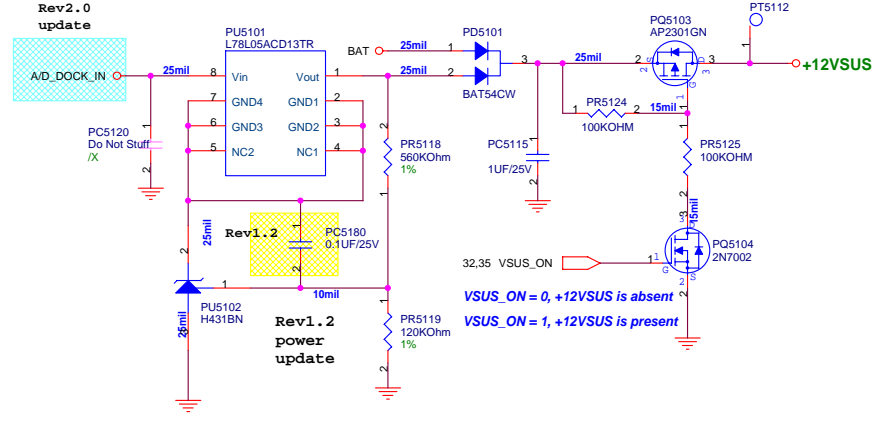
35 +3VA_EC
 Rev1.2 power update

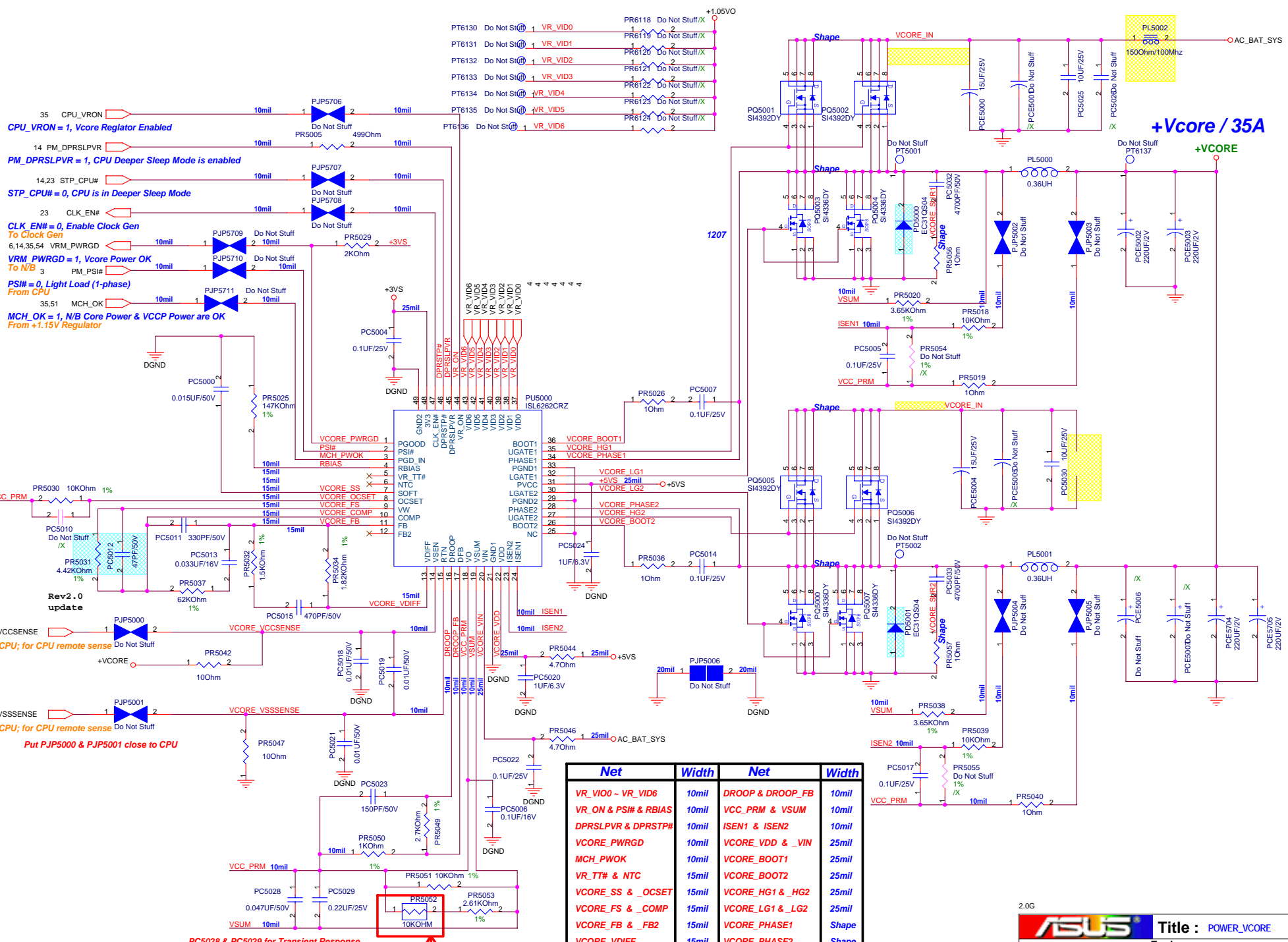
40 TSH#
 TSH# = 1; Battery absence
 TSH# = 0; Battery Plug-in

BAT_IN_OCH# = 1; Battery absence
 BAT_IN_OCH# = 0; Battery Plug-in



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil





35 CPU_VRON \Rightarrow 10mil \Rightarrow PJP5706 \Rightarrow 10mil

CPU_VRON = 1, Vcore Regulator Enabled

14 PM_DPRSPLPVR \Rightarrow 10mil \Rightarrow PJP5707 \Rightarrow 10mil

PM_DPRSPLPVR = 1, CPU Deeper Sleep Mode is enabled

14,23 STP_CPU# \Rightarrow 10mil \Rightarrow PJP5708 \Rightarrow 10mil

STP_CPU# = 0, CPU is in Deeper Sleep Mode

23 CLK_EN# \Rightarrow 10mil \Rightarrow PJP5709 \Rightarrow 10mil

CLK_EN# = 0, Enable Clock Gen To Clock Gen

6,14,35,54 VRM_PWRGD \Rightarrow 10mil \Rightarrow PJP5710 \Rightarrow 10mil

VRM_PWRGD = 1, Vcore Power OK To N/B

35,51 MCH_OK \Rightarrow 10mil \Rightarrow PJP5711 \Rightarrow 10mil

PS# = 0, Light Load (1-phase) From CPU

MCH_OK = 1, N/B Core Power & VCCP Power are OK From +1.15V Regulator

VCC_PRM 10mil

From CPU; for CPU remote sense

VSSsense 10mil

From CPU; for CPU remote sense

Put PJP5000 & PJP5001 close to CPU

PC5028 & PC5029 for Transient Response

Close to Phase 1 Inductor

Net	Width	Net	Width
VR_VID0 - VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PS# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSPLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCsense	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSsense	10mil	AC_BAT_SYS	Shape

2.0G

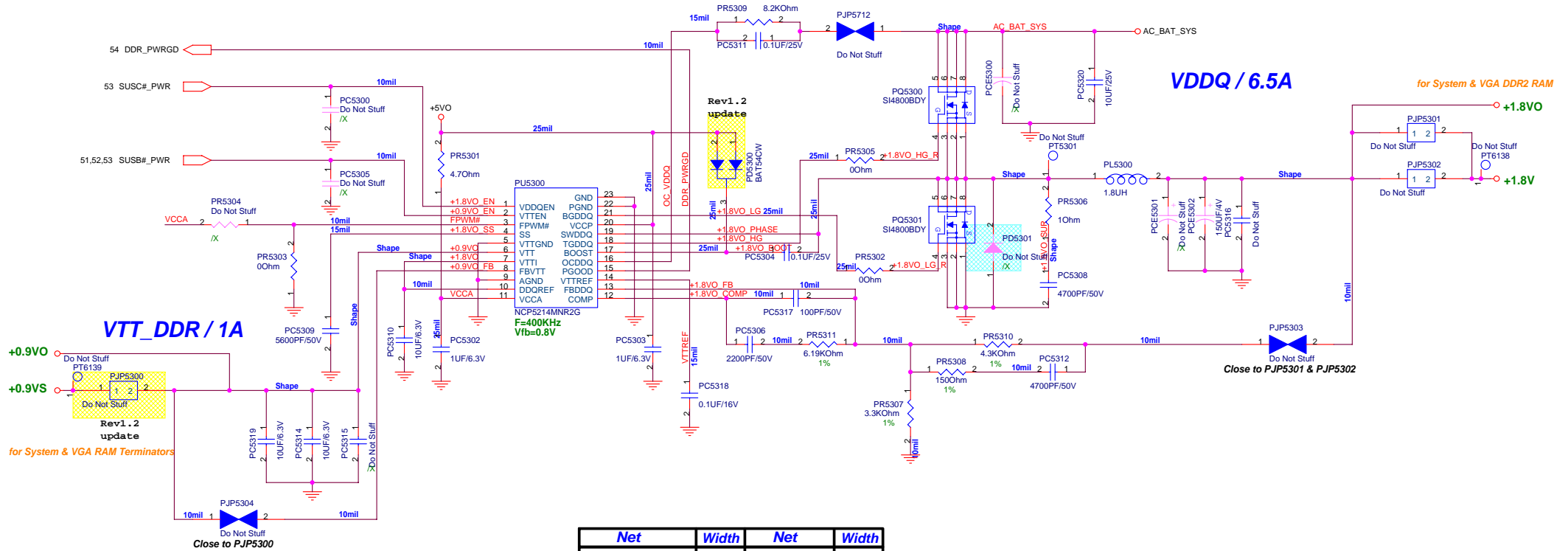
ASUS Title : POWER_VCORE

Engineer: _____

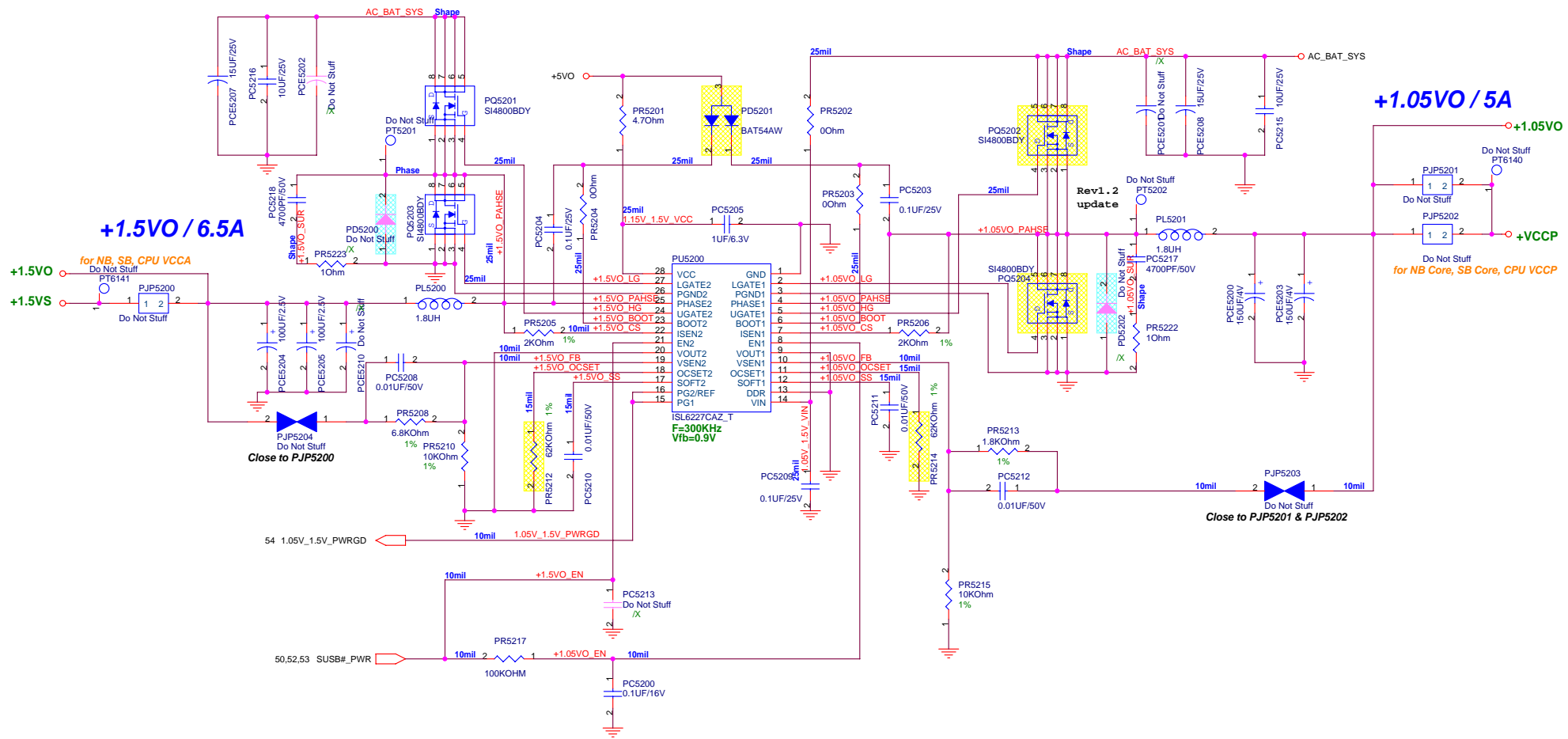
Size: _____ Project Name: _____ Rev: 2.00G

Custom: **NAPA**

Date: Friday, April 07, 2006 Sheet 49 of 57



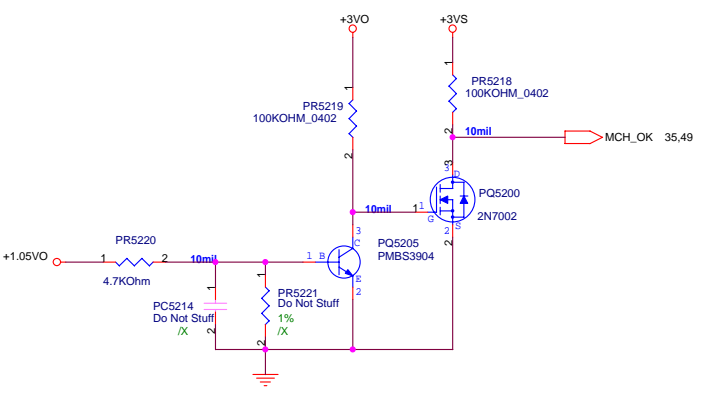
Net	Width	Net	Width
+1.8V0_EN	10mil	+1.8V0_BOOT	25mil
+1.8V0	Shape	+1.8V0_COMP	10mil
+0.9V0_EN	10mil	+1.8V0_HG_R	25mil
+0.9V0	Shape	+1.8V0_LG_R	25mil
+0.9V0_FB	10mil	+1.8V0_HG	25mil
+1.8V0 -> DDQREF	10mil	+1.8V0_LG	25mil
VTTREF	15mil	+1.8V0_PHASE	Shape
FPWM#	10mil	+1.8V0_SUR	Shape
VCCA	10mil	+1.8V0_FB	10mil
DDR_PWRGD	10mil	+1.8V0_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

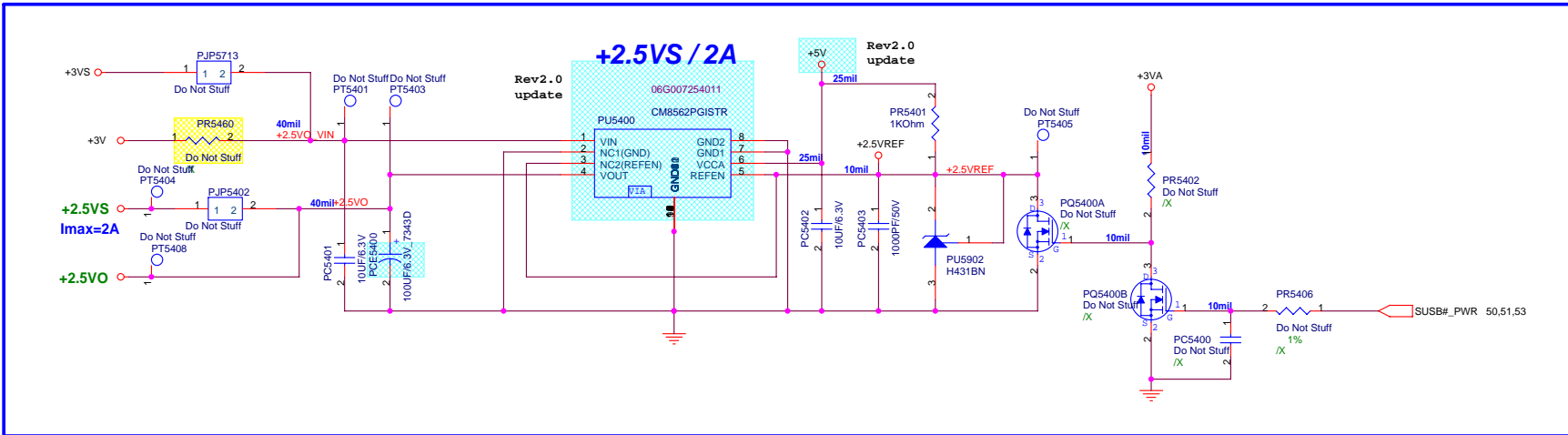
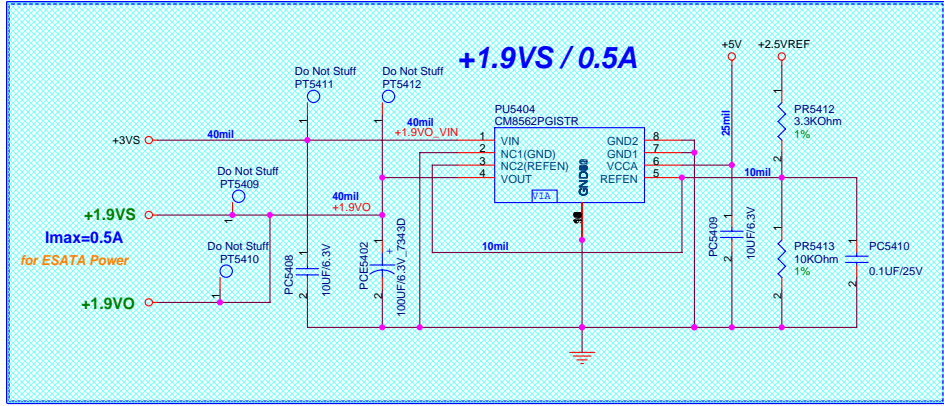
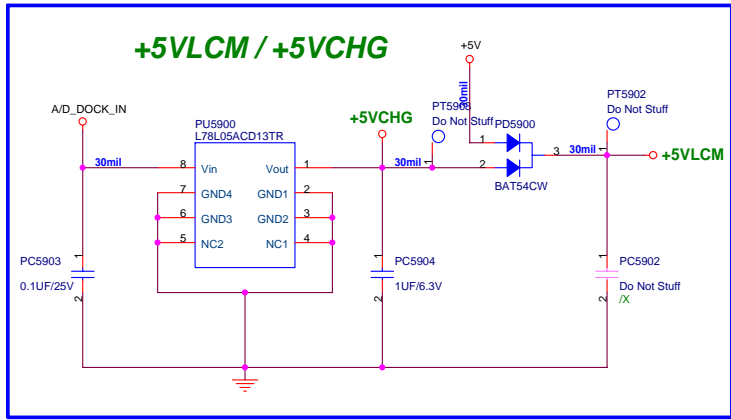
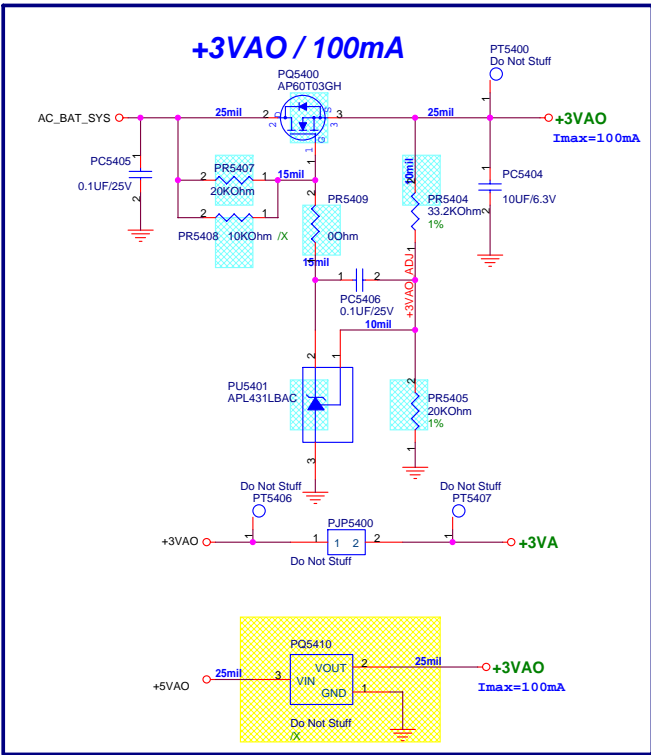


+1.5VO / 6.5A

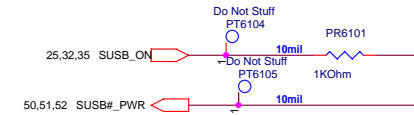
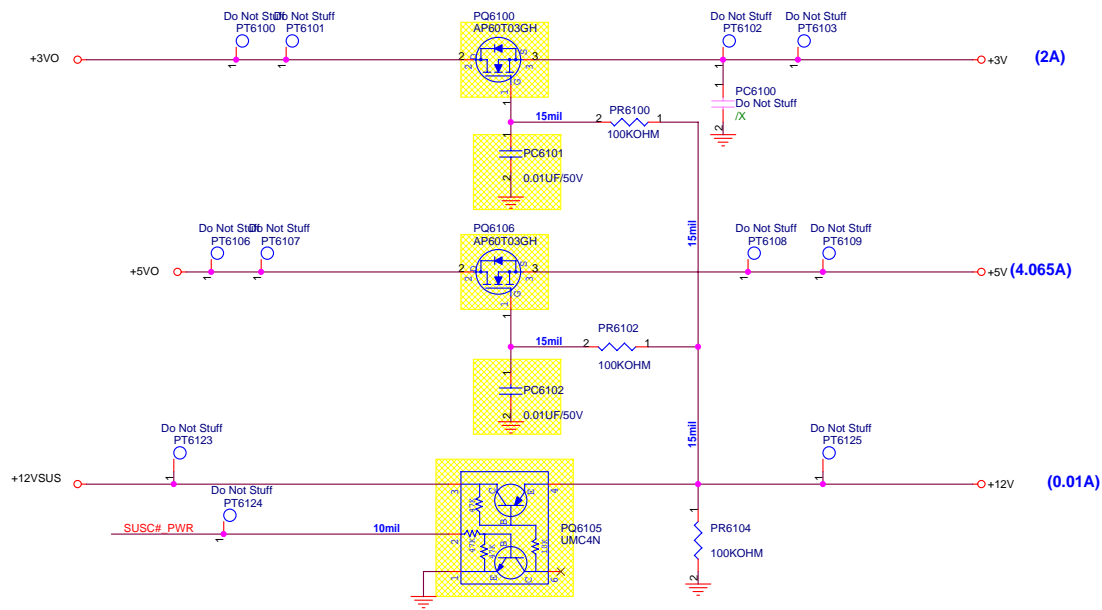
+1.05VO / 5A

Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

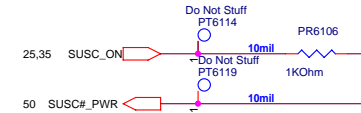
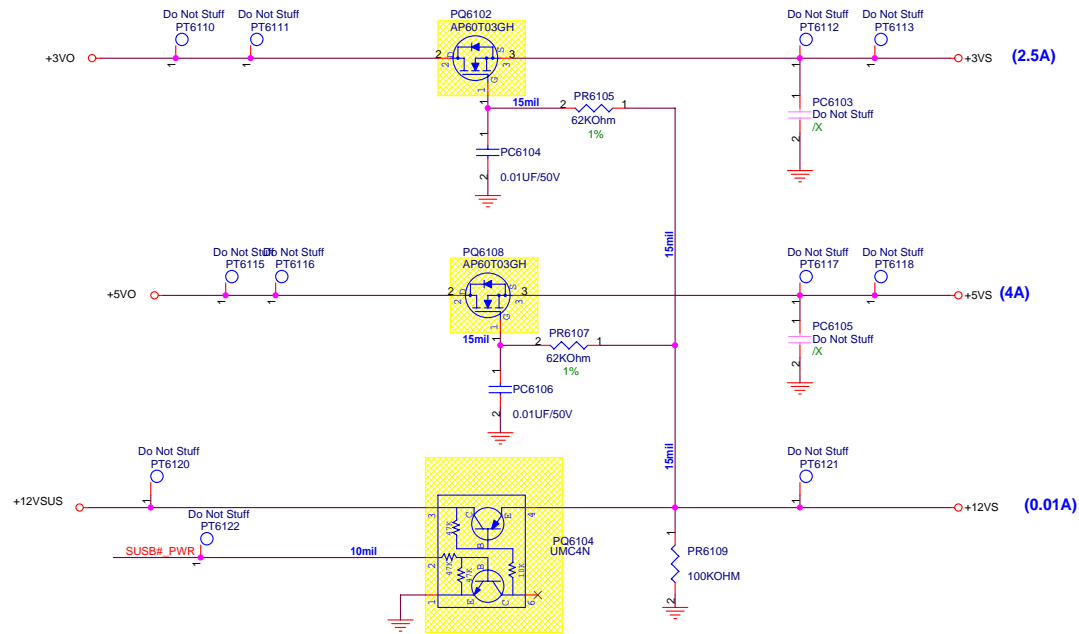




SUSC#_PWR POWER



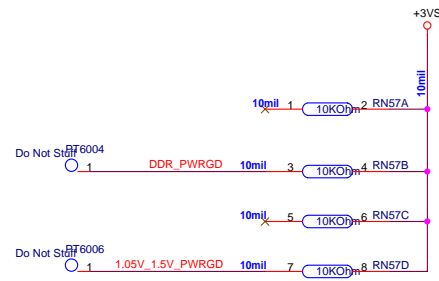
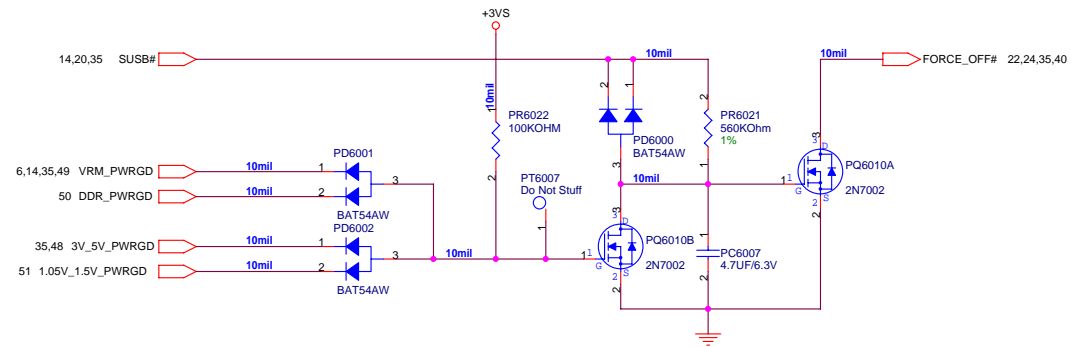
SUSB#_PWR POWER



2.0G

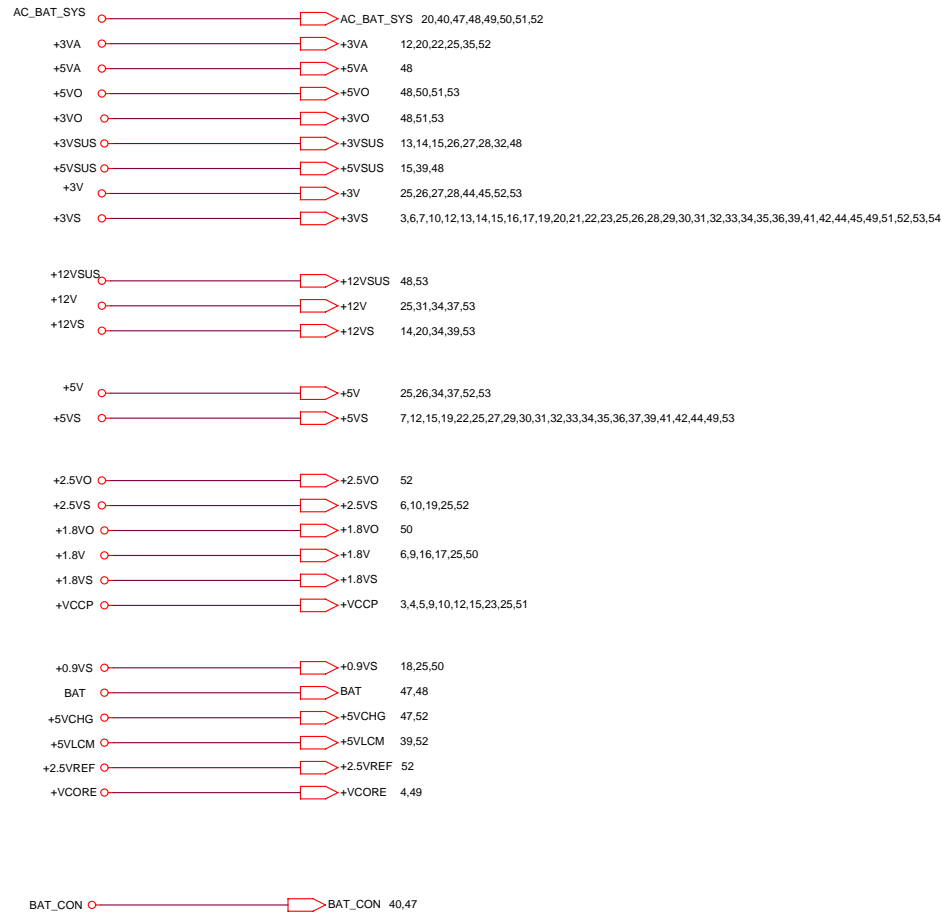
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<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.00G	
Date: Fnday, April 07, 2006		Sheet	53 of 57

Power Good Detector



2.0G

		Title : POWER_PROTECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.00G	
Date: Friday, April 07, 2006		Sheet	54 of 57



2.0G

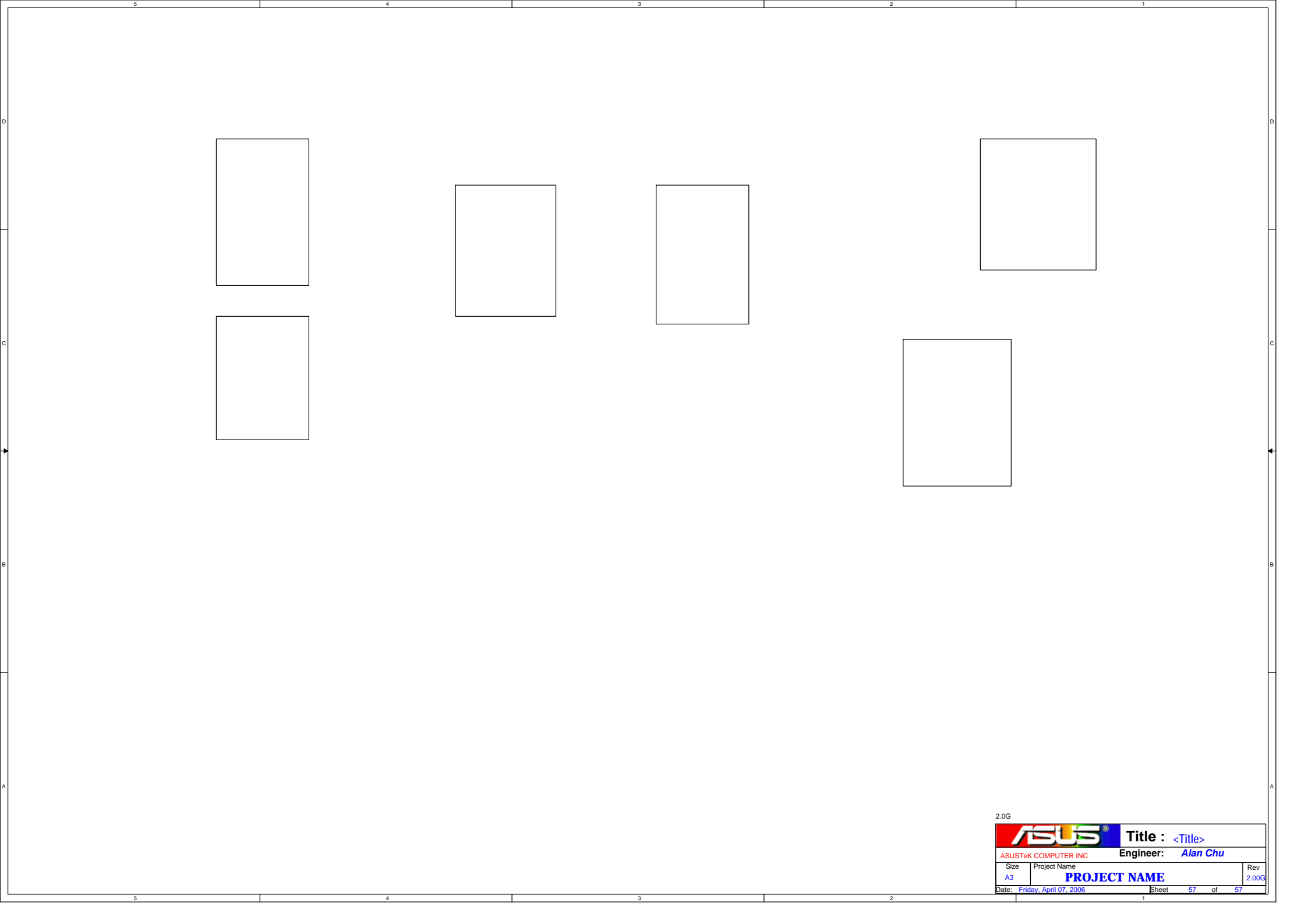
		Title : POWER_SIGNAL	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.0G	
Date: Friday, April 07, 2006		Sheet	55 of 57

Rev	Date	Description
1.0	10/04/05	1. Initial release.
2.0	03/27/06	1.EE Change U24 E-SATA Chip (Sil3132) to JMB360 <P42>
2.0	03/27/06	2.R60 10Mohm from /N change to load for 32.768KHz issue<P12>
2.0	03/27/06	3.R210 0Ohm from load change to /N for Card Reader PME# issue<P29>
2.0	03/27/06	4.Add D38 Diode for E_SATA LED<P39>
2.0	03/29/06	5.Modify CON14 pindefine for MS card can't detect issue<P31>
2.0	03/27/06	6.EE Change U11 LAN Chip from RTL8110SBL to RTL8110SCL<P26>
2.0	03/27/06	7.ME change SW2, SW3, SW4, SW5 type<P24>P/N:12G09103004P
2.0	03/27/06	8.ME change CON3 CRT connector color<P19>
2.0	03/28/06	9.Add Q74 MOSFET for USB protect MOSFET<P37>
2.0	03/27/06	10.Add R381 0 Ohm for LAN AVDDL Power select<P27>
2.0	03/27/06	11.Add CE13 100uF/6.3Vfor USB Droop issue<P37>
2.0	03/27/06	12.ME change CON32 from 10pin to 12pin <P37>
2.0	03/29/06	13.R75 from 22.6 ohm change to 20 ohm for USB Eye diagram issue<P13>
2.0	03/30/06	14.EMI Add C453,RC454,C455,C456 1000pF for EMI Solution <P34>
2.0	03/30/06	15.Keyboard switch BOM delete for software control<P36>
2.0	03/30/06	16.Delete Q1 and change net name from VRMPWRGD to VRM_PWRGD for Power sequence<P14>.
2.0	03/30/06	17.EMI add C457 100pF <H_CPURST# to GND> for EMI Solution <P3>
2.0	04/03/06	18.CN9要上1000PF的排容 for EMI Solution <P24>
2.0	04/03/06	19.預留一顆0402SIZE 100PF C459的電容 BUF_PLT_RST#對地 for EMI Solution <P13>
2.0	04/03/06	20.預留一顆0402SIZE 100PF C460的電容 PCL_RST#對地 for EMI Solution <P13>
2.0	04/03/06	21.預留一顆0402SIZE 100PF C458的電容 H_DPRSTP#對地 for EMI Solution <P3>
2.0	04/03/06	22.預留一顆0402SIZE 100PF C461的電容 ACZ_RST#對地 for EMI Solution <P27>
2.0	04/04/06	23.SW10 connect from SYS_RST# change to FORCE_OFF# for Marking spac <P24>
2.0	04/04/06	24.EMI add some resister on HDD signal for EMI solution<P42>
2.0	04/04/06	25.TV Conector Con6_pin7 from cvbs_con connect to GND for S-Video Spec <P21>
2.0	04/04/06	26.Add C51,C71 22uF,1uF Cap. for TV 水波紋issue<P10>
2.0	04/04/06	27.EMI add some cap. VCORE to GND for EMI solution<P3>
2.0		
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Rev	Date	Description

2.0G

		Title : History	
ASUSTek COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
Custom	Z96J	2.00G	
Date: Friday, April 07, 2006		Sheet 56 of 57	



2.0G

		Title : <Title>	
ASUSTeK COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
A3	PROJECT NAME	2.00G	
Date: Friday, April 07, 2006		Sheet 57 of 57	