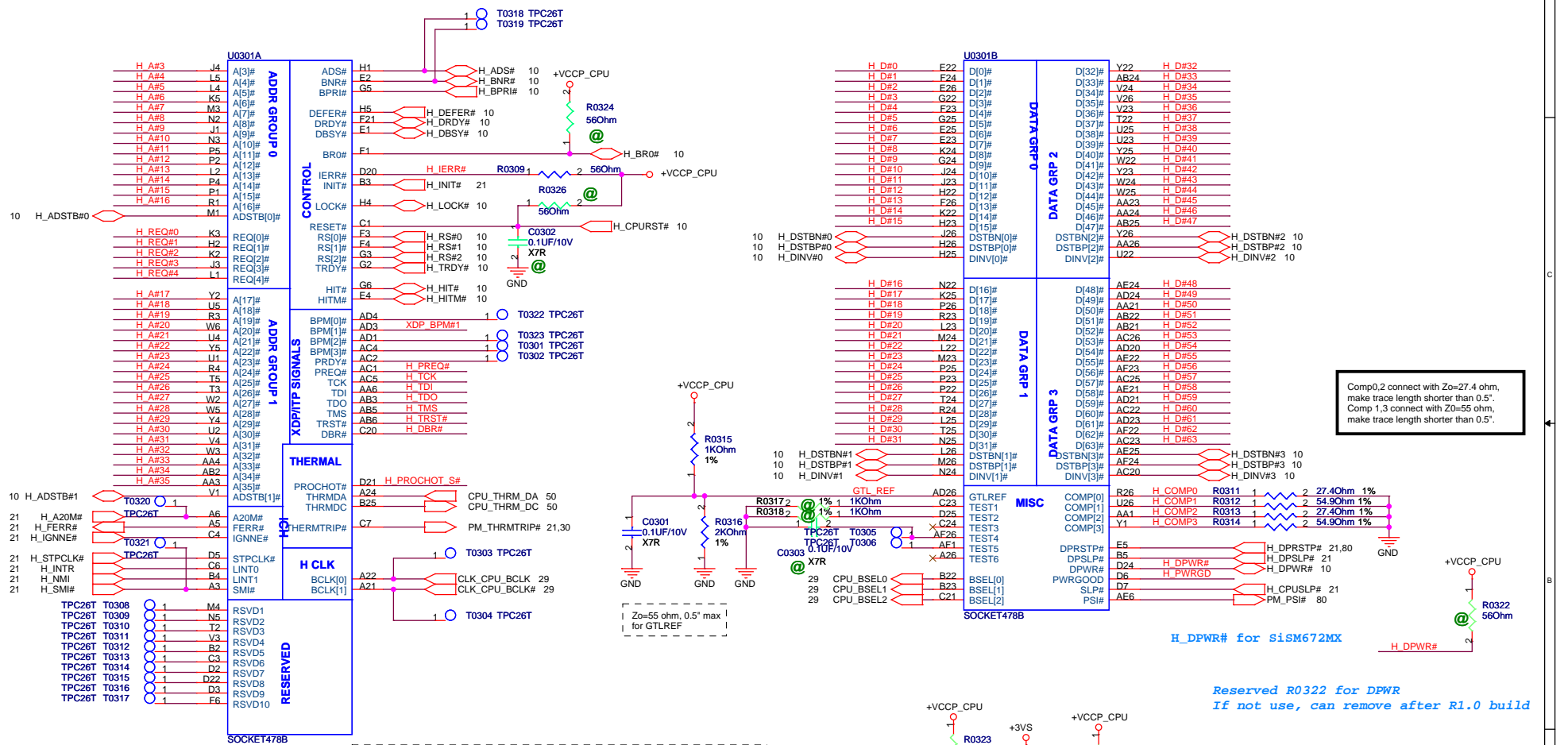


Power On Sequence
1 → 19

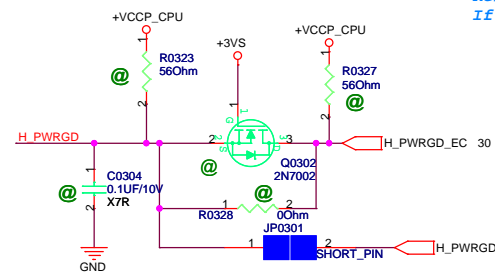
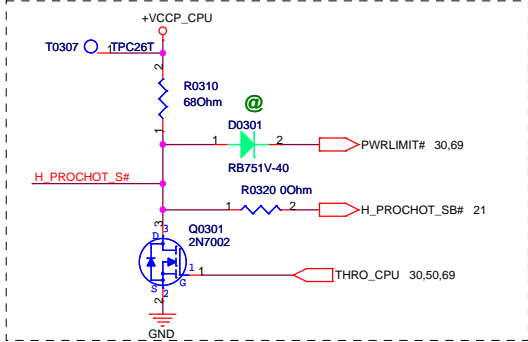
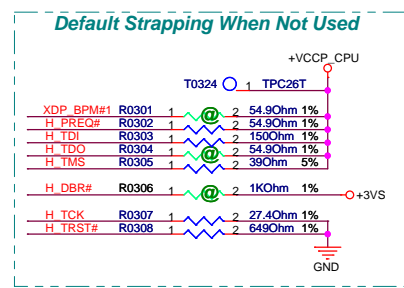


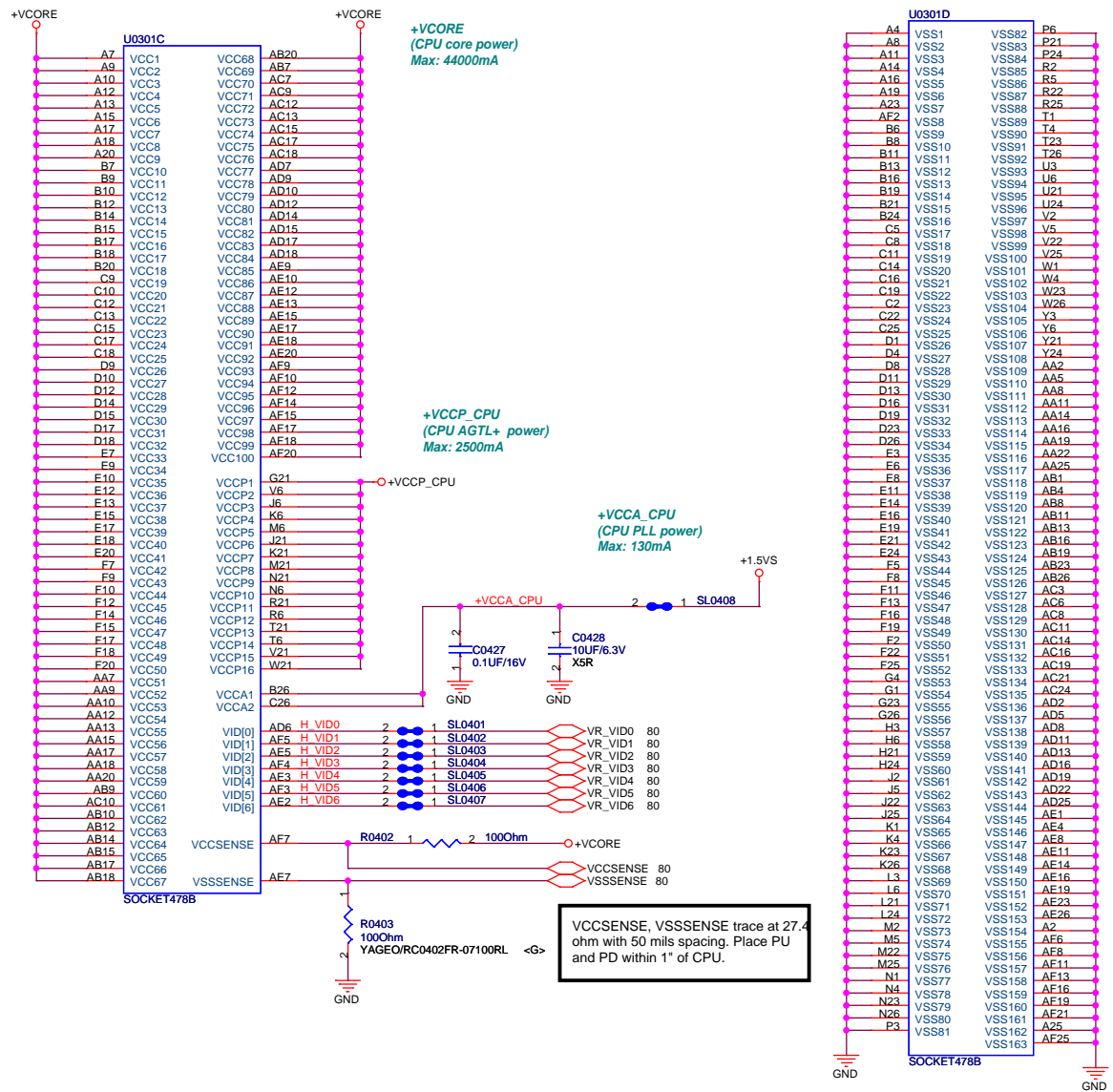
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Zo=55 ohm, 0.5" max for GTLREF

H_DPWR# for SISM672MX

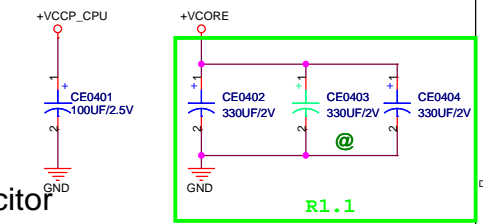
Reserved R0322 for DPWR
 If not use, can remove after R1.0 build



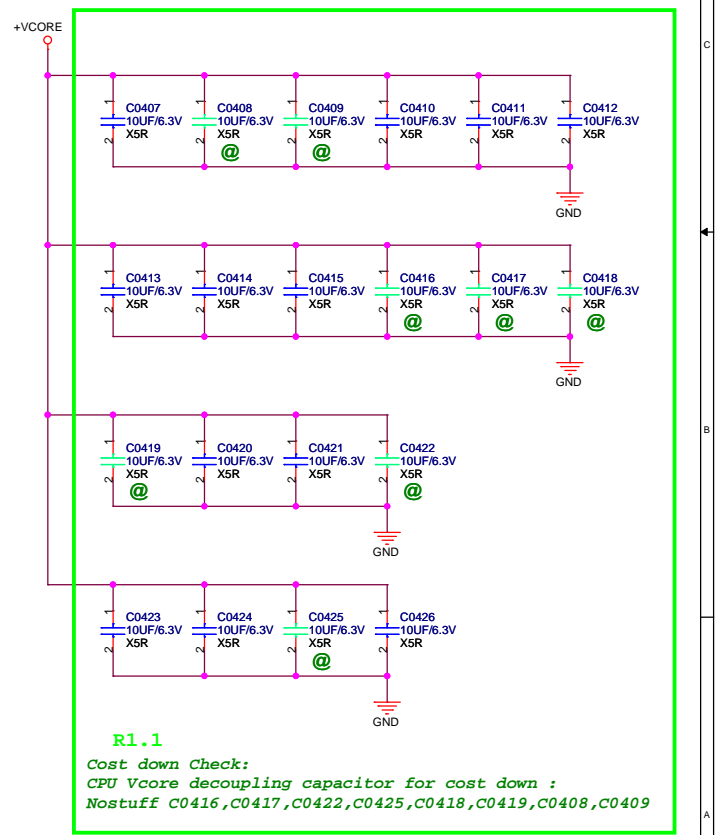
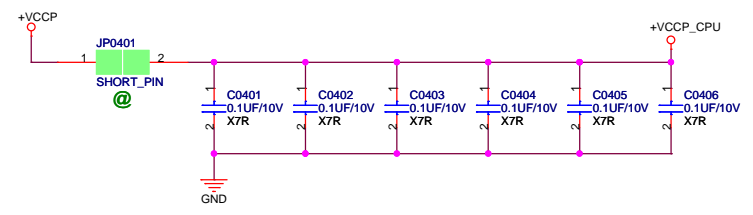


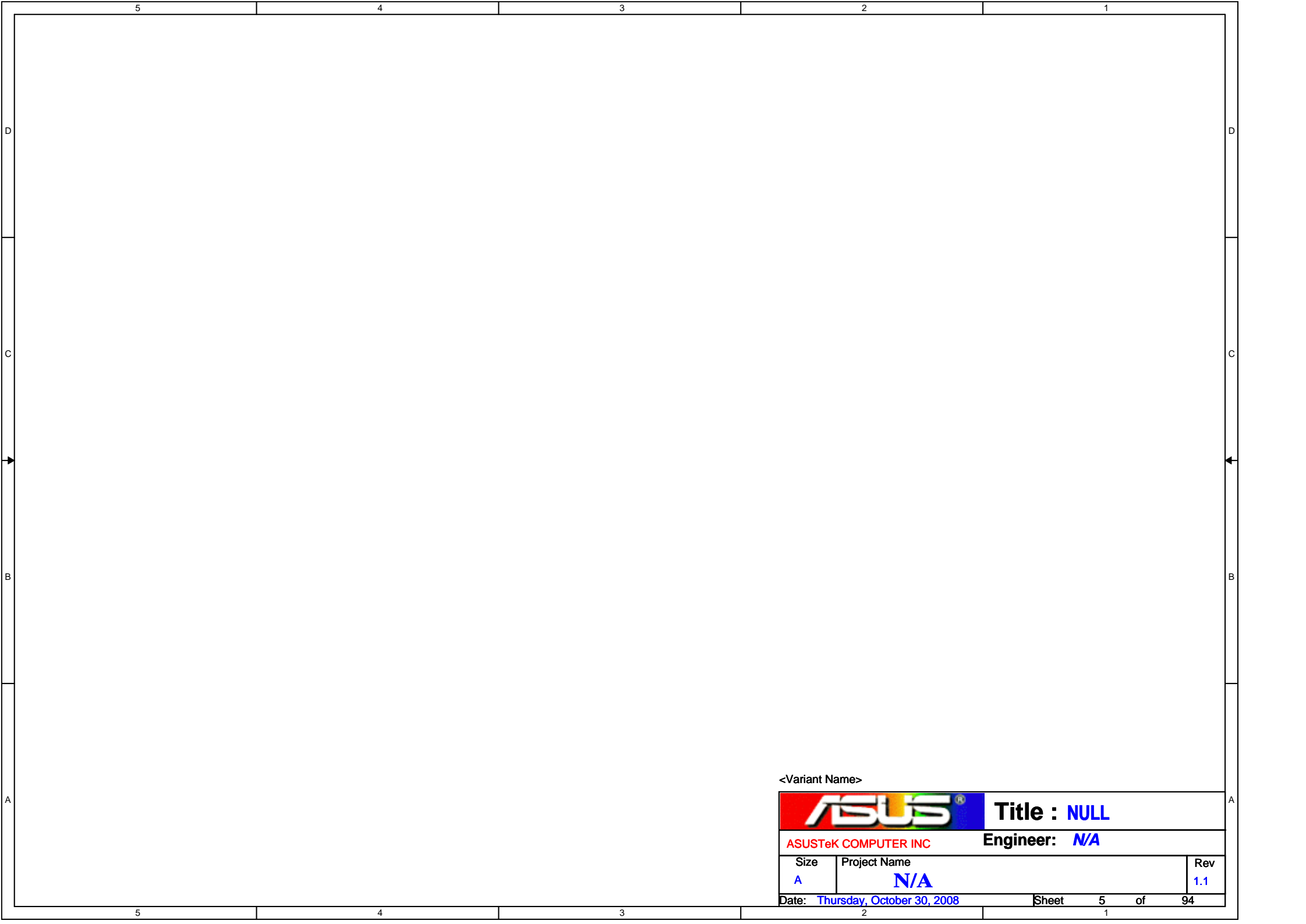
Decoupling guide from INTEL

VCCORE 22uF/10V * 32pcs
330uF/2V * 6pcs
VCCP 0.1uF * 6pcs for CPU
150uF * 1pcs for CPU



+VCCP Decoupling Capacitor (Place near CPU)





<Variant Name>

		Title : NULL
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ASUSTeK COMPUTER INC	Engineer: N/A
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Size	Project Name	Rev
A	N/A	1.1

Date: Thursday, October 30, 2008	Sheet 5 of 94
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D

D

C

C

B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: N/A
Size	Project Name	Rev
A	N/A	1.1
Date: Thursday, October 30, 2008		Sheet 6 of 94

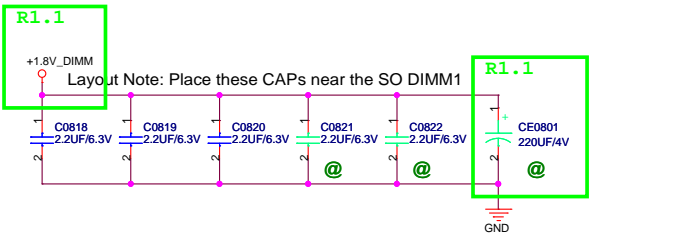
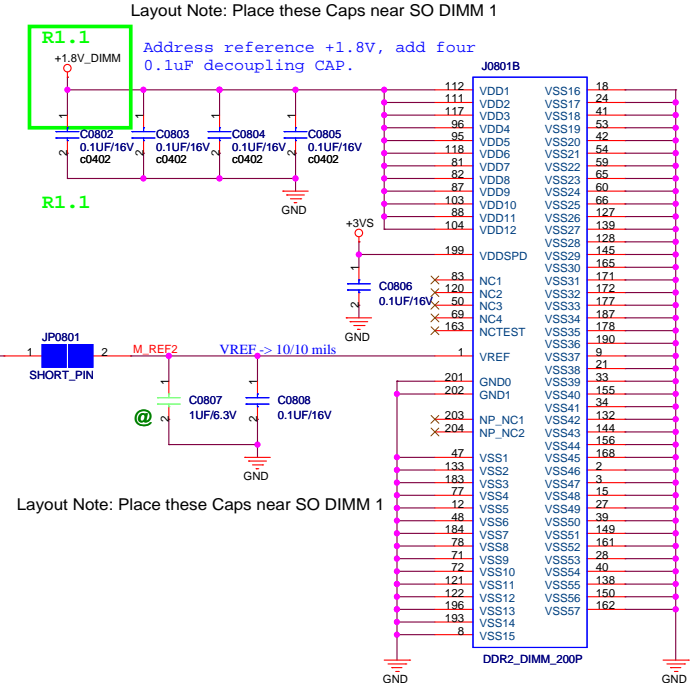
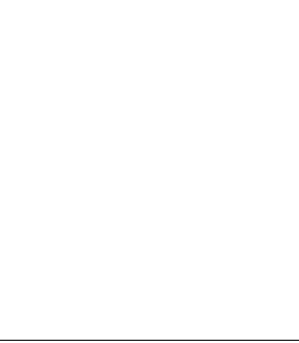
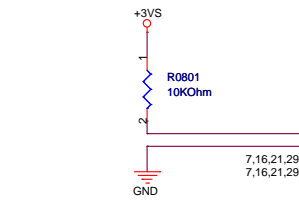
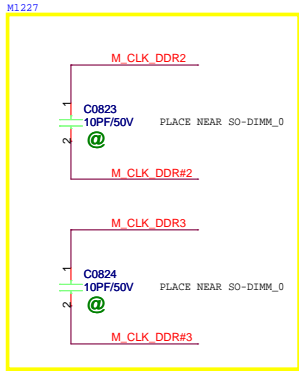
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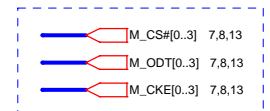
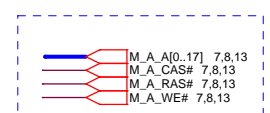
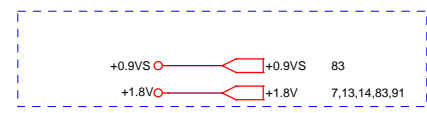
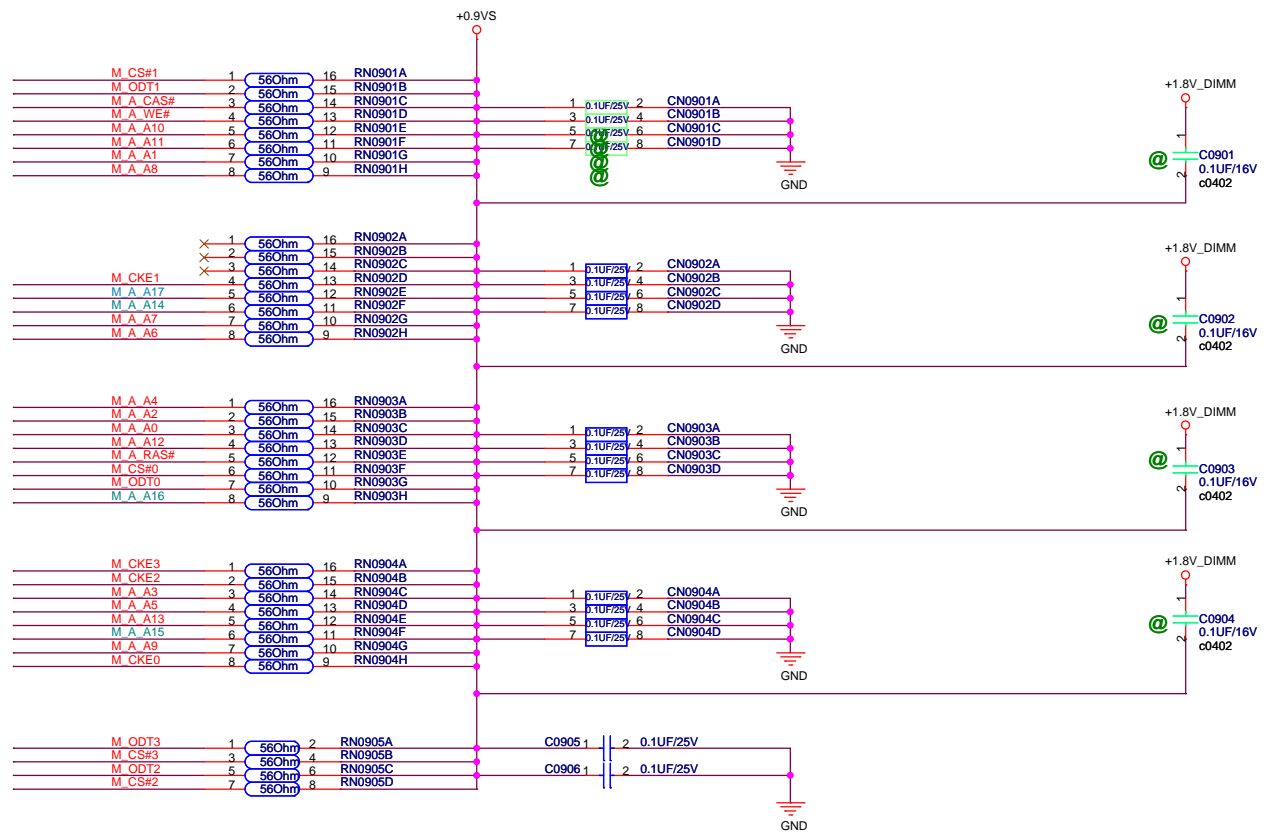
4

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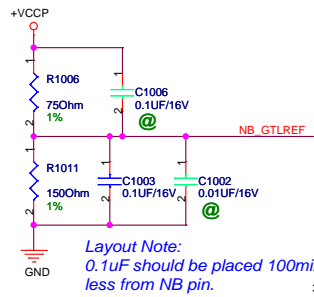
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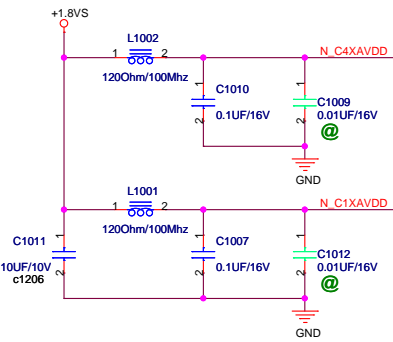
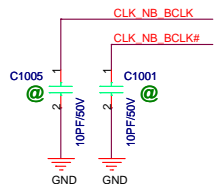


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

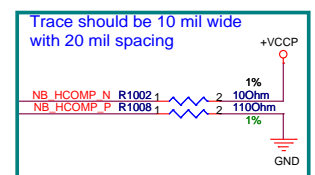
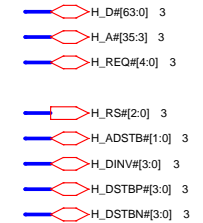
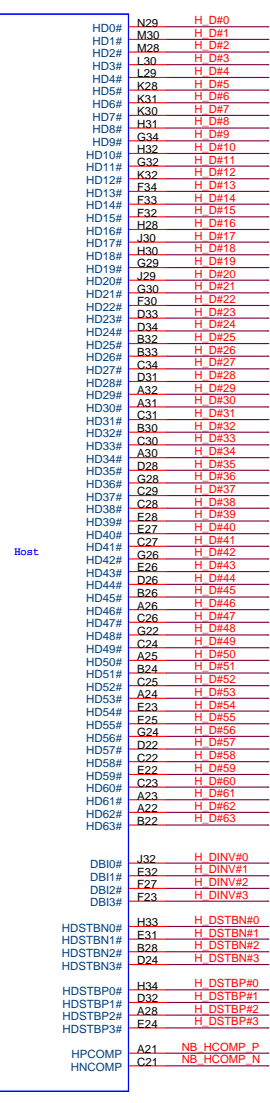
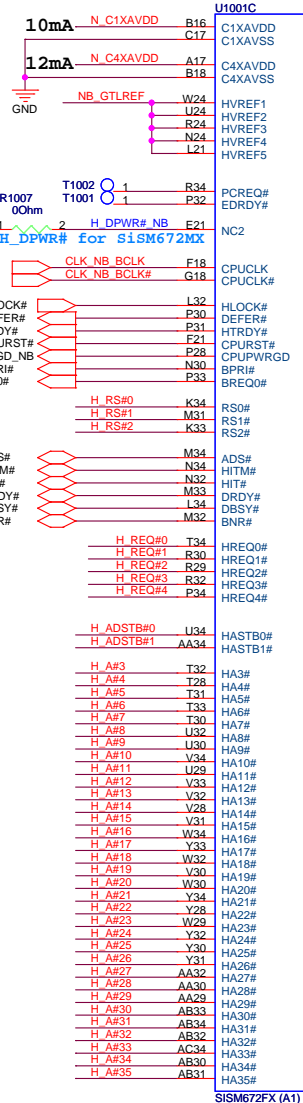
+VCCP 4,14,21,23,29,57,82
+1.8VS 11,13,14,16,20,21,22,23,25,57,83,91

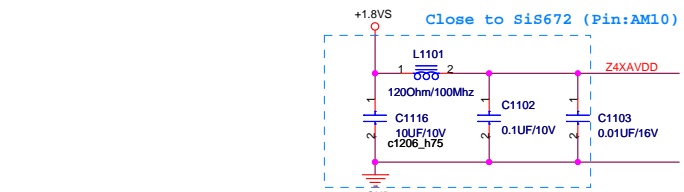


Layout Note:
0.1uF should be placed 100mils or less from NB pin.

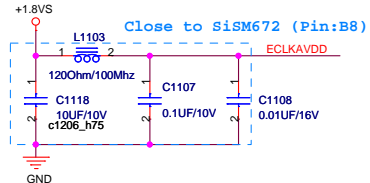
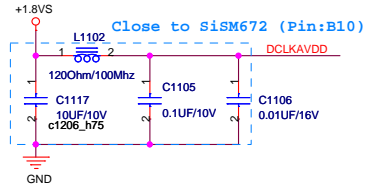
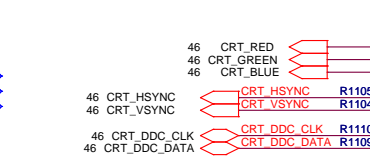
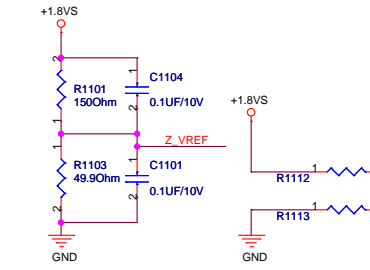
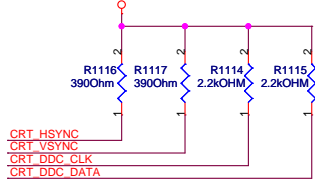
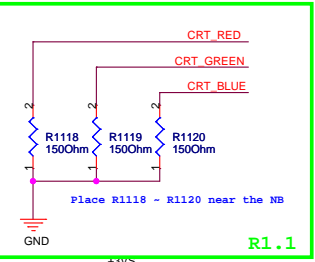


Total Power mW (Max)		
1.8VS	N_C1XAVDD	10mA
	N_C4XAVDD	12mA



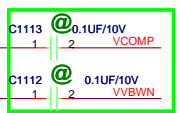
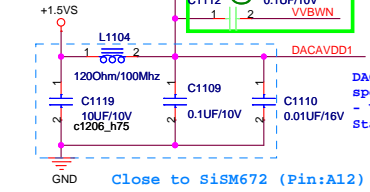


CRT_RED/GREEN/BLUE Trace layout use 5 mils

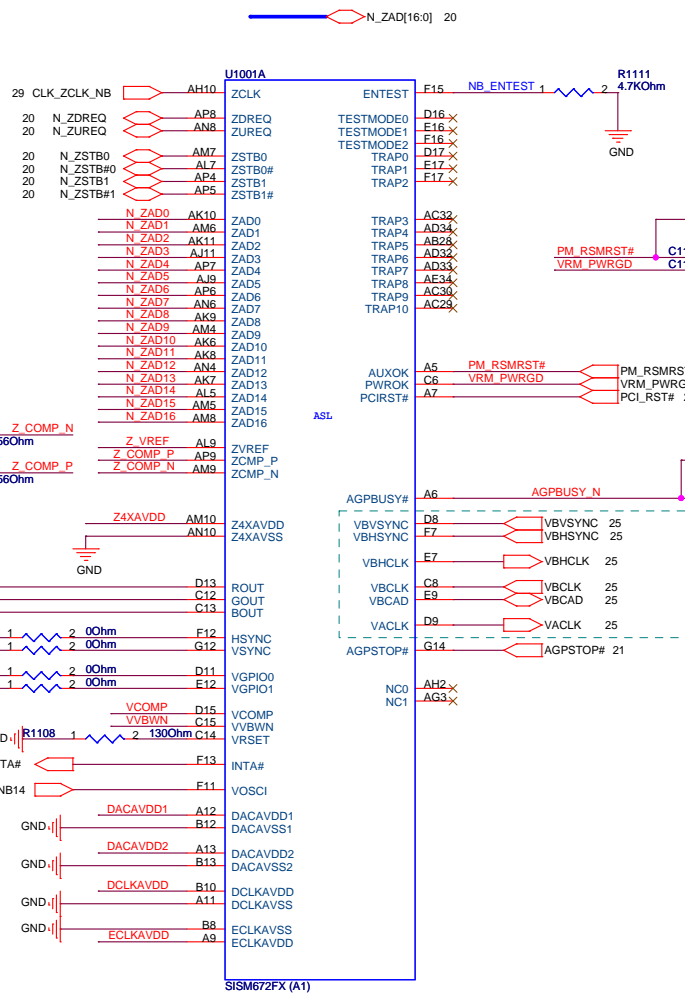


DACAVDD1 Voltage Spec = 1.5V +/- 5%

Sis have modify VCOMP and VVBWN power plan to DACAVDD1



DACAVDD1 For meet the specification of VESA - Video signal Standard



N_ZAD[16:0] 20

+1.8VS
+3VS
+1.5VS

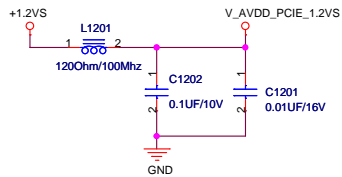
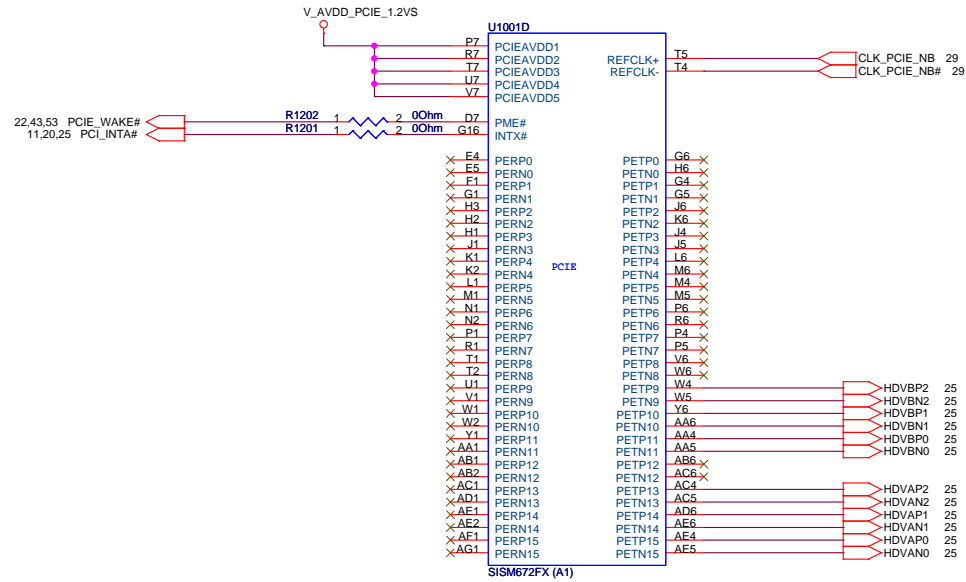
10,13,14,16,20,21,22,23,25,57,83,91
3,7,8,20,21,22,23,25,29,30,32,36,43,46,50,51,53,56,57,62,80,91,92
4,43,53,57,83

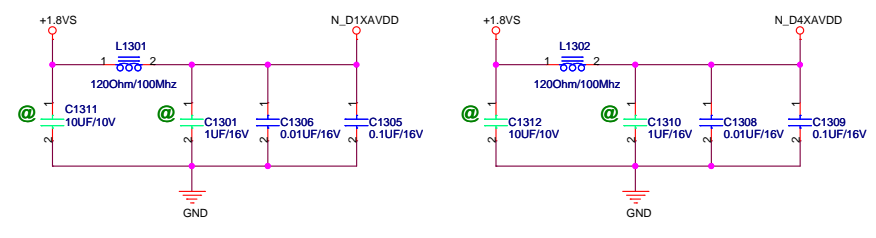
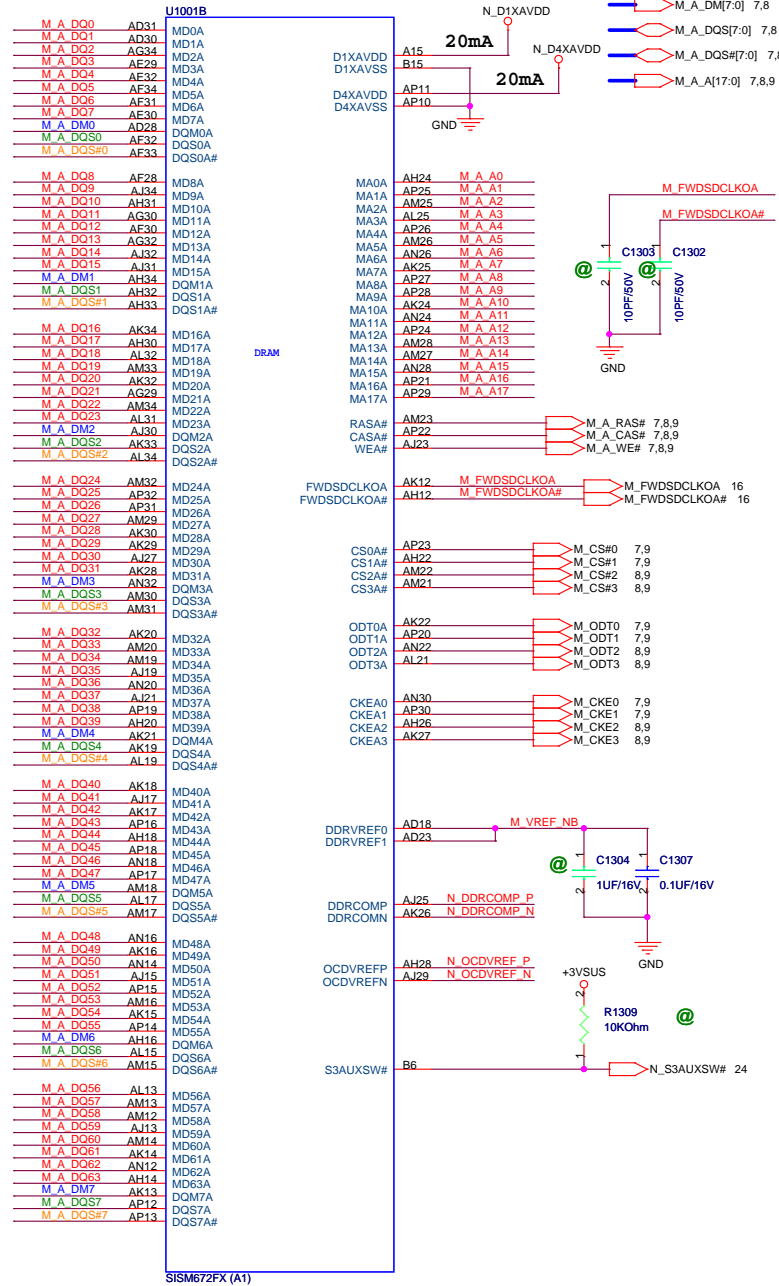
Total Power mW (Max)		
1.8VS	Z4XAVDD	10mA
1.8VS	DCLKAVDD	5mA
1.8VS	ECLKAVDD	5mA
1.5VS	DACAVDD1	73mA
1.8VS	DACAVDD2	73mA

For SiS307 Only

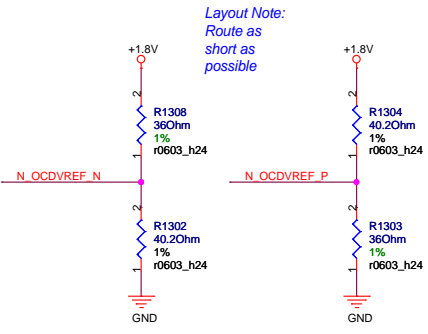
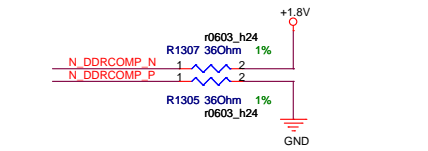
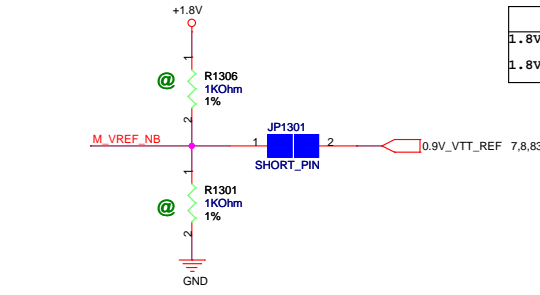
+1.2VS \rightarrow +1.2VS 14,57,91

Total Power mW(Max)		
1.2V	V_AVDD_PCIE_1.2V	190mA

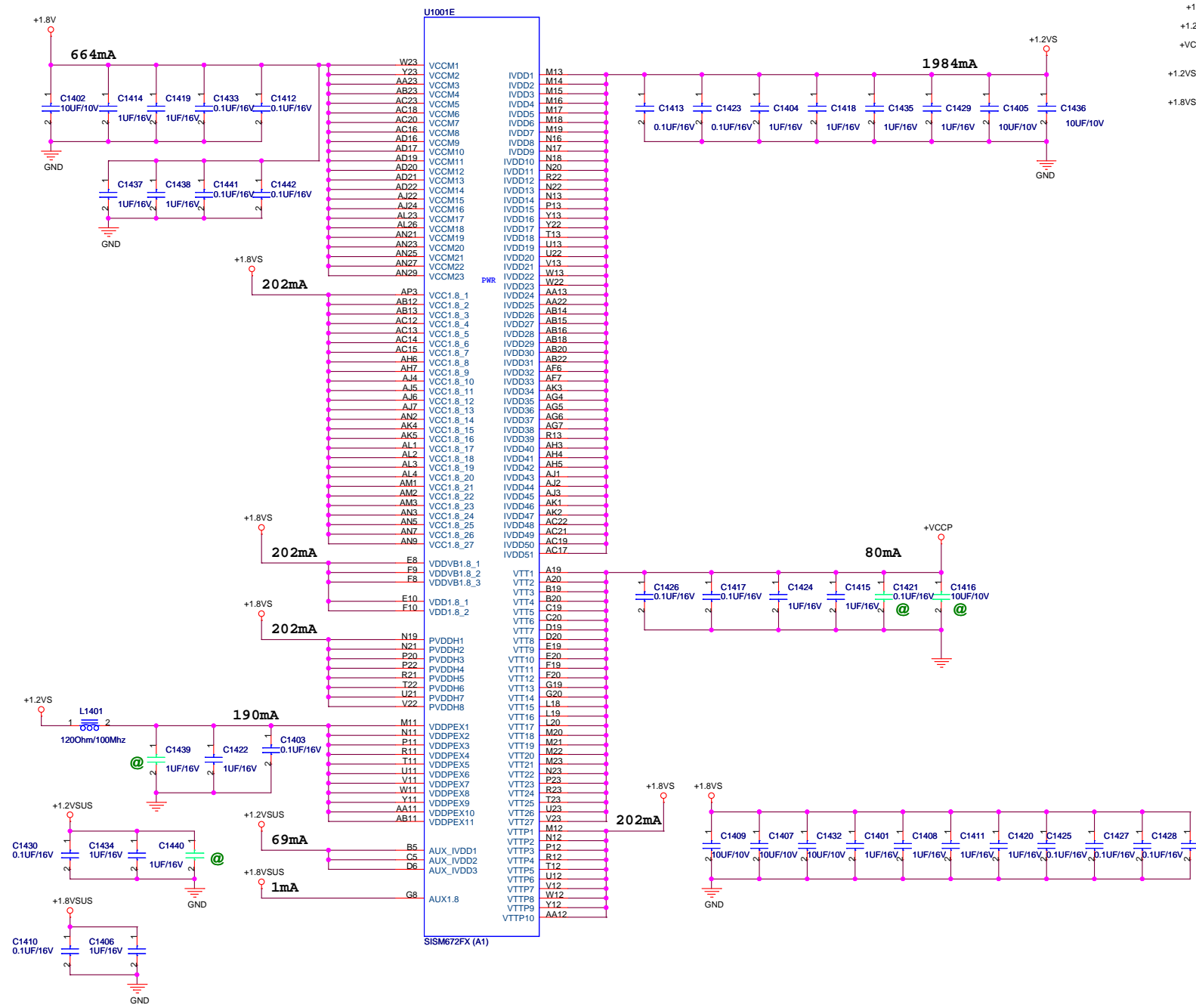




Total Power mW(Max)		
1.8VS	N_D1XAVDD	7mA
1.8VS	N_D4XAVDD	10mA

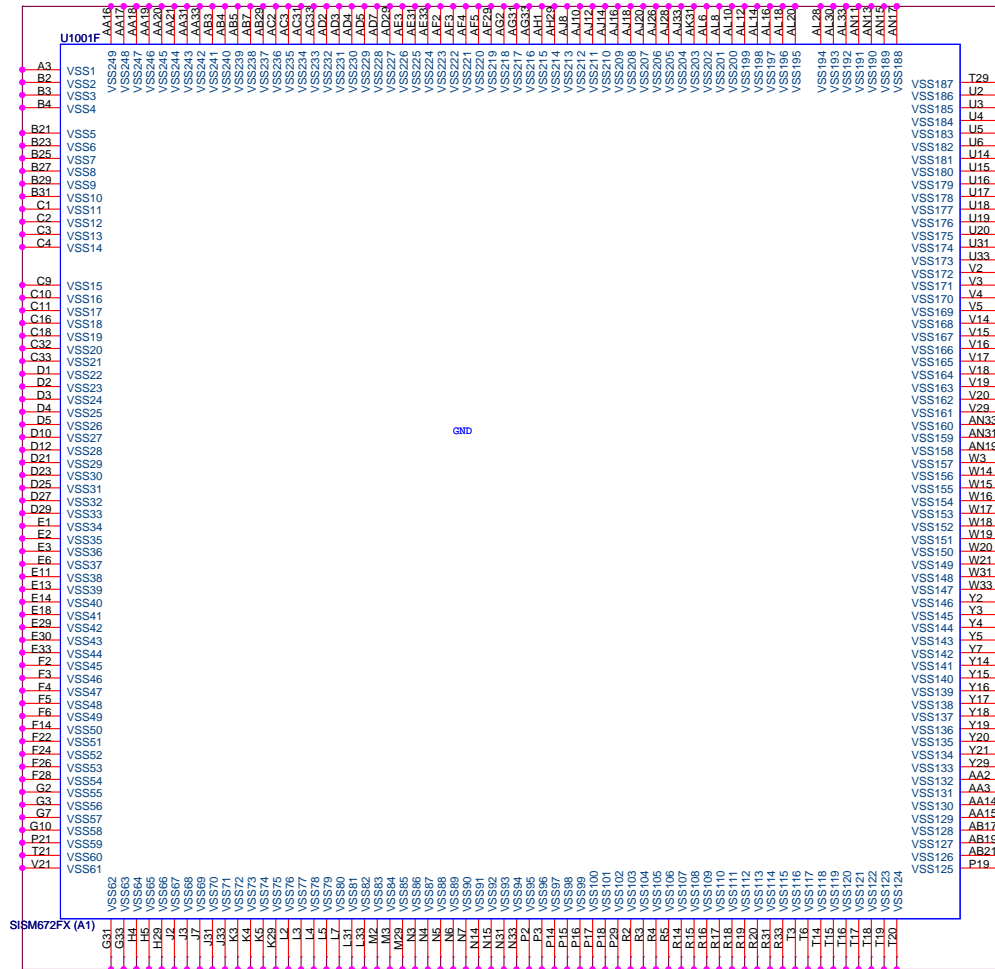


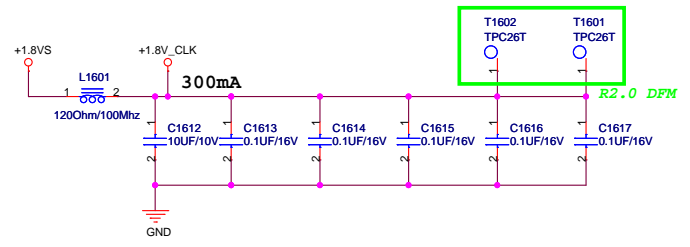
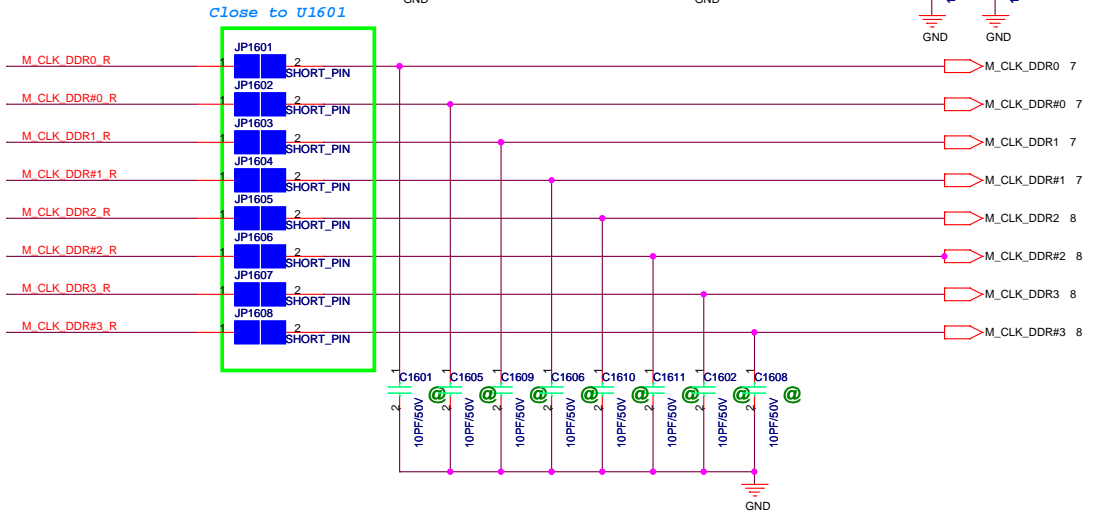
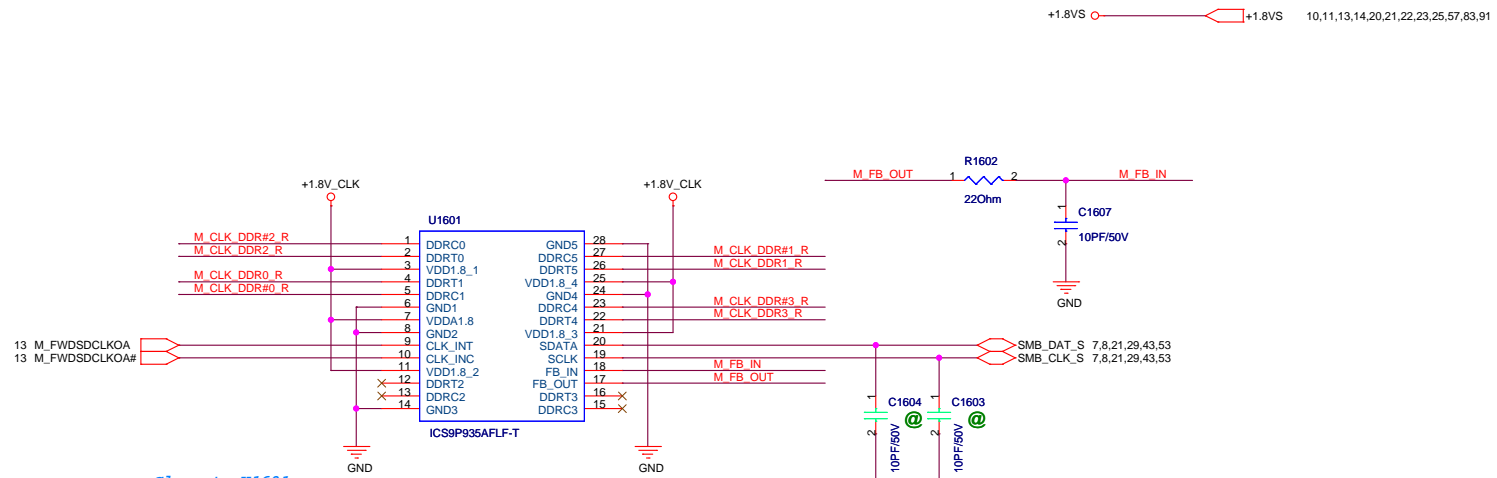
Layout Note:
Route as short as possible



+1.8VS	+1.8VS	10,11,13,16,20,21,22,23,25,57,83,91
+1.8V	+1.8V	7,13,83,91
+1.2VS	+1.2VS	12,57,91
+VCCP	+VCCP	4,10,21,23,29,57,82
+1.2VSUS	+1.2VSUS	82,91
+1.8VSUS	+1.8VSUS	21,22,23,83,91

SISM672 Total Power 4664mW(3D Mode)		
1.2VS	+1.2VS_NB	1984mA
1.8V	VCCM1-23	64mA
1.8VS	VCC1.8/VDDVB1.8/ VDD1.8/PVDDH/VITP	202mA
+VCCP	VTT1-27	80mA
	VDDPEX1-11	190mA





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D

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C


B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC.NB		Engineer: N/A
Size	Project Name	Rev
B	N/A	1.1
Date: Thursday, October 30, 2008		Sheet 17 of 94

5

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D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC .NB

Engineer: N/A

Size	Project Name	Rev
A	N/A	1.1

Date: Thursday, October 30, 2008

Sheet 18 of 94

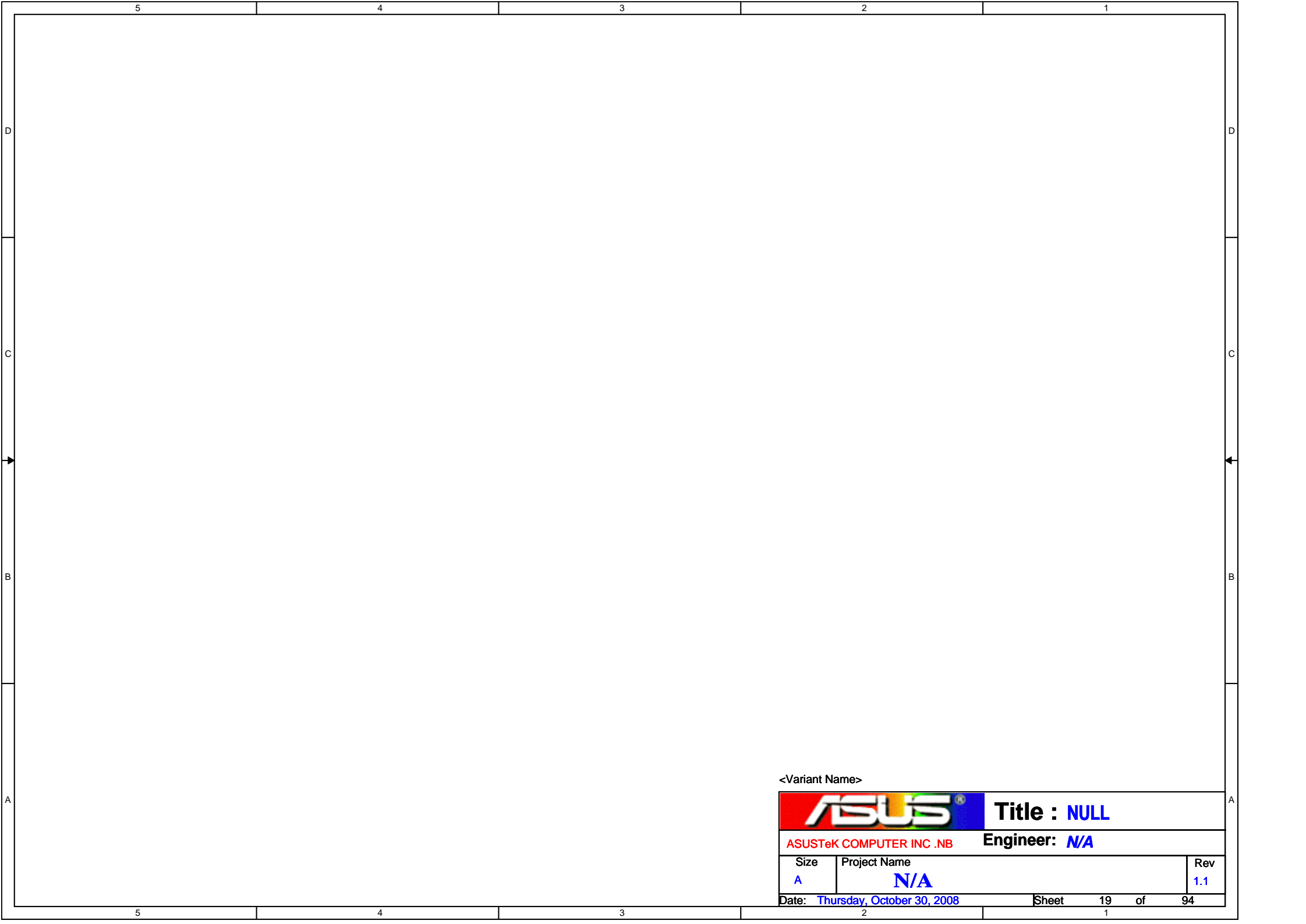
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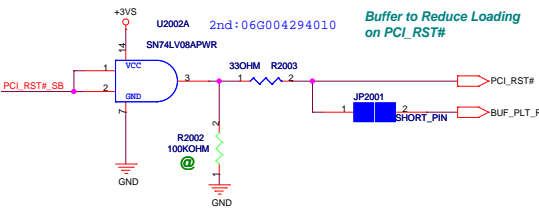


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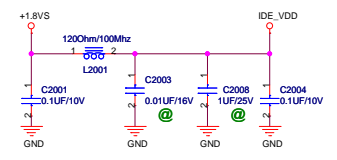
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ASUSTeK COMPUTER INC .NB	Engineer: N/A
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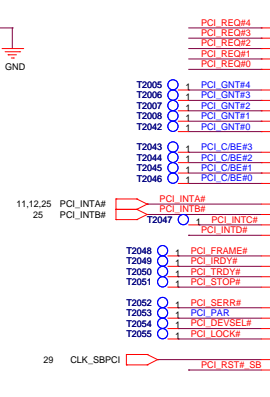
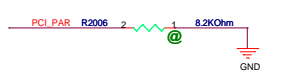
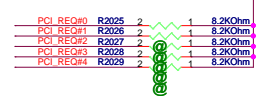
Size	Project Name	Rev
A	N/A	1.1



SB Part Number :02G020003910 sis968 B0

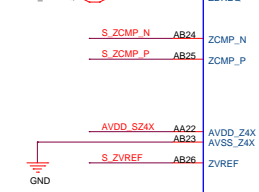
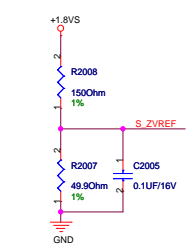
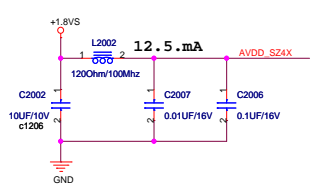
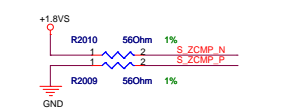


+1.8V	10,11,13,14,16,21,22,23,25,57,83,91
+3V	3,7,8,11,21,22,23,25,29,30,32,36,43,46,50,51,53,56,57,62,80,91,92
+3V	32,35,40,43,44,53,57,61,62,91



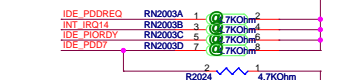
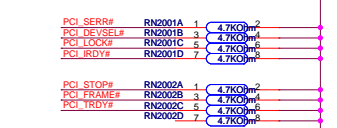
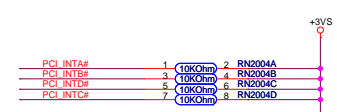
PCI

IDE



MuTIOI

SPI



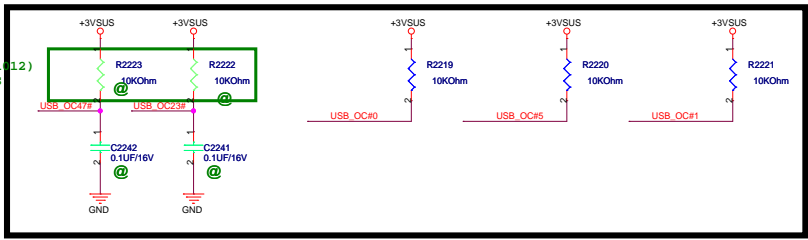
USB 0	CCD
USB 1	Finger Printer
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Bluetooth
USB 6	Newcard
USB 7	USB Conn.

U2001C

USB

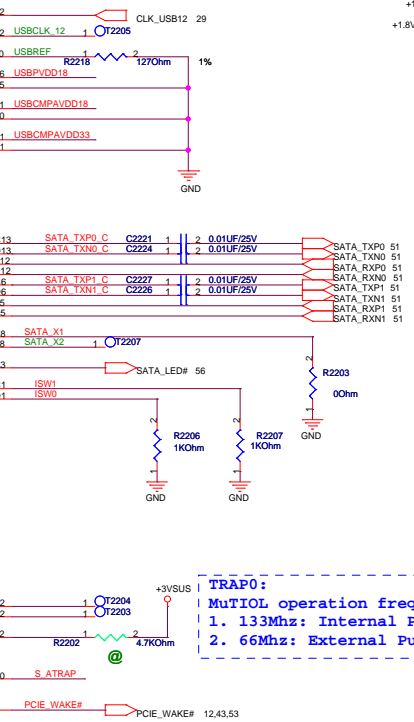
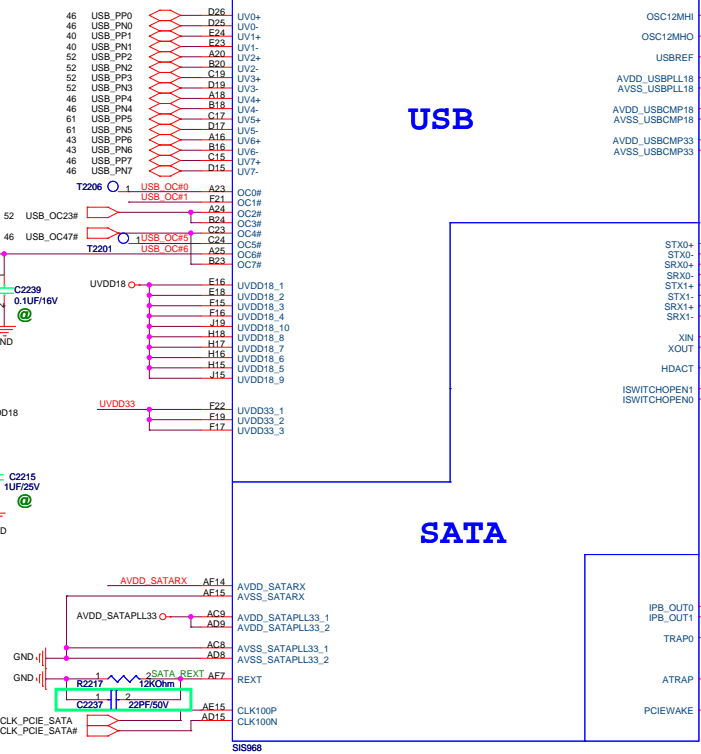
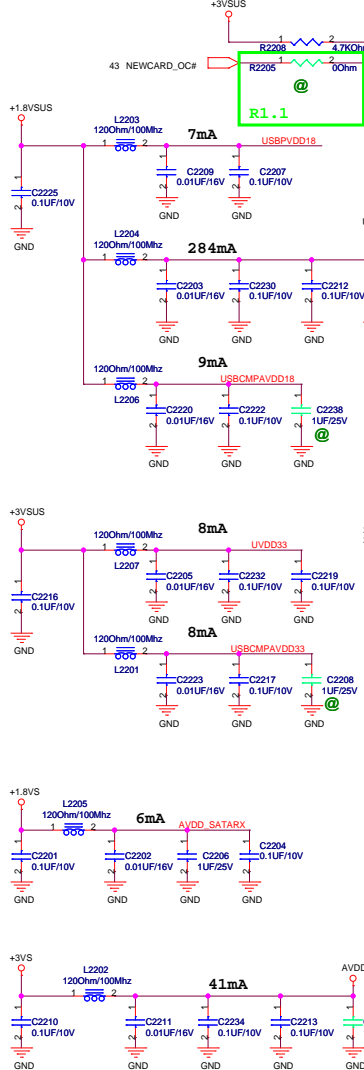
SATA

R2.0 R2223 and R2222 No-Stuff (20071 12)
Solved +5V leakage from USB OC +3VSUS

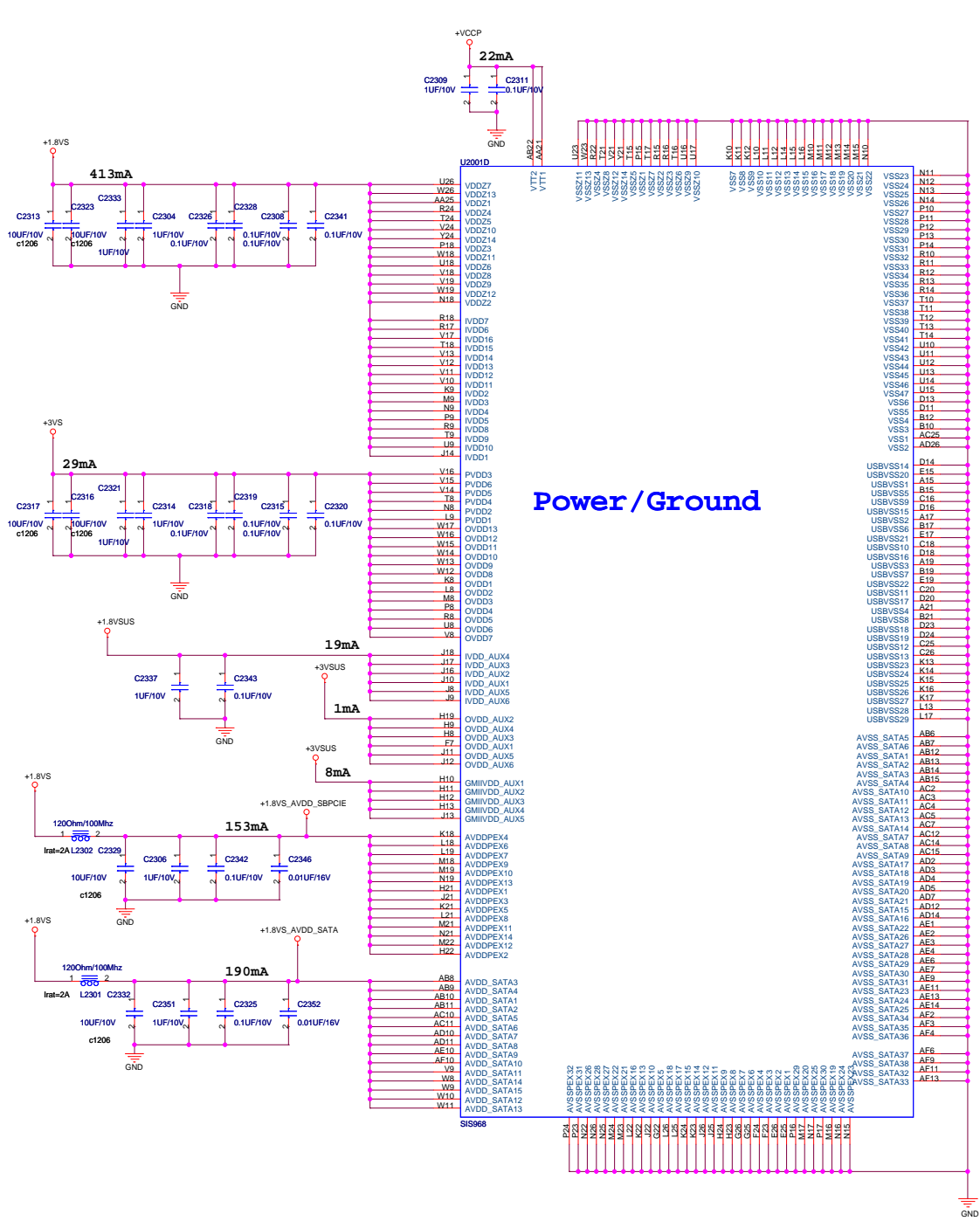


placed near SB

+3VSUS	13,21,23,24,30,33,35,37,46,53,81,91
+3VS	3,7,8,11,20,21,23,25,29,30,32,36,43,46,50,51,53,56,57,62,80,91,92
+1.8VS	10,11,13,14,16,20,21,23,25,57,83,91
+1.8VSUS	14,21,23,83,91

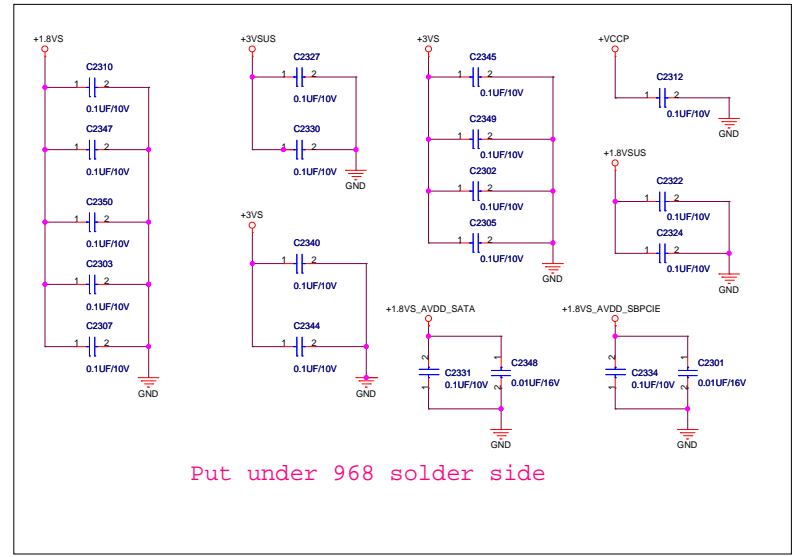
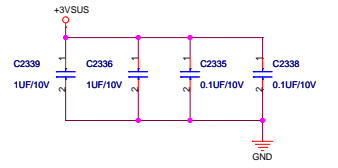


TRAP0:
MultiOL operation frequency select
1. 133Mhz: Internal Pull-down
2. 66Mhz: External Pull-up

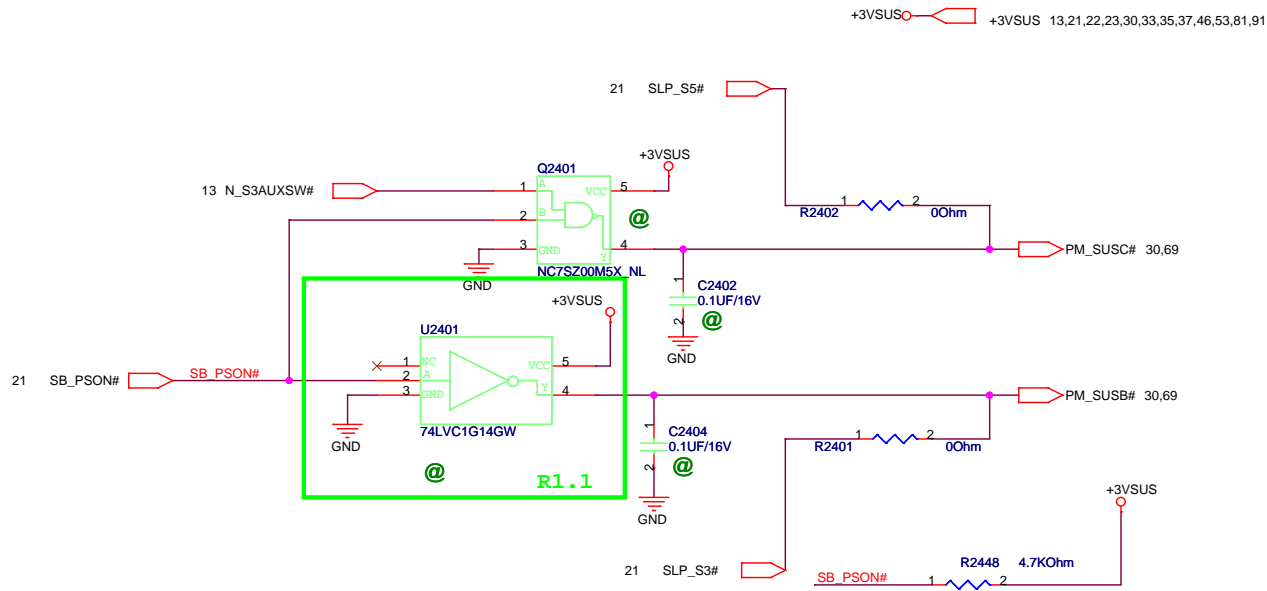


Power/Ground

+3VSUS	+3VSUS	13,21,22,24,30,33,35,37,46,53,81,91
+1.8VSUS	+1.8VSUS	14,21,22,83,91
+1.8VS	+1.8VS	10,11,13,14,16,20,21,22,25,57,83,91
+3VS	+3VS	3,7,8,11,20,21,22,25,29,30,32,36,43,46,50,51,53,56,57,62,80,91,92
+3V	+3V	32,35,40,43,44,53,57,61,62,91
+VCCP	+VCCP	4,10,14,21,29,57,82

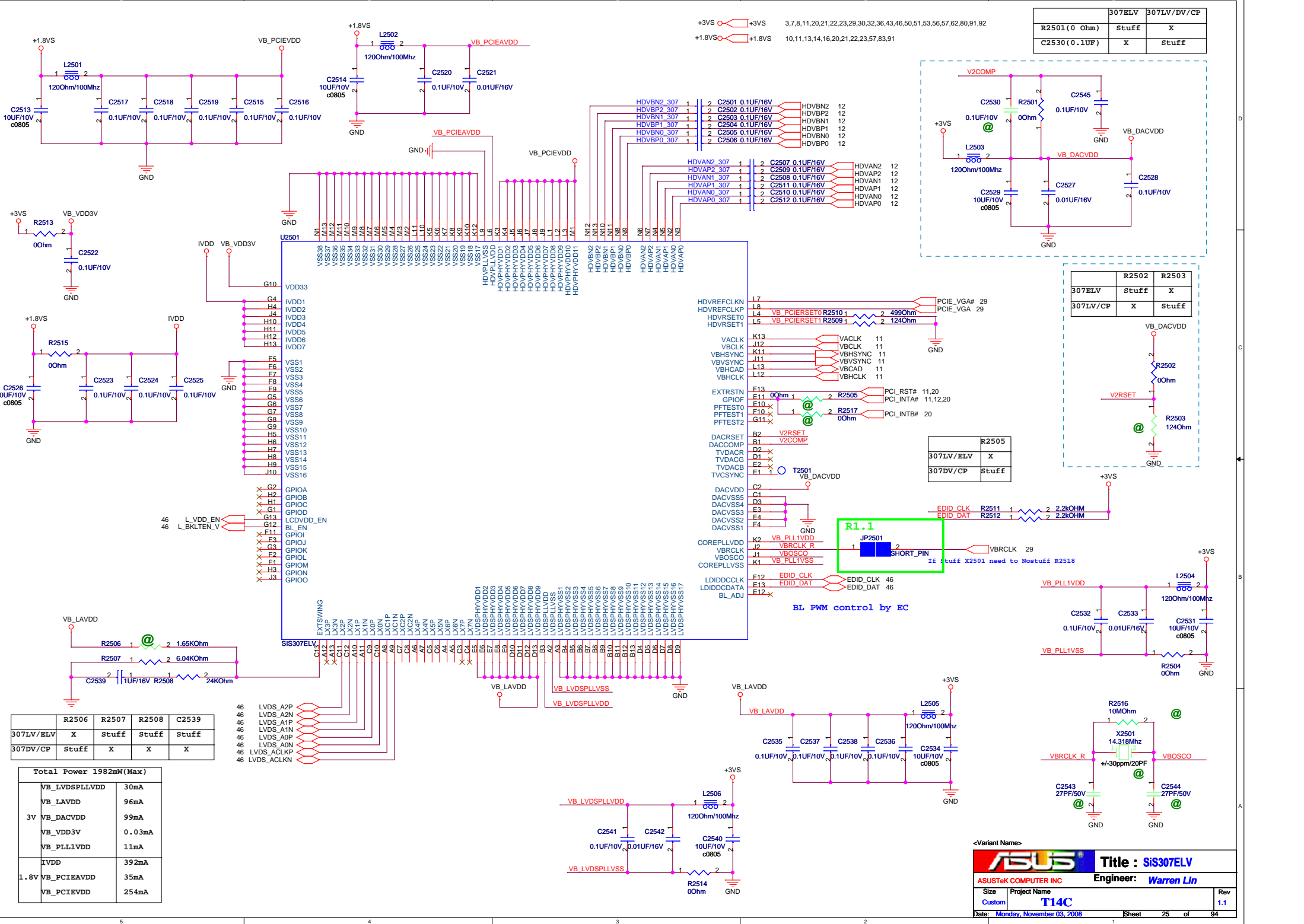


Put under 968 solder side



<Variant Name>

		Title : SB_SIS968 (STRAPING)-(5)
ASUSTeK COMPUTER INC		Engineer: Bruce
Size B	Project Name Z65	Rev 2.0
Date: Thursday, October 30, 2008	Sheet 24 of 94	1



	R2506	R2507	R2508	C2539
307LV/ELV	X	StuFF	StuFF	StuFF
307DV/CP	StuFF	X	X	X

Total Power 1982mW(Max)	
VB_LVDSPLLVD	30mA
VB_LAVDD	96mA
VB_DACVDD	99mA
VB_VDD3V	0.03mA
VB_PLL1VDD	11mA
IVDD	392mA
1.8V VB_PCIEAVDD	35mA
VB_PCIEVDD	25.4mA

	307ELV	307LV/DV/CP
R2501(0 Ohm)	StuFF	X
C2530(0.1uF)	X	StuFF

	R2502	R2503
307ELV	StuFF	X
307LV/CP	X	StuFF

	R2505
307LV/ELV	X
307DV/CP	StuFF

<Variant Name>

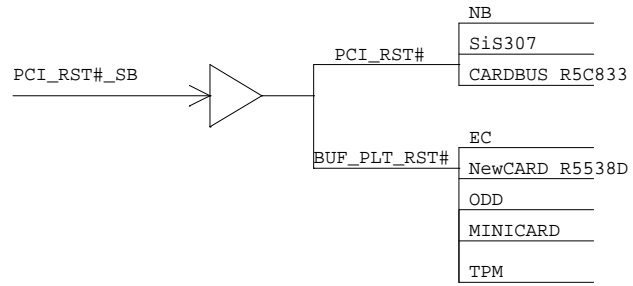
Title : SIS307ELV

ASUSTek COMPUTER INC Engineer: **Warren Lin**

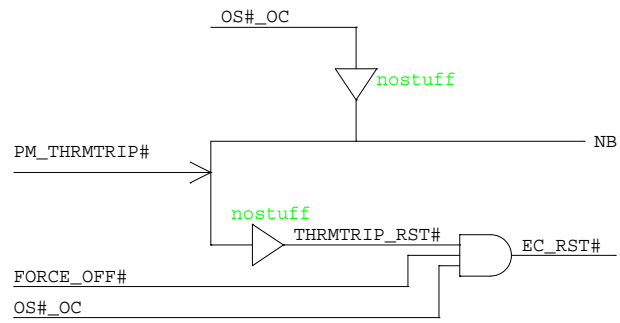
Size	Project Name	Rev
Custom	T14C	1.1

Date: **Monday, November 03, 2008** Sheet 25 of 94

PCI_RST#_SB TOPOLOGY



PM_THRMTRIP# and EC_RST# TOPOLOGY



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D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Bruce

Size
A

Project Name
N/A

Rev
1.1

Date: Thursday, October 30, 2008

Sheet 27 of 94

5


4

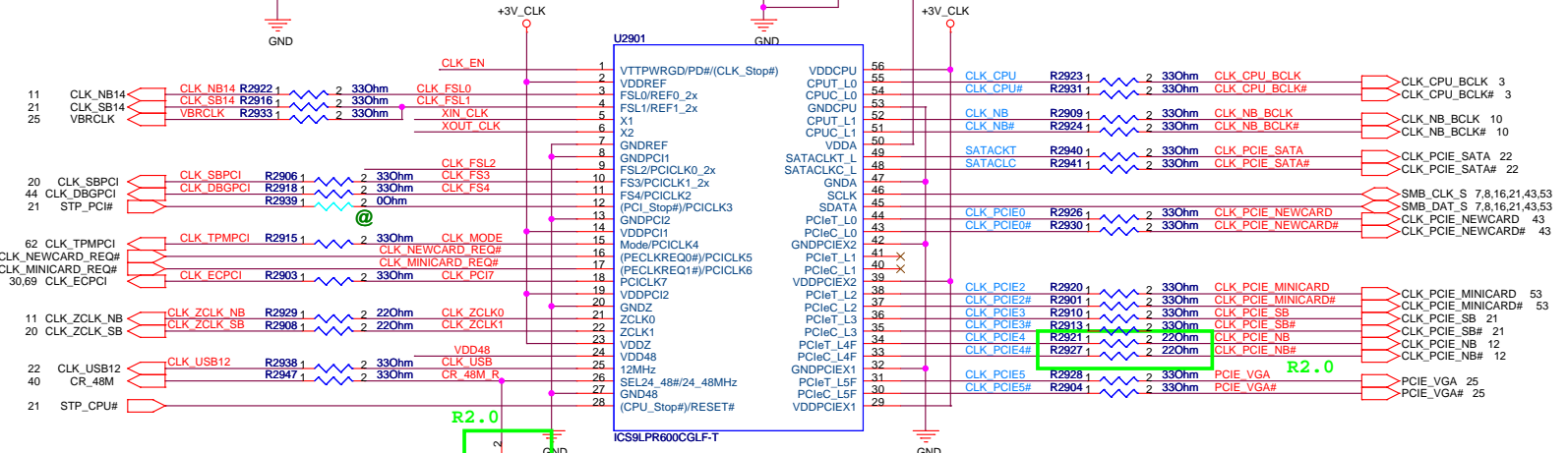
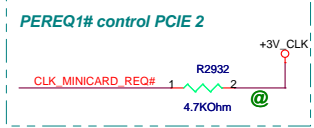
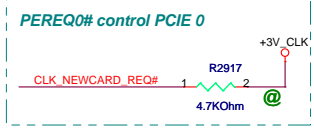
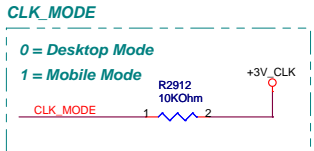
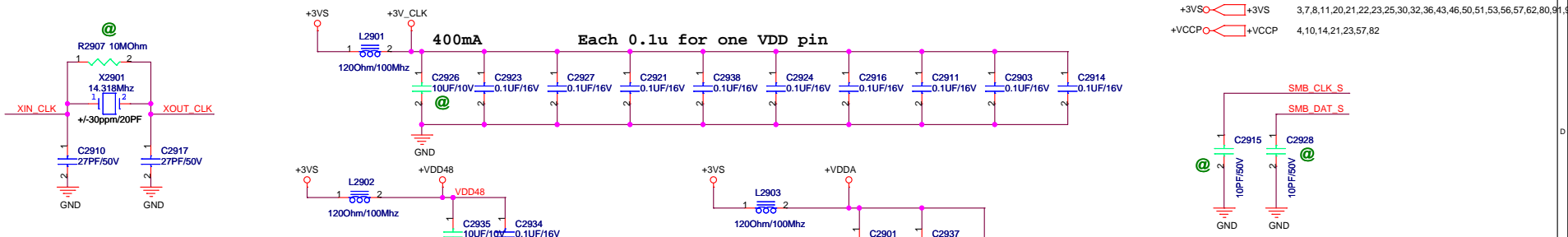
3

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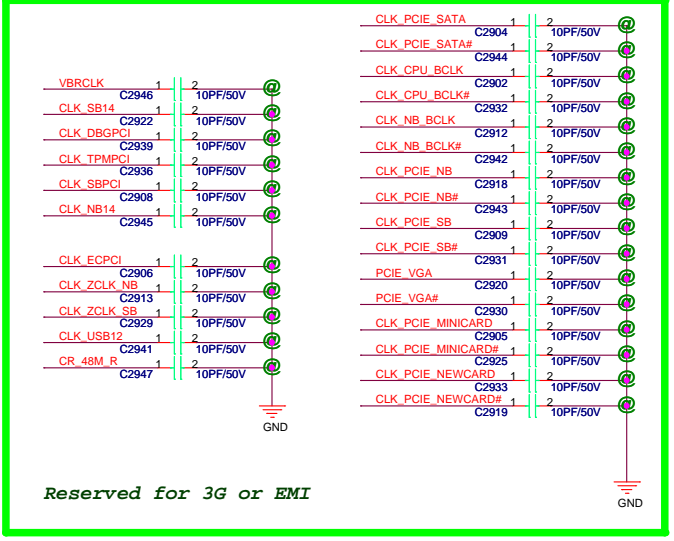
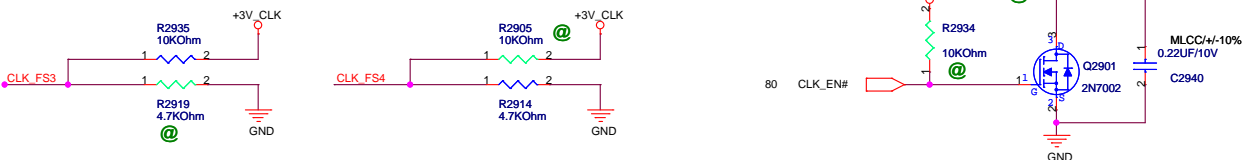
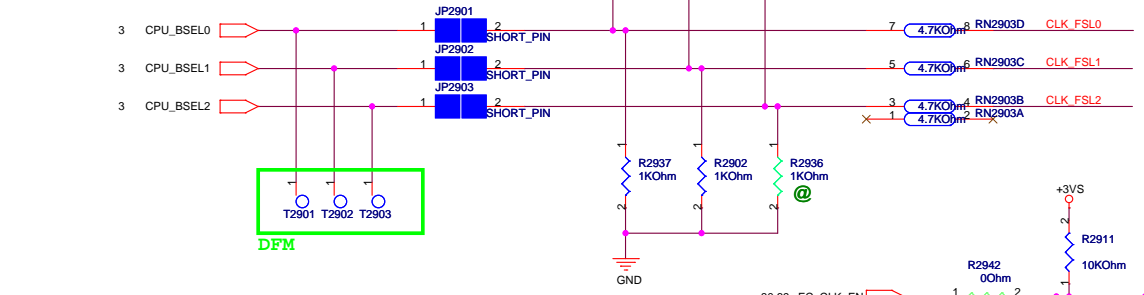
1



<Variant Name>		
		Title : NULL
ASUSTeK COMPUTER INC		Engineer: N/A
Size Custom	Project Name N/A	Rev 1.1
Date: Thursday, October 30, 2008		
Sheet 28 of 94		

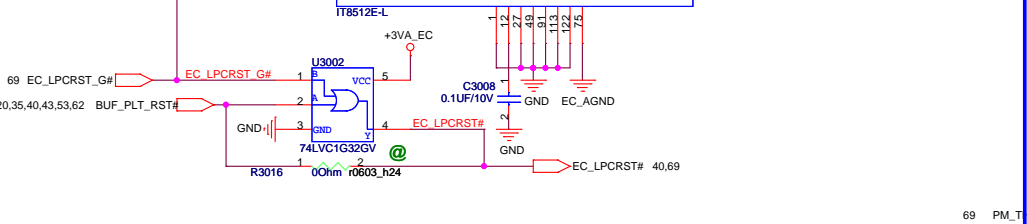
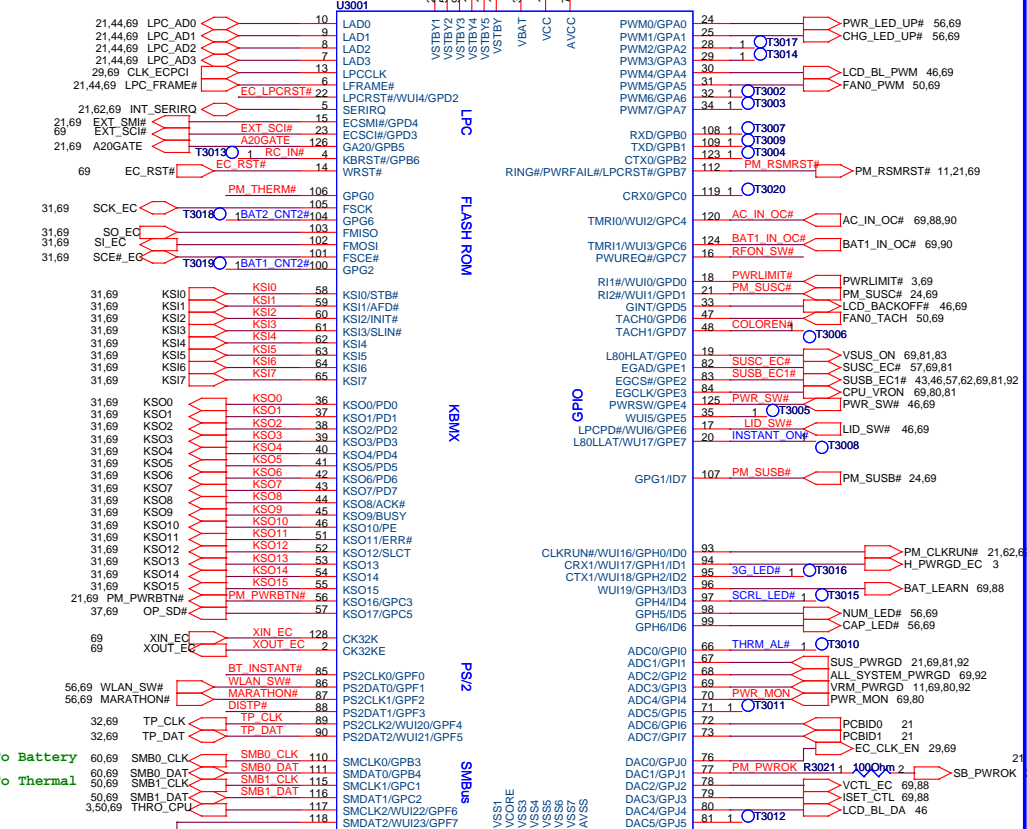


FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100
0	1	0	1	0	200	33	133	100	100
0	1	0	1	0	233	33	133	100	100

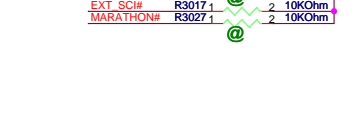
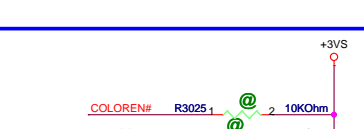
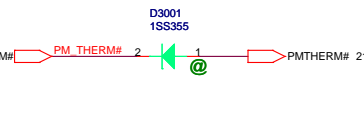
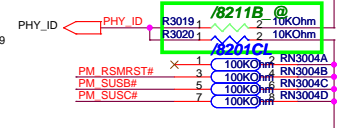
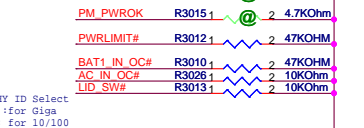
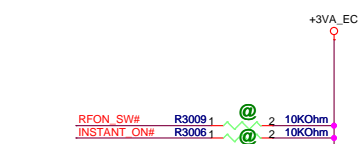
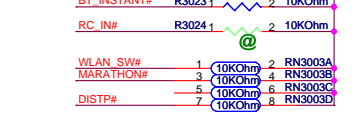
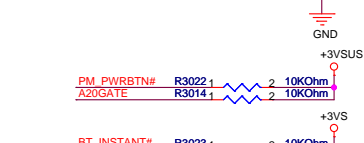
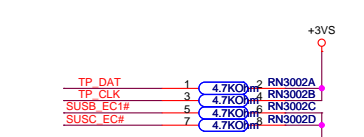
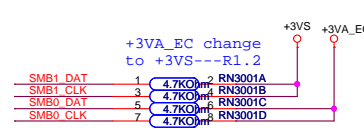


For IT8512 Core IC
 Standby (Sleep) Power Consumption:
 0.1mA * 3.3V = 0.33mW

ITE8502:06G042021010

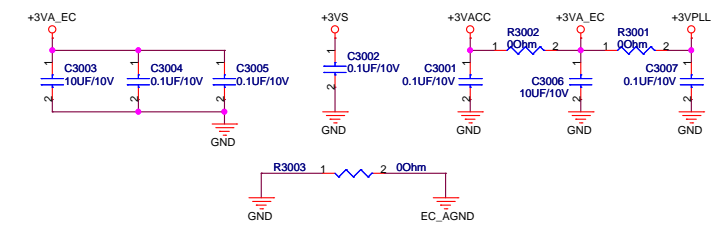


For Pull-up/Pull-down

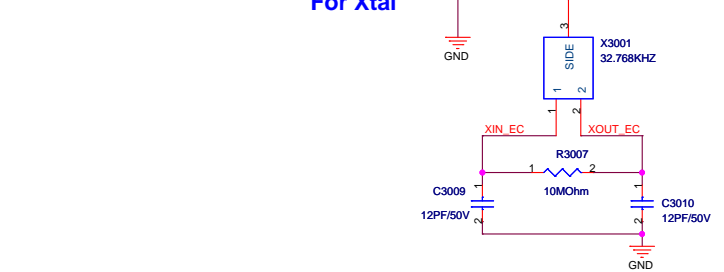


+3VA	21,46,50,57,60,81
+3VS	3,7,8,11,20,21,22,23,25,29,32,36,43,46,50,51,53,56,57,62,80,91,92
+5VS	32,36,37,38,46,50,51,56,57,80,91
+3VA_EC	+3VA_EC 31,46,69

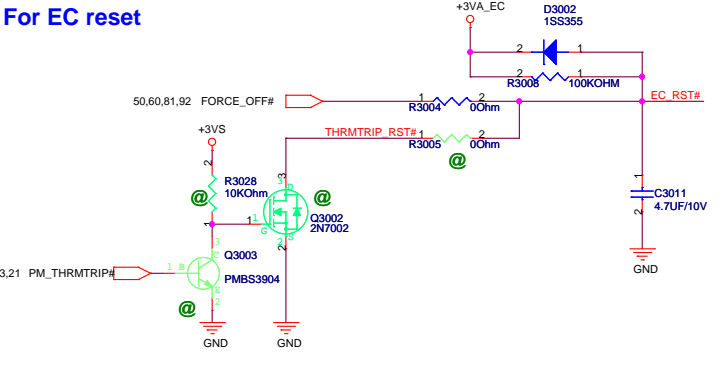
For IT8512 Power



For Xtal



For EC reset



For EC Hardware Strap

I/O Base Address	Share Memory	PP Enable
Note: It can be programmable by EC firmware	Note: It can be programmable by EC firmware	Note: Default Internal Pull-Low

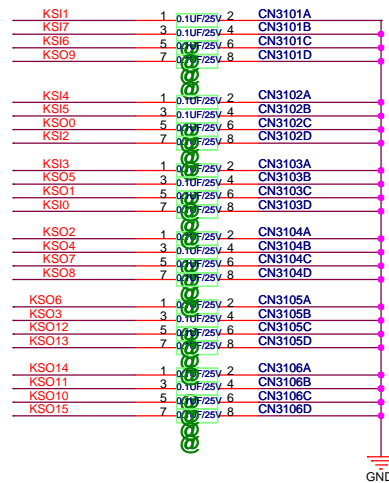
<Variant Name>

Title : EC-ITE8512 (1)

ASUSTeK COMPUTER INC Engineer: Bruce

Size	Project Name	Rev
Custom	Z65	1.1

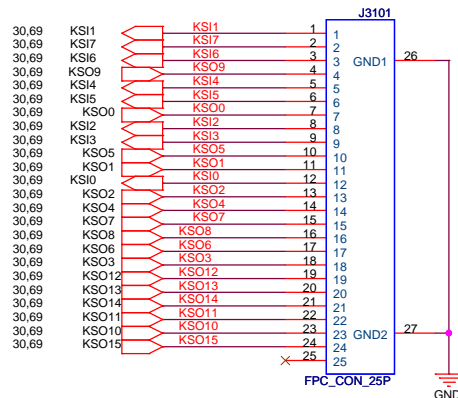
Date: Thursday, October 30, 2008 Sheet 30 of 94



+3VA_ECO \rightarrow +3VA_EC 30,46,69

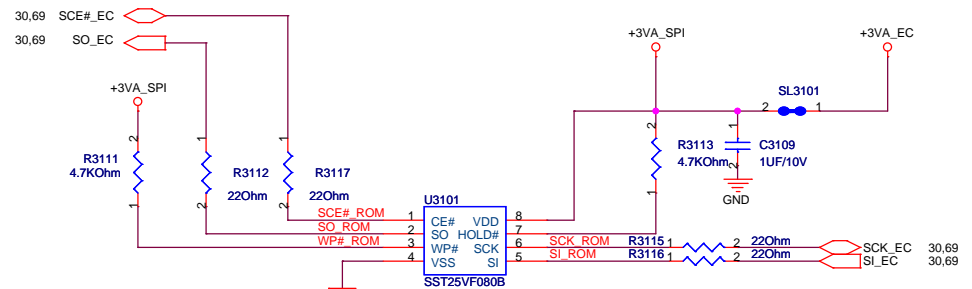
Keyboard Conn.

12G182102500
Z96 W/B



2nd Source:12G182102501

For 8M bits ISA ROM

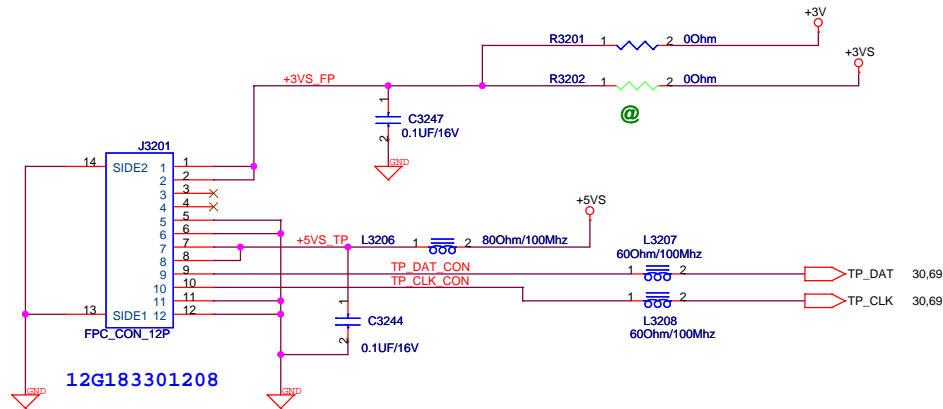


Second source:05G001208130

<Variant Name>

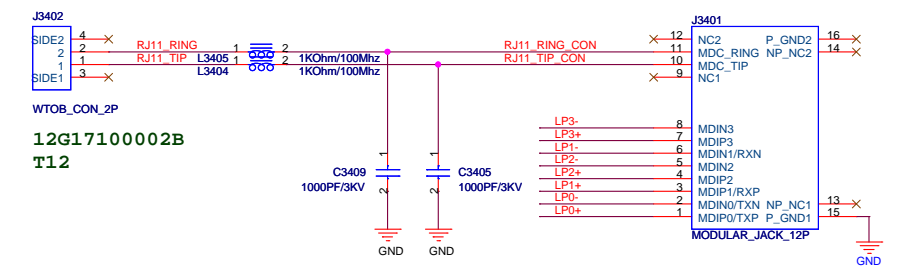
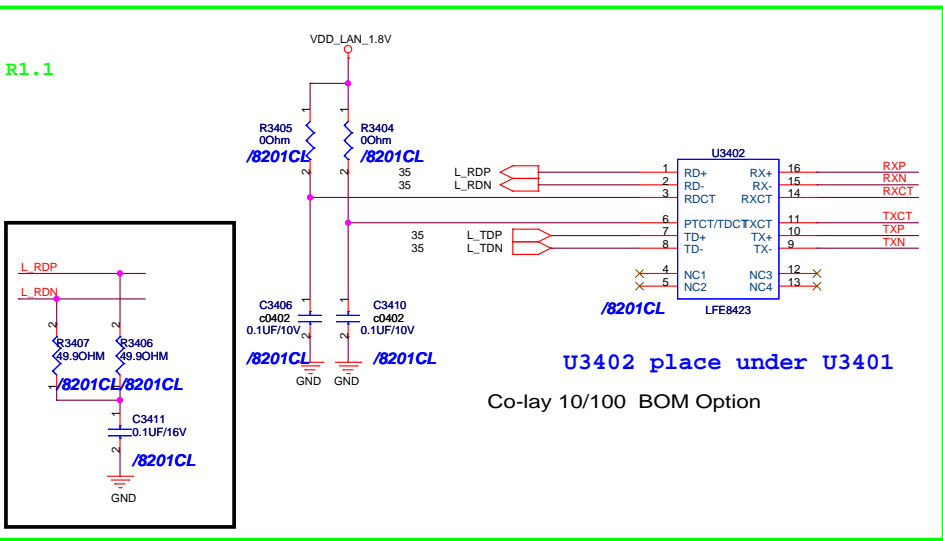
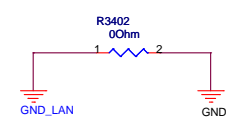
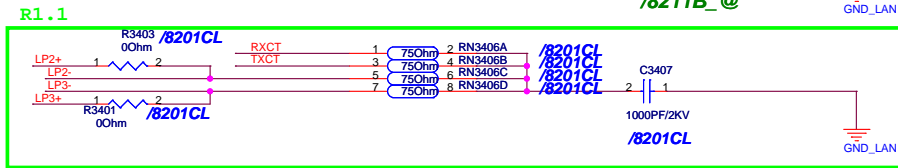
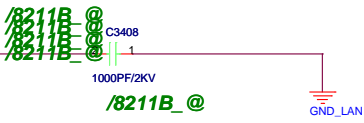
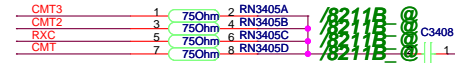
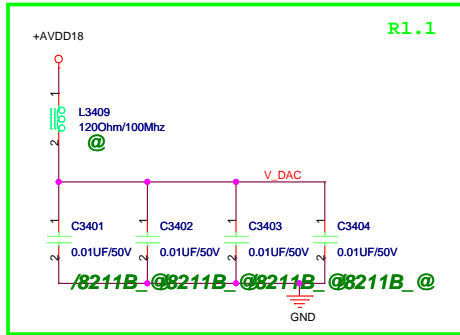
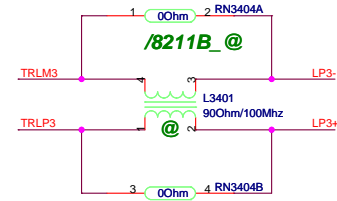
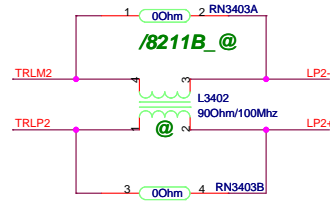
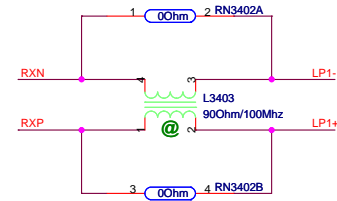
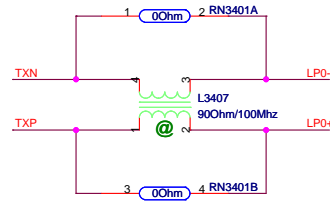
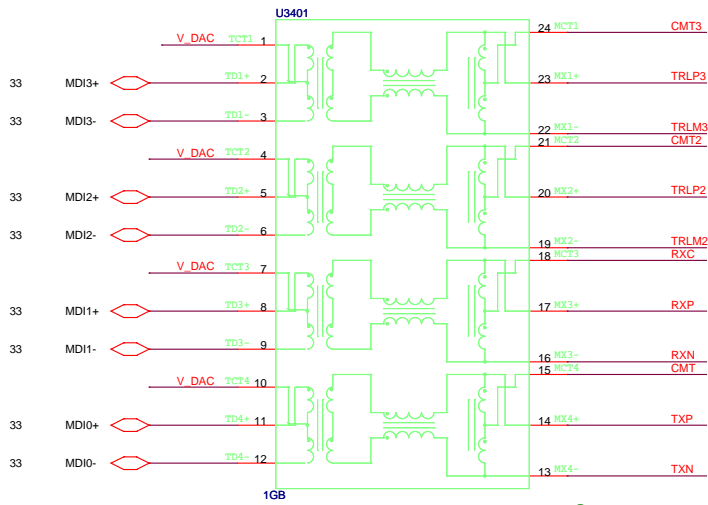
ASUS		Title : EC-ITE8511(2)
ASUSTek COMPUTER INC ETD		Engineer: Bruce
Size Custom	Project Name Z65	Rev 1.1
Date: Thursday, October 30, 2008	Sheet 31 of 94	

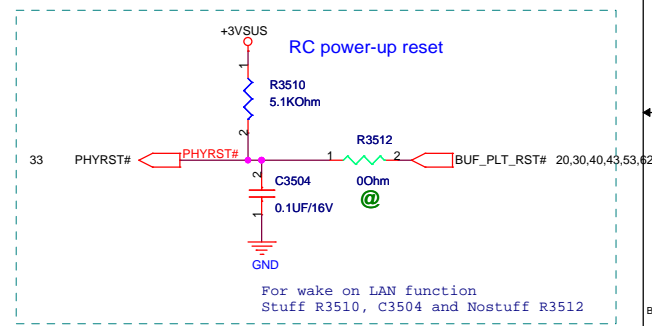
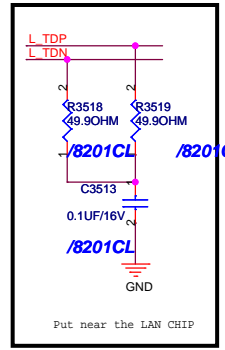
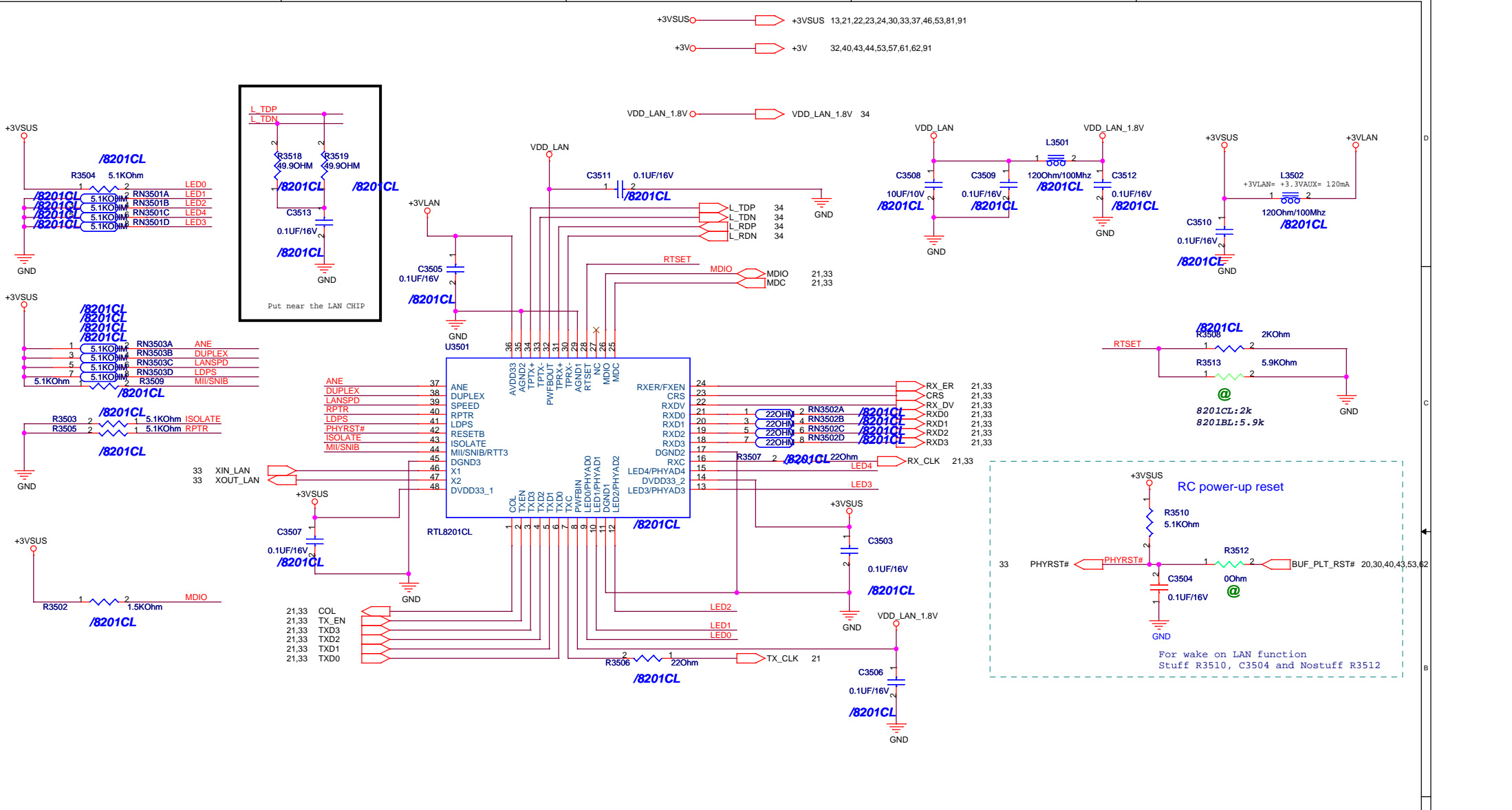
Touchpad



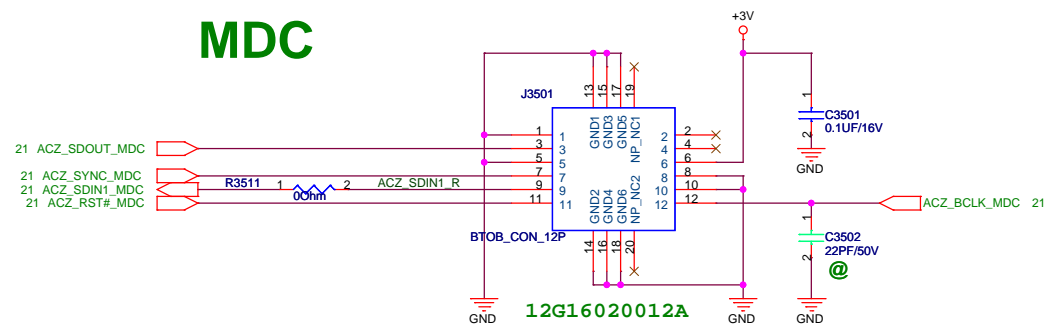
<Variant Name>

ASUS		Title : TouchPad	
ASUSTeK COMPUTER INC		Engineer: <i>Bruce</i>	
Size	Project Name		Rev
A3	Z65		1.1
Date:	Thursday, October 30, 2008	Sheet	32 of 94





MDC

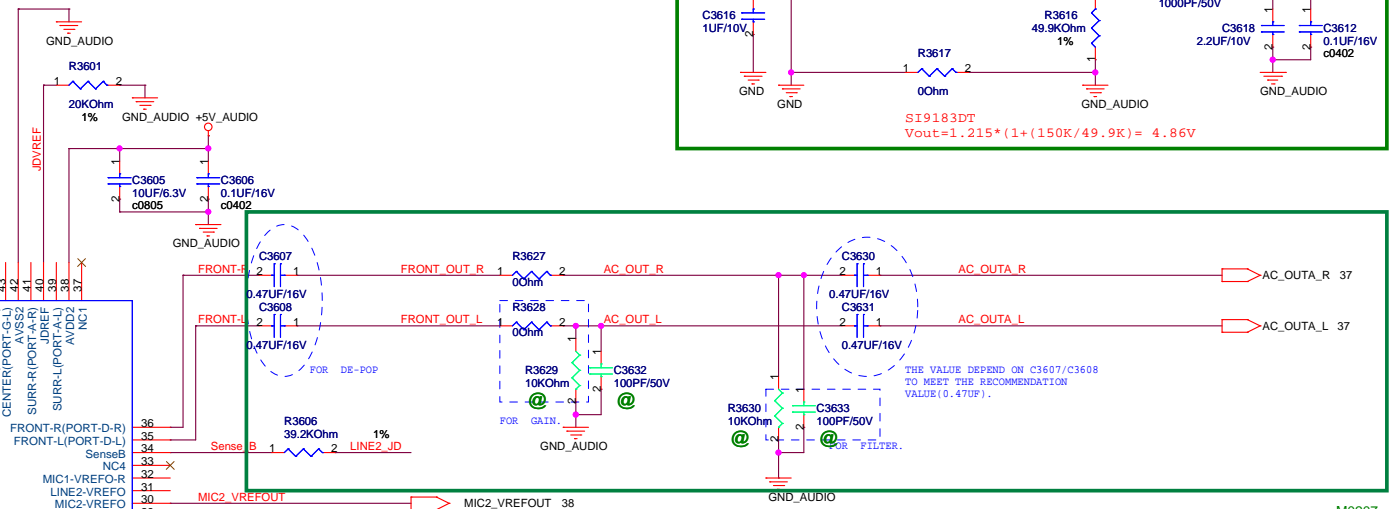
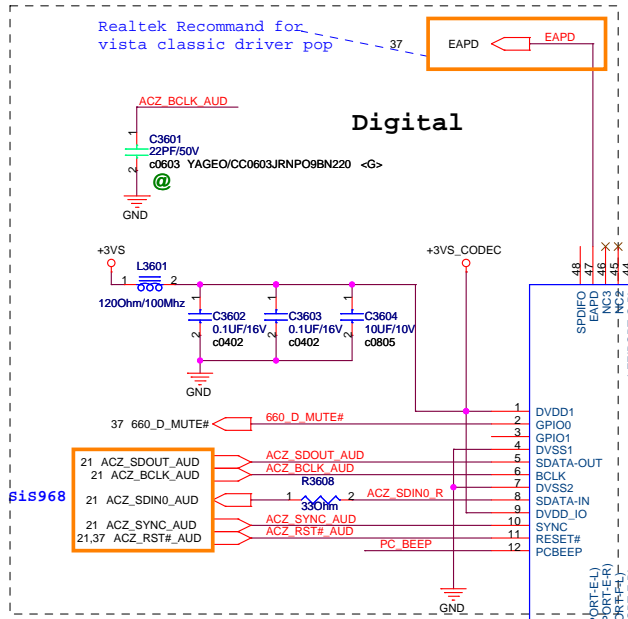
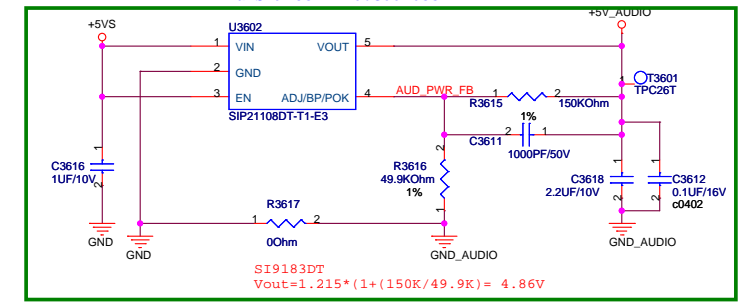


+5VS $= +5VS$ 30,32,37,38,46,50,51,56,57,80,91
 +5V_AUDIO $= +5V_AUDIO$ 38

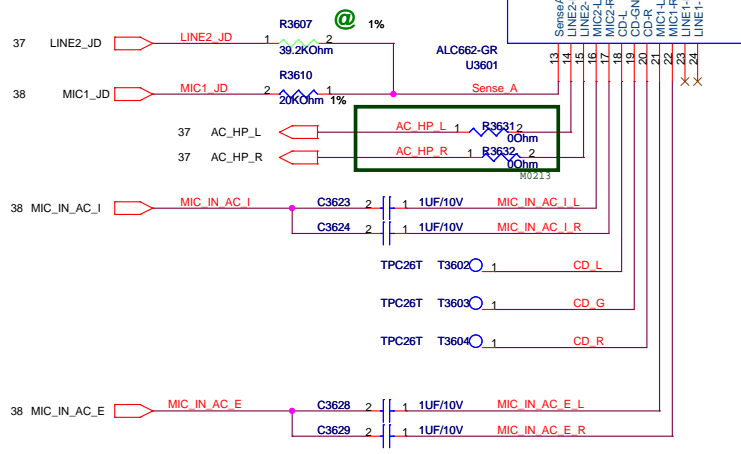
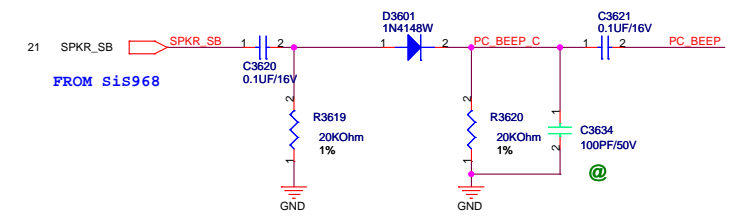
AUDIO POWER

R1.1
 2nd:SI9183DT 06G007055114

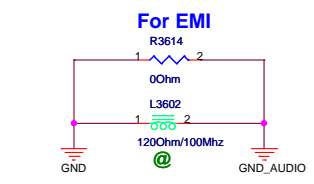
CODEC ALC662



PC BEEP



Input impedance: 64K ohm(Typical)

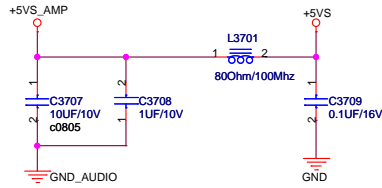


<Variant Name>

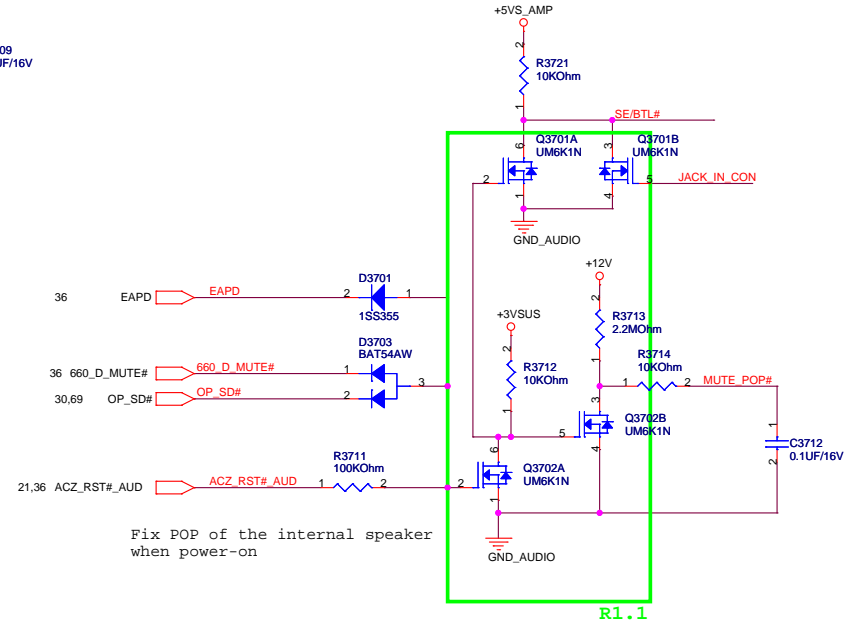
ASUS		Title : AUD_Codec ALC660(D)	
ASUSTek COMPUTER INC. NB1		Engineer: Bruce	
Size	Project Name	Rev	
Custom	T14C	1.1	
Date: Thursday, October 30, 2008	Sheet	36	of 94

AMP POWER

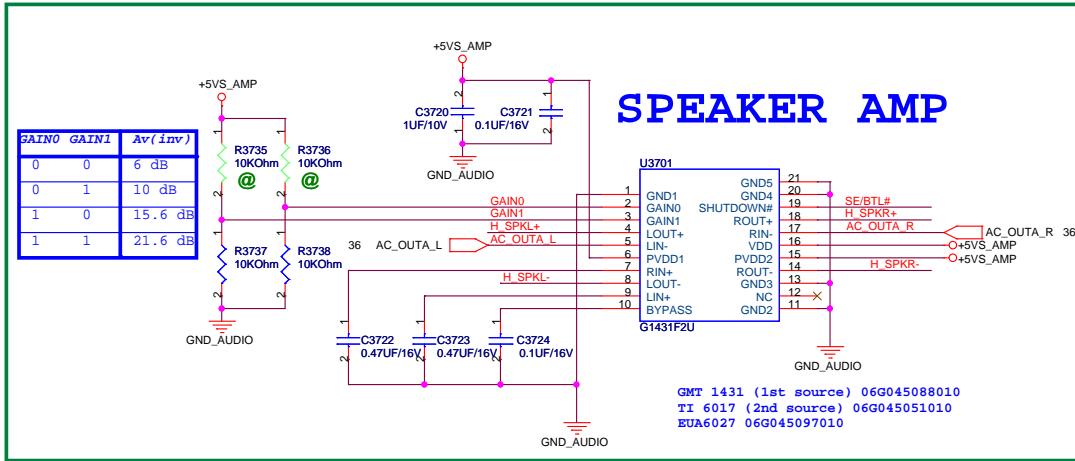
+5VSO +5VS 30,32,36,38,46,50,51,56,57,80,91



MUTE CONTROL



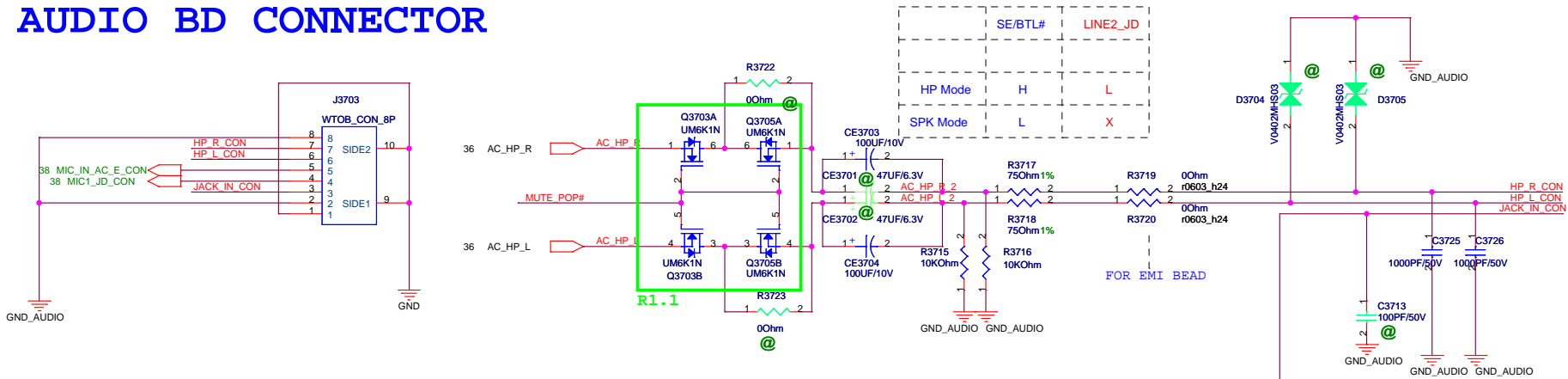
SPEAKER AMP



GMT 1431 (1st source) 06G045088010
TI 6017 (2nd source) 06G045051010
EUA6027 06G045097010

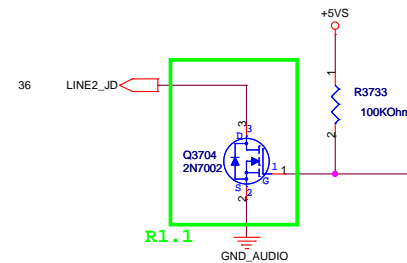
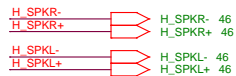
M0207

AUDIO BD CONNECTOR



HP CONN

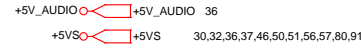
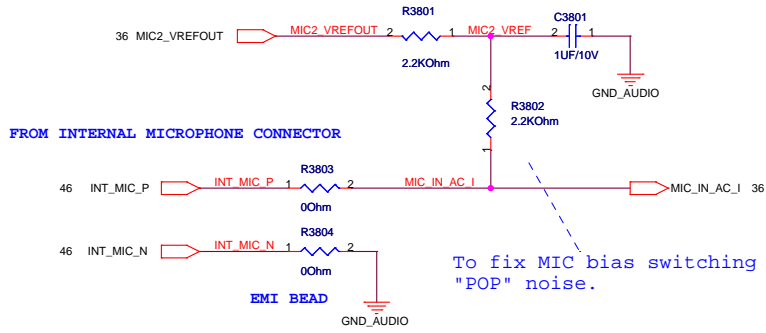
SPEAKER CONNECTOR



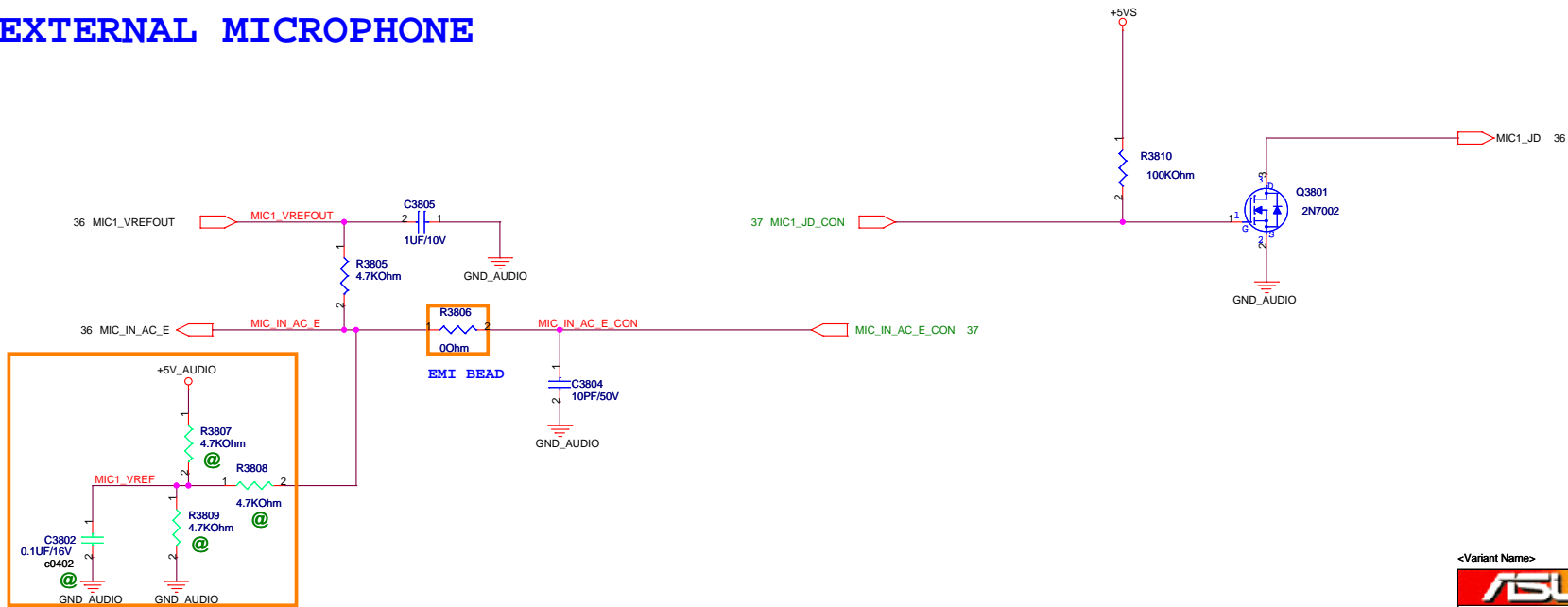
<-Variant Name>

ASUS		Title : AUDIO AMP	
ASUSTek COMPUTER INC. NB1		Engineer: Bruce	
Size	Project Name		
Custom	Z65		
Date: Thursday, October 30, 2008	Sheet 37 of 94	Rev 1.1	

INTERNAL MICROPHONE




EXTERNAL MICROPHONE

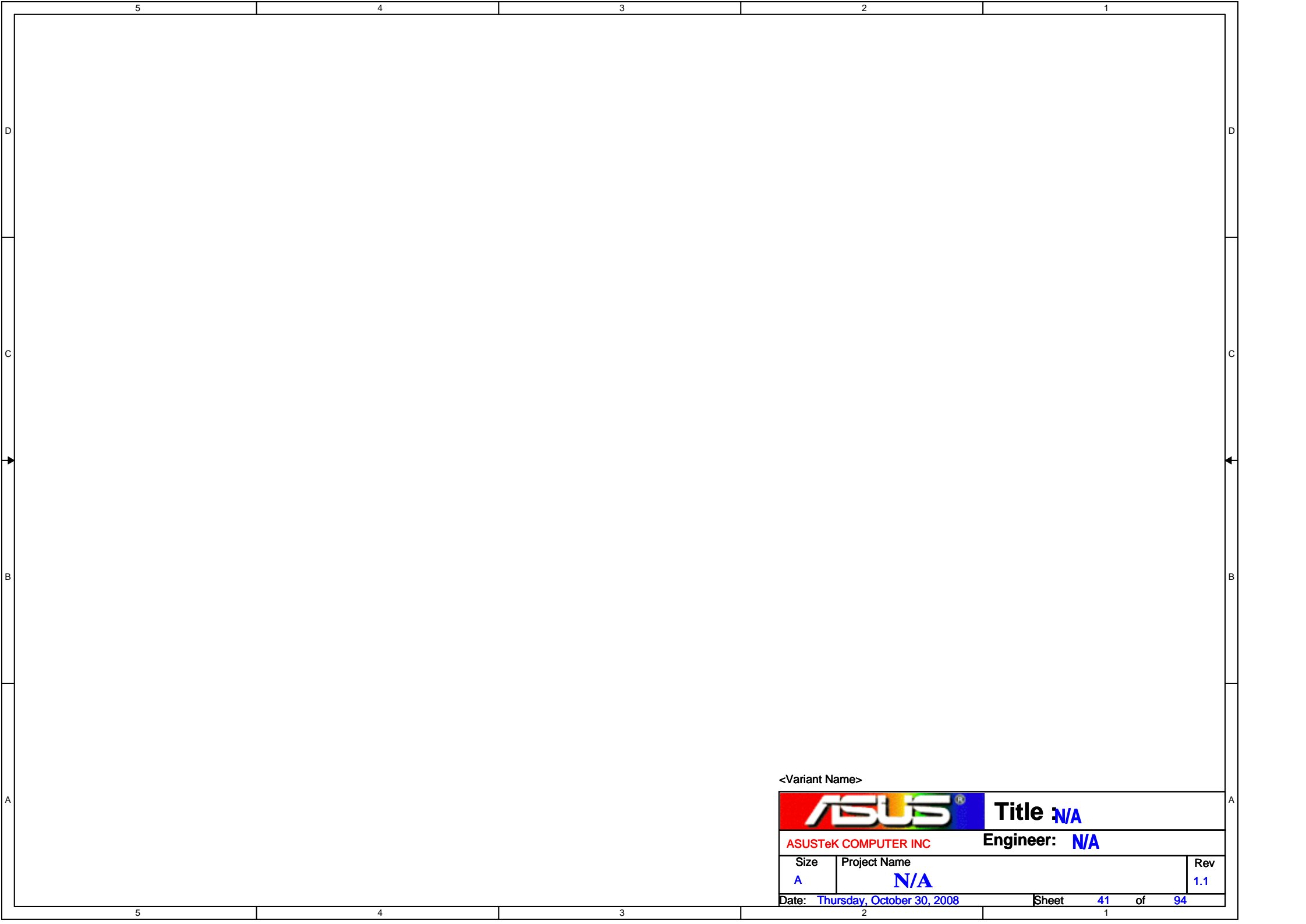


Reserved the external MIC bias(T filter).




<Variant Name>

		Title : Sub-Woofers (Empty)	
ASUSTek COMPUTER INC. NPI		Engineer: <i>Bruce</i>	
Size	Project Name	N/A	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Thursday, October 30, 2008	Sheet	39	of 94



<Variant Name>

		Title N/A	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A	N/A	1.1	
Date: Thursday, October 30, 2008		Sheet	41 of 94

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1

D

D

C

C

B

B

A

A

<Variant Name>



Title : **N/A**

ASUSTeK COMPUTER INC

Engineer: **N/A**

Size	Project Name	Rev
A	N/A	1.1

Date: **Thursday, October 30, 2008**

Sheet **42** of **94**

5

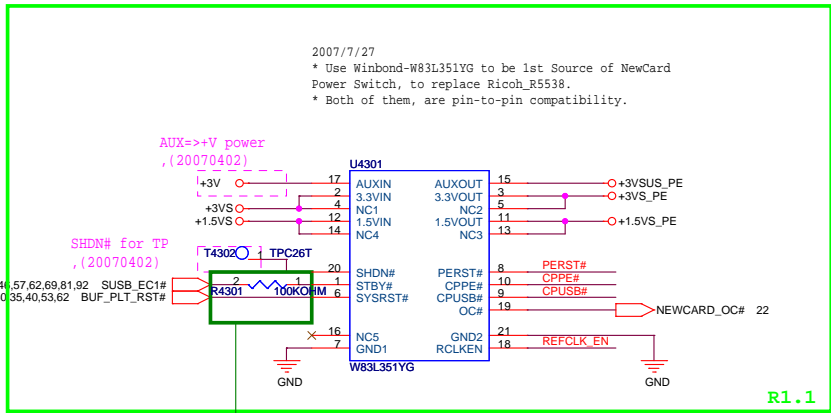
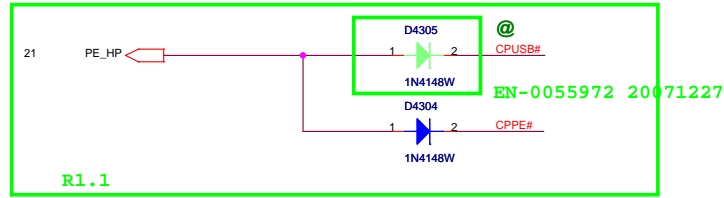
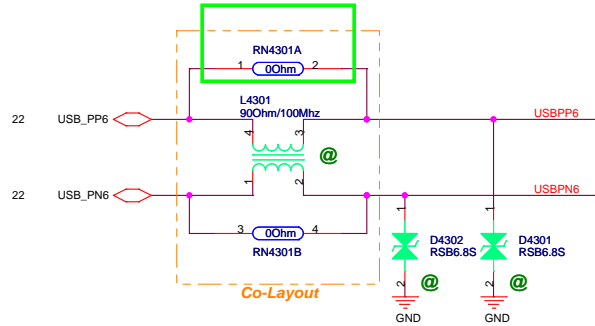
4

3

2

1

R2.0 RN4301 Stuff



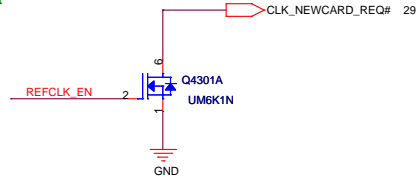
2007/7/27
 * Use Winbond-W83L351YG to be 1st Source of NewCard Power Switch, to replace Ricoh_R5538.
 * Both of them, are pin-to-pin compatibility.

AUX=>+V power
 ,(20070402)

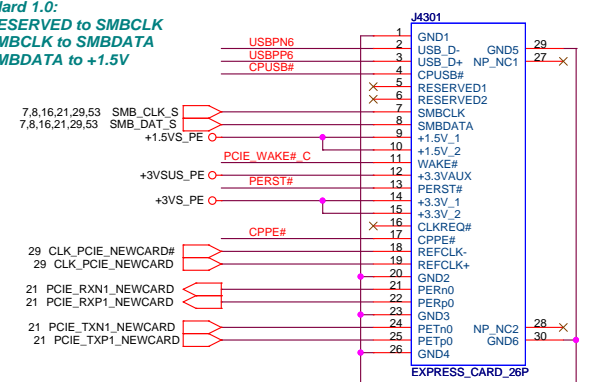
SHDN# for TP
 ,(20070402)

R1.1

Page43
 R2.0 Add R4301 when power on
 SUSB_EC1# leakage to U4301

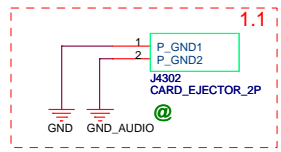


!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin6 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

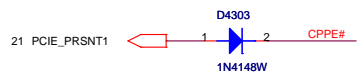
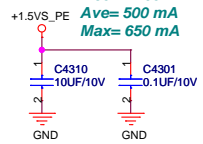
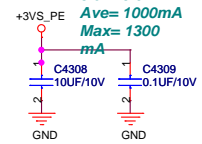
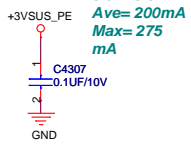
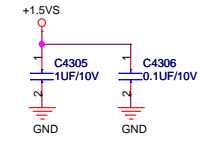
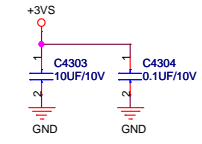
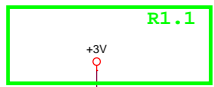


NewCard Header

12G161300261
 T14C



12G21C102603
 T14C



5

4

3

2

1

D

D

C

C

B

B

A

A



Title : CRT & DVI-I Conn.(Empty)

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
A	N/A	1.1

Date: Thursday, October 30, 2008

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5

4

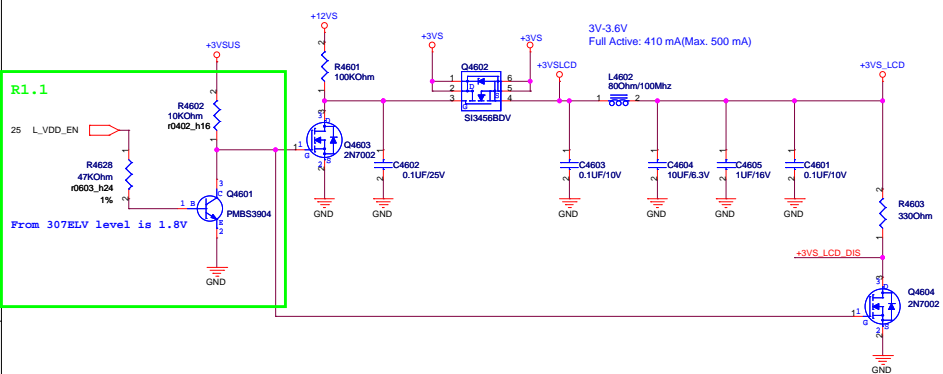
3

2

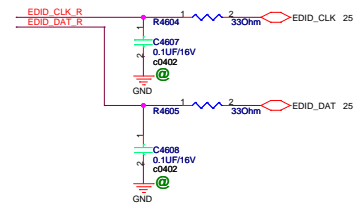
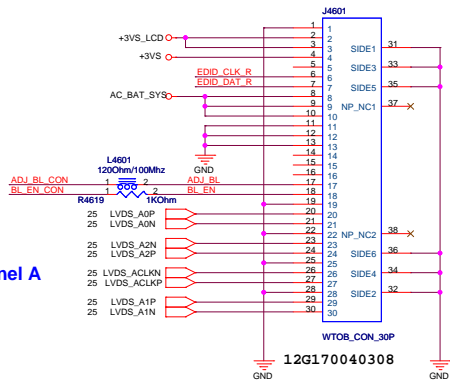
1

LCD Power

Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

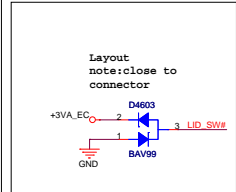
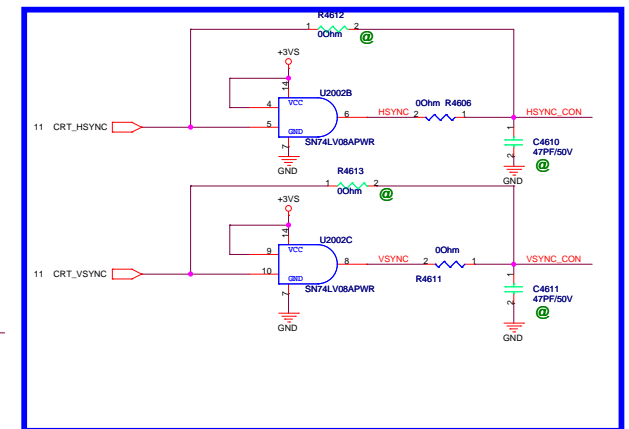
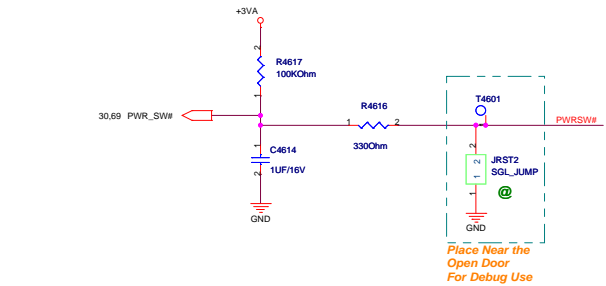
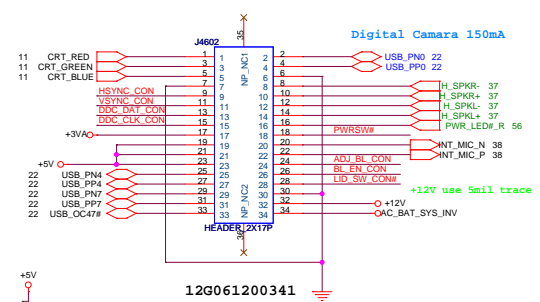


Channel A

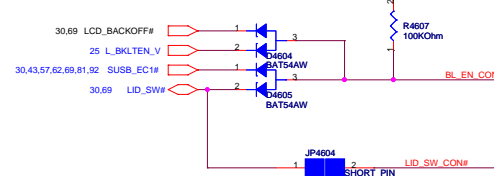
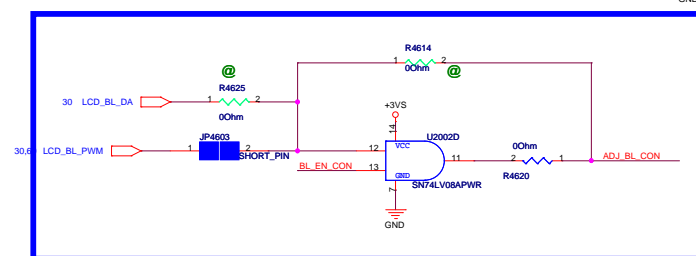
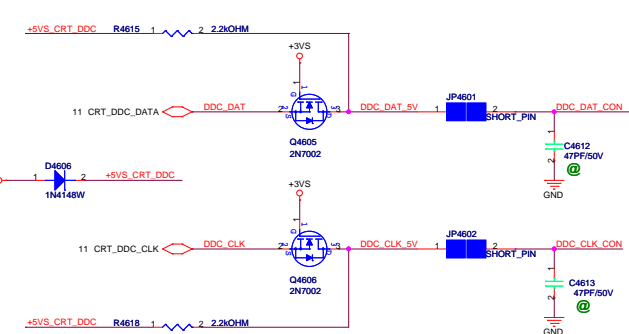


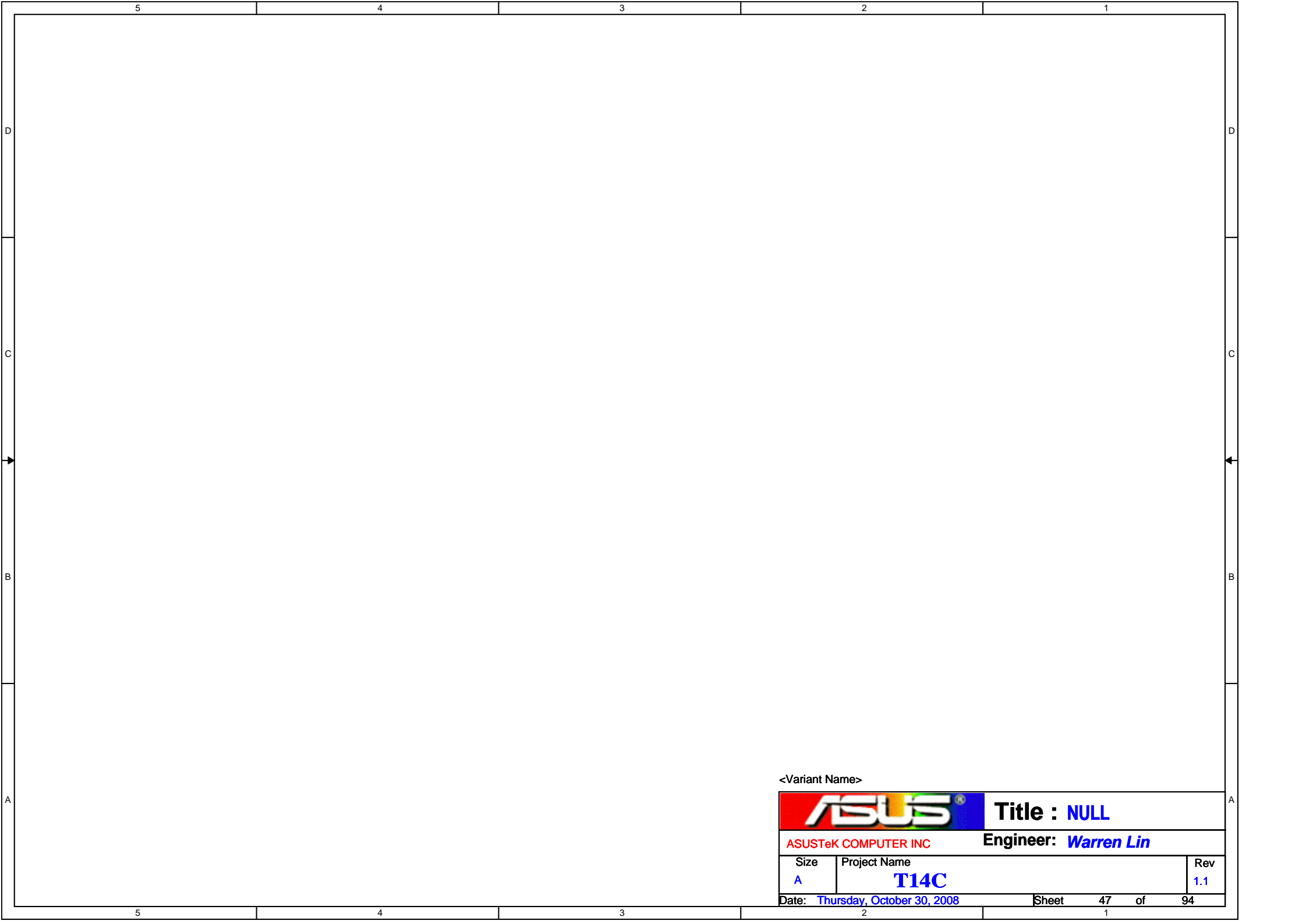
LCD LVDS Interface

BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.




BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.





<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 47 of 94

5

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		Title : NULL	
ASUSTek COMPUTER INC NPI		Engineer: <i>Warren Lin</i>	
Size	Project Name		Rev
Custom	P/N	T14C	1.1
Date: Thursday, October 30, 2008		<OrgAddr2>	
		Sheet	48 of 94

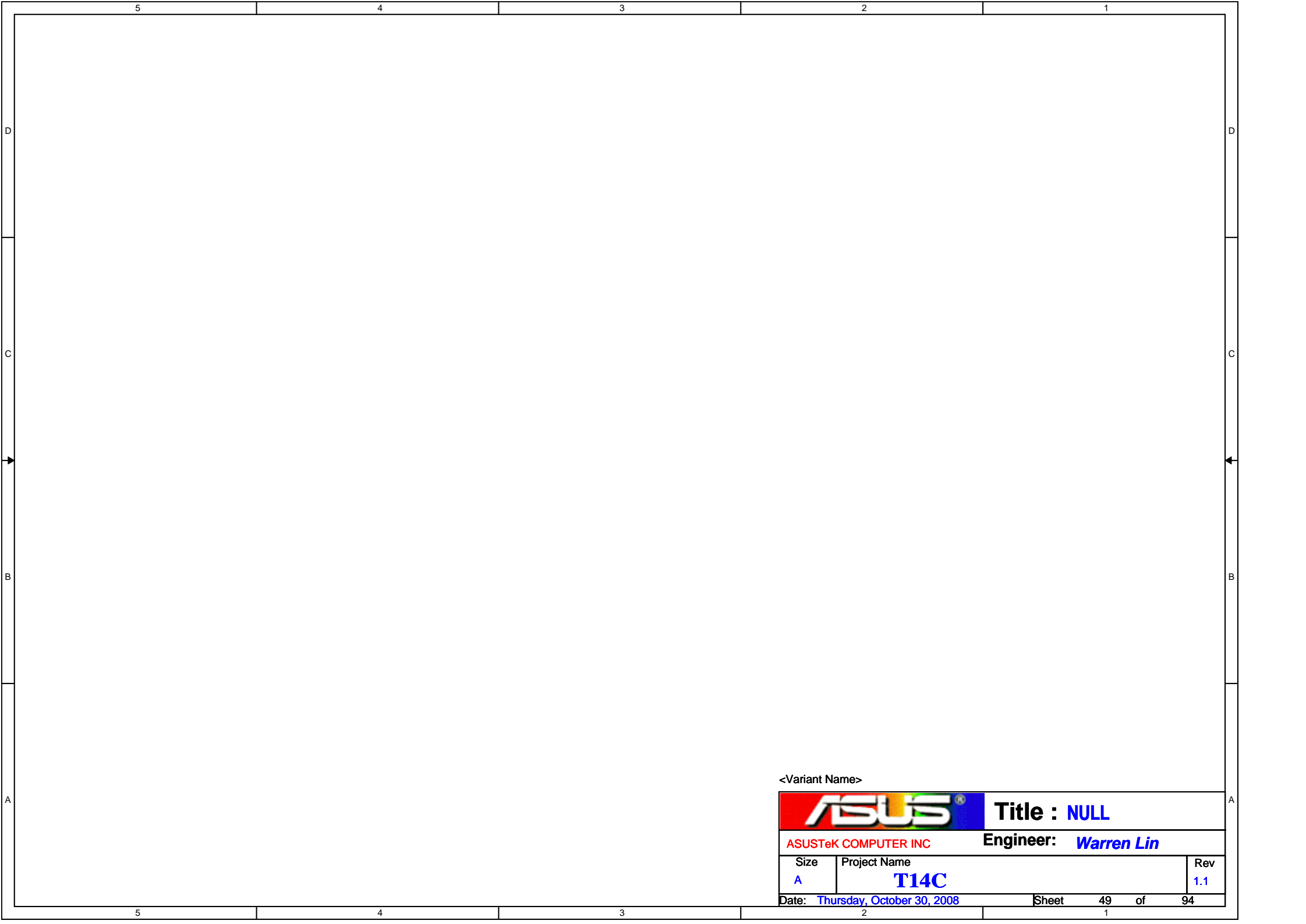
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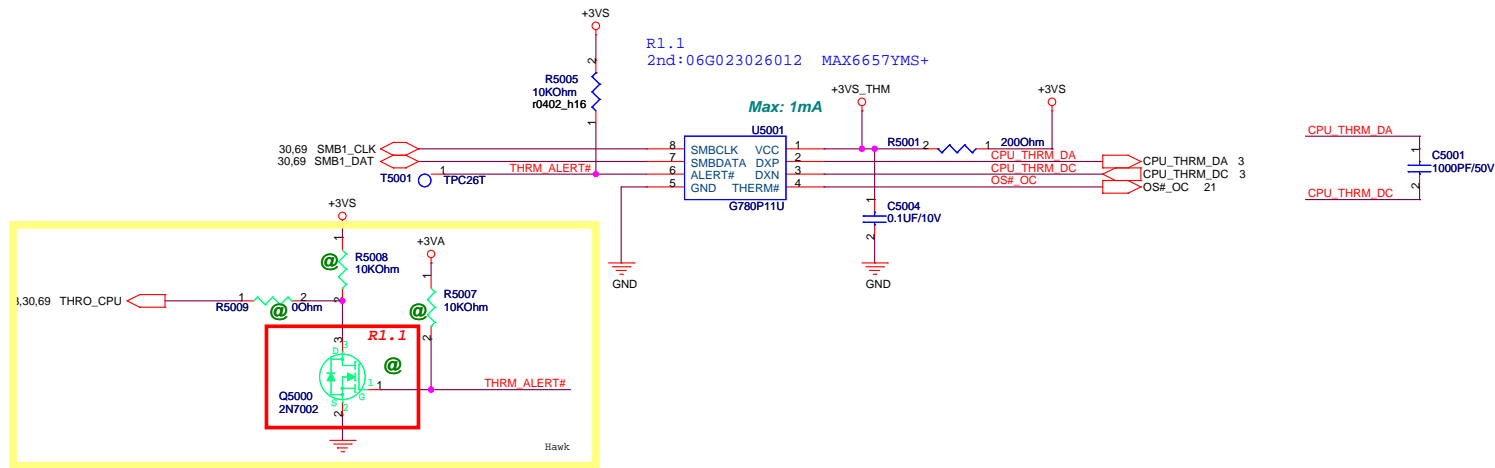
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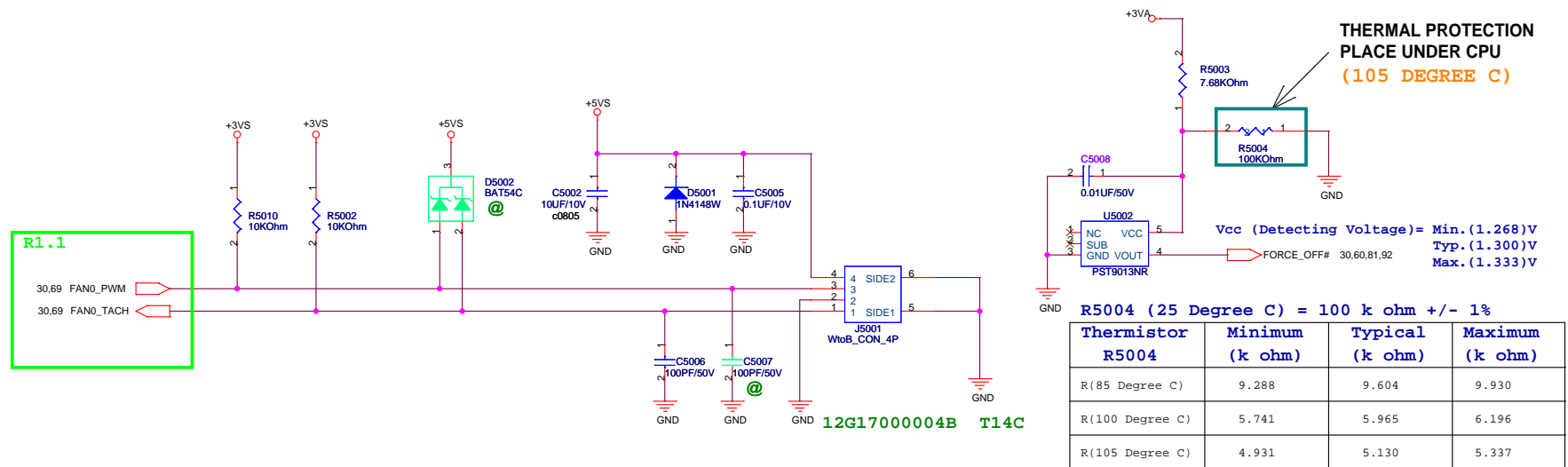
<Variant Name>



		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 49 of 94

Thermal Sensor



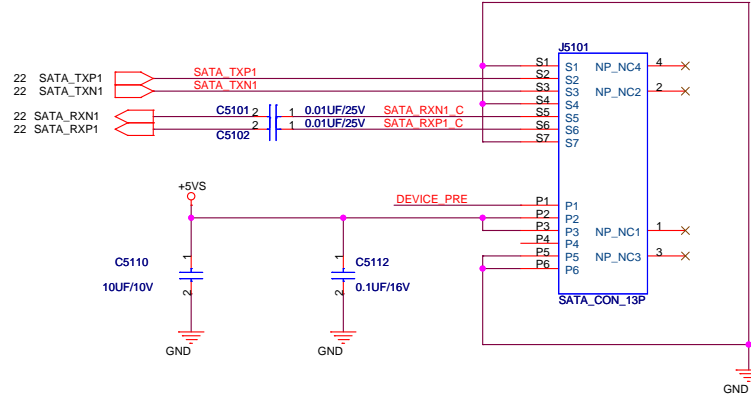
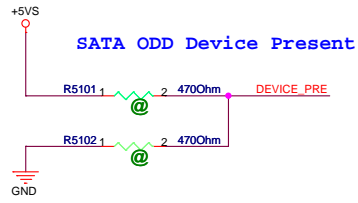
DC FAN Control



+3VS  +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,43,46,50,53,56,57,62,80,91,92
 +5VS  +5VS 30,32,36,37,38,46,50,56,57,80,91

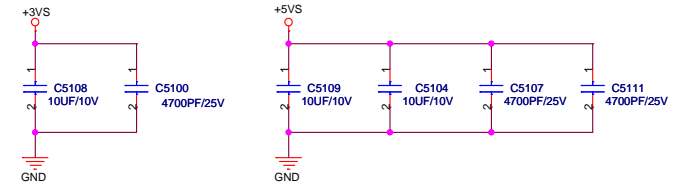
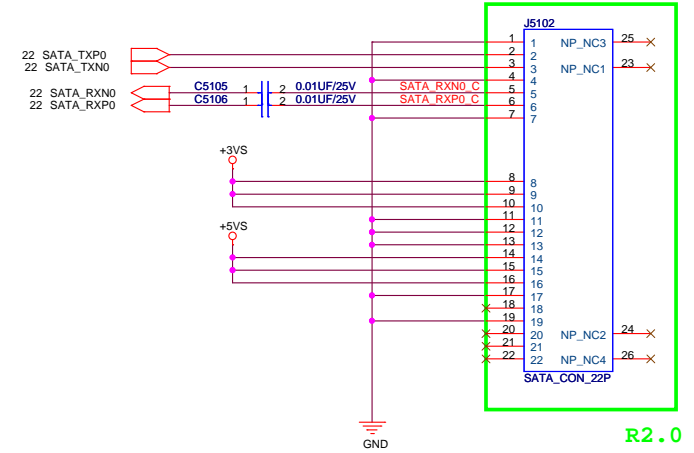
SATA ODD

12G15100013K/12G15100013R



SATA HDD

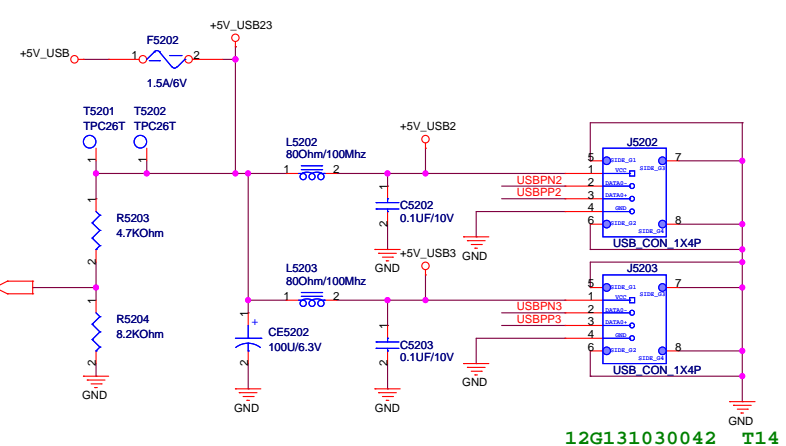
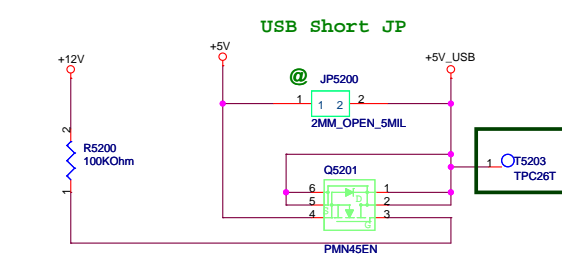
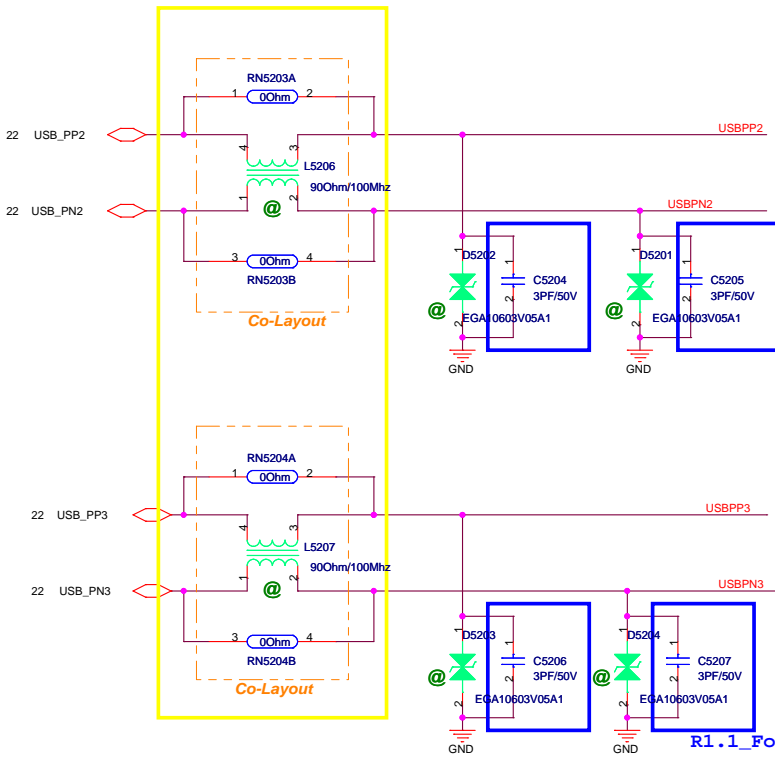
T14C 12G152000226



<Variant Name>

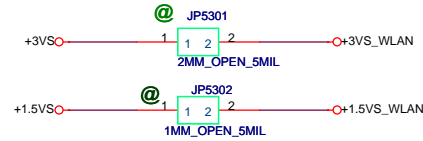
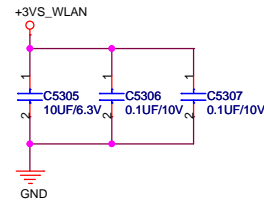
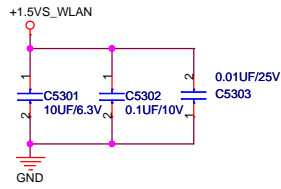
		Title : HDD & CDROM	
ASUSTeK COMPUTER INC		Engineer: Bruce	
Size	Project Name	Rev	
Custom	Z65	1.1	
Date: Thursday, October 30, 2008	Sheet	51	of 94

+5V +5V 46,56,57,83,91
 +12V +12V 37,46,61,91

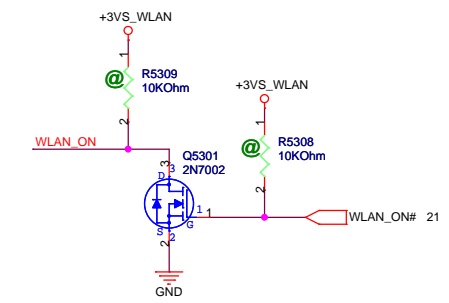
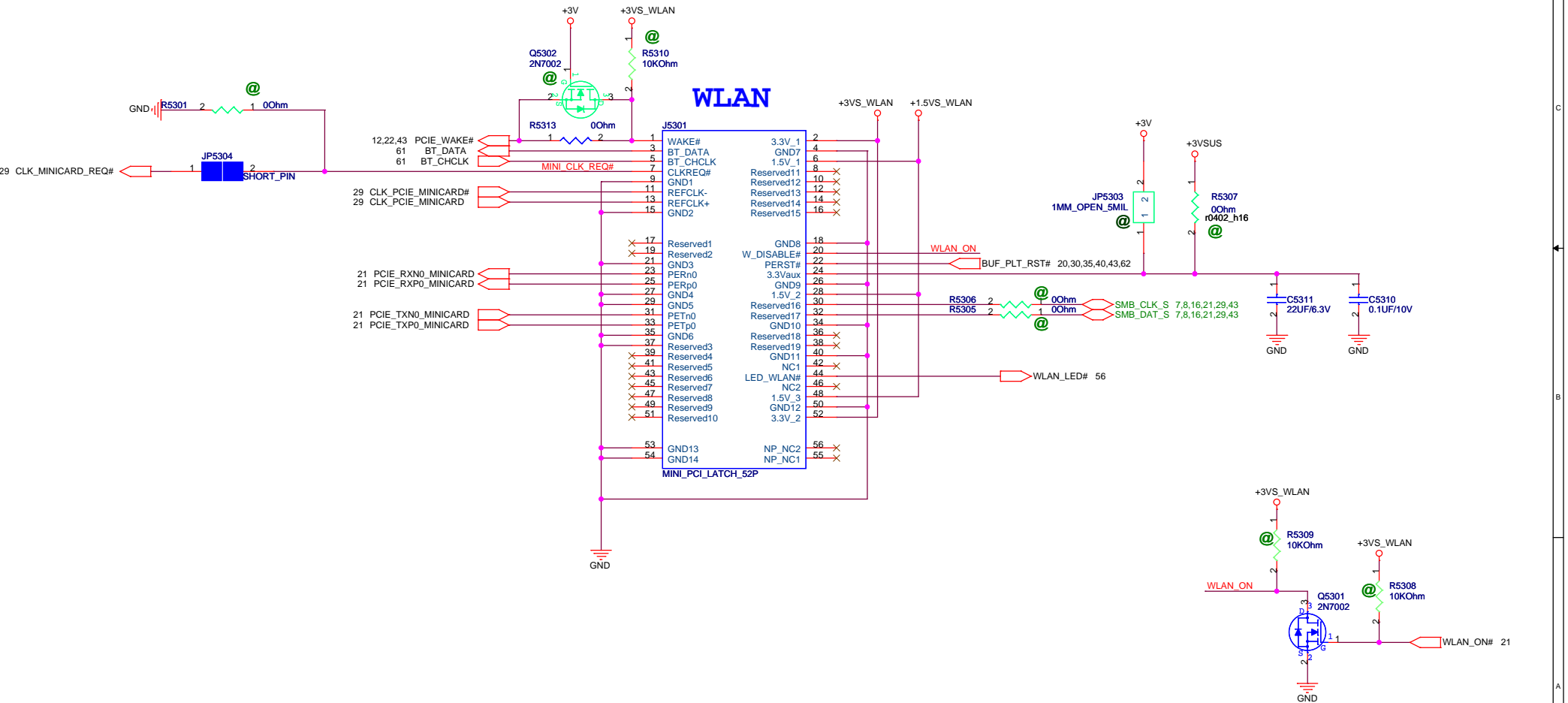


RI.1_For USB Rise/Fall time fast issue

		Title : USB CONN X 4	
		ASUSTeK COMPUTER INC. NB Engineer: Bruce	
Size	Project Name	Rev	
Custom	Z65	1.1	
Date: Thursday, October 30, 2008	Sheet	52	of 94

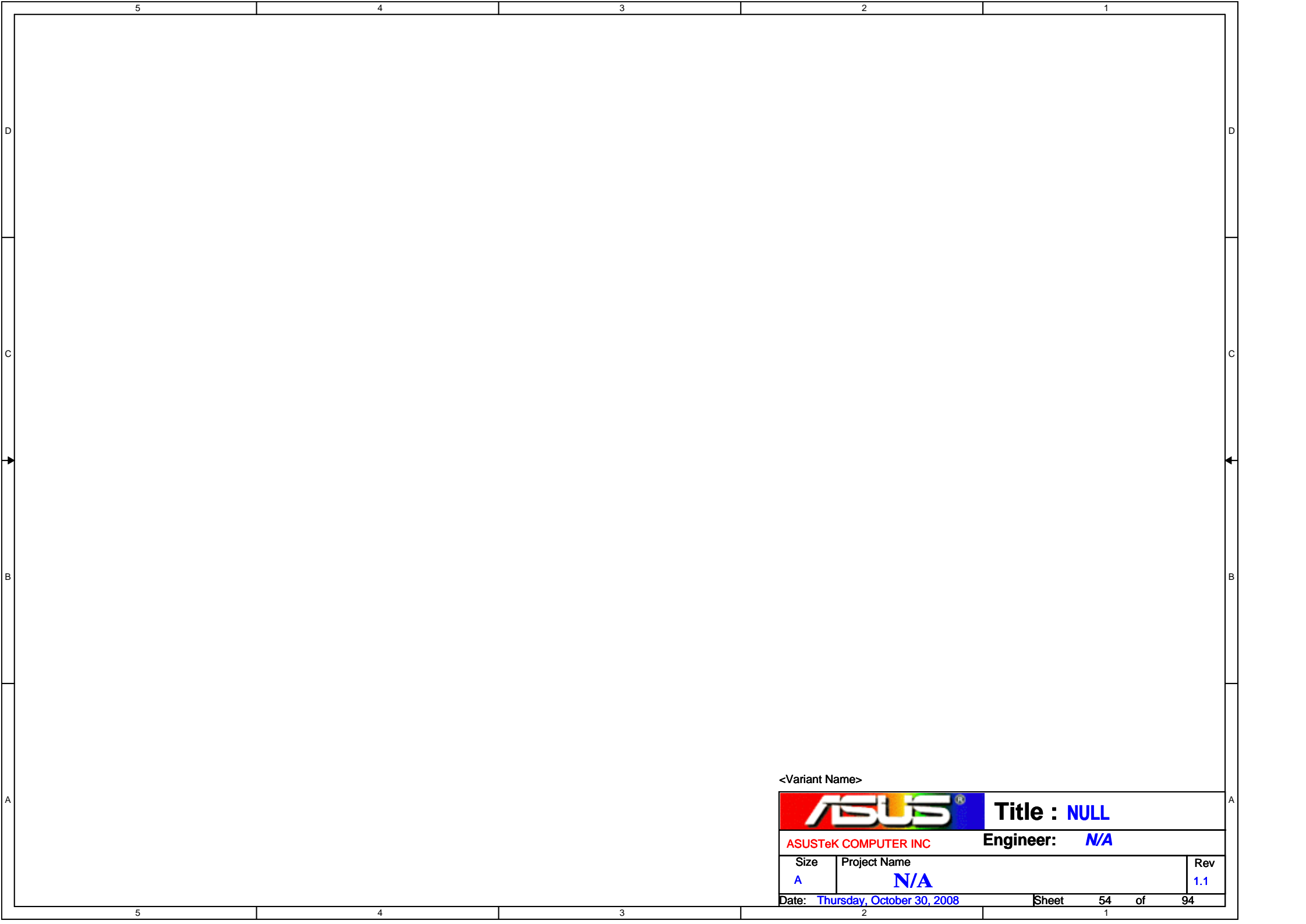


+3VS	+3VS	3,7,8,11,20,21,22,23,25,29,30,32,36,43,46,50,51,56,57,62,80,91,92
+3V	+3V	32,35,40,43,44,57,61,62,91
+1.5VS	+1.5VS	4,11,43,57,83




<Variant Name>

ASUS		Title : MINICARD
ASUSTek COMPUTER INC		Engineer: Bruce
Size	Project Name	Rev
Custom	Z65	1.1
Date: Thursday, October 30, 2008	Sheet 53 of 94	



<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: N/A
Size	Project Name	Rev
A	N/A	1.1
Date: Thursday, October 30, 2008		Sheet 54 of 94

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<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
A	N/A	1.1

Date: Thursday, October 30, 2008

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5

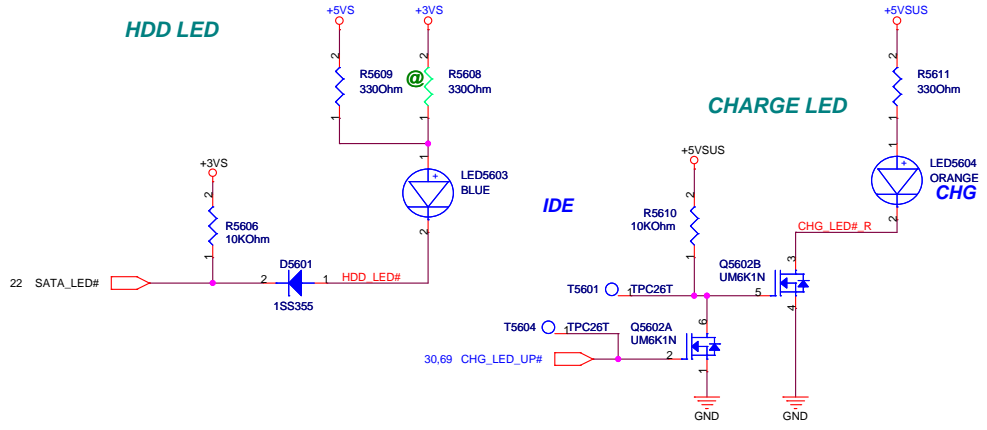
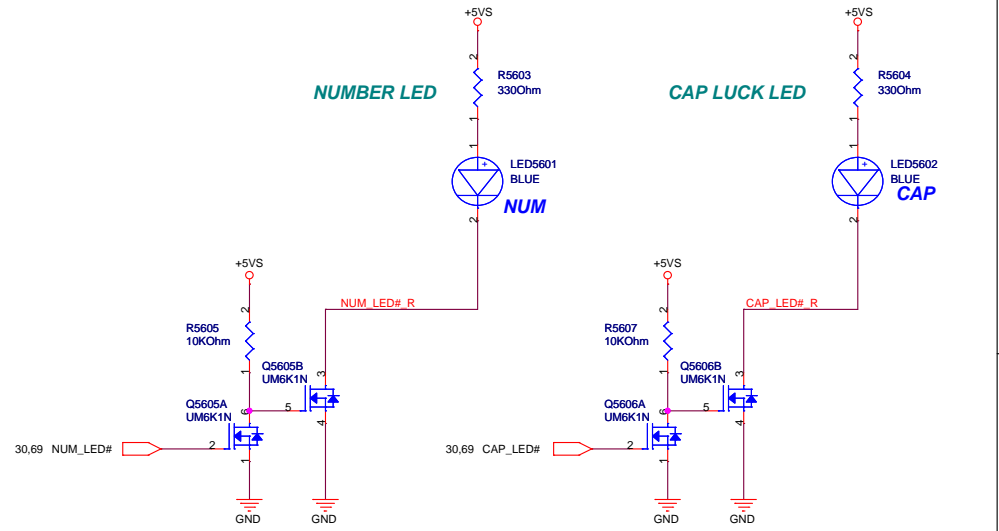
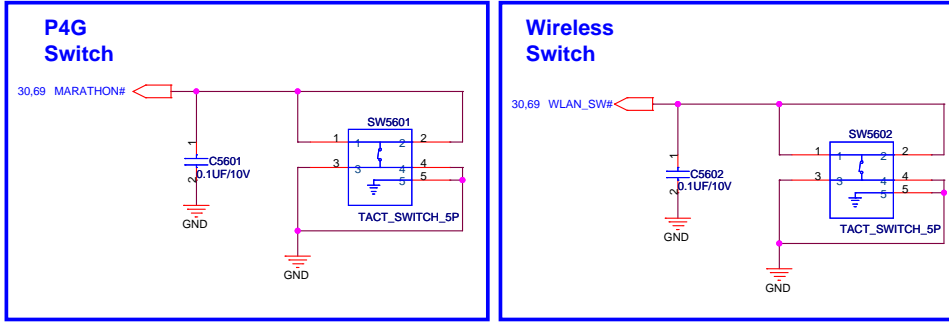
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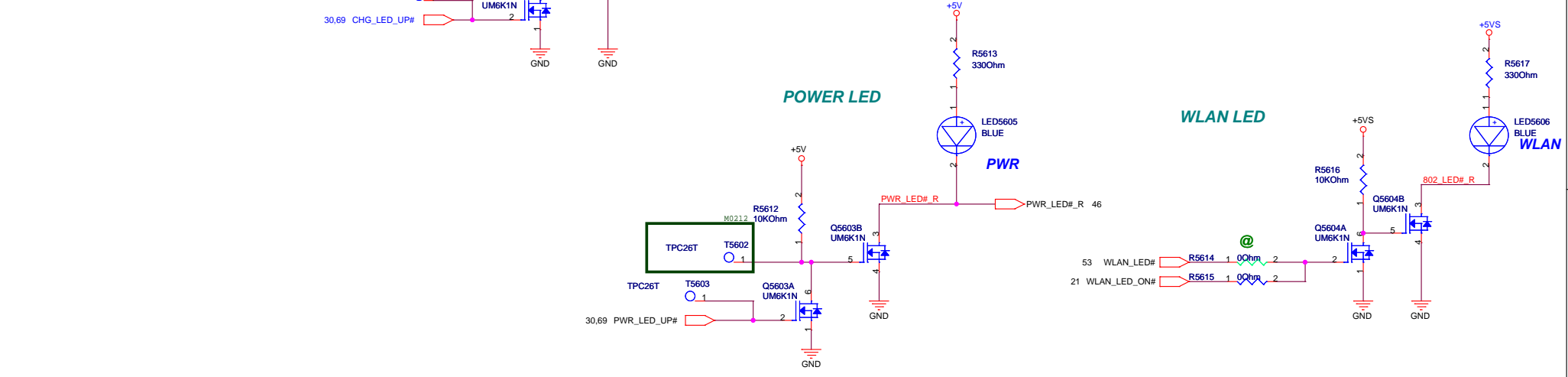
2










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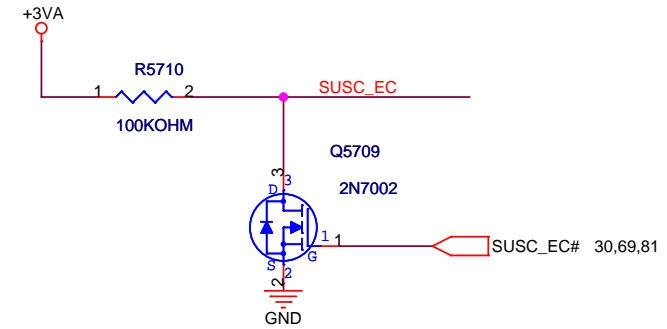
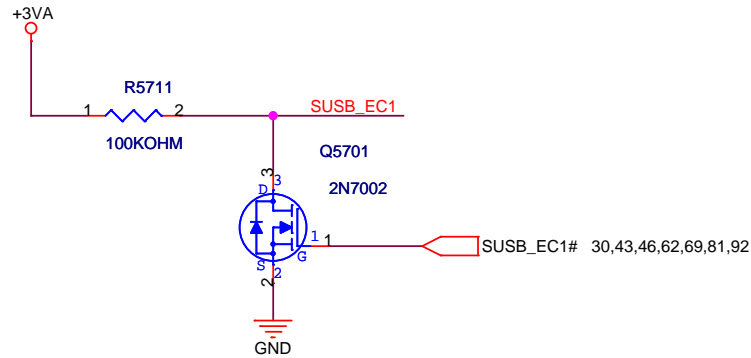
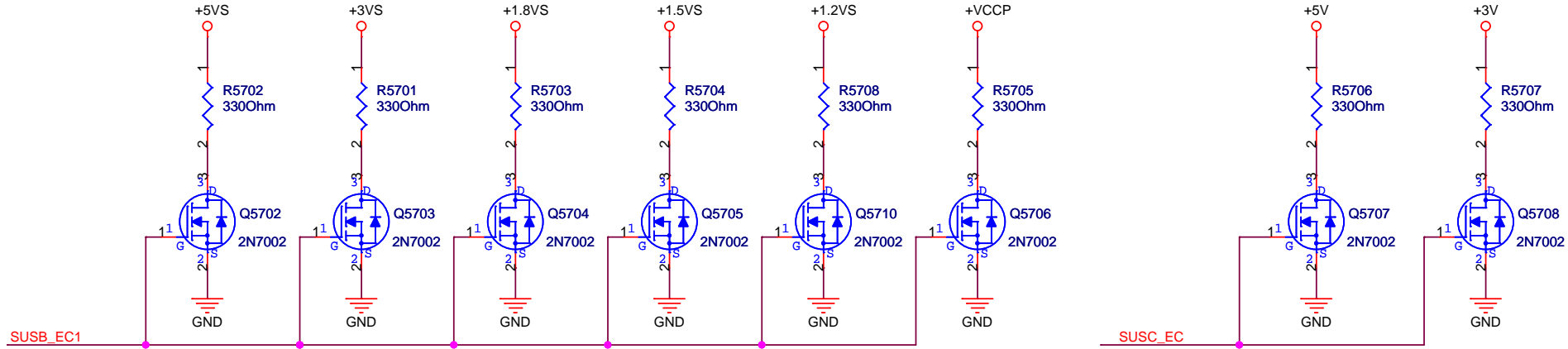
Main Board SW & LED



-LED Change Blue 07G015L00036



- +3VA  +3VA 21,30,46,50,60,81
- +3V  +3V 32,35,40,43,44,53,61,62,91
- +5V  +5V 46,52,56,83,91
- +VCCP  +VCCP 4,10,14,21,23,29,82
- +1.5VS  +1.5VS 4,11,43,53,83
- +3VS  +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,43,46,50,51,53,56,62,80,91,92
- +5VS  +5VS 30,32,36,37,38,46,50,51,56,80,91
- +1.8VS  +1.8VS 10,11,13,14,16,20,21,22,23,25,83,91
- +1.2VS  +1.2VS 12,14,91



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<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Warren Lin	
Size	Project Name	Rev	
Custom	T14C	1.1	
Date: Thursday, October 30, 2008		Sheet	58 of 94

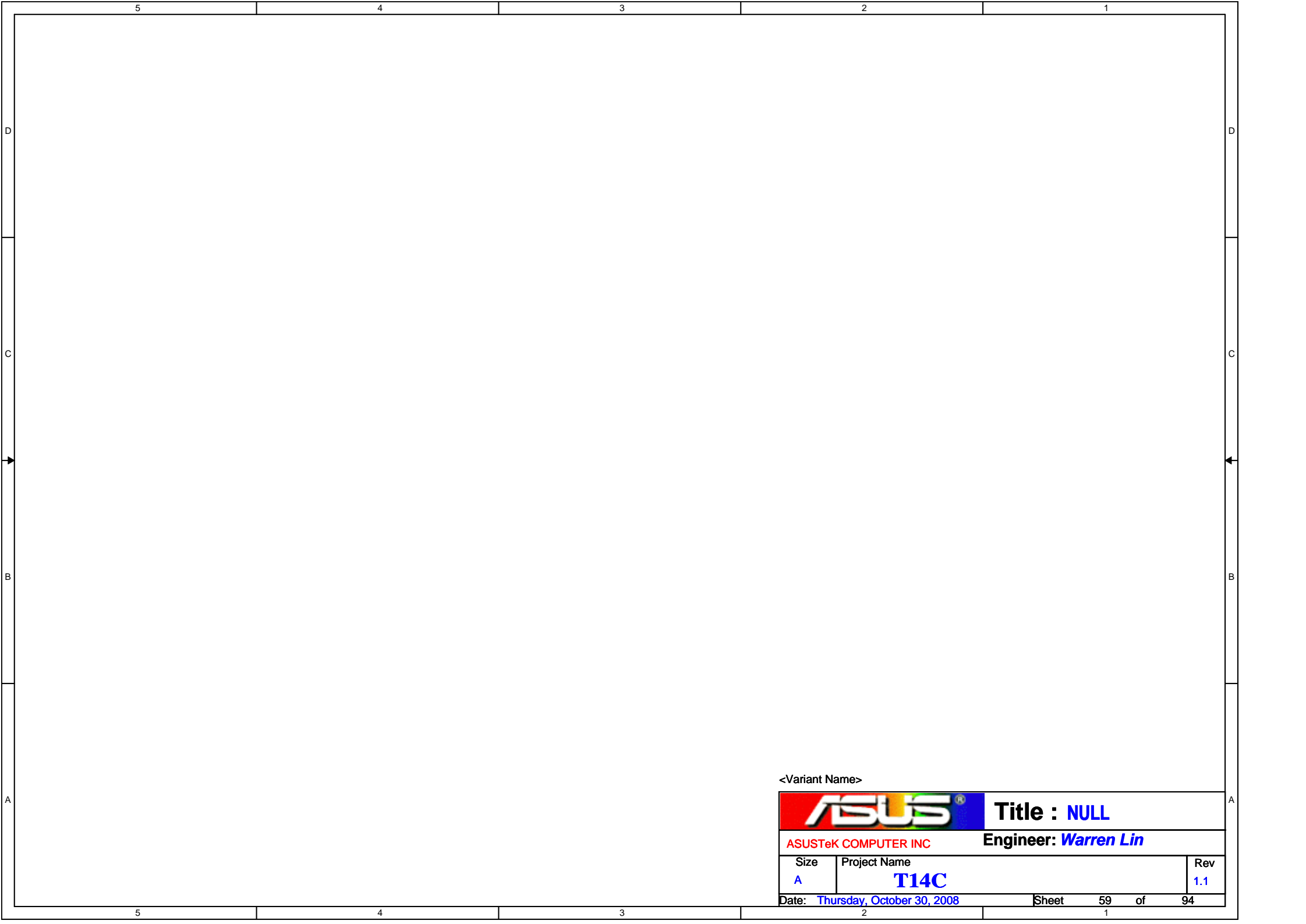
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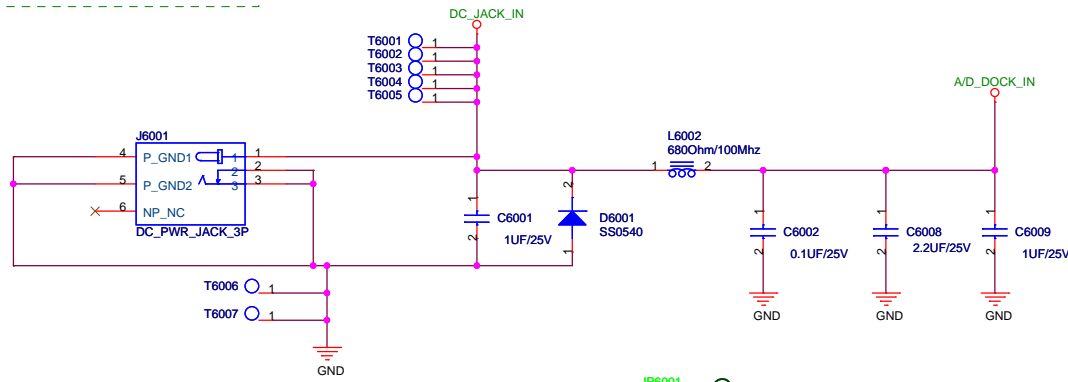
1



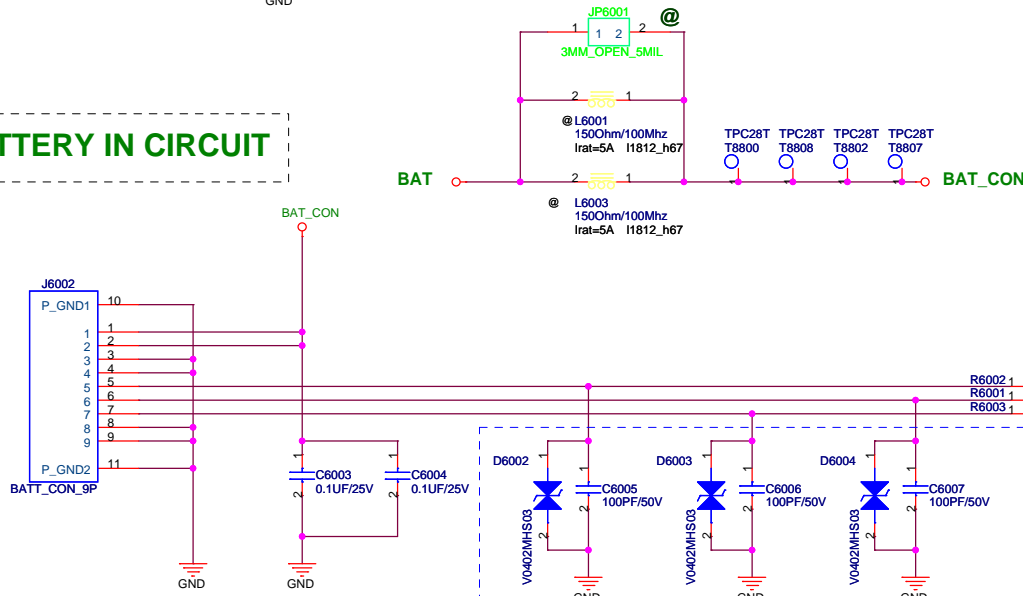
<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size	Project Name	Rev
A	T14C	1.1
Date: Thursday, October 30, 2008		Sheet 59 of 94

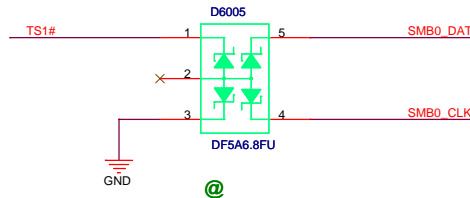
Adaptor IN Circuit



BATTERY IN CIRCUIT

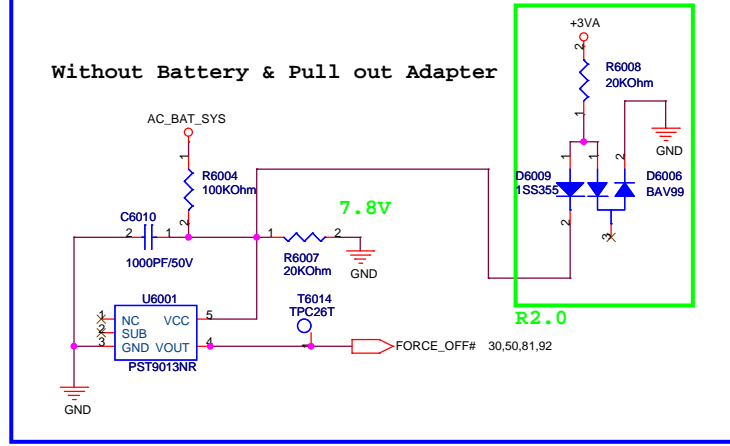


Layout Note:
Close to connector.



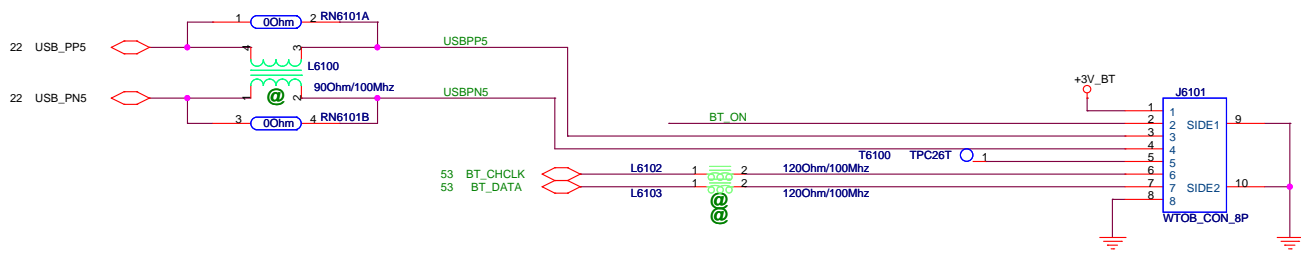
For cost issue and the specification does not meet the design.
Reserve the varistor DF5A6.8FU(07G001023010) in schematics.

Without Battery & Pull out Adapter

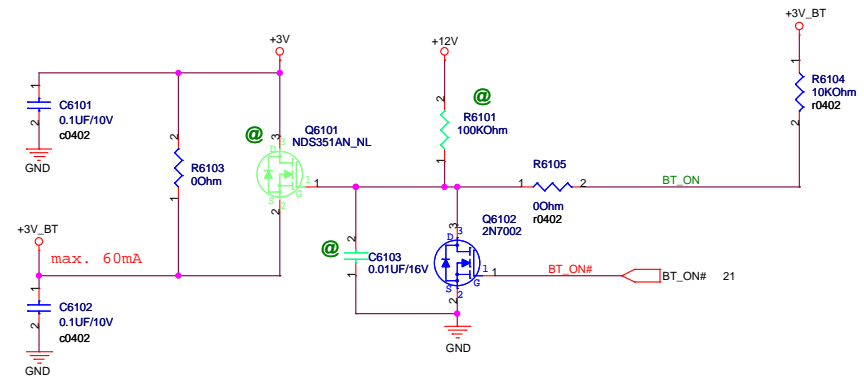


- AC_BAT_SYS AC_BAT_SYS 46,80,81,82,83,88
- BAT BAT 88
- A/D_DOCK_IN A/D_DOCK_IN 88,90

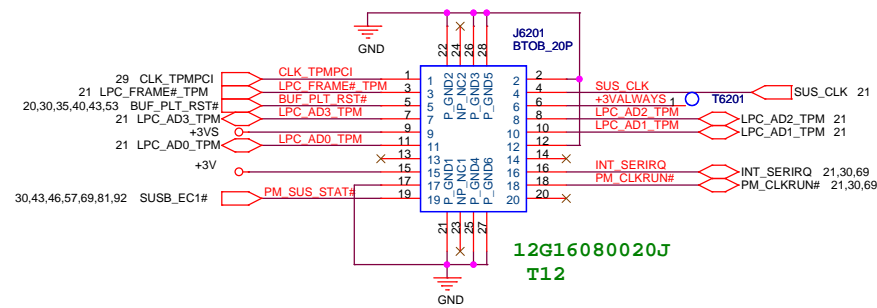
BLUETOOTH CONNECTOR



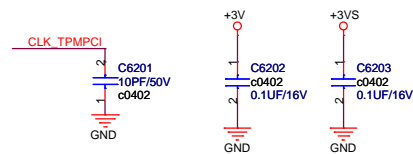
12G17101010L T12
12G170010083 T14



TPM Connector



+3VS +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,43,46,50,51,53,56,57,80,91,92
 +3V +3V 32,35,40,43,44,53,57,61,91



<Variant Name>

		Title : TPM	
ASUSTeK COMPUTER INC. NB		Engineer: Bruce	
Size	Project Name		Rev
Custom	Z65		1.1
Date: Thursday, October 30, 2008		Sheet	62 of 94



<Variant Name>



Title : Finger Print(Empty)

ASUSTeK COMPUTER INC. NB

Engineer: Bruce


Size	Project Name	Rev
Custom	Z65	1.1

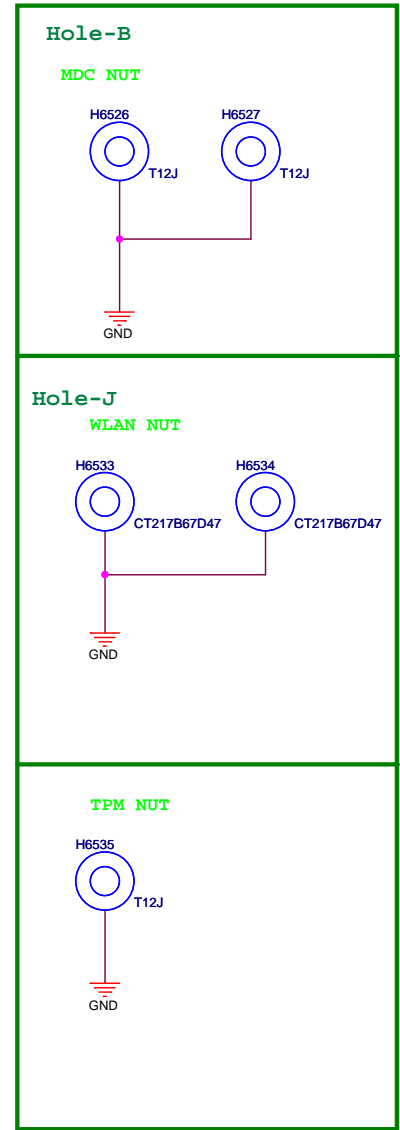
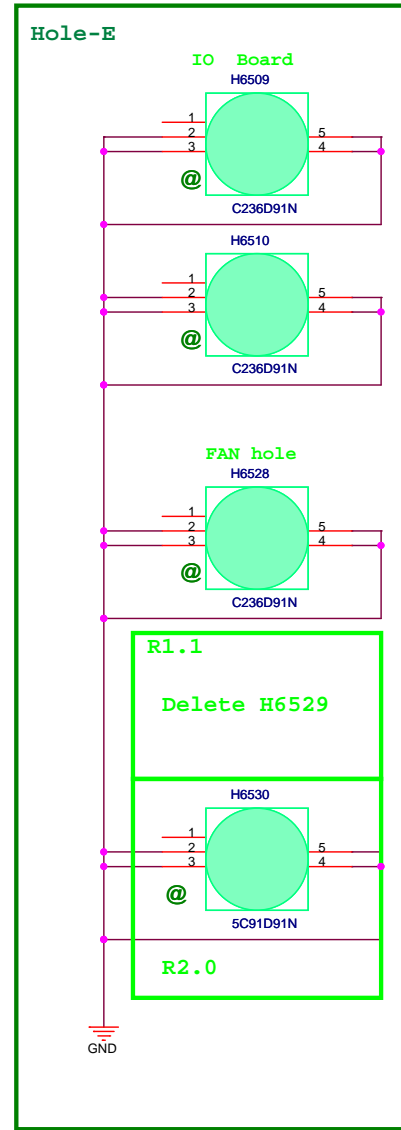
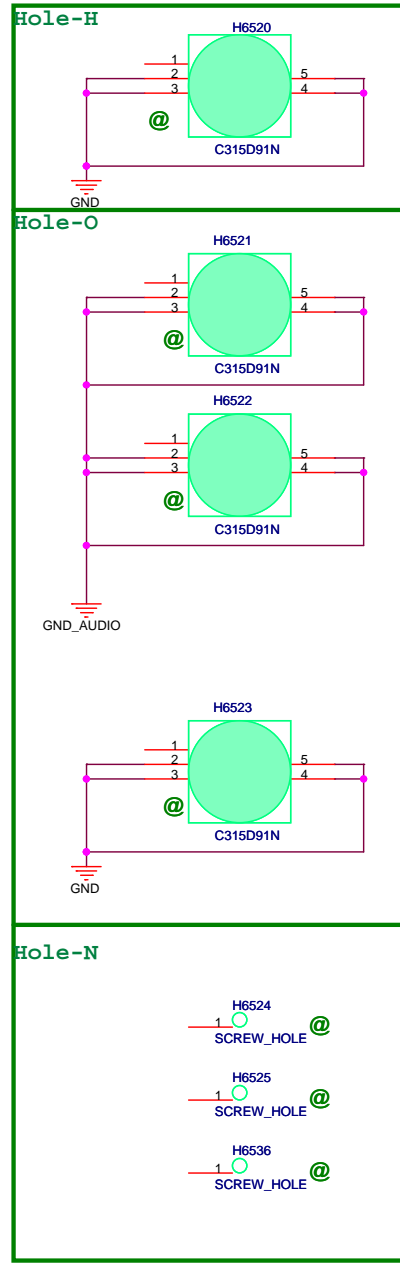
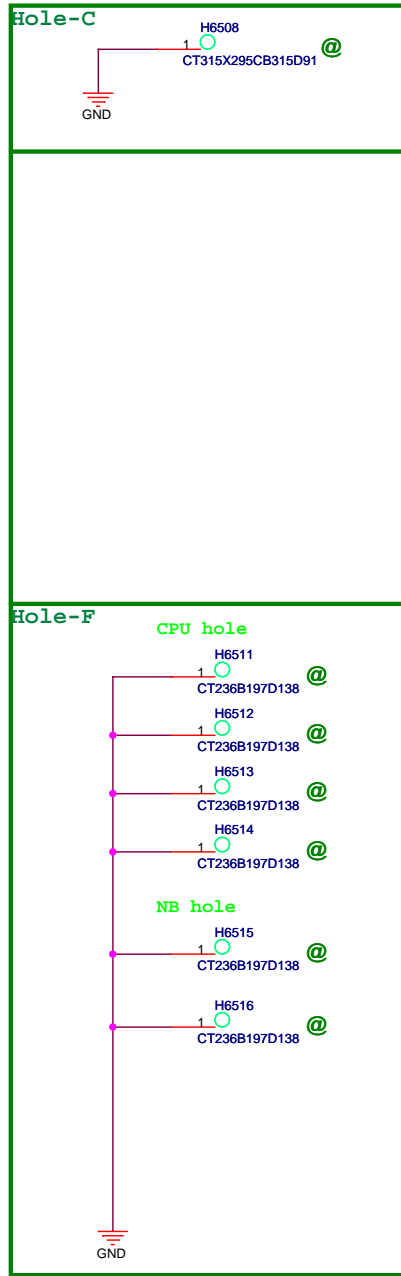
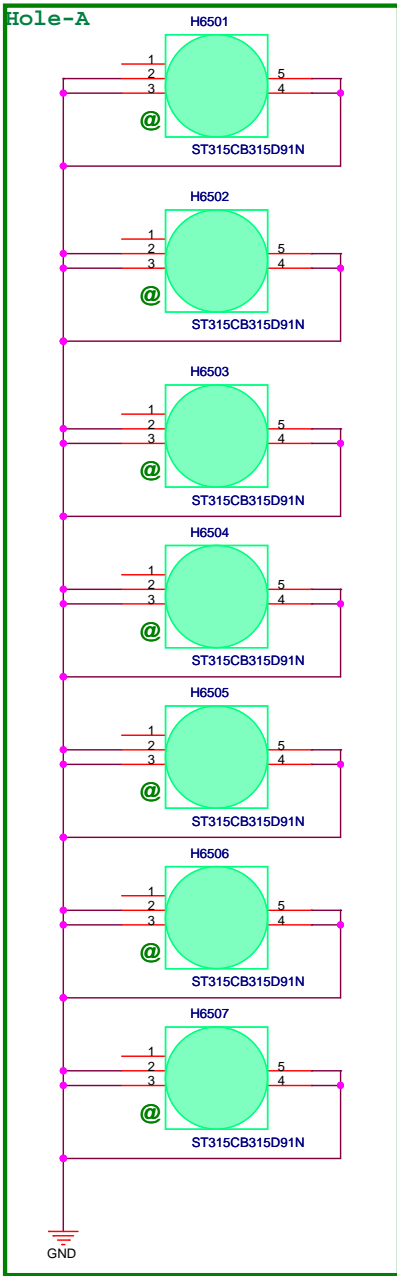
Date: Thursday, October 30, 2008

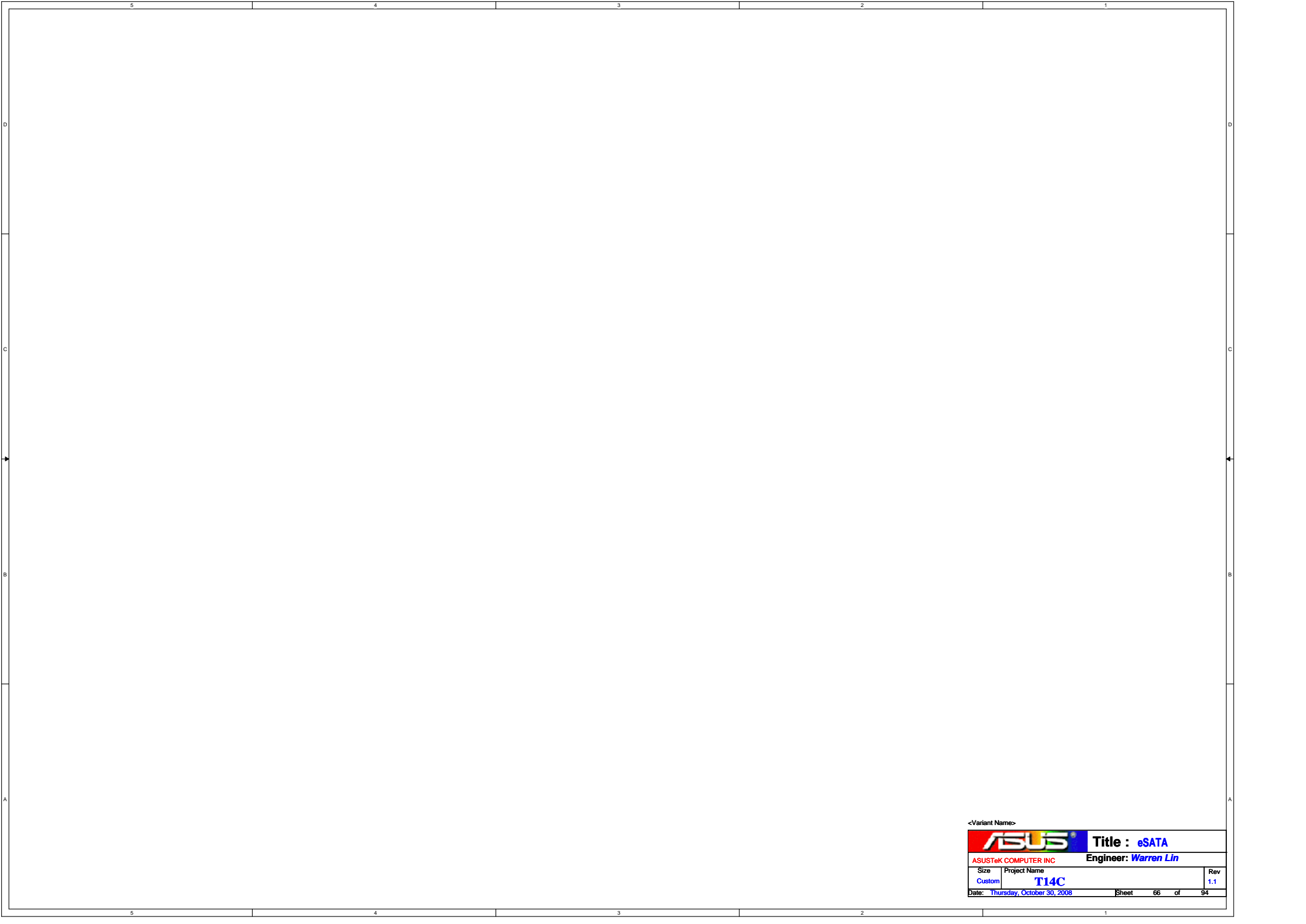
Sheet 63 of 94




<Variant Name>

		Title : NULL
ASUSTek COMPUTER INC		Engineer: N/A
Size	Project Name	Rev
Custom	N/A	1.1
Date: Thursday, October 30, 2008		Sheet 64 of 94



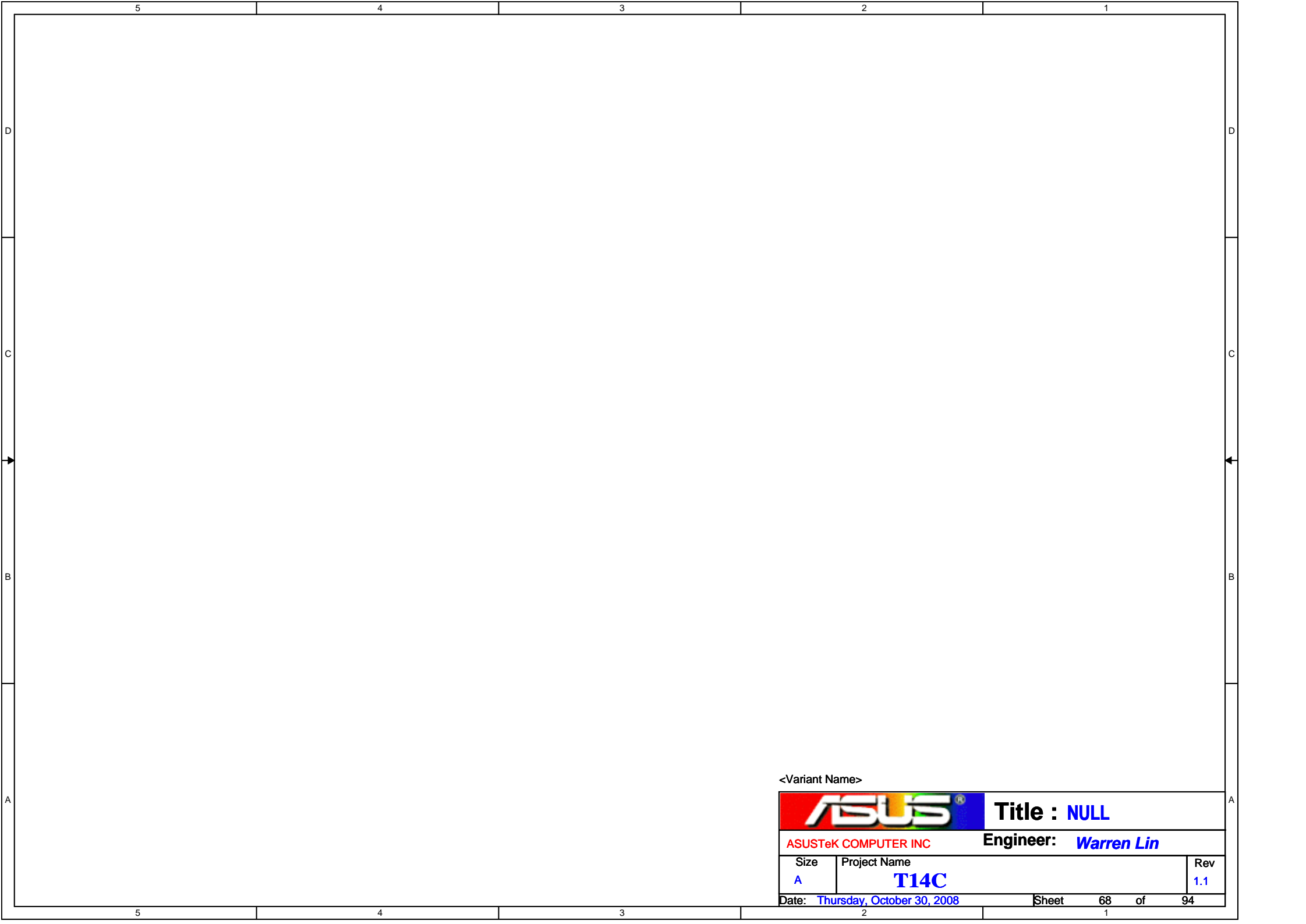


<Variant Name>


		Title : eSATA	
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>	
Size	Project Name	Rev	
Custom	T14C	1.1	
Date: Thursday, October 30, 2008	Sheet	66	of 94

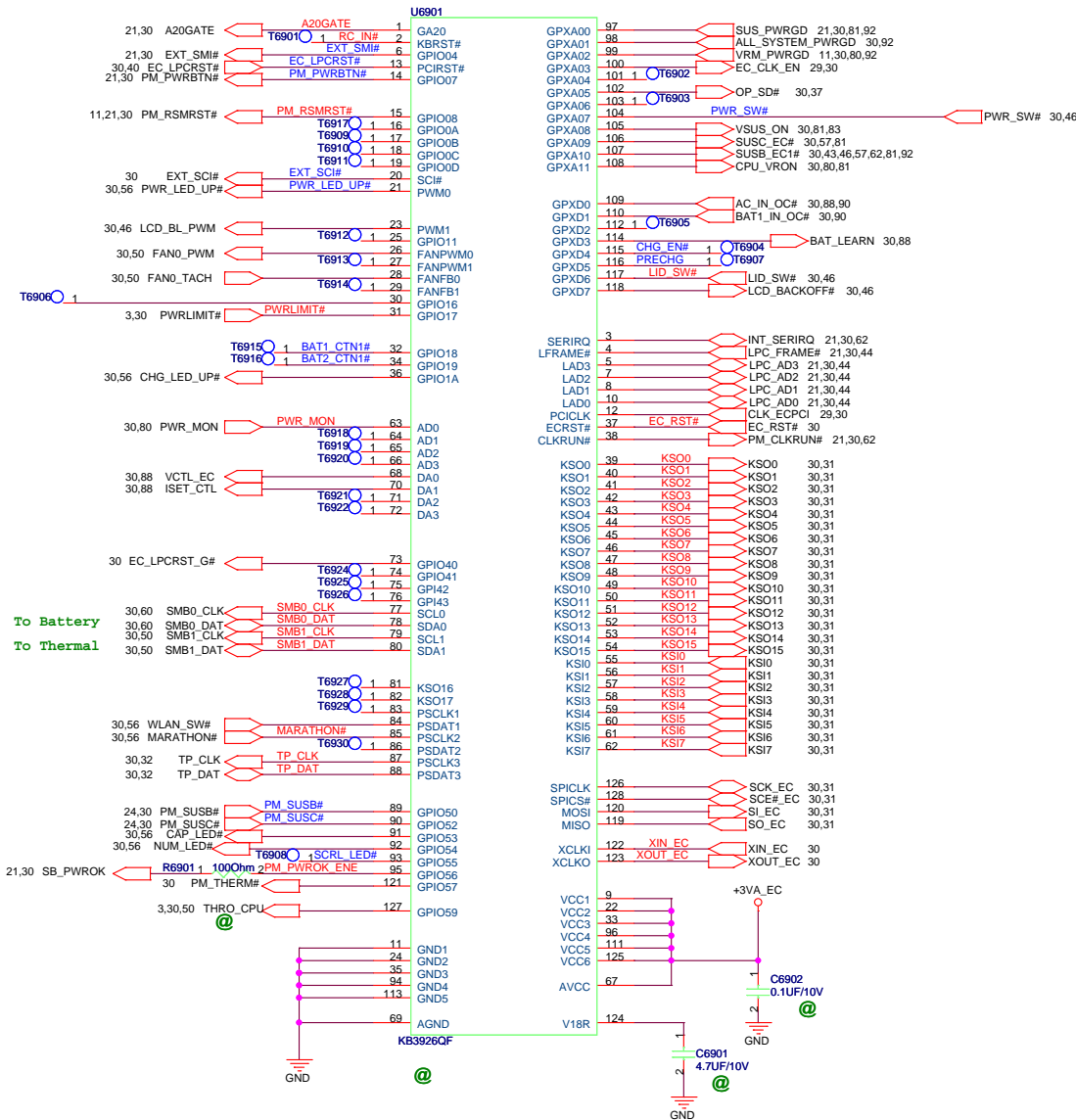
PCI Device	IDSEL#	REQ/GNT#	Interrupts
1394 (R5C833)	AD24	0	B
CARD READER (R5C833)	AD24	0	C

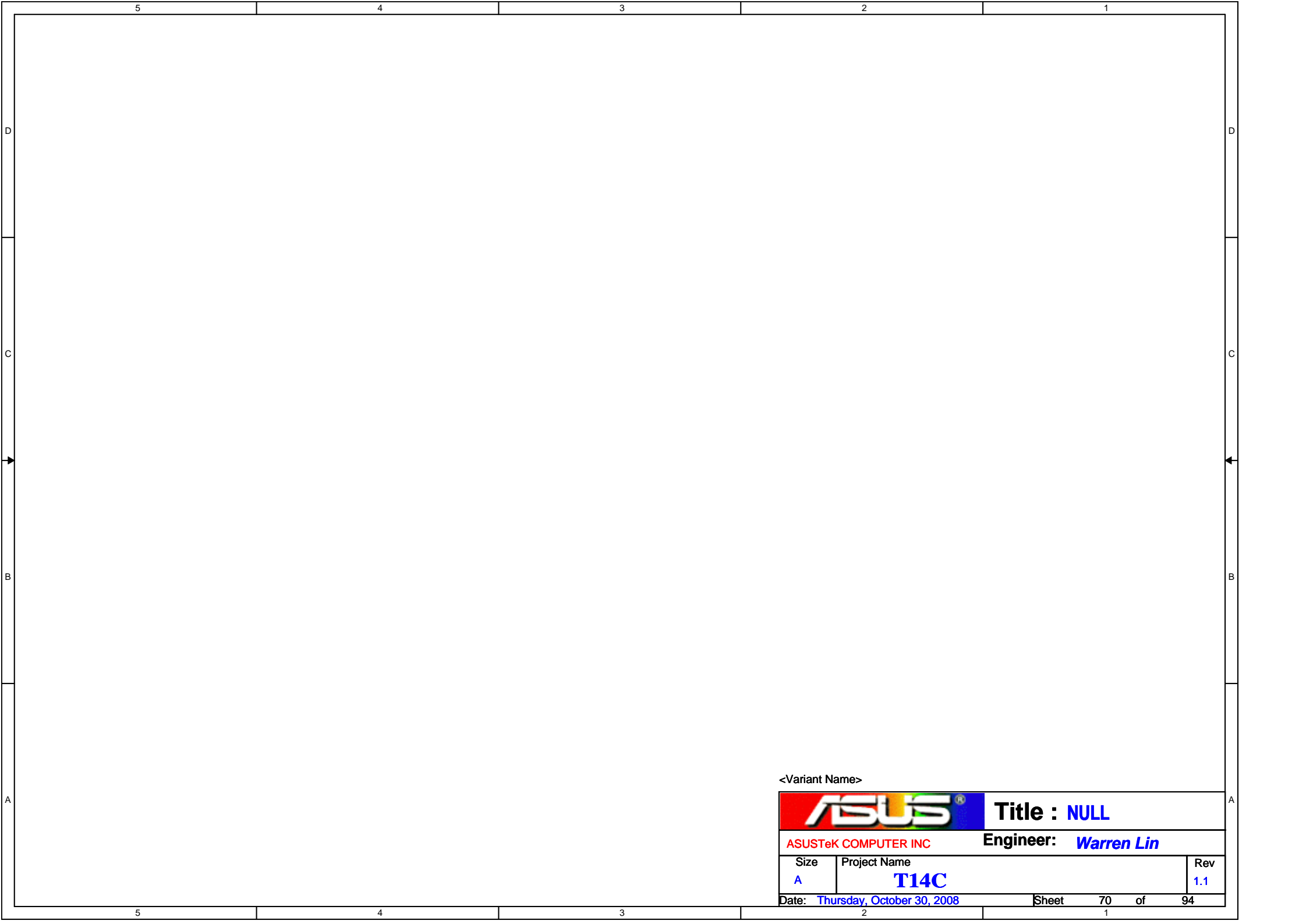
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)




<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size	Project Name	Rev
A	T14C	1.1
Date: Thursday, October 30, 2008		Sheet 68 of 94





<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size	Project Name	Rev
A	T14C	1.1
Date: Thursday, October 30, 2008		Sheet 70 of 94

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<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Warren Lin

Size
A

Project Name
T14C

Rev
1.1

Date: Thursday, October 30, 2008

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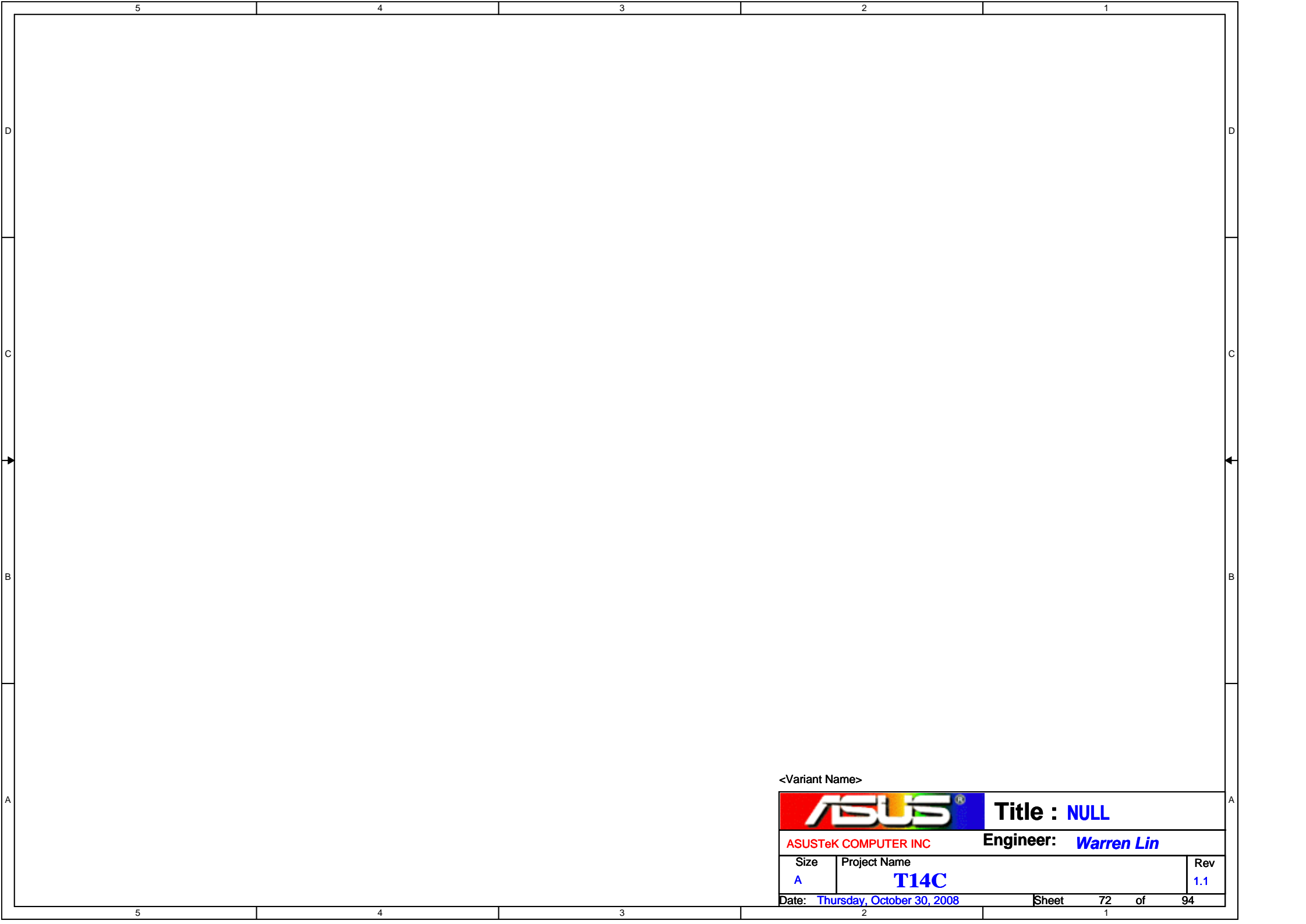
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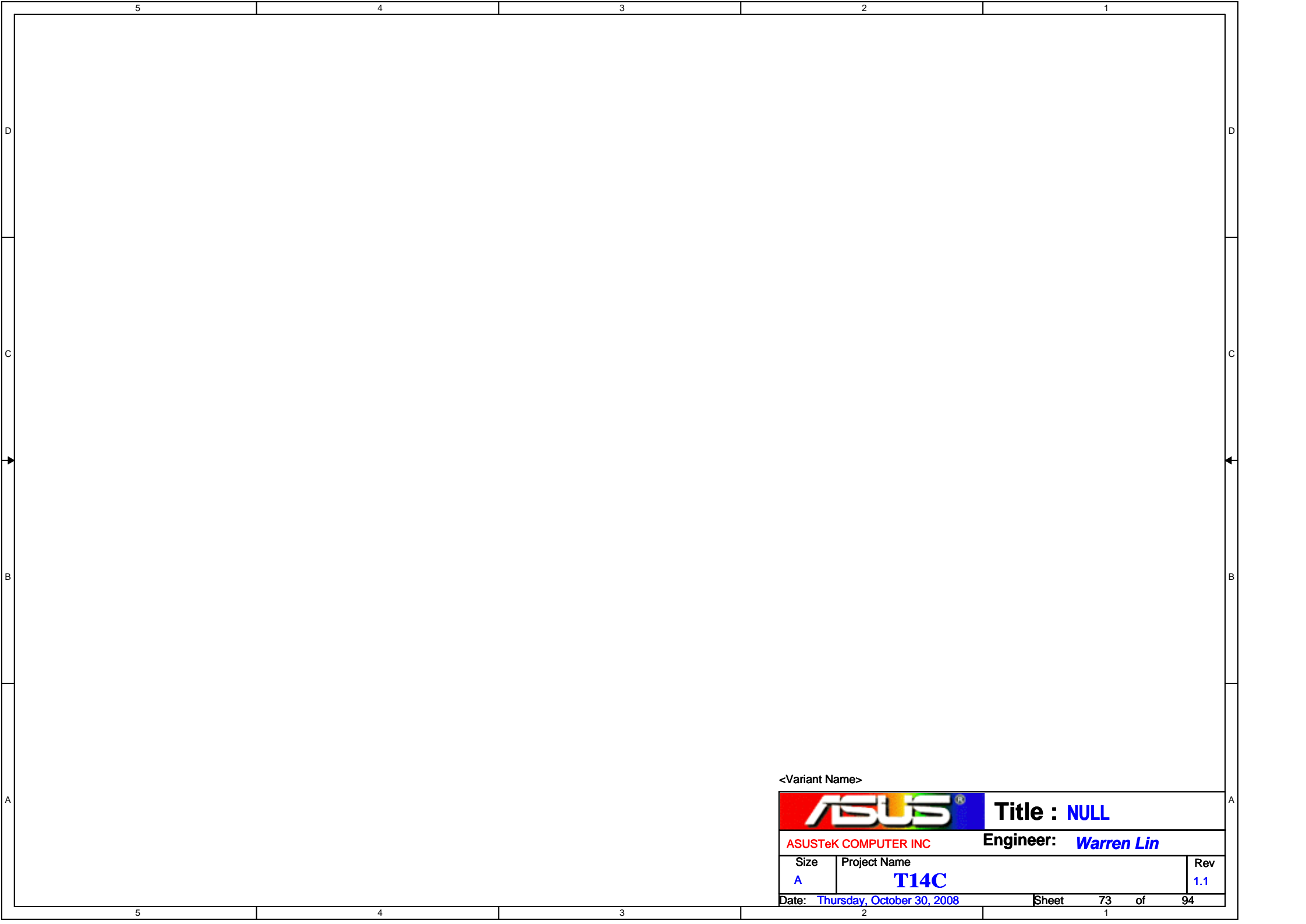
2

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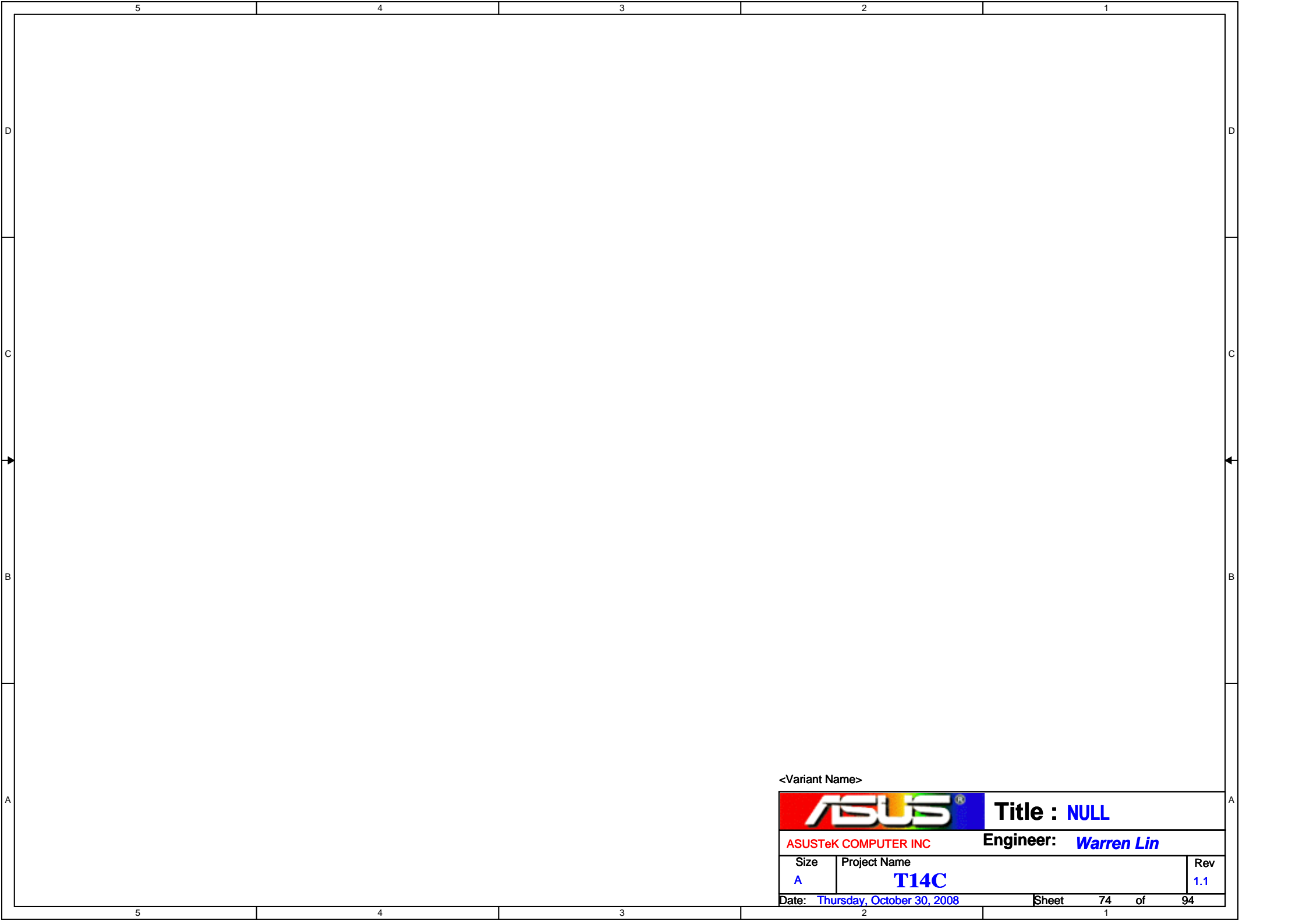
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		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 72 of 94




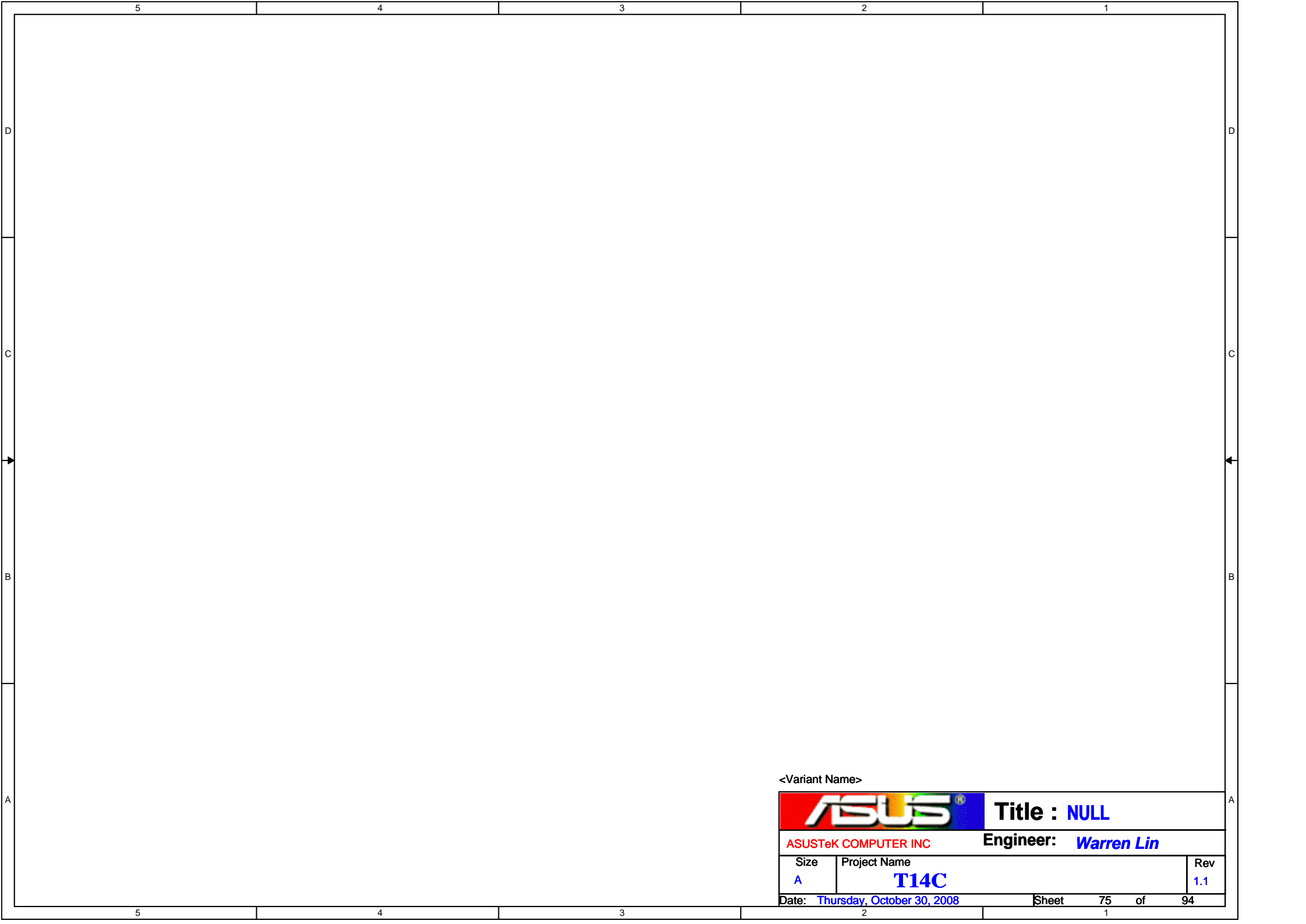
<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 73 of 94



<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size	Project Name	Rev
A	T14C	1.1
Date: Thursday, October 30, 2008		Sheet 74 of 94



<Variant Name>

		Title : NULL
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ASUSTeK COMPUTER INC	Engineer: Warren Lin
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Size	Project Name	Rev
A	T14C	1.1

Date: Thursday, October 30, 2008	Sheet 75 of 94
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		Title : Null	
ASUSTek COMPUTER INC		Engineer: <i>Warren Lin</i>	
Size	Project Name	Rev	
Custom	T14C	1.1	
Date: Thursday, October 30, 2008		Sheet	76 of 94

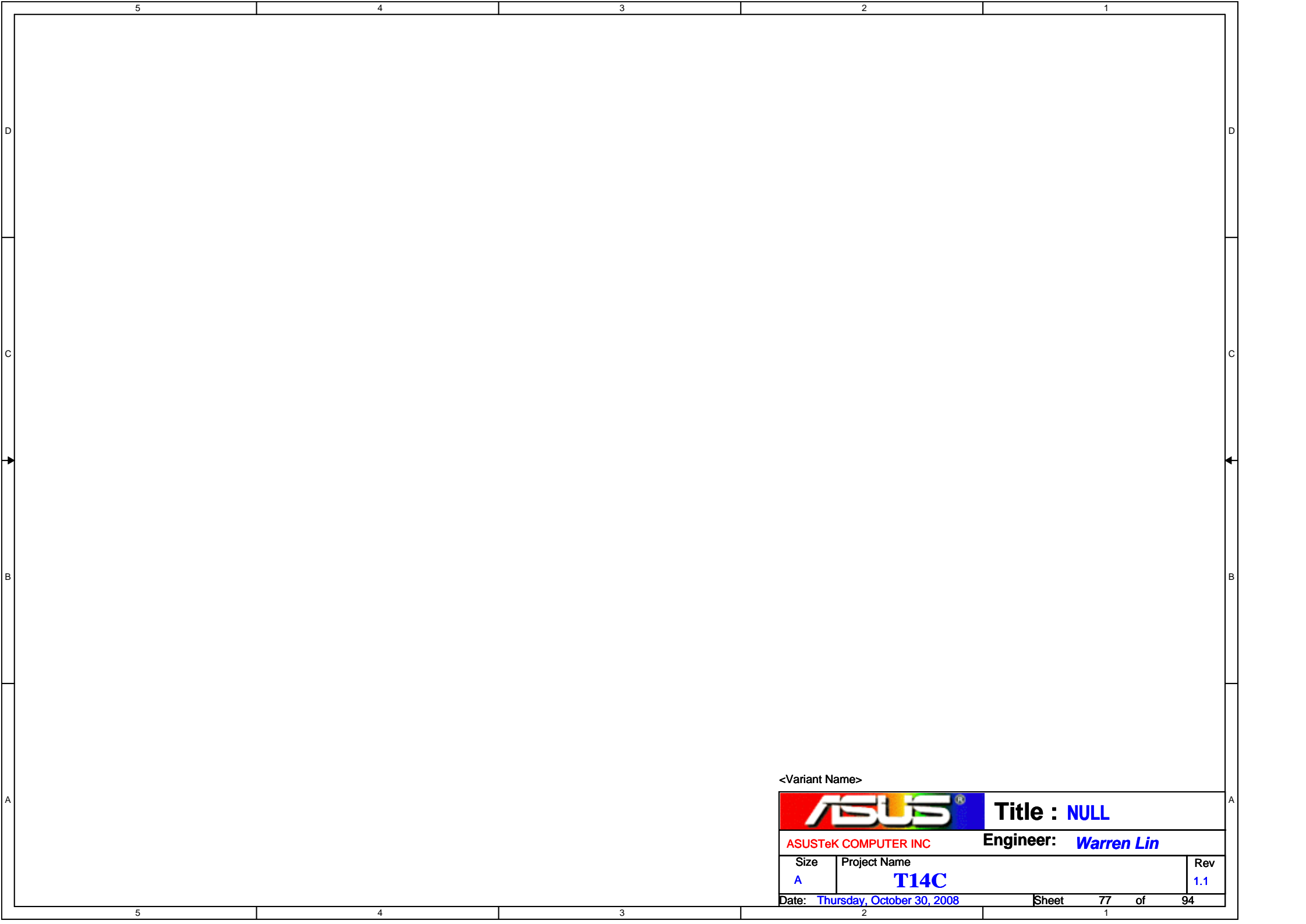
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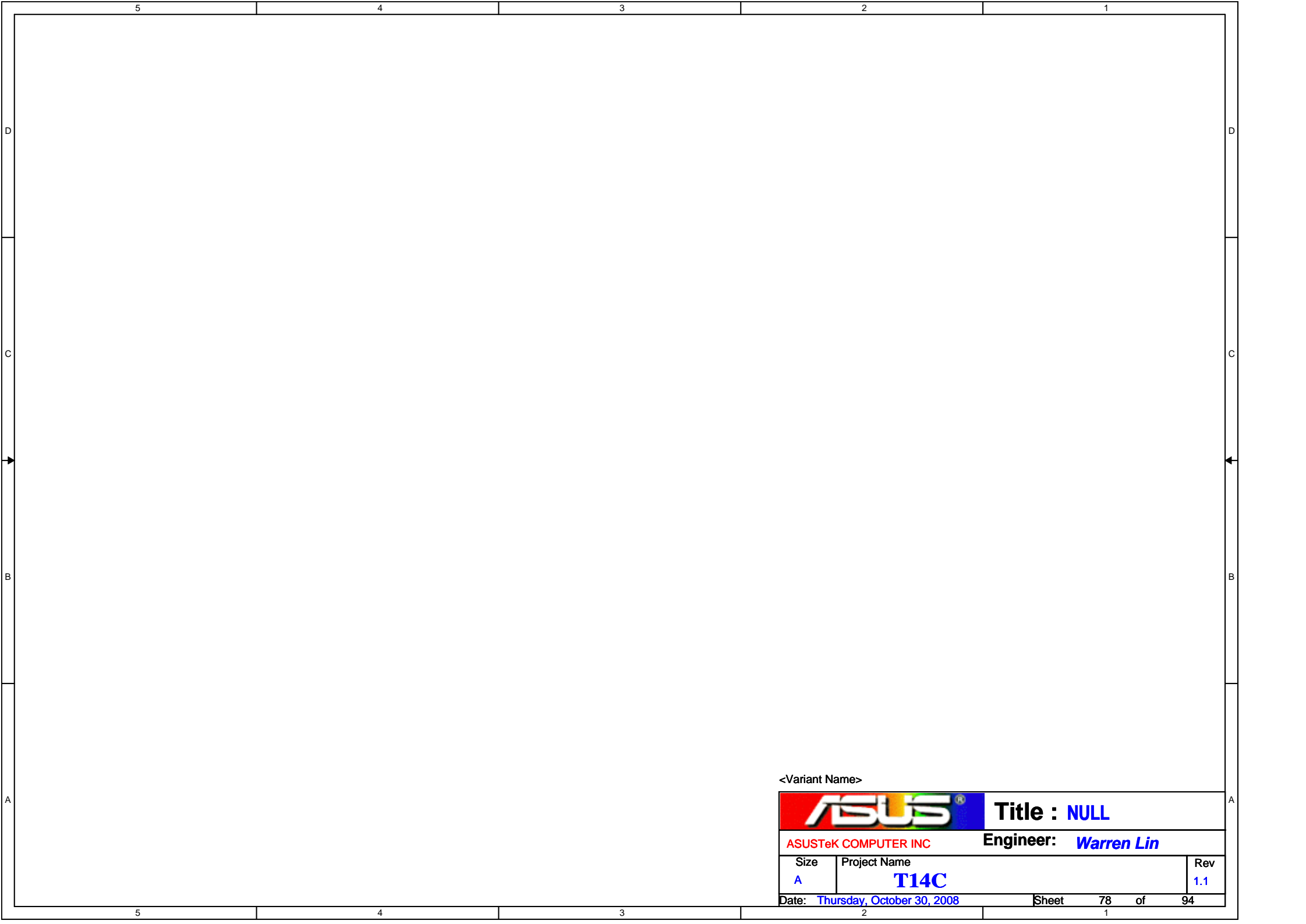
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<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Warren Lin</i>
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 77 of 94



<Variant Name>

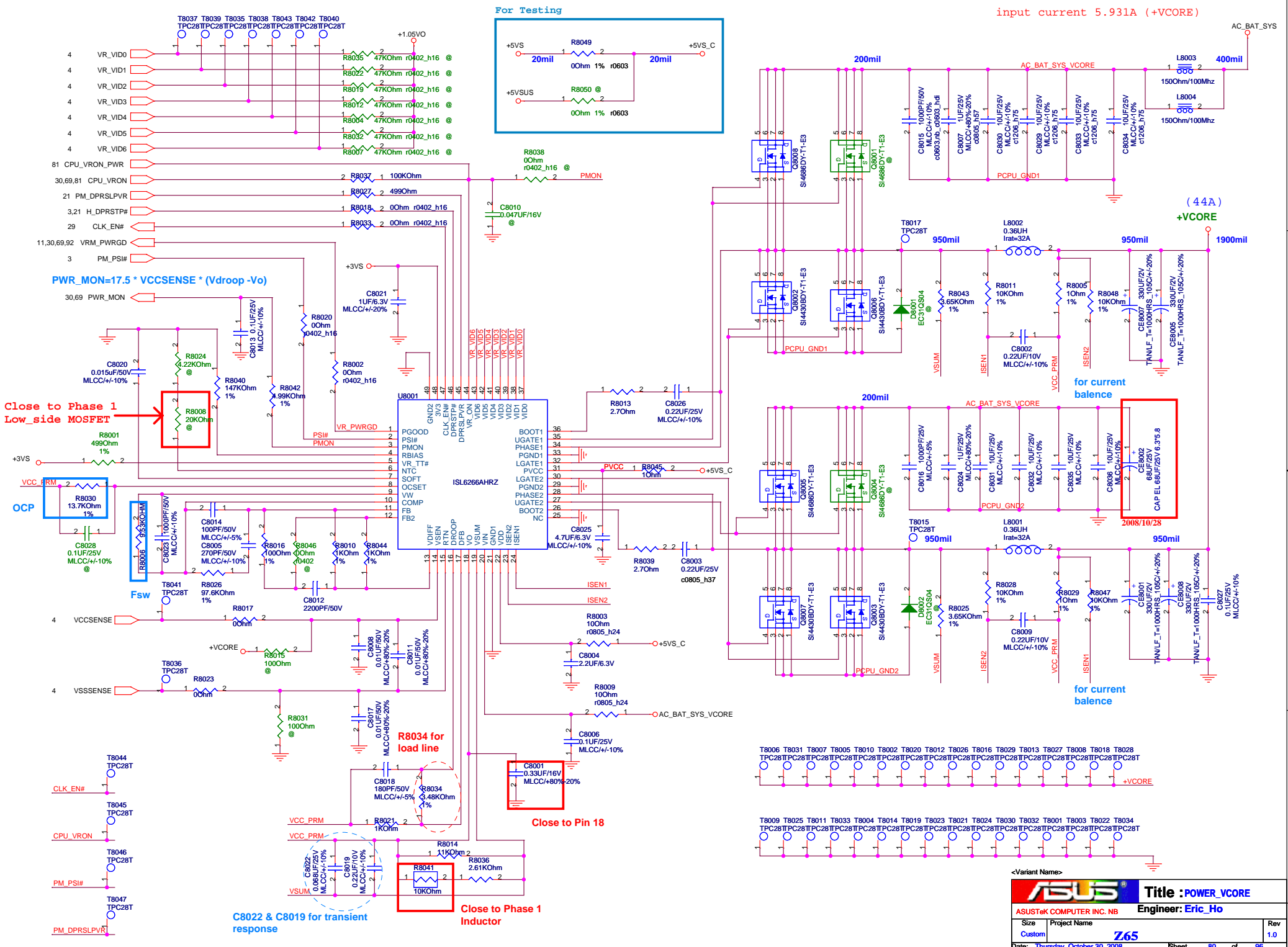
		Title : NULL
ASUSTeK COMPUTER INC		Engineer: Warren Lin
Size A	Project Name T14C	Rev 1.1
Date: Thursday, October 30, 2008		Sheet 78 of 94

Change Note:

R1.1 :

P04_RN0401 change to SL0401~SL0407
P52_For USB Rise/Fall time fast issue add C5204/05/06/07
P46_J4601 change connector, modify ADJ_BL_CON/BL_EN_CON, Change AC_BAT_SYS_INV to AC_BAT_SYS
P46_Remove R4624,R4609,R4614,R4608,R4610,Add SL4601~SL4605
P37_J3703 12 pin change to 8 pin
P32_Add CN3101~CN3105 For EMI
P32_DDR Buffer Del R1601/03/04/05/06/07/08/09 Add SL1601~SL1608
P37_Del Q9209,Q9208,Q9207
P29_RN2902 change short JP2901~JP2903
P16_SL1601~SL1608 change to short JP1601~JP1608
P25_R2518 change to short JP2501
P24_Del R2140

P46_Del J4601 pin5 ground net / U4601/U4602...
P53_DelR5315 and R5314 change to JP5303 and Name change RX5306 ->R5306,RX5307->R5307,RX5308->r5308
P25_R2518 change to short JP SL3101
P20_U2001 Change and R2004 ->JP2001
Package change R4604,R4605,R2914,R2917,R2919,R2932,R0301



input current 5.931A (+VCORE)

(44A)
+VCORE

Close to Phase 1
Low_side MOSFET

OCP
R8030
13.7KOhm
1%

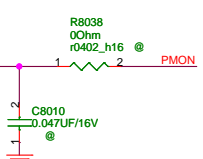
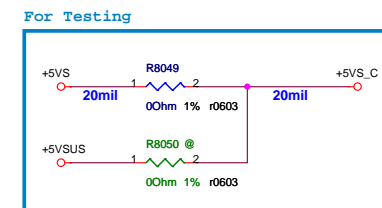
Fsw
T8041
TPC28T
R8026
97.6KOhm
1%

CLK_EN#
T8044
TPC28T

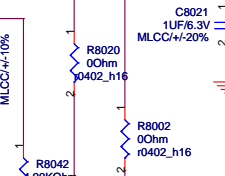
CPU_VRON
T8046
TPC28T

PM_PSI#
T8047
TPC28T

PM DPRSLPVR
T8047
TPC28T



PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)



Close to Phase 1
Low_side MOSFET

R8008
20KOhm

R8001
490Ohm
1%

R8030
13.7KOhm
1%

R8006
3.63KOhm

R8023
100PF/50V
MLCC+/-1.0%

R8016
100Ohm
1%

R8017
0.001UF/50V
MLCC+/-20%

R8015
100Ohm

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

R8017
0.001UF/50V
MLCC+/-20%

Close to Pin 18

C8001
0.33UF/16V
MLCC+/-20%

R8003
100Ohm
r0805_h24

R8009
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

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100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

R8003
100Ohm
r0805_h24

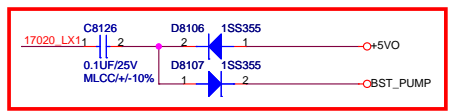
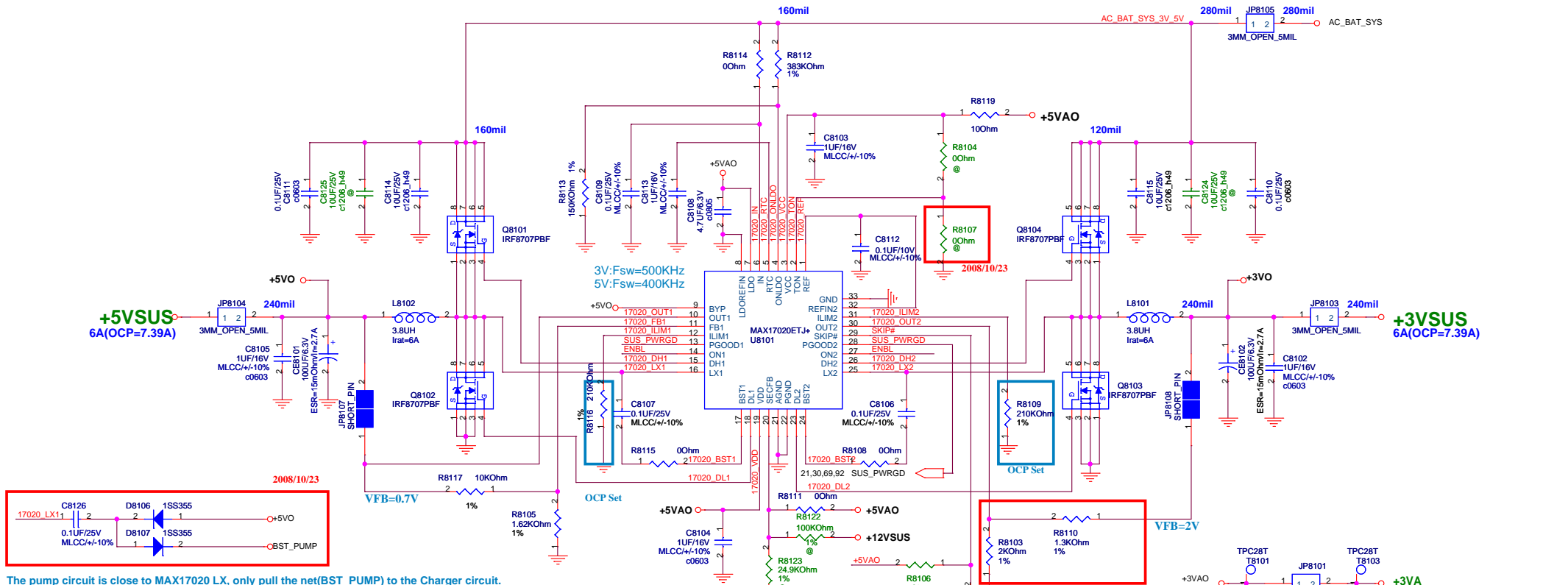
C8022 & C8019 for transient response

R8041
10KOhm

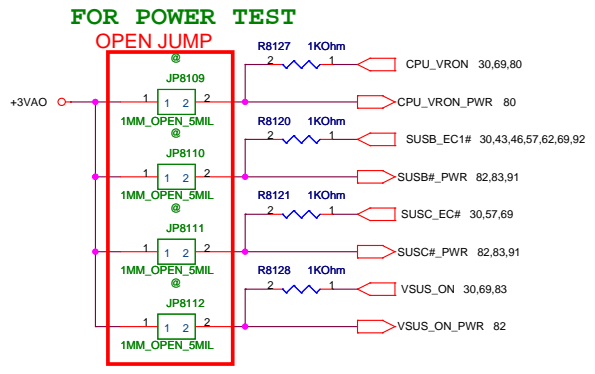
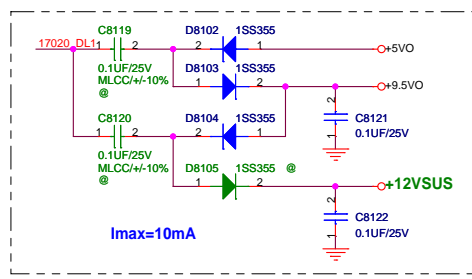
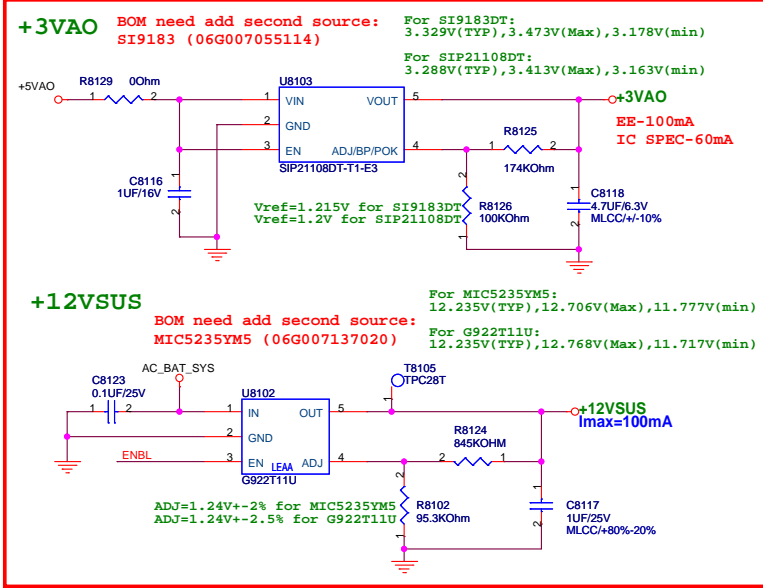
Close to Phase 1 Inductor

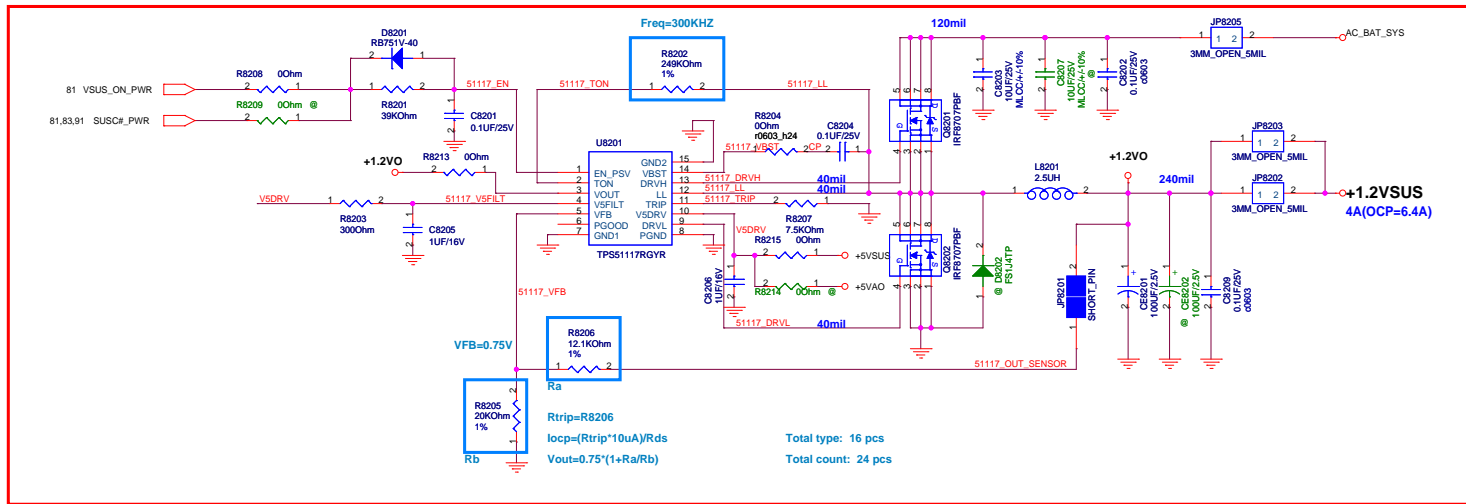
R8036
2.61KOhm

ASUS		Title : POWER_VCORE	
ASUSTek COMPUTER INC. NB		Engineer: Eric_Ho	
Size	Project Name	Rev	
Custom	Z65	1.0	
Date: Thursday, October 30, 2008		Sheet	80 of 96

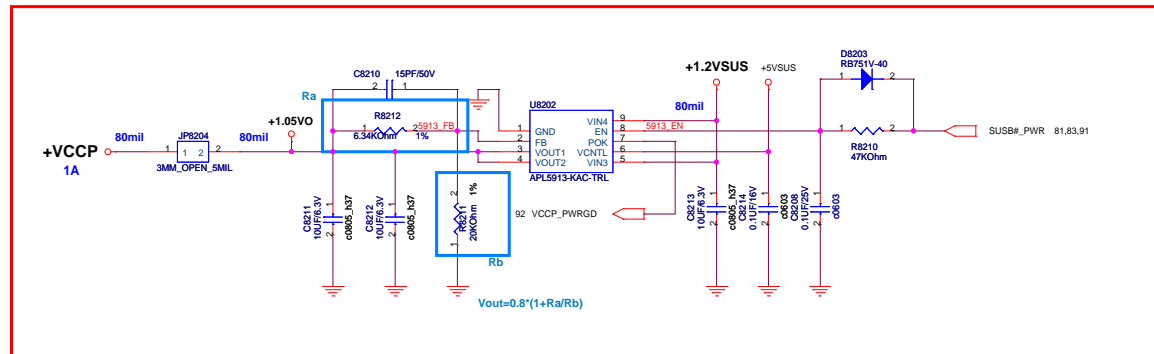


The pump circuit is close to MAX17020 LX, only pull the net(BST_PUMP) to the Charger circuit.

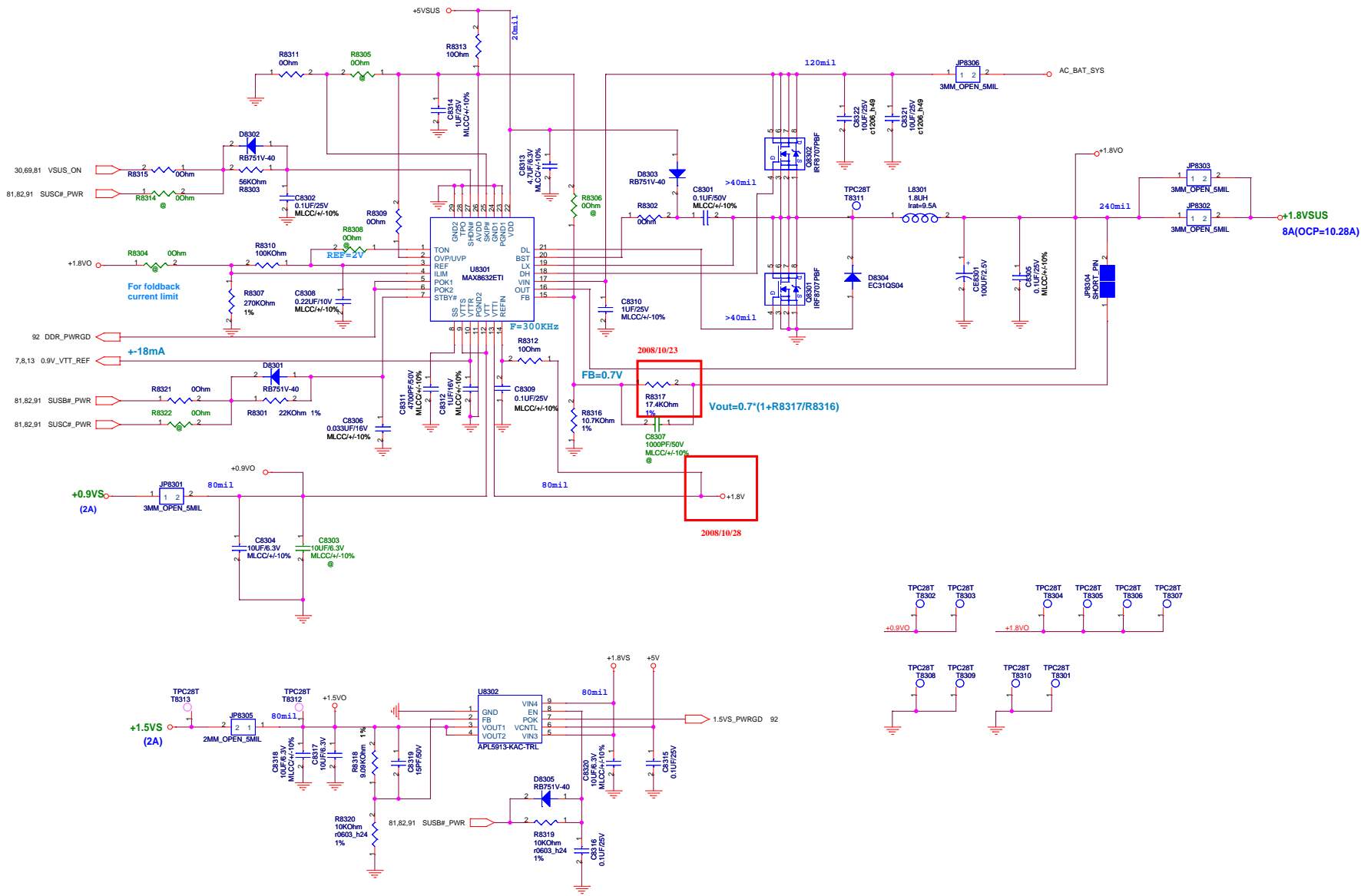




2008/10/28



2008/10/28



5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NA	
<OrgName>		Engineer: Eric_Ho	
Size	Project Name	Rev	
Custom	Z65	1.0	
Date: Thursday, October 30, 2008		Sheet	84 of 96

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

		Title : NA	
ASUSTeK COMPUTER INC. NB		Engineer: Eric_Ho	
Size	Project Name		Rev
C	Z65		1.0
Date: Thursday, October 30, 2008		Sheet	65 of 95

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

		Title :NA
<OrgName>		Engineer: Eric_Ho
Size	Project Name	Rev
B	Z65	1.0
Date: Thursday, October 30, 2008		Sheet 86 of 96

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



<OrgName> **Engineer: Eric_Ho**

Size	Project Name	Rev
Custom	Z65	1.0

5

4

3

2

1

POWER PATH & BAT_LEARN

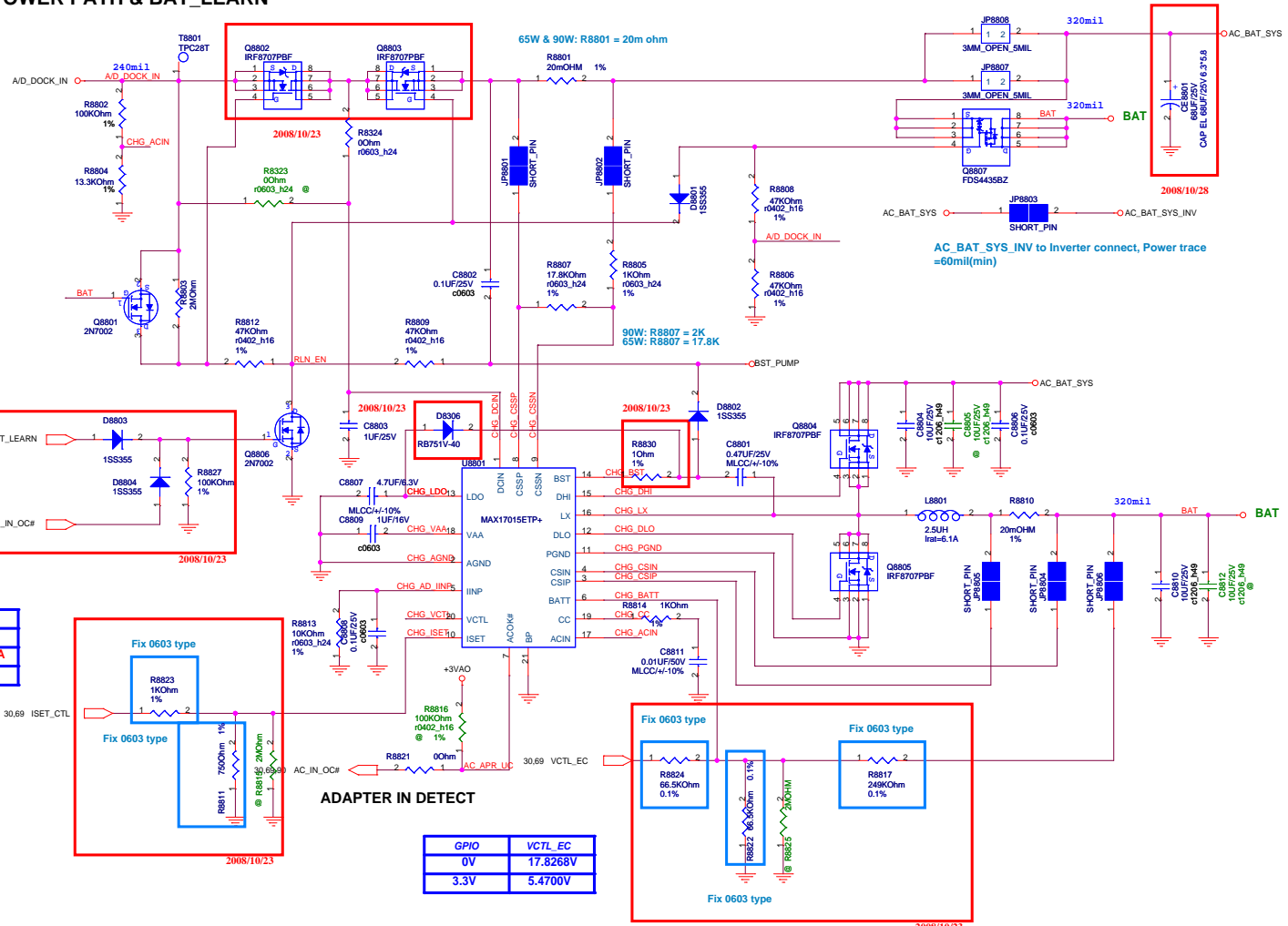
AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

AD_INP:
 $Input = Viinp / (RS1 * Giinp * Riinp)$
 $= Viinp / (15m\ \Omega * 2.8mA/V * 10K\ \Omega)$
 $= 2.38\ Viinp$

$VCTL = 0.3V$; CHG VOLTAGE = 4.25/CELL(4 CELL)
 $VCTL = 3.9V$; CHG VOLTAGE = 4.25/CELL(3 CELL)

VEC	ISET_CTL
0V	0A
0.1164V	0.1426A
3.3V	4.04A

GPIO	VCTL_EC
0V	17.8268V
3.3V	5.4700V



ADAPTER IN DETECT

5

4

3

2

1

D

D

C

C

B

B

A

A

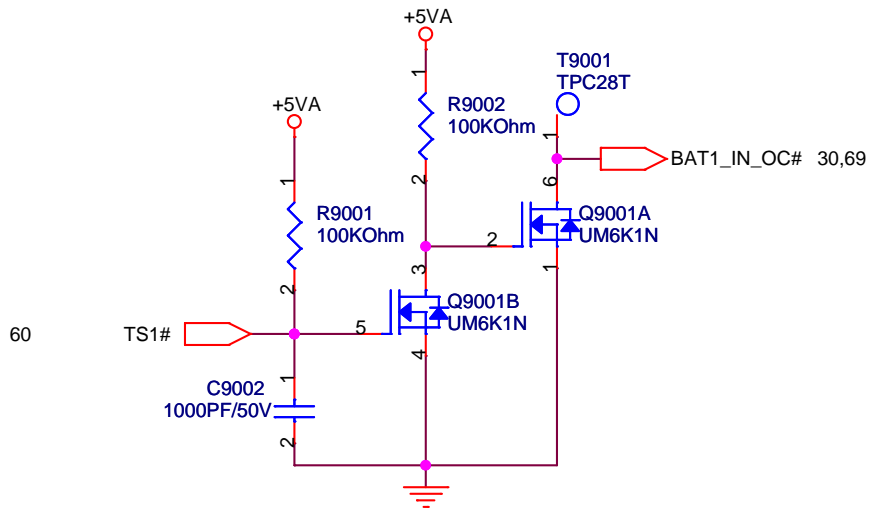
<Variant Name>



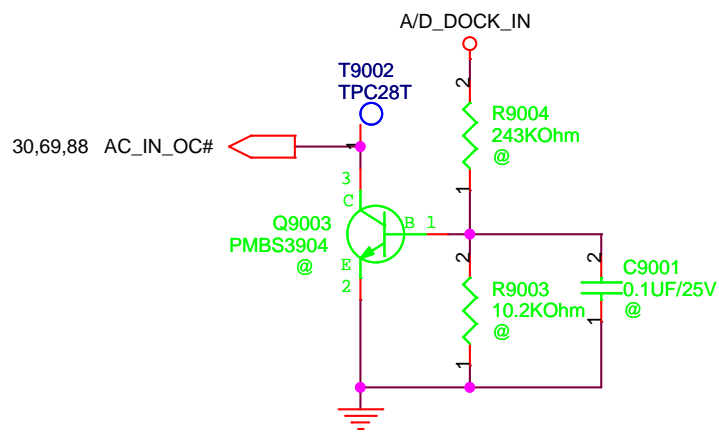
<OrgName> **Engineer: Eric_Ho**

Size	Project Name	Rev
Custom	Z65	1.0

BATTERY IN DETECT



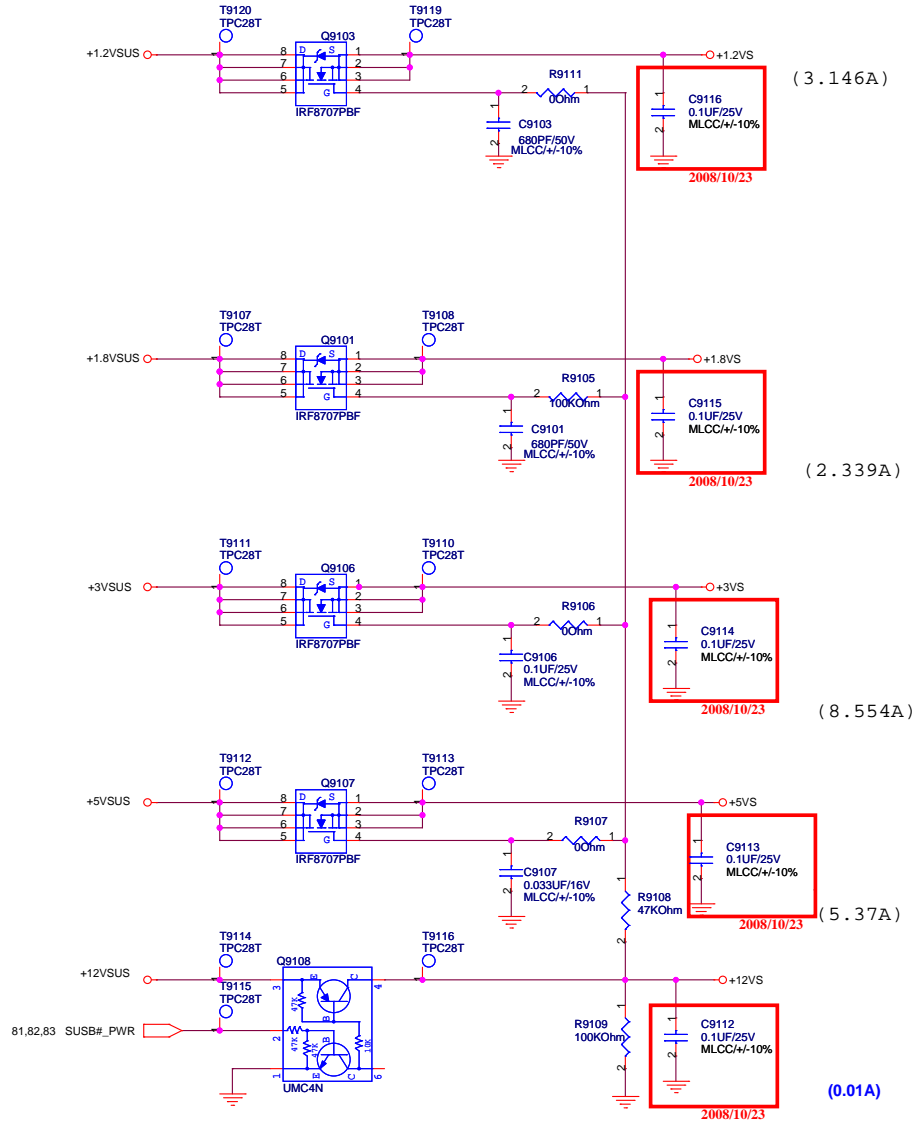
ADAPTER IN DETECT



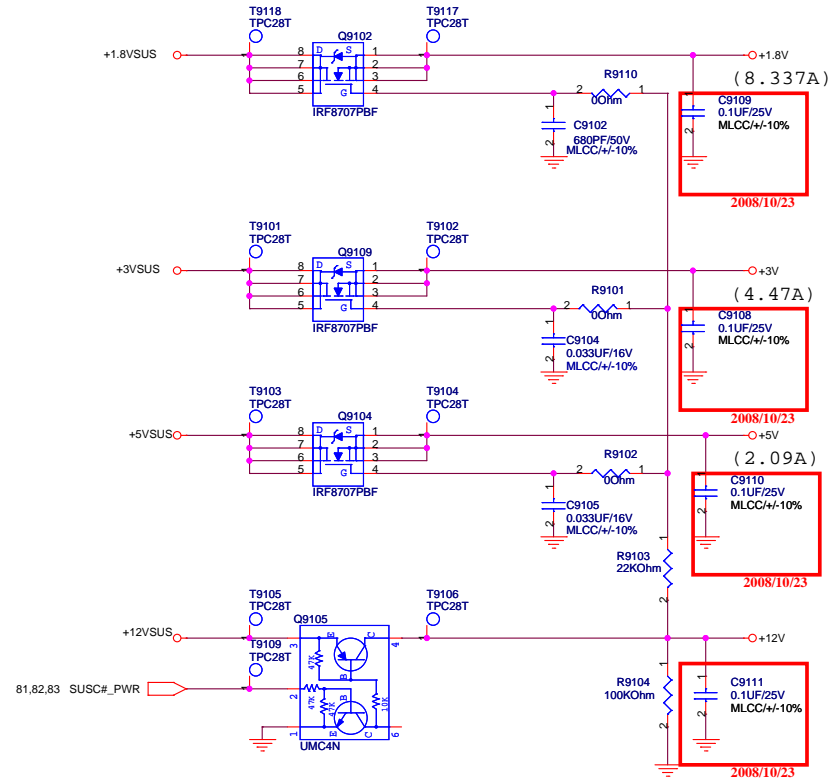
<Variant Name>

ASUS		Title : POWER_DETECT	
<OrgName>		Engineer: Eric_Ho	
Size A	Project Name Z65		Rev 1.0
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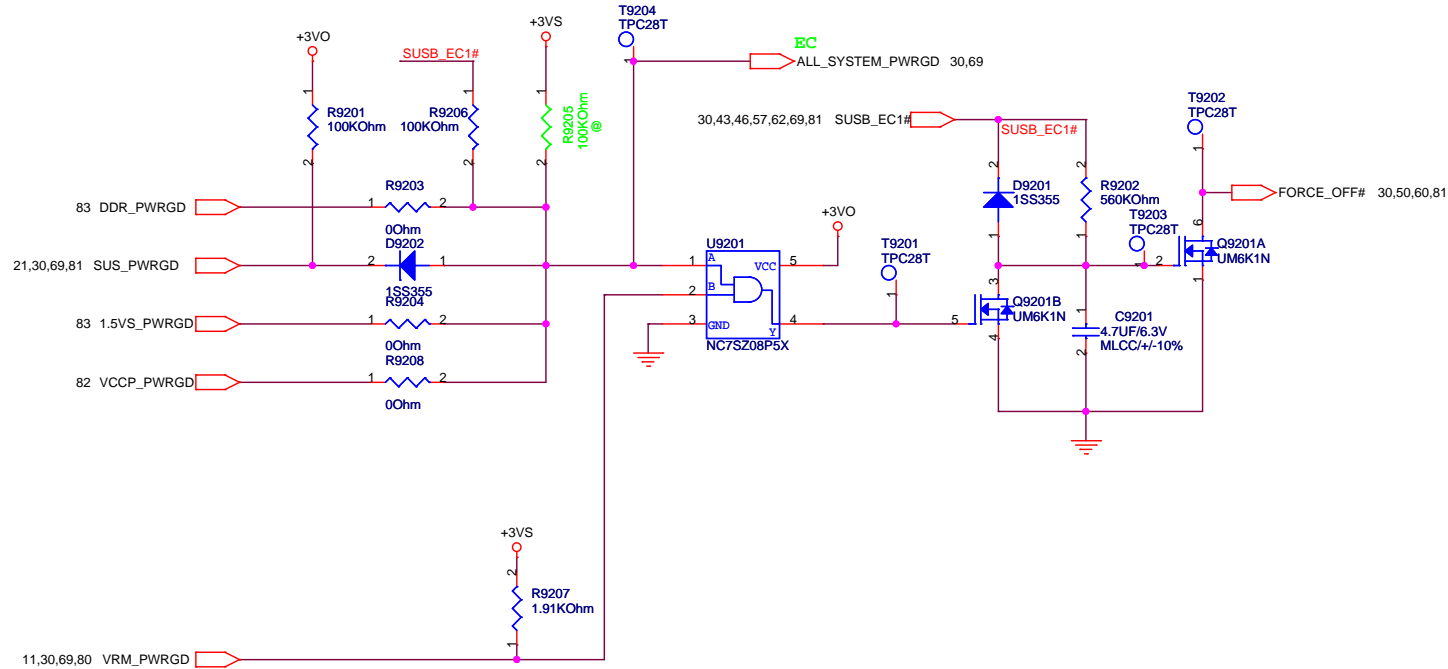
SUSB#_STAGE POWER



SUSC#_STAGE POWER



POWER GOOD DETECTOR



<Variant Name>


ASUS		Title : POWER_PROTECT	
<OrgName>		Engineer: Eric_Ho	
Size	Project Name		Rev
B	Z65		1.0
Date:	Thursday, October 30, 2008	Sheet	92 of 96

AC_BAT_SYS	AC_BAT_SYS	46,60,80,81,82,83,88
+3VA	+3VA	21,30,46,50,57,60,81
+5VA	+5VA	81,90
+5VO	+5VO	81
+3VO	+3VO	81,92
+3VSUS	+3VSUS	13,21,22,23,24,30,33,35,37,46,53,81,91
+5VSUS	+5VSUS	56,80,81,82,83,91
+3V	+3V	32,35,40,43,44,53,57,61,62,91
+3VS	+3VS	3,7,8,11,20,21,22,23,25,29,30,32,36,43,46,50,51,53,56,57,62,80,91,92
+12VSUS	+12VSUS	81,91
+12V	+12V	37,46,52,61,91
+12VS	+12VS	46,91
+5V	+5V	46,52,56,57,83,91
+5VS	+5VS	30,32,36,37,38,46,50,51,56,57,80,91
+1.8VO	+1.8VO	83
+1.8VSUS	+1.8VSUS	14,21,22,23,83,91
+1.8V	+1.8V	7,13,14,83,91
+1.8VS	+1.8VS	10,11,13,14,16,20,21,22,23,25,57,83,91
+1.5VS	+1.5VS	4,11,43,53,57,83
+VCCP	+VCCP	4,10,14,21,23,29,57,82
+0.9VS	+0.9VS	9,83
BAT	BAT	60,88
+VCORE	+VCORE	4,80
+1.2VO	+1.2VO	82
+1.2VS	+1.2VS	12,14,57,91
BAT_CON	BAT_CON	60

CHANGE LIST

07/21	SR	N/A

<Variant Name>



Title : POWER_SIGNAL

<OrgName> **Engineer:** Eric_Ho

Size	Project Name	Rev
Custom	Z65	1.0

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