

Z62H

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSV#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	R11#WUI0/GPD0	SUSB#	I
29	R12#WUI1/GPD1	SUSC#	I
30	LPCRST#WUI4/GPD2	PLT_RST#	I
31	ECSC#GPD3	EXT_SC#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#WUI6/GPE6	LID_EC#	I
25	CLKRUN#WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

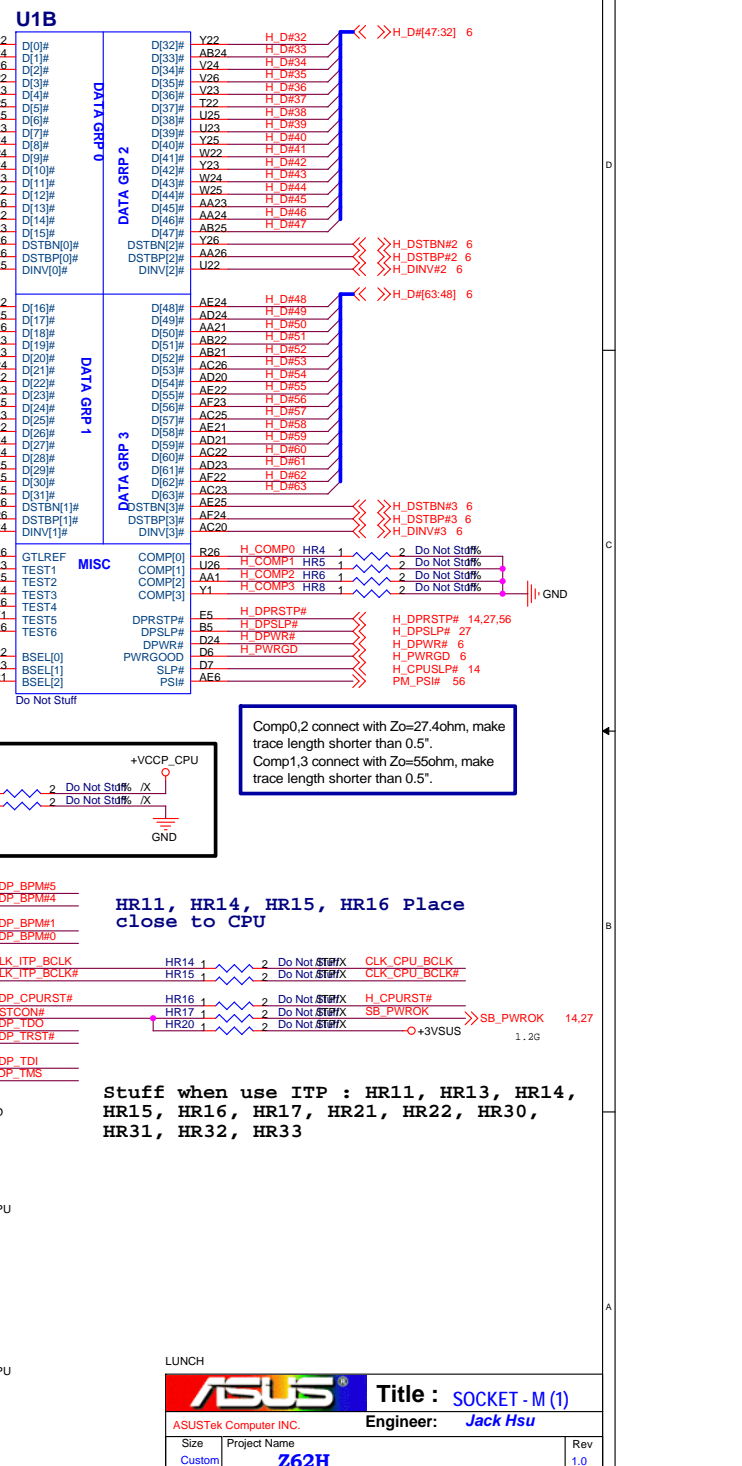
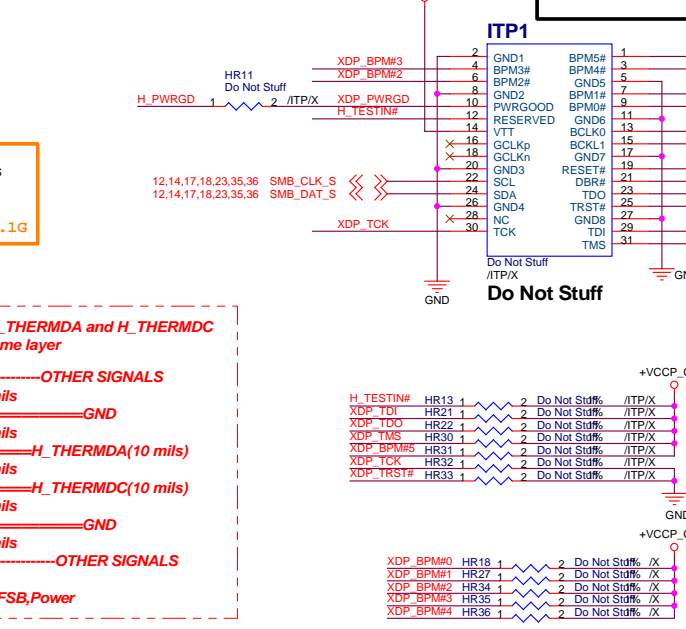
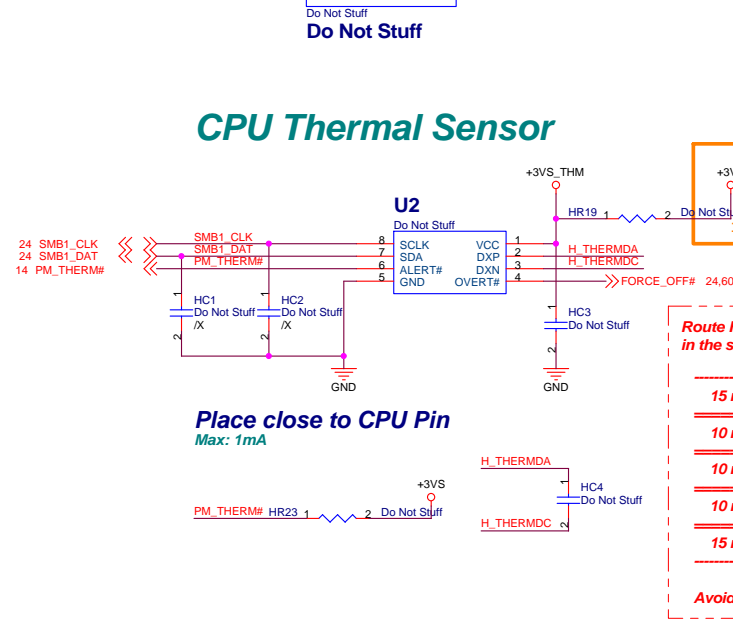
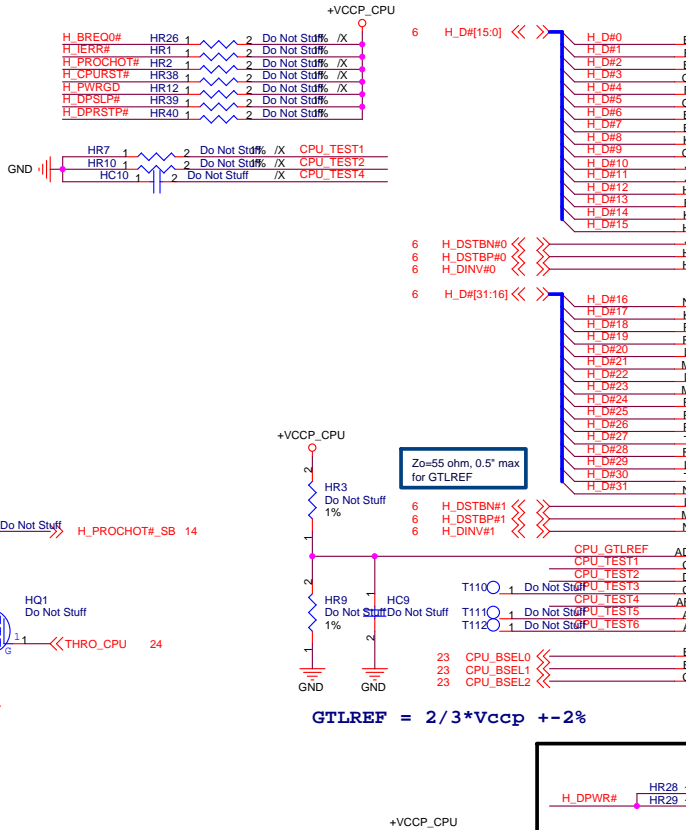
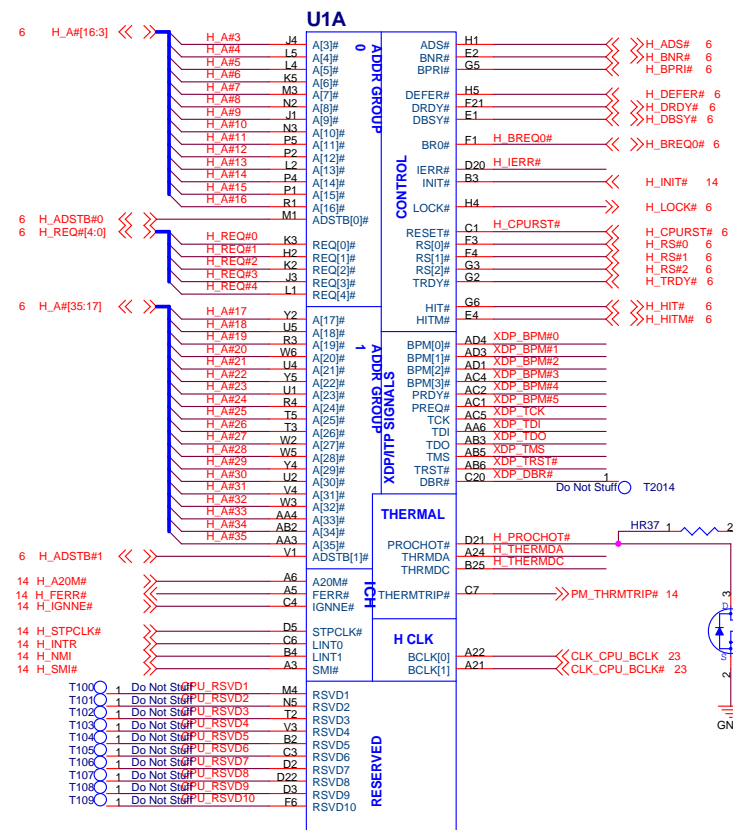
Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCL_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCL_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCL_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCL_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCL_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCL_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCL_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

LUNCH

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	2	of 63



Route H_THERMDA and H_THERMDC in the same layer

-----OTHER SIGNALS

15 mils -----GND

10 mils -----H_THERMDA(10 mils)

10 mils -----H_THERMDC(10 mils)

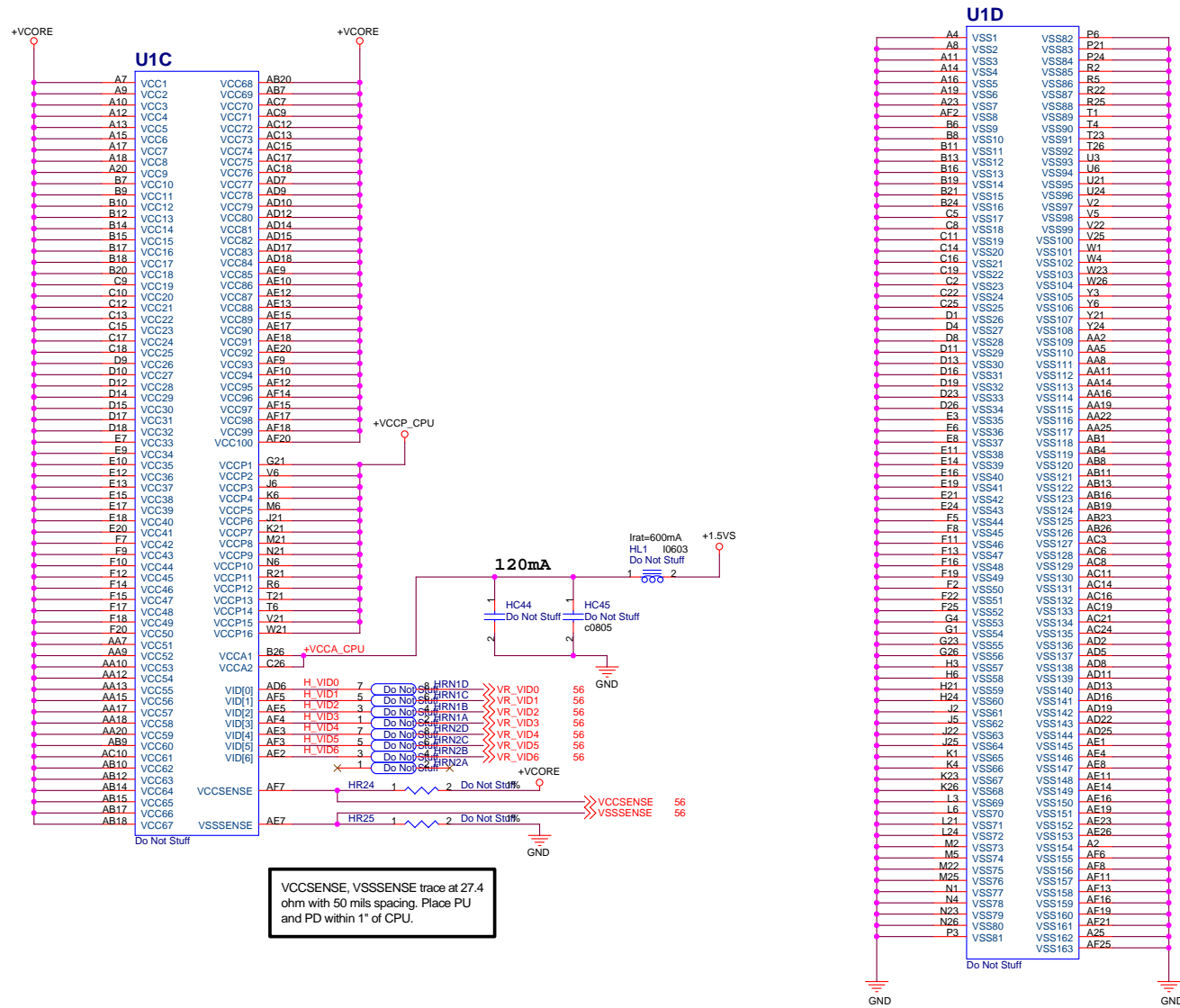
10 mils -----GND

15 mils -----OTHER SIGNALS

Avoid FSB,Power

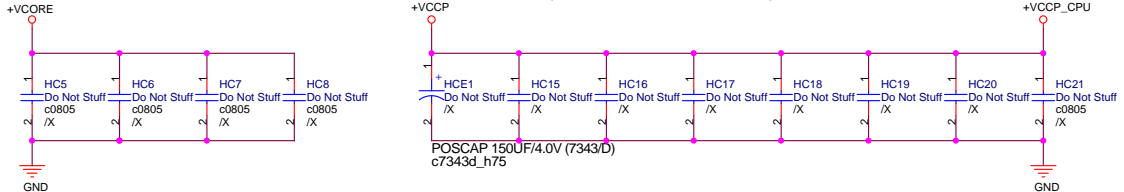
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".

Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

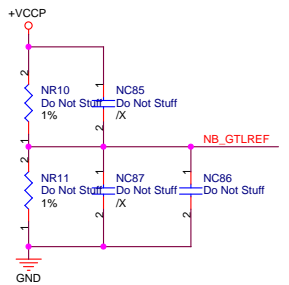
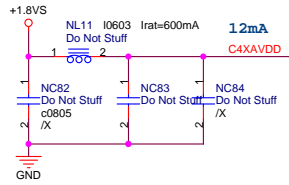
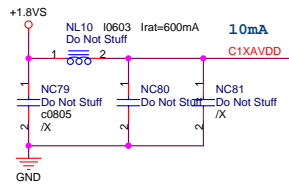
**+VCCP Decoupling Capacitor
(Place near CPU)**



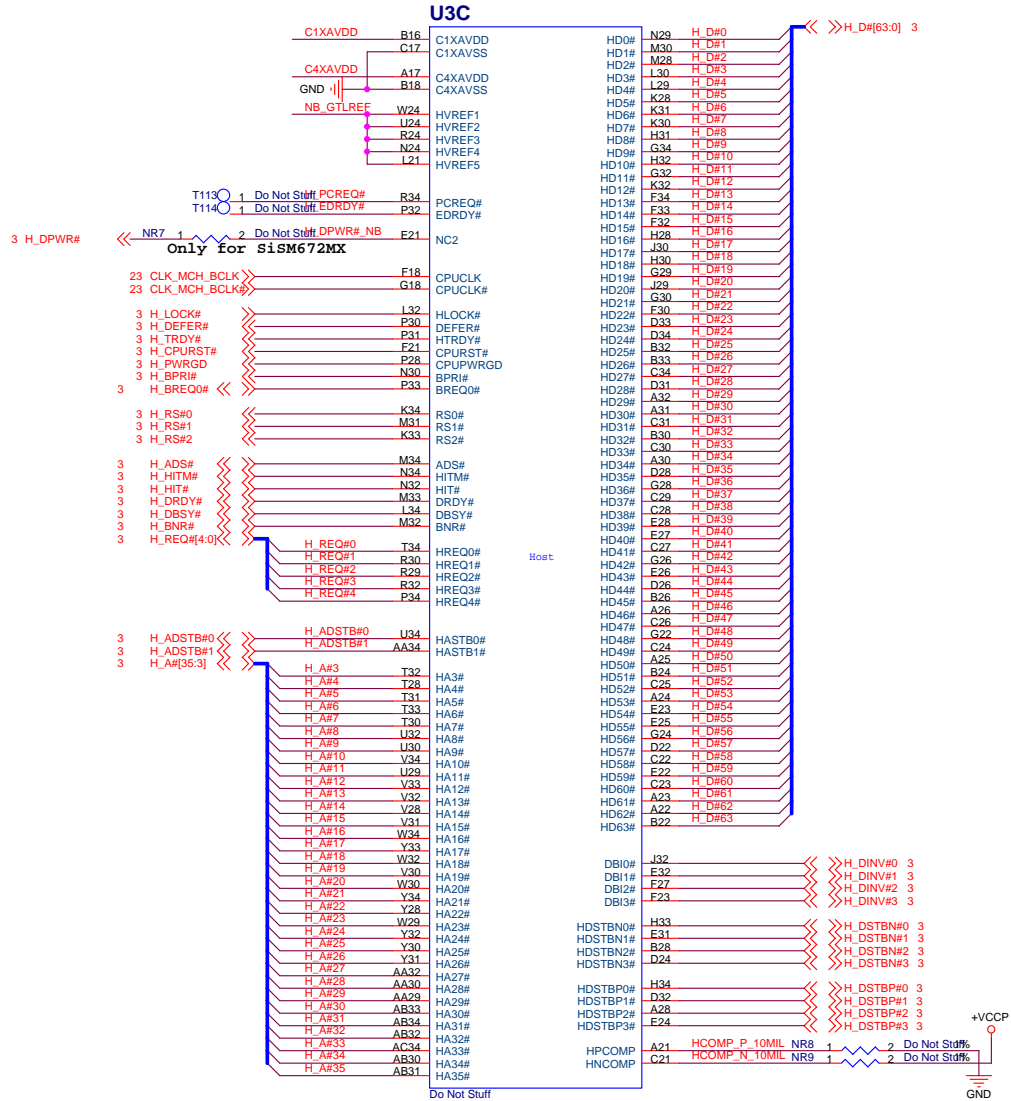
Non-Stuff

**Decoupling guide from INTEL
44A for Merom**

VCORE 22uF/10V * 32pcs, 330uF/2V * 6pcs
VCCP 0.1uF * 6pcs, 150uF * 1pcs



Place 0.1uF under M672 solder side, less 100mils from M672 Pin



LUNCH

ASUS Title : SiSM672 - HOST(1)

ASUSTek Computer INC. Engineer: Jack Hsu

Size Project Name

Custom Z62H Rev 1.0

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U3B

M A DQ0	AD31	MD0A
M A DQ1	AD30	MD1A
M A DQ2	AG34	MD2A
M A DQ3	AE29	MD3A
M A DQ4	AE32	MD4A
M A DQ5	AF34	MD5A
M A DQ6	AF31	MD6A
M A DQ7	AE30	MD7A
M A DM0	AD28	DQM0A
M A DQS0	AF32	DQS0A
M A DQS#0	AF33	DQS0A#
M A DQ8	AF28	MD8A
M A DQ9	AJ34	MD9A
M A DQ10	AH31	MD10A
M A DQ11	AG30	MD11A
M A DQ12	AF30	MD12A
M A DQ13	AG32	MD13A
M A DQ14	AJ32	MD14A
M A DQ15	AJ31	MD15A
M A DM1	AH34	DQM1A
M A DQS1	AH32	DQS1A
M A DQS#1	AH33	DQS1A#
M A DQ16	AK34	MD16A
M A DQ17	AH30	MD17A
M A DQ18	AL32	MD18A
M A DQ19	AK33	MD19A
M A DQ20	AK32	MD20A
M A DQ21	AG29	MD21A
M A DQ22	AM34	MD22A
M A DQ23	AL31	MD23A
M A DM2	AH30	DQM2A
M A DQS2	AK33	DQS2A
M A DQS#2	AL34	DQS2A#
M A DQ24	AK32	MD24A
M A DQ25	AP32	MD25A
M A DQ26	AP31	MD26A
M A DQ27	AM29	MD27A
M A DQ28	AK30	MD28A
M A DQ29	AK29	MD29A
M A DQ30	AJ27	MD30A
M A DQ31	AK28	MD31A
M A DM3	AN32	DQM3A
M A DQS3	AK30	DQS3A
M A DQS#3	AM31	DQS3A#
M A DQ32	AK20	MD32A
M A DQ33	AM20	MD33A
M A DQ34	AH19	MD34A
M A DQ35	AL19	MD35A
M A DQ36	AN20	MD36A
M A DQ37	AJ21	MD37A
M A DQ38	AP19	MD38A
M A DQ39	AH20	MD39A
M A DM4	AK21	DQM4A
M A DQS4	AK19	DQS4A
M A DQS#4	AL19	DQS4A#
M A DQ40	AK18	MD40A
M A DQ41	AJ17	MD41A
M A DQ42	AK17	MD42A
M A DQ43	AP16	MD43A
M A DQ44	AH18	MD44A
M A DQ45	AP18	MD45A
M A DQ46	AN18	MD46A
M A DQ47	AP17	MD47A
M A DM5	AM18	DQM5A
M A DQS5	AL17	DQS5A
M A DQS#5	AM17	DQS5A#
M A DQ48	AN16	MD48A
M A DQ49	AK16	MD49A
M A DQ50	AN14	MD50A
M A DQ51	AH15	MD51A
M A DQ52	AP15	MD52A
M A DQ53	AM16	MD53A
M A DQ54	AK15	MD54A
M A DQ55	AP14	MD55A
M A DM6	AH16	DQM6A
M A DQS6	AL15	DQS6A
M A DQS#6	AM15	DQS6A#
M A DQ56	AL13	MD56A
M A DQ57	AM13	MD57A
M A DQ58	AM12	MD58A
M A DQ59	AJ13	MD59A
M A DQ60	AM14	MD60A
M A DQ61	AK14	MD61A
M A DQ62	AN12	MD62A
M A DQ63	AH14	MD63A
M A DM7	AK13	DQM7A
M A DQS7	AP12	DQS7A
M A DQS#7	AP13	DQS7A#

Do Not Stuff

DRAM

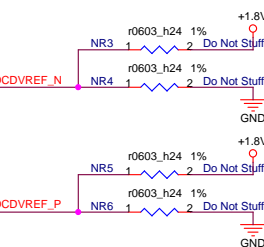
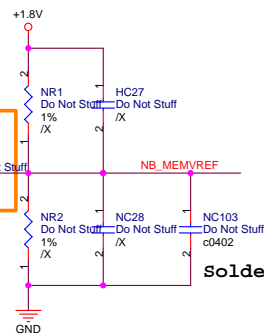
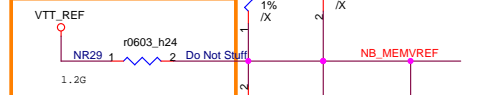
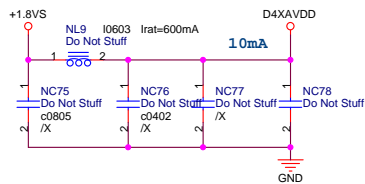
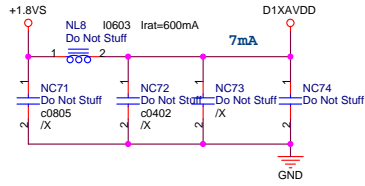
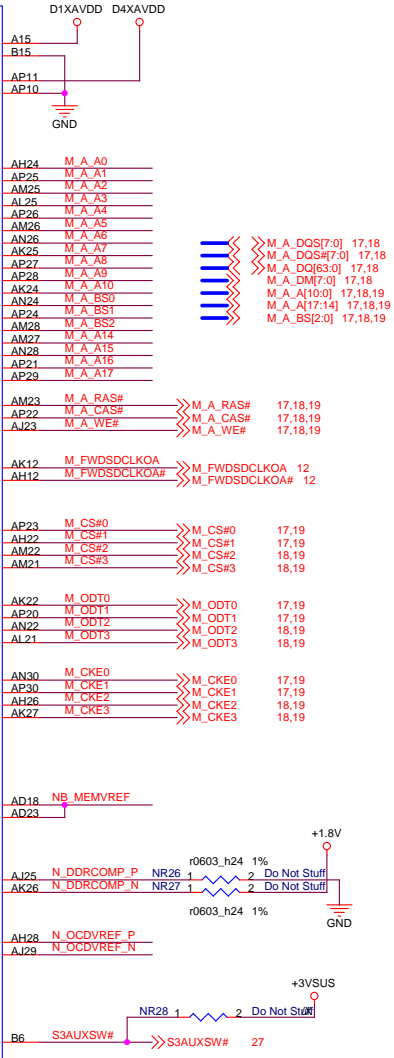
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DDRREF1

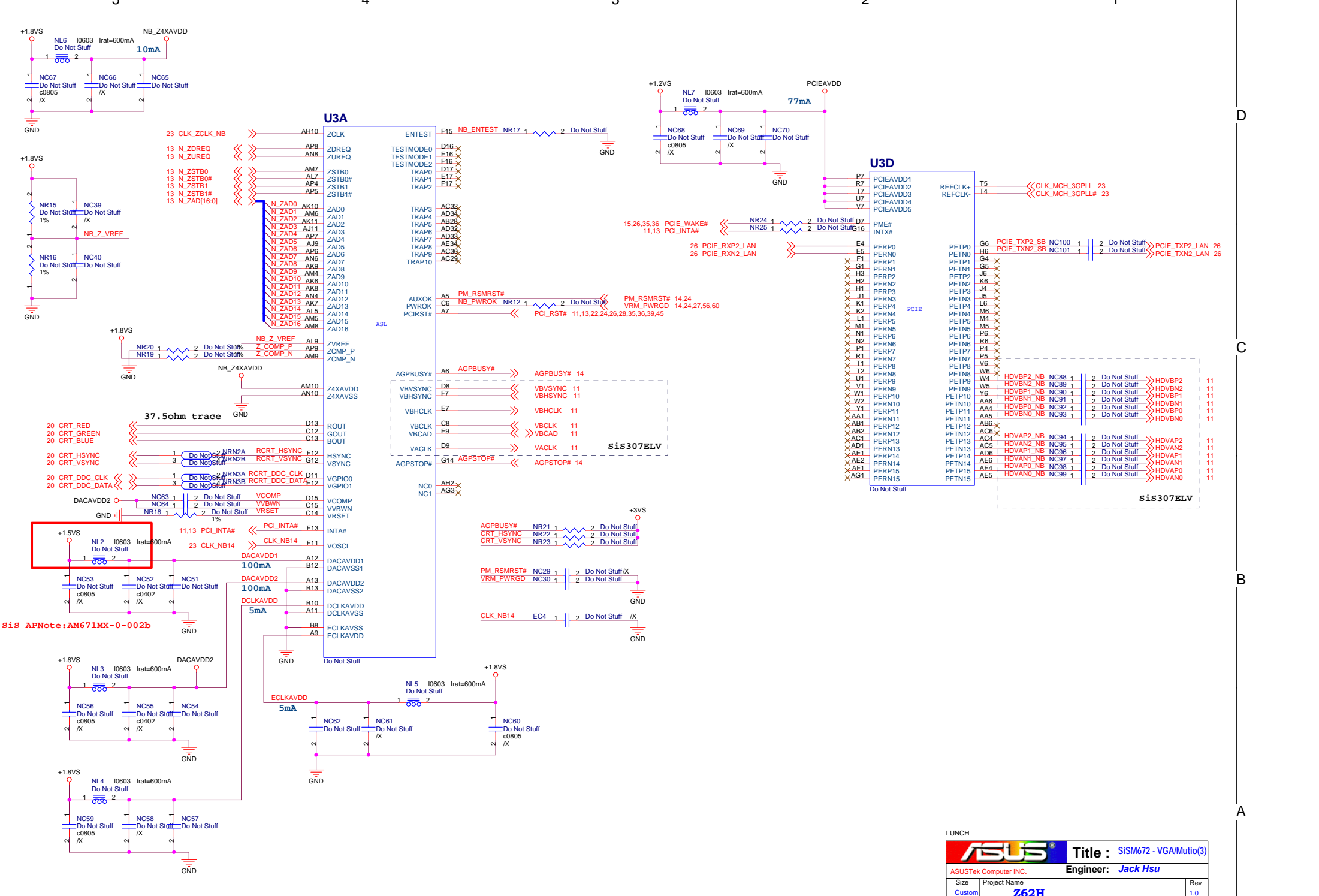
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OCDVREFP
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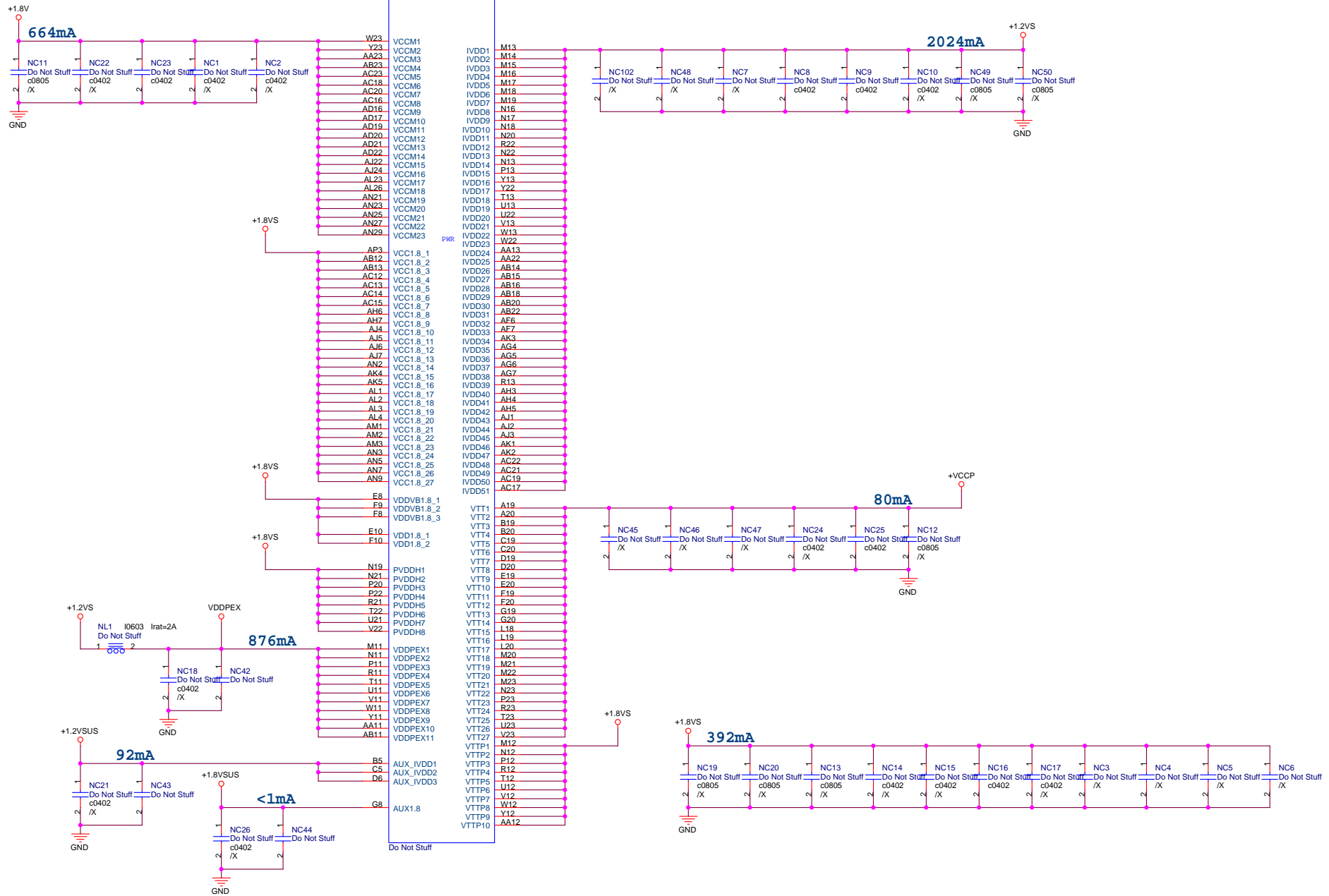
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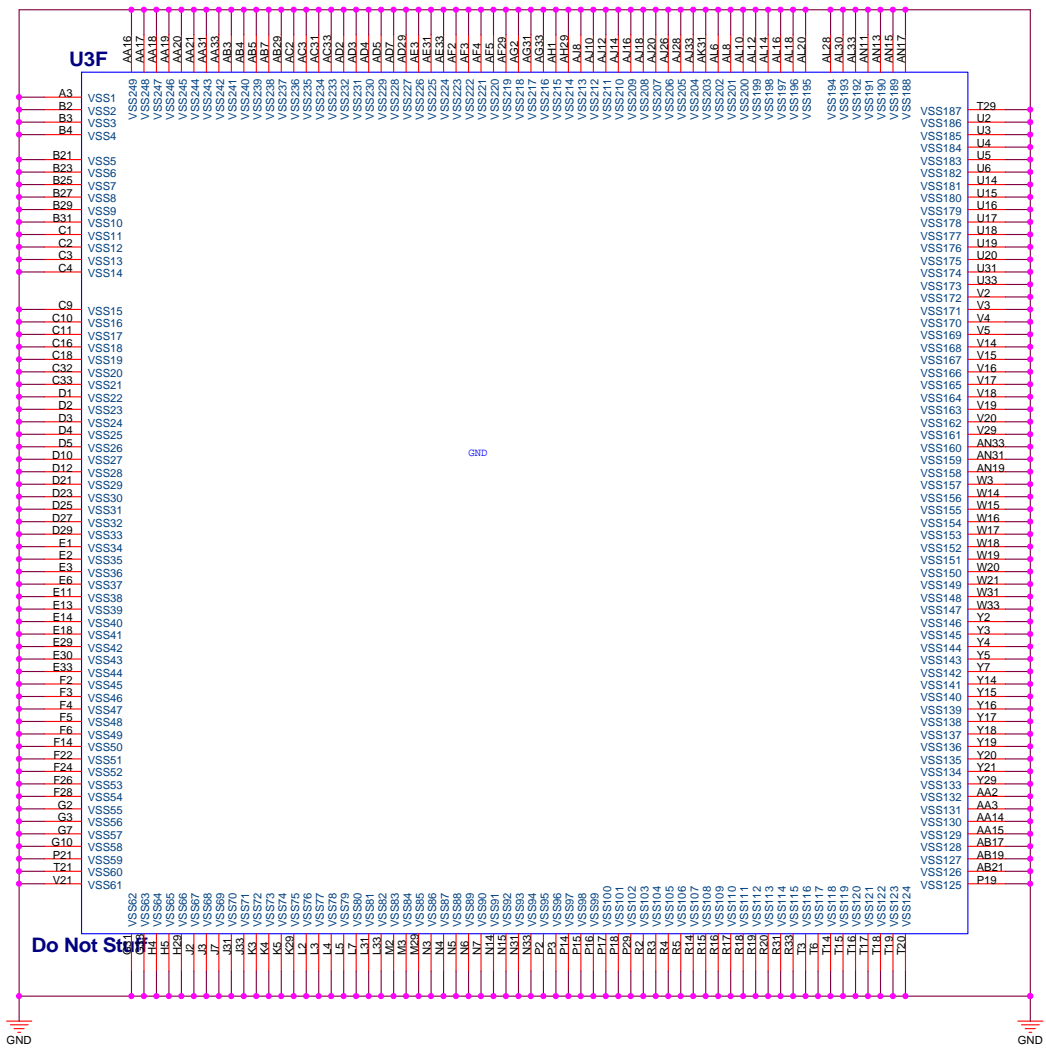


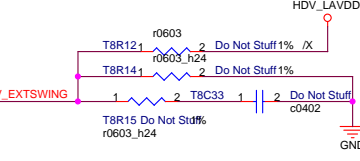
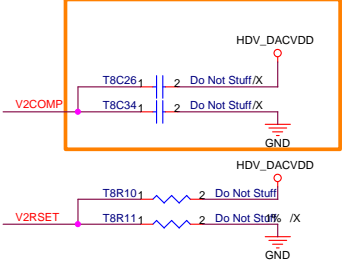
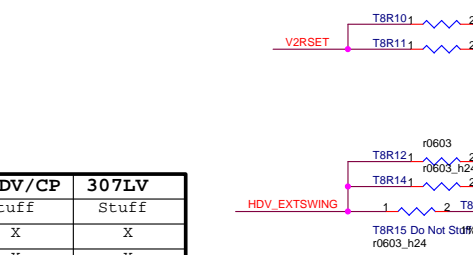
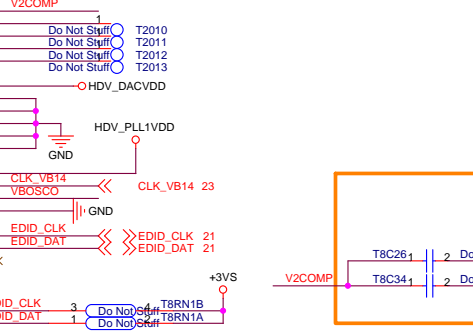
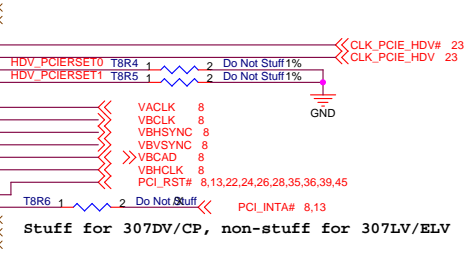
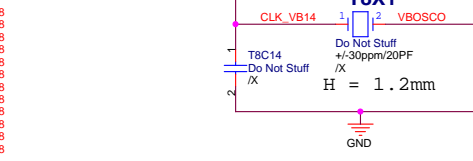
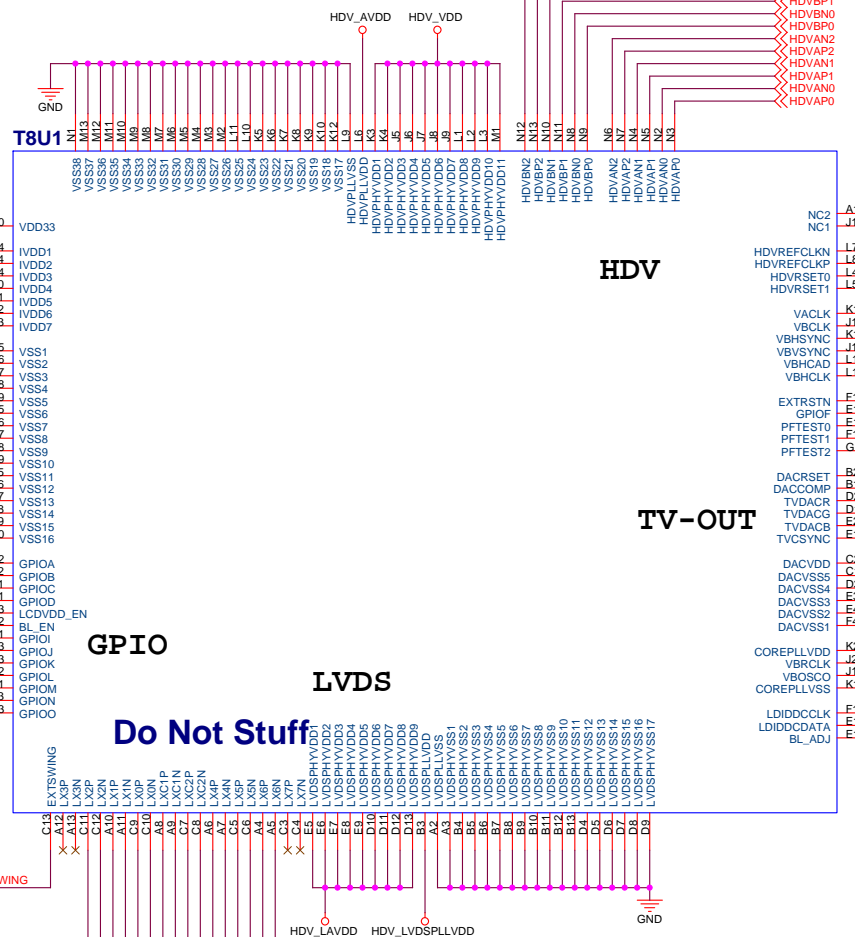
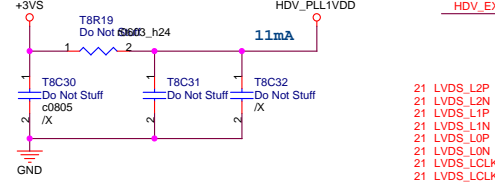
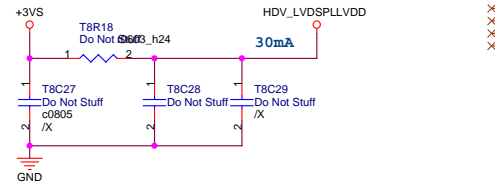
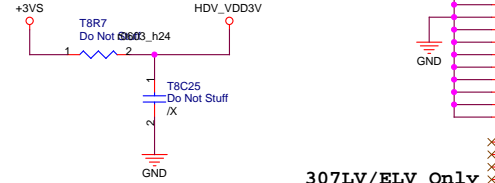
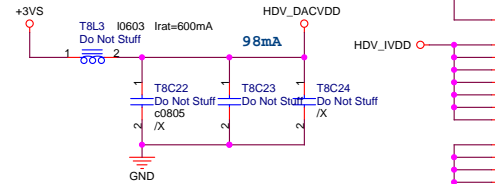
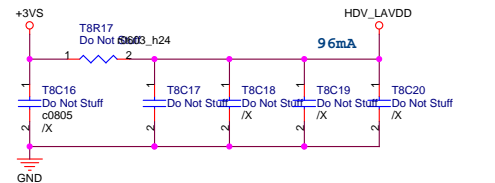
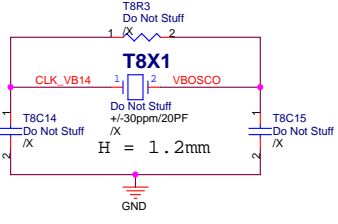
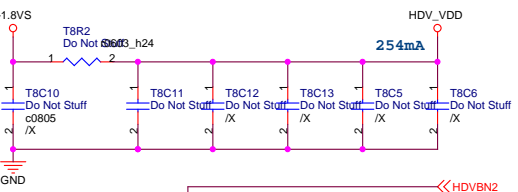
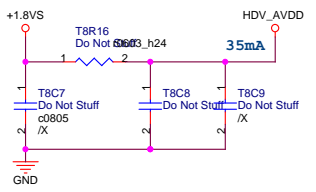
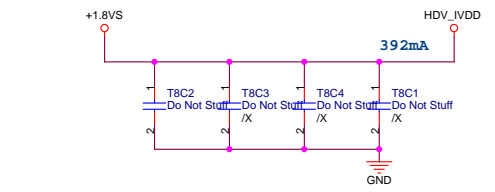
Solder side



U3E







	REF.	307ELV	307DV/CP	307LV
V2COMP	T8C26	0ohm	Stuff	Stuff
	T8RC34	X	X	X
V2RSET	T8R10	Stuff	X	X
	T8R11	X	Stuff	Stuff
EXTSWING	T8R12	X	Stuff	X
	T8R14	Stuff	X	Stuff
	T8R15	Stuff	X	Stuff
	T8C33	Stuff	X	Stuff

02G020003600 C.S SIS307LVMV(B0) BGA169 SIS SIS307LV
 02G020003601 C.S SIS307ELV(B0) BGA167 SIS SIS307ELV

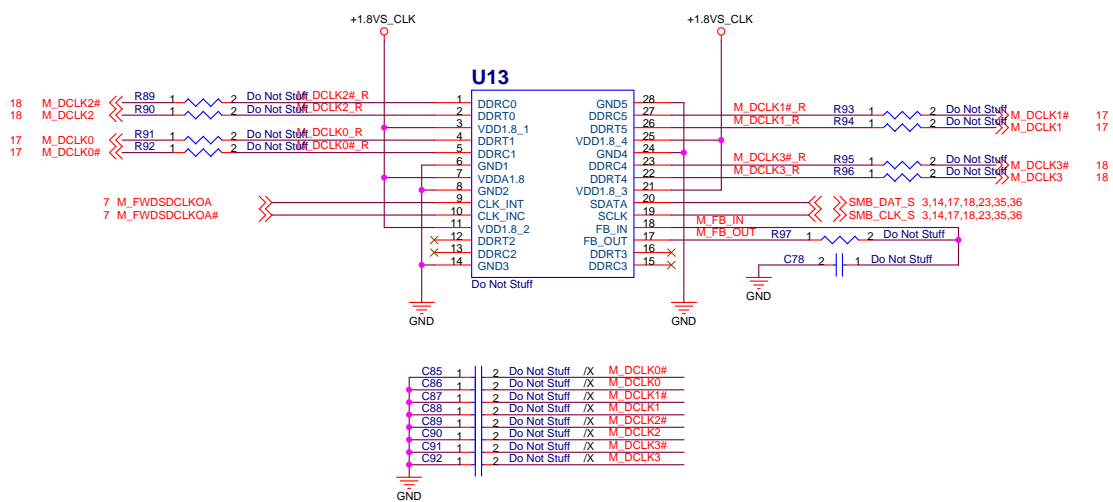
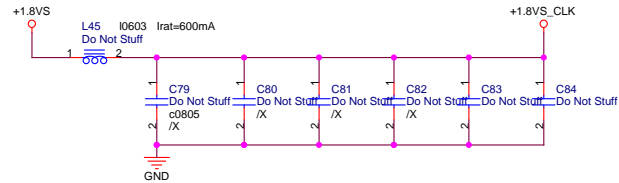
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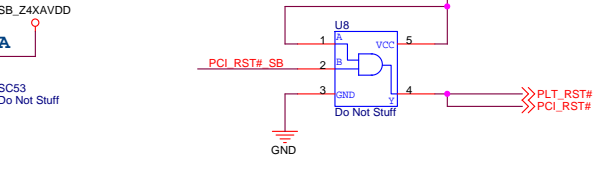
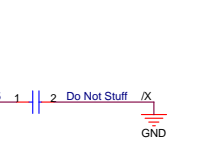
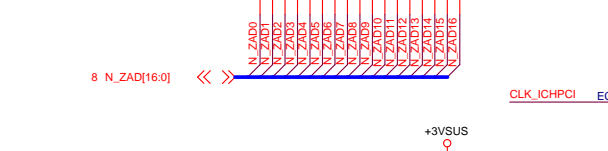
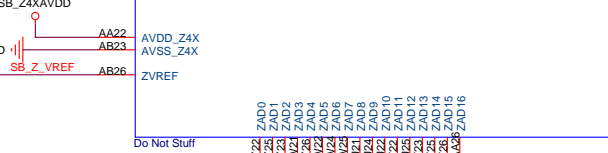
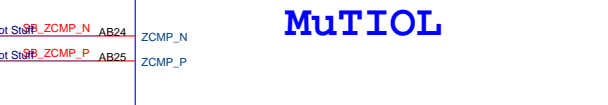
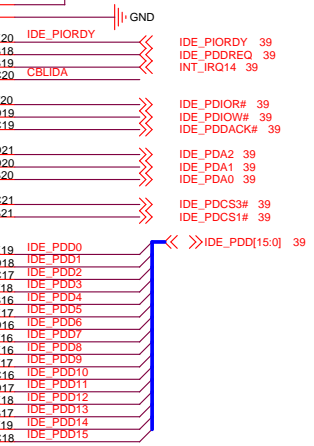
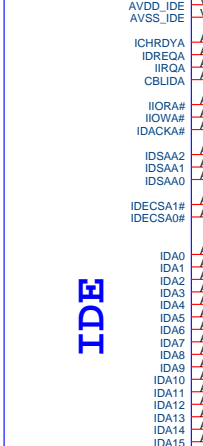
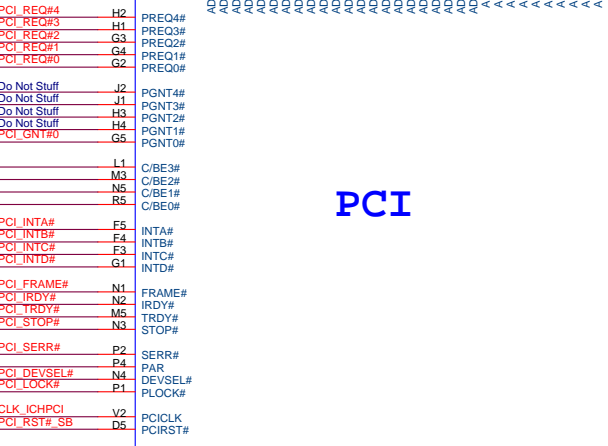
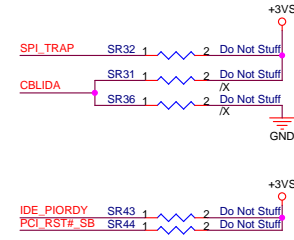
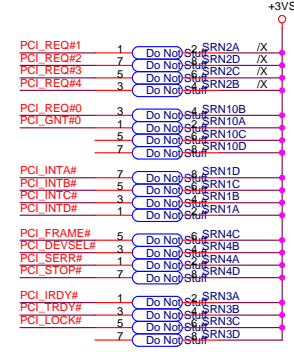
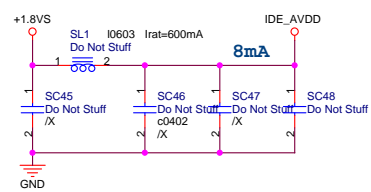
Title : SIS307ELV

ASUSTek Computer INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 11 of 63





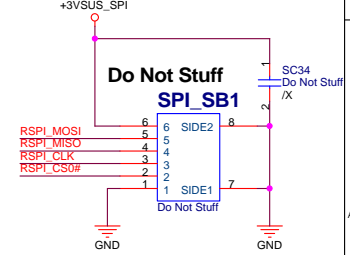
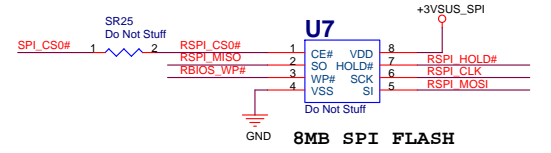
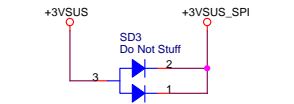
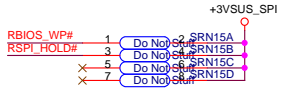
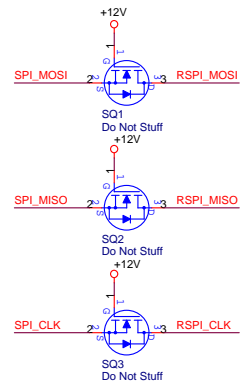
PCI

MuTIOL

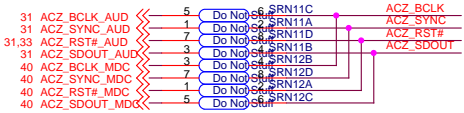
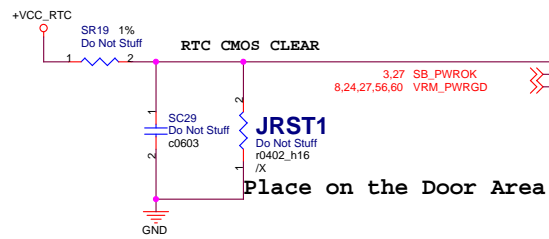
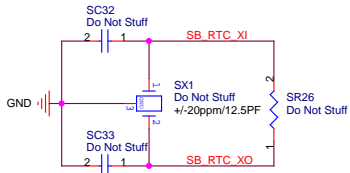
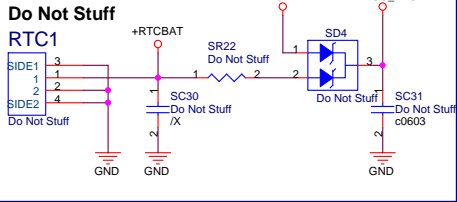
IDE

SPI

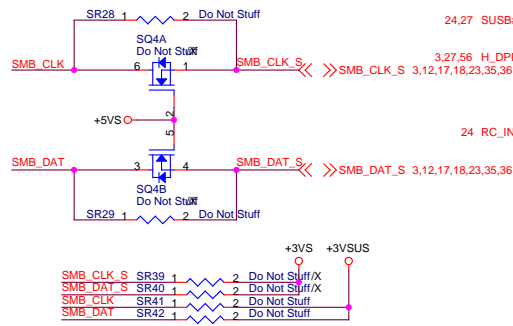
0 : LPC ROM 1 : SPI ROM



RTC BATTERY



SMBus



U6B

CPU_S

- 3 H_INIT# <<> AC23
- 3 H_A20M# <<> AE26
- 3 H_SM# <<> AD23
- 3 H_INTR <<> AC22
- 3 H_NMI <<> AE25
- 3 H_IGNNE# <<> AE24
- 3 H_FERR# <<> AE24
- 3 H_STPCLK# <<> AF25
- 3 H_CPUSLP# <<> AD24
- 8 AGPBUSY# <>> AE23
- 3 H_PROCHOT#_SB <<> AC24
- 3 PM_THRMTRIP# <<> AD25
- 24,44,45 LPC_AD0 <<> Y5
- 24,44,45 LPC_AD1 <<> AA4
- 24,44,45 LPC_AD2 <<> AB2
- 24,44,45 LPC_AD3 <<> AB3
- 24,44,45 LPC_FRAME# <<> AB1
- 24,44,45 LPC_LDRO# <<> AB4
- 24,28,45 INT_SERIRQ <<> AA5
- 24,44,45 LPC_AD0 <<> Y5
- 24,44,45 LPC_AD1 <<> AA4
- 24,44,45 LPC_AD2 <<> AB2
- 24,44,45 LPC_AD3 <<> AB3
- 24,44,45 LPC_FRAME# <<> AB1
- 24,44,45 LPC_LDRO# <<> AB4
- 24,28,45 INT_SERIRQ <<> AA5

APIC

LPC

RTC

SMBUS

HD Audio

ACPI/Others

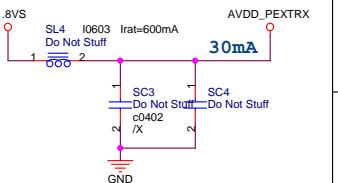
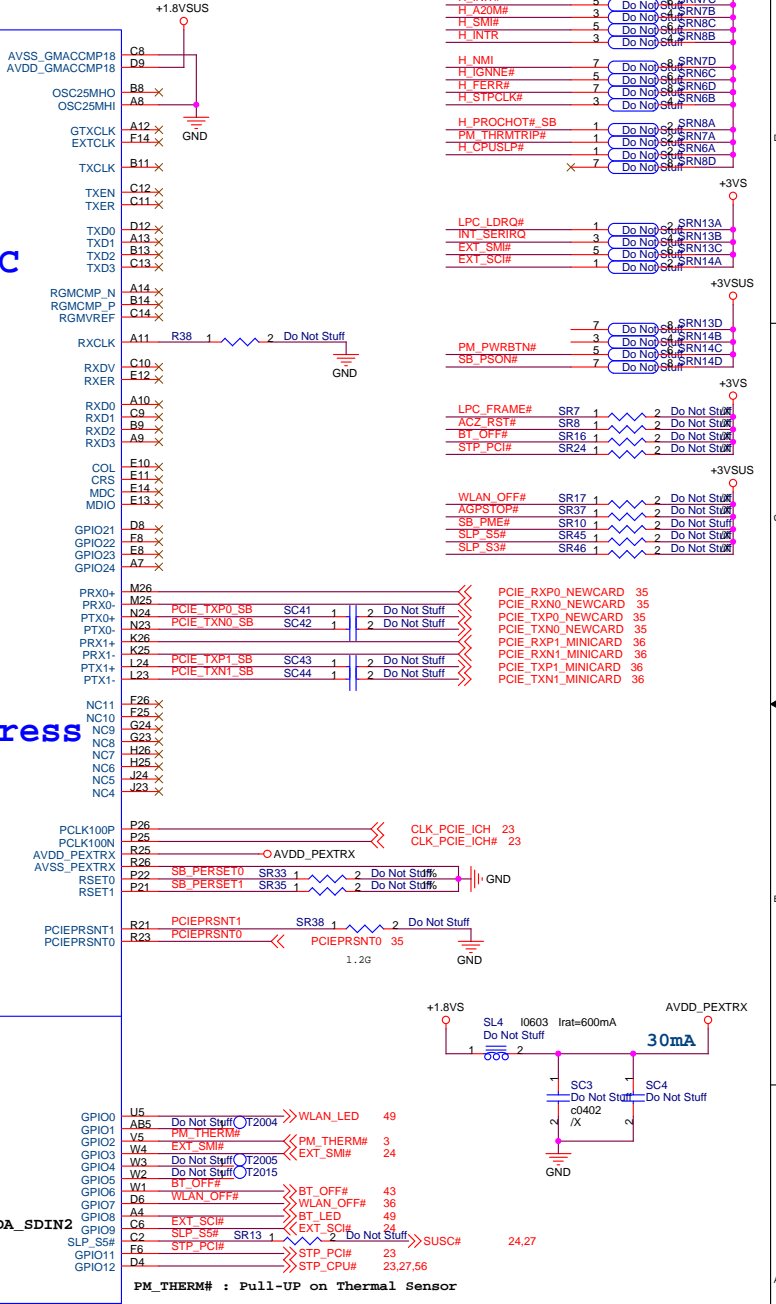
GPIO

- INIT# AC23
- A20M# AE26
- SM# AD23
- INTR AC22
- NMI AE25
- IGNNE# AE24
- FERR# AE24
- STPCLK# AF25
- CPUSLP#_CPUSTUP# AD24
- BMBUSY# AE23
- PROCHOT# AC24
- THERMTRIP# AD25
- LAD0 Y5
- LAD1 AA4
- LAD2 AB2
- LAD3 AB3
- LPC_FRAME# AB1
- LPC_LDRO# AB4
- SIRQ AA5
- OSC32KHO E2
- OSC32KHI E1
- BATOK F1
- PWROK E4
- RTCVDV D1
- RTCVSS D2
- GPIO20 W5
- GPIO19 Y4
- HDA_SDIN0 E5
- HDA_SDIN1 C4
- HDA_SDOUT Y3
- HDA_SYNC Y2
- HDA_RESET# B3
- HDA_BIT_CLK Y1
- OSCI AA2
- ENTEST F2
- SPK AA1
- PWRBTN# E6
- PM_P# A6
- SB_PSON# E7
- AUXOK C3
- ACPILED A5
- GPIO13 D3
- AGPSTOP# B5
- SUBSB# C7
- SR12 1 2 Do Not Stuff SR3#
- SR23 1 2 Do Not Stuff
- HA20GATE D7
- GA20# D7
- SLP_S3# B7
- DPRSTP# B7
- GPIO16
- GPIO17
- GA20# D7
- GPIO18 B4
- GPIO18
- Do Not Stuff
- CLK_SB14 EC6 1 2 Do Not Stuff IX
- AVDD_PEXTRX
- AVSS_PEXTRX
- RSET0
- RSET1
- PCIEPRSN1
- PCIEPRSN0
- GPIO10
- GPIO1
- GPIO2
- GPIO3
- GPIO4
- GPIO5
- GPIO6
- GPIO7
- GPIO8
- GPIO9
- SLP_S5#
- GPIO11
- GPIO12
- WLAN_LED 49
- PM_THERM# 3
- EXT_SM# 24
- BT_LED 49
- BT_OFF# 43
- WLAN_OFF# 36
- EXT_SC# 24
- SUSC# 24,27
- STP_CPU# 23
- STP_CPU# 23,27,56

GMAC

PCI Express

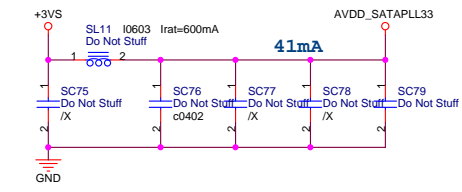
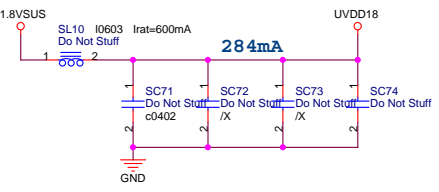
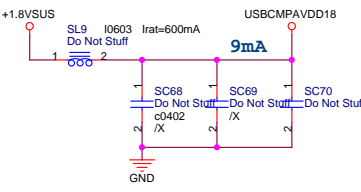
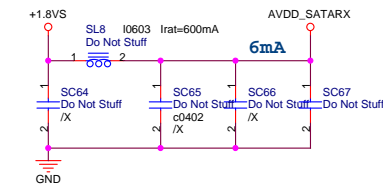
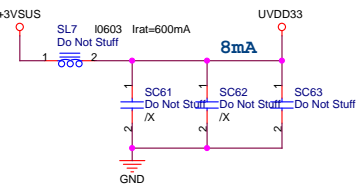
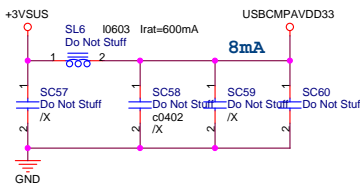
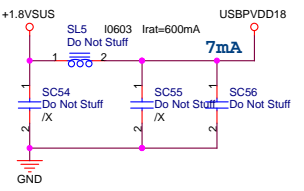
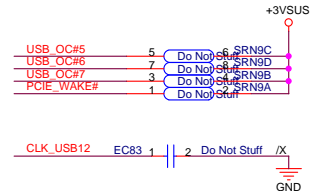
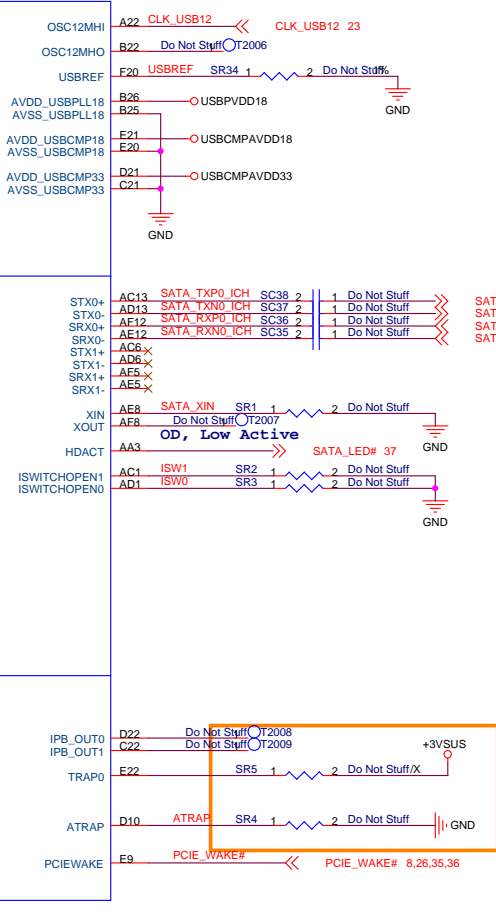
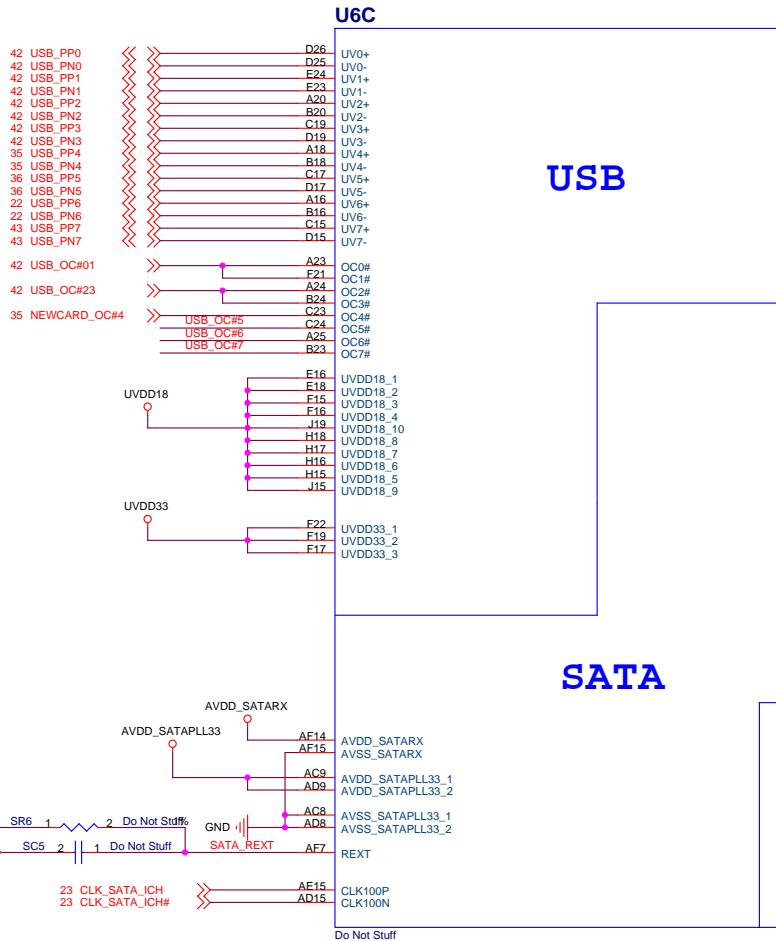
HDA_SDIN2



LUNCH

ASUS Title : SIS968 (1)
 ASUSTek Computer INC. Engineer: Jack Hsu
 Size Project Name
 Custom Z62H Rev 1.0
 Date: Thursday, August 09, 2007 Sheet 14 of 63

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth



U6D

Power / Ground

+1.8VS
522mA

+3VS
33mA

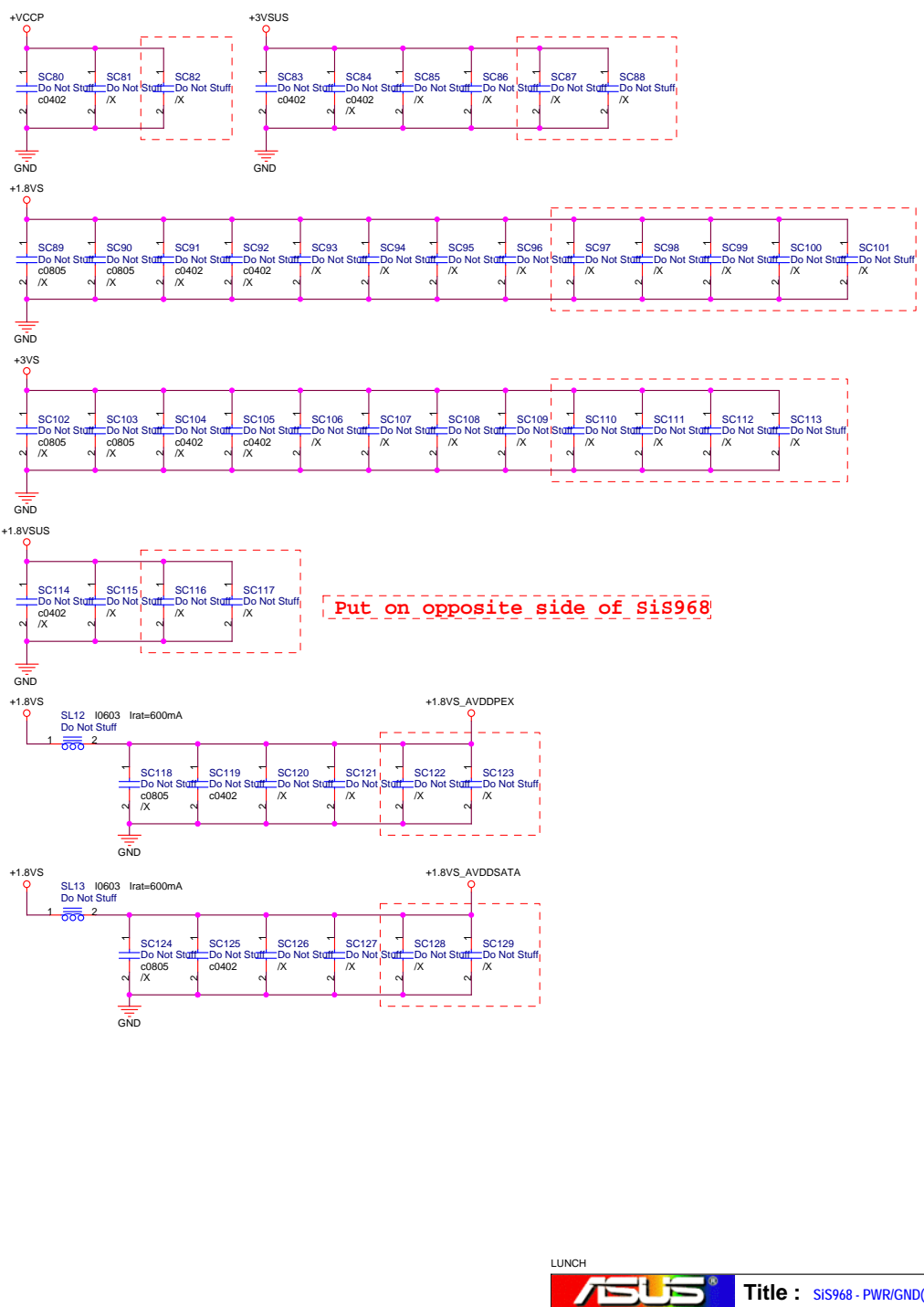
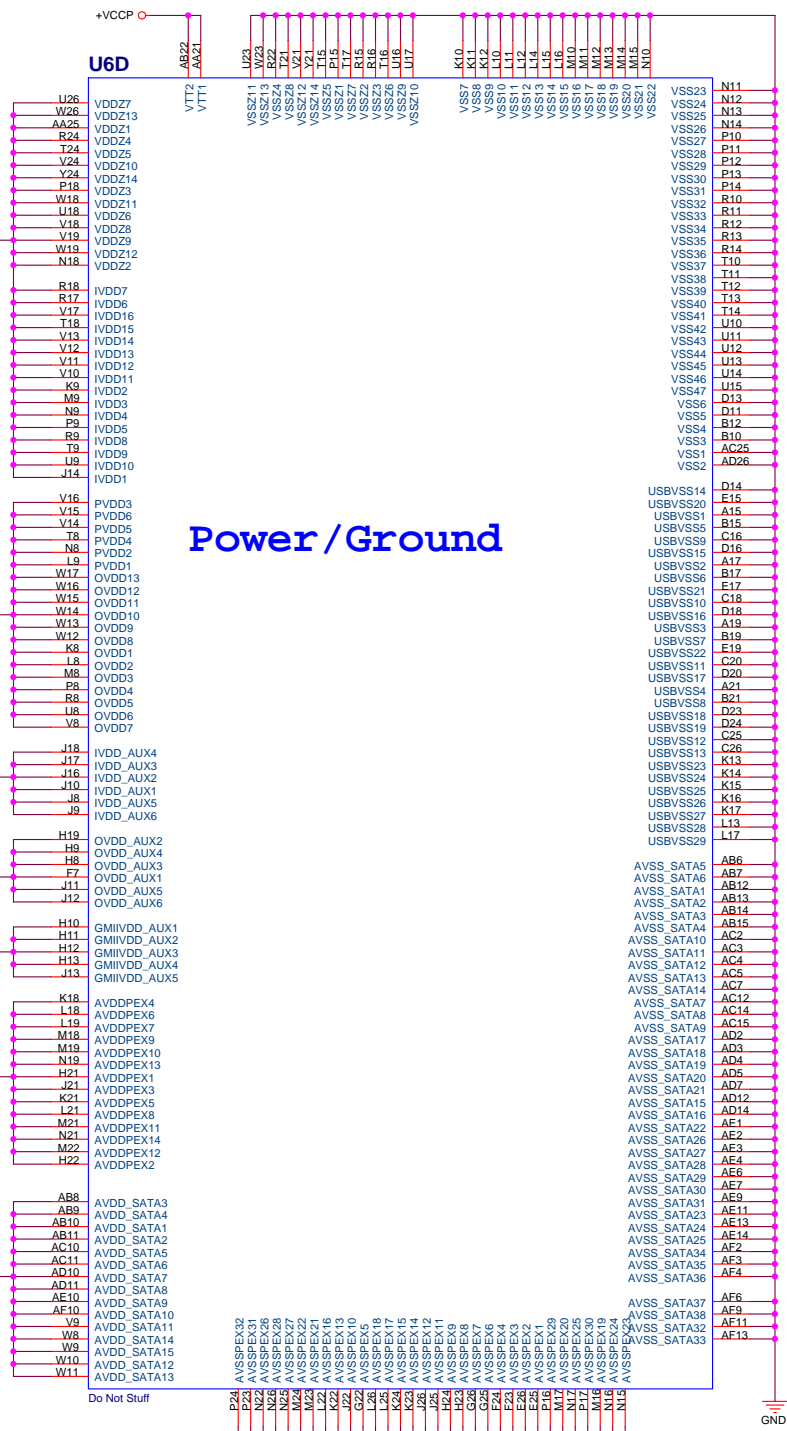
+1.8VSUS
19mA

+3VSUS
4mA

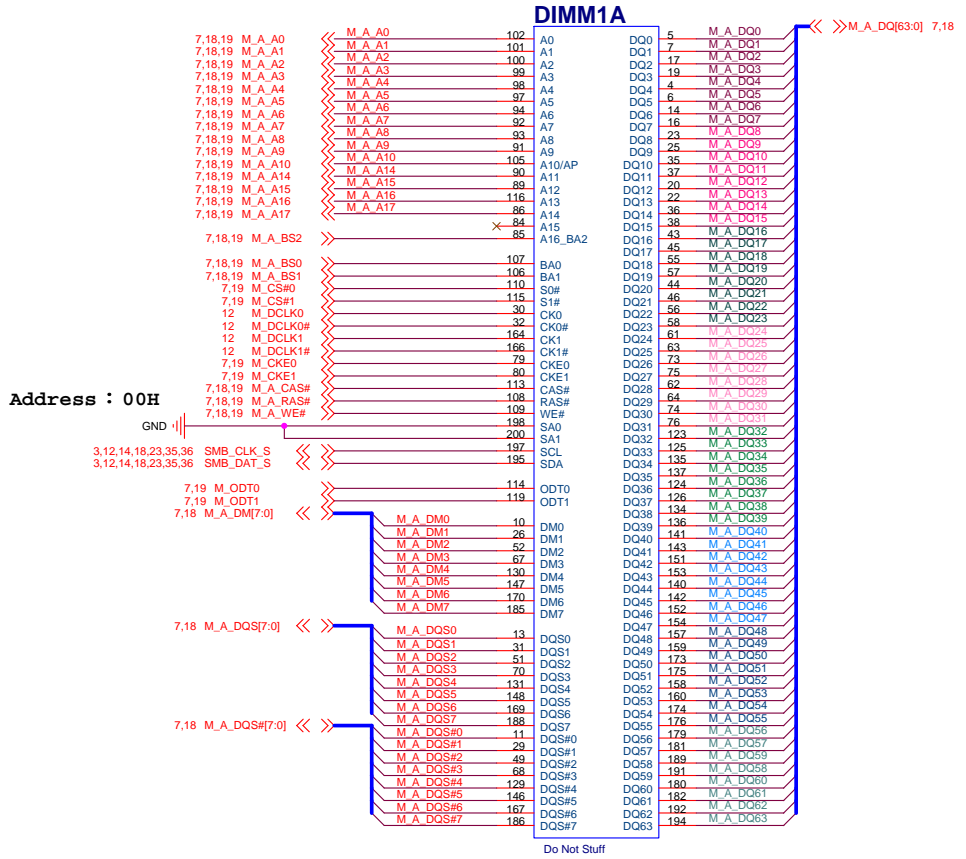
+3VSUS
8mA

+1.8VS_AVDDPEX
153mA

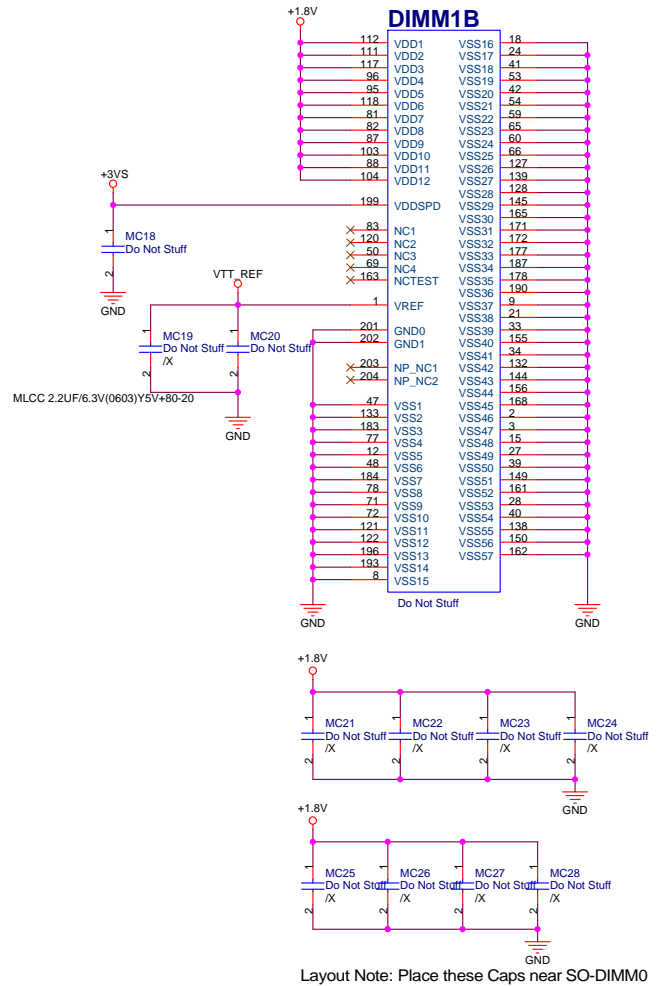
+1.8VS_AVDDSDATA
190mA

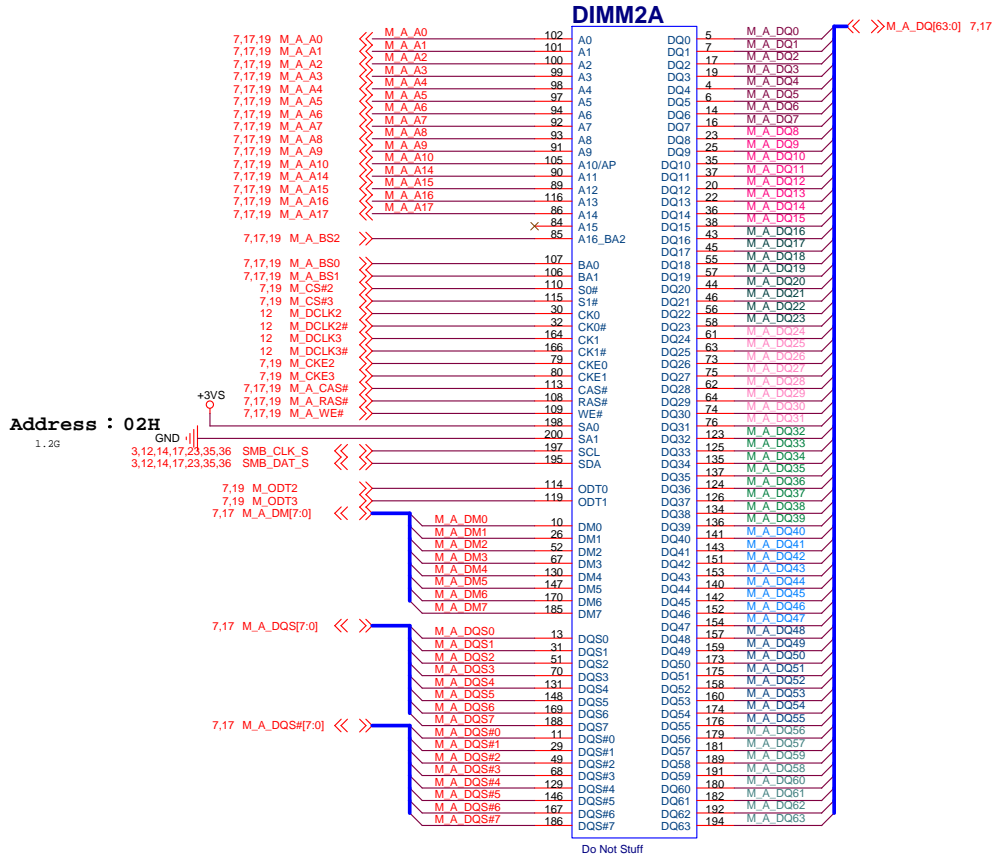


Put on opposite side of S1S968

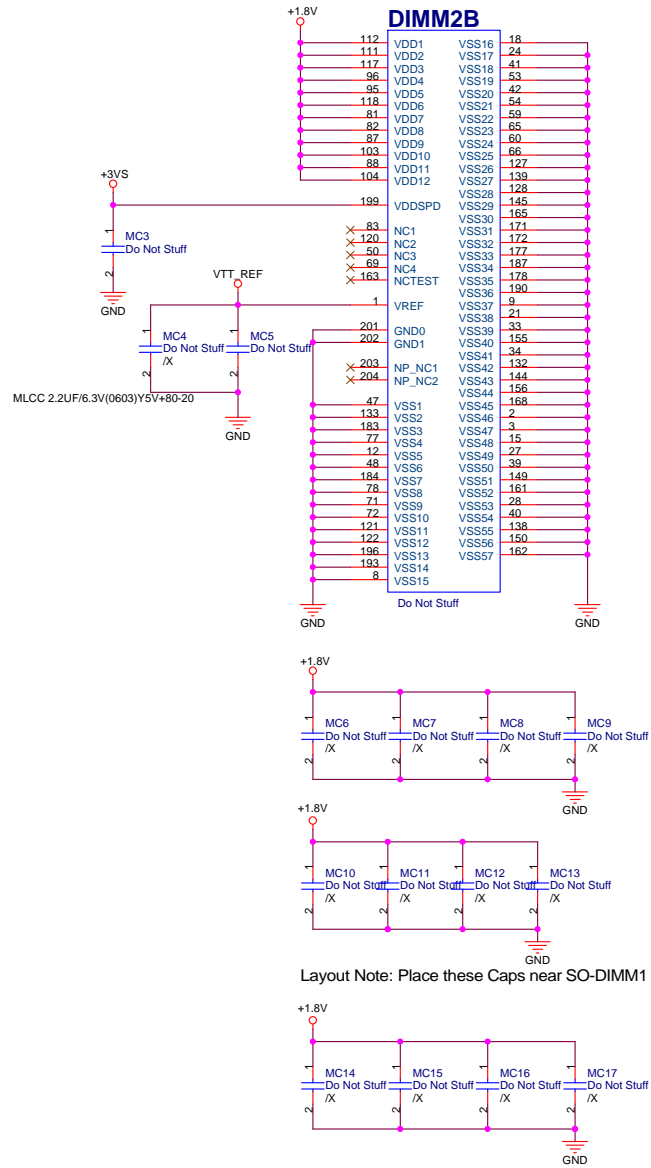


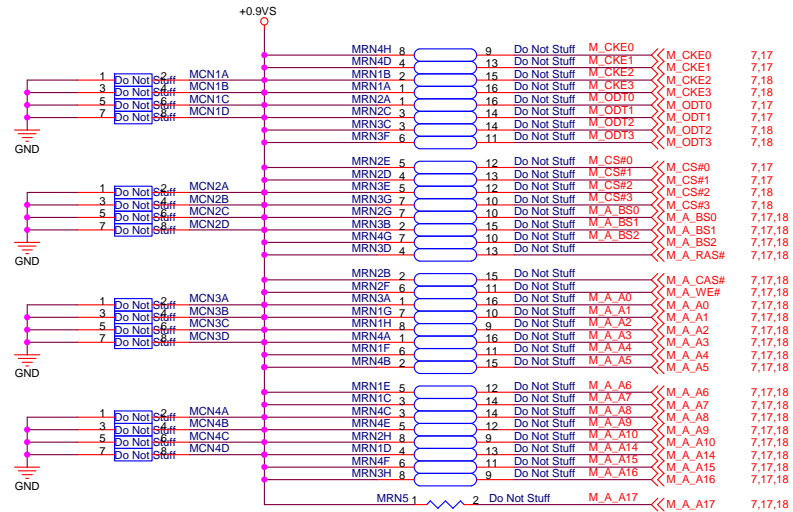
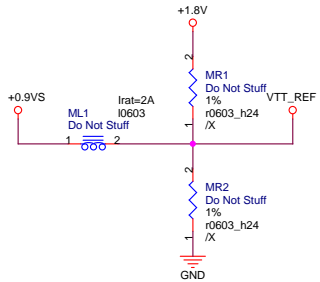
H=9.2mm Standard Type, 12G025C22000
Channel A, DIMM 0





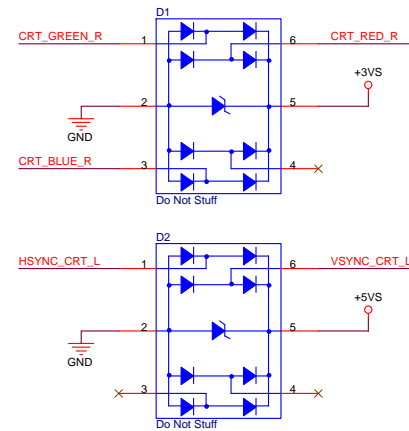
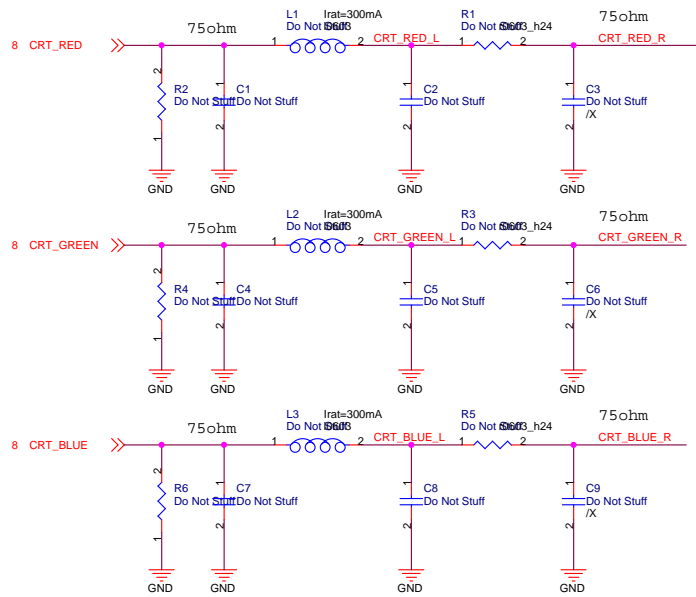
H=5.2mm Standard Type, 12G025122007
Channel A, DIMM 1





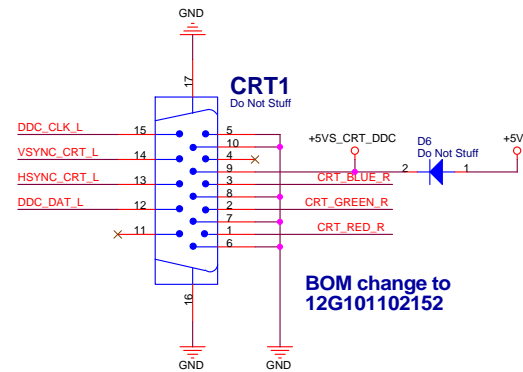
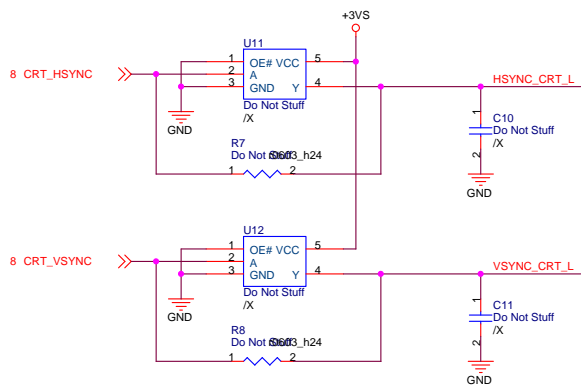
DDR2: Command, Control Signal need termination

Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V

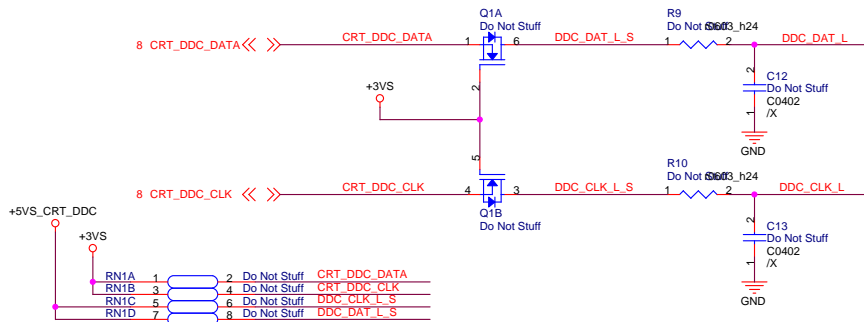


ESD Diodes

Place ESD Diodes near CRT Connector



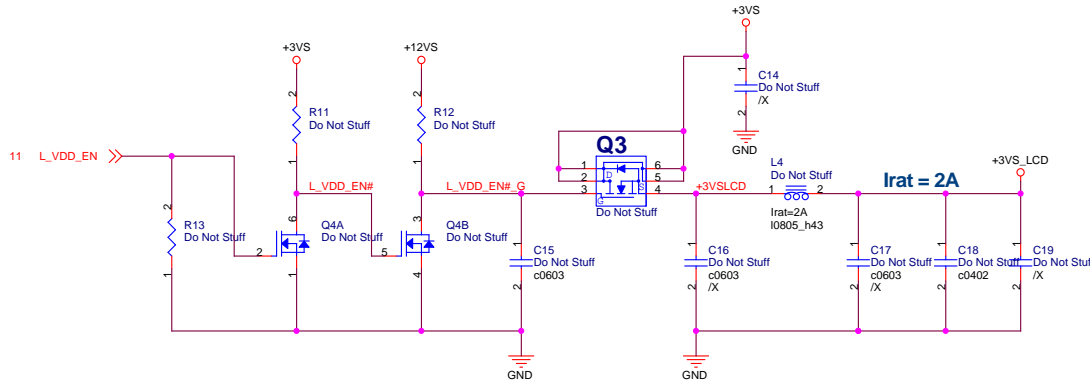
CRT Connector



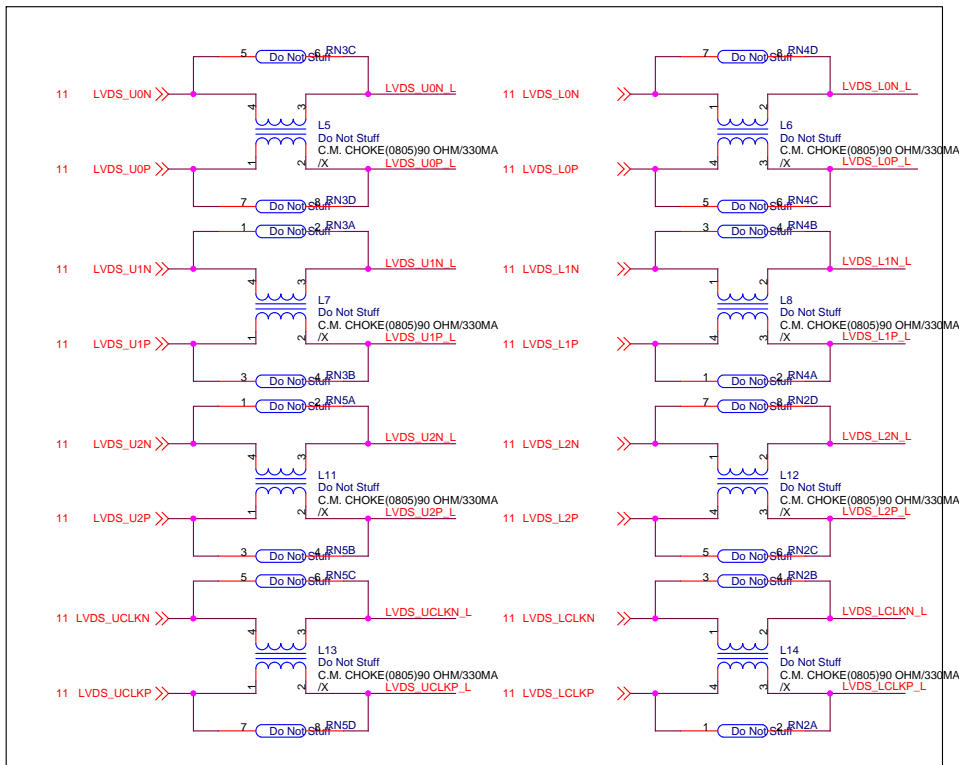
LUNCH

ASUS		Title : CRT Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	20	of 63

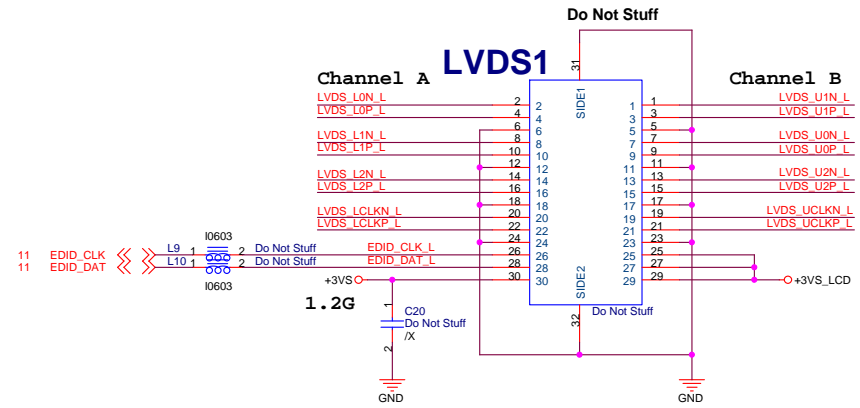
LCD Power Switch



LVDS NUT



LVDS Connector



Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

LUNCH

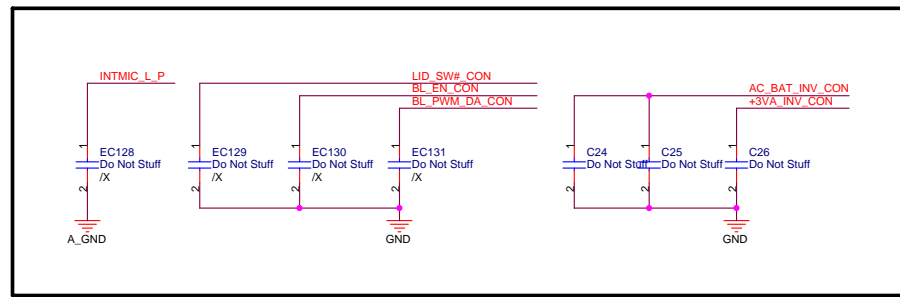
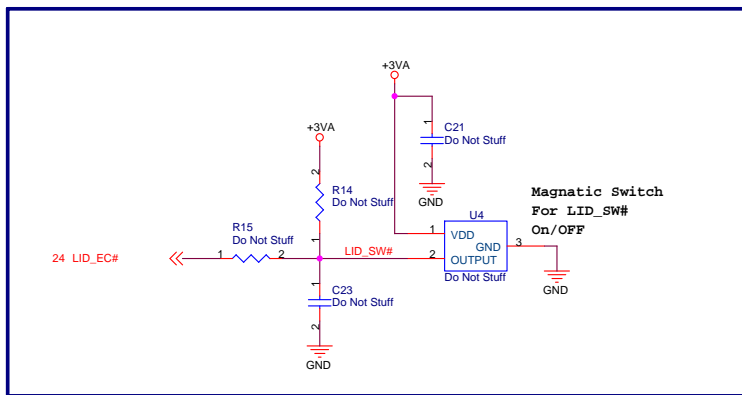
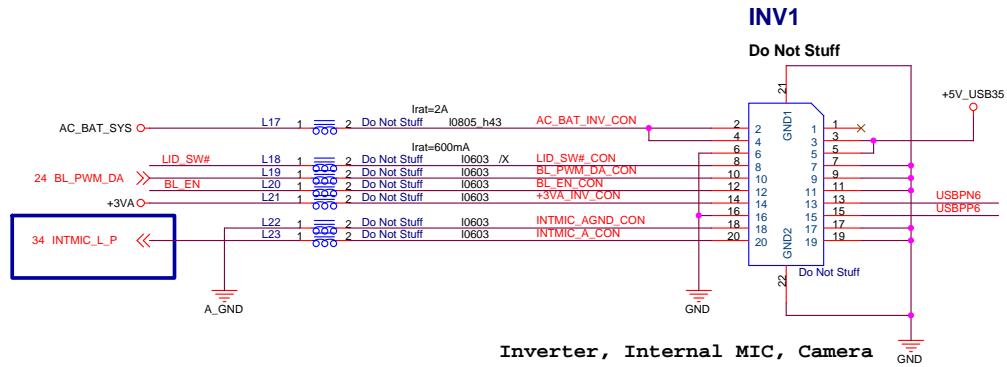
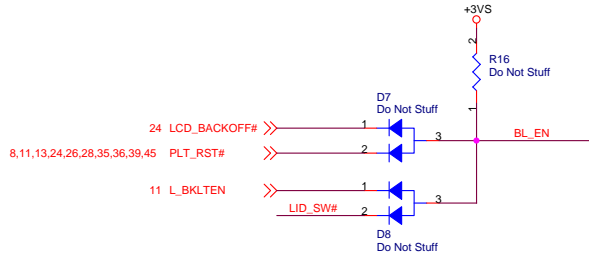
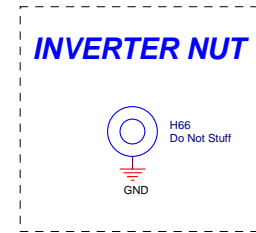
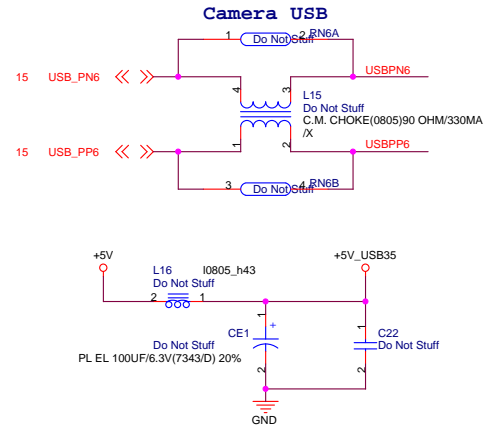
ASUS		Title : LVDS Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	21	of 63

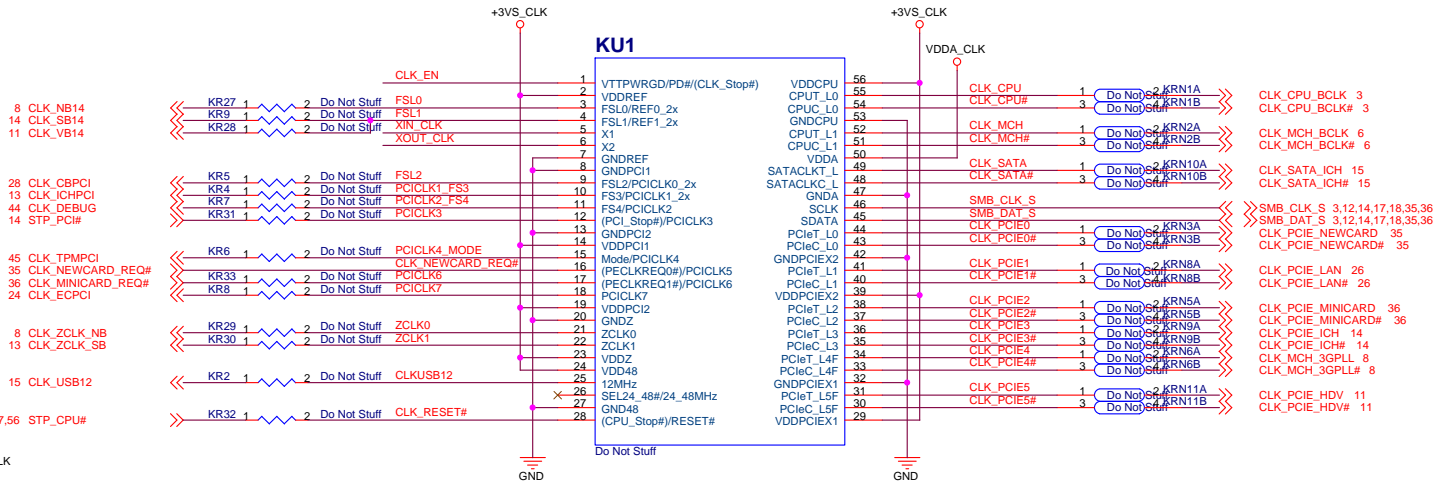
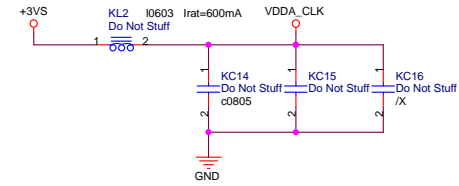
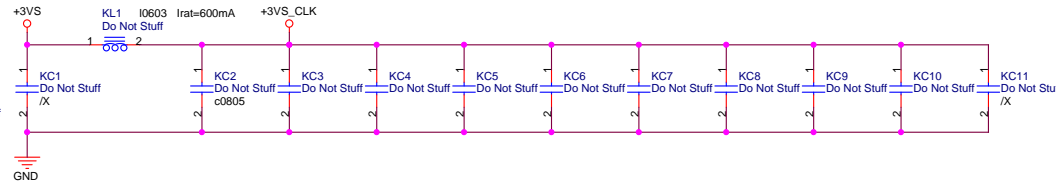
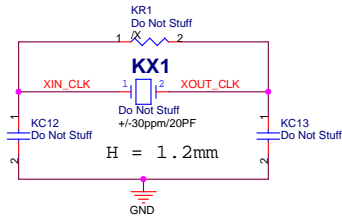
INVERTER Interface

BIOS
LCD_BACKOFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back light.

Inverter Board built in 14.1W LCD Panel





- 8 CLK_NB14
- 14 CLK_SB14
- 11 CLK_VB14

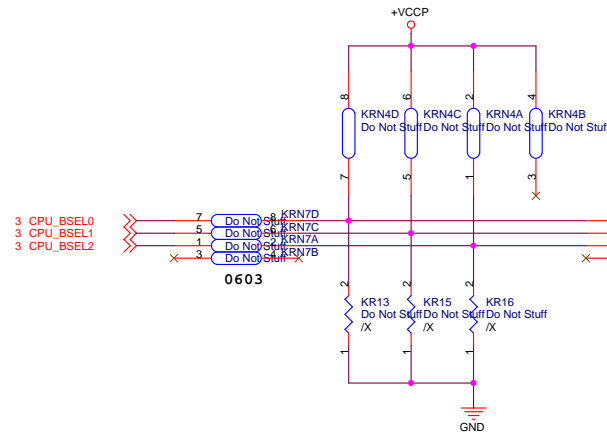
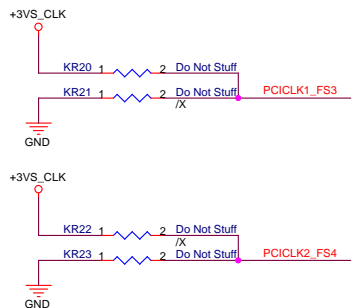
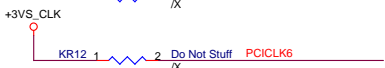
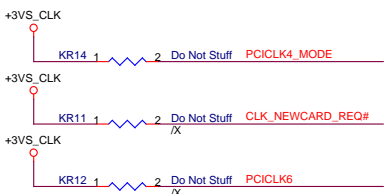
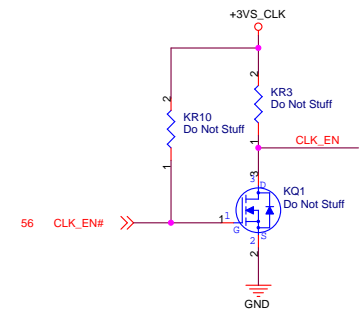
- 28 CLK_CBPCI
- 13 CLK_ICHPCI
- 44 CLK_DEBUG
- 14 STP_PCI#

- 45 CLK_TPMPCI
- 35 CLK_NEWCARD_REQ#
- 36 CLK_MINICARD_REQ#
- 24 CLK_ECPCI

- 8 CLK_ZCLK_NB
- 13 CLK_ZCLK_SB

- 15 CLK_USB12

- 14,27,56 STP_CPU#

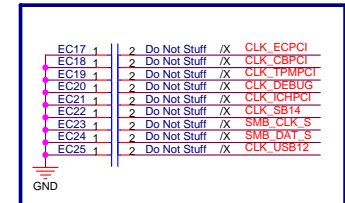


- 3 CPU_BSEL0
- 3 CPU_BSEL1
- 3 CPU_BSEL2

0603

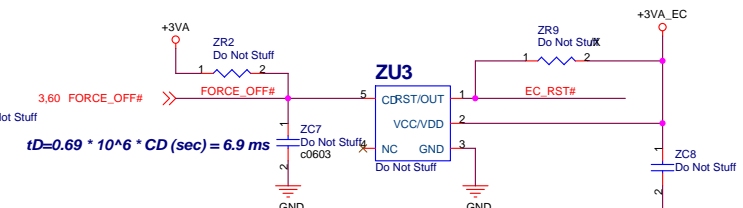
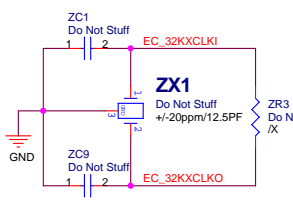
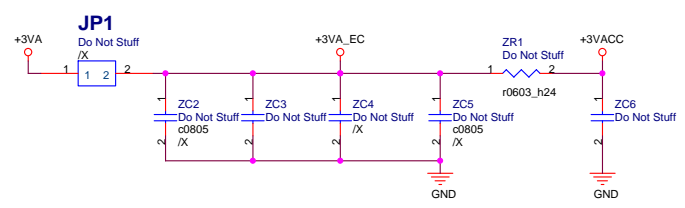
CLK trapped by CPU's BSEL

BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

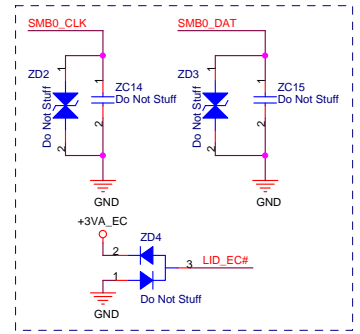
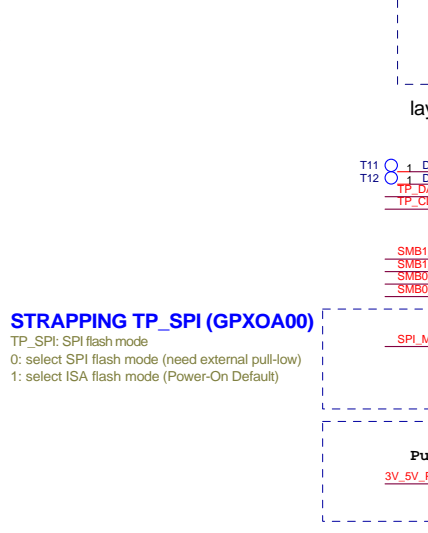
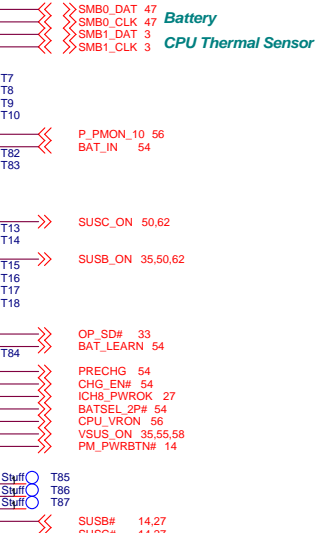
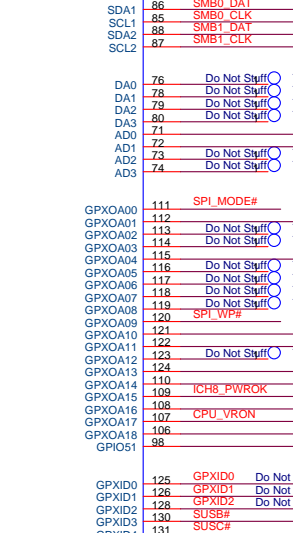
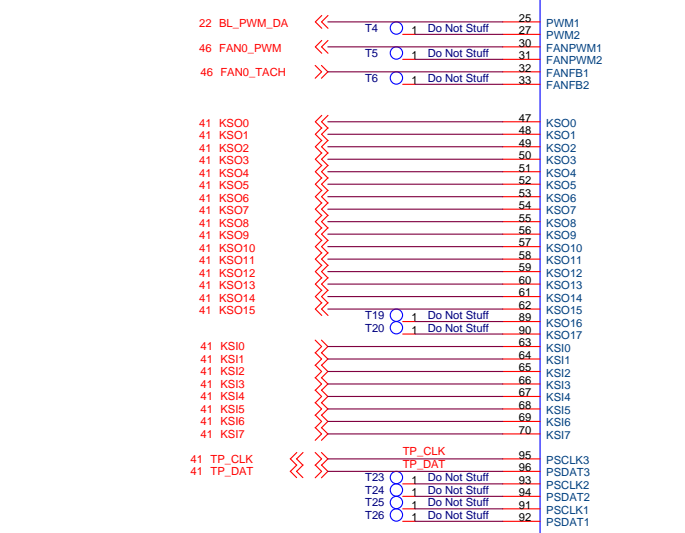
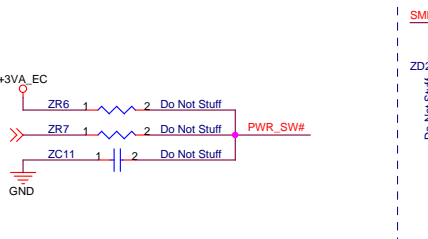
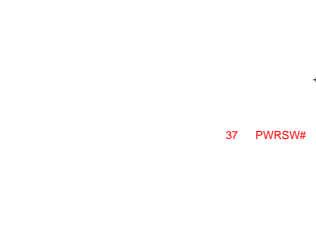
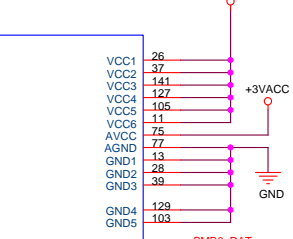
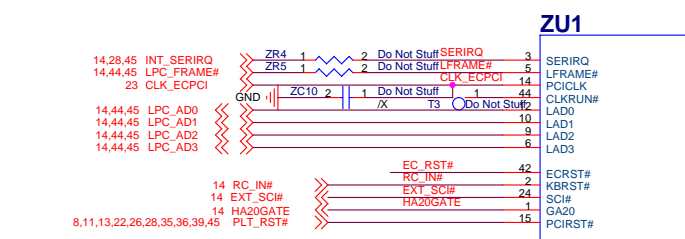


LUNCH

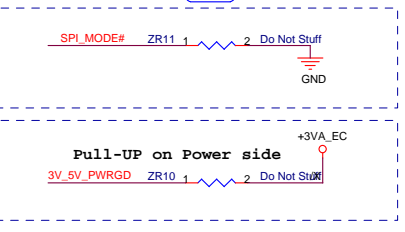
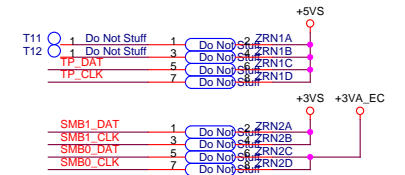
ASUS Title : ICS9LPR600
 ASUSTek Computer INC. Engineer: Jack Hsu
 Size Project Name
 Custom Z62H
 Date: Thursday, August 09, 2007 Sheet 23 of 63



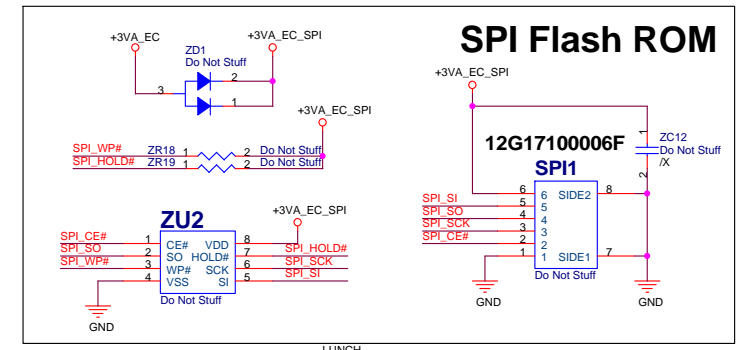
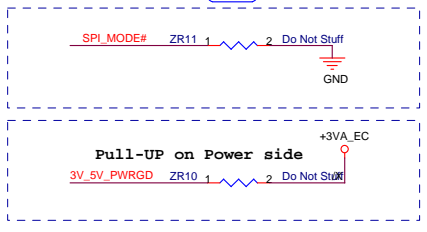
Detector Threshold: 2.7V, CMOS OUTPUT



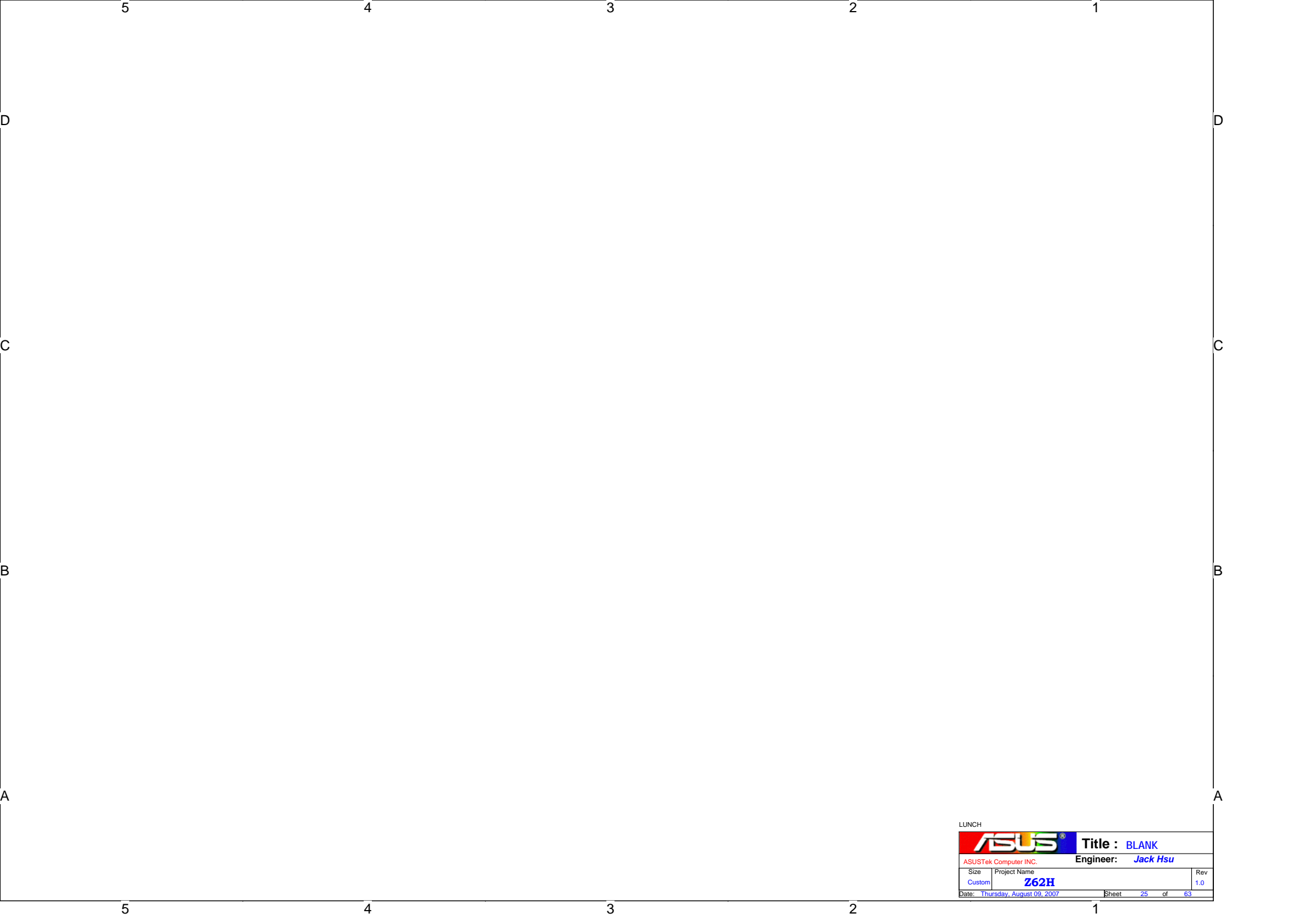
layout note: place close to connector



STRAPPING TP_SPI (GPXOA00)
 TP_SPI: SPI flash mode
 0: select SPI flash mode (need external pull-low)
 1: select ISA flash mode (Power-On Default)



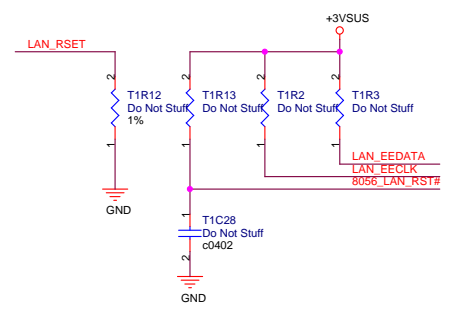
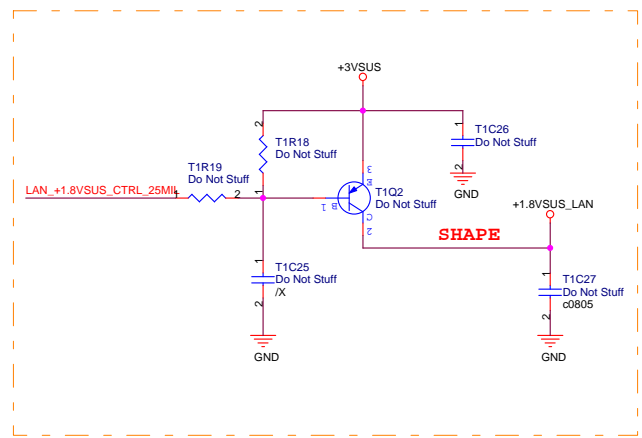
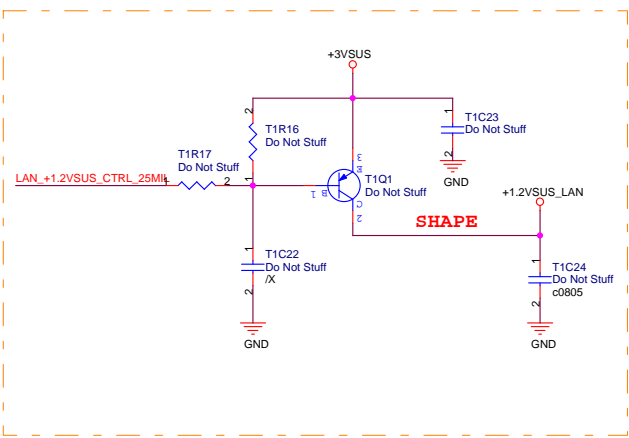
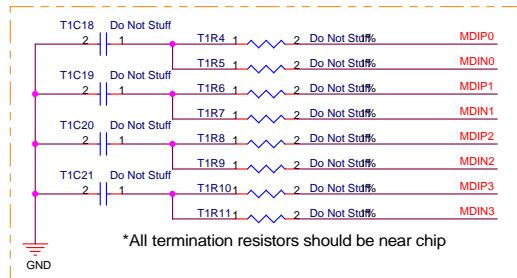
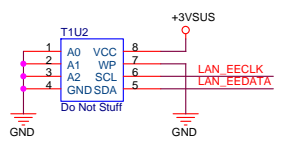
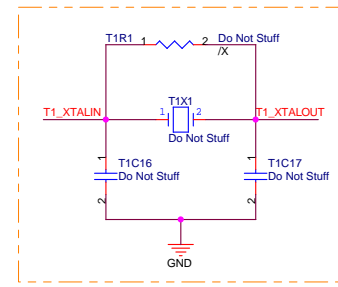
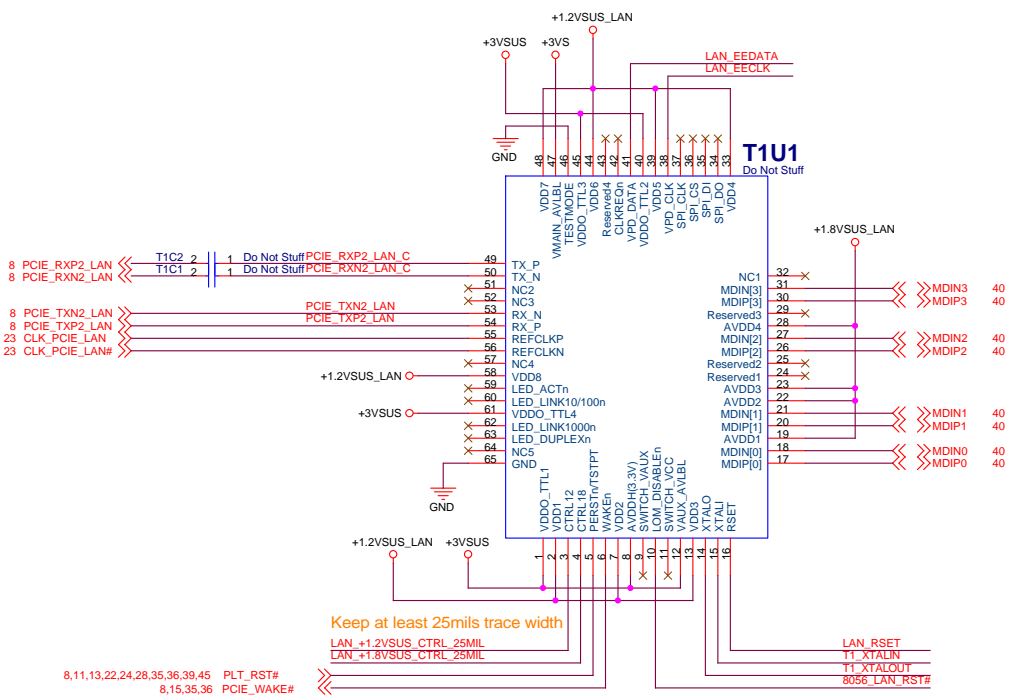
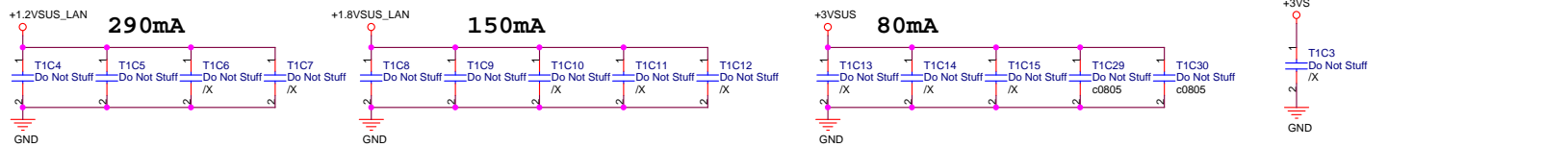
ASUS P/N:
 A0 : 02G890000400
 B1 : 02G890000410

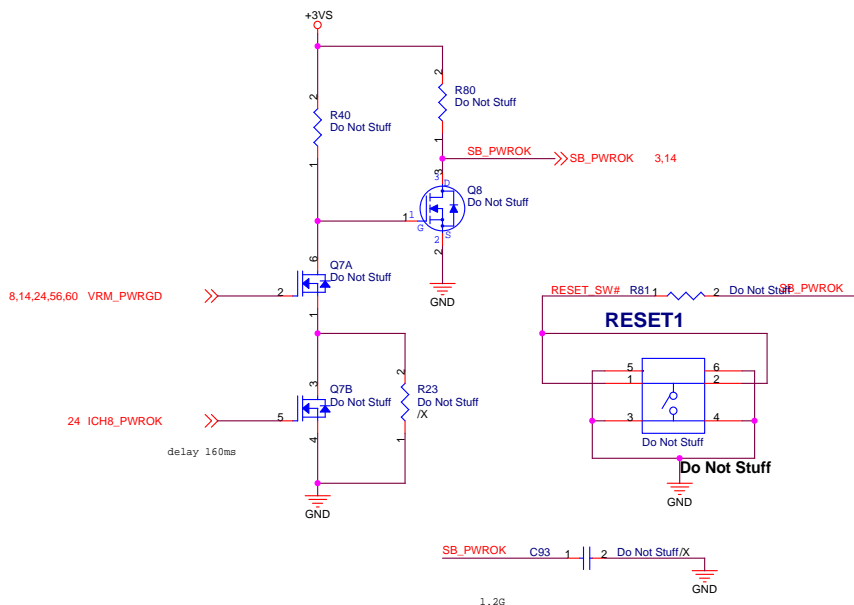
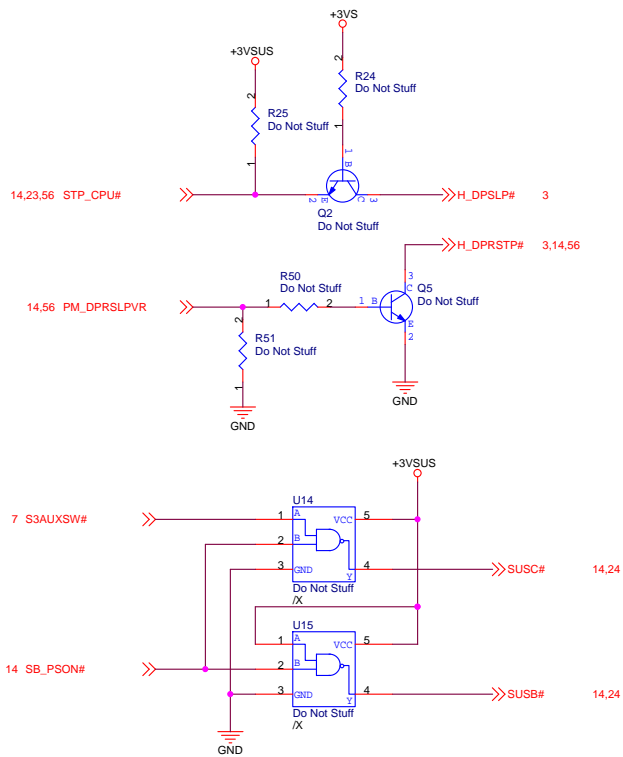


LUNCH

		Title : BLANK	
ASUSTek Computer INC.		Engineer: <i>Jack Hsu</i>	
Size Custom	Project Name Z62H	Date: <u>Thursday, August 09, 2007</u>	Rev 1.0
Date: <u>Thursday, August 09, 2007</u>		Sheet <u>25</u> of <u>63</u>	

ASUS P/N:
A2:02G751006700
B0:02G751006710





Power ON & OFF:

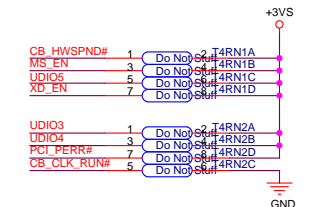
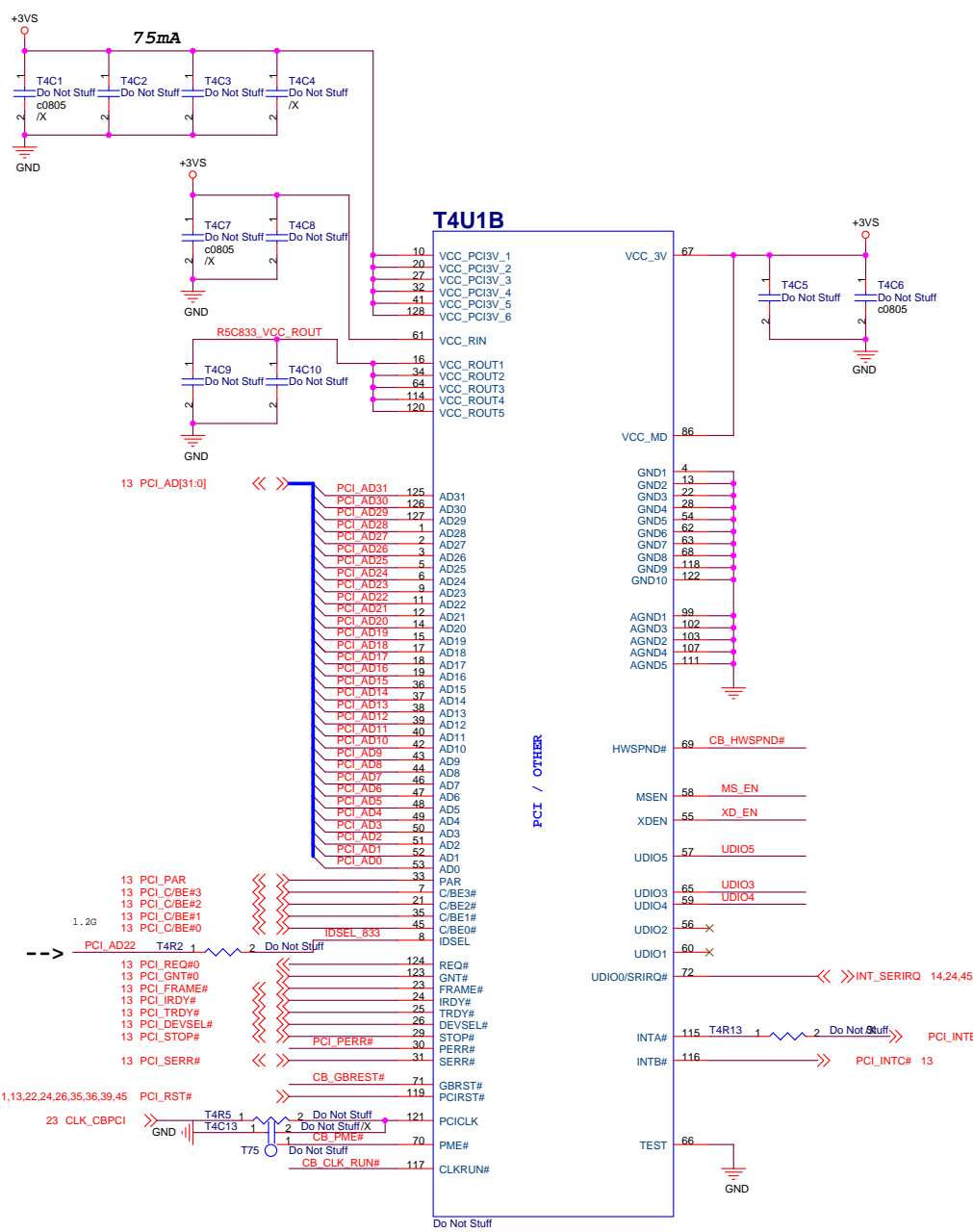
	S5	→ S0	→ S5
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC# (S4)	0	1	0
SUSB# (S3)	0	1	0
Power Status	System	Main	System

Sleep & Wake up

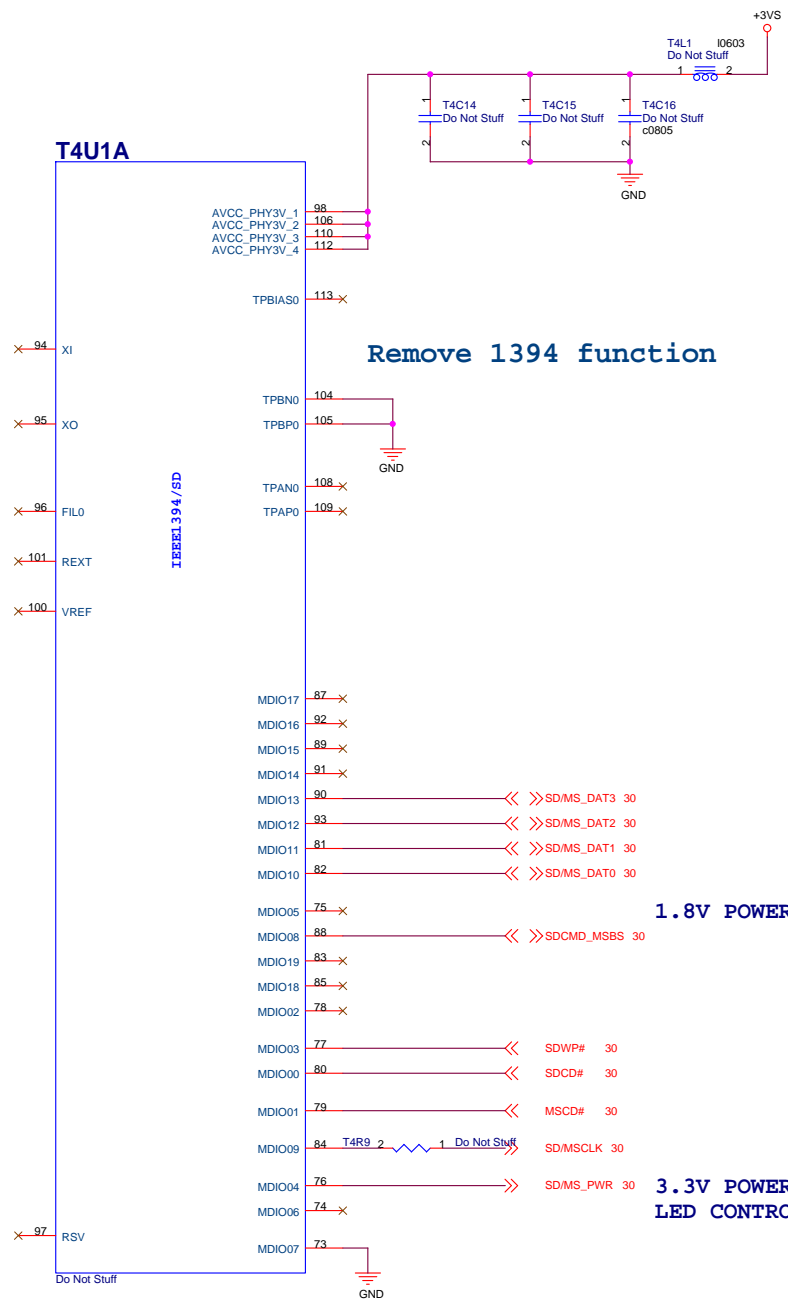
	S0	→ S3	→ S0
S3AUXSW#	1	0	0
SB_PSON#	0	0	1
SUSC# (S4)	1	1	1
SUSB# (S3)	1	1	0
Power Status	Main	Main	System, S4

LUNCH

		Title : OTHER
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	Z62H	1.0
Date: Thursday, August 09, 2007		Sheet 27 of 63



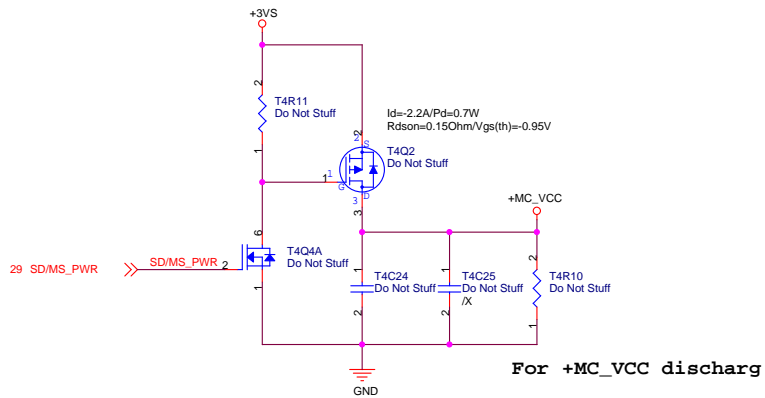
SD enable : UDIO3 pull-up
 MMC enable : UDIO4 pull-up
 Use EPROM : UDIO5 pull-down
 Otherwise : disable or non-use



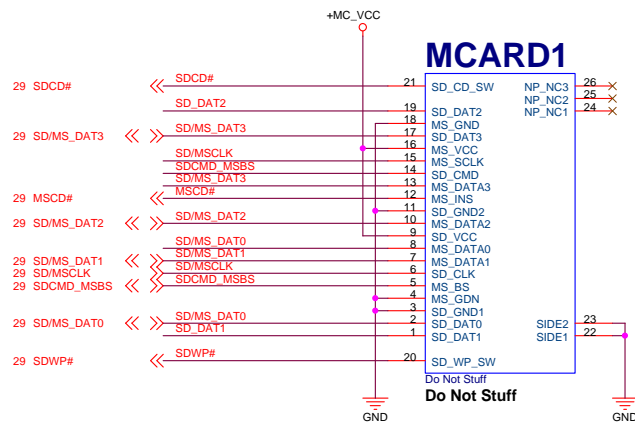
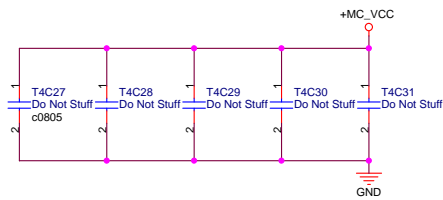
Remove 1394 function

1.8V POWER CONTROL

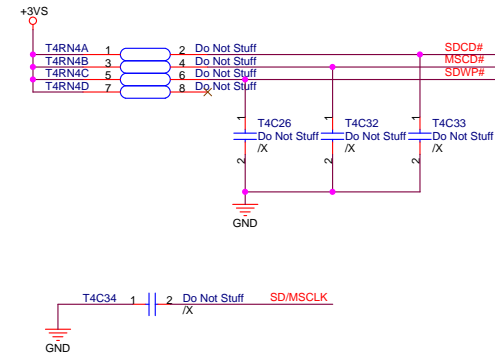
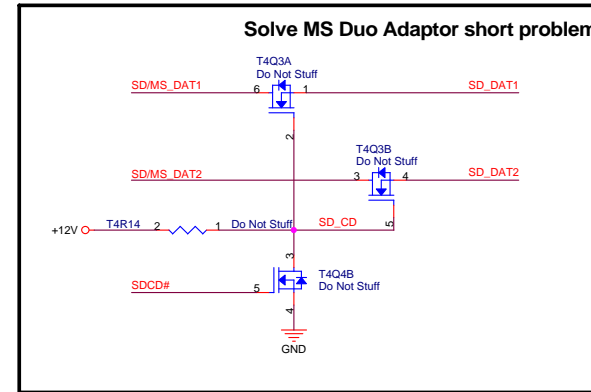
3.3V POWER CONTROL
LED CONTROL



Card Reader Power Switcher

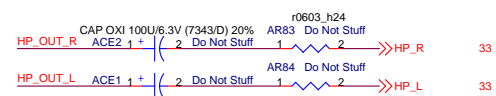
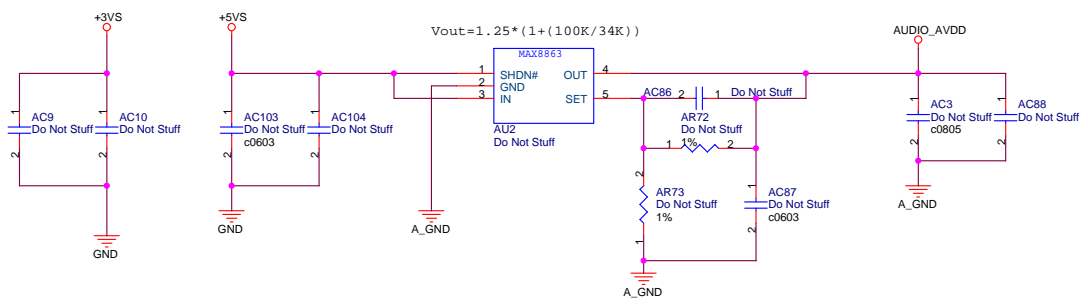
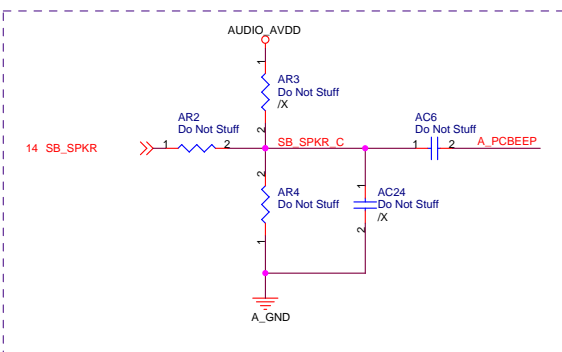


3 in 1 Card Reader

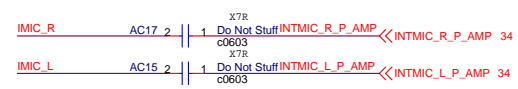


LUNCH

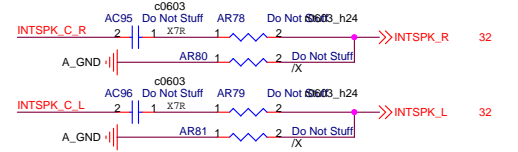
ASUS		Title 3 in 1 Card Reader	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	30	of 63



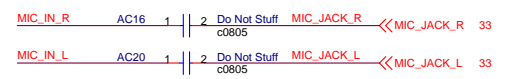
Headphone Output



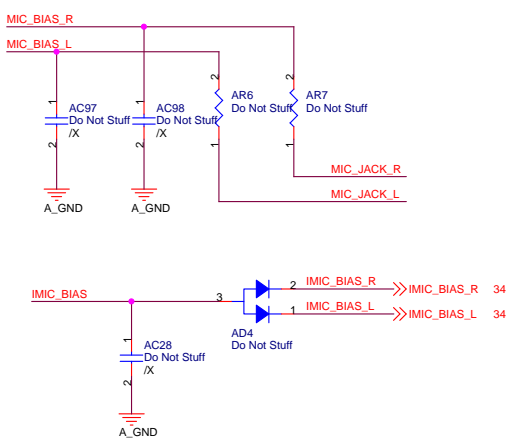
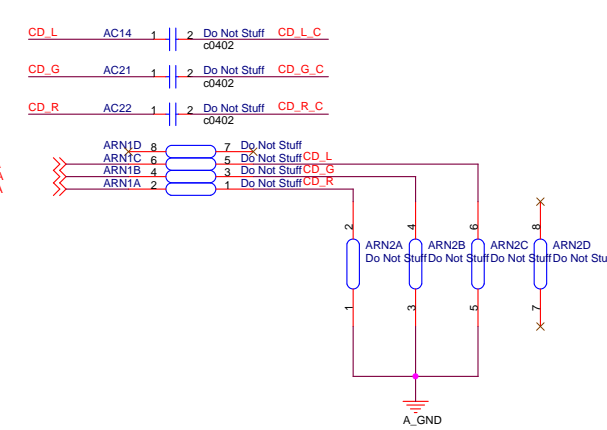
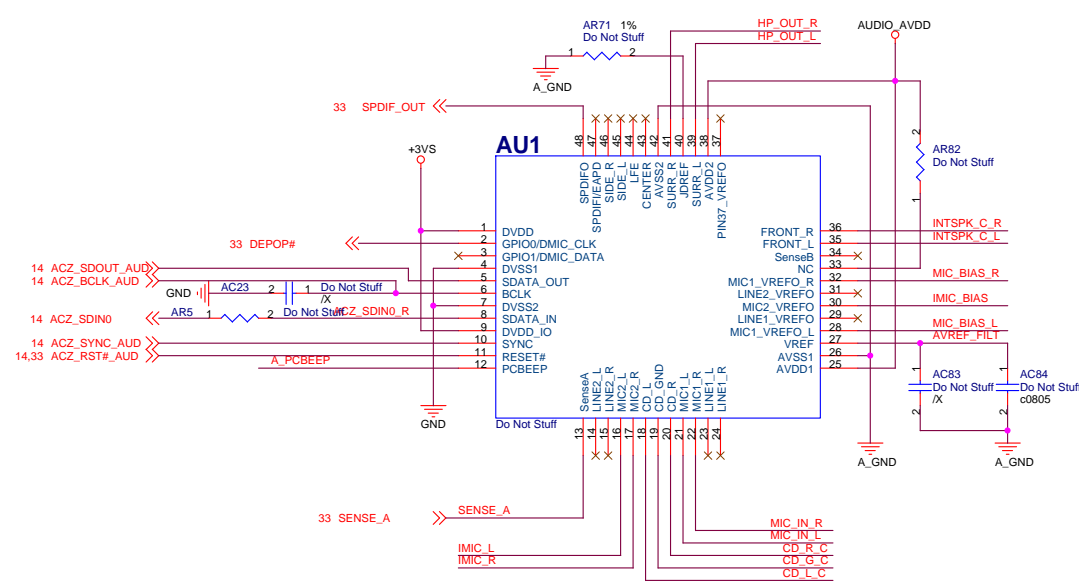
Internal MIC Input



Internal Speaker



MIC Input



02G611102200 C.S ALC883-GR LQFP-48 REALTEK AUDIO CODEC;HP ALC883

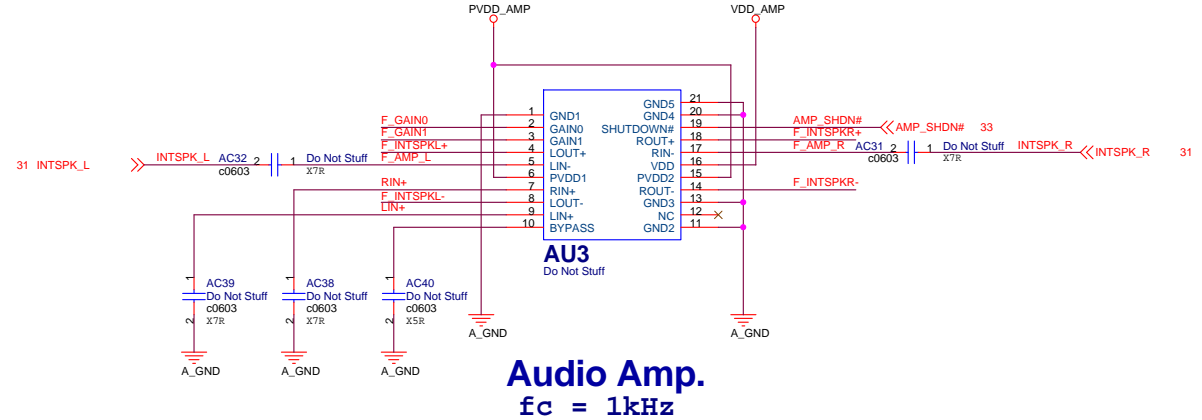
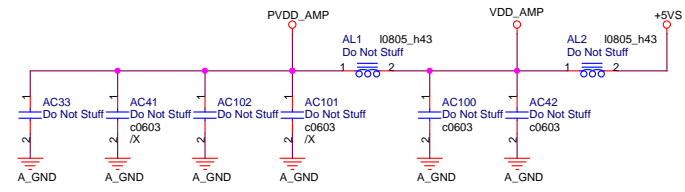
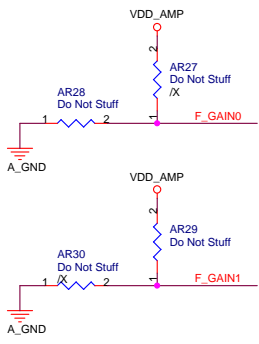
02G611001310 C.S ALC882 Rev:B1 LQFP-48 REALTEK AUDIO CODEC ALC882

02G611002910 C.S ALC888-GR A1 LQFP-48 REALTEK AUDIO CODEC ALC888_GR

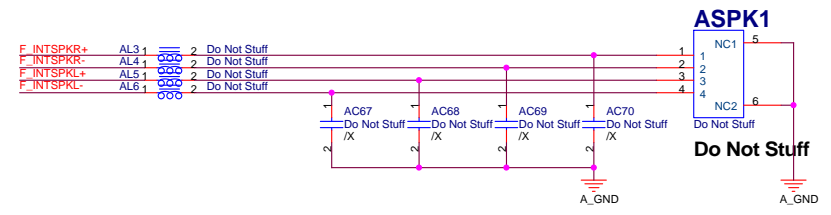
LUNCH		ASUS Title : Audio ALC882H	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	31	of 63

GAIN Control

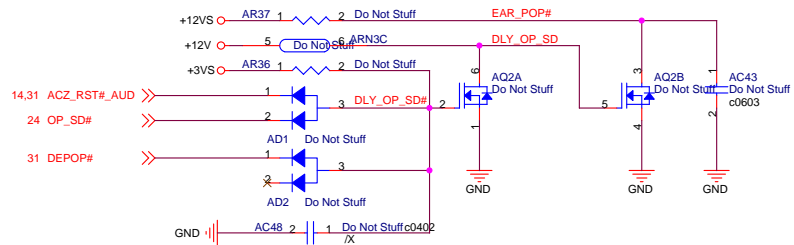
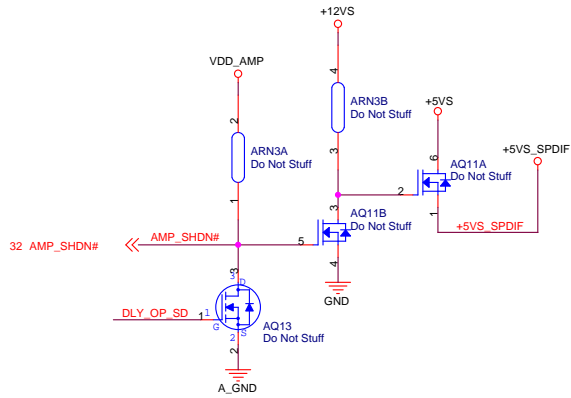
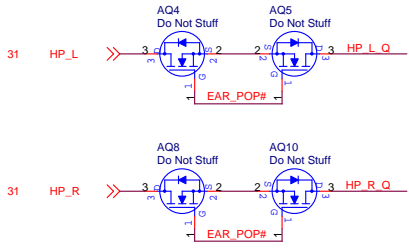
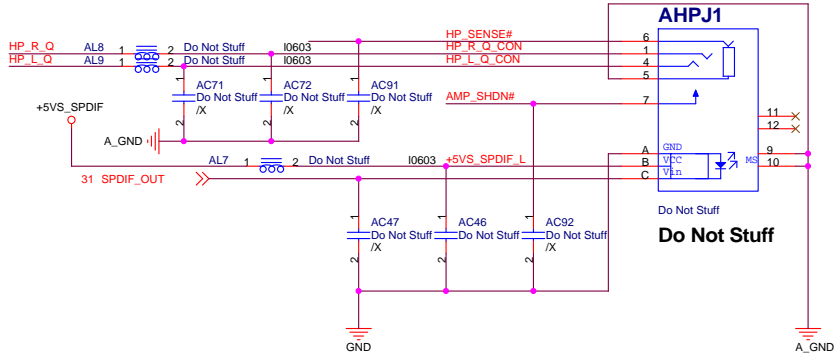
GAIN0	GAIN1	Gain
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



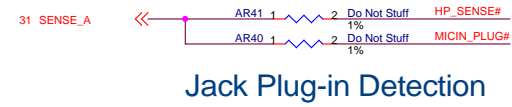
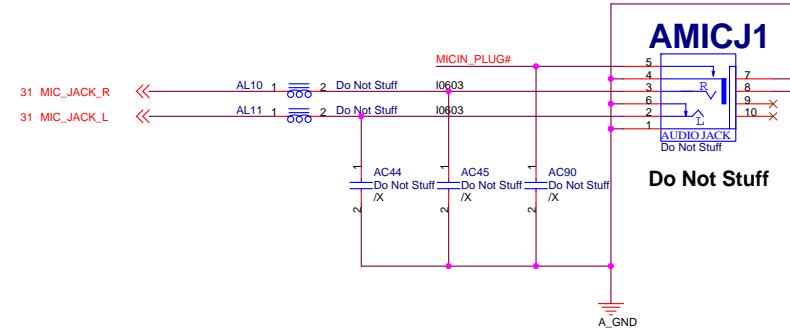
12G171000047 Internal Speaker Connector



Headphone & S/PDIF Jack



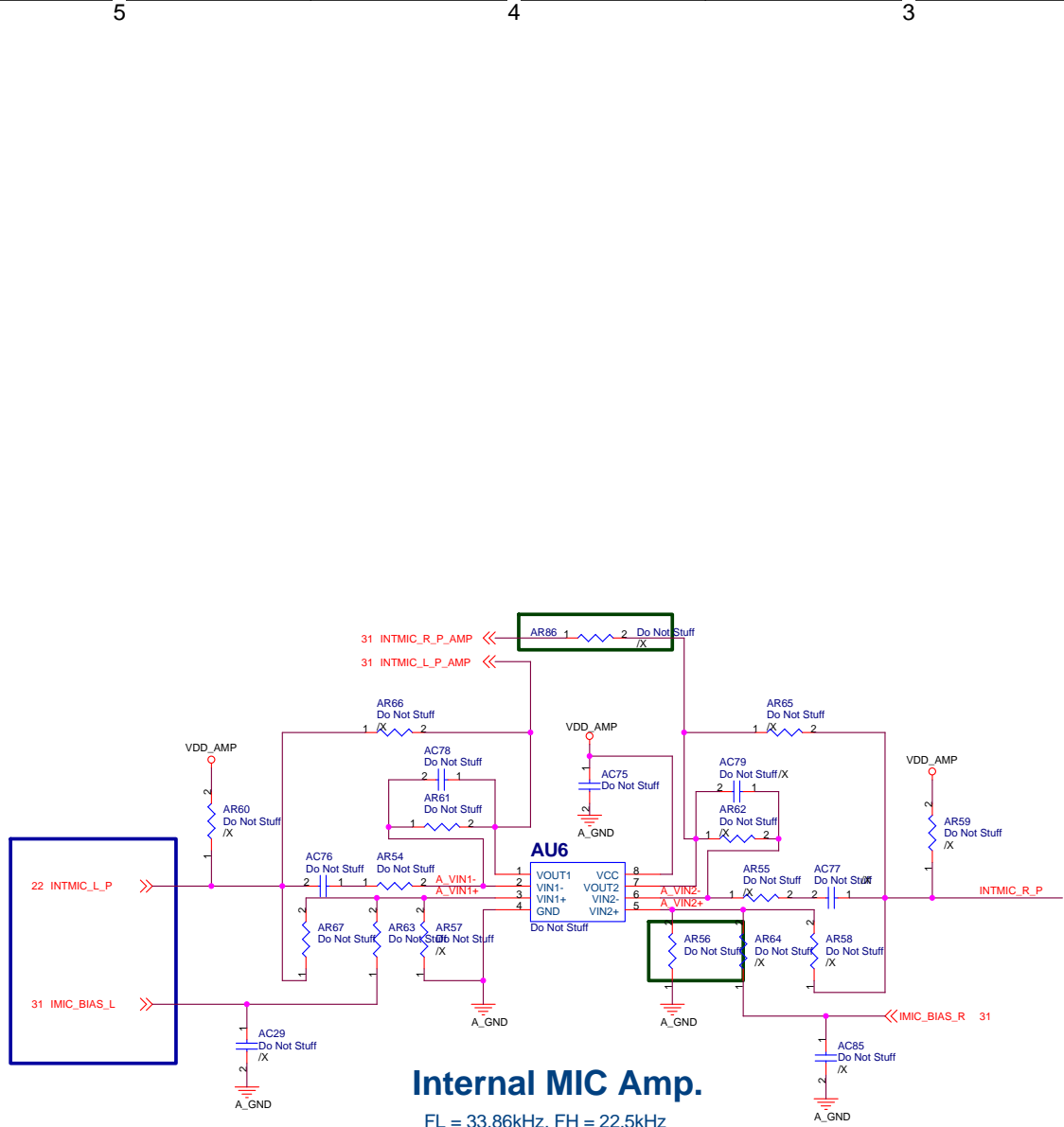
Microphone-In Jack



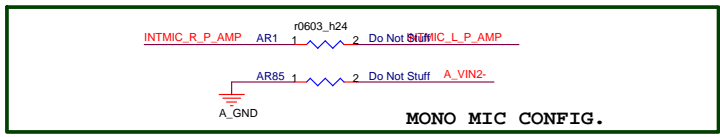
Jack Plug-in Detection

LUNCH

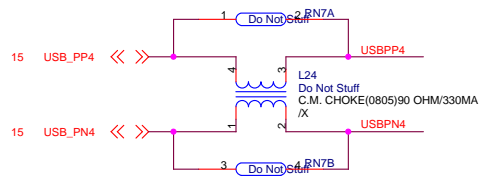
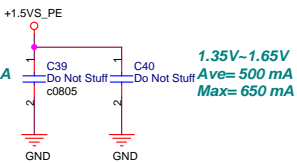
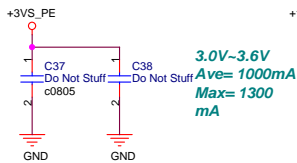
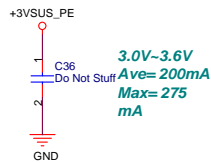
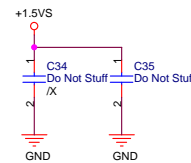
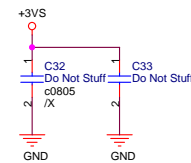
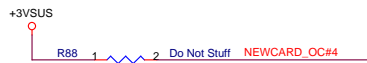
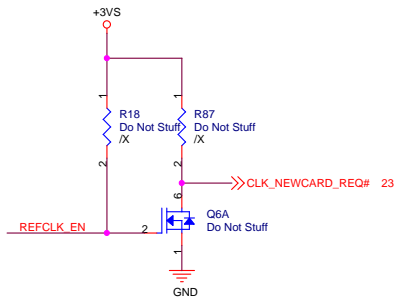
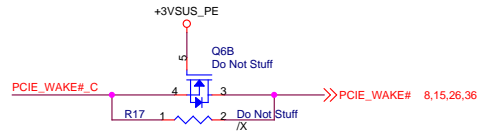
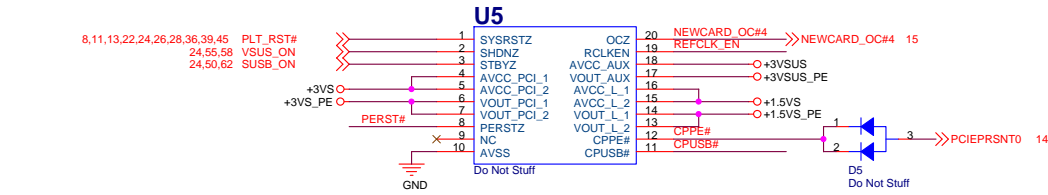
ASUS		Title : Audio JACK	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007		Sheet 33 of 63	



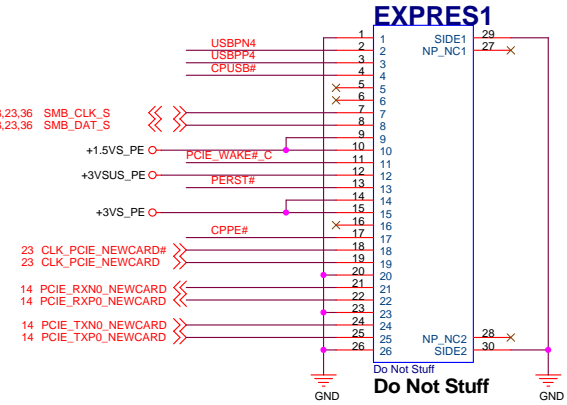
Internal MIC Amp.
 FL = 33.86kHz, FH = 22.5kHz



06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1
 06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

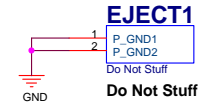


NewCard Header



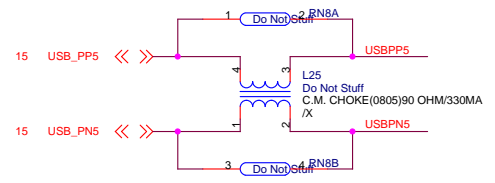
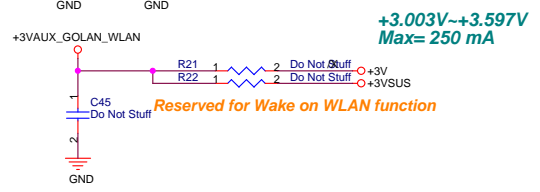
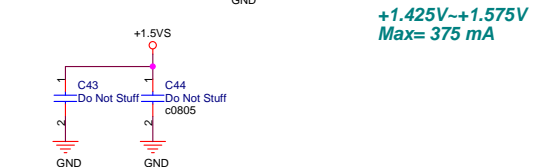
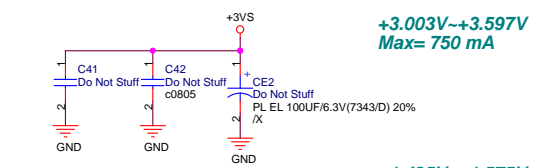
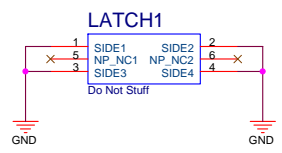
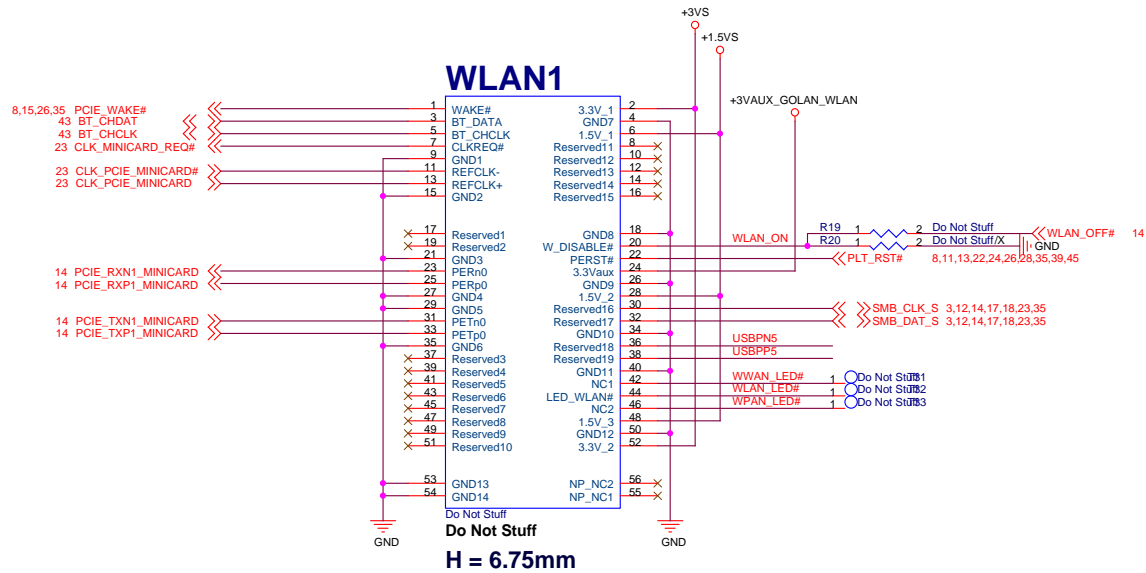
ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

NewCard Ejector

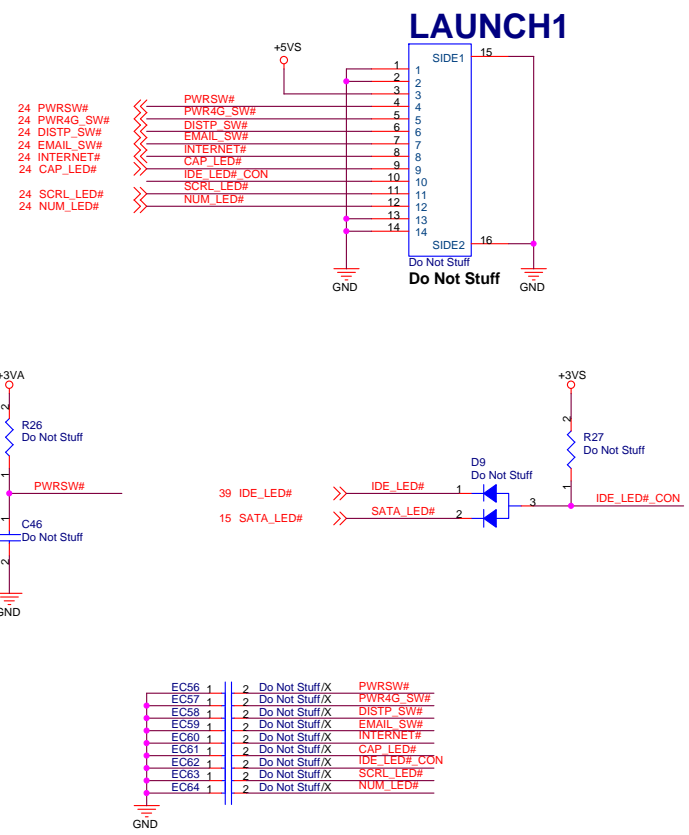


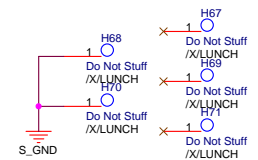
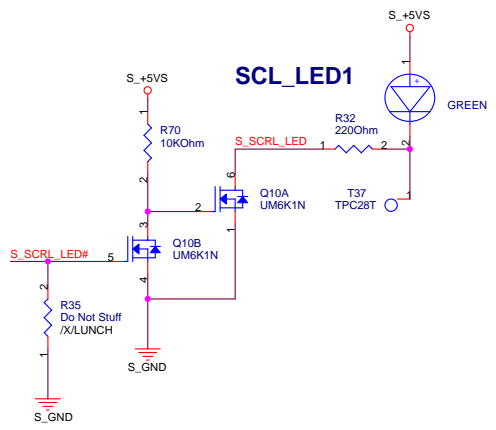
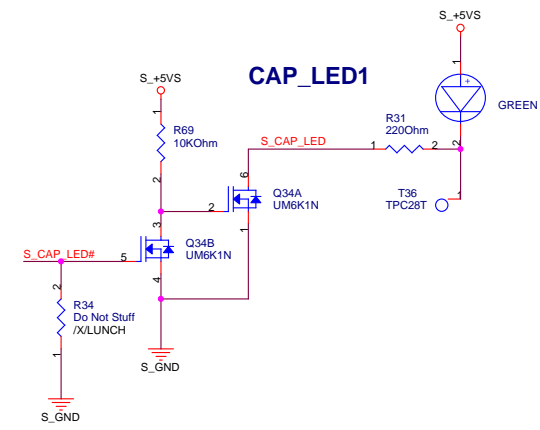
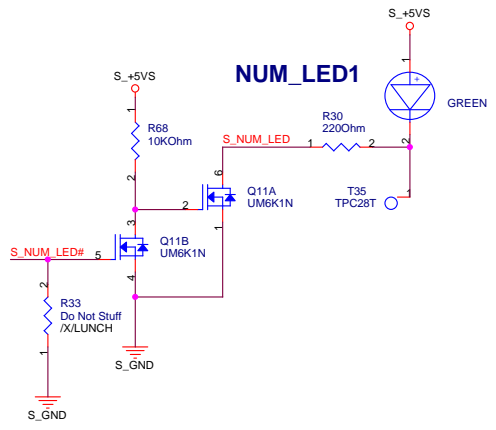
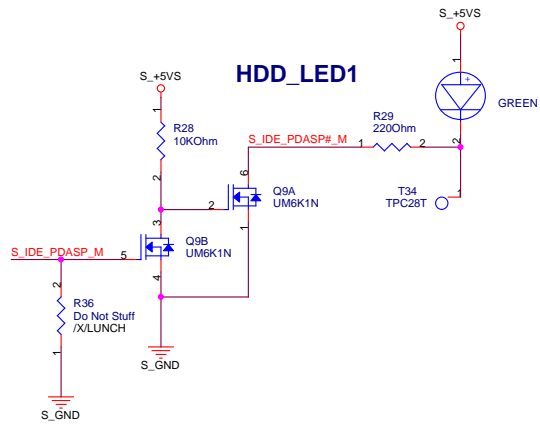
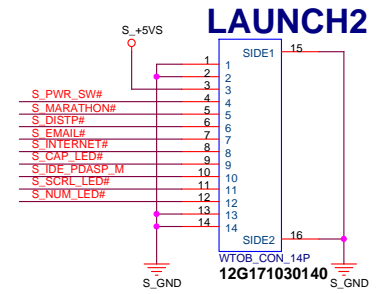
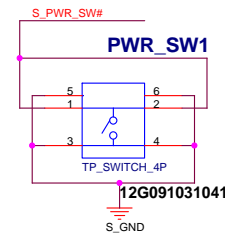
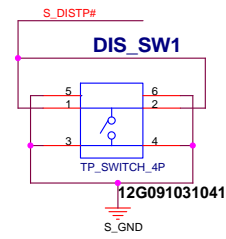
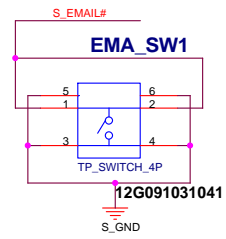
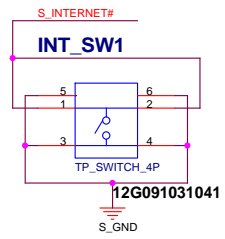
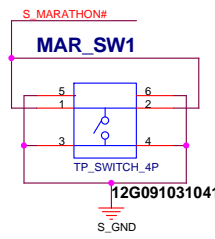
LUNCH

ASUS		Title : NEWCARD	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	35	of 63



LAUNCH BOARD Connector

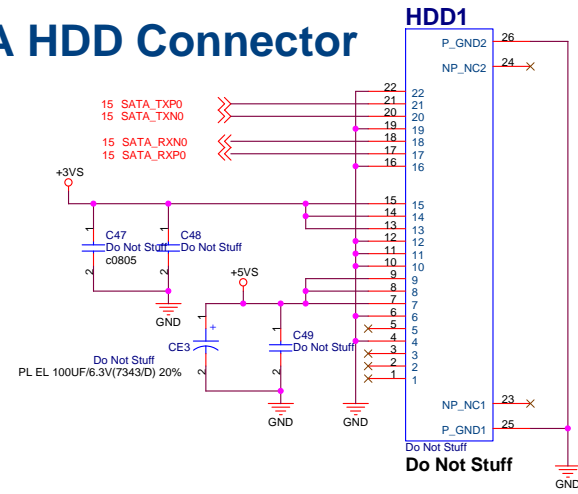




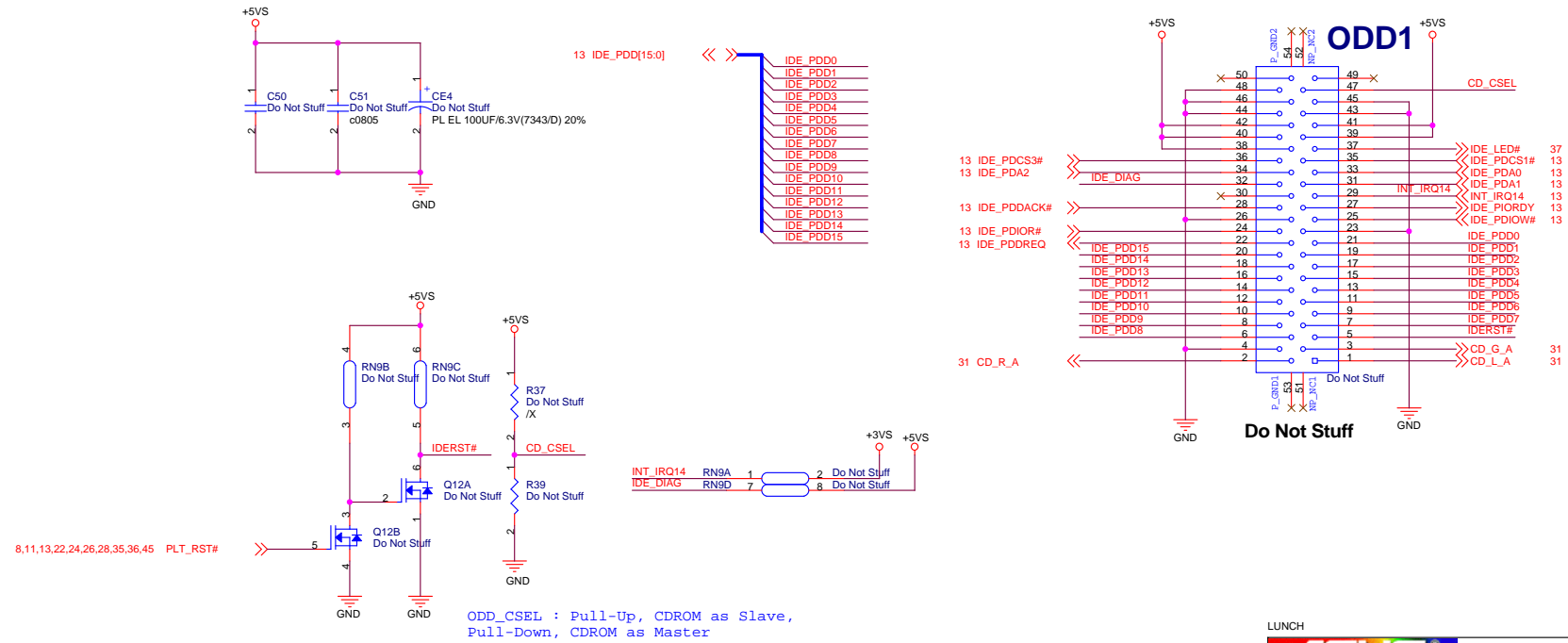
LUNCH

ASUS		Title : LAUNCH BOARD	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Monday, August 13, 2007	Sheet 38 of 63		

SATA HDD Connector



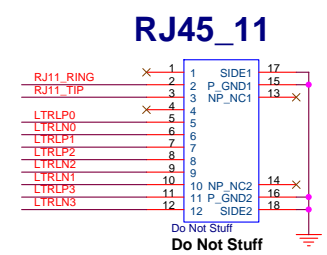
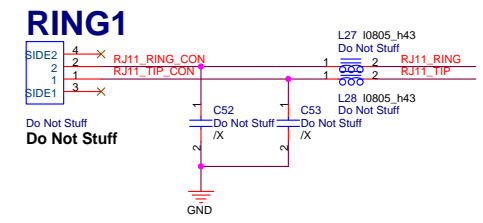
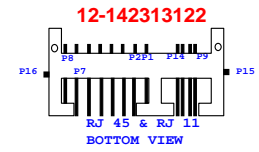
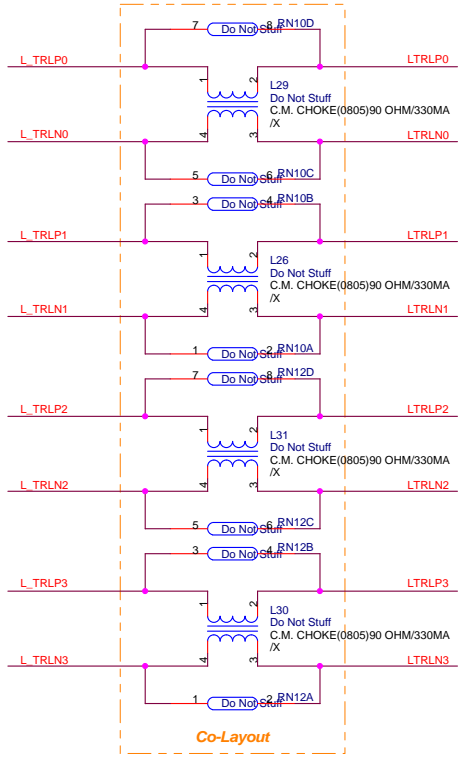
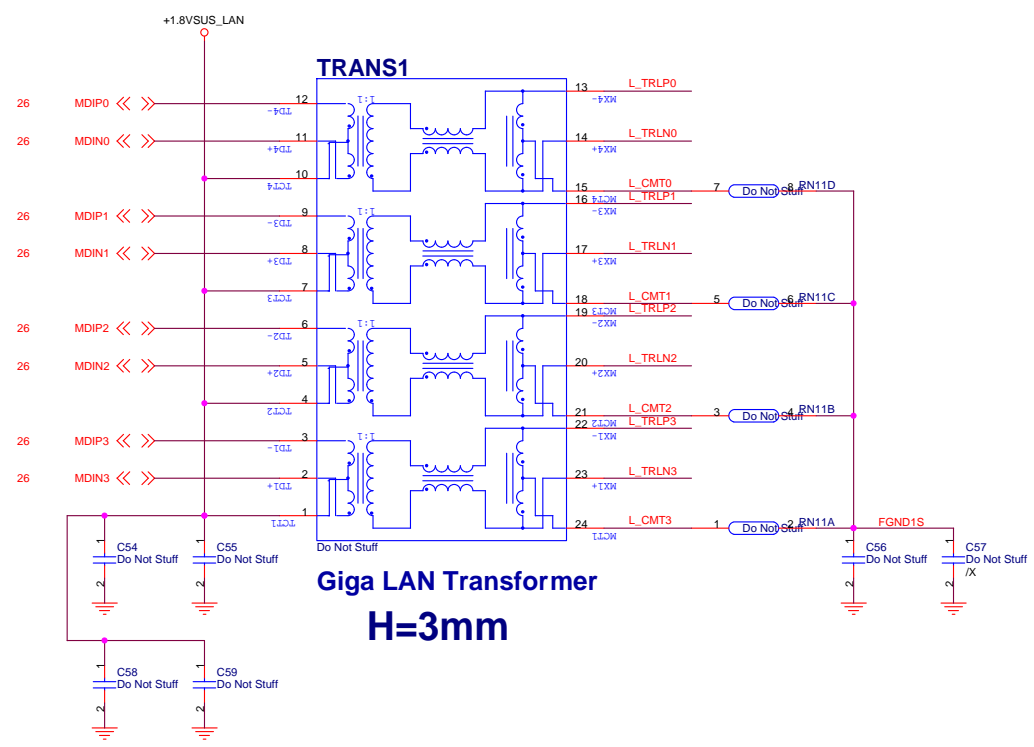
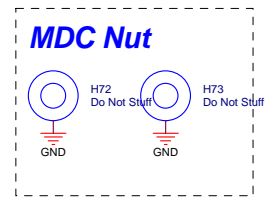
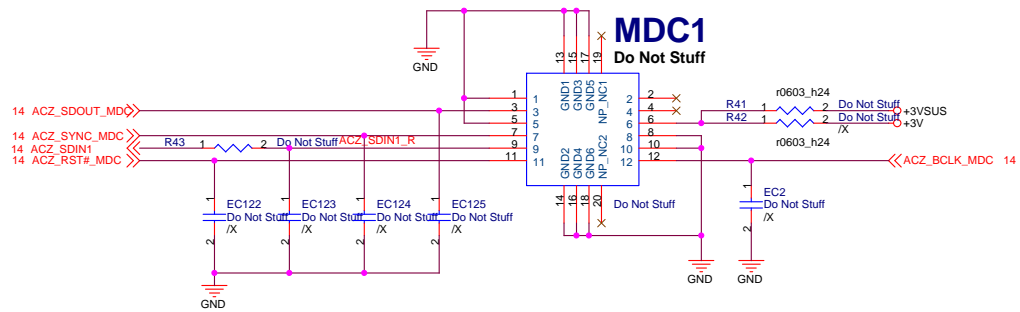
ODD Connector



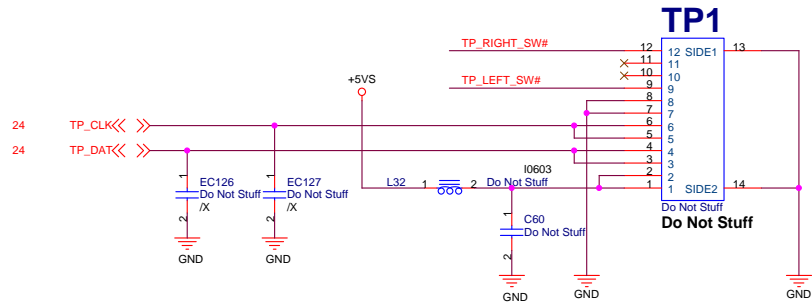
LUNCH

ASUS		Title : HDD & ODD	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007		Sheet	39 of 63

MDC Connector



TouchPad Connector

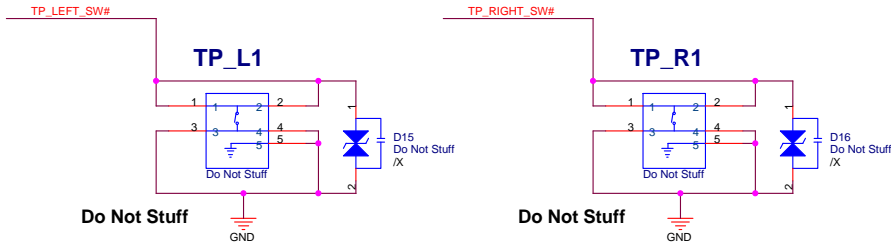
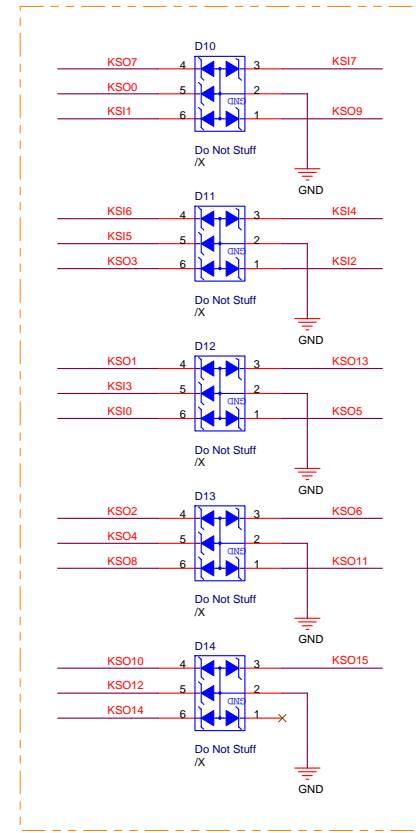
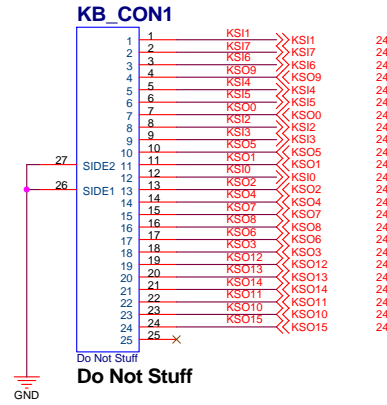


Touch pad Definition

1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

Z62F: pin1 reversal

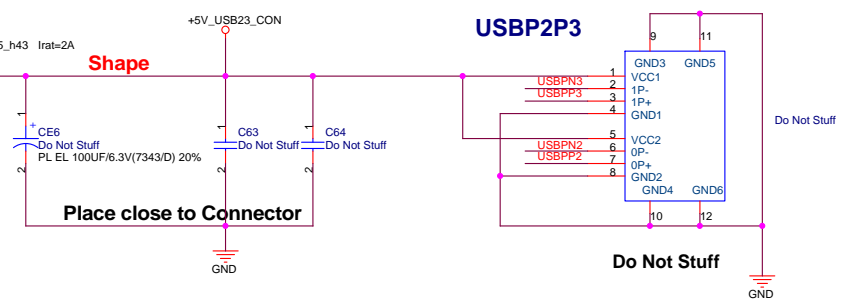
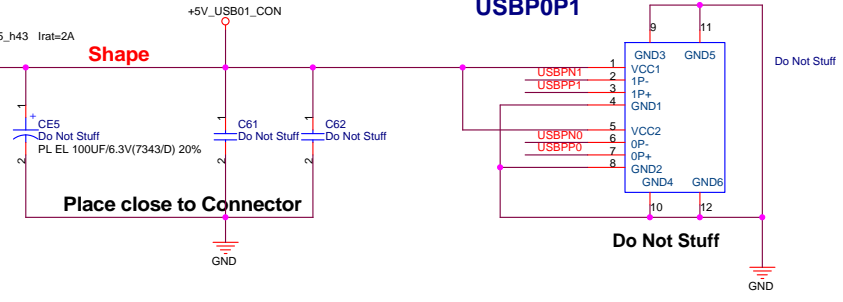
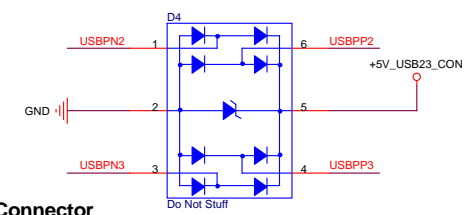
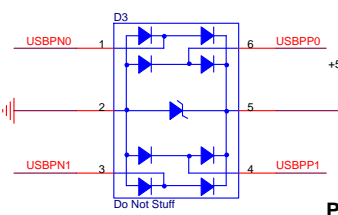
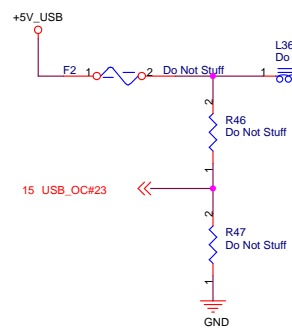
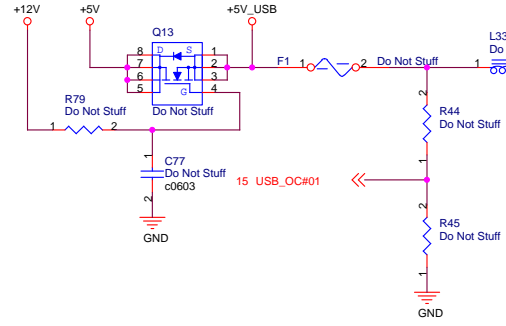
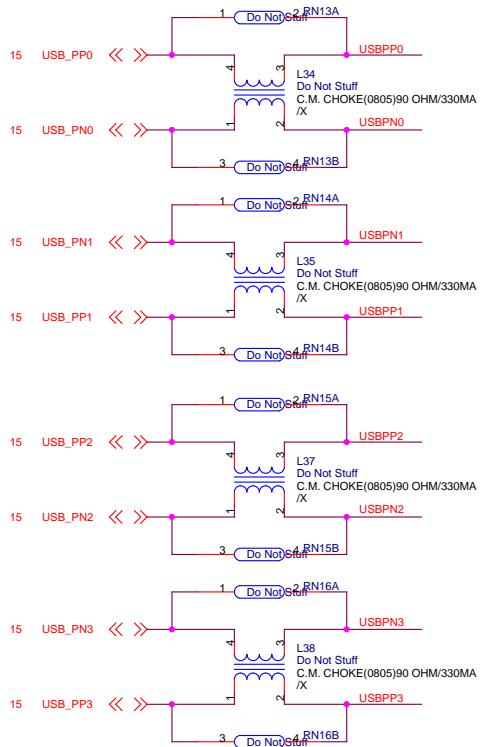
Keyboard Connector



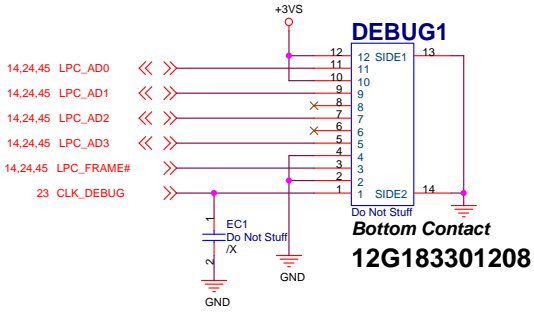
TOUCH PAD SWITCH

LUNCH

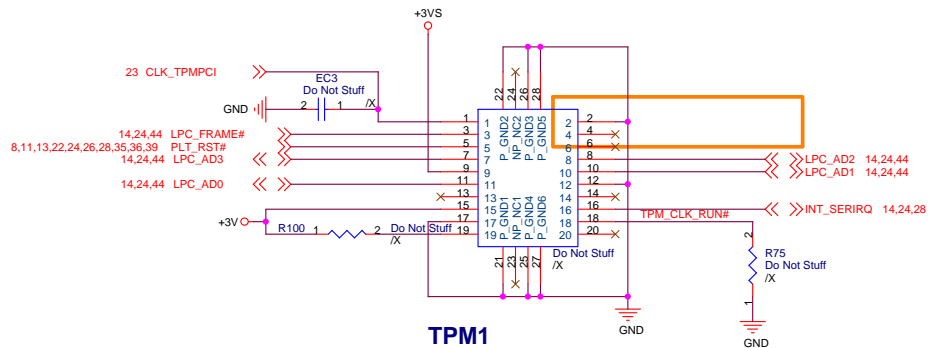
USB Power & OC Alert



Debug Connector

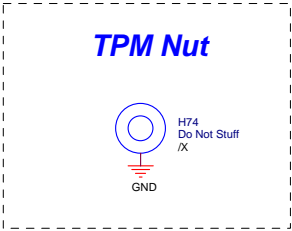


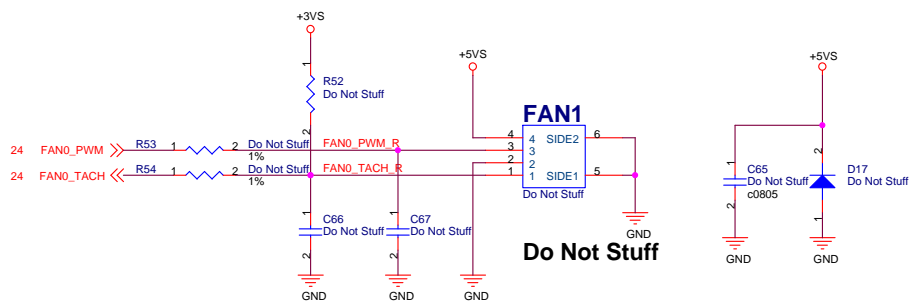
TPM Connector



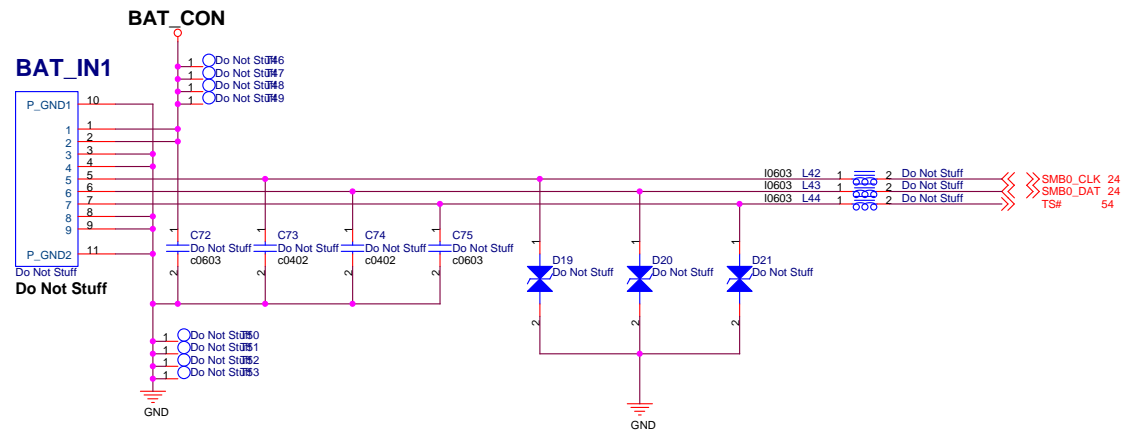
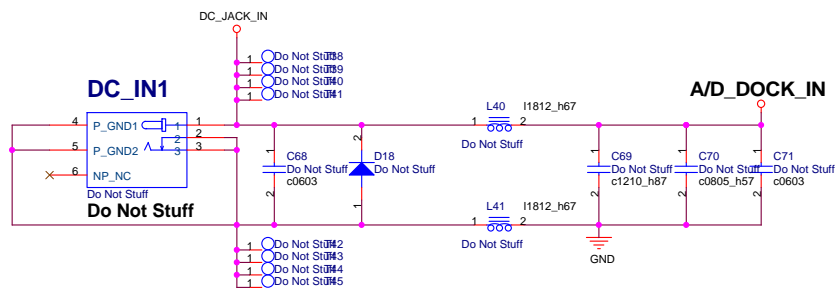
TPM1
12G16080020J

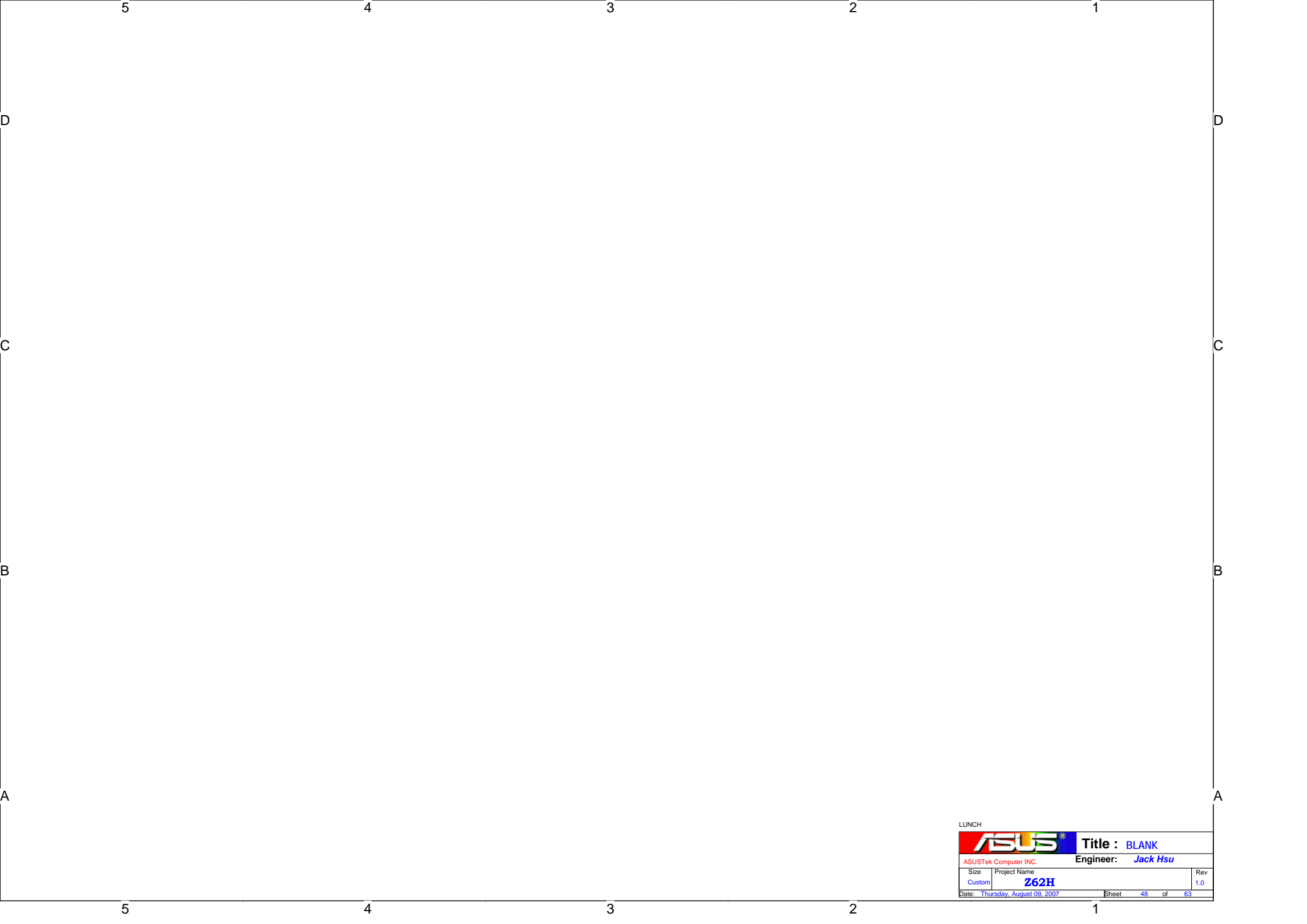
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
Removed!!





SYSTEM Fan Connector

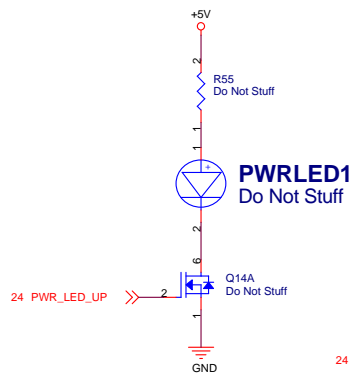




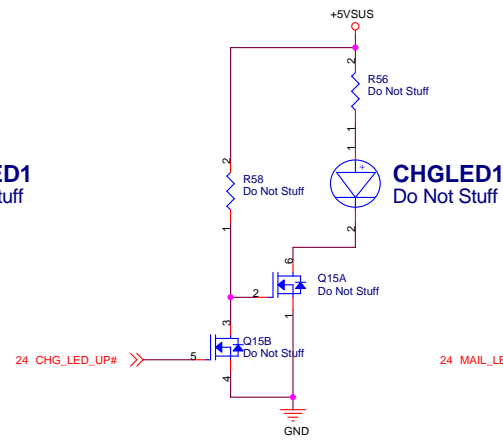
LUNCH

		Title : BLANK
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	Z62H	1.0
Date: Thursday, August 09, 2007	Sheet 48 of 63	

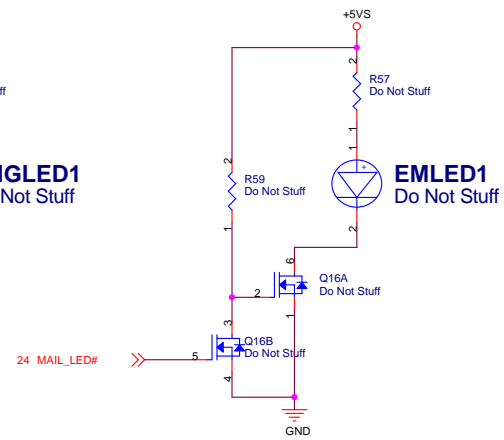
POWER LED



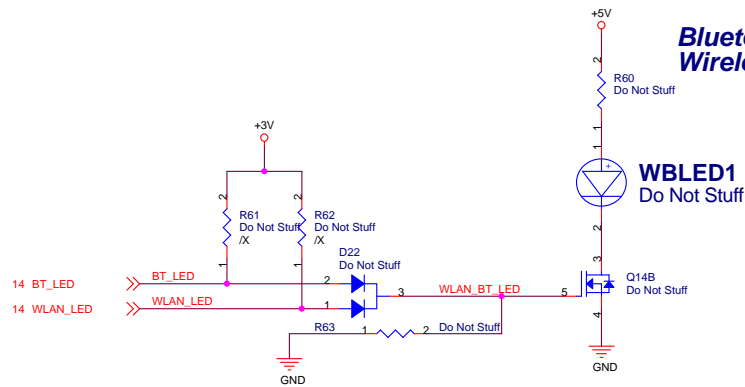
Battery Charge LED



Email LED

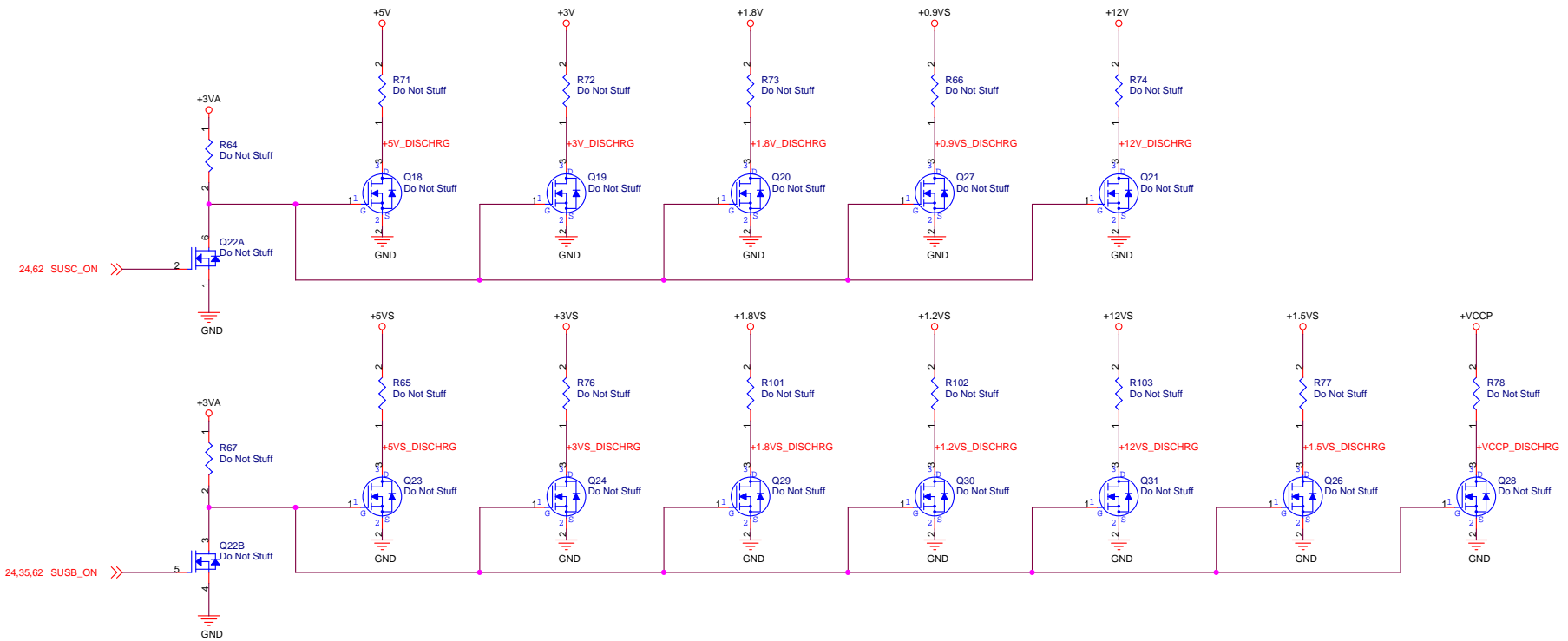


**Bluetooth LED
Wireless LED**



LUNCH

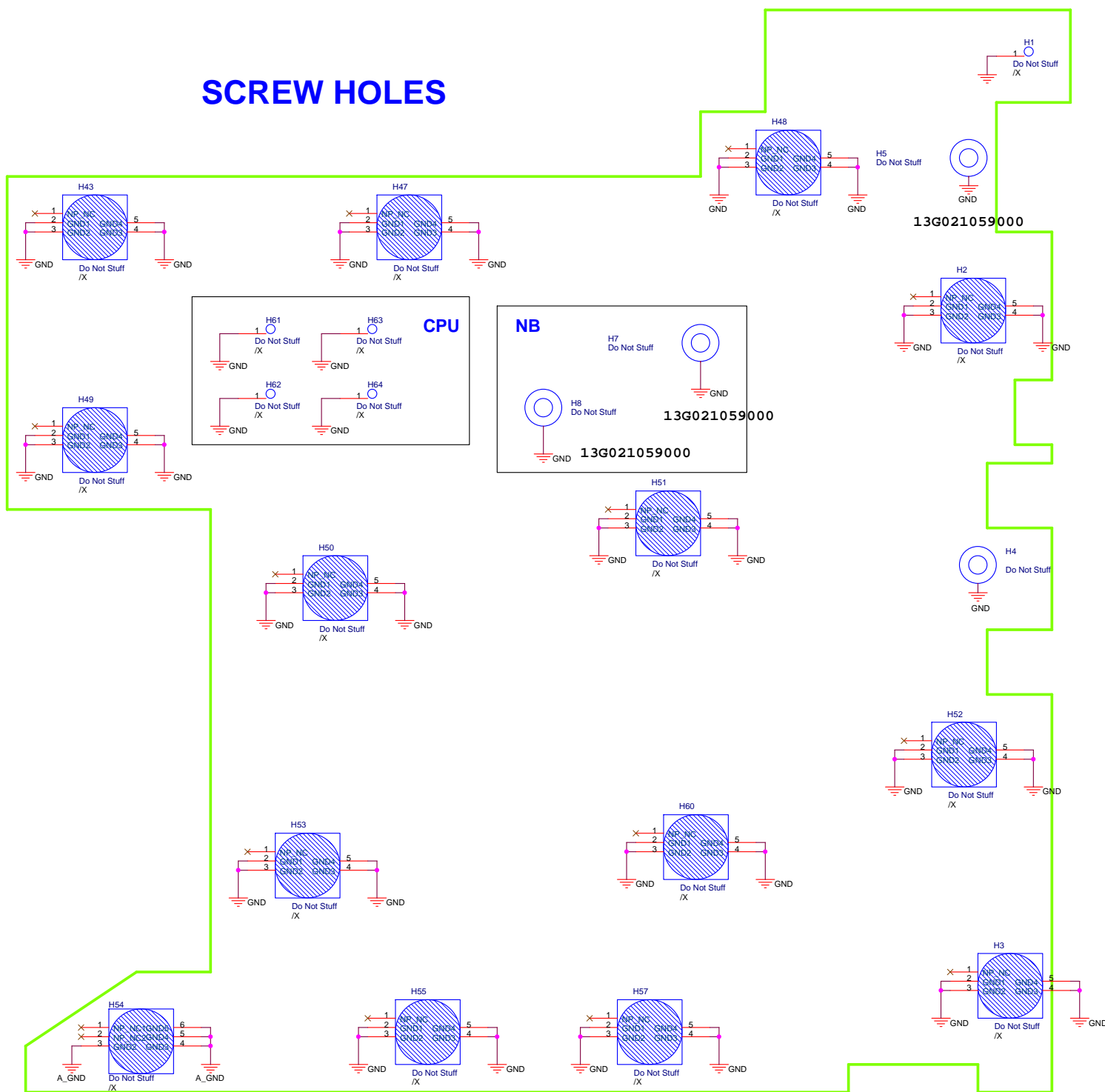
		Title : LED
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	Z62H	1.0
Date: Thursday, August 09, 2007		Sheet 49 of 63



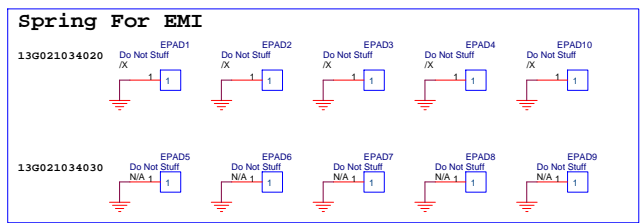
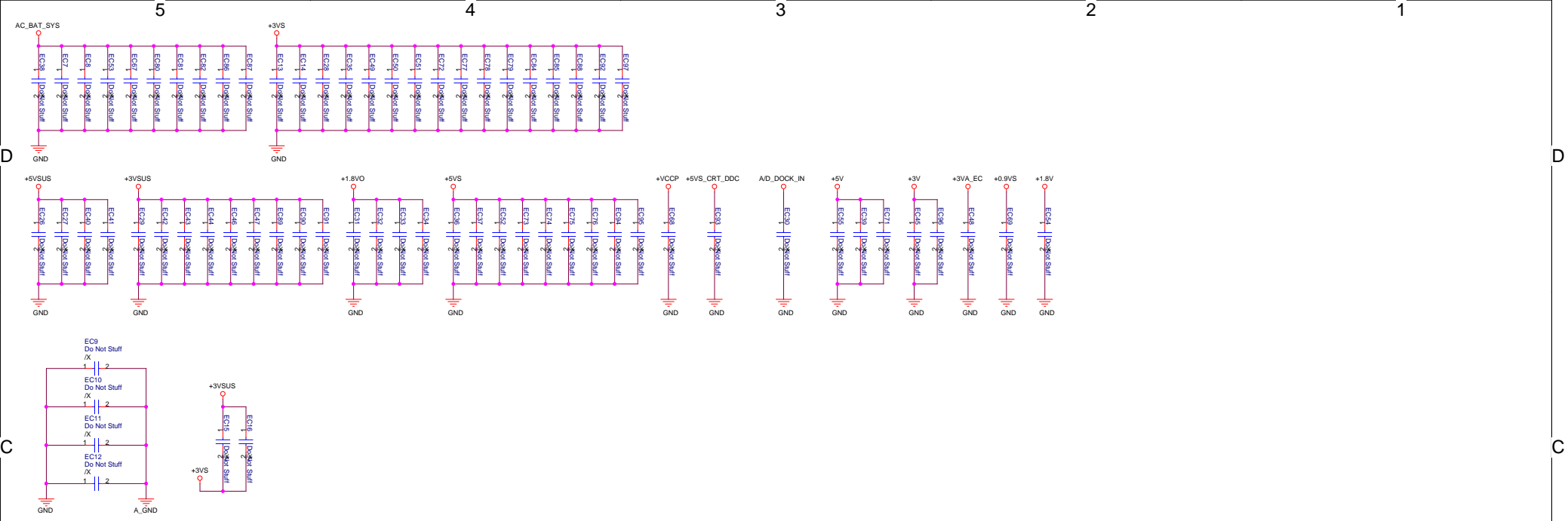
LUNCH

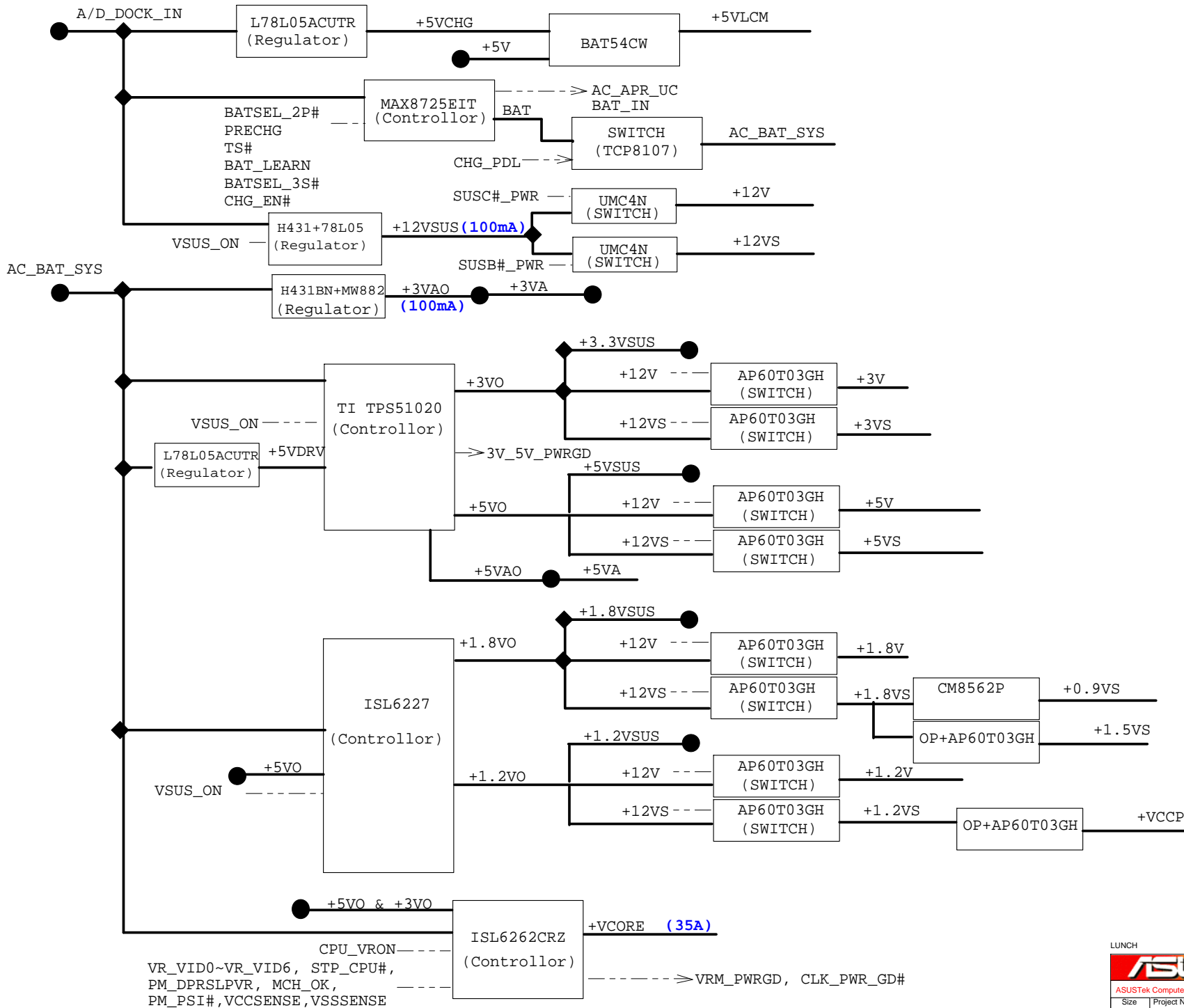
		Title : Discharger	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	50	of 63

SCREW HOLES



LUNCH		ASUS Title : Screw Hole	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
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Setting the Adapter Input Current Limit
 Adapter I_{in}(max) = [0.075V/R_{sense}(ADin)] * [V_{CLS}/V_{REF}]
 V_{CLS} = 2.865V
Adaptor Max. Current :
 PR5708=20K PR5714 = 178K; I_{limit} = 4.5A; 81W
 PR5708=27K PR5714 = 47K; I_{limit} = 3.175A; 60W

Setting the Charge Voltage
 V_{batt} = Cell * (V_{ref} + (V_{CTL} - 1.8V) / 9.52)
 V_{CTL} = 1.588V => V_{batt} = 4.2V

Setting the Charge Current
 Charge Current I_{chg} = [0.075V/R_{sense}(CHG)] * [V_{CTL}/3.6V]
 R_{sense}(CHG) = 15m Ohm
Pre-Charging Mode :
 Precharging current = 148 - 152mA
 V_{ctl} = 0.107V - 0.109V
Battery Cell Selection :
 BATSEL_2P# = 1, 3 Cells; V_{ctl} = 2.084V
 => I_{charge} = 1.6933A
 BATSEL_2P# = 0, 6 or 9 Cells; V_{ctl} = 2.111V
 => I_{charge} = 2.9329A
 PR5709=120K PR5715 = 120K; I_{charge} = 2.9329A

Mode pin : V_{mode} > 2.8V (try to LDO pin) ----> 4 Cells
 2.0 > V_{mode} > 1.6V (floating) ----> 3 Cells
 0.8 > V_{mode} (try to GND) ----> Learning mode
 V_{CTL} < 0.8V or DCIN < 7V --> Charger Disable

MAX8725_REF : 4.2235V
 MAX8725_LDO : 5.4V

24 BATSEL_2P#
 BATSEL_2P# = 1, 3 Cells
 BATSEL_2P# = 0, 6 or 9 Cells

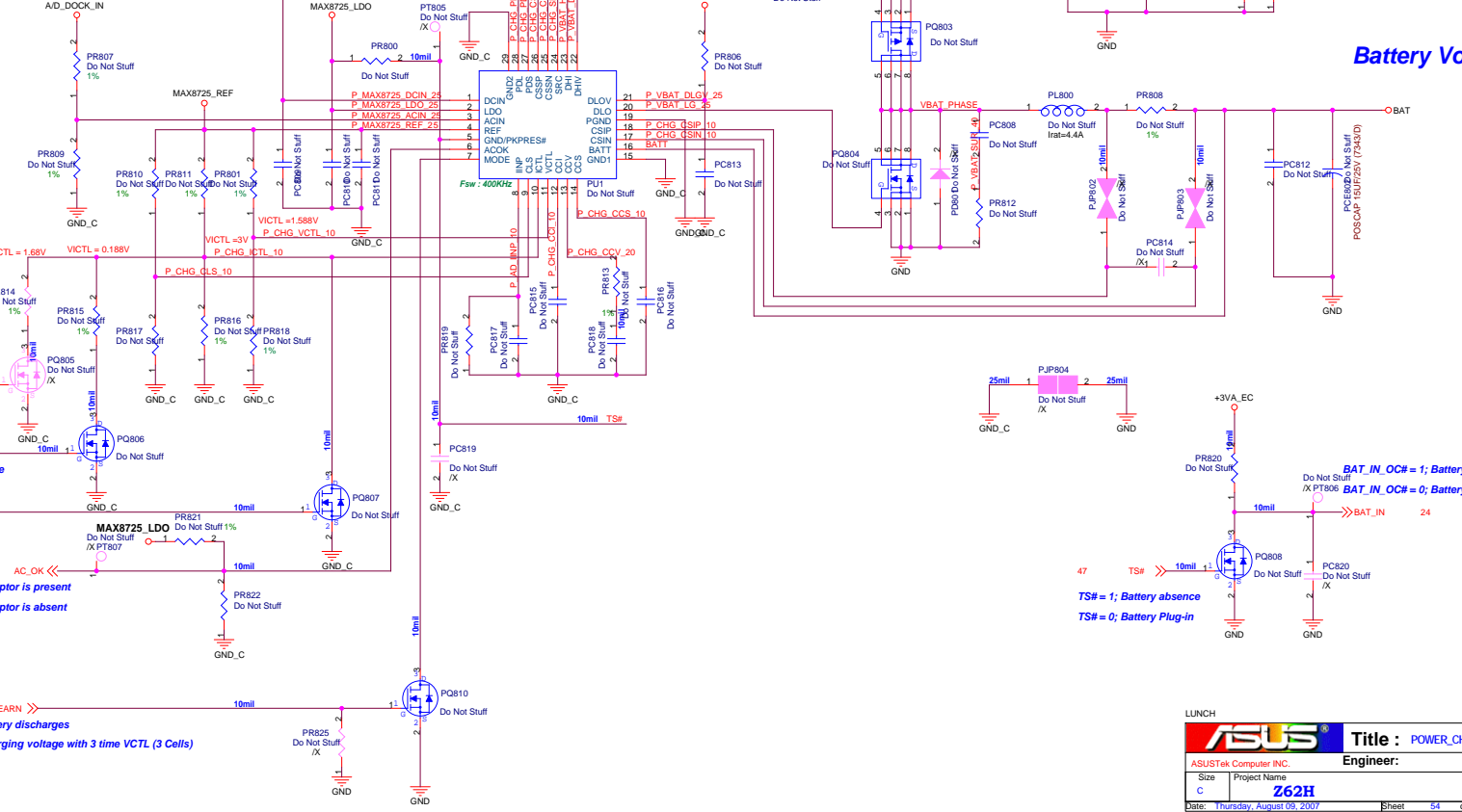
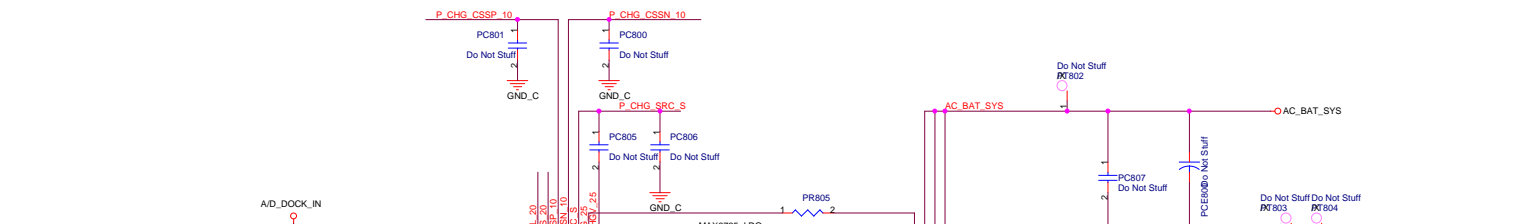
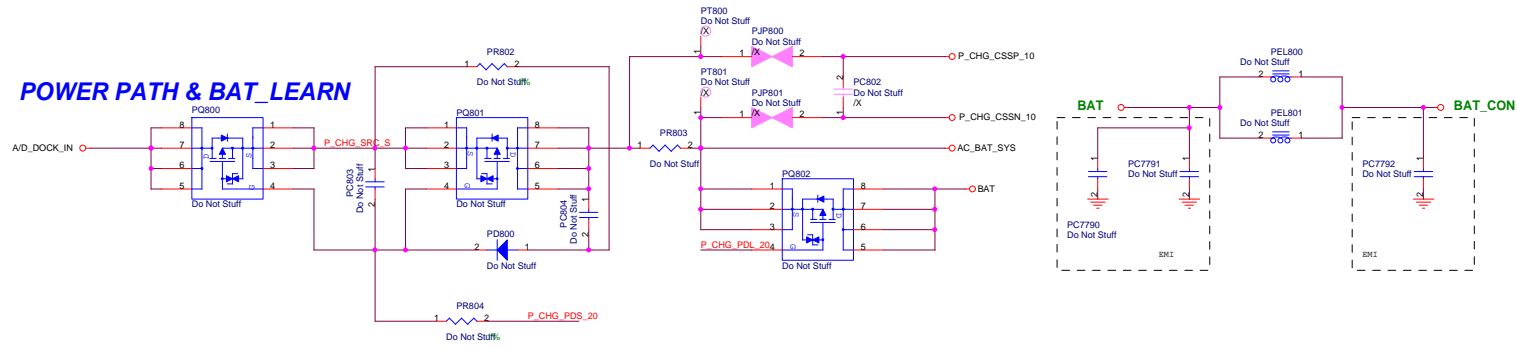
24 PRECHG
 PRECHG = 1, Pre-Charging Mode
 Charging Current = 156mA

24 CHG_EN#
 CHG_EN# = 1, Charger Disabled
 CHG_EN# = 0, Charger Enabled

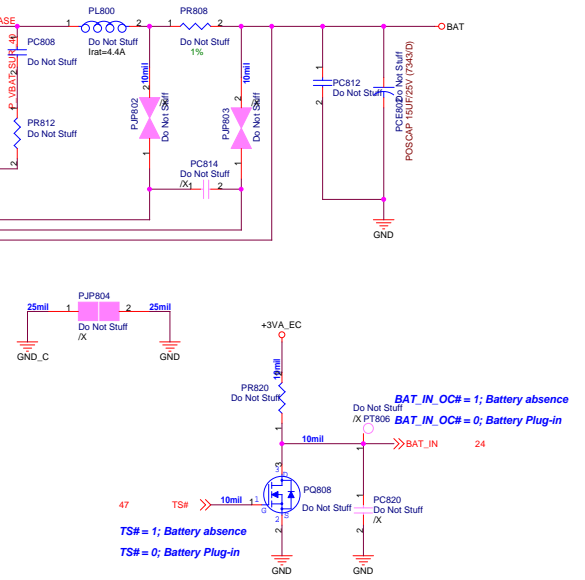
24 AC_OK
 AC_OK = 1, Adaptor is present
 AC_OK = 0, Adaptor is absent

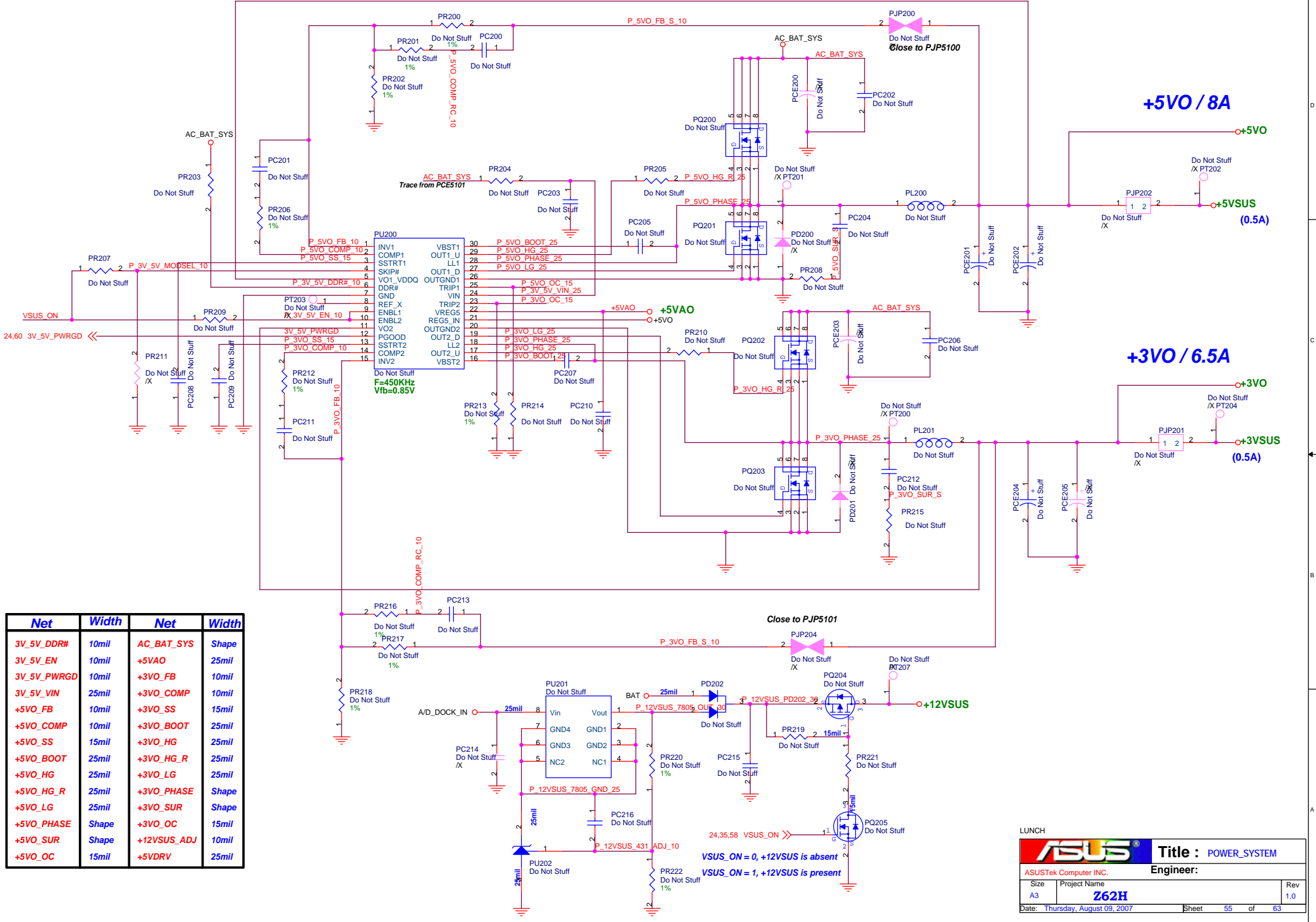
24 BAT_LEARN
 BAT_LEARN = 1, Battery discharges
 BAT_LEARN = 0, charging voltage with 3 time V_{CTL} (3 Cells)

POWER PATH & BAT LEARN



Battery Voltage





Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5V0_FB	10mil	+3VO_SS	15mil
+5V0_COMP	10mil	+3VO_BOOT	25mil
+5V0_SS	15mil	+3VO_HG	25mil
+5V0_BOOT	25mil	+3VO_HG_R	25mil
+5V0_HG	25mil	+3VO_LG	25mil
+5V0_HG_R	25mil	+3VO_PHASE	Shape
+5V0_LG	25mil	+3VO_OC	15mil
+5V0_PHASE	Shape	+3VO_SUR	Shape
+5V0_SUR	Shape	+12VSUS_ADJ	10mil
+5V0_OC	15mil	+5VDRV	25mil

LUNCH

ASUS		Title : POWER_SYSTEM	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
A3	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	55	of 63

24 CPU_VRON >>> CPU_VRON = 1, Vcore Regulator Enabled
 PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
 14.27 PM_DPRSLPVR

3.14,27 H_DPRSTP# >>> STP_CPU# = 0, CPU is in Deeper Sleep Mode
 14.23,27 STP_CPU#

23 CLK_EN# <<< CLK_EN# = 0, Enable Clock Gen
 To Clock Gen

VRM_PWRGD <<< VRM_PWRGD = 1, Vcore Power OK
 To N/B

PS# = 0, Light Load (1-phase)
 From CPU

24 P_MON_10 <<< P_MON_10

4 VCCSENSE >>> From CPU; for CPU remote sense

2.00 <<< VSSSENSE >>> From CPU; for CPU remote sense

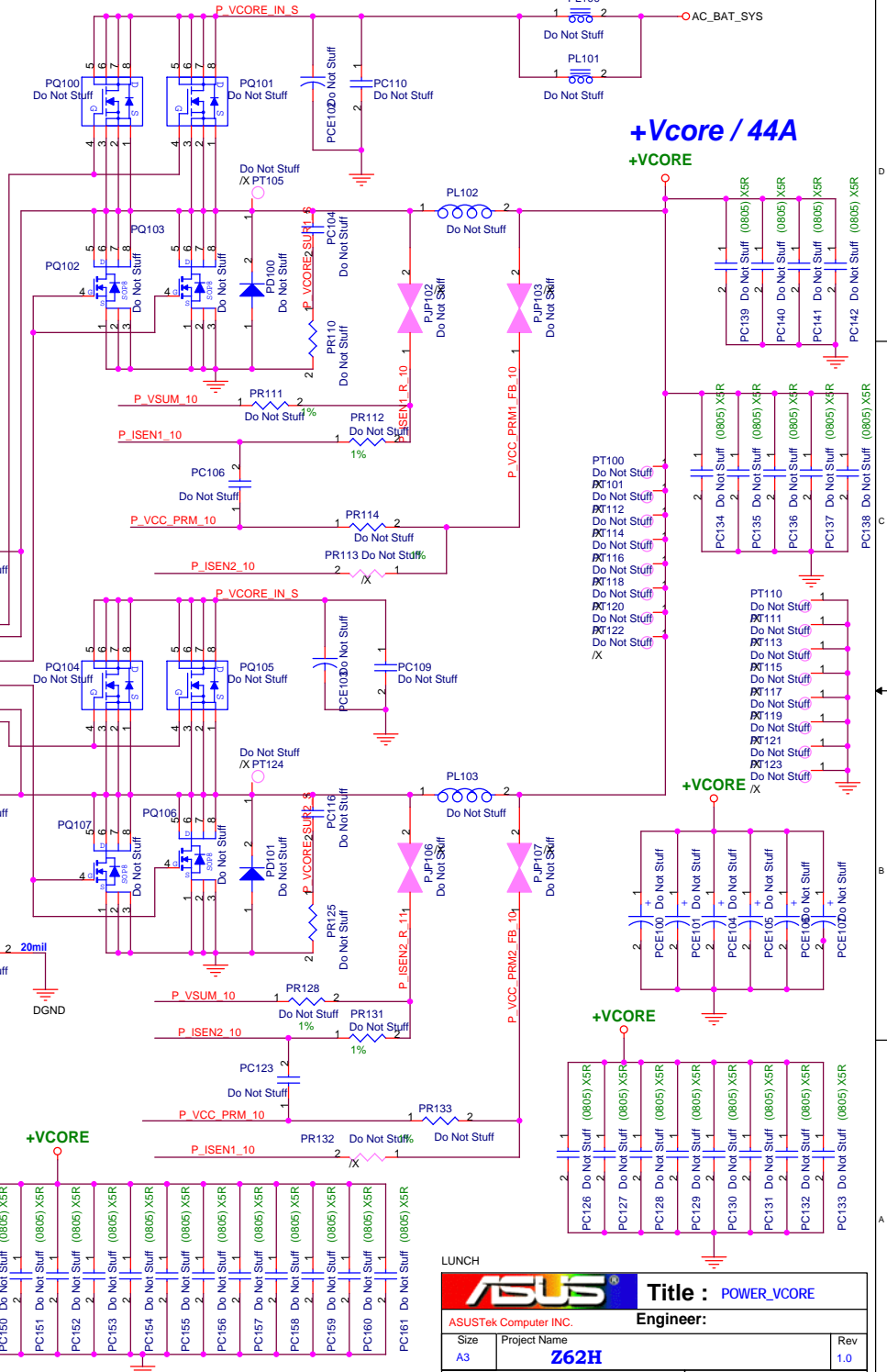
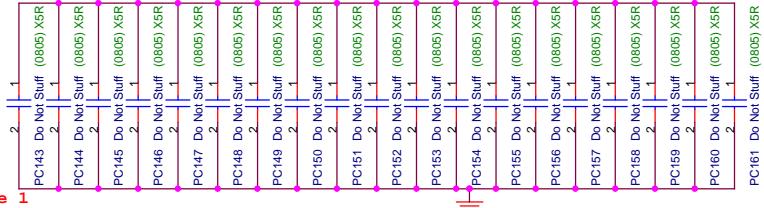
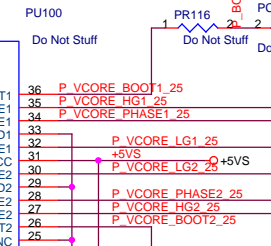
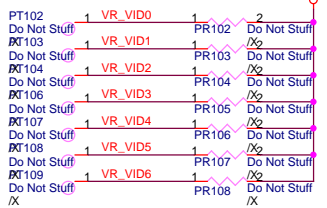
Put PJP110 & PJP112 close to CPU

V1.01

SEL0	SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

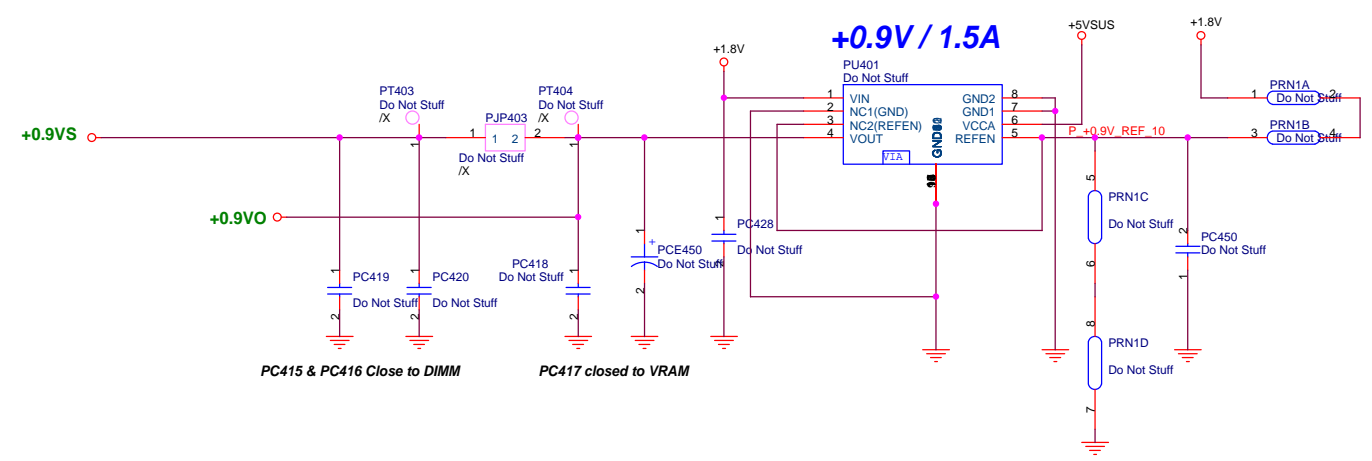
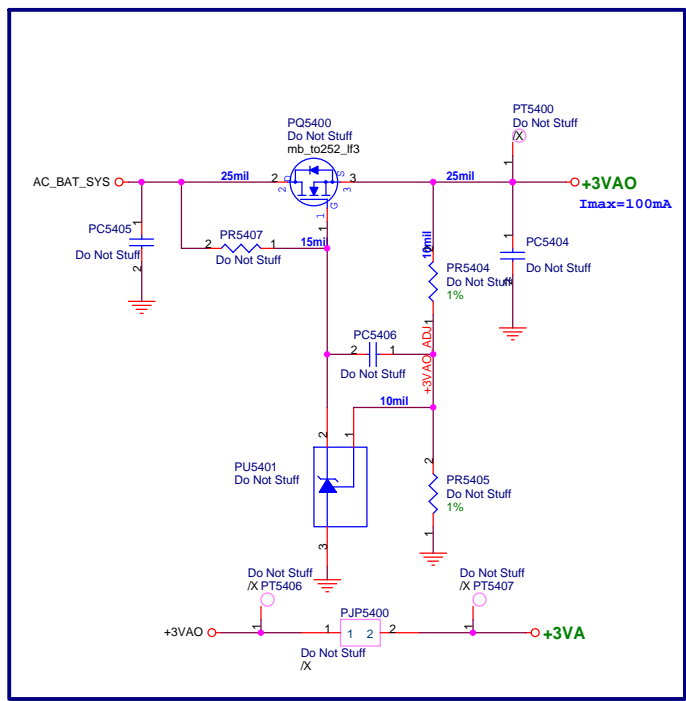
PC162 & PC163 for Transient Response

Close to Phase 1 Inductor



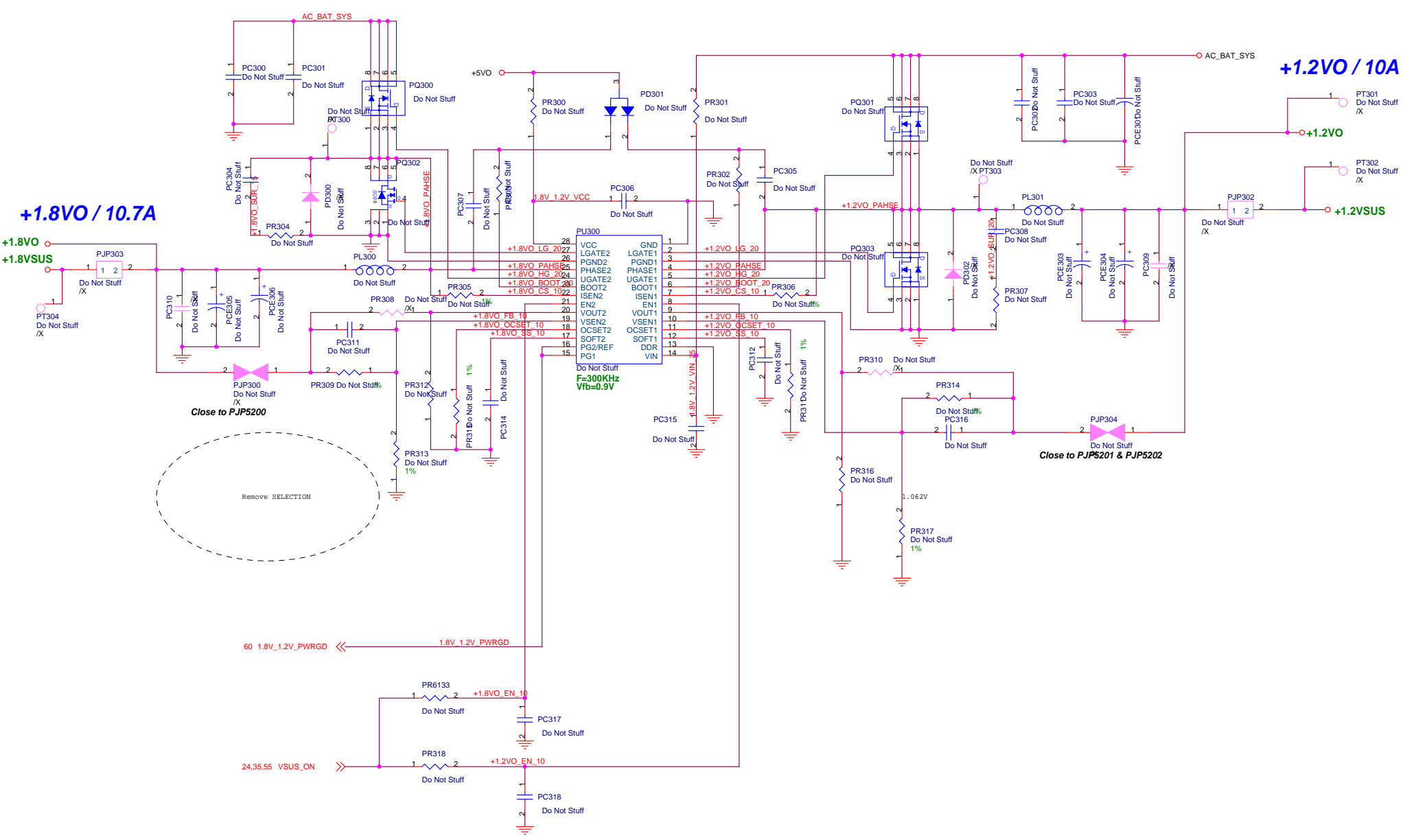
LUNCH

Title : POWER_VCORE
 ASUSTek Computer INC. **Engineer:**
 Size A3 Project Name **262H**
 Date: Thursday, August 09, 2007 Sheet 56 of 63



DDR Power Rev:1.00
LUNCH

ASUS		Title :	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
A3			1.0
Date: Thursday, August 09, 2007			Sheet 57 of 63



+1.8VO / 10.7A

+1.2VO / 10A

+1.8VO
+1.8VSUS

+1.2VO

+1.2VSUS

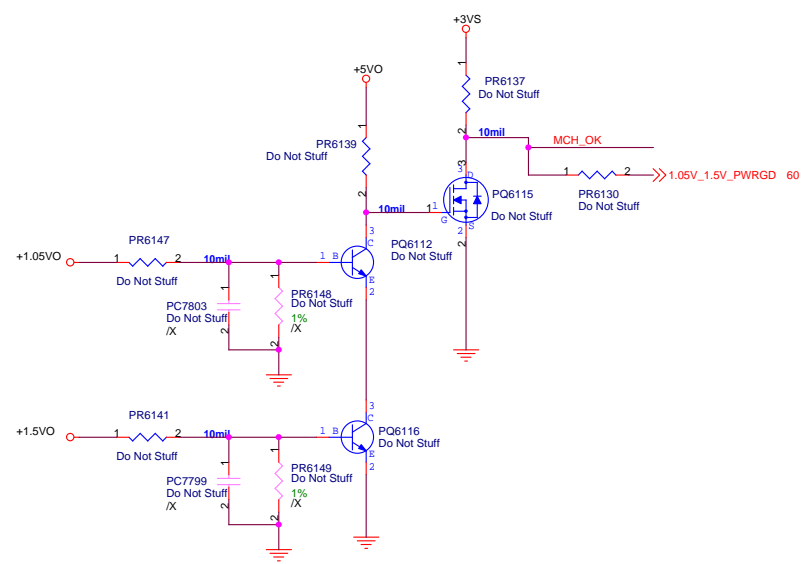
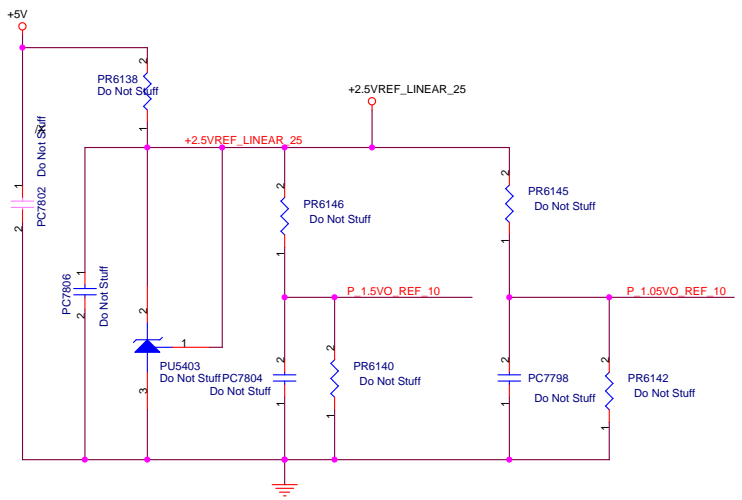
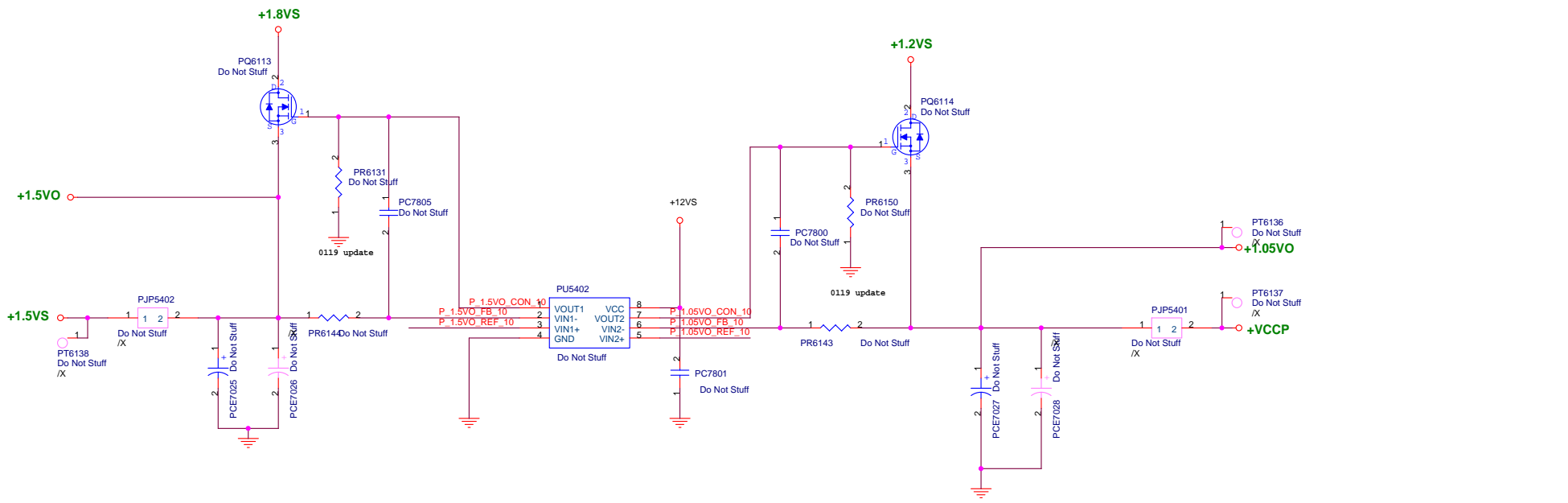
Remove SELECTION

Close to PJP5200

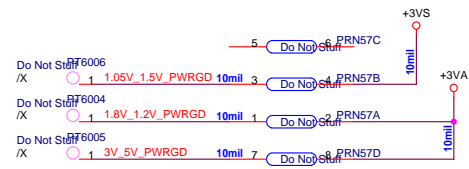
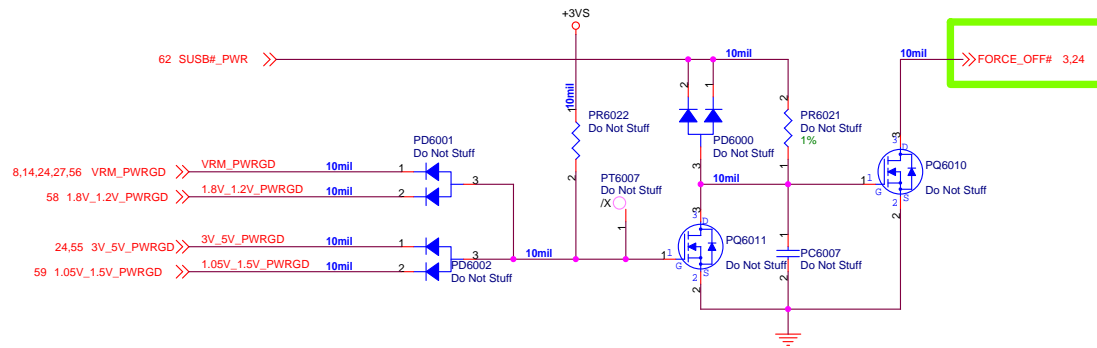
Close to PJP5201 & PJP5202

LUNCH

ASUS		Title :POWER_UO_1.5VS & 1.0VS	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	Z62H	1.0	
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Power Good Detector



1.2G

LUNCH

		Title : POWER_PROTECT	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom	Z62H		1.0
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5

4

3

2

1

D

D

C

C

B

B

A

A

LUNCH

		Title : POWER_BLANK	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007		Sheet	61 of 63

5

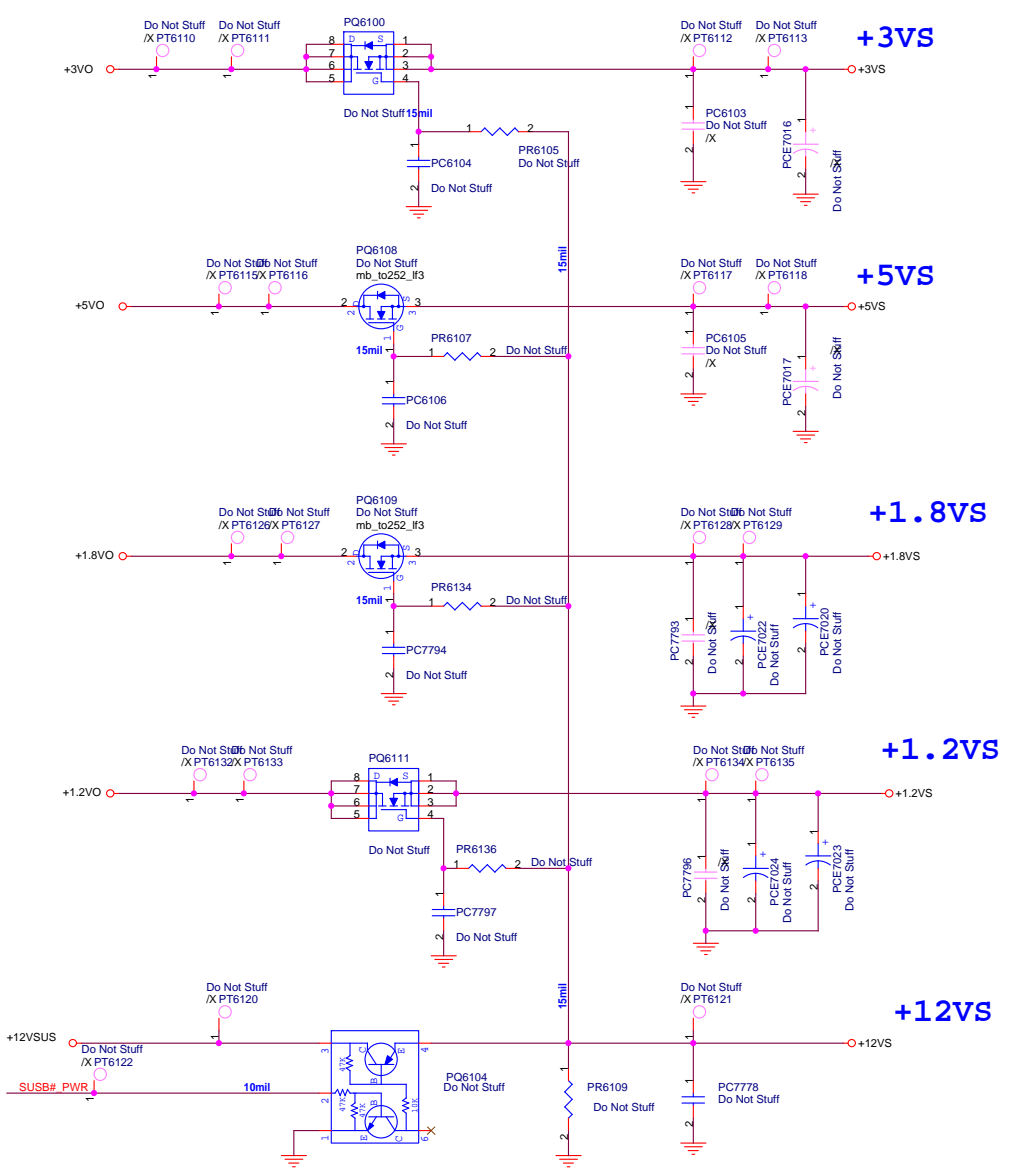
4

3

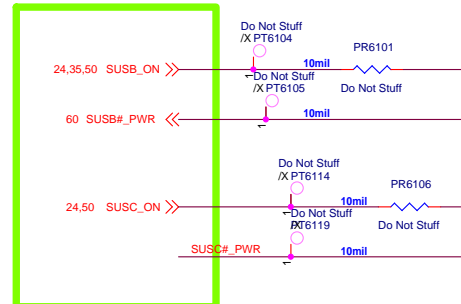
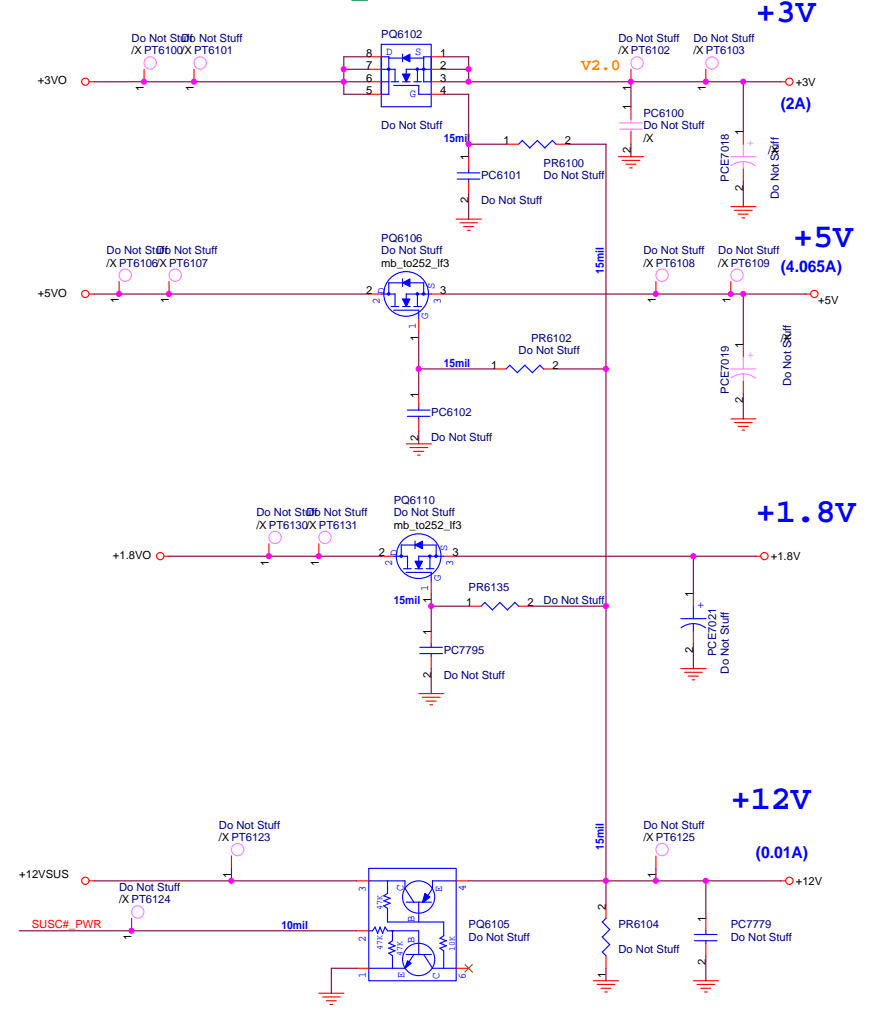
2

1

SUSB#_PWR POWER



SUSC#_PWR POWER



LUNCH

Title : POWER_LOAD SWITCH

ASUSTek Computer INC. **Engineer:**

Size	Project Name	Rev
Custom	Z62H	1.0

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