KL6A Intel Huron River Platform with Discrete GFX

01

FAN / THERMAL
EMC2103-2

DDRIII-SODIMM1
PG 13

DDRIII-SODIMM2
PG 14

Dual Channel DDR3
1333/1600 1.5V

DDR SYSTEM MEMORY

<MCH Process>
SandyBridge 0.61

rPGA 988

PCI-E

Graphics Interfaces

PG 3,4,5,6

FDI DMI

PCI-Express

Nvidia
N12P-GE
N12P-GV1 973p
N12P-GV

PG 15,16,17,18,19,20,21

27MHz

DMIX4

FDI DMI

CougarPoint 0.7
PCH

PG 7,8,9,10,11,12

SATA - HDD
PG 27
SATA1 150MB

SATA - CD-ROM
PG 27
SATA3 150MB

USB+eSATA
PG 27
SATA4 150MB

Speaker
PG 26

Audio Jack
(External MIC)
PG 26

Head-Phone Jack
PG 26

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ALC269
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IHDA

A-MIC
PG 26

32.768KHz
LPC

EC
IT8518
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INT_CRT
CRT
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INT_LVDS
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Port 10
Card Reader
RTS5139
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5-IN-1 Card
Reader CONN
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PCI-E

X1
Mini PCI-E Card
(WLAN)
PAGE 30

X1
LAN
Realtek
(10/100/1G LAN)
RTL8111E-VB-GR
RTL8105E
PAGE 25

25MHz

REGULATOR (DDR3)
1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU

REGULATOR
+1.05V_VTT,+1.8V

DC/DC
3VPCU, 5VPCU, +15V
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CPU Core
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VGA Core Discrete
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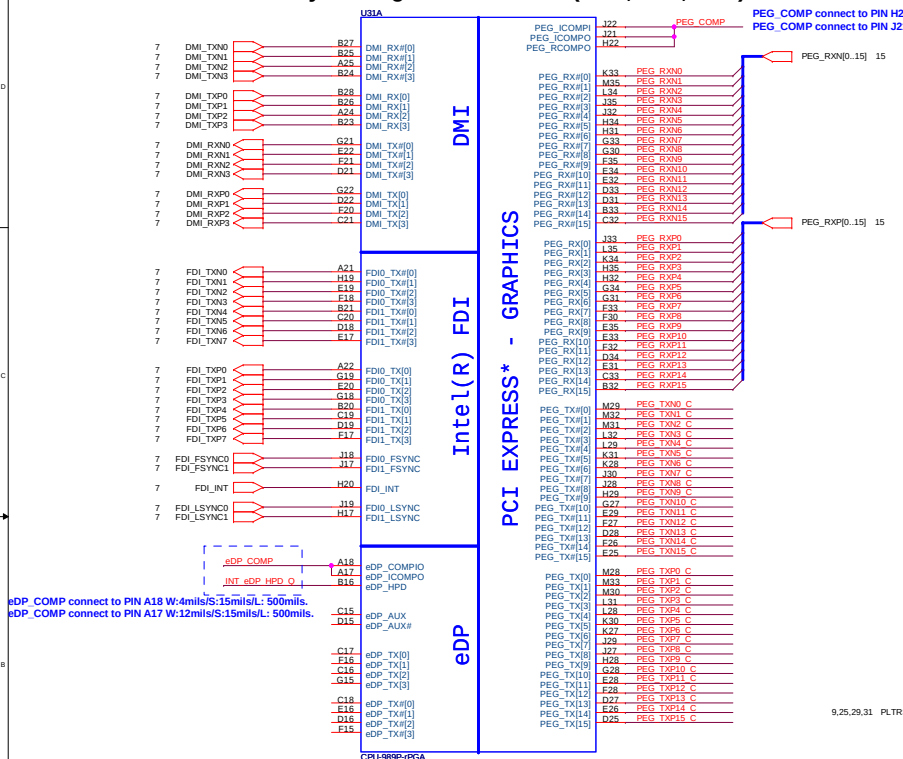
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,30,31,32,33,34,35	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	11,12,38	RTC		S0~S5
3VPCU	+3.3V	11,15,18,25,26,28,30,31,34,36	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	11,30,31,32,33,34,36	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,30,32,34	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	18,30	LAN POWER	LAN_ON	
5V_S5	+5V	12,20,30	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,11,12,21,22,30	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	26,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
+VCC_GFX_CORE	+0.9V~+1.2V	6,36	VGA CORE POWER	MAIN_ON	S0
0.9VSMDDR_VTERM	+0.75V	5,14,32	DDR2 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,15,16,17,19,25,27,28,30	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,6,9,10,11,12,14,15,16,17,18,19,21,22,23,24,26,28,30,32,33,34,35	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,21,32	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	6,8,12,17,22,23,36	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V	+1.05V	3,4,6,9,12,30,33	PCH CORE POWER	MAIN_ON	S0
VCC_CORE		6,30,35	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	L_VDD_EN	S0
BAT-V	+10V~+17V	31	MAIN BATTERY	CHG_PBATT	S0~S5

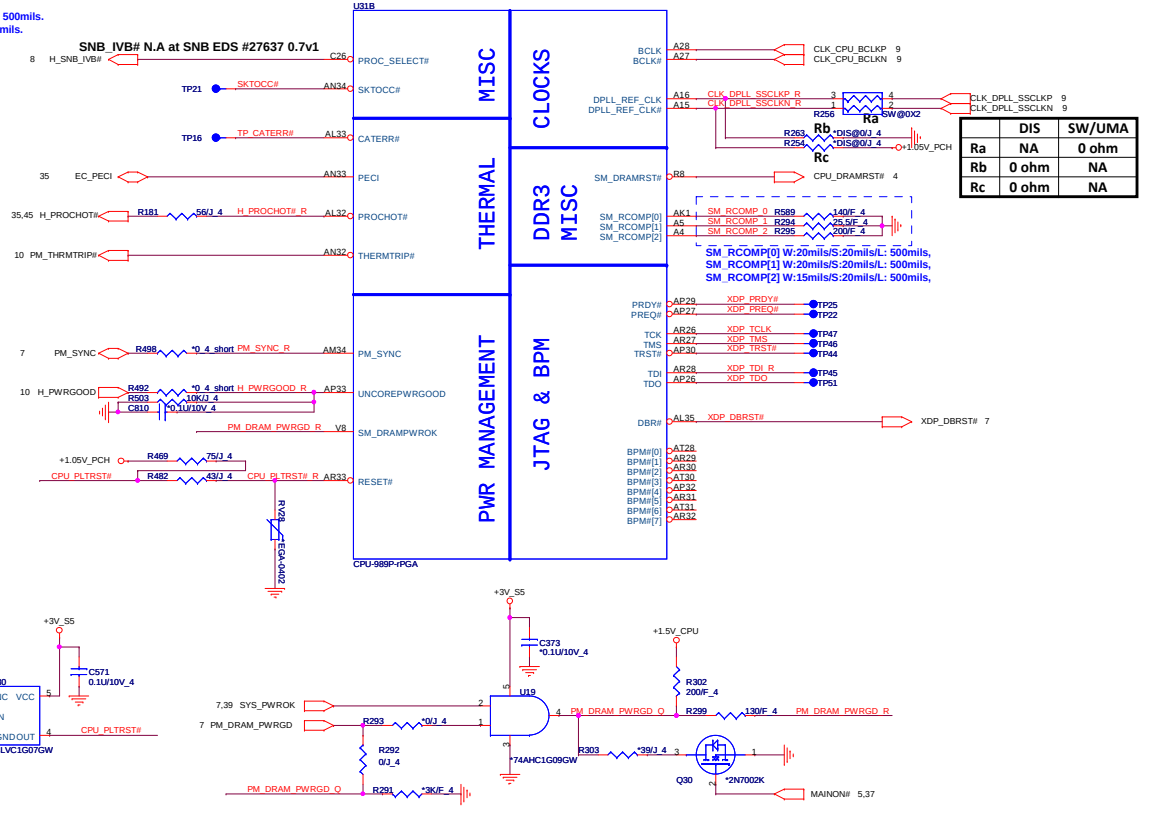
Sandy Bridge Processor (DMI,PEG,FDI)



eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

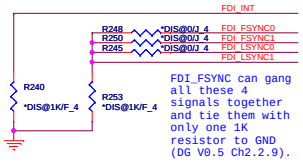
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

Sandy Bridge Processor (CLK,MISC,JTAG)



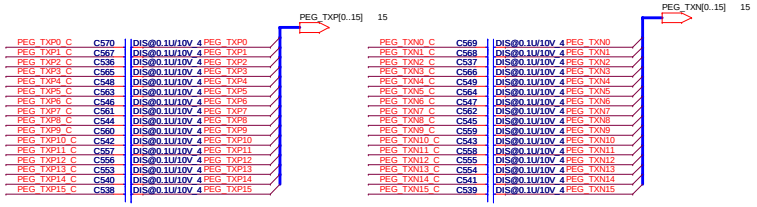
	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

FDI Disable

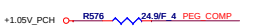


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

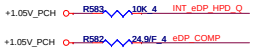
PEG x16 (UMA Non-stuff)



DP & PEG Compensation

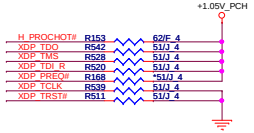


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



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Sandy Bridge Processor (DDR3)

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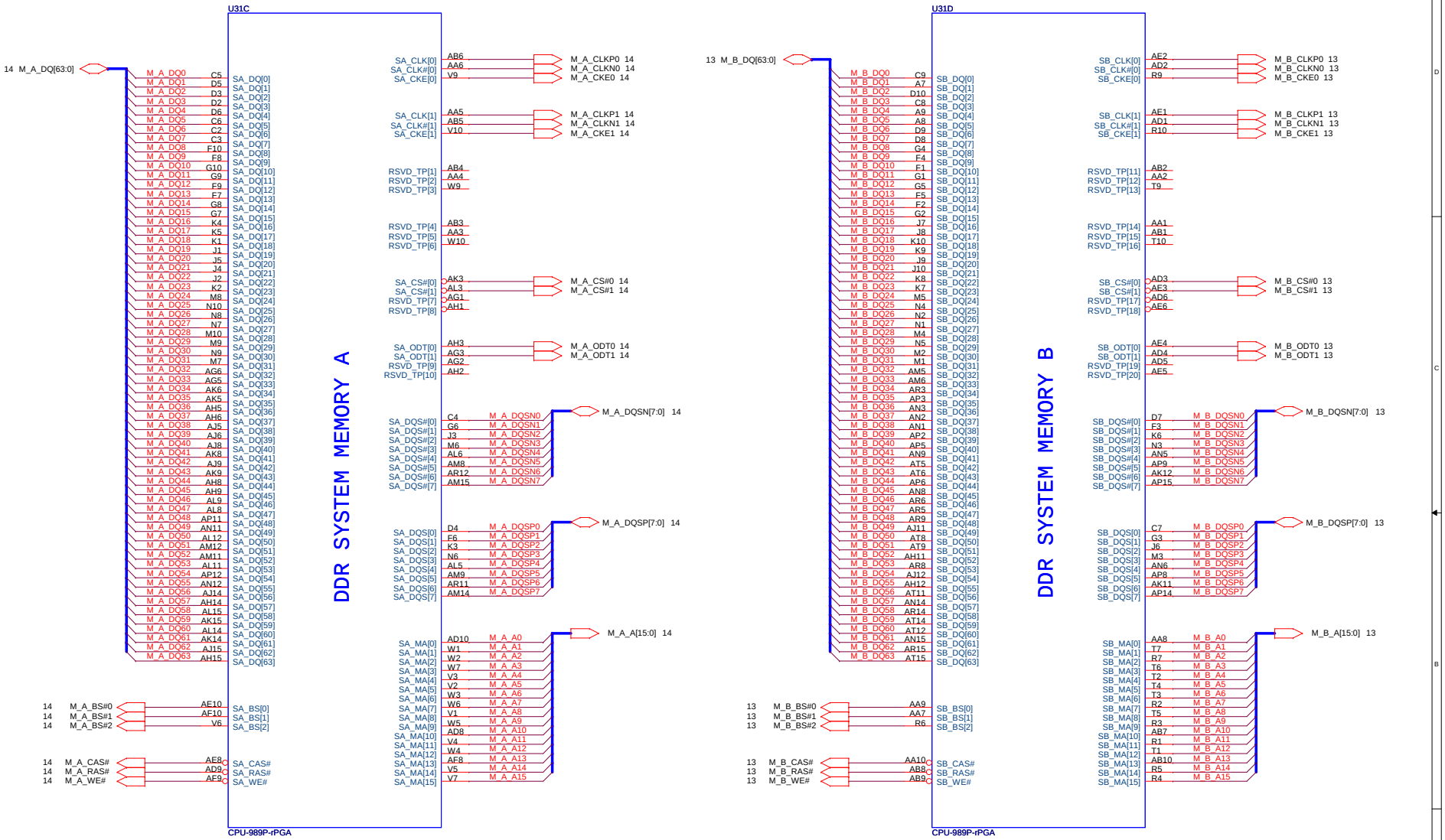

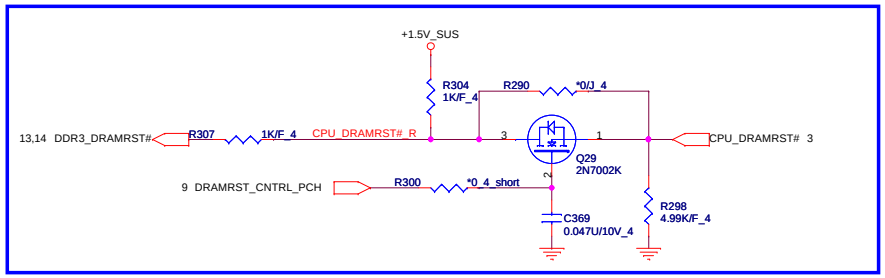

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
VREF
SA RAIL
1.8V RAIL
MISC

U31F
CPU-989P-rPGA
U31G
CPU-989P-rPGA

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
R169 54.9/F_4
H_CPU_SVIDCLK R182 *0_4 short VR_SVID_CLK 45

Place PU resistor close to CPU
R171 130/F_4

SVID DATA
Close to VR
R161 130/F_4
H_CPU_SVIDAT R183 *0_4 short VR_SVID_DATA 45

Place PU resistor close to CPU
R160 75/J_4
H_CPU_SVIDALRT# R170 43/J_4 R159 *0_4 short VR_SVID_ALERT# 45

SVID ALERT

4.5A
Q31 AO4496
Q32 DMN601K-7
3/26 DB add for Intel. Placement close to CPU.

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

22uF (Reserved)

Ra	DIS	SW
Ra	0 ohm	NA

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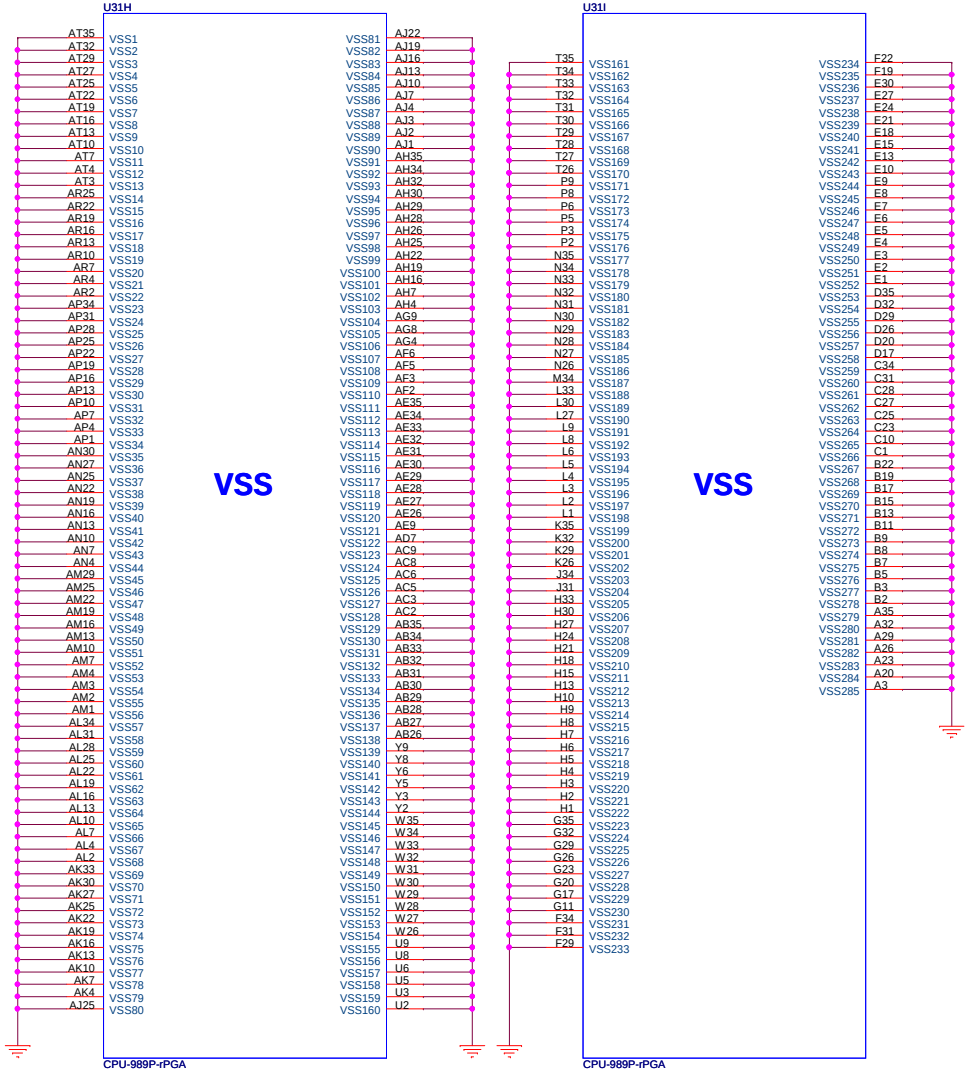
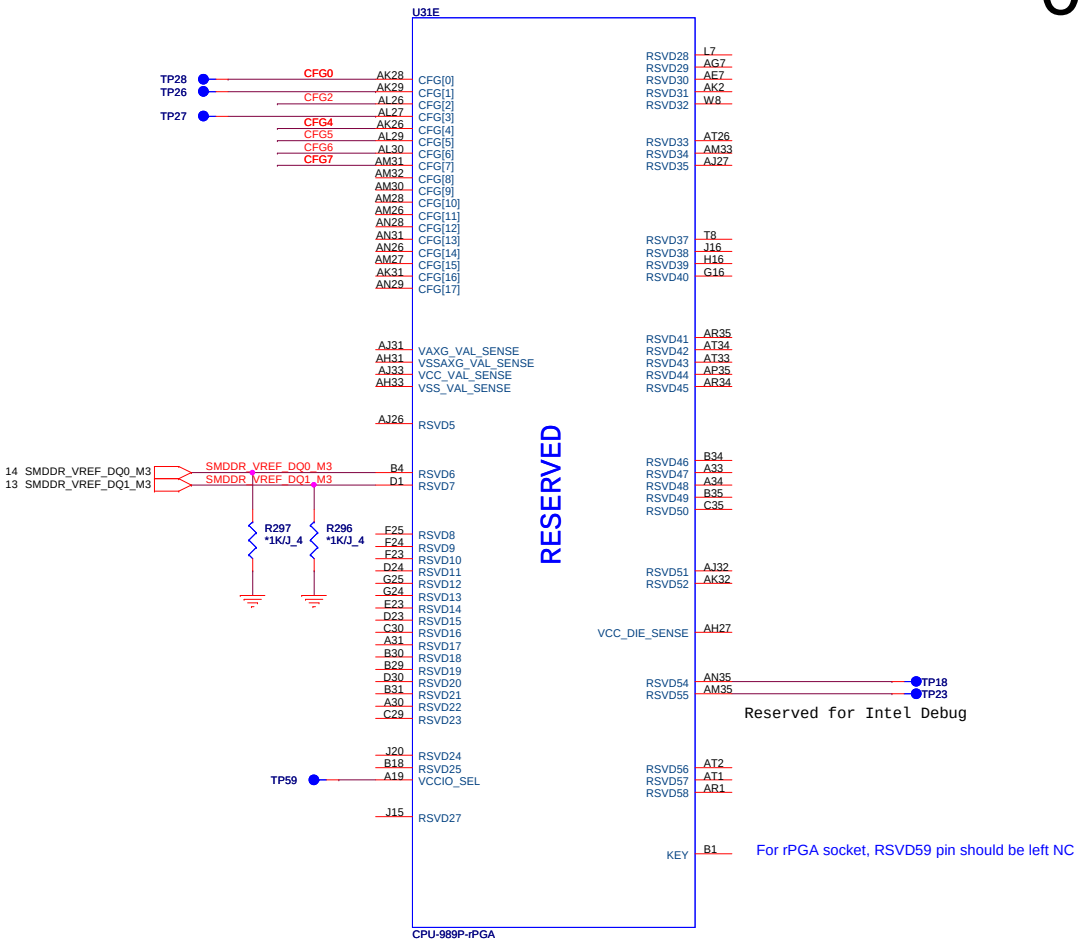
Sandy Bridge Processor (GND)



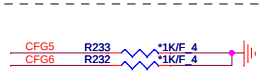
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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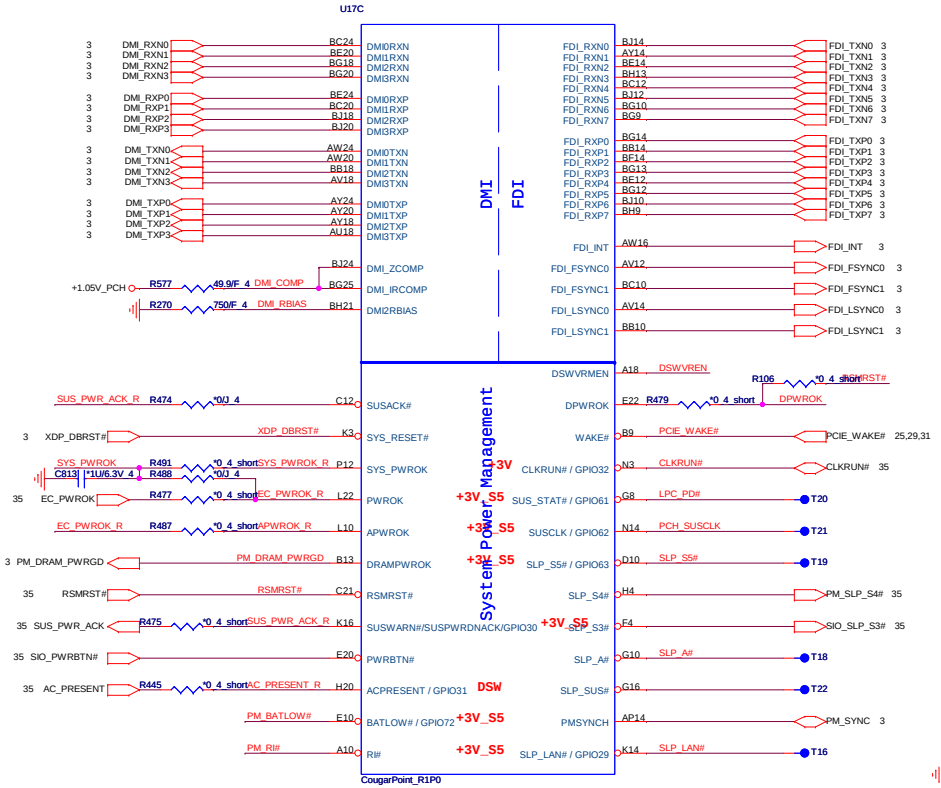
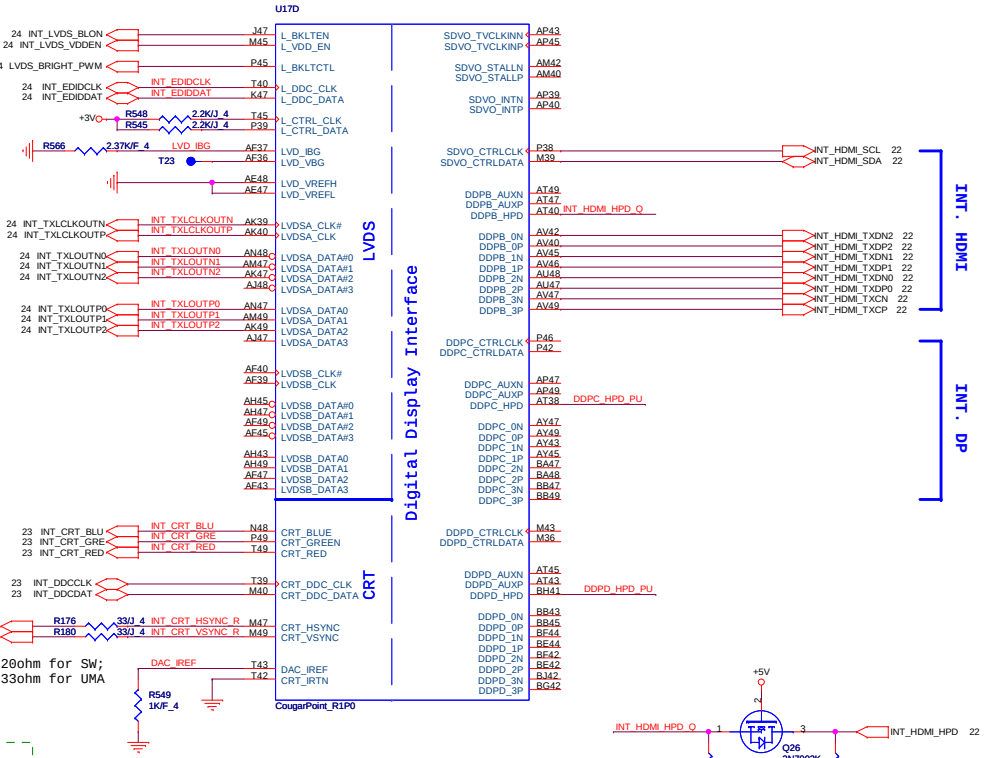
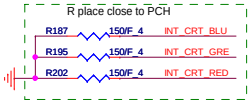
Cougar Point (DMI,FDI,PM)

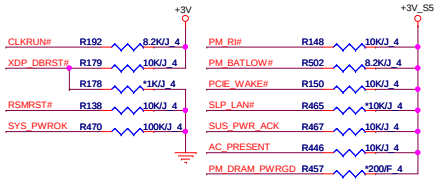


Cougar Point (LVDS,DDI)

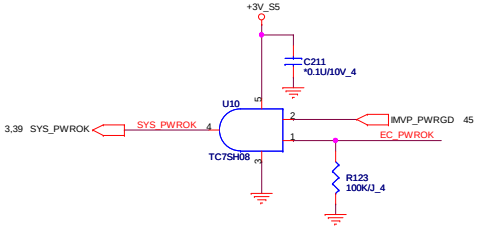


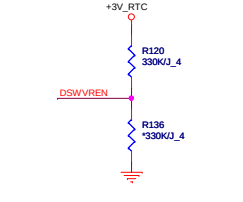


PCH Pull-high/low(CLG)

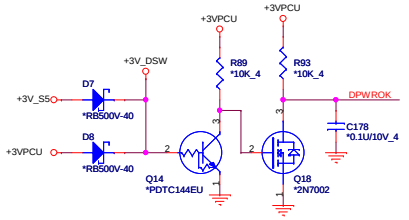


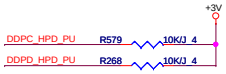
System PWR_OK(CLG)





DPWROK FOR DSW





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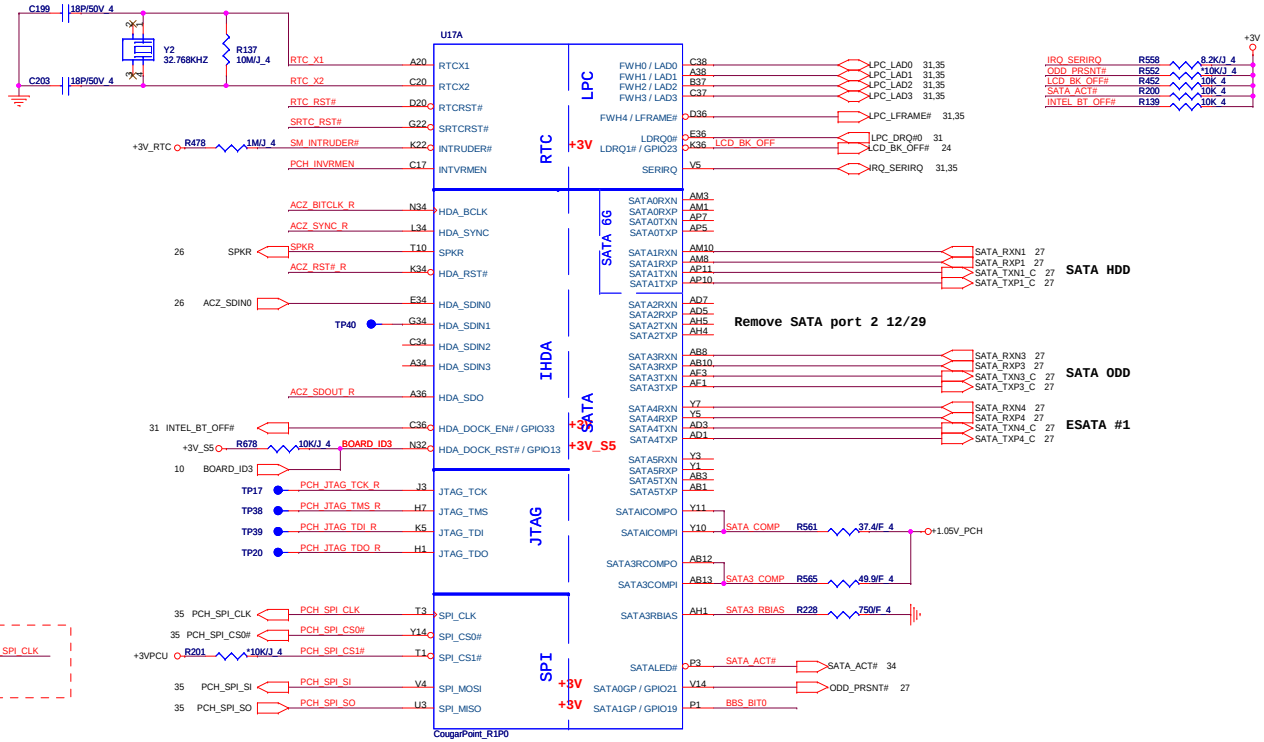
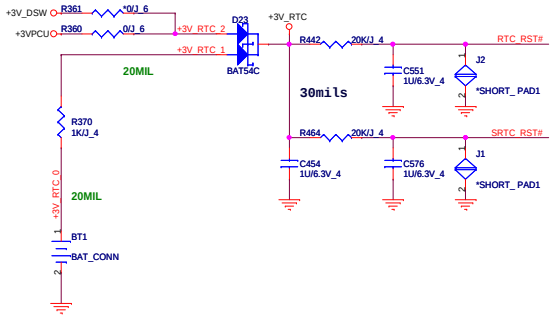
PCH2(CLG)

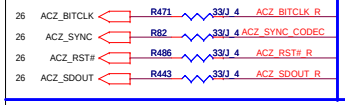
Cougar Point (HDA,JTAG,SATA)



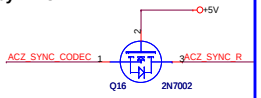
RTC Circuitry(RTC)



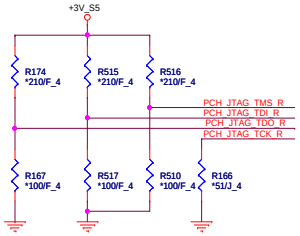
HDA Bus(CLG)



To Separate Codec Sync by PD3



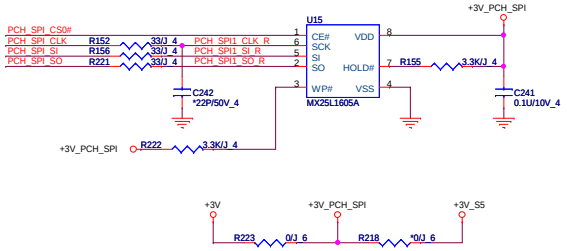
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

32Mbit (4M Byte), SPI

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



RF request

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R557 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R521 *1K/J_4 PCI_GNT3# 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R121 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R504 *1K/J_4 BBS_BIT1 9 R193 *1K/J_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R463 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R265 2.2K/J_4 +1.8V R266 4.7K/J_4 DF_TVS 10 H_SNB_IVB# 3
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R522 *1K/J_4 PLL_ODVR_EN 10
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R81 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R146 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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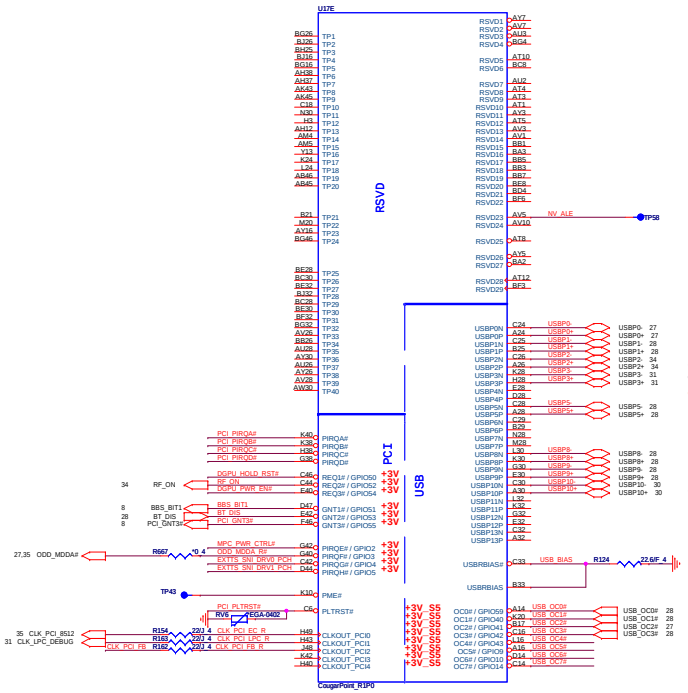
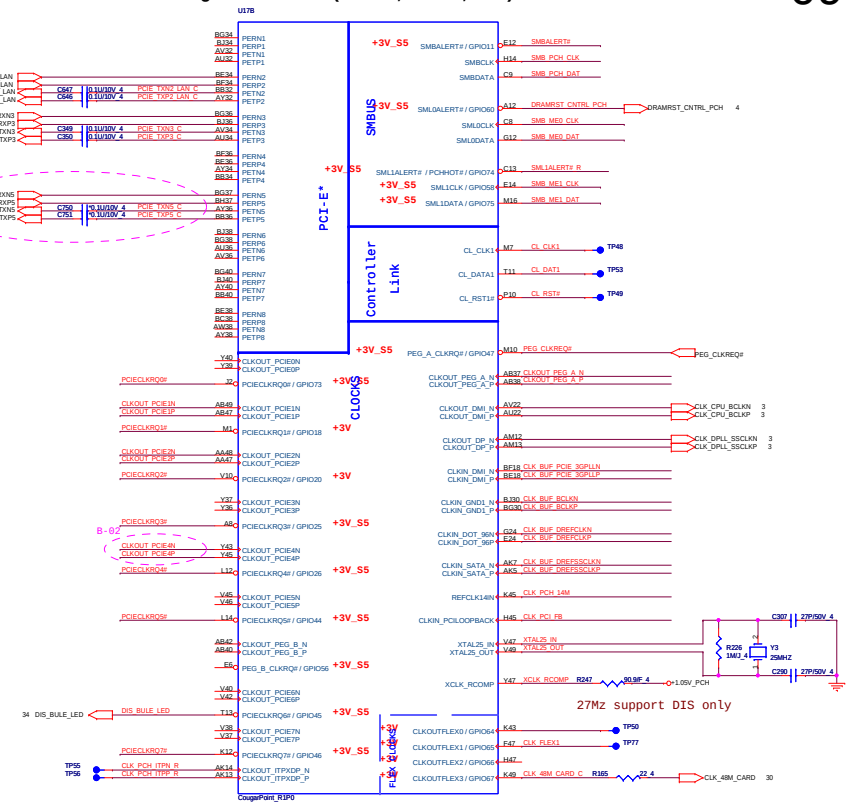
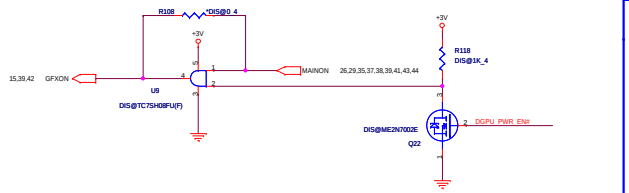
Cougar Point-M (PCI,USB,NVRAM)



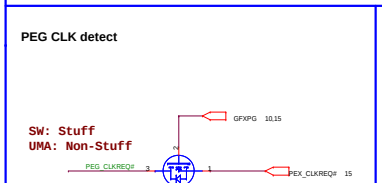
Cougar Point-M (PCI-E,SMBUS,CLK)



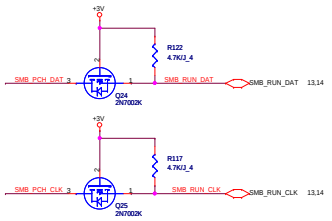
DGPU Power ON



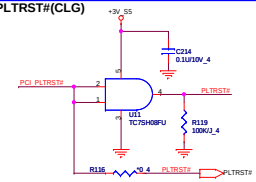
PEG CLK detect



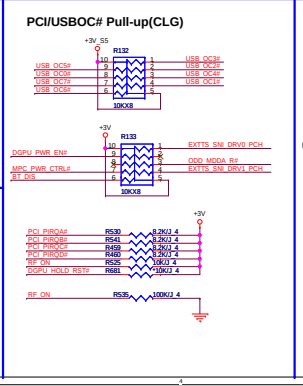
SMBus(CLK)



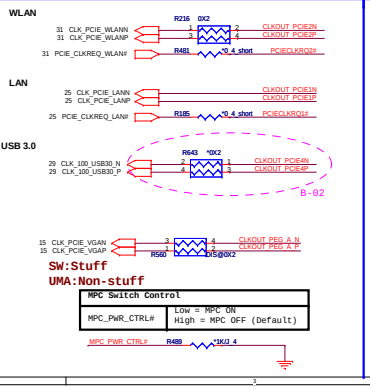
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)

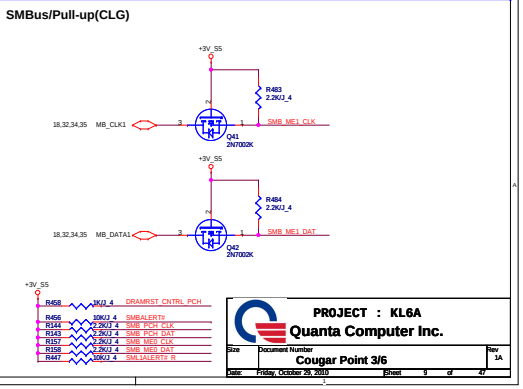


WLAN / LAN / USB 3.0

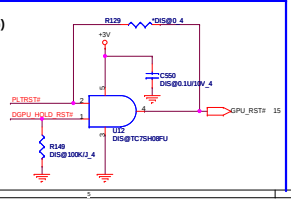


CLK_REQ/Strap Pin(CLG)

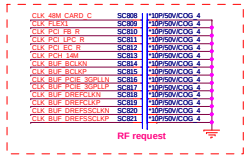
SMBus/Pull-up(CLG)



GPU RST#(CLG)



RF request



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Cougar Point (GPIO,VSS_NCTF,RSVD)

U17F

S_GPIO R546 100_4 — T7 BMBUSY# / GPIO0 +3V
29,35 EC_EXT_SMI# — A42 TACH1 / GPIO1 +3V
BOARD_ID1 — H36 TACH2 / GPIO6 +3V
35 EC_EXT_SCI# — E38 TACH3 / GPIO7 +3V
TP76 ICC_EN# — C10 GPIO8 +3V_S5
31 LAN_DISABLE# — C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R — G2 GPIO15 +3V_S5
BOARD_ID0 — U2 SATA4GP / GPIO16 +3V
GFXPG_R — D40 TACH0 / GPIO17 +3V
BIOS_REC — T5 SCLOCK / GPIO22 +3V
USB30_ID — E8 GPIO24 / MEM_LED +3V_S5
GPIO27 — E16 GPIO27 DSW
8 PLL_ODVR_EN — R536 *0_4_short PLL_ODVR_EN_R — P8 GPIO28 +3V_S5
SYSTEM_ID — K1 STP_PCI# / GPIO34 +3V
28 BT_ON# — K4 GPIO35 +3V
TP54 DMI_OVRVLTG — V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG — M5 SATA3GP / GPIO37 +3V
MFG_MODE — N2 SLOAD / GPIO38 +3V
DGPU_PRSNT# — M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP — V13 SDATAOUT1 / GPIO48 +3V
32,35 TEMP_ALERT# — V3 SATA5GP / GPIO49 +3V
SV_DET — D6 GPIO57 +3V_S5

GPIO

C40 TACH4 / GPIO68 — CPU_ID
B41 TACH5 / GPIO69 — R126 1.5K/F_4
C41 TACH6 / GPIO70 — COLOR_ENGINE_DET
A40 TACH7 / GPIO71 — BOARD_ID2

CPU/MISC

P4 A20GATE — EC_A20GATE 35
AU16 PECI — TP57
P5 RCIN# — EC_RCIN 35
AY11 PROCPWRGD — H_PWRGOOD 3
AY10 THRMTRIP# — R578 390/J_4 — PM_THRMTRIP# 3
T14 INIT3_3V#
AY1 DF_TVS — DF_TVS 8

AH8 TS_VSS1
AK11 TS_VSS2
AH10 TS_VSS3
AK10 TS_VSS4
P37 NC_1

NCTF

A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14

BG2 VSS_NCTF_15
BG48 VSS_NCTF_16
BH3 VSS_NCTF_17
BH47 VSS_NCTF_18
BJ4 VSS_NCTF_19
BJ44 VSS_NCTF_20
BJ45 VSS_NCTF_21
BJ46 VSS_NCTF_22
BJ5 VSS_NCTF_23
BJ6 VSS_NCTF_24
C2 VSS_NCTF_25
C48 VSS_NCTF_26
D1 VSS_NCTF_27
D49 VSS_NCTF_28
E1 VSS_NCTF_29
E49 VSS_NCTF_30
F1 VSS_NCTF_31
F49 VSS_NCTF_32

CougarPoint_R1P0

R114 *DIS@0_4 — +3V
GFXPG_R — GFXPG_R — U8 — HWPG 35,39,40,41,43,44,45 — GFXPG 9,15
DIS@TC7SH08FU(F)

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R164 10K/J_4
+3V
COLOR_ENGINE_DET R644 10K_4
EC_EXT_SMI# R127 10K/J_4
EC_EXT_SCI# R461 10K/J_4
EC_A20GATE R543 10K/J_4
EC_RCIN# R556 10K/J_4
TEMP_ALERT# R211 10K/J_4
BT_ON# R507 10K/J_4
GPIO27 R490 10K/J_4
GFXPG_R R113 DIS@10K/J_4

Board ID

B-04

Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID3 GPIO13	ID1 GPIO6	ID0 GPIO16	CPU_ID GPIO68
SDV	1	1	0	0	0	1
SIV	1	1	0	0	1	1
SIT	1	1	0	1	0	1
SVT	1	1	0	1	1	1
SOVP	1	1	1	0	0	1

Board ID use below GPIO:
BOARD_ID0
BOARD_ID1
BOARD_ID3

ID2: 0-->6 layer
1-->8 layer

System ID: 0-->KL5
1-->KL6

CPU_ID: 0-->35W
1-->45W

+3V
R675 *10K/J_4 CPU_ID R676 10K/J_4
R207 10K/J_4 BOARD_ID0 R199 *10K/J_4
R462 *10K/J_4 BOARD_ID1 R444 10K/J_4
R140 10K/J_4 BOARD_ID2 R125 *10K/J_4
R147 *10K/J_4 SYSTEM_ID R142 10K/J_4
+3V_S5
R682 10K/J_4 BOARD_ID3 R683 *10K/J_4
BOARD_ID3 8

SV_SET_UP
High = Strong (Default)
TEST_SET_UP R559 10K/J_4 R555 *0/J_4 +3V

USB30_ID	GPIO24
USB3.0	0
Non-USB3.0	1

+3V_S5
R679 *10K/J_4 USB30_ID R680 10K/J_4

+3V
R509 *10K/J_4 SV_DET R501 100K/J_4

HOST_ALERT#1_R R508 1K/J_4 +3V_S5
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

+3V
R533 *10K/J_4 DGPU_PRSNT# R532 DIS@100K/J_4

SGPIO

+3V
S_GPIO R551 10K/J_4 R550 *0/J_4

MFG-TEST

+3V
MFG_MODE R184 10K/J_4 R194 *0/J_4

+3V
R526 100K/J_4 FDI_OVRVLTG R527 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
DMI_OVRVLTG R668 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R547 10K/J_4 R554 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

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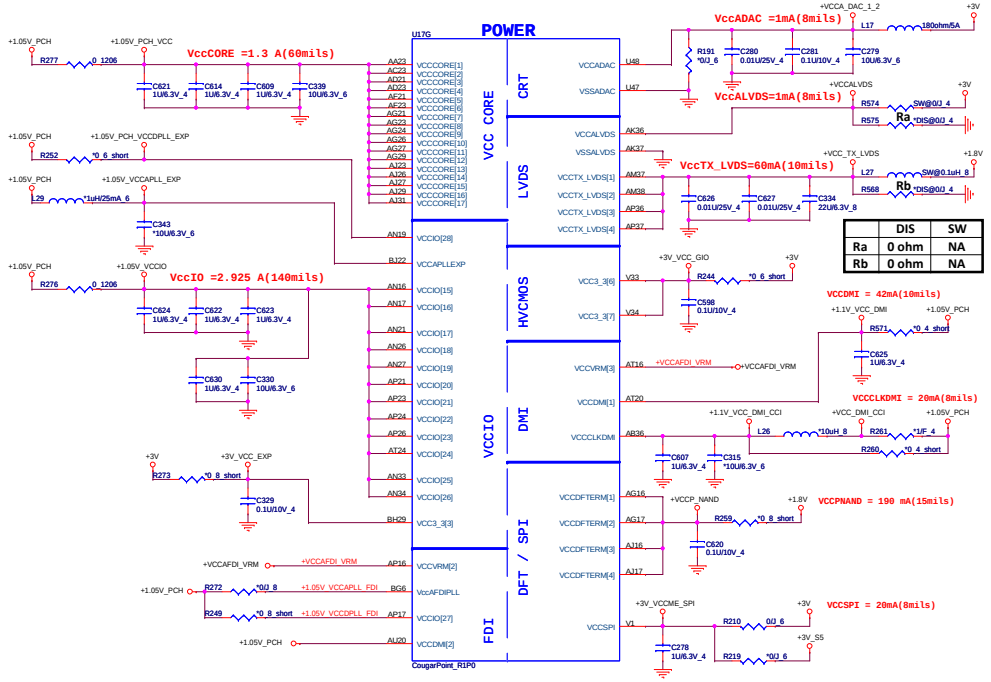
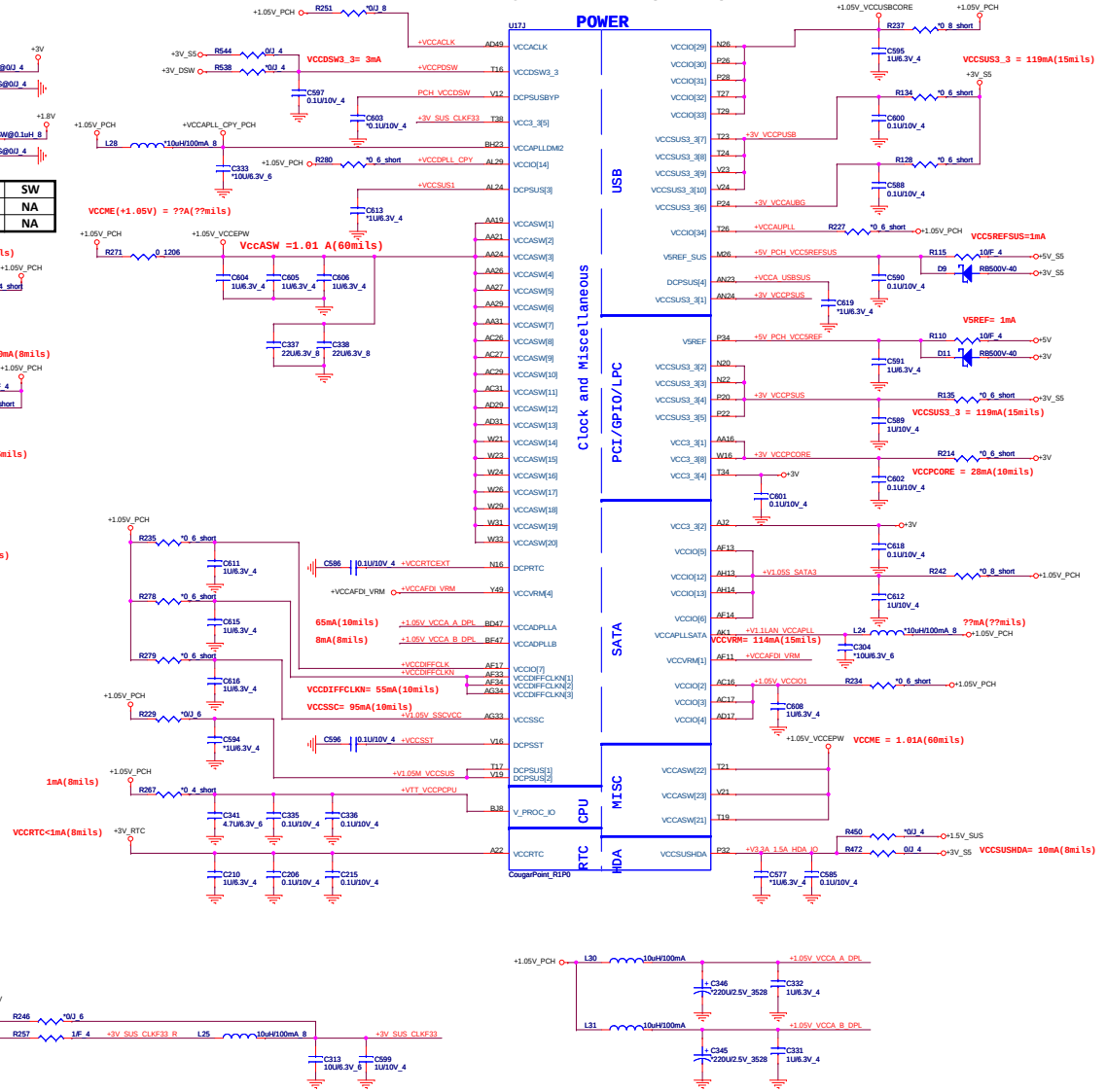
COUGAR POINT (POWER)



Cougar Point-M (POWER)



	DIS	SW
Ra	0 ohm	NA
Rb	0 ohm	NA

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Quanta Computer Inc.

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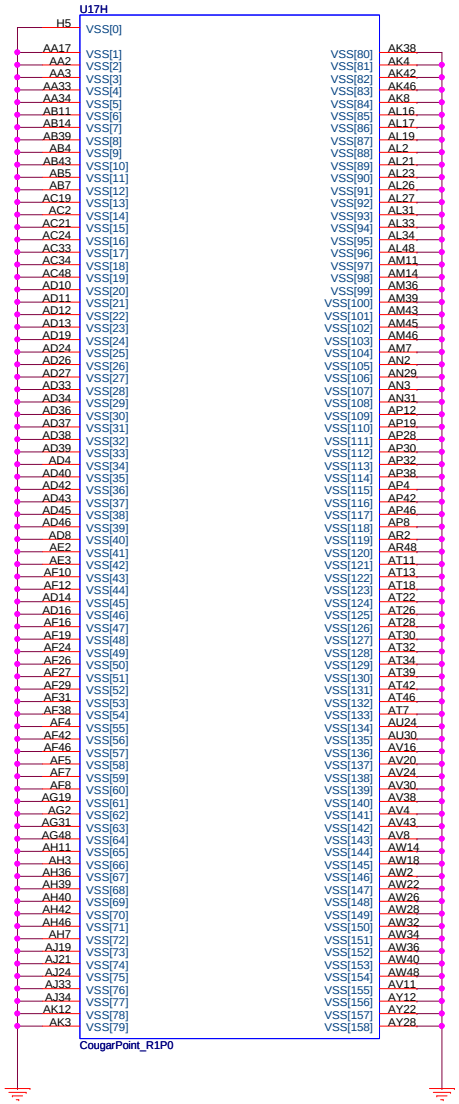
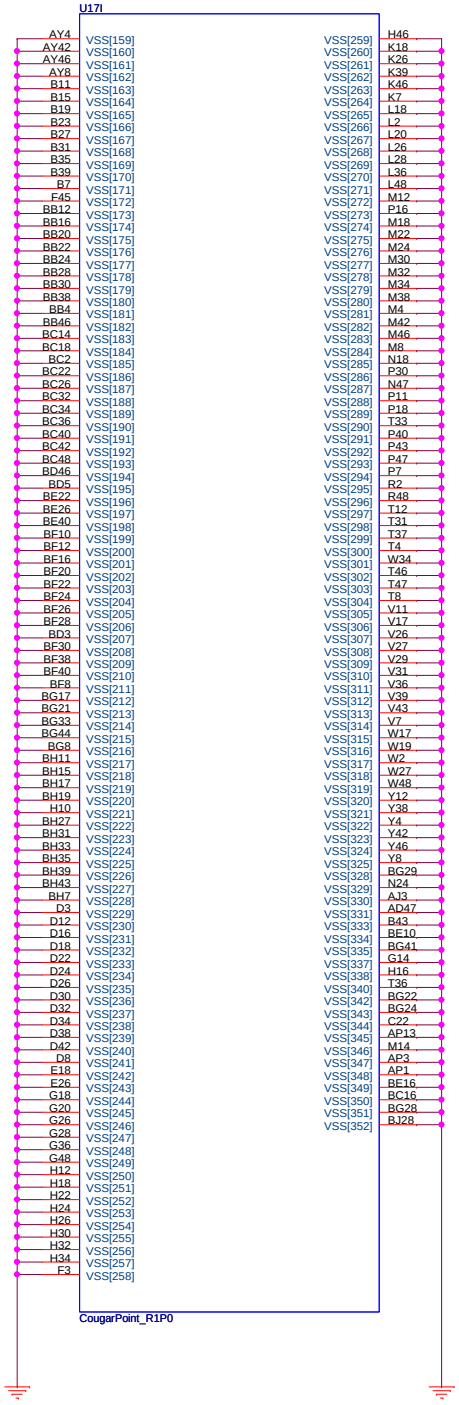
IBEX PEAK-M (GND)





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Quanta Computer Inc.

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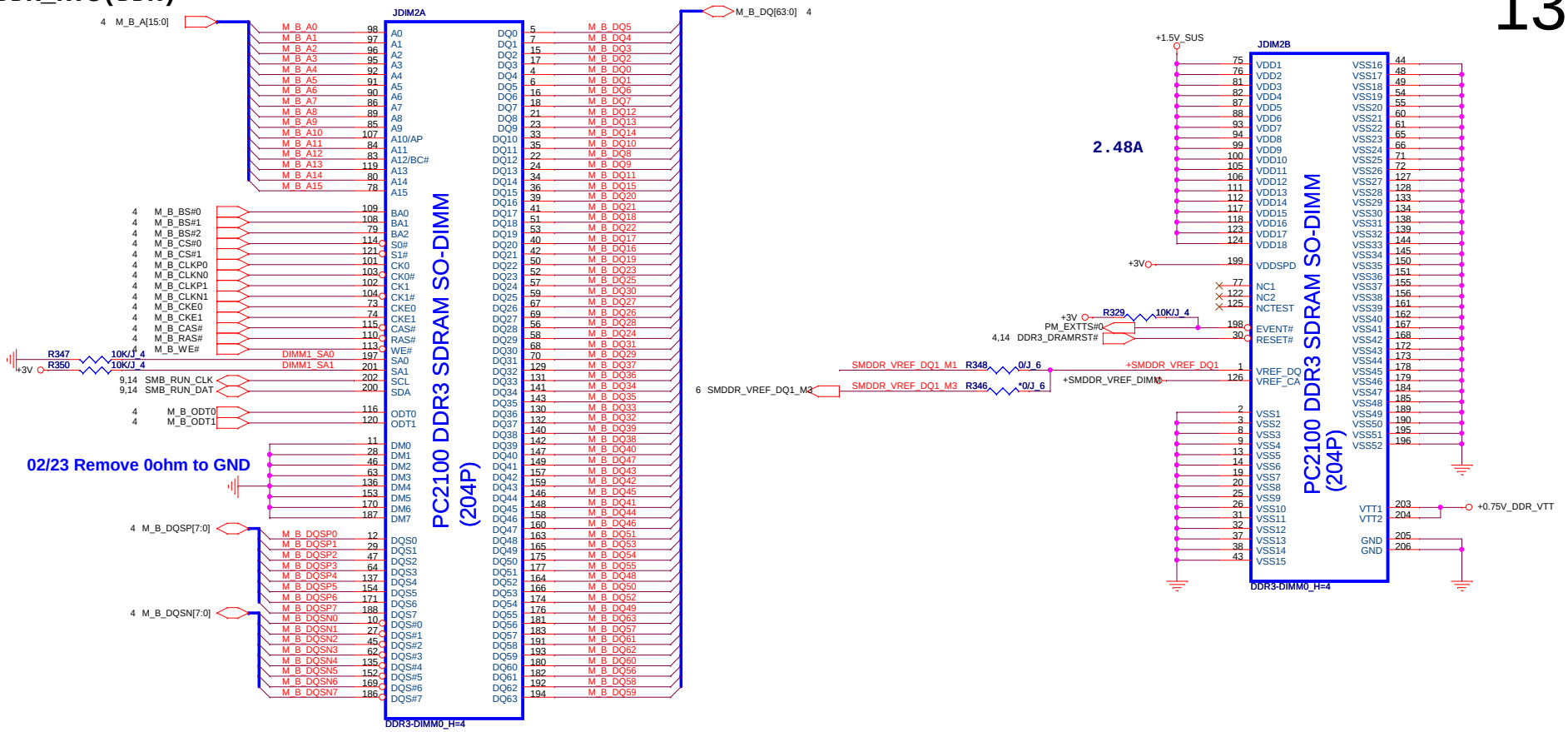
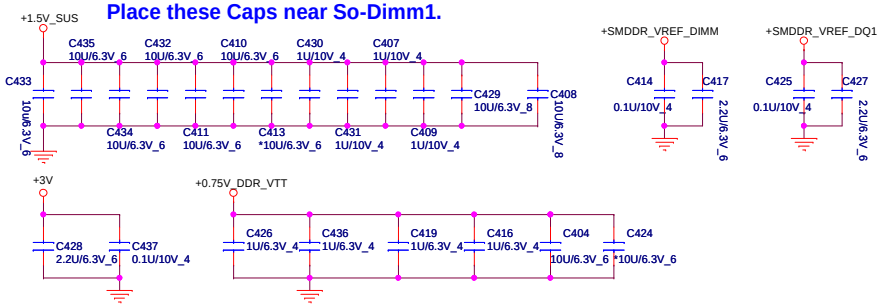
DDR_RVS(DDR)

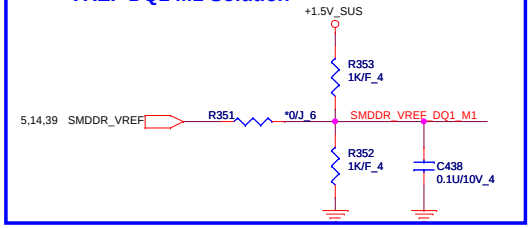


Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

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	DDRIII SO-DIMM-0	1A

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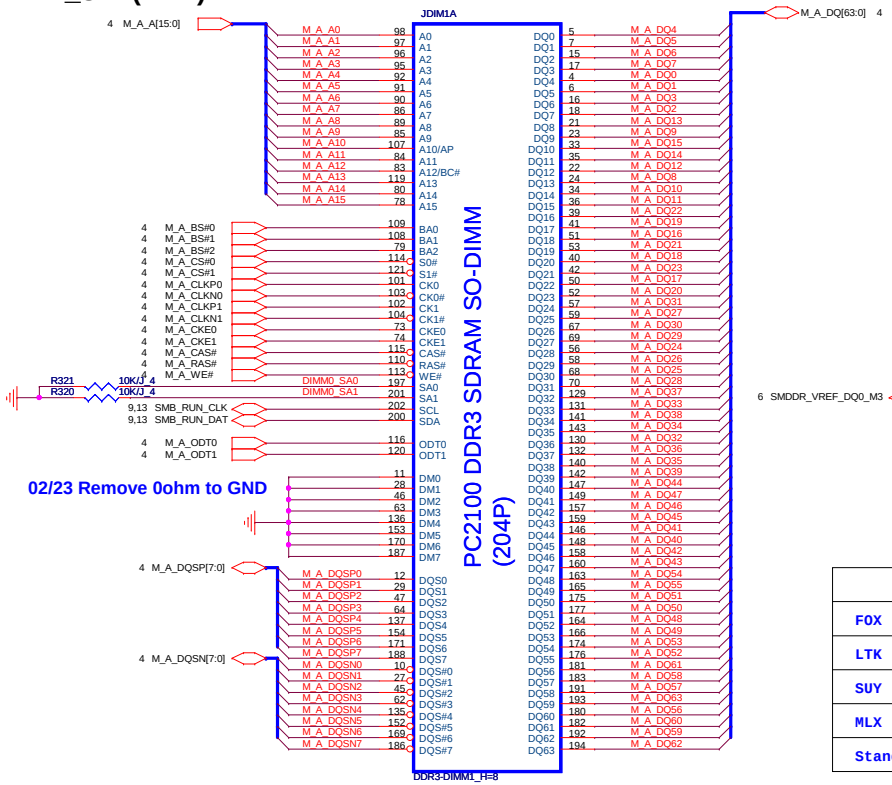
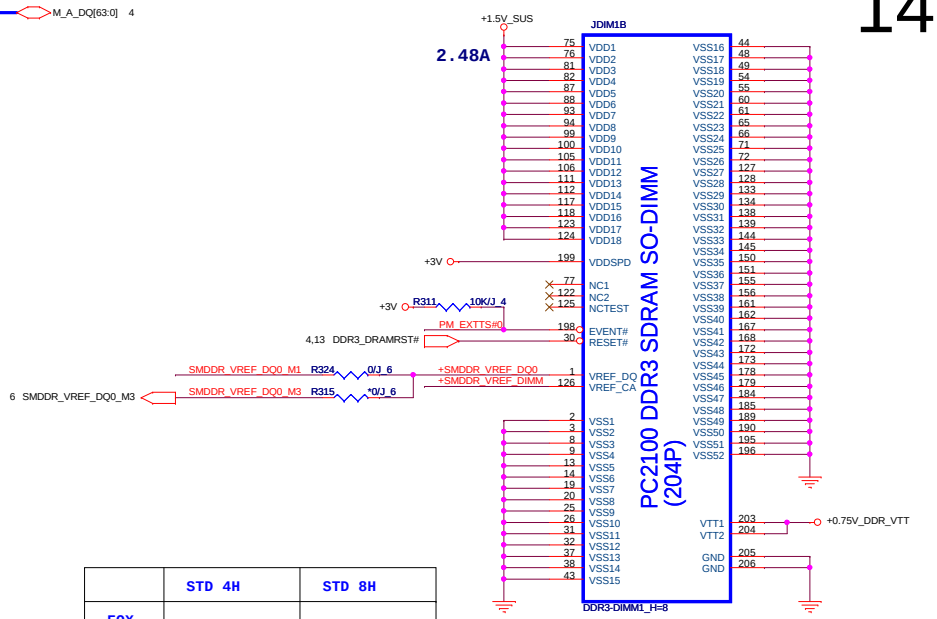
DDR_STD(DDR)



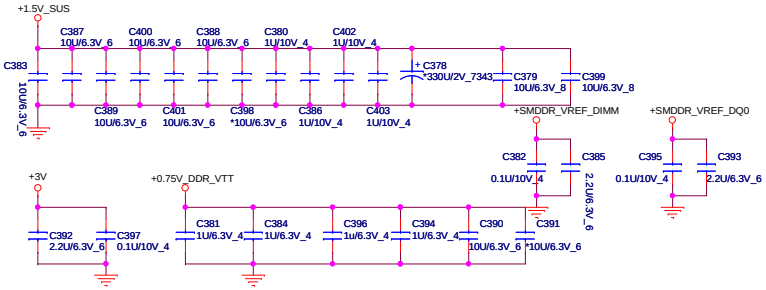
02/23 Remove 0ohm to GND

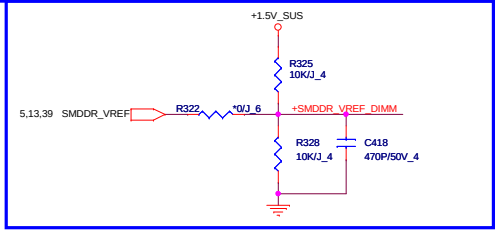


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

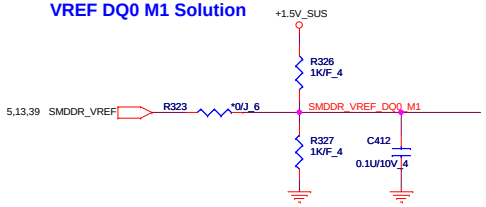
VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



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Quanta Computer Inc.

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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

0.5A

+1.05V_GFX_PCIE

C171 0.1U/10V_4
C167 0.1U/10V_4
C172 1U/6.3V_4
C173 1U/6.3V_4
C216 4.7U/6.3V_6
C201 10U/6.3V_8
C213 22U/6.3V_8

1.6A

+1.05V_GFX_PCIE

C169 0.1U/10V_4
C154 0.1U/10V_4
C155 1U/6.3V_4
C156 1U/6.3V_4
C166 4.7U/6.3V_6
C195 10U/6.3V_8
C212 22U/6.3V_8

CAP CLOSE TO BGA

U28A
fcbga973-nvidia-n12p-ge
COMMON

AK16 PEX_IOVDD_1
AK17 PEX_IOVDD_2
AK21 PEX_IOVDD_3
AK24 PEX_IOVDD_4
AK27 PEX_IOVDD_5

AG11 PEX_IOVDDQ_1
AG12 PEX_IOVDDQ_2
AG13 PEX_IOVDDQ_3
AG15 PEX_IOVDDQ_4
AG16 PEX_IOVDDQ_5
AG17 PEX_IOVDDQ_6
AG18 PEX_IOVDDQ_7
AG22 PEX_IOVDDQ_8
AG23 PEX_IOVDDQ_9
AG24 PEX_IOVDDQ_10
AG25 PEX_IOVDDQ_11
AG26 PEX_IOVDDQ_12
AJ14 PEX_IOVDDQ_13
AJ15 PEX_IOVDDQ_14
AJ19 PEX_IOVDDQ_15
AJ21 PEX_IOVDDQ_16
AJ22 PEX_IOVDDQ_17
AJ24 PEX_IOVDDQ_18
AJ25 PEX_IOVDDQ_19
AJ27 PEX_IOVDDQ_20
AK18 PEX_IOVDDQ_21
AK20 PEX_IOVDDQ_22
AK23 PEX_IOVDDQ_23
AK26 PEX_IOVDDQ_24
AL16 PEX_IOVDDQ_25

+3V_GPU

C107 4.7U/6.3V_6
C93 1U/6.3V_4
C82 0.1U/10V_4
C86 0.1U/10V_4
C97 0.1U/10V_4

J10 VDD33_1
J11 VDD33_2
J12 VDD33_3
J13 VDD33_4
J9 VDD33_5

GFX_CORE

AD20 VDD_SENSE
D35 NC_9/ VDD_SENSE
P7 NC_16/ VDD_SENSE

12~16 mils width for 110mA

AD19 GND_SENSE
E35 NC_10/ GND_SENSE
R7 NC_17/ GND_SENSE

+1.05V_GFX_PCIE

L15 BLM18PG121SN
C196 0.1U/10V_4
C187 1U/6.3V_4
C200 4.7U/6.3V_6

+PEX_PLLVDD

AG14 PEX_PLLVDD

12~16 mils width

+3V_GPU

L1 0/J_6 +PEX_SVDD_3V3

C64 1U/6.3V_4
C153 0.1U/10V_4
C76 4.7U/6.3V_6

AG19 PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
F7 NC_12/ PEX_SVDD_3V3

AG20 PEX_CAL_PU_GND/ NC
A2 NC_1
AB7 NC_2
AD6 NC_3
AF6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
E7 NC_11
H32 NC_13
M7 NC_14
P6 NC_15
U7 NC_18
V6 NC_19

R60 *10K/J_4 PGOOD

R420 *40.2K/F_4 MULTI_STRAP_REF2_GND

PCI EXPRESS

PEX_RX0 AP17 PEG_TXP15 3
PEX_RX0* AN17 PEG_TXN15 3
PEX_RX1 AN19 PEG_TXP14 3
PEX_RX1* AP19 PEG_TXN14 3
PEX_RX2 AR19 PEG_TXP13 3
PEX_RX2* AR20 PEG_TXN13 3
PEX_RX3 AP20 PEG_TXP12 3
PEX_RX3* AN20 PEG_TXN12 3
PEX_RX4 AN22 PEG_TXP11 3
PEX_RX4* AP22 PEG_TXN11 3
PEX_RX5 AR22 PEG_TXP10 3
PEX_RX5* AR23 PEG_TXN10 3
PEX_RX6 AP23 PEG_TXP9 3
PEX_RX6* AN23 PEG_TXN9 3
PEX_RX7 AN25 PEG_TXP8 3
PEX_RX7* AP25 PEG_TXN8 3
PEX_RX8 AR25 PEG_TXP7 3
PEX_RX8* AR26 PEG_TXN7 3
PEX_RX9 AP26 PEG_TXP6 3
PEX_RX9* AN26 PEG_TXN6 3
PEX_RX10 AN28 PEG_TXP5 3
PEX_RX10* AP28 PEG_TXN5 3
PEX_RX11 AR28 PEG_TXP4 3
PEX_RX11* AR29 PEG_TXN4 3
PEX_RX12 AP29 PEG_TXP3 3
PEX_RX12* AN29 PEG_TXN3 3
PEX_RX13 AN31 PEG_TXP2 3
PEX_RX13* AP31 PEG_TXN2 3
PEX_RX14 AR31 PEG_TXP1 3
PEX_RX14* AR32 PEG_TXN1 3
PEX_RX15 AR34 PEG_TXP0 3
PEX_RX15* AP34 PEG_TXN0 3

PEX_TX0 AL17 PEG_RXP15_C C260 0.1U/10V_4 PEG_RXP15 3
PEX_TX0* AM17 PEG_RXN15_C C259 0.1U/10V_4 PEG_RXN15 3
PEX_TX1 AM18 PEG_RXP14_C C231 0.1U/10V_4 PEG_RXP14 3
PEX_TX1* AM19 PEG_RXN14_C C232 0.1U/10V_4 PEG_RXN14 3
PEX_TX2 AL19 PEG_RXP13_C C258 0.1U/10V_4 PEG_RXP13 3
PEX_TX2* AK19 PEG_RXN13_C C257 0.1U/10V_4 PEG_RXN13 3
PEX_TX3 AL20 PEG_RXP12_C C230 0.1U/10V_4 PEG_RXP12 3
PEX_TX3* AM20 PEG_RXN12_C C229 0.1U/10V_4 PEG_RXN12 3
PEX_TX4 AM21 PEG_RXP11_C C255 0.1U/10V_4 PEG_RXP11 3
PEX_TX4* AM22 PEG_RXN11_C C256 0.1U/10V_4 PEG_RXN11 3
PEX_TX5 AL22 PEG_RXP10_C C228 0.1U/10V_4 PEG_RXP10 3
PEX_TX5* AK22 PEG_RXN10_C C227 0.1U/10V_4 PEG_RXN10 3
PEX_TX6 AL23 PEG_RXP9_C C254 0.1U/10V_4 PEG_RXP9 3
PEX_TX6* AM23 PEG_RXN9_C C253 0.1U/10V_4 PEG_RXN9 3
PEX_TX7 AM24 PEG_RXP8_C C226 0.1U/10V_4 PEG_RXP8 3
PEX_TX7* AM25 PEG_RXN8_C C225 0.1U/10V_4 PEG_RXN8 3
PEX_TX8 AL25 PEG_RXP7_C C252 0.1U/10V_4 PEG_RXP7 3
PEX_TX8* AK25 PEG_RXN7_C C251 0.1U/10V_4 PEG_RXN7 3
PEX_TX9 AL26 PEG_RXP6_C C224 0.1U/10V_4 PEG_RXP6 3
PEX_TX9* AM26 PEG_RXN6_C C223 0.1U/10V_4 PEG_RXN6 3
PEX_TX10 AM27 PEG_RXP5_C C250 0.1U/10V_4 PEG_RXP5 3
PEX_TX10* AM28 PEG_RXN5_C C249 0.1U/10V_4 PEG_RXN5 3
PEX_TX11 AL28 PEG_RXP4_C C222 0.1U/10V_4 PEG_RXP4 3
PEX_TX11* AK28 PEG_RXN4_C C221 0.1U/10V_4 PEG_RXN4 3
PEX_TX12 AK29 PEG_RXP3_C C219 0.1U/10V_4 PEG_RXP3 3
PEX_TX12* AL29 PEG_RXN3_C C220 0.1U/10V_4 PEG_RXN3 3
PEX_TX13 AM29 PEG_RXP2_C C248 0.1U/10V_4 PEG_RXP2 3
PEX_TX13* AM30 PEG_RXN2_C C247 0.1U/10V_4 PEG_RXN2 3
PEX_TX14 AM31 PEG_RXP1_C C218 0.1U/10V_4 PEG_RXP1 3
PEX_TX14* AM32 PEG_RXN1_C C217 0.1U/10V_4 PEG_RXN1 3
PEX_TX15 AN32 PEG_RXP0_C C245 0.1U/10V_4 PEG_RXP0 3
PEX_TX15* AP32 PEG_RXN0_C C246 0.1U/10V_4 PEG_RXN0 3

PEX_REFCLK AR16 CLK_PCIE_VGAP 9
PEX_REFCLK* AR17 CLK_PCIE_VGAN 9

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK R90 *200/J_4
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK#

PEX_RST* AM16 VGA_RST# R435 *0_4_short GPU_RST# GPU_RST# 9

R441 1 2 100K/J_4

PEX_CLKREQ* AR13 R468 10K/J_4 +3V_GPU PEX_CLKREQ# 9

PEX_TERMP AG21 PEX_TERMP R79 2.49K/F_4

TESTMODE AP35 TESTMODE R141 10K/J_4

9,39,42 GFXON

R107 0/J_4

C179 *1U/6.3V_4

+3V_GPU

R104 EV@10K/F_4
R85 EV@10K/F_4
GFXPG 9,10
Q19 MMBT3904

+1.8V_GPU R101 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C197
R80 *EV@0_4
Q17 PDTC143TT

+1.5V_GPU R72 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C147
Q12 PDTC143TT

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE

D6 RB500V-40
D5 RB500V-40

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

+1.05V_GFX_PCIE +3V

R102 *100K/F_4
R109 *390/F_4
R112 *8.2K_4
Q20 *ME2N7002E
Q21 *MMBT3904
+3V_GPU_EN
+3V_GPU_EN 44

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(PCIe)	1A
Date: Friday, October 29, 2010	Sheet 15 of 47	

U28B
fcbga973-nvidia-n12p-ge
COMMON

MEMORY I/F A

U28C
fcbga973-nvidia-n12p-ge
COMMON

MEMORY I/F C

3/18 Change to 60.4ohm

POP For Debug only

PLACE NEAR BALLS

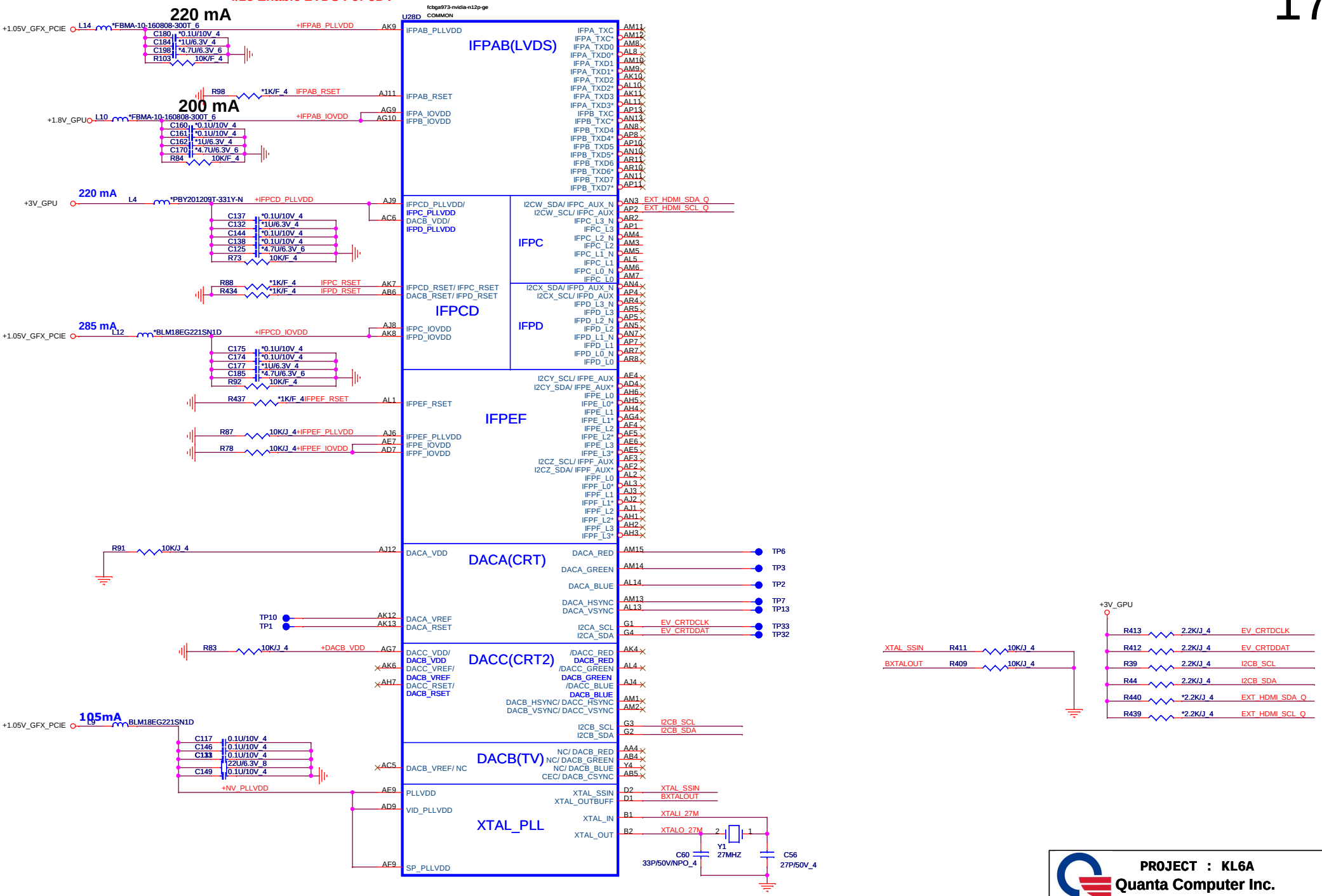
PLACE UNDER BALLS

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(MEM IF)	1A

Date: Friday, October 29, 2010 Sheet 16 of 47

4/28 Enable LVDS For 3DV



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(Display)	1A
Date: Friday, October 29, 2010	Sheet 17 of 47	

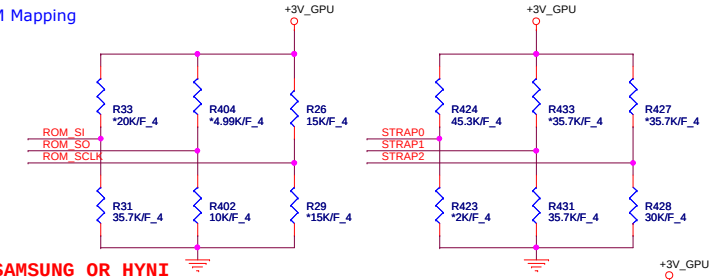
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 2GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW06	H5TQ2G63BFR-12C
0x7(0111)	800MHz 2GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT507	K4W2G1646B-HC12
0x6(0110)	900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

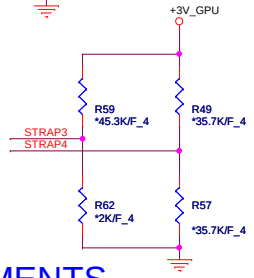
ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

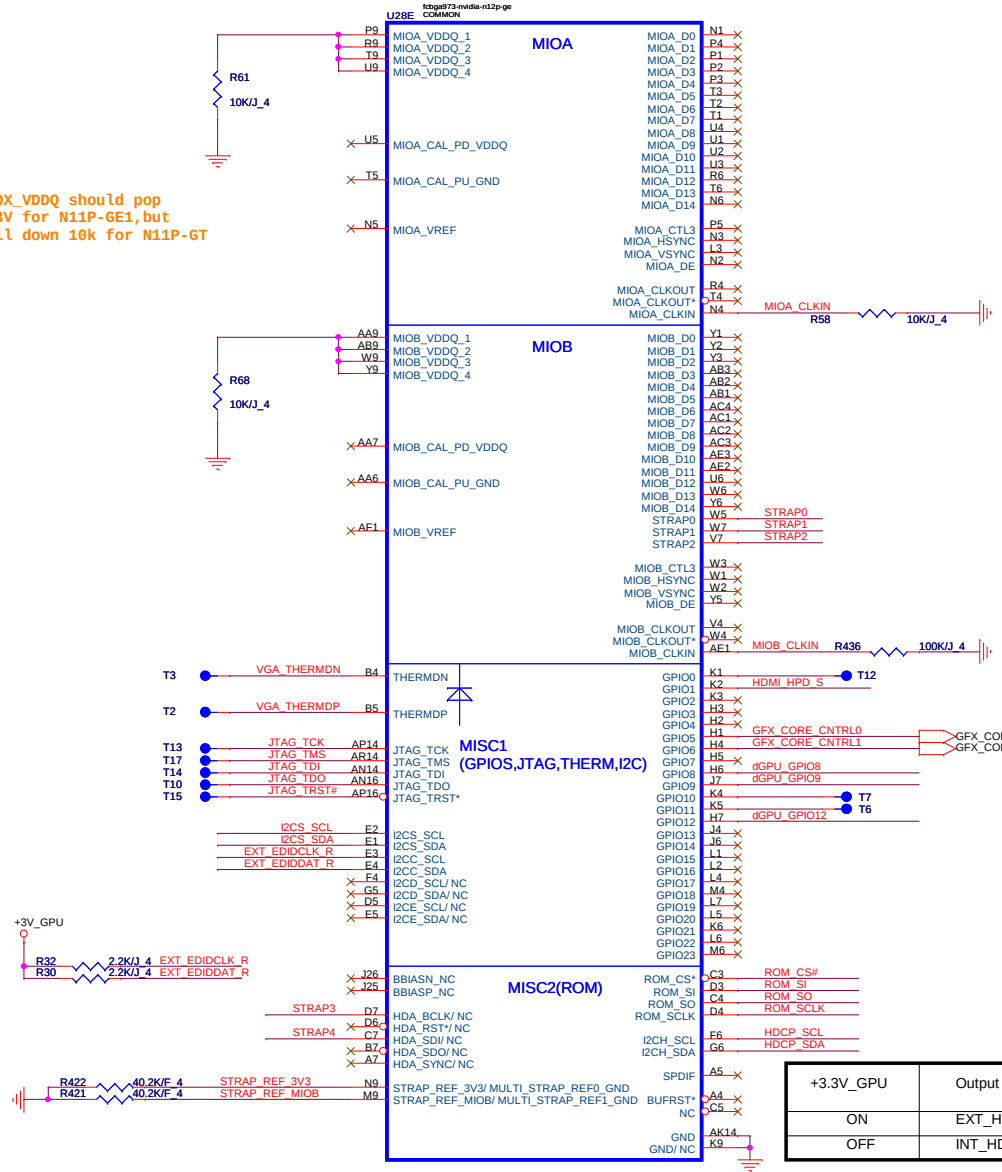


SAMSUNG OR HYNI

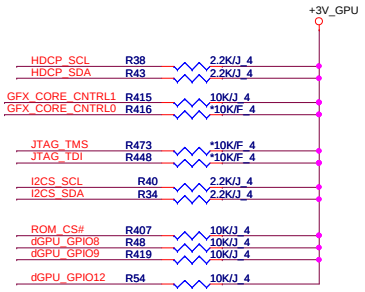
N12P-GE ROM_SO 10K pull low
Strap2 30K pull low
N12P-GV1 ROM_SO 10K pull low
Strap2 45K pull low
N12P-GV ROM_SO 10K pull high
Strap2 45K pull high
Strap3 5K pull low
Strap4 20K pull low



MIOX_VDDQ should pop 3.3V for N11P-GE1,but pull down 10k for N11P-GT



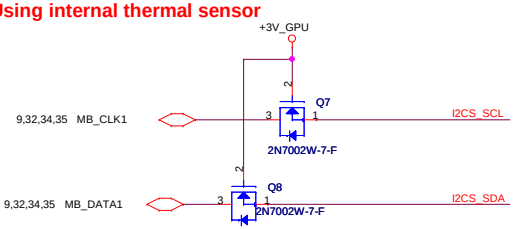
+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

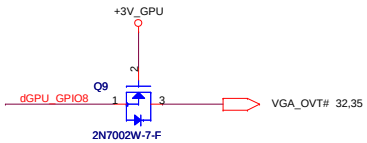


GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Using internal thermal sensor





PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(GPIO/STRAP)	1A

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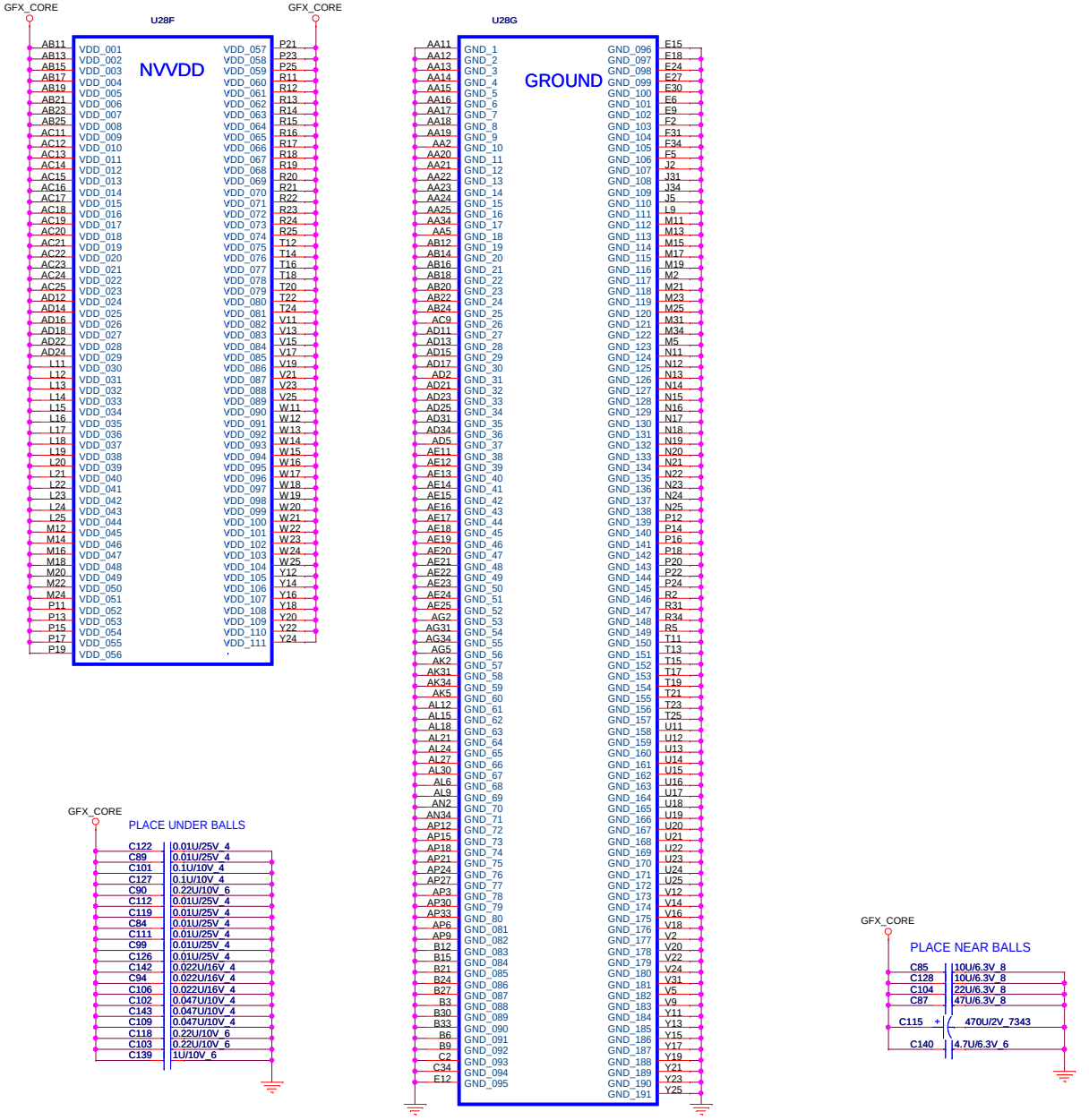


PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(POWER)	1A

Date: Friday, October 29, 2010 Sheet 19 of 47

16 VMA_DQ[63..0]
16 VMA_DM[7..0]
16 VMA_WDQS[7..0]
16 VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

U4 / U27 / U7 / U29 — 96-BALL SDRAM DDR3 K4W1G1646E-HC11

Should be 240 Ohms +-1%

R67 240/F_4 · R410 240/F_4 · R97 240/F_4 · R430 240/F_4

+1.5V_GPU

R417 1.33K/F_4 · R414 1.33K/F_4 · VREFC_VMA1 · C518 0.01U/25V_4

R52 1.33K/F_4 · R45 1.33K/F_4 · VREFD_VMA1 · C70 0.01U/25V_4

C123 *10U/6.3V_6

R77 1.33K/F_4 · R86 1.33K/F_4 · VREFC_VMA3 · C159 0.01U/25V_4

R425 1.33K/F_4 · R426 1.33K/F_4 · VREFD_VMA3 · C529 0.01U/25V_4

Placement has to be close to VRAM

R405 162/F_4 · VMA_CLKP0 · VMA_CLKN0

R95 162/F_4 · VMA_CLKP1 · VMA_CLKN1

C528	C65	C168	C145	C531
C186	C7	C15	C234	C235
C133	C535			

C572	C526	C527	C533	C532
C71	C523	C524	C574	C573
C236	C194			

C32	C48	C52	C55	C507
C100	C525	C59	C88	C58
C114	C176			

C510	C520	C513	C514	C72
C4	C5	C515	C519	C522
C183	C516			

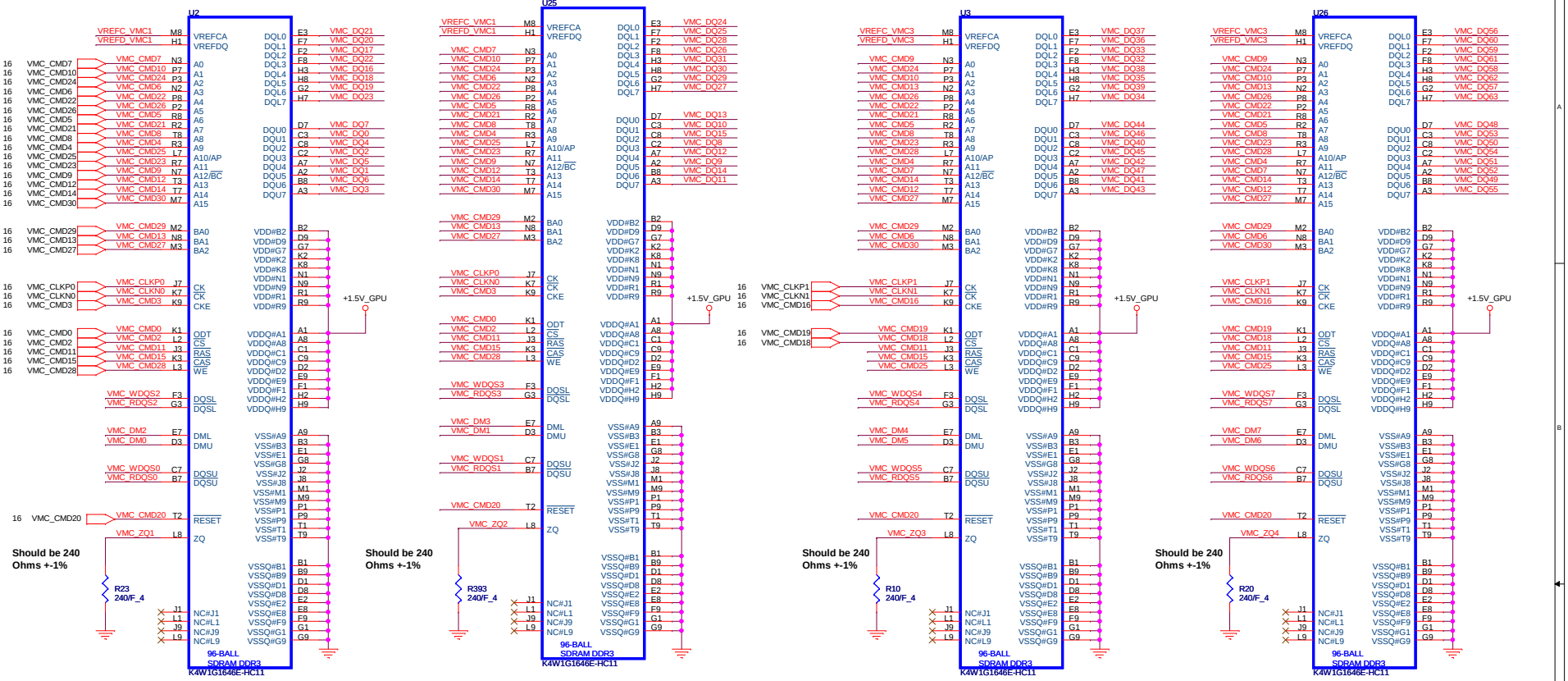
All 1U/6.3V_4

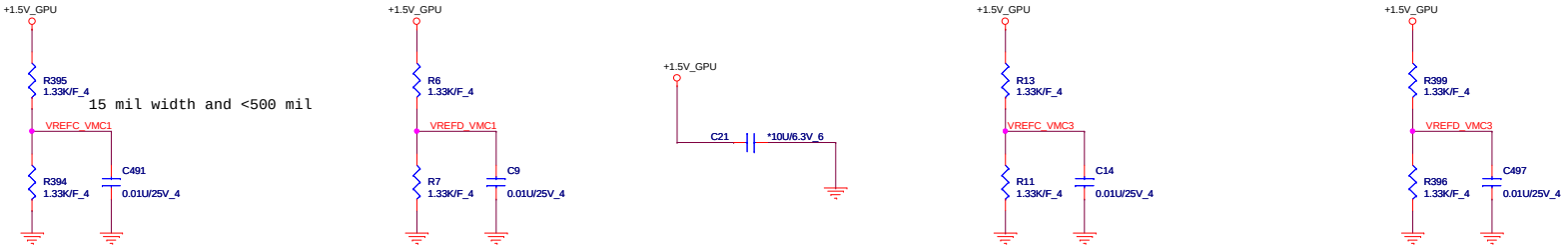
PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(VRAM-1)	1A
Date: Friday, October 29, 2010	Sheet 20 of 47	

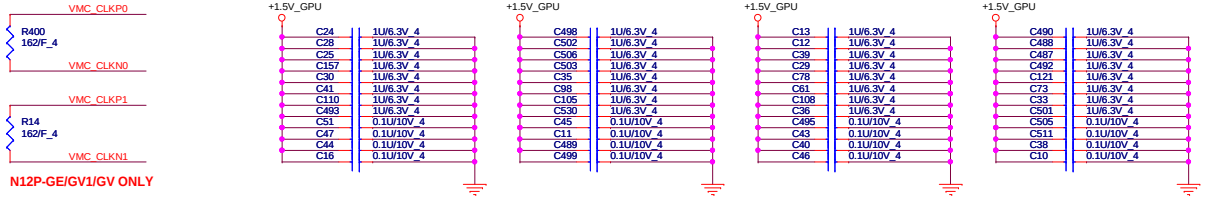
CHANNEL B: 512MB/1024MB DDR3

16 VMC_DQ[63..0]
16 VMC_DM[7..0]
16 VMC_WDQS[7..0]
16 VMC_RDQS[7..0]

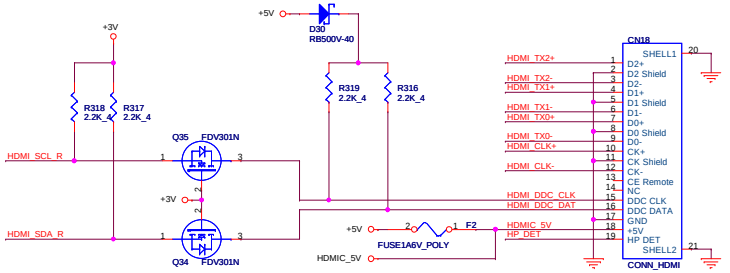




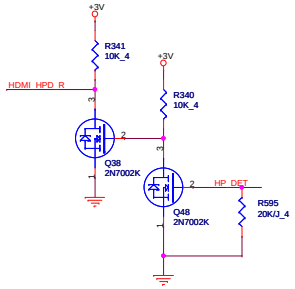
Placement has to be close to VRAM

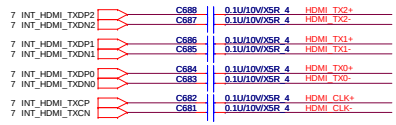


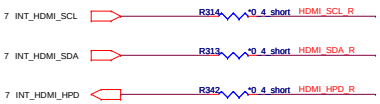
PROJECT : KL6A		
Quanta Computer Inc.		
Size	Document Number: VGA-N12P GB2-128(VRAM-2)	Rev: 1A
Date: Friday, October 29, 2010	Sheet 21 of 47	

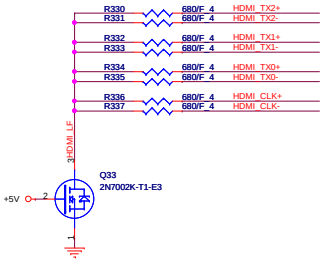


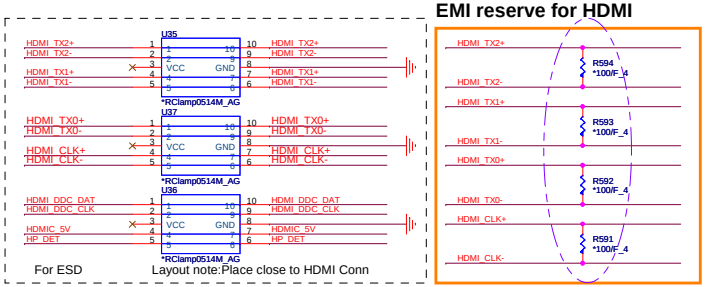
HDMI Hot-PLUG to EC and GPU











EMI reserve for HDMI

7,8,11,23,26,27,32,33,34,35,36,37,38,45 +5V
7,8,9,10,11,13,14,15,23,24,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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Layout Note:
Setting R,G,B trace impedance to 50 ohm.

7 INT_CRT_RED
7 INT_CRT_GRE
7 INT_CRT_BLU
L23 BLM18BA470SN1
L22 BLM18BA470SN1
L21 BLM18BA470SN1
CRT_R1
CRT_G1
CRT_B1
R230 150/F_4
R225 150/F_4
R215 150/F_4
C305 5.6P/50V/COG_4
C291 5.6P/50V/COG_4
C285 5.6P/50V/COG_4
C284 5.6P/50V/COG_4
C292 5.6P/50V/COG_4
C306 5.6P/50V/COG_4
TP19
CRT_VCC
D26 RB500V-40
C617 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
C274 *VARISTOR_4
CRT_VCC_R
CN14 CRT_CONN

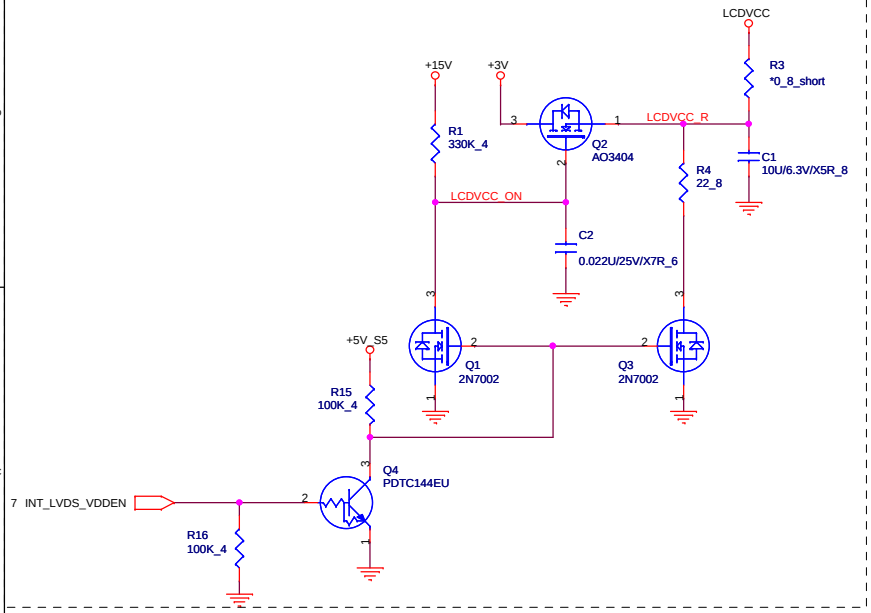
7 INT_CRT_VSYNC
7 INT_CRT_HSYNC
+5V
U14 AHCT1G125DCH
U16 AHCT1G125DCH
C286 0.1U/10V/X5R_4
VGAVSYNC_R
VGAHSYNC_R
R188 10_4
R203 10_4
Place near U37,U38 < 200 mil
CRTVSYNC1
CRTHSYNC1
C275 *10P/50V/COG_4
C265 *10P/50V/COG_4
L16 HB-1T1608-121JT
L20 HB-1T1608-121JT
CRTVSYNC
CRTHSYNC
C277 10P/50V/COG_4
C264 10P/50V/COG_4
Place near CN5002 connector < 200 mil

+3V
R567 2.2K_4
R553 2.2K_4
CRT_VCC
R564 4.7K_4
R540 4.7K_4
7 INT_DDCCLK
7 INT_DDCDAT
Q43 2N7002K-T1-E3
Q44 2N7002K-T1-E3
DDCCLK
DDCDAT
C610 *10P/50V/COG_4
C587 *10P/50V/COG_4

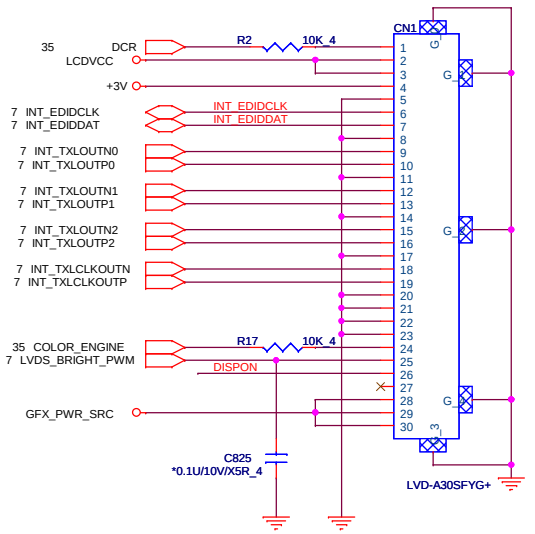
ESD PROTECTION
D21 *TVSS5VESPT CRT_R1
D20 *TVSS5VESPT CRT_G1
D18 *TVSS5VESPT CRT_B1
D15 *TVSS5VESPT CRTVSYNC
D16 *TVSS5VESPT CRTHSYNC
D25 *TVSS5VESPT DDCCLK
D27 *TVSS5VESPT DDCDAT

PROJECT : KL6A
Quanta Computer Inc.
Size Custom | Document Number CRT CONN | Rev 1A
Date: Friday, October 29, 2010 | Sheet 23 of 47

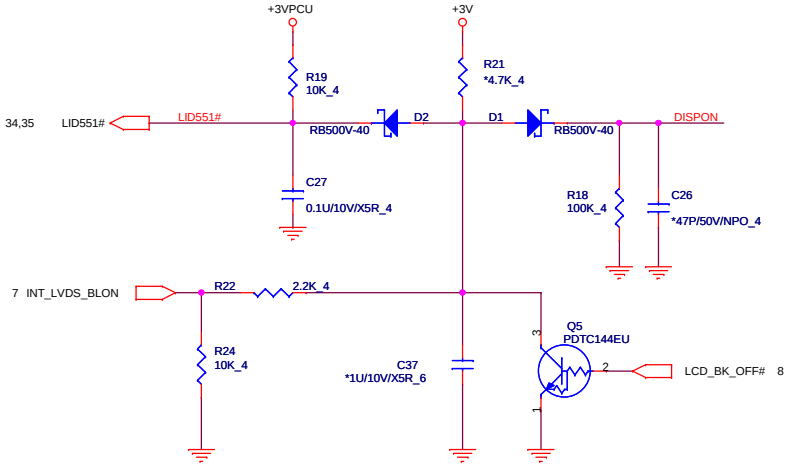
LCDVCC

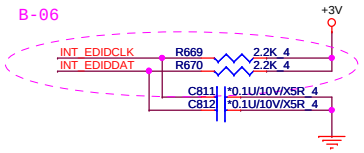


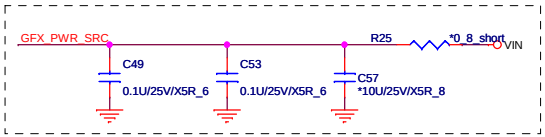
7,8,9,10,11,13,14,15,22,23,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V
27,28,29,37,39,40,41,44 +15V
7,8,25,27,33,34,35,37,38,40,41 +3VPCU
36,38,39,40,42,43,44,45 VIN



back light







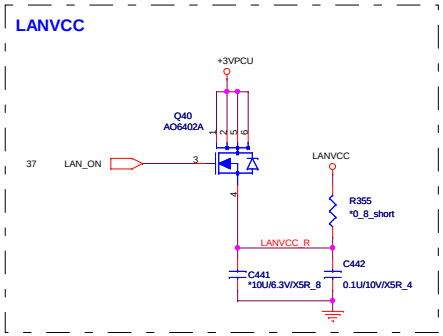
PROJECT : KL6A

Quanta Computer Inc.

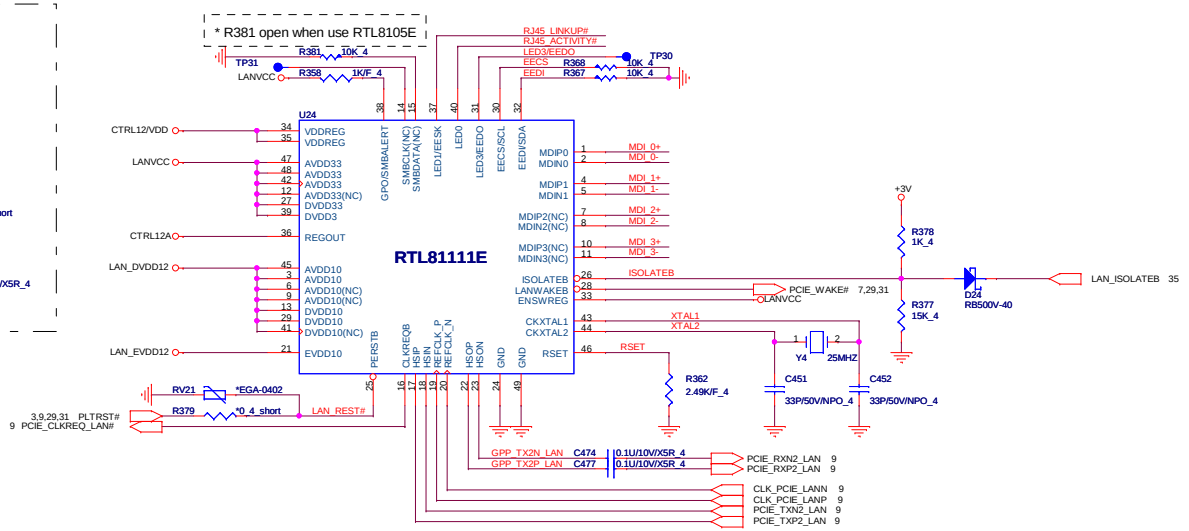
Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Friday, October 29, 2010 Sheet 24 of 47

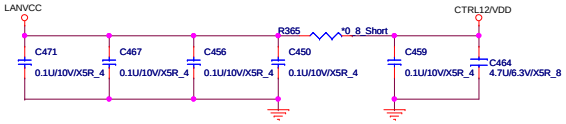
LANVCC



* R381 open when use RTL8105E

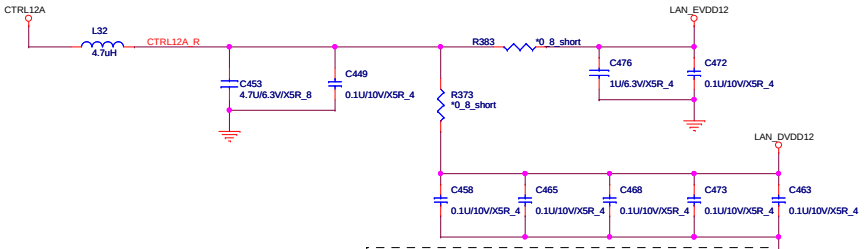


* C476 and C472 are for U24 LAN_EVDD12 pin 21.



* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

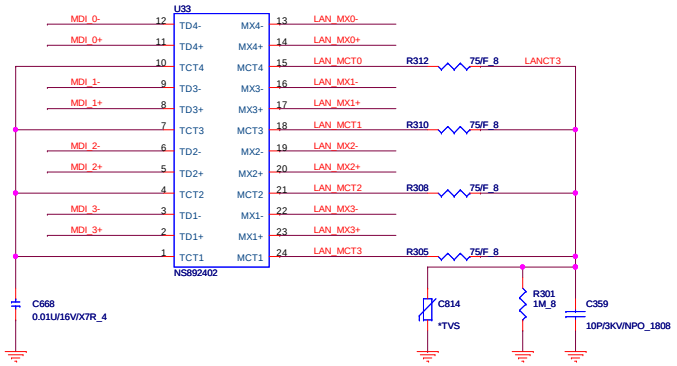
Place C5113 ,C5094 closed to U5006 pins44,45.



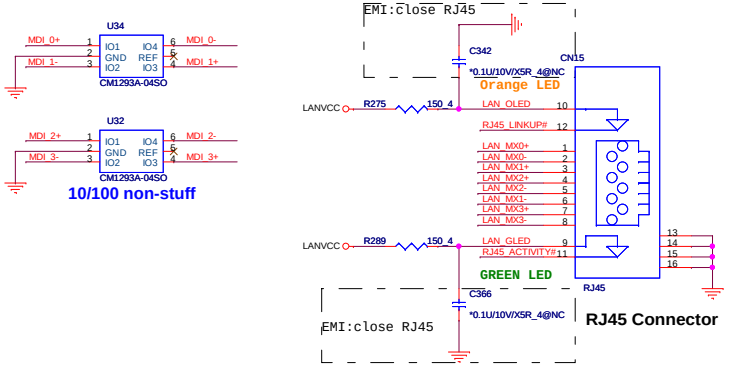
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout:All termination signal should have 20 mil trace

Tramsformer



RJ45 Connector

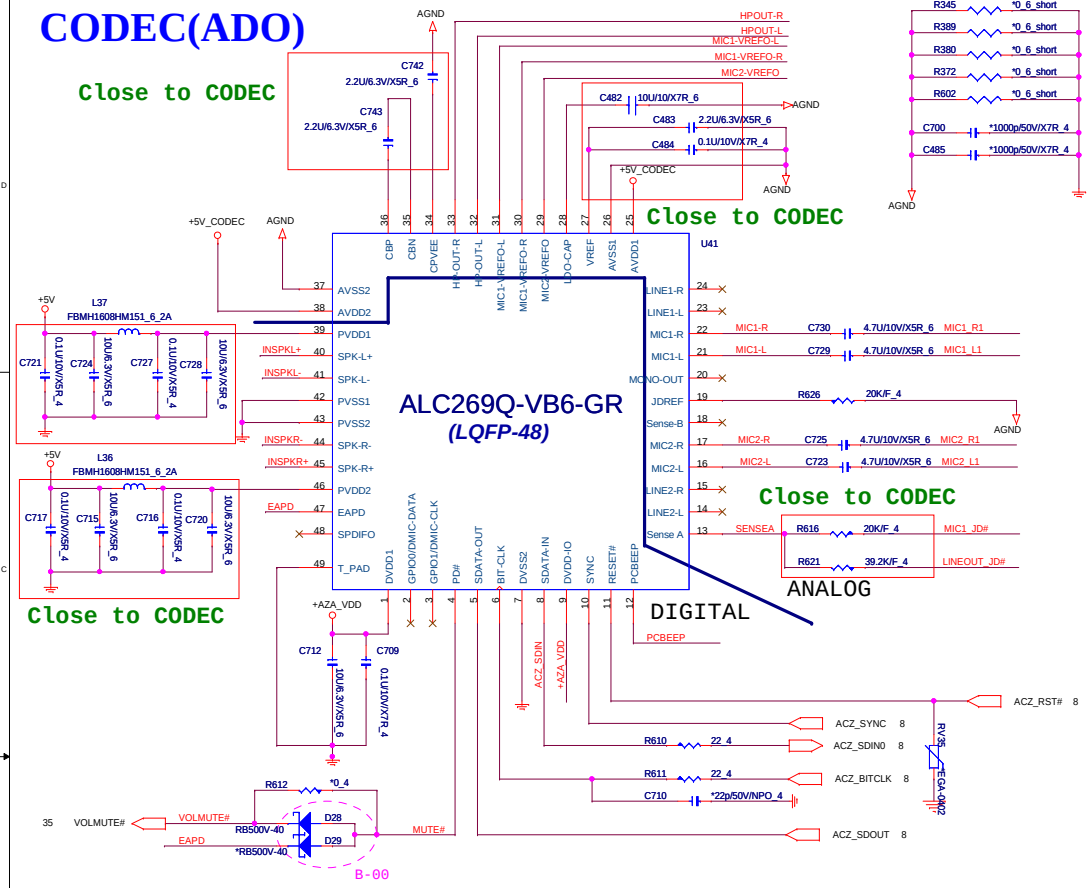


PROJECT : KL6A
Quanta Computer Inc.

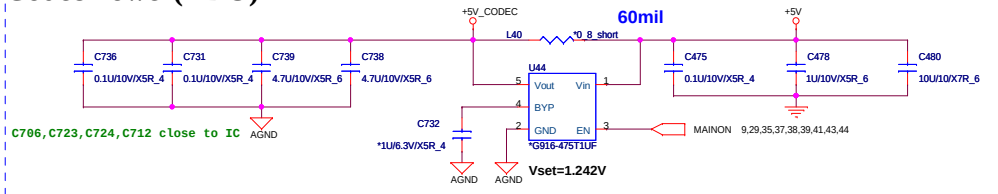
Size	Document Number	Rev
Custom	RTL8111EL-VB	1A

Date: Friday, October 29, 2010 Sheet 25 of 47

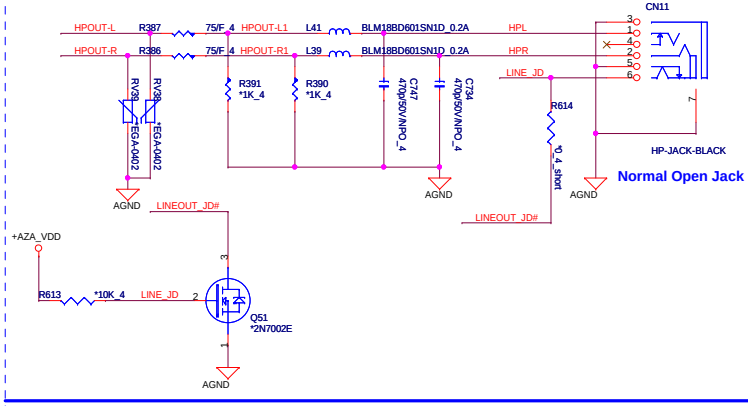
CODEC(ADO)



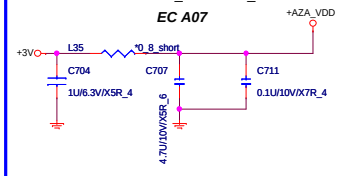
Codec Power(ADO)



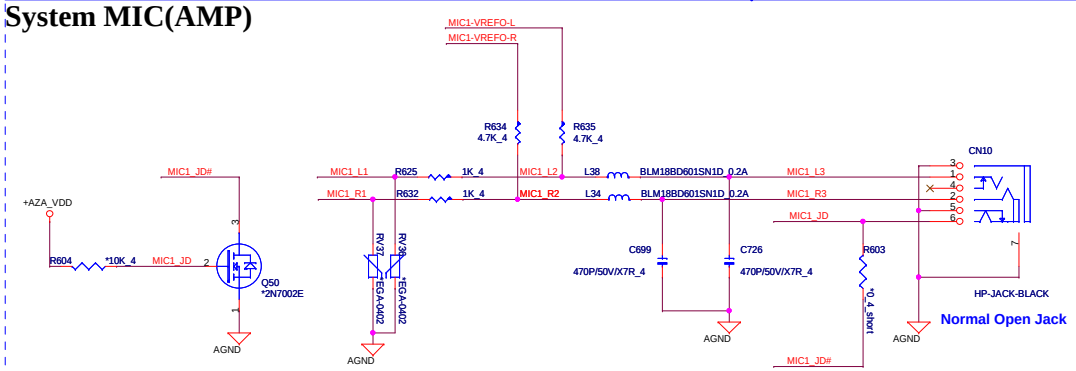
Earphone(AMP)



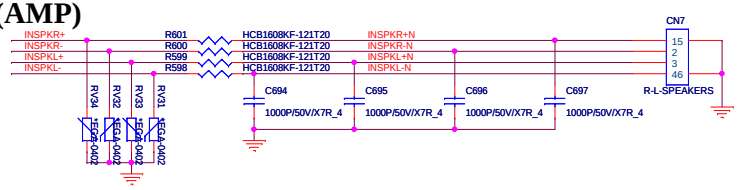
HDA Power(ADO)



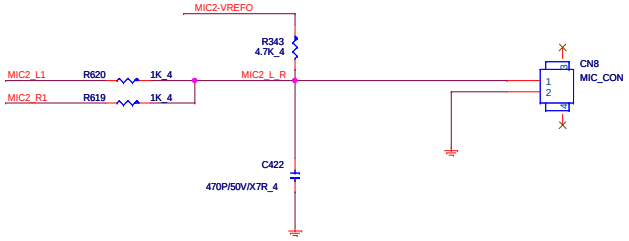
System MIC(AMP)



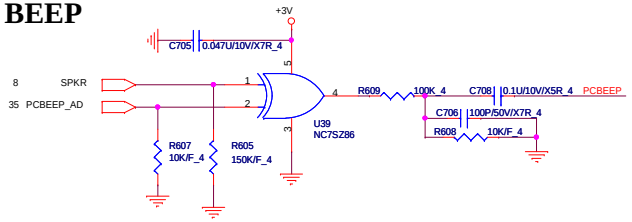
Speaker(AMP)



INTERNAL MIC



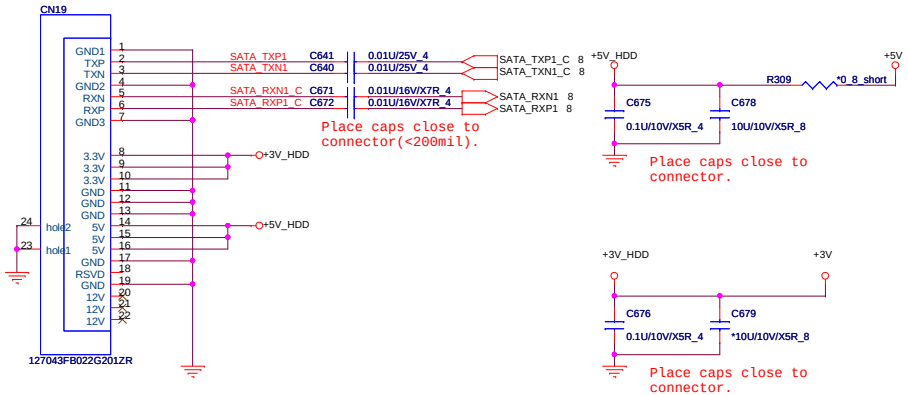
PC BEEP



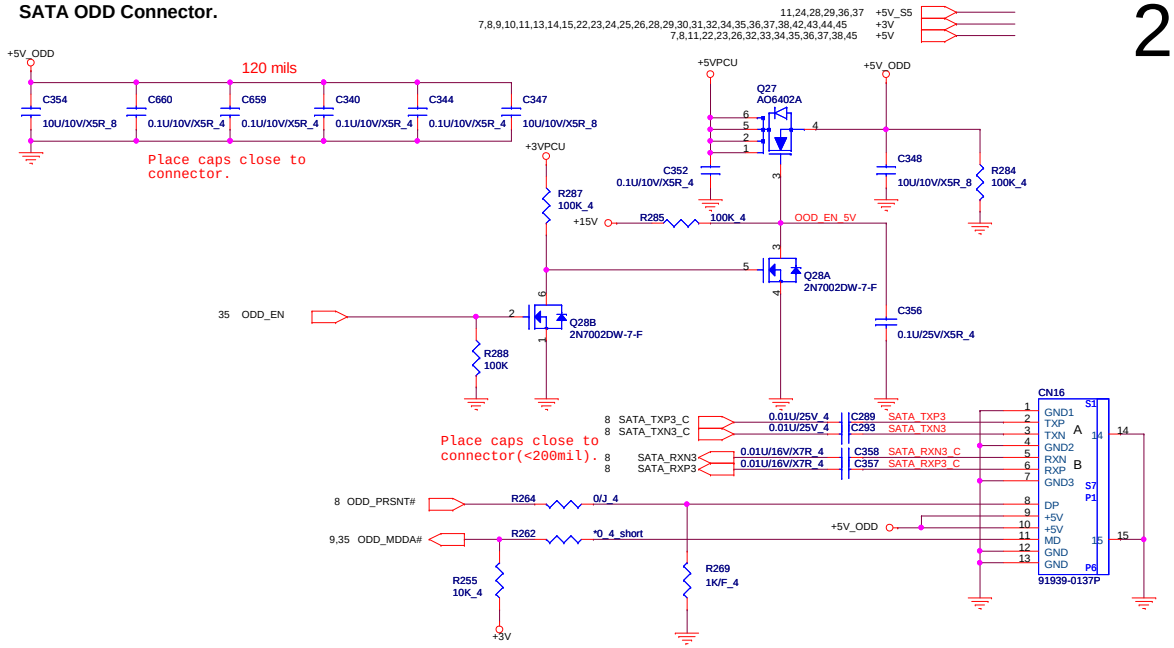
PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A
Date: Friday, October 29, 2010	Sheet 26 of 47	

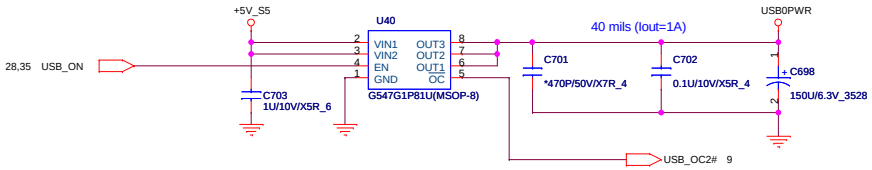
SATA HDD Connector.

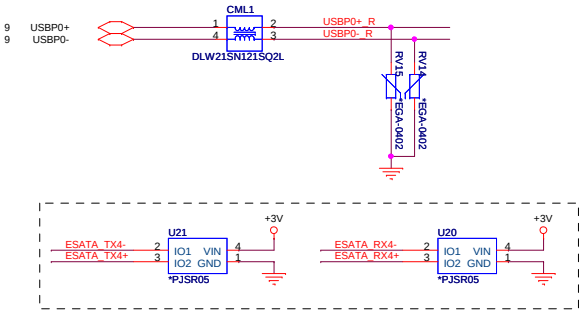


SATA ODD Connector.

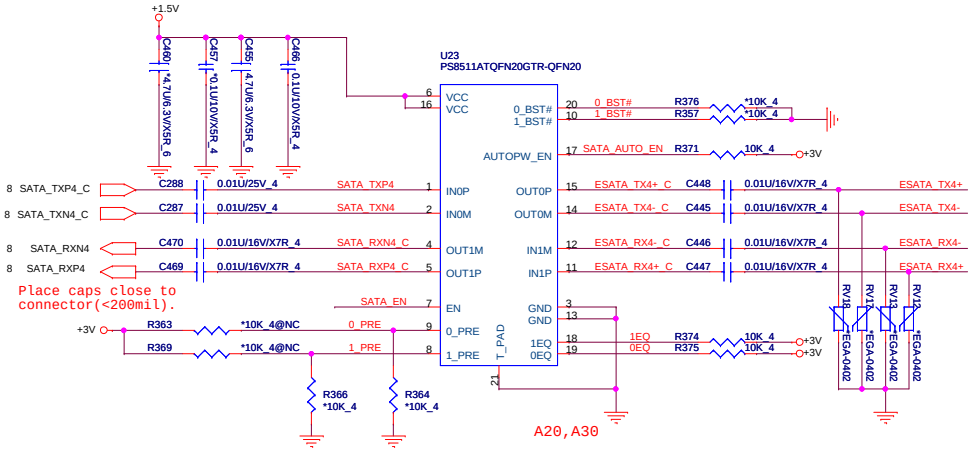


USB + E-SATA





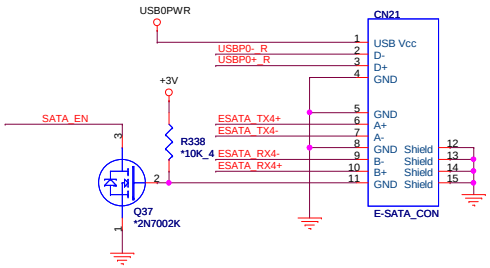
E-SATA RE-DRIVER



All straps of PS8511A have int. PL 150Kohm.

EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB 0



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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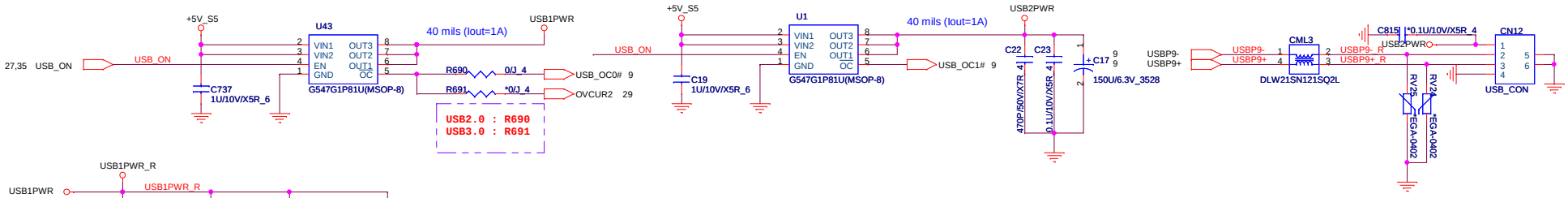
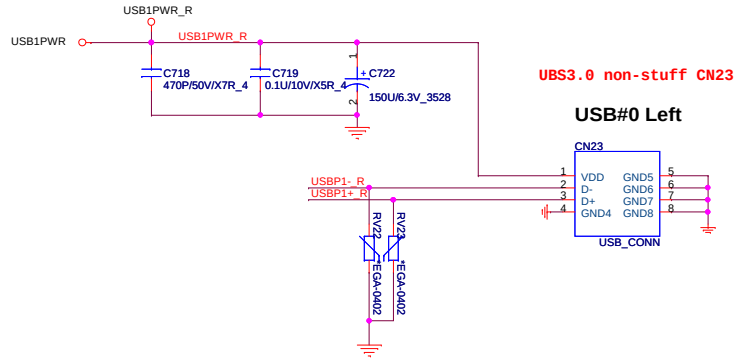
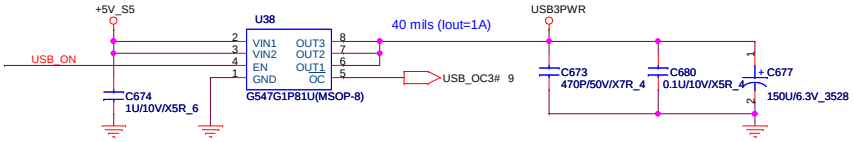
11,24,27,29,36,37 +5V_S5
7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V
24,27,29,37,39,40,41,44 +15V

USB2.0*3

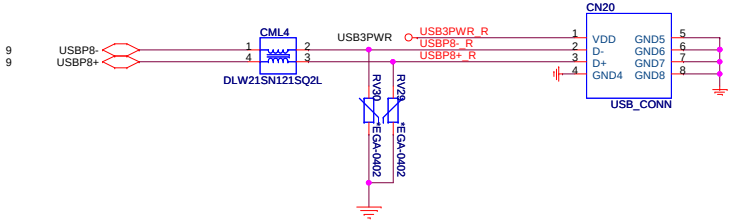
USB#1 Daughter board

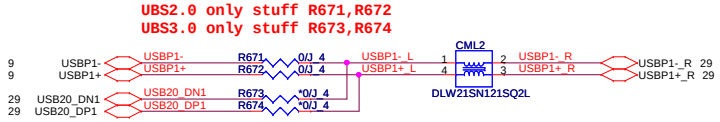




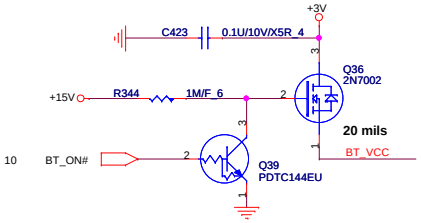


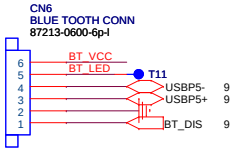
USB#2 Right





BLUETOOTH





PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	BT/USBX3	1A

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REAR USB PORT X1

USB3.0 PORT1

SUY USB3.0: DFHS09FR063

C754, C752 close to CN24

SPI Flash ROM

Copy From ZN7

U47

VL800 / VL801 QFN88
VL800 4PORT
VL801 2PORT

For debug only.
Don't connect to system SMBus

Near PCIEx Slot

Remove power for VL801

ESD

*RClamp0544.TBT
msop10-4_9-5

X'tal 25MHz

25MHz/20pF/30ppm

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

For USB3.0

Remove SUSD turn on switch (From PCU to SUS)
(Used +3V_S5 power plane)

Power circuit (+1.05_SUS)

For USB3.0

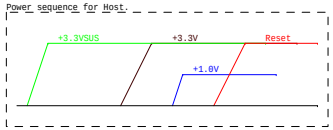
Vout =0.8(1+R1/R2)

For +3V_SUS (Power for wake up)

For +3V_RUN

For +1.05_SUS (Power for wake up)

Power sequence for Host.



PROJECT :	KL6A
Quanta Computer Inc.	
Size: C	Document Number: USB3.0 *1
Rev: 1A	
Date: Friday, October 29, 2010	Sheet 29 of 47

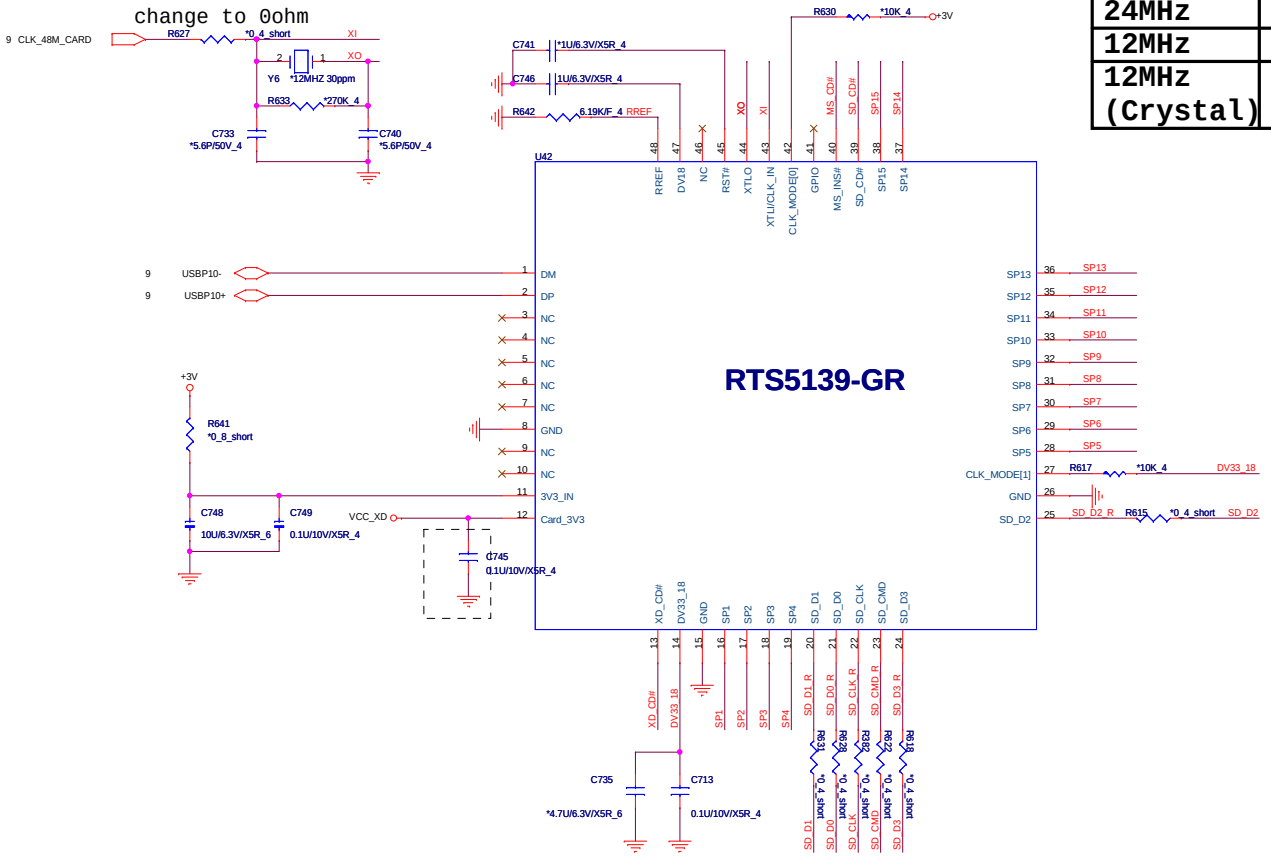
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

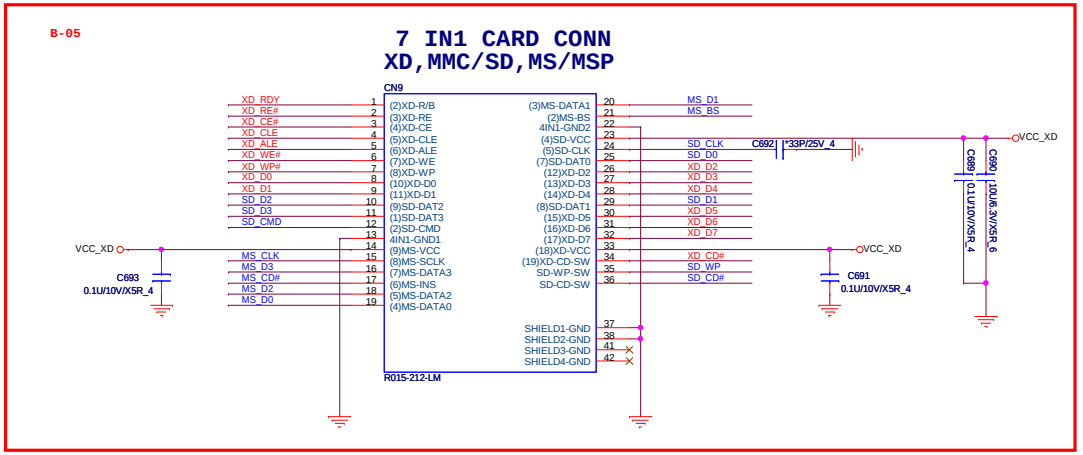
Note:

SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139

SD,MS 4bit only





PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

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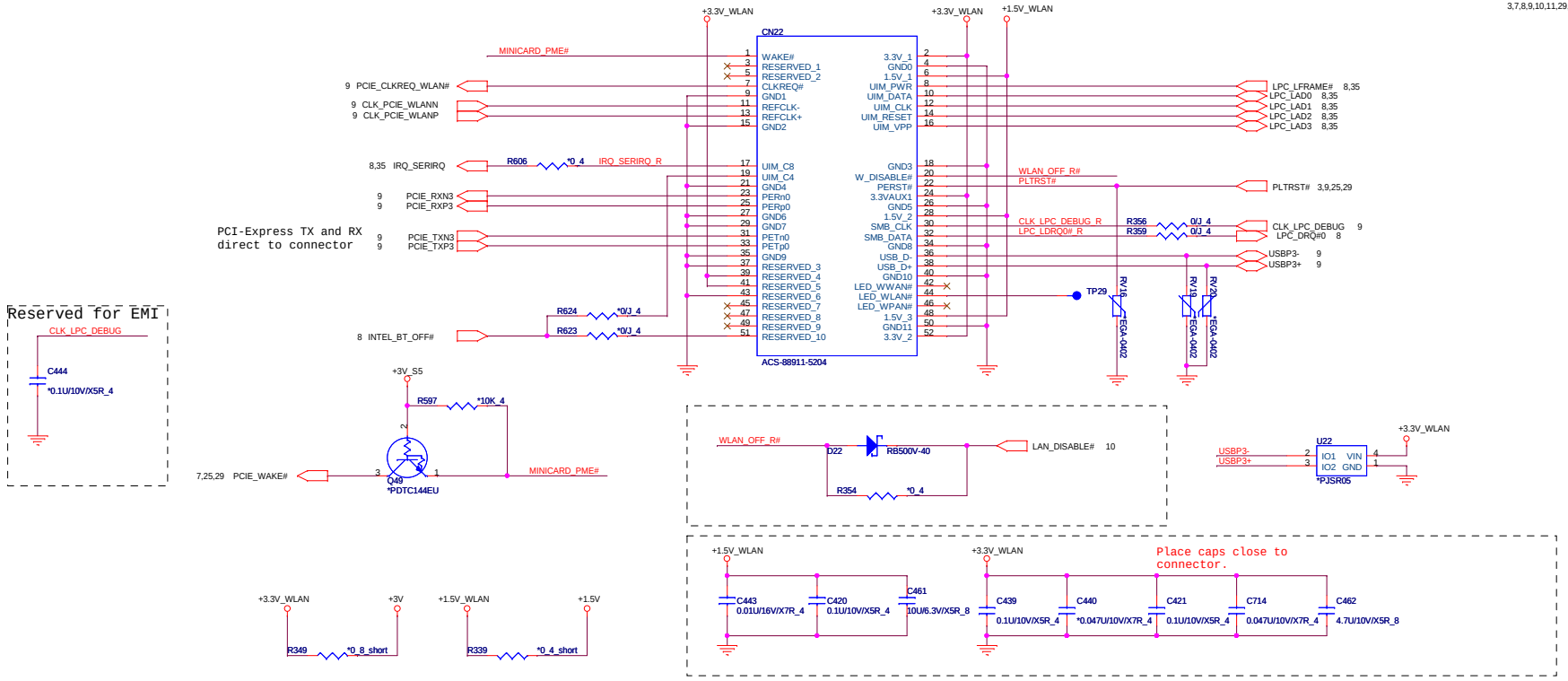
MiniCard WLAN connector

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,32,34,35,36,37,38,42,43,44,45 +3V
11,27,37 +1.5V
3,7,8,9,10,11,29,34,37 +3V_S5

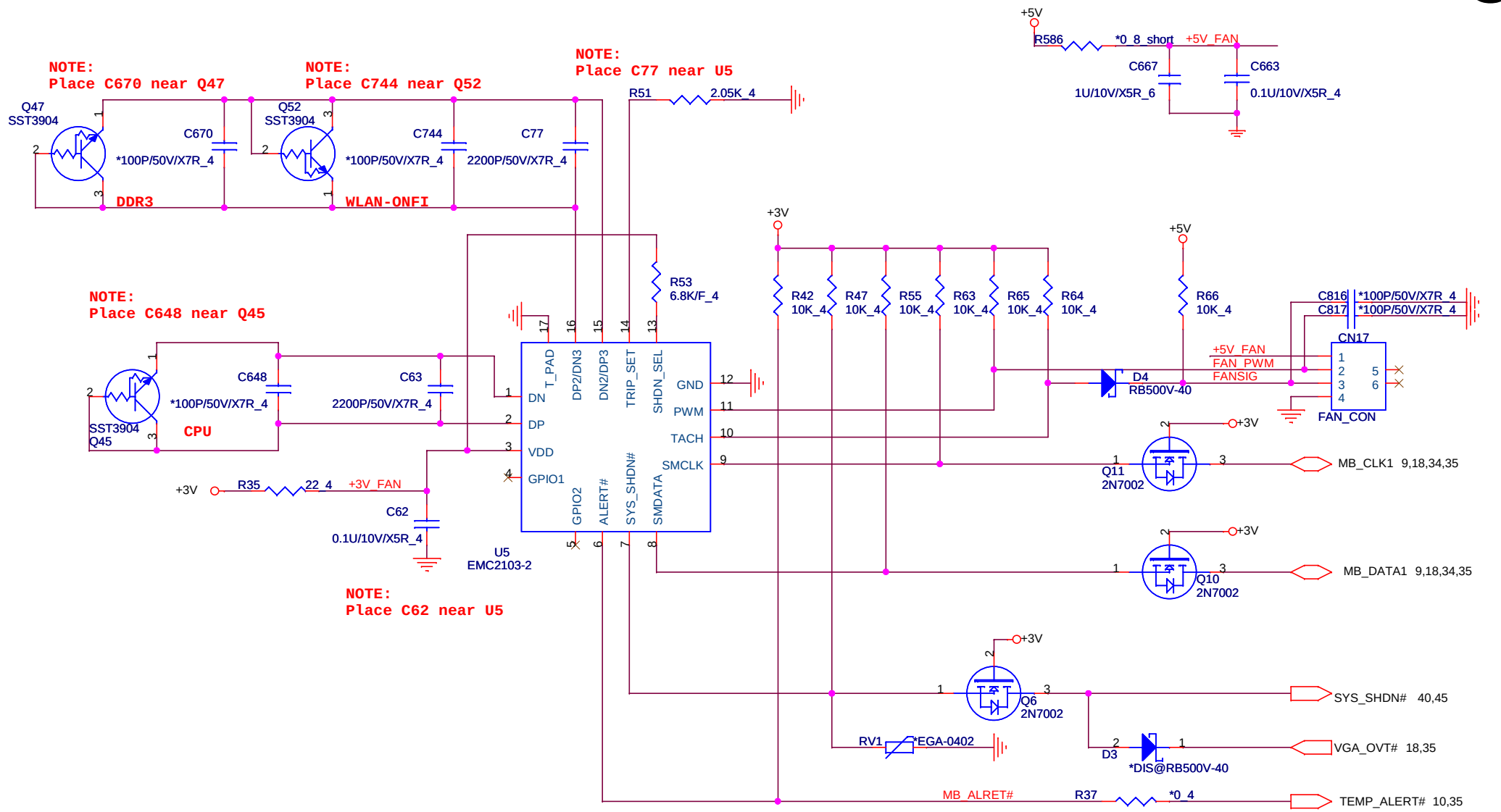


PROJECT :	KL6A
Quanta Computer Inc.	
Size: Custom	Document Number: MINI-Card WLAN
Rev:	1A
Date: Friday, October 29, 2010	Sheet 31 of 47

FAN CONTROL

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,34,35,36,37,38,42,43,44,45 +3V
7,8,11,22,23,26,27,33,34,35,36,37,38,45 +5V

32



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A

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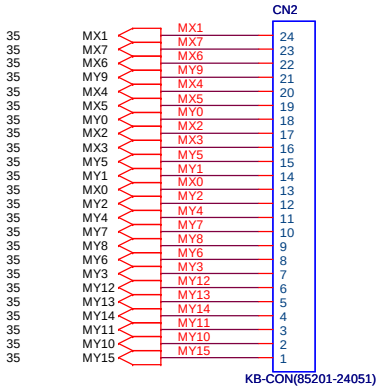
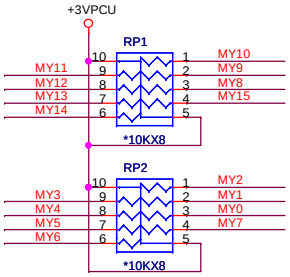
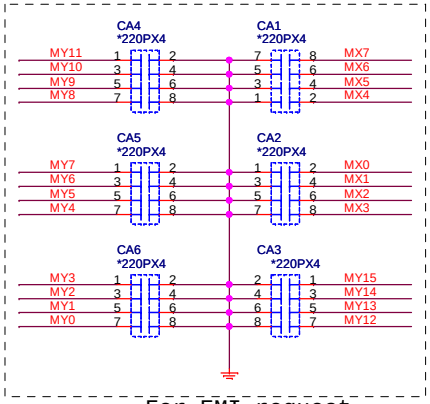
KEYBOARD

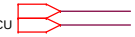




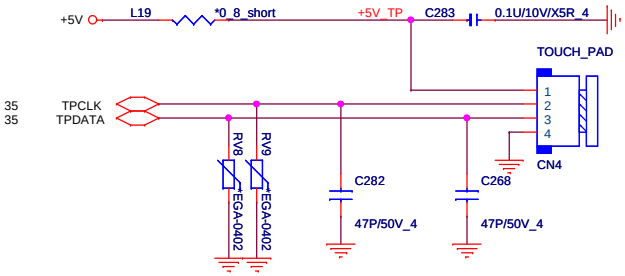


For EMI request

7,8,11,22,23,26,27,32,34,35,36,37,38,45 +5V
7,8,24,25,27,34,35,37,38,40,41 +3VPCU



Touch pad



PROJECT : KL6A			
Quanta Computer Inc.			
Size: Custom	Document Number: K/B, T/P		Rev: 1A
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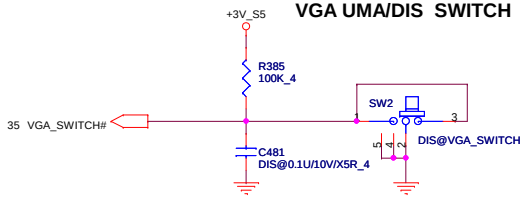
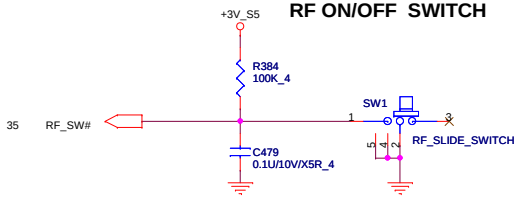
3,7,8,9,10,11,29,31,37 +3V_S5
7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,32,35,36,37,38,42,43,44,45 +3V

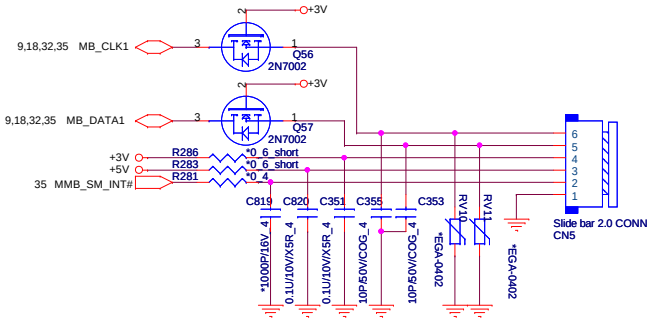
VGA UMA/DIS SWITCH



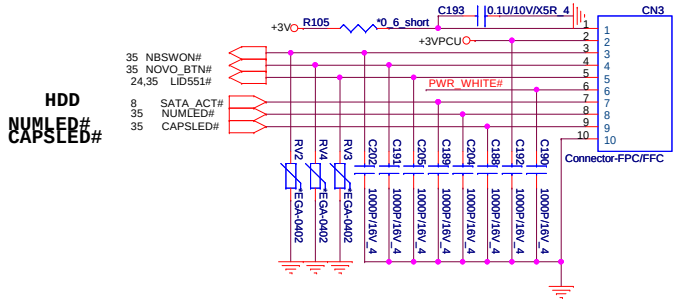
RF ON/OFF SWITCH



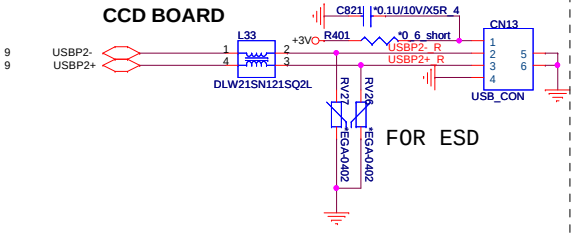
CAPACITANNCE BUTTON BOARD



POWER BOARD



CCD BOARD



PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: B TO B CON/LED	Rev: 1A
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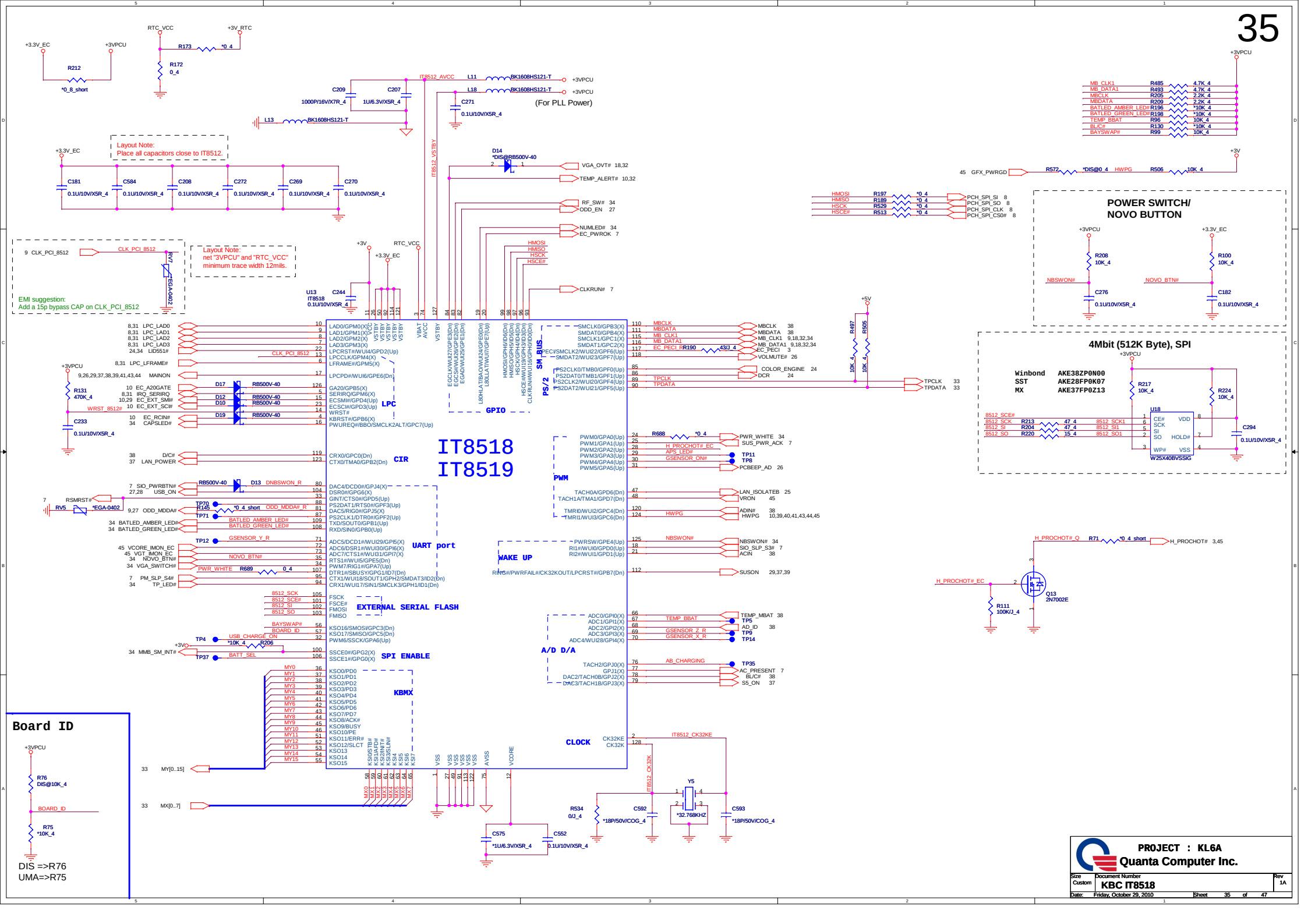
IT8518
IT8519
LPC
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
CIR
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512
(For PLL Power)
POWER SWITCH/
NOVO BUTTON
4Mbit (512K Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
Board ID
DIS =>R76
UMA=>R75
PROJECT : KL6A
Quanta Computer Inc.
KBC IT8518
Date: Friday, October 29, 2010
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Screw for ME

WLAN

HOLE18 H-TC217BC142D102P2

HOLE19 H-TC217BC75I75D35P2

SMT NUT H=4/7mm

VGA

HOLE16 DIS@H-TC5_5BC4I3D3P2

HOLE17 DIS@H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

CPU BKT

HOLE9 *C142D102N

HOLE15 AGND *HG-TC276BC315D106P2

HOLE13 *HG-TC276BC315D106P2

HOLE12 *HG-TC276BC315D106P2

HOLE11 *HG-TC276BC315D106P2

HOLE14 *HG-TC276BC315D106P2

HOLE8 *HG-TC276BC315D106P2

HOLE5 *HG-TC276BC315D106P2

HOLE6 *HG-TC276BC315D106P2

HOLE4 *H-TC276BC315D106P2

HOLE3 *H-TC276BC315D106P2

HOLE2 *H-TC276BC315D106P2

HOLE10 *H-BS236X150D59PB

HOLE7 *H-BC197D59PB

HOLE20 *Spad-re1010x45np

HOLE21 *Spad-re1010x45np

HOLE22 *spad-kl6-1np

HOLE23 *spad-kl6-2np

HOLE24 *spad-re160x774np

HOLE25 *spad-re225x460np

EMI suggestion

VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	+5V	+VCC_GFX	+VCC_GFX
C367	C54	C31	C415	C296	C20	C406	C405	C50	C807	C808	C809
*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	2200P/50V/X7R_4

B-08

+5V_S5		+3V	+3V		+1.05V_PCH	+1.05V_PCH		+1.5V_SUS	GFX_CORE		VIN
SC822	*0.1U/25V/X5R_4	SC823	*0.1U/25V/X5R_4			SC824	*0.1U/25V/X5R_4		SC825	*0.1U/25V/X5R_4	
SC826	*0.1U/25V/X5R_4	SC827	*0.1U/25V/X5R_4			SC828	*0.1U/25V/X5R_4		SC829	*0.1U/25V/X5R_4	
SC830	*0.1U/25V/X5R_4	SC831	*0.1U/25V/X5R_4			VIN		+3V			
SC832	*0.1U/25V/X5R_4	SC833	*0.1U/25V/X5R_4			SC834	*0.1U/25V/X5R_4		+VCC_CORE		VIN
SC869	*0.1U/25V/X5R_4	SC870	*0.1U/25V/X5R_4			SC838	*0.1U/25V/X5R_4		SC835	*0.1U/25V/X5R_4	
VIN		+1.5V_SUS		+3V		SC841	*0.1U/25V/X5R_4		SC837	*0.1U/25V/X5R_4	
SC839	0.1U/25V/X5R_4	SC840	*0.1U/25V/X5R_4			SC844	*0.1U/25V/X5R_4		+5V_S5		+1.5V_SUS
SC842	0.1U/25V/X5R_4	SC843	*0.1U/25V/X5R_4			SC847	*0.1U/25V/X5R_4		SC854	*0.1U/25V/X5R_4	
SC845	0.1U/25V/X5R_4	SC846	*0.1U/25V/X5R_4			SC850	*0.1U/25V/X5R_4		VIN		+5V
SC848	0.1U/25V/X5R_4	SC849	*0.1U/25V/X5R_4			+5V		+5V_S5	SC866	*0.1U/25V/X5R_4	
SC851	0.1U/25V/X5R_4	SC852	*0.1U/25V/X5R_4			SC865	*0.1U/25V/X5R_4				
SC855	*0.1U/25V/X5R_4	SC856	*0.1U/25V/X5R_4			SC868	*0.1U/25V/X5R_4				
SC857	0.1U/25V/X5R_4	SC858	*0.1U/25V/X5R_4								
SC859	*0.1U/25V/X5R_4	SC860	*0.1U/25V/X5R_4			HDMIC_5V			SC872	*0.1U/25V/X5R_4	
SC861	0.1U/25V/X5R_4	SC862	*0.1U/25V/X5R_4			SC876	*0.1U/25V/X5R_4		SC873	*0.1U/25V/X5R_4	
SC863	0.1U/25V/X5R_4	SC864	*0.1U/25V/X5R_4						SC874	*0.1U/25V/X5R_4	
		SC867	*0.1U/25V/X5R_4						SC875	*0.1U/25V/X5R_4	

ESD suggestion

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLD & SKEW	1A

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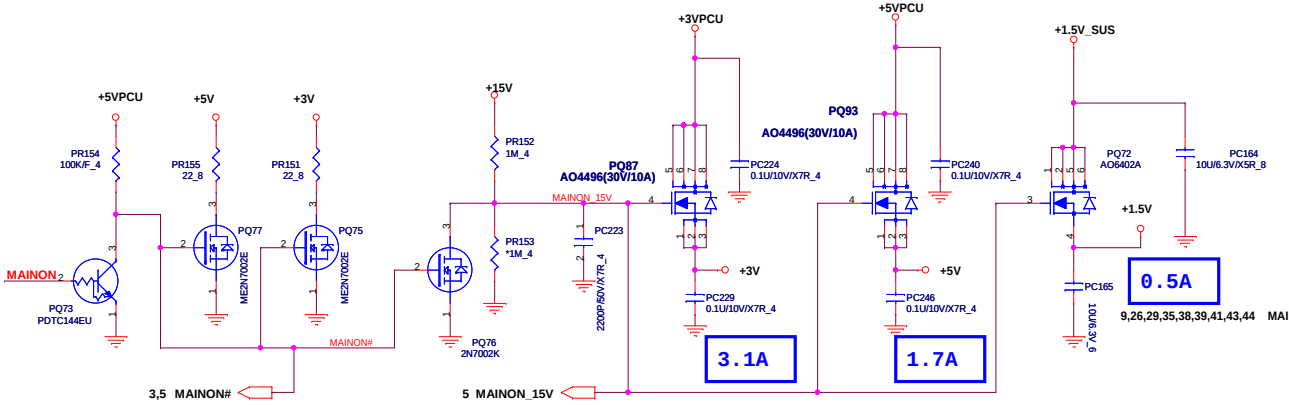
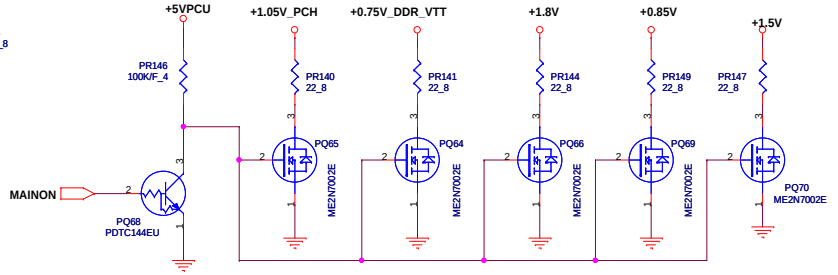
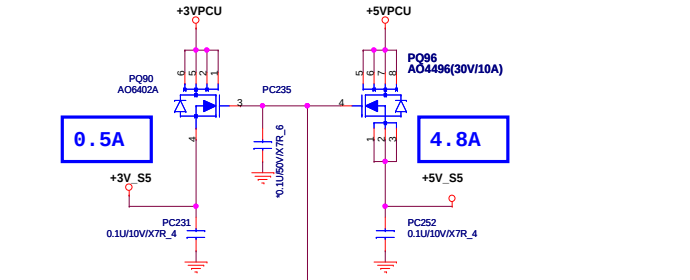
DISCHARGE

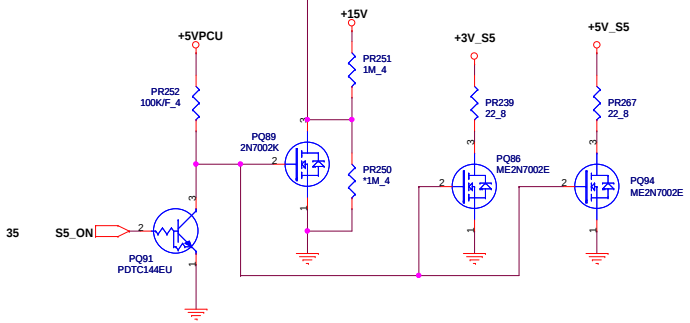
+3V, +5V,+1.5V

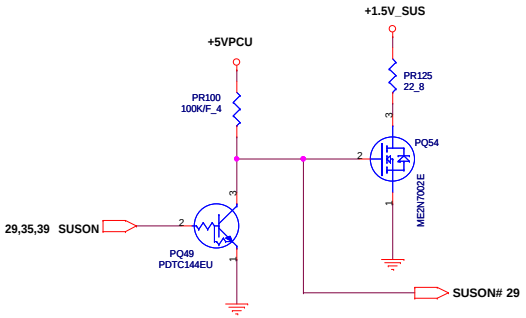




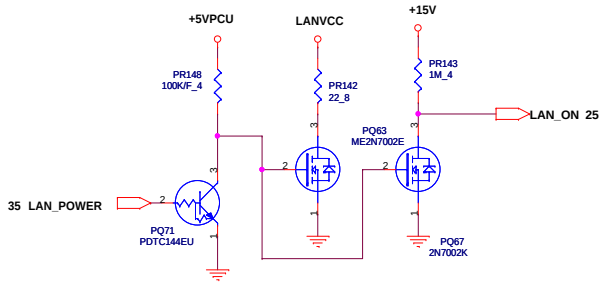
3V_S5, 5V_S5

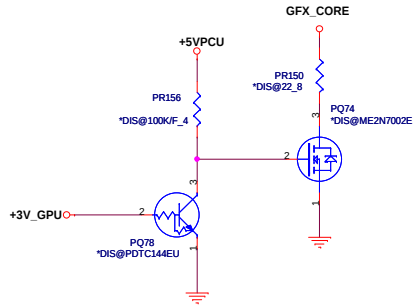






LANVCC





PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: Discharge	Rev: 1A
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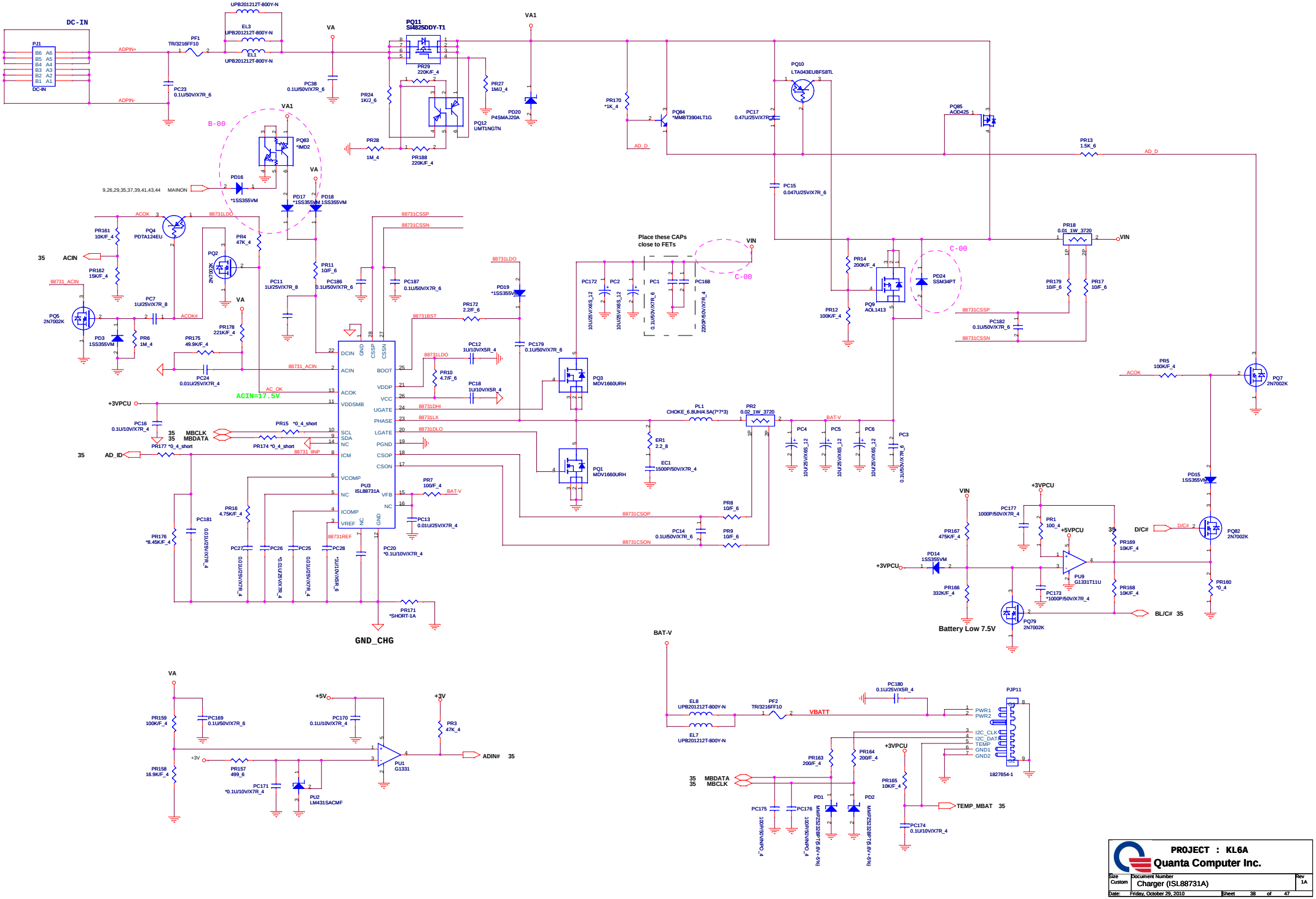
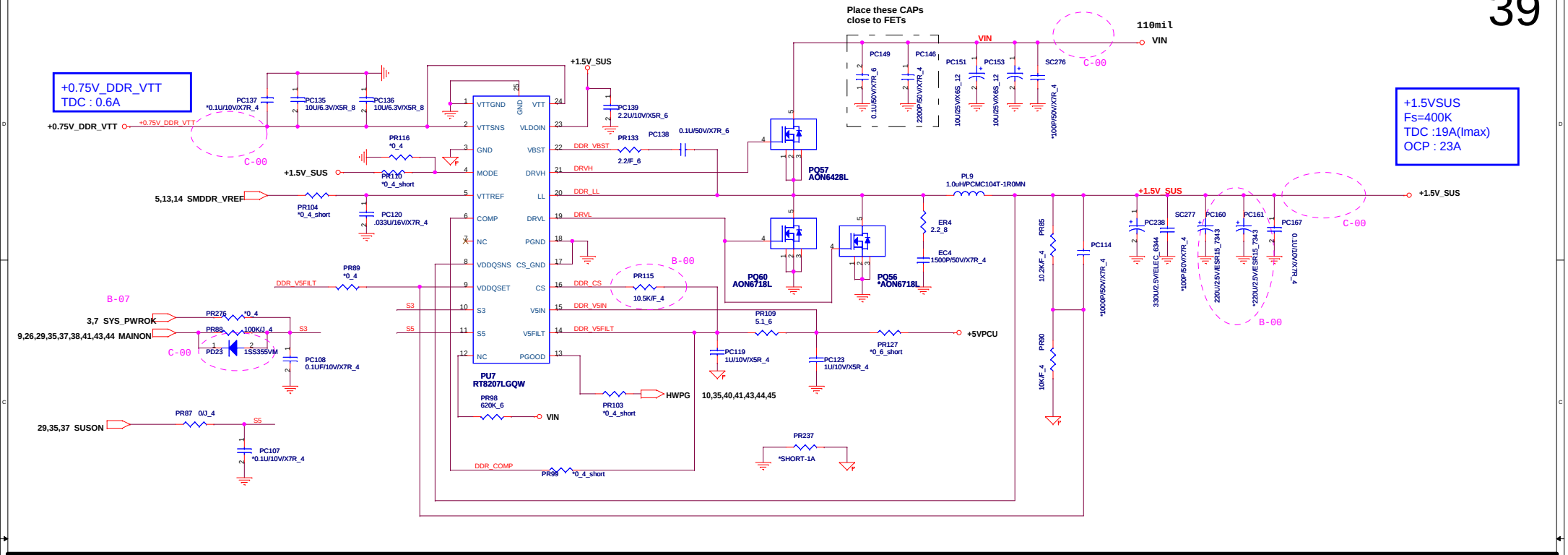
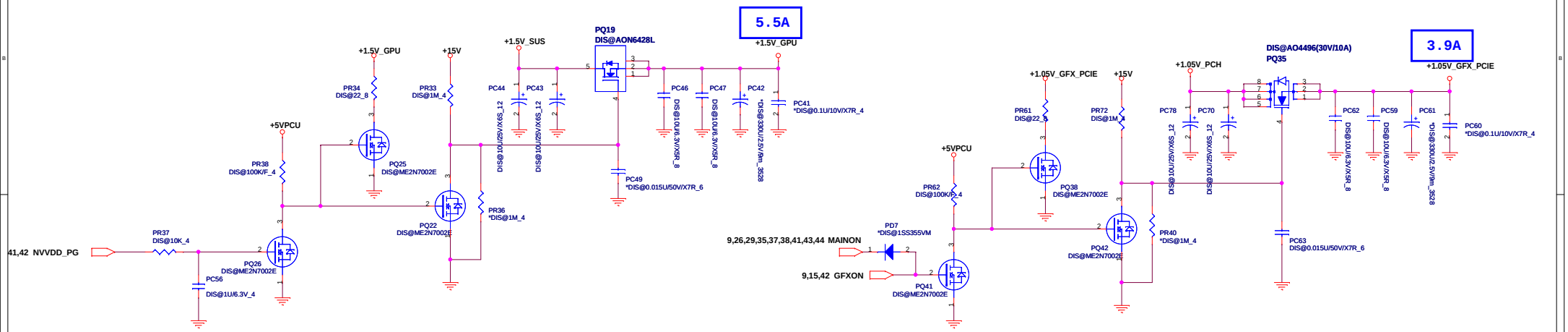


PROJECT : KL6A			
Quanta Computer Inc.			
Size: Custom	Document Number: Charger (ISL88731A)		Rev: 1A
Date: Friday, October 29, 2010	Sheet 38 of 47		





PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207LGQW)	1A
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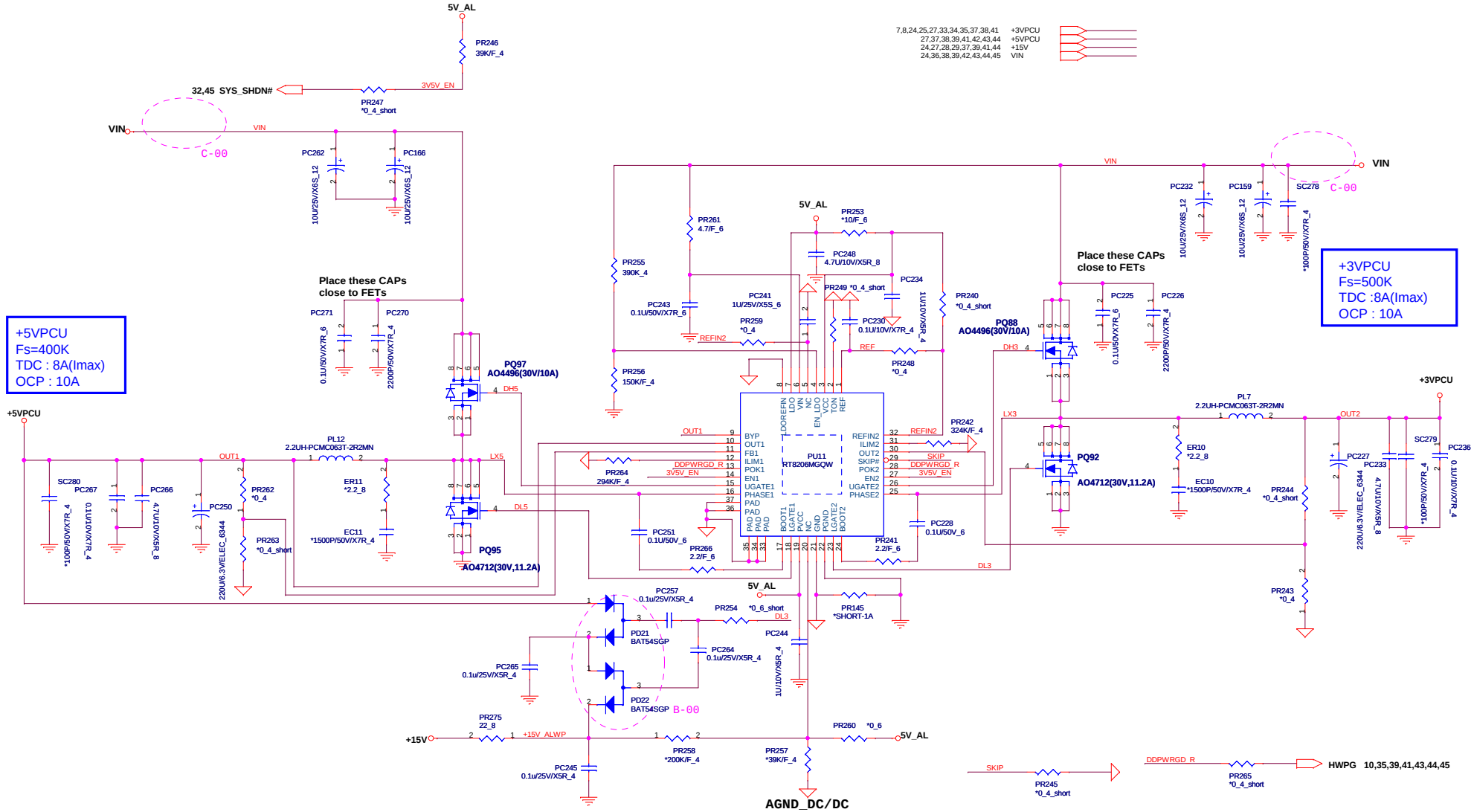

PROJECT : KL6A			
Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (RT8206MGQW)		Rev: 1A
Date: Friday, October 29, 2010	Sheet 40 of 47		

+1.8V
TDC : 2.3A

+3VPCU
C-00
+3VPCU_1.8V
PC268 10U/6.3V_8
PC269 0.1U/10V_4

PU12 HPA00835RTER
16 VIN
1 VIN
2 VIN
15 EN
14 PWRGD
7 COMP
8 RT/CLK
9 SS
10 PH
11 PH
12 PH
13 BOOT
6 VSNS
3 GND
4 GND
5 AGND
PAD 22 21 20 19 18 17

PL10
1UH/11A-PCMD063T-1R0MN
+1.8V
C-00
PR270 *0_6_short
PC254 0.1U/25V_4

9,26,29,35,37,38,39,43,44 MAINON
PR272 0/J_4
PC259 *0.01U/50V_4
10,35,39,40,43,44,45 HWPG
PC256 *100P/50V_4
PR271 15K/F_4
PC261 1200p/50V_4
PR269 182K/F_4
PC253 0.01U/50V_4
HPA00835-1.8_VFB

R1 PR273 127K/F_4
R2 PR274 100K/F_4
PC247 0.1U/10V_4
PC237 10U/6.3V_8
SC281 *100P/50V/X7R_4
PC242 10U/6.3V_8

V0=0.8*(R1+R2)/R2

0.3A

+1.8V_GPU
+15V
+1.8V
DIS@AO6402A
PQ47
+1.8V_GPU
PR86 DIS@22_8
PR77 DIS@1M_4
PC105 DIS@0.1U/10V_4
PC104 DIS@0.1U/10V_4
+5VPCU
PR114 DIS@100K/F_4
PQ53 DIS@ME2N7002E
PQ51 DIS@ME2N7002E
PR76 *DIS@1M_4
PC106 *DIS@2200P/50V_4
39,42 NVVDD_PG
PR124 DIS@0/J_4
PC128 *DIS@0.1U/10V_4
PQ52 DIS@ME2N7002E

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (HPA00835RTER)	1A
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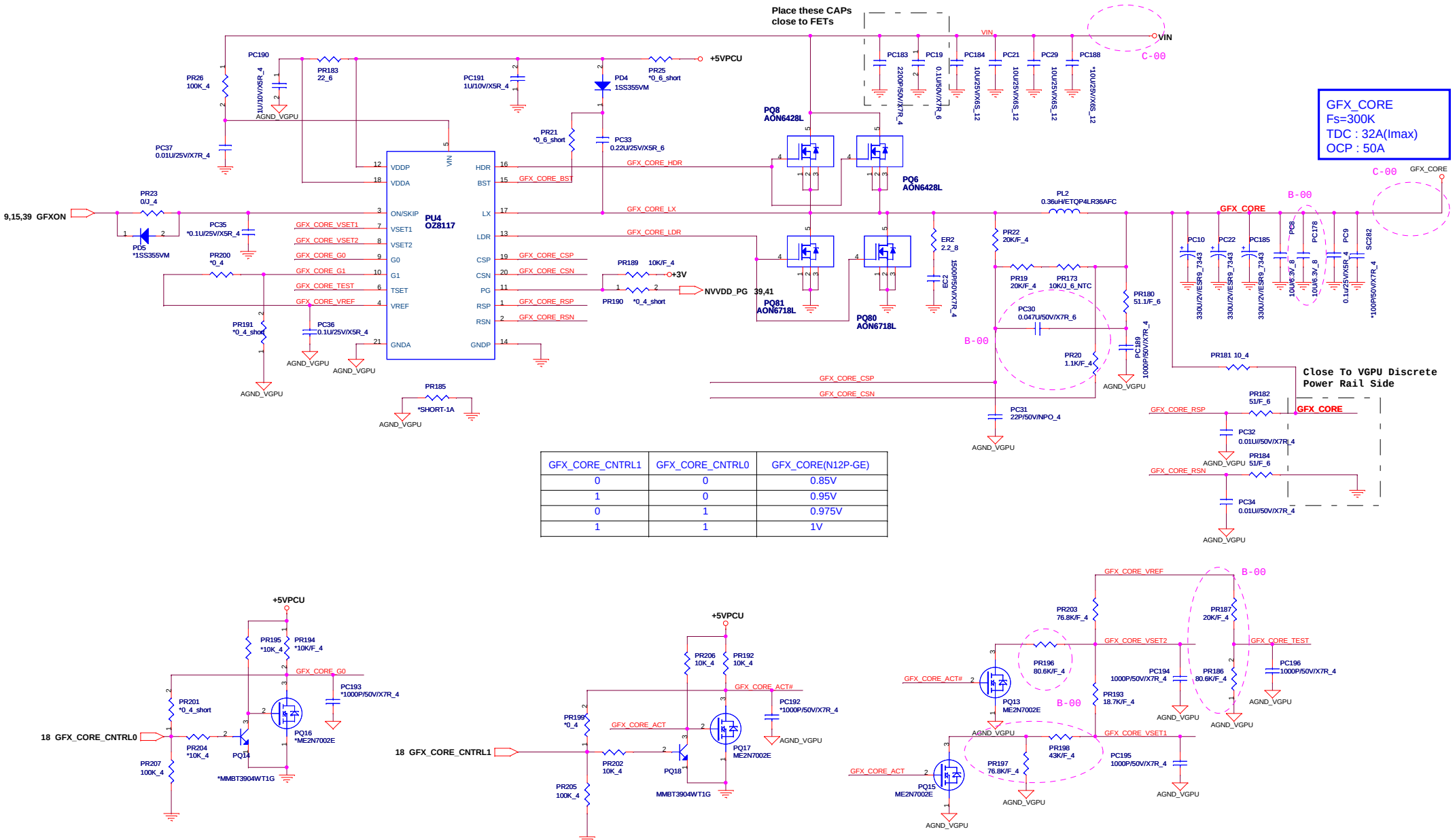

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	GFX_CORE(N12P-GE)
0	0	0.85V
1	0	0.95V
0	1	0.975V
1	1	1V

Quanta Computer Inc.	PROJECT : KL6A	
Size	Document Number: +VGPU_CORE (OZ8117)	Rev: 1A
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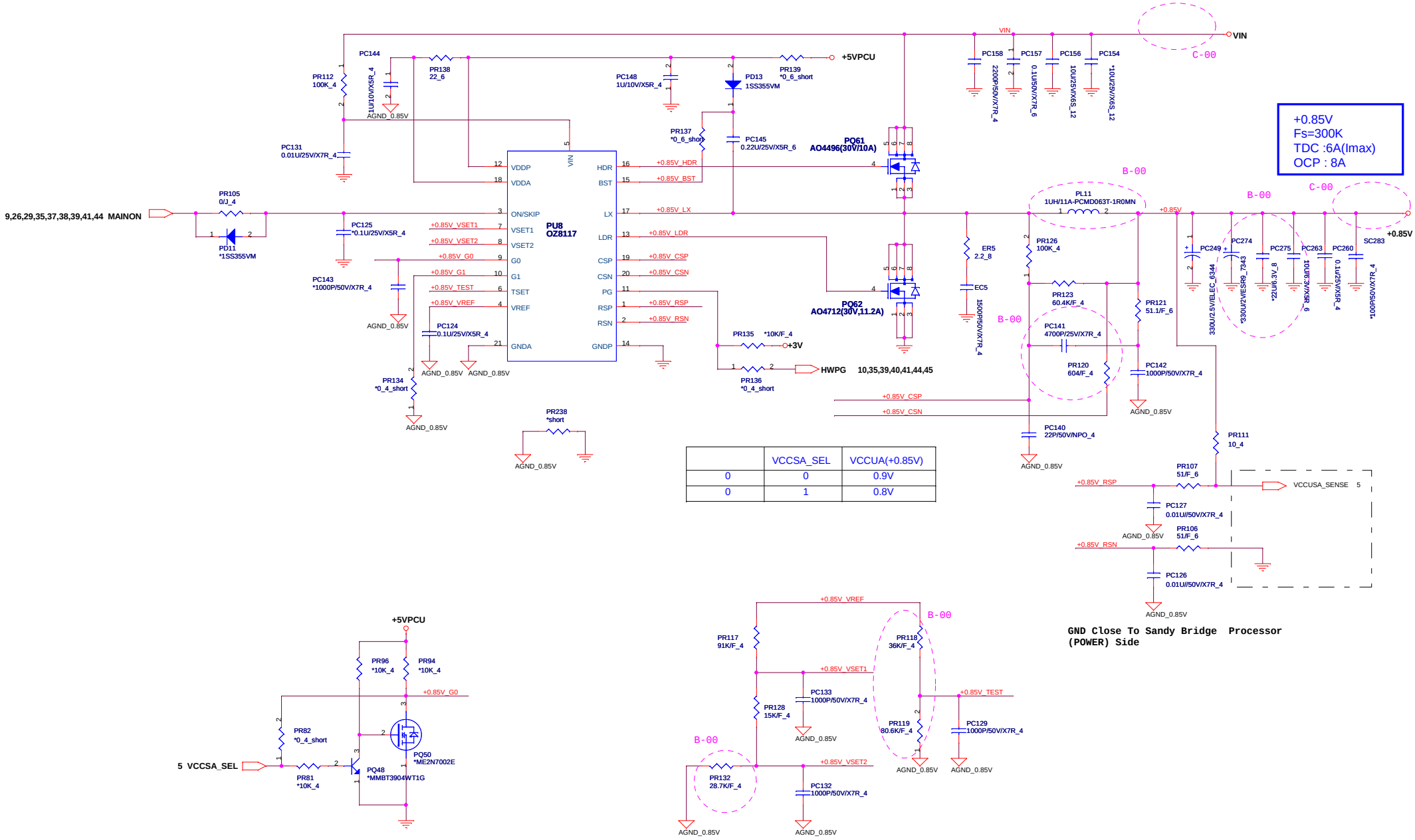
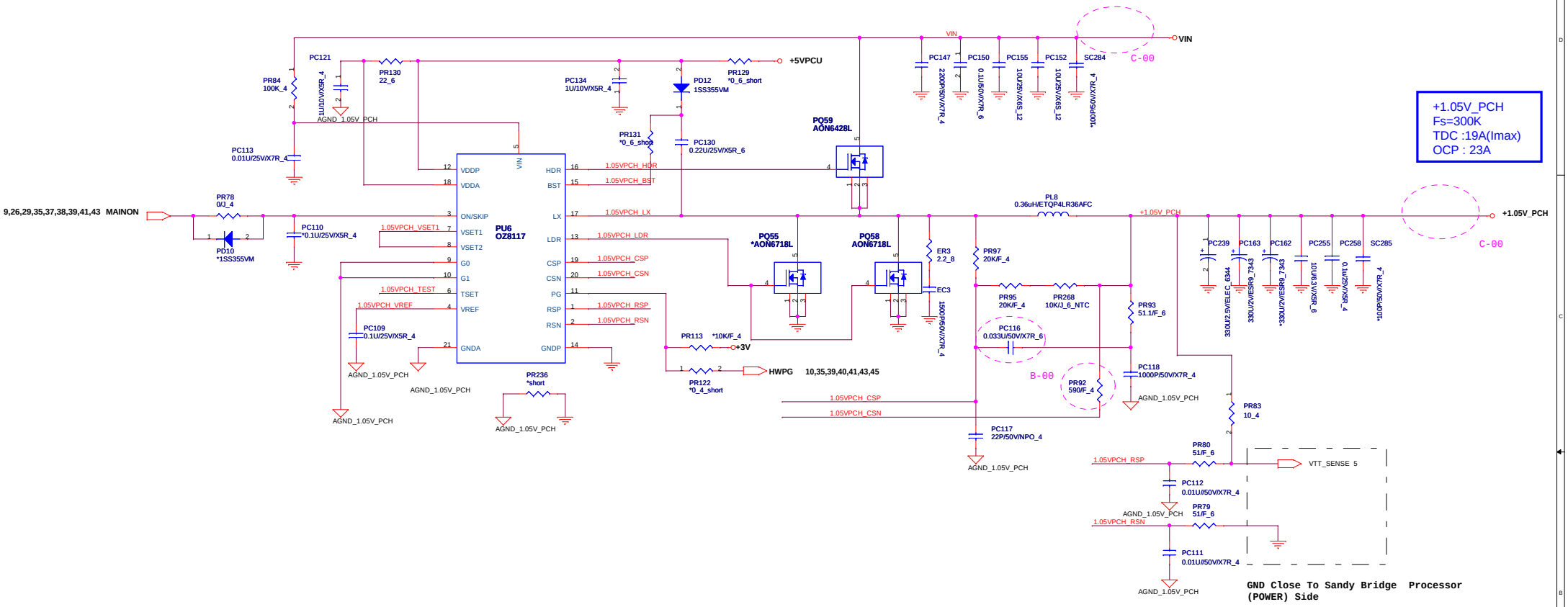
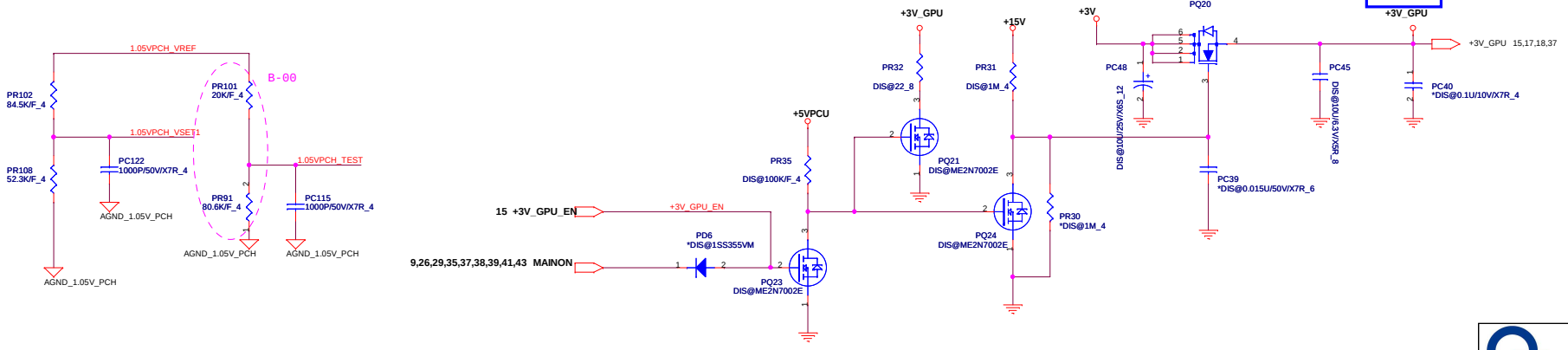


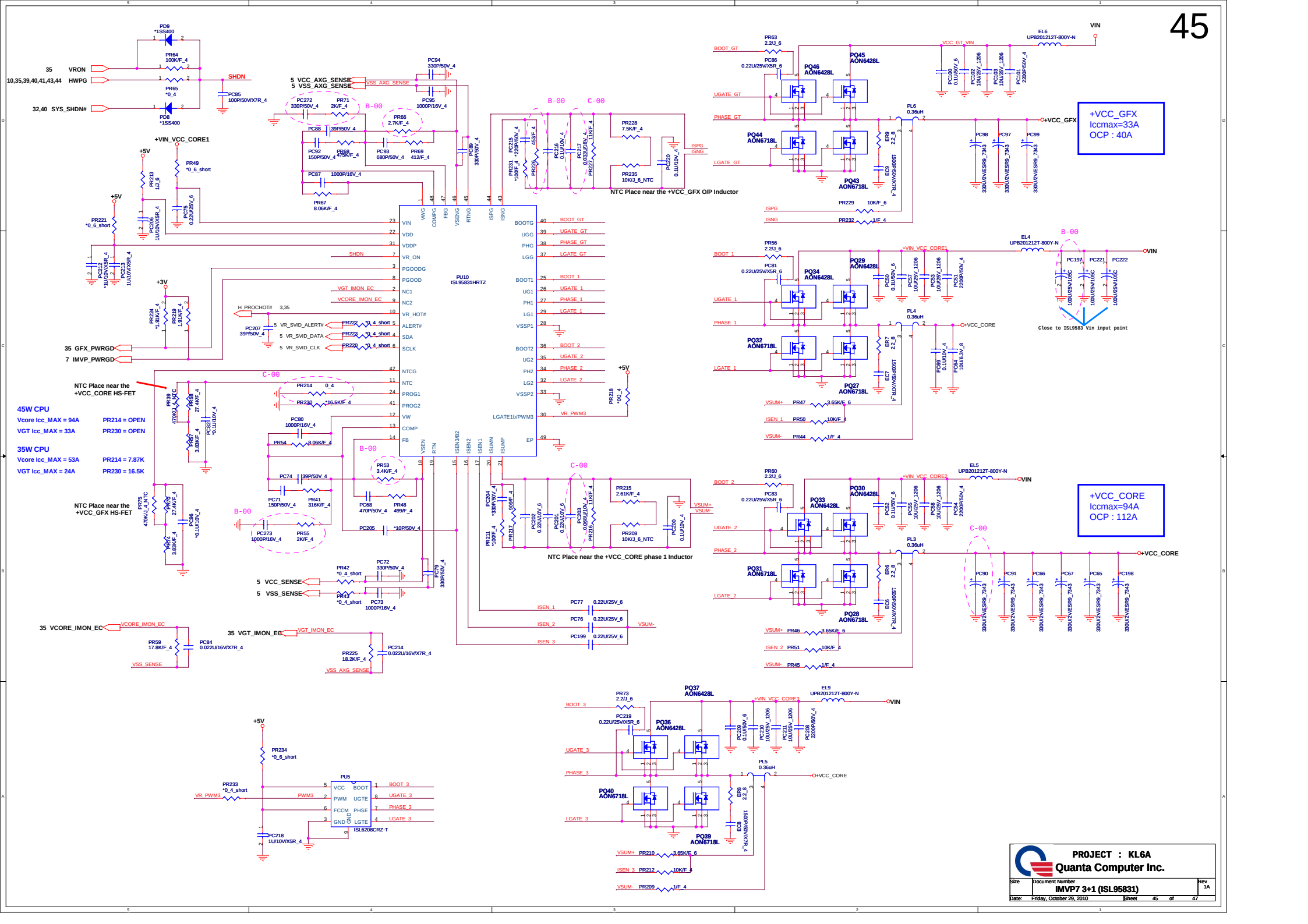
	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

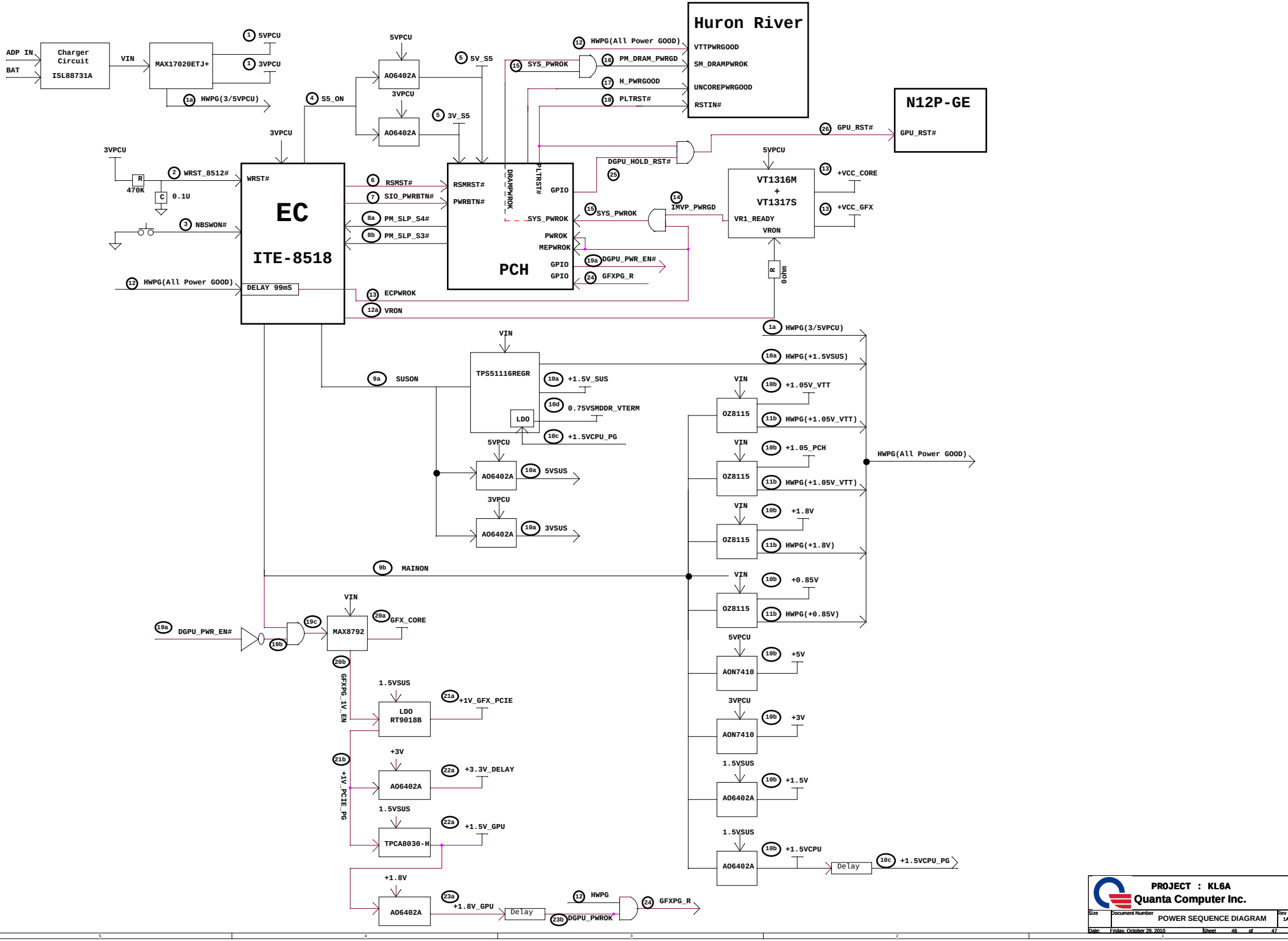
PROJECT :	KL6A
Quanta Computer Inc.	
Size	Document Number: +0.85V (OZ8117) — Rev 1A
Date: Friday, October 29, 2010	Sheet 43 of 47





PROJECT : KL6A		
Quanta Computer Inc.		
Size	Document Number: +1.05_PCH (OZ8115)	Rev: 1A
Date: Friday, October 29, 2010	Sheet 44 of 47	


PU10
ISL95831HRTZ
+VCC_GFX
Iccmax=33A
OCP : 40A
+VCC_CORE
Iccmax=94A
OCP : 112A
NTC Place near the +VCC_GFX O/P Inductor
NTC Place near the +VCC_CORE phase 1 Inductor
NTC Place near the +VCC_CORE HS-FET
NTC Place near the +VCC_GFX HS-FET
45W CPU
Vcore Icc_MAX = 94A
VGT Icc_MAX = 33A
PR214 = OPEN
PR230 = OPEN
35W CPU
Vcore Icc_MAX = 53A
VGT Icc_MAX = 24A
PR214 = 7.87K
PR230 = 16.5K
Close to ISL9583 Vin input point
PROJECT : KL6A
Quanta Computer Inc.
IMVP7 3+1 (ISL95831)
Friday, October 29, 2010


Huron River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
N12P-GE
GPU_RST#
ADP IN
BAT
Charger Circuit
ISL88731A
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
S5_ON
AO6402A
5V_S5
3V_S5
SYS_PWROK
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
HWPG(All Power GOOD)
GPU_RST#
DGPU_HOLD_RST#
EC
ITE-8518
WRST#
WRST_8512#
R 470K
C 0.1U
NBSWON#
RSMST#
SIO_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
DELAY 99mS
ECPWROK
VRON
PCH
RSMRST#
PWRBTN#
DRAMPWROK
PLTRST#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_PWR_EN#
GFXPG_R
IMVP_PWRGD
VT1316M + VT1317S
VR1_READY
VRON
+VCC_CORE
+VCC_GFX
R 0ohm
HWPG(All Power GOOD)
SUSON
MAINON
TPS51116REGR
LDO
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
5VSUS
3VSUS
OZ8115
+1.05V_VTT
HWPG(+1.05V_VTT)
+1.05_PCH
+1.8V
HWPG(+1.8V)
+0.85V
HWPG(+0.85V)
AON7410
+5V
+3V
+1.5V
+1.5VCPU
Delay
+1.5VCPU_PG
MAX8792
GFX_CORE
DGPU_PWR_EN#
GFXPG_1V_EN
+1V_PCIE_PG
LDO RT9018B
+1V_GFX_PCIE
+3.3V_DELAY
TPCA8030-H
+1.5V_GPU
+1.8V_GPU
DGPU_PWROK
HWPG
GFXPG_R
PROJECT : KL6A
Quanta Computer Inc.
POWER SEQUENCE DIAGRAM
Size
Document Number
Rev 1A
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KL6A / Z470 Huron River Schematic EC Tracking Record A (for SIV --> SIT,C)October 18, 2010

EC #	Page	CMVC #	Description	Date	Part Affected
C-00	1~46		Remove 0ohm resistor	1018	
C-01	9		Remov 27MHz from PCH	1018	
C-02	28,32, 34,36		Add capacitor for ESD/EMI suggestion	1018	

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Size	Document Number	Rev
Custom	EC Tracking Record A	1A

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